Enhancement-mode Polar Sourced Gallium Nitride MOSFET

by

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Abstract

All commercially fabricated Gallium Nitride (GaN) based power transistors to date have been heterojunction field effect transistors (HFET). The major down fall of this design architecture is the inability to produce an inherently true normally-off device. The more traditional metal-oxide-semiconductor field effect transistor (MOSFET) design has the potential for power efficiency and enhancement-mode device operation. GaN has been touted as the next promising semiconductor for use in high frequency and high power applications. Various potential applications range from low frequency switching solid state transformers to inverters beyond 10 GHz frequency. These devices require high current densities, large breakdown voltages and the ability to operate in high temperature environments. Modern HFET technology has higher off-state leakage current caused from the minimum carrier density under the channel being larger than a conventional depleted GaN MOSFET. This behavior is crucial for high power applications as the off-state power consumption has become one of the essential design parameters. To date, the limiting factors of producing a GaN MOSFET are the fabrication issues associated to essential components within the MOSFET architecture; a high quality gate dielectric and a large concentration of electrons along the source and drain.

Over the past decade, gate dielectrics grown on GaN have been extensively studied to obtain low interface defects, low leakage current and high channel mobility. Numerous fabrication methods have been attempted to produce an interface worthy for a device; however, the quality of the dielectrics on GaN have been insufficient to compete against an HFET design. The surface passivation of the semiconductor interface states has been studied and considered one of the most significant fabrication processes in a GaN MOSFET. Through a novel low temperature plasma-enhanced atomic layer deposition (PEALD) pretreatment, we have demonstrated interface traps densities below 10^{11} $cm^{-2}eV^{-1}$, with corresponding dielectric capacitance densities greater than 2 $\mu F/cm^2$ for ZrO_2 and HfO_2 films. For the first time a dielectric on GaN has produced a high capacitance density ($>$ 5x), whilst maintaining a high quality interface which significantly reduced the interface trap density

($<$ 10x). This low temperature deposition technique has the ability to be applied to any current GaN technology for MOS applications.

GaN MOSFETs with a ZrO_2 gate dielectric were fabricated on GaN-on-sapphire templates for the purpose of potential power switching applications. The GaN MOSFET design demonstrated enhancement-mode behavior without the complexity of high temperature fabrication and complex etching. The devices incorporated a unique selective deposition technique of ultra-thin PEALD AlN and ZrO_2 films. This novel fabrication technique was one of the first reported low temperature processed unintentionally doped enhancement-mode GaN MOSFET with a peak current density of 50 $\mu A/mm$, a peak transconductance of 40 $\mu S/mm$, an intrinsic transconductance of 0.73 mS/mm and a channel electron mobility excess of 300 cm^2/Vs. The advantage of the MOSFET architecture was depicted through the engineering capabilities of the threshold voltage of the device.

As power electronic systems desire improved internal power components for next generation circuit designs, the GaN MOSFET has shown great potential over the GaN HFET based on optimized simulations and the demonstration of high quality materials. This work has characterized novel low temperature PEALD gate dielectrics with improved properties on GaN for the potential of improved GaN MOSFET characteristics. Novel ultra-thin PEALD AlN films produced high electron densities along the source and drain regions through low temperature deposition. With the incorporation of these films and conventional commercial fabrication techniques the GaN MOSFET will have a distinct impact on power electronics.

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Preface

I, Kyle M. Bothe, am the principal contributor to all seven chapters in this thesis. In the thesis, Chapter 2 is based on the journal publication no. 4 and the conference publication no. 1 and no. 3. The work published in journal publication no. 1, no. 3 and no. 5 is described in Chapter 4. The basis of Chapter 5 included results published in journal publication no. 6 and conference publication no. 4 and no. 5. Finally, Chapter 6 is based on work included in the U.S. Provisional Patent no. 2 and conference publication no. 6. The work resulting in journal publication no. 2 and no. 7 and U.S. Provisional Patent no. 1 were not a part of the thesis.

Peter A. von Hauff had assisted me with the fabrication and characterization of the high-κ dielectrics MOSCAPS discussed in Chapter 4 section 4.3 and 4.4.

Amir Afshar had provided the deposition of the optimized high-κ rare earth metal oxides mentioned in Chapter 4, Chapter 5 and Chapter 6. Amir also assisted with the post fabricated annealing discussed in Chapter 5 section 5.4.1 and Chapter 6 section 6.3.1.

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Pouyan Motamedi had provided the deposition of the optimized PEALD AlN films mentioned in Chapter 5 and Chapter 6.

Triratna Muneshwar had provided the deposition of the optimized PEALD ZrN films mentioned in Chapter 5.

Alex M. Ma provided assistance with the fabrication of the GaN MOSFETs and the method for low-temperature lift-off of PEALD gate oxides.

Below is the list of published and submitted referred journals and conference papers that are resulted from my Ph.D. work.

Publications

Journal Publications

1. Kyle M. Bothe, Peter A. von Hauff, Amir Afshar, Ali Foroughi-Abari, Kenneth C. Cadien and Douglas W. Barlage, "Capacitance Modeling and Characterization of Planar MOSCAP Devices for Wideband-gap Semiconductors with High-κ Dielectrics", IEEE Transactions on Electron Devices 59(10) 2662-2666 (2012)

2. Alex M. Ma, Manisha Gupta, Fatema Rezwana Chowdhury, Mei Shen, Kyle M. Bothe, Karthik Shankar, Ying Tsui, and Douglas W. Barlage, "Zinc Oxide Thin Film Transistors with Schottky Source Barriers", Solid-State Electronics 76 104-108 (2012)

3. Peter A. von Hauff, Amir Afshar, Ali Foroughi-Abari, Kyle M. Bothe, Kenneth C. Cadien and Douglas W. Barlage, "ZrO_2 on GaN Metal Oxide Semiconductor with Low Hysteresis via Atomic Layer Deposition" Applied Physics Letters 102, 251601 (2013)

4. Kyle M. Bothe and Douglas W. Barlage, "Underlying Design Advantages for GaN MOSFETs Compared with GaN HFETs for Power Applications", Journal of Computational Electronics 13(1) 217-223 (2013)

5. Kyle M. Bothe, Peter A. von Hauff, Amir Afshar, Ali Foroughi-Abari, Kenneth C. Cadien and Douglas W. Barlage, "Electrical Comparison of HfO_2 and ZrO_2 Gate Dielectrics on GaN" IEEE Transaction on Electron Devices 60(12) 4119-4124 (2013)

6. Kevin J. Voon, Kyle M. Bothe, Pouyan Motamedi, Kenneth C. Cadien and Douglas W. Barlage, "Polarization Charge Properties of Low-Temperature Atomic Layer Deposition of AlN on GaN" Journal of Physics D: Applied Physics 47 345104 (2014)

7. Mourad Benlamri, Kyle M. Bothe, Alex M. Ma, Gem Shoute, Amir Afshar, Himani Sharma, Arash Mohammadpour, Manish Gupta, Kenneth C. Cadien, Ying Tsui, Karthik Shankar, and Douglas W. Barlage, "High-Mobility Solution-Processed Zinc Oxide Thin Films on Silicon Nitride" Physics Status Solidi: RRL (8) 871-875 (2014)

U.S Patent Applications

1. Alex M. Ma, Manish Gupta, Kyle M. Bothe, Amir Afshar, Kenneth C. Cadien, Douglas W. Barlage, "Buried Source Schottky Barrier Thin Film Transistor And Method of Manufacture" U.S Provisional Patent Application No.61/913,601

2. Kyle M. Bothe, Alex M. Ma, Kevin J. Voon, Amir Afshar, Triratna Muneshwar, Pouyan Motamedi, Kenneth C. Cadien, Douglas W. Barlage, "Polar Source Gallium Nitride MOSFET Structure and Method of Fabrication" U.S Provisional Patent Application No. 61/967,239

Conference Proceedings

1. Kyle M. Bothe, Mark Johnson, Douglas W. Barlage, "TCAD Modeling and Simulation of a Field Plated GaN MOSFET for High Voltage Applications", CS MANTECH Conference, Palm Springs (2011)

2. Peter A. von Hauff, Kyle M. Bothe, Amir Afshar, Ali Foroughi-Abari, Kenneth C. Cadien and Douglas W. Barlage, "High Mobility (210cm2/Vs), High Capacitance (7.2uF/cm2) ZrO_2 on GaN Metal Oxide Semiconductor" CS MANTECH Conference, Boston (2012)

3. Kyle M. Bothe, Peter A. von Hauff, Amir Afshar, Ali Foroughi-Abari, Kenneth C. Cadien and Douglas W. Barlage, "GaN MOSFET: Projections for High Power High Frequency Applications" International Conference on Simulation in Semiconductor Processes and Devices, Denver (2012)

4. Kevin J. Voon, Kyle M. Bothe, Pouyan Motamedi, Kenneth C. Cadien and Douglas W. Barlage, "Engineered Tunneling Contacts with Low-Temperature Atomic Layer Deposition of AlN on GaN", CS MANTECH Conference, Denver (2014)

5. Kyle M. Bothe, Alex M. Ma, Kevin J. Voon, Amir Afshar, Pouyan Motamedi, Kenneth C. Cadien, Douglas W. Barlage, "Selective Deposition of Low Temperature AlN Ohmic Contacts for GaN Devices" CS MANTECH Conference, Denver (2014)

6. Kyle M. Bothe, Alex M. Ma, Amir Afshar, Pouyan Motamedi, Kenneth C. Cadien, Douglas W. Barlage, "Impact of Post Fabrication Annealing PEALD ZrO_2 for GaN MOSFETs" CS MANTECH Conference, Scottsdale (2015)

In Preparation

1. Kyle M. Bothe, Alex M. Ma, Kevin J. Voon, Amir Afshar, Triratna Muneshwar, Pouyan Motamedi, Kenneth C. Cadien, Douglas W. Barlage, "Reliability of Ultrathin PEALD Nitride Based Films in GaN FETs"

2. Kevin J. Voon, Kyle M. Bothe, Triratna Muneshwar, Kenneth C. Cadien, Douglas W. Barlage, "Polarization Charge Properties of Low-Temperature Atomic Layer Deposition of Semiconductor"

Contents

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Chapter 1

Introduction

1.1 Motivation

The perpetual strive to advance electronic systems has become a repetitive occurrence between improving device characteristics and optimizing the design of the system. A power systems overall electronic performance such as power handling, efficiency, size, and reliability are strongly dependent on the enhancements made to individual semiconductor devices. Many power electronic systems require the transistors to operate under extreme temperatures and large power modes of operation [1]. Until now, silicon (Si) has been the dominating semiconductor substrate in power electronics because of the prior knowledge and processing techniques acquired from complementary-metal-oxide-semiconductor (CMOS) technology. However, current silicon based technology has been unable to maintain next generation specifications due to the physical properties that limit the device performance [2]. This is not due to the design of the silicon transistors; rather, the electrical properties of a narrow band-gap has started to reach its limits in the power electronics industry. Conversely, gallium nitride (GaN) has gained significant interest over many researched semiconductors because of the preferential material properties ideal for a wide range of electronic applications [3], shown in Figure 1.1. The next generation power market for GaN devices has been estimated to be $300 million by 2015 with a growth rate over 30% per year [4]. A conservative growth rate, predicts that GaN based devices should reach approximately 5% of the $40 billion power market by 2020.

Gallium nitride has unique semiconductor properties, such that a combination of band-gap, critical electric field, and electron saturation velocity has the potential to advance the

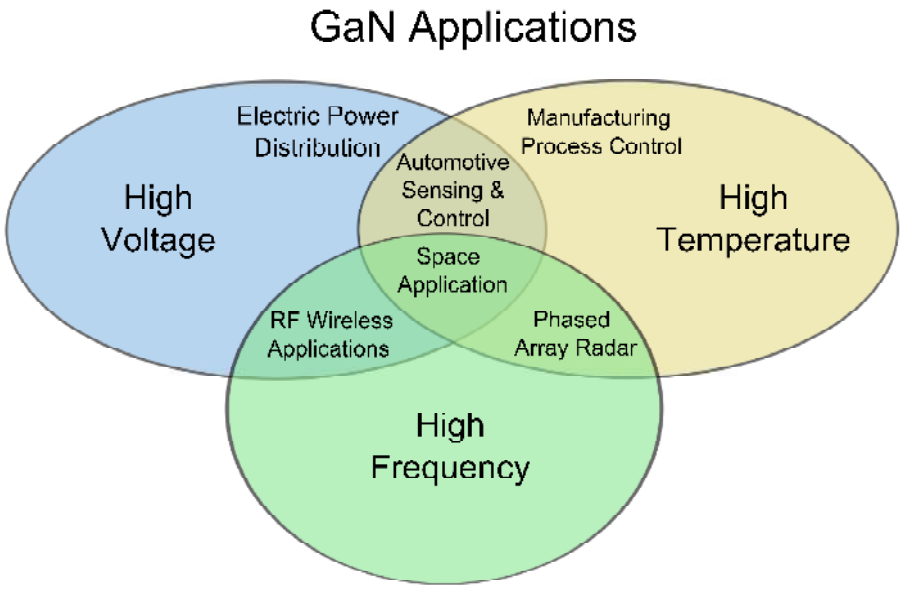


Figure 1.1: The various markets and applications for GaN based devices. The inherent material properties of GaN are starting to replace incumbent technologies unable to advance electronic components required for new applications [3].

transistors switching frequency, operating temperature and blocking voltage (off-state drain voltage) [5]. The material properties of well-known semiconductors, [6–10], commonly used to fabricate microelectronic devices were compiled and tabulated below in Table 1.1. The band-gap, E_G, intrinsic carrier concentration, n_i, dielectric constant, ϵ_r, electron mobility, μ_n, critical electric field, E_C, electron saturation velocity, ν_s, and thermal conductivity, Φ_k were considered the most important electronic properties of semiconductors. The wider band gap semiconductors, GaN and SiC, inherently produce lower intrinsic carrier concentrations which were beneficial for lower junction leakage at higher operating temperatures. Furthermore, wide band gap semiconductors have demonstrated larger critical electric fields compared to small band gap semiconductors such as Si and GaAs. The semiconductors with

Table 1.1: Material Properties of Semiconductors for Electronic Devices

Material	Si	GaAs	4H-SiC	GaN
E_G (eV)	1.12	1.42	2.6	3.37
n_i (cm^{-3})	1.5x10^{10}	2.1x10^{6}	8.2x10^{-9}	1.9x10^{-10}
ϵ_r	11.8	10.8	9.6	9.7
μ_n (cm^2/Vs)	1350	8500	700	900
E_C (MV/cm)	0.3	0.4	3	5
ν_s (cm/s)	1.3x10^{7}	1.2x10^{7}	0.8x10^{7}	3.0x10^{7}
Φ_k (W/cmK)	1.3	0.6	4.5	1.3

higher critical electric fields will achieve the desired power rating within a smaller drift region; i.e. smaller device dimensions. Thus, the specific on-resistance of the devices will be lower for GaN and SiC compared to Si or GaAs [11]. In addition, the reduced switching losses and improved temperature handling will further permit higher switching frequencies and reduce the size and weight of many passive components within the circuit.

1.2 Figure of Merits

The main device characteristics used to evaluate power devices are breakdown voltage, V_{BV}, on-resistance, r_{on}, peak current density, I_{max}, substrate leakage, I_{off}, and material reliability. These electrical characteristics are all dependent on the material properties of the semiconductor. Figure of merits (FOM) were generated from similar systems relative to material properties to compare the potential transistor improvements between various semiconductors with respect to silicon. The relationship between basic material properties of the semiconductor and common device characteristics for transistors were used to create Johnson's figure of merit ($JFOM$), Baligas figure of merit ($BFOM$), Baliga's high frequency figure of merit ($BHFFOM$), Keyes figure of merit ($KFOM$) and the combined figure of merit ($CFOM$).

Johnson's figure of merit was formulated to compare the switching capabilities of semiconductors based on the potential cut-off frequency of an equivalent dimensioned device [12]. The trade off between cut-off frequency, f_T, and maximum applied voltage, V_m, were shown to be equivalent to the critical electric field and saturation velocity of the semiconductor shown in (1.1). The $JFOM$ suggested that wider band gap materials would improve the switching characteristics over narrow band gap semiconductors (i.e Si) which inherently have low critical electric fields.

$$JFOM = V_m f_T = \frac{E_C \nu_s}{2\pi} \tag{1.1}$$

Similarly, Baliga's ($BFOM$) comparison for power devices (1.2) was originated from the relationship of the transistors on-resistance and channel depletion width [13]. By applying the comparison of the breakdown voltage, V_B with respect to the specific on-resistance, r_{on}, of the drift region, the $BFOM$, compared the dielectric constant, carrier mobility and critical electric field of semiconductors for power devices. Like the $JFOM$, the $BFOM$ strongly suggested wide band gap materials were required to improve and advance the device characteristics over silicon based power devices. The evaluation of semiconductors for high frequency and high power applications (1.3) known as Baliga's high frequency figure of merit ($BHFFOM$) was created from the material properties which effected the on-resistance,

r_{on}, and input capacitance, C_{in}, of the device [11]. The on-resistance was dependent on the critical electric field, mobility and dielectric constant and the input capacitance was based on the semiconductors dielectric constant and depletion width. Again, this comparison suggested that wide band gap materials were capable of withstanding large electric fields, while maintaining larger channel mobilities will be successful.

$$BFOM = \frac{V_B^2}{r_{on}} = \epsilon_r \mu_n E_C^3 \tag{1.2}$$

$$BHFFOM = \frac{1}{r_{on} C_{in}} = \mu_n E_C^2 \tag{1.3}$$

Devices that operate in high temperature applications are most effected by the degradation of carrier mobility and background doping concentration [14–16]. These effects were known to reduce the on-off ratio of the device, through reduced current density and increased leakage current. To account for thermal degradation of various semiconductors, the Keyes figure of merit ($KFOM$) for thermal management in integrated circuits, (1.4), was dictated by the thermal conductivity, saturation velocity and dielectric constant of the material. This figure of merit was originally used to compare the impact of high density circuitry in Si-based CMOS rather than high temperature environments in high power electronic applications. However, the results with respect to the materials of interest for thermal management were still applicable.

Lastly, the combined figure of merit ($CFOM$) evaluated the substrate quality for the potential in high temperature, high power and high frequency applications [17]. The $CFOM$ (1.5) was created through the combination of $BHFFOM$ and $KFOM$. A semiconductor with the capability of high frequency and high power applications must also have the potential to manage self heating from the device switching. For example, if a device operated at 300^oC the intrinsic substrate background doping for a narrow band-gap (Si) and a wide band-gap (GaN) are 6x10^{14} cm^{-3} and 1x10^3 cm^{-3} respectively. The small band gap material depletion width would significantly shrink due to the increased background doping leading to a higher leakage current.

$$KFOM = \frac{\Phi_k \nu_s}{\epsilon_r} \tag{1.4}$$

$$CFOM = \Phi_k \epsilon_r \mu_n \nu_s E_C^2 \tag{1.5}$$

The previously discussed figure of merits were tabulated and normalize to silicon in Table 1.2. Based on the physical properties of the semiconductors, GaN has the potential for a broad range of power applications compared to the other materials discussed. In addition,

Table 1.2: Figure of Merits based on Material Properties for Power Electronic Devices

Material	Si	GaAs	4H-SiC	GaN
$JFOM$	1	2	38	1479
$BFOM$	1	16	531	1206
$BHFFOM$	1	11	64	87
$CFOM$	1	11	33	164
$KFOM$	1	0.3	2.5	4.3
Overall	1	10^3	10^8	10^{11}

silicon carbide was also ranked well for the potential use in power devices. However, many fundamental issues of the material limited the advancement of this semiconductor over GaN for power devices. The most detrimental properties were the crystal orientation, mobility and band gap defects [18, 19]. In addition, the total consideration of all the figures of merits strongly suggested that GaN has the best possibility for next generation high power, high frequency and high temperature applications portrayed in Figure 1.2. Each material shown was only capable of operating within the triangular region defined by temperature, breakdown voltage and current density. As depicted below, GaN has the largest possible range of device operation for transistor applications compared to Si and GaAs.

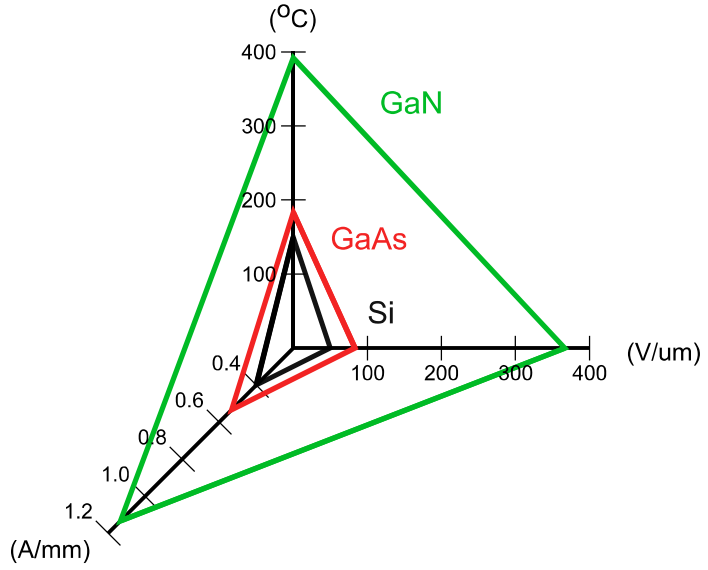


Figure 1.2: A visual comparison of peak operation capabilities for Si, GaAs and GaN based on temperature and power applications. GaN has the ability to replace all silicon power devices based on the ability to operate 200^oC higher and withstand electric fields larger than 300 $V/\mu m$.

1.3 Gallium Nitride Transistors

Over the last decade, GaN based devices have been regularly discussed in literature regarding the device characteristics and reliability for high frequency and high power applications [20–41]. The three main design architecture for GaN field effect transistors, shown in Figure 1.3, are the heterojunction field effect transistor (HFET), metal oxide semiconductor heterojunction field effect transistor (MOS-HFET) and the metal oxide semiconductor field effect transistor (MOSFET). The devices look similar in shape and metalization design; however, the gate film stacks along the channel are significantly different for each transistor. The HFET and MOS-HFET both have a 2-dimension electron gas (2DEG) formed along the AlGaN/GaN or AlN/GaN polarized interface [42]. The major difference is the HFET uses a Schottky metal at the gate, whereas the MOS-HFET has a gate dielectric. The Schottky gate has many issues, such as depletion-mode operation and higher gate leakage [43]; however, the HFET is currently capable of producing high current densities for a given gate length. The MOS-HFET has a similar architecture as the HFET, but the gate dielectric has been included to reduce the gate leakage current during operation [43]. Fluorine plasma pretreatments along the GaN channel surface was a common technique to shift the devices turn-on voltage positive. This pretreatment to the GaN adjusted the Fermi level under the channel, requiring a positive gate bias to form the 2DEG channel rather than a negative bias to turn the device off [44]. This has improved the sub-threshold

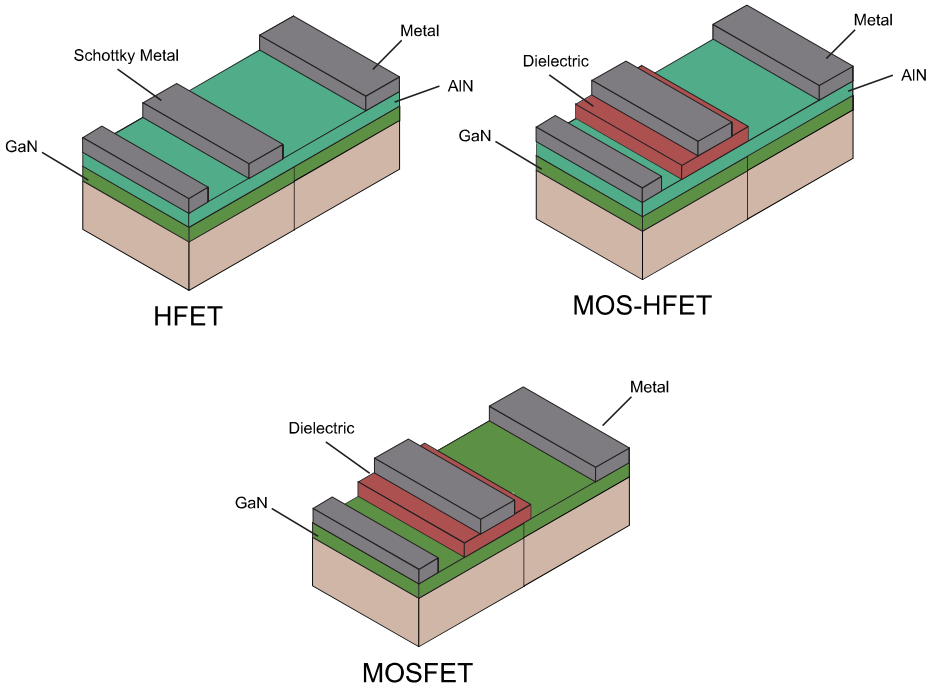


Figure 1.3: The three most common GaN device architectures under investigation for power applications are the (a) HFET, (b) MOS-HFET and (c) MOSFET.

leakage current; however, the performance of the device was degraded due to higher sheet resistance and lower channel mobility due to fluorine induced interface defects [45].

Lastly, the metal oxide semiconductor field effect transistor (MOSFET) architecture only has a dielectric along the gate [14, 15]. By removing the AlN or AlGaN film and the inherent 2DEG along the interface, the turn-on voltage of the device becomes strictly positive. This produced an enhancement-mode transistor where the device was normally-off at zero gate bias. Various gate dielectrics for GaN MOSFETs have been investigated to rectify issues that have reduced the capacitance density and channel field effect mobility. In-turn an improved dielectric and interface along the channel has the potential to advance the peak current density and cutoff frequency of the device.

The majority of the scientific research has been aimed towards improving the off-state of the HFET design for high power applications. The following Table 1.3 highlights significant

Table 1.3: GaN Device Characteristics for Different Design Architectures

	L_G (μm)	L_{GD} (μm)	V_t (+/-)	I_{DS} (mA/mm)	g_m (mS/mm)	V_{BV} (V)	r_{on} ($m\Omega cm^2$)	Ref.
HFET	4	3	-	10	28	30*	6.6	[20]
	1.5	10	-	800	160	594*	3.3	[21]
	2	4	+	130	70	300	30	[22]
	2	125	-	150	50	8300*	186	[23]
	2	7.5	+	200	70	800	2.6	[24]
	1.5	12	+	275	150	1100	6.2	[25]
	1.5	12	+	380	246	1100*	/	[26]
	3	20	-	463	102	1160	7.5	[27]
	0.2	1.3	-	1300	470	/	/	[28]
MOSHFET	2	15	+	300	180	600	9.3	[29]
	2	2	+	326	130	274	0.7	[30]
	2	6	-	770	142	/	/	[31]
	2	6	-	640	147	/	/	[31]
	2	6	-	140	140	/	/	[31]
	1.8	2	-	650	160	130*	0.2	[32]
	0.12	0.2	+	1150	510	8	/	[33]
	1	5	-	0.15	/	/	200	[34]
	0.07	0.04	+	740	250	12	/	[35]
	5	10	+	225	136	385	/	[36]
MOSFET	20	/	+	25	2	/	/	[37]
	4	16	+	/	/	730	34	[38]
	1	16	+	10	4	/	/	[39]
	4	16	+	4	4	/	/	[39]
	0.16	10	+	530	100	565	2	[40]
	0.25	5	+	263	72	39	/	[41]
* indicates $V_{GS} < 0$V when breakdown voltage was measured								

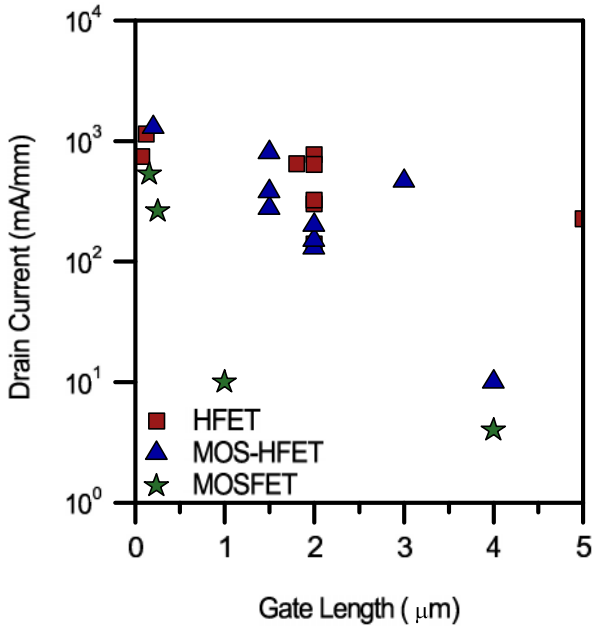


Figure 1.4: Peak current density with respect to gate length for the GaN HFET, MOS-HFET and MOSFET.

devices found in literature with their corresponding device characteristics that are important for high power applications. The main advantage current MOS-HFET technology has over the GaN MOSFET are large current densities for a given gate length, shown in Figure 1.4. However, roughly half of the devices are depletion mode devices, whereas all of the GaN MOSFETs are normally-off enhancement-mode transistors. The MOSFET architectures inherent off-state behavior is advantageous over techniques required to shift the threshold voltage of a depletion mode device [46].

The peak current density trend-line as the gate lengths are reduced vary for the HFET and MOSFET architecture. This is mostly due to the HFET behaving as a junction field effect transistor (JFET) rather than a MOSFET. The major difference of the device is that at zero gate bias the JFET has a 2DEG formed, whereas the MOSFET has a depleted channel with virtually no carriers. The JFET (1.6) and the MOSFET (1.7) have significantly different expressions of the saturation current density where the mobility (μ_n), electron charge (q), device width (W), gate length (L), 2DEG (n_s), source resistance (R_s), voltage L (V_L), capacitance density (C_{ox}), and gate-threshold voltage ($V_{GT} = V_G - V_{th}$) were used.

$$I_{sat_{HFET}} = \frac{\frac{qn_sW\mu_n}{L}V_{GT}}{1 + \frac{qn_sW\mu_n}{L}R_s + \sqrt{1 + 2\frac{qn_sW\mu_n}{L}R_s + \left(\frac{V_{GT}}{V_L}\right)^2}} \tag{1.6}$$

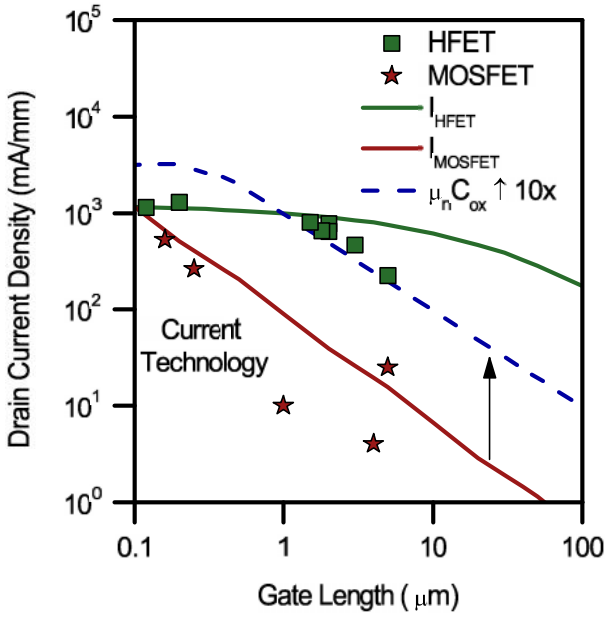


Figure 1.5: HFET and MOSFET peak current density with respect to gate length based on GaN properties. Improving the channel mobility and capacitance density of current GaN MOSFET technology has the potential to surpass HFET characteristics below 2 μm gate lengths.

$$I_{sat_{MOSFET}} = \frac{\mu_n C_{ox} W}{2L} V_{GT}^2 \tag{1.7}$$

The HFET has significantly larger current densities than the MOSFET at large gate lengths ($> 10\ \mu m$) due to the JFET behavior of the device and large number of carriers under the channel. However, current fabricated GaN MOSFET devices have comparable saturation current density as the HFET when the gate lengths are reduced below 100 nm, shown in Figure 1.5. Furthermore, through an improved gate dielectric and interface, the channel mobility and capacitance density of the GaN MOSFET has the potential to improve devices saturation current by minimally 10x. This could be achieved by improving the dielectric capacitance from 0.5 $\mu F/cm^2$ to 2.5 $\mu F/cm^2$ and the saturation channel mobility from 100 cm^2/Vs to 200 cm^2/Vs. This improvement along the channel has the potential to compete with the HFET saturation current density around a gate length of 2 μm. Through improved material properties of the device, the GaN MOSFET has the potential to compete with the GaN HFET for current density for power applications.

In the following chapters, the design advantages of a GaN MOSFET over a GaN HFET were examined along the with characterization of gate dielectrics and the fabrication of an enhancement-mode GaN MOSFET for the potential use in power electronics.

1.4 Synopsis of Thesis

Current GaN based devices have failed to reach the full potential of the material due to the inherent behavior of the HFET design and unsolved material engineering for the MOSFET. Through development at the University of Alberta, ultra-thin films grown with atomic layer deposition on GaN make it possible to fabricate high quality gate oxides. This thesis is focused on the design, fabrication and characterization of a novel enhancement-mode GaN MOSFET for power applications. Through the unique design this device attempts to improve the current density and breakdown characteristics for GaN transistors.

The following chapter examines the potential GaN MOSFETs have as a power transistor through simulations and models to predict the device characteristics given near ideal materials. Through simulation, the MOSFET design was optimized and compared to a modeled fabricated GaN HFET. An in-depth study was conducted to determine the underlying advances the GaN MOSFET has over HFETs for power devices.

Limitations that separate the simulations of GaN MOSFETs from fabricated devices are the non-ideal material complications and techniques used to fabricate the device. Current fabrication methods for GaN HFET technology will not guarantee a fully functional MOSFET due to high temperature degradation of the gate dielectric. Chapter 3 examines the material and technology requirements for an enhancement-mode GaN MOSFET to be fabricated with minimal processing issues. With novel materials and deposition techniques, the GaN MOSFET can be realized for power electronics.

Chapter 4 contains the investigation of low temperature high-κ rare earth metal oxides on GaN for the MOS gate dielectric. The electrical characteristics of ZrO_2 and HfO_2 MOS capacitors on GaN were examined to evaluate the quality of the interface and charge control of the GaN channel. The low temperature plasma enhanced deposition technique was shown to significantly improve the capacitance density, gate leakage, field effect mobility and charge control within the channel over previous attempts of dielectrics shown in literature.

For transistors to operate correctly the source and drain must provide enough carriers to ensure that device saturation occurs. Chapter 5 examines the materials used to create high carrier concentrations in select regions of the device. Novel low temperature AlN and ZrN_x films were fabricated and characterized on GaN templates. Through electrical characterization the contact resistance, 2 dimensional electron gas, sheet resistance, and interface mobility of the films were examined. To ensure device longevity, the reliability of the films proposed were examined for potential device lifetimes.

Chapter 6 covers the fabrication methods used to build the GaN MOSFET through the use of low temperature plasma-enhanced atomic layer deposition of ZrO_2 and AlN. The electrical characterizations of the MOSFET examine the effect of dimensions, thicknesses and materials. The transistors design architecture and device dimensions were examined to

improve the maximum drain voltage during the off-state.

The final chapter summarizes the overall results of the novel GaN MOSFET fabricated and characterized in this report. The novel GaN MOSFET was demonstrated for the potential to provide a novel normally-off transistor and advance power transistor characteristics. This chapter will also provide future insight into work related to this project and potential MOS projects worth pursuing with the novel rare earth metal oxides.

Chapter 2

Device Design and Simulation

2.1 Introduction

The promising material properties that GaN has to offer as a semiconductor device for high power switching applications are only possible when the architectural design of the device has been utilized to its fullest extent. Before the fabrication of a device began, a systematic optimization of dimensions, film thicknesses and design features (Figure 2.1) were required to demonstrate an improved device performance over current technology. Technology computer aided design (TCAD) simulations have allowed semiconductor devices to be optimization with relatively no time or cost when compared to full fabrication processes. Many properties of the MOSFET device, such as electron, current and electric field strength distributions, require simulations to extract these behaviors since these results are not capable of being physically measured. Following the design and optimization of the GaN MOSFET, a detailed comparison to a modeled GaN HFET was investigated to examine the underlying design advantages the GaN MOSFET has over the HFET.

The peak current density and off-state breakdown voltage are two main device characteristics which are important for high voltage and high power applications in GaN FETs [11]. The microelectronic device simulation software, Synopsis Sentaurus TCAD, was used to simultaneously solve the Poisson equation along with the continuity of carriers and the Schrodinger equation in defined regions and domains of the device [47]. The coupled equations were solved with finite element analysis methods which included the material properties such as electron mobility, effective electron mass, dielectric constant, and band gap [48]. To predict the drain-source breakdown voltage of the device, avalanche generation models

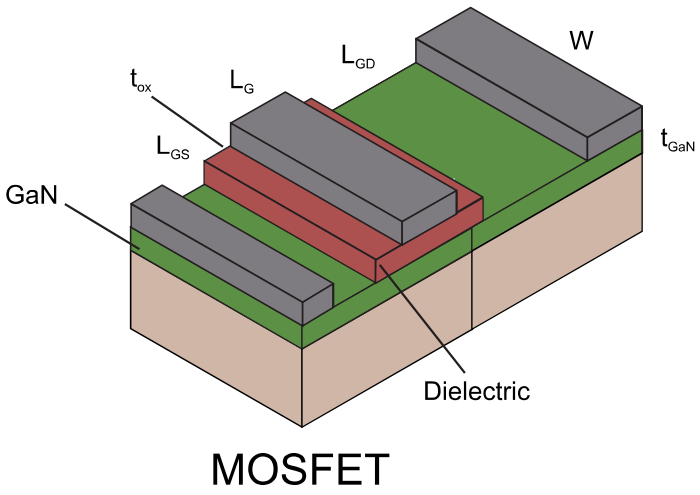


Figure 2.1: The GaN MOSFET design and dimensions to be optimized for improved device characteristics. The device architecture was optimized before field plates were included which were used to improve the breakdown voltage.

were included based on well-known impact ionization parameters for each material [49, 50]. These semiconductor material dependent parameters determine whether a carrier has the required energy to excite another carrier into the conduction band through evaluation of material space charge and mean free path within a collision [51, 52]. The generation of an electron has the potential for a repetitive multiplication process, known as the avalanche effect, to be catastrophic for electronic devices [53, 54]. Through systematic simulations, the architecture of the device was manipulated to minimize the effects of early device breakdown.

2.2 Device Optimization

To optimize the GaN MOSFET multiple lengths and dimensions were considered to produce an enhancement-mode high power transistor. Similar to silicon technology, the substrate thickness was fixed to be less than 1/3 the gate length of the device [55]. Based on the desired gate length and body thickness, the maximum doping concentration of the substrate was determined, as shown in Figure 2.2. The voltage dependent depletion width under the MOS channel (2.1) was obtained from the MOS surface depletion effect described in many solid state device physics textbooks [14, 15, 56]. The gate voltage was defined as the sum of flatband voltage, V_{FB}, the semiconductor band bending surface voltage drop, ϕ_s, and voltage drop across the dielectrics, V_{ox} [56]. The flatband voltage (2.2) was defined by the work function offset between the gate metal and the semiconductor which was dependent on

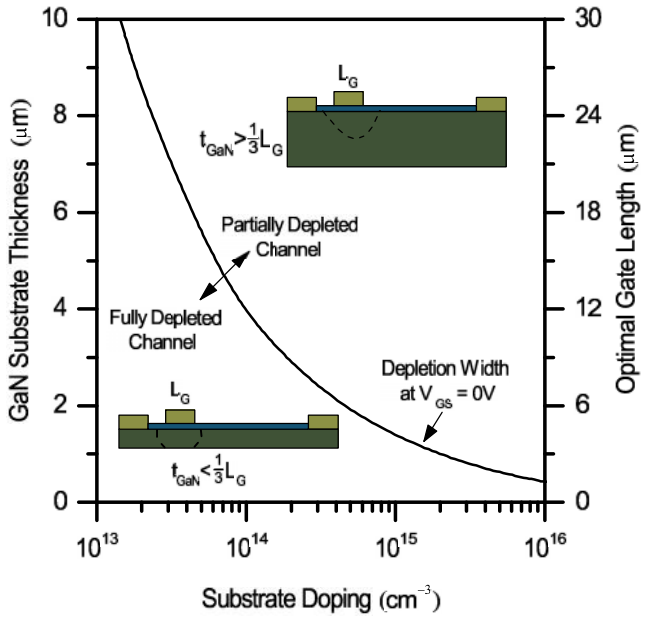


Figure 2.2: The maximum substrate thickness of the GaN and equivalent minimum gate length were determined based on the depletion width determined from the substrate doping concentration. Any combination of thickness and substrate doping that remains below the curve will produce a fully depleted channel.

the gate work function, ψ_m, semiconductor electron affinity, χ_s, doping concentration, N_D, and effective conduction band density of states, N_C [14,15]. The depletion width extracted from (2.1) was used to relate the doping concentration to substrate deletion width at zero gate bias as shown in (2.3).

$$V_G = V_{FB} + \phi_s + V_{ox} = V_{FB} + \frac{qN_D W_{DEP}^2}{2\epsilon_s \epsilon_o} + \frac{qN_D W_{DEP}}{C_{ox}} \tag{2.1}$$

$$V_{FB} = \psi_m - \chi_s - k_B T \ln\left(\frac{N_D}{N_C}\right) \tag{2.2}$$

$$W_{DEP} = \sqrt{\left(\frac{\epsilon_s \epsilon_o}{C_{ox}}\right)^2 + \frac{2\epsilon_s \epsilon_o}{qN_D}\left[\psi_m - \chi_s - k_B T \ln\left(\frac{N_D}{N_C}\right)\right]} - \frac{\epsilon_s \epsilon_o}{C_{ox}} \tag{2.3}$$

To determine the approximate substrate thickness and doping concentration, initial material properties of the gate were assumed to be comparable to Platinum (ψ_m=5.3 eV) [57]. However, if the gate metal had a smaller work function, such as Nickel (ψ_m=4.6 eV) [57],

a lower doping concentration would provide an equivalent depletion width [14]. Furthermore, the dielectric capacitance density was conservatively estimated as an ultra-thin (6 nm) HfO_2 film. Based on an anticipated relative dielectric constant, ϵ_r=24, and dielectric thickness, the corresponding oxide capacitance density (2.4) was initially approximated as $3.5\mu\text{F}/cm^2$. Unlike the gate metal work function, the depletion width was not significantly affected by the dielectric capacitance density for substrates with doping concentrations below $5\text{x}10^{15}cm^{-3}$. The channel of the device was not fully depleted when substrates were thicker than the respective depletion width (above the line in Figure 2.2), which led to larger off-state leakage current. A maximum substrate doping concentration obtained from (2.3) ensured that the depletion width was always larger than the GaN thickness to ensure a fully depleted device.

$$C_{ox} = \frac{\epsilon_r \epsilon_o}{t_{ox}} \tag{2.4}$$

To optimize the gate length, shown in Figure 2.3, the corresponding body thickness and doping concentrations were adjusted to ensure consistent body depletion discussed earlier. The gate-source and gate-drain lengths were simulated with lengths of 1μm and 12μm, respectively for all gate lengths. As predicted through parallel-plate breakdown

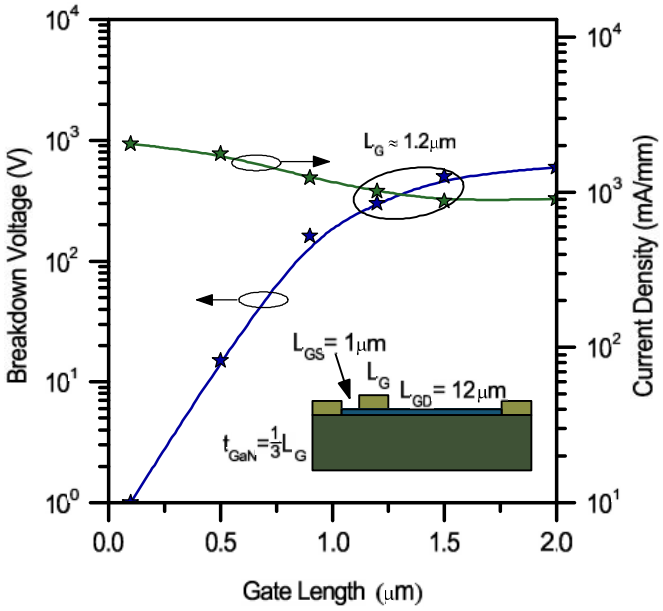


Figure 2.3: The simulated device breakdown voltage and peak current density based on gate length. Through optimization of the gate length the power rating was largest at a gate dimension of 1.2μm.

theory (2.5), a larger fully depleted gate channel was able to assist the overall breakdown voltage of the device [11]. This agreed with simulation; however, the breakdown voltage saturated after a gate length of 1μm. Beyond this gate length the breakdown voltage was more dependent on the gate-drain separation. Conversely, the MOSFET current density described in (2.6) was used to confirm that the current degraded as the gate length was increased [55, 56]. The optimized gate length was determined when the breakdown voltage began to saturate and the current density was not critically degraded. The optimized gate length (1.2μm) was determined when the peak power rating of the device ($P = V_{BV} * I_{DS}$) was maximized based on a large breakdown voltage and peak current density.

$$V_{BV} = \frac{qN_D L_G^2}{2\epsilon_s \epsilon_o} \tag{2.5}$$

$$I_{DS} = \frac{W}{2L_G} C_{ox} \mu_n \left(V_{GS} - V_t\right)^2 \tag{2.6}$$

Following the optimization of the gate length, the gate-source separation length simulations were swept from 100nm to 5μm. Again, the breakdown voltage and current density,

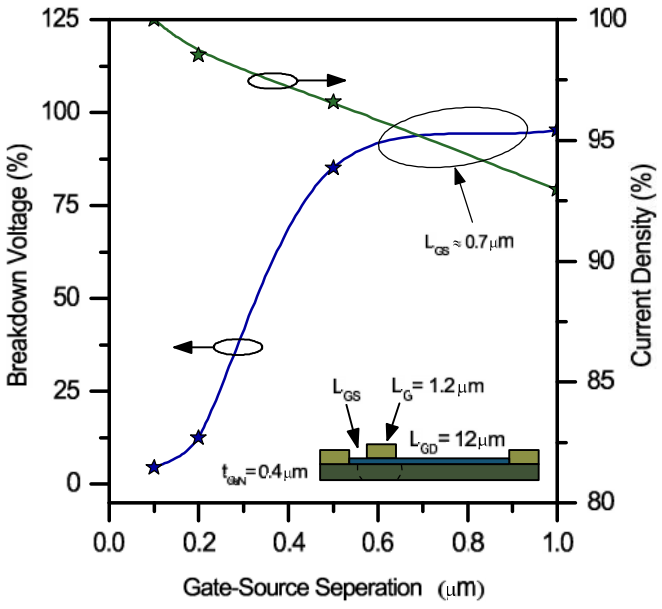


Figure 2.4: The gate-source length dependence on breakdown voltage and current density for the GaN MOSFET. The gate-source separation was optimized to a peak power rating of 0.7μm.

shown in Figure 2.4, were compared to determine the peak overall power rating of the device. As the gate-source length was increased, the breakdown voltage of the device improved until saturation began around 1μm. Conversely, as the breakdown voltage improved the current density decreased which created a peak maximum power rating based on the source-gate length. The peak power rating was maximized when the gate-source length was 0.7μm. Any gate-source separation larger than the optimized length not only reduced the overall power rating but increased the total length of the device. The larger device length decreased the overall number of die for a given template which was undesired for potential fabrication purposes.

Following the optimization of the GaN MOSFET for high power applications, the addition of novel architectures were examined to further improve the device power rating (Figure 2.5). Through the addition of field plates attached to the source and gate with silicon nitride encapsulation, it was shown that the breakdown voltage of the device increased without significant degradation of the transistors device characteristics [58–60]. First the field plate length was optimized by holding the height constant at 3μm. The breakdown voltage was improved as the field plate length was stretched longer; however, the parasitic capacitance become significantly large. The increased gate-source capacitance (C_{GS}) prevents a higher switching capability (2.7) known as the cutoff frequency [61]. The optimal field plate length was determined by selecting the largest breakdown voltage where the parasitic capacitance was minimal. With the breakdown voltage no longer improving beyond 3μm, only the parasitic capacitance increased for any longer field plates. Thus, the optimized source field plate length placed along the drain region was determine to be 1/3 of the gate-drain separation. Similar methods used to determine the length of the field plate were conducted to optimize the height of the source field plate to improve the breakdown voltage of the device during off-state operation. The field plate height was lowered from 10μm to 500nm. At 10μm the

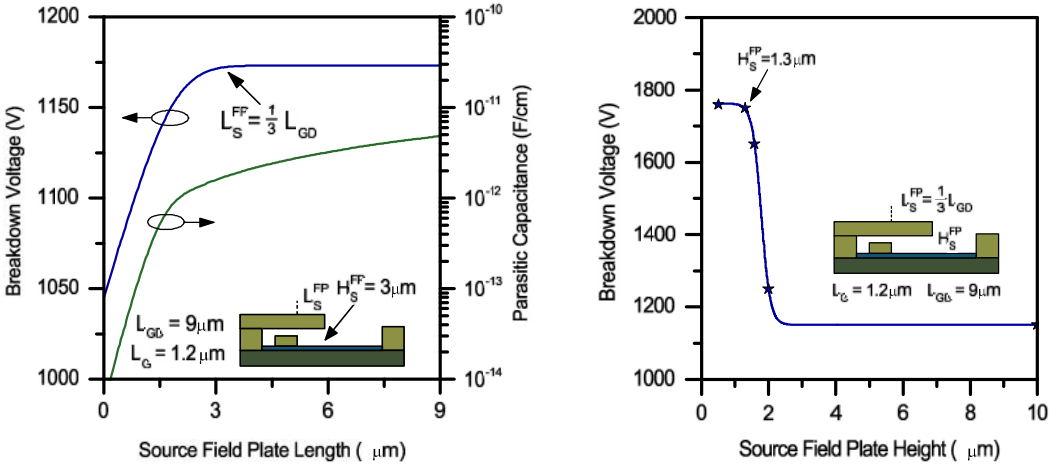


Figure 2.5: Optimization of the source field plate based on length and height.

field plated behaved in a similar manor as the device without a field plate. Below the field plate height of 1.3μm would result in a higher parasitic capacitance without a significant increase in breakdown voltage. Similar methods used to optimize the source field plate were used to optimize the gate field plate. The gate field plate was found to be most effective at a height of 300nm and a length set to 1/2 the overlap of the source field plate (ie 1.5μm for a L_{GD}=9μm). Utilizing both the source and gate to suppress the electric fields along the drain at the ends of the field plates, the breakdown voltage of the device was significantly improved [62].

$$f_T = \frac{g_m}{2\pi C_{GS}} \tag{2.7}$$

The overall breakdown voltage, shown in Figure 2.6, compares different gate-drain (drift region) lengths of the optimized GaN MOSFET with and without field plates to one of the leading field plated GaN HFET. The GaN HFET exceeded the GaN MOSFET without field plates for all drift region lengths. However, as the field plates were included to the MOSFET design, the MOSFET had the capability to withstand the higher electric fields. Through TCAD simulation of the GaN transistors, an in-depth understanding of the device behavior indicated how the MOSFET produced larger breakdown voltages then the HFET.

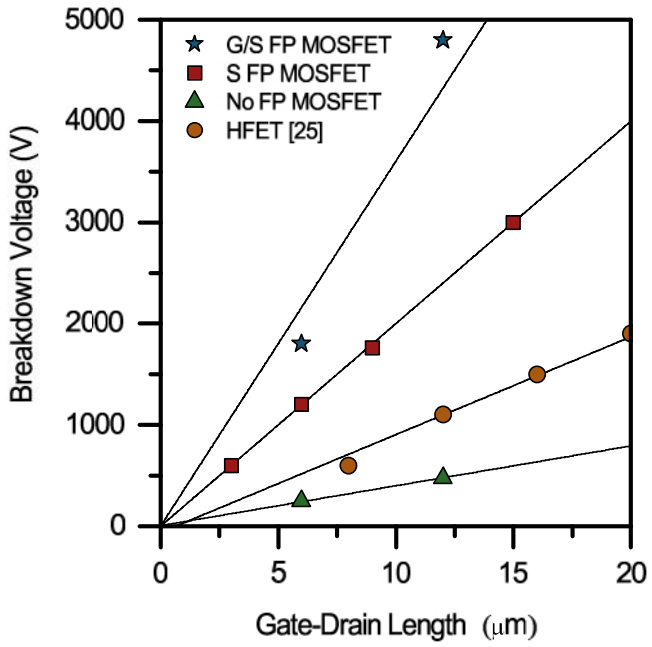


Figure 2.6: The improved breakdown voltage with respect to drift region of the GaN MOSFET with field plates compared to current HFET technology.

2.3 Device Comparison

To understand the underlying design advantages the MOSFET has over the HFET, similar dimensioned GaN devices, shown in Table 2.1, were simulated. Both devices utilized the optimized field plates for both the source and gate. First the conventional device characteristics such as the family of curves (I_{DS}-V_{DS}), transfer curve (I_{DS}-V_{GS}), and the breakdown voltage were examined. Following investigation of the device characteristics, the internal material properties such as mobility, carrier concentration, and electric field distribution produced from the device architecture were examined for important modes of device operation. Simulations were required to extract the electron distribution and electric field due to the inability of a direct electrical measurement of these characteristics.

Table 2.1: Optimized GaN MOSFET and HFET Dimensions

Dimension	GaN MOSFET	GaN HFET
Gate Length (L_G)	1.5 μm	1.5 μm
Drain Length (L_{GD})	8 μm	8 μm
Source Length (L_{GS})	0.7 μm	0.7 μm
Body Thickness (t_{GaN})	0.4 μm	0.4 μm
AlN Thickness (t_{AlN})	N/A	2 nm
Oxide Thickness (t_{ox})	10 nm	3 nm
Source FP Height ($H_{S_{FP}}$)	1.3 μm	1.3 μm
Source FP Length ($L_{S_{FP}}$)	2.6 μm	2.6 μm
Gate FP Height ($H_{G_{FP}}$)	0.2 μm	0.2 μm
Gate FP Length ($L_{G_{FP}}$)	1.3 μm	1.3 μm

The results of the family of curve and transfer curve for both the GaN MOSFET and GaN HFET, shown in Figure 2.7, were simulated for a gate length of 1.5μm. The gate length of the MOSFET was increased from the optimized value to match the simulated GaN HFET which replicated one of the leading fabricated devices [25]. The architectural difference between the MOSFET and HFET designs and the material layers and thicknesses along the gate produced different turn-on voltages. The polarized channel in the GaN HFET required a gate voltage of 0.5V or larger to produce conduction whereas the MOSFET required 1.6 V. However, comparing the drain current with respect to the applied electric field in the channel, it was shown that both devices behave similarly. Regardless of the architecture, the electric field dependent characteristics were nearly identical.

During off-state operation (i.e. $V_{GS} = 0$ V), the drain bias was increased to determine the breakdown voltage of the devices. The current density with respect to voltage was simulated (Figure 2.7c) to determine the leakage current. Once the current density surpassed 80

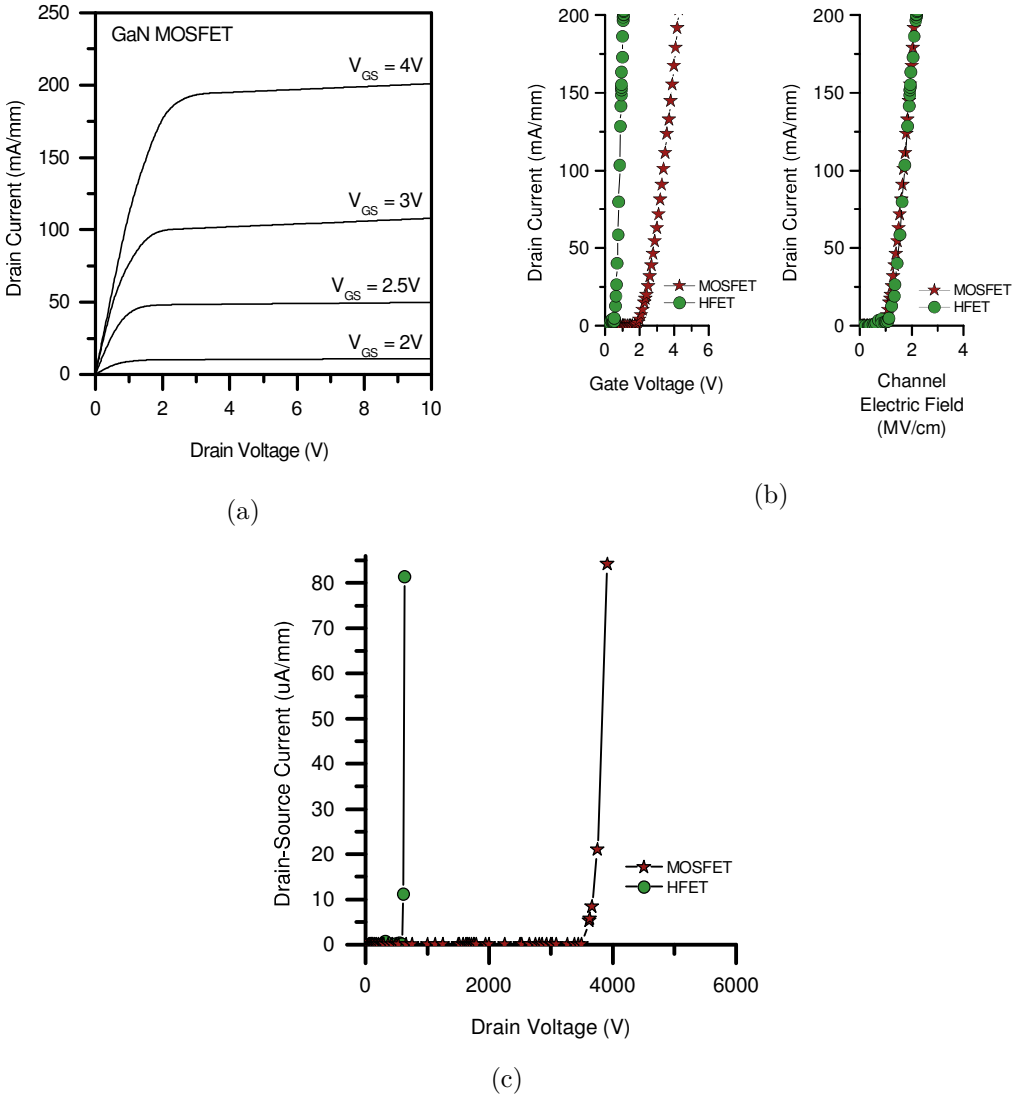


Figure 2.7: (a) Simulated GaN MOSFET family of curves. (b) Voltage and electric field dependence transfer characteristics for the simulate MOSFET and HFET. (c) Breakdown voltage of the simulated HFET (600 V) and MOSFET (3500 V) with similar sized dimensions.

μA/mm, the device was considered to have too large of a leakage current to be considered off. This voltage was considered to be the breakdown voltage of the device. With both devices simulated with equivalent gate and drain lengths, the GaN MOSFET (3500 V) was found to potentially produce a breakdown voltage five times larger than the Gan HFET (600 V). The MOSFET was able to produce similar current densities and withstand larger drain voltages than the HFET. To determine the underlying behavior between devices, the carrier mobility, electron distribution and electric field distribution during on and off states were examined.

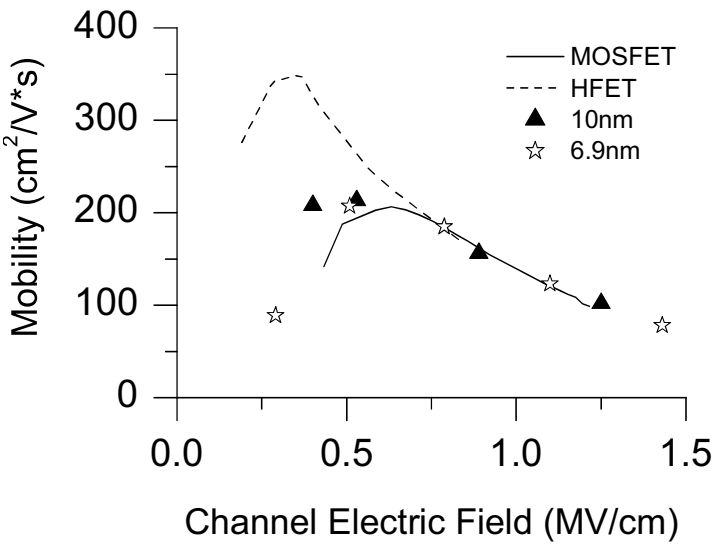


Figure 2.8: The effective electron channel mobility was extracted from the simulated family of curves for the GaN MOSFET and GaN HFET.

From the family of curves simulations the effective field effect mobility of the electrons, shown in Figure 2.8, was extracted by using the conventional experimental technique applied to the simulated data [16]. These results were in agreement with measured MOS mobility results of oxides on GaN [63–65]. The GaN HFET was found to produce a larger peak mobility than the MOSFET during low electric fields. However, the higher electron mobility during sub-threshold operation does not simply imply an improved device. As both devices were operating significantly beyond turn-on voltage, the field effect mobility was equivalent. Thus, the total current was roughly equal during this regime of device operation.

During on-state operation, the MOSFET and HFET produced equivalent field effect mobility and current densities. By including quantized models, which include the quantum mechanical effects, the electron distribution beneath the channel were extracted from the simulations. Classically, the peak carrier distribution was assumed to travel along the interface, whereas the quantum mechanics showed that the dielectric layers cause the peak carriers to travel a few nanometers within the GaN substrate. The carrier transport electron distribution profiles under the channel at the source edge, middle and drain edge were compared between the MOSFET and HFET for different modes of operation, shown in Figure 2.9.

When the gate voltage was below threshold voltage for both devices, the GaN HFET had 10^4 more carriers under the channel than the MOSFET. For a regime where both devices should be off, the MOSFET has a lower number of carriers within the channel compared to the HFET. The HFET was unable to maintain a low concentration due to the 2DEG channel formed from the polarized AlN/GaN interface. During sub-threshold gate biasing, the MOSFET completely depleted the channel; whereas the HFET was not as effective

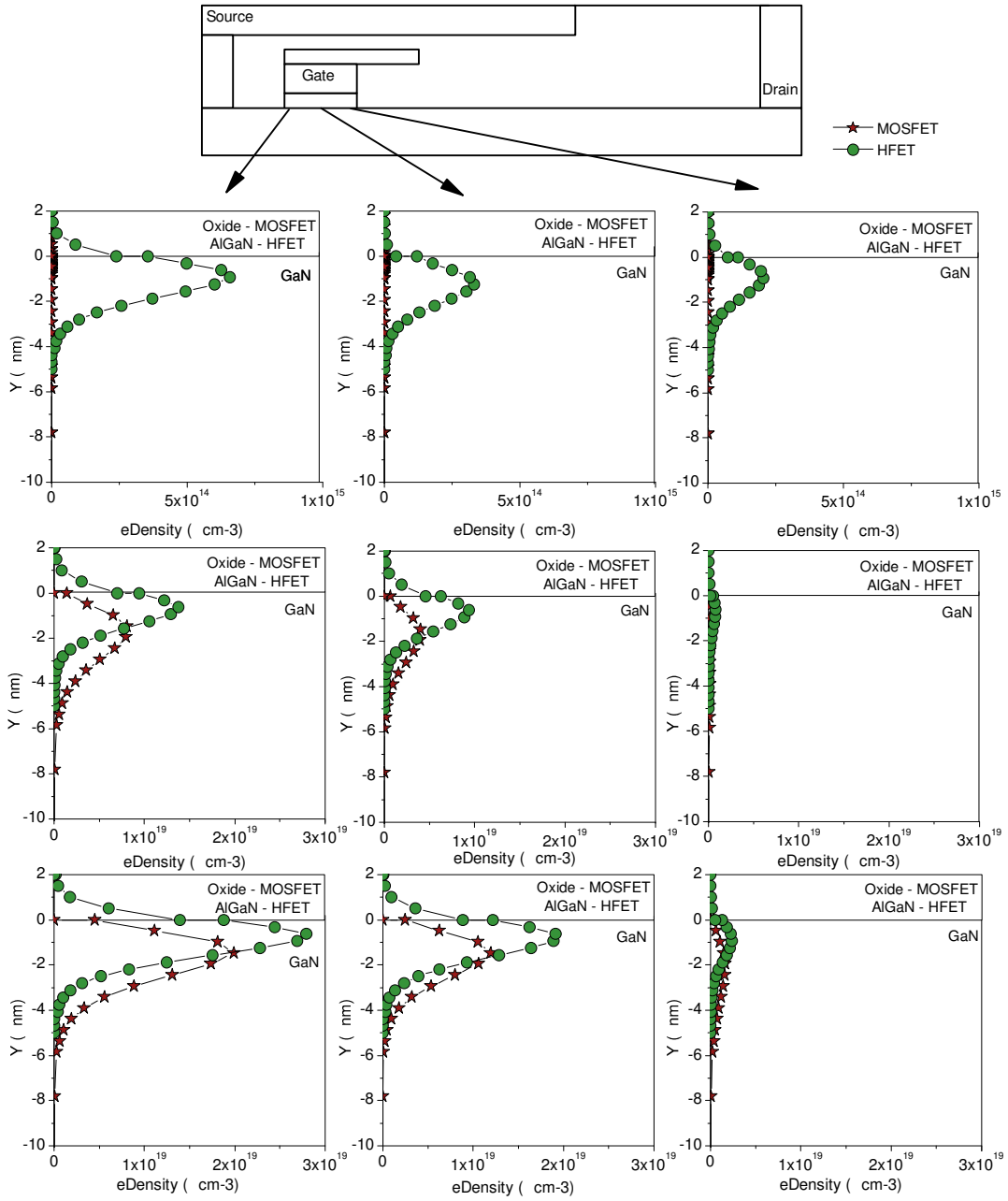


Figure 2.9: The electron density during various modes of operation under the gate of the MOSFET and HFET. The electron distribution in the channel was examined near the source edge, middle and drain edge. (Top) The device is off, i.e. $V_{GS} < V_t$, (Middle) I_{DS} = 40 mA/mm, (Bottom) I_{DS} =175 mA/mm.

which led to more carriers within the gate region.

Electron profiles of both devices during on-state operation (40 mA/mm and 175 mA/mm) are shown in Figure 2.9. These peak electron distributions are highest under the channel on the source side and shrink relatively linearly to the gate-drain edge. These simulations were consistent with the channel pinch off and channel length shortening effects found in enhancement mode devices. Again, this confirmed that the GaN MOSFET and GaN HFET both behaved as enhancement mode devices [14, 15]. For a given equivalent drain current density, both devices exhibit similar carrier densities under the channel even though the HFET produced slightly high peak density. However, the MOSFET channel was found to have a broader carrier distribution which produced an equivalent current density as the HFET.

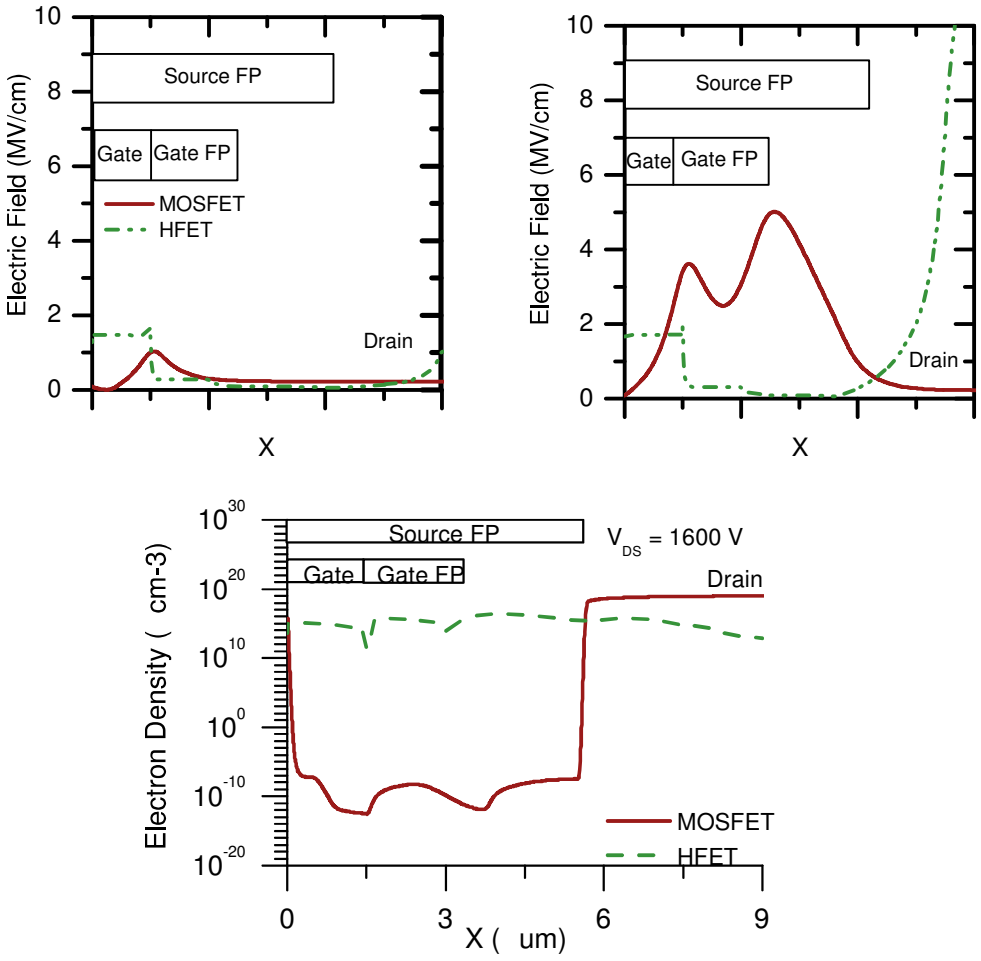


Figure 2.10: The electric field under the gate and drain region when (*Left*) V_{DS}=100V and (*Right*) V_{DS}=1600V. (*Bottom*) The electron density for both devices under the gate and drift region at V_{DS}=1600V. The MOSFET suppressed the electric field and maintain a low concentration of carriers under the gate whereas the HFET was unable to control the channel depletion.

Though both devices produced similar family of curves under low drain bias, the two devices' architectures did not exhibit similar breakdown voltages. The early breakdown effect of the HFET was examined through the simulations that included the electric field and carrier density as the devices before and after breakdown voltage (Figure 2.10). The source and gate field plates were able to manage the electric field along the drain and suppress the breakdown effect. However, once breakdown was initiated, the electric field was too large for the field plate structures to suppress the avalanche effect. Though both devices has the same optimized field plate structures, the GaN MOSFET was able to maintain a breakdown five times larger. The inherent design architecture and physical nature of the GaN HFET caused an earlier breakdown than the GaN MOSFET due to channel control under the gate. The electron density along the device from gate to drain, shown in Figure 2.10, depicts the low carrier concentration in the MOSFET at 1/2 V_{VB}^{MOSFET}; whereas, the HFET was beyond breakdown and was unable to prevent current from conducting during post breakdown at 3 V_{VB}^{HFET}. By using the MOSFET architecture, the channel region truly depletes the entire body correctly, allowing for a complete off-state. Conversely, the HFET did not remove all of the carriers within the channel when the device was off at zero bias. The induced polarization along the interface between the AlN/GaN created a 2DEG making the minimum carrier concentration much higher than the fully depleted GaN MOSFET. Thus, given the similar device dimensions as a GaN HFET, the MOSFET should potentially surpass the breakdown voltage while producing similar on-state characteristics.

2.4 Summary

Through calibrated models and simulations, the GaN MOSFET was optimized for high power applications. With multiple variables required, a systematic process was conducted to determine the lengths and thicknesses of the architecture. Once the optimal device was created, the MOSFET was compared to a simulated HFET. Through simulation, the internal operations of the devices were examined. It was shown that both devices obtained equivalent carrier concentrations within the channel. Though the peak concentration and distribution varied slightly, the overall current density was comparable. During sub-threshold gate voltages, the GaN MOSFET was capable of completely depleting the channel and removing almost all of the electrons. Conversely, the polarization effects in the HFET hindered the ability for the HFET to remove as many carriers as the MOSFET. Thus, the minimum carrier concentration of both devices became an important consideration when attempting to prevent early breakdown effects within power devices. The simulations confirmed the GaN MOSFET was more proficient at maintaining a lower minimum carrier concentration

over the GaN HFET; thus a higher standoff voltage was capable (5x breakdown voltage). Through the use of the MOSFET, GaN has the potential to surpass current GaN based devices for high power applications. The requirement for improved materials within the device has prevented the GaN MOSFET from approaching the maximum potential of the design. The following chapters examine improved fabrication techniques and subsequent material characteristics which were incorporated into the GaN MOSFET.

Chapter 3

Fabrication Techniques

3.1 Introduction

Semiconductor device simulations predicted that the GaN MOSFET was advantageous over the commonly used AlGaN/GaN or AlN/GaN HFET designs for power applications. The inherent properties of a MOSFET provides the potential for higher device switching frequency, improved charge control within the channel, reduced leakage current during off-state operation and higher breakdown voltage. The following diagram, Figure 3.1, depicts some of the most important regions of the device where detrimental fabrication issues are most likely to occur. The following listed device regions are considered the six most important components required to produce an effective enhancement-mode transistor.

1. Gate Dielectric
   - The GaN/dielectric interface must produce an unpinned, low interface trap density and a large peak capacitance to ensure optimal charge control within the channel.

2. Source/Drain Doping
   - The source and drain doped regions must produce a high number of carriers whilst maintaining a large sheet mobility to reduce parasitic resistances.

3. Source/Drain Contacts
   - The metal contacts used for the source and drain must produce a low contact resistance to the GaN.

4. Gate Metal

   - To produce an enhancement-mode device, the gate metal must create a positive turn-on voltage to prevent conduction at zero gate voltage.

5. GaN Substrate

   - The substrate material must have low density of dislocations and defects to ensure a high quality film for high breakdown applications.

6. Device Isolation

   - The device must be unable to conduct current from the source to drain without traveling under the gate.

To fabricate a fully-functioning enhancement-mode GaN MOSFET, novel films and fabrication techniques are required to provide higher quality interfaces. The gate dielectric and metal stack are the most important region of the MOSFET because the dielectric/GaN interface forms the channel and dictates the turn-on voltage and current density of the device. The number of carriers provided along the source and drain are crucial to ensure enough carriers are able to inject into the channel. Furthermore, for a true off-state to occur, the defects within the bulk are desired to be obsolete to prevent uncontrolled conduction around the gate. The ohmic contacts and device isolation are important; however these regions do not dictate whether the transistor is an enhancement-mode or depletion-mode device. To reduce the fabrication cost and processing time, these regions of the device were not optimized.

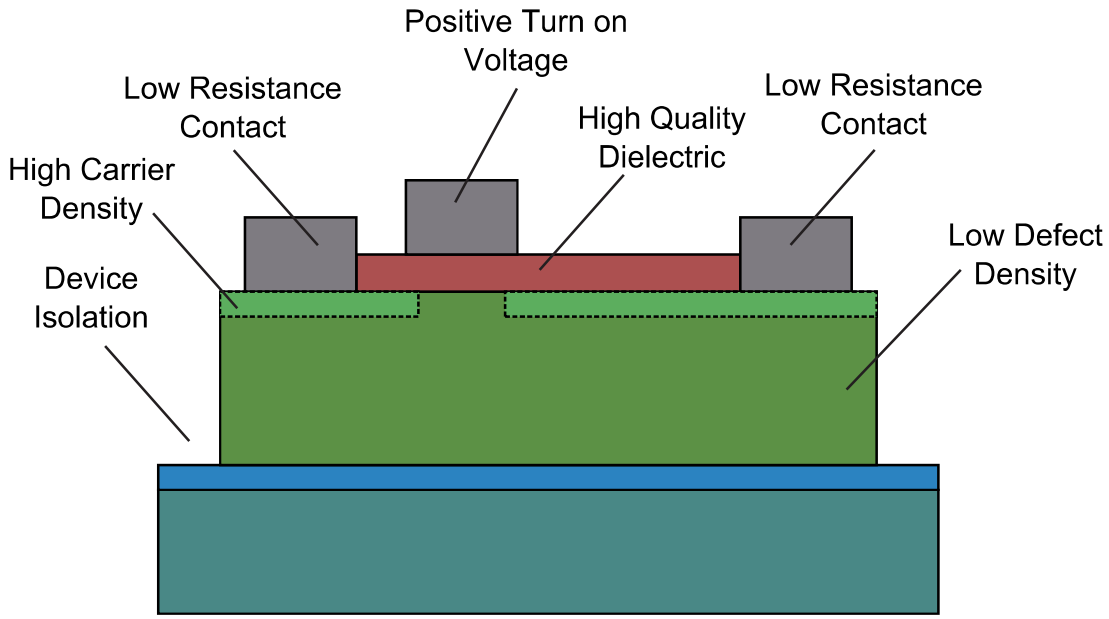


Figure 3.1: Important regions and materials of the GaN MOSFET which require novel fabrication techniques for improved device performance.

3.2 Gate Dielectrics for GaN

High gate leakage is one of the current limitations that prevent GaN based transistors from high power applications. MOSFETs require low leakage current to ensure low noise and improved reliability along the channel. Furthermore, high frequency dispersion is related to the charging of surface states near the drain edge of the gate. These traps do not respond quickly to the high frequency signal thereby affecting the high frequency performance.

To reduce this effect, the interface between the gate dielectric and semiconductor must have a low density of interface states (interface traps) and high capacitance density, shown in Figure 3.2. The improved interface will in turn increase the carrier channel mobility of the device, thus further improving the current density and cut-off frequency of the device. Likewise, a large capacitance density gate dielectric will further improve the charge control under the gate region.

Over the past decade, the attempts to produce a low D_{it} and high C_{ox} on GaN for MOS applications, (Table 3.1), have barely reached the $1\mu F/cm^2$ and $1\text{x}10^{11}eV^{-1}cm^{-2}$ [66–80]. The collection of these films were deposited by chemical vapour deposition (CVD),

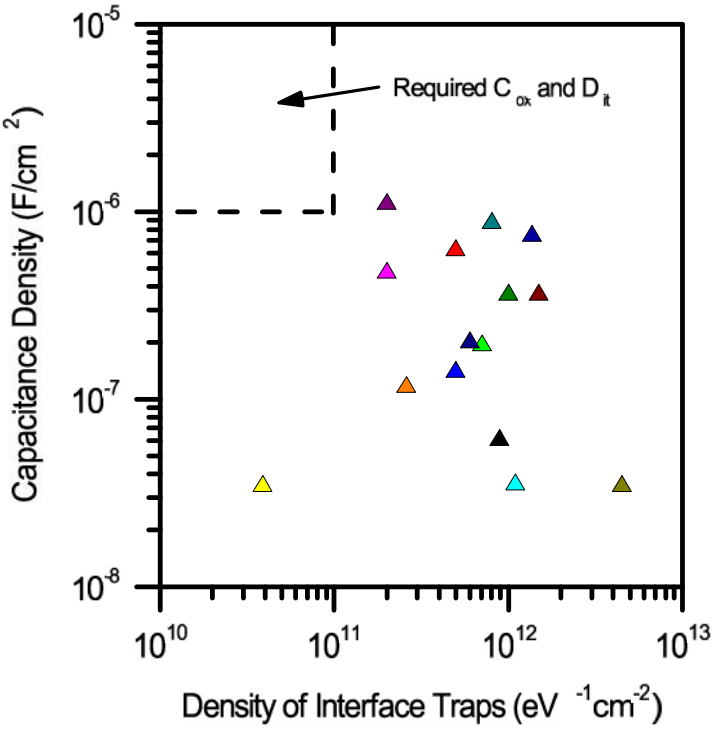


Figure 3.2: Density of interface traps and capacitance density of dielectric on GaN. These techniques were unable to obtain the high charge control and low interface traps required for a MOSFET.

Table 3.1: Gate Dielectrics for GaN Applications

Film Type	Growth Technique	Film Thickness	C_{ox} ($\mu F/cm^2$)	D_{it} ($eV^{-1}cm^{-2}$)	Year
SiO_2	PECVD	56 nm	0.06	$8.9x10^{11}$	1996
TiO_2	MOCVD	19 nm	0.62	$5.0x10^{11}$	1997
Ta_2O_5	RF-Sputter	91 nm	0.05	$4.1x10^{11}$	2000
SiO_2/SiN	JVD	20/20 nm	0.14	$5.0x10^{11}$	2001
Sc_2O_3	MBE	10 nm	0.40	$1.2x10^{12}$	2001
Sc_2O_3	MOCVD	48 nm	0.31	$5.0x10^{11}$	2002
MgO	MBE	80 nm	0.47	$2.0x10^{11}$	2002
SiO_2/Ga_2O_3	Sputter/DO	100/15 nm	0.03	$3.9x10^{10}$	2003
SiO_2	Sputter	100 nm	0.03	$4.5x10^{12}$	2003
Al_2O_3	ALD	16 nm	0.20	$6.0x10^{12}$	2005
HfO_2	ALD	9 nm	1.10	$2.0x10^{11}$	2007
HfO_2	MOCVD	13 nm	0.36	$1.5x10^{12}$	2007
ZrO_2	MOCVD	13 nm	0.36	$1.0x10^{12}$	2007
Ta_2O_5	ALD	6 nm	0.87	$8.0x10^{11}$	2011
HfO_2	ALD	6 nm	0.74	$1.4x10^{12}$	2011

plasma-enhance CVD (PECVD), metal-organic chemical vapour deposition (MOCVD), jet vapour depostion (JVD), molecular beam epitaxy (MBE), dry oxidation (DO) and atomic layer deposition (ALD) with various surface pretreatments. One of the most promising pretreatments for GaN has been a low temperature oxygen-plasma in conjunction with PEALD [65, 81].

3.3 Source/Drain Carriers

Supplying carriers to the channel of a MOSFET is crucial for high current densities when the device is operating at the maximum gate voltage. If the source and drain regions of the device do not have sufficient number of carriers the device will lack conduction and gate control, typically observed in the transfer characteristics of the device. Conventional MOSFET devices use ion implantation to define the channel, source and drain regions of the device. Through heavily doping the source and drain regions the assumption is that the channel has an ample amount of carriers.

One of the major issues with doping GaN is the large activation energy ($\sim$ 150 meV) required for the p-type dopant magnesium (Mg) compared to ($\sim$ 20 meV) for the n-type dopant silicon. The large activation energy produces a large temperature variation between 300 K and 500 K operation. The most common technique to produce a dopant within

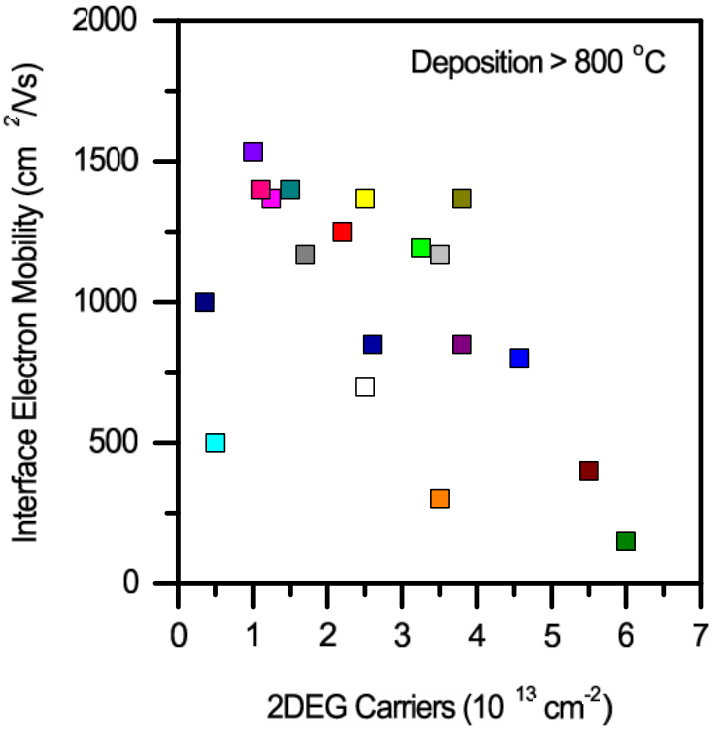


Figure 3.3: Polarized 2DEG carriers and corresponding sheet mobility for AlN and AlGaN films.

semiconductors is ion implantation. The main complications associated with this technique and GaN are high post anneal to activate the dopant. This technique requires a high nitrogen over-pressured environment to ensure that the nitrogen within the semiconductor does not off gas.

Polarized films, AlGaN and AlN, have been used to create high carrier densities with large electron mobilities along the GaN interface. The conventional technique to produce AlN films is with high temperate techniques such as MBE and metal organic vapor phase epitaxy (MOVPE) to produce high carrier densities, shown in Figure 3.3 [82–89]. However, the carrier mobility of the 2DEG is dependent on the quality of the films interface. Novel low temperature PEALD techniques have been investigated to produce high carrier density films on GaN [34, 90]. This allowed for the selective deposition of AlN through PEALD photoresist lift-off. Through the integration of low temperature AlN, novel fabrication techniques will avoid the requirement of etching.

3.4 GaN Metalization

To ensure low loss and high conduction, the contact resistance of the source and drain must be as low as possible. Most commonly used metals on GaN form Schottky barrier contacts, due to the high electron affinity of GaN compared to many metals such a Al, Cr, Ni and Pt. Through empirical studies, the metal stack of Ti/Al/Ni/Au has formed low contact resistance with GaN through high temperature annealing, shown in Figure 3.4. Alternate methods such as tunneling contacts have been studied to reduce the high processing temperatures and cost of complex metal stacks [91]. The incorporation of tunneling contacts significantly reduced the required annealing temperatures for low resistive contacts on GaN [82–84, 92–95]. Through a lower annealing temperature the overall thermal budget of the device can be reduced to prevent gate oxide degradation.

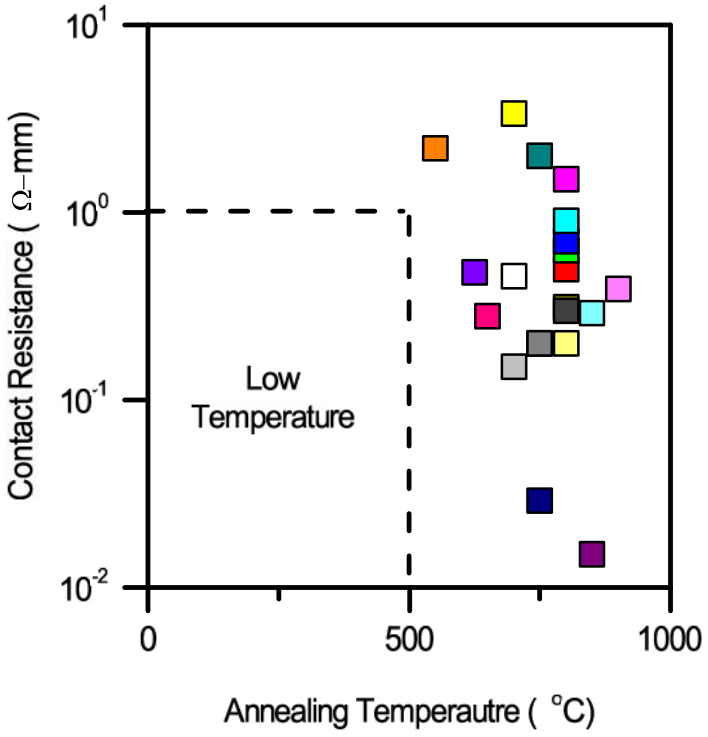


Figure 3.4: Contact resistance with respect to annealing temperatures to produce ohmic contacts on GaN. The current techniques require high annealing temperatures and complex metal stacks.

Table 3.2: Contact Resistance for GaN based Devices

Contact Metal	AlN Film	Temperature (^oC)	Time (sec)	R_c ($\Omega \cdot mm$)
Ti/Al/Ni/Au	3.0 nm	700	120	0.46
	1.7 nm	800	30	0.50
	3.0 nm	800	30	0.63
	4.5 nm	800	30	0.70
	5.5 nm	800	30	0.90
	3.0 nm	700	30	3.38
	3.0 nm	800	30	0.31
	–	750	30	2.00
	1.0 nm	750	30	0.20
Ti/Al/Mo/Au	2.5 nm	600	30	2.50
	2.5 nm	700	30	1.00
	2.5 nm	800	30	0.20
	2.5 nm	850	30	0.25
	2.5 nm	900	30	0.30
	2.5 nm	1000	30	0.50
Ti/Al/Ni/Au	30 nm	550	60	2.20
	30 nm	625	60	0.48
	30 nm	650	60	0.28
	30 nm	700	60	0.15
	30 nm	750	60	0.20
	30 nm	800	60	0.20
	30 nm	850	60	0.29
	30 nm	900	60	0.39
	30 nm	800	60	0.30
Al	–	500	30	1200
Au	–	500	30	600
Ti/Au	–	500	30	120
Ti/Au	–	700	20	12.0
Ti/Al	–	700	20	1.20
Ti/Al	–	900	30	0.01
Ti/Al/Ti/Au	–	700	600	0.12

3.5 GaN Substrates

Semiconductor devices require high purity and low defect density to ensure large yields and stable device design. Over the past 10 years, the quality of GaN-on-sapphire and GaN-on-silicon templates have improved drastically through hydride vapour phase epitaxy (HVPE) developed by Kyma technologies. The major advantage of this method is the higher growth

rates and low material costs compared to MOCVD. Currently, macro defects are nearly minimized $< 5\ cm^{-2}$ while effective doping concentrations of semi-insulating templates are well below $10^{14}\ cm^{-3}$. The effective doping was caused from interstitial defects where electrons within the semiconductor are promoted into the conduction band. As mentioned in Chapter 2, the effective doping of the material strongly dictates the depletion width under the channel of the device. The substrate doping has been reduced enough to allow a Cr gate metal to deplete the entire semiconductor under the channel. This has allowed the potential for improved off-state and enhancement-mode devices.

3.6 Device Isolation

Fabricated semiconductor devices, such as the architecture discussed earlier, require electrical isolation between the contact pads. This prevents the source and drain from unintentionally conducting around the gate when the device should be off. The active area of a silicon based device is conventionally defined by mesa etching or implant isolation. However, fabrication complexities arise in III-V devices with the inability to oxidize regions of the wafer which has been a common technique used in silicon technology.

A simplistic suggestion to isolate the active device was to remove all of the unwanted semiconductor surrounding the device, shown in Figure 3.5. This method removed the possibility of current flowing around the device. However, etching such a durable material has become a minor nuisance. The most common and most efficient method to etch GaN is by a reactive ion beam etching technique with various gas mixtures such as BCl_3 or $CH_4/H_2/Ar/N_2$ [96].

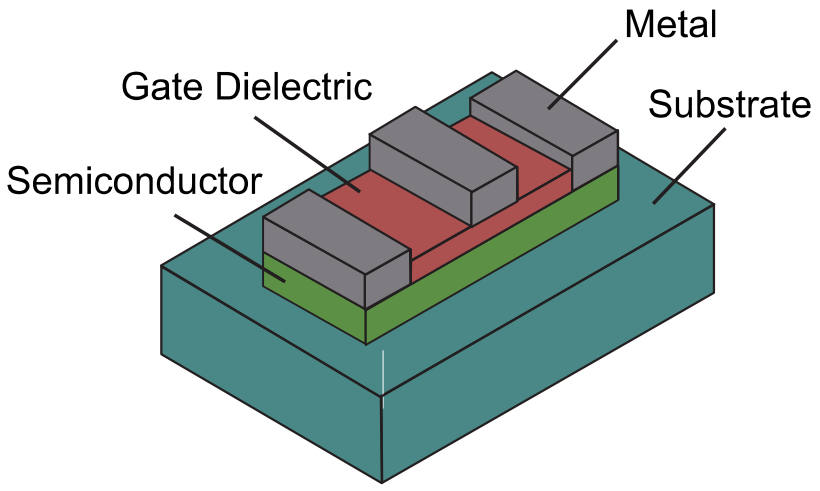


Figure 3.5: Schematic of GaN MOSFET with mesa etching to reduce the leakage current through the unused bulk GaN.

An alternative to etching GaN for isolation is through high energy oxygen ion implantation. This technique has been shown to produce non-conductive GaN [97]. The oxygen isolation is similar to doping a substrate; however, the oxygen implanted GaN template becomes highly resistive. The methods mentioned are effective at device isolation and are common techniques used in GaN HFET technology.

3.7 Summary

To produce a viable enhancement-mode GaN MOSFET, novel fabrication techniques are required to improve the oxide interface, carrier density and contact resistance. Low temperature processing has the potential to minimize complex and expensive processing techniques to reduce the overall cost of the device. With the incorporation of novel low temperature selective deposition lift-off methods the ultra-thin films will not require complex etching. Furthermore, the reduced chemical processing defects and surface states will be minimized to maintain the improved MOS channel and material interfaces. The following chapters will characterize low temperature deposited films which improved various regions of the GaN MOSFET. These improvements suggested that an enhancement-mode GaN MOSFET has the potential to advance power electronic applications.

Chapter 4

Gate Dielectric Characterization

4.1 Introduction

Arguably the most fundamental regions of the MOSFET are the surfaces along the channel and the interface behavior between the gate dielectric and the semiconductor. The interaction between these two materials ultimately dictates the quality of the MOS channel and therefore the device mobility and performance. To determine the optimal and compatible gate dielectric for GaN MOS applications, various dielectrics materials were considered. The ability to fabricate a high quality gate dielectric with a compatible dielectric/GaN conduction band offset has the potential to reduce the electron tunneling probability and improve the gate control of the device. A suitable gate dielectric must have a large enough band-gap to align above and below the band-gap of GaN, shown in Figure 4.1. The conduction band offset must be sufficiently large enough (>1eV) to reduce the detrimental effect of a thermally excited electron jumping over the conduction band edge [98,99]. The effective mass of the electron in the gate oxide significantly contributes to the probability of an electron tunneling through the film. It has been shown through the Wentzel-Kramers-Brillouin (WKB) tunneling approximation that larger effective electron masses in the dielectric reduce tunneling leakage [100,101]. The peak capacitance density of the MOS structure strongly depends on the dielectric constant of the gate dielectric. Based on dielectric constant, effective mass and conduction band offset, as shown in Figure 4.1, the best choice of dielectrics to examine are HfO_2 and ZrO_2. Both films were expected to produce large relative dielectric constants, [102], capacitance densities and low effective masses [100, 103, 104].

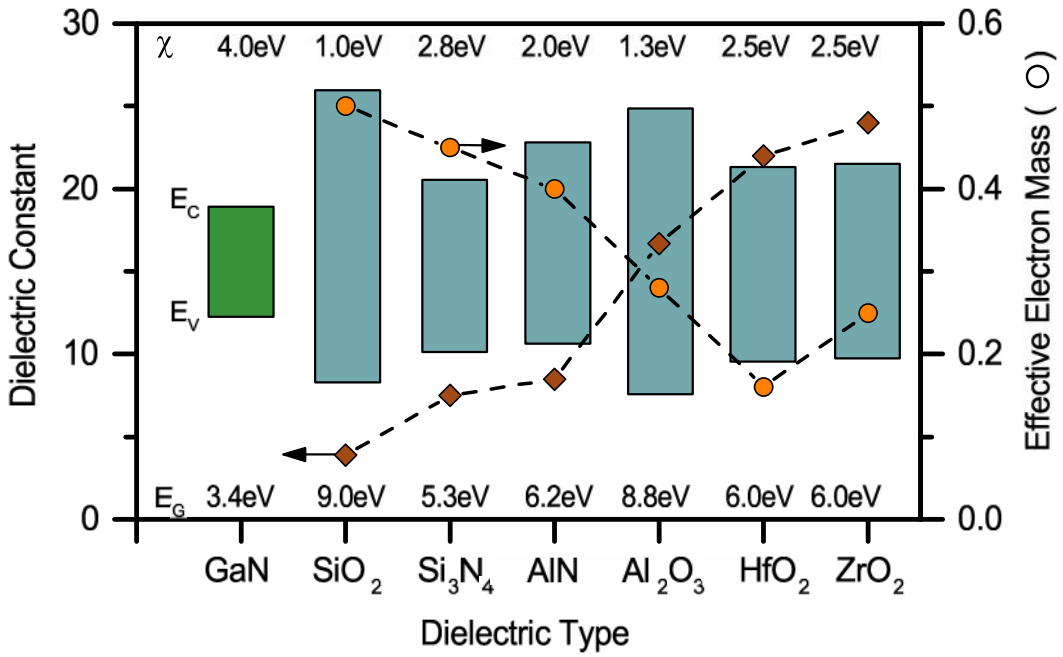


Figure 4.1: Dielectric constant and effective electron mass for potential gate dielectrics for GaN based devices. The corresponding band diagram and conduction band offset can be inferred for each material.

4.2 Dielectric Fabrication

To examine the interface quality between the high-κ film and GaN, planar MOSCAP structures, shown in Figure 4.2, were fabricated on N^+ GaN templates (5x$10^{18} cm^{-3}$). The high-κ dielectrics were grown by an optimized low temperature plasma enhanced atomic layer deposition (PEALD) technique [105]. The growth of the films were deposited in a Kurt J. Lesker chamber whilst maintaining a constant temperature (100^oC) and pressure (1.07 Torr). The alternating precursor gases dose/purge times were respectively oxygen (2.00/2.00s) and either tetrakis(dimethylamido)-zirconium (0.04/5.00s) for a ZrO_2 film or tetrakis(dimethylamido)-hafnium (0.04/5.00s) for a HfO_2 film. The templates were deposited with three different thicknesses (58, 40, 30 cycles) for both dielectric films. The contacts were fabricated with sputtered chromium because of the inherent sticking behavior and compatible work function to produce a positive flatband voltage. An atmospheric post fabrication anneal at 415^oC for 15 minutes was used to activate the gate dielectric.

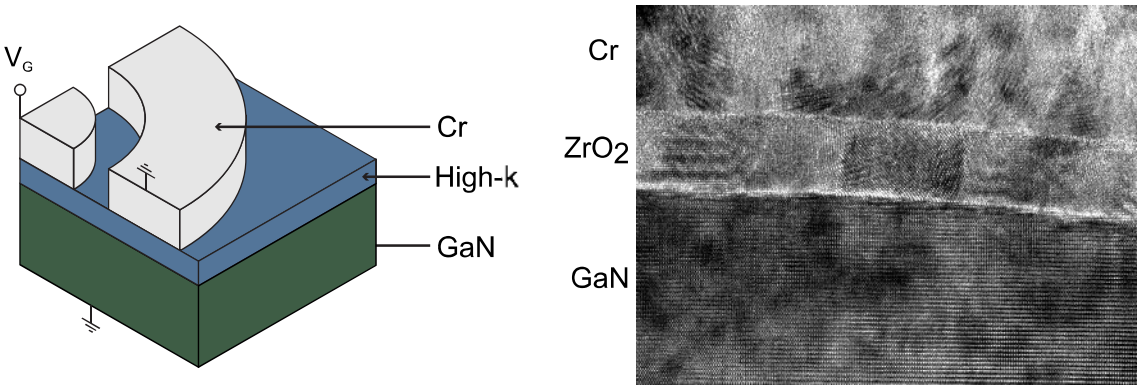


Figure 4.2: (*Left*) Schematic of the MOSCAP used to evaluate the dielectric/GaN interface. (*Right*) TEM image of the high-k dielectric film grown on GaN via PEALD.

4.3 Current-Voltage Measurements

Conventional device measurements were obtained on a Keithley 4200-Semiconductor Characterization System to evaluate the dielectric-semiconductor quality and behavior. The measurements were biased through the inner contact while the outer portion of the MOSCAP was grounded (Figure 4.2). First, current-voltage measurements (Figure 4.3) were obtained for all of the samples. By examining the voltage and film dependent leakage current properties, we were able to characterize the behavior and quality of the films deposited on GaN.

4.3.1 Frenkel-Poole Conduction

The Frenkel-Poole (F-P) leakage conduction model was used to predict the field enhanced thermal emission of carriers from bulk and interface traps [106–108]. By applying an electric field, E, across the dielectric, the barrier height of the traps are reduced by $\zeta\sqrt{E}$. The F-P current density model was described in (4.1), where the elementary charge, q, the Boltzmann constant, k_b, the absolute temperature, T, the dielectric constant, ϵ_r, and oxide parameter ζ, shown in (4.2) were used. The films' material parameters were extracted from capacitance-voltage measurements. The barrier height of the traps or the effective conduction band offset, Φ_{CB}, was obtained by matching the model to experimental results for each film thickness.

$$J = CE \exp\left(\frac{q\Phi_{CB} - \zeta\sqrt{E}}{\xi k_b T}\right) \tag{4.1}$$

$$\zeta = \sqrt{\frac{q^3}{\pi\epsilon_r\epsilon_o}} \tag{4.2}$$

$$\ln\left(\frac{J}{E}\right) = \frac{\zeta}{\xi k_b T}\sqrt{E} + \ln C - \frac{q\Phi_{CB}}{\xi k_b T} \tag{4.3}$$

The linearized plot (4.3) was achieved by plotting (4.1) in the form of $\ln\left(\frac{J}{E}\right)$ vs $\sqrt{E}$. The converted current leakage was used to extract the barrier height between the GaN conduction band and the effective conduction band of the dielectric [109]. The material parameter constant, $C = qN_C\mu_n$ was dependent on the GaN conduction band density of states, N_C, and the electron mobility in the channel, μ_n [107]. By fitting the results in (Figure 4.3) to the F-P model (4.3), we were able to find the conduction band offset for ZrO_2 (1.3+/-10%) and HfO_2 (1.33+/-10%). These values were consistent with expected values found in literature for ZrO_2 (1.4 eV) and HfO_2 (1.5 eV) [110]. Based on the results, the effective barrier height was not significantly degraded from trap assisted tunneling within the film. Thus, the main conduction mechanism which caused the majority of leakage current in the ultra-thin films was quantum mechanical direct tunneling. The HfO_2 films were slightly degraded more than the ZrO_2 films which was the first indication that the ZrO_2 films potentially have lower interface defects than the HfO_2 films.

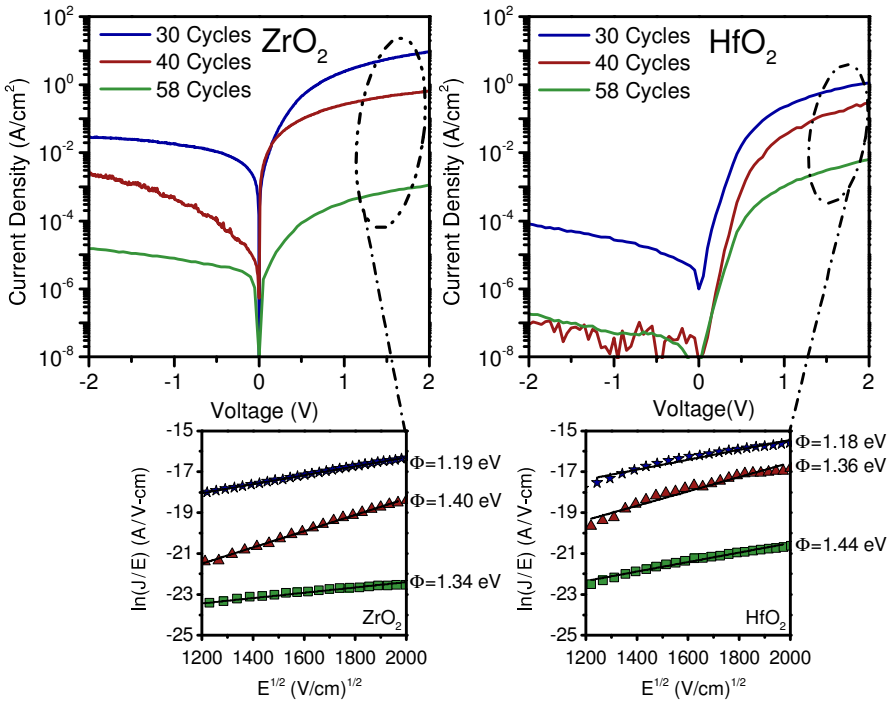


Figure 4.3: Measured current densities with respect to voltage for all film samples. The results were converted into F-P plots to obtain the conduction band offset between the dielectric and GaN.

4.3.2 Quantum Mechanical Tunneling

The MOSCAP direct tunneling current was modeled with quantum mechanical equations that were solved by a novel algorithm known as the transfer matrix method (TMM) [111, 112]. This second-order differential expansion technique has been used to solve similar equations found in microwave waveguides and optoelectronic applications [113]. Through the use of TMM, complex equations can be quickly solved while maintaining high precision [111]. The wave properties of the electrons in the MOS can be described by the second-order steady state differential equation (4.4), known as the time-independent Schrodinger equation.

$$\left[\frac{-\hbar^2}{8\pi^2}\frac{d}{dx}\frac{1}{m^*(x)}\frac{d}{dx}+V(x)\right]\Psi(x)=E\Psi(x) \tag{4.4}$$

$$\Psi(x)=A_j e^{p_j(x)}+B_j e^{-p_j(x)} \tag{4.5}$$

$$p_j(x)=\begin{cases}\Gamma_0\cdot x & j=0\\ \Gamma_j\cdot(x-x_{j-1}) & j>0\end{cases} \tag{4.6}$$

$$\Gamma_j(E)=i\sqrt{\frac{8\pi^2 m_j^*}{\hbar^2}\cdot(E-V_j)} \tag{4.7}$$

The potential profile of the MOS (Figure 4.4) was discretized into N regions, where the potential and effective electron mass at position x_j are V_j and m_j^*, respectively. The corresponding solutions (4.5) to region j were expressed as complex exponential functions along with (4.6) and (4.7). To define the constants A_j and B_j, the boundary conditions found in (4.8) and (4.9) relate the constants found in layer $j+1$ to the constants in layer j. As defined in (4.8), the wave function must remain continuous along x at each interface. Conversely, the derivative boundary condition (4.9) ensured the system maintains stationary eigenstates for boundaries with different effective mass properties [111, 114].

$$\Psi_{j-1}(x_{j-1})=\Psi_j(x_{j-1}) \tag{4.8}$$

$$\frac{1}{m_{j-1}^*}\frac{d}{dx}[\Psi_{j-1}(x_{j-1})]=\frac{1}{m_j^*}\frac{d}{dx}[\Psi_j(x_{j-1})] \tag{4.9}$$

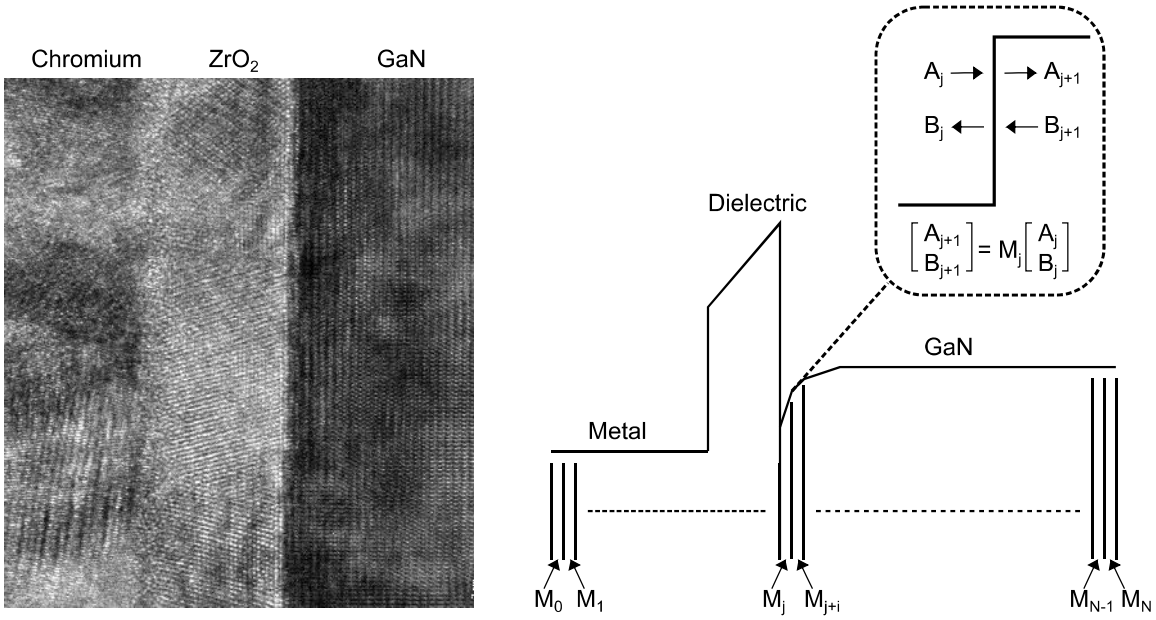


Figure 4.4: (*Left*) Cross section image of the MOSCAP. (*Right*) The illustration of the conduction band used to determine the electron tunneling through the dielectric from the transfer matrix method.

Applying the boundary condition through each layer, we can express any region with constants A and B as shown (4.10) and (4.11). Applying (4.10) to each layer produced a relation of the coefficients (A and B) between the input ($j = 0$) and output layers ($j = N + 1$) (4.12). This in-turn produced the transmission probability (4.13) of the electrons with a given energy level, E. The wavenumber, k, was used to determine the transmission probability and defined as $k_j = \sqrt{2m_j^*(E - V_j)}/\hbar$ in region j.

$$\begin{bmatrix} A_{j+1} \\ B_{j+1} \end{bmatrix} = M_j \begin{bmatrix} A_j \\ B_j \end{bmatrix} \tag{4.10}$$

$$M_j = \frac{1}{2}\begin{bmatrix} \left(1 + \frac{m_{j+1}^* k_j}{m_j^* k_{j+1}}\right) e^{-i(k_{j+1}-k_j)x_j} & \left(1 - \frac{m_{j+1}^* k_j}{m_j^* k_{j+1}}\right) e^{-i(k_{j+1}+k_j)x_j} \\ \left(1 - \frac{m_{j+1}^* k_j}{m_j^* k_{j+1}}\right) e^{i(k_{j+1}+k_j)x_j} & \left(1 + \frac{m_{j+1}^* k_j}{m_j^* k_{j+1}}\right) e^{i(k_{j+1}-k_j)x_j} \end{bmatrix} \tag{4.11}$$

$$\begin{bmatrix} A_j \\ B_j \end{bmatrix} = M \begin{bmatrix} A_0 \\ B_0 \end{bmatrix}$$
$$M = \prod_{l=0}^{j-1} M_l = \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix} \tag{4.12}$$

$$D(E) = \frac{m^*_{N+1}}{m^*_0}\frac{k_0}{k_{N+1}}\left|\frac{1}{M_{22}}\right|^2 \tag{4.13}$$

Once the tunneling probability was determined for the energy level in the GaN channel, the number of carriers (Q) within the channel (obtained from $C-V$) was multiplied to determine the total current density (4.14) for each gate voltage [115]. The extracted dielectric properties were obtained from current and capacitance measurement such as conduction band offset, voltage dependent carrier density and dielectric constant. Subsequently, the effective electron mass of dielectric included in the tunneling probability was the only unknown property to match the model to the current-voltage measurements.

$$J_G = 0.6 * \frac{2q}{(3\pi\hbar q m_{GaN})^{1/3}}\left(\frac{\epsilon_{ox}F_{ox}}{\epsilon_{GaN}}\right)QD(E) \tag{4.14}$$

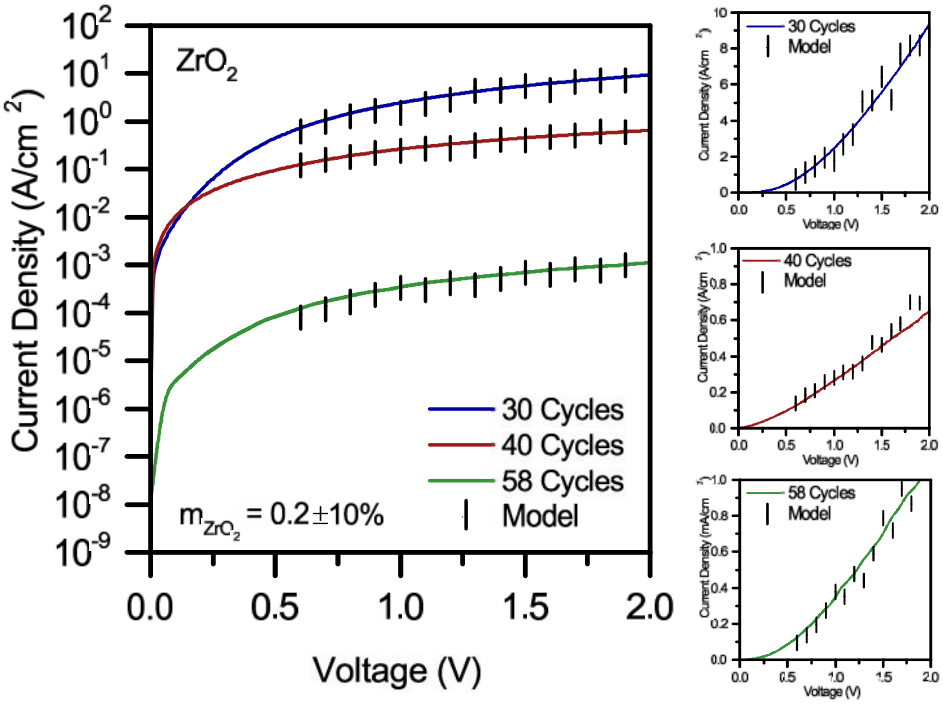


Figure 4.5: The modeled quantum mechanical tunneling current was used to confirm the measured conduction mechanisms and to extract the effective electron mass of the ZrO_2 films. The model (with error bars) was matched to the measured results by creating the band structure for a given voltage and adjusting the effective mass of the dielectric. The effective electron mass of the ZrO_2 films was determined as $m_{ZrO_2} = 0.2$.

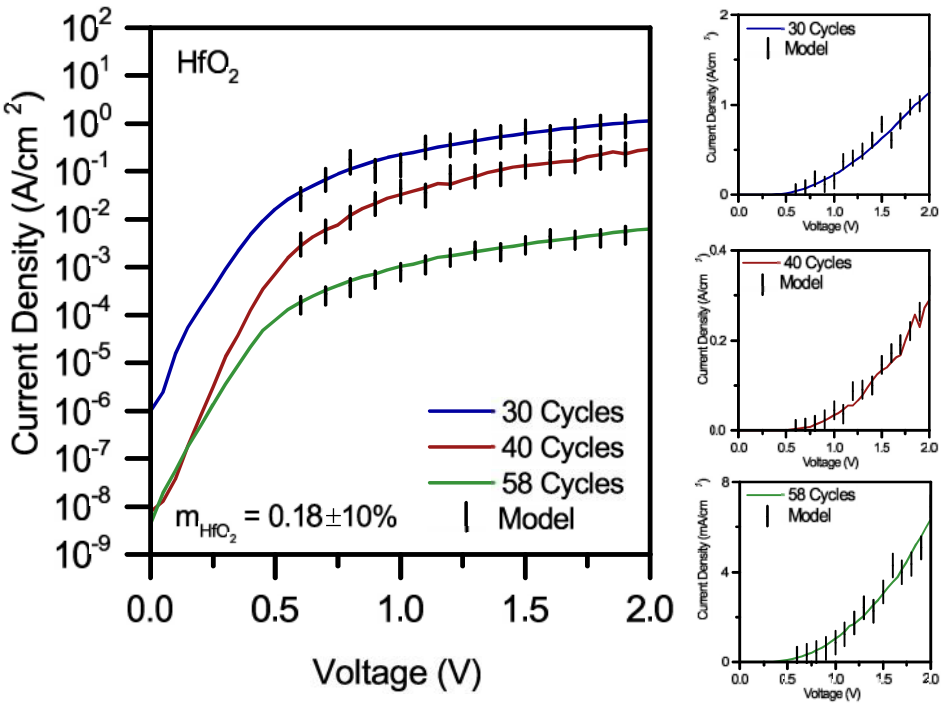


Figure 4.6: The modeled quantum mechanical tunneling current was used to confirm the measured conduction mechanisms and to extract the effective electron mass of the the HfO_2 films. The model (with error bars) was matched to the measured results by creating the band structure for a given voltage and adjusting the effective mass of the dielectric. The effective electron mass of the HfO_2 films was determined as $m_{HfO_2} = 0.18$.

Forward biased current density measurements, shown in Figure 4.5 and Figure 4.6 were obtained for all of the films and compared to the quantum tunneling results. As expected, the thinner films produced larger leakage currents due to the higher tunneling probability through the film. To match the measurements, the effective electron mass was only adjusted and determined as 0.2+/- 10% and 0.18+/-10% for ZrO_2 and HfO_2, respectively. This method confirmed the theoretical calculation of the low effective electron mass of these high-κ films.

4.4 Capacitance-Voltage Measurements

As stated earlier, capacitance measurements were used to obtain some of the dielectric properties that were required for the current density models. To evaluate the ultra-thin films capacitance-frequency measurements, a distributed model was formulated to extract the capacitance density and effective field effect mobility. By describing the MOSCAP as an equivalent lumped circuit model through the use of transmission line theory [63], we were

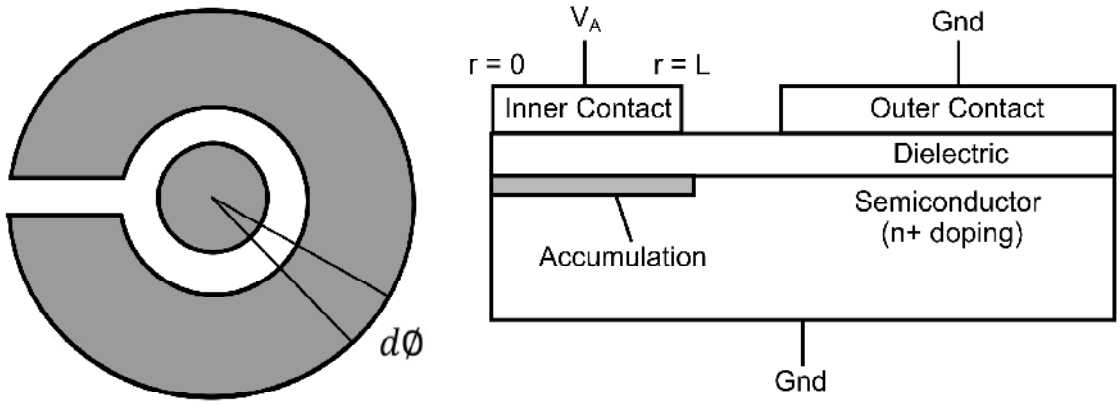


Figure 4.7: (Left) An illustration of the modeled planar MOSCAP. (Right) The radial cross section of the modeled planar MOSCAP.

able to separate the properties of the dielectric and semiconductor. This model described the dielectric and semiconductor accumulation layer of the MOSCAP shown in Figure 4.7. By extracting these characteristics of the device, it was possible to understand the quality of the dielectric-semiconductor interface as well as provide an insight into the gate quality and effective channel mobility for a MOSFET structure.

The equivalent circuit model used to define the MOSCAP behavior, shown in Figure 4.8, were represented as passive electrical components. The characteristic impedance of the lumped circuit was modeled as an accumulation layer represented by the series resistance while the ultra-thin dielectric was represented by a shunt capacitance and conductance. This technique has been commonly used to describe the channel resistance in the semiconductors [116]. However, the impedance, Z_L, which connects the semiconductor under the inner contact to the outer contact, was considered as a resistor that was dependent on the doping concentration of the semiconductor and the distance between contacts.

By using the transmission line lumped circuit model technique, the characteristic impedance Z_0 (4.15) and corresponding propagation delay γ (4.16) are described by using the model parameters R_s, C_p, G_p and the operating frequency ($\omega = 2\pi f$). Through the use of complex algebra identities, the imaginary square root of the propagation delay was described by the real values α and β in terms of the model parameters as show in (4.17) and (4.18) respectively.

$$Z_0 = \sqrt{\frac{R_s}{G_p + j\omega C_p}} \tag{4.15}$$

$$\gamma = \sqrt{R_s(G_p + j\omega C_p)} = \alpha + j\beta \tag{4.16}$$

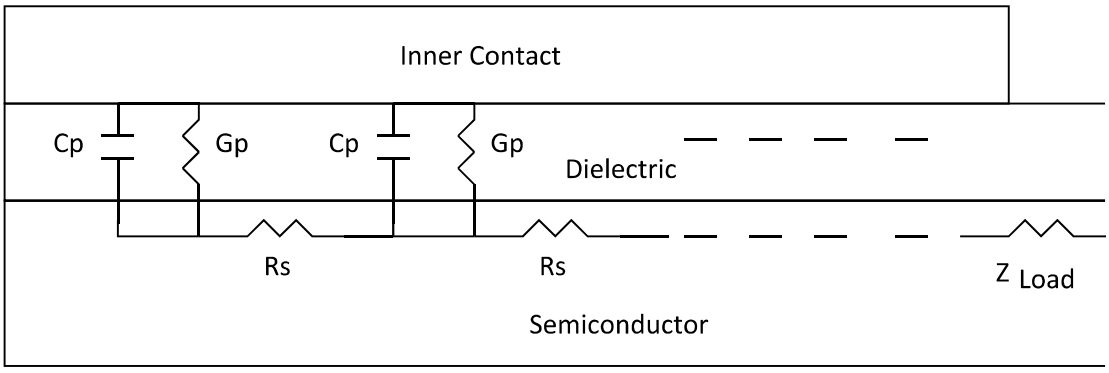


Figure 4.8: Equivalent lumped circuit model under the inner contact for the planar MOSCAP.

$$\alpha = \frac{\sqrt{2}}{2}\sqrt{\sqrt{(R_s G_p)^2 + (\omega C_p R_s)^2} + R_s G_p} \tag{4.17}$$

$$\beta = \frac{\sqrt{2}}{2}\sqrt{\sqrt{(R_s G_p)^2 + (\omega C_p R_s)^2} - R_s G_p} \tag{4.18}$$

An infinitesimals slice of the inner contact was considered as a transmission line with a characteristic impedance of Z_0. The combination of the theory of small reflections (4.19) and tapered transmission line theory (4.20) were used to determine the reflection coefficient of the infinitesimal slice [117]. The tapered line of the inner contact (Figure 4.9) assumed that the characteristic impedance began at the center of the inner contact and varied as a function of distance. The edge of the inner contact was assumed to connect to the load impedance that represented the resistance of the semiconductor and resistance to the outer contact. From triangular tapered line theory stated that the area gradually changes the impedance as a function of radii from the characteristic impedance to the load impedance shown in (4.20).

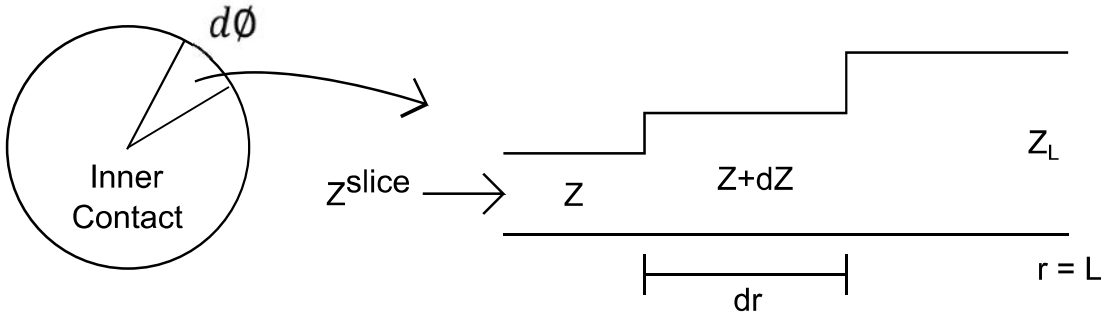


Figure 4.9: A small slice of the inner contact ($\partial\phi$) visually converted into the equivalent triangular tapered transmission line.

$$\Gamma(\omega) = \frac{1}{2}\int_0^L e^{-2\gamma r}\frac{\partial}{\partial r}\ln\left(\frac{Z}{Z_0}\right)dr \tag{4.19}$$

$$Z(r) = \begin{cases} Z_0 e^{2\frac{r}{L}\ln\left(\frac{Z_L}{Z_0}\right)} & 0 \le r \le \frac{L}{2} \\ Z_0 e^{\left(4\frac{r}{L}-2\frac{r^2}{L^2}-1\right)\ln\left(\frac{Z_L}{Z_0}\right)} & \frac{L}{2} \le r \le L \end{cases} \tag{4.20}$$

Through the use of the two equations above, the reflection coefficient of the infinite decimal area with radius L, was explicitly calculated and shown in the equation below (4.21). Once the reflection coefficient of the transmission line was determined, the effective input impedance can be calculated from the characteristic impedance and the ration $(1+\Gamma)/(1-\Gamma)$. The entire input impedance of the inner contact was calculated in (4.22), by taking the integral of the input impedance of the infinitesimal area (Z_{Slice}) with respect of the radial direction ($\partial\phi$). By assuming that the small tapered region was independent about any rotation a simple multiplication of the factor 2π was sufficient.

$$\begin{aligned}\Gamma(\omega) = &\frac{\ln\left(\frac{Z_L}{Z_0}\right)}{2L(\alpha+j\beta)^2}\left[1-e^{-L(\alpha+j\beta)}\left(\alpha L+j\beta L+1\right)\right] \\ &+\frac{\ln\left(\frac{Z_L}{Z_0}\right)}{2L^2(\alpha+j\beta)^2}\left[e^{-2L(\alpha+j\beta)}+e^{-L(\alpha+j\beta)}\left(\alpha L+j\beta L-1\right)\right]\end{aligned} \tag{4.21}$$

$$Z_{in} = 2\pi Z^{slice} = 2\pi Z_0\left(\frac{1+\Gamma}{1-\Gamma}\right) \tag{4.22}$$

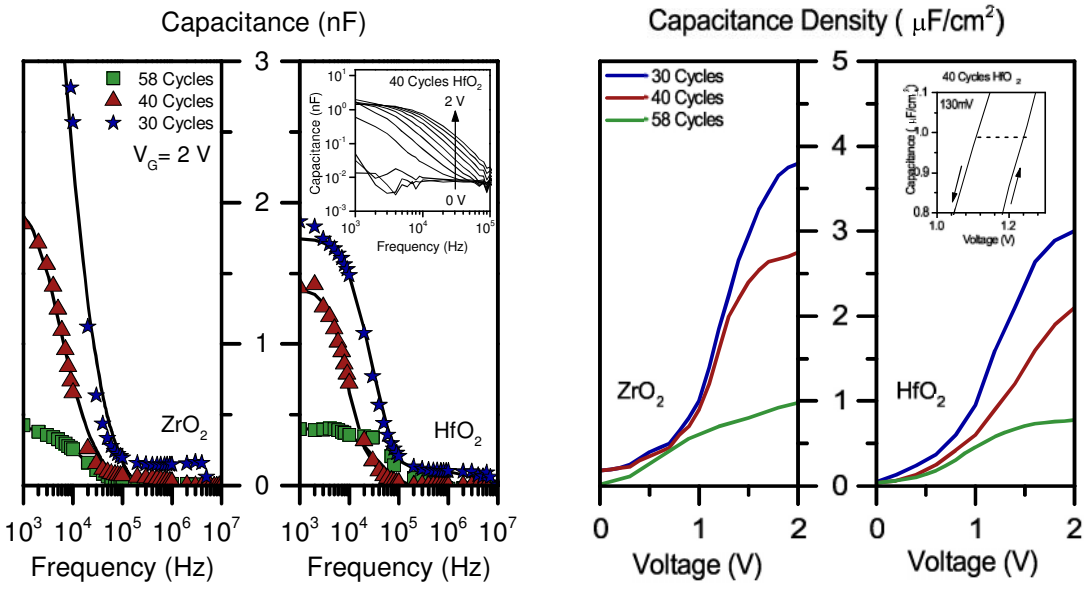
The input impedance of the total inner contact contained real and imaginary components. The real component of the admittance corresponded to the physical measured conductance ($G_{Measured}$), while the imaginary portion described the measured capacitance of the planar MOSCAP. By plotting (4.23) with respect to frequency, the capacitance-frequency measurement was replicated for a given inner contact voltage by adjusting the model parameters, shown in Figure 4.10a. Once the experimental data was correctly fitted to the model for a given device length L, the four parameters (R_s, C_p, G_p, and Z_L) were used to extract and characterize the interface quality.

$$C(f) = \frac{imag(Y_{in})}{2\pi f} = \frac{imag(1/Z_{in})}{2\pi f} \tag{4.23}$$

The capacitance density, shown in Figure 4.10b, was extracted from the model for each voltage by matching the measured $C - f$ spectrum to the model. The model and measurements confirmed the ZrO_2 films produced larger capacitance densities compared to the HfO_2 films for an equivalent growth cycle. The relative dielectric constant of the films were found through (4.24) which included the accumulation thickness within the GaN. Based on in-situ ellipsometry measurements during the growth, the ZrO_2 and HfO_2 films produced nearly equivalent growth rates and film thicknesses. Measurements indicated that the dielectric constant increased as the films became thinner for both rare earth metal oxides. This agreed with glancing XRD measurements of similar depositions which confirmed the film changed from amorphous to semi-crystalline as the film thickness increased.

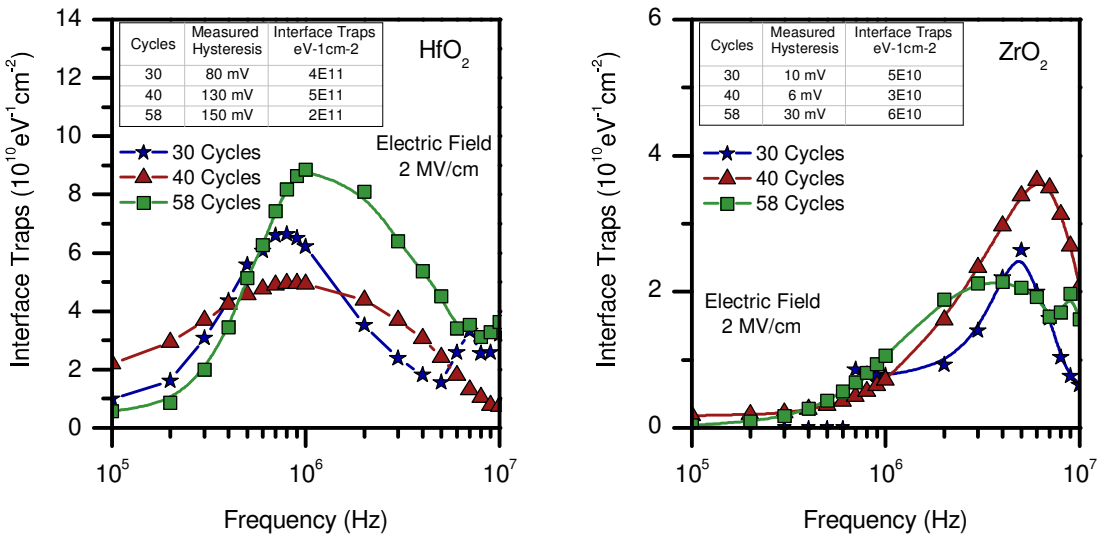
$$C_{peak} = \epsilon_0 \left(\frac{t_{ox}}{\epsilon_r} + \frac{t_{acc}}{\epsilon_s} \right)^{-1} \tag{4.24}$$

Low frequency hysteresis C-V measurements (Figure 4.10) were used to compare the density of interface traps along the dielectric and GaN surface. By sweeping the capacitance with respect to voltage, the interface traps were filled which caused a charging effect to shift the flatband voltage in the reverse sweep. By using a low frequency signal (10 kHz), we



(a) (b)

Figure 4.10: (a) Capacitance-frequency measurements used to characterize the films through a planar MOSCAP model. (Inset) Voltage dependence of 40 cycles HfO_2 C-f plots (b) The extracted capacitance density of the MOSCAP obtained from the C-f measurements. (Inset) Hysteresis of the 40 cycles C-V at 10 kHz.



(a) (b)

Figure 4.11: Density of interface traps along the dielectric/GaN surface obtained from $G_p - \omega$ and hysteresis measurements for (a) HfO_2 and (b) ZrO_2.

ensured that the interface traps would respond and create the largest possible shift. The hysteresis, ΔV, was used to determine the number of traps along the interface (4.25); where dielectric capacitance, $C_{ox} = \epsilon_{ox}/t_{ox}$, and the band-gap, E_G, of the semiconductor were known.

$$D_{it} = \Delta V \frac{C_{ox}}{qE_G} \tag{4.25}$$

The hysteresis results were compared to the conductance method (Figure 4.11) by extracting the conductance with respect to frequency while the gate was biased above the flat-band voltage. Both techniques were upon agreement that the HfO_2 films (Figure 4.11a) produced roughly 2-10 times more interface traps than the ZrO_2 films (Figure 4.11b). The narrow distribution of traps with respect to frequency in the ZrO_2 suggested there was nearly a single energy level along the interface rather than the broad HfO_2 distribution resulting from a more continuous distribution of traps along the energy levels throughout the GaN band-gap [16].

The results were compiled and compared (Table 4.1) for all films and thicknesses. The most important characteristics extracted from the model were the capacitance density, the dielectric constant, the peak electron channel mobility, the density of interface traps and the maximum operating voltage. The electron channel mobility was obtained from the MOSCAP model parameters C_p and R_s [63]. The maximum voltage for each film was determined when the current density increased due to high leakage; this was also observed

Table 4.1: Extracted Dielectric Properties on GaN

Film Type	# Cycles	Capacitance Density	Relative Dielectric	Peak Mobility	D_{it} (ΔV)	D_{it} $(G_p - \omega)$	Max Voltage
ZrO_2	30	3.8 $\mu F/cm^2$	34.8 +/- 4	360 cm^2/Vs	5x10^{10}	3x10^{10}	2V
	40	2.6 $\mu F/cm^2$	22.8 +/- 2	387 cm^2/Vs	3x10^{10}	4x10^{10}	4V
	58	1.1 $\mu F/cm^2$	12.1 +/- 1	370 cm^2/Vs	6x10^{10}	2x10^{10}	5V
HfO_2	30	3.0 $\mu F/cm^2$	22.9 +/- 4	263 cm^2/Vs	40x10^{10}	7x10^{10}	2V
	40	2.1 $\mu F/cm^2$	16.9 +/- 2	243 cm^2/Vs	50x10^{10}	5x10^{10}	4V
	58	0.8 $\mu F/cm^2$	8.1 +/- 1	233 cm^2/Vs	20x10^{10}	9x10^{10}	5V

when the measured capacitance drastically dropped due to Fowler-Nordhiem (F-N) leakage [100, 118]. This occurred when the conduction band of the dielectric was significantly bent due to high electric fields across the ultra-thin oxide. In turn, the effective thickness appeared obsolete which exponentially increased the tunneling probability and leakage current density as well. Compared to literature, these films were able to obtain high capacitance densities while maintaining a low interface trap density, shown in Figure 4.12 [66–80]. These characterized films provided a high capacitance density and low density of interface traps for a potential GaN MOSFET to surpass current HFET technology.

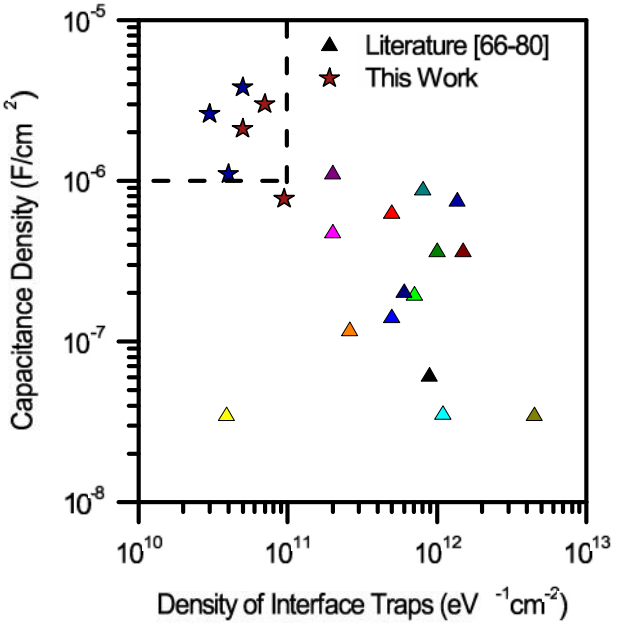


Figure 4.12: The dielectric properties of the low temperature PEALD HfO_2 (red stars) and ZrO_2 (blue stars) films compared to literature (triangles). The ultra-thin films were able improve the capacitance density and interface traps by a factor of 30.

Based on the experimental results of the planar MOSCAP, it was determined that ZrO_2 films enhanced the performance and device characteristics over HfO_2 and other gate dielectrics. The ZrO_2 films produced the largest capacitance density and lowest interface defects which in turn produced large dielectric constants and large peak electron mobility, respectively. Though the thinnest ZrO_2 films (30 cycles) produced the best results, the maximum voltage before uncontrollable gate leakage (F-N) occurred at half of 40 and 58 cycles maximum voltage. Thus, the 40 cycle ZrO_2 film would maintain sufficient gate leakage while providing high quality control of the GaN channel.

4.5 Summary

The novel low temperature plasma-enhanced atomic layer deposition of rare earth metal oxides improved the GaN channel interface over conventional dielectric deposition techniques. The films were able to produce a high capacitance while preventing a low density interface traps along the channel. From electrical measurements, the MOSCAP mobility of the ZrO_2 films were improved over the HfO_2 films by $> 100\ cm^2/Vs$. The improvement was a direct results of the GaN and ZrO_2 interface and the reduce density of traps. Based on the extracted results a ZrO_2/GaN gate dielectric would have the potential to improve the charge control more effectively than the PEALD HfO_2 and films found in literature. The minimized density of interface traps suggested the channel mobility on the MOSFET has the potential to surpass 300 cm^2/Vs.

With the most important interface of the device resolved and characterized, the following chapter will examine the novel technique used to overcome the complications arising from ion implantation in GaN for the source/drain regions as well as the substrate doping required for optimal device performance.

Chapter 5

Source and Drain Characterization

5.1 Introduction

Following the characterization of the gate dielectric and channel interface, PEALD films were examined for use along the source and drain to supply carriers to the channel of the device. A low sheet resistance in addition to a low contact resistance are imperative to minimize overall parasitic resistances within the MOSFET. Negligible parasitic resistance will allow the drain current to be dictated by the channel, rather than being limited by the contact resistances outside of the device. As discussed earlier the techniques required to physically dope the semiconductor through ion implantation or growth diffusion are expensive and complex. Following an ion implantation, high annealing temperatures are required to fix the defects formed in the substrate and along the interface. To circumvent this issue, polarized films grown on GaN were examined to produce a high concentration of carriers along the interface to behave as the source and drain regions.

It has been well documented how specific polarized films on GaN are capable of creating a 2-dimensional electron gas carriers (2DEG) along the interface. These large carrier densities along the interface have the equivalence to highly doped regions in GaN from conventional doping techniques [83, 86, 119, 120]. Based on Wentzel-Kramers-Brillouin (WKB) approximation of quantum mechanic tunneling, the incorporation of an ultra-thin film, a low conduction band offset and a small effective electron mass have the potential to realize tunneling contacts [100, 101]. In addition, the proposed 2DEG formed along source and drain regions has been shown to provide a high mobility interface to further reduce the device parasitic resistances. A large band gap film was preferred to promote conduction

through the GaN rather than the thin film. Lastly, the reliability of the films for high power applications must be able to surpass current AlGaN HFET technology. With GaN striving to become the next generation high power transistor, the reliability of the films are essential for longevity of the device.

Based on effective mass, band-gap, electron affinity, polarization and atomic mass, as shown in Figure 5.1, the nitride films that were examined for the incorporation in the GaN MOSFET were AlN and ZrN. ZrN has been demonstrated as a metallic film when the chemical composition between nitrogen and zirconium was 1:1. However, as the nitrogen content was increased the ZrN_x film demonstrated semiconductor behavior [121–123]. The ZrN_x semiconductor phase, like AlN films, has the potential to create a 2DEG along the GaN interface; however, to date this has not been investigated to the fullest extent. InN and TiN were not consider since TiN does not have a band gap and InN/GaN would form a channel in the InN rather than the GaN. Thus, these two materials were not useful nitride films for the source and drain region. Conversely, AlN films have the potential to provide a large 2DEG and wide band-gap, ideal for the source and drain regions, while ultra-thin ZrN films provided a compatible electron affinity to GaN, a large atomic mass for the potential of improved reliability for incorporation into the contacts and high electric field regions.

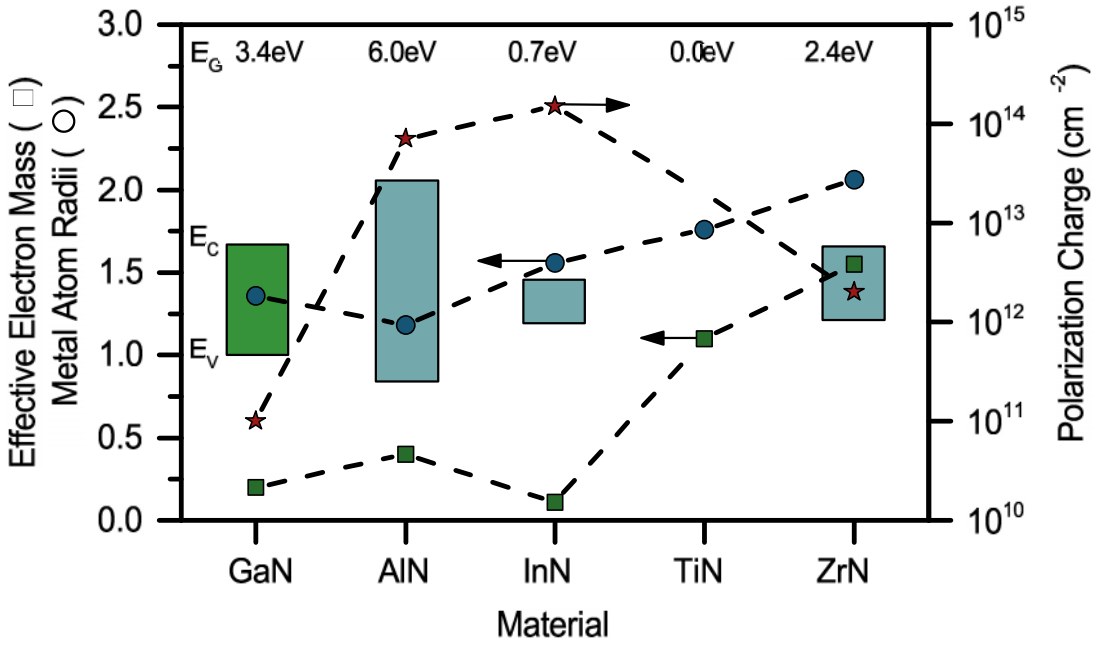


Figure 5.1: The proposed nitride based films for the source/drain regions compared three electrical properties imperative to produce low ohmic contacts, high carrier densities and a reliable device; the effective electron mass, metal atomic radii and polarization charge were compared between the nitride films. AlN has the potential to form the largest 2DEG along the interface, while ensuring the current would flow through the GaN.

5.2 Nitride Film Fabrication

The fabrication techniques used to grow the AlN and ZrN_x films were similar to the techniques discussed in the previous chapter for the gate dielectrics. However, rather than using an oxygen plasma as one of the precursors, forming gas ($H_2 + N_2$) was used as the nitrogen plasma precursor. The films were deposited in a Kurt J. Lesker chamber at a constant pressure of 1 Torr. The alternating precursor gases used were forming gas and trimethylaluminum (TMA) for AlN, or tetrakis(dimethylamido)-zirconium (TDMAZ) for ZrN_x films. The growth temperature of the films, AlN (230^oC) and ZrN_x (150^oC), were based on optimized growth conditions based of XRD described in [124]. The AlN films does/purge times for the forming gas and TMA were (10.00/7.00s) and (0.02/7.00s), respectively. Likewise, the ZrN_x films were optimized for forming gas and TDMAZ with does/purge times of (9.00/9.00s) and (0.10/9.00s), respectively. The ZrN_x deposition parameters were adjusted such that the semiconductor phase was grown rather than the metallic ZrN_x film (Zr:N = 1:1). The semiconductor film was produced by creating the ZrN_x ($x \approx 1.3$) chemical structure, which created a band-gap of approximately $E_G = 1 - 2eV$ [121–123, 125, 126].

To initially characterize the films, approximately 3 nm films were deposited on GaN, shown in Figure 5.2. Depending on the material, the number of PEALD cycles were different

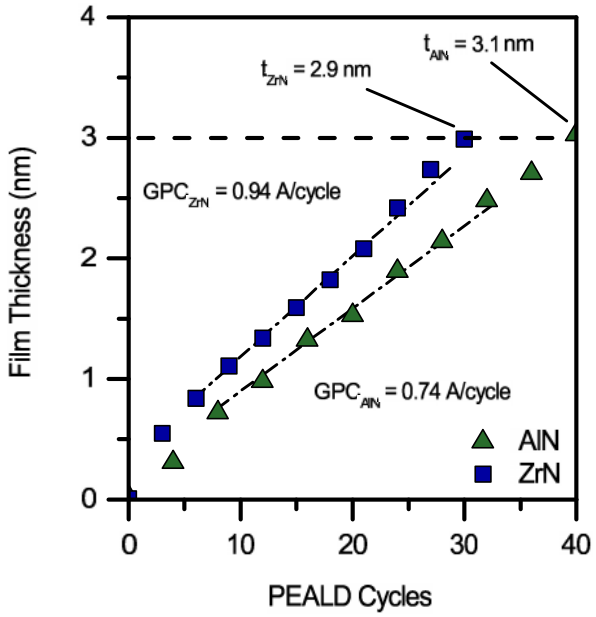


Figure 5.2: The film thickness for AlN and ZrN_x with respect to PEALD cycle were obtained from in-situ ellipsometry; courtesy of Pouyan Motamedi (AlN) and Triratna Muneshwar (ZrN_x).

for AlN (40 cycles) and ZrN_x (30 cycles). The growth per cycle rate for each material was determined from in-situ ellipsometry. Following the growth of the films, the metals under investigation were sputtered and patterned by a photoresist lift-off technique. Once these films were characterized, other film thicknesses of AlN and ZrN_x were examined to further improve the contact and sheet resistance.

5.3 Characterization Methods

Test structures, shown in Figure 5.3, were used to characterize the films along the source and drain regions through current-voltage (I-V) and capacitance-voltage (C-V) measurements. These measurements were used to extract the contact resistance, sheet resistance, 2DEG carriers and 2DEG mobility. The three test devices fabricated were transfer length method structures (TLM), metal oxide semiconductor transfer length method structures (MOS-TLM) and metal oxide semiconductor heterojunction capacitors (MOSHCAP). The MOS-TLMs and MOSHCAP included the characterized ZrO_2 film (40 cycles) discussed in the previous chapter.

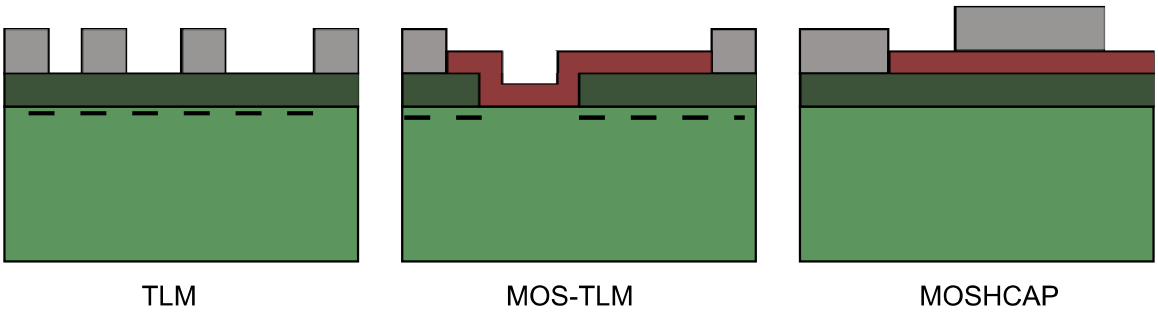


Figure 5.3: Schematic of the test structures to evaluate the AlN and ZrN_x films. The TLM structures were used to evaluate the contact and sheet resistance produced by the 2DEG along the GaN interface. The MOS-TLM included a non-polarized region to extract the contact and sheet resistance of the nitride film, in addition to confirming the GaN sheet resistance. The advantage of the MOSHCAP was to extract the 2DEG through capacitance-voltage measurements.

Current-voltage measurements were obtained for the TLM and MOS-TLM to evaluate the contact behavior. The total resistance between the gaps were used to determine the sheet resistance (R_{sh}) of the films interface and contact resistance (R_c) of the metal deposited [16]. A first indication whether the nitride film and GaN interface induced a polarized charge was determined from the sheet resistance. An increased carrier density along the films interface behaved similar to a doped region along the GaN template which would lower

the sheet resistance. The incorporation of a tunneling contact has the potential to reduce the complexity of the metal stack and high annealing temperatures [84, 127]. It has been shown that the contact resistance of tunneling contacts has a strong dependence on the thickness of the film, the carrier density at the interface and the workfunction of the contact metal [82, 128].

The 2DEG density formed along the interface of the ZrN_x/GaN and AlN/GaN interfaces was determined from the capacitance measurements of MOS-HFET diodes. This was achieved by determining the amount of charge under the channel between reverse bias pinch-off voltage (V_{Pinch}) and flat-band voltage (V_{FB}). A gate dielectric was used to create a capacitor which could control the 2DEG channel. By comparing the depletion capacitance measurements with expected values of a MOS, the 2DEG could be determined. The conductivity of the interface can be related to the sheet resistance of the films (5.1) and the 2DEG concentration (5.2) to extract the 2DEG mobility of the film [14–16]. The interface mobility (5.3) was calculated based on the extracted sheet resistance obtained from the TLMs and the 2DEG carriers extracted from the MOSH capacitors. This technique is commonly used to characterize the mobility and interface quality of the 2DEG of the thin films grown on a semiconductor [85].

$$\sigma = \frac{1}{\rho} = \frac{1}{R_{sh} \cdot t_{2DEG}} \tag{5.1}$$

$$\sigma = nq\mu_e = \frac{N_{2DEG}}{t_{2DEG}} q\mu_e \tag{5.2}$$

$$\mu_e = \frac{1}{qR_{sh}N_{2DEG}} \tag{5.3}$$

5.4 Aluminum Nitride

The incorporation of AlN on GaN, shown in Figure 5.4, has be known to form a 2DEG along the interface due to an induced polarization charge. To characterize the AlN film Si-doped GaN (N^+) and unintentionally-doped GaN (N^-) templates were used to examine the 2DEG formation along the interface and tunneling contact resistance. It has been shown that the 2DEG formed along the interface has a strong dependence on the surface potential of the GaN substrate due to substrate doping [129]. An ultra-thin 3 nm AlN film was deposited on different doped GaN templates in an attempt to produce a low ohmic contact with a high

tunneling probability of electrons the barrier. The tunneling probability of the films was constant; however, the formation of the 2DEG along the interface was strongly dependent on the substrate doping [130]. Current and capacitance measurements associated with voltage and frequency dependence were examined to evaluate the films for the potential use in the GaN MOSFET architecture.

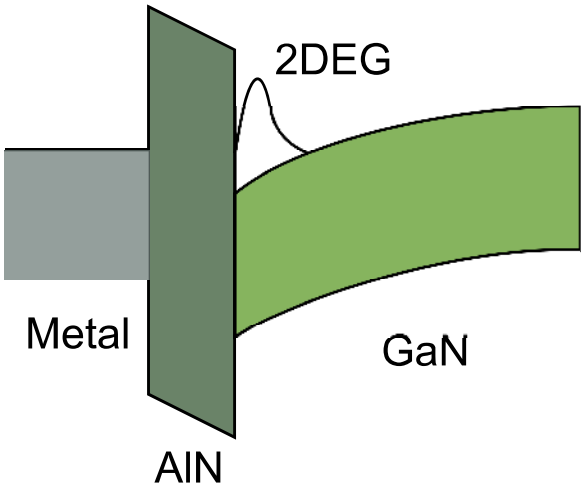
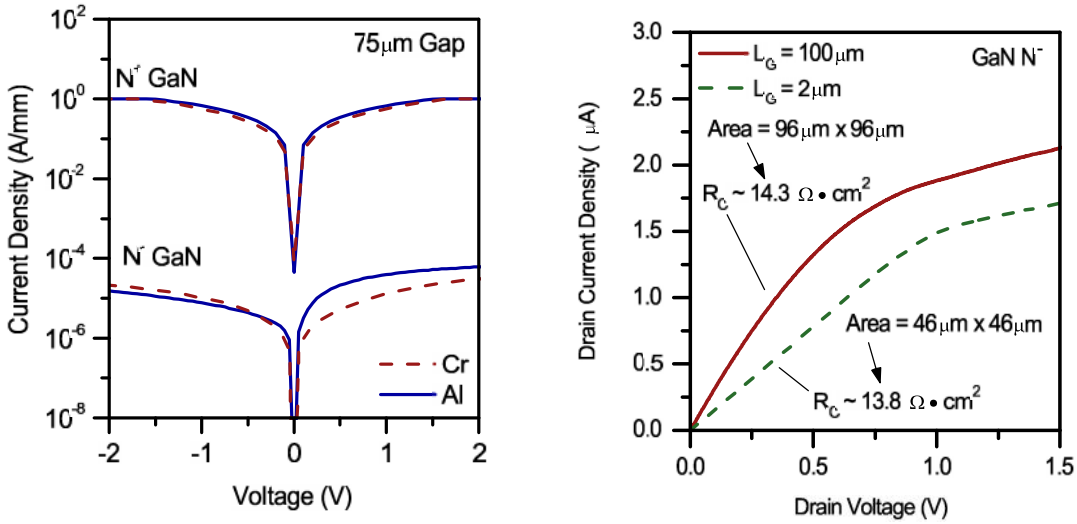


Figure 5.4: The band structure of the AlN/GaN with the induced 2DEG carriers formed along the interface.

5.4.1 Current-Voltage Characterization

The DC current-voltage measurements were obtained for tradition TLMs as-well as MOS-TLMs to extract the contact and sheet resistance of the AlN films grown on the various doped GaN templates. The higher doped GaN produced large current densities, shown in Figure 5.5a, regardless of the metal contact compared to the unintentionally doped GaN. However, The Al contacts were able to improve the contact resistance by roughly 20% over the Cr metalization contact. The low metal workfunction improved the tunneling probability which in-turn reduced the tunneling contact resistance. The normalized contact resistance was determined to be consistent for all device dimensions, as shown in Figure 5.5b. The smaller devices features produced more resistive contacts, however the contact resistivity of the contacts were consistent.

The results of the N^+ GaN MOS-TLMs and N^- GaN TLMs, shown in Figure 5.6, were used to extract the sheet resistance and tunneling contact resistance of the metal/AlN/GaN. The total resistance of the MOS-TLM (5.4) was described by the contact resistance, and sheet resistance of the gate, source and drain regions. The slope of the gate-drain MOS-TLM was used to extract the sheet resistance of the AlN/GaN. Likewise, the contact resistance was extracted from the y-intercept once the source and gate region was canceled out. As



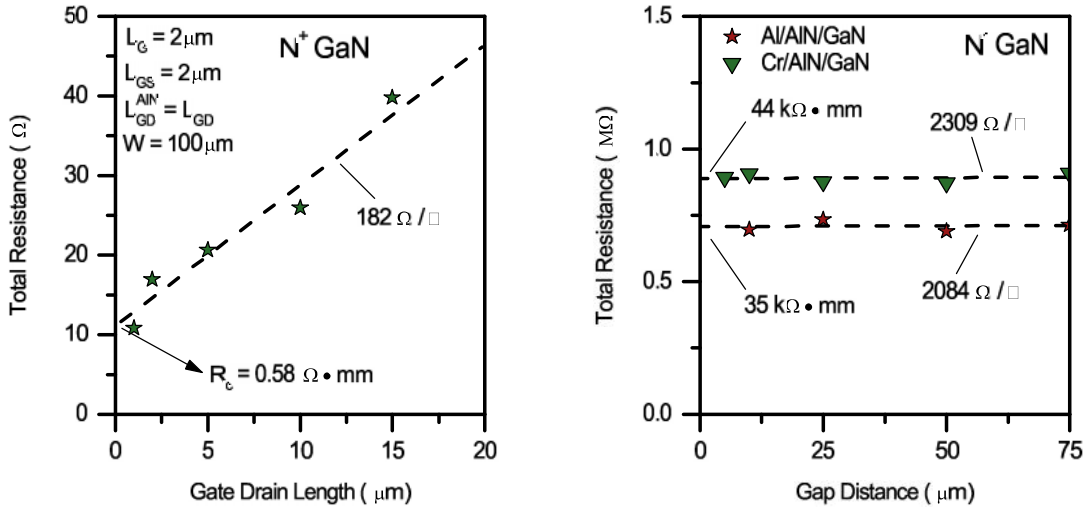
(a) (b)

Figure 5.5: (a) The I-V measurements from the 75 μm gap TLM followed the trend as the doping of the GaN was reduced. In addition, the Al metal contact produced higher current densities than the Cr counter part for both cases of GaN templates. (b) The Cr MOS-TLM results on N^- GaN confirmed the contact resistance from two devices with different contact areas. The extracted contact resistivity between the different dimension devices was less than 5%.

expected the higher doped templates produced a lower sheet resistance compared to the N- GaN substrates. Furthermore, the large amount of carriers under the metal contact, significantly reduced the contact resistance.

$$R_{tot} = 2R_c + R^S_{AlN}\frac{L_{GS}}{W} + R^G_{ZrO_2}\frac{L_G}{W} + R^D_{ZrO_2}\frac{X_{ox}L_{GD}}{W} + R^D_{AlN}\frac{(1-X_{ox})L_{GD}}{W} \tag{5.4}$$

The extracted sheet resistance and contact properties obtained from the TLM I-V results were compiled in Table 5.1. As expected, the metal contact did not effect the 2DEG sheet resistance at the AlN/GaN interface. However, the background doping concentration significantly dictated the sheet resistance and in-turn the tunneling contacts. Through the use of a the lower electron affinity metal (Al), the contact resistance was reduce for both GaN doping concentrations.



(a) (b)

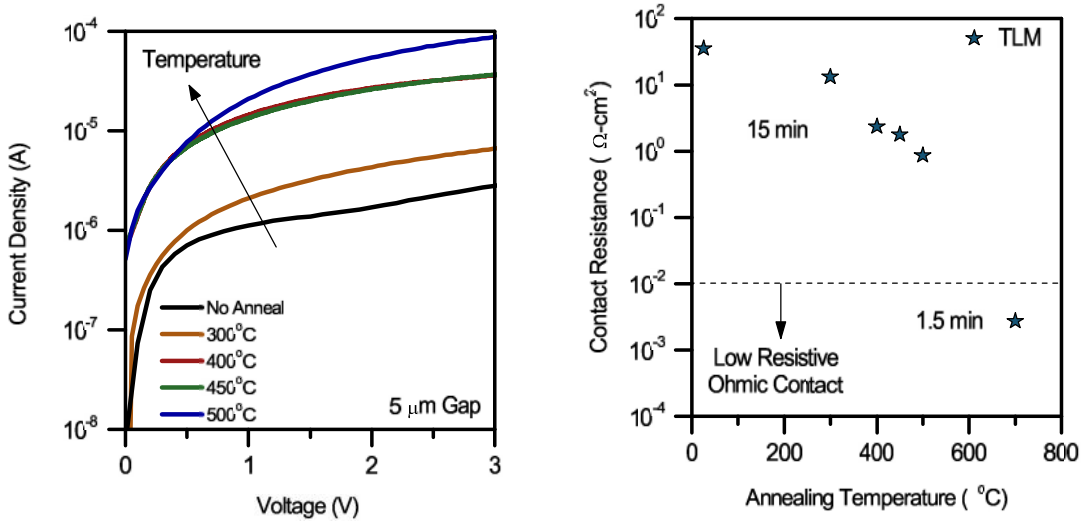
Figure 5.6: (a) The N^+ GaN Cr MOS-TLM and the (b) N^- GaN TLM results used to extracted the contact and sheet resistance. The N^+ GaN templates produced lower contact and sheet resistance compared to the N^- GaN.

Table 5.1: Extracted Contact and Sheet Resistance Properties of AlN on GaN templates

GaN Doping	Device	R_{Cr} $(\Omega \cdot mm\ )$	R_{Al} $(\Omega \cdot mm\ )$	R_{GaN} (Ω/sqr)	R_{AlN} (Ω/sqr)
N^+	TLM	0.61	0.45	616	184
	MOS-TLM	0.58	0.40		236
N^-	TLM	45x10^3	35x10^3	5000	2309
	MOS-TLM	39x10^3	28x10^3		2084

Post Fabrication Annealing

It has been well documented that post fabricated annealing has the ability to reduce the contact resistance by orders of magnitude [92–95]. Extensive studies of AlGaN/GaN have shown the contact resistance significantly improves at higher temperatures for a wide range of annealing times [83, 93, 131]. This allows the process to be accurate and consistent with each batch fabricated. The 3 nm AlN on N^- GaN template was used for the annealing study to improve the contact resistance. The GaN template was exposed to the noted temperature for 15 minutes before electrical characterization was performed. Conventional TLM structures were measured to examine the contact resistance of the device as discussed earlier.



(a) (b)

Figure 5.7: (a) As the TLM structures were annealed the current density of the 5 μm TLM gap increased. (b) The improved conduction was strongly dependent on the reduced contact resistance with respect to annealing temperature. Annealing the device at 700^oC was found to produce a low ohmic contact ($5\text{x}10^{-3}\ \Omega \cdot cm^2$)

The contact resistance at each annealing temperature was extracted from the I-V measurements of the 5 μm TLM gap, shown in Figure 5.7a. The sheet resistance of the AlN/GaN gap was neglected since the gap resistance was more than 2 orders of magnitude smaller than the contact resistance. The contact resistance with respect to annealing temperature was displayed in Figure 5.7b. The results agreed with literature, that higher temperatures, regardless of the annealing time will improve the contact resistance for GaN based devices.

With the contact and sheet resistance characterized from the I-V results, the amount of the carriers formed along the thin film and GaN interface was examined through the frequency dispersion of capacitance and conductance results. In-conjunction with the sheet resistance, the capacitance-voltage measurements were used to extract the polarization as well as provide the characteristics required to obtain the 2DEG mobility along the AlN/GaN interface.

5.4.2 Capacitance-Voltage Characterization

The capacitance-voltage frequency response of a semiconductor device is the most accurate method to extract the behavior of the carriers within and along the interface of ultra-thin films. The 2DEG carriers formed along the interface were evaluated through the comparison between convention MOSCAPs and AlN MOSCAPs during reverse depletion regime. The

Table 5.2: AlN Dielectric Constant Extracted from Peak Capacitance Density

Gate Stack	Thickness (nm)	Capacitance ($\mu F/cm^2$)	t_{acc} (nm)	ϵ_r
ZrO_2	6.0 ± 0.2	2.56	1.0	22.8 ± 2.0
ZrO_2/AlN	6.0 ± 0.2 3.1 ± 0.2	1.36	0.8	22.8 ± 2.0 9.3 ± 0.6
AlN	3.1 ± 0.2	2.15	0.8	9.3 ± 0.5

accumulated carriers below the theoretical flatland voltage were a result of the induced polarization effect caused from the AlN and GaN [132]. To improve the accuracy of the C-V results the characterized ZrO_2 was included in the gate stack to reduce the tunneling conductance through the gate. The difference in peak capacitance was a result of the gate stack with and without the ZrO_2, shown in Table 5.2.

The peak capacitance density obtained in strong accumulation in conjunction with the accumulation thickness determined the dielectric constant of the AlN film. The accumulation thickness, shown in Figure 5.8, was determined from the 2D Poisson-Schroedinger equation. The AlN was assumed to have a narrow channel, similar to the simulated AlN (0.75-0.95 nm). Likewise, the ZrO_2 was expected to have a slightly larger channel than

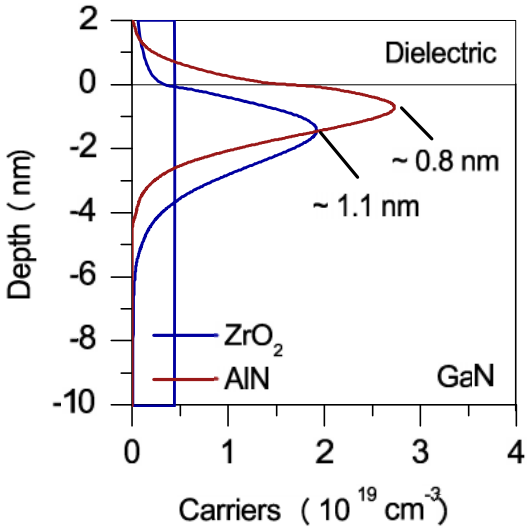


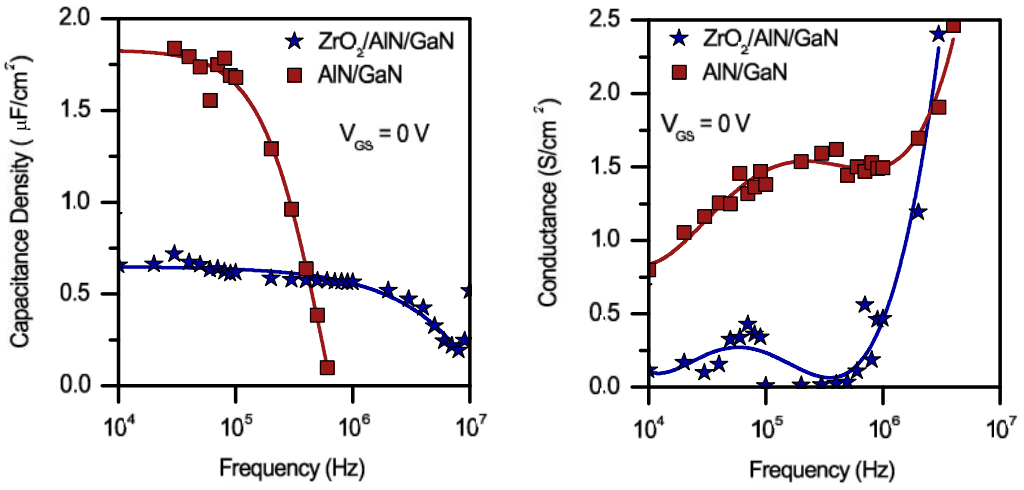
Figure 5.8: The simulated accumulation thickness for the AlN/GaN and ZrO_2/GaN to extract the dielectric constant of the films. The effective mass of the films determined the location of the peak centroid and the amount of carriers within the dielectric film. AlN allowed 4x the amount of carriers into the film compared to the ZrO_2 film.

the AlN. Whereas, the effective mass ratio between ZrO_2/GaN was expected to produce a smaller channel than the conventional SiO_2/GaN (1.2-1.4 nm). Thus, the accumulation centroids for ZrO_2 and AlN were assumed 1.0 nm and 0.8 nm, respectively.

Polarized Charge Extraction

The inclusion of the gate dielectric significantly improved the consistency of the capacitance frequency spectrum, Figure 5.9a, and reduced the conductance of the thin films, Figure 5.9b, allowing for a more accurate measurement of the 2DEG. A reverse biased capacitance-voltage measurement was required to extract the 2DEG charge formed along the AlN/GaN interface. As the herterojunction was depleted, the 2DEG charge (Q_{2DEG}) was removed from the polar induced quantum well at the pinch-off voltage (V_{Pinch}). The area beneath the capacitance measurement (C_m) (5.5) between flat-band voltage (V_{FB}) and V_{Pinch} was considered as the total charge produced from the AlN film. Removing the theoretical depletion charge within the GaN provided a more accurate extraction of the 2DEG charge and in-turn the 2DEG carriers (5.6).

$$Q_{2DEG} = \int_{V_{Pinch}}^{V_{FB}} C_m dV - Q_{Dep} \tag{5.5}$$



(a) (b)

Figure 5.9: The (a) capacitance and (b) conductance frequency dispersion based on the MOSCAP with and without a gate dielectric (ZrO_2) under one of the metal contacts. By including the gate dielectric, the leakage conductance was reduced which provided less frequency dispersion than the AlN metal films.

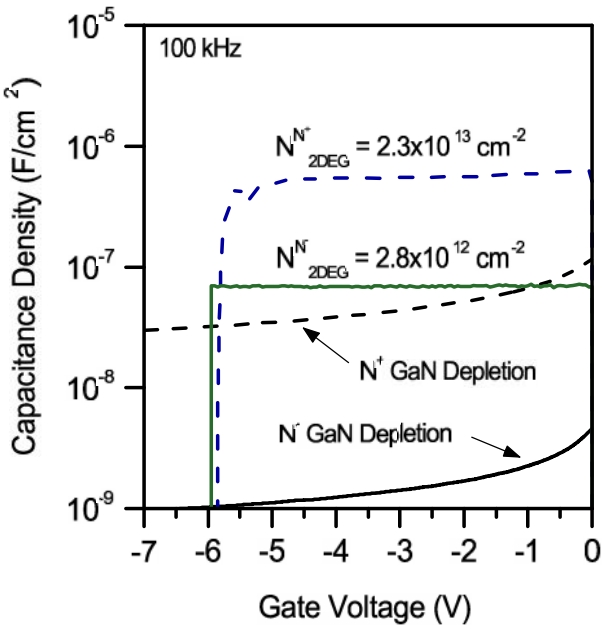


Figure 5.10: The reverse C-V gate bias of the MOSHCAPs used to extract the 2DEG for both GaN templates. The area between the C-V measurement and the theoretical depletion capacitance for GaN was the polarization interface charge. The N^+ GaN (blue) produced a 2DEG roughly 10x larger than the N^- GaN (green).

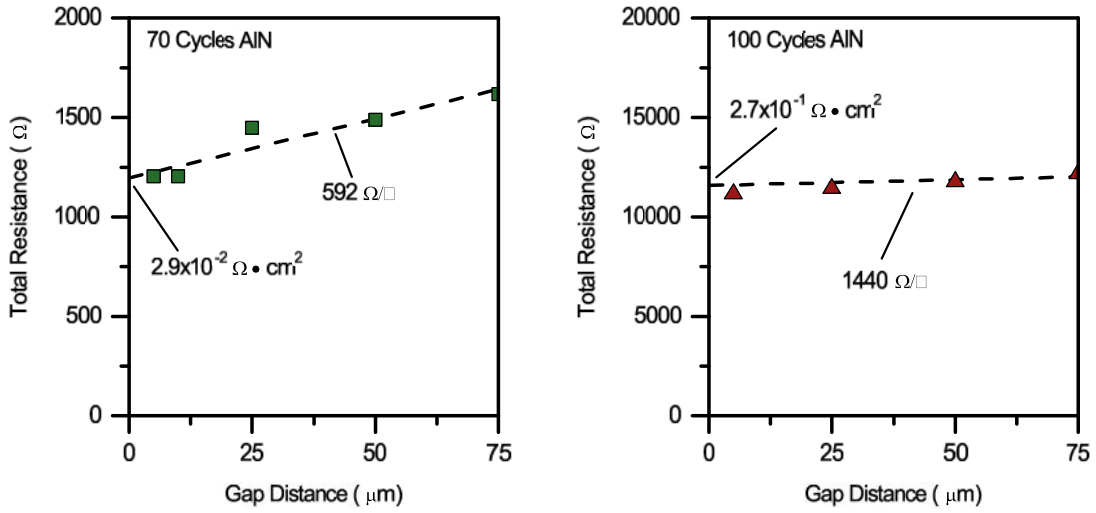
$$N_{2DEG} = \frac{Q_{2DEG}}{q} \tag{5.6}$$

The charge carrier density, Figure 5.10, was determined from the area beneath the capacitance-voltage measurements between flat-band voltage and pinch-off voltage. The inclusion of the dielectric film reduced the leakage current which produced a more consistent measurement of the 2DEG, 2.9x10^{13} $\pm$ 0.4x10^{13}cm^{-2}, with negligible frequency dispersion. The 2DEG carriers obtained from the capacitance for the N$^+$ and N$^-$ GaN confirmed that the variation between the TLM sheet resistance was consistent. The unintentionally doped GaN produced a lower 2DEG extracted from the C-V measurements, shown in Figure 5.10. The theoretical depletion capacitance for N$^+$ and N$^-$ GaN were included to confirm the increase of carriers from a non-polarized interface. This has been theorized that the film crystal orientation and effective polarization was dependent on substrate doping [129]. The peak carrier density along the AlN/GaN interface was determined from the thickness dependence 2DEG polarization effect.

5.4.3 AlN Thickness Dependence

The post fabrication anneal was shown to improve the contact resistance of the structures, however the sheet resistance remained unchanged. The 2DEG carriers along the GaN interface have been shown to increase with AlN thickness [85, 129]. The PEALD process grew 5.7 nm and 7.9 nm films which required 70 and 100 cycles, respectively. Improving the sheet resistance along the AlN/GaN interface would imply that the carriers within the 2DEG increased. In-turn, the tunneling contact resistance would improve, if the increased 2DEG offset the reduce tunneling probability of the larger film thickness.

Current-voltage measurements of conventional TLMs were used to extract the sheet and contact resistance, shown in Figure 5.11. As the AlN film thickness doubled from 40 to 70 cycles, the sheet resistance was reduced by a factor of 4. This suggested the amount of 2DEG carrier along the interface increased, assuming the channel mobility remained roughly constant. The 100 cycles AlN demonstrated a significant increase in the sheet resistance compared to the 70 cycle film, Figure 5.11b. It has been theorized that strain relaxation and dislocations within the AlN reduce the polarization strain when the thickness was beyond a critical value [129, 132]. The expected critical relaxation thickness for AlN was theoretically 6 nm [133], which agreed with the maximum 2DEG determined for the 70 cycle film. Beyond the critical film thickness, strain relaxation occurred, preventing an increase in 2DEG for thicker AlN films.



(a) (b)

Figure 5.11: The extracted contact and sheet resistance from the 5.7 nm and 7.9 nm AlN/GaN films.

The tunneling contact resistance and extracted sheet resistance and 2DEG for each film thickness was compiled in Table 5.3. The largest 2DEG produced by the 70 cycle AlN film improved the contact resistance by more than an order of magnitude compared to the 40 cycle and 100 cycle films. As the AlN films were increased to 70 and 100 cycles the sheet resistance obtained from the TLMs decrease and increase, respectively. This was consistent with the prediction based on the strain relaxation of the AlN beyond 6 nm. Based on the extracted sheet resistance from the I-V measurements, and 2DEG carrier density the interface channel mobility (5.3) was obtained. The results, shown in Table 5.3, were also compared to the 3 nm AlN on N^+ GaN and a semi-insulating (SI) GaN template. The SI GaN template was patterned with a 6 nm AlN. To increase the 2DEG and reduce the sheet resistance the channel was diffusion doped with Si. Titanium contacts were deposited and annealed at 415^oC to form ohmic contacts with Si doped AlN/GaN regions. Based on the contact resistance, the doped GaN was capable of providing low contact resistance without the required high temperature annealing. However, the semi-insulating template required high temperature annealing to produce equivalent sheet resistance and contact resistant as the unintentionally doped GaN.

Table 5.3: Extracted Sheet and Contact Resistance

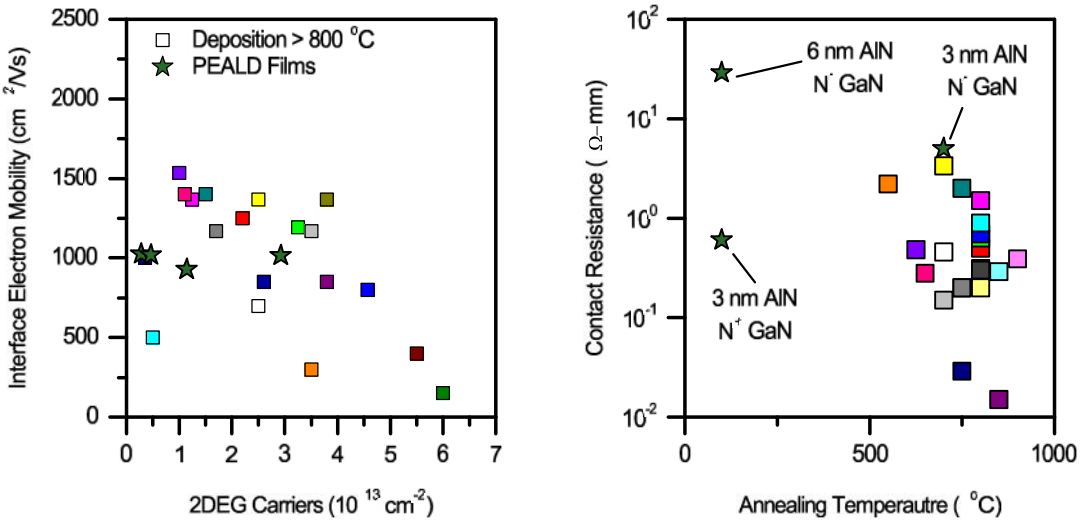
GaN Doping	AlN (nm)	R_C $(\Omega \cdot cm^2)$	R_{AlN} (Ω/sqr)	N_{2DEG} $(10^{13}cm^{-2})$	μ_e (cm^2/Vs)
N^+	3.2	3.1x10^{-4}	210 ± 10	2.39	1215 ± 46
N^-	3.2	1.7x10^{1}	2178 ± 130	0.28	1024 ± 58
	5.7	2.9x10^{-2}	592 ± 30	1.14	926 ± 45
	7.9	1.6x10^{-1}	1307 ± 50	0.47	1017 ± 38
SI	5.7	3.5x10^{-2}	610 ± 50	-	-

5.4.4 AlN Summary

Low temperature PEALD ALN films were demonstrated for the potential incorporation along the source and drain of a GAN MOSFET. The ultra-thin films produced large 2DEG carrier densities along the GaN interface while maintaining large channel mobilities. The PEALD films were able to produce similar 2DEG carrier densities and channel carrier mobility (Figure 5.12a) compared to convention MOCVD and MBE deposition techniques with growth temperatures 600^oC higher than the PEALD films characterized. This confirmed the large carriers densities and high interface mobility was possible with low temperature PEALD deposition techniques.

The large induced carrier density along the GaN interface provided the possibility of tunneling contacts through the AlN film. This reduced the required annealing temperature to achieve an ohmic contact, shown in Figure 5.12b, compared to conventional ohmic contacts for GaN. Furthermore, the metal contact did not required complex metal stacks; instead the tunneling contact resistance was based on the work function of the metal. Moreover, through annealing the contacts, the undoped GaN produced equivalent contact resistances compared to literature.

The electrical properties of the low temperature AlN films confirmed large carrier densities for the potential use in a GaN MOSFET along the source and drain regions. Through AlN tunneling contacts, doped GaN provided a low ohmic contact comparable to current technology, where as the undoped GaN required high temperature annealing to achieve similar values. The following section examined novel ZrN_x materials to further improve the reliability of the high electric field regions and potential advance the overall device characteristics of the GaN transistor.



(a) (b)

Figure 5.12: (a) The comparison between carrier density to channel mobility of AlN films on GaN. The low temperature films produced equivalent 2DEG charge and carrier mobility as conventional high temperature deposition techniques. (b) The contact resistance of the doped GaN tunneling contact produced similar values to high temperature annealed metal contacts on GaN.

5.5 Zirconium Nitride

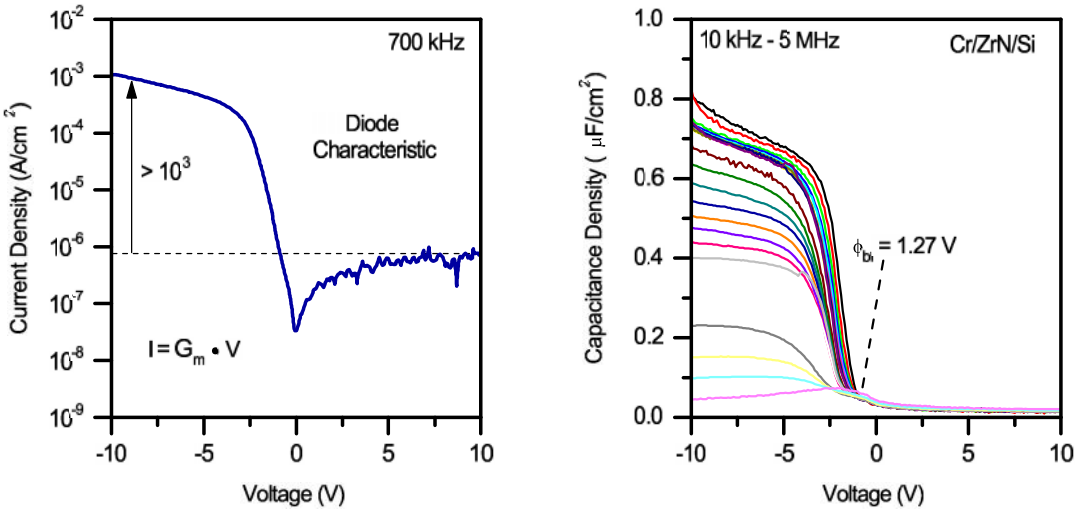
The semiconductor phase ZrN_x was also considered for regions along the source/drain of the GaN MOSFET because of the potential polarization, longevity and stability of the material. As mentioned early, the ZrN_x films electrical behavior (metallic or semiconductor) was based on the stoichiometric ratio between Zr and N. Again, the conventional metallic ZrN was produced by maintaining a 1:1 ratio between Zr and N. However, increasing the nitrogen content within the films has shown to shift the material from a metal to a semiconductor with a band-gap around 2 eV [125]. X-ray photon spectroscopy (XPS) of the deposited ZrN_x films contained an increase N content (x = 1.2) for the films discussed in this chapter.

The electrical material properties of ZrN_x, such as effective electron mass (m_e), relative dielectric constant (ϵ_r), conduction band density of states (N_C), valence band density of states (N_V), and electron mobility (μ_e), have not been extensively examined or extracted from electrical measurements. To obtain these properties, ultra-thin PEALD films were grown on p-type Si, N^+ GaN and N^- GaN templates. Various test structures discussed earlier were fabricated to evaluate the material properties of ZrN_x and extracted the electrical properties. The silicon wafer was used to confirm the XPS data that the ZrN_x film was non-metallic through characterization the film grown on the most well known semiconductor. The p-type silicon was expected to produce a pN heterojunction which would allow for the extraction multiple material properties through the C-V depletion region.

5.5.1 ZrN_x on Silicon

The ZrN_x/Si stack was pattern with chromium metal contacts to ensure adhesion and form an ohmic contact on the pN junction. The 3 nm ZrN_x was characterized with current-voltage and capacitance-voltage measurements through the pN heterojunction to the back side silicon wafer. The silicon was placed to ground while the metal contact was biased on the top side of the structure.

Through the current-voltage measurement, shown in Figure 5.13a, the results confirmed that the films formed a non-ohmic contact. The Cr/ZrN_x/Si stack restricted current in one direction while producing a large current in the other; i.e. a diode. This suggested a pN-junction or Schottky barrier was formed along one of the interfaces. To determine which junction was formed along the materials interface, the capacitance-voltage frequency spectrum (Figure 5.13b) was obtained. The reverse C-V bias behaved similar to an accumulation MOS capacitance on silicon. The theoretical built-in potential for metallic ZrN on p-type silicon would be a maximum of 0.4 V, compared to the extracted $\phi_{bi} = 1.27$ eV. This was the first electrical confirmation that the ZrN_x was a semiconductor rather than a metal. Furthermore, the capacitance of the Schottky metal contact would have dropped



(a) (b)

Figure 5.13: (a) The measured I-V of the ZrN_x/Si junction, courtesy of Kevin Voon. (b) The frequency dependent C-V measurements of the ZrN_x/Si, courtesy of Kevin Voon. The rectifying current density confirmed that a Schottky contact or pn-junction was formed. The extract built-in potential ($\phi_{bi} = 1.27$ eV) of the material system confirmed a p-n junction was formed at the ZrN_x/Si interface.

to zero for voltage biases beyond the built-in potential. During the accumulation portion of the measurement, the dielectric constant of the ZrN_x was extracted through the peak capacitance density. The accumulation of holes along the surface and a native oxide was included in the model to describe a more accurate representation of the series capacitance (5.7).

$$\epsilon_{ZrN} = \frac{t_{ox}}{\epsilon_0}\left(\frac{1}{C_m} - \frac{t_{acc}}{\epsilon_{Si}\epsilon_0} - \frac{t_{SiO_2}}{\epsilon_{SiO_2}\epsilon_0}\right) \tag{5.7}$$

The peak capacitance density (0.75 $\mu F/cm^2$) was extracted from the low frequency (10 kHz) C-V measurement to extract the dielectric constant of ZrN_x, shown in Table 5.4. The accumulation thickness of holes along the silicon channel was assumed to have a finite thickness of roughly 1.1 nm [15,134]. This thickness was assumed equivalent to an inversion layer of holes in an n-type silicon. The native oxide (SiO_2) was assumed to have a negligible thickness less than a quarter of a nanometer. The dielectric constant ($\epsilon_{ZrN} = 7.2$) remained constant before the cut-off frequency (10^5 Hz) of the structure.

Through Poisson and Gauss equations the depletion lengths within the materials were described by the dielectric properties and doping concentrations [14]. Boundary conditions

Table 5.4: ZrN Dielectric Constant Extracted from Peak Capacitance Density

C_m $(\mu F/cm^2)$	t_{ZrN} (nm)	t_{acc} (nm)	t_{SiO_2} (nm)	ϵ_r
0.75	7.3 ± 0.25	1.1	0.25	7.2 ± 0.3

were applied at the interface to ensure the continuity of electric displacement and built-in potential were consistent from either side of the junction. Through these equations the depletion widths in the ZrN_x (5.8) and Si (5.9) were defined accordingly. The depletion width of the entire junction was the two lengths combined to form a capacitor along the junction (5.10). The built-in potential of a pN-junction was also defined from the difference in Fermi levels between the two materials, represented in (5.11). The theoretical values of effective conduction band and valence band density of states for Si were 3.2x10$^{19}cm^{-3}$ and 1.8x10$^{19}cm^{-3}$, respectively. The third term was neglected as the theoretical density of states for silicon and ZrN_x were expected to have similar values. Using the slope and intercept of the measured inverse squared capacitance (Figure 5.14), in-conjunction with (5.10) and (5.11) the built-in potential, the ZrN_x doping, the silicon doping and the expected ZrN_x band-gap were obtained. In addition, the effective conduction and valence band density of states for were extracted, to further determine the effective masses for electrons (m_e) and holes (m_h).

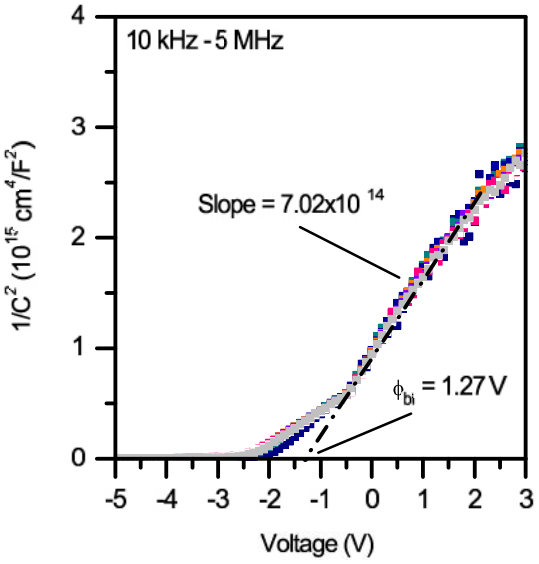


Figure 5.14: Inverse squared capacitance of the measured test structure which was used to extract the electrical properties of the ZrN_x film. The built-in potential was obtained from the x-axis intercept and the silicon doping concentration of was extracted from the slope.

$$x_n = \sqrt{\frac{2N_{A_{Si}}\epsilon_{Si}\epsilon_{ZrN_x}\left(\phi_{bi}+V\right)}{qN_{D_{ZrN_x}}\left(N_{D_{ZrN_x}}\epsilon_{ZrN_x}-N_{A_{Si}}\epsilon_{Si}\right)}} \tag{5.8}$$

$$x_p = \sqrt{\frac{2N_{D_{ZrN_x}}\epsilon_{Si}\epsilon_{ZrN_x}\left(\phi_{bi}+V\right)}{qN_{A_{Si}}\left(N_{D_{ZrN_x}}\epsilon_{ZrN_x}-N_{A_{Si}}\epsilon_{Si}\right)}} \tag{5.9}$$

$$C_{dep} = \sqrt{\frac{qN_{D_{ZrN_x}}N_{A_{Si}}\epsilon_{ZrN_x}\epsilon_{Si}}{2\left(N_{D_{ZrN_x}}\epsilon_{ZrN_x}+N_{A_{Si}}\epsilon_{Si}\right)\left(\phi_{bi}+V\right)}} \tag{5.10}$$

$$\phi_{bi} = \frac{\Delta E_C - \Delta E_V}{2} + \frac{kT}{q}\ln\frac{N_{D_{ZrN_x}}N_{A_{Si}}}{n_{i_{ZrN_x}}n_{i_{Si}}} + \frac{kT}{2q}\ln\frac{N_{V_{ZrN_x}}N_{C_{Si}}}{N_{C_{ZrN_x}}N_{V_{Si}}} \tag{5.11}$$

Through self-consistent solving of (5.10) and (5.11), the built-in potential, doping concentrations and band-gap were extracted to Table 5.5. The measured and theoretical built-in potential confirmed a pN-junction was formed along interface rather than a metallic ZrN_x/Si Schottky barrier. The extracted data confirmed a lightly doped silicon wafer (2x10$^{16}cm^{-3}$), while the ZrN_x was effectively higher doped (5x10$^{17}cm^{-3}$). Likewise, the intrinsic carrier concentration, band-gap, effective density of states and effective electron and hole masses were extracted from the capacitance-voltage measurements.

Table 5.5: Extracted Electronic Properties of ZrN_x

N_C	6.1x10$^{19}cm^{-3}$
N_V	1.9x10$^{19}cm^{-3}$
n_i	5.9x10$^{4}cm^{-3}$
E_G	1.7 eV
χ_s	3.95 eV
ϵ_r	7.2
m_e	1.80
m_h	0.85

The properties of the ZrN_x were obtained from the unique pN heterojunction formed with silicon, which confirmed the semiconductor present rather than a metallic refractory metal nitride. Knowing the electrical properties of silicon, the characterization of the thin film was possible through the band diagram and Poisson and Gauss equations. Furthermore,

the understanding of the electrical behavior for ZrN_x grown on other materials will have a stronger impact knowing the doping concentration and band structure. Films were grown on various doped GaN templates to evaluate ZrN_x/GaN interface for the potential use in GaN based applications. Similar device structures fabricated for AlN/GaN characterization were used to extract electrical properties of ZrN_x/GaN interface.

5.5.2 ZrN_x on GaN

The extraction of many fundamental properties of the ZrN_x material was possible since a non-polarized well known semiconductor, silicon, was used to evaluate the pN heterojunction. In-turn, we were able to predict the band diagram of ZrN_x and the expected band bending when deposited on different GaN templates, shown in Figure 5.15). The N^+ GaN template was expected to produce a 2DEG along the GaN interface due to the free electron carriers moving from the ZrN_x to the GaN. This effect was similar to modulation doping in AlGaAs/GaAs heterojunction devices [14].

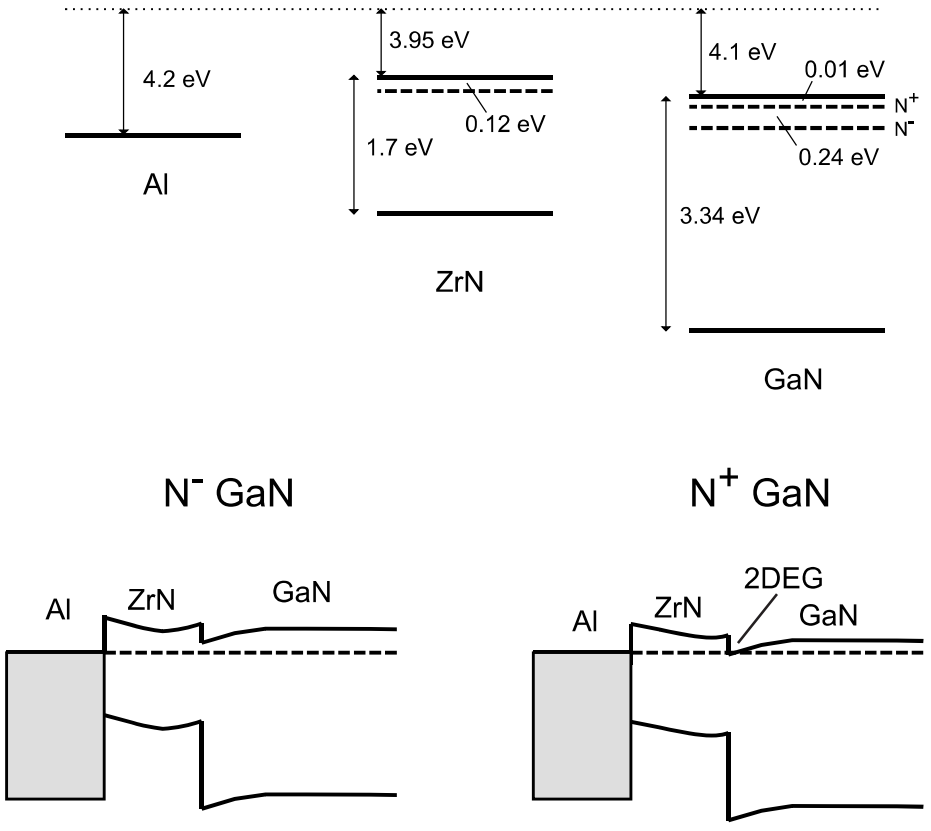


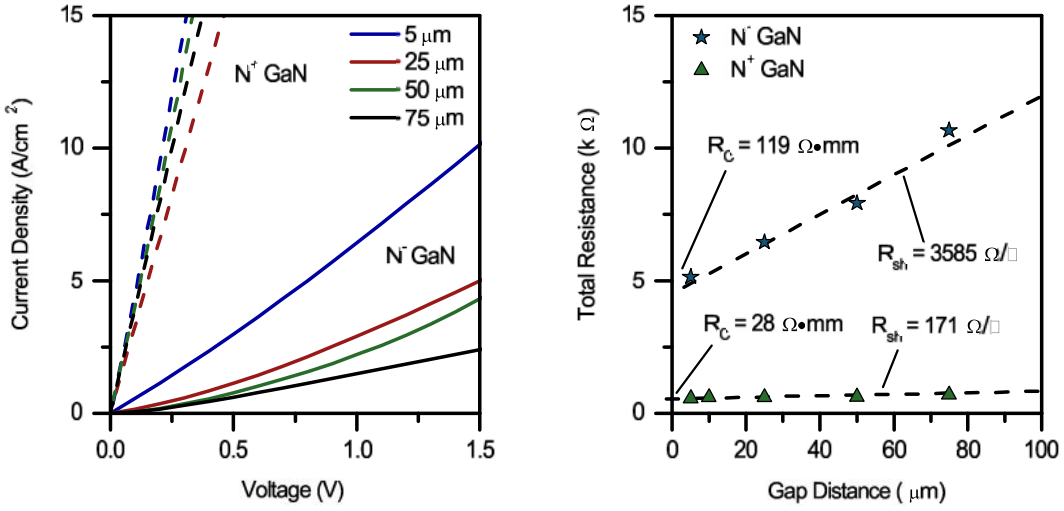
Figure 5.15: The expected band diagrams for ZrN_x on different background doped GaN templates based on the extracted electrical parameters obtained from the silicon measurements.

To evaluate the electrical interaction between ZrN_x and GaN, ultra-thin 3 nm PEALD ZrN_x (40 cycles) films were deposited on Si-doped GaN (N^+) and unintentionally-doped GaN (N^-) templates. These templates have different Fermi levels, which will change the built-in potential and electrical behavior based on the expected Fermi level within the ZrN_x. The TLM test structures and MOSHCAPs where fabricated with Al metal contacts and a ZrO_2 (40 cycles) gate dielectric.

Current-Voltage Characterization

To evaluate the quality of the contact resistance of the Al/ZrN_x/GaN system, I-V measurements of conventional TLM structures were used on both GaN templates. By varying the gap distance, the sheet resistance of the films would indicate whether a 2DEG was formed along the GaN interface. Similar to the AlN film, the GaN doping and Fermi level, played a significant role in the current density of the structures, shown in Figure 5.16a. As expected the Si-doped GaN reduced the resistances which increased the current by roughly 8x. Furthermore, the N^+ template was less dependent on the gap distance, which confirmed the sheet resistance was much smaller than the N^- GaN sample. The contact resistance and sheet resistance for both templates (Figure 5.16b) were extracted from the TLM resistance results.

As expected from the band diagram, the N^+ GaN formed a 2DEG along the interface



(a) (b)

Figure 5.16: (a) The current-voltage results of the N^- (Solid) and N^+ (Dashed) GaN templates. (b) The total resistance with respect to TLM distance used to extract the contact resistance and sheet resistance of the ZrN_x/GaN interface.

as the sheet resistance of the GaN reduced from 600 Ω/sqr to 171 Ω/sqr. Similarly, the N^- GaN template reduced the sheet resistance by roughly half of the original unintentionally doped GaN. If we assumed non-polarization effect occurred within the ZrN_x the effectively N^+ doped ZrN_x would have transfered free electrons to the GaN quantum well based on (5.12) [14]. The amount of carriers transfered into the quantum well was dependent on the number of carriers in the ZrN_x, the thickness of the ZrN_x, the conduction band offset and Fermi level. The ultra-thin layer of ZrN_x was assumed to provide all of the carriers within the film to the quantum well. Based on modulation doping effect the expected number of carriers within the quantum well was 2.15x$10^{12} cm^{-2}$ and 0.67x$10^{12} cm^{-2}$ for N^+ and N^- GaN, respectively.

$$n_s = \frac{\epsilon_{ZrN}}{qt_{ZrN}} \left(\frac{qN_d}{2\epsilon_{ZrN}} t_{ZrN}^2 + \frac{\Delta E_C - E_f}{q} - \phi_{bi} \right) \tag{5.12}$$

Capacitance-Voltage Characterization

To confirm the predicted modulation doped 2DEG along the interface, capacitance-voltage frequency spectroscopy of MOSHCAPs were obtained. The techniques used to evaluate the AlN films were applied to the ZrN_x films on GaN. Similar to the AlN, the reverse bias depletion region provided the information about the number of carriers within the quantum well.

The reverse voltage bias depleted the carriers along the quantum channel to determine the total electron density at equilibrium, obtained from C-V measurements (Figure 5.17). Again, the increased capacitance compared to the expected depletion capacitance was due to 2DEG carriers. The 2DEG measured along the interface was significantly larger than the expect 2DEG resulting from the modulation doped free carriers within the film. The additional carriers provided were caused from the polarization of ZrN_x. This confirmed that the ZrN_x films had a piezoelectric polarization effect similar to AlN and AlGaN.

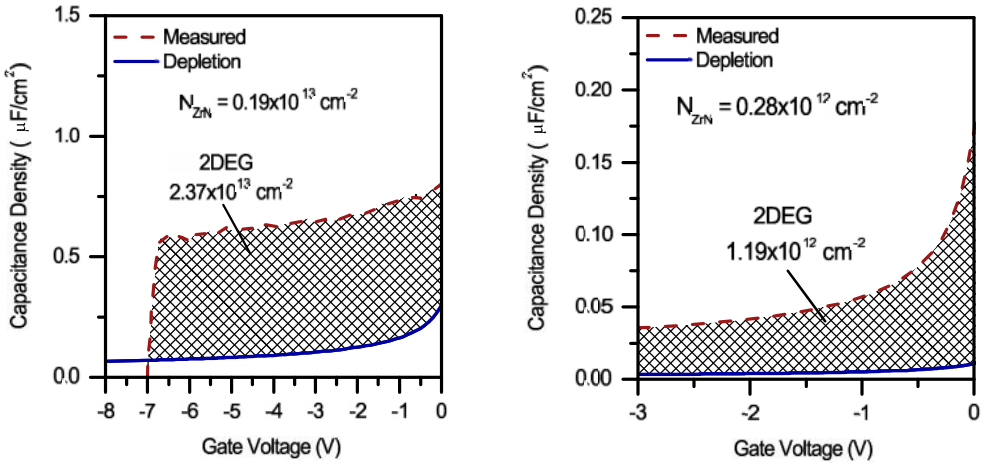
To confirm the dielectric properties of ZrN_x, the capacitance of forward bias MOSHCAPs were evaluated to confirm the channel location and band diagram. Interestingly, the forward bias C-V results of the MOSHCAPs were different depending on the background doping of the GaN templates. The doped GaN, which formed a larger 2DEG carrier concentration along the interface, produced the expected peak capacitance density (Figure 5.18a) for a ZrO_2/ZrN_x MOSHCAP. The capacitance was lower than the peak capacitance of 40 cycles of ZrO_2 on GaN, which was similar to the AlN MOSHCAPs which had multiple layers of dielectric films. This confirmed carriers accumulated along the GaN interface during forward bias, depicted in Figure 5.18c.

The lower doped GaN templates produced capacitance densities corresponding to a dielectric film of only a 40 cycle ZrO_2 film, shown in Figure 5.18b. For this to happen the accumulation of electrons occured within the ZrN_x film, rather than the GaN interface. At zero bias a small 2DEG was formed along the GaN interface, however at forward bias, accumulation occurred within the ZrN_x, shown in Figure 5.18d.

To confirm the dielectric constant and accumulation thickness of the ZrN_x, the peak capacitance was modeled for both the N^+ (5.13) and N^- (5.14) GaN templates. The ZrO_2 film capacitance was assumed equivalent to the results extracted from the previous chapter on gate dielectrics. Similarly, the channel thickness in GaN and ZrN_x were 0.9 nm and 1.0 nm, respectively. The tighter 2DEG channel within the GaN was determined from the dielectric ratio difference between AlN and ZrN_x. Solving both capacitance equations confirmed a ZrN_x dielectric constant of 7.4, which was within 5% of the extracted value obtain from the silicon test structures.

$$\frac{1}{C_{N^+}} = \frac{\epsilon_{ZrO_2}\epsilon_0}{t_{ZrO_2}} + \frac{\epsilon_{ZrN_x}\epsilon_0}{t_{ZrN_x}} + \frac{\epsilon_{GaN}\epsilon_0}{t_{acc}} \tag{5.13}$$

$$\frac{1}{C_{N^-}} = \frac{\epsilon_{ZrO_2}\epsilon_0}{t_{ZrO_2}} + \frac{\epsilon_{ZrN_x}\epsilon_0}{t_{acc}} \tag{5.14}$$



(a) (b)

Figure 5.17: Reverse bias C-V measurements of the ZrO_2/ZrN_x/GaN MOSHCAPs extracted the 2DEG along the GaN interface for (a) N^+ and (b) N^- GaN templates. The plots included the theoretical 2DEG expected from ZrN_x modulation doping (N_{ZrN}). The additional charge in the reverse bias confirmed that ZrN_x had polarization properties.

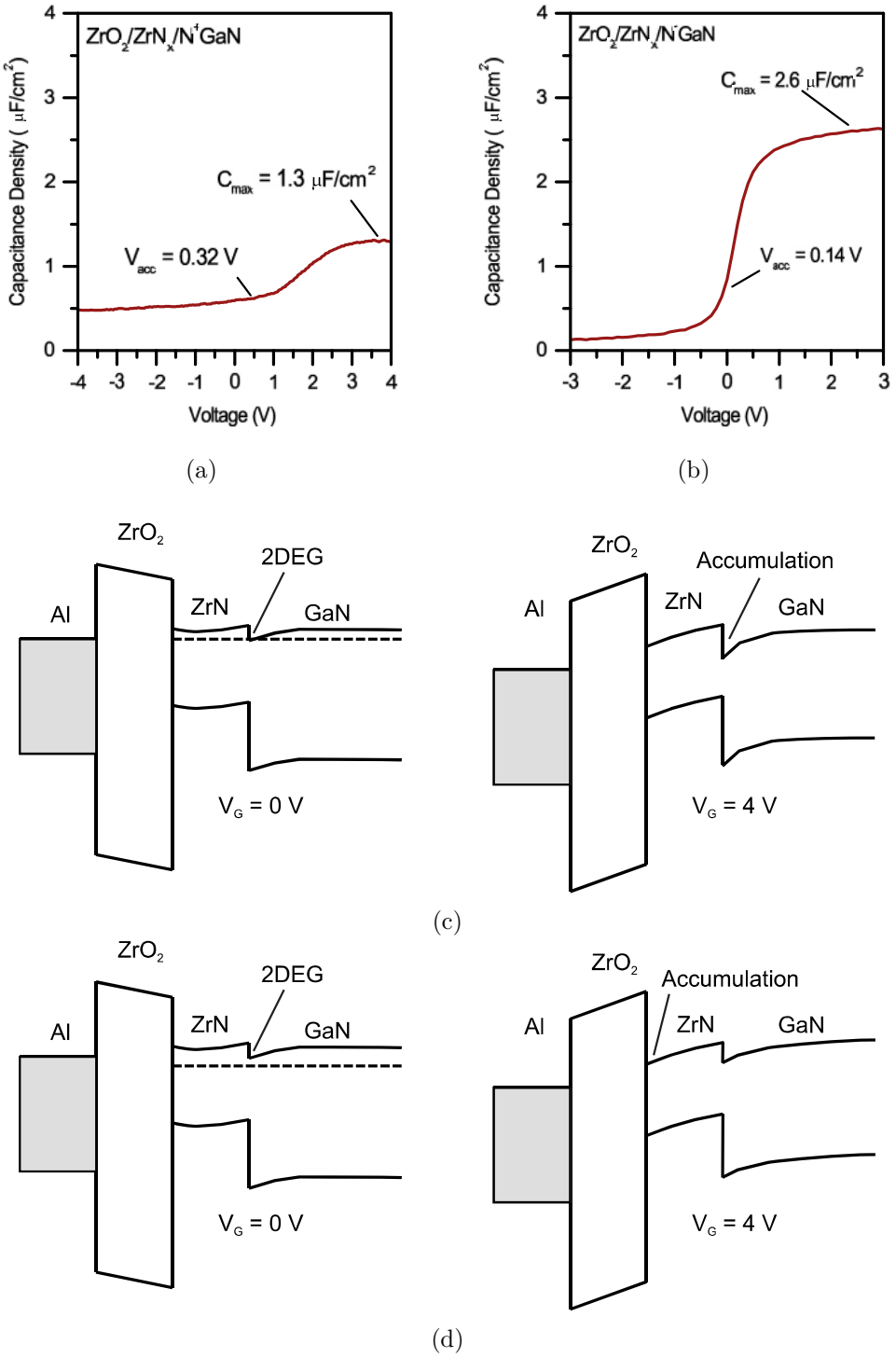


Figure 5.18: Low frequency C-V to obtain the dielectric characteristics of ZrN_x on (a) N^+ GaN and (b) N^- GaN. (c) The band diagram at zero bias and strong accumulation regime on N^+ GaN were both along the ZrN_x/GaN interface. (d) The accumulation of the electrons for the N^- GaN template occurred along the $Zr0_2/ZrN_x$ interface.

The band structure and electrical properties extracted from ZrN_x/GaN were comparable to the results extracted from the results on silicon. The increased 2DEG with respect to expected modulation doping effect, confirmed that ZrN_x had polarization effects similar to AlN. However, the electron carrier density formed along the ZrN_x/GaN interface was lower than the AlN, which suggested the polarization of the ZrN_x was weaker than AlN films. The measurements of the sheet resistance and 2DEG provided the channel mobility, Table 5.6. Based on the interface mobility, the films produced a high quality interface with the GaN.

Table 5.6: ZrN_x 2DEG Properties

GaN Doping	ZrN_x (nm)	R_{ZrN_x} (Ω/sqr)	N_{2DEG} $(10^{13}cm^{-2})$	μ_e (cm^2/Vs)
N^+	2.9	200 ± 25	2.37	1318 ± 100
N^-	2.9	3586 ± 200	0.12	1469 ± 100

Thickness Dependence

To evaluate the thickness dependence of the 2DEG and contact resistance of the Metal/ZrN_x/GaN, 1 nm films were grown on unintentionally doped GaN. The contacts were deposited with Pt and Al to compare the effect of workfunction with contact resistance. Through I-V and C-V measurements, the contact resistance and carrier density were extracted, shown in Table 5.7. The 2DEG of the 1 nm ZrN_x produced a lower 2DEG than the 3 nm film for both metal contacts. However, the contact resistance of the Pt was an order of magnitude larger than the Al. The large workfunction difference between Pt and Al significantly effected the contact resistance on the ZrN_x/GaN, as expected.

Table 5.7: ZrN_x Contact Resistance Properties

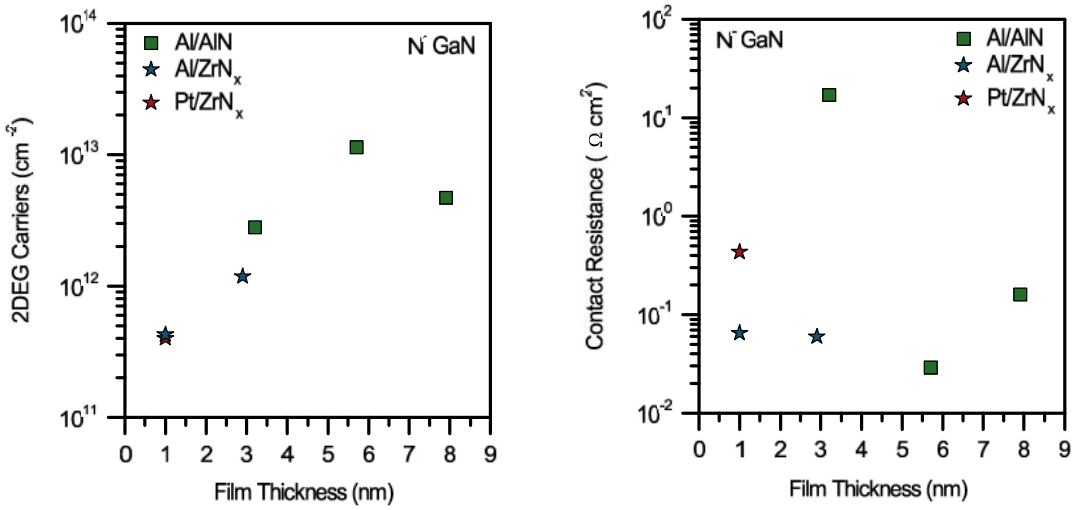
GaN Doping	ZrN_x (nm)	Metal Contact	N_{2DEG} $(10^{13}cm^{-2})$	R_c (Ωcm^2)
N^-	1.0	Pt	0.04	$4.3x10^{-1}$
N^-	1.0	Al	0.04	$6.5x10^{-2}$
N^-	3.0	Al	0.12	$5.9x10^{-2}$
N^+	3.0	Al	2.37	$1.4x10^{-2}$

5.5.3 ZrN_x Summary

The ZrN_x films were characterized on p-type silicon and various doped GaN templates to extract multiple electrical properties of the semiconductor. The pN heterojunction formed with silicon confirmed the properties obtained from the nN heterojunction on GaN. Through C-V characterization of the ZrN_x films the dielectric constant, band-gap, intrinsic carrier concentration, conduction and valence band effective density of states, electron affinity, effective masses of holes and electrons were obtained electrically. The band-gap was determine as 1.7 ev with a dielectric semiconductor relative dielectric constant of 7.2. Based on the band-gap, the intrinsic carrier concentration was estimated in the range of $10^4 cm^{-3}$. Through electrical extraction the effective density of state were found to infer the effective electron mass ($m_e = 1.8$) and hole mass ($m_e = 0.85$). As the ZrN_x was grown on GaN templates the heterojunction produced a 2DEG along the GaN interface which confirmed the films had polarization properties similar to AlN. The ZrN_x films were able to produce ohmic contacts without the requirement of high temperature annealing.

5.6 AlN and ZrN_x Comparison

Through various film thicknesses, the 2DEG carrier density (Figure 5.19a) and contact resistance (Figure 5.19b) were compared for the purpose of the potential incorporation into a GaN MOSFET. As expected, the 2DEG was more dependent on film thickness for



(a) (b)

Figure 5.19: (a) 2DEG carriers density and (b) Contract resistance based on the film thickness of AlN and ZrN_x.

AlN compared to ZrN_x, which remained constant beyond 3 nm. Likewise, the 2DEG was independent of the contact metal for both the AlN and ZrN_x on unintentionally doped GaN. The contact resistance was independent based on film thickness for both nitride films. The lowest contact tunneling resistance was not the thinnest layer of AlN, which agreed with the ZrN_x. Conversely the ZrN_x was not depend on film thickness, however contact metal increased the resistance by an order of magnitude.

The contact resistance (Figure 5.20) of the AlN films were strongly dependent on the 2DEG within the quantum well, which confirmed direct tunneling was the mode of the conduction. Conversely, the low conduction band offset between ZrN_x and GaN produced a contact that was independent on the 2DEG. Thus, the contact resistance was strongly dependent on the Schottky barrier height that was formed along the metal/ZrN_x interface. Post-fabrication annealing of these films was shown to significantly reduce the contact resistance of the films. The annealing temperature and time was strongly dependent on the metal stack, which requires further investigation to improve the parasitic contact resistance in the device.

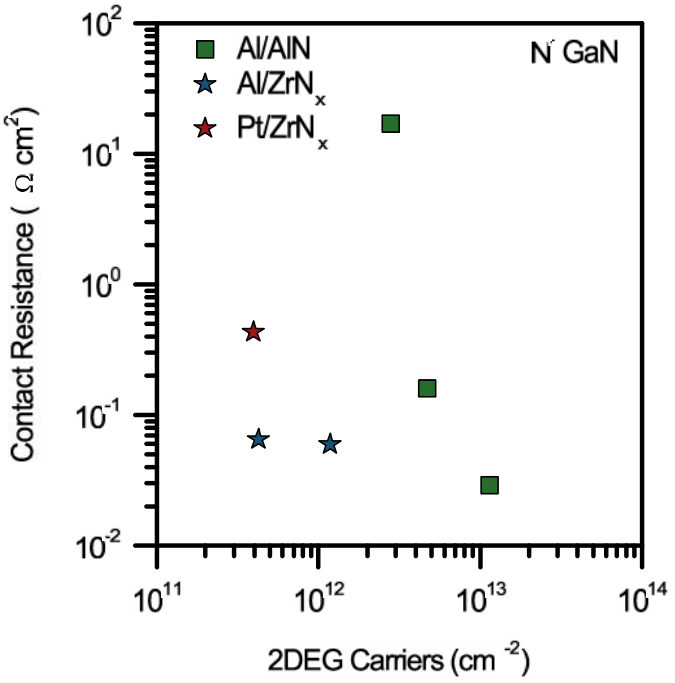


Figure 5.20: Contact resistance of the nitride films compared to the 2DEG formed along the GaN interface.

5.7 Nitride Reliability

The reliability of high voltage switching devices and consistent material stability within high electric fields and high temperatures is an ongoing issue [135–137]. The GaN based device has the potential to breakdown much earlier under high electric fields [138]. Conventional low electric field stress measurements have overestimated the true lifetime of the device before electrical degradation occurs. The materials must ensure consistent device operation under high electric fields, where the nominal device will be operating. Optimal reliability tests should examine the gate-source region, to inspect the effects of electrons traveling through a controlled and measurable high electric field. In this study, we examined the reliability of AlN, ZrN_x and ZrO_2 films incorporated in GaN MOSHCAPs, Figure 5.3 , under high electric fields.

The devices were exposed to gate-injected current which was ramped with respect to time, shown in Figure 5.21 As the current was injected through the gate, the voltage was monitored to inspect potential breakdown of the device. This method has been commonly used to evaluate the channel interface for MOS devices. Capacitance-voltage measurements, shown in Figure 5.22, were obtained after each gate current injection step to track the shift of the flat-band voltage. The sensitivity of the flat-band voltage due to defects accurately

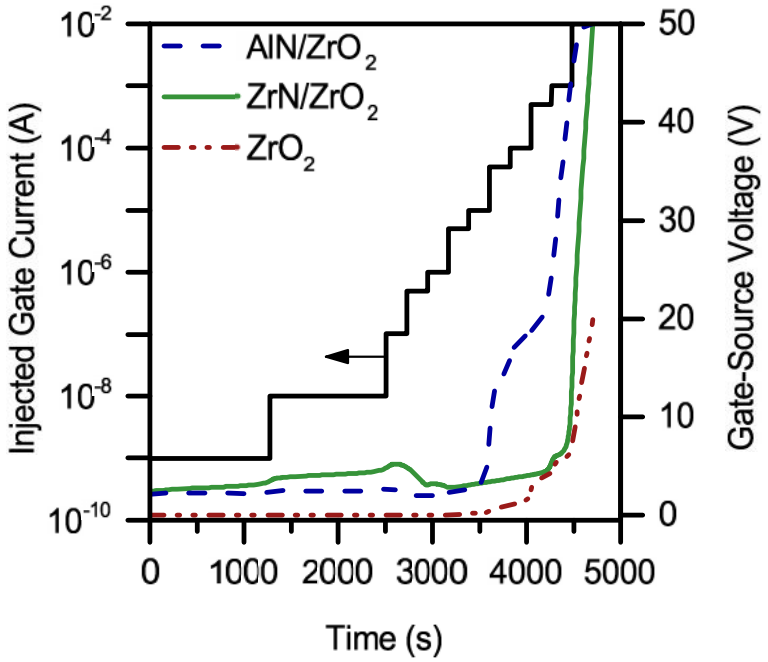


Figure 5.21: Measured gate voltage based on injected gate current for different MOS GaN devices. The voltage increased as the materials in the device failed due to defects produced within the films.

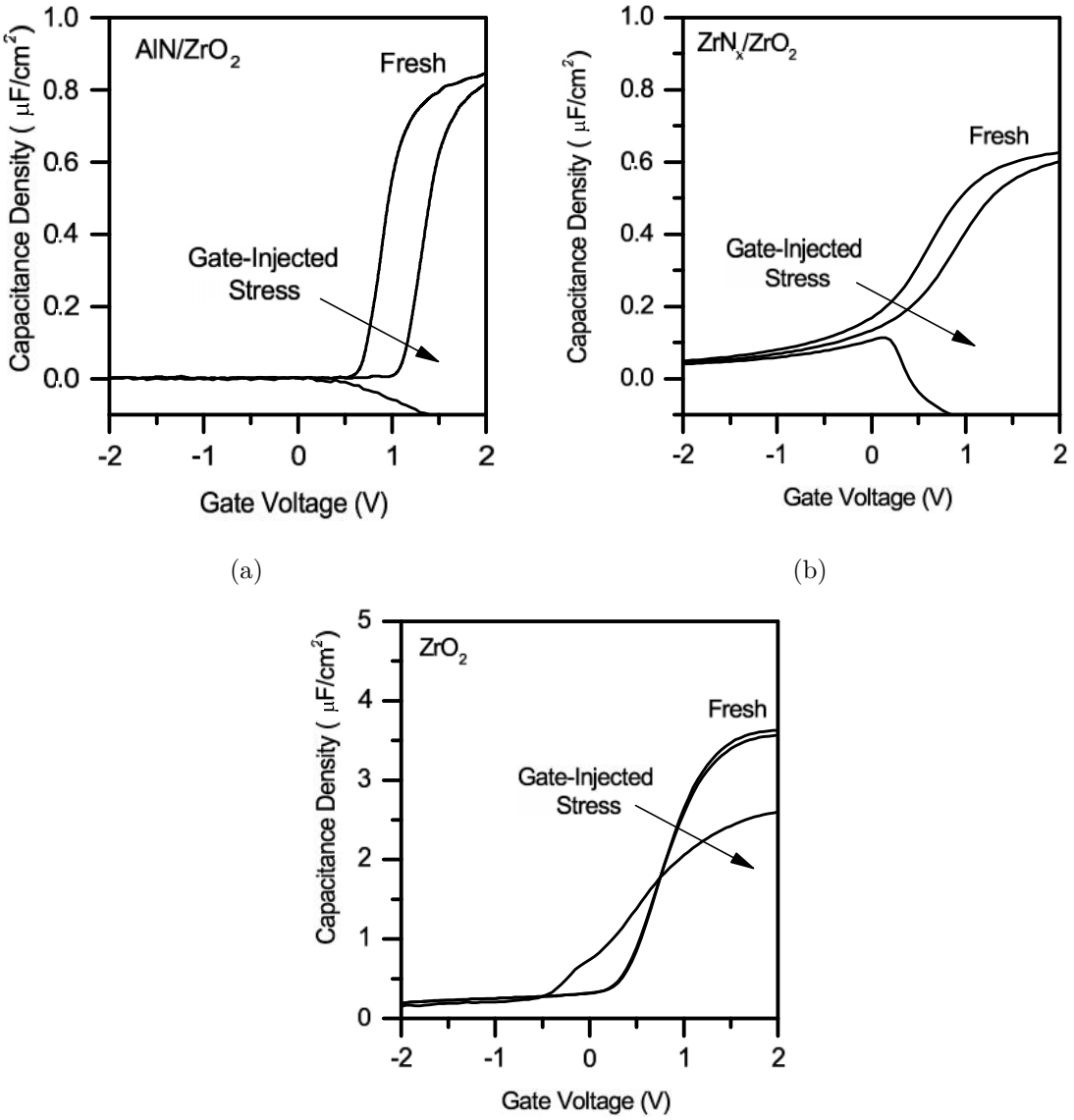


Figure 5.22: Capacitance-voltage measurements (100 kHz) for (a) AlN/ZrO_2 (b) ZrN_x/ZrO_2 and (c) ZrO_2 were shifted as breakdown occurred due to electron induced defects within the films.

allowed the ability to track the failure after stressing the device. Multiple frequency measurements (5 kHz - 1 MHz) were used to confirm the flat-band voltage of each device [14]. The flat-band voltage shift was due to the induced defects formed along the interface of the films as electrons were injected through the gate and source dielectric stack [16].

The time dependent current injection measurements were used to track the number of electrons that were sent through the gate films (Figure 5.23). The shift in the capacitance-voltage measurements allowed for the comparison of flat-band voltage with the number of

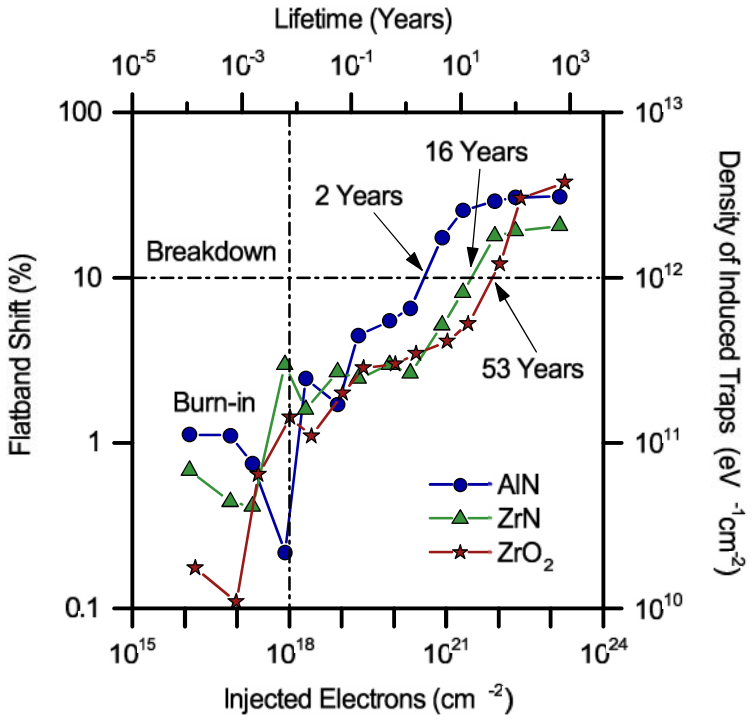
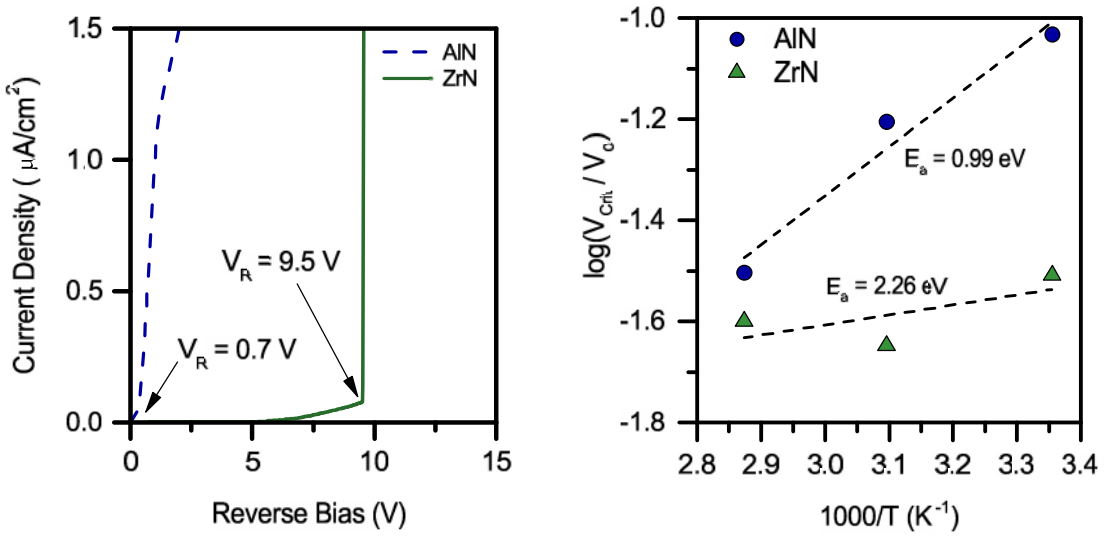


Figure 5.23: Flat-band voltage shift and the associated traps within the film caused from electrons injected through the gate. Lifetime of the devices based on worst case scenario of 10 $\mu A/mm$ gate leakage. The lifetime ratio remains constant regardless of the leakage current; i.e. The AlN film degraded 8x faster than the ZrN_x film.

electrons that traveled through the films. Initial fluctuations of the flat-band voltage shift was expected and commonly known as the burn-in effect of the device. Typically hydrogen and mobile ions within the film cause fluctuations until removed through soft biasing (low gate current injection). The induced trap densities within the films were obtained through the shift of the ΔV_{FB} [139].

Breakdown was considered to occur once the flat-band voltage of the device migrated 10% from the initial measurement. The lifetime of the devices, shown in Figure 5.23, were based on a constant leakage current traveling through the material over the lifetime of the device. A worst case gate leakage of 10 $\mu A/mm$ was assumed and determined that the AlN would fail after two years. However, at the same current density the ZrN_x and ZrO_2 films would maintain consistent operation for 8 and 25 times longer than AlN. We believe the large Zr atoms were able to withstand the electrical migration effects compared to the smaller and more mobile Al atoms.

The migration and defect effects were also portrayed through breakdown of the devices. Based on the breakdown voltage, shown in Figure 5.24a, we were able to extract the critical electric field of the films. The AlN films were consistent with literature and withstood electric fields up to 2 MV/cm [140, 141]. Conversely, the ZrN_x films maintained electric



(a) (b)

Figure 5.24: (a) Reverse breakdown characteristics of the AlN and ZrN_x films to extract the materials critical electric field at 25^oC. (b) The materials reverse breakdown based on temperature. Based on the temperature dependence, the ZrN_x was more stable compared to the AlN.

fields beyond 20 MV/cm. The large critical electric field again demonstrated that ZrN_x has the capability of operating within high power devices to improve the overall reliability. We believe this is the first reported critical electric field of an ultra-thin ZrN_x film incorporated within a GaN based device. As the temperature was increased, the voltage required to break the film decreased accordingly. This relationship between critical breakdown and temperature was used to extract the breakdown activation energy of the films [138]. The activation energy represented the films breakdown behavior during higher temperature operation (Figure 5.24b). The activation energy associated with temperature of the AlN films on GaN was consistent with other reported values [136]. In addition, we found that the activation energy of the ZrN_x was nearly 2 times improved over the AlN based device which provides reliability at higher operating temperatures.

Based on the gate injection stress technique the degradation of the films occurred at different rates. The AlN film was found to be more susceptible to failure than both ZrN_x and ZrO_2 films. Through reliability projection techniques, the ZrN_x and ZrO_2 based films provide 8x and 25x lifetime improvements over the AlN based device. Furthermore, the critical voltage of the AlN was determined to be more sensitive to temperature than ZrN_x. The integration of novel films, such as ZrN_x and ZrO_2, has the potential to improve the overall reliability of GaN based devices for high power applications.

5.8 Summary

The goal of the source/drain regions within a GaN MOSFET is to provide high carriers to the channel and reduce the contact resistance. Low temperature PEALD AlN and ZrN_x were examined for the potential use along the source and drain. Electrical measurements confirmed that both of the nitride based films had polarizing behavior, which produced a 2DEG along the GaN interface. Examining the reliability of the nitride films, provided a strong insight into the use of both films within the MOSFET. The less stable, high 2DEG AlN films have the potential for use along the lower electric field portions of the device. These regions are typically beneath the contacts, assuming near ideal ohmic contacts are achieved. Furthermore, the region between the source and gate has shown to have lower electric field strengths compared to the drain region. The ZrN_x films have the potential to provide 2DEG carriers along the GaN interface, while able to provide high material stability during large electric fields.

The ultra-thin nitride films characterized have shown important properties required within the GaN MOSFET to reduce the contact resistance, provide carriers and device stability. Through the incorporation of both films within the device has to potential to advance the GaN MOSFET for high power electronics with improved device reliability.

Chapter 6

GaN MOSFET Fabrication and Characterization

6.1 Introduction

The previous sections examined the potential of low temperature PEALD films to replace high temperature processing for GaN MOSFETs. The electrical characteristics of low temperature grown ZrO_2 and HfO_2 gate dielectrics demonstrated significant improvement over current technology and recent literature. Likewise, PEALD AlN and ZrN_x films were capable of supplying large carrier densities along the GaN interface without the complexity of selective area growth and ion implantation. This chapter presents a demonstration of a novel GaN MOSFET fabricated with ultra-thin PEALD films. The ZrO_2 film was used based on the extracted dielectric characteristics determined in Chapter 4. The ZrO_2 on GaN improved the interface traps, dielectric constant and channel mobility compared to the HfO_2. The selectively grown AlN films were used for the source and drain region to provide electrons to the channel. The following sections described the techniques and processes used to fabricate the GaN MOSFET with low temperature PEALD films. The GaN MOSFET was characterized through electrical current and capacitance measurements based on gate and drain voltages. The GaN MOSFET has a legitimate attempt to dominate the power electronic market with the incorporation of novel films and fabrication techniques.

6.2 Device Fabrication

In this section, the process flow and methods used during each fabrication step were described with the corresponding schematic of the films following each fabrication step. Devices were fabricated on two types of GaN-on-sapphire templates; Si-doped and uninten-

tionally doped GaN. The majority of the device regions were sub-10nm films deposited with a novel low temperature atomic layer deposition technique. The major advantage that PEALD grown films have over other techniques are the atomically consistent film thickness and large scale consistency across the entire wafer. This provided a negligible variation between similar designed devices on the wafer.

Alignment Marks

The GaN template and the PEALD films for the gate, source and drain regions were transparent which made layer to layer alignment impossible. To overcome this issue metal alignment marks (Figure 6.1) were deposited across the wafer to ensure each layer was aligned on top of the previous layer correctly. A negative photoresist lift-off technique was used to prevent metal from being in contract where the active region of the devices were.

First photoresist was spun onto the template to produce a 1.3 μm film which was followed by a soft bake at 90^oC for 120 seconds. The photoresist film was exposed to 356 nm ultraviolet light through the mask for 3 seconds. The wafer was again baked for 90 seconds at 115^oC to activate the negative resist properties of the film. Following the second bake, which converted the resist from positive to negative, the template was exposed to UV light for 60 seconds and developed in AZ400K developer for 35 secs. A thin layer (20 nm) of titanium tungsten (TiW) was sputtered on the wafer. The metal of choice for this step was irreverent other than the stickiness to the GaN and a large melting point to withstand various annealing steps. Following the metal deposition, the template was soaked in acetone to remove the resist along with the unwanted metal film. The alignment marks on the mask were designed to ensure the largest misalignment of a device was sub-micro (< 1 μm).

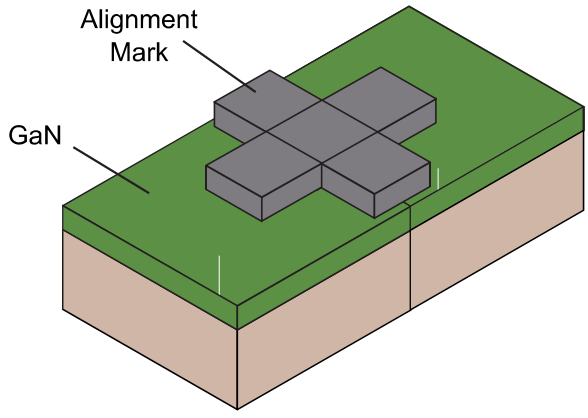


Figure 6.1: Alignment marks were placed on the GaN template to align future layers.

Source and Drain Regions

The first film of the device grown on the template was the AlN films along the source and drain region, shown in Figure 6.2. Again, the negative photoresist lift-off technique was used to pattern the regions where AlN would be deposited. The AlN film was deposited with the same technique discussed in Chapter 5. The photoresist and unwanted AlN was removed with acetone which was significantly easier than attempting to control the etching of ultra-thin AlN.

During the growth of the AlN, the photoresist was near the maximum suggested temperature use before potential re-flow began. This resulted in the photoresist adhering to the template compared to room temperature depositions. Following the growth of the film, the templates were submerged into acetone for 10 min with ultrasonic vibrations to ensure all of the resist was removed.

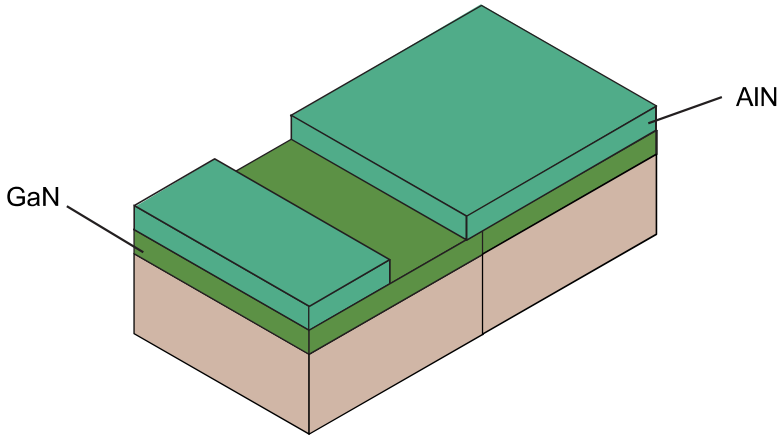


Figure 6.2: The negative photoresist lift-off technique defined the source and drain regions where the ultra-thin ALN films was deposited. The gate region was protected with photoresist to ensure volatile Al atoms did not disturb the GaN interface.

Gate Dielectric

The gate dielectric was defined in the same fashion as the source and drain regions. The negative photoresist lift-off techniques provided a quick process to produce the selective deposition of ultra-thin ZrO_2 films. As mentioned earlier, the 40 cycle PEALD ZrO_2 film was used as the gate dielectric for the GaN MOSFET. This films was used to reduce the leakage current and improve the control of the channel. The advantage of using the ZrO_2 film was that the peak capacitance density of the film was above 2 $\mu F/cm^2$ and the D_{it} was on the order of 10^{10} $eV^{-1}cm^{-2}$. In addition the film was able to handle a maximum gate voltage of 4 V.

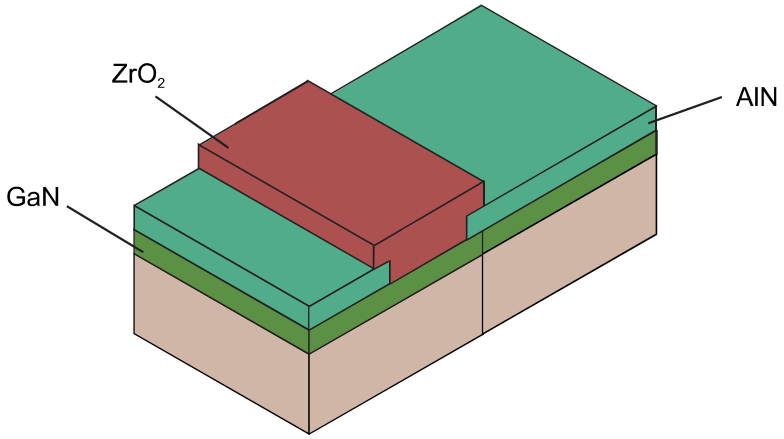


Figure 6.3: The regions for the ZrO_2 gate dielectric were defined with same negative photoresist process that defined the source and drain regions. The ZrO_2 overlapped the ALN along the source and drain to ensure the gate metal would not come into contact with AlN.

The growth of the gate dielectric was grown at 100^oC reducing the adhesion of the photoresist to the GaN template. This reduced the time length of the templates required in the acetone to lift-off the film. Furthermore, the ultrasonic vibrations were not required to remove the unwanted photoresist.

Metalization

With all of the PEALD films selectively deposited in the specific regions, the gate, source and drain contact metals (Figure 6.4) were defined with negative photoresist for metal lift-off. Again the lift-off technique provided a quick and efficient method to define the contacts without the use of chemical etching. The major advantage of using a single mask for the source, gate and drain was the self-aligned gate process. Regardless of the misalignment between the layers the contacts were consistently the designed distance apart. This provided more consistent device characteristics, however the optimal source/drain contact was not necessarily the ideal gate metal and vise versa.

SiN_x Encapsulation

During the encapsulation fabrication step of the device, the SiN_x was deposited by PECVD at 300^{o}C for 15 minutes. The purpose of this step was to protect the device from contaminates on the surface, as well as allowing for isolated contact pads for testing. Growing the film at a higher temperature was intended to simultaneously active the gate dielectric. The gate dielectric annealing typically removes unwanted mobile ions within the film along with

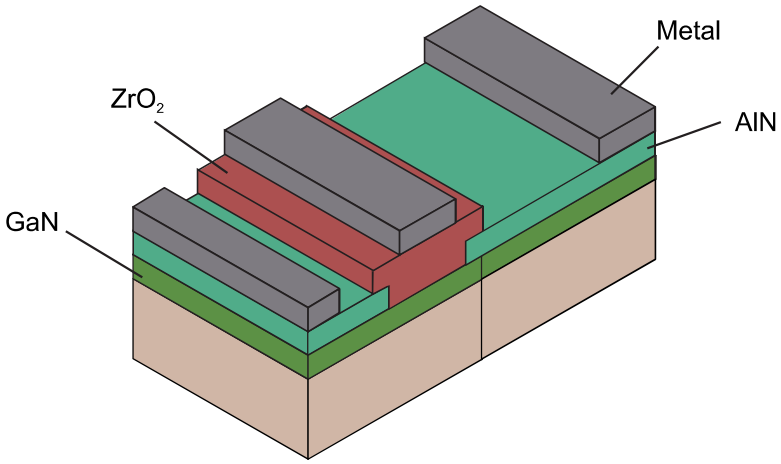


Figure 6.4: The source, drain and gate contacts were all deposited at the same time to reduce the fabrication steps of the device.

reducing interface defects which lead to threshold voltage shifts. Furthermore, the improvement of the relative dielectric constant of the gate dielectric was demonstrated through post fabrication annealing [142, 143]. This in turn will improve the potential current density and channel mobility of the MOSFET.

6.3 Device Characterization

The GaN MOSFETs were fabricated with the process described above to compare the material properties behavior within a fully fabricated device. Most notably, the behavior based on the doping concentration of the GaN templates were examined in attempt to reduce the substrate leakage and ensure enhancement-mode behavior. The metalization layer (Cr and Al) was examined to determine the quality of the depletion effect under the channel based on the doping. The $100\mu m$ x $100\mu m$ GaN MOSFET devices, shown in Figure 6.5, were characterized to ensure the contact resistance was minimized by the large source and drain contacts pads. To characterize the GaN MOSFET FatFETs, conventional current-voltage and capacitance-voltage measurements were obtained with the Keithley 4200-SCS. The GaN MOSFET device characteristics were organized into two sections; one which examined the on-state regime of the device while the other examined the transistors off-state and breakdown voltage. To evaluate the on-state portion of the transistor the threshold voltage, sub-threshold slope, density of interface traps, peak current density and electron field effect mobility were examined. The threshold voltage of the MOSFET provided the information regarding the transistor operation; i.e. normally-on or normally-off. Furthermore, the sub-threshold slope, D_{it} and channel mobility were used to determine the quality of the metal/dielectric and GaN interface.

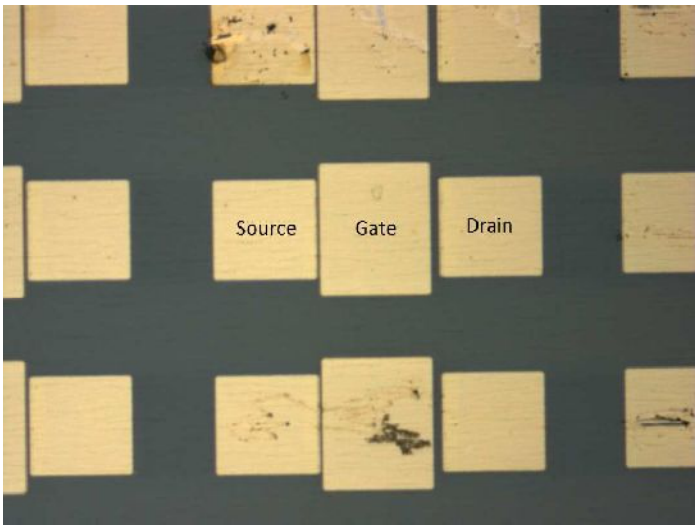


Figure 6.5: Confocal image of the 100μm x 100μm FatFETs used to evaluate the quality of the GaN MOSFET fabricated with the ultra-thin PEALD films. The gate was extended 10 μm beyond the width of the source and drain to reduce the substrate leakage current.

6.3.1 GaN MOSFET Operation

The on-state operation of the GaN MOSFETs were examined with respect to different materials incorporated within the devices. The background doping, gate metal and device dimensions were adjusted to determine the effects for the potential use in power electronics. Furthermore, the intrinsic transconductance of the GaN MOSFET was extracted to determine the true potential of the device with commercially fabricated source and drain interconnect contacts. The devices were also exposed to post fabrication annealing to examine the effect of oxide degradation and contact resistance reduction.

Substrate Doping

The quality of the off-state has a strong dependence on the threshold voltage and substrate leakage current of the device. To produce an enhancement-mode MOSFET, the accumulation of carriers must be limited to gate voltages greater than zero. In addition, the substrate leakage of the device must be minimal to prevent conduction at a gate voltage of $V_{GS} = 0$ V. The leakage current was based on the depletion width of the channel which was strongly dependent on the doping concentration of the GaN, shown in Figure 6.6. FatFET GaN MOSFETs were examined to determine the threshold voltage and off-state leakage current of the devices based on the background doping of the GaN templates.

Capacitance-voltage measurements, shown in Figure 6.7, confirmed the accumulation of electron were consistent with the doping of the templates, $V_{acc} = 0.4$ V and $V_{acc} = 1.3$ V for

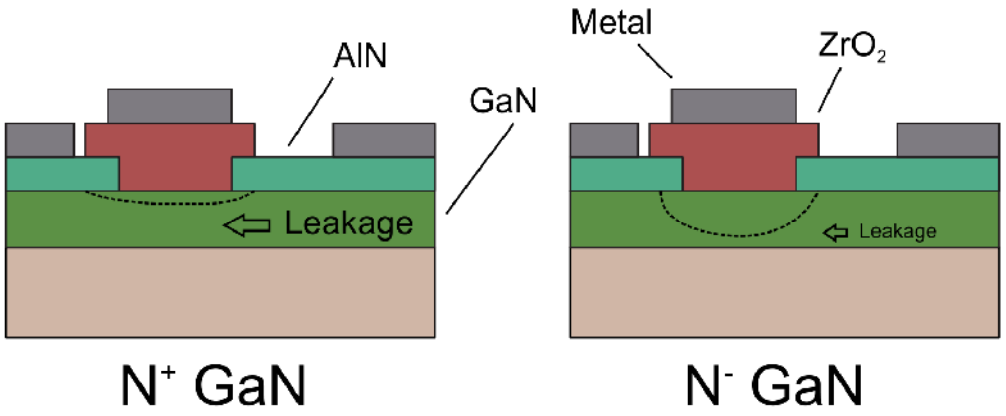
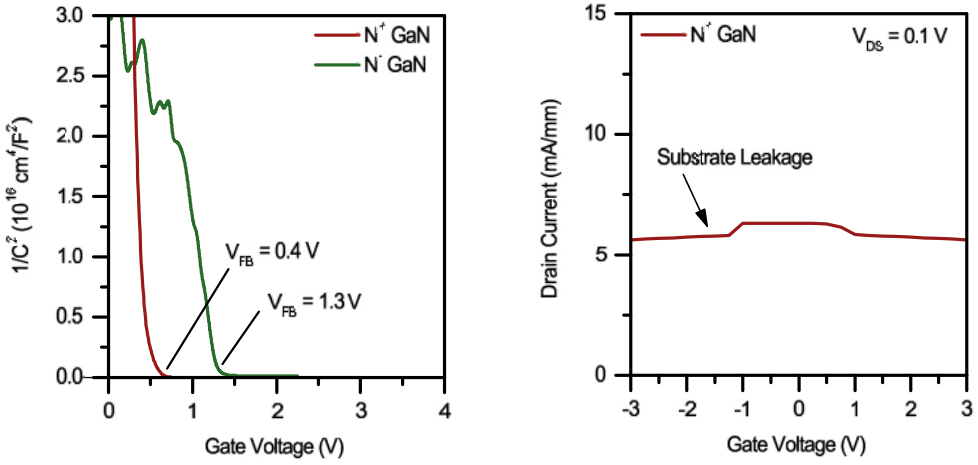


Figure 6.6: A representation of the leakage current under the channel based dependence on the depletion width (dashed region). The lower doped GaN produced a larger depleted channel which was expected to create a lower leakage current.

N^+ GaN and N^- GaN, respectively. Based solely on the extracted accumulation voltage of the MOS channels would suggest that both substrates would produce enhancement-mode MOSFETs. However, based on the transfer characteristics of the GaN MOSFET, shown in Figure 6.7b, the N^+ GaN was unable turn-off the device and control the channel. The N^+ GaN template was unable to control the substrate leakage current, due to the low resistivity ($< 0.05\ \Omega$ cm) of the GaN template. While the device was off ($V_{GS} < 0$ V), the current would flow around the depleted gate region. The depletion width discussed in Chapter 2



(a) (b)

Figure 6.7: (a) The inverse squared capacitance with respect to gate voltage for the N^+ GaN (red) and N^- GaN (green). The x-axis intercept was used to extract the accumulation voltage of the channel MOS. (b) The drain current (red) at $V_{DS} = 0.1$ V for N^+ GaN with respect to gate voltage.

required less than 50 nm to ensure a fully depleted channel in the N^+ GaN. This confirmed the 4.3 μm N^+ GaN was not suitable to produce an enhancement-mode GaN MOSFET. Conversely, the resistive N^- template was able to significantly reduce the substrate leakage current during the off state of the device.

The reduced off-state current, allowed for the enhancement-mode behavior of the MOSFET (Figure 6.8) to be achieved with a positive gate bias. The extracted doping concentration (1.4x10^{14} cm^{-3}) obtained from the slope of the $1/C^2 - V$ suggested the chromium gate would produce a depleted channel depth of 2.9 μm. The partially depleted channel depth was close to the range of the N^- GaN template thickness 5 +/- 1.5 μm. However, the leakage current was a result of the gate unable to fully deplete the GaN under the channel .

The drain saturation voltage, $V_{D_{sat}}$, of long channel devices (6.1) can be approximated for a MOSFET architecture. The family of curves (Figure 6.8a) and the MOSFET transfer curves (Figure 6.8b) were used to determine the threshold voltage of the MOSFET. The threshold voltage obtained from the drain saturation voltage was estimated as 1.4 +/- 0.1 V and consistent to the x-axis intercept obtained from the transfer curve (1.35 V). The GaN MOSFET further confirmed enhancement-mode operation as the drain current increased with positive gate bias. The on-resistance (6.2) was extracted from the linear regime of family of curves during on-state operation at $V_{GS} = 3$ V. The specific on-resistance was determined as 32.9 $\Omega \cdot cm^2$. This was roughly 10^3x larger than current technology, which was

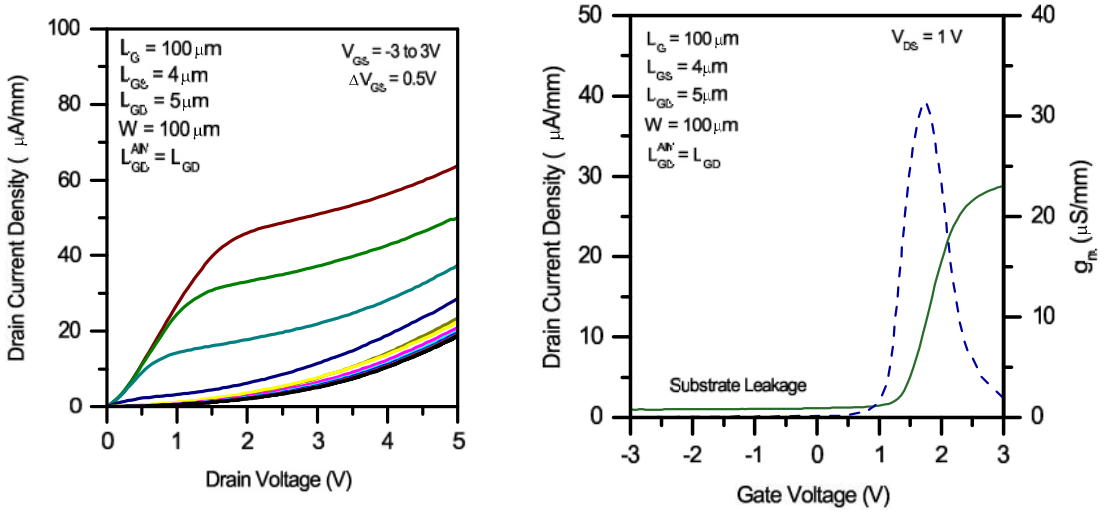


Figure 6.8: (a) The family of curves for the N^- GaN MOSFET. The drain saturation voltage of the MOSFET was consistent with conventional MOSFET models where $V_{D_{sat}} = V_{GS} - V_t$. (b) The drain current (green solid) and transconductance (blue dashed) at $V_{DS} = 1$ V for N^- GaN with respect to gate voltage. The device demonstrated enhancement-mode operation, with a turn-on voltage of 1.35 V.

a result of the large parasitic resistances at the source and drain interconnects. Through optimized metalization the on-resistance of the device would be managed to a value more comparable to literature.

$$V_{D_{sat}} = V_{GS} - V_{th} \tag{6.1}$$

$$R_{on} = R_{tot} \cdot W \cdot (L_G + L_{GS} + L_{GD}) \tag{6.2}$$

Gate Metal Stack

It is well known that the threshold voltage strictly dictates the required gate voltage for the MOSFET transistor to be considered on and off. The ability to adjust the threshold voltage is important for design purposes of the transistors behavior. Depending on the device application, the precision of the threshold voltage can be crucial. For power electronics, the ability to ensure a positive and consistent threshold voltage with respect to devices across a wafer is important. The threshold voltage (6.3) can be designed based on the metal-semiconductor workfunction difference (Φ_{ms}), the interface traps (Q_{it}), depletion charge (Q_{Dep}), gate dielectric (C_{ox}) and the surface potential ($2\phi_F$). The interface traps are conventionally minimized to reduce the interface traps becoming an issue. Furthermore, the depletion and surface potential and capacitance density are typically predetermined as the semiconductors background doping and gate oxide are known. The most simplistic method to control the threshold voltage of the transistor was through an adjustment the gate metal workfunction.

$$V_{th} = \Phi_{ms} - \frac{Q_{it}}{C_{ox}} - \frac{Q_{Dep}}{C_{ox}} - 2\phi_F \tag{6.3}$$

The gate metal workfunction strongly dictated the depletion depth beneath the channel. For example, a Al gate metal was expected to deplete only 1.7 μm, whereas a Cr gate metal depleted nearly twice as much 2.9 μm. Based on the depletion depth, the Cr metal was expected to produce a larger turn-on voltage compared to the Al gate. The MOSFETs turn-on voltage (threshold voltage) was determined from the transfer curves; the gate voltage (V_{GS}) was swept from -3 V to 3 V while the drain voltage (V_{DS}) was held constant at 1 V. The drain current and transconductance was measured with respect to the gate voltage, shown in Figure 6.9. The difference in workfunction of the metals from Al to Cr shifted the

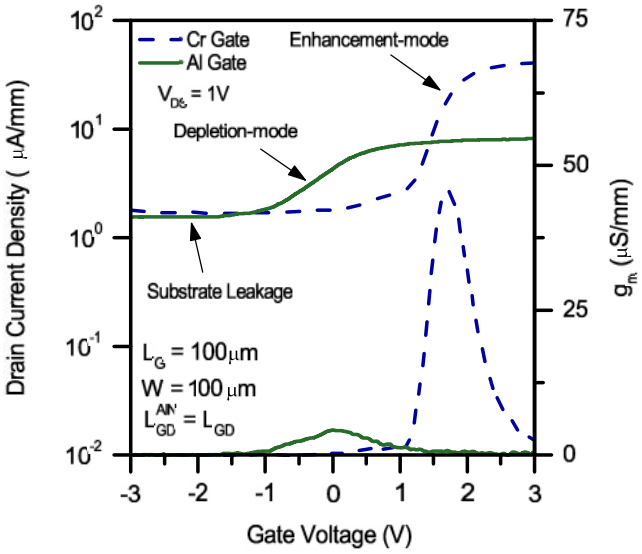


Figure 6.9: The transfer and transconductance characteristics of the GaN MOSFET had a strong dependence with the work function of the gate metal. When the gate metal was exchanged from Al (Ψ_{Al} = 4.2 eV) to Cr (Ψ_{Cr} = 4.7 eV) the MOSFET characteristics shifted from normally-on (V_t = -0.25 V) to normally-off (V_t = 1.3 V). The enhancement-mode MOSFET improved current density (2x) and transconductance (5x) over the Al gate device.

GaN MOSFET behavior from a depletion-mode transistor to an enhancement-mode device, respectively.

The enhancement-mode transistor produced a device turn-on voltage of 1.3 V, whereas the Al gate required a negative gate voltage to turn the device off. Furthermore, the Cr gate allowed for the MOSFET to produce a larger peak current density compared to the depletion-mode Al gate device, which was also confirmed from the transconductance. As expected, the larger transconductance MOSFET produced the larger peak current density. Furthermore, the substrate leakage current in the reverse gate bias was equivalent. Larger drain biases on the N^- GaN templates allowed current to conduct around the gate depletion region. However, the reduced peak current density agreed with a depletion-mode device and a potential indication of an undesirable interface defects caused from gate metal.

To confirm the channel interface quality, the sub-threshold slope of the MOSFETs were extracted at low drain biases (V_{DS} = 0.2 V). The sub-threshold slope (6.4) of the devices were extracted from the transfer curves during the transistors off-state. The inverse slope of the logarithmic drain current with respect to gate voltage is an excellent method of determining the quality of the gate dielectric interface [144, 145]. The sub-threshold slope (S), shown in Figure 6.10, confirmed the Al gate degraded the dielectric interface compared to Cr metal. The Cr gate produced a sub-threshold slope of 123 mV/dec which was 7x lower

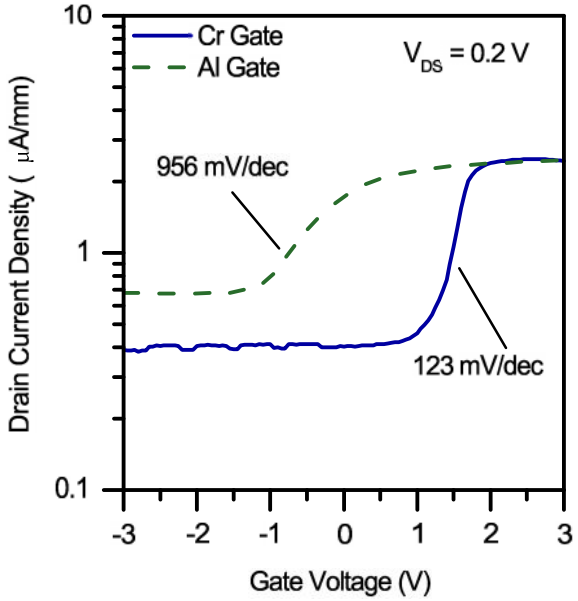


Figure 6.10: The sub-threshold slopes of the GaN MOSFETs were extracted from the low transverse electric field transfer characteristics for the Al (Green) and Cr (Blue) gate metals. The enhancement-mode GaN MOSFET produced a sharper sub-threshold slope compared to the depletion-mode transistor.

than the Al device (956 mV/dec). This was an indication that the channel of the Al device was degraded from the 300^oC SiN encapsulation process. Furthermore, the sub-threshold drain leakage current was 3x lower for the Cr gate compared to the Al gate. Again, the smaller depletion width caused leakage issues for the Al gate devices.

$$\frac{1}{S} = \frac{d}{dV_{GS}} log(I_D) \tag{6.4}$$

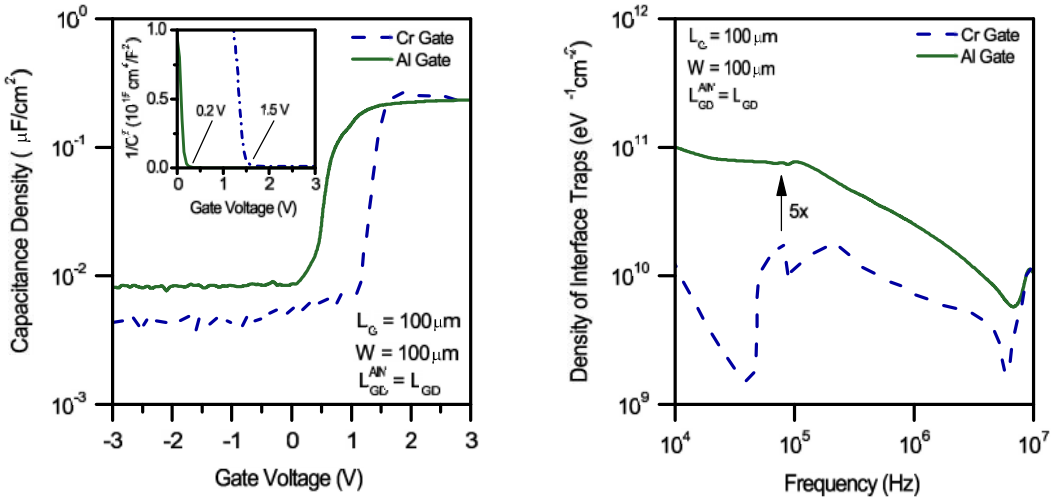
The sub-threshold slope (6.5) was approximated by the differential capacitance of the depletion (C_{Dep}), the interface traps (C_{it}) and the dielectric capacitance (C_{ox}) [14,16]. The sub-threshold slope (6.6) was further expanded to only have the density on interface traps as an unknown variable. Rearranging the expression provided an insight into the density of interface traps (6.7) along the channel. Based on the sub-threshold slope of the GaN MOSFETs, the extracted D_{it} for Cr and Al were $2.5\text{x}10^{11} cm^{-2} eV^{-1}$ and $4.8\text{x}10^{12} cm^{-2} eV^{-1}$, respectively. The extracted D_{it} from the sub-threshold slope has been shown as a method of comparison between devices, however the conductance frequency measurements are a more accurate method for extracting the interface trap density.

$$S = \frac{kT}{q} ln(10) \left[1 + \frac{C_{Dep} + C_{it}}{C_{ox}} \right] \tag{6.5}$$

$$S = \frac{kT}{q \log(e)} \left[1 + \frac{qD_{it} + \left(\frac{qN_A \epsilon_s}{3\phi_F - 2\frac{kT}{q}} \right)^{1/2}}{C_{ox}} \right] \tag{6.6}$$

$$qD_{it} = C_{ox} \left(\frac{qS \log(e)}{kT} - 1 \right) - \left(\frac{qN_A \epsilon_s}{3\phi_F - 2\frac{kT}{q}} \right)^{1/2} \tag{6.7}$$

Capacitance-voltage measurements, shown in Figure 6.11a, were used to confirm the transistor characteristics of the gate metals. The capacitance with respect to gate voltage was used to determine the flatband voltage beneath the channel. These values were comparable to the extract turn-on voltage of the MOSFETs based on the current-voltage measurements. Furthermore, the lower depletion capacitance Cr gate was able to reduce the number of carriers within the channel during the off-state of the device compared to the



(a) (b)

Figure 6.11: (a)The gate-source capacitance of the oxide was obtain at low frequency (50 kHz) to determine the peak capacitance density and extract the flat band voltage of the MOS stack, shown in the inset. During reverse gate bias, the Cr metal was capable of depleting more charge from under the gate compared to the Al gate stack. (b) The density of interface traps were obtained from the conductance frequency spectrum. The Al/ZrO_2 gate stack degraded the interface, which produced a 5x more traps compared to the Cr metal.

Al gate metal. This confirmed that the larger workfunction metal was able to depleted the channel most effectively. The conductance frequency spectrum was used to extract the density of interface traps along the channel through the conductance frequency spectrum [16]. The conductance method, shown in Figure 6.11b, and sub-threshold slope confirmed the Al degraded the channel an device characteristics compared to the Cr gate metal. The extracted density of interface traps confirmed the Al gate metal produced more defects (5x) along the GaN channel following the encapsulation of the devices.

The density of interface traps along the channel, shown in Table 6.1, were extracted from three different techniques; the sub-threshold slope, conductance dispersion and the C-V hysteresis. As expected, the techniques produced slightly different results based on the measurement used to extract the D_{it}. However the methods which included the AC signal was more consistent to the results discussed in Chapter 4. The sub-threshold D_{it} extraction was the least accurate for these transistors because of the excess substrate leakage around the depletion region. This slightly increased the overall D_{it} compared to the frequency dependent techniques. However, all of the extraction techniques confirmed that the Al gate metal diffused more readily through the gate dielectric which increased the density of interface traps compared to the Cr gate metal.

Table 6.1: The Extracted Density of Interface Traps

Extraction Technique	Al/ZrO_2/GaN ($cm^{-2}eV^{-1}$)	Cr/ZrO_2/GaN ($cm^{-2}eV^{-1}$)
Sub-threshold Swing	4.8x10^{12}	2.5x10^{11}
Conductance Dispersion	1.0x10^{11}	1.7x10^{10}
C-V Hysteresis	1.1x10^{11}	4.8x10^{10}

The design of the GaN MOSFET architecture utilized the simplicity of the gate metal workfunction to control the threshold voltage of the device. This was demonstrate through the modification of the gate metal workfunction from 4.2 eV to 4.7 eV by using Al and Cr, respectively. The Al gate metal produced a depletion-mode GaN MOSFET due to the MOS flatband voltage occurring at equilibrium ($V_{GS} \approx 0$ V). Conversely, the Cr metal depleted the MOS channel at equilibrium, which ensured the transistor was a normally-off enhancement-mode MOSFET. The sub-threshold slope and frequency dispersion confirmed the Cr gate metal stack reduced diffusion and interface traps along the channel during fabrication. The reverse voltage depletion capacitance confirmed that the Al was unable to removed the charge under the channel like the enhancement-mode transistor.

Channel Mobility Extraction

The extracted field effect channel mobility, has a strong dependence on the quality of the ohmic contacts and parasitic resistance along the source and drain. The parasitic resistances, depicted in Figure 6.12, have the potential to significantly reduce the true extracted electron mobility of the channel. The source parasitic resistance degrades the internal gate voltage between the actual source and gate of the transistor. The internal gate voltage (6.8) can be expressed by the voltage drops across the entire device and the unintentional source resistance. Furthermore, the internal drain voltage (6.9) was determined from the applied drain voltage and the resistance of the source and drain.

The internal transconductance (6.10) of the GaN MOSFET was extracted based on the variation of the drain current with respect to the internal gate voltage. This transconductance was more indicative to the true behavior of the MOSFET with optimized source and drain interconnects. Furthermore, the field effect mobility of the transistor based on the internal transconductance represents the MOSFET characteristics compared to the external parasitic results.

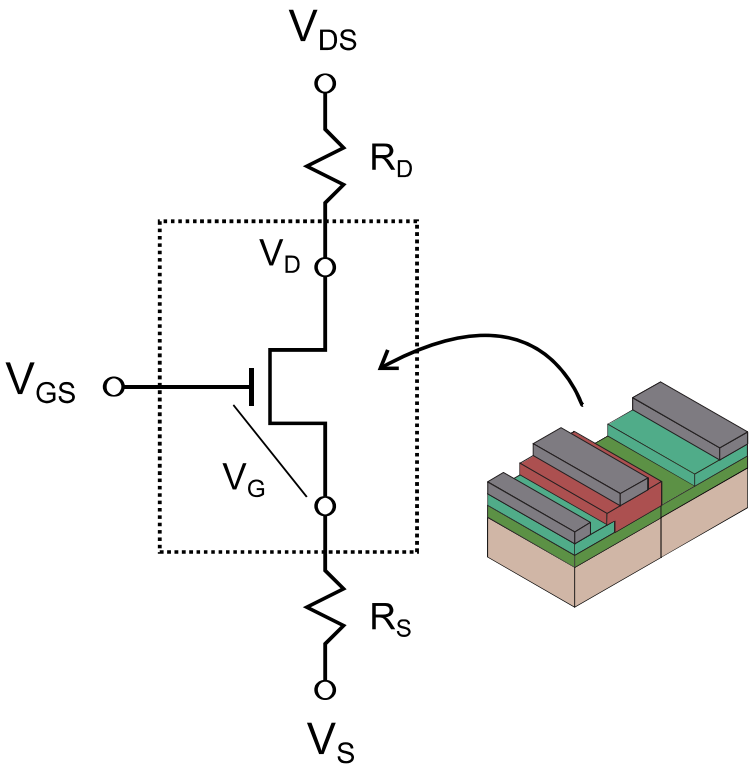


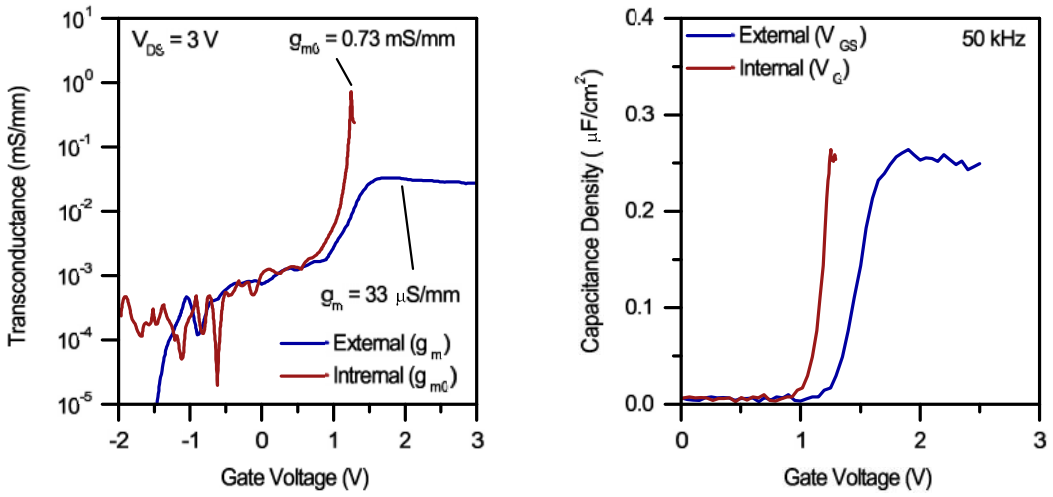
Figure 6.12: The internal voltage drops are dependent on the external voltage biases and parasitic resistances along the source and drain interconnects. The MOSFET only experienced the internal bias for the drain (V_D) and gate (V_G) based on the external gate and drain voltages.

$$V_G = V_{GS} - I_D R_S \tag{6.8}$$

$$V_D = V_{DS} - I_D \left(R_S + R_D\right) \tag{6.9}$$

$$g_{m0} = \frac{\partial I_D}{\partial V_G} \tag{6.10}$$

The interconnect parasitic resistance was obtained from TLM measurements discussed in Chapter 5. The additional resistance was roughly 6 orders of magnitude larger than conventional contacts incorporated in conventional GaN devices. This led to large voltage drops across the source and drain contact regions. Furthermore, the variation between the transconductance and internal transconductance, shown in Figure 6.13a, were very different. The extracted external transconductance (g_m) for the FatFET peaked at 33 $\mu S/mm$ due to the large resistance at the source contact. However, the intrinsic transconductance (g_{m0}) suggested that the GaN MOSFET could produced a transconductance of 0.73 mS/mm if the parasitics were minimized. The peak gate capacitance density was also limited because of the parasitic source resistance, shown in Figure 6.13b.



(a) (b)

Figure 6.13: (a) The external and internal transconductance of the 100 μm x 100 μm GaN MOSFET at V_D = 3 V. The peak intrinsic transconductance was 0.73 mS/mm. (b) The capacitance-voltage based on the external and internal gate voltage.

The external transconductance of the 100 μm x 100 μm GaN MOSFET was extremely promising as the peak transconductance was around 40 $\mu S/mm$. This was comparable to smaller channel GaN MOSFET devices with optimized contacts transconductance 12.5 $\mu S/mm$ ($L_G = 16\mu m$) and 7.5 $\mu S/mm$ ($L_G = 40\mu m$) at equivalent drain voltages [96]. The ratio between the transconductance and gate lengths of the devices (6.11) strongly implied that the ZrO_2 PEALD GaN MOSFET improved the combination of the capacitance density and channel mobility ($\mu_{eff}C_{ox}$). The ZrO_2 GaN MOSFET was compared to $L_G = 16\mu m$ and $L_G = 40\mu m$ GaN MOSFETs where $\mu_{eff}C_{ox}$ was improved by 25x and 16.7x, respectively. The measured capacitance ZrO_2 gate dielectric improved the C_{ox} over the SiO_2 gate dielectric by a factor of 5.7. This implied that the peak channel electron mobility was improved and surpassed 200 cm^2/Vs.

$$\frac{g_m L}{W} = \mu_{eff} C_{ox} \tag{6.11}$$

In addition, the GaN MOSFET intrinsic transconductance (0.73 mS/mm) was larger than a 200 μm GaN HFET (0.42 mS/mm) with reduced parasitic resistances [146]. The improved ZrO_2 gate dielectric interface GaN MOSFET intrinsic transconductance produced an equivalent value to an optimized 20 μm GaN MOSFET with SiO_2. The effective electron mobility (6.12) from the channel was extracted from the low drain voltage, drain current (I_{DS}). The gate length (L), width (W), charge density (Q_{tot}) were all known and obtained through confirmation of optical microscope or capacitance-voltage measurement.

$$\mu_{eff} = \frac{L}{W Q_{tot}} \frac{I_{DS}}{V_D} \tag{6.12}$$

The intrinsic extracted mobility, shown in Figure 6.14, produced a peak mobility of 480 cm^2/Vs whereas the parasitic resistance reduced the extracted mobility to 240 cm^2/Vs. This extracted channel mobility was equivalent with some of the leading GaN MOSFET channel mobilities [37, 147]. However, with a reduced source parasitic resistance the GaN MOSFET mobility has the ability to surpass literature. As expected, the improved transconductance was in-part due to the improved channel mobility of the ZrO_2/GaN gate dielectric. With the incorporation of the high quality ZrO_2 dielectric with improved source/drain metalization, the GaN MOSFET has a viable opportunity in the transistor industry.

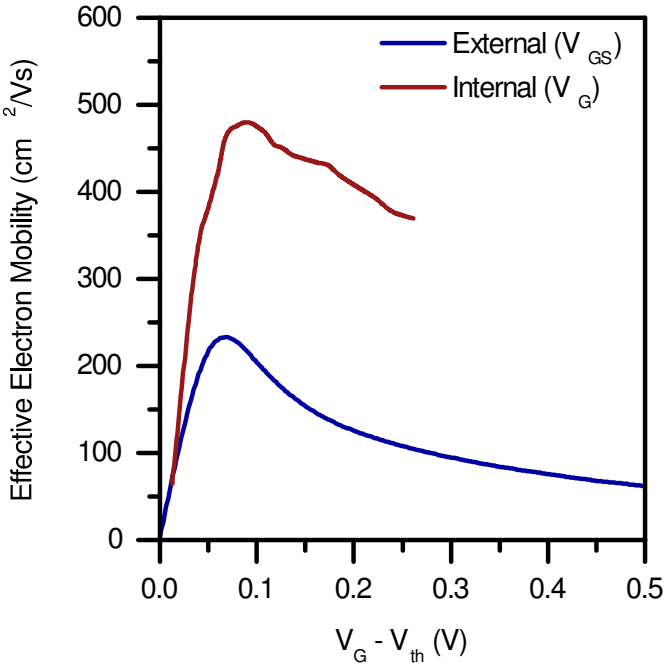
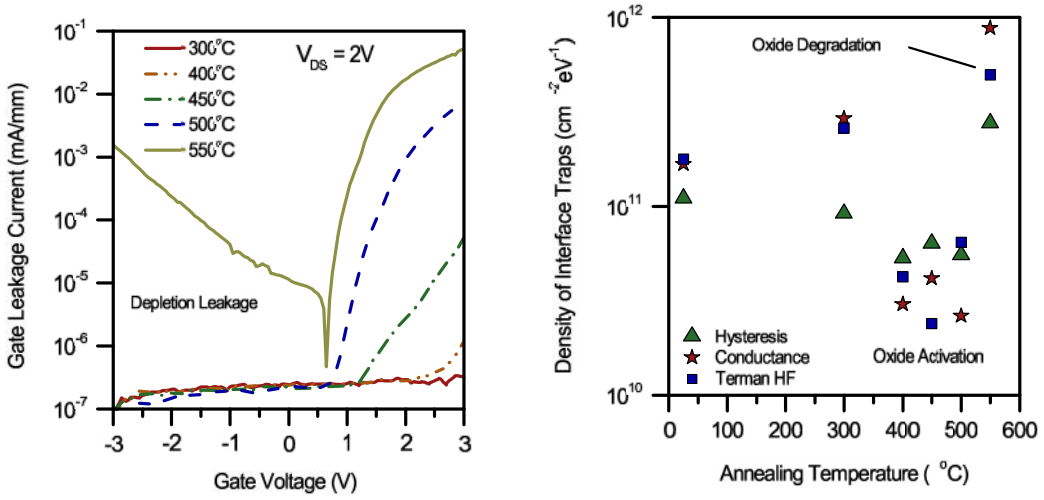


Figure 6.14: The effective electron mobility of the FatFET obtained at low drain bias. The mobility based on the external gate biases was determined to have a peak mobility of 230 cm^2/Vs Conversely, the peak electron mobility of the GaN MOSFET without parasitic resistance has the potential to reach 480 cm^2/Vs .

Post Fabrication Annealing

To reduce the parasitic resistances at the source and drain, the tunneling contacts were required to be significantly lower. The most simplistic and cost effective technique was achieved through a post fabrication anneal of the devices. The devices were annealed for 15 minutes at 400^oC, 450^oC, 500^oC and 550^oC in a nitrogen rich environment. Between each annealing temperature, the electrical characteristics of the devices were obtained to extract the threshold voltage, on-resistance, peak current density and peak transconductance from the family of curves and transfer curves.

As the annealing temperature was increased the gate leakage with respect to gate voltage, shown in Figure 6.15a, became significantly degraded. Beyond 500^oC the depletion gate leakage ($V_{GS} < 0$ V) was the first indication that severe dielectric degradation occurred. This was most likely due to the Cr atoms from the gate metal diffusing into the ZrO_2 gate dielectric. These metal atoms behave as conduction site within the film, which allow current to flow through the dielectric more readily. The extracted density of interface traps with respect to annealing temperature, shown in Figure 6.15b, used the conductance extraction,



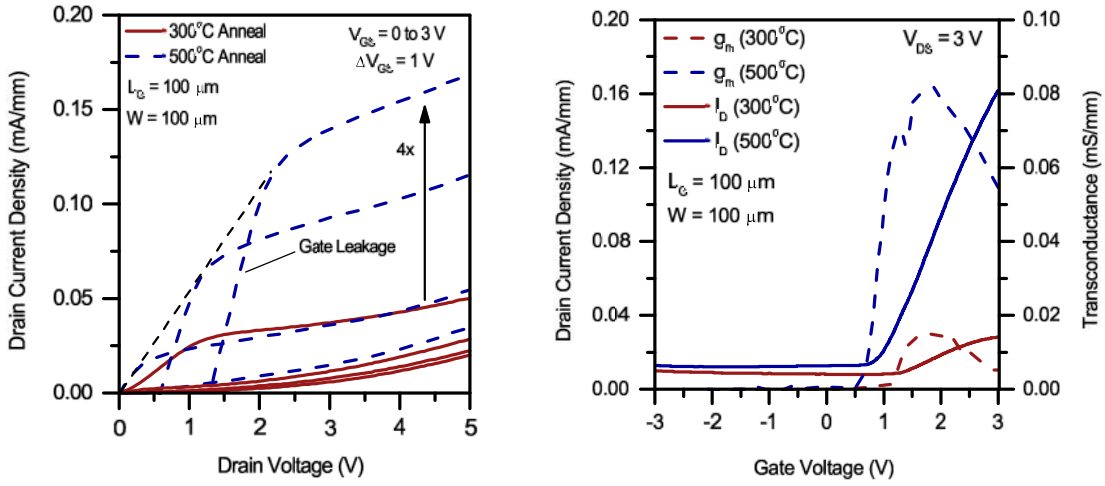
(a) (b)

Figure 6.15: (a) The gate leakage current of the FatFET as the gate voltage was swept from reverse to forward bias. Higher annealing temperatures increased the conduction leakage through the dielectric. (b) The extracted density of interface traps based on annealing temperature. The gate oxide was electrically activated between 400^oC and 500^oC before the gate dielectric was critically degraded.

low frequency hysteresis and high frequency Terman shift to evaluate the degradation of the gate dielectric. The activation temperature of the Cr/ZrO_2/GaN MOS stack was found to be within the range of 400^oC and 500^oC. Within this range the D_{it} and the reverse bias gate leakage was minimized before gate dielectric degradation.

The diffusion through the gate dielectric was a good indication that the Cr was able to diffuse through the AlN to improve the contact resistance. This was confirmed through the family of curves, shown in Figure 6.16a, which improved the peak drain saturation current density. The low drain voltage produced high gate leakage, however smaller devices and contact annealing would have reduced this effect. At the peak gate voltage (V_{GS} = 3 V) the drain saturation current density was increased from 0.04 mA/mm to 0.17 mA/mm as the annealing temp went from 300^oC to 500^oC. The 4x agreed with the expected reduction of the contact resistance, discussed in Chapter 5. Furthermore, the normalized on-resistance obtained from the linear region of the family of curves produced an non-annealed on-resistance of 32.9 $\Omega\ cm^2$, whereas the 500^oC annealed devices were able to reduce the on-resistance to 10.6 $\Omega\ cm^2$ ($\downarrow$ 3x). The new on-resistance was still very large; however the annealing demonstrated that the reduction of the parasitic resistance will further improve the device characteristics over other Gan MOSFET devices.

The GaN MOSFET transfer characteristics (Figure 6.16b) based on annealing temperature improved the current density and transconductance compared to the non annealed device. Through temperature activation of the gate dielectric, the threshold voltage was



(a) (b)

Figure 6.16: (a) The FatFET family of curves after the device was annealed at 300^oC (red) and 500^oC (blue). The drain current was improved by a factor a 4x over the low temperature annealed device. (b) The transfer characteristics after the device was annealed at 300^oC (red) and 500^oC (blue). The transconductance quadrupled over the original fabricated device due to the reduce series resistances.

shifted closer to the nominal expected value. This shift of the threshold voltage was not the major factor in the increased transistor properties. Rather the improved contact resistances reduced the degradation of the device characteristics which allowed the transconductance of the GaN MOSFET to increase to 0.08 mS/mm. Comparing the peak mobility of the GaN MOSFET discussed earlier, the 100 μm channel with a 80 $\mu S/mm$ transconductance would be expected to obtain a mobility in the range of 433 cm^2/Vs. This was confirmed that the trend was towards the intrinsic transconductance mobility with optimal ohmic contacts, shown in Figure 6.14.

Through post fabrication annealing, the electrical characteristics of the enhancement-mode GaN MOSFET were improved at 500^oC. Beyond this temperature the gate dielectric was unable to prevent conduction through the barrier. With an optimized annealing and process flow the contact resistance will be minimal without the degradation of the gate dielectric and channel.

Gate Length Reduction

The GaN MOSFETs test structures discussed earlier were extremely long channeled devices compared to commercially fabrication products. To obtain large current densities, the gate length must be shortened. It has been shown that the benefit of reducing the gate length also arises from the reduced gate leakage current. One of the major advantages of scaling the gate length by L, was the reduced gate leakage in ultra-thin gate dielectrics [116]. This further improves the undesired losses which increase the efficiency of the transistor. In addition, the switching frequency and device area are improved through the shrinking of the gate length. To examine the potential improvement, the gate length of the enhancement-mode GaN MOSFET was reduced to 10 μm and compared to the 100 μm FATFET. The goal of the decreased gate length was to improve the gate leakage, current density and transconductance.

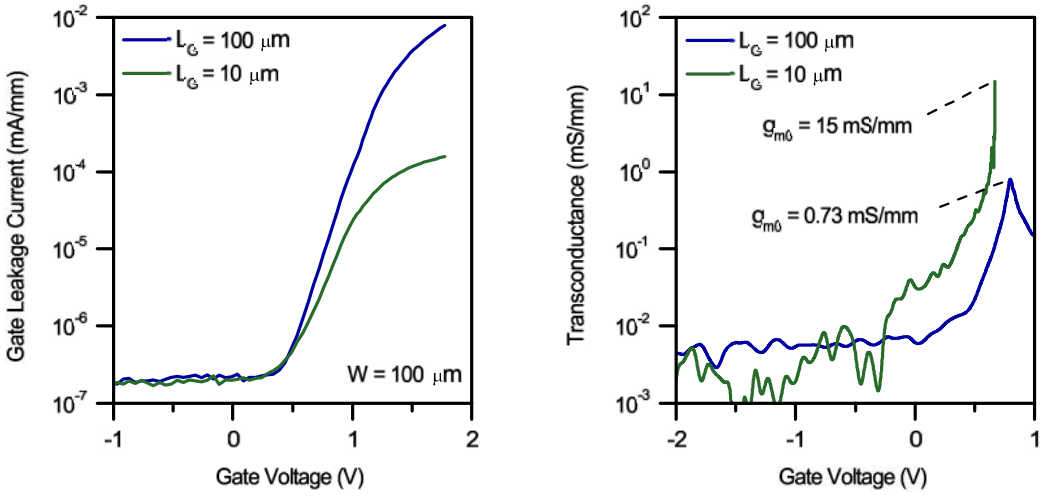
$$Y_{AC} = 2\frac{\tanh(\gamma\frac{L}{2})}{Z_0} \tag{6.13}$$

The AC gate admittance (6.13) was formulated based on a transmission line circuit model for ultra-thin leaky gate dielectrics [116]. The AC gate admittance (Y_{AC}) was defined by the characteristic intrinsic impedance (6.14) and the propagation delay (6.15). The intrinsic impedance and the propagation delay were defined by the normalized channel series resistance (r_s), the normalized tunneling resistance (r_t), the normalized capacitance density (C) and frequency (ω). Taking the frequency to zero, the DC leakage admittance was approximated through Taylor series expansion of the dependence of gate length was simplified in (6.16) and predicted that the reduced gate length of L would result in a reduction of the gate leakage by L^2.

$$Z_0 = \sqrt{\frac{r_s r_t}{1 + j\omega C r_t}} \tag{6.14}$$

$$\gamma = \sqrt{\frac{r_s}{r_t} + j\omega C r_s} \tag{6.15}$$

$$\frac{Y_{DC}}{L} \approx \frac{1}{r_t} - \frac{1}{12}\frac{r_s}{r_t^2}L^2 \tag{6.16}$$



(a) (b)

Figure 6.17: (a) The leakage current through the gate dielectric with respect to gate voltage. The leakage current was reduced by a factor of 100 as the gate length was reduced from 100 μm to 10 μm. (b) The GaN MOSFETs extracted intrinsic transconductance were compared based on gate length. The 10 μm channel increased the intrinsic transconductance to 15 mS/mm over the 100 μm GaN MOSFET channel.

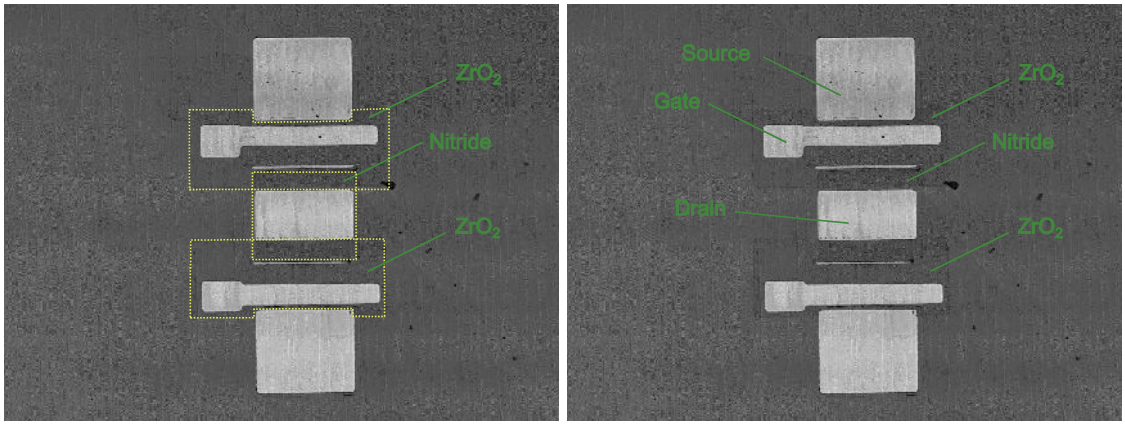
The gate leakage current of the 10 μm gate length, shown in Figure 6.17a, confirmed the gate leakage was reduced L^2 compared to the 100 μm FATFET. The leakage current obtained for both cases were relatively small compared to the drain current; however, the power efficiency has the potential to be improved as the transistor leakage was reduced by 100x.

The peak drain current of the devices was masked by the parasitic resistances at the source and drain. Thus, the intrinsic transconductance of the MOSFET, shown in Figure 6.17b, were compared to examine the effect of gate length. By reducing the gate length by a factor of 10x, the intrinsic transconductance improved by 20x. This extracted transconductance was better than conventional low-dielectric gate oxides with large density of interface traps and low capacitance densities. Again, with the advancement of traditional ohmic contacts, the novel GaN MOSFET will surpass current GaN transistors.

6.3.2 Breakdown Voltage Characterization

The off-state maximum drain voltage has become a very important entity of the power transistor. Without the ability to withstand large drain voltages the device cannot support high power electronic applications. Numerous techniques have been examined to suppress the electric fields along the drain to improve the voltage rating of the device. The most common technique for GaN HFETs are optimized gate biased field plates exposed along the drain region [25,60,148]. Other non-conventional techniques have demonstrated methods that removed the semiconductor where the peak electric field occurred [27], grounded multiple field plates [62], or grounded source and gate staircase field plates along the drain [149]. These techniques have been able to improve the voltage rating of HFET architectures; however, the GaN MOSFET has the potential to efficiently remove the carriers from the channel and withstand large drain voltages. The fabricated GaN MOSFET architecture was examined to determine the effect of device breakdown with respect to transistor architecture, device dimensions, template background doping and field plate structures. The variation of these parameters allowed for an in-depth understanding of the quality of the transistors off-state.

The off-state drain current of the GaN MOSFET was examined through high voltage drain biasing while the device was considered off. The source and gate of the transistor, shown in Figure 6.18, were grounded whilst the drain was swept from 0 V to 400 V. The drain and source currents were measured to determine the potential voltage rating of the devices. The conventional standard for GaN power devices considered device breakdown to occur when the off-state drain current reached 80 $\mu A/mm$ [25]. Beyond this drain current



(a) (b)

Figure 6.18: A confocal image of the GaN MOSFET used to measure the breakdown voltage. (a) The dashed lines are where the transparent films were patterned and deposited. (b) The source and gate contacts were grounded while the drain voltage was increased. The confocal image allowed for the transparent ZrO_2 and ZrN films to be imaged. The AlN optical properties were identical to GaN making imaging nearly impossible.

the device was no longer consider off. This universal standard has allowed easy comparison of breakdown voltage between similar GaN based devices.

GaN Template Doping

The drain current with respect to drain voltage was obtained for three different GaN templates, shown in Figure 6.19. Similar to the threshold voltage, the breakdown voltage has a strong dependence on the background doping of the GaN. The silicon doped GaN template was unable to prevent current flow as soon as the drain was bias; which was indicative from the operation examined earlier. The N^- GaN partially depleted the channel to push the off-state breakdown until 12 V. The on-state provided a demonstration of enactment-mode behavior, however the N^- GaN was unable to prevent off-state leakage current for high power electronics. Conversely, the semi-insulating GaN templates were able to form a fully depleted channel under the gate. This reduced the off-state drain leakage current and significantly increased the maximum drain voltage. For a GaN MOSFET to have the potential for power electronics, the background doping caused from film defects during growth must be minimal.

The examination of background doping confirmed simulations, discussed in Chapter 2, that during the off-state a low electron concentration of carriers along the channel are critical GaN power MOSFETs. The following sections examined the effects of substrate leakage with respect to the device architecture and device dimensions.

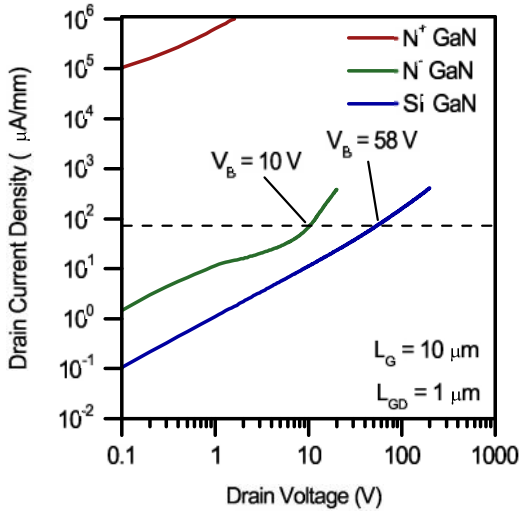


Figure 6.19: The substrate leakage current with respect to GaN background doing as a function of drain voltage. The semi-insulating GaN was capable of preventing the substrate leakage current beyond 50 V.

Gate-Drain Separation

The simulations discussed in Chapter 2 predicted that the breakdown voltage of the transistor was strongly dependent on the distance between the gate and drain contacts. Two transistor designs, shown in Figure 6.20, were used to compare the ability to withstand the electric fields along the drift region. The conventional MOS-HFET and MOSFET designs utilized the ZrO_2 gate dielectric (6.9 nm) to reduce the leakage current to the gate. Both transistors utilized the AlN films along the source and drain regions to provide carriers to the device. The significant variation between the two transistor architecture, was the AlN (5.7 nm) along the channel in the MOS-HFET. This increased the overall minimum carrier concentration at zero gate bias, which prevented the device from withstanding large drain voltages. Conversely, the MOSFET has been shown to reduce the minimum carrier concentration during the depleted channel which improved the breakdown voltage [46, 150].

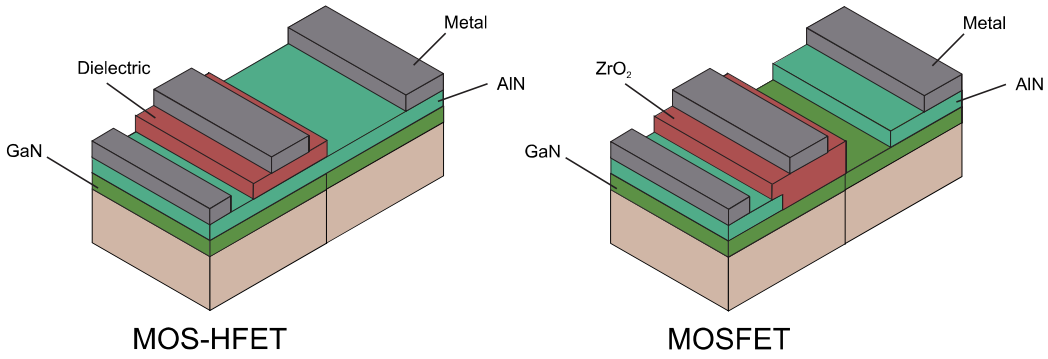
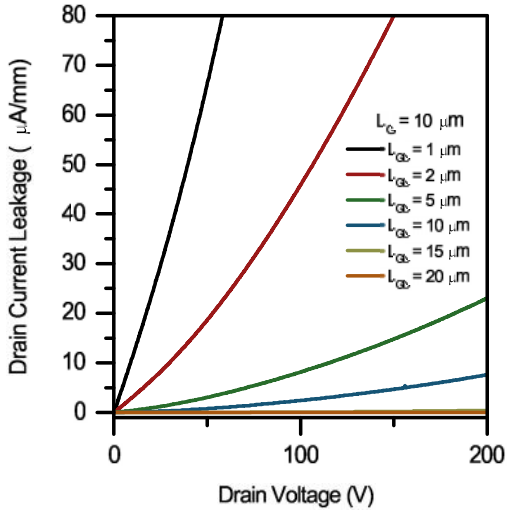


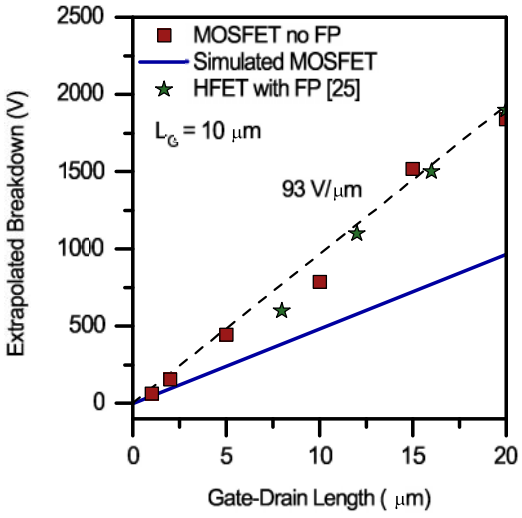
Figure 6.20: The GaN MOS-HFET and MOSFET transistor architectures were compared for the potential maximum drain voltage before the leakage current becomes 80 $\mu A/mm$. The significant variation between transistors was the ultra-thin AlN film under the gate metal.

The current density of the transistors were obtained as the drain voltage was swept to 200 V, shown in Figure 6.21a. The HFET architecture was determine to reach the breakdown current below 20 V for all gate-drain separations. This suggested that the GaN HFET was unable to fully the deplete the channel (i.e. depletion mode transistor) compared to the GaN MOSFET (i.e enhancement-mode transistor). The additional resistance along the drain from the GaN MOSFET in-conjunction with the lower carrier concentration beneath the channel improved the breakdown voltage. The drain leakage current was considered as a soft-breakdown due to the lack of a p-type GaN region beneath the gate. However, the semi-insulating GaN channel was able to reduce the leakage current sufficient to prevent significant conduction before 200 V. The limitation of the Keithley 4200-SCS prevented extremely high voltage measurements beyond 400 V. The leakage current and drain voltage

were compared in log scales to extrapolate the potential breakdown voltage of the devices. The electric field strength was significantly lower than the maximum critical field strength of GaN which allowed for the extrapolation of the leakage current to be assumed as the mechanism for device breakdown. This device breakdown voltage was not catastrophic breakdown caused from high electric fields. Instead the device was considered to no longer



(a)



(b)

Figure 6.21: (a) The measured drain leakage current during the off-state of the GaN MOSFET. As the gate-drain length was increase, the device was capable of improving the maximum drain voltage. (b) The extrapolated breakdown voltage trend for the GaN MOSFET (red square) with respect to the drift region. The breakdown voltage of the leading GaN HFET device (green star) and the simulated GaN MOSFET (blue) were included.

be off due to the depletion leakage under the channel caused from sub-critical electric field strengths.

The comparison of the extrapolated breakdown with respect to drift region (gate-drain) length, shown in Figure 6.21b, provided the average electric field strength along the drain. The GaN MOSFET without field plate architectures were able to maintain a 93 $V/\mu m$ electric field strength along the drain. This was larger than the expected simulations due to the recessed AlN drain, shown in Figure 6.20. The extract depleted region along the drain improved the breakdown voltage over the highly doped drain obtained from simulation. The average field strength along the drain of the recessed drain and the leading GaN HFET design with optimized field plates and gate stacks [25] were found to produce an equivalent drain voltage rating. Moreover, the HFET required a source and gate field plate to minimize breakdown effects compared to the inherently normally-off MOSFET without field plates.

The inherent MOS design has a preferential off-state compared to the HFET architectures, which required optimized structures to obtain equivalent drain voltage ratings. The MOS incorporated within a GaN power transistor and the appropriately designed field plates will significantly reduce the leakage current and suppress the peak electric fields to ensure high voltage applications are possible.

Field Plate Architecture

The leading GaN MOS-HFET breakdown voltage shown in Figure 6.21b, was capable of suppressing the electric fields because of the inclusion of a field plate along the drain. It has been shown that a field plate along the drain has the potential to reduce the electric field along the gate-drain edge by half [21, 46, 59, 151]. Based on the optimal height, length and dielectric, the field place has to ability to prolong the off-state of the transistor before breakdown by suppressing the peak electric field by more than half [46, 150]. To improve the drain voltage rating of the PEALD GaN MOSFET, floating field plates were fabricated on the ZrO_2 film midway in the drift region, shown in Figure 6.18. The metal field plates were self aligned during the metalization step of the gate, source and drain contacts. The floating field plate was to behave as a voltage divider across the drain region. This would potentially reduce the electric field near the drain edge of the gate. The floating field plate was not the optimal design examined in Chapter 2, however the effects would demonstrate the advantage of the incorporation of a field plate for prolonged breakdown voltages in GaN MOSFET.

The drain leakage current of a GaN MOSFET ($L_G = 10\ \mu m$ and $L_{GD} = 2\ \mu m$) with and without the floating field plates was compared with respect to drain voltage, shown in Figure 6.22. The gate and source contacts were grounded, while the drain voltage was swept from 0 V to 400 V. The breakdown voltage was obtained when the drain leakage current

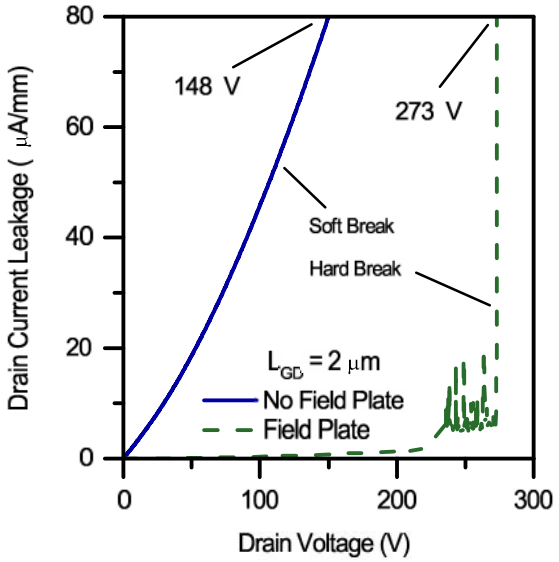


Figure 6.22: The measured drain off-state leakage current for a 10 μm gate GaN MOSFET with (solid green) and without (dashed blue) a floating field plate. The floating field plate increased the average critical electric field along the drain from 0.74 MV/cm to 1.4 MV/cm.

reached 80 $\mu A/mm$. The non-field plate GaN MOSFET reached the breakdown limit at 148 V compared to the floating field plated MOSFET which suppressed breakdown to 273 V. The leakage current with respect to drain voltage produced a soft breakdown; whereas, the field plate suppressed the electric field to reduce the leakage current before breakdown occurred. The field plated MOSFET pushed the breakdown voltage by 2x and created a hard breakdown, rather than a soft breakdown. Through the addition of a floating field plate the breakdown voltage was able to suppress the average drain electric field strength to 140 $V/\mu m$. With optimized field plates demonstrated in simulations, the GaN MOSFET will further improve the average drain field strength.

Gate Length Dependence

The channel length of a MOSFET has the ability to increase current density, improve switching frequency and reduce gate leakage current. However, during the off-state the breakdown voltage has been shown to have negligible effect of the drain voltage rating of the device. The majority of the drain voltage drop occurs along the drain regions rather than below the gate. The gate region is essentially only used to reduce the current flowing from the drain current. Simulations shown in Chapter 2 of the breakdown voltage of the MOSFET confirmed the majority of the high electric field strength occurred along the drain.

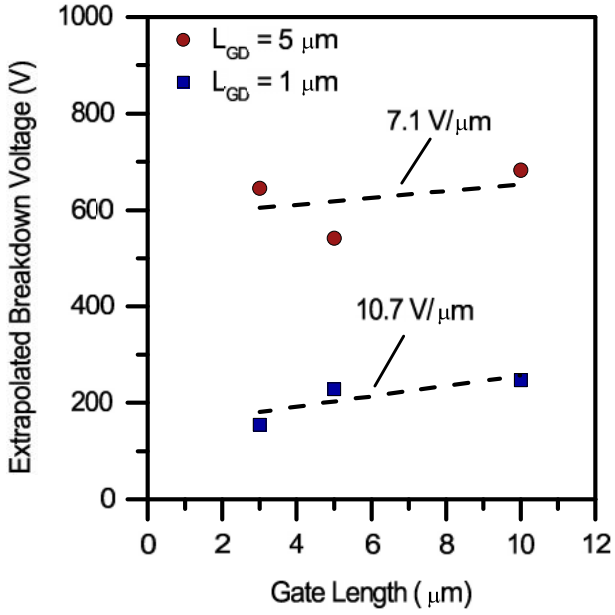


Figure 6.23: The gate length extrapolated maximum drain voltage of GaN MOSFET architectures with different drift regions; $L_{GD} = 1\ \mu m$ (squares) $L_{GD} = 5\ \mu m$ (circles).

The electric field under the MOS channel was well below the point of avalanche effects and catastrophic breakdown. Furthermore, initial simulations predicted that the breakdown voltage of the GaN MOSFET was not significantly effected by larger gate lengths.

The drain leakage current for different gate length MOSFETs ($L_G = 3$, 5 and 10 μm) were examined for channel length variation. The off-state drain leakage current for different gate lengths and drain-gate lengths, shown in Figure 6.23, confirmed the drains drift region dictated the breakdown voltage rather than the gate length. Again, this was in agreement with the simulations obtained in Chapter 2 which examined the dependence on the gate length. The negligible gate length effect on the drain breakdown voltage has the potential to increase current density (i.e. power rating), while maintaining a large voltage rating. Overall, the maximum power rating of the GaN MOSFET has the ability to surpass current HFET technology while maintaining a higher quality off-state.

Gate-Source Overlap

It has been shown for low voltage silicon technology, that the source region must be present beneath the gate metal. This overlap ensured a reduced drain-induce barrier lowering effect (DIBL) [152–154] and gate-source edge electric field [155, 156]. As the source overlap was pulled out from the gate the DIBL increased, shown in Figure 6.24, which implied the

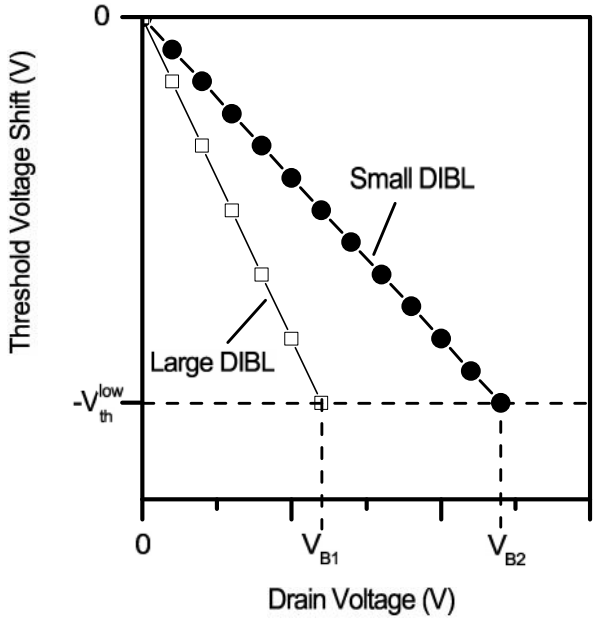


Figure 6.24: The breakdown of the device can be considered when the shift of the threshold voltage reached the low drain threshold voltage (V_{th}^{low}). This is where the large drain voltage was considered as $V_{th} = 0$ V.

threshold voltage degraded at large drain voltages. Furthermore, it has been demonstrated that the off-state leakage current is reduced as the source is overlapped under the gate [156]. Threshold voltage variation creates a problem regarding the on-state operation; however, a large DIBL effect has the potential to significantly degrade the quality of the off-state. This would reduce the maximum drain voltage applied to the drain before the device is no longer considered off, shown in Figure 6.24. Through simulation is was determined that the breakdown occurs from higher electron energy and electric field strength at the gate-source edge. Ultimately, the device trends towards a depletion mode transistor, rather than an enhancement mode normally-off device.

The optimal location of the gate-source overlap is critical for the peak transistor characteristics. However, due to the alignment fabrication difficulties present in the facility the extreme cases of overlap and under-lap were examined. The gate-source overlap of the GaN MOSFET was examined at two locations; 0.1 μm under the gate (L_{ov} = 0.1 μm) and 0.5 μm away from the gate (L_{ov} = -0.5 μm). Pulling the AlN away from the gate ultimately degraded the maximum voltage on the drain before the device was considered on. The source was not fully depleted at the gate edge which resulted in a larger leakage current and early onset of breakdown, shown in Figure 6.25. The extrapolated breakdown voltage with respect to drain drift region of GaN MOSFETs were examined for the recessed source and overlapped source. The overlapped gate-source breakdown line was 10x larger than

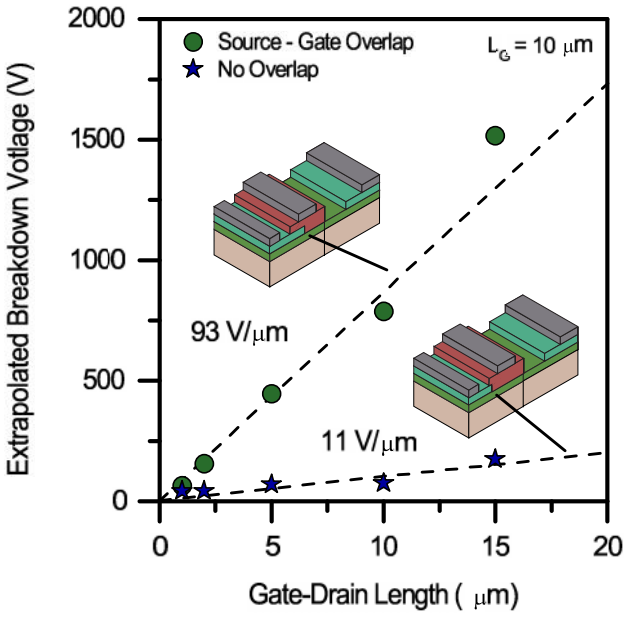


Figure 6.25: The extrapolated breakdown voltage based on the substrate leakage current was examined as the AlN on the source-gate edge was removed from under the gate metal. A source-gate overlap of 100 nm ensured the breakdown voltage was close to 100 V/um. Removing the source carriers from under the gate prevented the transistor from withstanding larger drain voltages.

the recessed source. This was somewhat counter intuitive, pulling the carriers farther away on the source edge increased the leakage current and reduced the overall maximum drain voltage.

The gate-source overlap was demonstrated as one of the most imperative regions of the GaN MOSFET to ensure an off-state was achieved. The GaN MOSFET was able to produce an improved breakdown voltage with a non-optimized gate-source overlap of 100 nm. The optimal length of this region will have a significant improvement on the transistor properties. Thus, advanced simulations of the gate-source region, film stack and overlap dimensions are imperative to obtain the minimal DIBL effect to improve the overall maximum drain voltage.

6.4 Summary

The demonstration of an enhancement-mode GaN MOSFET was achieved with low temperature PEALD films along the gate, source and drain regions. Utilizing the low temperature deposition allowed for the GaN MOSFET to be fabricated without the use of chemical

to etch films or high temperature growth techniques. This reduced the overall number of fabrication steps, as well as photo-lithography masks.

The turn-on voltage of the transistor was controlled through the workfunction of the gate metal. By using Cr as the gate metal the device turn-on voltage was determined as 1.3 V, whereas the lower workfunction metal (Al) produced a depletion-mode device. The control of the flat-band voltage of the MOS channel based on the metallic workfunction provided a simplistic design feature for the turn-on voltage of the MOSFET.

The breakdown voltage of fabricated GaN MOSFET and GaN MOS-HFET were examined with different gate-drain lengths. The non-field plated GaN MOSFET architecture was able to withstand drain voltages equivalent to the leading optimized field plated MOS-HFET in literature. With the improvement of optimized field plates, the MOSFET has the ability to reduce the gate-drain separation to achieve an equivalent drain voltage rating.

The extraction of the channel mobility through the intrinsic transconductance, suggested that the novel GaN MOSFET demonstrated has the potential to reach current HFET technology once the parasitic resistances are maintained. Furthermore, a peak channel mobility above 200 cm^2/Vs was one of the leading MOS mobility for GaN transistors. This was obtained from the improved interface along the channel due to the developed PEALD deposition technique for rare earth metal oxides. The MOSFET architecture has been shown to produce promising current densities and potential maximum drain voltages. Through the incorporation of low temperature PEALD films along with conventional GaN fabrication techniques, the GaN MOSFET has the potential for high power electronics.

Chapter 7

Summary and Conclusions

To advance high power electronic devices, novel GaN transistors are required to surpass current GaN HFET technology. The wide range of applications that require a switching device with high power, high frequency and high temperature capabilities has mainly driven GaN research in HFETs, MOSHFETs and MOSFETs. Conventional gate dielectric fabrication techniques have been unable to maintain the density of interface traps, which in-turn reduce the peak capacitance density and channel mobility. With hindered device characteristics, the GaN MOSFET has been unable to compete with modern HFET technology. This thesis examined the use of low temperature PEALD films for the incorporation into the gate, source and drain regions of the device to improve the characteristics of the GaN MOSFET.

Preliminary high-κ rare earth metal oxides on GaN were examined for potential use in a GaN MOSFET. Ultra-thin low temperature PEALD ZrO_2 and HfO_2 films were examined to determine the optimal material type and thickness for the proposed GaN MOSFET architecture. Through electrical extraction and characterization, Table 7.1, the ZrO_2 film produced larger capacitance densities ($> 3\ \mu F/cm^2$) and lower density of interface traps ($< 5\text{x}10^{10}\ eV^{-1}cm^{-2}$) compared to the HfO_2 and current GaN MOS structures found in

Table 7.1: Low Temperature PEALD Gate Dielectrics on GaN

Film Type	Growth Cycles	Film Thickness	Dielectric ϵ_r	C_{ox} $(\mu F/cm^2)$	D_{it} $(eV^{-1}cm^{-2})$	μ_n (cm^2/Vs)
HfO_2	30	3.2 nm	22.9	3.0	$40\text{x}10^{10}$	263
	40	5.4 nm	16.9	2.1	$50\text{x}10^{10}$	243
	58	8.5 nm	8.1	0.8	$20\text{x}10^{10}$	233
ZrO_2	30	3.2 nm	34.8	3.8	$5\text{x}10^{10}$	360
	40	5.4 nm	22.8	2.6	$3\text{x}10^{10}$	387
	58	8.5 nm	12.1	1.1	$6\text{x}10^{10}$	370

Table 7.2: Ultra-thin Low Temperature PEALD AlN Films on GaN Templates

Film Type	Growth Cycles	Film Thickness	R_{AlN} (Ω/sqr)	N_{2DEG} $(10^{13}cm^{-2})$	μ_e (cm^2/Vs)
N^+ GaN	40	3.2 nm	210	2.39	1245
	70	5.7 nm	175	3.04	1175
	100	7.9 nm	550	0.91	1249
N^- GaN	40	3.2 nm	2178	0.28	1024
	70	5.7 nm	592	1.14	926
	100	7.9 nm	1307	0.47	1017

literature. The ZrO_2 films produced larger relative dielectric constants and higher peak electron mobilities compared to the HfO_2 films. Based on the extracted dielectric interface characteristics, the rare-earth metal oxide films have the ability to improve GaN MOS applications for switching applications.

Low temperature plasma-enhanced atomic layer deposition AlN grown films were demonstrated on GaN for the purpose to produce high carrier densities along the interface. The AlN film thickness and GaN template background doping were strongly dependent on the resulting sheet resistance and 2DEG, shown in Table 7.2. The low temperature deposition technique was able to produce equivalent carrier densities compared to conventional higher temperature ($> 800^oC$) techniques. A selective PEALD photoresist lift-off technique was capable to pattern the films without the use of complex etching and mask fabrication processes.

Enhancement-mode GaN MOSFETs were fabricated using low temperature PEALD AlN films for the active source and drain regions. This produced carriers along the source and drain without the difficulties associated with ion implantation. The characterized high quality 40 cycles ZrO_2 film was used as the gate dielectric for the fabricated MOSFET device. The GaN MOSFETs exhibited normally-off behavior ($V_t \approx 1.3$ V) with the use of a Cr gate metal workfunction. Switching the gate metal to Al significantly degraded the device characteristics, shown in Table 7.3, due to the depletion-mode operation. The use

Table 7.3: GaN MOSFET Device Characteristics

Gate Metal	V_t (V)	Sub-threshold (mV/dec)	I_{DS} (mA/mm)	g_m $(\mu S/mm)$	D_{it} $(cm^{-2}eV^{-1})$
Al	-0.15	956	0.01	6.5	$1.1\text{x}10^{11}$
Cr	1.3	123	0.17	45	$1.7\text{x}10^{10}$

of unintentionally doped GaN templates did not prevent substrate leakage current during the off state of the device for both Cr and Al gate metal. To correct a lower doped GaN template, which produced a true off-state, was examined for drain breakdown voltage. The parasitic contact resistance was not optimized for the test devices which limited overall peak current density. However, the intrinsic transconductance of the fabricated MOSFET was able to surpass many GaN MOSFET devices with smaller channel lengths. Based on the intrinsic transconductance, the GaN MOSFET has the potential to compete with current HFET technology as the channel was reduced.

Further investigation of the breakdown voltage on semi-insulating GaN-on-sapphire templates confirmed simulations which predicted the improved off-state performance the MOSFET architecture has over HFET designs. The most important region of the MOSFET which dictated the breakdown voltage and off-state characteristics of the device was the gate-source edge and gate carrier density overlap. Without the overlap of the gate metal and source carriers, the device was a severally degraded from an increased DIBL effect. With an appropriated gate-source overlap, the average drain electric field strength was extracted from the extrapolated breakdown voltage with respect to gate-drain separation. The non-field plated MOSFET design was capable of withstanding equivalent field strengths ($\sim$ 90 V/μm) to the optimized gate and source field plated MOS-HFET designed. With the incorporation of field plates, the simulated GaN MOSFET has shown the ability to improve the maximum drain voltage along the drift region compared to the HFET architecture. Floating field plates were fabricated along the drain region to suppress peak electric fields in a MOSFET structure, shown in Table 7.4. The extracted average field strength along the drain without a field plate and a floating field plate were 90 V/μm and 147 V/μm, respectively. Through the inclusion of floating field plates, the GaN MOSFET has demonstrated significant off-state characteristics over the GaN HFET for potential power applications. With the addition of optimized field plates the GaN MOSFET design has a significant advantage over HFET architecture for high voltage applications.

Table 7.4: GaN MOSFET Breakdown Voltage Characteristics

Simulation					
L_{GD}	1 μm	2 μm	5 μm	10 μm	Avg Field
No Field Plate	41 V	80 V	220 V	420 V	42 V/μm
Source FP	-	350 V	1200 V	2150 V	210 V/μm
Gate/Source FP	-	-	1800 V	4990 V	429 V/μm
Experimental					
L_{GD}	1 μm	2 μm	5 μm	10 μm	Avg Field
No Field Plate	65 V	148 V	446 V	787 V	90 V/μm
Floating FP	-	273 V	681 V	1495 V	147 V/μm

Low temperature PEALD films demonstrated the simplicity of ALD lift-off fabrication and the ability to attain or surpass high temperature processing techniques. The GaN MOSFET demonstrated a normally-off ($V_{th}>$ 0 V), enhancement-mode transistor with the ability of producing a channel mobility of 230 cm^2/Vs. The potential of low temperature processing in-conjunction with high temperature processing has the potential to further improve the GaN MOSFET device for use in high power applications.

7.1 Directions for Future Work

The enhancement-mode GaN MOSFET with the incorporation of a rare earth metal oxide was used to demonstrate the potential the MOSFET has to surpass current GaN technology. To produce a fully functioning GaN MOSFET with the desired breakdown voltage and current density, the investigation of leakage current and parasitic resistances are imperative. The use of semi-insulating GaN templates will reduce the leakage current, which in-turn will improve the maximum operating drain voltage. Future work will address the parasitic resistance to reduce the contact resistance through conventional HFET fabrication techniques. Diffusion barriers along interfaces should also be considered in order to prevent degradation from diffusion during various annealing steps during fabrication.

The incorporation of conventional techniques used in GaN HFETs and low temperature PEALD films discussed in this dissertation should be examined for the potential to improve the GaN MOSFET characteristics. The use of this novel technology has demonstrated the potential for GaN MOS applications and will further advance the GaN MOSFET design for power electronics.

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