UNIVERSITY OF ALBERTA

A SIGNAL DETECTION TECHNIQUE FOR ISLANDING DETECTION OF DISTRIBUTED GENERATORS USING POWER LINE SIGNALING

BY

JATINDER SINGH HAYER 

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ABSTRACT

Recent developments in the electricity market have provided new opportunities for Independent Power Producers (IPP's) with small generating facilities to sell electricity to the utilities in Alberta. These generating facilities provide three major advantages: they help utilities save significant amounts of capital which they would otherwise have to invest for setting up new generation facilities, they reduce pollution by utilizing emissions for power generation and they reduce line losses due to their proximity to the load centers. For IPP's, one of the major obstacles in the way of getting permission for interconnecting with utility power lines is the islanding of distributed generator (DG). Means must be provided by either the IPP or the utility to detect this condition and disconnect the DG from the network within a specific time period after islanding. Current islanding detection techniques are expensive and may not work under certain conditions. An islanding detection scheme using distribution line signaling has been proposed by the Power Engineering group at the University of Alberta. A signal, that can be detected at all DG sites by signal detectors, is broadcast continuously from the substation. In case of islanding, detectors can no longer detect the signal, and hence the DG is disconnected from the system. This thesis discusses the development and performance evaluation of a signal detection method to be used with the proposed signaling technique. A signal detector must be capable of accurate signal detection and should have a response time in the order of 500 ms. A signal detector device has been developed and its performance has been evaluated by means of various laboratory experiments. Signal detection method is capable of accurate signal detection and indicating a loss of signal within a specified time period after the islanding takes place.

To my teachers

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SYMBOLS & ABBREVIATIONS

ω	Angular Frequency (radians/sec)
AMR	Automated Meter Reading
C	Capacitance
CB	Circuit Breaker
DAQ	Data Acquisition Device
DG	Distributed Generator
e_{mod}	Transient component of system voltage
f	Frequency (Hz)
$i(t)$	Current as a function of time
K	Constant
KVAR/ VAR	kilo volt-amps / volt-amps (Reactive)
L	Inductance
p.u.	Per Unit
PLC	Programmable Logic Controller
R	Resistance
RMS	Root-mean-squared
ROCOF	Rate Of Change of Frequency Relay

SCADA	Supervisory Control and Data Acquisition system
SCR	Silicon Controlled Rectifier
v(t)	Voltage as a function of time

Chapter 1

INTRODUCTION

With the deregulation of electricity markets, dispersed embedded generators also called distributed storage and generation (DSG) facilities or simply distributed generators (DG) are becoming ever more popular in North America. A DG is a power source of typically 5kW to 20MW capacity connected to a distribution grid away from the main substation.

IEEE definition of a dispersed storage and generation (DSG) facility: [7]

1. Has a power producing capacity of 80 MW or less
2. Produces electric energy using a primary energy source consisting of at least 75% biomass, waste, renewable resources, or a combination thereof on an annual basis.
3. Is less than 50% owned by the electric utility

In markets like Alberta's, DG's can serve a dual purpose: they can help meet the growing energy requirements, especially during peak load hours, and; utilizing emissions from oil and gas facilities, can also help to reduce pollution. Dispersed power sources, being closer to the load, also help reduce line losses. However, the interconnection arrangement requires properly protecting DG's against islanding as well as protecting the

loads connected to the grid against degradation of power quality that may arise due to the presence of DG's in the distribution system.

A major challenge in the area of protection and control is islanding detection. When a service area in the proximity of a DG is disconnected from the rest of the distribution network, with a DG as its only power source, it is called an island. An islanded system, due to the absence of a stiff power source, is prone to power quality problems as the DG itself might not be able to maintain voltage and frequency within acceptable levels. There are other issues that need to be addressed before interconnecting a DG to a distribution network. These issues include out of phase reclosing, coordination of protection devices, and personnel safety, as discussed in the following sections of this chapter.

1.1 Islanding: Definition & Implications

In this section, a power island is described and possible consequences of the unintended operation of a DG under islanded condition are discussed. Major concerns while a DG is islanded include public and personnel safety, power quality, co-ordination of protection devices, and the safety of the DG.

1.1.1 Islanding

When a section of a power distribution network is isolated from the rest of the system and is supported by a power source other than the main substation, it is called an

islanded system. Figure 1.1 shows a typical distribution network that has two DGs at different locations interconnected to the system. Under normal operating conditions, the substation supplies most of the energy and a fraction of the total load is supported by the DG.

In Figure 1.1, if circuit breaker CB3 is tripped due to a fault in the system, the portion of the distribution network to the right of CB3 will be isolated from the rest of the system, resulting in an islanded system. The main power source – the substation, no longer supplies any power to the islanded system.

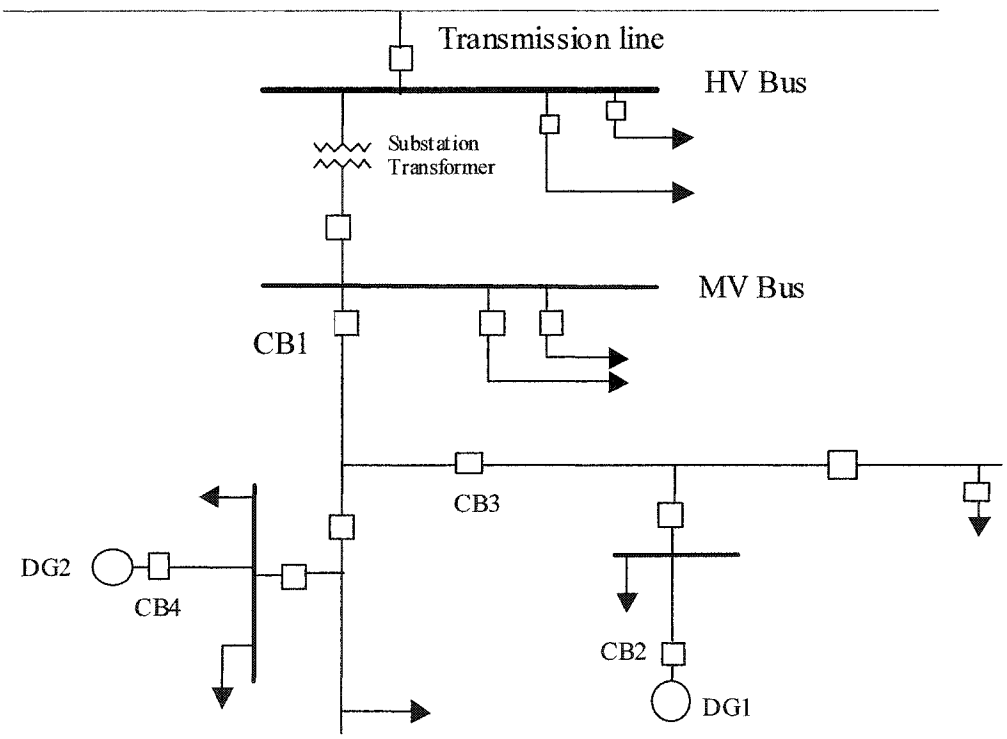

Figure (1.1): Distribution System with DGs – Normal Operation

As shown in Figure 1.2, if DG1 remains connected to the distribution line, the loads to the right of CB3 will be supported by DG1 alone. DG1 and loads in its proximity isolated from the substation constitute an islanded system. This system, due to the absence of a stiff power source, is very unstable which may lead to serious implications.

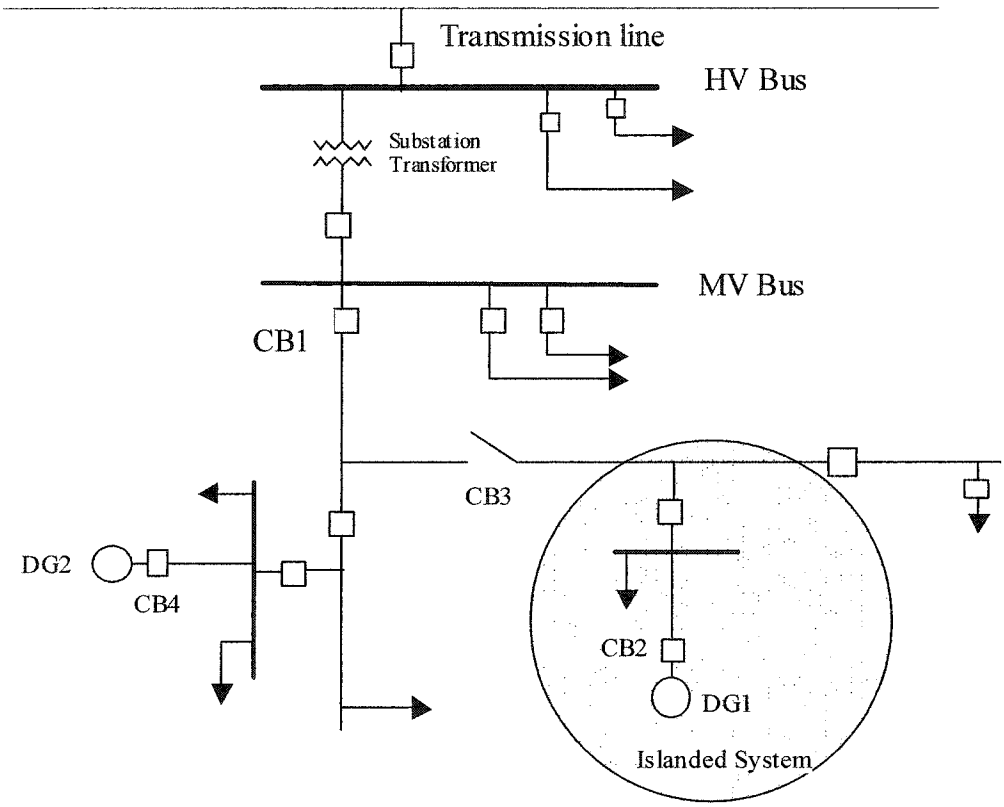

Figure (1.2): Distribution System with DG – Islanded Operation

It should be noted that sometimes an islanded operation is desired, particularly in remote areas where a single or multiple generators are capable of supplying electricity at acceptable power quality levels to the entire load in the area. In this thesis, the detection and prevention of undesired islands is discussed.

1.1.2 Implications of DG Islanding

Power Quality

When a DG is islanded, the voltage and frequency provided to customers inside the island are out of the utility's control, yet the utility remains responsible to these customers [8]. It is possible that an islanded DG may keep supplying power to connected loads even when the power quality level is less than acceptable unless the measures are taken in advance to avoid such conditions.

Public and Personnel Safety

Line worker safety can be jeopardized by DG sources feeding a system after primary sources have been opened and tagged out unless the utility has a means to disconnect DGs on its own during service and repairs. The public is at risk if the utility does not have the capability to de-energize downed lines [8].

Protection Device Coordination

Short circuit current availability is drastically reduced in the absence of the primary current source, the substation. Protection systems therefore will be uncoordinated, increasing the risk of equipment damage due to faults [8].

Out-of-Phase Reclosing

Reclosers are used to eliminate the possibility of permanent power outage due to temporary faults. Utility breakers and circuit re-closers are likely to reconnect the island to a larger power source when out of phase. In the case of rotating generators, large

mechanical torques and currents are created due to out of phase re-closing, which can damage the generator or prime mover. For DG sources such as solar panels, using electronic inverters, fast current limiting functions of an inverter provide self-protection, thereby reducing the risk of damage due to out-of-phase reclosing.

Another phenomenon that takes place during out of phase re-closing is generation of transients on distribution networks that are potentially damaging to all equipment connected to the line. The magnitude of these transients typically ranges between 2 p.u. and 3 p.u., depending upon the level of capacitance and damping in the system [8, 9].

Induction generators are also at risk. When an induction generator is disconnected from a utility system, it slows down or speeds up depending on how much load remains connected to the machine. This change in speed will generally result in a change in voltage magnitude and phase relationship of the isolated unit with respect to the utility source voltage. Should the isolating switch be re-closed when the voltage across the open switch exceeds a certain value, excessive machine winding and shaft stresses will be produced. This situation is potentially a hazardous, particularly if self-excitation has occurred [7].

1.2 Objectives and Scope

A number of products are available for islanding detection, but they are either too expensive or have limited reliability. There is a need to develop a simple, reliable and

economical islanding detection technique. An islanding detection scheme was proposed by the Power Engineering Group at the University of Alberta [12].

This technique utilizes a signal as a circuit continuity check to detect an island. The idea is to continuously broadcast a signal to various DG sites through a power line. Signal detectors are installed at each DG site. If the signal is not detected at a particular DG site, the site can be considered as islanded and should be tripped.

This thesis aims to present the development of a signal detection method for the proposed signalling technique. The detector must be capable of detecting an islanding condition with a time delay less than the recloser operation time.

The scope of this thesis can be summarised as:

- To review the proposed islanding detection scheme using distribution line communication method for islanding detection; and analyze signal characteristics.
- To develop a prototype device for signal detection.
- To investigate the performance of the signal detection device in terms of accuracy of signal detection and response time.

1.3 Outline of Thesis

This thesis describes the operation and investigates the performance of a signal detector to be used for the purpose of islanding detection in a scheme proposed at the

University of Alberta. The proposed method of islanding detection involves the broadcast of a signal from the substation on the distribution network and the detection of signal at each DG facility.

To accomplish the objectives set at the start of this project, the following methodologies were adopted:

- A brief review of the proposed islanding detection scheme was conducted
- PSCAD simulation program was used to verify the claims made in literature [1,2,3], and to analyze effects of changing network conditions on signal properties.
- A prototype signal detection device was developed and its performance was tested in lab experiments using a prototype signal generator and a line model.

Chapter 2 starts off with a brief review of existing islanding detection techniques and the technique proposed at University of Alberta. A description of the signal generator in the proposed scheme is also presented.

Chapter 3 presents the analysis of results obtained by PSCAD simulations. Effects of load variation and changing VAR compensation levels are discussed in detail. This analysis helps identify core requirements of the signal detector for reliable operation in islanding detection.

Chapter 4 describes the signal detection method and its implementation. A pilot device was developed using National Instruments® data acquisition hardware (DAQ) and LabVIEW programming software. The detection algorithm is discussed in detail and the fundamental differences between signal detection methods for Automated Remote Meter Reading and islanding detection are briefly discussed.

Chapter 5 focuses on performance evaluation of the detector. Test methods and laboratory test results are presented. During the performance evaluation of prototype signal detector, performance parameters of vital importance are accuracy of signal detection and response time.

Chapter 6 discusses the conclusions derived from this thesis, and offers suggestions for future work.

Chapter 2

A POWER LINE SIGNALING BASED ISLANDING DETECTION SCHEME

This chapter presents a review of existing islanding detection techniques and the technique proposed at the University of Alberta. IEEE Standards and the sections of Alberta Guide, relevant to islanding detection of DGs are discussed. A description of the signal generator in the proposed scheme is also presented. The last section discusses a signal detection method employed in AMR systems.

2.0 Introduction

Islanding detection is an important part of the overall protection scheme of the electric generators connected to utility distribution networks. The growing interest in distributed generation has resulted in an extensive research effort towards innovative islanding detection and protection techniques. Most existing techniques rely on power mismatch between the DG and load. Under certain conditions, however, this difference might not be enough for protection devices to detect. As discussed in Chapter 1, a DG and the neighboring loads are at risk if the generator is not disconnected from the distribution grid when it is islanded. If the protection device is over-sensitive, it may

result in nuisance tripping of the DG due to common disturbances experienced by a distribution network.

A review of existing islanding detection methods and their limitations is presented in this chapter. IEEE and the Alberta Guidelines for DG interconnection as they apply to islanding detection are also discussed. Contradictions in these guidelines for islanding and other protection requirements are discussed as well. In the final sections, a review of a scheme for islanding detection using the power line signaling technique proposed at the University of Alberta is presented. Signal generation and detection mechanism are briefly discussed.

2.1 Current Methods of Islanding Detection & Prevention

There are a number of methods available for islanding detection. Some of them use information of electrical quantities available at the DG terminals; and use that information to determine if the DG is islanded. These methods rely on the power mismatch between the source and load, and are referred to as *DG Side Islanding Detection Methods.* Other methods use information available at sites away from the DG to determine if it is islanded. Transfer trip schemes, directly controlled by the utility, are used to disconnect the DG from the distribution network. Such techniques monitor the state of circuit breakers; i.e., open or closed, and use this information to determine if a particular DG is islanded; these are called *Utility Side Islanding Detection Methods.*

2.1.1 DG Side Islanding Detection

The methods, in which the islanding detection and/or prevention device is located at the DG terminals, are called DG side islanding detection methods. These methods can be further divided into *passive* and *active* methods. The passive schemes attempt to detect an islanding condition based on a change in magnitude and/or frequency of the voltage and current signals available at the DG terminals. Active methods involve injecting a small disturbance into the system; and determining if the DG is islanded, based on system response to that disturbance.

Most techniques monitor the system frequency. If there is a change in the system frequency greater than a preset threshold, the DG is considered to be islanded, and will be tripped. Some techniques measure the rate of change of frequency to determine if a DG is islanded. These schemes exploit the fact that system frequency changes if there is a large mismatch between load and power-source capacity. In view of the fact that the frequency is constant when the substation is available as a power source, it is possible to detect the islanding condition by checking the magnitude and rate of frequency change. Some other techniques use change in voltage level to determine if a DG is islanded.

The active schemes require that small disturbances be injected into the system at the DG terminals and measure system response to these disturbances. For example, the terminal voltage of the DG could be varied at a very slow rate. Such voltage variations will increase frequency change when the DG is feeding into an islanded section of the

distribution network; and hence, improve the accuracy and response time of the frequency change methods. Another example of active techniques is to measure the system impedance by analyzing the system response to high frequency signals. The impedance can vary over a wide range depending on the availability of the entire distribution system.

Some of the features of DG side islanding detection methods can be described as follows:

- These methods are simple and inexpensive as compared to utility side methods, since they don't require an additional communication network or complex multi-signal processor units.
- These methods are unreliable when the load-generation mismatch is small. When a distributed generator, delivering close to zero amount of power, is islanded; the change in magnitude of quantities being monitored, i.e. voltage or frequency, may not be detectable by the detection device.
- The utility has no means to control or monitor the tripping of the DG.
- Most local methods are subject to nuisance tripping.

2.1.2 Utility Side Islanding Detection

These methods detect islanding based on information collected at remote sites, and communicating the trip signal to disconnect the DG in case of islanding. An example of these methods is the transfer trip of generators using SCADA-based telecommunication technologies.

In a telecommunication-based method, each DG site has a receiver, and all circuit breakers in the line leading up to the DG site from the station have transmitters. The state of the CB auxiliary contacts is constantly monitored and the transmitters send this information to a centralized control station. When a switching operation causes a loss of grid, a logical function determines the islanded areas. Then a transfer trip scheme is used to open the inter-ties connecting the islanded DG's to the grid.

Similar setup is used in the Relay Telecom Protection Scheme. The only difference is that the relay-telecom method takes advantage of the RS 232 - 485 communication ports available in the protective devices to exchange information.

Features of the utility controlled methods can be summarized as:

- They are direct
- They are not subject to nuisance tripping.
- They are under direct control of the utility.
- The same system can provide a signal to enable the re-connection of the DG after the fault clearance.
- All circuit breakers leading up to a DG must be monitored. In other words, each breaker needs a transmitter. This increases the cost and complexity of the system.

2.1.3 Limitations of conventional Islanding detection methods

Currently, telecom based is the most commonly used utility side islanding detection method. Current telecom technologies can be easily employed for islanding

detection. However, the cost is much higher as compared to DG side techniques, particularly in areas where DG owners must provide their own radio coverage. The fact that each breaker needs a transmitter increases the cost and complexity of the system. Due to the practice of feeder configuration (i.e. part of the feeder reconnected to another feeder), the situation could become very difficult to manage, even if the telecom cost were acceptable. Another problem is to fit into the required fault-clearance time in order to trip the inter-tie breaker before the re-connection of the system and the DG. The traffic-management of information is done by a Programmable Logic Controller (PLC) in the power and transformer stations. The scan cycle of the PLC adds a considerable time delay between the detection of islanding and operation of the protection device.

Because of the above difficulties, recent research effort and product development has focused on the DG side detection schemes. Of all the DG side techniques rate of change of frequency (*ROCOF*) is probably the most popular. A few commercial products based on this principle have been developed and employed in the field. It is a simple and reliable method, as long as the load connected to the DG during islanding is significantly larger than the DG capacity. But if the load-capacity mismatch is very small, the scheme is not as reliable. Other passive schemes such as rate of change of voltage, current, power, or reactive power, exhibit the same drawback.

To improve upon the passive techniques, the active schemes require injection of small disturbances into the system at the DG terminals. These methods can cause other problems. As all DG's need to inject disturbances into the system, the potential

interactions among DG's can affect system performance and protection device operation. The idea of injecting high frequency signals at DG terminals to monitor system impedance will encounter the same problem.

From the point of view of medium and small distributed-generators, we can conclude that, at the moment, there is no method or protective system that guarantees reliable operation and low cost implementation. Hence, there is a need to develop a reliable and economical technology for islanding detection and prevention.

2.2 Alberta/IEEE Guidelines for DG Interconnections and Islanding Detection

Alberta and most other provinces and states have developed standard guidelines for DG interconnection. IEEE/ANSI Std. 1001-1988 provides details on protection requirements for DG facilities. This section describes the contradictions in these guidelines in regard to islanding detection. While this discussion refers specifically to the Alberta Guidelines, as stated above, other states and provinces have similar guidelines.

Every generating facility is required to have under/over frequency and under/over voltage relays. These relays, in turn, are required to have time delay capability, and the delay between detection of an abnormal condition and tripping of circuit breaker (if the disturbance persists) to disconnect the DG from the distribution network is a function of the magnitude of disturbance. Table 2.1 shows the time delay requirements for tripping by under/over frequency relay. Under/over voltage relay

operation requirements are shown in table 2.2. These delays are required to prevent CB tripping due to temporary faults or disturbances on the network. This is necessary to avoid nuisance tripping, which can aggravate a minor disturbance by removing an energy source (DG) from the network.

Under Frequency Limit	**Over Frequency Limit**	**Minimum Time**
60.0 – 59.5 Hz	60.0 – 60.5 Hz	N/A (continuous operation)
59.4 – 58.5 Hz	60.6 – 61.5 Hz	3 minutes
58.4 – 57.9 Hz	61.6 – 61.7 Hz	30 Seconds
57.8 – 57.4 Hz		7.5 Seconds
57.3 – 56.9 Hz		45 Cycles
56.8 – 56.5 Hz		7.2 Cycles
Less than 56.4 Hz	Greater than 61.7 Hz	Instantaneous trip

Table (2.1): Under/Over Frequency Relay delay settings

RMS VOLTAGE	**TRIP TIME**
$V \leq 50\%$ (of Nominal Voltage)	Instantaneous
$50\% < V < 90\%$	120 Cycles
$90\% < V < 106\%$	No Trip
$106\% < V < 120\%$	30 Cycles
$V \geq 120\%$	Instantaneous

Table (2.2): Under/Over Voltage Relay delay settings

Risk of an out-of-phase recloser operation also increases due to these time delays. Reclosing can take place while the relay waits for the required time to elapse before tripping the CB, when the DG is islanded. As can be seen from the two tables, if an islanded DG is able to maintain a frequency of 57.5Hz and a voltage at 70% of the nominal voltage, it will stay connected to the network for at least 2 seconds, which is enough time for the recloser to operate, and potentially damaging the DG and/or causing voltage transients.

To avoid situations like the above, some utilities require that the location of the DG should be such that if it is islanded, there is enough load in the island to cause frequency/voltage change requiring an instantaneous tripping of the inter-connecting CB. However, it is not always possible to pick and choose DG location since it is dictated by proximity to the source of energy, such as a river for hydro generation or flare gas in the case of co-generation plants. It is, therefore, absolutely necessary to identify an islanding condition and distinguish it from other system disturbances for safe and reliable operation of DG's in parallel with the utility.

2.3 Islanding Detection by Distribution Line Signalling

To overcome the problems associated with present islanding detection methods, a power line signaling based scheme is proposed at the University of Alberta. A signal is broadcast continuously over the distribution line. The signal is generated and coupled on

to the distribution line at the substation, and all DG facilities are equipped with signal detectors (see figure 2.1).

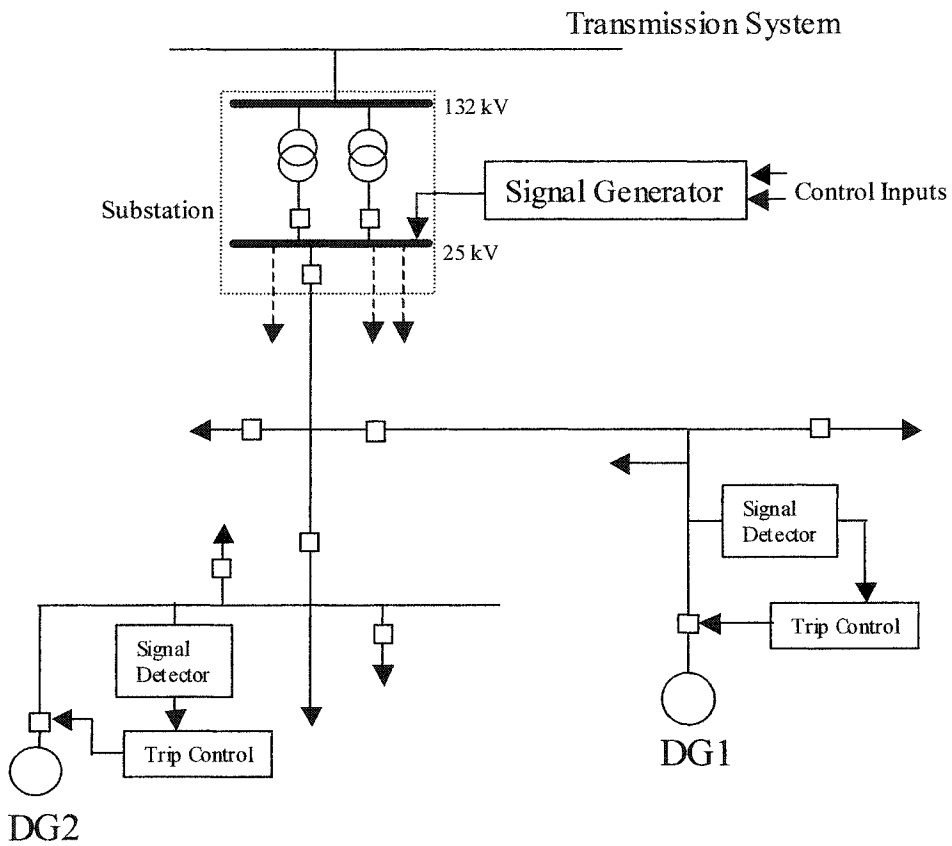

Figure (2.1): Proposed Islanding Detection Scheme

A signal detector can detect the signal unless the DG is islanded or signal broadcast is halted, in which case, the signal can no longer be detected and the DG is disconnected from the distribution line. This scheme is simple and fundamentally different from the published methods and has a combination of the best features of telecommunication based and DG side detection methods.

2.3.1 Islanding Detection: Main Requirements

When implementing an islanding detection method, a few concerns have to be addressed. The following lists some of the "must have" attributes of any islanding detection scheme:

- A very high degree of reliability of the detection system is required. Once the power in the main feeder is lost, the utility will rely on this protection scheme to disconnect the DG from the feeder. The utility does not, however, have any means to confirm if the DG has been disconnected.

- The response time of the system is of utmost importance. Reclosers usually operate within one second. If the recloser operation takes place before the DG is disconnected from the system, the DG, being out of synchronism with the distribution system, can get damaged. Therefore, the detection of islanding and subsequent tripping of the DG should take place within a few cycles (~500ms).

- The detection system must be accurate. If a nuisance tripping takes place, the quality of power supply to the consumers might be compromised due to the unavailability of DG as an energy source.

- In the case of power failure at one feeder, the connected loads are sometimes switched on to another feeder. It is therefore necessary that the detection system be able to operate under these circumstances.

2.3.2 Selection of Signalling Technology

The proposed method involves the broadcast of signal on the distribution line. The distribution network is designed to provide maximum efficiency at 60 Hz and is a hostile medium for high frequency signals. An extensive review of available signalling technologies was conducted at the University of Alberta. Factors such as length of feeders, dynamic nature of the distribution system, signal attenuation due to capacitor banks, noise sources, and effect of signalling on power quality were considered. After the review, it was concluded that *zero-crossing distortion* technique was the most suitable technology for islanding detection [13]. In the signal generation scheme, system voltage waveform is altered near zero crossing, and this change is detected by comparing two consecutive cycles, only one of which has its waveform altered. Signal attenuation is minimal since the signal is transient oscillatory in nature and has 60Hz as its major harmonic component. This technique has been employed for AMR by ATCO and is patented under US patent no. 4658238 [10, 1].

2.3.3 Signal Generation

Signal generation involves altering the system voltage waveform near zero crossing points by drawing small current pulses from the substation transformer winding. The signal generator consists of a switching circuit connected across the substation transformer. Current pulses are drawn near zero crossing points of voltage waveform through an impedance which is essentially a current limiting series R-L circuit.

In the equivalent circuit diagram in Figure 2.2, leakage reactance of substation transformer is represented by L_i and winding resistance by R_i. 'S' is a switching device such as SCR. When switch S is closed, current i_c flows through the control impedance that consists of resistance R_C and inductance L_C. A narrow triggering pulse enables the self-commutating SCR to start conducting and the conduction stops once the current i_c reaches zero value [1].

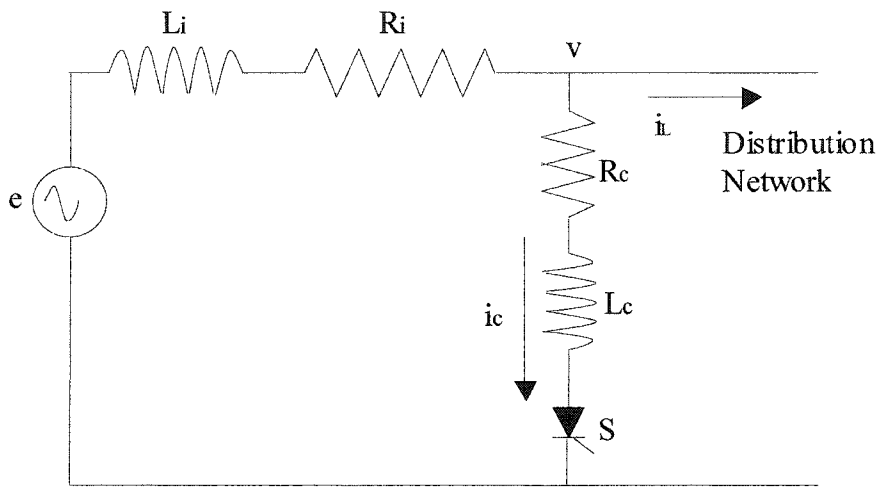

Figure (2.2) Equivalent Circuit Diagram for Zero-crossing Distortion Signal Generation

From the circuit analysis point of view, if 'e' is the transformer induced voltage and i_L is the load current. The voltage at feeder terminals at any given moment:

$$v = e - (R_i + L_i \frac{d}{dt})(i_c + i_L) \quad \ldots\ldots\ldots\ldots\ldots (1)$$

Where i_L is the load current

Assuming that there are no energy storage devices in the distribution network and that load current can be subtracted from the total current coming out of the transformer,

the difference between a modulated and a non-modulated voltage cycle can be derived using equation (1) as:

$$e_{mod} = -\left(R_l + L_l \frac{d}{dt}\right) i_c \qquad \text{for} \qquad t_1 < t < t_2$$

$$e_{mod} = 0 \qquad \text{for} \qquad \begin{matrix} 0 \le t \le t_1 \\ t_2 \le t \le 2\pi \end{matrix}$$

Where e_{mod} represents the difference in voltage in a modulated and a non-modulated cycle.

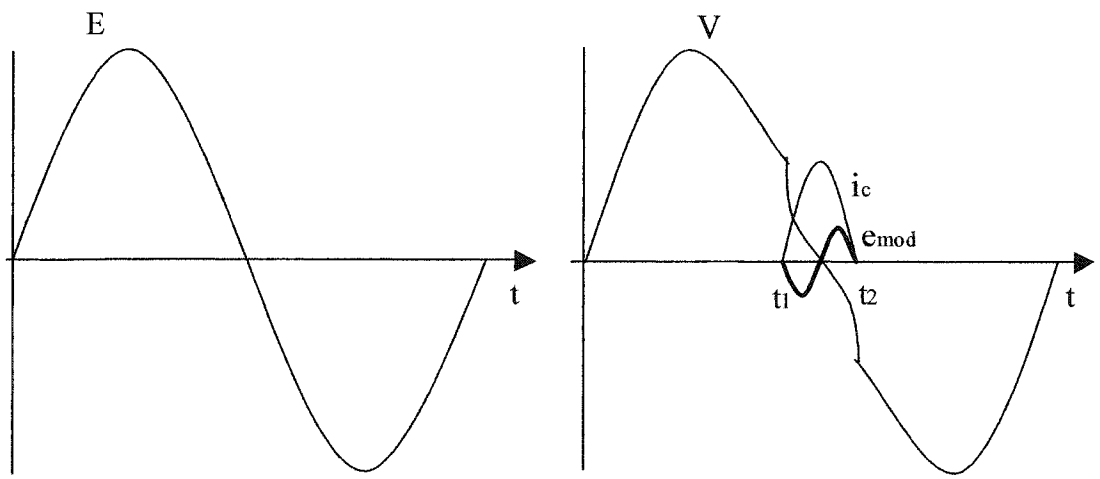

Figure (2.3) Zero crossing Distortion - Signal Generation Waveforms

Leakage impedance of substation transformers can range between 6 to 10% of the base impedance[1] at rated system frequency [1]; therefore, a significant drop in voltage

[1] Base Impedance = $\left[\frac{(\text{Base kV})^2}{\text{Base MVA}}\right]$; Base kV and MVA refer to rated kV and MVA of the transformer.

takes place even with smaller current pulses. For example, on a 5MVA, 11kV transformer, a current pulse of 25A peak is enough to cause a peak voltage dip of 2% of rated voltage. As shown in figure 2.3, the current pulse lasts till the current through control impedance hits zero, after which conduction stops.

The above derivation does not take into account the effects of energy storage devices i.e. inductors and capacitors in the distribution network or the change in load current after switch 'S' is closed. Signal-generation phenomenon is explained below by means of a numerical example. Note that the circuit has been simplified for ease of calculations. The load and the feeder are lumped together and the entire capacitance in the circuit has been represented by a capacitor at the substation end of the line. The control impedance has been replaced by a resistance element.

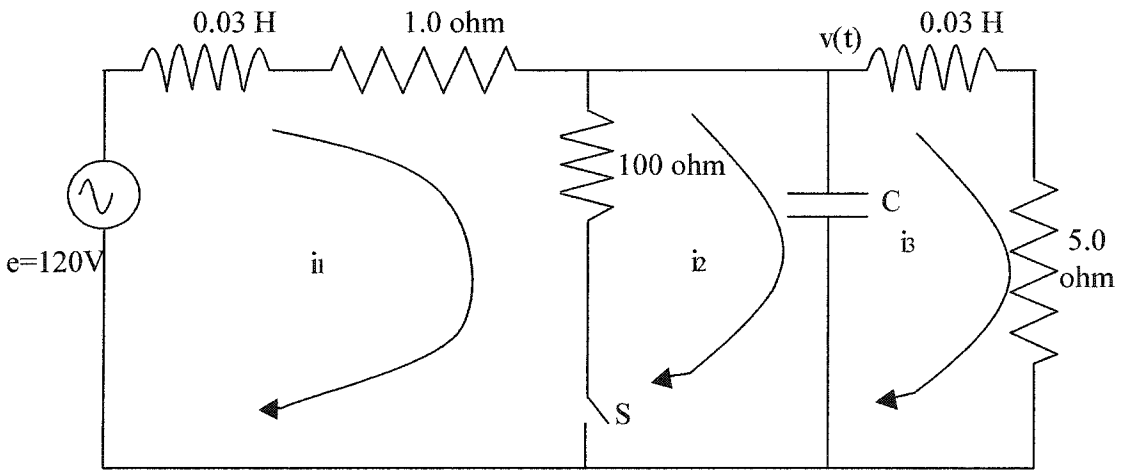

Figure (2.4): Signal Generation Analysis

To fully compensate the load in Figure 2.4, C = 196.2 μF. If switch 'S' is open before t = 0 and the circuit is in steady state condition, for a 60 Hz system voltage and current phasors can be represented as:

$$v(t) = 154.711\sin(\omega t + 150)$$
$$i_1(t) = i_2(t) = 5.0589\sin(\omega t + 150)$$
$$i_3(t) = 12.511\sin(\omega t + 83.8502) \qquad \text{for } -\infty < t \le 0$$
$$e(t) = 120\sqrt{2}\sin(\omega t + 169.7028)$$

Initial conditions can thus be determined as:

$$i_1(0) = 2.52945A$$
$$i_3(0) = 12.4394A$$
$$v(0) = 77.3555V$$

Switch 'S' is closed at t = 0 and the mesh-analysis equations can be written as:

$$0.03\frac{di_1(t)}{dt} + 101i_1(t) - 100i_2(t) = e(t) \quad \text{.....(1)}$$

$$-100i_1(t) + 100i_2(t) + \frac{1}{192.2e-06}\int_{-\infty}^{t} i_2(t)dt - \frac{1}{192.2e-06}\int_{-\infty}^{t} i_3(t)dt = 0 \quad \text{.....(2)}$$

$$-\frac{1}{192.2e-06}\int_{-\infty}^{t} i_2(t)dt + 0.03\frac{di_3(t)}{dt} + 5i_3(t) + \frac{1}{192.2e-06}\int_{-\infty}^{t} i_3(t)dt = 0 \quad \text{.....(3)}$$

Taking Laplace's transform for equations 1,2 and 3, we get

$$(0.03s+101)I_1(s)-100I_2(s)=E(s)+0.03(2.52945).....(4)$$

$$-100I_1(s)+(100+\frac{5097}{s})I_2(s)-\frac{5097}{s}I_3(s)=\frac{-77.3555}{s}.....(5)$$

$$-\frac{5097}{s}I_2(s)+(0.03+100+\frac{5097}{s})I_3(s)=0.03(12.4394)+\frac{77.3555}{s}.....(6)$$

From 4,5 and 6, we get

$$\begin{bmatrix} 0.03s+101 & -100 & 0 \\ -100 & 100+5097/s & -5097/s \\ 0 & -5097/s & 0.03s+5+-5097/s \end{bmatrix}\begin{bmatrix} I_1(s) \\ I_2(s) \\ I_3(s) \end{bmatrix}=\begin{bmatrix} E(s)+0.076 \\ -77.35/s \\ 0.373+77.35/s \end{bmatrix}$$

and

$$\Delta=\begin{vmatrix} 0.03s+101 & -100 & 0 \\ -100 & 100+5097/s & -5097/s \\ 0 & -5097/s & 0.03s+5+-5097/s \end{vmatrix}$$

Roots of 's' in Δ will determine the frequency of oscillation and its decay rate.

Expanding Δ and determining roots of *'s'* we get:

$$\Delta=\frac{0.09}{s}\left[(s+100.65)\left\{(s+75.16)^2+(578.59)^2\right\}\right]$$

We now calculate Δ_1, Δ_2 and Δ_3 by replacing the corresponding column in Δ by the terms on right hand side of equations 4, 5 and 6.

$$\Delta_1 = \begin{vmatrix} 120\sqrt{2}\left(\frac{0.17875s - 370.928}{s^2+\omega^2}\right) + 0.07588 & -100 & 0 \\ \frac{-77.355}{s} & 100 + \frac{5097}{s} & -\frac{5097}{s} \\ 0.3732 + \frac{77.3555}{s} & -\frac{5097}{s} & 0.03s + 5 + \frac{5097}{s} \end{vmatrix}$$

$$\text{or } \Delta_1 = \frac{120\sqrt{2}}{s}\left(\frac{0.53625s^3 - 996.076s^2 - 198515101.7}{s^2+\omega^2}\right) + \frac{1}{s}\left(0.22765s^2 - 182.5214s + 192144.8264\right)$$

and

$$I_1(s) = \frac{\Delta_1}{\Delta} = \frac{120\sqrt{2}}{0.09}\left(\frac{0.53625s^3 - 996.076s^2 - 198515101.7}{(s^2+\omega^2)(s+100.65)\{(s+75.16)^2 + 578.59^2\}}\right) + \frac{1}{0.09}\left(\frac{0.22765s^2 - 182.5214s + 192144.8264}{(s+100.65)\{(s+75.16)^2 + 578.59^2\}}\right)$$

taking Inverse Laplace Transform

$$i_1(t) = 6.306\sin(\omega t + 144.85^\circ) - 0.1278e^{-100.65t} + 1.0361e^{-75.16t}\sin(578.59t - 69.86^\circ) \quad \text{.....(7)}$$

Similarly,

$$i_2(t) = 4.829\sin(\omega t + 144.85^\circ) - 0.1252e^{-100.65t} + 1.0387e^{-75.16t}\sin(578.59t - 59.89^\circ) \quad \text{.....(8)}$$

$$i_3(t) = 11.943\sin(\omega t + 78.70^\circ) - 0.13036e^{-100.65t} + 1.0257e^{-75.16t}\sin(578.59t + 123.27^\circ) \quad \text{.....(9)}$$

$$\text{and } v(t) = 0.03\frac{di_3(t)}{dt} + 5i_3(t)$$

$$\therefore v(t) = 147.6924\sin(\omega t + 144.85) - 0.258178e^{-100.65t} + 18.02587e^{-75.16t}\sin(578.59t + 204.282^\circ) \quad \text{.....(10)}$$

current through 100Ω resistor

$$i_s(t) = i_1(t) - i_2(t) \quad \text{.....(11)}$$

From equations 7, 8 and 11, it is determined that i_s reaches zero at t = 0.0013496 sec or 29.1514° after 'S' is closed.

We assume that 'S' is an ideal switch that opens instantly after current through it reaches zero. The circuit conditions at this instant t = t_0 = 0.0013496 sec, serve as initial conditions in circuit-analysis for the period when 'S' is opened again.

$i_1(t_0) = 0.1496$ A

$i_3(t_0) = 11.4472$ A

$v(t_0) = -0.00094$ V

Using mesh analysis, we get the following equations:

$$i_1(t) + 0.03\frac{di_1(t)}{dt} + \frac{1}{192.2e-06}\int_{-\infty}^{t} i_1(t)dt - \frac{1}{192.2e-06}\int_{-\infty}^{t} i_3(t)dt = e(t) \quad \text{.....(12)}$$

$$-\frac{1}{192.2e-06}\int_{-\infty}^{t} i_1(t)dt + 0.03\frac{di_3(t)}{dt} + 5.0i_3(t) + \frac{1}{192.2e-06}\int_{-\infty}^{t} i_3(t)dt = 0 \quad \text{.....(13)}$$

Again, solving equations 12 and 13 by Laplace's Transform method we get,

$$i_1(t) = 5.0589\sin(\omega t + 150°) + 0.01626e^{-101.32(t-t0)} + 0.148e^{-49.318(t-t0)}\sin(576.99t + 23.37°) \quad \text{.....(14)}$$

$$i_3(t) = 12.511\sin(\omega t + 83.85°) + 0.0169e^{-101.32(t-t0)} + 0.145e^{-49.318(t-t0)}\sin(576.99t - 143.43°) \quad \text{.....(15)}$$

$$v(t) = 154.711\sin(\omega t + 150) + 0.0331e^{-101.32(t-t0)} + 2.569e^{-49.318(t-t0)}\sin(576.99t - 64.92°) \quad \text{.....(16)}$$

Equations (10) and (16) represent the phenomenon of damped transient oscillation generation in an active network. A plot of voltage waveform with and without operation of switch 'S' and difference in two waveforms is shown in Figure 2.5.

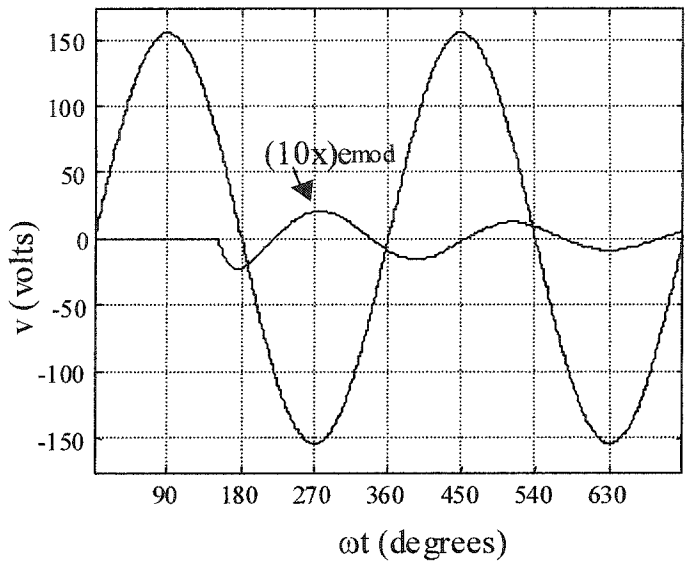

Figure (2.5): Numerical example- calculated e_{mod} and 'v' plot

The analysis shows that due to the switching, transient oscillations of current take place on the feeder, which in turn cause transient oscillatory voltage drops. Two distinct oscillations take place, one after the switch is closed and the other after the switch has been opened again.

2.3.4 Signal Generator

In a preferred implementation of signal generation, a step down transformer is used to isolate the switching device and gate control circuit from higher voltage levels. Figure 2.6 describes the working of the signal generator.

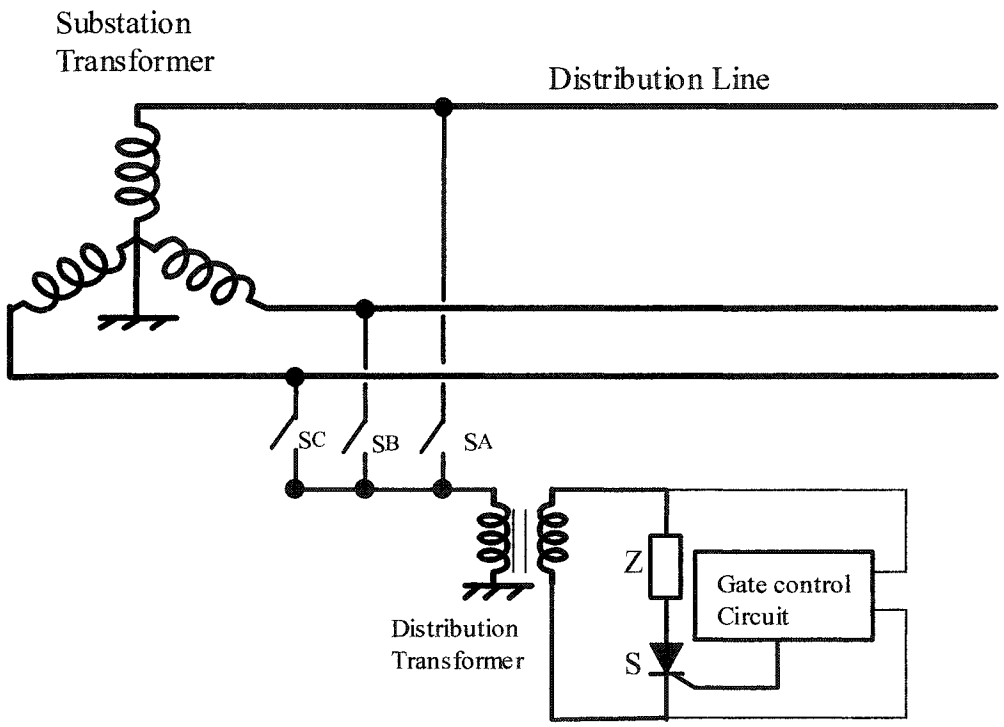

Figure (2.6): Signal Generation – Line to Neutral Switching

By using switches S_A, S_B, and S_C, it is possible to use any one of the three phases for signal broadcasting. At any given time, only one of the three switches is closed. The voltage wave is modulated, by triggering thyristor 'S' with a gate pulse just before zero crossing. The shown implementation is for phase to neutral switching but line-to-line

switching is also possible with a similar switching and control set-up. 'Z' consists of an R-L series circuit and the value of 'Z' is such that a detectable signal is generated under all load conditions. As will be discussed in the following sections of this report, with increasing load, signal strength decreases.

Figure 2.7 shows the schematic diagram of a gate control circuit. The voltage stepped down at distribution transformer is further reduced to instrumentation levels and fed to a bridge rectifier. After rectification and filtering, a potential divider R1-R2 is connected across the DC voltage. Voltage across R2 feeds into one input of a comparator. The reduced voltage (sinusoidal) is connected to the other input of the comparator. The values of R1 and R2 are such that voltage across R2 is equal to the instantaneous value of sinusoidal voltage at which switching is desired (φ = 150 - 155°).

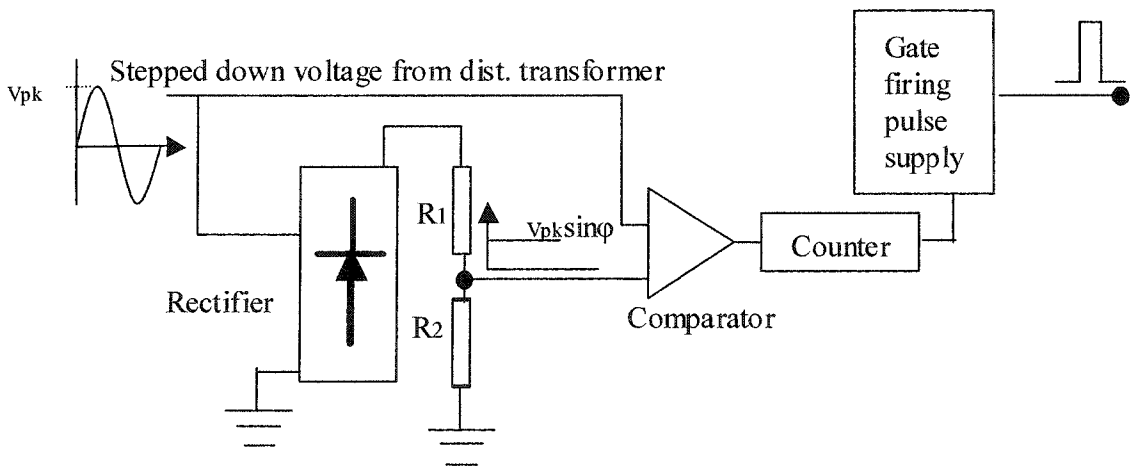

Figure (2.7): Firing Pulse Circuit Block Diagram

The comparator operates in only one direction – falling or rising, depending upon detection requirements. For modulating every fourth cycle of the voltage wave, the counter is set at four and reinitializes to zero after four pulses at its input. A high counter output triggers the firing pulse.

In Figure 2.8, 'S' is a pulse triggered SCR. The timing of the gating pulse is such that SCR starts conducting at 25 to 30° before positive to negative zero crossing and the pulse width is just enough to start SCR conduction as shown in the figure.

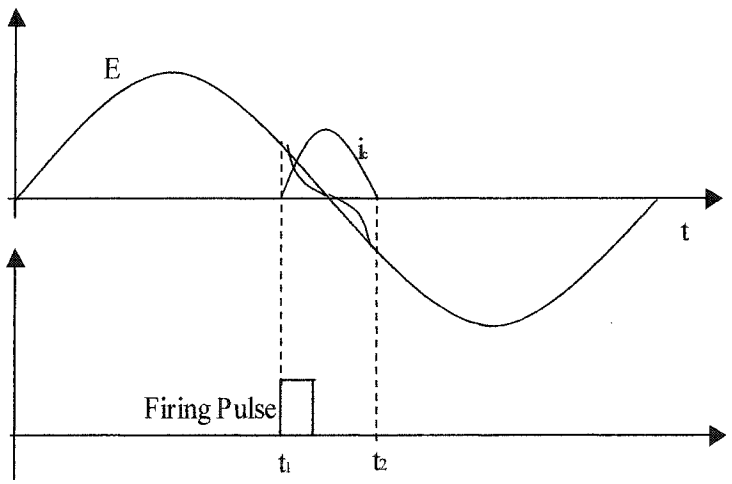

Figure (2.8): Triggering Pulse for Signal Generation

As soon as the current through SCR reaches zero, conduction must stop. This is easily achievable with self-commutating switching devices such as thyristors. Signal detection involves comparing un-modulated and modulated cycles of the voltage wave;

therefore, two consecutive cycles cannot be modulated. In the preferred scheme one in every three or four cycles is modulated.

2.3.5 Signal Detection

Signal detection involves comparing two voltage waveform cycles, only one of which has been modulated. As the distortion of the wave is centred near the zero crossing point, it provides locations for timing and signal search for detection. Current techniques of signal detection are slope-based detection techniques. These schemes exploit the fact that the slope of voltage wave near zero crossing points in a modulated cycle is different from that in an unmodulated cycle. Figure 2.9 shows implementation of one such technique.

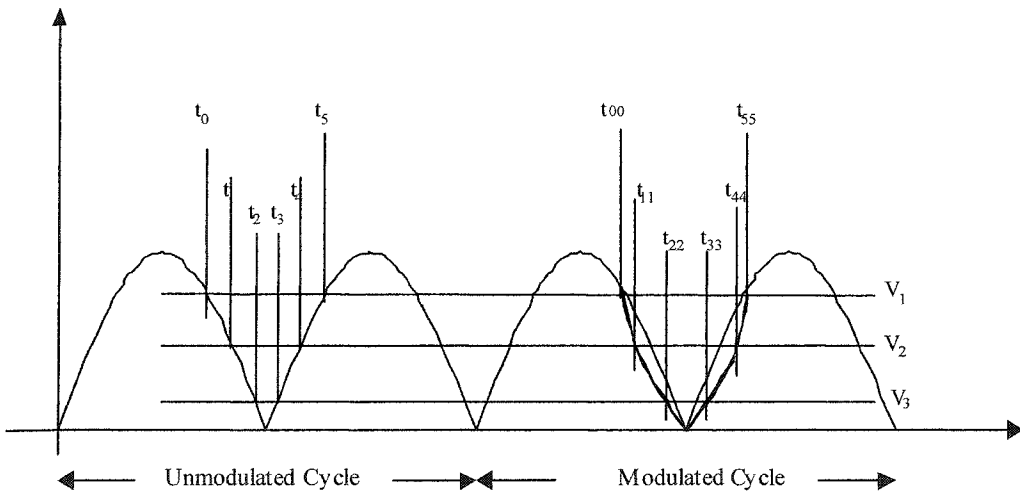

Figure (2.9): Outbound Signal Detection [11]

As shown in this figure, multiple voltage levels are set, and the time taken to go from one voltage level to the next is recorded. It can be seen that time intervals are different for modulated and unmodulated cycles. Similarly, voltage levels can be recorded at fixed time intervals and based on difference in voltage levels, the presence or absence of signal can be determined. With changing system conditions, such as load and VAR compensation levels, location of maximum slope variation in the waveform will also change. Signal detection accuracy can be enhanced with a detection method that can detect signal under all system conditions.

Signal Detection is the most critical part of the proposed scheme and the main focus of this thesis. A DG stays connected to network as long as the signal can be detected. This raises a new concern: if signal is temporarily lost due to a system disturbance while the DG is not islanded, a nuisance tripping will take place. To avoid nuisance tripping, the detection system should have a ride through capability i.e. the breaker control should trip the CB only if the signal is undetectable for a certain length of time. The maximum ride through period will be dictated by the recloser operation time. Reclosers usually operate within 1sec; therefore, a ride-through period in the range of 200ms or 10-15 cycles is appropriate.

2.4 Summary

Limitations of existing techniques discussed in section 2.3.1 have prompted a great deal of research effort towards reliable islanding detection methods. The proposed

islanding detection scheme is expected to perform virtually under all system conditions. The proposed scheme requires the broadcast of signal over the distribution lines and its detection at DG facilities. Signal detection is a critical component of the proposed scheme and requires a new signal monitoring method suitable for islanding detection. An islanding detection specific signal detection technique is presented in this thesis. Reliability of signal detection can be improved and a ride through mechanism implemented with the new detection method.

Chapter 3

SIGNAL PROPAGATION CHARACTERISTICS

3.0 Introduction

In the previous chapter an islanding detection scheme employing distribution line signaling was described, and the signal generation was discussed in detail. In this chapter, signal characteristics are analyzed. This analysis dictates the requirements of the signal detection method. The effects of change in load and reactive power compensation level are described using the Laplace Transform method of circuit analysis and PSCAD simulation programs.

3.1 System Operating Conditions & Signal Characteristics

Distribution network is a dynamic system; i.e. one in which operating conditions keep on changing from time to time. For example, load on a feeder can change over a wide range throughout the day. Similarly, capacitor banks are switched in and out of the network to optimize the reactive power compensation. As the distribution line is the signal transmission medium, changing network conditions will affect signal characteristics. From a signal detection point of view, it is vital that these changes be taken into consideration while implementing a detection method to achieve consistently accurate results. In this section, we will discuss the effects of changing loads and reactive power compensation levels.

Signal characteristics are discussed in an IEEE paper [1] which discusses the tests indicating that signal strength increases by as much as 30% and the frequency is higher at off-peak load hours when the loads are light and many capacitor banks are switched off, as compared to peak-load hours. Frequency of oscillation is a function of system parameters and ranges between 240 – 600Hz [2,3]. These results were verified using PSCAD simulation software and lab experiments.

3.1.1 Physical Model of Distribution Line

The process of signal generation can be viewed as an intentional introduction of a controlled disturbance or fault at a substation. This disturbance causes transients that propagate throughout the network. The magnitude and shape of these transients will be different at different locations in the network. At any given time the magnitude and shape of a transient oscillation will depend on factors such as capacitance in the system, load, and magnitude of the disturbance.

A simple single feeder distribution line model is shown in Figure 3.1. The model consists of a transformer represented as a voltage source 'e' with a series impedance R_1-L_1, a distribution line (T model) with branches R_2-L_2, R_3-L_3 and capacitor branch 'C', a load represented by R_4-L_4, and a switch 'S' in series with an R-L impedance. R-L represents the control impedance used to limit the switching current.

During steady state conditions, switch 'S' is open, and the voltages and currents flowing in all branches are as shown in Figure 3.1. The values of currents and voltages at

the time of switching serve as initial conditions for transient analysis when 'S' is closed. 'S' is opened after the current flowing through it reaches zero, and we are interested in system response during the time period when 'S' is closed, and after 'S' is opened again.

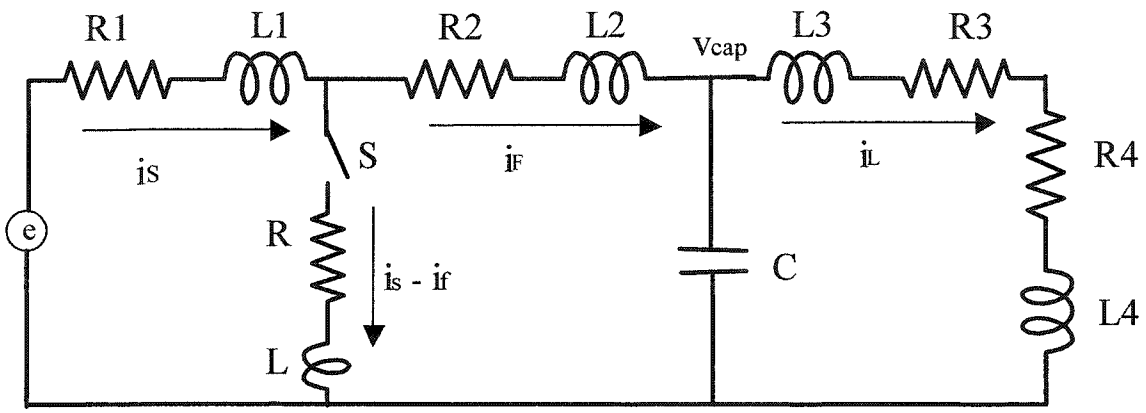

Figure (3.1): Linear Lumped Parameter Model of a Distribution Feeder

Three regions of interest in the analysis of each signal-generation event can be described as:

1) 'S' is open and system operates under steady state conditions $[-\infty < t < 0]$

2) 'S' is closed $[0 \leq t < t_0]$

3) 'S' is open $[t > t_0]$

Where '0' represents the moment when 'S' is closed and t_0 refers to the moment when 'S' is open again.

The first part is a simple load flow problem, and its solution will give initial conditions for the second part. For transient analysis, the circuit can be described by the following differential equations:

$$\frac{di_s}{dt} = \frac{1}{k}\left[(L + L_2)e - (R_1L + R_1L_2 + RL_2)i_s - (LR_2 - RL_2)i_f - Lv_{cap}\right]$$

$$\frac{di_f}{dt} = \frac{1}{k}\left[Le - (R_1L - RL_1)i_s - (R_2L_1 + R_2L + RL_1)i_f - (L1 + L)v_{cap}\right]$$

$$\frac{di_L}{dt} = \frac{1}{(L_3 + L_4)}\left[v_{cap} - (R_3 + R_4)i_L\right]$$

$$\frac{dv_{cap}}{dt} = \frac{1}{C}\left[i_f - i_L\right]$$

where $k = L_1L + L_1L_2 + LL_2$

From the above set of equations, it can be seen that the magnitude and frequency of a transient oscillation is a function of inductance and capacitance in the line as well as system operating conditions. However, it will be difficult to say the least, to do analytical calculations for the above system manually. Therefore, the system is further simplified.

3.1.2 Circuit Analysis using a Simplified Model

The circuit of Figure 3.1 is further simplified to perform analytical calculations manually. Purpose of these calculations is to describe the phenomenon of transient oscillation generation and change in the magnitude and frequency of the oscillation with changing system conditions. The effects of changing load and reactive power compensation levels on the oscillation frequency and magnitude are discussed. The circuit is simplified by bringing the capacitor 'C' at feeder terminals on the substation side, lumping together the line and load impedances as R3-L3; and using only a

resistance element (R2) to limit the current through the switch. Figure 3.2 shows the simplified circuit. The numerical example described in Chapter 2 has again been used for discussion in this section.

R1 and L1 refer to the leakage impedance of the substation-transformer and are therefore constant, R3 is also constant. The variables are R3, L3 and C.

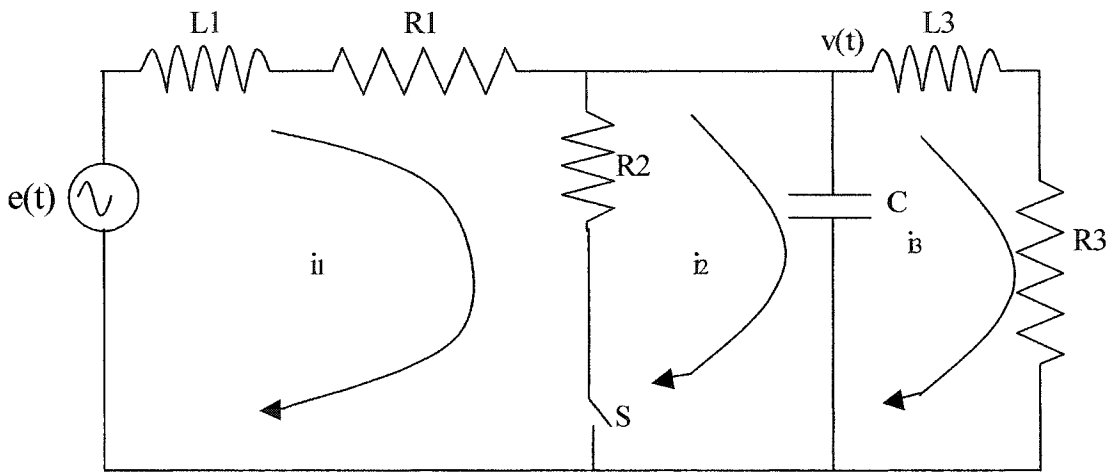

Figure (3.2): Simplified Model of a Distribution Feeder

Before closing switch 'S', the circuit is assumed to be under steady state and initial values of i_1, i_3 and v are calculated. These values will be used to determine initial conditions for the circuit. When 'S' is closed, the circuit equations can be written as:

$$\left.\begin{aligned} L_1\frac{di_1(t)}{dt}+(R_1+R_2)i_1(t)-R_2i_2(t)&=e(t)\\ -R_1i_1(t)+R_2i_2(t)+\frac{1}{C}\int(i_2(t)-i_3(t))dt&=0\\ L_3\frac{di_3(t)}{dt}+\frac{1}{C}\int(i_3(t)-i_2(t))dt&=0 \end{aligned}\right]\text{--I}$$

Using Laplace Transform method, from equation set (I), we get:

$$\begin{bmatrix} L_1s+R_1+R_2 & -R_2 & 0\\ -R_2 & R_2+(Cs)^{-1} & -(Cs)^{-1}\\ 0 & -(Cs)^{-1} & L_3s+R_3+(Cs)^{-1}\end{bmatrix}\begin{bmatrix} I_1(s)\\ I_2(s)\\ I_3(s)\end{bmatrix}=\begin{bmatrix} E(s)+i_1(0)L_1\\ -v(0)/s\\ i_3(0)L_3+v(0)/s\end{bmatrix}\quad\ldots(1)$$

$$\text{and }\Delta=\begin{vmatrix} L_1s+R_1+R_2 & -R_2 & 0\\ -R_2 & R_2+(Cs)^{-1} & -(Cs)^{-1}\\ 0 & -(Cs)^{-1} & L_3s+R_3+(Cs)^{-1}\end{vmatrix}$$

Expanding Δ, a polynomial is obtained the roots of which represent the frequency and the decay coefficient of the disturbance. Determinants Δ_1, Δ_2, and Δ_3 can be obtained by replacing first, second and third columns of Δ respectively with voltage terms on the right side of equation (1). i_1, i_2 and i_3 are calculated by taking Inverse Laplace Transform of determinant ratios as described below:

$$i_n(t)=\mathrm{L}^{-1}\left[\frac{\Delta_n}{\Delta}\right];\ \text{where n}=1,2,3$$

.....(2)

v(t) can then be evaluated as:

$$v(t) = L_3 \frac{di_3(t)}{dt} + R_3 i_3(t)$$

.....(3)

Similarly, for the period after 'S' opens, the magnitudes of currents and voltage just before the opening of the switch will serve as initial conditions. If conduction stops at $t = t_0$, Laplace Transformation of the circuit yields:

$$\begin{bmatrix} L_1 s + R_1 + (Cs)^{-1} & -(Cs)^{-1} \\ -(Cs)^{-1} & L_3 s + R_3 + (Cs)^{-1} \end{bmatrix} \begin{bmatrix} I_1(s) \\ I_3(s) \end{bmatrix} = \begin{bmatrix} E(s) + i_1(t_0)L_1 - v(t_0)s^{-1} \\ i_3(t_0)L_3 + v(t_0)s^{-1} \end{bmatrix}$$

and

$$\Delta = \begin{vmatrix} L_1 s + R_1 + (Cs)^{-1} & (Cs)^{-1} \\ (Cs)^{-1} & L_3 s + R_3 + (Cs)^{-1} \end{vmatrix}$$

The roots of polynomial obtained by expanding Δ will represent the frequency and decay coefficient of the disturbance after the switch is open. Δ_1 and Δ_3 can be calculated in the same manner as before. Currents and voltages will again be calculated using equations 2 and 3.

3.1.3 Effect of Load Variation

A solution was obtained for *v(t)* in Chapter 2 with the following circuit parameters:

L1 = L3 = 0.03 H, C = 196.2 μF, R1 = 1.0 Ω, R2 = 100.0 Ω and R3 = 5.0 Ω

The solution for *v(t)* is re-written here for reference:

$$
\begin{aligned}
&v(t) = 154.711\sin(\omega t + 150°) \\
&\text{for } -\infty < t < 0 \\
&v(t) = 147.692\sin(\omega t + 144.85°) - 0.258e^{-100.65t} + 18.026e^{-75.16t}\sin(578.59t + 204.28°) \\
&\text{for } 0 \le t < t_0 \\
&v(t) = 154.711\sin(\omega t + 150°) + 0.033e^{-101.32(t-t0)} + 2.569e^{-49.34(t-t0)}\sin(577t - 106.54°) \\
&\text{for } t_0 \le t < \infty \\
&\text{where } t_0 = 0.00135\,\text{sec}
\end{aligned}
\qquad \text{.....(4)}
$$

Let's say that load has been reduced such that new values for R3 and L3 are 20Ω and 0.12H respectively with R1, L1 and R3 remaining constant. To have a unity power factor, the capacitance required, C = 49.046 μF.

Solving for v(t), we get the following:

$$v(t) = 167.626\sin(\omega t + 150°)$$

for $-\infty < t < 0$

$$v(t) = 163.381\sin(\omega t + 143.82°) - 0.285e^{-139.78t} + 28.69e^{-132.05t}\sin(917.34t + 205.46°)$$

for $0 \le t < t_0$

$$v(t) = 167.626\sin(\omega t + 150°) + 0.219e^{-140.46(t-t0)} + 8.996e^{-29.768(t-t0)}\sin(919.7t - 121.72°)$$

for $t_0 \le t < \infty$

where $t_0 = 0.001276$ sec

.....(5)

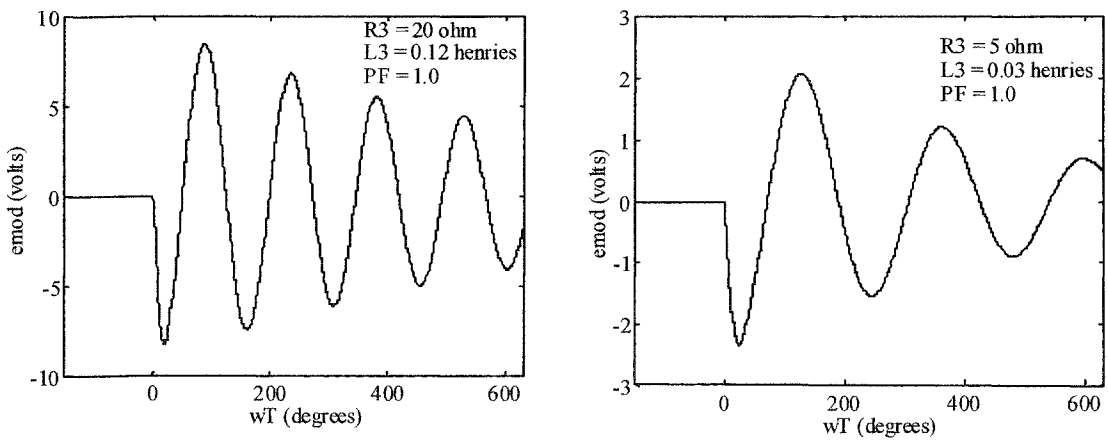

Figure (3.3): Comparison of oscillations at ¼ and full load

Looking at equation sets (4) and (5) and Figure 3.3, we observe the following:

1. The frequency of oscillation has increased.
2. The post fault ($t > t_0$) coefficient of decay for sinusoidal oscillation has decreased and the decay coefficient for the DC component of disturbance has increased.
3. The decay constants during fault ($0 < t < t_0$) have increased.

Note that in Figure 3.3, transient components have been extracted by subtracting the steady-state voltages from their respective transient state voltages. We are interested in post fault behavior of the system and Figure 3.4 shows the effect of increasing load inductance on post-fault decay coefficient if the resistance is constant. Figure 3.5 shows the effect of increasing resistance with constant inductance on post-fault decay coefficient. In each case capacitance is such that the power factor is unity.

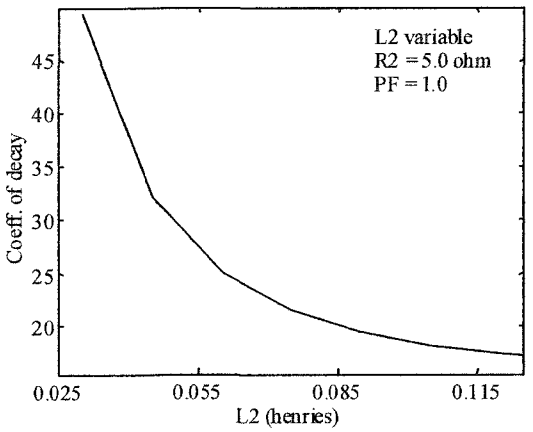

Figure (3.4): Effect of Change in Load Inductance on Post-Fault Decay-Coefficient (Resistance constant)

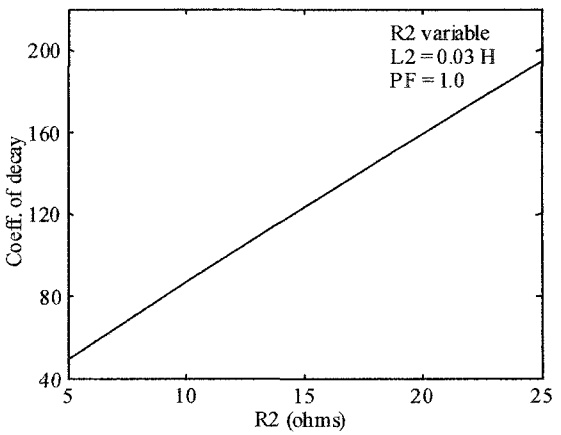

Figure (3.5): Effect of Change in Load Resistance on Post-Fault Decay-Coefficient (Inductance constant)

Figure 3.6 and 3.7 show the change in post-fault decay coefficient and oscillation frequency respectively with decreasing load. Figure 3.6 depicts combined effects of increasing R3 and L3 on post fault decay. As shown in Figures 3.4 and 3.5, while decay rate increases linearly with increasing resistance, it decreases with increase in inductance in a non-linear fashion and the net effect, shown in Figure 3.6, is a decrease in decay rate.

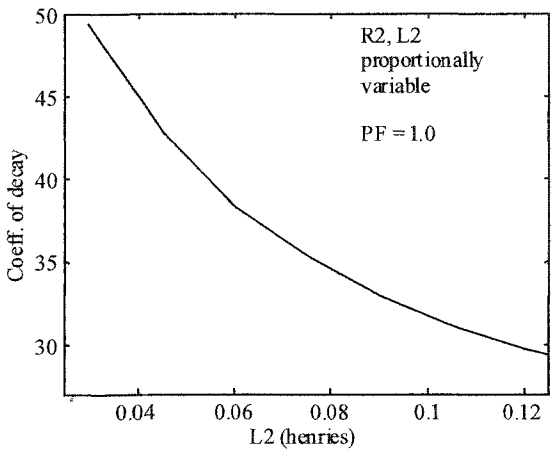

Figure (3.6): Effect of decreasing Load on post-fault decay coefficient (R2, L2 increase proportionally)

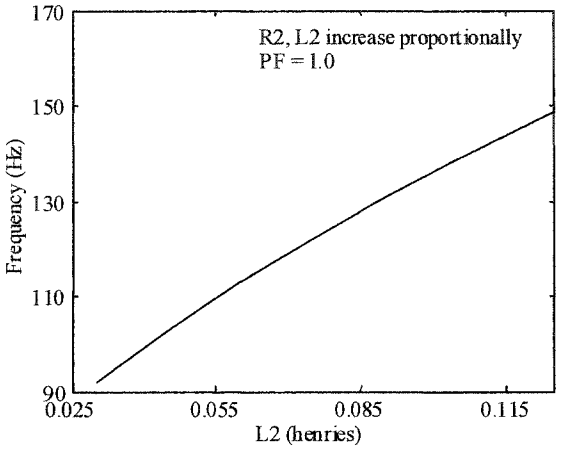

Figure (3.7): Effect of decreasing load on oscillation frequency (R2, L2 increase proportionally)

Following conclusions can be drawn from this analysis:

1. As the capacitance requirements decrease, the frequency of oscillation increases with decreasing loads.
2. The magnitude of the oscillation increases as the load is reduced.
3. The oscillation decay is slower in highly inductive loads and is faster in highly resistive loads.

3.1.4 Effect of VAR compensation level

Using the same numerical example that was discussed in section 3.1.3, we will now analyze the effect of changing reactive compensation level on the oscillation frequency. In the following analysis, calculations are based on less than optimum capacitance in the network.

We use the same circuit parameters except that compensation level is half of what is required to get a unity power factor. Therefore, the circuit parameters in this case will be:

R1 = 1.0 Ω, L1 = L3 = 0.03 H, R2 = 100.0 Ω, R3 = 5.0 Ω

and C = 196.2/2 = 98.1μF

Solving for *v(t)*, we get the following equations:

$$\left.\begin{aligned} v(t) &= 114.0\sin(\omega t + 150°) \\ &\text{for } -\infty < t < 0 \\ v(t) &= 111.1\sin(\omega t + 145.9°) - 0.189e^{-99.98t} + 11.89e^{-100.98t}\sin(821.68t + 205°) \\ &\text{for } 0 \le t < t_0 \\ v(t) &= 114.0\sin(\omega t + 150°) + 0.024e^{-100.66(t-t0)} + 3.56e^{-49.67(t-t0)}\sin(820.18t - 114.27°) \\ &\text{for } t_0 \le t < \infty \\ &\text{where } t_0 = 0.00135\,\text{sec} \end{aligned}\right\} \quad \text{.....(6)}$$

Comparing equation sets (4) and (6) we observe that the oscillation frequency has increased significantly and post fault decay coefficient is almost the same. However, there is an increase in decay coefficient for the period when the switch is closed. Which means that effect of change in 'C' on post fault decay is almost negligible as compared to the effect of changing R3-L3, but with R2 in circuit during current flow through 'S' ($0 < t < t_0$), effect of reduced 'C' on oscillation decay is significant. The magnitude of oscillation peak has also increased slightly.

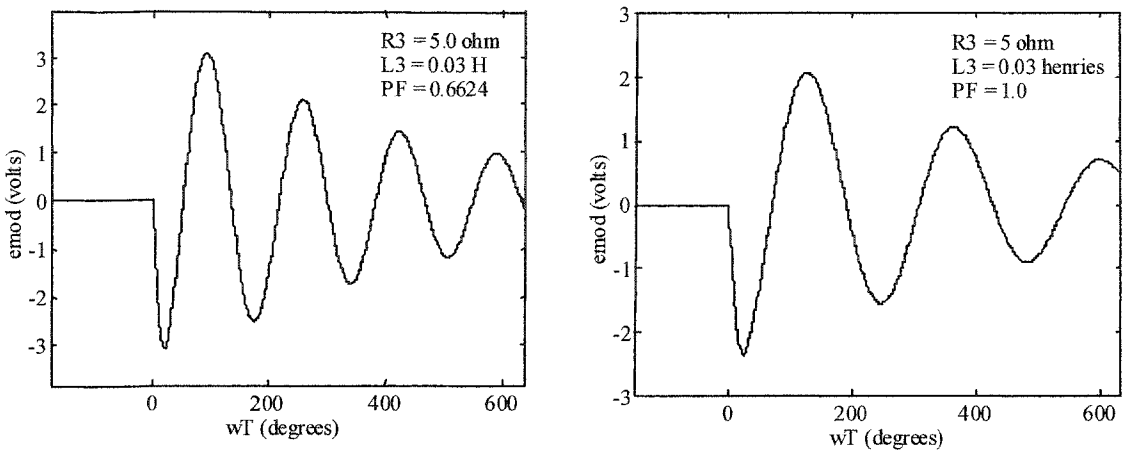

Figure (3.8): Effect of Reactive Compensation level on Oscillation Propagation

From our discussion above, we can conclude that:

1. Frequency of oscillation increases with decreasing reactive compensation level in the system.

2. Post-fault decay rate is relatively unaffected by change in capacitance and is more dependent on resistance to inductance ratio on the load side.

3.2 Analysis by simulation using PSCAD

As higher order differential equations are not so easy to solve manually, simplified single-phase model was used in the previous section for circuit analysis. In this section we use PSCAD simulation software to analyze signal characteristics on a three phase systems. The PSCAD simulation software has built-in mathematical models for electrical components and uses numerical integration techniques to solve differential equations. A three-phase model of a distribution system feeder was used in the

simulations. To measure the system response to signal-generation, the post-disturbance magnitudes of quantities of interest were compared against their steady state or pre-disturbance magnitudes.

Figure 3.9 shows the model used in simulations. The transmission system is presented as an ideal three-phase voltage source connected to a distribution transformer. The distribution transformer in turn is connected to a feeder. A balanced three-phase R-L load is connected directly to the feeder. Following are equivalent circuit parameters for the distribution transformer:

Capacity = 5MVA

Secondary Voltage = 11kV (L-L)

Leakage Impedance = 0.08 p.u.

Thyristor model parameters are:

On Resistance: 0.0 ohm

Off Resistance: 1.0 E08 ohm

Reverse Withstand Voltage: 1.0 E05 kV

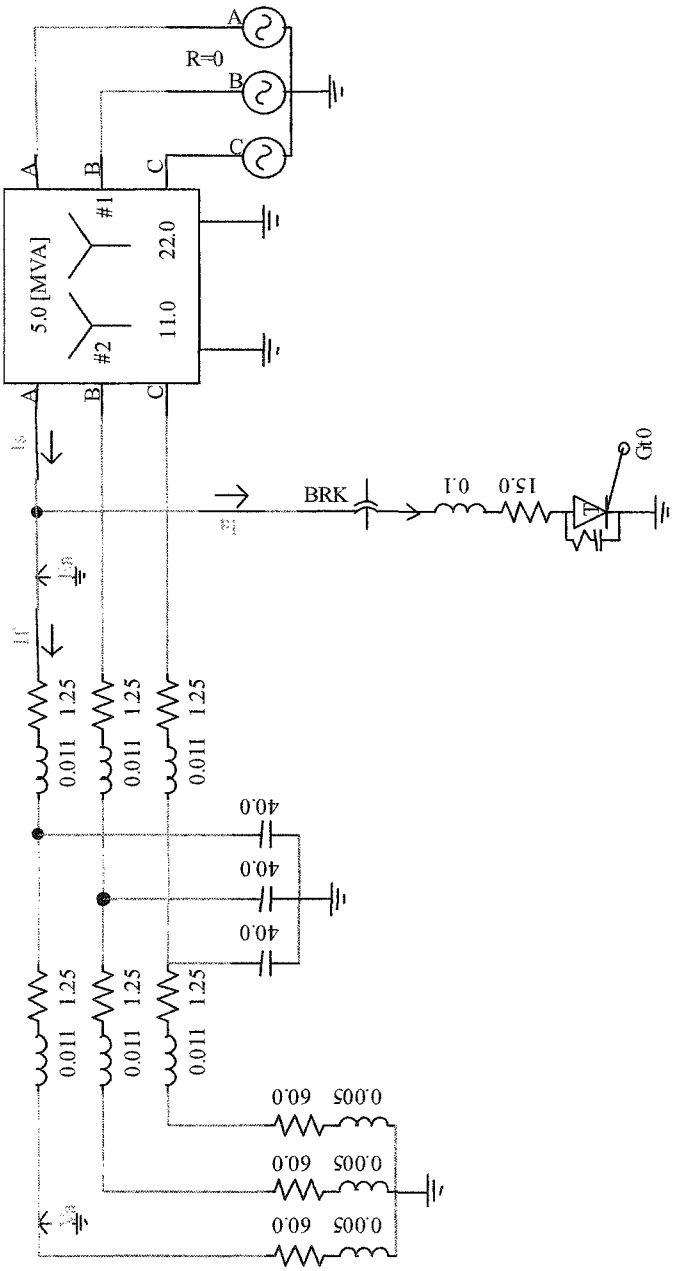

Figure (3.10): Modulating Current and System Voltage Waveforms – PSCAD Simulation

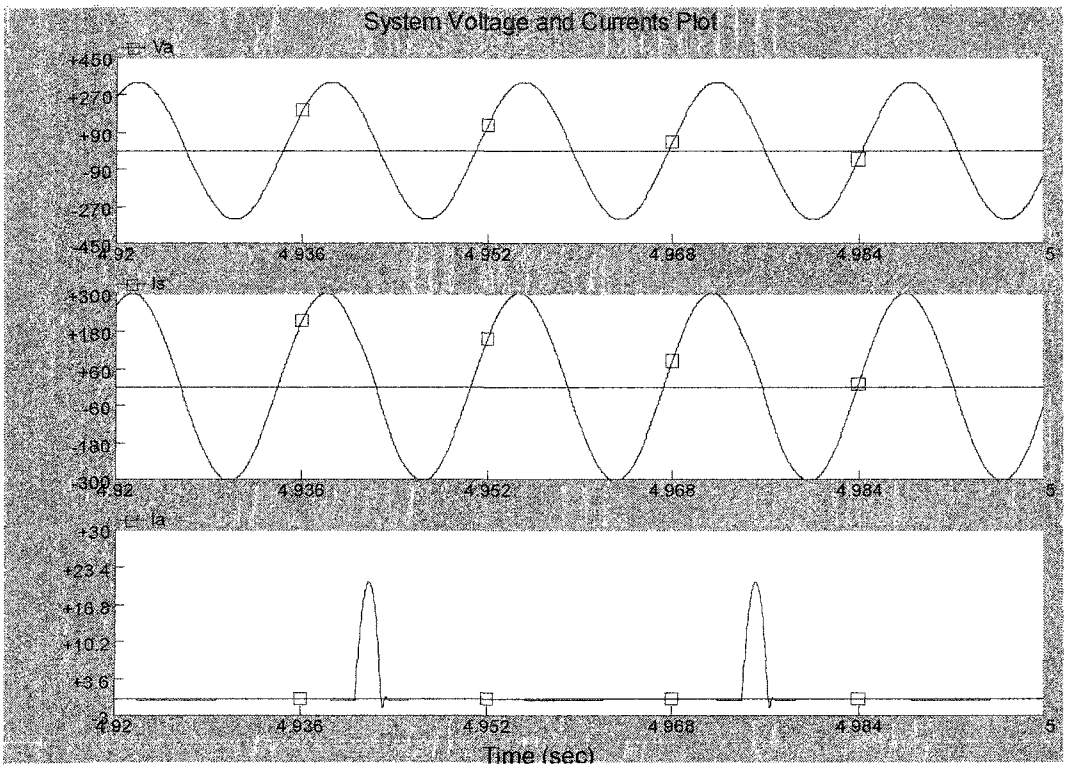

Figure (3.10): Modulating Current and System Voltage Waveforms – PSCAD Simulation

3.2.1 Effects of Load and Reactive Power Compensation Variation on Signal Properties

Simulation results have shown that the magnitude and decay rate of modulation voltage (e_{mod}) changes with varying loads and reactive power compensation levels. Figure 3.11 shows simulation results when signal generation takes place at 4MVA load. The resistance and inductance is 20 Ω and 5 mH respectively in each phase. A unity power factor is obtained by connecting a capacitor of 30 μF in each phase and the capacitors and load are connected in star. Note that e_{mod} has been scaled up by 20:1. The transient components for currents and voltage have been obtained by comparing their respective waveforms during transient and steady state conditions. In Figure 3.11, i_a, i_s and i_f represent current through the thryristor, current from the substation and feeder current respectively.

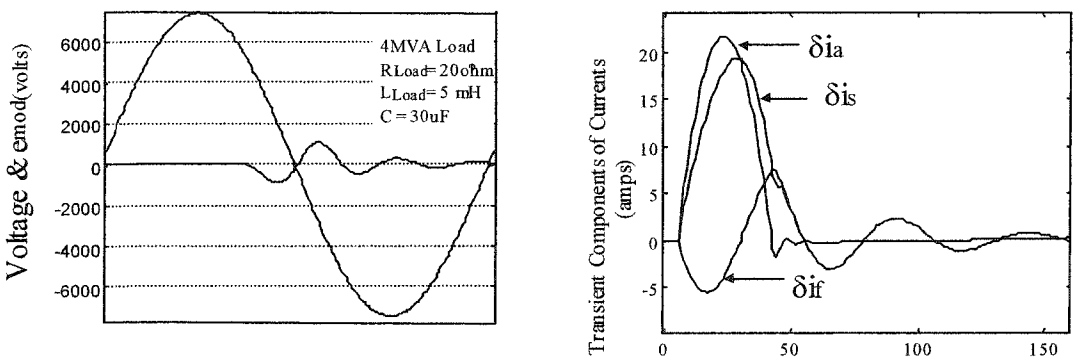

Figure (3.11): Transient Components of Voltage and Currents - Load: 4MVA

In the next simulation run, the values of load resistance and inductance were increased threefold to 60 Ω and 15 mH respectively and the load was 1.87 MVA. The

capacitance in each phase was 7 μF for unity power factor. Results of this simulation are displayed in Figure 3.12 in the same format as they were in the previous figure.

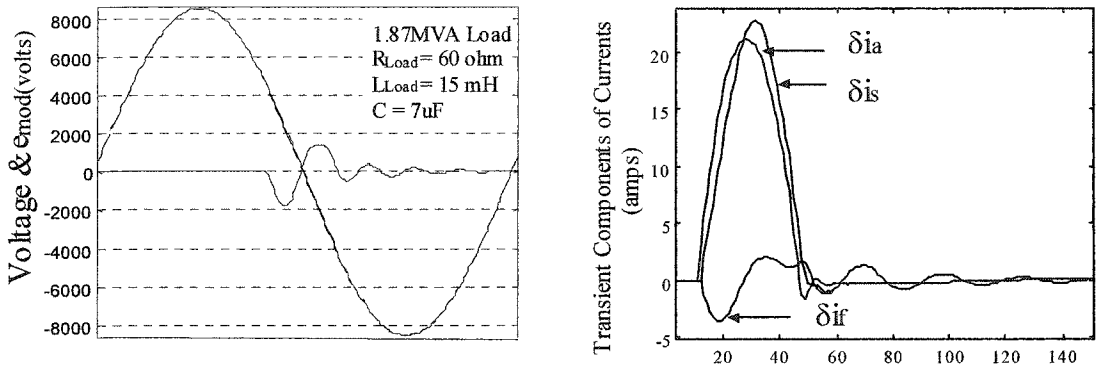

Figure (3.12): Transient Components of Voltage & Currents

High Inductance Load: 1.87 MVA

From Figures 3.11 and 3.12, it can be observed that 'δi_s' is the major contributor to thyristor current 'δi_a', and contribution by the feeder 'δi_f' is very small. It can also be seen that as the capacitance in the system reduces at smaller loads, feeder contribution to thyristor current also decreases. Another effect of reduced capacitance is increase in oscillation frequency as shown in the figures above.

The rate of oscillation decay is primarily dependent on load resistance and inductance. During off peak hours when most of the inductive loads are switched off, the demand for reactive compensation is very small. This case is illustrated in the third simulation run where load resistance is 60 Ω and load inductance 5 mH for 1.87 MVA

load. To have a power factor closer to unity, the capacitance required is 4 μF per phase. The results for this simulation run are shown in Figure 3.13.

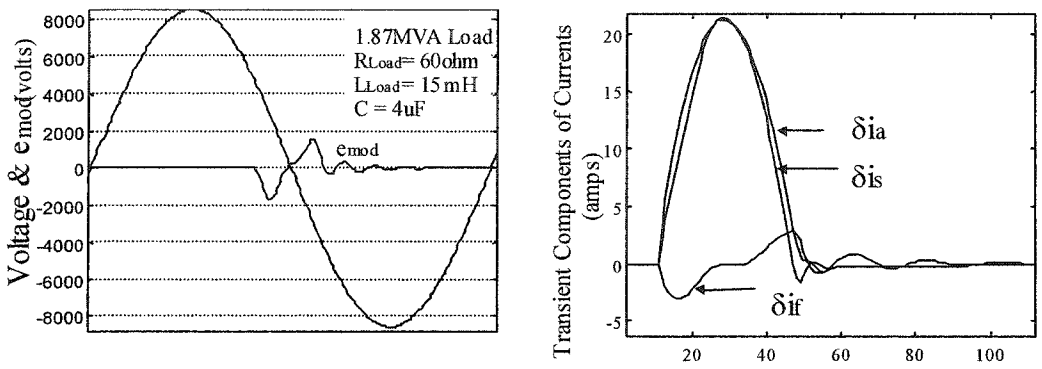

Figure (3.13): Transient Components of Voltage & Currents

Low Inductance Load: 1.87 MVA

We can see that the frequency in this case is higher compared to previous two runs and the decay rate is also higher. The increase in frequency is caused by reduction in capacitance and higher decay rate is due to a higher resistance to inductance ratio in comparison to previous runs.

Comparison of Figures 3.11, 3.12 and 3.13 reveals the following:

1. Due to reduced capacitance at smaller loads, the current contribution by the feeder to the fault current also reduces.
2. The frequency of oscillation increases with decreasing loads as capacitance in the circuit decreases.
3. The rate of oscillation decay increases during off peak hours when most of the inductive loads are off, due to an increase in resistance to inductance ratio.

3.3 Signal Characteristics and Detection Mechanism

An analysis of the simulation results and conclusions drawn in previous studies reveal that the signal oscillation can have different magnitude and frequency under different network conditions [1]. Current signal detection techniques, that rely on difference in voltage slopes of modulated and unmodulated cycles at specific instants, may not provide consistent performance with varying system conditions.

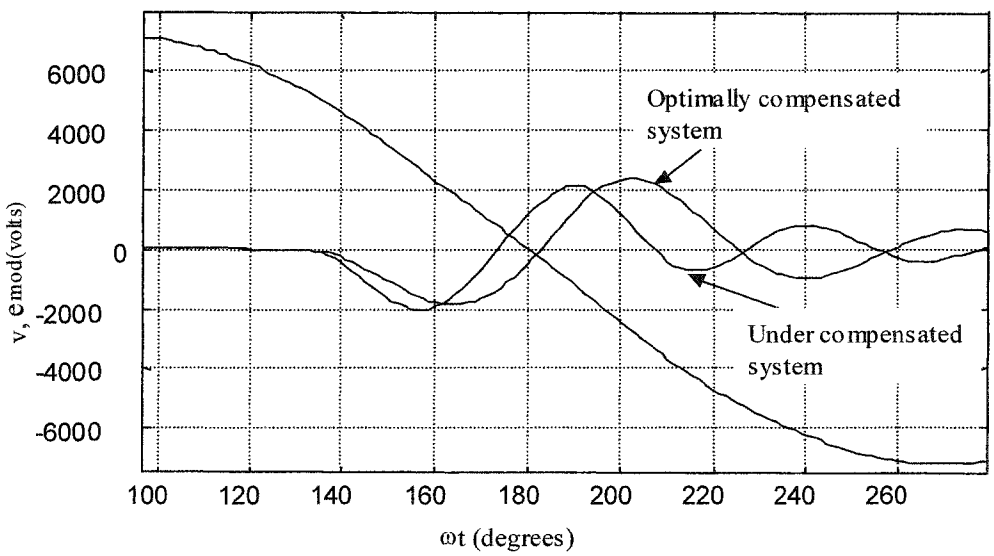

Figure (3.14): Oscillation waveforms at different compensation levels

As shown in Figure 3.14, 210° of the system voltage cycle is a good sampling point for detecting signal if the system is optimally compensated as the difference between voltages of modulated and unmodulated cycles at that point is considerable, but the difference between voltages at the same point for the under-compensted system is almost zero. Due to varying frequency of oscillation, it is not easy to set thresholds for signal detection criteria if the voltage is sampled only at specified moments. Comparing the entire cycles, instead of measuring slopes at specific moments, would provide a more

reliable method of signal detection. A detailed discussion on signal detection is presented in Chapter 4.

Another point of interest is the fact that even though the frequency and magnitude of oscillation change, they do so within limits. Most of the time, oscillation frequency is closer to 300Hz [1]. The simulation and analysis results show that the transient oscillations have exponentially decaying waveforms with decay coefficient values of the order of a few hundred. Figures 3.11, 3.12, 3.13 and 3.14 show that magnitudes of oscillations peaks fall below ¼ of the initial peak value after about 210° of the system voltage cycle, which means that a significant part of the oscillation is confined in a region ranging from 150 to 210° of the system voltage cycle. This range provides a time slot for signal search for detection.

3.4 Conclusions

Following conclusions can be drawn from the analysis of simulation results:

- Oscillation frequency and magnitude change with the amount of capacitance and load in the circuit.
- Signal strength generally increases with decreasing load. It can be 30% larger during light load conditions as compared to peak load hours and the signal frequency ranges between 240 – 600Hz depending on system operating conditions.
- Comparing the entire voltage cycles instead of measuring slopes at fixed time intervals can enhance signal detection accuracy.

Chapter 4

SIGNAL DETECTOR

4.0 Introduction

Discussion in Chapter 3 has established the requirements of a signal detection method. It can be said that the older signal detection techniques cannot be applied as such for islanding detection. These techniques are AMR specific and do not have the capabilities required for islanding detection. It is not critical in an AMR system if a false detection or non-detection takes place, because, if the communication fails once, another message can be sent. For islanding detection, there is no second chance. If signal detection malfunctions, false tripping can occur frequently. To eliminate this problem and make the detection algorithm more suitable for islanding detection, a new method of signal detection is presented in this chapter. This detection method requires the entire waveform of voltage to be sampled and used for the comparison of modulated and unmodulated cycles for signal detection. It also has a *ride-through* capability so that if the signal were temporarily undetectable due to a system disturbance, the DG would not be tripped right away. Maximum ride through time is dictated by recloser operation time. A detailed description of the prototype device developed for signal detection is also provided in this chapter.

4.1 Signal Detection

A new computer based technique for signal detection has been developed. This technique of signal detection involves continuous sampling of voltage and processing the sampled data in real time. Voltage slope based techniques of signal detection measure time intervals in going from one voltage level to another in each cycle. Signal detection criteria requires that the difference in time taken to go from one voltage level to another in two cycles be greater than a predetermined threshold in the modulation region of the voltage cycle (see Figure 4.2). A brief description of one such method is presented in Chapter 2.

The discussion in Chapter 3 reveals that, with changing load and VAR compensation levels, the difference in voltage slopes of modulated and umodulated cycles will change, and it is possible that under certain system conditions this difference may be below threshold even if the signal were present. As described in Figure 3.14, suppose the voltage difference between two cycles is compared at times corresponding to 210° of the system voltage cycle and the threshold is set at 60 volts. As can be seen in Figure 3.14, the signal detection will be accurate in the optimum compensation case but not in the under-compensation case because the difference in that case at 210° is closer to zero although the signal is present. Some discussion on this topic is presented in section 4.3 where the performance of the slope based detection method is compared to the new detection technique. Continuous sampling of voltage wave in the new scheme minimizes the possibility of missing the signal due to sampling at specified time intervals only.

4.1.1 Signal Detection Criteria

Figure 4.1 shows an unmodulated cycle followed by a modulated cycle. Two cycles are compared for signal detection. Difference between two cycles (e_{mod}) is shown in Figure 4.2

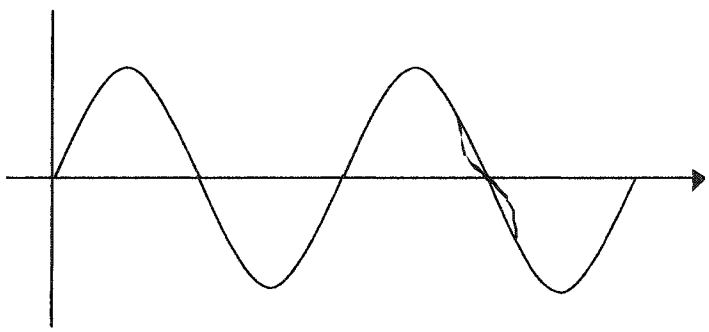

Figure (4.1): System Voltage Waveform – Modulation

The system voltage is constantly sampled, and data acquired by sampling is stored in a temporary memory location for processing. To separate cycles, negative to positive crossover points are identified. Once the cycles have been identified and separated, two consecutive cycles are paired up and one is subtracted from the other. Figure 4.2 shows the result of comparing a modulated cycle with an unmodulated one. The system voltage waveform is shown for reference and e_{mod} has been scaled up (1:20) for clarity.

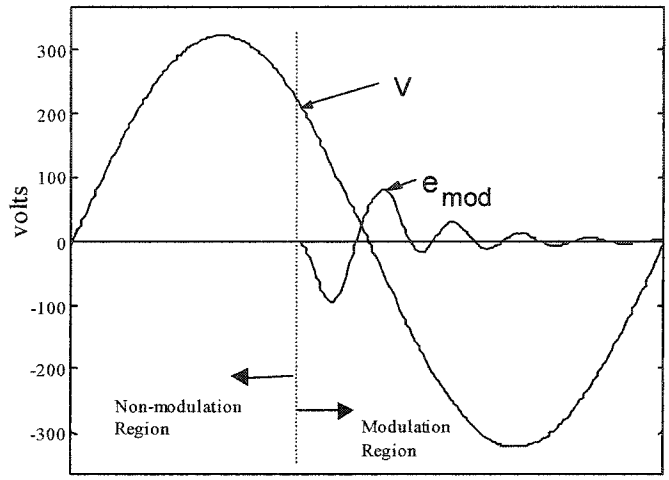

Figure (4.2): Comparison of Unmodulated and Modulated Cycle

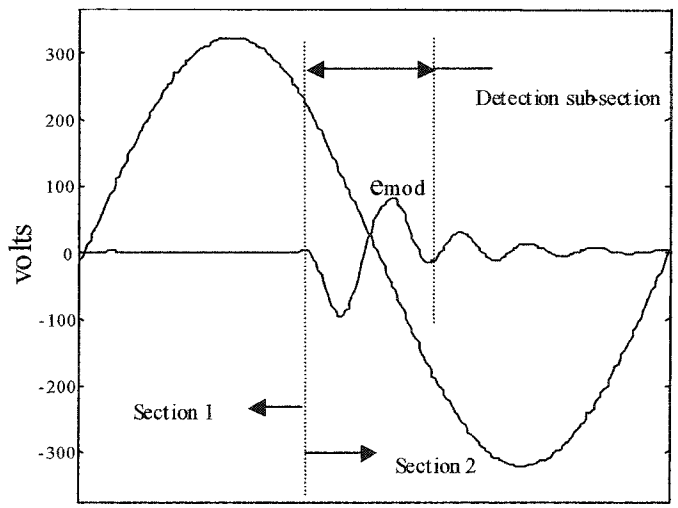

Figure (4.3): Signal Detection – Dividing e_{mod} into Sections

The next step is to divide e_{mod} into sections and subsections as shown in Figure 4.3. The first section ranges from system voltage rising zero crossing point to about 150°

of cycle and is called non-modulation region. Section 2 ranges from 151° to the end of the system voltage cycle and is called modulation region. The detection subsection is part of section 2. It consists of the part of e_{mod} ranging from 151° to about 210° of the system voltage cycle.

Root mean square values[2] (RMS) of e_{mod} in section1 and the detection subsection are then calculated. As shown in Figure 4.3, e_{mod} magnitude is much higher in the detection-subsection than in section 1 and the rest of section 2. These RMS values are compared against preset thresholds. The presence of signal can be confirmed only if RMS value in section 1 is below a threshold V_1 and RMS in the detection subsection is above a threshold V_2. The magnitude of V_1 is in the order of 0.3%, and that of V_2 is in the order of 1.2% of the system voltage RMS. This criterion of signal detection is necessary to distinguish between noise due to system disturbances and genuine signal.

Figure 4.4 shows noise due to the starting of a large induction motor. As shown in this figure, the starting of large induction motors can cause noise that may be of the order V_2, but this noise will also cause distortion levels to go higher than V_1 in section 1, and therefore, false signal detection can be avoided. A comparison of Figures 4.4 and 4.3 clearly shows the difference between noise and genuine signal.

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[2] RMS of a function f(t) over period 'T' is defined as: $f(t)_{RMS} = \sqrt{\frac{1}{T}\sum_{0}^{T} f^2(t)}$

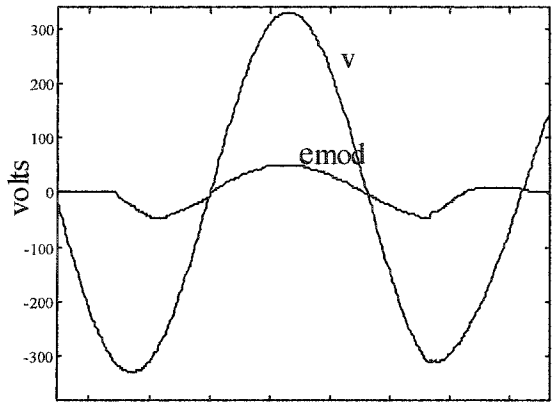


Figure 4.4: Induction Motor Starting Transient as seen by Detector

It can be seen that for accurate signal detection, thresholds are required for both section 1 and the detection subsection. If the level of difference between modulated and unmodulated cycles is above the threshold V_1 in section 1, it will be considered as noise even if the condition for detection in signal subsection is met.

The following table sums up the criterion to confirm signal presence.

Section 1 $e_{mod} < V_1$	Detection Subsection $e_{mod} > V_2$	Signal Present
No	No	No
Yes	No	No
No	Yes	No
Yes	Yes	Yes

Table (4.1) Signal Detection Criteria

The following is a step-by-step description of the signal detection mechanism:

1. *Data Acquisition*: Sampled data is stored in a cyclic buffer so that, while data in one half of the memory is being processed, the other half can acquire new data. At any given time, one half of the data buffer has data for p number of cycles, which is being processed, while the other half is acquiring data for the same number of cycles. p is the number of cycles corresponding to time delay between the loss of signal and the tripping of CB to disconnect DG from the grid (ride-through time).

2. *Zero-crossing Detection*: Processing of acquired data starts with zero-crossing detection and separation of data into different cycles. Note that the zero-crossing detection edge is opposite of the edge near which modulation of voltage takes place. Arrays of data for each cycle are marked as C_1, C_2 ....Cp.

3. *Cycle Subtraction*: Each odd cycle (an array of numbers) is subtracted from the consecutive even cycle. If the sampling rate is 'k' samples per cycle, difference between two cycles is: $J = C_{(i+1)}[1:k] - C_i[1:k]$, where 'i' represents the cycle number.

4. *Division of 'J' into sections and Computation of RMS of e_{mod} in each section:* The array obtained by subtracting two cycles (J), is divided into sections and subsections. Section 1 is from the start of voltage cycle to 150° and section 2 from end of section 1 till the end of the voltage cycle. The detection subsection is

the part of J in section 2, ranging from 151 to 210° of the voltage cycle (see figure 4.3). RMS of elements of J in section 1 and detection subsection is computed.

5. *Application of Signal detection Criterion*: Computed RMS values are compared against thresholds for both sections. For genuine signal detection, RMS of the measured distortion should be below preset threshold V_1 in section 1 and more than preset threshold V_2 in the detection subsection.

4.1.2 Detection Algorithm

The following is a simplified description of the signal detection program. Lab VIEW software was used for real time signal detection. Lab VIEW program code is available in Appendix1.

1. **Start**
2. Enter Nominal System Voltage (V_N), Frequency (f_N), S_R (sampling rate - points per cycle), p (number of cycles in the data buffer – corresponds to ride through time)
3. A = [] (empty array); Count = 0, f = f_N

Data Acquisition:

4. Acquire voltage sampling data

Sampling frequency $f_s = 256*f$

Computations:

5. Compute system voltage and frequency (V, f)
6. C = [A; B] (insert B after the final element of A)
7. m = Dimension[C]

System Voltage and Frequency Check

8. Compare frequency 'f' and RMS value V of system voltage waveform with nominal values.
9. Is $(0.95)V_N \leq V \leq (1.05)V_N$; No: Go to 27
10. Is $(0.98)\ f_N \leq f \leq (1.02)\ f_N$; No: Go to 27
11. Set threshold values for signal detection in waveform cycle sections 1 and 2 as per $V_1 = xV$ and $V_2 = yV$; i = 0

Zero Crossing detection:

12. Detect and store negative to positive zero crossing points in the acquired data n_1, n_2, n_3 ... etc. up to n_p (Final - to + zero crossing)
13. A = [C((p –l) : m)]
14. i = i + 1;

Synchronization of cycles:

15. $C_i = [C\{n_i : (n_{(i+1)} - 1)\}]$;

16. $d = n_{(i+1)} - n_i$;

17. $C_{(i+1)} = [C\{n_{(i+1)} : (n_{(i+1)} + d - 1)\}]$

Cycle subtraction:

18. Compute $J = [C_{(i+1)}] - [C_i]$

Separation of modulation and non–modulation regions:

19. u = Integer[(150/360)*Sr], v = [Sr]

    S = [J(1:u)] T = [J((u+1):v)]

    T_1 = T(min:max)

Signal Detection:

20. Compute S_{rms} & T_{1rms}

21. Is $S_{rms} \leq V_1$; No: Go to 24

22. Is $T_{1rms} > V_2$; No: Go to 24

23. Signal Present: Count = 0; Go to 26

24. Signal NOT present: Count = Count + 1

25. Is Count > 5; Yes: Go to 27

26. Is $n_{(i+1)} = n_p$; Yes: Go to 4 ; No: Go to 14

27. TRIP Circuit Breaker

28. End

4.2 Technical Considerations

The following are some of the factors taken into consideration in the development of signal detector.

4.2.1 Signal Detection Thresholds

Setting the signal detection thresholds requires careful examination of signal propagation characteristics. Effects of signaling on power quality limit the maximum magnitude of e_{mod}. To determine the signal levels, data was collected at a load site employing TWACS® AMR system. Figure 4.5 shows a plot of the system voltage and e_{mod} at the load site. In the plot, e_{mod} has been scaled up 1:20 for clarity.

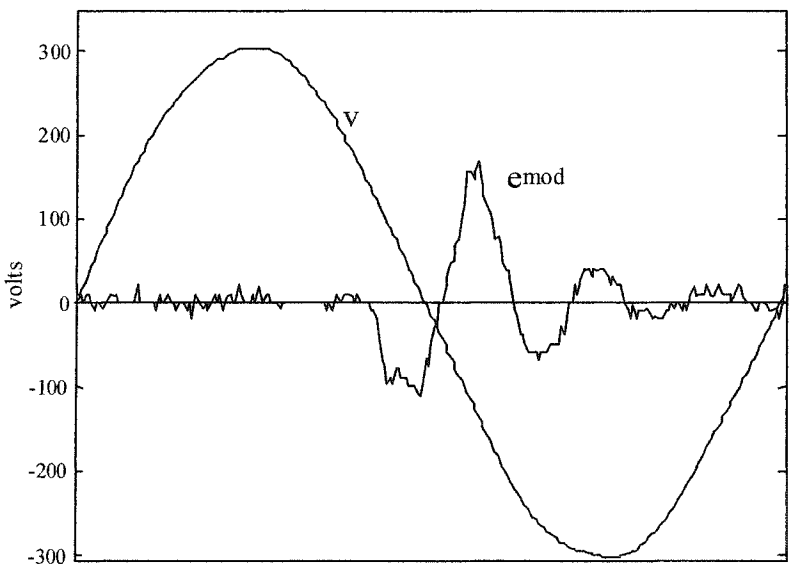


Figure (4.5): Signal Waveform

The data was collected on three different instances and levels of e_{mod} in modulation and non-modulation regions were evaluated. Figure 4.6 shows the e_{mod} levels in the modulation region during the presence and absence of a signal. Plots of e_{mod} RMS in non-modulation and detection subsection regions are shown in Figure 4.7.

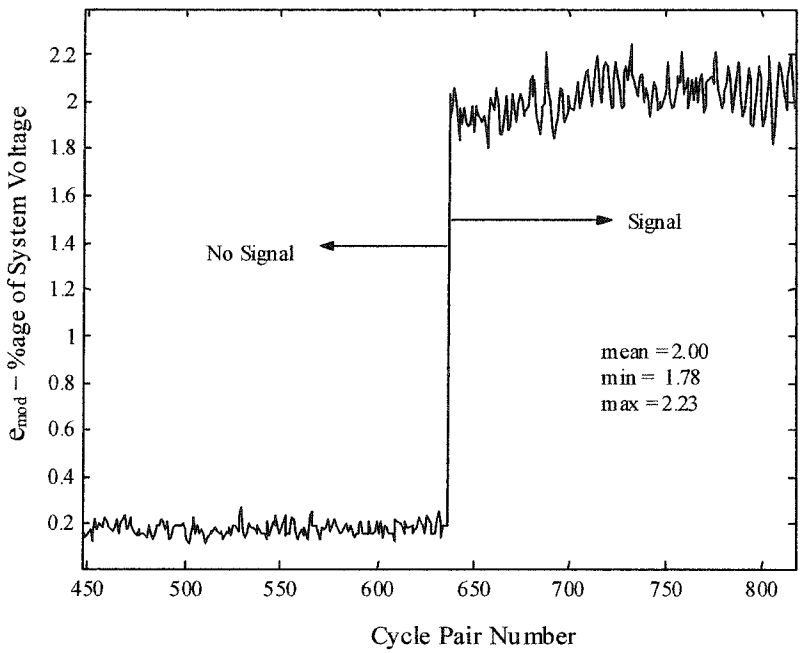


Figure (4.6): e_{mod} RMS in Detection Subsection

Figures 4.6 and 4.7 shows that e_{mod} levels in detection sub-section are much higher than the levels in non-modulation region when the signal is present. e_{mod} can be as high as 2.2% of the system voltage in the modulation region when the signal is present.

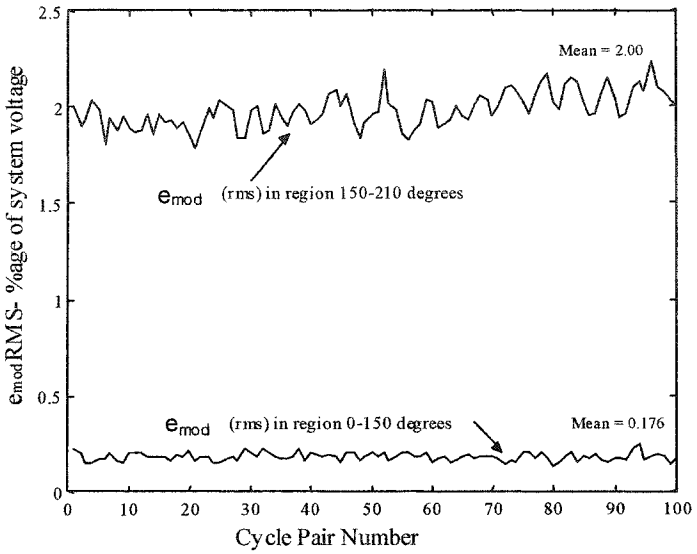
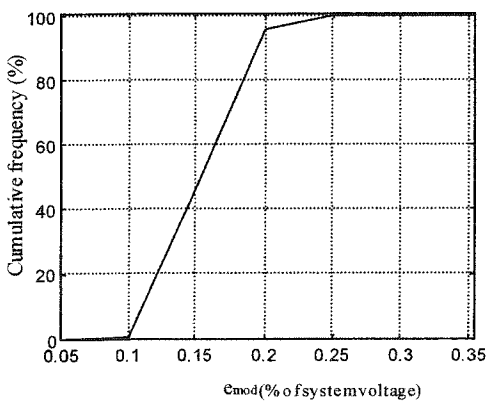
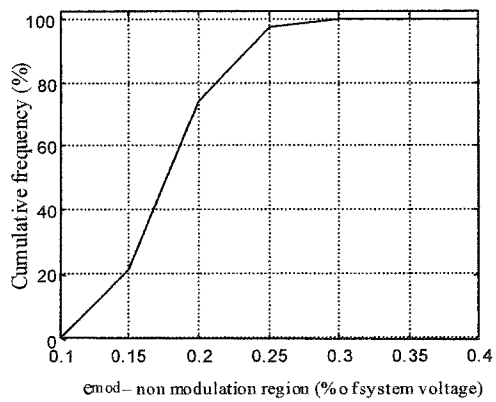


Figure (4.7): Comparison of e_{mod} in detection subsection and non-modulation region

A statistical analysis of the e_{mod} values is described in the following figures. Figures 4.8 and 4.9 show the cumulative frequency plot of e_{mod} values in the non-modulation region for two instances when data was collected at an AMR site.



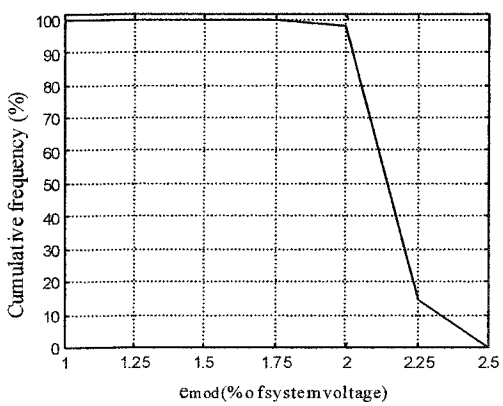
Figure(4.8): e_{mod} Magnitude cumulative frequency plot for non-modulation region- Case1



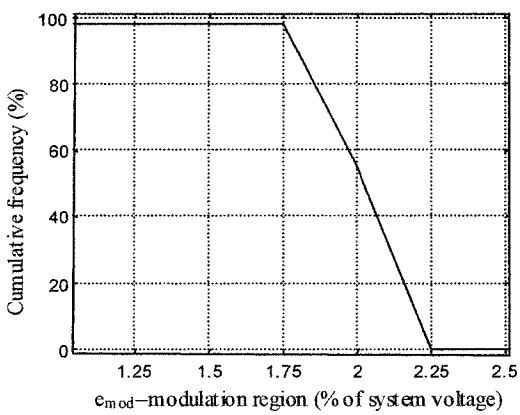
Figure(4.9): e_{mod} Magnitude cumulative frequency plot for non-modulation region- Case2

It is observed from these figures that in the non-modulation region, e_{mod} magnitude ranges between 0.1 to ~0.3% of the system voltage with almost 95% of the values being less than 0.25%. In other words if the threshold for the non-modulation modulation region is set to a value higher than 0.3%, the chances of missing a signal under normal conditions are close to zero whereas half the signals might be lost if the threshold is below 0.2% of the system voltage.

Figures 4.10 and 4.11 show the cumulative frequency plot of e_{mod} values in the modulation region when the signal is present. In this case we are interested in knowing the maximum limit we can go to therefore the plot is in the reverse order.



Figure(4.10): e_{mod} Magnitude cumulative frequency plot for modulation region-Case1



Figure(4.11): e_{mod} Magnitude cumulative frequency plot for modulation region-Case2

As shown in these figures, more than 90% of e_{mod} values in the modulation region have a magnitude higher than 1.70% of the system voltage and if the e_{mod} threshold in modulation region is lower than 1.5%, the chances of missing a signal under normal conditions are close to zero.

Considering the above results and keeping an extra margin of safety, the threshold for non-modulation region is set at 0.35 and threshold for modulation region at 1.2% of the system voltage. Lab tests have shown that detection device has performed well with these thresholds. Following table shows device performance at different threshold levels.

Threshold		Missed Signals/hour	False Signal Detection/hour	False Trips/hour
Modulation Region	Non-modulation Region			
0.6	0.35	2	4	0
1.2	0.35	2	0	0
1.2	0.30	19	0	0

Table (4.2): Detection Device Performance at different threshold level

We are primarily concerned about the safety of the generator and false tripping. However, if we had to choose between false signal detection and a missed signal, the choice would be the latter as it does not jeopardize the safety of the DG. Looking at the above table, with the chosen threshold values less than one signal was missed per hour and there were no false trips and no false signal detections.

4.2.2 Signal Detection: Modulation Region

So far, the discussion in this chapter was based on having a detection subsection in a region from 150 to 210° of the system voltage cycle. The objective is to select a region that provides maximum difference between RMS of e_{mod} in modulation and non-modulation region. Non-modulation region will always be in the region from 0 to150° of system voltage cycle; but the detection subsection can be shortened or lengthened. We have seen during analysis in Chapter 3 that there are two distinct oscillation peaks that occur after the start of fault (when the switch is first closed) and after the fault is cleared (switch is reopened).

The oscillations have an exponentially decaying sinusoidal waveform:

$$e_{mod}(t) = Ae^{-at}\sin(\omega t + \gamma)$$

RMS of e_{mod} is the squared-root of summation of squared instantaneous values over a period 'T', divided by 'T' as described below:

$$RMS = \sqrt{\frac{1}{T}\sum_{0}^{T} e_{mod}{}^{2}(t)} \quad \text{.....(1)}$$

Figure 4.12 shows a comparison of mean RMS values of e_{mod} for detection subsection range of 150-210° and that for detection subsection range of 150-180° at different VAR compensation levels. It can be seen that, shortening the detection subsection provides very small advantage under conditions when the system is excessively over-compensated. In the over-compensated case as the frequency is low, the

first oscillation peak occurs near 180° whereas the second peak occurs after 210° and therefore, most of the sampled values of higher magnitudes come into consideration over a smaller 'T'. In the under-compensated case, the second oscillation peak occurs near 210° due to higher frequency and provides an advantage for having the modulation region range of 150-210°. The system normally operates at a power factor closer to unity or lagging; therefore, the optimum choice for detection subsection is 150-210° of the system voltage cycle.

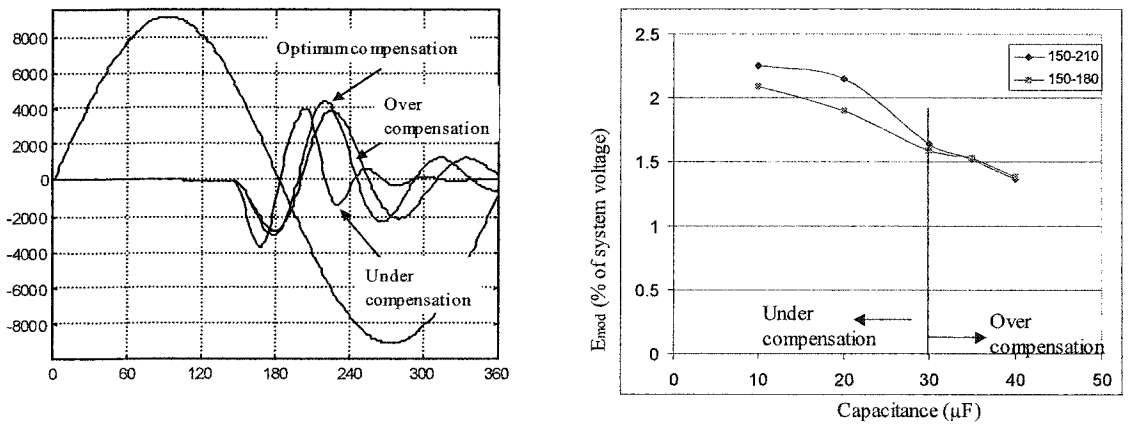


Figure (4.12): Comparison of e_{mod} RMS for different lengths of detection subsection

As the oscillation tends to decay to very small levels beyond 210° of the system voltage cycle, lengthening of detection subsection will not provide any advantage as described below:

Consider a case where the oscillation follows a function:

$$f(t) = 6e^{-400t}\sin(800\pi t)$$

$$\text{then, } f_{RMS} = \sqrt{\frac{1}{T}\sum_{0}^{T} f^2(t)}$$

If 'T' corresponds to one cycle, RMS = 2.75 and for two cycles, RMS = 2.07

So, we can see that beyond first cycle of oscillation, the RMS value decreases significantly and hence, lengthening the modulation region is not advantageous.

4.2.3 System Disturbances and the Ride Through Mechanism

There is a possibility that due to a disturbance or signal-generator malfunction, the signal might be temporarily undetectable even when islanding has not occurred. Under such circumstances it is required that the detection system be able to ride-through for a short period of a few cycles so that signal detection can resume as soon as the system is back to its normal operating conditions after the disturbance. The detection-algorithm has provision for a 10 cycle ride-through. The ride through time can be increased or decreased depending upon response time requirements, and the maximum ride through period is dictated by the recloser operation time. It is required that DG be disconnected before recloser operation which may reconnect the two systems when out of phase.

Most disturbances last only a few cycles. For example, disturbances due to switching of heavy loads, or transients due to capacitor switching usually last for a short time period of a few cycles.

Voltage disturbances due to transformer inrush phenomenon can last longer than a few cycles. Magnetizing inrush currents occur due to the non-linearity of the transformer core magnetizing characteristics.

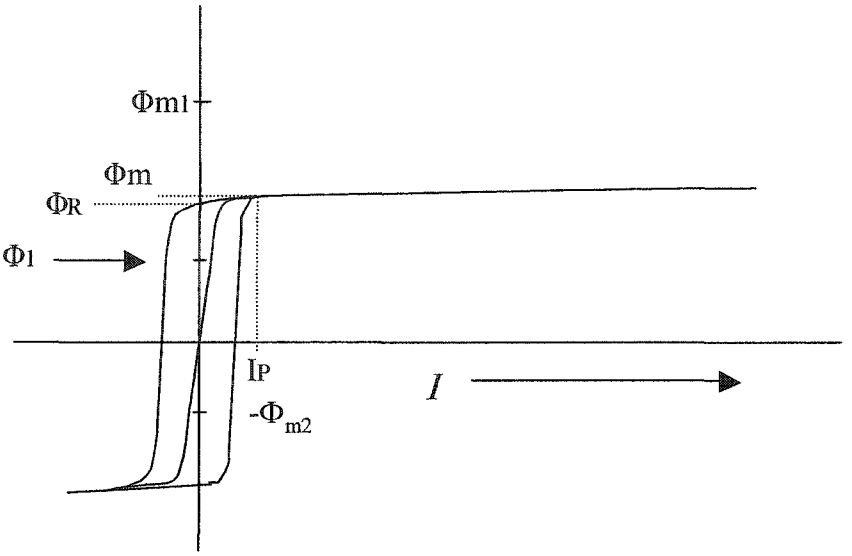


Figure (4.13): Magnetization characteristics of a Transformer Core

Figure 4.13 shows the magnetizing curve and hysteresis loop of a transformer core. Under steady-state, the flux varies between $+\Phi_m$ and $-\Phi_m$ while the current varies between $+I_p$ and $-I_p$. To estimate the current when the voltage is first applied to the transformer we need to determine the condition at the last time transformer was switched off. Figure 4.13 shows that there is a considerable remanent flux $\pm\Phi_R$ in the core when current passes through zero, which is removed only when current is reversed. Thus, we expect there to be significant remanent flux after the transformer has been switched off, however, it will be less than Φ_R because a transient current will flow in the transformer winding after the transformer has been disconnected from the mains, as a consequence of transformer discharging its own capacitance [9].

If the value of remanent flux is $+\Phi_1$ and assume that when transformer is switched on, the polarity of the voltage is such that it requires flux to increase positively. The worst case scenario is that the voltage is passing through zero, the flux will have to increment by $+\Phi_m$ before the voltage peak is reached. Since the flux started off at Φ_1, it will have to reach Φ_{m1}, before reversing. It is obvious from Figure 4.13 that because of saturation, an enormous amount of current would be drawn from the supply. On the following negative half-cycle, the peak flux will only be $-\Phi_{m2,}$ so that the current will be less than normal. We have considered the worst-case scenario but this condition has the same probability of occurring as any other. The inrush currents in transformers are several times their rated load currents. The current starts to decay exponentially because a transformer is a series R-L circuit after all. The winding resistance and core losses account for resistance R. Inductance L being non-linear, the time constant for decay (L/R) cannot be readily defined. In practice it may take several seconds for the transformer inrush current to reach its steady-state value [9]. Therefore, while implementing this islanding detection method probability of transformer inrush phenomenon must be evaluated.

Figure 4.14 shows a genuine signal and transient due to induction motor starting. The e_{mod} magnitudes in section 1 and detection subsection are shown in Figure 4.15.

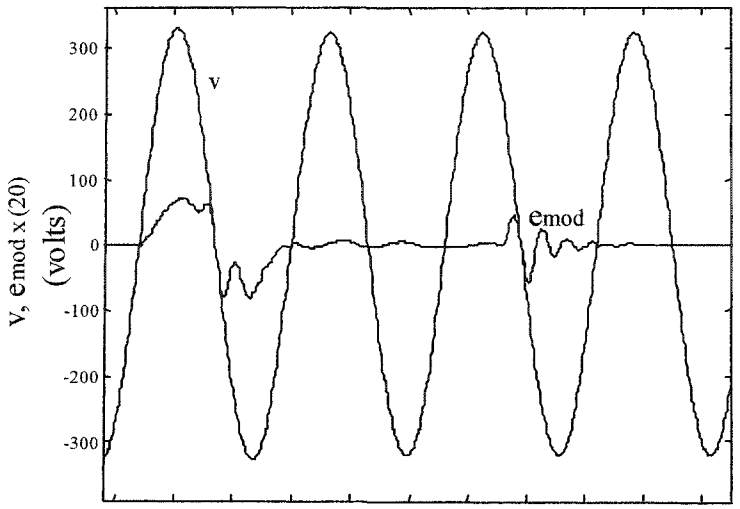


Figure (4.14): Motor Starting Transient and Genuine Signal

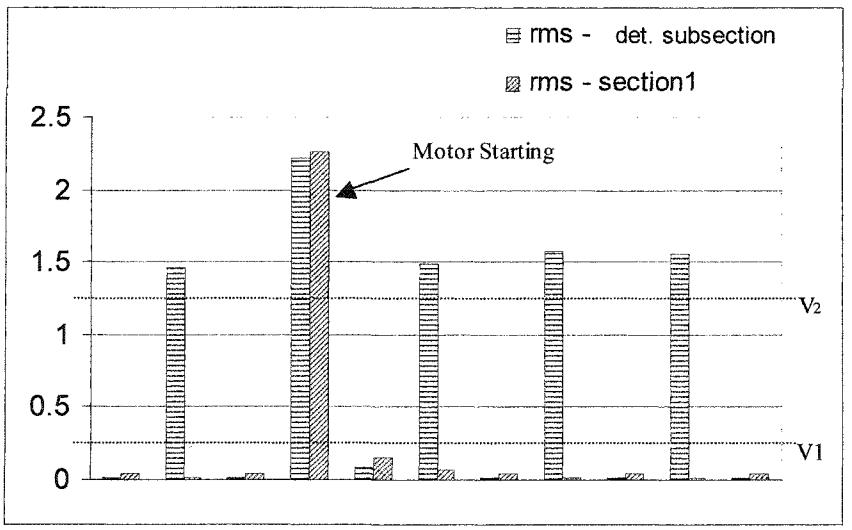


Figure (4.15): Signal Detection during Motor Switching

Figure 4.15 shows the working of the signal detector during a transient. As shown in this figure, modulation takes place every other cycle and under normal operating conditions, e_{mod} levels in detection subsection are above threshold V_2 and levels in

section 1 below threshold V_1. However, when motor switching takes place, levels in section 1 go above threshold V_1. The detector will indicate no signal for the cycle/s where effects of motor starting are predominant, even though, signal was present. The signal will be detected as soon as transient dies out, and due to the ride through capability, islanding will not be indicated. Similar comments could be made regarding transients due to capacitor-bank switching and other short disturbances.

4.2.4 Change in System Voltage and Frequency

The magnitude of system voltage changes due to variation of the total load, transformer tap changing, and capacitor bank switching. The system frequency can also change due to an unbalance in load and generation. Changes in magnitude and frequency of the system voltage are not huge concerns for signal detection as long as these changes don't occur as frequently as every few cycles.

Signal detector requires that the system voltage consistently follow a function, $v = V_a \sin 2\pi ft$, where V_a is the voltage amplitude and f is the system frequency, for at least two cycles that are being compared to determine signal presence. If the frequency or magnitude of v changes from cycle to cycle, signal detection is difficult if not impossible. However, it does not matter what the magnitude or frequency is as long as they stay constant.

If the magnitude and/or frequency of system voltage stabilize within the ride-through period at a new value after a change takes place, signal detector performance

will not be compromised. It is almost impossible that magnitude or frequency of system voltage vary as frequently as every couple of cycles, and if it does happen, it is best to disconnect the DG from the grid.

4.2.5 Sampling Rate

For accurate comparison of two cycles, voltage sampling rate should ideally be an integer multiple of the system frequency. If not, results of the comparison of two cycles will have a certain degree of error. The degree of error is inversely proportional to sampling rate.

If voltage pattern consistently follows the function:

$$v = V_a \sin 2\pi ft$$

Where V_a is the voltage amplitude and f is the system frequency

The ideal sampling frequency would be $f_s = Kf$; K being an integer. K is also the number of sampling points per cycle. As shown in Figure 4.11, if the sampling frequency is not an integer multiple of 'f' even though the two cycles are identical, they would appear to be different to the data processing device. In the shown figure samples are taken at regular time intervals Δt.

$$\Delta t = \frac{1}{f_s}$$

$$\text{For } f_s = Kf, \qquad \Delta t = \frac{1}{Kf}$$

Which means K points in every cycle.

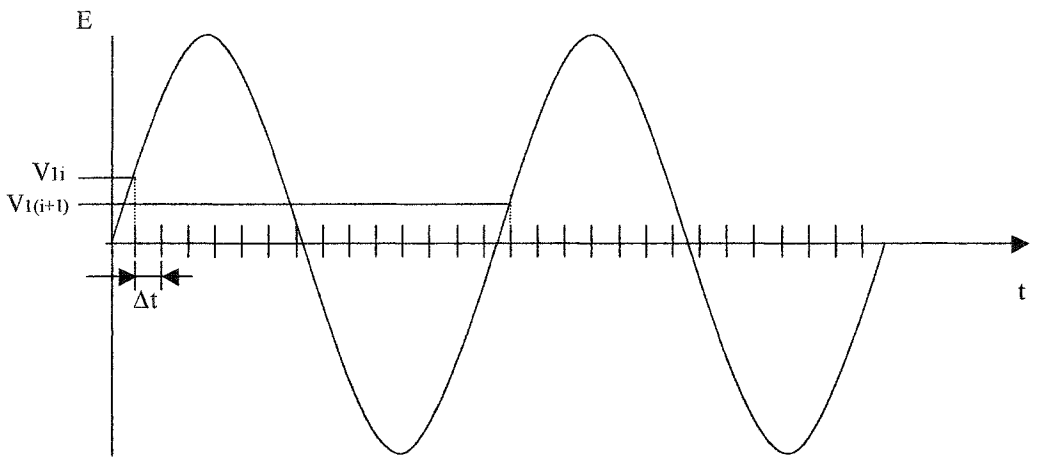


Figure (4.16): Effect of sampling frequency on cycle comparison accuracy

Though we are processing data of a sampled 60Hz wave, but the intent here is to extract a transient oscillation the frequency of which can be as high as 600Hz. We are also interested in calculating the RMS of this oscillation, which means that we should have a number of points to accurately evaluate the RMS. A sampling rate of 6kHz would represent one complete cycle of 600Hz wave by 10 data points and 12kHz would represent the same cycle over 20 data points and so on. Obviously as the sampling rate increases, margin of error for comparison of two cycles is reduced. The sampling rate would ultimately be decided by the desired accuracy of signal detection. To find an appropriate sampling rate, performance of signal detector was evaluated at different sampling rates during different times of the day and the results are presented in the following table.

Sampling Rate (s^{-1})	Thresholds		Missed Signals/hour	False Trips/hour
	Modulation region	Non-modulation region		
15000	1.2	0.35	2	0
7500	1.2	0.35	12	0.16
3750	1.2	0.35	62566	3124

Table (4.3): Signal Detector performance at different sampling rates

As we can see from Table 4.3, sampling rate of 3.75kHz does not even come close to the required performance. The risk of false tripping almost four times a day at 7.5kHz sample rate is too high. A sampling rate of 15kHz provides acceptable reliability.

4.3 Comparison with Slope-based Algorithm

In this section, the limitations of slope-based technique are highlighted by comparing results of employing both techniques for signal detection. Data collected at the AMR site on three occasions was processed using both techniques for signal detection. Details of a slope-based technique are provided in section 2.3. The following slope-based signal detection algorithm was used in this analysis:

Slope-based Algorithm:

1. Start
2. Sample the system voltage waveform and compute average DC value for each of five successive cycles V_{av}
3. Using zero crossings points compute sampling rate for each cycle
4. Compute the running average of V_{avg} for five cycles
5. Set the voltage levels V_0, V_1, V_2, ... V_6 and threshold time differences 'x'
6. Find moments in time (t_{n11}, t_{n22}...etc.) when each voltage levels V_0 through V_6 are crossed going from lower to higher value
7. Interpolate to find the exact moment when the levels are crossed
8. Compute the time intervals (del t1, delt2, ...etc) for going from one voltage level to another
9. Detect the next negative to positive zero-crossing
10. Find moments in time (t_{n11}, t_{n22}...etc.) when each voltage levels V_0 through V_6 are crossed going from lower to higher value
11. Interpolate to find the exact moment when the levels are crossed
12. Compute the time intervals (del t11, del t22....etc) for going from one voltage level to another
13. Compare del t1, delt2..etc against del t11, del t22 .....etc.
14. If two of the three delt's are greater than threshold x Go to next step, otherwise go to step 20
15. Signal present Go to 6
16. Signal NOT present Go to 6

Different levels of V_0 through V_6 were used to seek the best performance for all three cases. Time differences in going from one voltage level to the other were compared between two cycles to determine the presence of signal. The threshold for time difference in going from one voltage level to the other was set at 20μs and the criteria required that two out of three time-differences be above or equal to the threshold. Figure 4.17 provides a graphical presentation of the algorithm. Note that only four of six levels of voltage are shown in the figure. As can be seen from the results in Table 4.4, if a combination is good for one case it does not necessarily mean that it will work for other system conditions as well. To say the least, it is very difficult to set the voltage points such that the algorithm would work under all system conditions.

	Sampling points (degrees elect.)			Slope-based Threshold (μs)	RMS-based Threshold (%)	Missed Signals (%)	
	1	2	3			Slope-based	RMS-based
Case1	150-160	175-185	190-200	20	1.2	9	0
Case2	150-160	175-185	190-200	20	1.2	0	0
Case3	150-160	175-185	190-200	20	1.2	2	0
Case1	155-165	170-180	195-205	20	1.2	17	0
Case2	155-165	170-180	195-205	20	1.2	1	0
Case3	155-165	170-180	195-205	20	1.2	2	0

Table (4.4): Performance of Slope-based Technique v/s Proposed Technique

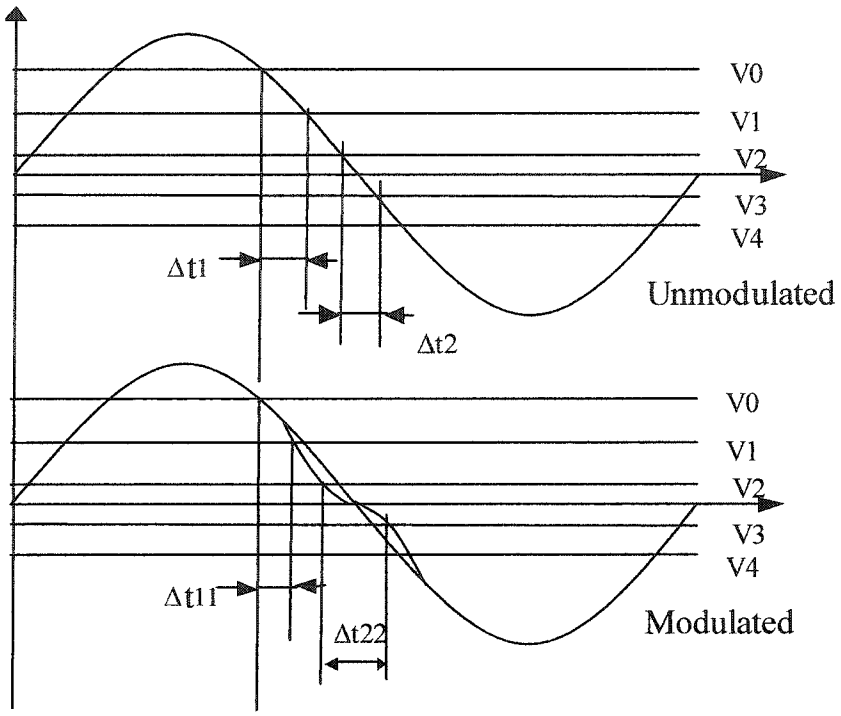


Figure (4.17): Slope based detection method

4.4 Detection Device

A pilot device has been developed as part of this research. National Instruments® software and hardware was used in the developments of this device. The detection set-up includes:

1. A step down transformer (120/5V)
2. A Data Acquisition (DAQ) device and computer interface
3. Lab VIEW programming software
4. A Pentium 3 desktop computer

The device was used in laboratory tests at 70 - 120V. A signal generator prototype was used to modulate the voltage across a transformer connected to a model distribution line. Load and the signal detector are connected at the end of the line. Various components of the signal detector are shown in a schematic diagram in Figure 4.18. A picture of detection setup is shown in Figure 4.19.

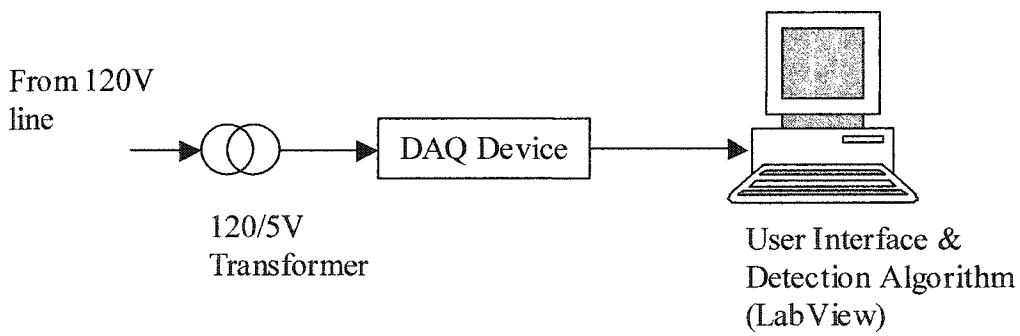


Figure (4.18): Signal Detector Schematic Diagram

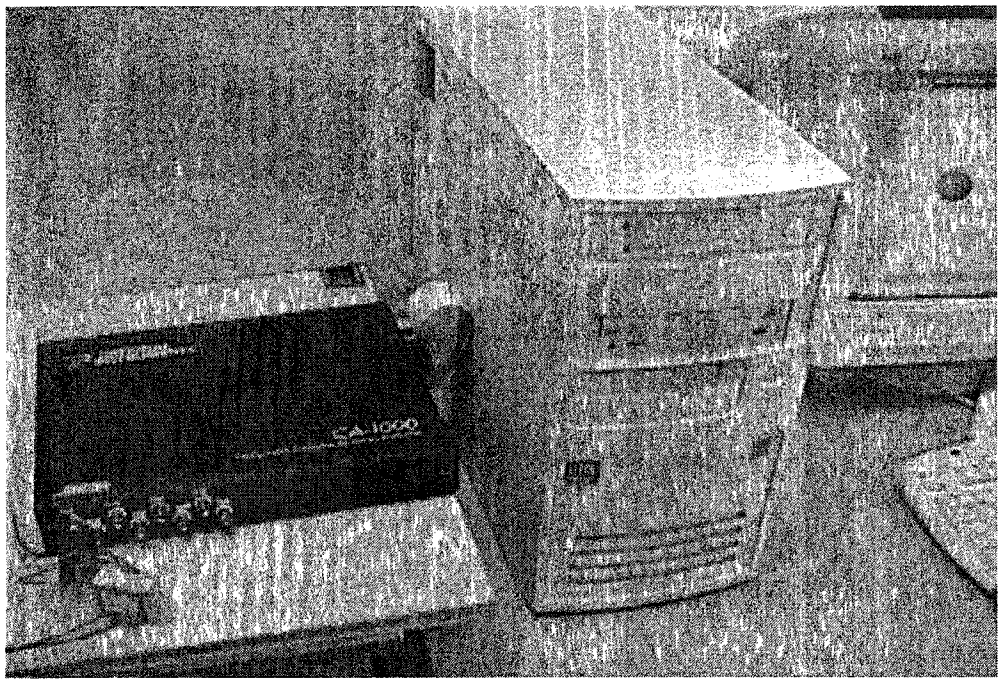


Figure (4.19): Signal Detector Setup

The DAQ device is rated for a maximum of –10 to +10V peak-to-peak voltage. Therefore, voltage is stepped down using a 120/5V transformer before connecting to the data acquisition device. Acquired data is processed by a Pentium-3 desktop-computer, and the results and waveforms are displayed on the graphic screen.

A user interface has been provided in the program. It lets the user specify detection criteria. Parameters such as RMS thresholds (V_1 and V_2), sampling rate, rising or falling zero crossing synchronization, ride through time etc. can be adjusted within certain limits. The user interface screen is shown in Figure 4.20

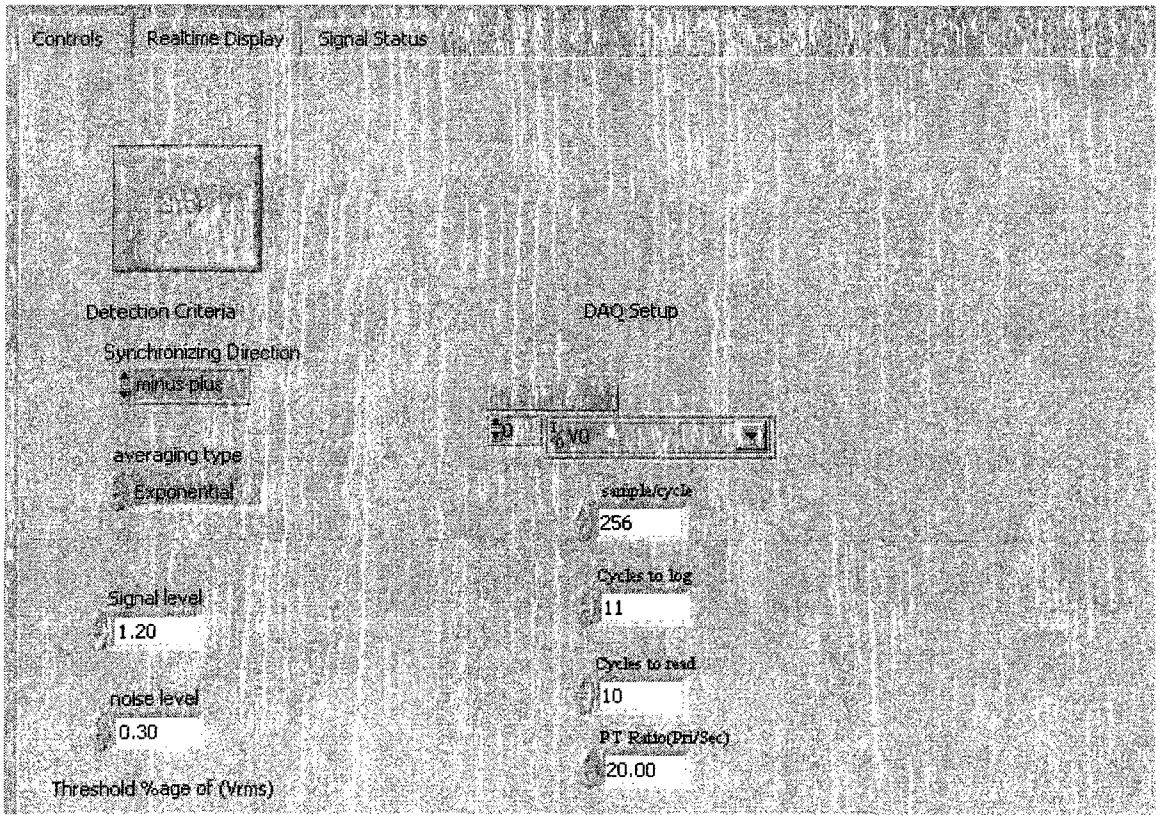


Figure (4.20): Detection Program User Interface – Parameter Specification

A display screen has been provided to indicate the status of signal detection at any time. The indicator LED stays green if the signal is present and turns red if the signal is lost for longer than the ride-through period. The system voltage and signal waveform are also displayed on a separate screen. A display when signal is present is shown in Figure 4.21 and a display, when signal is not present, is shown in Figure 4.22.

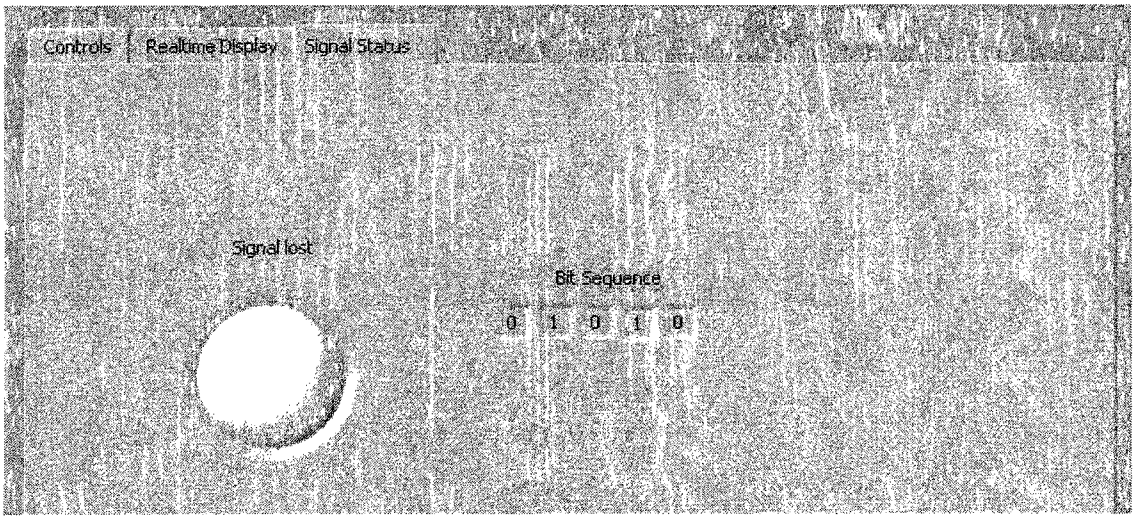


Figure (4.21): Detection Program Display Screen – Signal Present

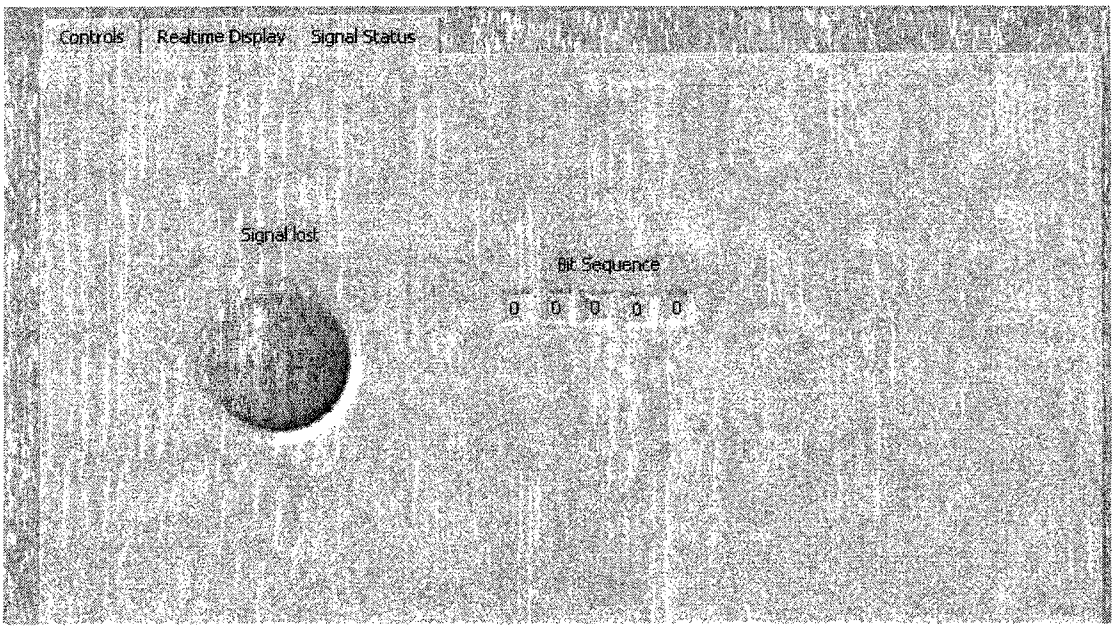


Figure (4.22): Detection Program Display Screen – Signal Not Present

Chapter 5

PERFORMANCE EVALUATION OF SIGNAL DETECTOR

This chapter presents the results and procedures of tests conducted on the signal detector. The main performance indicators are signal detection accuracy and response time of the detector to loss of signal. The ride through mechanism has also been tested.

5.0 Introduction

The primary objective for developing the signal detector is to detect and indicate loss of signal within a specified time. The response time requirement is determined by the operating time of reclosers in the distribution network. A loss of signal indicates islanding. Laboratory tests were conducted to investigate the performance of the signal detector by verifying that:

1) Accurate signal detection is possible at different loads and line capacitances.
2) The ride-through mechanism works.
3) Time delay between the deactivation of signal and indication of lost signal by the program is below required response time.

5.1 Test Procedures & Results

Three performance parameters were investigated in the tests: signal detection accuracy, response time, and ride-through mechanism. The basic test set-up in the single-phase format for experimental investigation is shown in Figure 5.1.

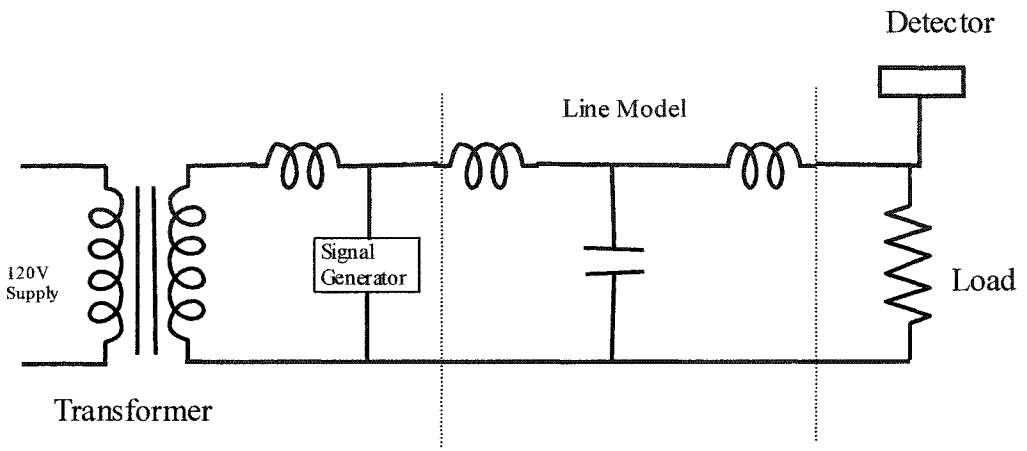


Figure (5.1): Lab Test Set-up

An autotransformer is connected across a 120V power supply with the signal generator at its output terminals. Load or capacitance in the set-up can be changed. To make up for low leakage impedance of the autotransformer, an inductor was connected in series. Procedures for each test and results are described in the following sections.

5.1.1 Signal Detection Accuracy

The signal generator can be configured to modulate every other cycle or one in every seven cycles and any number in between; i.e., one cycle in every 3, 4, 5 or 6 cycles.

If the presence of signal is represented by bit '1' and absence by bit '0', different bit patterns can be achieved depending upon the signal generator configuration. As the signal detection requires comparison of two cycles, two consecutive cycles cannot be modulated. As shown in Figure 5.2, if every other cycle is modulated and cycles are monitored in groups of ten, a bit pattern [11111] can be achieved.

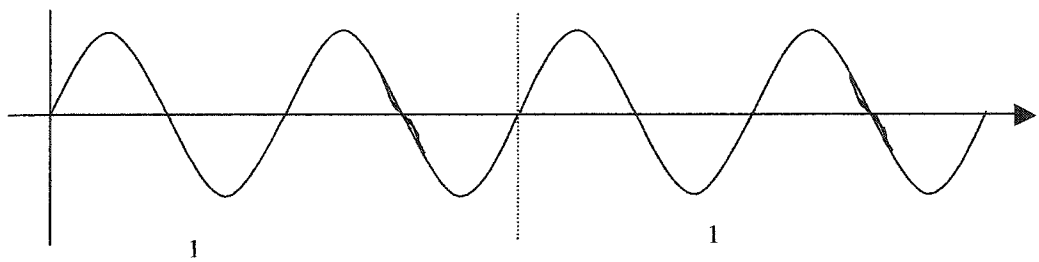


Figure (5.2): One in two Cycles Modulated – bit pattern 11111

Similarly, if one in every four cycles is modulated, the bit pattern will be either [01010] or [10101] depending upon whether either of the first two cycles is modulated or not.

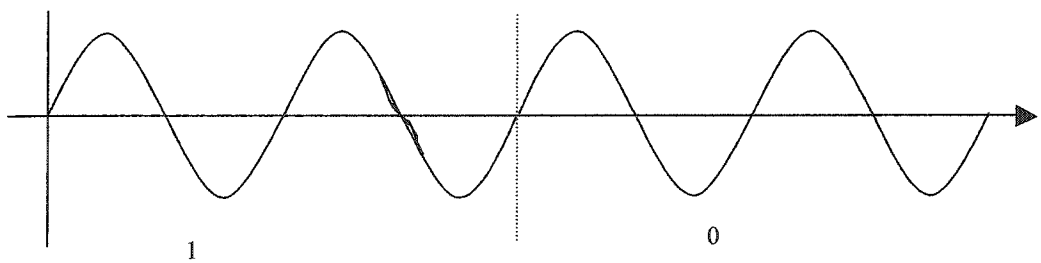


Figure (5.3): One in four Cycles Modulated – Bit pattern 10101

Different modulation configurations of the signal generator were implemented and corresponding bit patterns were observed on the graphic display screen. Tests were repeated during different times of day and at different load and capacitance in the circuit. Signal detection was achieved with perfect accuracy in all tests. Thresholds for signal detection are such that the weakest signals can be detected and distinguished from noise by the signal detector.

Figures 5.4 and 5.5 show the bit patterns as indicated by the detection program for different signal generation configurations.

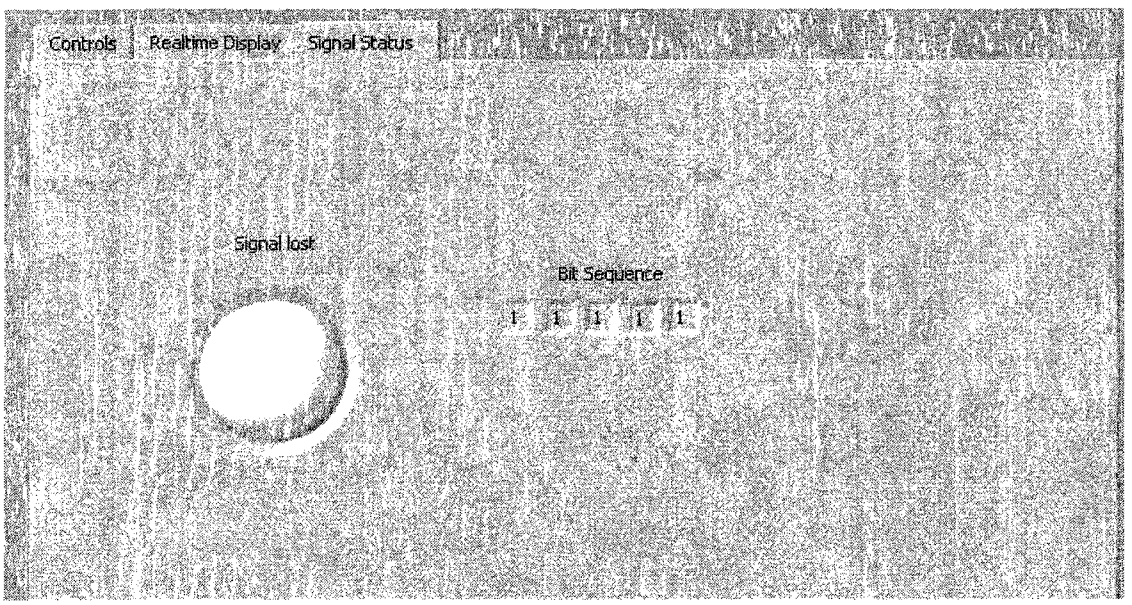


Figure (5.4): Bit Sequence - Every Second Cycle Modulated

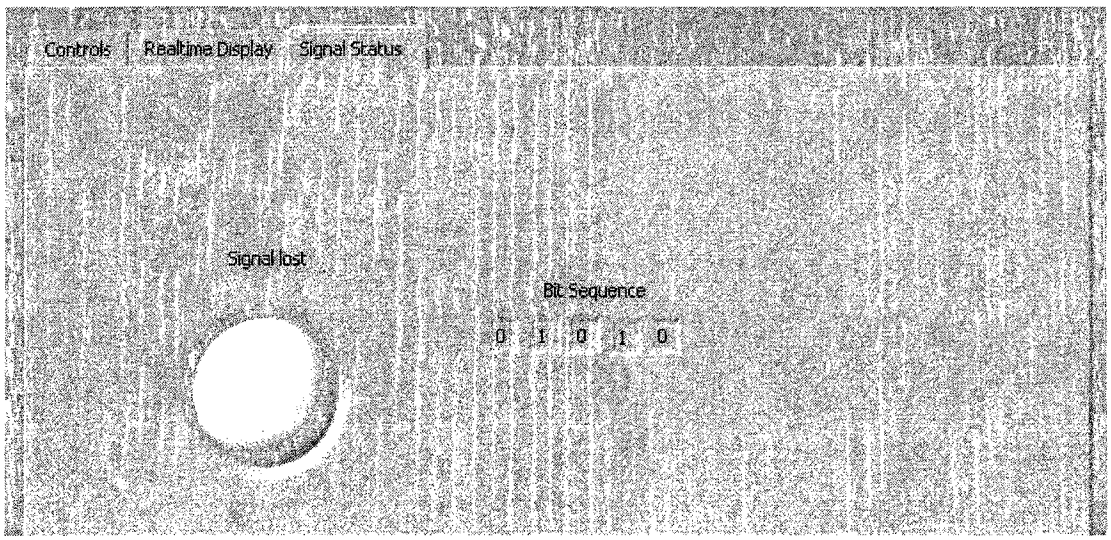


Figure (5.5): Bit Sequence - Every Fourth Cycle Modulated

5.1.2 Response Time

An indicator is provided on a graphics display screen (see figure 5.6) that turns on if the signal is lost. To determine the response time of the detector, the signal generator was deactivated while the detection program was running and the time taken by the indicator to indicate loss of signal was noted. The test was repeated a number of times and it was observed that each time the signal was deactivated, the lost signal indicator turned on virtually instantly.

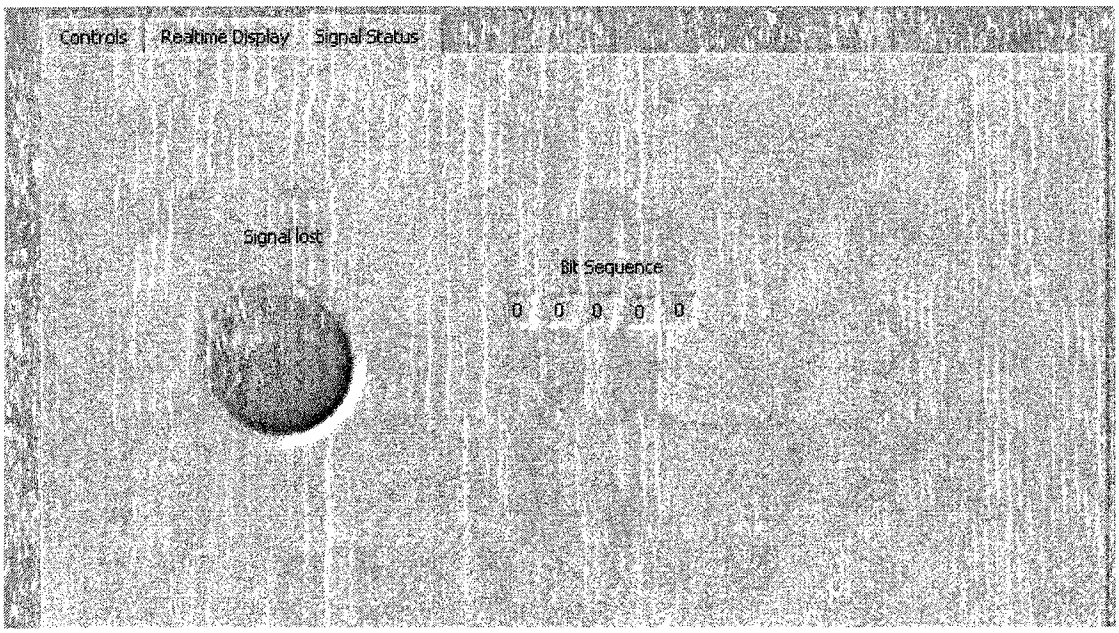


Figure (5.6): Signal Status Indicator – Signal Lost

5.1.3 Ride Through Mechanism

The ride-through mechanism was tested using two methods. In the first test, the signal generator was configured to modulate one in every seven cycles and signal detection was observed. In another test, signal was injected every three cycles and the bit pattern was monitored while a capacitor or inductor was switched on and off in the line. It was observed that due to very large noise while signal detection did not take place in one pair of cycles, it was detected in another pair and due to the ride through mechanism signal detector did not indicate a loss of signal. Figure 5.7 shows a screen capture of one such instance when a capacitor was switched into the circuit.

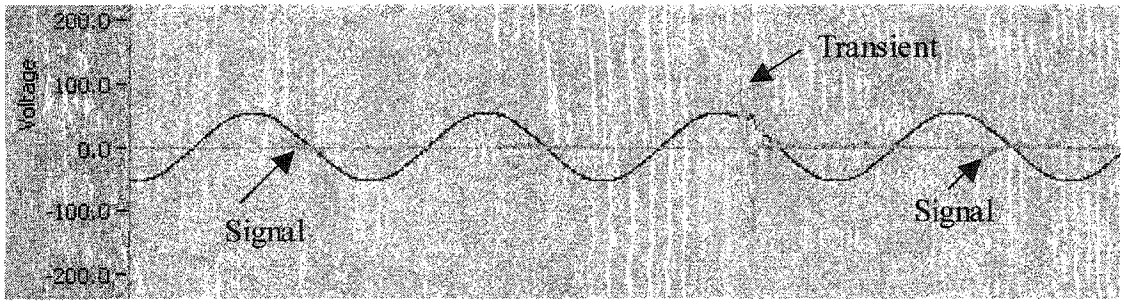


Figure (5.7): Signal Detection after a Transient

In this case, the transient lasted for only two half-cycles, and the signal detection resumed right after.

5.2 Threshold and Sampling Rate Sensitivity

Tests were conducted to obtain optimum values of thresholds and sampling rate for signal detection. In this section a summary of these tests is presented. Keeping the primary objective of DG protection and reliability to avoid false detection in mind, tests were conducted to see how the device behaves at different threshold levels and what are the chances of missing a signal, false signal detection and false trips.

Table 5.1 shows the results of different tests:

Modulation-region Threshold	Nonmodulation Region Threshold	Sample Rate s^{-1}	Test Duration Hours	Missed Signals/hr	False Detections/hr	False trips/hr
1.2	0.35	15000	10	2	**	0
1.2	0.35	7500	10	12	**	0.16
1.2	0.3	15000	10	12	**	0
1.2	0.3	7500	10	30	**	2
0.5	0.35	7500	22	**	42	**
0.5	0.35	15000	18	**	8	**
0.6	0.35	7500	12	**	15	**
0.6	0.35	15000	22	**	4	**
0.7	0.35	7500	10	**	14	**
0.7	0.35	15000	10	**	2	**
1.2	0.35	15000	17	**	0	**
1.2	0.35	7500	7	**	3	**

Table (5.1): Threshold and Sampling Rate Sensitivity Test Results

5.3 Lab Conclusions

The main objective of the lab tests was to evaluate the performance of the signal detector in terms of signal detection accuracy and response time. The performance of ride through mechanism was also evaluated.

It can be concluded from ongoing discussion that the signal detector has demonstrated all the required capabilities for islanding detection application. Tests have shown that the current signal detector can accurately detect zero crossing distortion type signals. The ride through mechanism helps avoid nuisance tripping due to temporary loss of signal while the system is not islanded. Most importantly, the response time of detector is well within limits that may be imposed due to operation of reclosers in the distribution line.

Chapter 6

CONCLUSIONS AND RECOMMENDATIONS

This thesis presents the development of a novel method of signal monitoring for the detection and prevention of islanding of distributed generators. The investigation was intended to determine the potential of using a distribution line communication technique for DG islanding prevention and the development of a signal detector.

Review of an islanding detection technique proposed by the Power Engineering Group at the University of Alberta is discussed in chapters 1 and 2 along with a study of currently available islanding detection technologies. A brief description of the proposed signal generation mechanism is also presented in Chapter 2. It is concluded that the proposed scheme can provide a better alternative to the existing islanding detection techniques. However, a new signal detection method is required to apply this signaling technique for islanding detection.

The next step was to verify the results presented in literature regarding signal propagation characteristics. PSCAD simulation programs were developed to observe the effects of load and VAR compensation variation on signal characteristics, and the results are presented in Chapter 3. It was observed that signal strength increased with decreasing loads on the network and that change in capacitance also caused change in signal frequency. It was also observed major part of the signal oscillation is confined about the

zero-crossing point. Requirements of the signal detection technique were established based on conclusions drawn in chapters 2 and 3.

Chapter 4 describes the new signal detection method in detail. The objective of developing the new signal detection technique is to have a reliable signal detection mechanism and a response time to indicate loss of signal smaller than the recloser operation time. Complete cycle comparison and ride-through mechanism are the salient features of the new technique.

Experimental tests were conducted in the lab to evaluate the performance of the detection device. Results of these tests are presented in Chapter 5. Accuracy of signal detection and response time of detector are the performance parameters of interest. After the initial troubleshooting and debugging phase, the device exhibited desired response and detected loss of signal in all tests. Detection of signal loss was virtually instantaneous; there was no detectable delay between the deactivation of signal and indication by the detector that the signal was lost. The working of the ride-through mechanism was also verified by modulating one in every seven cycles and by temporarily introducing noise.

The potential of DG technology to become an important part of present day electric distribution systems, and limited capabilities of available islanding detection techniques inspired the work presented in this thesis. Previous work in this area revealed

that there was a need for a reliable and inexpensive method of detecting and preventing formation of power islands in distribution networks with DG sources.

Current islanding detection and prevention schemes with the islanding detection device at the DG facilities can fail at a certain range of loads in the island. This range of loads, known as non-detection zones (NDZ), lies in the range of loads that can be observed in actual power systems. Even if measures are taken to eliminate the NDZ, some techniques suffer from other drawbacks such as power quality degradation and the requirement of expensive additional equipment. Some schemes work only with custom made generators. Based on these observations, the study was targeted to develop a simple, reliable and inexpensive technique that would have no NDZ and minimal effect on power quality.

A signaling method was chosen at the University of Alberta after an extensive study of available distribution line communication technologies. The main reasons for selecting zero crossing distortion technique are simplicity of signal generation and the lack of signal coupling requirements, and most importantly, the proven success of this technology in AMR application. As the distance between substation and DG may be in the range of 15-40km, signal attenuation had to be small; otherwise, line repeaters or signal boosters may have been required, adding to the cost. The signalling technique meets all these requirements.

The primary objective of this research was to develop a signal detection scheme that can monitor the signal and indicate if signal has been lost, in real time. Due to the dynamic nature of distribution networks and various noise sources, there is a certain possibility that signal may be undetectable for a very short time even though islanding has not taken place. A ride through mechanism has been implemented in the detection scheme to avoid nuisance tripping of the DG. Tripping takes place if the signal is not detected for time equivalent to 10 cycles (~167 ms). This delay time can be increased if recloser operation is slow.

The signal detection algorithm requires that the system voltage be monitored continuously; therefore, it is very easy to implement under/over voltage and frequency functions as described in the Alberta Technical Guide for DG interconnections or IEEE guidelines. In the case of a voltage or frequency anomaly, over/under frequency/voltage will overrule the signal detection method of islanding detection for the inter-tie disconnection.

Laboratory test results illustrate successful implementation of the islanding detection scheme. The signal detection scheme is application specific and has features that rectify problems associated with older automated remote meter reading (AMR) specific detection methods. Some of the features of islanding prevention scheme can be summarised as follows:

- Non-detection Zones are virtually absent
- Technology is easy to implement, inexpensive and reliable
- Laboratory tests have verified the proof of concept

A novel signal detection scheme for the purpose of islanding prevention has been developed. Laboratory tests have demonstrated the proof of concept. There is good potential of commercialization of this concept.

This research has established the proof of concept for using zero-crossing distortion type signals for islanding detection of DG's. Lab tests indicate that the proposed scheme has good potential to be successful in the field. Further investigation work in this research area is required to bring the technology up to a level where it can be applied in the field on medium voltage distribution networks.

As a next step, a signal generator should be developed that can generate signal on a distribution voltage levels. After preliminary functional testing and evaluation of the signal generator and detector, field tests should be conducted. Signals should be generated by modulating voltage at the substation, and the signal detector should be tested at DG and customer sites supplied by the substation. The response time and accuracy of signal detection should be evaluated along with effects of DG penetration level on signal propagation characteristics. Upon successful completion of the field tests, this technology can be commercialized and improvements in signal generator and detector can be implemented as dictated by the performance requirements.

The final step in this research will be to integrate AMR and islanding detection systems. Channel sharing or timesharing or both might be required for the parallel operation of the two systems. The signal detection scheme will need adjustments for seamless integration with the AMR system. Major research effort is required to estimate the level of interference between the two communication systems and to find ways to minimize its effects on the performance of both. A close collaboration with the TWACS® organization will be required for successful integration of islanding detection and AMR systems.

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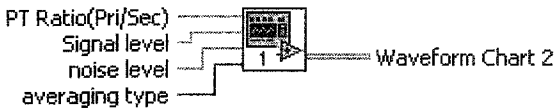
Appendix A

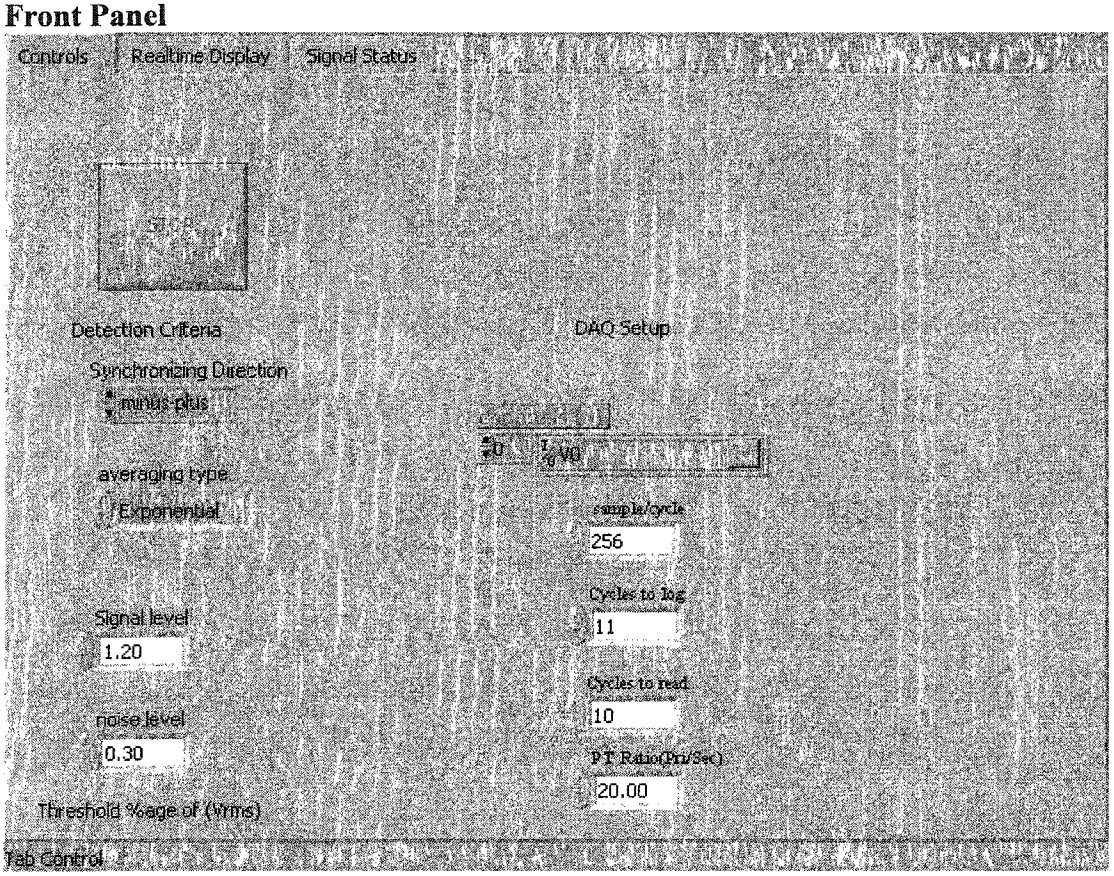
LABVIEW CODE

dtctnBWfltr_data1.vi

Connector Pane



Front Panel



Controls and Indicators

sample/cycle

Cycles to log

Cycles to read

PT Ratio(Pri/Sec) This is the PT ratio if you use it in station. ratio=primary:secondary, for example, if primary=10kV, secondary=100V, then input 100. input 1 if you use voltage probe only

channels (0) channels specifies the set of analog input channels.

channel (0) channels specifies the set of analog input channels.

averaging type averaging type is the type of averaging used during the measurement. In this single-point-per-block VI, the integration time is selected automatically by your input record length.

Synchronizing Direction direction is the kind of zero crossing. The user can choose from either, minus-plus, and plus-minus.

Signal level

noise level

Tab Control

Waveform Chart 2

scan backlog scan backlog is the amount of data remaining in the buffer after this VI completes.

Signal lost

List of SubVIs

Zero Crossing PtByPt.vi
C:\Program Files\National Instruments\LabVIEW 6.1\vi.lib\ptbypt\Other Functions.llb\Zero Crossing PtByPt.vi

Basic Averaged DC-RMS.vi
C:\Program Files\National Instruments\LabVIEW 6.1\vi.lib\measure\madcrms.llb\Basic Averaged DC-RMS.vi

Basic Averaged DC-RMS for 1 Chan.vi
C:\Program Files\National Instruments\LabVIEW 6.1\vi.lib\measure\madcrms.llb\Basic Averaged DC-RMS for 1 Chan.vi

AI Start.vi
C:\Program Files\National Instruments\LabVIEW 6.1\vi.lib\daq\ai.llb\AI Start.vi

AI Config.vi
C:\Program Files\National Instruments\LabVIEW 6.1\vi.lib\daq\ai.llb\AI Config.vi

AI Read.vi
C:\Program Files\National Instruments\LabVIEW 6.1\vi.lib\daq\ai.llb\AI Read.vi

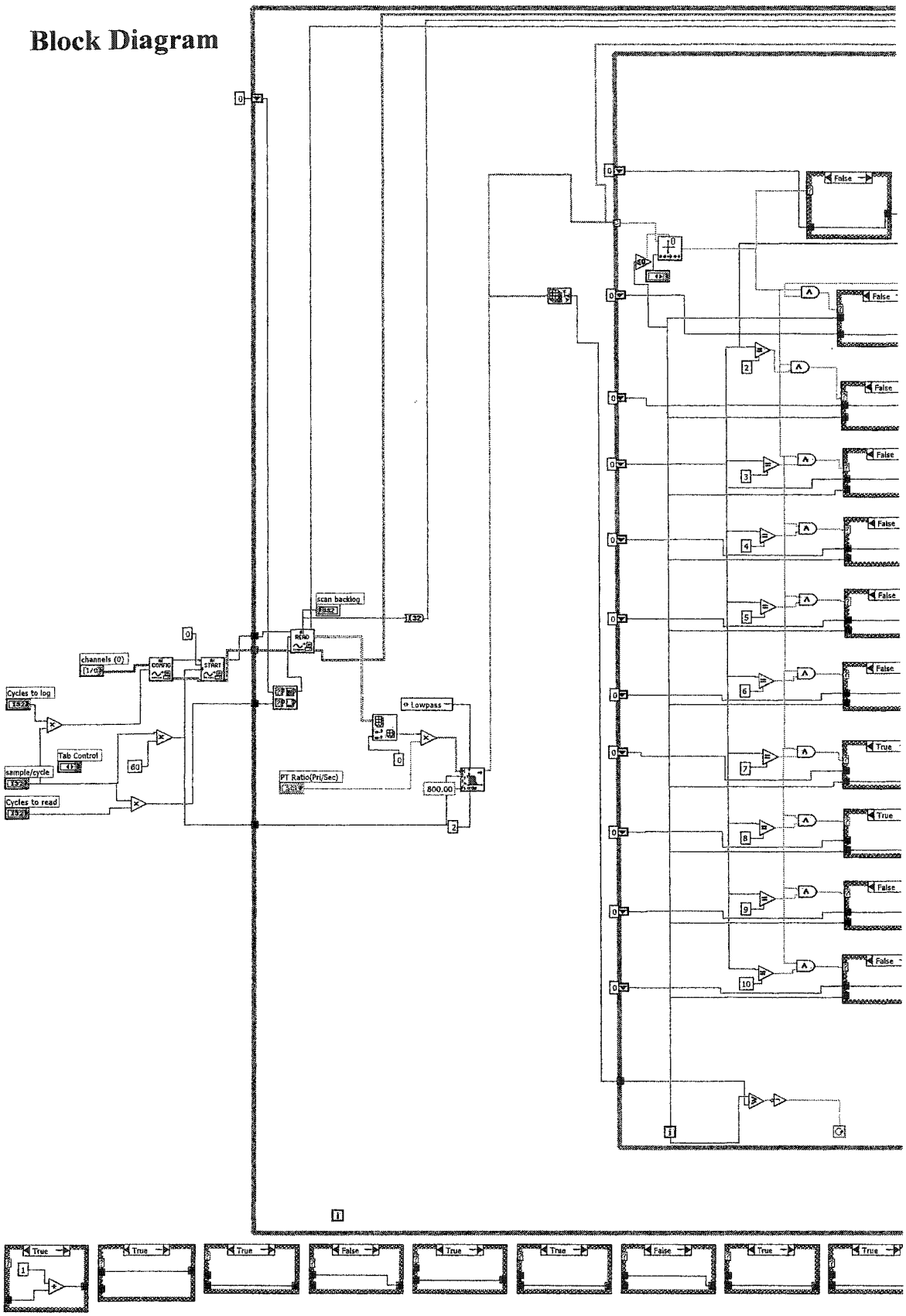
AI Read (scaled array).vi
C:\Program Files\National Instruments\LabVIEW 6.1\vi.lib\DAQ\ai.llb\AI Read (scaled array).vi

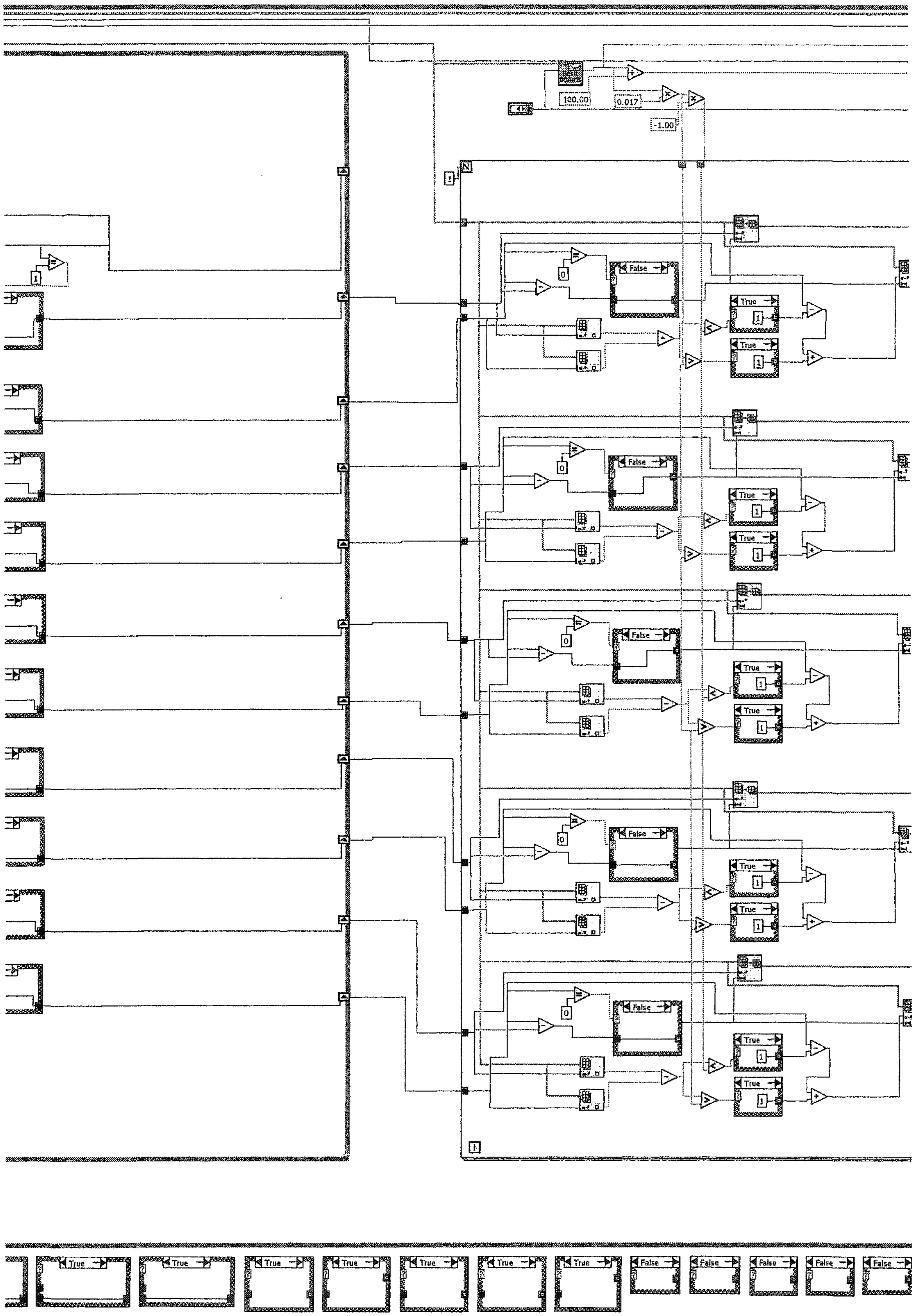
AI Clear.vi
C:\Program Files\National Instruments\LabVIEW 6.1\vi.lib\daq\ai.llb\AI Clear.vi

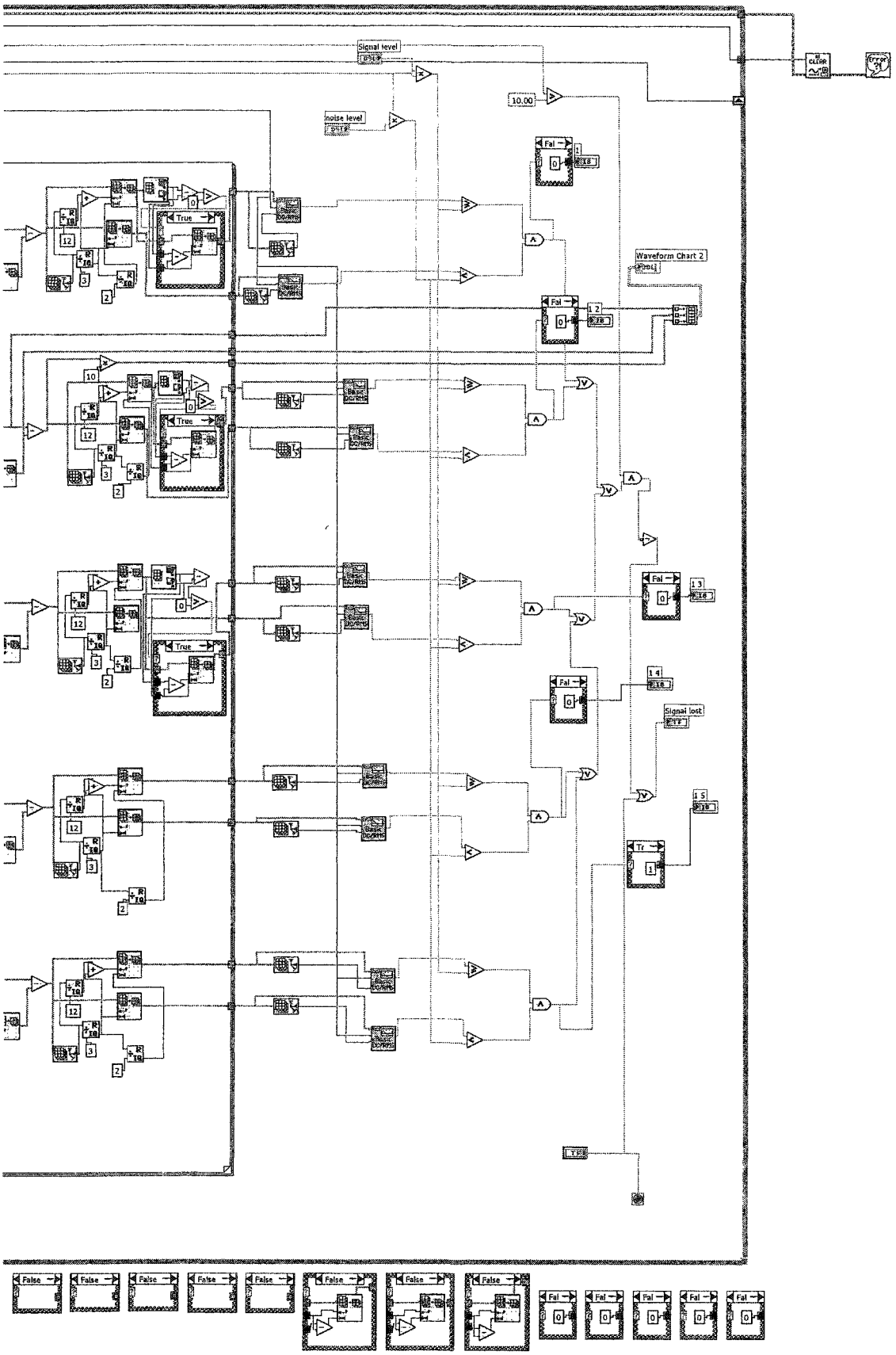
Simple Error Handler.vi
C:\Program Files\National Instruments\LabVIEW 6.1\vi.lib\Utility\error.llb\Simple Error Handler.vi

Butterworth Filter.vi
C:\Program Files\National Instruments\LabVIEW 6.1\vi.lib\Analysis\3filter.llb\Butterworth Filter.vi

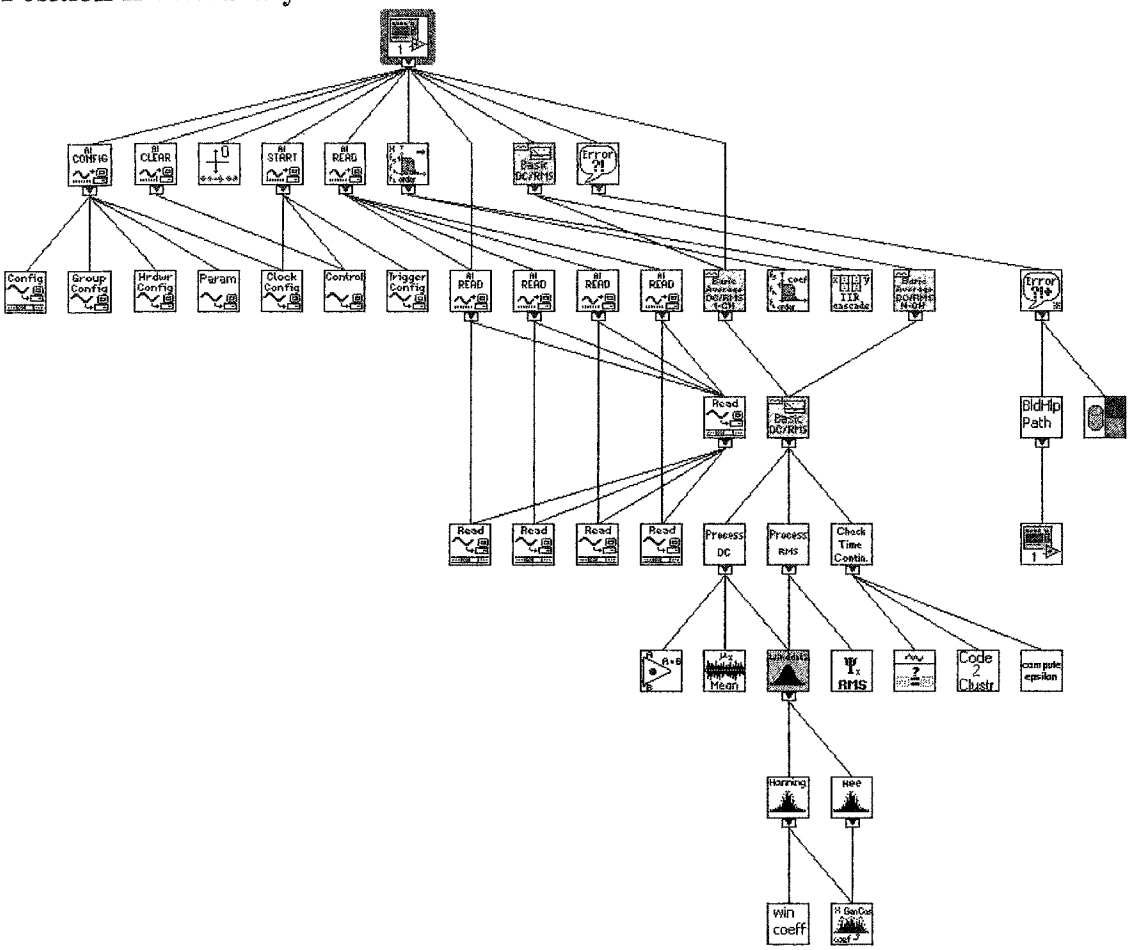
Block Diagram







Position in Hierarchy



Appendix B

MATLAB PROGRAM – SLOPE-BASED ALGORITHM

```
%%%%%%%%%% Algorithm 1: Time based  %%%%%%%%%%%%%%%
load cus1.txt
Aab = cus1(:,4)-cus1(:,5);
A = Aab;

j = 1;
i  = 200;
R = [];
n = 1;
V = [];
Vav = 0;
rate = 0;
%%%%%%% Calculate sampling rate per cycle and avg voltage %%%%%%%
for n = 1:5
  while n<=5
  if A(i) < 0
    if A(i)*A(i+1)<=0
      if A(i+3) > 0
        x = i;
        break
      else
        i = i+1;
      end
    else
      i = i+1;
    end
  else
    i = i+1;
  end
  end
  i = i+5;
  while n<=5
  if A(i) < 0
    if A(i)*A(i+1)<=0
      if A(i+3) > 0 %%(To avoid multiple zero-crossings)%%
        y = i;
        break
      else
        i = i+1;
      end
    else
```

```
        i = i+1;
      end
    else
      i = i+1;
    end
    end
    r = y - x;
    rate = (rate+r);
    V = abs([A(x:y)]);
    Vav = Vav+sum(V,1)/(y-x);
    n = n+1;
  end
  sr = round(rate/(n-1));
  Vavg = Vav/(n-1);
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  i = 210120;
  n = 440000;
  v0 = 2*Vavg*sin(135*pi/180);
  v1 = 2*Vavg*sin(150*pi/180);
  v2 = 2*Vavg*sin(160*pi/180);
  v3 = 2*Vavg*sin(175*pi/180);
  v4 = 2*Vavg*sin(185*pi/180);
  v5 = 2*Vavg*sin(190*pi/180);
  v6 = 2*Vavg*sin(200*pi/180);
  R = [];
  x = 0.35;
  y = 0.35;
  z = 0.35;
  T = A;
  while i < (n-sr)
  while i<n
    if T(i,j)< 0
      if T((i+2),j)<=0
      break
    else
      i = i+1;
    end
  else
    i = i+1;
  end

  end

  while i < n
    if T(i,j)*T(i+1,j)<=0
      break
```

```
  else
    i = i+1;
  end
end

while i<n
  if T(i+1,j)-T(i,j)< 0
    if T(i+1,j)-v0 <=0
      t0 = i+(T(i,j)-v0)/(T(i,j)-T(i+1,j));
      break
    else
      i = i+1;
    end

    else
      i = i+1;
    end
end


while i<n
  if T(i+1,j)-T(i,j)< 0
    if T(i+1,j)-v1 <=0
      t1 = i+(T(i,j)-v1)/(T(i,j)-T(i+1,j));
      break
    else
      i = i+1;
    end

    else
      i = i+1;
    end
end

while i<n
    if T(i+1,j)-v2 <=0
      t2 = i+(T(i,j)-v2)/(T(i,j)-T(i+1,j));
      break
    else
      i = i+1;
    end
  end

while i<n
    if T(i+1,j)-v3 <=0
      t3 = i+(T(i,j)-v3)/(T(i,j)-T(i+1,j));
```

```
      break
    else
      i = i+1;
    end
  end

while i<n
    if T(i+1,j)-v4 <=0
      t4 = i+(T(i,j)-v4)/(T(i,j)-T(i+1,j));
      break
    else
      i = i+1;
    end
  end

while i<n
    if T(i+1,j)-v5 <=0
      t5 = i+(T(i,j)-v5)/(T(i,j)-T(i+1,j));
      break
    else
      i = i+1;
    end
end

while i<n
    if T(i+1,j)-v6 <=0
      t6 = i+(T(i,j)-v6)/(T(i,j)-T(i+1,j));
      break
    else
      i = i+1;
    end
  end

  delt0 = t2-t0;
  delt1 = t2-t1;
  delt2 = t4-t3;
  delt3 = t6-t5;


while i < n-330
   if T(i,j)*T(i+1,j)<=0
     break
  else
    i = i+1;
  end
end
```

```
while i<n
  if T(i+1,j)-T(i,j)< 0
    if T(i+1,j)-v0 <=0
      t00 = i+(T(i,j)-v0)/(T(i,j)-T(i+1,j));
      break
    else
      i = i+1;
    end

    else
      i = i+1;
    end
end


while i<n
  if T(i+1,j)-T(i,j)< 0
    if T(i+1,j)-v1 <=0
      t11 = i+(T(i,j)-v1)/(T(i,j)-T(i+1,j));
      break
    else
      i = i+1;
    end

    else
      i = i+1;
    end
end

while i<n
    if T(i+1,j)-v2 <=0
      t22 = i+(T(i,j)-v2)/(T(i,j)-T(i+1,j));
      break
    else
      i = i+1;
    end
  end

while i<n
    if T(i+1,j)-v3 <=0
      t33 = i+(T(i,j)-v3)/(T(i,j)-T(i+1,j));
      break
    else
      i = i+1;
    end
```

```
  end

while i<n
    if T(i+1,j)-v4 <=0
      t44 = i+(T(i,j)-v4)/(T(i,j)-T(i+1,j));
      break
    else
      i = i+1;
    end
  end

while i<n
    if T(i+1,j)-v5 <=0
      t55 = i+(T(i,j)-v5)/(T(i,j)-T(i+1,j));
      break
    else
      i = i+1;
    end
end

while i<n
    if T(i+1,j)-v6 <=0
      t66 = i+(T(i,j)-v6)/(T(i,j)-T(i+1,j));
      t77 = i+1;
      break
    else
      i = i+1;
    end
  end

  delt00 = t22-t00;
  delt11 = t22-t11;
  delt22 = t44-t33;
  delt33 = t66-t55;
while i<n
if abs(delt1-delt11) > x
  if abs(delt2-delt22) > y
      s = 1;
      R = [R s];
      elseif abs(delt3-delt33) > z
      s = 1;
      R = [R s];
      break
    else
    end
  else
```

```
  end

 if abs(delt2-delt22) > z
    if abs(delt3-delt33) > z
      s = 1;
      R = [R s];
      break
    else
      s = 0;
      R = [R s];
      break
    end

  else
    s = 0;
    R = [R s];
    break
   end
end
    if i >= (n-2*sr)
     break
  end
end
stairs(R)
```