IEEE Open Journal of the
Industrial Electronics Society

Received 12 August 2020; revised 11 September 2020; accepted 20 September 2020. Date of publication 22 September 2020; date of current version 3 October 2020. The review of this paper was arranged by Associate Editor Hong Li.

Digital Object Identifier 10.1109/OJIES.2020.3025927

Heterogeneous Real-Time Co-Emulation for Communication-Enabled Global Control of AC/DC Grid Integrated With Renewable Energy

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This work was supported by the Natural Science, and Engineering Research Council of Canada (NSERC).

ABSTRACT The information, and communication technologies (ICTs) are increasingly merging with the conventional power systems. For the design, and development of modern AC/DC grids with integrated renewable energy sources, the system-level control schemes with ICTs involved should be evaluated in a co-simulation framework. In this work, a heterogeneous hardware real-time co-emulator composed of FPGAs, many-core GPU, and multi-core CPU devices is proposed to study the communication-enabled global control schemes of hybrid AC/DC networks. The electromagnetic transient (EMT) power system emulation is conducted on the Xilinx FPGA boards to provide nearly continuous instantaneous waveforms for cyber layer sampling; the communication layer is simulated on the ARM CPU cores of the embedded NVIDIA Jetson platform for flexible computing, and programming;, and the control functions for modular multi-level converters are executed on GPU cores of the Jetson platform for parallel calculation. The data exchange between FPGAs, and Jetson is achieved via the PCI express interface, which simulates the sampling operation of the AC phasor measurement unit (PMU), and DC merging unit (DC-MU). The power overflow, and DC fault cases are investigated to demonstrate the validity, and effectiveness of the proposed co-emulation hardware architecture, and global control schemes.

INDEX TERMS Co-emulation, communication network simulation, cyber-physical systems, electromagnetic transients, embedded systems, field programmable gate arrays, graphics processors, multi-processing, real-time systems, renewable energies.

I. INTRODUCTION

WITH the development of modern power systems, the information and communication technologies (ICT) are increasingly involved in the control, protection and normal operation of power system equipment and infrastructure, which introduced the so called cyber-physical system concept. In such a system, various power equipment such as the generator, circuit breaker and power electronics converter can be controlled by the centralized system-level controller through communication links [1]. The ICT-enabled power system operation and control needs to be evaluated in a co-simulation platform, which creates new challenges to the existing power system simulators [2], [3].

To simulate the entire behaviours of a cyber-physical system, the precise evaluation of power and communication system is required while the interaction between the two domains should also be considered. The existing co-simulation research is mostly focused on the software-based approaches to combine the simulators in the two domains together by designing specific data exchange interface and synchronization policies. Such software-based co-simulators mainly distinguish from each other by the type of power/communication system simulators used, the scheme of data exchange between the two domains, and the application scenarios. For example, both the network-simulator-2 (NS-2) and NS-3 were used in [4]–[8] for communication network modeling in

the co-simulation, and the open-source discrete event based simulator OMNeT++ was used to model smart grid in [9]–[11]. The global event-driven co-simulator (GECO) [12] interfaced the power system dynamic simulator PSLF and network simulator NS-2, and the synchronization is based on a global event driven on-demand mechanism. The combination of power system transient simulator PSCAD/EMTDC [13] and network simulator NS-2 is utilized in the electric power and communication synchronizing simulator (EPOCHS) [14], and the application scenario is the wide area monitoring. The performance of the above software-based co-simulators is dramatically limited by the software environment, which face difficulties to perform fast simulation for large-scale cyber-physical power systems.

On the other hand, the AC/DC grid with integrated renewable energies proposes challenges to the system-level control for stability, security and fault recovery [15], [16]. The power generated by renewable generators such as offshore wind farms is transmitted to the AC grid through the high voltage DC (HVDC) transmission, which should be controlled dynamically to match the generation and consumption. The existing AD/DC control schemes mostly focused on the control algorithm for a single modular multilevel converter (MMC) [17], [18], or the control strategy in a small scale system without communication networks involved [19]–[21]. However, the local measurement based control is not optimized in the system-scale and easily delayed without a global view [22]. The cyber layer creates the required capabilities to perform the global measurement and control, and ICT-enabled power electronic converters that play important roles for power flow control can also receive the control command from the system-level controller to change the corresponding parameters. This type of control for the cyber-physical AC/DC grid with integrated renewable energies should be evaluated in terms of system stability, but to the best of our knowledge, it has not been studied in the previous co-simulation work and remains to be investigated.

Based on the above observations, this work proposes an heterogeneous real-time EMT-based power and communication system co-emulator realized on multiple Jetson and FPGA platforms for global control of hybrid AC/DC networks. The NVIDIA Jetson AGX Xavier embedded platform [23] is an artificial intelligence (AI) computer for autonomous machines, delivering the performance of a 512-core GPU workstation within an embedded module, which can perform heavy computation tasks. Taking advantage of the PCI express (PCIe) interface based connection between Jetson and the FPGA, a complete hardware solution is developed to provide all the required capabilities for cyber-physical system co-emulation. The contributions of this work are summarized as follows:

1) The EMT-based power system emulation is executed on FPGA boards with a microsecond level time-step, which can provide a nearly continuous measurement to the AC and DC sampling unit; the MMC converter control functions and communication modules run on the Jetson embedded platform, which perform fast and flexible computation for complex tasks;
2) The interaction between the two domains are emulated in a realistic way: power system measurement data sampling and converter controller sampling operation is achieved via the read operation from the FPGA memory, and the control and protection commands are pushed to the power system emulation via the write operation to the FPGA memory;
3) Based on the proposed heterogeneous co-emulation architecture, the global control schemes are studied on the AC/DC grid integrated with wind farms. By utilizing the communication network to perform global control strategies with fast responses, the influence of power overflow and DC fault can be reduced efficiently.

The rest of the paper is organized as follows: Section II describes the ICT-enable hybrid AC/DC grid with latest development of smart power equipment. Section III proposes the Jetson-FPGA based co-emulation hardware architecture. Section IV introduces the hardware implementation details of proposed co-emulator for the test system. Section V presents the emulation results based on the global control schemes. Finally, the conclusions are drawn in Section VI.

II. ICT-ENABLED HYBRID AC/DC GRID

This section introduces the AC/DC test power system with integrated renewable energies, the corresponding communication network, and the ICT-enabled power equipment.

A. HYBRID AC/DC POWER SYSTEM

To investigate the global control and protection of modern power systems, a hybrid AC/DC grid composed of onshore and offshore generation, AC and DC transmission, AC/DC and DC-DC converters as well as renewable energy sources is required. In this work, the AC/DC grid composed of an onshore IEEE 39-bus system [24], a subsystem of the CIGRÉ B4 DC test grid [24] and 2 offshore wind farms is chosen as the test system, which can emulate a modern AC/DC power system practically. The CIGRÉ DC grid consists of three interconnected DC systems (DCSs) called DCS1, DCS2, and DCS3, and the bipole HVDC meshed grid DCS3 with $\pm$200 kV is selected for DC test system, as shown in Fig. 1. The MMC converter topology is applied to the AC/DC converters. The offshore wind farms are responsible to power generation, and the generated power is transmitted to the AC grid through the AC/DC and DC/AC conversion. Such a complex AC/DC power system not only creates challenges for system-level control and protection under different contingencies, but also makes the real-time co-emulation of EMT-based power system and communication network quite challenging.

B. COMMUNICATION NETWORK

With the cyber layer involved, the real-time status of the power system can be measured and gathered, and then the global view based control strategies can be performed. The

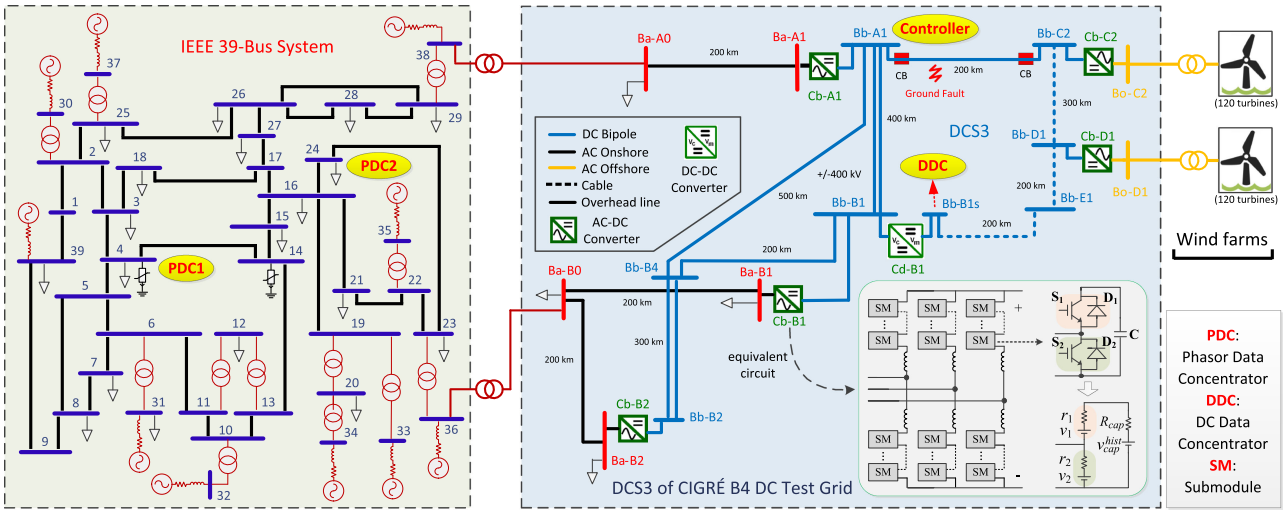

FIG. 1. Hybrid AC/DC test power system used in this work.

communication network is built based on the advanced metering infrastructure (AMI), for example, typically in each bus or substation, the merging unit (MU) is deployed to gather the signals from voltage and current sources at a synchronized sampling rate. Although the communication links are not revealed in Fig. 1, in this work, each AC bus is assumed to have a phasor measurement (PMU) [25] installed, and each DC bus is assumed to have a DC merging unit (DC-MU) installed, which compose the basic communication element in the cyber layer.

The PMU at AC buses can use the digital samples obtained by MU to compute the phasor values and periodically report to the control system, where a phasor is a complex quantity to present the sinusoidal wave of an electrical signal. For example, a sinusoidal signal is given as:

$$x(t) = X_m \cos(\omega t + \varphi), \tag{1}$$

where X_m is the magnitude of the waveform, and φ is the angular starting point. Then the corresponding phasor is expressed using the RMS value:

$$X = \frac{X_m}{\sqrt{2}}\angle\varphi = \frac{X_m}{\sqrt{2}}(\cos\varphi + j\sin\varphi) = X_r + jX_i \tag{2}$$

The rule of PMU is to estimate the magnitude and angle of a signal according to the sampling measurements. For DC buses, the DC voltage, current, and power are measured by DC-MU since there is no phasor data.

The control system is built on the cyber layer, in which the local controllers and centralized system-level control center are connected via specific control network architectures such as the tree-based topology and mesh topology. The local controller can be a phasor data concentrator (PDC) that collects AC phasor measurements from PMUs in its region, or a DC data concentrator (DDC) that collects DC measurements from DC-MUs. The measurement collection operation of PDC is performed using a specific reporting rate [25]. In fact, the main function of the communication network is to provide a two-way communication between smart meters and controllers to modify the related circuit parameters according to the service requirements. In this work, two PDCs (PDC1 and PDC2) are deployed at AC Bus4 and Bus24, and one DDC is deployed at DC bus Bb-B1s, as shown in Fig. 1. The system-level controller is deployed at Bb-A1.

C. ICT-ENABLED POWER SYSTEM EQUIPMENT

In the conventional power system, the power equipment is generally controlled by electrical quantities locally. In cyber-physical power systems, the ICT-enabled devices can receive control commands from remote controllers to change the corresponding parameters. By utilizing the ICT-enabled controllable power equipment, flexible strategies and fast response to faults can be realized. Typically, the AC/DC circuit breakers (CBs) are ICT-enabled for protection. For example, when a DC line ground fault is detected by a DC breaker, the line could be isolated by the DC breaker immediately; but the corresponding fault information is required to be sent to the centralized controller for subsequent stability control. The communication functions are also increasingly deployed in generator and controllable load for flexible power supply and load balancing. For example, if the power generated from a machine exceeds the consumption, the corresponding control command from the control center can guide the machine to reduce power generation or just close the supply for a period. Another important power system equipment is the converter in DC grid, which is typically controlled by the outer/inner loop control and modulation schemes for DC voltage or power regulations. However, with ICT involved, the power electronics converter can also receive the control command from remote controllers to change the values of regulated quantities according to system-level purpose [26].

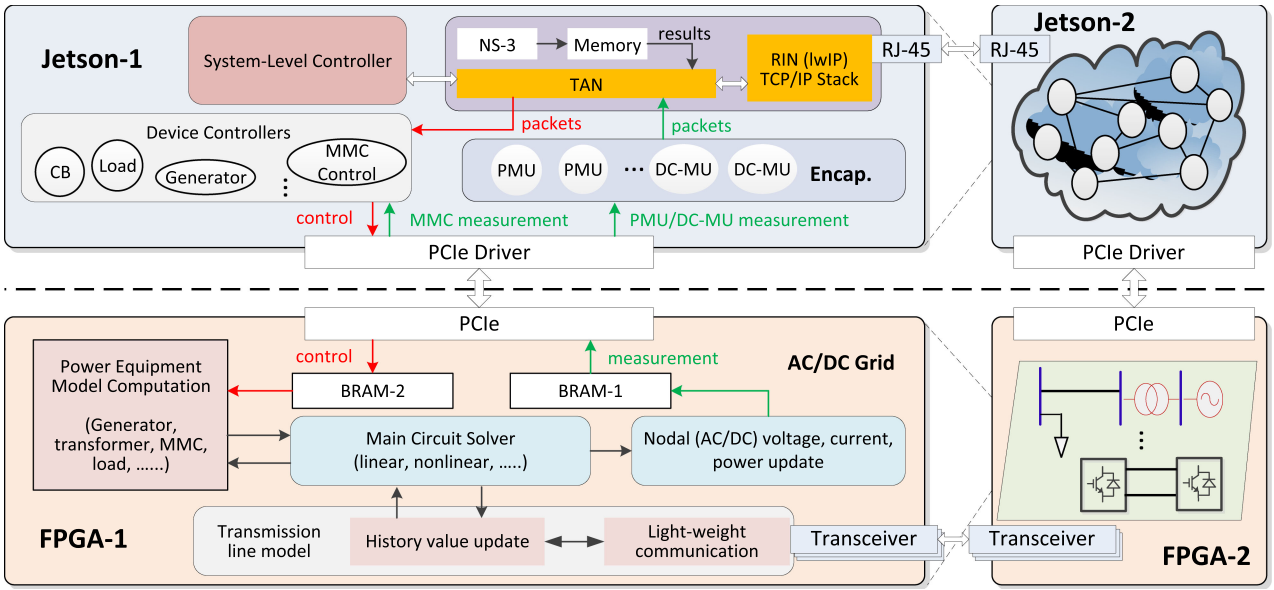

FIG. 2. **Top level architecture of the heterogeneous co-emulation hardware architecture on the multiple Jetson-FPGA platform.**

III. HETEROGENOUS REAL-TIME CO-EMULATION ARCHITECTURE ON MULTIPLE JETSON-FPGA PLATFORM

Based on the above introduced aspects in cyber-physical power systems, this section describes the proposed real-time co-emulation architecture on the Jetson-FPGA embedded platform.

A. CO-EMULATION ARCHITECTURE

The top-level architecture of the proposed co-emulation architecture is shown in Fig. 2, wherein the power system EMT emulation and communication network simulation are separated to the FPGA and Jetson respectively. Since the two FPGA and Jetson embedded platforms have the same processing architecture, only one detailed architecture of the Jetson-FPGA platform is shown in Fig. 2. For the interaction between the two domains, the PCIe bus is used to connect the FPGA and Jetson platform. The two block RAMs (BRAM-1 and BRAM-2) are used to store the measurement data and control command respectively: after the calculation of each time-step (at microsecond level for EMT emulation), the nodal voltages, currents and other power quantities of interest are written to BRAM-1; while the BRAM-2 is used to receive the control command from the control center or the gate signals from the MMC control functions. The multi-board scheme is also be applied to extend the resources for large-scale system simulation.

The data exchange and synchronization between the two domains mainly refers to two operations: measurement data sampling, and control command provisioning. These two operations become quite convenient in the proposed co-emulation architecture: for the measurement data sampling operation, the simulated PMUs and DC-MUs in the Jetson embedded platform can read the measurement data from BRAM-1 via the PCIe driver function at a configurable rate; for the control command delivery, the corresponding instructions can be written to BRAM-2 at any time to change the circuit parameters in the FPGA computation. These operations do not influence the normal simulation in the power system domain, which makes the real-time EMT emulation possible. Since the proposed heterogeneous co-emulator is targeting the real-time co-emulation of power system and communication network, the hybrid Jetson-FPGA hardware platform is utilized, which may not be as flexible as the pure software-based co-simulator and more programming effort needs to be invested when the emulated test system changes.

B. HYBRID AC/DC GRID EMT EMULATION

In this work, the EMT emulation is conducted for the power system, because it not only can capture the transient-level waveforms, but can also provide continuous signals due to the small time-step sizes so that the measured data to PMUs and DC-MUs is accurate enough. Typically, real-time emulation can be achieved on FPGA boards even for large-scale AC/DC grids [27]. However, in co-emulation, the extra operations are introduced: writing measurement data to BRAM-1 and reading control command from BRAM-2. The number of measured data is large if the electrical quantities of each bus are required, then it costs a considerable latency to write data to BRAM-1 since in each clock cycle only one data can be written. In this work, this operation is delayed for one time-step, which means, the results of the last time-step calculation are written to the BRAM-1 while the circuit is computed for the current time-step. Since the interval of sampling is larger than the time-step size of EMT emulation, the one time-step delay is acceptable. The same policy can be applied to the read operations to achieve real-time EMT emulation.

When the multi-board solution is adopted, the power system is decomposed into subsystems using the traveling-wave line model (TLM) or frequency-dependent line model (FDLM). Then the two ends of a transmission line can be computed in two FPGA boards concurrently and exchange their data after each time-step. This type of data exchange between the two FPGA boards should be executed via fast transmission protocol and transceivers to ensure the transmission delay is minimized for real-time emulation.

C. COMMUNICATION NETWORK EMULATION

The communication network is built on communication devices with specific protocols, thus the task of communication system simulation is to simulate the behaviour of network forwarding devices and transmission links. In the related works, various network simulators such as NS-2/NS-3, OpenNet, OMNet++ have been utilized to conduct the network-domain simulation. However, the existing solutions are not applicable to the proposed co-emulation architecture, because: 1) using the created virtual network, new interfaces are required to be developed for synchronizing the measurement data, which is time-costly and make the real-time co-emulation infeasible; 2) for large-scale AC/DC test power systems, hundreds of nodes need to be instantiated if each node is regarded with a PMU installed, then each node needs to receive the corresponding sampling data and generate data packets, which greatly increases the simulation latency.

Different from the pure network simulation that aims to investigate the packet transmission or test new protocols, the essential goal of the co-emulation is to study the influence of the cyber layer on the physical layer, i.e., how the power system is improved under the support of communication network. Therefore, the end-to-end communication parameters such as the transmission latencies and packet losses are of the greatest concern. Based on this observation, in this work, the communication module is implemented in a hybrid manner as shown in Fig. 2: transmission abstraction based networking (TAN) and real network interface based networking (RIN). TAN on a Jetson embedded platform is used for the networking within the corresponding power system area emulated on the connected FPGA board, which reads the results from the NS-3 simulator in advance and then uses the resulting transmission parameters to abstract the packet transmission. This simplification is to accelerate the co-emulation process to real-time, while the used transmission parameters obtained by the network simulator are also practical and reasonable. RIN is used for inter-board networking, which is executed on the real-world network interfaces of the Jetson embedded platform to simulate the packet transmission between different power system areas. The measurement data packet generation function is also included in the architecture, which is used to simulate the behaviour of PMUs and DC-MUs that sample measurement data from power system and encapsulate the measurement into network packets to be sent to the PDC.

IV. HARDWARE IMPLEMENTATION OF TEST SYSTEM

The test system is implemented on the Jetson-FPGA platform. Two Xilinx VCU118 FPGA boards and two NVIDIA Jetson embedded platforms are utilized.

A. HETEROGENEOUS CO-EMULATOR HARDWARE RESOURCES AND SET-UP

The Xilinx VCU118 evaluation board provides a hardware environment for developing and evaluating designs targeting the UltraScale+ XCVU9P-L2FLGA2104 device. The VCU118 evaluation board provides features common to many evaluation systems, including the dual small form-factor pluggable (QSFP+) connector and sixteen-lane PCI express interface. The 16-lane PCIe edge connector performs data transfers at the rate of 8.0 GT/s for Gen3 applications, and the XCVU9P-L2FLGA2104 device is deployed on the VCU118 to support up to Gen3 x8 channels. The two quad (4-channel) QSFP+ (28 Gb/s) connectors accept 28 Gb/s QSFP+ optical modules. Each connector is housed within a single 28 Gb/s QSFP+ cage assembly.

The NVIDIA Jetson embedded platforms provide the performance and power efficiency to run autonomous machines software. Each Jetson embedded platform is a complete System-on-Module (SOM), with CPU, GPU, PMIC, DRAM, and flash storage–saving development time and money. The 512-core Volta GPU with tensor cores, the 8-core ARM v8.2 64-bit CPU, 32 GB 256-bit memory, x8 PCIe interface and RJ45 gigabit ethernet interface enable the proposed heterogeneous co-emulation architecture to be completed implemented.

The two Xilinx FPGA boards run at the clock frequency of 100 MHz. The Ubuntu 18.04 Linux operating system runs on the NVIDIA Jetson embedded platform at 2 GHz frequency. According to the top level co-emulation architecture, the heterogeneous hardware platform set up is shown in Fig. 3. The digital-to-analog converter (DAC) adapter that connects the VCU118 board and oscilloscope is used to show the real-time waveforms; the two NVIDIA Jetson embedded platforms are connected via the RJ-45 ethernet port for network data packet transmission, while each Jetson embedded platform is connected with a VCU118 board via the PCIe cable; and the two VCU118 boards are connected via the QSFP+ transceivers for fast data exchange.

B. FPGA IMPLEMENTATION

The AC/DC grid is partitioned into two parts to be allocated to the two FPGA boards: IEEE 39-bus system and its connected AC buses in DCS-3 (Ba-A0, Ba-B0), and, the rest part of the grid. The applied AC equipment models are the same as those of PSCAD/EMTDC [13] used for verification: the synchronous machine is modeled as a Norton current source, and since the current source representation uses the terminal voltages to calculate the injected currents, a characteristic impedance is used to terminate the machine to the network; the AC4A type exciter control model [13] is attached with

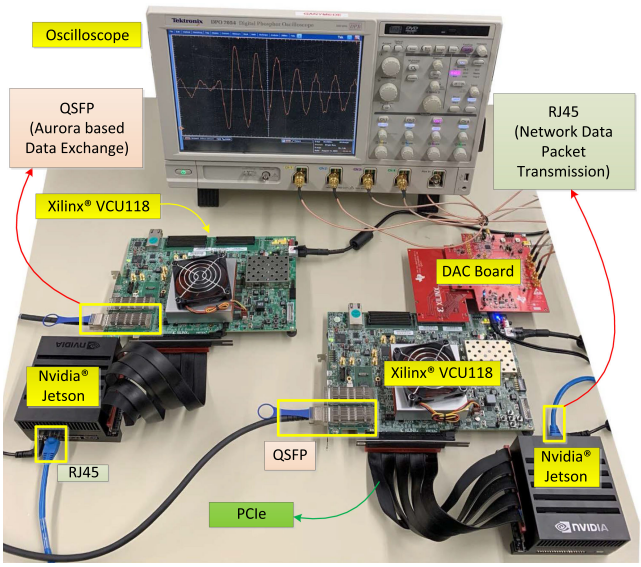

FIG. 3. **Hardware setup for the heterogeneous co-emulator.**

the machine to provide a feedback for the field voltage; the transformer model uses a conductance matrix generated by the equivalent RLC circuit to compute the voltages of the coupled winding terminals given a known equivalent current injection; the Bergeron transmission line model is a traveling wave line model, which utilizes the transmission latency of a line to decouple the two connected subsystems and make the concurrent computation of the two line ends possible.

For the MMC converter model, the two FPGA boards do not have enough resources to compute all the detailed models, and thus a hybrid modeling scheme is applied: the AC-DC and DC-AC converters use the ideal switch based equivalent circuit model, while the DC-DC converter is modeled as the DC transformers. The windfarm generator model is also simplified as duplication of a single generation unit [28], since the complex wind farm model involving hundreds of generation units consumes significant computation resources and is not the object of interest in this work. In the ideal switch based equivalent MMC model, the IGBT and diode nonlinear switching transients are ignored while only the electrical model is presented. The Thévenin equivalent circuit for each submodule (SM) is represented using $r_{sm,eq}$ and $v_{sm,eq}$ in series [29] as shown in Fig. 1:

$$r_{sm,eq} = \frac{r_2(r_1 + R_{cap})}{r_1 + r_2 + R_{cap}} \tag{3}$$

$$v_{sm,eq}(t) = \frac{r_{sm}}{r_2} v_2 + \frac{r_{sm}}{r_1 + R_{cap}} (v_{cap}^{Hist}(t - \Delta t) - v_1) \tag{4}$$

where $R_{cap} = \frac{\Delta t}{2C}$ is the equivalent resistance of the capacitor, r_1 and r_2 are equivalent resistances of the two switches, and the values are equal to R_{ON} or R_{OFF} depending on the gate signals (1 or 0). The capacitor voltage $v_{cap}(t)$ can be derived using Trapezoidal rule:

$$v_{cap}(t) = R_{cap} i_{cap}(t) + v_{cap}^{Hist}(t - \Delta t) \tag{5}$$

TABLE 1. **FPGA Hardware Resource Consumption of the Test System**

Board	LUT	FF	BRAM	DSP	Latency
VCU118-1	90.3%	95.2%	57.1%	91.2%	15.7μs
VCU118-2	93.1%	89.1%	50.3%	96.9%	18.6μs

where

$$v_{cap}^{Hist}(t - \Delta t) = R_{cap} i_{cap}(t - \Delta t) + v_{cap}(t - \Delta t) \tag{6}$$

After the main network equation composed of the equivalent circuit together with other electrical elements is solved, $i_{sm}(t)$ is known. Then the current through the capacitor of each SM is updated:

$$i_{cap}(t) = \frac{r_2 i_{sm}(t) + v_1 + v_2 - v_{cap}^{Hist}(t - \Delta t)}{r_1 + r_2 + R_{cap}} \tag{7}$$

Similarly, the Thévenin equivalence for one converter arm is the superposition of equivalent resistance and voltage of all SMs in the arm. In this work, the 51-level MMC converter structure is applied.

The PCIe connected memory BRAM-1 and BRAM2 are implemented as Xilinx IP cores with AXI-4 interfaces. BRAM-1 with size of 32bit $\times$ 1024 is used to store the measurement data, including the three phase nodal voltages and line currents, which is enough to for storing measurements of the subsystem in one FPGA board. For BRAM-2, the control command is mainly used for the converters and generators. The control command for generators instructs if the turbines of the wind farms should power off or not; while the control command for converters refers to the reference values of the controlled quantities and the gate signals for ideal switch based equivalent MMC model. Since a 32-bit control command can contain several switch signals, the size of 32bit $\times$ 1024 is also adopted.

The fast data exchange of the transmission line history items between the two FPGA boards is achieved by using the simple lightweight communication core, the Xilinx Aurora core. The AXI4-stream user interface enables convenient connection between other modules. The experimental test shows that after about 60 clocks of link initialization, the 64-bit data can be transferred between two boards continuously, which means that the latency of transferring n 64-bit data is about $(n + 60)$ clocks.

The hardware resource consumption and maximum processing latency for one time-step computation are presented in Table 1. It can be observed that the resource costs of the two boards are relatively balanced to fully exploit the FPGA programmable resources. The processing latency of one time-step indicates the minimum time-step size that can be applied for real-time EMT emulation. Note that the BRAM read and write operations are one time-step delayed, which can be done when the other calculations are being performed. Therefore, the two boards can use the same time-step size of 20 μs.

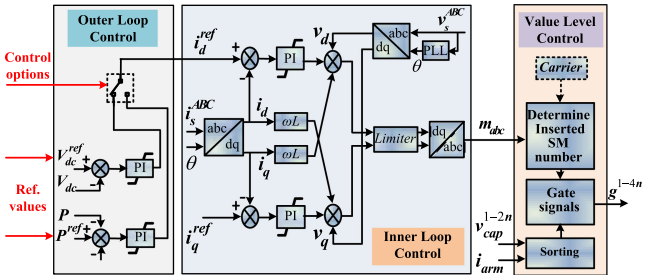

FIG. 4. The ICT-enabled PD-SPWM MMC control scheme.

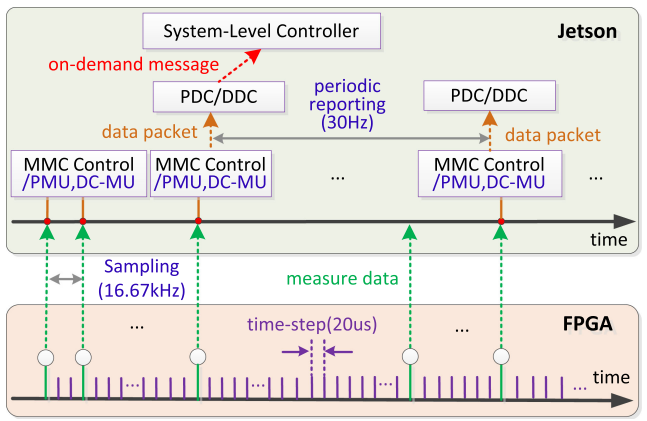

FIG. 5. Demonstration of interaction between power system emulation and communication network simulation.

C. JETSON IMPLEMENTATION

The MMC controller function is computed in the Jetson, which is composed of the outer loop control, inner loop control, and the value-level control, as shown in Fig. 4. The outer loop control uses the terminal DC voltage or active power as the reference to generate control signals; the inner current loop control is to generate the modulation signals, which uses the phase-disposition sinusoidal pulse width modulation (PD-SPWM) method [30]; the value-level control is used to generate gate signals for each switch in MMC. In this work, the MMC converters (Cb-A1, Cb-B1, and Cb-B2) connecting to the on-shore 39-bus system are utilized for DC voltage regulation, while the other two converters control the active power flow. This configuration can also be changed during the emulation according to system-level operations, since the controlled quantities and reference values are configurable by the system-level controller, as shown in Fig. 4. These MMC controllers of different MMC converters are computed in the GPU cores of the Jetson embedded platform to fully leverage the parallel capabilities of the heterogeneous platform. The MMC controller measurement sampling rate is set as same as the PMU and DC-MU sampling rate for simplicity: every 60 μs the values are sampled as shown in Fig. 5, which is about 278 samples per cycle (16.67 kHz) for the 60 Hz power system.

The packet generation module uses the PCIe driver functions to read the measurement data in BRAM-1 of the FPGA at the sampling rate. Then the corresponding phasors are computed using the measurement voltage and current, and the phasor data are encapsulated as the network packets and sent to the PDC functions with a reporting rate of 30 Hz. This process is to simulate the measurement operation of PMUs and DC-MUs. The IEEE Std. C37.118.2 [31] primarily describes the presentation of synchrophasor data packet in a bit-mapped format. The standardized communication protocol, IEC 61850 - Communication Networks and Systems in Substations [32], also describes a similar approach to presentation and has been mainly used in the communication between protection relays and control systems. In this work, the bit-map of the packet follows IEC 61850. The PDC/DDC function checks the received phasor data or DC data to see if there are abnormal conditions; and if abnormal conditions are detected, the corresponding messages are sent to the center system-level controller in an "on-demand" pattern, as shown in Fig. 5.

In the transmission abstraction based networking (TAN), the transmission process between PMUs and PDCs and between PDCs and the system-level controller is handled based on the resulting parameters: end-to-end communication delay and loss rate. For example, if the PMU at Bus 7 generates a data packet to be sent to the PDC at Bus 4, then the data packet is generated in packet generation module and then is sent to the PDC function by passing the TAN function. In this implementation, the values chosen for the delay and loss are determined based on the testing results from the real network simulator NS-3 [8]. The corresponding capabilities of the network devices and links are configurable in the NS-3 simulator. In fact, there are two essential parameters in the NS-3 setup that may affect the end-to-end transmission delay: the transmission delay of each link, and, the forwarding rate of each device. In this work, the forwarding rate of each device is set at 100 Mbps, which is a common value for devices in cyber-physical systems; and the transmission delay is set at 1 ms/200 km, which is also a practical value for the signal transmission. Then the link delays of different transmission lines with different length are computed accordingly.

In the real network interface based networking (RIN), the light-weight IP (lwIP) stack [33] is installed. Through the lwIP application programming interface, users can add customized networking functions. In this work, the IEC 61850 packet format and data encapsulation are implemented based on the existing echo server code to achieve the specific communication patterns of cyber-physical systems. Since the TAN module uses the resulting end-to-end parameters output by NS-3 and the measurement sampling is also performed using the system timer, the network simulation actually runs in real-time. By coordinating with the power system emulation, the real-time co-emulation can be achieved on the heterogeneous Jetson-FPGA platform.

V. REAL-TIME HARDWARE EMULATION RESULTS FOR COMMUNICATION-ENABLED GLOBAL CONTROL

Based on the implementation of the proposed hardware co-emulator, the global control schemes for the AC/DC test

power system is studied and emulated for the two cases: power overflow and DC fault protection. Since the existing co-simulators are not fully open-sourced and are implemented on disparate platforms, it is extremely difficult to evaluate the test power system using the existing co-simulators for comparison. However, the emulation results and the proposed ICT-enabled global control scheme are still reasonable due to the standard test power systems, commonly used power equipment EMT models, practical fault cases, and realistic control strategies.

A. CASE STUDY 1: POWER OVERFLOW PROTECTION

One major concern of the hybrid AC/DC grid integrated with renewable energies is to control the generated power by the offshore wind farms to precisely match the onshore consumption. When the power generated by the wind farms far exceeds the consumption of the AC side, the extra power can easily cause grid congestion, damage to the power equipment, and even blackouts. With the help of communication networks, the power flow at each bus can be monitored in real-time and the system-level control strategies can be generated to respond to the abnormal conditions quickly. In this case, the original power generated by each wind farm is 100MW, and total 200MW power flows to the Bus38 and Bus36 of the AC grid. At simulation time of 12 s, the power generated by two wind farms starts to increase to 900MW and 700MW respectively, which causes the power overflow on the AC side. After the PMU measurement on the Bus38 and Bus36 are collected by PDC2 and sent to the system-level controller located on DC Bus Bb-A1, the corresponding control commands that instruct the wind farms to decrease the generation are sent to the two wind farms; and the commands that change the reference values of power flows are sent to the converter Cb-C2 and Cb-D1.

This process was emulated on the heterogeneous hardware co-emulator, and the results with 55 ms and 250 ms response delay and without protection (NoP) are shown in Fig. 6. Note that the response delay is between the time when the PMU phasor magnitude exceeded the threshold and the time when the corresponding power equipment received the control command. The 55 ms delay was obtained by the real-time co-emulation, which included the reporting delay (30 Hz, about 33 ms), transmission delay (13 ms), control command generation delay, and the control taking effect delay. The 250 ms delay is chosen to be compared to the 55 ms delay to show the influence of longer response, which can be regarded as the situation where a communication link fault happens and a larger response latency is generated due to the latency of data packet re-routing. The waveforms of power and current phasor magnitude in Fig. 6 are all from the view of PMUs and DC-MUs. It can be observed from Fig. 6(a) that without the system-level control, the power overflow could cause huge increase of the power to Bus38 and Bus36.

For the case with protection, the PDC2 detected the current flow to Bus38 and Bus36, and the threshold of phasor magnitude (RMS value) is set at 1.2kA, which is 4 times of that under the normal condition. After the current phasor

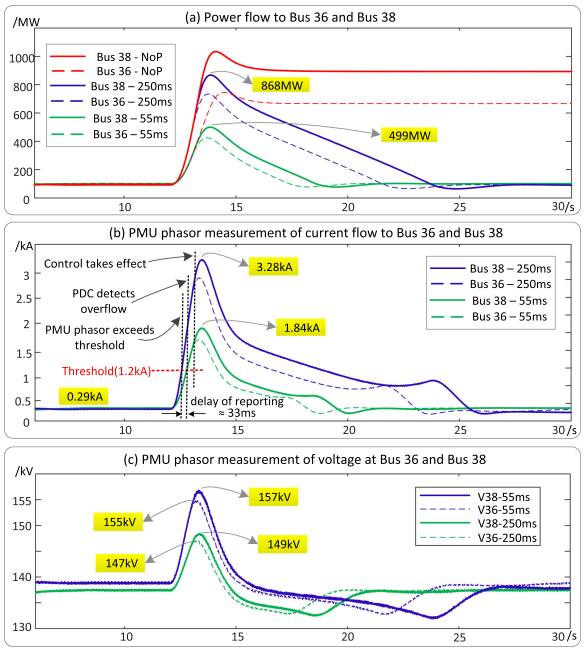

FIG. 6. Power overflow case: (a) comparison of the power flowing to Bus36 and Bus38 with 55 ms, 250 ms response delay and without protection; (b-c) comparison of phasor magnitude of the current flowing to Bus36 and Bus38 and bus voltages with 55 ms and 250 ms response delay.

magnitude of PMU38 at Bus38 exceeded the threshold, the PDC2 detected the abnormal condition after a reporting delay. In this case, since the 30 Hz reporting rate is used, the reporting delay is at most 33 ms. Then the PDC2 generated related data packets and sent to the controller via the communication network. The total communication delay included the delay from PMU38 to PDC2, the delay from PDC2 to controller, and from controller to windfarm and converter Cb-C2/Cb-D1, which was about 13 ms resulting from the NS-3 simulator. The system-level controller held a global view of the system topology and made a decision that shut down some turbines of the wind farms to reduce the generated power to 100MW and reduces the reference values of the converters. From Fig. 6(b)(c) it can be observed that when the power generated by the wind farms increased quickly, the impact of difference of response delay was amplified on the resulting current and voltage. Therefore, a small communication delay can benefit the global stability. Besides, it can be also seen that after the control command took effect, there was still a short increase of the current, because it took time to release the power stored in the capacitors of MMC submodules.

B. CASE STUDY 2: DC FAULT PROTECTION

The DC line ground fault is an important type of faults that can cause inreversible damages to the converters and should be protected against prior to the commissioning of HVDC grid. DC circuit breakers can be installed on the two ends of the DC lines, and they can isolate the fault when it is detected. The fast transient signal detection scheme [34] can be applied in this process. However, after a circuit breaker cuts the

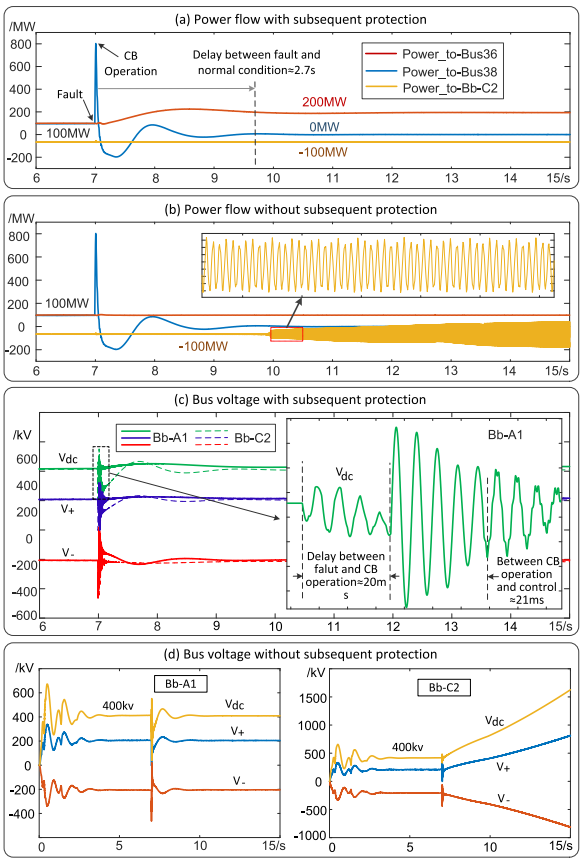

FIG. 7. DC fault protection case: (a-b) power flowing to different buses with and without subsequent protection; (c-d) positive, negative pole voltage and DC voltage of converter Bb-A1 and Bb-C2 with and without subsequent protection.

corresponding DC line, the original power flowing along the DC line requires to be redirected to reduce the impact on the other DC power equipment. In this case, the DC line ground fault occurred on the line connecting the bus Bb-A1 and Bb-C2; then the DC circuit breakers at the two ends turned off to cut the line down when detecting the fault (20 ms detection and action delay is assumed). After the line was isolated, the corresponding fault messages were sent to the controller, and the control command to change the reference power of the converters was generated to redirect the power flow. To demonstrate the effect of power flow redirection, the line between bus Bb-C2 and Bb-D1 was open at the beginning, and it was closed when the controller sent command to bus Bb-C2 and Bb-D1 after the DC fault.

The process was emulated on the hardware co-emulator and the results are presented in Fig. 7. It can be observed from Fig. 7(a)(b) that with system-level control, the original 100MW power flowing on the DC line between Bb-A1 and Bb-C2 was redirected to DC bus Bb-D1, and thus the power flowing to Bus36 increased to 200MW; although it took about 2.7 s to return to the normal condition. Without the system-level control, the extra power could cause instability of the converter Cb-C2. From the DC voltages shown in Fig. 7(c), it can be seen that after the CB operation, there is a 21 ms of transmission and control computation delay before the control command took effect. The power redirection did not cause a big perturbation to the V_{dc}, which indicates the global control strategy is reasonable to reduce the system instability compared to purely cutting off the line without subsequent protection operations.

VI. CONCLUSION

To study the ICT-enabled global control for AC/DC grids integrated with renewable energy, the co-simulation platform is required to evaluate the interaction between the power system and communication network. In this work, a heterogeneous hardware real-time co-emulator is proposed and built on the multiple Jetson-FPGA platform. The EMT-based power system simulation is executed on FPGA boards to provide a continuous measurement to the phasor measurement unit (PMU) and DC merging unit (DC-MU); the MMC converter control functions and communication modules run on the Jetson embedded platform to perform fast and flexible computational tasks; and the interaction between the two domains are simulated through the read and write operations via the PCIe connector. The multi-board scheme is applied to extend the computational capabilities and resources to accommodate large-scale systems. The hybrid AC/DC grid with wind farms is emulated on the FPGA-Jeston based co-emulator, and the ICT-enabled global control schemes are investigated for the two case studies: power overflow and DC fault. The proposed heterogeneous co-emulator can be applied in fast emulation of practical large-scale cyber-physical power systems, and the investigated global control schemes can be applied to improve the system stability and controllability. The co-emulation of micro-grids and future distribution systems will be studied in future work.

APPENDIX A
CIRCUIT PARAMETERS

Parameters of the test system: AC base values: 100MVA, 230 kV, 60 Hz; Synchronous generator: 22 kV; Generator connected transformer: 22 kV/230 kV; AC transformers in 39-bus system: 230 kV/230 kV, leakage inductance 0.2pu, copper loss 0.004pu; AC transformers for AC and DC system connection: 230 kV/500 kV; DC voltage: $\pm$200 kV; MMC: 51-level, $V_{dc} = 400$kV, $N = 50$; DC-DC converter: 400 kV/400 kV; Windfarm generated power: 100MW; Transmission lines: the length of lines in the IEEE 39-bus system and the length of DC lines in CIGRÉ DC grid is the same as [24].

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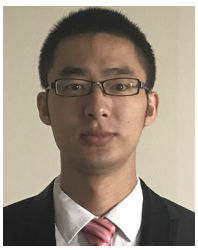

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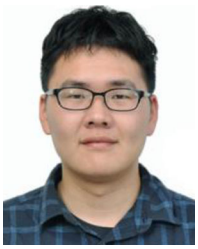

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