Design of an Integrated mm-wave Area and Energy-Efficient Analog (RF) Beamformer

by

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Abstract

The rising demand for high-data-rate services has led to increased congestion in traditional low-GHz RF wireless communication channels. To alleviate this bandwidth shortage, higher-frequency bands like millimeter-wave and sub-THz frequencies are used. However, these higher-frequency signals suffer from greater path losses, limiting their communication range. Directional and phased array antennas have emerged as solutions to this challenge, enabling the focused transmission or reception of signals in specific directions to extend the communication range. Phased array systems, utilizing techniques known as beamforming, adjust phase shifts between antenna elements to create directional beams. Their advantages include faster response times, greater flexibility, and smaller form factors compared to mechanical alternatives, making them popular in various modern wireless applications. Moreover, there is a growing demand for energy-efficient and compact phased array systems to make them more suitable for use in applications in which battery life and device sizes are the main concerns, ranging from handheld 5G/6G devices to UAV and satellite communication equipment. This study proposes innovative circuit solutions to meet this demand, addressing RF analog beamforming and exploring methods to improve power efficiency and reduce chip size.

In loving memory of my father

To my mother, Azam, whose unwavering encouragement has ignited my passion for learning

To my two sons, Soroush and Sepehr, whose understanding and patience during this pursuit of knowledge meant spending less time together, yet their presence has been my source of strength.

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Abbreviations

$\Delta\theta_{max@f_l}$ maximum achievable phase shift at the lowest frequency.

Γ_{in} Input Reflection Coefficient.

k_i Scaling Coefficient.

k_{max} Maximum Scaling Coefficient.

$|\Gamma_{in,max}|$ maximum absolute value of the Input Reflection Coefficient.

$|\Gamma_{in_{max}}|$ maximum magnitude of the input reflection coefficient.

ADC Analog-to-Digital Converter.

ATL Artificial Transmission Line.

CG Common Gate.

CMOS Complementary Metal–Oxide–Semiconductor.

DA Distributed Amplifier.

DAC Digital-to-Analog Converter.

DSP Digital Signal Processor.

EIRP Equivalent Isotropic Radiated Power.

FOM Figure of Merit.

GSG Ground-Signal-Ground.

IDC Insulation Displacement Connector.

IL Insertion Loss.

LNA Low-Noise Amplifier.

LO Local Oscillator.

LWA leaky wave antenna.

PCB Printed Circuit Board.

Pseudo-DA Pseudo-Distributed Amplifier.

PVT Process, Voltage, and Temperature.

RFC Radio Frequency Choke.

RL Return Loss.

RTPS Reflection Type Phase Shifter.

SNR Signal-to-Noise Ratio.

SOLT Short/Open/Load/Through.

STPS Switched Type Phase Shifter.

Tapered TTL Tapered Tunable Transmission Line.

TTL Tunable Transmission Line.

TTLPS Tunable Transmission Line Phase Shifter.

Tunable-ATL Tunable Artificial Transmission Line.

VGA Variable Gain Amplifier.

VMB Vector Modulator Based.

Chapter 1

Introduction

1.1 Motivation

Since the demand for higher data rate services continues to increase, the available bandwidth in traditional low-GHz RF wireless communications becomes increasingly congested. Developing new wireless technologies that use higher frequency bands, such as millimeter-wave and sub-THz frequencies, is considered as one of the most promising solutions to address the bandwidth shortage [1–3]. However, millimetre-wave signals experience increased free space and atmospheric losses when compared to lower-frequency signals. Moreover, the propagation of high-frequency radio waves is often hindered by higher absorption rates when encountering obstacles such as buildings, trees, and raindrops. Consequently, these factors collectively contribute to a reduction in the overall range of communication [4]. To overcome these challenges, directional and phased array antennas are typically used to focus a transmitted or received signal in a particular direction or towards a specific receiver to improve the Signal-to-Noise Ratio (SNR) and increase the system transmission range [5]. Utilizing either of these methods increases the capability for directional wireless communication, as opposed to the traditional omnidirectional communication that is common in the lower RF frequency range. While the omnidirectional approach offers alignment-free communication, directional communication presents numerous advantages. It is more energy-efficient due to targeted delivery, facilitates multiple simultaneous communications at the same frequency, reduces susceptibility to multipath fading, and avoids interference with other communication channels [6].

Phased array systems are essentially arrays of multiple antenna elements. They

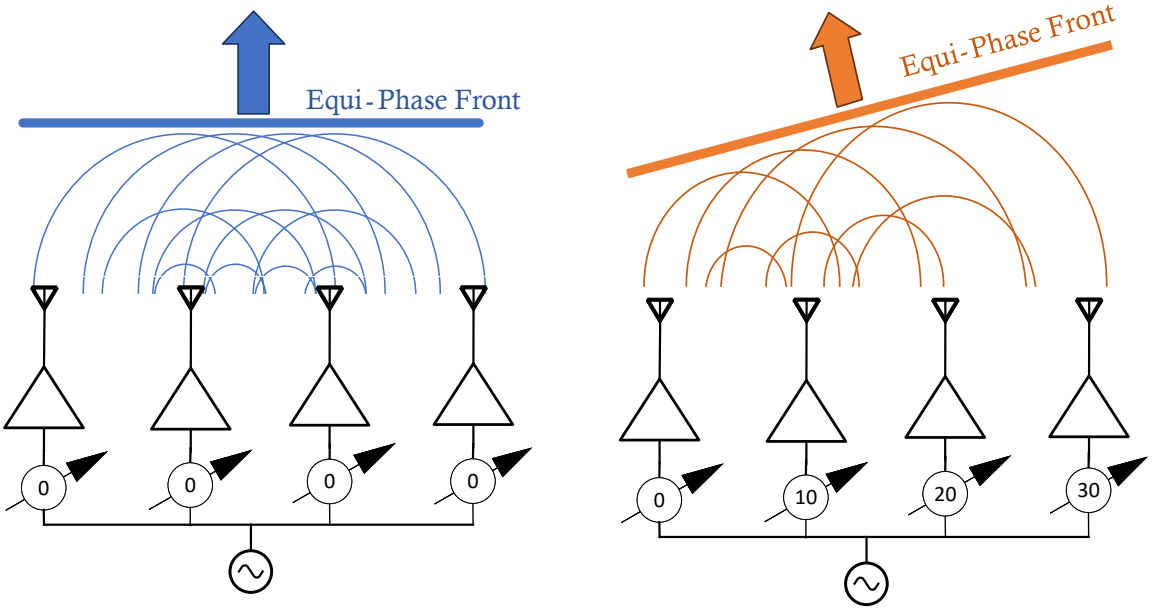


Figure 1.1: Phase array concept.

use a variety of techniques to control the amplitudes and phase shifts between the element signals in the array to create a constructive interference pattern that results in a directional beam. Moreover, these techniques, which are generally called beamforming, provide the ability to steer the beam in a specific direction without physically moving the antenna by independently adjusting the phase and amplitude of each array element's signal [7]. Fig. 1.1 provides an intuitive representation, demonstrating how the manipulation of the phase for each antenna element within an array enables the dynamic adjustment of the equi-phase front of the radiated signal. This visual insight underscores the capability of phased arrays to alter the direction of signal radiation by controlling individual antenna phases. It is worth noting that phased arrays find utility in both transmitters and receivers, showcasing their versatility in diverse applications across communication systems.

In a phased array receiver, in addition to the mentioned benefits, for fixed antenna sizes, the SNR consistently improves within an array due to the presence of uncorrelated noise in parallel independent receivers. It is crucial to note that the advantage of noise reduction is contingent upon the independence of the noise sources. Therefore, the extent of the SNR improvement is influenced by the specific architecture of the phased array (beamforming). As illustrated in Fig. 1.2, the array manipulates

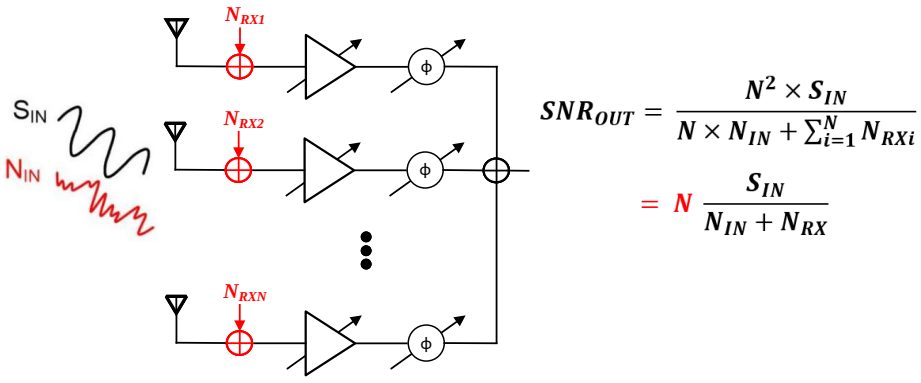


Figure 1.2: SNR improvement in a phased array system.

the phase of input signals to achieve constructive addition at the output port. Importantly, since the input noise in each branch of the array (N_{RX_i}) is statistically independent of others, constructive addition does not apply to these noise sources. Consequently, the SNR undergoes improvement by a factor of n, where n represents the number of elements in the array.

Due to the faster response time, greater flexibility, and smaller size of the phased array antennas in comparison to mechanical directional counterparts [8], they have become increasingly popular in a wide range of growing wireless applications. For example, phased array systems are widely used in 5G/6G, satellite communication wireless transceivers, automotive radars, and medical imaging systems [9]. Specifically, as there is a widespread demand for using high-rate millimeter wireless communication in consumer electronic devices, such as smartphones and tablets, it is desirable to further reduce the power consumption and size of the beamformers to arrive at an energy-efficient, low-cost phased array solution.

This study is focused on proposing new circuit ideas to reduce the area and power consumption of integrated beamformers. In this chapter, a brief description of beamforming and the possible realization of the beamformers in analog, digital, and hybrid domains is provided. The details of the RF analog beamforming, a widely used method for on-chip realization, are further elaborated and its advantages and disadvantages are discussed. The possible solutions and previous work on improving the power consumption and reducing the chip area of the RF analog beamformer are also investigated.

1.2 Beamforming Fundamentals

Beamforming, or Spatial Filtering, is a technique that focuses or directs a transmitted or received signal in a specific direction [7]. This technique is essential in many wireless communication and radar systems. In modern 5G/6G wireless communication systems, increasing demand for higher data rates requires the utilization of frequency bands in the millimeter wave region and above. Due to the high path and penetration losses at millimeter wavelengths, beamforming is needed to overcome path losses and establish robust communication links by concentrating the radiation energy in the desired direction [10]. In radar systems, beamforming is needed to track high-speed targets with high angular resolution [11]. Phased array antenna systems are often used for directional transmission and reception of directional EM beams by progressively setting the phase of signals for elements of the antenna array.

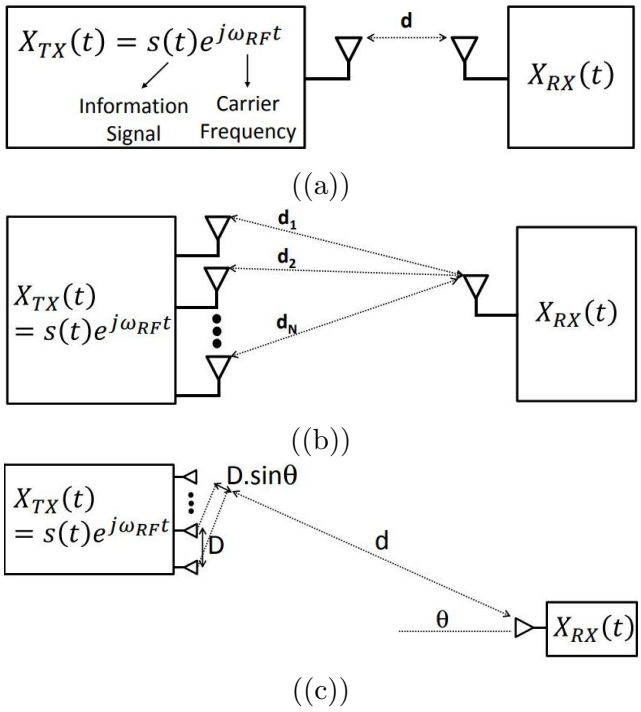


Figure 1.3: (a) Single transmitter and receiver. (b) Generalized N transmitter to one receiver (c) Linear phased array with N elements.

In the context of a wireless transmitter system, the modulated signal at the output (as illustrated in Fig. 1.3(a)) is generally represented as

$$X_{TX}(t) = S(t)e^{j\omega_{RF}t}, \tag{1.1}$$

where $S(t)$ denotes the information signal and $e^{j\omega_{RF}t}$ represents the carrier frequency. Upon transmission through an omnidirectional antenna, the received signal at a receiver positioned at a distance d is given by

$$\begin{aligned} X_{RX}(t) &= \frac{k}{d^2} X_{TX}(t - \frac{d}{c}) \\ &= \frac{k}{d^2} S(t - \frac{d}{c}) e^{j\omega_{RF}(t - \frac{d}{c})} \\ &= \frac{k}{d^2} e^{-j2\pi \frac{d}{\lambda}} S(t - \frac{d}{c}) e^{j\omega_{RF}t}, \end{aligned} \tag{1.2}$$

where k is a constant, c is the wave propagation velocity, and λ denotes the wavelength defined as

$$\lambda = \frac{c}{\omega_{RF}}. \tag{1.3}$$

When considering N transmitters emitting the same modulated signal X_{TX}, the received signal can be calculated using

$$X_{RX}(t) = \sum_{i=1}^{N} \frac{k}{d_i^2} e^{-j2\pi \frac{d_i}{\lambda}} S(t - \frac{d_i}{c}) e^{j\omega_{RF}t}. \tag{1.4}$$

Assuming negligible variations in d_i in the d_i/c term, and with the receiver located far from the transmitter, this expression can be approximated as

$$X_{RX}(t) \approx \frac{k}{d^2} \sum_{i=1}^{N} e^{-j2\pi \frac{d_i}{\lambda}} S(t - \frac{d}{c}) e^{j\omega_{RF}t}. \tag{1.5}$$

In a linear array system, as depicted in Fig. 1.3(c), the antenna elements are equally spaced at a distance D between each consecutive elements. In this case, d_i can be replaced by $d_i = d + (i-1)Dsin(\theta)$. As a result, (1.5) is changed to

$$X_{RX}(t) \approx \frac{k}{d^2} e^{-j2\pi \frac{d}{\lambda}} \sum_{i=1}^{N} e^{-j2\pi(i-1)\frac{D}{\lambda} sin(\theta)} S(t - \frac{d}{c}) e^{j\omega_{RF}t}. \tag{1.6}$$

The part highlighted in red is known as the Array Factor. This factor plays a significant role in influencing the pattern and directs the pattern toward the desired point.

Increasing the number of antenna elements results in a more pronounced effect on the pattern, notably achieving a narrower beamwidth. Fig. 1.4(a) to Fig. 1.4(d) visually illustrate the array factor for a linear array configuration with antenna elements spaced at $\lambda/2$, showcasing the impact of varying the number of elements (2, 4, 16, and 64) on the array factor.

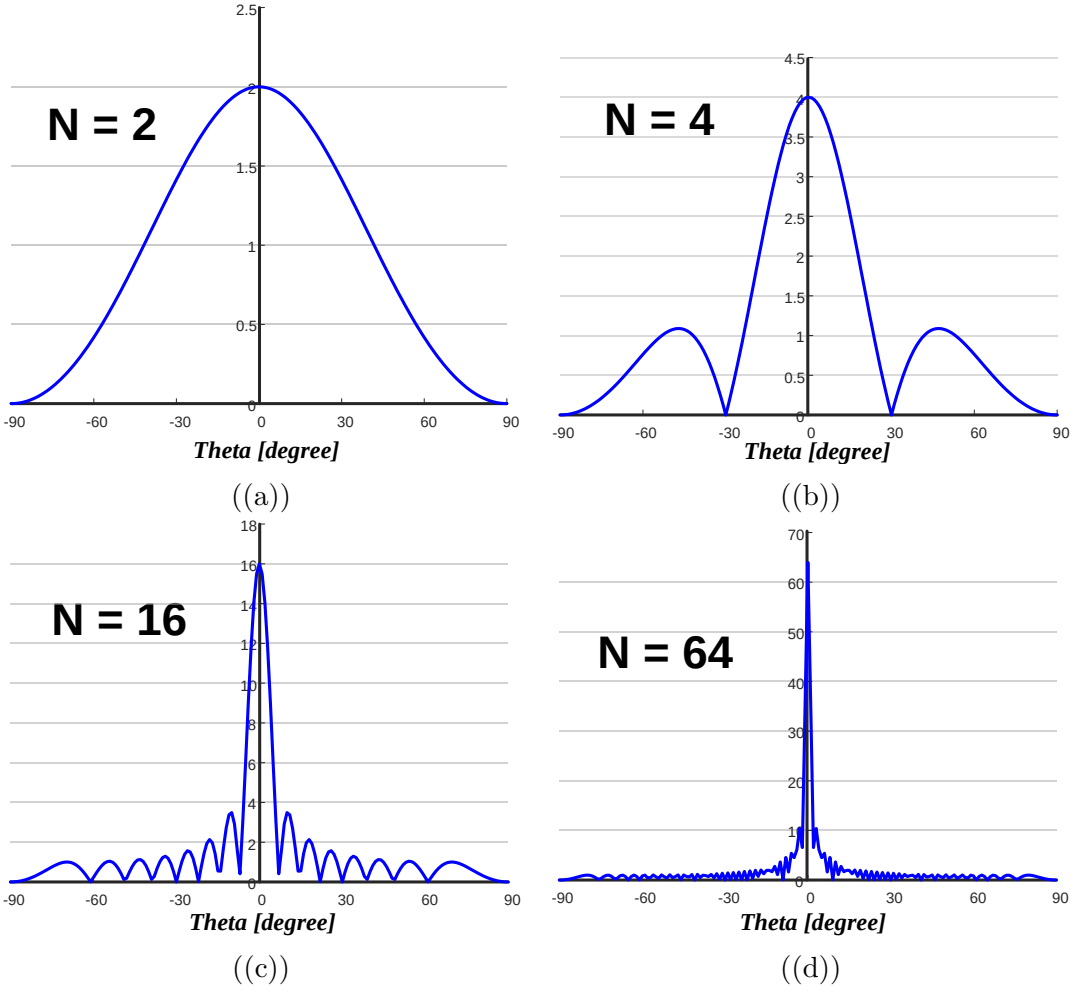


Figure 1.4: Array Factor for a Linear Array when $D = \dfrac{\lambda}{2}$ and (a) $N = 2$ (b) $N = 4$ (c) $N = 16$ (d) $N = 64$

As previously noted, the primary distinction between a phased array system and an antenna array lies in the independent manipulation of phase and amplitude in each channel within the former (refer to Fig. 1.1). The ability to control the phase of signals in individual antenna elements facilitates beam steering. Given that the phase shifter in the i-th element introduces an additional phase shift of $\phi_i = (i-1)\phi_0$, the

array factor in (1.6) can be reformulated as

$$AF = \sum_{i=1}^{N} e^{-j2\pi(i-1)(\frac{D}{\lambda}sin(\theta)+\frac{\phi_0}{2\pi})}. \tag{1.7}$$

By varying the value of ϕ_0, it becomes possible to alter the direction in which the phased array is oriented. Figs. 1.5(a) to 1.5(d), visually represent the changes in the main beam direction of a phased array consisting of 16 antenna elements, where the spacing between the antennas is $\lambda/2$. These figures provide a depiction of how adjusting the parameter ϕ_0 influences the directional characteristics of the main beam in the phased array configuration.

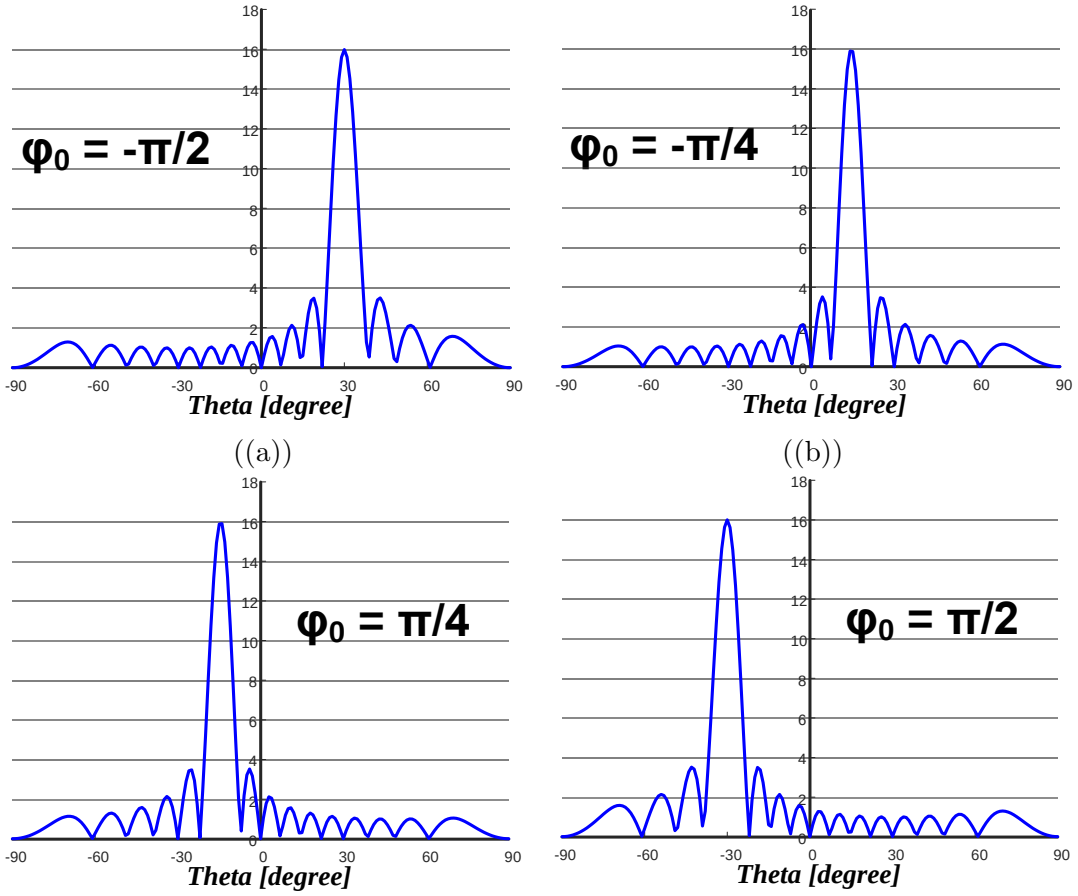


Figure 1.5: Array Factor for a Phased Array when $N = 16$, $D = \frac{\lambda}{2}$, and (a) $\Phi_0 = -\frac{\pi}{2}$ (b) $\Phi_0 = -\frac{\pi}{4}$ (c) $\Phi_0 = \frac{\pi}{4}$ (d) $\Phi_0 = \frac{\pi}{2}$.

1.3 Beamforming Techniques

Beamforming can be performed in any of the digital, analog, or hybrid digital-analog domains. The choice of domain depends on the specific requirements and constraints of the application. Digital beamforming is favored in situations demanding precise control, adaptability, and the ability to implement sophisticated algorithms [12]. Analog beamforming, on the other hand, is preferred in scenarios where simplicity, low power consumption, and real-time processing are essential. Hybrid digital-analog beamforming offers a middle ground, allowing for a tailored approach to meet the specific needs of diverse applications, making beamforming a versatile and powerful technology across a spectrum of domains. The block diagrams and a brief description of each method will be further discussed in this section.

1.3.1 Digital Beamforming

In a digital beamformer, as shown in Fig. 1.6, the received signals from each antenna are digitized and processed digitally. Therefore, the required number of high-speed Analog-to-Digital Converters (ADCs) and RF chains, including Frequency Converter (Mixer) and Low-Noise Amplifier (LNA), is equal to the number of array's elements demanding high power consumption to perform beamforming. Requiring a synchronized Local Oscillator (LO) distribution for frequency conversion in each branch adds to their implementation complexity.

The digital beamformer employs digital signal processing (DSP) to manipulate the signals in the digital domain. This enables real-time adjustments and precise control over the beam, allowing for enhanced performance in various applications. Consequently, this type of beamformer offers higher angular resolution, lower side lobe magnitudes, increased radiated power, and a simpler calibration process [9]. As in digital beamformers, each antenna element requires a dedicated high-speed mixed-signal data converter and a high-performance RF frequency converter, the high power consumption and the cost associated with the implementation of such a complex system prevent purely digital front ends from being utilized in many applications with power/cost restrictions. As another limitation of this technique, it should be noted that using digital signal processing in digital beamformers introduces some

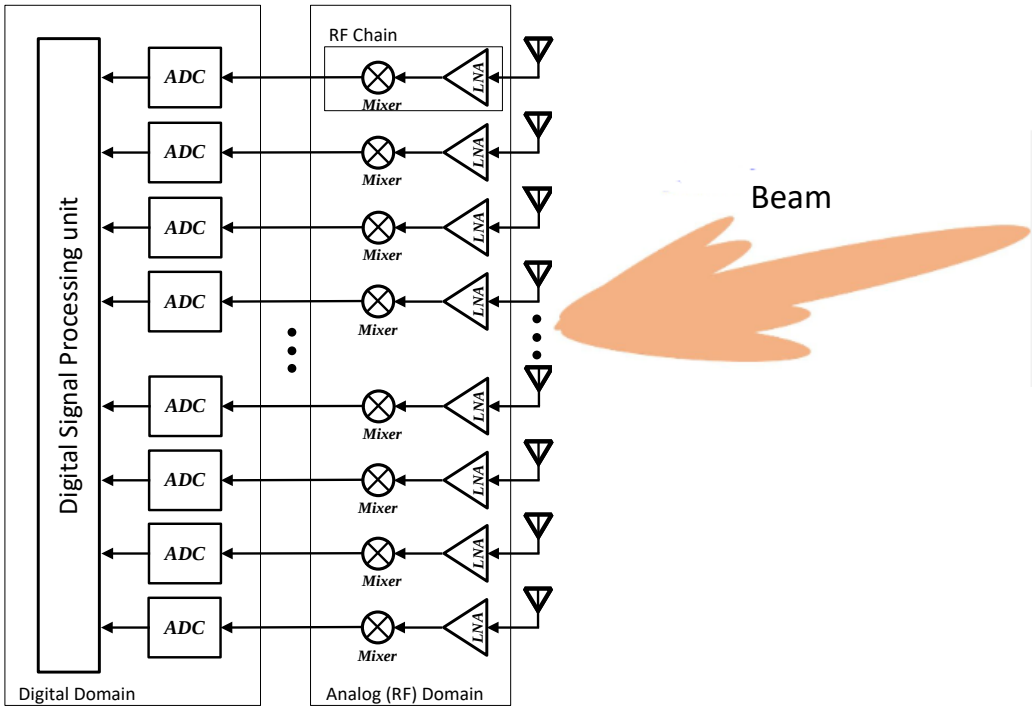


Figure 1.6: Block diagram of a Digital Beamformer (Receiving mode).

delay, which can be a critical factor in applications where real-time responsiveness is crucial.

1.3.2 Analog Beamforming

The analog beamformers perform the task using analog building blocks, such as phase shifters and variable gain amplifiers, by combining the phase-shifted transmitted/received signals in the analog domain (see Fig. 1.7). Since ADC/Digital-to-Analog Converters (DACs) or Digital Signal Processors (DSPs) are not required in the beamforming process, analog beamformers consume significantly less power and can be constructed at lower cost in a smaller form factor in comparison to their digital counterparts [5].

Moreover, as only one frequency mixer is required in an analog beamformer, eliminating the LO distribution circuitry further simplifies the scheme. Generally, analog beamforming systems are often simpler in design and implementation compared to digital systems, making them more straightforward to configure and maintain. In addition, they operate in real-time without the latency introduced by digital signal

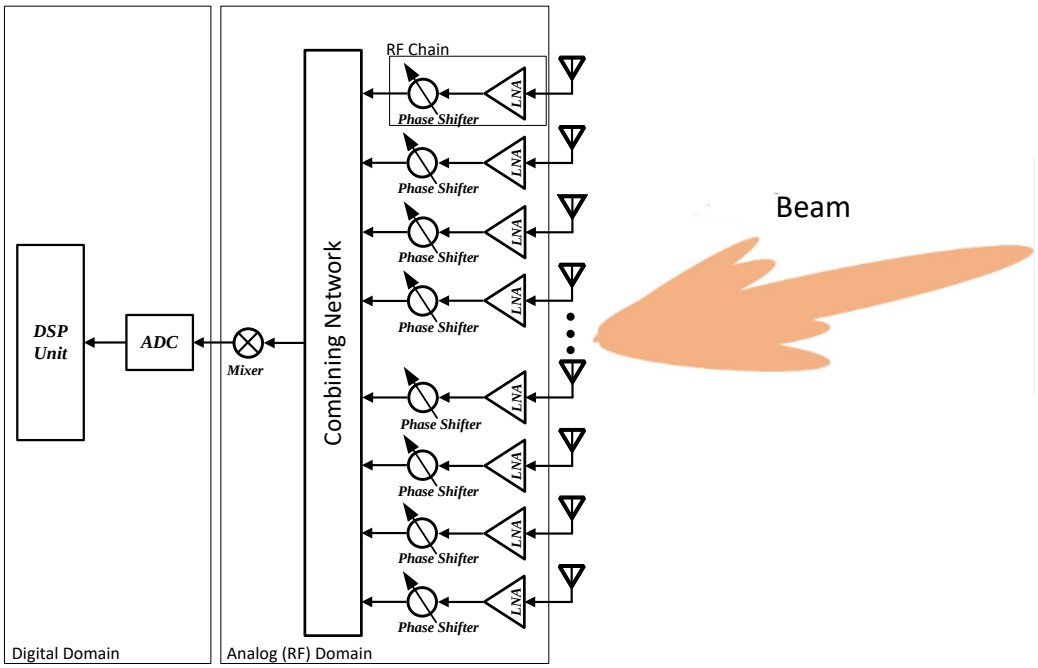


Figure 1.7: Block diagram of an Analog (RF) Beamformer (Receiving mode).

processing, making it suitable for applications where immediate response is critical. However, this type of beamformer lacks the adaptability of digital systems. Furthermore, as adjustments to the beam characteristics are performed in the analog domain, this method has less accuracy and provides lower angle resolution.

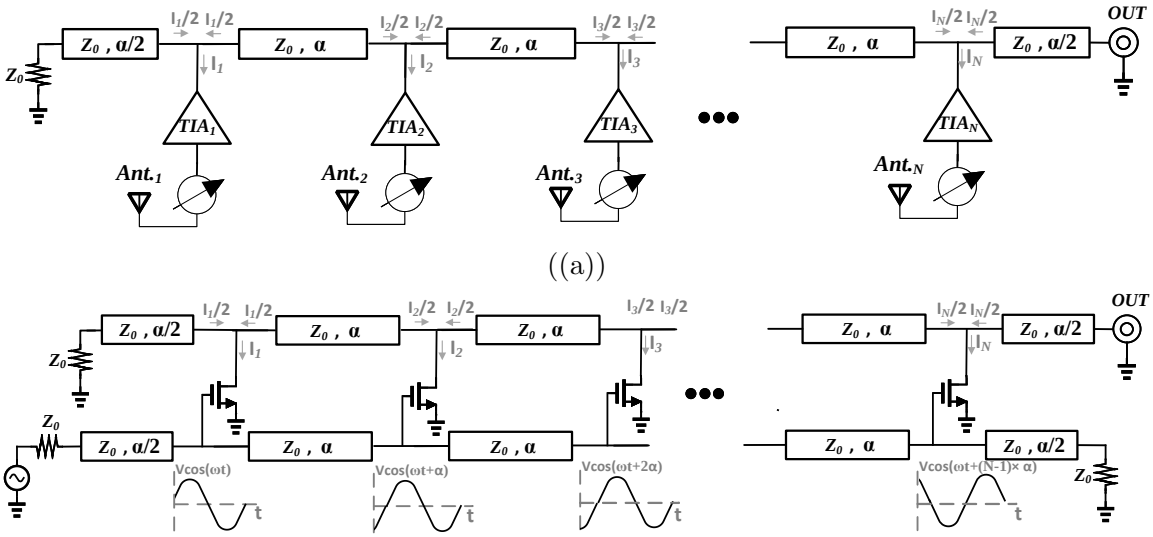


Figure 1.8: (a) Analog beamformer with series-fed combining network, (b) Classical Distributed Amplifier (DA)

The methodology illustrated in Fig. 1.7 is commonly referred to as a parallel-fed combining network. However, an alternative approach, known as series-fed combining, is depicted in Fig. 1.8(a). In this configuration, if the phase difference between the output currents of consecutive Trans Impedance Amplifiers (TIAs) matches the electrical length of the transmission lines connecting them, then half of each branch's current is constructively summed at the output port. Nevertheless, the other halves are wasted in the terminated port.

The series-fed combining network in an analog beamformer functions similarly to a conventional Distributed Amplifier (DA), as shown in Fig. 1.8(b). In a DA, the input and output transmission lines are designed to absorb the input and output parasitic capacitance of TIAs, enabling a wide operational bandwidth [13]. Consequently, in a DA, the sacrifice of half of the currents in the terminated port is accepted as the cost for achieving ultra-wideband performance.

However, in a phased array with a series-fed combiner, the absence of an input transmission line can lead to a significant restriction in the operational bandwidth due to the parasitic input capacitance of the TIAs. This limitation underscores the importance of considering the specific design context and trade-offs when choosing between the parallel-fed and series-fed combining networks for optimal performance in specific practical applications.

Despite its apparent inefficiency, the series-fed beamforming method has distinct advantages that render it a viable consideration in certain scenarios. First, it has been demonstrated that series-fed beamformers can generate multiple simultaneous beams. This capability is noteworthy as it enhances the area efficiency of the beamformer [14] Second, in cases where the electrical length of the transmission lines within the series combining network is tunable, as depicted in Fig. 1.9, it becomes possible to eliminate the need for a phase shifter in each branch. This specific implementation contributes to making the beamformer more area-efficient, a topic that will be explored in greater detail in Chapter 4.

1.3.3 Hybrid Analog/Digital Beamforming

Hybrid Analog/Digital beamforming is a cutting-edge signal processing approach that amalgamates the advantages of both analog and digital beamforming techniques. This

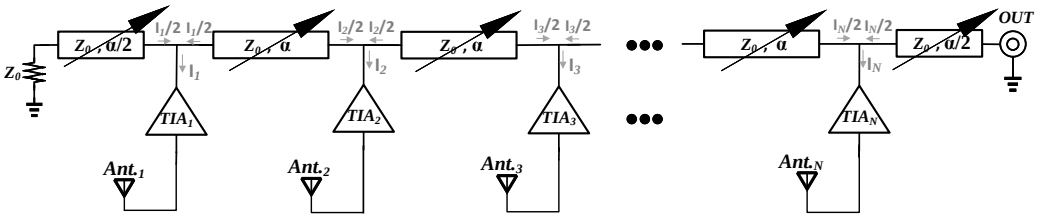


Figure 1.9: Block diagram of an Analog (RF) Beamformer (Receiving mode).

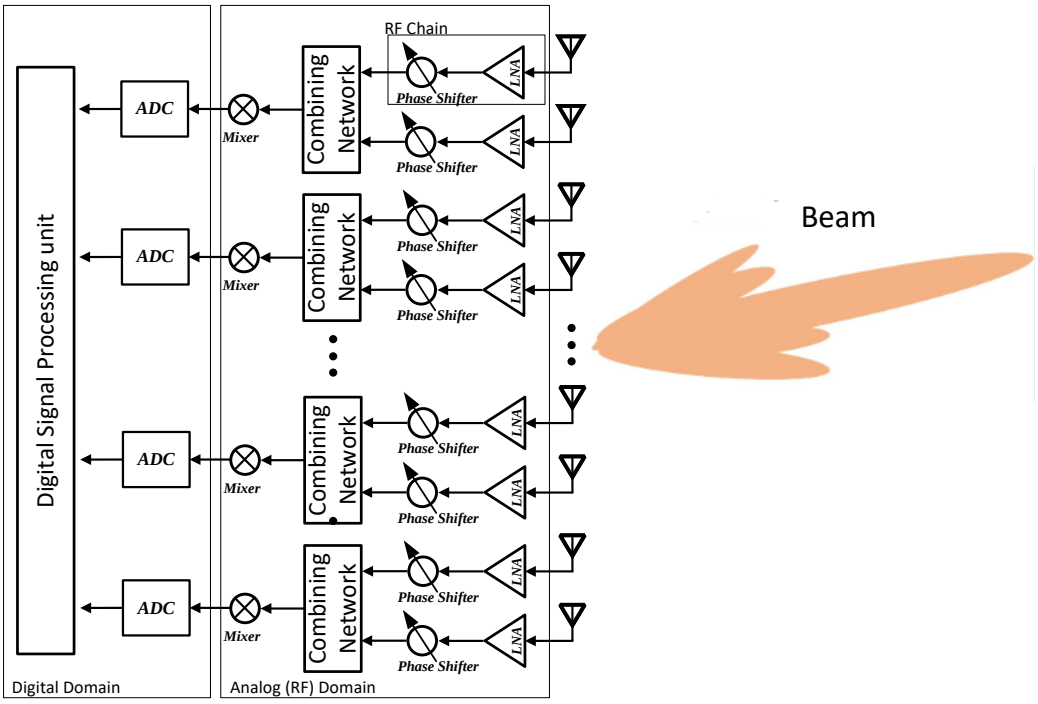


Figure 1.10: Block diagram of a Hybrid Beamformer (Receiving mode).

technique has gained prominence in modern communication and radar systems for its ability to strike a balance between the efficiency of analog beamforming and the adaptability of digital beamforming [9]. Hybrid beamformers perform beamforming for a subset of phased array elements in the analog domain while processing the transmitted/received signals of each subset in the digital domain (See Fig. 1.10). In fact, each subset in a hybrid beamformer acts as an analog (RF) beamformer but with a smaller number of antenna elements. This means that for the digital beamformer part, a simpler LO distribution network is required and the number of required ADCs (DACs in transmitting mode) is significantly reduced. Consequently, by reducing the number of required power-hungry elements, hybrid beamforming provides a compromise solution between analog and digital beamforming [15]. Hybrid

Table 1.1: Comparing Beamforming Methods

Parameters	RF beamforming	Hybrid beamforming	Digital beamforming
Main Required Blocks	Attenuator/Phase Shifter*	ADC/DAC**+ Attenuator/Phase Shifter** + Simple LODN	ADC/DAC * + Complex LODN***
Flexibility	Low	Moderate/High	High
Complexity	Low	Moderate	High
Power Consumption	Low	Moderate	High
Cost	Low	Moderate/Low	High

* per antenna element
** fewer than the number of the antenna elements
*** Local Oscillator Distribution Network (LODN)

beamformers possess several advantages over the other methods. First, the digital processing component allows for fine adjustments, leading to enhanced signal quality, reduced interference, and improved overall system performance. In addition, they exhibit lower latency compared to fully digital systems, making them suitable for applications where real-time responsiveness is essential. Finally, the hybrid nature of the architecture provides flexibility in design, allowing for customization based on specific application requirements and constraints.

1.3.4 Comparison of Beamforming Methods

Table 1.1 presents a comparative analysis of three beamforming methods. The contents of the table suggest that the selection of the appropriate method is highly contingent upon the specific requirements of the desired application. In cellular network applications, at the base station side, usually high-performance equipment is required, and simultaneously high power consumption and large-size devices can be tolerated. Therefore, wherever phased array systems are required, digital beamformers would likely be the proper choice. On the other side, in the end-user equipment of the cellular networks, which are usually implemented on-chip, reducing the power consumption and the size of the handheld devices are crucial. Consequently, in such applications, the phased array system must use analog or hybrid beamformers to trade off some performance to get more area and energy-efficient design. Given these considerations and acknowledging the crucial significance of analog beamformers in the modern millimeter-wave transceivers, the subsequent chapter is devoted to a comprehensive examination of the architectures, building blocks, and challenges inherent in this category of beamforming technique.

1.4 Objectives

The main objective of this study is to develop energy-efficient and compact beamformers to design phased array systems that can be implemented in handheld devices or used in applications with strict limitations on size and power consumption. To address this goal, two main subjects are investigated in this research. Since phase shifters are the key component of analog (RF) beamformers, the design of an area-efficient phase shifter is determined as the first objective of this study. It is well-known that TTL phase shifters have useful capabilities such as having a wide operational frequency band, consuming no power, and providing continuous phase shift. However, at the same time, they are not very popular in on-chip design because of their large size and their excess insertion loss. Accordingly, proposing an area-efficient TTL phase shifters, to make them more appropriate for on-chip realization, is an interesting research subject. Therefore, chapter 3 of this study is dedicated to the design of a new Tapered TTL phase shifter which reduces the consuming chip area and improves the insertion loss performance. To verify the efficacy of the proposed phase shifter design, a wideband (Ku/K/Ka band) Tapered TTL phase shifter is designed, fabricated, and tested with its measurement results presented in this chapter.

The other objective of this research is to propose a new distributed beamformer that combines all functions of an analog (RF) beamformer in a single circuit thereby reducing the overall power consumption, occupied chip area, and fabrication costs. In Chapter 4, the design process for optimizing the beamformer gain, noise performance, and beam steering capability of the proposed design is presented and supported by mathematical analysis. Moreover, to demonstrate the effectiveness of the proposed beamforming approach, the fabrication process and measurement results of a four-element K-band beamformer of this type are discussed in this chapter

Chapter 2

Analog (RF) Beamformers Literature Review

2.1 Introduction

Analog (RF) beamforming is the simplest beamforming architecture. This approach forms the foundation of beamforming techniques, leveraging RF phase shifters to dynamically control the direction and characteristics of transmitted or received electromagnetic signals. As shown in Fig. 1.7, this type of beamformer relies on a single ADC (or DAC in transmitting mode). This gives this architecture low complexity and low power consumption, which makes it particularly suitable for scenarios where resource efficiency is critical.

The key to the success of this architecture lies in the precision and resolution of RF phase shifters. These components play a pivotal role in dynamically adjusting the phase of the signals, allowing for the steering of beams in specific directions. As the resolution of phase shifters increases, so does the beamforming performance, enabling finer control and optimization of the transmitted or received beams.

It should be noted using only analog (RF) or hybrid beamformers may not adequately address the increasing demand for newer wireless equipment with longer battery life and smaller form factors. Consequently, extensive research and development efforts are currently being undertaken to further reduce the cost and power consumption of these beamformers while maintaining acceptable performance [15]. Many studies have been conducted to find new approaches to design and implement more energy-efficient and less area-consuming phase shifters as the key building blocks of

analog (RF) beamformers. Nonetheless, several other researchers focused on proposing innovative and more integrated designs and schemes for the entire beamformer rather than using the conventional architecture shown in Fig. 1.7. In this chapter, a comprehensive review of both kinds of studies is performed.

2.2 Recent Advances in Implementing RF Phase Shifters

In analog or hybrid beamformers, the phase shifters are often required to produce the desired phase shift range and resolution with low return and insertion losses while being implemented at the lowest possible cost and with the minimum possible power consumption as the number of required phase shifters scales linearly with the number of antenna elements in a phased-array antenna system. The phase shifters can be constructed using several different techniques including vector modulation circuits, switched delay lines, tunable reflective loads, and loaded transmission lines, where the phase shifts are created using passive or active circuit components or both.

2.2.1 Vector Modulator Based (VMB) Phase Shifters

The vector modulation method creates a phase-shifted signal by summing two orthogonal current vectors (I and Q) with different weights. The typical block diagram of a VMB phase shifter is shown in Fig. 2.1. As can be seen, a VMB phase shifter consists of three main parts: a 90-degree hybrid coupler, a Variable Gain Amplifier (VGA) in the I and Q branches, and an Analog Adder. Given that VGAs, integral components of the VMB phase shifter, must consume DC power, they are classified as active phase shifters. Diverging from passive phase shifters, active phase shifters introduce gain rather than loss. This unique characteristic eliminates the need for additional amplifiers in transceivers utilizing passive phase shifters to compensate for signal losses. Consequently, the elimination of this amplification requirement enhances the overall power efficiency of transceivers equipped with active phase shifters. Despite their advantages, active phase shifters come with trade-offs. Their gain-oriented nature implies a lower noise figure compared to passive alternatives. However, it is essential to note that they simultaneously exhibit increased nonlinearity. As a result, active

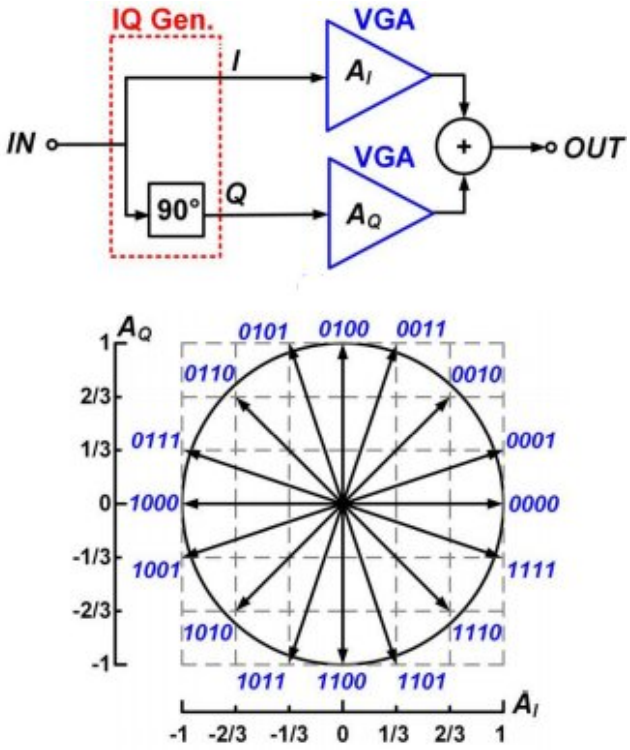


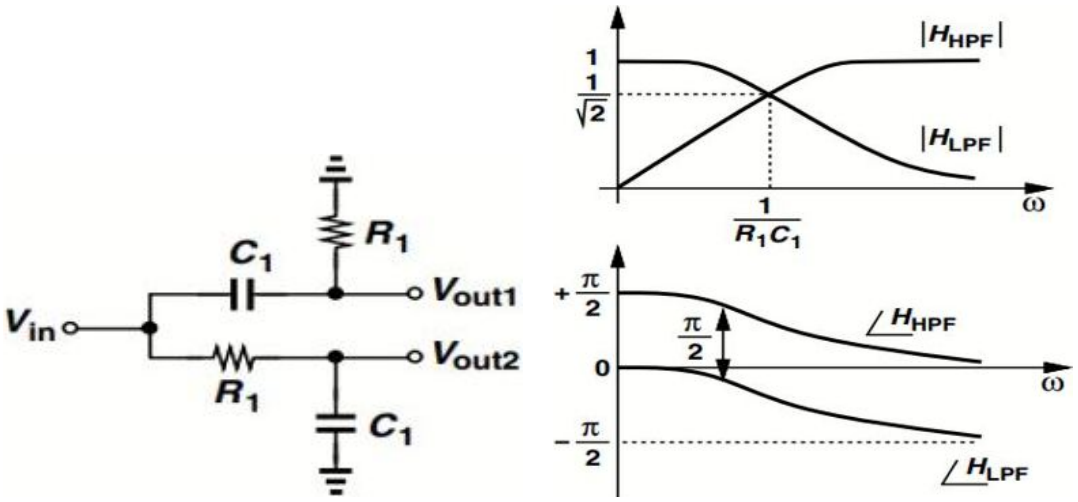
Figure 2.1: The Block diagram of a typical VMB phase shifter [16]

phase shifters find greater utility in applications that prioritize sensitivity to noise, such as receivers, as opposed to those necessitating a higher degree of linearity, such as transmitters. In order to enhance the performance of this type of phase shifters, various studies have been conducted to explore avenues for improvement in each constituent building block of VMB phase shifters. The forthcoming sections will delve into the detailed elaboration of select studies addressing these enhancements.

Quadrature (90-degree) Hybrid Coupler

For accurate phase shifting, it is essential that the signals in the I and Q branches have an exact 90 degree phase shift and equal amplitudes. Utilizing an RC-CR circuit is the most well-known method to provide suitable I and Q signals. This method is based on the phase lead and phase lag, which are applied by CR and RC network as demonstrated in Fig. 2.2.

As observed, the quadrature hybrid under consideration produces a satisfactory phase difference across its operational bandwidth. However, a noteworthy deficiency is discerned in its amplitude difference, particularly when deviating slightly from



((a)) ((b))

Figure 2.2: (a) schematic and (b) phase and amplitude relation between two outputs of an RC-CR network [17]

the center frequency. As previously elucidated, the VMB phase shifter relies on the weighted amplification of the In-phase (I) and Quadrature-phase (Q) signals. Consequently, the utilization of this specific quadrature hybrid is notably limited within the realm of VMB phase shifters, primarily due to its constrained amplitude balance performance.

For the purpose of arriving at a wideband 90-degree hybrid coupler with a good amplitude balance, a wide variety of techniques based on Poly Phase Filters (PPF) [18, 19] or Quadrature All-pass Filter (QAF) [16, 20] is reported.

The Poly Phase Filter is a modified version of the classical RC-CR network, inheriting key traits from its predecessor. It demonstrates good phase balance, a legacy from the RC-CR network, and achieves effective amplitude balance, especially when employing more sections [21]. The configuration of a wideband, millimeter-wave Poly Phase Filter (PPF) is depicted in Fig. 2.3(a), resembling 3 stages of RC networks interconnected in cascade. Each stage comprises four identical resistors and four identical capacitors, with variations in their values from one stage to the next. In Fig. 2.3(a), In+ and In- represent the differential inputs, $I+$ and $I-$ are the differential outputs of the I path, and $Q+$ and $Q-$ are the differential outputs of the Q path. PPFs operate on the principle of the 'stagger tuning' technique, employing two or more cascaded stages of RC-CR networks to smooth the amplitude of the

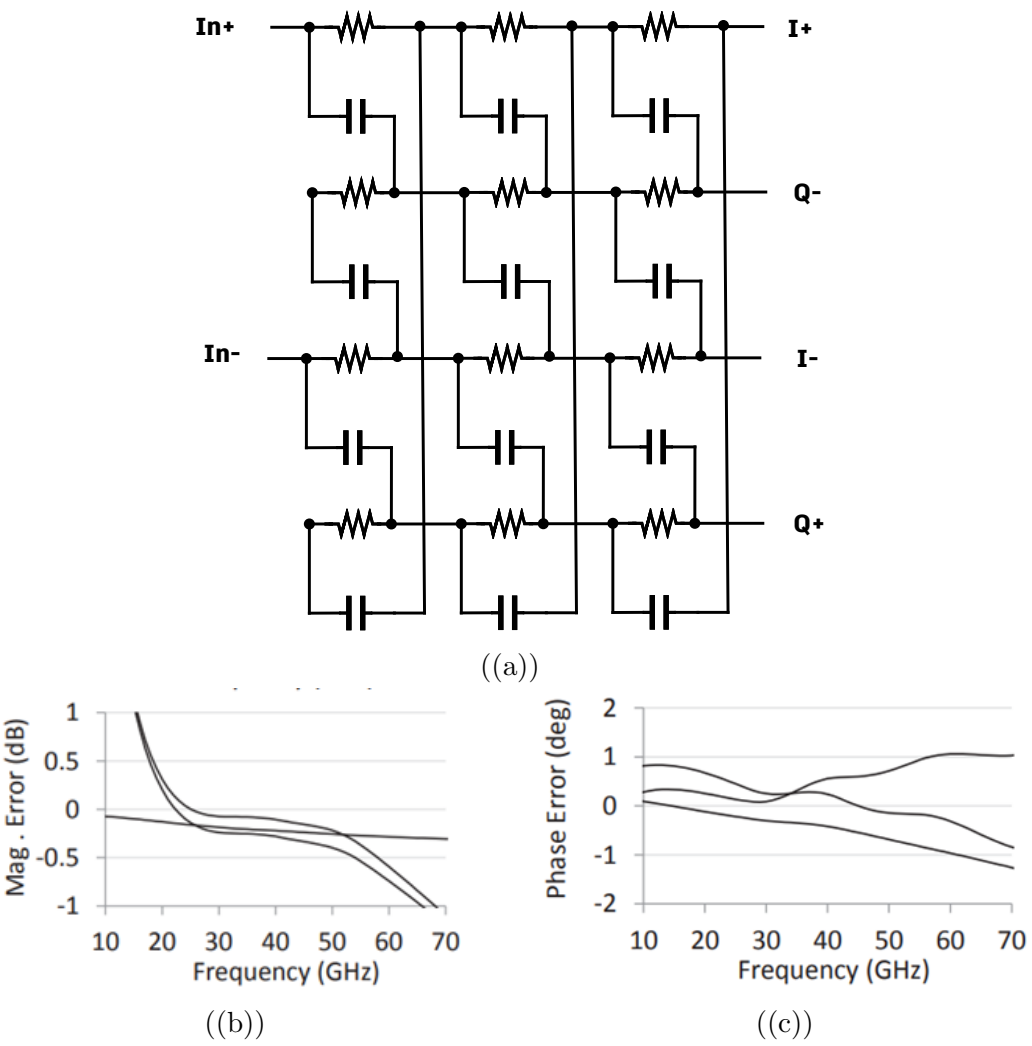


Figure 2.3: (a) Schematic and (b) amplitude balance and (c) phase balance of a millimeter-wave PPF [18]

generated quadrature signal and extend the bandwidth [21]. As an example, the millimeter-wave PPF, introduced in [18], shows great phase and amplitude balance over its operational bandwidth. The measurement results show less than ±0.5 dB magnitude ripple and less than ±1 degree phase error over more than 30 GHz bandwidth, as shown in Fig. 2.3(b) and Fig. 2.3(c), respectively. The reported insertion loss for this configuration is around 19 dB.

PPFs, when employed as quadrature generators, presents numerous advantages over conventional RC-CR techniques [22]:

Simplicity in Implementation: PPFs achieve simplicity by utilizing only resistors and capacitors in their design.

Mitigation of CMOS Process Variation Challenges: The stagger-tuning technique is employed by PPFs to address CMOS process variation challenges without requiring additional complex tuning circuitry.

Well-Suited for Wideband Quadrature Signal Generation: PPFs exhibit suitability for the generation of quadrature signals in a wide bandwidth.

These characteristics render PPFs highly suitable for CMOS implementation, especially as RF quadrature generators, where they are specifically referred to as RF CMOS PPFs. However, despite their appropriateness for RF quadrature signal generation in a CMOS process, RF CMOS PPFs manifest certain drawbacks:

Insertion Loss of 3 dB per Stage: Passive filters in RF CMOS PPFs result in an insertion loss of 3 dB per stage. Moreover, unlike matched configurations, PPFs usually don't adhere to impedance matching [18]. However, they often incur excessive loss, which can impact overall performance.

Need for Buffers (Amplifiers): Buffers, or amplifiers, are often required to compensate for signal attenuation.

Power-Hungry Buffers for High Accuracy: Achieving high accuracy in quadrature signal generation necessitates multiple cascaded stages, leading to power-hungry buffers.

Thermal Noise Impact: When used in the signal path, the thermal noise of resistors adversely affects the noise figure (NF) of the receiver.

In a Quadrature All-Pass Filter (QAF) the quadrature generation is based on the orthogonal phase splitting between V_{OQ} and V_{OI} in the series R-L-C resonators, as shown in Fig. 2.4. The Transfer function of this network can be written as

$$\begin{bmatrix} V_{OI} \\ V_{OQ} \end{bmatrix} = V_{in} \times \begin{bmatrix} \dfrac{s(s+\frac{\omega_0}{Q})}{s^2+\frac{\omega_0}{Q}s+\omega_0^2} \\ \dfrac{\frac{\omega_0}{Q}(s+Q\omega_0)}{s^2+\frac{\omega_0}{Q}s+\omega_0^2} \end{bmatrix}, \tag{2.1}$$

where $\omega_0 = 1/\sqrt{LC}$ and $Q = \sqrt{L/C}/R$. Considering the above-mentioned transfer function, a consistent 90-degree phase shift between the I and Q paths for all values of ω can be ensured. Moreover, it shows that, while having $Q = 1$, a 3-dB voltage

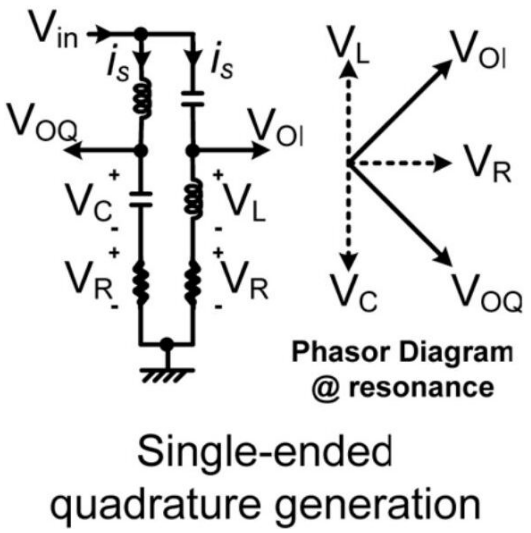


Figure 2.4: Generation of resonance-based second-order all-pass quadrature network (Single-ended configuration) [23]

gain can be achieved at the center frequency, selecting Q in the $0.8 \leq Q \leq 1$ results in a 2 to 3 dB voltage gain over a wideband frequency range as 3:1 [20].

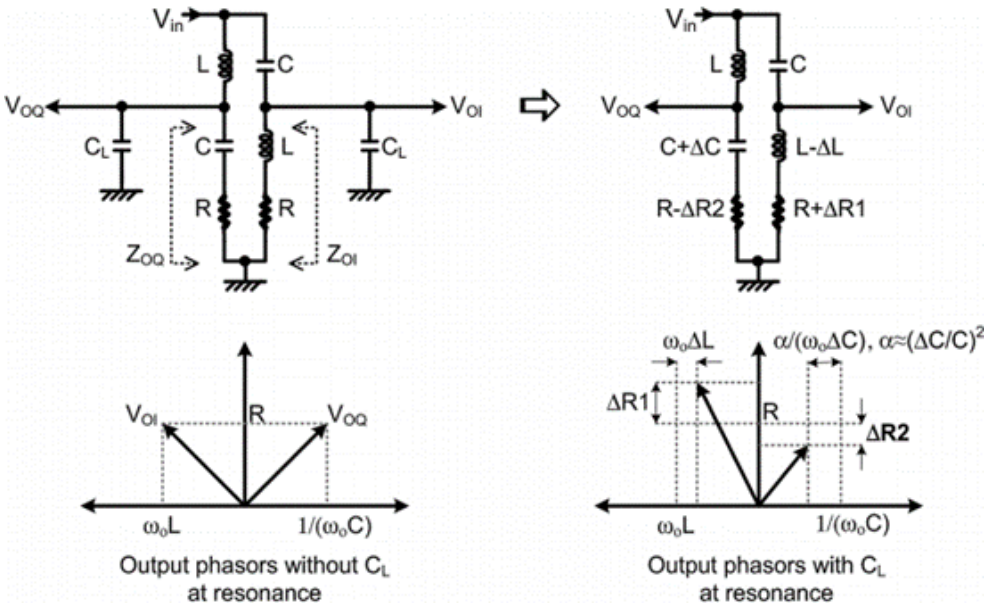


Figure 2.5: Effect of load capacitance on quadrature accuracy in a single-ended QAF [20]

Even with the numerous advantages of the single-ended configuration of the QAF network, it has limited usage in practical applications due to its sensitivity to the load capacitance [23]. The concept of the problem is illustrated in Fig. 2.5. As can be

seen, the load capacitances affect Z_{OI} $(R + j\omega L)$ and Z_{OQ} $(R + 1/j\omega C)$ in a different manner. Intuitively, one can conclude that the load capacitance (C_L) reduces the effective L and decreases the loaded Quality factor (increasing R to $R + \Delta R_1$) in Z_{OI}, while for Z_{OQ} it increases the effective C and the loaded Quality factor (decreasing R to $R - \Delta R_2$), which results in I and Q imbalance.

If the QAF network, shown in Fig. 2.4 is modified to the differential configuration, which is shown in Fig. 2.6(a), the real ground can be eliminated because the differential architecture provides a virtual ground at those points. By eliminating the real ground, the series L-C resonator can be substituted by a wire, as shown in Fig. 2.6(b), and the architecture, shown in Fig. 2.6(c), can be used as a differential QAF. The differential configuration in the all-pass mode can mitigate these errors. This is attributed to the fact that any output node impedance in Fig. 2.6(c) is constructed from both low-pass and high-pass networks, offering counterbalances to the impact of C_L

Variable-Gain Amplifiers (VGAs) and Analog Differential Adder

The VGAs employed in this type of beamformer must possess the capability to amplify signals in both positive and negative polarities, facilitating a complete 360-degree phase shift. The precision of this phase shift is directly dependent on the gain resolution of the VGAs.

Furthermore, as discussed earlier, the amplified I and Q signals must be combined to perform the desired phase shift. As a result,

improvement in analog differential adder and combining the function of the adder with VGA is another interesting subject that is investigated in some studies [24, 25]. As an example, in a study, it is proposed that by controlling the transconductance gain (g_m) of the differential adder via controlling the tail current sources, the function of the adder and variable gain amplification are integrated into one circuit (as shown in Fig. 2.7). Moreover, to amplify I and Q signals with both positive and negative polarity, the Input signals must be applied in differential mode. In addition, if the in-phase signal (I) is required to be amplified in positive polarity the Q_1 and Q_4 transistors must be activated while the Q_2 and Q_3 transistors are deactivated. However, if the amplification with negative polarity is required, the condition must

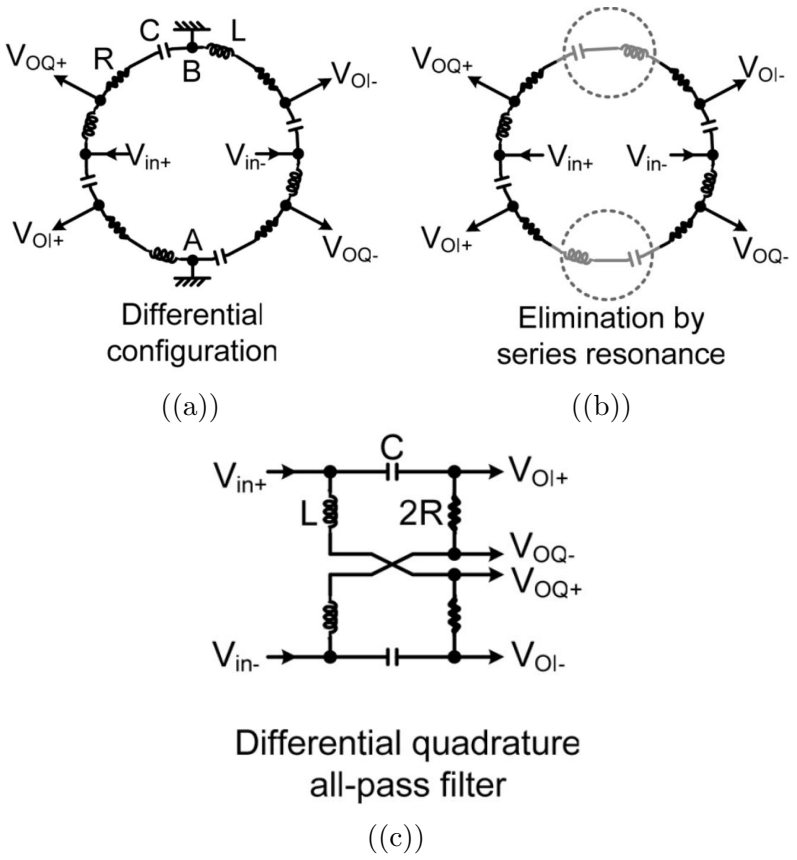


Figure 2.6: (a) Differential formation of QAF, (b) Elimination of redundancy, and (c) Differential quadrature all-pass filter. [23]

be opposite. Similarly, for the positive polarity amplification in the quadrature-phase signal (Q), the Q_5 and Q_8 transistors must be activated while the Q_6 and Q_7 transistors are deactivated. Whereas, for negative polarity amplification, the activated and deactivated transistors must be switched.

Fig. 2.8 provides a detailed depiction of the operational principles of a VGA/Differential Adder. Within this circuit, when the S_I (S_Q) switches are in the ON position, the S_{IB} (S_{QB}) switches are in the OFF position, leading to the amplification of the In-Phase (Quadrature) signal with positive polarity. Conversely, when the S_IB and S_QB) switches are ON, and the S_I (S_Q) switches are OFF, the In-Phase (Quadrature) signal undergoes amplification with negative polarity.

In the context of positive polarity amplification, the tail current denoted as I_{IB} (I_{QB}) flows through M_{S1} (M_{S3}), activating the pair of transistors M_1 and M_4 (M_5 and M_8). Conversely, during negative polarity amplification, the tail current flows

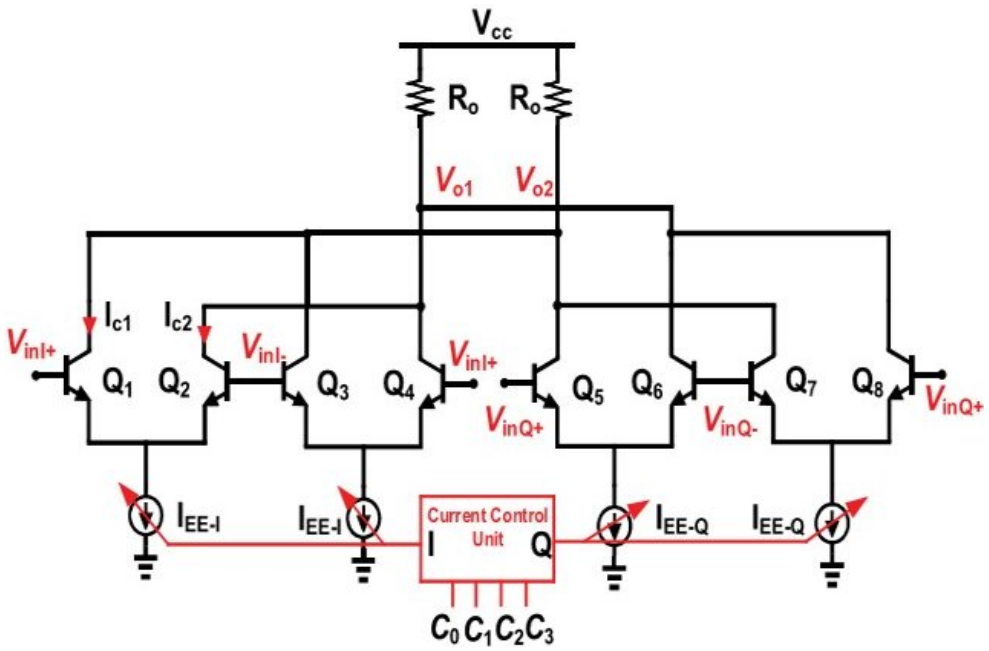


Figure 2.7: Combining the variable gain amplification and differential adding function by controlling tail currents in adder [24]

through M_{S2} (M_{S4}), activating the pair of transistors M_2 and M_3 (M_6 and M_7). It is noteworthy that the gain of VGAs in both the I and Q paths can be individually adjusted by independently varying the tail currents I_{IB} and I_{QB}.

Furthermore, as the differential pairs transform the amplified signals into currents, connecting the drains of the corresponding transistors to the appropriate ends of a common load results in the addition of the weighted-amplified I and Q signals.

Generally, one can say that although VMB phase shifters use active devices in their structure, and consequently consume DC power, they can provide gain and can be implemented in a smaller area compared to their passive counterparts [26, 27].

2.2.2 Passive Phase Shifters

A passive phase shifter is a device that introduces a controlled phase shift to an input signal without amplifying it. Since this type of phase shifter does not consume DC power, they become very popular in growing low-power millimeter-wave sensors [28, 29]. The passive phase shifters can be divided into three main categories: STPSs, Reflection Type Phase Shifters (RTPSs), and Tunable Transmission Line Phase Shifters (TTLPSs). In this section, the introduced types of passive phase shifters and their

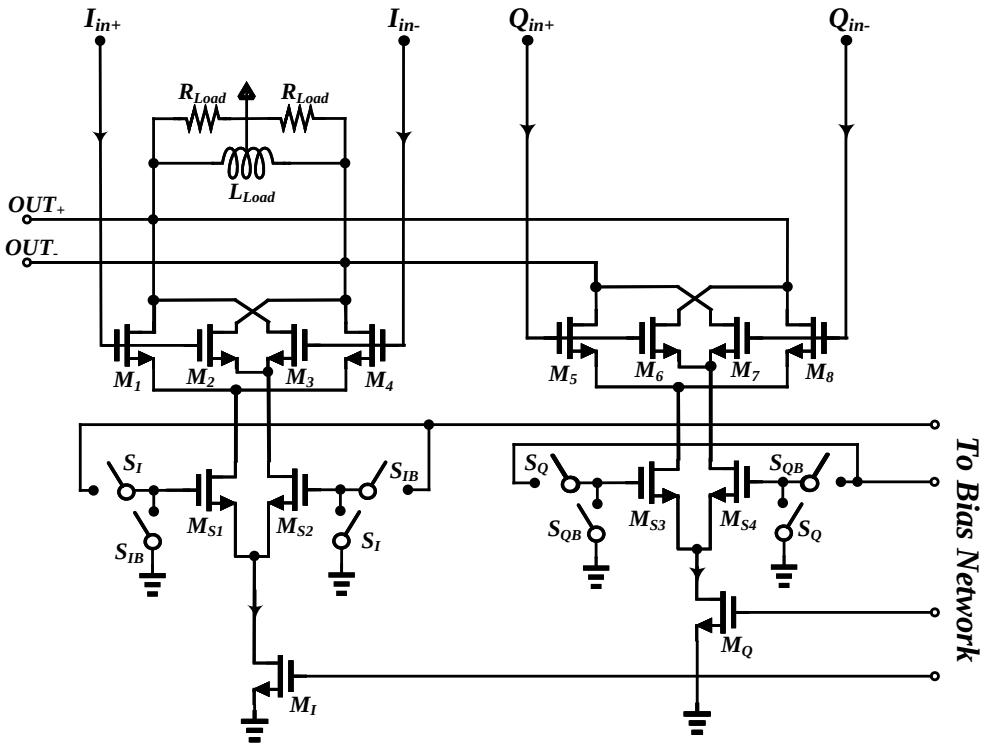


Figure 2.8: An Analog differential adder/VGA implemented in CMOS [25]

challenges have been reviewed.

Switched Type Phase Shifters (STPS)

As shown in Fig. 2.9, in the switched type phase shifters, also known as switched delay line phase shifters, using a proper combination of switches, the input signal passes through different paths with different electrical lengths (constructed using transmission lines or lumped element components) and then obtains the desired phase shift [30]. Assuming equivalent propagation constants (β) and matched conditions for both lines, shown in Fig. 2.9, if both input and output ports are switched to the lower transmission line, then the input and output signals will be expressed as:

$$V_{in} = V^+ \cos(\omega t) \tag{2.2}$$

and

$$V_{out} = V^+ \cos(\omega t - \beta L), \tag{2.3}$$

However, in the event of the port switching to the upper transmission line, then the output voltage modifies to

$$V_{out} = V^{+} \cos\left(\omega t - \beta(L + \frac{\Delta L}{2})\right). \tag{2.4}$$

The additional phase difference of $\beta\Delta L/2$ in (2.4), represents the introduced phase shift achievable through this method. Notably, the adjustment of the length difference between the upper and lower transmission lines allows for the attainment of arbitrary phase shifts. It is essential to recognize that, post-circuit implementation, the amount of phase shift becomes fixed. Consequently, to obtain varying phase shift values, it becomes imperative to increase the number of paths and switches in the circuit.

These switched delay line phase shifters consume no power but they have a limited resolution because of the limited number of switches and delay elements that can be constructed at reasonable cost[28, 30].

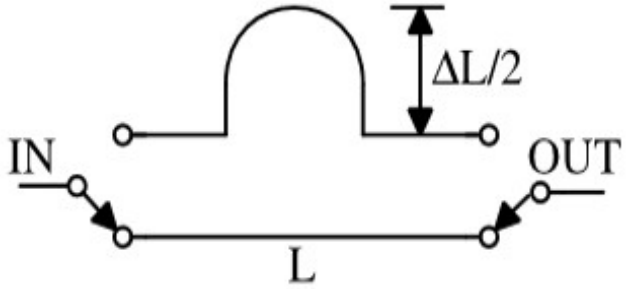


Figure 2.9: Switched delay line phase shifter concept

In the on-chip realization of the delay line, instead of a real transmission line, a Π cell, which consists of a series inductor and two shunt capacitances, is used to create an ATL cell. Equivalently, a T connection of two series inductors and one shunt capacitor can form an ATL cell. In the ATL cell, the proper selection of inductor and capacitance values helps to construct a network that behaves like a matched transmission line and provides the desired phase shift (see chapter 3 and 4). It is important to notice that the ATL cell can only model the transmission lines with the electrical length of up to 90 degrees. Consequently, to construct a phase shifter with a complete range of phase shifts (360 degree) with a desired resolution, a sufficient number of cells with different electrical lengths must be cascaded. Moreover, switches

must be properly used along the cells to effectively include and exclude them in the phase shift chain whenever it is required. An example of such ATL cell and proper method of its including and excluding is shown in Fig. 2.10(a) [28].

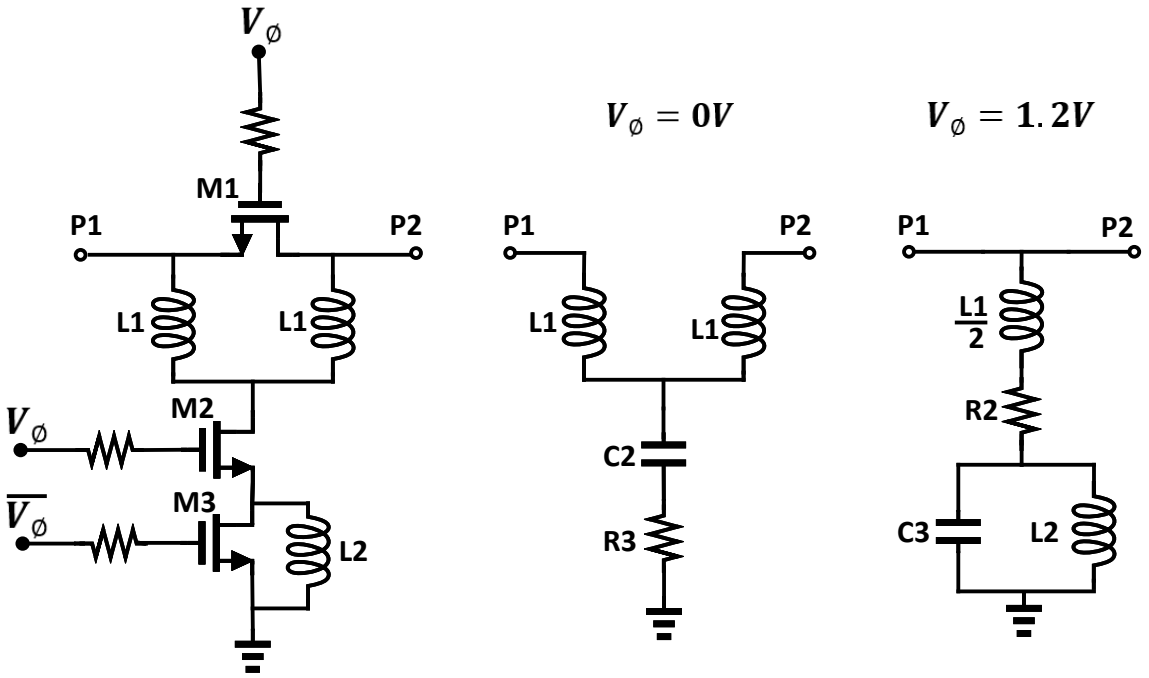


Figure 2.10: Example of ATL cell including/excluding mechanism in an STPS [28]

In the examined circuit, when the voltage across the phase control input (V_ϕ) is maintained at 0 V, both transistors M_1 and M_2 assumed to be in the OFF state, while transistor M_3 is switched ON. Under this configuration, the circuit depicted in Fig. 2.10(a) can be effectively modeled by the circuit presented in Fig. 2.10(b). Notably, in this model, the direct path between the input and output ports (P1 and P2) is eliminated, and the inductor L_2 is bypassed by the activated M3 transistors. Assuming proper sizing of M_2, the parasitic capacitance C_2 associated with its OFF state, in conjunction with two identical inductors connected to the ports (two L_1 inductors), forms a T cell capable of achieving the desired delay (phase shift). Furthermore, to mitigate losses within the cell, it is imperative to minimize the ON state resistance of M_3 (R_3).

Conversely, when V_ϕ is set to 1.2 V, the circuit model undergoes a transformation to the configuration illustrated in Fig. 2.10(c). Under this condition, the input and output ports are directly connected. Additionally, if the design of M3 is such that its

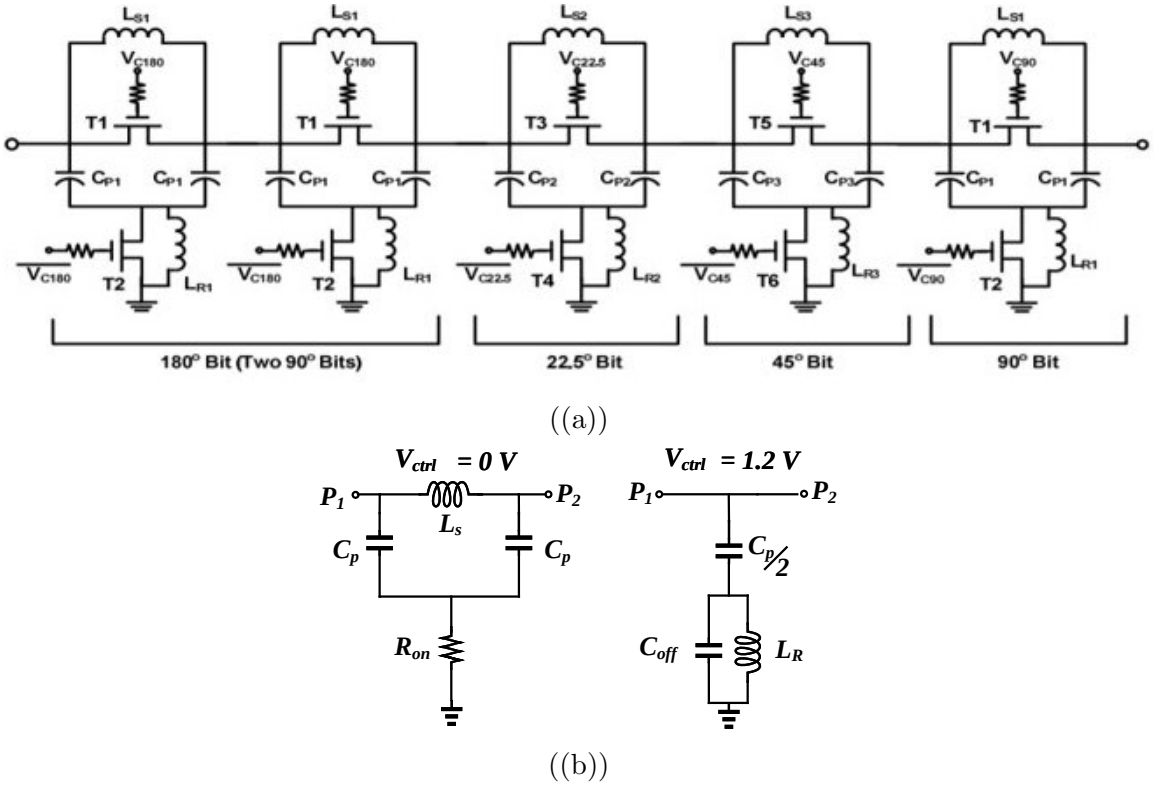


Figure 2.11: (a) A 4-bit switched delay line 67 to 78 GHz phase shifter and (b) the ATL cell including/excluding mechanism [30]

OFF state capacitance (C_3) and L_2 together form a parallel resonator at the operational frequency, the shunt path will not impose a loading effect on the through path between P1 and P2. This strategic design ensures optimal performance of the circuit in various operational states, contributing to the overall efficiency of the system.

Fig. 2.11 illustrates another instance of a switched delay line phase shifter employing ATL cells configured in a T arrangement. To incorporate a cell into the phase shift chain, the series transistor (T1/T3 or T5) must be in the OFF state, while the shunt transistor (T2/T4 or T6) needs to be in the ON state. Similar to the aforementioned case, minimizing the ON resistance of the shunt transistors is imperative for mitigating losses within the ATL cell.

Conversely, to exclude a cell from the chain, the states of the switches must be reversed. Activating the series transistors (T1/T3 or T5) to the ON state bypasses the series inductors (L_{si}) of the cell. Furthermore, through careful design of the inductors operating in parallel with the shunt transistors (L_{Ri}), it is possible to establish a

parallel resonator with the OFF-state capacitance of the transistors. This strategic configuration ensures that the shunt branches do not impose a loading effect on the path between the input and output ports, optimizing the performance of the phase shifter.

Reflection Type Phase Shifters (RTPS)

A block diagram of a typical Reflective Type Phase Shifter (RTPS) is shown in Fig. 2.12. An RTPS produces a phase shift by controlling the phase of a reflective load connected to a 90-degree hybrid coupler [29, 31, 32]. With the incident voltage at the input port denoted V_1^+, the incident voltages at the Through (THRU) and Coupled (CPLD) ports are

$$\begin{aligned} V_{THRU}^+ &= \frac{-j}{\sqrt{2}} V_1^+ \\ V_{CPLD}^+ &= \frac{1}{\sqrt{2}} V_1^+. \end{aligned} \tag{2.5}$$

Since both two ports are connected to the loads, which have identical reflection coefficients equal to Γ_T, the reflected voltage at these ports will be

$$\begin{aligned} V_{THRU}^- &= \frac{-j}{\sqrt{2}} \Gamma_T V_1^+ \\ V_{CPLD}^- &= \frac{1}{\sqrt{2}} \Gamma_T V_1^+. \end{aligned} \tag{2.6}$$

Assuming that the Isolation port (ISO) is connected to a matched termination, the voltage at this port can be calculated as

$$V_{ISO} = \frac{1}{\sqrt{2}} V_{THRU}^- + \frac{-j}{\sqrt{2}} V_{CPLD}^-. \tag{2.7}$$

Using (2.6), equation (2.7) can be simplified to

$$\begin{aligned} V_{ISO} &= \frac{1}{\sqrt{2}} \frac{-j}{\sqrt{2}} \Gamma_T V_1^+ + \frac{-j}{\sqrt{2}} \frac{1}{\sqrt{2}} \Gamma_T V_1^+ \\ &= \frac{-j}{2} \Gamma_T V_1^+ + \frac{-j}{2} \Gamma_T V_1^+ \\ &= -j \Gamma_T V_1^+. \end{aligned} \tag{2.8}$$

Evidently, the variation in the phase of the load (Z_T) connected at the THRU and CPLD terminals of the hybrid coupler induces a corresponding change in the phase of the output signal, where the degree of phase shift aligns with the phase of the

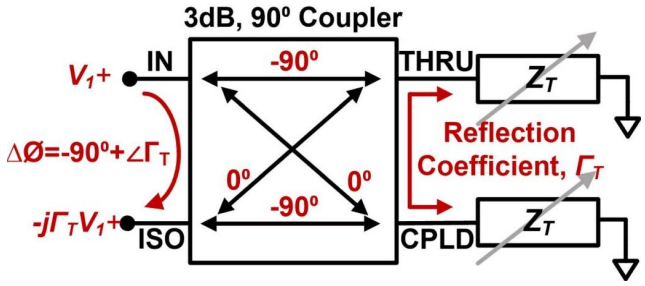


Figure 2.12: Block diagram of a typical reflection-type phase shifter [33]

reflection coefficient of the loads ($\angle\Gamma_T$). The reflected voltage at the input port can be calculated as

$$V_1^- = \frac{-j}{\sqrt{2}}V_{THRU}^- + \frac{1}{\sqrt{2}}V_{CPLD}^-. \tag{2.9}$$

Similar to the calculation of the isolation port's voltage, one can use (2.6) to simplify (2.9) to

$$\begin{aligned} V_1^- &= \frac{-j}{\sqrt{2}}\frac{-j}{\sqrt{2}}\Gamma_T V_1^+ + \frac{1}{\sqrt{2}}\frac{1}{\sqrt{2}}\Gamma_T V_1^+ \\ &= \frac{-1}{2}\Gamma_T V_1^+ + \frac{1}{2}\Gamma_T V_1^+ \\ &= 0. \end{aligned} \tag{2.10}$$

Equation (2.10) shows that utilizing a 90-degree hybrid coupler establishes a matched condition for the input signal, independent of the load's reflection coefficient magnitude. Conversely, as shown in (2.8), the magnitude of the output signal is directly proportional to $|\Gamma_T|$. Consequently, to minimize the insertion loss of this phase shifter, it is imperative to ensure that

$$|\Gamma_T| \approx 1. \tag{2.11}$$

Moreover, to achieve low insertion loss across all phases, equation (2.2) must be maintained while the phase of the load varies.

While consuming no power, the limited bandwidth of 90-degree hybrid couplers and the variability of the load reflection coefficient magnitude often lead to narrowband phase shifters with high variable insertion losses particularly if implemented on-chip [33]. To overcome these limitations, several solutions are reported [31, 33]. As an example, Fig. 2.13 shows a Reflective Type phase shifter in which a π network of a series inductor and two shunt varactors are used to create a variable reflective load.

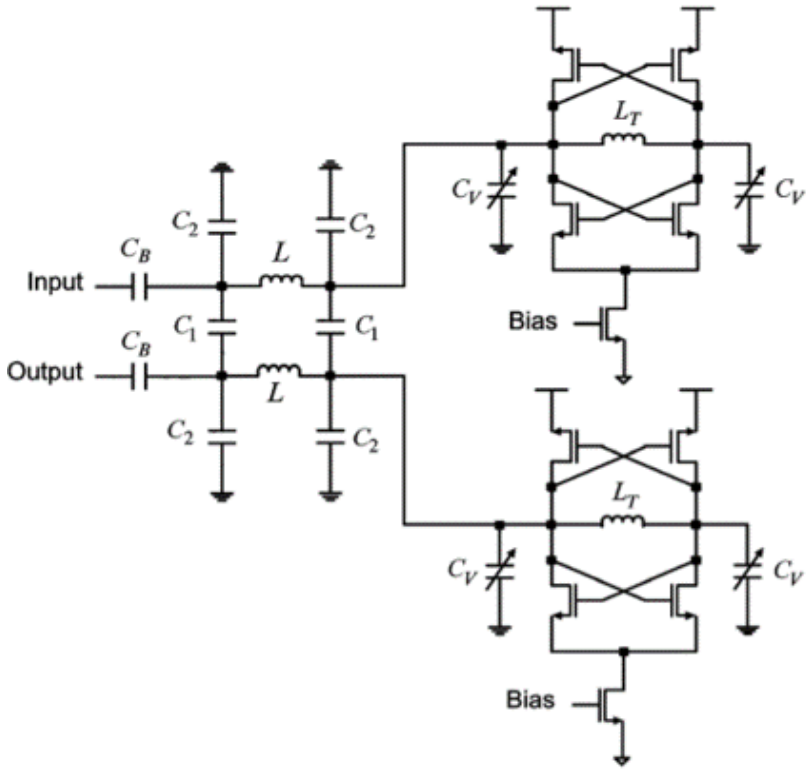


Figure 2.13: Reflective Type Phase Shifter with Loss compensation [31]

To keep the magnitude of the reflection coefficient of the reflective load around one ($|\Gamma_L| = 1$), a negative resistance is placed in parallel with the inductor to compensate for its loss.

It is a well-established phenomenon that at the input of a short-circuited transmission line, there exists a superposition of the incident voltage and its delayed (phase-shifted) reflection [34]. The delay associated with the reflected voltage is precisely twice the delay between the input and the location of the short circuit. Consequently, a configuration employing multiple switches along a transmission line, as illustrated in Fig. 2.14, can be utilized. By maintaining all switches in the OFF state, except for the switch positioned at the desired location (providing the required delay or equivalently phase shift) in the ON state, a range of delay signals with varying amounts of delay (phase shift) can be obtained.

The potential significance of such a phase shifter is more highlighted if the non-delayed signal can be eliminated. This would yield substantial advantages for two primary reasons. First, under the assumption of a low-loss implementation of both

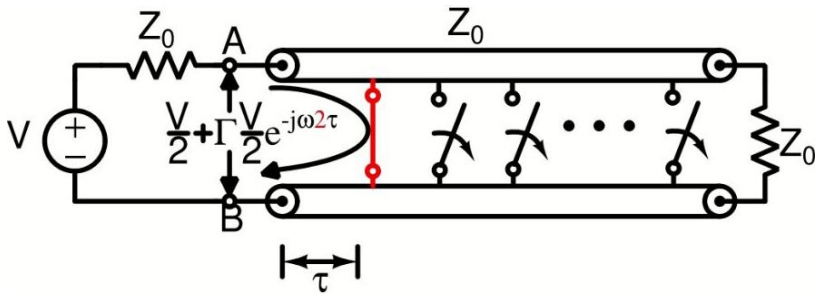


Figure 2.14: Operation of a switched transmission line phase shifter [35]

the transmission line and switches, the magnitude of the reflected signal approximates that of the incident voltage, resulting in negligible insertion loss. Second, the achievable delay (phase shift) is twice the electrical length of the transmission line, rendering this approach highly area-efficient.

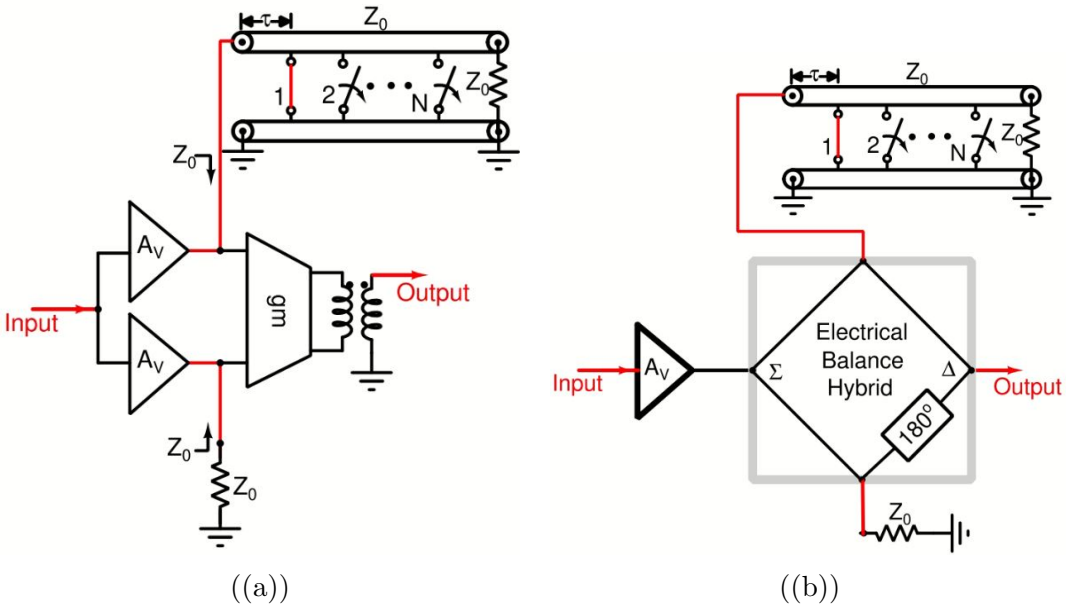


Figure 2.15: Cancellation of non-delayed signal: (a) Active approach. (b) Passive approach employing a Hybrid coupler. [35]

The authors in reference [35] proposed an innovative method for canceling the non-delayed signal, which can be implemented using either an active or passive approach, as depicted in Fig. 2.15(a) and Fig. 2.15(b), respectively. In this method, the input signal undergoes division into two samples. One of these samples is then applied to the switch-loaded transmission line, resulting in the simultaneous presence of both delayed and non-delayed signals at the input of the transmission line. Subsequently,

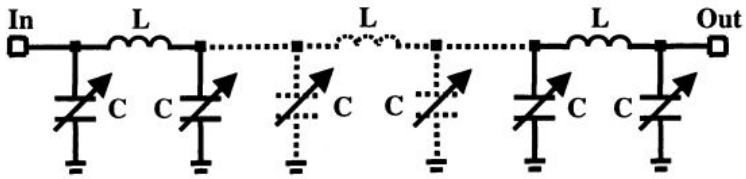
by differentiating the other sample from the signal at the input of the transmission line, the non-delayed portion of the signal is effectively canceled, leaving only the delayed (phase-shifted) component.

Fig. 2.15 illustrates the cancellation of the non-delayed signal using both an active approach, Fig. 2.15(a), and a passive approach employing a Hybrid coupler, Fig. 2.15(b)) [35]. This technique offers a promising solution for enhancing the performance of phase shifters by eliminating undesired components and preserving the desired phase-shifted signals.

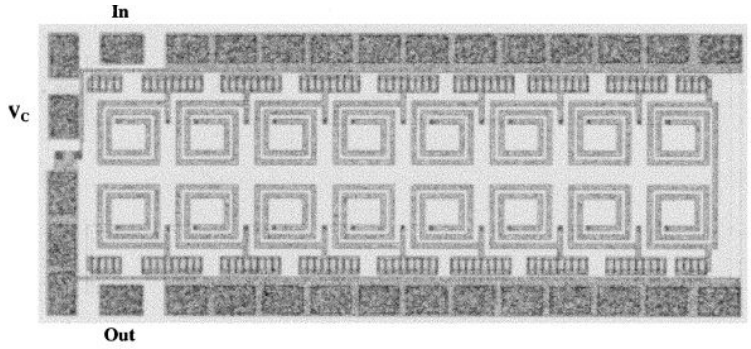
Tunable Transmission Line Phase Shifters

Instead of using multiple switches and ATL cells with fixed capacitors, an ATL cell can be loaded with varactors to create a tunable continuous phase shift by controlling the DC biasing of the varactors. Both the T and Π configurations of the ATL cell (shown in Fig. 2.10 and Fig. 2.11, respectively) can be used for this propose. However, the T configuration emerges as the preferred choice due to its minimal requirement for area-consuming inductors. Combining neighboring varactor capacitances further enhances efficiency. The distributed phase shifter, employing low-pass structures, minimizes bias complexity, grounding varactor anodes without necessitating additional bias circuitry. The connection of all varactor cathodes through inductors allows the control voltage to be fed into a single inductor node, streamlining the control mechanism. Variations in cathode voltage potential enable the application of positive voltage within the primary control range. While consuming no power, these varactor-loaded cells (known as Tunable-ATL cells) provide large bandwidth and fine phase resolution. However, Tunable Transmission Line (TTL) phase shifters, which are formed by cascading multiple Tunable-ATL cells, exhibit high Insertion Loss (IL) and occupy a relatively large area, particularly when realized on-chip, because of the large size and low quality factor of the on-chip passive components [26]. It should be noted, like the switched delay line phase shifter, the values of the cell's inductor and capacitance of varactors must be calculated properly to achieve good matching performance (see Chapters 3 and 4). Fig. 2.16 shows the circuit model and a sample of on-chip implementation of this type of phase shifter.

Table 2.1 presents a comprehensive comparison of diverse phase-shifting methods,



((a))



((b))

Figure 2.16: (a) The circuit model and (b) On-chip realization of C-Band Tunable Transmission Line (TTL) phase shifter. Chip size is $1.4mm \times 0.6mm$ [36]

Table 2.1: Comparing Phase Shifting Methods

Parameters	**VMB**	**STPS**	**RTPS**	**TTL**
Bandwidth	Low/Moderate	High	Low/Moderate	High
Complexity	High	Low	Moderate	Low
Power Consumption	High	No	No	No
Chip Area Consumption	Low	High	Moderate	High
Phase resolution	High	Low	High/Moderate	High

encompassing both active and passive variants. Notably, TTL phase shifters exhibit distinct advantages over other types. They boast zero DC power consumption, expansive bandwidth, and high phase resolution. However, the sole drawback lies in their substantial chip area requirement. Addressing this limitation through innovative methods could render TTL phase shifters highly advantageous for on-chip implementation in the evolving landscape of compact, high-data-rate wireless devices. Chapter 3 of this thesis elaborates the details of an innovative method which is used to make a compact TTL phase shifter.

2.3 Recent Advances in Analog (RF) Beamformers

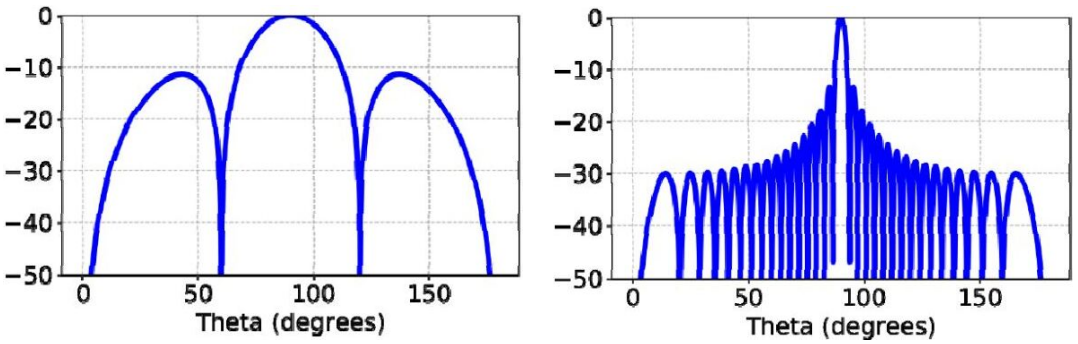
2.3.1 Requiring a large scale phased array

Fig. 1.2 illustrates that in a phased array receiver, increasing the number of antenna elements proportionally enhances the overall SNR. In wireless communication systems, the radiated power is commonly characterized using Equivalent Isotropic Radiated Power (EIRP). EIRP is calculated as the product of the transmitter's output power and the antenna gain. This metric effectively illustrates the transmitter's output power under the assumption that the antenna pattern is isotropic. In essence, EIRP provides insight into the potential power output if the antenna radiated uniformly in all directions. For a phased array transmitter, utilizing n antenna elements amplifies the EIRP by a factor of n^2, while power consumption only increases linearly by a factor of n. This method proves to be the most efficient way to combine transmitter power [37].

Moreover, augmenting the number of antenna elements results in a narrower beamwidth and causes a greater concentration of power in the desired pointing direction. Although the first sidelobe level remains invariant in the array pattern, increasing the number of elements brings the first sidelobe closer to the main lobe, effectively reducing overall sidelobe power [37]. Fig. 2.17(a) and Fig. 2.17(b) depict the normalized patterns for a uniform array with 16 and 1024 antenna elements, respectively. Notably, despite both cases having the first sidelobe level only 13 dB lower than the mainlobe's peak, the radiated power in undesired directions significantly diminishes in the array with 1024 elements.

To enable the integration of a greater number of elements in a phased array system, the phased array scaling approach is introduced [37]. This strategy addresses two primary concerns: first, the development of a replicable unit tile containing antennas and circuits, and second, the effective tiling of these units to construct a larger phased array.

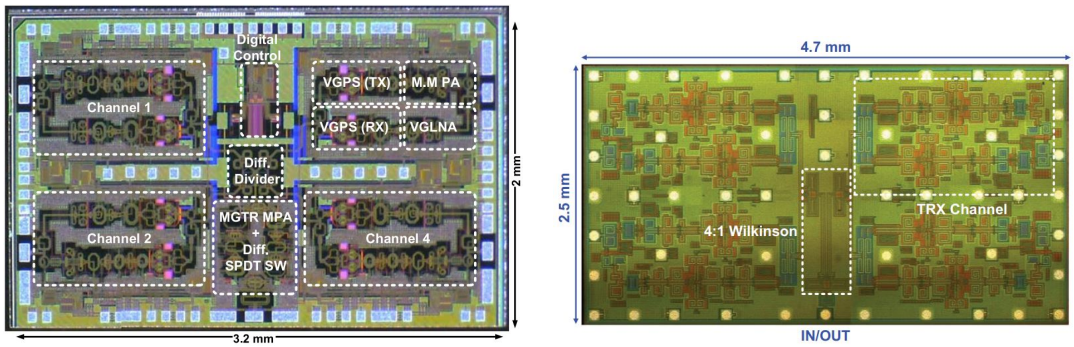
Fig. 2.18(a) shows the die photograph of a 28-GHz fully differential four-channel



((a)) ((b))

Figure 2.17: Normalized array factor of a uniform phased array system with (a) 16 and (b) 1024 elements [37]

beamforming front-end IC with variable gain phase shifters (VGPSs) [38]. This work achieves a compact chip size by utilizing VGPS, which combines phase and gain control within a single block through their proposed dual-vector synthesis technique. The authors further demonstrate a 64-element brick-type phased array antenna employing the four-channel core chips, exhibiting an EIRP of 54.4 dBm at 28 GHz.



((a)) ((b))

Figure 2.18: (a) 28-GHz four-channel beamforming front-end IC [38] and (b) 28-GHz 2x2 TRX array [39]

Another instance is presented in [39], where a 32-element phased-array architecture, based on a 28-32 GHz silicon core chip, is designed. This architecture features 4 transmit/receive elements, each equipped with 14 dB gain control and 6-bit phase control. Eight of these chips are arranged on a printed circuit board (PCB) with integrated antennas and Wilkinson combiners to constitute the 32-element array.

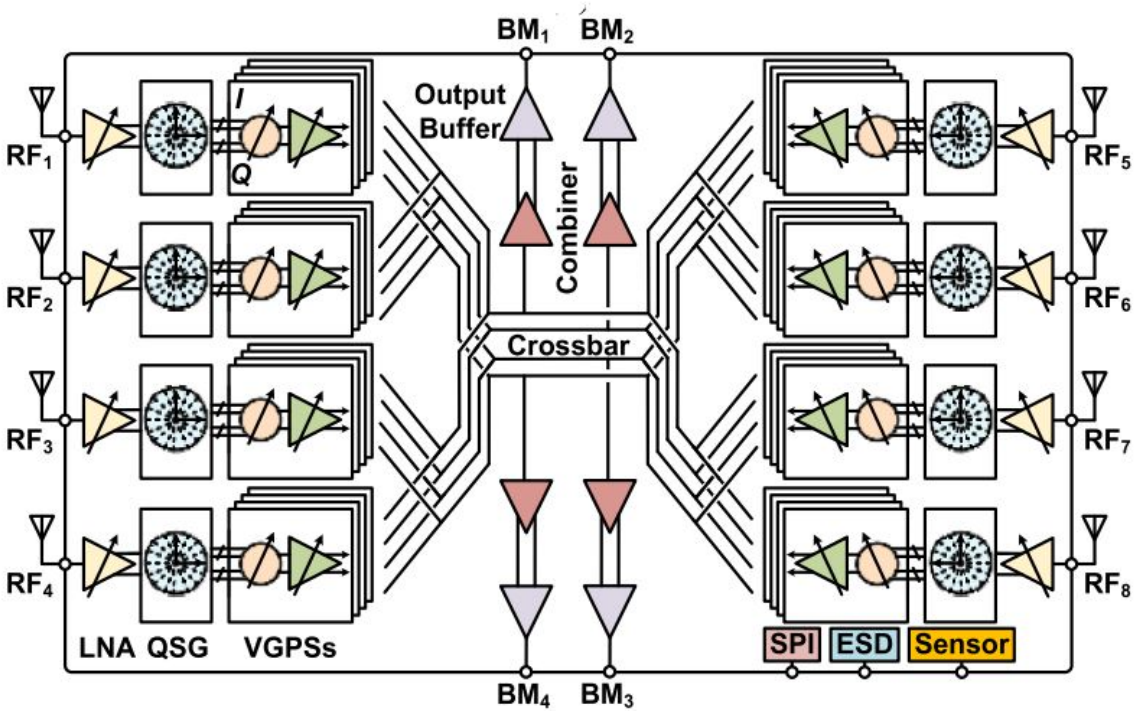


Figure 2.19: Architecture of a Ka-Band eight-element, four-beam phased-array receiver front end [42]

2.3.2 Novel Architectures for Multiple Beam Phased Arrays

In addition to modern cellular applications (millimeter-wave 5G), integrated analog (RF) beamformers have been widely applied in other wireless applications, like UAV and satellite communication, where power consumption and the size of the devices are of serious concerns. As a consequence, reducing the size and power consumption of such beamformers is crucial. To achieve this goal, there are several recent works that focus on developing compact and energy-efficient RF chains. As the simplified block diagram of an RF chain shown in Fig. 1.7, the RF chain consists of an LNA and a phase shifter (in receiving mode). However, in addition to these blocks, a real RF chain has a gain control mechanism (usually a digital step attenuator) and several other gain blocks for loss compensation. Improving the performance of each of these blocks or combining functions of different blocks into a single circuit were the subjects of several researches [14, 40, 41]

On the other hand, several recent studies focus on utilizing more than one simultaneous beam from a beamformer with a given area and power consumption. In such

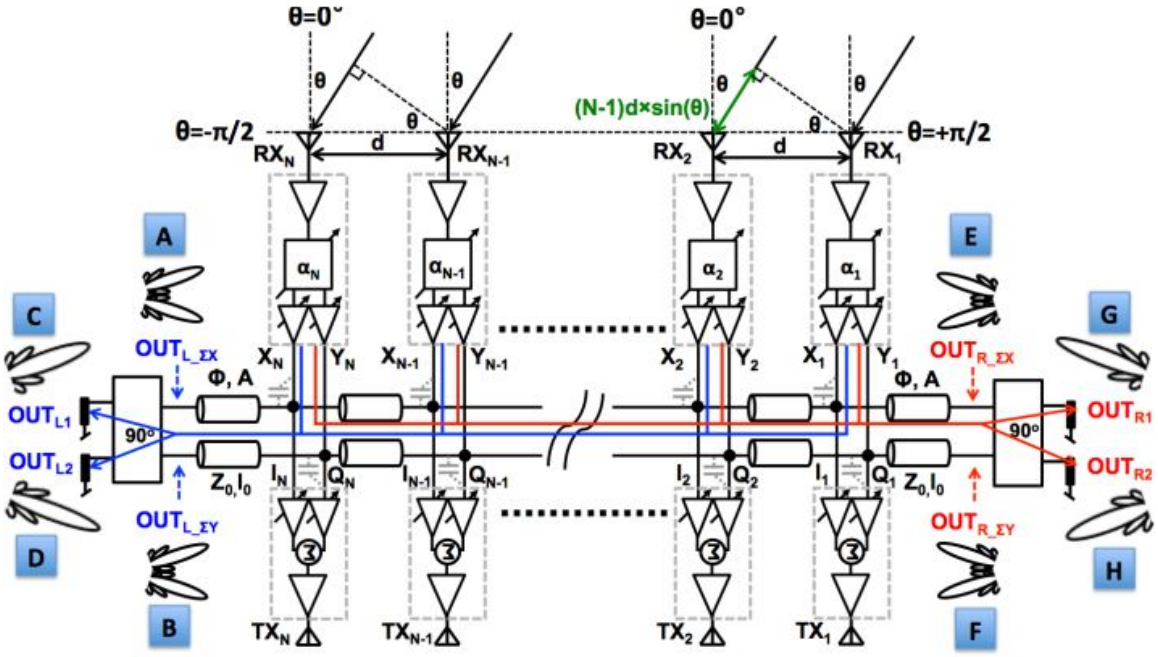


Figure 2.20: Block diagrams of a 28-GHz series-fed distributed beamformer [43]

systems usually one beam is steered independently while the other beam(s) act as a mirror or an offset of the main beam and help to cover multiple spots simultaneously which is highly desired in UAV and satellite communication. As an example, the authors in [42] use an active combining scheme to enable compact implementation of their proposed beamformer (the block diagram is shown in Fig. 2.19). Although taking this approach leads to forming an eight-element four-beam phased-array receiver front end in a small chip area, the power consumption is increased noticeably.

As another example, the study in [43] showed that by using a series-feed network, a distributed beamformer that is capable of supporting up to four simultaneous beams can be constructed. Of these four beams, the first beam can be independently controlled, the second beam is created as a mirror image of the first, the third beam is shifted relative to the first according to the phase shift within the series-feed structure, and the fourth beam mirrors the shifted beam. The block diagram of the beamformer is shown in Fig. 2.20. As a contribution to the recent advances in RF beamformers discussed here, Chapter 4 of this thesis provides the details of the design and fabrication of a compact RF beamformer with pseudo-distributed amplifier architecture in K-band.

Chapter 3

Area-Efficient Tapered Tunable Transmission Line Phase Shifters

In the previous chapter, TTL phase shifters, which are usually constructed by cascading identical ATL cells, are introduced. In addition, it is mentioned that although it seems that TTL phase shifters are suitable candidates because of their zero power consumption, large bandwidth, and good linearity, they have not been widely used in integrated designs because of their relatively large chip area caused by the construction of the on-chip inductors. In this chapter, a novel compact Tapered TTL phase shifter is proposed to reduce the overall chip area and hence the cost of the chip fabrication. Similar to the conventional TTL phase shifter, Fig. 3.1(a), the proposed phase shifter is constructed by cascading ATL cells. In the proposed design, while maintaining the electrical length of the ATL cells, the cells' inductor size is gradually decreased, or tapered, from the outer to the inner cells reaching the minimum ATL cell's inductor in the middle cells as shown in Fig. 3.1(b). The tapering process is designed and implemented in such a way that the return and insertion losses of the proposed phase shifter remain in an acceptable range. The design process for optimal sizing of the tapered cells is provided to achieve a compromise between matching performance and area efficiency and is supported by mathematical analysis. To prove the efficacy of the proposed tapering method, a Ku/K/Ka band MMIC phase shifter is fabricated in a standard 65-nm Complementary Metal–Oxide–Semiconductor (CMOS) technology and the measurement results are reported. The fabricated phase shifter provides phase control of up to 180° and low loss performance over the 16.5-31 GHz frequency range.

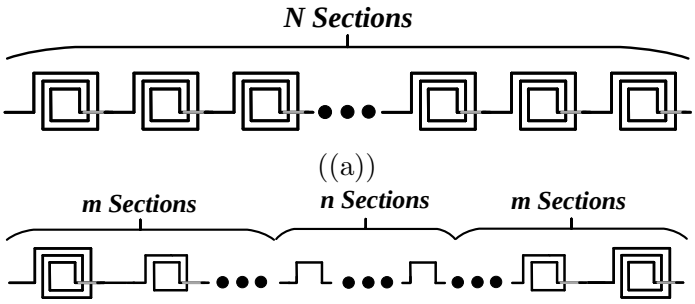


Figure 3.1: The appearance of the inductors in the layout of (a) an N-cell conventional and (b) an N-cell proposed Tapered TTL phase shifter

3.1 Proposed Tapered TTL Phase Shifter

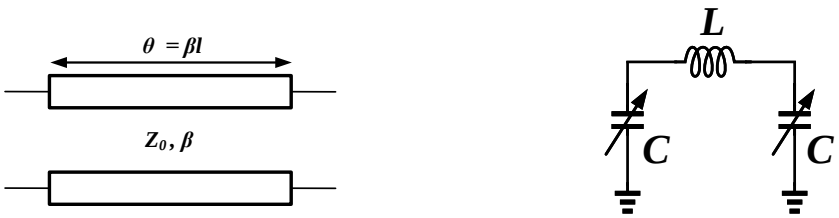


Figure 3.2: (a) Transmission line with electrical length θ and (b) lumped-element realization of transmission line

Tunable transmission line phase shifters are constructed on-chip by cascading several π-ATL cells incorporating on-chip inductors and varactors (shown in Fig. 3.2) as it is not economical to integrate conventional transmission lines on-chip because of their large size. The ABCD matrix of a lossless transmission line with an electrical length θ and with characteristic impedance Z_0 (Fig. 3.2(a)) can be written as [34]:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} cos\theta & jZ_0 sin\theta \\ jY_0 sin\theta & cos\theta \end{bmatrix}. \tag{3.1}$$

On the other side, the ABCD matrix of a π-ATL cell, Fig. 3.2(b), can be expressed as [44]:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 - LC\omega^2 & jL\omega \\ 2jC\omega - jLC^2\omega^3 & 1 - LC\omega^2 \end{bmatrix}. \tag{3.2}$$

Comparing the A (or D) elements of both matrices, one can verify that for a π-ATL cell to act as a transmission line of electrical length θ (as long as $\theta \leq 90^o$), the following relation must hold true between the values of L, C, and θ at the operation frequency ω:

$$\theta = \arccos(1 - LC\omega^2). \tag{3.3}$$

To tune the electrical length of a π-ATL cell to produce a controllable phase shift, the value of L or C or both must be varied by a control signal. As it is not possible to change the inductance of on-chip inductors, variable capacitors (varactors) are utilized to vary the phase shift of ATL cells. These varactors can be constructed using transistors. Considering that C varies as

$$C_{min} \leq C \leq C_{max}, \tag{3.4}$$

the maximum phase shift that can be achieved by varying the varactor's capacitance within its maximum range is calculated as

$$\Delta\theta_{max} = \arccos(1 - LC_{max}\omega^2) - \arccos(1 - LC_{min}\omega^2). \tag{3.5}$$

If it is assumed that the π-ATL cell's input and output are matched to Z_0 when the varactors are at their middle value ($C_0 = \sqrt{C_{max}C_{min}}$) and the electrical length is equal to θ_0 (mid-range electrical length), as shown in [36], the maximum achievable phase shift ($\Delta\theta_{max}$) and the insertion loss of the cell are directly proportional to θ_0. Therefore, to increase the $\Delta\theta_{max}$, it is required to increase θ_0 as long as the insertion loss remains acceptable. Equalizing the B elements in (3.2) and (3.1) results in

$$L\omega = Z_0 \sin\theta_0. \tag{3.6}$$

According to (3.6), the inductor reactance ($L\omega$) is directly proportional to θ_0 for small θ_0. It means that at a given frequency (ω), having a larger θ_0 requires a larger inductance (L). Furthermore, as can be seen from (3.6) for a given θ_0 and Z_0, the inductance is inversely proportional to ω. Consequently, it can be concluded that if this type of π-ATL cell is intended for using in wideband, TTL based phase shifters, the required phase shift at the lowest operating frequency determines the minimum size of the inductors.

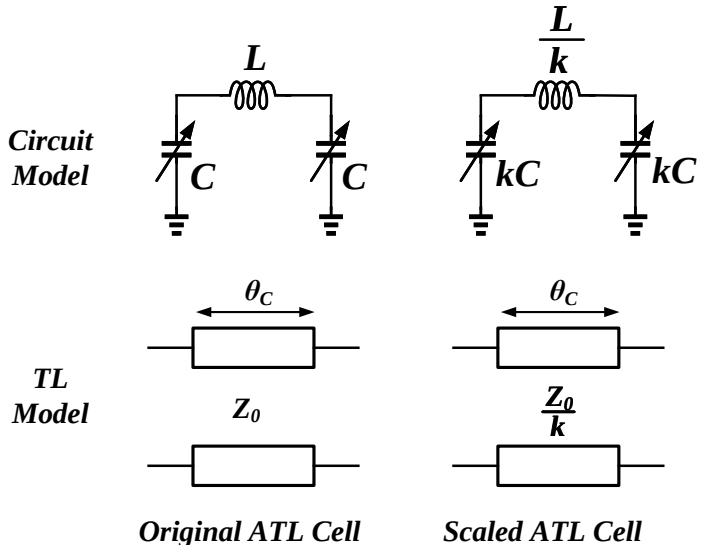


Figure 3.3: Original and scaled π-ATLs and their equivalent TL models.

In order to reduce the size of a π-ATL cell without changing its electrical length, we propose scaling the cell's inductor and varactors as follows:

$$\begin{cases} L_{new} = \dfrac{L}{k} \\ C_{new} = kC \end{cases} \tag{3.7}$$

as shown in Fig. 3.3. Based on (3.3) the new ATL cell will have the same electrical length as the old cell. However, based on (3.6) the characteristic impedance of the new cell is equal to

$$Z_{0new} = \frac{Z_0}{k}. \tag{3.8}$$

To design an area efficient multi-cell π-ATL phase shifter, with proper input and output matching to Z_0, one solution is to cascade multiple scaled ATL cells and use transformers at both ends to convert Z_0/k to Z_0, similar to the technique reported in the design of an area efficient DA [45]. However, the low coupling coefficient, low quality factor, and the size of the on-chip transformers increase the insertion loss and the overall size of the circuit if this method is used for the design of the phase shifters. Instead of using transformers, we suggest scaling down (tapering) the ATL cell sizes from the input and output ports toward the center of a multi-cell TTL phase shifter, as shown in Fig. 3.1(b). If the proposed Tapered TTL phase shifter is properly designed, one can achieve proper input and output impedance matching

while reducing the size of the TTL phase shifter and producing the same phase shift, as in a conventional non-tapered TTL phase shifter.

In the proposed phase shifter, the characteristic impedance of the equivalent transmission lines is scaled down from the outer to the inner cells. One can use the "small reflections theorem" in [34] to properly match the input and output port of the phase shifter to the desired port impedances. If we assume that an N-cell Tapered TTL phase shifter (see Fig. 3.1(b)) has m tapered cells at both sides and n minimum-size cells in the middle, increasing m results in better matching performance while reducing m results in more chip area reduction (recalling that N is constant and equal to $n + 2m$).

Based on the discussed trade-off, we note that there is an optimum value for m which simultaneously leads to acceptable matching performance and considerable chip area efficiency. It should also be noted that finding the optimum number of m is equivalent to finding the optimum distribution for the scaling factors between the tapered cells. The next section provides the analysis for calculating the optimum number of tapered cells and the resulting insertion loss.

3.2 Analysis of Tapered Tunable Transmission Line (TTTL) Based Phase Shifter

To arrive at the design process for the proposed Tapered TTL phase shifter that optimizes the number of cells and size of required cells' inductors, capacitors, and the tapering factor k, the first step is to model the structure using transmission line theory.

By equalizing the B and C elements in (3.2) and (3.1), one can write [46]:

$$L\omega = Z_C \sin\theta_C \tag{3.9}$$

and

$$C\omega = \frac{1}{Z_C}\frac{1-\cos\theta_C}{\sin\theta_C} \tag{3.10}$$

where θ_C and Z_C are the electrical length and characteristic impedance of the cell respectively, and the subscript C indicates the dependency of their values on the

varactors' capacitance. By substituting θ_C from (3.3) into (3.9) and/or (3.10), Z_C can be calculated in terms of L and C as

$$Z_C = \sqrt{\frac{L}{C(2 - LC\omega^2)}}. \tag{3.11}$$

Eqns. (3.3) and (3.11) show that if L and C are, respectively, scaled up and down by the scaling factor of k, as described in (3.7), Z_C will be scaled down with the same scaling factor while θ_C has remained unchanged.

Using the developed transmission line model, in the next subsection an analysis is provided to find the optimum distribution of the scaling factors between m tapered cells of an N-cell Tapered TTL phase shifter. Then, the equations for the calculation of the insertion and return losses of the optimum phase shifter are derived in the following subsection.

3.2.1 Calculation of Optimum Scaling Factor

In a general case of the Tapered TTL phase shifter, illustrated in Fig. 3.4, it is assumed that the proposed phase shifter consists of m tapered cells at the beginning and m tapered cells at the end. The first and the last cells' characteristic impedance (Z_1) is chosen to be equal to Z_0 where their varactors' capacitance is at their mid-range. Consequently, the inductor and capacitance of the varactor of the cells at both ends of the transmission line can be found by equating Z_C to Z_0, where C is equal to C_0.

Moving forward from the second to the m^{th} cells, the inductor/varactor of the $(i+1)^{th}$ cell (where $i = 1, 2, ..., m-1$) is scaled down/up by the scaling factor of k_i from the immediate previous cell, respectively. On the other side, moving backward from the $(N-1)^{th}$ to the $(N-m+1)^{th}$ cell, the inductor/varactor of the $(N-i)^{th}$ cell (where $i = 1, 2, ..., m$) is scaled up/down from the immediate previous cell by the scaling factor of k_i, respectively. There are also $(N-2m)$ ATL cells with minimum size inductor (area) in the middle. Based on that, we define the Maximum Scaling Coefficient (k_{max}) as the product of all scaling factors from outer cells to inner cells:

$$k_{max} = \prod_{i=1}^{m} k_i. \tag{3.12}$$

Consequently, the characteristic impedance of the second to m^{th} cell (Z_i) is defined as

$$Z_i = \frac{Z_1}{\prod_{j=2}^{i} k_{j-1}} \tag{3.13}$$

where $i = 2, 3, ..., m$ and Z_1 is equal to Z_C and obtained from (3.11). The product of Scaling Coefficients (k_is) should gradually change the characteristic impedance of the cells from Z_C to Z_C/k_{max} through the first to the $(m+1)^{\text{th}}$ ATL cell. Conversely, the $(N-m+1)^{\text{th}}$ to $(N-1)^{\text{th}}$ ATL cells' characteristic impedances must change from Z_N/k_{max} to Z_N (See **??**) where $Z_N = Z_1$ if the input and output impedances are equal. Therefore, for those cells, the cell's characteristic impedance can be written as

$$Z_i = \frac{Z_1}{\prod_{j=i}^{N} k_{N-j}} \tag{3.14}$$

where $i = N-m+1, N-m, ..., N-1$.

For the first reflection plane, which is the connection of the input port and the first cell, the partial reflection coefficient, which describes the immediate reflection between two consecutive transmission lines with different characteristic impedances [34], can be written as

$$\Gamma_1 = \frac{Z_1 - Z_0}{Z_1 + Z_0}. \tag{3.15}$$

Additionally, for the second to the m^{th} cell, based on (3.13), the partial reflection coefficient for the plane between two consecutive i and $i+1$ cells, can be expressed as:

$$\Gamma_{i+1} = \frac{Z_{i+1} - Z_i}{Z_{i+1} + Z_i} = \frac{\dfrac{Z_1}{\prod_{j=1}^{i+1} k_j} - \dfrac{Z_1}{\prod_{j=1}^{i} k_j}}{\dfrac{Z_1}{\prod_{j=1}^{i+1} k_j} + \dfrac{Z_1}{\prod_{j=1}^{i} k_j}} = \frac{1 - k_{i+1}}{1 + k_{i+1}} \tag{3.16}$$

where $i = 1, 2, .., m-1$.

For the $(N-m)^{th}$ to the $(N-1)^{th}$ cell, the partial reflection coefficient between

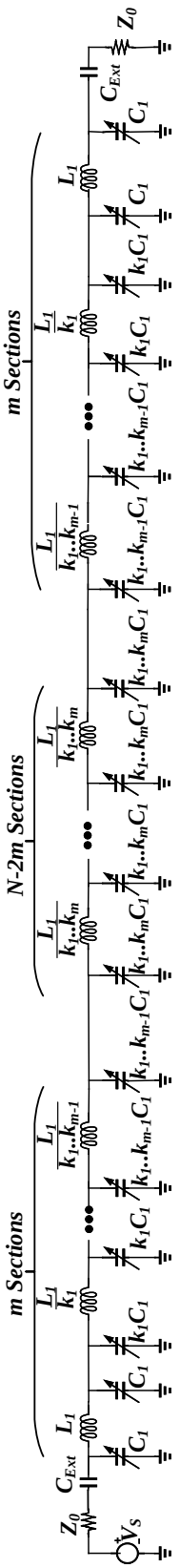


Figure 3.4: Circuit model of an N cascaded π-ATL cells having $2m$ tapered cells with arbitrary scaling factors distribution

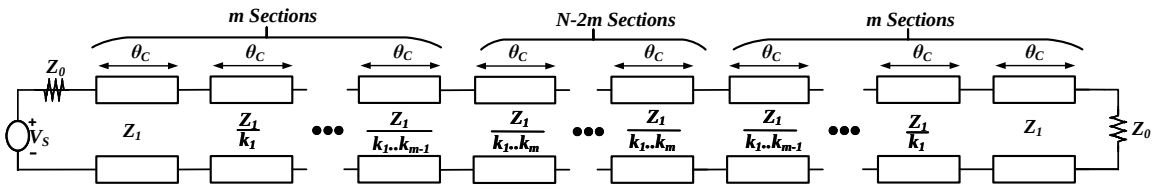


Figure 3.5: Transmission line model of an N cascaded π-ATL cells having $2m$ tapered cells with arbitrary scaling factors distribution

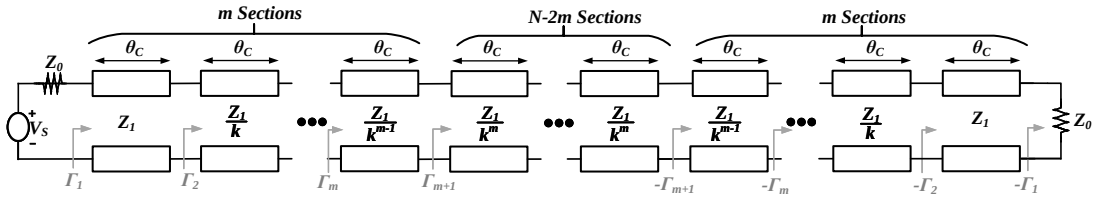


Figure 3.6: N cascaded π-ATL cells having $2m$ tapered cells with optimum scaling factors distribution (partial reflection coefficients are shown)

two consecutive i and $i+1$ cells, based on (3.14), can be calculated by

$$\begin{aligned}\Gamma_i = \frac{Z_{i+1}-Z_i}{Z_{i+1}+Z_i} &= \frac{\dfrac{Z_1}{\prod_{j=i+1}^{N} k_{N-j}} - \dfrac{Z_1}{\prod_{j=i}^{N} k_{N-j}}}{\dfrac{Z_1}{\prod_{j=i+1}^{N} k_{N-j}} + \dfrac{Z_1}{\prod_{j=i}^{N} k_{N-j}}} \\ &= \frac{k_{N-i-1}-1}{k_{N-i-1}+1}\end{aligned} \tag{3.17}$$

where $i = N-m+1, N-m, ..., N-1$. Finally, the partial reflection coefficient at the plane of the connection between the last cell and the output terminal port is equal to:

$$\Gamma_{N+1} = \frac{Z_0 - Z_1}{Z_1 + Z_0}. \tag{3.18}$$

Equations (3.15) to (3.18) show that the partial reflection coefficients for symmetrical planes, which are equidistant from the input and output ports, have the same magnitude and only differ in sign. Finally, the partial reflection coefficients in the planes of the connection of the middle ATL cells, which have the same characteristic impedances, are all equal to zero.

For further processing, we consider the condition that if all the k_i are chosen to be close enough to 1 such that all partial reflection coefficients have a magnitude less than 0.1, the small reflection theorem can be utilized for further simplification of the

problem [34]. Then, the Input Reflection Coefficient (Γ_{in}) can be calculated as

$$\begin{aligned}\Gamma_{in} =&\Gamma_1 + \Gamma_2 e^{-j2\theta} + ... + \Gamma_m e^{-j2(m-1)\theta} + \Gamma_{m+1} e^{-j2(m)\theta} + \\ &\Gamma_{N-m+1} e^{-j2(N-m)\theta} + \Gamma_{N-m+2} e^{-j2(N-m+1)\theta} + ... + \\ &\Gamma_N e^{-j2(N-1)\theta} + \Gamma_{N+1} e^{-j2(N)\theta}\end{aligned} \tag{3.19}$$

Up to now, we assumed that the ATL cells are lossless. However, in the practical realization of an ATL cell, the cell's inductor and both varactors have a limited quality factor and introduce loss to the network. For computing this loss, one can add series and parallel resistances to inductor and capacitors of the lumped model of each cell (Fig. 3.2(b)), respectively, and make complicated analysis based on lumped element ABCD matrices. For easier calculations, we can use the low-loss transmission line model. In a low-loss transmission line, it is assumed that the electrical length (θ_C) and characteristic impedance (Z_C) are remained unchanged while each traveling voltage signal, in addition to the $e^{-j\theta_C}$ phase shift, is attenuated by a factor of $e^{-\alpha}$. Based on this definition, for each ATL cell in the proposed phase shifter shown in Fig. 3.5, we introduce an attenuation factor $e^{-\alpha_j}$ where $j = 1, 2, ..., N$. It should be noted that similar cells should have similar attenuation factors. As a result, by assuming such attenuation factors, (3.19) is changed into

$$\begin{aligned}\Gamma_{in} =&\Gamma_1 + \sum_{i=2}^{m+1} [\Gamma_i e^{-j2(i-1)\theta} \prod_{j=1}^{i-1} e^{-2\alpha_{j-1}}] - \\ &\Gamma_{m+1} e^{-j2(N-m)\theta} \prod_{j=1}^{N-m} e^{-2\alpha_j} - \\ &\sum_{i=1}^{m} [\Gamma_{m-i+1} e^{-j2(N-m+i)\theta} \prod_{j=1}^{N-m+i} e^{-2\alpha_j}].\end{aligned} \tag{3.20}$$

Eq. (3.20) shows that the reflections from the planes that are closer to the load side experience more loss than the reflections from the first cells. As a consequence, we can only keep Γ_1 and the first summation terms in (3.20) and rewrite it as

$$\Gamma_{in} \approx \Gamma_1 + \sum_{i=2}^{m} [\Gamma_i e^{-j2(i-1)\theta} \prod_{j=1}^{i-1} e^{-2\alpha_j}]. \tag{3.21}$$

The magnitude of the input reflection coefficients calculated in (3.21) is maximized when all the $e^{-j2(i-1)\theta}$ terms are assumed to be equal to 1, requiring that $2(i-1)\theta =$

$2k\pi$ for all i from 1 to m. Then, for the maximum absolute value of the Input Reflection Coefficient ($|\Gamma_{in,max}|$) we can write:

$$|\Gamma_{in,max}| \leq \sum_{i=1}^{m} |\Gamma_i| \tag{3.22}$$

knowing that all the $e^{-2\alpha_j}$ factors are smaller than one. Substituting the partial reflection coefficients from (3.16) and (3.17) in (3.22), $|\Gamma_{in,max}|$ can be written as

$$|\Gamma_{in,max}| \leq |\sum_{i=1}^{m} \frac{1-k_i}{1+k_i} + \Gamma_1|. \tag{3.23}$$

If we assume that the first and the last cells are properly matched to the source and load impedances, Γ_1 is negligible in comparison to the first term of (3.23). As a consequence, to minimize the $|\Gamma_{in,max}|$, the following function should be minimized:

$$\sum_{i=1}^{m} \frac{k_i - 1}{k_i + 1} = \frac{m(m+1)}{2} - 2\sum_{i=1}^{m} \frac{1}{k_i + 1}. \tag{3.24}$$

Knowing that the product of all the k_i is equal to k_{max} according to (3.12), one can conclude that (3.24) will be minimized if all the k_i are equal, i.e.

$$k_1 = k_2 = ... = k_m = \sqrt[m]{k_{max}}. \tag{3.25}$$

The above analysis is also valid for Γ_{out}. This means that input and output return losses will be minimized if the cells are scaled uniformly (same scaling factor of $\sqrt[m]{k_{max}}$) from the input and output ports toward the center. The transmission line model of the optimum phase shifter is shown in Fig. 3.6.

3.2.2 Calculation of Loss

The total loss of the proposed optimum phase shifter (Fig. 3.6) is caused by the loss due to the limited quality factor of the cell's elements ($IL_{atn.}$) and the loss by the mismatch at the input port (ML):

$$S_{21} = \frac{1}{ML \times IL_{atn}}. \tag{3.26}$$

where IL_{atn} can be expressed as

$$IL_{atn} = \frac{1}{\prod_{i=1}^{N} e^{-\alpha_i}} \tag{3.27}$$

and ML can be written as [47]

$$ML = \frac{1}{1 - |\Gamma_{in}|^2} \tag{3.28}$$

and where Γ_{in} is calculated by

$$\Gamma_{in} \approx \Gamma_1 + \frac{1 - \sqrt[m]{k_{max}}}{1 + \sqrt[m]{k_{max}}} \sum_{i=2}^{m} [e^{-j2(i-1)\theta} \prod_{j=1}^{i-1} e^{-2\alpha_j}], \tag{3.29}$$

which is obtained from (3.21) while considering the optimum design of the tapered cells given by (3.25).

3.3 Design Procedure

In this section, a step-by-step procedure for the design of the proposed Tapered TTL phase shifters is presented. The main aim of the phase shifter design is to achieve the specified phase shift range over the entire frequency band from the lowest operating frequency (f_l) to the highest operating frequency (f_u), while the $Area/|S_{21}|$ (as a criterion for efficient design) is minimized and, simultaneously, the return loss remains below an acceptable range. The output of the design procedure must ultimately define parameters like the total number of cells (N), the number of tapered cells ($2m$), and the physical specifications of the inductors and varactors of the tapered and middle minimum-sized cells. In Section 3.2, we have shown that the scaled ATL cell and the original cell have the same electrical length. Therefore, one can conclude that in designing a phase shifter with a specified desired amount of phase shift, both the Tapered TTL phase shifter and its conventional counterpart should have the same total number of cells. Consequently, the design procedure can begin by designing a conventional TTL phase shifter. Once the number of cells and electrical length of each cell are determined, the Tapered TTL phase shifter can be designed by finding the remaining parameters including the number of tapered cells (m) and the scaling factor of the minimum sized cells (k_{max}).

3.3.1 Design of a Non-Tapered Conventional TTL Phase Shifter

Considering that the varactors of a cell have their mid-range capacitance (C_0), one can use (3.3) to show that at the operating frequency (f), the relationship between

the mid-range electrical length of the cell (θ_{0f}) and cell's components can be described as

$$LC_0\omega^2 = 2sin^2(\frac{\theta_{0f}}{2}), \tag{3.30}$$

where L is the inductance of the cell's inductor. If we define the reference frequency (f_{ref}) as the frequency at which the cell's characteristic impedance is matched to the impedance of the input and output ports (Z_0) with the varactors at their mid-range, substituting (3.30) in (3.11) shows that

$$\sqrt{\frac{L}{2C_0}} = Z_0 \cos\frac{\theta_{0f_{ref}}}{2}. \tag{3.31}$$

Tuning the varactors' bias condition, the varactor's capacitance varies according to $C = \eta C_0$ where η's range is

$$\sqrt{\frac{C_{min}}{C_{max}}} \leq \eta \leq \sqrt{\frac{C_{max}}{C_{min}}}. \tag{3.32}$$

Substituting the results of (3.30) and (3.31) in (3.11), one can show that the cell's characteristic impedance (Z_C), for any arbitrary varactors' capacitance and operating frequency, can be calculated as

$$Z_C(\eta, f) = \frac{Z_0 \cos\frac{\theta_{0f_{ref}}}{2}}{\sqrt{\eta(1 - \eta sin^2(\frac{\theta_{0f_{ref}}}{2})(\frac{f}{f_{ref}})^2)}}. \tag{3.33}$$

This equation shows that at the frequencies other than f_{ref}, even if all varactors are in their mid-range ($\eta = 1$), there will be a mismatch at the input and the output ports. Since we know that in practical design the attenuation loss will be increased at the higher frequencies, defining $f_{ref} = f_u$ and $\theta_0 = \theta_{0f_u}$, we minimize the mismatch loss at the higher frequency parts of operating bandwidth and, as a consequence, create a balance in the total insertion loss. Similarly, using (3.3), the phase shift of a cell for any arbitrary varactors' capacitance (bias condition), in the operating frequency range, can be expressed as

$$\theta(\eta, f) = \arccos(1 - 2\eta sin^2(\frac{\theta_{0f_u}}{2})(\frac{f}{f_u})^2). \tag{3.34}$$

As shown in (3.34), the cell's phase shift is increased by increasing the frequency, hence the number of cells is determined by the maximum achievable phase shift at the lowest frequency ($\Delta\theta_{max@f_l}$) of a cell. Using (3.34), one can easily show that $\Delta\theta_{max@f_l}$ is equal to

$$\begin{aligned}\Delta\theta_{max@f_l} = &\arccos\left(1-2\sqrt{\frac{C_{min}}{C_{max}}}sin^2(\frac{\theta_{0f_u}}{2}))(\frac{f_l}{f_u})^2\right)- \\ &\arccos\left(1-2\sqrt{\frac{C_{max}}{C_{min}}}sin^2(\frac{\theta_{0f_u}}{2})(\frac{f_l}{f_u})^2\right).\end{aligned} \tag{3.35}$$

Using (3.35), the graph of $\Delta\theta_{max@f_l}$ as a function of θ_{0f_u} for different values of C_{max}/C_{min} (1.5, 2, 3 and 3.5) is shown in Fig. 3.7. As expected, the graph confirms that having a greater C_{max}/C_{min} results in a greater phase shift. Moreover, it shows that increasing θ_{0f_u}, which requires larger inductor and C_0 sizes, leads to an increasing value of $\Delta\theta_{max@f_l}$. It should be noted that the maximum achievable amount of C_{max}/C_{min} depends on the target semiconductor technology. For instance, in our 65-nm CMOS process, C_{max}/C_{min} is limited to 3 for varactors with acceptable quality factor ($Q \geq 15$). Consequently, the only way of obtaining larger $\Delta\theta_{max@f_l}$ for a cell is to increase θ_{0f_u}. However, we will show later that using a larger inductor and larger varactors to increase θ_{0f_u} degrades the matching condition as we deviate from f_{ref} and C_0. As a result, the maximum available phase shift of a cell is limited. Therefore, to achieve the desired phase shift, multiple cells must be cascaded. The required number of cells (N) can be computed as

$$N = floor[\frac{Desired\ Phase\ Shift}{\Delta\theta_{max@f_l}}] + 1. \tag{3.36}$$

where the $floor$ function returns the largest integer which is less than the operand.

Now, to investigate how choosing larger θ_{0f_u} degrades matching condition in an N-cell conventional TTL phase shifter, we need to calculate the return loss as a function of θ_{0f_u}. In such a phase shifter, all of the partial reflection coefficients (Γ_i's), except $i = 1$, are equal to zero. However, using (3.33), Γ_1 can be written as

$$\begin{aligned}\Gamma_1(\eta, f) = &\frac{Z(\eta,f) - Z_0}{Z(\eta,f) + Z_0} = \\ &\frac{\cos\frac{\theta_{0f_u}}{2} - \sqrt{\eta(1-\eta sin^2(\frac{\theta_{0f_u}}{2})(\frac{f}{f_u})^2)}}{\cos\frac{\theta_{0f_u}}{2} + \sqrt{\eta(1-\eta sin^2(\frac{\theta_{0f_u}}{2})(\frac{f}{f_u})^2)}}.\end{aligned} \tag{3.37}$$

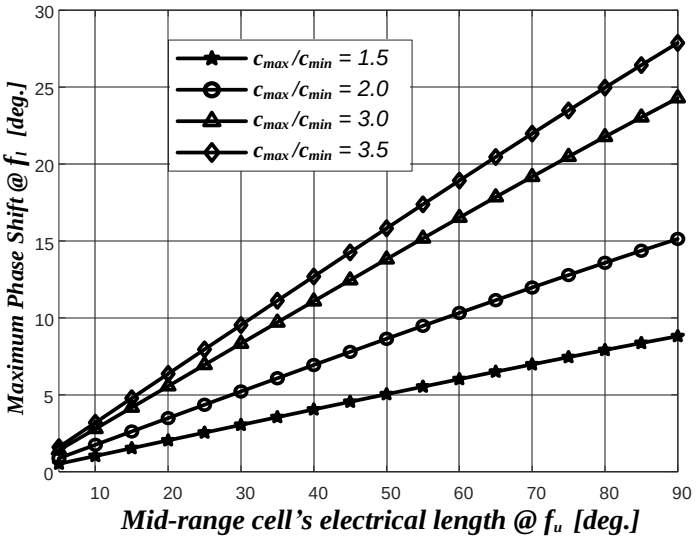


Figure 3.7: The maximum phase shift at the lowest frequency ($\Delta\theta_{max@f_l}$) vs. θ_{0f_u} in a conventional ATL cell for different values of C_{max}/C_{min}.

It can be shown that for a wideband design ($f_u/f_l \geq 2$) and the practical value of varactors' range ($C_{max}/C_{min} \leq 4$), the greatest mismatch occurs at the lowest frequency (f_l), with $\eta = \sqrt{C_{max}/C_{min}}$. Consequently, the maximum value of Γ_1 can be calculated as

$$\Gamma_{1_{(max)}} = \frac{\cos\frac{\theta_{0f_u}}{2} - \sqrt{\sqrt{\frac{C_{max}}{C_{min}}} - \frac{C_{max}}{C_{min}} sin^2(\frac{\theta_{0f_u}}{2})(\frac{f_l}{f_u})^2}}{\cos\frac{\theta_{0f_u}}{2} + \sqrt{\sqrt{\frac{C_{max}}{C_{min}}} - \frac{C_{max}}{C_{min}} sin^2(\frac{\theta_{0f_u}}{2})(\frac{f_l}{f_u})^2}}. \tag{3.38}$$

There are two reflections at the input port of a TTL phase shifter. One reflection is due to the mismatch between the characteristic impedance of the first cell and the input port and the other is the reflection caused by the mismatch between the last cell and the output port which travels back to the input. In the practical design, even in low-loss cells, the second reflection term experiences enough loss which makes the second reflection negligible in comparison to the first one. As a result, considering $e^{-\alpha}$ as the attenuation factor of each cell, the input reflection coefficient (Γ_{in}) calculated from (3.19) can be approximated as

$$\Gamma_{in} \approx \Gamma_1 - \Gamma_1 e^{-j2(N)\theta} e^{-2(N)\alpha}. \tag{3.39}$$

As can be seen, the attenuation factor is influenced by a power of $2N$. This implies that even if the cells are low-loss (e.g., $e^{-\alpha} = 0.9$), for N values greater than or equal to 10, the impact of the second term diminishes significantly compared to the first term. Consequently, Equation (3.39) can be further simplified to

$$\Gamma_{in} \approx \Gamma_1. \tag{3.40}$$

The maximum reflection coefficient (S_{11max}) of the TTL phase shifter in dB scale can be expressed as [34]

$$S_{11max}(dB) = -R.L = 20\log\left(|\Gamma_{in_{max}}|\right) = 20\log\left(|\Gamma_{1_{(max)}}|\right), \tag{3.41}$$

where $\Gamma_{1_{(max)}}$ is obtained from (3.38). One of the most important criteria in the phase shifter design is that S_{11} should be below an acceptable value for all varactors' bias conditions and over the entire operating frequency range. Considering that we assumed the phase shifter is low loss and of a conventional type, $S_{11max} \leq -20\ dB$ can be considered as a standard design criterion. Consequently, for a given value for C_{max}/C_{min} and the desired fractional operational bandwidth (f_u/f_l), one can plot S_{11} as a function of θ_{0f_u} to find the acceptable range of θ_{0f_u}. Fig. 3.8 shows a sample of such a graph by assuming that in the desired design $f_u/f_l = 2$ and $C_{max}/C_{min} = 3$ in the target semiconductor technology. It can be seen that for S_{11} to remain below $-20\ dB$, θ_{0f_u} should vary only between

$$22(deg.) \leq \theta_{0f_u} \leq 53(deg.). \tag{3.42}$$

Evaluating (3.9) at f_u and at the varactors' capacitance mid-range value shows that

$$L = \frac{Z_0 \sin\left(\theta_{0f_u}\right)}{\omega} \tag{3.43}$$

which shows that the inductance value of the cell is proportional to $sin(\theta_{0f_u})$. If we assume the size of an on-chip inductor is proportional to its inductance value, the chip area of a conventional TTL phase shifter can be approximated by N times the inductors' size ($N \times \sin\left(\theta_{0f_u}\right)$) once normalized by the area of a 90 degree cell (Z_0/ω). This expression provides an approximation of the chip area which is needed for the optimum design of the phase shifters. For an area-efficient TTL phase shifter

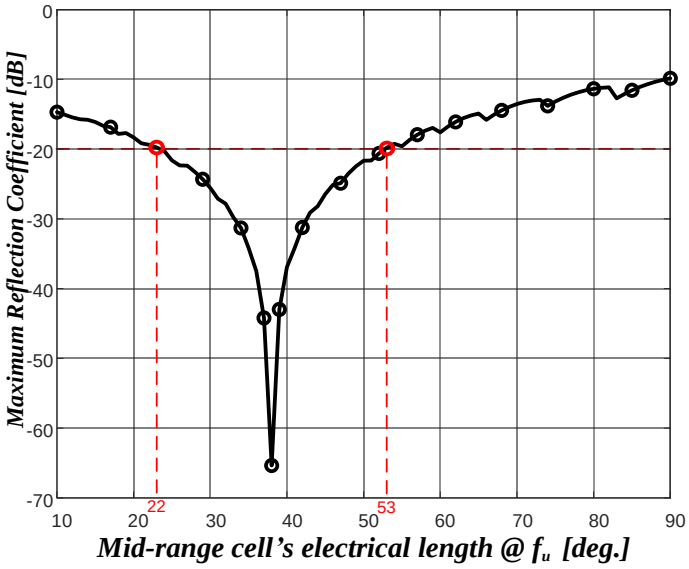


Figure 3.8: The maximum reflection coefficient (S_{11max}) of an 180 degree phase shifter as function of θ_{0f_u} in a conventional low-loss TTL phase shifter.

design while considering its RF performance at the same time, one can introduce the following Figure of Merit ($FOM_{lowloss}$)

$$\begin{aligned} FOM_{lowloss} = \frac{Area}{|S_{21_{max}}|} &= N \times \sin(\theta_{0f_u}) \times ML_{min} \\ &= \frac{N \times \sin(\theta_{0f_u})}{1 - |\Gamma_{1_{(max)}}|^2}. \end{aligned} \tag{3.44}$$

Minimizing (3.44) results in the most area-efficient design with the minimum insertion loss. For the mentioned technology limitations in our target technology ($C_{max}/C_{min} = 3$), to achieve a total phase shift of 180 degree over an octave bandwidth ($f_u/f_l = 2$), the above-defined $FOM_{lowloss}$ is plotted as a function of θ_{0f_u} in Fig. 3.9. The figure shows that the introduced FOM is a descending function of θ_{0f_u}. As a result, for the optimum design, considering the allowable range of θ_{0f_u} which is defined in (3.42), θ_{0f_u} should be equal to 53 degrees. Using (3.35) and (3.36) shows that in that case the number of needed cells (N) for 180 degree phase shift is equal to 13. In addition, after finding the θ_{0f_u} and N, the values of the cell's L and C_0 can be calculated by

$$\begin{aligned} L &= \frac{Z_0 \sin(\theta_{0f_u})}{2\pi f_u} \\ C_0 &= \frac{\tan(\frac{\theta_{0f_u}}{2})}{2\pi f_u Z_0}. \end{aligned} \tag{3.45}$$

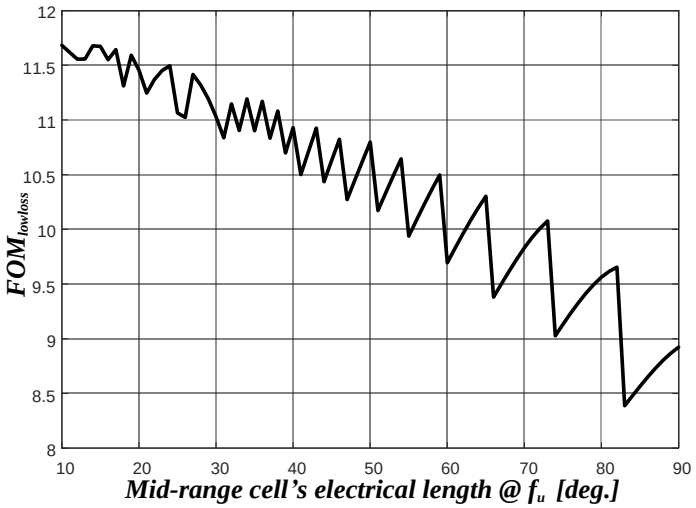


Figure 3.9: $FOM_{lowloss}$ of an 180 degree phase shifter as a function of θ_{0f_u} in a conventional lossless TTL phase shifter.

In the lossy case, as shown in (3.26), the insertion loss, in addition to the mismatch part (ML), has an attenuation part (IL_{atn}) as well. Consequently, the FOM which is calculated in (3.44), can be changed to

$$\begin{aligned} FOM_{Lossy} &= \frac{N \times \sin(\theta_{0f_u})}{|S_{21_{max}}|} \\ &= \frac{N \times \sin(\theta_{0f_u})}{(1 - |\Gamma_{1_{(max@f_u)}}|^2) \times (e^{-\alpha})^N}. \end{aligned} \tag{3.46}$$

It should be noted that the attenuation part ($e^{-\alpha}$) of the insertion loss is dominant, particularly for ATLs implemented on-chip and it is maximum at f_u. The attenuation constant ($e^{-\alpha}$) is a parameter that depends on the target semiconductor technology. Therefore, developing an analytical expression for FOM_{Lossy} is not a straightforward task. Consequently, the practical approach to account for the attenuation loss will be designed by iteration. In the first step of the design-by-iteration method, it is assumed that the ATL cells are low-loss. Therefore, the initial values for N and θ_{0f_u} are found by minimizing $FOM_{lowloss}$, defined in (3.44), while keeping $S_{11} \leq -20\ dB$. Based on the obtained value for θ_{0f_u}, the initial values of L and C_0 of the ATL cell are calculated by using (3.45). In the second step, the ATL cell constructed with L and C_0 is simulated using the models provided in the design kit of the target semiconductor technology to find the attenuation constant ($e^{-\alpha}$) of the cell. Taking the loss of cell

into account, new values of N and θ_{0f_u} can be found through an optimization process that minimizes FOM_{lossy}, defined in (3.46), while keeping $S_{11} \leq -20\ dB$. Using the new value for θ_{0f_u}, the values of L and C_0 are recalculated using (3.45). The procedure is continued by repeating the second step with new calculated values of L and C_0. Simulating ATL cell with the models of L and C_0 results in a new attenuation constant ($e^{-\alpha}$). Then, minimizing FOM_{lossy} (while keeping $S_{11} \leq -20\ dB$) by using new attenuation constant generates new values for N and θ_{0f_u} which must be used to repeat the second step of the process again. Finally, the iteration must be continued until N (or equivalently θ_{0f_u}) is converged to a single value.

3.3.2 Design of a Tapered TTL Phase Shifter

Hence, the number of total cells (N) and initial electrical length (θ_{0f_u}) of the proposed phase shifter and the conventional one are identical, the design equations for θ_{0f_u} and N, which are developed in the previous subsection, can be used in the design of the Tapered TTL phase shifter as well. However, as discussed in Section 3.2, in the Tapered TTL phase shifter, there are extra reflections between tapered cells which increase the mismatch part of the insertion loss (ML) comparing to the conventional one. In other words, while in the Tapered TTL phase shifter the same amount of the phase shift is produced, the goal is to implement the phase shifter in a smaller chip area at the cost of the higher return loss. Accordingly, in order to make a compromise between return loss performance and chip area efficiency in the proposed Tapered TTL phase shifter, the acceptable return loss is relaxed to $S_{11} \leq -10\ dB$ to accommodate for extra reflections.

In this section, like the conventional TTL phase shifter design, we assume that the reflection from the cells, which are closer to the output port, are considerably attenuated and do not reach the input port. Therefore, assuming that the proposed N-cell Tapered TTL phase shifter has m tapered cells at both input and output sides, Γ_{in} can be rewritten as

$$\Gamma_{in} = \sum_{i=1}^{m+1} \Gamma_i e^{-j2(i-1)\theta}. \tag{3.47}$$

Knowing that for $i = 2, 3, ..., N$, in any varactors' bias condition, the partial reflection

coefficients (Γ_i) still remain the same as those calculated in (3.29)

$$\Gamma_i = \frac{\sqrt[m]{k_{max}} - 1}{\sqrt[m]{k_{max}} + 1}, \tag{3.48}$$

because all the varactors are scaled uniformly Substituting (3.48) in (3.47), the input reflection coefficient can be written as

$$\Gamma_{in} = \Gamma_1 + \frac{\sqrt[m]{k_{max}} - 1}{\sqrt[m]{k_{max}} + 1} \sum_{i=2}^{m+1} e^{-j2(i-1)\theta}, \tag{3.49}$$

where the second term represents the effect of the extra reflections. As can be seen, this term is a function of the electrical length of the cell, the number of tapered cells (m), and the scaling factor of minimum-sized cells (k_{max}). We know from (3.34) that the cell's electrical length (θ) varies in the following interval:

$$\begin{aligned} &\arccos\left(1 - 2\sqrt{\frac{C_{min}}{C_{max}}} sin^2(\frac{\theta_{0f_u}}{2})\right)(\frac{f_l}{f_u})^2 \leq \theta \leq \\ &\arccos\left(1 - 2\sqrt{\frac{C_{min}}{C_{max}}} sin^2(\frac{\theta_{0f_u}}{2})\right) + \Delta\theta_{max}. \end{aligned} \tag{3.50}$$

and the maximum number of tapered cells (m_{max}) can be found by

$$m_{max} = \begin{cases} \frac{N}{2} & N\ is\ even \\ \frac{N-1}{2} & N\ is\ odd \end{cases} . \tag{3.51}$$

We are looking for the optimum values of m and k_{max}, to keep return loss over 10 dB (or equivalently $|\Gamma_{in}| \leq 0.3$) for all possible values of the cell's electrical length and simultaneously minimizing $Area/IL$ ratio.

Consequently, for any given values of m, sweeping θ in the interval defined in (3.50), one can record the $|\Gamma_{in_{max}}|$ as a function of k_{max}. Then, by intersecting the horizontal line of $|\Gamma_{in}| = 0.3$ ($|S_{11}| \leq -10\ dB$) with $|\Gamma_{in_{max}}|$ graphs, the maximum allowable value of k_{max} for each value of m can be extracted. In Fig. 3.10, the $|\Gamma_{in_{max}}|$ graphs for the Tapered TTL phase shifter, which produce the equivalent phase shift of the conventional phase shifter, discussed in the previous subsection, are plotted. The figure shows for the number of tapered cells (m) of $2, 3, 4, 5$ and 6, the maximum allowable scaling factor of the minimum sized cells (k_{max}) should be $1.4, 1.45, 1.8, 2.25$ and 2.6, respectively. Furthermore, similar to calculations in Section 3.2, to ensure that using small reflection theorem is valid, it is assumed that the partial reflection

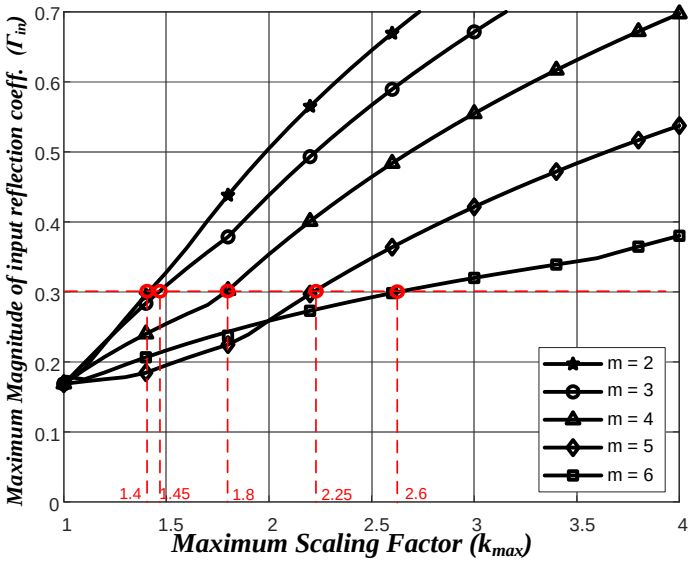


Figure 3.10: Magnitude of input reflection coefficient ($|\Gamma_{in_{max}}|$) versus k_{max} for $m = 2, 3, 4, 5$ and 6 where $\theta_{0f_u} = 53^o$ and $N = 13$.

coefficients are small ($|\Gamma_i| \leq 0.1$). Substituting (3.25) in (3.16), the condition that the partial reflection coefficients between tapered cells are small, results in

$$|\Gamma_{i+1}| = \frac{\sqrt[m]{k_{max}} - 1}{\sqrt[m]{k_{max}} + 1} \leq 0.1, \tag{3.52}$$

where $i = 1, 2, ...m$. Therefore, any pair of k_{max} and m values which are extracted from the Fig. 3.10 must be checked to satisfy (3.52) as well.

Finding the possible pair values of m and k_{max} from (Fig. 3.10), the characteristic impedance of each cell (Z_i) can be calculated as

$$Z_i = \begin{cases} Z_0 & 1^{st} \; and \; last \; cells \\ \frac{Z_0}{\sqrt[m]{k_{max}^i}} \quad (i=2,...,m-1) & Tapered \; cells \\ \frac{Z_0}{k_{max}} & Minimum - sized \; cells \end{cases} . \tag{3.53}$$

As the size of an on-chip inductor is proportional to its inductance value, the chip area of a Tapered TTL phase shifter can be estimated by the summation of cells' inductance values. Based on (3.53), for each pair of m and k_{max}, the area of the proposed Tapered TTL phase shifter, after eliminating common factors of $\sin(\theta_{0f_u})$ and Z_0, can be estimated as

$$Area \; \propto \; [2 + 2 \times \sum_{i=1}^{m-1} \frac{1}{\sqrt[m]{k_{max}^i}} + (N - 2m) \times \frac{1}{k_{max}}]. \tag{3.54}$$

Table 3.1: Area estimation for m and k_{max} pairs extracted from Fig. 3.10

m	k_{max}	$Area$	$\|\Gamma_{i+1}\|(i = 2, 3, ..., m_{max})$
2	1.4	8.9	0.03
3	1.45	8.3	0.03
4	1.8	7.5	0.05
5	2.25	6.9	0.07
6	2.6	7.1	0.09

Since all possible pairs of m and k_{max} satisfy the requirement of the maximum return loss, the most efficient design will be the one that minimizes the area.

For the assumed case (a 13-cell 180 degree phase shifter), the values of the estimated area for each pair of m and k_{max} (extracted from Fig. 3.10), are summarized in Table 3.1. As can be seen, the computed $|\Gamma_{i+1}|$ for $i = 1, 2, ..., m_{max}$ (see (3.52)) shows that the partial reflection coefficients between tapered cells for all pairs of m and k_{max}, are small enough to satisfy (3.52). Consequently, based on the estimated area, the optimum values for m and k_{max} are 5 and 2.25, respectively. Knowing the values of m and k_{max}, similar to TTL phase shifter, the inductance (L) and mid-range capacitance (C_0) values of each cell can be calculated by using (3.45) where Z_0 is replaced by each cell's characteristic impedance (Z_i) obtained in (3.53). In the lossy case of the tapered phase shifter as shown in (3.29), unlike the conventional one, the input reflection coefficient is also affected by the cell's attenuation factor ($e^{-\alpha_j}$). Similar to the conventional case, $e^{-\alpha_j}$ of cells depends on the target semiconductor technology and should also be extracted by simulating the real cells in a proper CAD tool. Therefore, for accounting attenuation of cells, the design process of Tapered TTL phase shifter should be iterative. It means that in the first step m, k_{max} and consequently L and C_0 of the cells should be computed by minimizing (3.54) while assuming that the cells are lossless. Then, constructed cells should be simulated in a proper CAD tool which provides the target semiconductor technology models to extract $e^{-\alpha_j}$ values. As the maximum insertion loss is mostly determined by the high-frequency attenuation factor, the $e^{-\alpha_j}$ factors should be extracted at f_u. In the next step, the input reflection coefficient must be calculated by (3.29). Similar to the

case of lossy conventional TTL phase shifter, a FOM can be defined as

$$FOM_{lossy} = Area \times IL_{atn} = \frac{2 + 2 \times \sum_{i=1}^{m-1} \frac{1}{\sqrt[m]{k_{max}^i}} + (N - 2m) \times \frac{1}{k_{max}}}{\prod_{j=1}^{N} e^{-\alpha_j}}. \quad (3.55)$$

After running simulations for different pairs of m and k_{max}, the pair that minimizes the (3.55) should be selected for the final design.

3.4 Ku/K/Ka Band Tapered TTL Phase Shifter

As a Tapered TTL phase shifter example, the complete design process, simulation, fabrication, and measurement results of a Ku/K/Ka Band Tapered TTL phase shifter which provides continuous phase shift up to a maximum of 180 degree, are presented in this section.

3.4.1 Design of a Ku/K/Ka Band Tapered TTL Phase Shifter

The proposed phase shifter is designed to provide 0 to 180 degree phase shift continuously over the 16.5 (f_l) to 33 GHz (f_u) frequency band. A standard 65-nm CMOS technology is chosen for the implementation of the proposed phase shifter.

As mentioned in the previous section, the first step of the design procedure is designing a conventional TTL phase shifter. For the chosen 65-nm CMOS technology, C_{max}/C_{min} is limited to 3 for a minimum quality factor of 15.

Using the method described in Section 3.3.1, we first find optimum values of $N = 13$ and the corresponding $\theta_{0f_u} = 53$ degrees for the low-loss design. The corresponding cell, constructed with L equal to $237.5pH$ and C_0 equal to $52fF$, is implemented using the models provided in the design kit. The simulation results show that for the 50Ω cell with $\theta_{0f_u} = 53^o$, the attenuation factor ($e^{-\alpha}$) is equal to 0.842. For the lossy case, we need to find new values for N and θ_{0f_u} that minimize the FOM defined in (3.46) via an optimization process. As shown in Table 3.2, in this case the optimum values for θ_{0f_u} and N are equal to 59 degree and 11, respectively. Based on these values, the cell's inductance value (L) and varactors' mid-range capacitance (C_0) are optimized to $315pH$ and $61fF$, respectively.

Table 3.2: Design table for matched cells in conventional TTL phase shifter in 65 nm cmos Technology

L [pH]	C_0 [fF]	θ_0 [$deg.$] @33 GHz	$\Delta\theta_{max}$ [$deg.$] @16.5 GHz	N	Γ_1 @33 GHz	$e^{-\alpha}$ @33 GHz	IL_{total} [dB] @33 GHz	FOM_{lossy}
210	**40.7**	43	12.5	**15**	0.07	0.863	9.6	**93.7**
262.5	**50.9**	51	14.5	**13**	0.1	0.842	9.8	**94.1**
290.5	**54.8**	52	15.5	**12**	0.11	0.832	9.6	**90.2**
315	**61**	59	17	**11**	0.12	0.822	9.4	**82.6**
350	**67.8**	68	19	**10**	0.15	0.79	10.3	**100.2**
385	**74.6**	79	20.3	**9**	0.29	0.763	11	**110.3**

Table 3.3: Attenuation factor for cells with different Characteristic Impedance in 65 nm cmos Technology

k_{max}	Z_{C_0} [Ω]	L [pH]	C_0 [fF]	$e^{-\alpha}$ @ 33GHz
1	50	315	61	**0.822**
1.5	33.33	210	91.5	**0.823**
2	25	157.5	122	**0.827**
2.5	20	126	152.5	**0.828**
3	16.8	105	183	**0.825**
4	12.5	78.7	244	**0.823**

Knowing the results of the conventional design ($N = 11$ and $\theta_{0f_u} = 59^o$), the process of the low-loss tapered design is started by extracting initial values for k_{max} and m, without considering the cells' attenuation factor ($e^{-\alpha_j}$). Simulating several scaled cells with different scaling factors (k_{max}) in the target semiconductor technology shows that the attenuation factor is found to be approximately the same for all of them (see Table 3.3). Consequently, the process of finding optimum values for k_{max} and m can be directly started by calculating $|\Gamma_{in_{max}}|$ through (3.29), where all ($e^{-\alpha_j}$) are equal to 0.822. In Fig. 3.11, for a different number of tapered cells ($m = 2, 3, 4$ and 5), the maximum magnitude of the phase shifter's input reflection coefficient is plotted as a function of k_{max}. Considering the return loss of better than 10 dB, the maximum allowable k_{max} for each value of m is extracted from Fig. 3.11 and are given in Table 3.4. Based on these results, the optimum design for the proposed Tapered TTL phase shifter, the outer cells, at both input and output sides, must be designed with the inductor and varactor values corresponding to the matched cell (50Ω) while the second to the fourth outer cells (at both sides) are scaled by the factors of $\sqrt[4]{2.25}$,

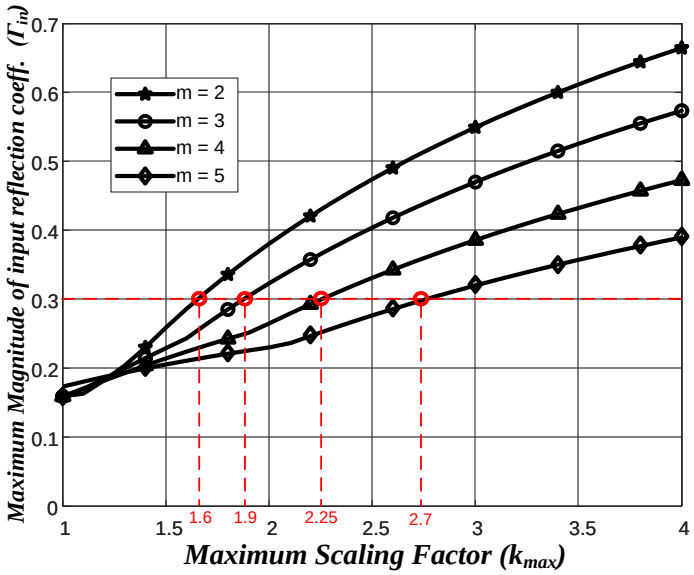


Figure 3.11: Magnitude of input reflection coefficient at $\theta_0 f_u$ versus k_{max} for $m = 2, 3, 4$ and 5 for the 180 degree, Ku/K/Ka band, 11-cell Tapered TTL phase shifter.

Table 3.4: Extracted pairs of m and k_{max} in 65nm CMOS Technology for Return loss better than 10 dB and estimated FOM

m	k_{max}	FOM_{Lossy}
2	1.75	64.9
3	1.85	66.2
4	2.25	63.8
5	2.75	64

$\sqrt[4]{2.25^2}$ and $\sqrt[4]{2.25^3}$, respectively. The remaining three inner cells are all designed with the minimum size which is scaled by the factor of 2.25 from the first and the last cells.

3.4.2 Tape-out and Fabrication

In both conventional and Tapered TTL phase shifters, the inductors are implemented on the topmost metal layer (Metal 9) to obtain the highest quality factor possible. All of the inductors of the conventional TTL phase shifter have the same inductance value of 282 pH. To make a compact floor plan for the phase shifter (as shown in Fig. 3.12), the first inductor is implemented with a 9 um wide Metal 9 trace with 1.5 turns and the inner radius of 23.2 um. All other inductors have the same width but they have 1.75 turns and their inner radii are equal to 18.5 um. The number of

Table 3.5: Physical dimensions of the cell inductors and varactors in the fabricated Tapered TTL phase shifter

Cell's No.	Inductor Parameters			Varactor Parameters	
	T	$R\ [um]$	$L\ [pH]$	G	B
1	1.75	15	210	2	15
2 or 10	1.25	19.5	160	2	19
3 or 9	1.25	15	123	2	25
4 or 8	0.75	22.3	89	2	34
5, 6 or 7	0.75	15.5	65	2	45
11	1.5	18.5	210	2	15

groups (G) of all varactors in the conventional phase shifter is equal to 2. In each group, the number of fingers (B) is equal to 12 and the width (W) and length per finger (L) are equal to 1.1 um and 200 nm, respectively.

In the Tapered TTL phase shifter, the trace width of all inductors in all cells equals to 9 um. Moreover, the length per finger (L) and the width per finger (W) of the varactors are identical and equal to 200 nm and 1 um, respectively. For the minimum-sized cells (3 middle cells) the inductors have 0.75 turn and their radius is equal to 15.5 um. The varactors in those cells have 2 groups and 45 fingers. The physical dimensions of the inductors and varactors of all cells are summarized in Table 3.5. As can be seen from the table, the inductance value of the first and last cells is smaller than the value that is computed for the 50Ω cell. This difference is mainly due to the optimization and tuning that is performed for the removal of the parasitic effects of the traces which are used to connect the first and the last cells to the input and output ports, respectively. Furthermore, it should be noted that the inductors in the first and the last cells are implemented with a different number of turns and dimensions in order to produce the most compact floor plan.

The final 11-cell Tapered TTL phase shifter is laid out for fabrication (Fig. 3.12, the upper circuit). As mentioned in the previous section, to compare the area efficiency of the proposed phase shifter with the conventional design, the conventional non-Tapered 11-cell TTL phase shifter is also fabricated. The layout of this phase shifter

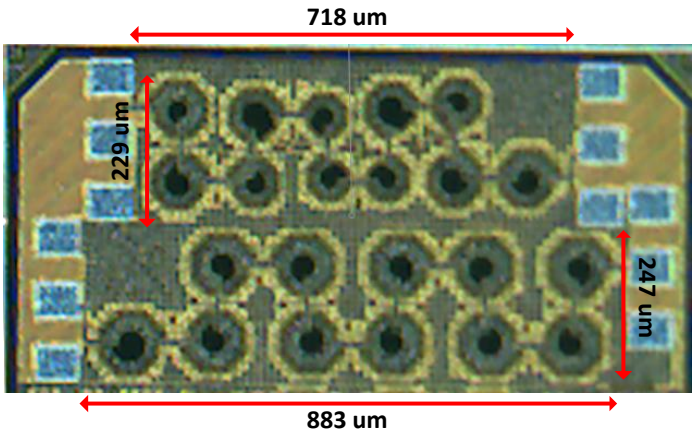


Figure 3.12: Implemented 11-cell Tapered TTL (Upper) and TTL (Lower) Phase Shifters in 65nm CMOS technology.

is also shown in Fig. 3.12 (the lower circuit).

3.4.3 Measurements

The phase shifter performance was measured by on-wafer probing. The Keysight E8361C PNA calibrated up to 40 GHz using standard Short/Open/Load/Through (SOLT) method along with a CASCADE 110-GHz Ground-Signal-Ground (GSG) probe station is used for measuring the phase shifter S-parameters. As shown in the measurement setup in Fig. 3.13, the biasing voltage of the phase shifter's varactors is applied via wideband (up to 65 GHz) Bias Tees (SHF 65 BT) which are cascaded with the probes. The input and output pad parasitic effects on the phase shifter are de-embedded by measuring the scattering parameters of a single isolated dummy GSG pad on the fabricated chip.

Fig. 3.14(a) shows the measurement results of the relative phase of the fabricated 11-cell Tapered TTL phase shifter as a function of frequency for different control voltages. As can be seen, since for the same variation of control voltage, the amount of phase shift is increased by increasing the operating frequency, the desired 180 degree phase shift can be achieved by a more limited control voltage range at the higher frequencies. For example, Fig. 3.14(a) shows that for providing a 180 degree phase shift at 16.5 GHz, the control voltage must vary between -0.5 to $+0.5$V while for the same phase shift at 24 GHz, it should vary between -0.5 to near $+0.1$V and it should vary only between -0.5 to -0.1V at 31 GHz.

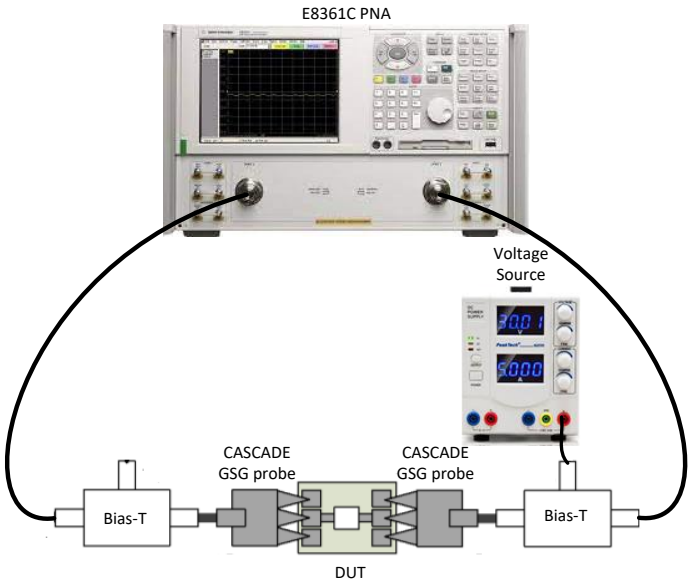


Figure 3.13: Measurement setup.

The measurement results for the insertion loss of the fabricated phase shifter are shown in Fig. 3.14(b). The figure shows that at the lower edge of the band (16.5 GHz), the insertion loss of the phase shifter varies between 3.5 to 7 dB, while at 24 GHz the insertion loss is between 5 to 10 dB and at 31 GHz it changes between 6.5 to 10.5 dB. Considering that insertion loss has a low-pass frequency response, the frequency at which the average insertion loss (averaging over the required control voltage range) is 3 dB lesser than the average insertion loss at 16.5 GHz, is defined as the upper edge of the operating frequency band. By this definition, the highest operating frequency (f_u) is 31 GHz.

The measurement results for the return loss of the fabricated chip are plotted in Fig. 3.14(c). This plot shows that for any control voltage and at any operating frequency, the S_{11} is less than $-10\ dB$. For the conventional TTL phase shifter, similar graphs of measurement results are provided and plotted in Fig. 3.15. Defining the lower edge frequency for the conventional TTL phase shifter as the minimum frequency at which 180 degree phase shift can be achieved, the lower operating frequency edge was found to be 18.5 GHz. Knowing that at 18.5 GHz, the average insertion loss in TTL phase shifter is around 6 dB, the upper operating frequency (f_u) with an average insertion loss of 9 dB is 31 GHz. Comparison between the insertion losses of both phase shifters shows that, despite the fact that average insertion loss is approx-

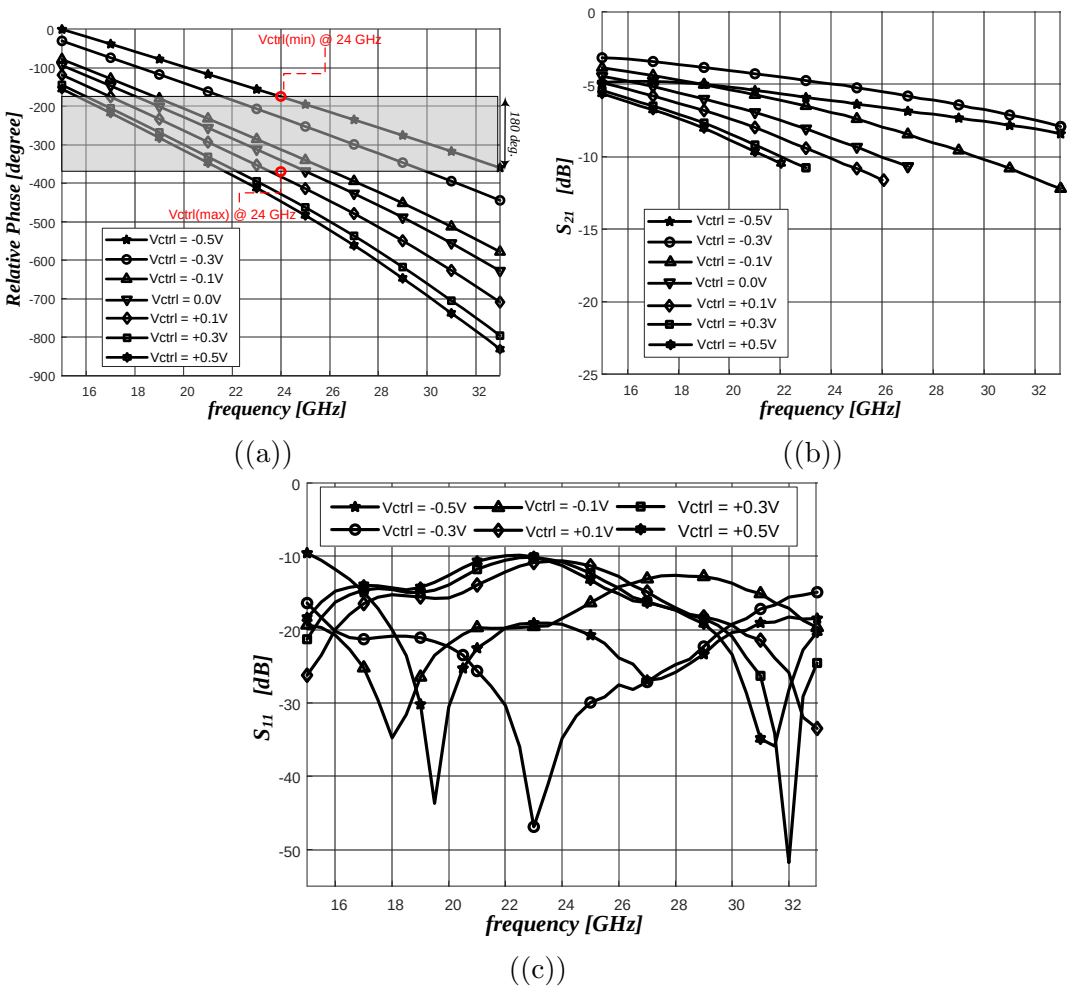


Figure 3.14: Measured (a) Relative Phase, (b) S_{21} and (c) S_{11} of the 11-cell Tapered TTL phase shifter versus frequency for different control voltages.

imately the same, in the Tapered TTL phase shifter, varying control voltage results in more fluctuation in the insertion loss because of the extra inter-cell reflections.

In our design, the mutual coupling between the inductors of the cells is not taken into account as we minimized the mutual coupling between inductors using grounded guard rings. However, the guard ring does not entirely eliminate the mutual coupling and it can result in the increase of the cells' inductance. As a consequence, increasing the cell's inductance can cause excessive deviation of the cell's characteristic impedance from port impedances whenever the cell's varactors capacitance is high (varactors are forward-biased). Neglecting this mutual coupling results in a considerable difference between the predicted performance (via simulation) and measurement results, particularly at the end of the frequency band. As an example, while

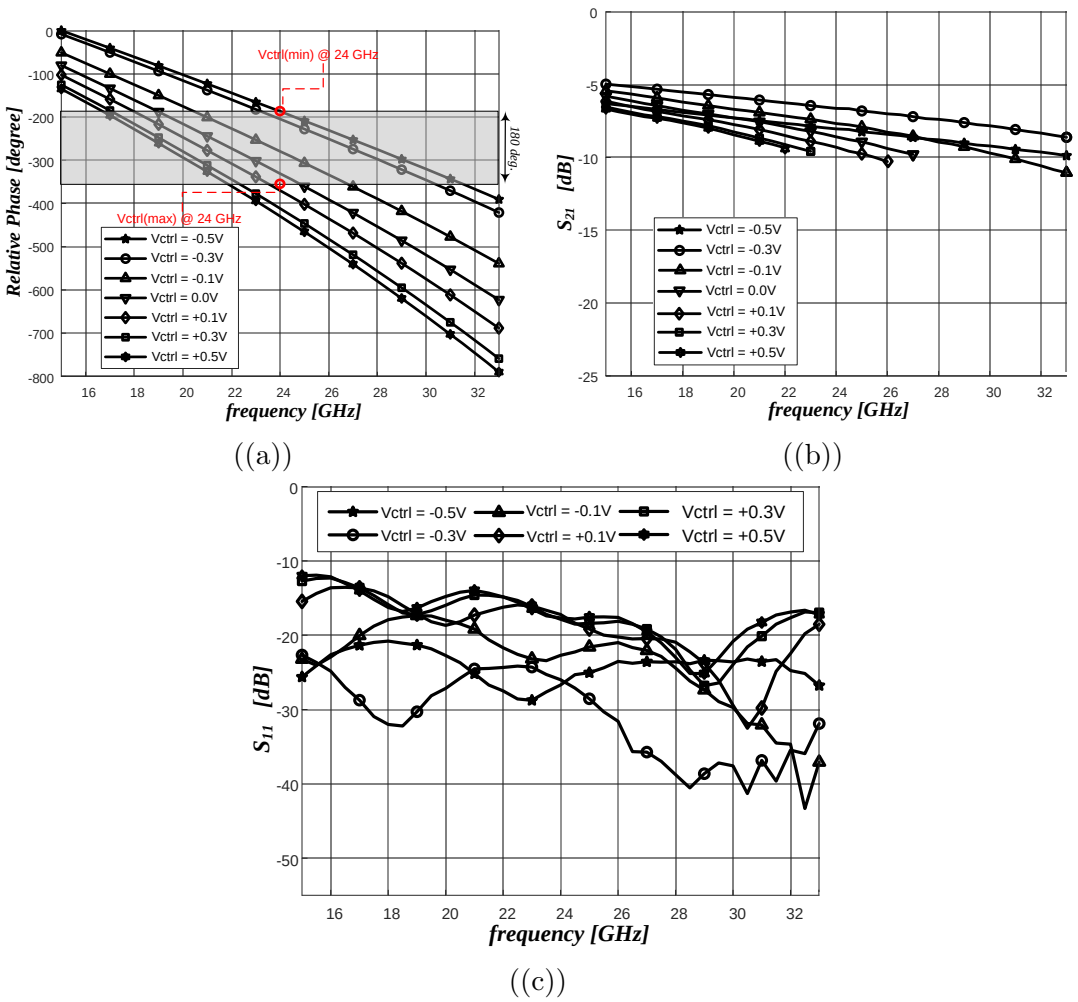


Figure 3.15: Measured (a) Relative Phase, (b) S_{21} and (c) S_{11} of the 11-cell TTL phase shifter versus frequency for different control voltages.

the average difference between simulated and measured results (in all varactors' bias conditions) at 16.5 GHz is less than 5%, it is increased to 15% at 31 GHz.

As the non-linear components in the proposed Tapered phase shifter are the varactors, the proposed circuit is expected to behave very linearly. To examine the linearity performance of the proposed phase shifter, the simulation results of the input-referred third intersection point (IIP3) at some selected frequencies within the operating bandwidth and for the control voltages corresponding to relative zero and 180 degree phase shifts, are reported in Table 3.6. For these cases, the minimum IIP3 is 15 dBm which is considered an acceptable value in many applications.

The delay per size $[ps/mm^2]$ and the insertion loss per delay $[dB/ps]$ are two

Table 3.6: Input referred third intersection point (IIP3)

$frequency$	$Control\ Voltage$	$IIP3$
16.5 GHz	-0.5V (0 deg.)	22.7 dBm
	+0.5V (180 deg.)	22.2 dBm
18.0 GHz	-0.5V (0 deg.)	24.0 dBm
	+0.5V (180 deg.)	21.2 dBm
22.0 GHz	-0.5V (0 deg.)	21.8 dBm
	+0.25V (180 deg.)	16.8 dBm
26.0 GHz	-0.5V (0 deg.)	16.9 dBm
	+0.1V (180 deg.)	15.0 dBm
28.0 GHz	-0.5V (0 deg.)	17 dBm
	+0.0V (180 deg.)	15.2 dBm
31.0 GHz	-0.5V (0 deg.)	21.2 dBm
	-0.1V (180 deg.)	18.4 dBm

well-known Figure of Merits (FOMs) which are widely used to compare the area efficiency and high-frequency electrical performance of the phase shifters [48]. The phase shifters with the larger delay per size are considered to be more area-efficient designs while the ones with the lower insertion loss per unit delay have better RF performance. These FOMs are calculated and reported in Table 3.7 for the proposed Tapered TTL phase shifter, the equivalent conventional design, and other millimeter wave phase shifters reported in the literature. In the computation of the mentioned FOMs, for each phase shifter, the reported *Delay* and *Loss* have been considered as the average of the maximum provided delay and the insertion loss of the phase shifter over its bandwidth, respectively. Table 3.7 shows that in Tapered TTL phase shifter, comparing to the conventional design has the same insertion loss but the area efficiency is increased by more than 25 percent. In addition to the mentioned FOMs, to evaluate both area efficiency and insertion loss by a single quantity, we suggest another figure of merit defined as

$$FOM1 = \frac{\frac{Delay}{Size}}{\frac{IL}{Delay}}. \tag{3.56}$$

As a result, the dimension of the $FOM1$ will be $[ps^2/(dB.mm^2)]$. Based on the value of $FOM1$ for the reported Phase shifters in Table 3.7, the proposed design noticeably outperforms others.

Table 3.7: Comparison table with related research works.

	This work (Conventional)	**This work (Tapered)**	**[35]**	**[44]**	**[49]**	**[50]**	**[51]**	**[48]**	**[52]**
Technology	**CMOS 65nm**	**CMOS 65nm**	CMOS 65nm	CMOS 65nm	CMOS 0.18um	BiCMOS 0.13um	CMOS 65nm	CMOS 0.13um	SiGe 0.25um
Frequency Range (GHz)	**18.5-31**	**16.5-31**	26-30	57-64	8-18	19.7-22.8	28-35	15-40	10-50
Topology	**Tunable TL**	**Tapered TTL**	RTPS	Tunable TL	TTD	Tunable TL	STPS	TTD	TTD
Phase Shift (deg)	**180**	**180**	160~180	133	125ps	360	290~360	40ps	32.8ps
Phase Resolution (deg)	**Cont.**	**Cont.**	11.25	Cont.	3.9ps	Cont.	5.2	5ps	Cont.
Average IL (dB)	**7**	**7.2**	16.5	7.8	19	13	12.5	14	15.5
Maximum IL (dB)	**10.5**	**12.2**	17.5	23.3	23	15	17	16	17
Delay (ps)	**21.1**	**22.7**	16.67	5.8	125ps	20	28.57	40	32.8
Power Consumption (mW)	**0**	**0**	0	0	0	10.4	0	24.6	0
Area (mm^2)	**0.22**	**0.17**	0.17	0.042	2	0.28	0.24	0.99	0.22
Loss/Delay (dB/ps)	**0.389**	**0.402**	1.01	1.62	0.152	1.53	0.438	0.400	0.473
Delay/Area (ps/mm^2)	**122.7**	**178.2**	98.1	154.3	62.5	71.4	119	40.4	149.1
$FOM1^*$ ($ps^2/(dB.mm^2)$)	**315.4**	**443.3**	97.1	95.24	411.2	46.7	271.7	101	315.5

* FOM1 is defined in (3.56)

3.5 Discussion and Conclusion

TTL phase shifters are widely recognized as effective solutions for implementing beamformers due to their attributes, including broad bandwidths, precise phase resolutions, and excellent linearity—all achieved without power consumption. However, challenges arise when these phase shifters are realized on-chip, manifesting in high ILs and substantial chip area occupation. These issues stem from the large size and low-quality factor of on-chip passive components. In this contribution, we introduce a Tapered TTL approach, achieved by scaling down the sizes of phase shifter cells towards the middle of the transmission line. Properly designed using the proposed method, these phase shifters demonstrate significantly improved area efficiency while maintaining the same phase shift range and insertion/return losses as conventional TTL phase shifters. Fabricated using 65-nm CMOS technology, the eleven-cell Tapered TTL phase shifter achieves commendable area efficiency, occupying 25% less chip area than its non-tapered counterpart. Importantly, it delivers a 180-degree phase shift over the frequency range of 16.5 to 31 GHz, while exhibiting the same average insertion loss of around 7 dB. This advancement marks a promising development for on-chip beamforming applications, combining enhanced area efficiency with consistent performance across the specified frequency range.

Chapter 4

Area-Efficient Analog Beamformers with Pseudo-Distributed Amplifier Architecture

This chapter presents an area-efficient receiving analog beamformer that utilizes a Pseudo-Distributed Amplifier architecture. The proposed beamformer integrates all of the building blocks of a typical analog beamformer, including the LNA, phase shifter, and power combining network, into a single circuit, thereby reducing the overall power consumption, consumed chip area, and fabrication costs. The design process for optimizing the beamformer gain, noise performance, and beam steering capability is presented and supported by mathematical analysis. To demonstrate the effectiveness of the proposed beamforming approach, a 4-element 21-23 GHz analog beamformer is fabricated in standard 65-nm CMOS technology and the measurement results are reported.

4.1 Proposed Pseudo Distributed Amplifier Beamformer

The block diagram of a typical receiving analog beamformer is shown in Fig. 4.1. It shows that such an analog beamformer consists of at least three building blocks for the array's element including a variable-gain LNA, a phase shifter, and a power combining network.

Although analog beamformers consume significantly less power and can be implemented at a lower cost compared to digital and hybrid beamformers, there is a

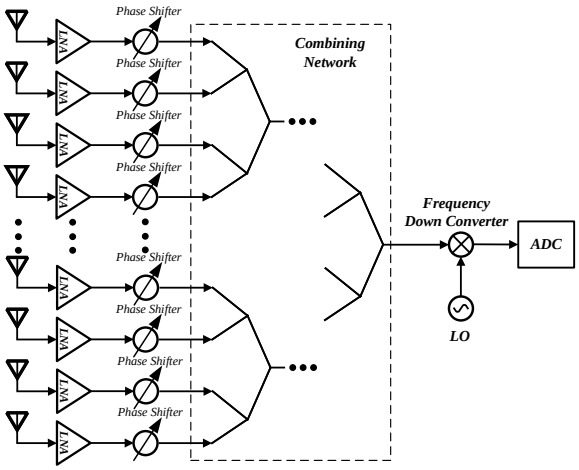


Figure 4.1: A receiver with an analog RF beamformer

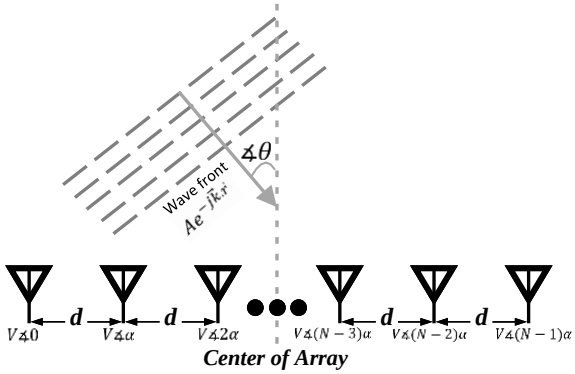


Figure 4.2: A N-element linear antenna array

strong demand for the development of low-cost energy-efficient analog beamformers for deployment in portable consumer electronic devices. Here we propose a complete analog beamformer using a DA topology combining the functionality of the LNA, phase shifter, and the power combiner into a single circuit.

4.1.1 Design Concept

Within a line receiver antenna array incorporating N individual antenna elements, if the radiated plane wave is received at an angle of arrival θ relative to the array, as depicted in Fig. 4.2, the resulting signals induced at the output terminals of the array antennas will possess equal amplitudes and progressive phases. The phase shift (α)

between received signals at each successive pair of elements can be calculated as

$$\alpha = \frac{2\pi d}{\lambda} \sin(\theta), \tag{4.1}$$

where λ is the wavelength of the received wave assuming uniform distancing of d between array's elements.

Similarly, within a traditional DA, as illustrated in Fig. 4.3(a), the phase shift between the gate voltage of two consecutive transistors corresponds to the electrical length of the transmission line connecting their respective gates. As a result, the drain current of each transistor can be calculated as

$$I_i = g_m V e^{-j(N-i)\alpha}, \tag{4.2}$$

where g_m is the transistor's transconductance. Considering that the output transmission lines linking the drains of the transistors have an electrical length identical to that of the gate input transmission lines, the drain currents of the transistors combine constructively at the output port. As a consequence, the total current at the output port, denoted by I_{out}, can be expressed as

$$I_{out} = \sum_{i=1}^{N} \frac{1}{2} g_{m_i} V e^{-j(i-1)\alpha} e^{-j(N-i)\alpha}, \tag{4.3}$$

which can be reduced to

$$I_{out} = \frac{N g_m V e^{-j(N-1)\alpha}}{2}. \tag{4.4}$$

where N is the number of transistors in DA.

If the input transmission lines of the DA are removed and the gates of the transistors are directly connected to the antenna elements of an array whose phase shift between their received signals is α, as depicted in Fig. 4.3(b) and each delay line between transistor drains is introducing the phase shift equal to α, then the resulting structure should perform like a conventional DA combining the drain currents of the transistors constructively (i.e. each consecutive current increases the current at the output terminal). In the ideal case the output currents of the gain cells will be added in phase at the output port, when the angle of arrival θ will produce the progressive

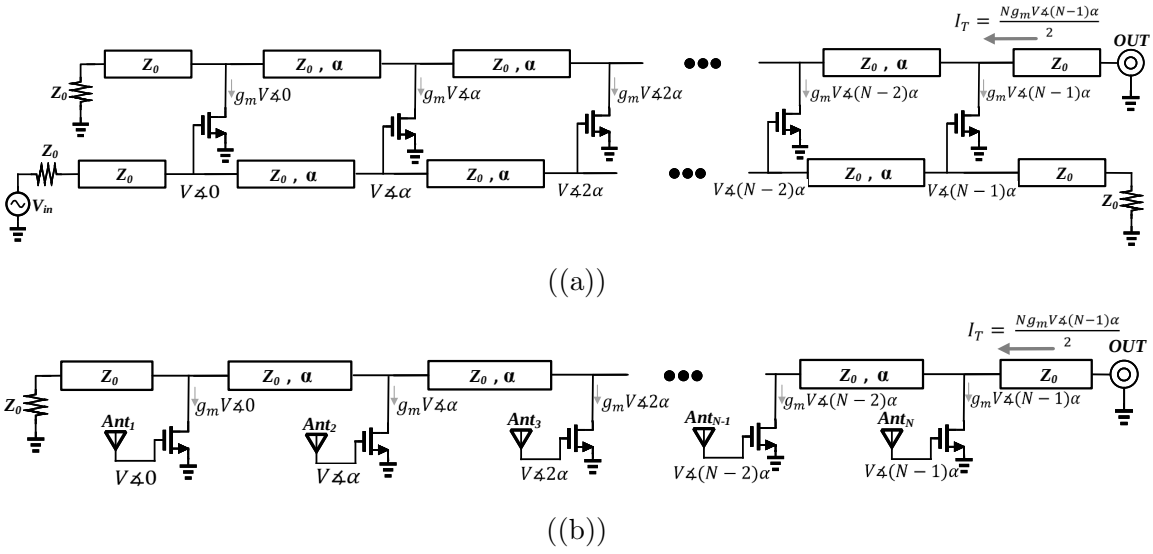


Figure 4.3: (a) Conventional distributed amplifier, and (b) proposed RF analog beamformer architecture

phase shift of α between consecutive array elements in exact accordance to (4.1). From the other side, if the delay lines are introducing the phase shifts

$$\alpha = \frac{2\pi d}{\lambda} \sin(\theta) \pm \frac{2\pi}{N}, \tag{4.5}$$

then it can be easily shown that output currents of the gain cells are combined destructively, i.e., each consecutive current is decreasing the current at the output terminal, and, if the angle of arrival θ is such that (4.5) is exactly satisfied, the output current will be zero. The above analysis shows that the proposed Pseudo-Distributed Amplifier (Pseudo-DA) circuit possesses the ability to amplify and constructively combine signals from a specific direction of arrival, while simultaneously attenuating (nullifying) signals arriving from other directions. Additionally, adjusting the electrical length of the output transmission lines linking the drains of the transistors, it is possible to steer the main beam direction. Thus, the proposed circuit operates as an analog beamformer combining the functionality of an amplifier, a phase shifter, and a power combiner into one circuit. The setup illustrated in Fig. 4.3(a) is typically utilized as a non-radiating broadband distributed amplifier. However, it offers flexibility, as either the drain line, the gate line, or both can be transformed into leaky wave antennas (LWAs) [53]. In leaky wave antennas, the transmission lines are used as the radiating elements. Several techniques are used to make the transmission line with

a low Q-factor to allow for radiation [54]. However, in our proposed beamformer the drain transmission line is used as a series-fed combining network and consequently, it must be designed in such a way to reduce the leakage of electromagnetic energy. The main challenge in the on-chip implementation of the suggested beamformer is the proper realization of the required tunable output transmission line. This task is particularly critical due to the imperative of achieving optimal area efficiency to minimize fabrication costs and minimize losses to enhance energy efficiency. In order to address this challenge comprehensively, the subsequent section will undertake a comprehensive survey of a systematic approach dedicated to designing such a tunable transmission line.

4.2 Lumped Element Design of On-Chip Transmission Lines with Tunable Electrical Length

In the previous chapter, we discussed the design of Tunable-ATL cells based on the transmission line model. In this chapter, we offer an alternative methodology for the design of Tunable-ATL cells based on a lumped element model of the cells, as discussed below.

4.2.1 Analysis of an ATL Cell

In the previous chapter, we showed that an ATL cell may be described by its $[ABCD]$ matrix as [44]

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 - LC\omega^2 & jL\omega \\ 2jC\omega - jLC^2\omega^3 & 1 - LC\omega^2 \end{bmatrix}. \tag{4.6}$$

The determinant of the cell's $[ABCD]$ matrix can be calculated as

$$\Delta = AD - BC \tag{4.7}$$

which is equal to one as this two-port network is reciprocal. Knowing that the input impedance (Z_{in}) of a transmission line loaded with an impedance equal to its characteristic impedance (Z_c) results in the input impedance being equal to Z_c, one can

write

$$Z_{in} = \frac{V_1}{I_1} = \frac{AV_2 - BI_2}{CV_2 - DI_2} = \frac{AZ_c + B}{CZ_c + D} = Z_c. \tag{4.8}$$

Considering $A = D$, one finds from (4.6) and (4.8) that

$$Z_c = \sqrt{\frac{B}{C}} = \sqrt{\frac{L}{C(2 - \omega^2 LC)}}. \tag{4.9}$$

The characteristic transmission γ, which is also defined at the condition of characteristic loading, relates the output and input voltages of an ATL cell as

$$V_2 = V_1 e^{-\gamma}. \tag{4.10}$$

By referencing the $[ABCD]$ matrix definition, which dictates that $V_1 = AV_2 - BI_2$, one can verify that

$$\frac{V_1}{V_2} = A + \frac{B}{Z_c} = A + \sqrt{BC} = e^{\gamma} \tag{4.11}$$

which gives

$$e^{\gamma} = A + \sqrt{BC} = (1 - \omega^2 LC) + j\omega\sqrt{LC(2 - \omega^2 LC)}. \tag{4.12}$$

Recalling that $A = D$ and using (4.7), one can write

$$\Delta = A^2 - BC = (A + \sqrt{BC})(A - \sqrt{BC}) = 1 = e^{\gamma} e^{-\gamma} \tag{4.13}$$

which results in

$$e^{-\gamma} = A - \sqrt{BC}. \tag{4.14}$$

From (4.11) and (4.14) one can find

$$A = \frac{e^{\gamma} + e^{-\gamma}}{2} = \cosh\gamma \tag{4.15}$$

and

$$\sqrt{BC} = \frac{e^{\gamma} - e^{-\gamma}}{2} = \sinh\gamma. \tag{4.16}$$

Finally, it can be concluded from (4.9) and (4.16) that

$$B = Z_c \sinh\gamma \tag{4.17}$$

and

$$C = Z_c^{-1} \sinh \gamma. \tag{4.18}$$

Hence, the ATL cell's $ABCD$ matrix can be rewritten as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh \gamma & Z_c \sinh \gamma \\ Z_c^{-1} \sinh \gamma & \cosh \gamma \end{bmatrix}. \tag{4.19}$$

The $ABCD$ matrix, which is derived in (4.19), is equivalent to the $ABCD$ matrix of a transmission line whose characteristic impedance and propagation constant is equal to Z_c and γ, respectively.

Using (4.12), it can be easily verified that the magnitude of the V_1/V_2 ratio, $|e^{\gamma}|$, is equal to one. Consequently, (4.11) can be rewritten as

$$\begin{aligned} \frac{V_1}{V_2} &= (1 - \omega^2 LC) + j\omega\sqrt{LC(2 - \omega^2 LC)} \\ &= \cos\alpha + j \sin\alpha = e^{j\alpha}. \end{aligned} \tag{4.20}$$

In other words, one can write

$$V_2 = V_1 e^{-j\alpha}, \tag{4.21}$$

where α is equal to

$$\alpha = \arcsin\left(\omega\sqrt{LC(2 - \omega^2 LC)}\right). \tag{4.22}$$

In an ATL cell, substituting capacitors with varactors enables modification of the cell's electrical length, as depicted in (4.22). Nevertheless, the alteration of the varactors' capacitance, as indicated in (4.9), concurrently affects the characteristic impedance of the cell. Consequently, adjusting the capacitance of the varactors not only tunes the electrical length of the cell but also induces mismatch loss.

Upon closer examination of equation (4.22), it becomes apparent that the relationship between frequency and the electrical length of the cell is non-linear, suggesting that the transmission line model of the cell exhibits dispersive behavior. However, in the context of circuit design, non-dispersive transmission lines are preferred due to their associated benefits, such as preserving signal integrity, facilitating wide bandwidth, and simplifying system design[29].

Assuming that

$$\omega^2 LC << 2, \tag{4.23}$$

then (4.22) is reduced to

$$\alpha = \arcsin\left(\omega\sqrt{LC(2-\omega^2 LC)}\right) \approx \arcsin\left(\omega\sqrt{2LC}\right). \tag{4.24}$$

Using the approximation of $x \approx \sin(x)$, for small x, (4.24) can be further simplified to

$$\alpha \approx \omega\sqrt{2LC} \tag{4.25}$$

which implies that, as long as the condition in (4.23) is held, the proposed Tunable-ATL cell is non-dispersive.

In typical semiconductor CMOS fabrication techniques, the ratio of the maximum to the minimum capacitance of a varactor remains constant regardless of its size [17]. As a result, one may express the ratio of the maximum to the minimum capacitance of a varactor as

$$r_c = \frac{C_{max}}{C_{min}}, \tag{4.26}$$

and determine that the varactor's capacitance can be varied according to

$$\frac{C_0}{\sqrt{r_c}} \leq C \leq \sqrt{r_c} C_0, \tag{4.27}$$

where C_0 represents the capacitance at mid-range and is defined as

$$C_0 = \sqrt{C_{max} C_{min}}. \tag{4.28}$$

Hence, the Tunable-ATL cell's maximum attainable phase shift ($\Delta\theta_{max}$) can be determined as

$$\Delta\theta_{max} = \alpha_{max} - \alpha_{min} = \omega\sqrt{2LC_0}\left[\sqrt[4]{r_c} - \frac{1}{\sqrt[4]{r_c}}\right]. \tag{4.29}$$

If the electrical length of the cell is defined as the mid-range electrical length, α_0, when the varactors' capacitance is equal to C_0, then (4.29) can be expressed in a different form as

$$\Delta\theta_{max} = \alpha_0\left[\sqrt[4]{r_c} - \frac{1}{\sqrt[4]{r_c}}\right]. \tag{4.30}$$

Assuming the condition stated in (4.23), the equation presented in (4.9) can be simplified to

$$Z_c = \sqrt{\frac{L}{2C}}. \tag{4.31}$$

Consequently, if the Tunable-ATL cell is adjusted to match the impedance Z_0 of the ports when the varactors are at their mid-range capacitance value C_0, the cell's characteristic impedance will vary within the range specified by as

$$\frac{Z_0}{\sqrt[4]{r_c}} \leq Z_c \leq Z_0 \sqrt[4]{r_c} \tag{4.32}$$

Thus, when the Tunable-ATL cell is matched to the port's impedance at its mid-range varactors' capacitance value, the maximum deviation from Z_0 and, correspondingly, the mismatch loss, is minimized and is the same for both minimum and maximum varactors' capacitance values. Based on the preceding discussion, the design procedure for a Tunable-ATL cell can be summarized as follows: Initially, the desired maximum frequency shift $\Delta\theta_{max}$ and the targeted semiconductor technology must be specified as inputs. It is worth noting that since r_c is a parameter that varies with the semiconductor technology, choosing the semiconductor technology would automatically determine the value of r_c.

In the subsequent stage, equation (4.30) can be utilized to extract the mid-range electrical length α_0 of the Tunable-ATL cell. As discussed earlier, the calculated value of α_0 for a desired $\Delta\theta_{max}$, often does not conform to the small electrical length approximation. Hence, instead of employing a Tunable-ATL cell with a large α_0, a cascade of N cells having a smaller α_0' can be utilized. Therefore, determining the number N_{cell} of required cascaded cells and their maximum electrical length is the next step. To satisfy the condition of the small electrical length approximation, it is adequate to ensure that the maximum electrical length α_0' of the cascaded cells is less than or equal to 45^o. In practical designs, employing a smaller number of cascaded Tunable-ATL cells results in a more compact design and reduced insertion loss [36]. Hence, the smallest value of

$$\alpha_0' = \frac{\Delta\theta_{max}}{N_{cell}[\sqrt[4]{r_c} - \frac{1}{\sqrt[4]{r_c}}]} \leq 45^o \tag{4.33}$$

would be an appropriate choice for the required number of cascaded cells. In the final step of the design process, knowing that the mid-range electrical length of the cascaded cells is

$$\alpha_0' = \frac{\alpha_0}{N_{cell}}, \tag{4.34}$$

L and C_0 can be calculated by

$$L = \frac{\alpha_0' Z_0}{\omega} \tag{4.35}$$

and

$$C_0 = \frac{\alpha_0'}{2Z_0\omega}, \tag{4.36}$$

respectively.

4.3 Design of a 4-Element K Band Analog Beamformer with a Pseudo-DA Architecture

To verify the efficacy of the proposed approach, this section presents the complete design procedure of a 4-element K band beamformer with a Pseudo-DA architecture. The designed Pseudo-DA beamformer is then fabricated using a standard 65-nm CMOS technology. The procedure begins by illustrating the design of the Tunable-ATL cell, which is a critical component of the Pseudo-DA architecture and, subsequently, by discussing the design of the transconductance gain cell and input matching network. The simulation results of the overall performance of the beamformer are then presented. Finally, the measurement results of the fabricated beamformer are analyzed in the subsequent section.

4.3.1 Design of Tunable Output Transmission Line

It is desired that the proposed K band beamformer provides the ability to steer the through at least 100 degrees ($\Delta\theta_{max} = 100^o$). Knowing that in the target semiconductor technology (standard 65-nm CMOS), r_c is equal to 3.5, one can use (4.30) to calculate

$$\alpha_0 = \frac{\Delta\theta_{max}}{\sqrt[4]{r_c} - \frac{1}{\sqrt[4]{r_c}}} = \frac{100^o}{\sqrt[4]{3.5} - \frac{1}{\sqrt[4]{3.5}}} = 157^o \tag{4.37}$$

which is obviously far away from the small electrical length approximation. As a consequence, using (4.33), the minimum number of required cascaded cells can be calculated as

$$N_{cell} \geq 4. \tag{4.38}$$

Choosing $N_{cell} = 4$, the Tunable-ATL cell's mid-range electrical length (α_0') is equal to

$$\alpha_0' = \frac{157^o}{4} = 39.25^o. \tag{4.39}$$

Consequently, the Tunable-ATL cell's inductance (L) and mid-range capacitance (C_0) values can be calculated by using (4.35) and (4.36), which are equal to 247 pH and 49.5 fF, respectively.

In the next step, the cell is implemented and simulated in the circuit simulator that supports the CAD model of the target semiconductor technology. The S-parameters simulation results show that by choosing the values of L and C_0, as shown in the table of Fig. 4.4(a), each Tunable-ATL cell can achieve a tuning range of over 35 degrees of electrical length across the entire bandwidth while still maintaining acceptable matching performance. This suggests that cascading only three such cells can provide the desired beam steering capability. The simulation results of the electrical length, insertion/return losses, and the characteristic impedance of the three cascaded Tunable-ATL cells for various bias conditions, are presented in Fig. 4.4(b) to Fig. 4.4(d), respectively. As can be seen, at 22 GHz the electrical length of the cascaded cells changes from 210 to 320 degree with the control voltage varying from 0.7 to 1.7V, while the characteristic impedance remains within the acceptable range of 38 to 53 Ω and the input and output return losses remain below −13 dB over 20 to 24 GHz band.

4.3.2 Design of Transconductance Gain Cells and Input Matching Circuit

In a DA, the transconductance gain cells amplify the input signals and transform them into currents that are added constructively at the output of the drain transmission

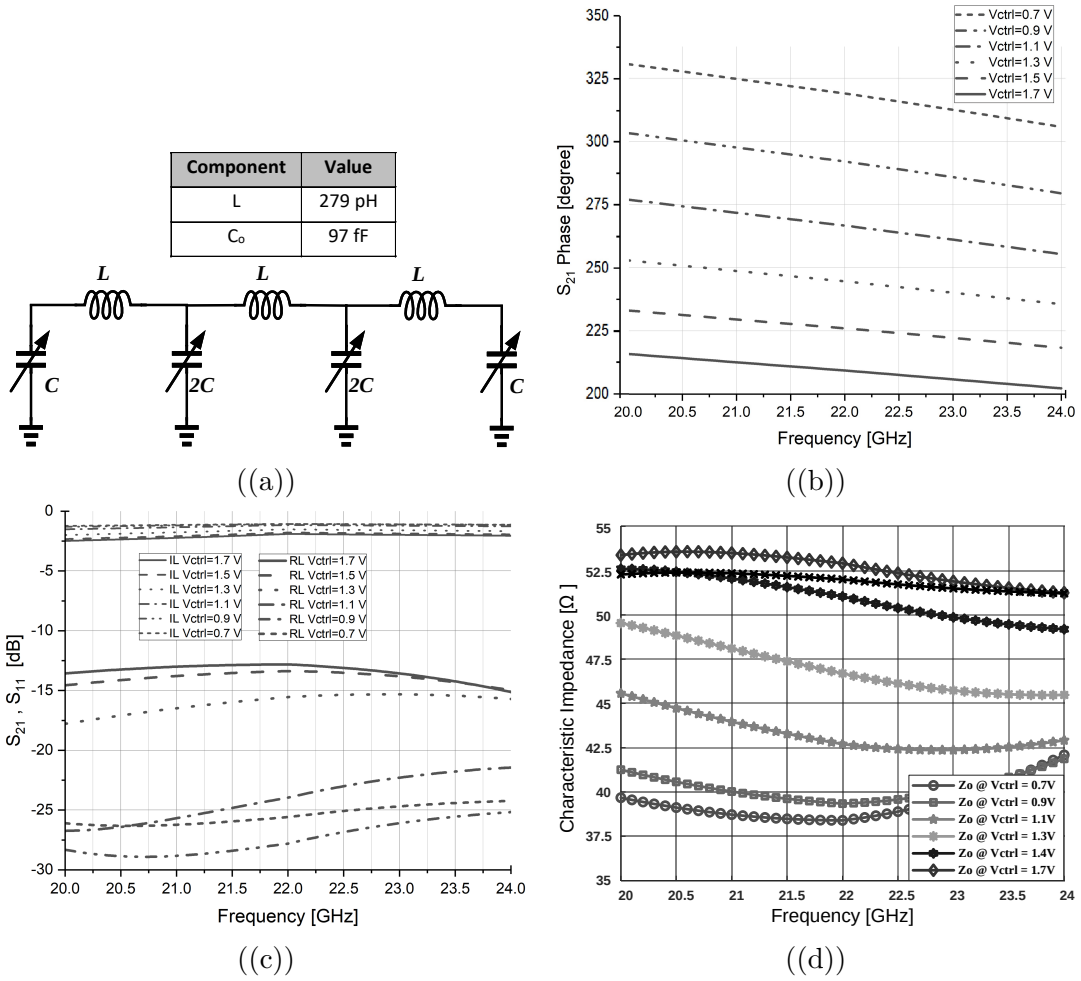


Figure 4.4: (a) Schematic, (b) electrical length, (c) Insertion and Return loss, and (d) characteristic impedance of simulated Tunable-ATL.

line. If single transistors with transconductance of g_m are used as gain cells, then the voltage gain of an N-element beamformer can be calculated as

$$|A_{v_{max}}| = |\frac{V_{OUT}}{V}| = \frac{I_{OUT} \times Z_0}{V} = \frac{N g_m Z_0}{2}, \tag{4.40}$$

where I_{OUT} is obtained from (4.4), assuming that the drain transmission line is terminated in its own characteristic impedance (Z_0) and all currents are added in phase. With the typical characteristic impedance (Z_0) of 50 Ω (a relatively modest value), both N and g_m must be increased to realize the intended gain for the beamformer. However, given that the value of N is usually predefined regarding the other beamformer parameters, like beamwidth and the positioning of nulls within the array

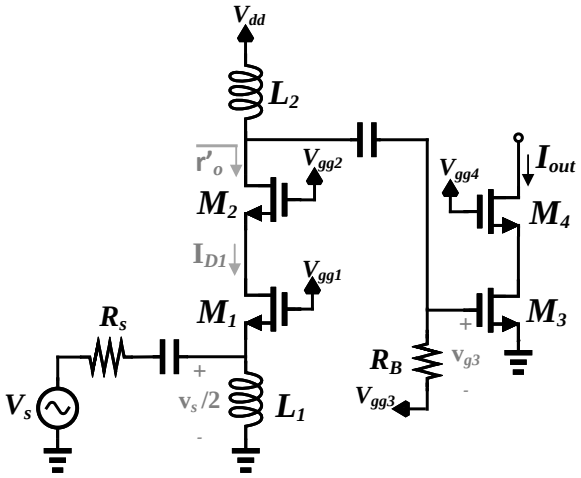


Figure 4.5: The designed transconductance gain cell for the proposed K band beamformer

pattern, it can not be used to serve as an adjustable parameter for gain manipulation. In the short-channel MOSFET transistors (including the selected 65-nm CMOS technology) transconductance (g_m) can not be increased by increasing the drain current unless excessive DC power consumed due to their nonlinear relationship [17]. Therefore, in order to increase the gain of the beamformer, the dimensions of the transistors must be enlarged. However, this enlargement results in increased parasitic capacitances of the transistors, consequently leading to a notable deterioration in high-frequency performance. Furthermore, in the short-channel transistors, the output resistance (r_o) is also decreased [17]. Accordingly, where the transconductance gain cell is realized using a single transistor, this low output resistance can effectively divert a substantial fraction of the drain currents, thereby reducing the gain of the beamformer system.

To address the limitations outlined earlier for the single-stage transconductance gain cell, we have developed a two-stage cascode transconductance gain cell for our K-band beamformer, as depicted in Fig. 4.5. The first stage uses a Common Gate (CG) topology to facilitate input matching, while the cascode configuration in the second stage results in an output resistance r_{out} of $r_{o4}(1 + g_{m4}r_{o3})$, which greatly surpasses the loading impedance of the gain cell $Z_o/2$. This enables the gain cell to behave as an ideal current source and prevents the output power dissipation in the gain cell's output resistance. Furthermore, assuming that the biasing resistor R_B is

much larger than the first stage output resistance $r_o^{'}$, we can calculate the equivalent transconductance gain (G_m) of the proposed gain cell as:

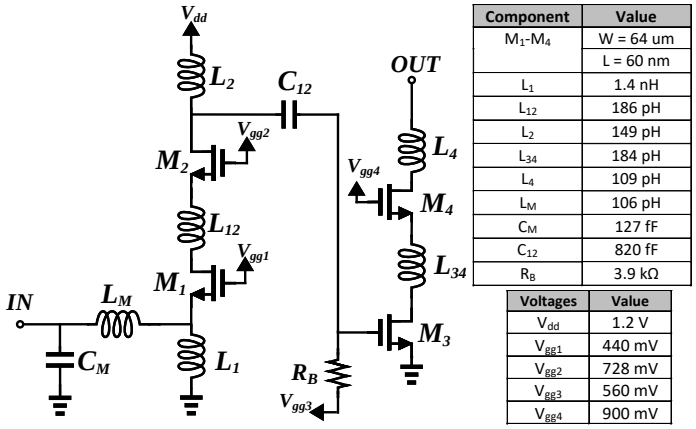
$$G_m = \frac{I_{out}}{v_s} = g_{m1} g_{m3} r_o^{'} = g_{m1} g_{m3} r_{o2} (1 + g_{m2} r_{o1}). \tag{4.41}$$

Using the cascode configuration provides another important advantage. This type of amplifier configuration significantly reduces the reverse gain and makes the amplifier stages, to some extent, unilateral and as a consequence, ensures the gain cells' stability. However, for the designed gain cell, the stability was verified by stability simulations which confirmed that both stability factors of μ and $\mu^{'}$ are greater than one over the frequency range between 1 to 40 GHz. These are necessary and sufficient conditions for the stability of the gain cells [55].

It is worth noting that the calculation provided for G_m and r_{out} of the proposed gain cell does not take into account the effect of parasitic capacitors, which is often significant in applications involving high frequencies, like the K-band beamformer we are discussing. The presence of these parasitic capacitors can considerably constrain the bandwidth of the gain cell. To address this challenge, a commonly adopted approach involves inserting inductors between the transistors, as illustrated in Fig. 4.6(a). This method entails the creation of LC-ladder filters that effectively mitigate the effects of parasitic capacitance while also isolating the loading effects of each stage from those preceding and following it [56].

Given the common-gate configuration of the input stage, the input impedance of the gain cell can be expressed as $1/(g_{m1} + C_{ss1} j\omega)$, where C_{ss1} represents the sum of all parasitic capacitances linked to the source of M_1. The incorporation of L_M and C_M into the gain cell's input, as depicted in Fig. 4.6(a), serves a dual purpose. This arrangement not only creates a ladder network that effectively eliminates the parasitic effects of C_{ss1} but also provides the flexibility to opt for a larger g_{m1} value, rather than sticking to $1/g_{m1} = 50\Omega$. This choice helps us achieve both higher gain and enhanced input-matching performance. It is important to notice that L_1 has the role of a Radio Frequency Choke (RFC) and, consequently, its variation does not affect the performance of the gain cell.

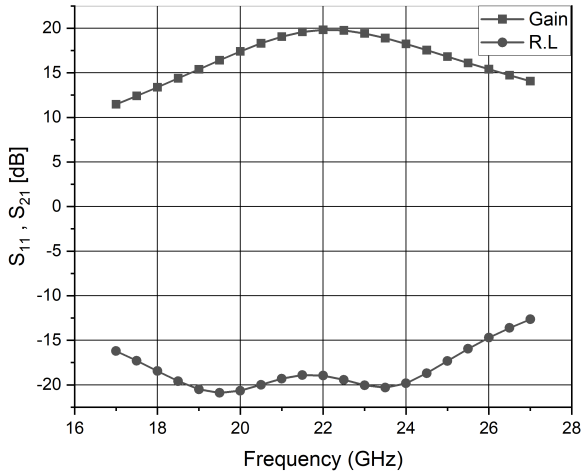
Taking the above approach and using the proposed transconductance gain cell con-



Component	Value
M_1-M_4	W = 64 um
	L = 60 nm
L_1	1.4 nH
L_{12}	186 pH
L_2	149 pH
L_{34}	184 pH
L_4	109 pH
L_M	106 pH
C_M	127 fF
C_{12}	820 fF
R_B	3.9 kΩ

Voltages	Value
V_{dd}	1.2 V
V_{gg1}	440 mV
V_{gg2}	728 mV
V_{gg3}	560 mV
V_{gg4}	900 mV

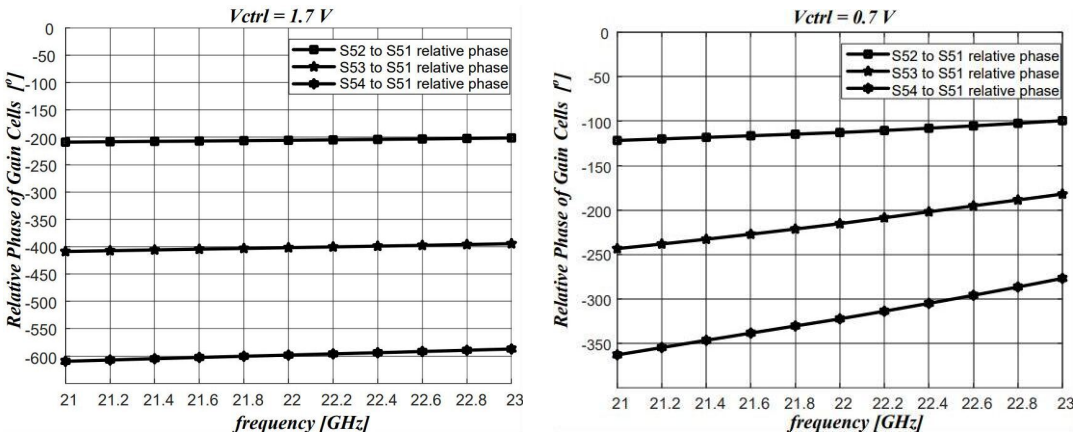
((a))



((b))

Figure 4.6: (a) The implemented transconductance gain cell of the K-band beamformer and (b) its simulated gain and return loss

figuration, we modeled the gain cell in the CAD tool that supports the component model of the selected semiconductor technology. Multiple simulations and optimizations were conducted within the CAD tool to enhance the gain cell's performance with respect to G_m, Return Loss (RL), frequency response, and power consumption. The final optimized values of the components of the transconductance gain cell and its S-parameters simulation results are presented in Fig. 4.6(a) and Fig. 4.6(b), respectively. The simulation results show a maximum gain of 20 dB at 23 GHz while the gain cell's S_{11} remains below -15 dB over 18 to 26 GHz. The maximum gain is intentionally decided to be tuned at higher frequencies to compensate for the high-frequency loss of the ATL cells.



((a)) ((b))

Figure 4.7: Relative phase responses of gain cells at (a) V_{ctrl} = 1.7 V and (b) V_{ctrl} = 0.7 V

Assuming that the phase of the first gain cell (from its input to the beamformer's output) is the reference phase, then the relative phase of the gain cells is plotted for the lower and the upper range of the varactors' control voltage as shown in Fig. 4.7. When the control voltage (V_{ctrl}) is equal to 1.7V, the varactor's capacitance is less dispersive than for other control voltages. In this case, the distances between characteristics are nearly equal, and they are nearly horizontal (see Fig. 4.7(a)). It means that the input signals of the gain cells will arrive at the output with the phases that provide their summation (ideal constructive addition at the output). When the control voltage is equal to 0.7V, the situation is different (see Fig. 4.7(b)), and yet the signals are added in such a way that the output current is still increasing with each signal. With the lower control voltage, the varactors are forward-biased. In this condition, the capacitance of the varactors is at its highest value, but they are more dispersive. Therefore, contrary to the condition when the larger control voltage is applied, the relative phase difference between the gain cells varies with frequency causing eventually, as shown in the next section, a slight reduction in the peak of the array pattern.

4.3.3 Beamforming Simulation Results

The proposed 4-element K-band beamformer is constructed by connecting four match-

ed transconductance gain cells with a cascade of tunable transmission lines, as depicted in Fig. 4.8. As can be seen, to facilitate tuning of the varactors in the Tunable-ATL cells, the gate terminals of all varactors are connected to the control voltage (V_{ctrl}) thorough a Radio Frequency Choke (RFC) which is connected at the one end of the output transmission line. Considering that in the selected 65-nm CMOS technology, the varactors can achieve their maximum tuning range by varying the bias voltage within the range of -0.5 to $+0.5V$, while the transistor's bias voltage (V_{dd}) is set to $1.2V$, the required V_{ctrl} should be within the range of

$$0.7V \leq V_{ctrl} \leq 1.7V. \tag{4.42}$$

To simulate the behavior of a plane wave incident from a specified angle of arrival, four synchronized signals with equal amplitudes and progressive phases are applied to the inputs of the gain cells. The phase of the input signals is determined by $k\alpha$, where α represents the angle of arrival according to Equation (1), and k varies from zero to three. By sweeping the value of α and recording the magnitude of the output voltage for a given V_{ctrl}, the beamforming and beam steering performance can be evaluated. The beamforming performance at frequencies of 21, 22, and 23 GHz is shown in Fig. 4.9(a) to Fig. 4.9(c), respectively. As can be seen, the values of the ATL cells' components are optimized in such a way that provide at least 110 degrees of phase shift at the lower edge of the frequency band (21 GHz). In addition, the simulation results show that the maximum array gain of 20, 21, and 23 dB is achieved at 21, 22, and 23 GHz, respectively, while the variation in the array gain is limited to 2.5 dB over the entire phase shift range.

In the layout design of the Tunable-ATL cells, each inductor is surrounded by a grounded seal ring to minimize mutual coupling between the inductors of adjacent cells. However, to achieve a compact layout for the beamformer, the mutual coupling, particularly among closely located cells, remains significant. Therefore, to account for this mutual coupling effect, a comprehensive electromagnetic (EM) simulation is conducted. Fig. 4.10 presents the EM simulation results, indicating a decrease of 2 to 4 dB in the beamformer's array gain at lower control voltage levels. This reduction can be attributed to the mutual coupling, which effectively increases the inductance

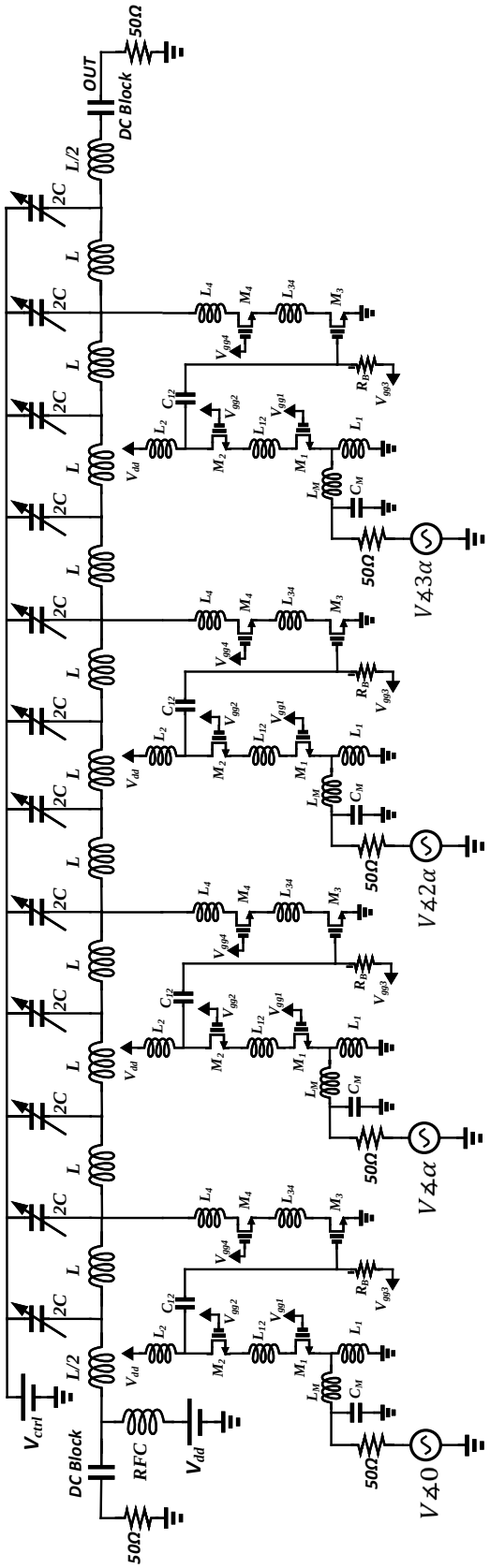
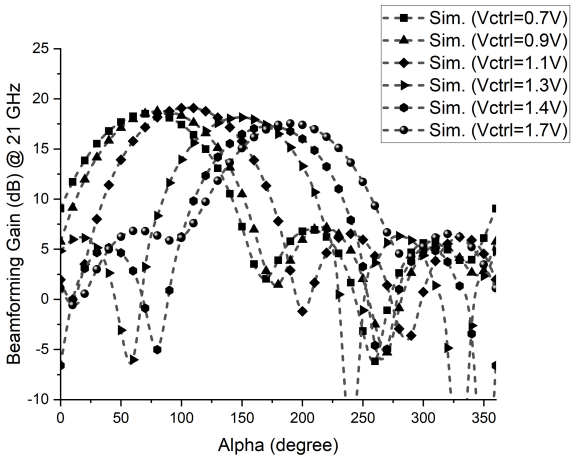


Figure 4.8: Simulation setup for the designed K-band beamformer



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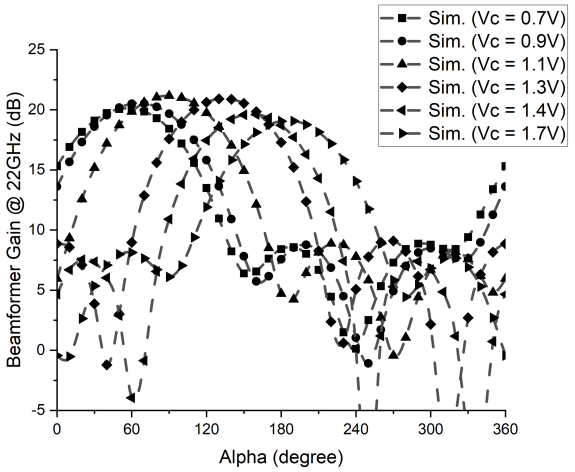

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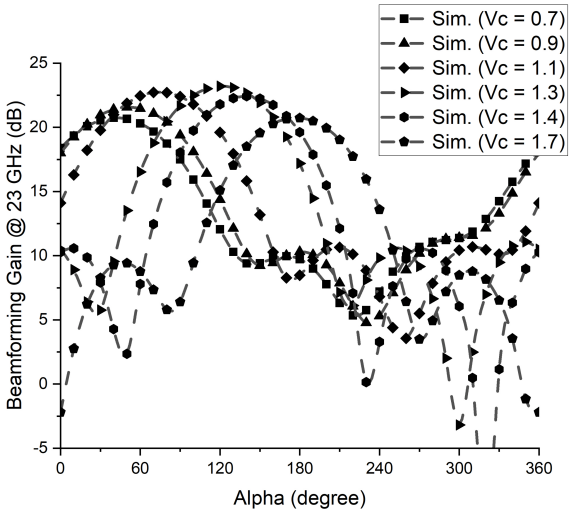
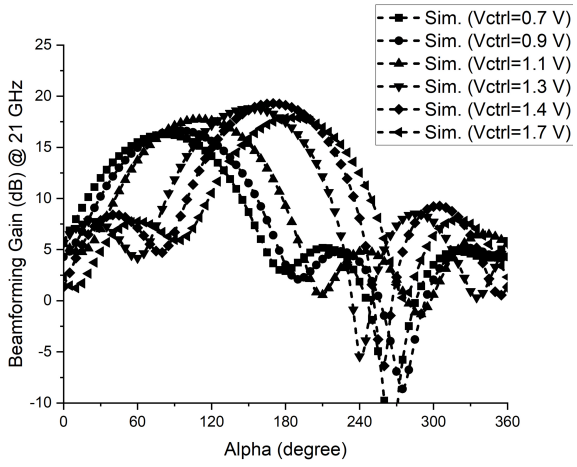


((c))

Figure 4.9: Simulation results of the array pattern for (a) 21 GHz, (b) 22 GHz, and (c) 23 GHz



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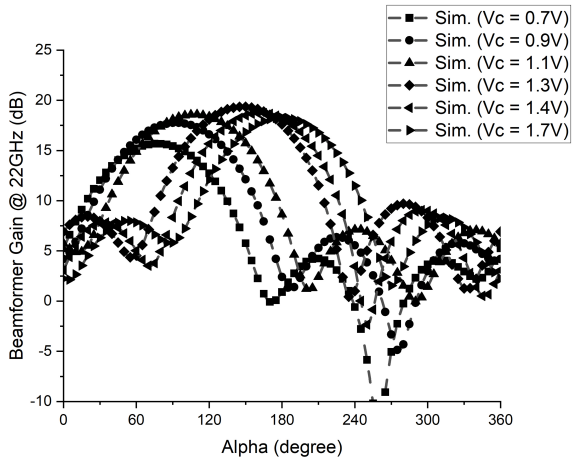

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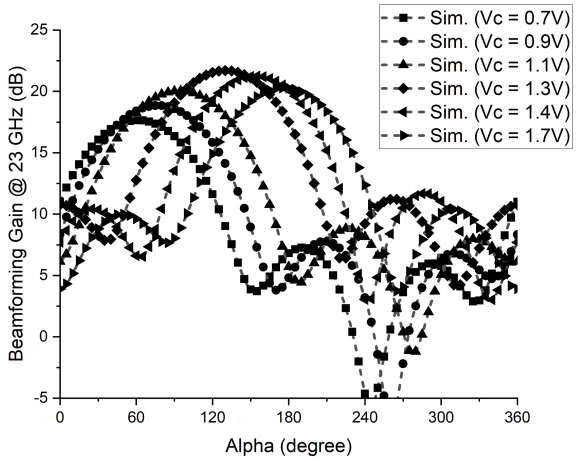
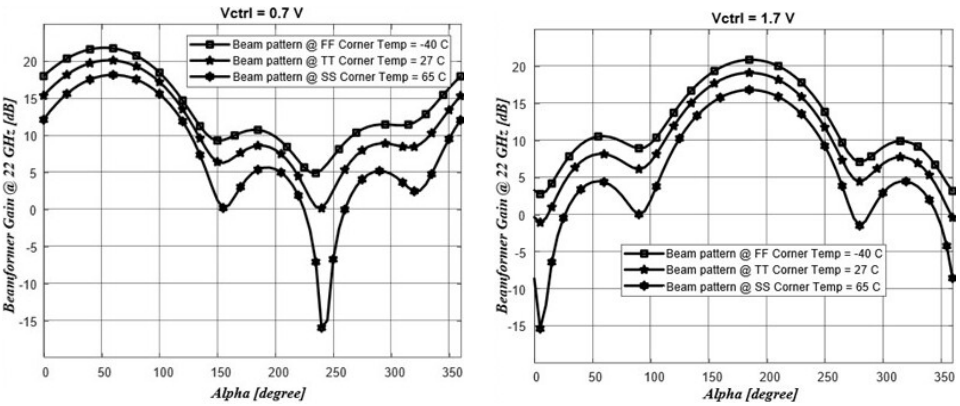


((c))

Figure 4.10: Simulation results of the array pattern when the mutual coupling between ATL cells is taken to account for (a) 21 GHz, (b) 22 GHz, and (c) 23 GHz



((a)) ((b))

Figure 4.11: Variation of beamformer's gain for nominal and the process corners when (a) $V_{ctrl} = 0.7V$ and (b) $V_{ctrl} = 1.7V$

of the Tunable-ATL cell's inductor and consequently raises the insertion loss of the cell [57].

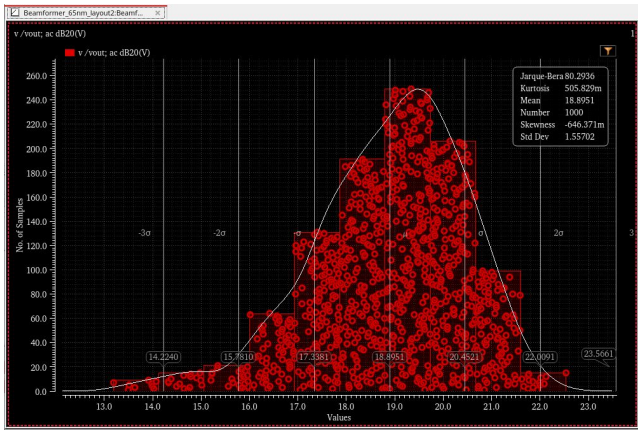
4.3.4 Sensitivity to PVT variations

To investigate the sensitivity of the proposed design to PVT variations, several different process corners, including TT, FF, FS, SF, and SS, for all semiconductor devices (RFMOS transistors, MOS-CAPS, RF-MIM-CAPS, and MIM-CAPS) over different temperatures in the interval of -40 to 65 degree of Celsius, are examined. As it was discussed earlier, the biasing gate voltage of the second stage of the gain cells can be tuned for different conditions. If V_{gg3} and V_{gg4} (see Fig. 4.6(a)) are obtained from a Proportional To Absolute Temperature (PTAT) source with a slope of 1.0 mV/deg, then the variation of the beamformer gain (at the peak of the gain pattern) due to PVT variation is limited to only around 4 dB. Fig. 4.11(a) and Fig. 4.11(b) show the variation of the beamformer gain for nominal and the process corners and the temperature extremes where the control voltage is 0.7V and 1.7V, respectively. Analyzing the graphs illustrated in Fig. 4.11 reveals how PVT variations affect the beamformer's gain pattern. Notably, these variations predominantly impact the values of the pattern gain at its peak and sidelobe, as opposed to causing significant shifts in their positions. Consequently, to make a statistical analysis of the design sensitivity, in the performed Monte Carlo simulation, given the positional information of the peak and

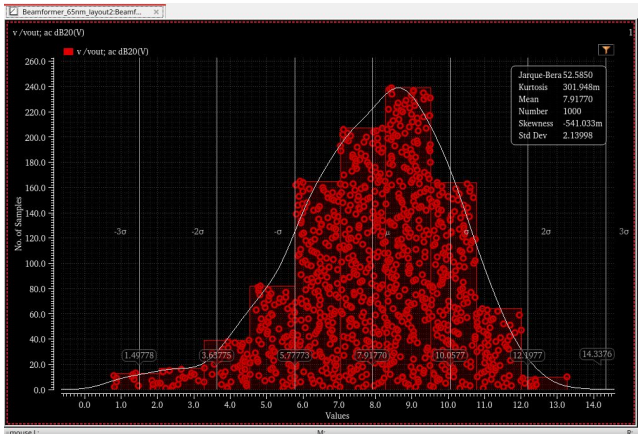
Table 4.1: Beamformer's pattern statistics (V_{ctrl} = 1.7V)

	Pattern Peak	Pattern Sidelobe
Alpha [deg.]	180	60
Mean [dB]	18.9	7.9
STD [dB]	1.56	2.1

sidelobe for each control voltage, the distribution of gain pattern variations at these critical points is investigated. The simulation, encompassing 1000 iterations, was executed with different control voltages. The resulting simulation outcomes, including the mean and standard deviation, when the control voltage is equal to 1.7V, are shown in Table 4.1. The graphs for the statistics analysis for peak and first sidelobe level (when Vctrl = 1.7 V) are also shown in Fig. 4.12(a) and Fig. 4.12(b), respectively.



((a))



((b))

Figure 4.12: Monte Carlo simulation results when Vctrl = 1.7 V at 22 GHz for (a) pattern's peak ($\phi = 180$) and (b) first sidelobe ($\phi = 60$).

4.3.5 Verifying Beamformer Stability

In each stage of the gain cell, the cascode configuration is used. Using this configuration significantly reduced the reverse gain and made the amplifier stages, to some extent, unilateral. Moreover, with a careful design of the biasing network of the gain stages, including the use of decoupling capacitors and minimizing the coupling between traces, the unintentional feedback paths are eliminated. To verify the stability of the beamformer, the stability factors of mu and mu-prime were obtained via simulation in Virtuoso cadence for each gain cell (gain cell 1 to gain cell 4) for different control voltages ($0.7V \leq V_{ctrl} \leq 1.7$). The simulation results show that these factors are greater than 1 over the frequency range from 1 GHz to 40 GHz. This condition ensures unconditional stability for the beamformer. The Mu and Mu-prime factors versus frequency are plotted where $V_{ctrl} = 1.2$ and presented in Fig. 4.13

4.3.6 Verifying Beamformer Linearity

In a CMOS varactor, applying negative biasing voltage (anode to cathode) makes the depletion region thicker. A thicker depletion region means the varactor is less affected by the RF signal, making it more linear. On the other hand, applying a positive biasing voltage makes the depletion region thinner, making the varactor more responsive to the RF signal. Consequently, the linearity of a CMOS varactor depends on its biasing voltage. In the proposed beamformer, our simulations show that the P1dB, a measure of linearity, is mainly affected by the gain cells. The simulation results indicate that the IP1dB of the transmission line is around 10 dBm, and the OP1dB of the gain cell is around -3 dBm. To verify this issue in simulation, we first found the 1 dB compression point of the beamformer by running a Periodic Steady State (PSS) simulation in Virtuoso Cadence at the mid-range frequency, 22 GHz. Based on the simulation results, it is found that the average input referred 1 dB compression point of the beamformer (IP1dB) is equal to -20.6 dBm.

In the next step, for a certain control voltage, the varactors of the beamformer are replaced by an equivalent R-C circuit which provides the same frequency response while being ideally linear. The S parameters simulation results show that the equivalent R-C circuit consists of a 2 Ohm resistor in series with a 223 fF capacitor.

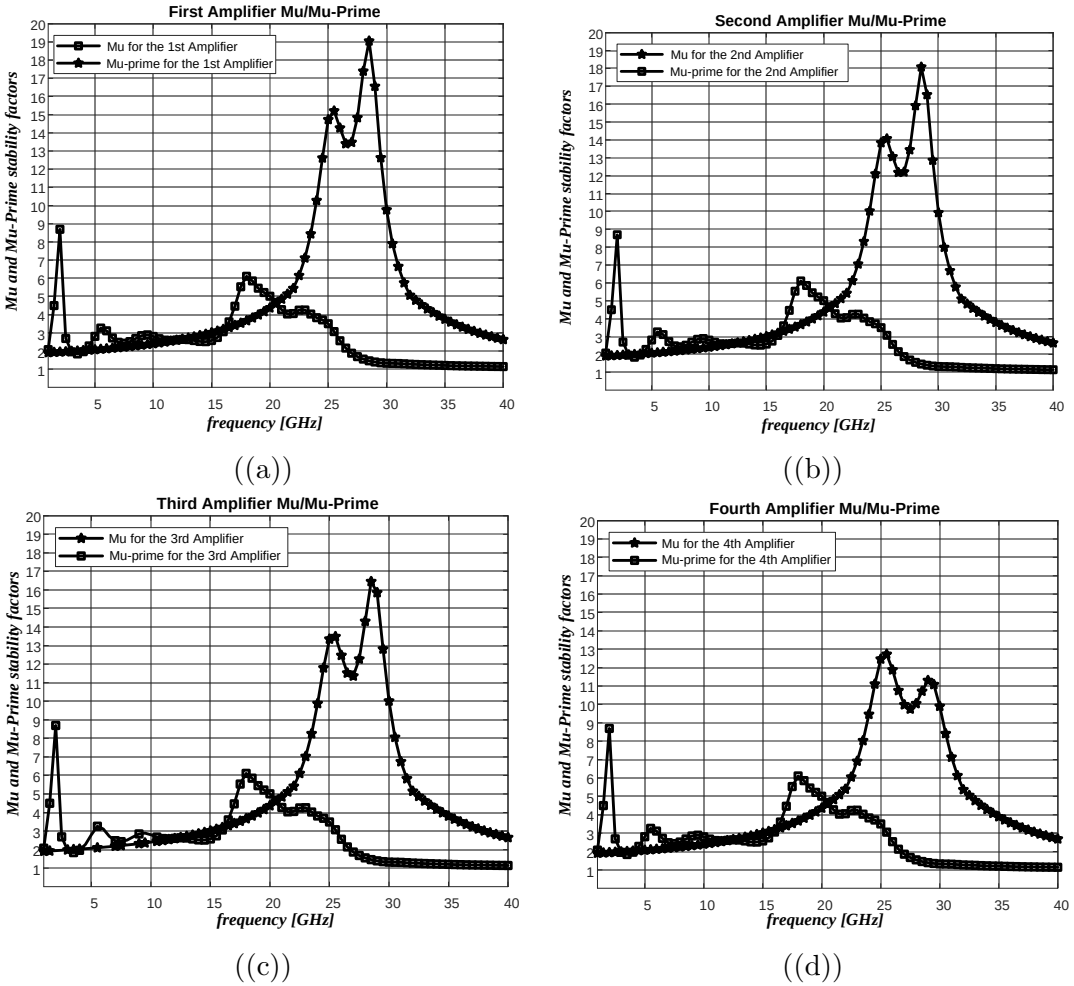


Figure 4.13: Mu and Mu-Prime vs. frequency when Vctrl = 1.2V for the (a) First, (b) Second, (b) Third, and (c) Fourth Amplifier.

Replacing varactors with such an ideal linear circuit removes the non-linearity effects of the varactors on the beamformer performance. Relaunching the pss simulation, it is investigated that the 1 dB compression point of the beamformer with idealized varactors remained approximately the same.

4.4 K-band Analog Beamformer Fabrication and Measurement Results

4.4.1 Tape-out and Fabrication

In the fabricated beamformer, the inductors of both Tunable-ATL and transconductance gain cells are implemented on the topmost metal layer (Metal 9) to obtain the

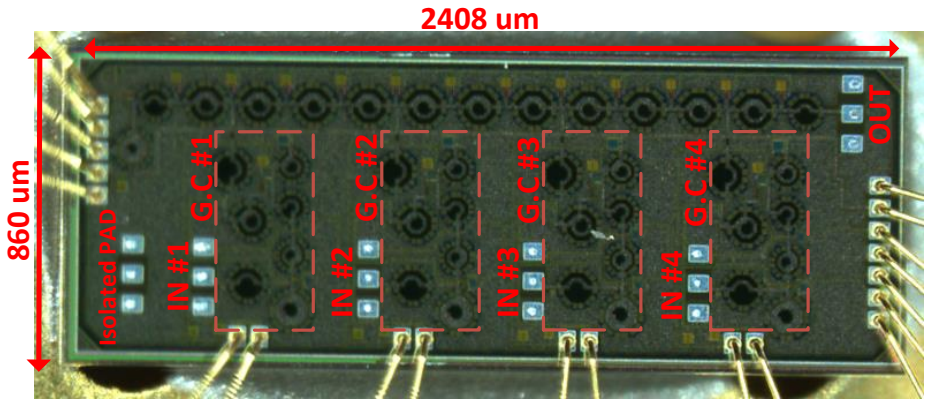


Figure 4.14: Implemented 4-element K-band analog beamformer in 65-nm CMOS technology.

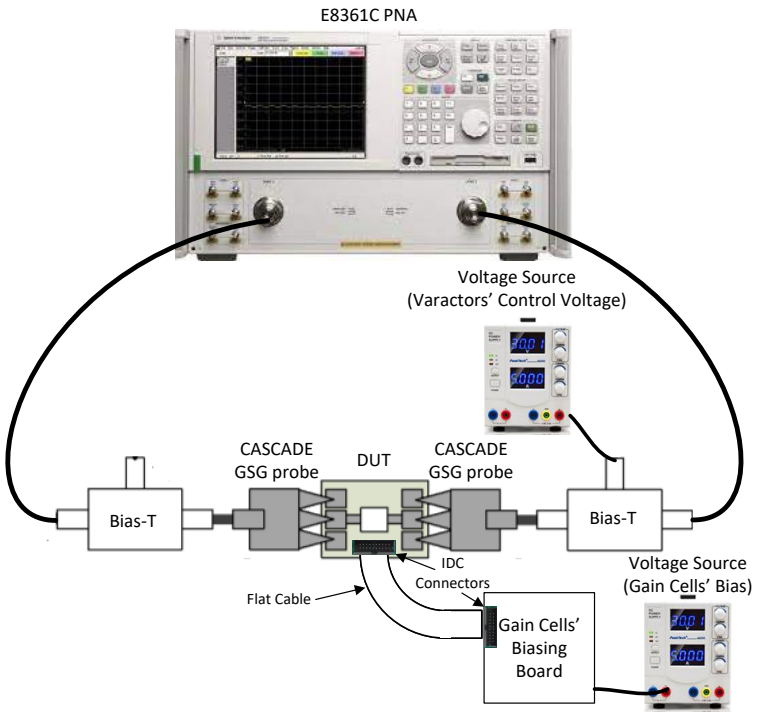
highest quality factor possible. To achieve the desired inductance value of 279 pH for all inductors in the Tunable-ATL cells over the operational bandwidth of 21 to 23 GHz, the trace width, radius, and the number of turns for all cells' inductors are chosen to be equal to 9 um, 21 um, and 1.5, respectively. The first and last inductors must have half the inductance value of the cells' inductor and thus, are implemented with the same trace width but with a radius of 18 um and 0.5 turn. Within the Tunable-ATL cells, the varactors are uniform, possessing the same number of groups (G), number of fingers (B), width (W), and length per finger (L), which are equal to 1, 32, 1 um, and 250 nm, respectively.

As mentioned previously, the transconductance gain cells also feature multiple inductors, with their respective inductance values provided in the table presented in Fig. 4.6(a). The radius and number of turns for each inductor in the gain cell are carefully selected to ensure a compact floor plan for the beamformer while maintaining acceptable performance levels. Fig. 4.14 shows the die microphotograph of the implemented beamformer in the standard 65-nm CMOS technology.

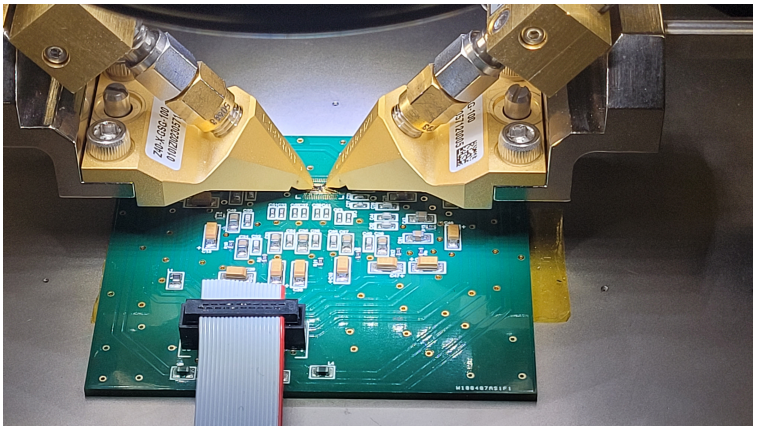
4.4.2 Measurements

To validate the performance of the fabricated beamformer experimentally, we first measured the S-parameters of the two-port networks of the beamformer, where the input port is one of the gain cell's input and the output port is the output port of the beamformer as simultaneous excitation of all four inputs is not possible. As can

be seen in Fig. 4.14, each transconductance gain cell in the fabricated chip is connected to a GSG pad, which serves as an input port for the gain cell. Additionally, the output transmission line is connected to another GSG pad (located at the top right), designated as the beamformer output. Using on-wafer probing through these GSG pads, four two-port S-parameter measurements can be performed to characterize the two-port networks formed between each gain cell's input and the beamformer output. In order to deembed the effect of the GSG pads on the performance of the beamformer, an isolated single GSG pad is also fabricated on the most left bottom of the chip, and its parasitic capacitance is measured by the same on-wafer probe. To conduct the S-parameter measurements, a Keysight E8361C PNA calibrated up to 40 GHz, employing the standard SOLT calibration kit, is utilized. The measurements are performed in conjunction with a CASCADE 110 GHz GSG probe station. It should be noted that to perform the S-parameter measurement, it is necessary to apply bias voltages to the gain cells and the control voltage to the varactors. To simplify the process of supplying bias voltages to the gain cells, the beamformer is mounted on a Printed Circuit Board (PCB), and the bias pads are connected to the board using wire bonding (see Fig. 4.15(b)). The required voltages for the PCB, depicted in Fig. 4.15, are provided through an Insulation Displacement Connector (IDC). However, the required control voltage for the varactors of the beamformer is applied via a wideband (up to 65 GHz) Bias Tee (SHF 65 BT) which is cascaded with the output probe. To demonstrate the matching performance of the output tunable transmission line of the beamformer, Fig. 4.16 plots the measured output return loss ($|S_{55}|$) for various bias conditions. Within the operational bandwidth of the beamformer, the output return loss ($|S_{55}|$) consistently remains in an acceptable range of less than -10 dB. This observation suggests effective control of the characteristic impedance variation in the output tunable transmission line across the entire control voltage range. The measured results of the two-port S-parameter measurements are plotted in Fig. 4.17. As can be seen, the gain cells are being matched in a wide frequency range (Return Loss is better than 10 dB over 19 to 28 GHz.). However, in the low control voltage values, where the varactors are forward biased and consequently the value of their capacitance is large, the gain of the gain cells is drastically reduced at higher frequencies. Specifically, the gain cell which has the farthest distance to the



((a))



((b))

Figure 4.15: (a) Block diagram of characterization setup for measuring beamformer's S-parameters and (b) Printed Circuit Board (PCB) of tested beamformer.

output (G.C 1) is more affected. This gain reduction is expected, as we know that by increasing the capacitance value of the ATL cells, their insertion loss is increased at higher frequencies [36]. In fact, this parameter practically restricts the upper limit of the beamformer's operational frequency. Two-port S-parameter measurement between each gain cell input pad and the output pad of the beamformer provides four sets of s2p files which are used to model the beamformer as a five-port network. Uti-

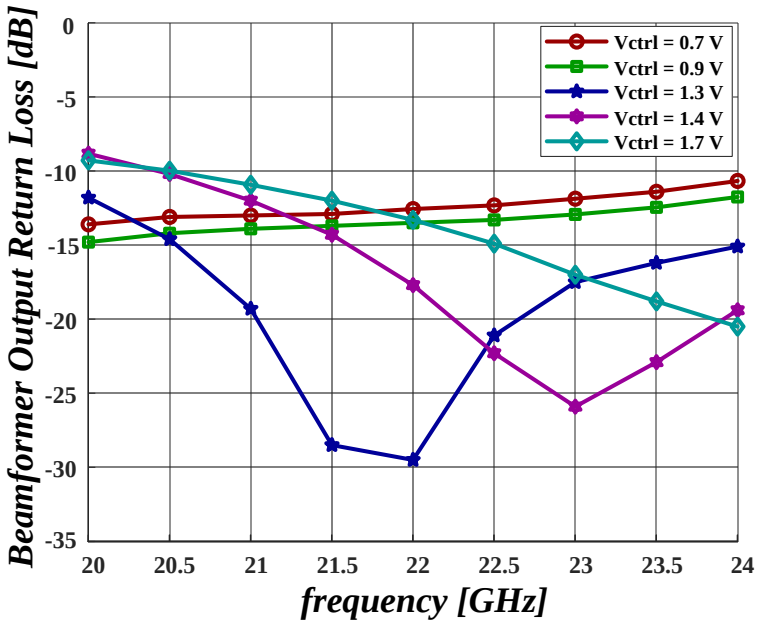


Figure 4.16: Measured output return loss ($|S_{55}|$) of beamformer at different biasing conditions.

lizing the generated s5p file for each given control voltage, the array factor of the beamformer can be calculated. The calculated array pattern for 22 GHz is sketched in Fig. 4.18. We used some simplifying assumptions in calculating and sketching the reconstructed pattern of the beamformer from the measured S-parameters data. First, we assumed that the array's antenna elements are of Omnidirectional type. As a result, we plotted the array factor rather than the array pattern. Next, we also assumed that the mutual coupling between the antenna elements is negligible. This implies that the array pattern, for any arbitrary antenna elements, can be calculated by multiplication of the array factors and the beam pattern of the antenna element.

The graphs show a good agreement between the measured results and the simulation results of the beamformer where the mutual coupling between cells is taken into account. The measured results show that by changing the varactors' control voltage from 0.7 to 1.7 V, the electrical length of the ATL cells varies about 110 degree. During this beam steering, the array gain is changed between 16 to 20 dB while the side lobe levels remain at least 10 dB less than the main lobe.

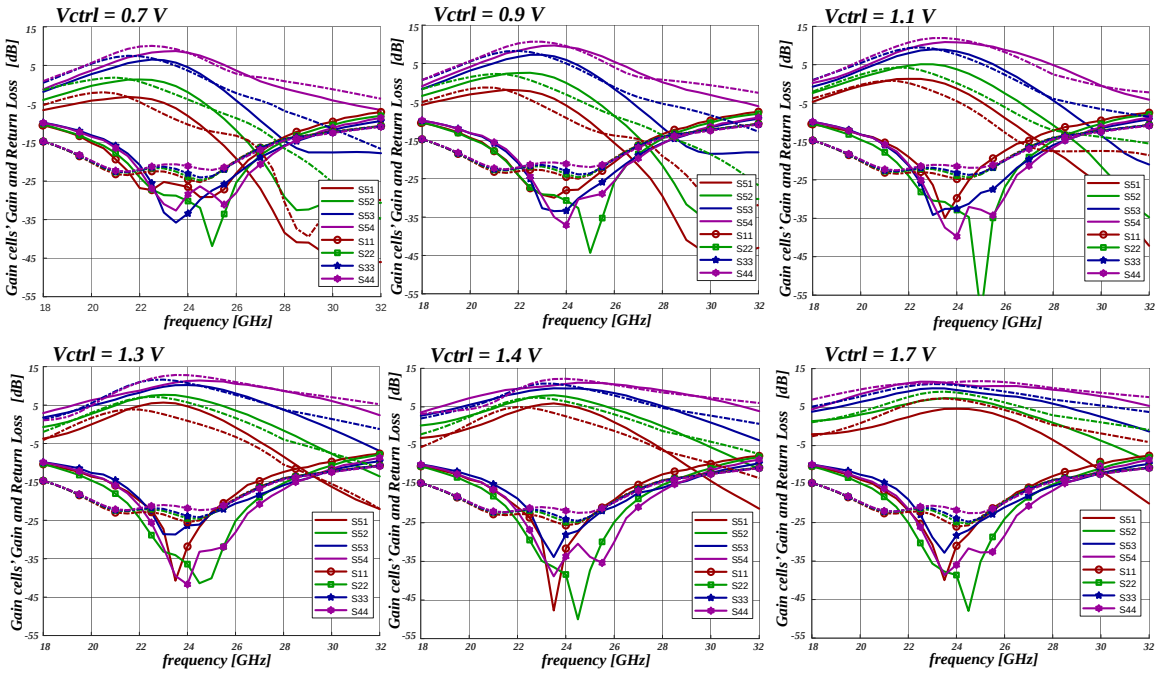


Figure 4.17: Measured (solid lines) and simulated (dotted lines) S parameters of fabricated beamformer.

4.4.3 Comparison to Other Work

In a phased array system, using a larger number of antenna elements (N_E) increases the array gain. In addition, it is highly desired that a phased array system be able to provide multiple simultaneous beams [40–42]. Therefore, the larger number of antenna elements (N_E) and the larger number of simultaneous beams (N_B) that a beamformer can support in a given die area, it would be considered a more cost-effective design. As a consequence, the $power/(N_E \times N_B)$ and $Area/(N_E \times N_B)$ can be defined as two FOMs that can used to evaluate the area efficiency of a phased array system with the smaller FOM showing the more efficient design.

In Fig. 4.2, it is shown that for a plane wave with an angle of arrival of θ, the phase difference between the output signals of the antenna elements of the array (α) will be progressive from left to right. However, if it is assumed that the angle of arrival is equal to $-\theta$, then the phase difference between output signals will be the same but the phase progression direction is reversed and it would be from right to left. On the other hand, it can be easily shown that if in the proposed beamformer (shown Fig. 4.3(b)) the phase progression direction is opposed, then by swapping the terminated and the

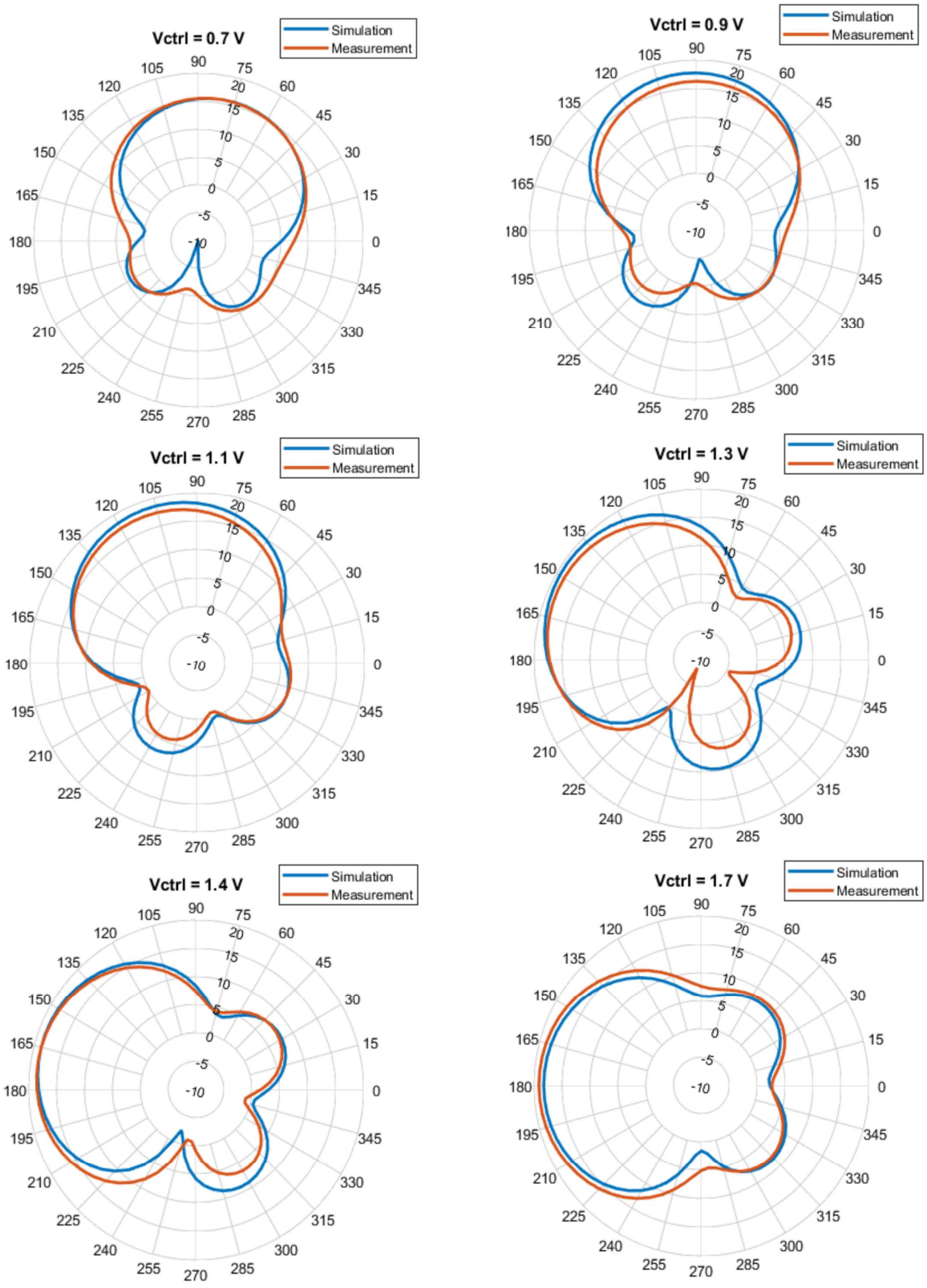


Figure 4.18: Simulated beamforming pattern based on measured and simulated S parameters of fabricated beamformer at 22 GHz

output end of the output tunable transmission line, the same beamforming results can be achieved. It means that by using both ends as two independent outputs, the proposed beamformer provides two simultaneous beams that direct to θ and $-\theta$ and can be steered by changing the control voltage of the varactors. Therefore, one can claim that in the proposed beamformer the number of simultaneous beams (N_B) is equal to two. Considering the above discussion, Table 4.2 summarizes the performance of the proposed design, and other millimeter wave beamformers (phased array systems) reported in the literature. The reported value of the area-efficiency FOM shows that the proposed design noticeably outperforms others while its power-efficiency FOM is ranked in the second place after [40]. Moreover, the proposed design achieved the Noise Figure of 5.1 dB and a measured input 1 dB compression point (P_{1dB}) of -18.5 dBm. In the scope of this work, we planned to develop a low-cost beamformer that can be utilized in cheap and low-power-consumption devices. Considering such applications, we defined reducing chip area and power consumption as the highest priorities for the proposed beamformer. Nonetheless, we expect that it also shows an acceptable performance in terms of gain, noise performance, and linearity. As an example in terms of P1dB our design got second place. However, the work with slightly better performance (less than 2 dB) consumes more than 5 times more power [43]. A similar situation can be seen regarding the gain and noise figure performance. First, it should be noted that the arrays introduced in [42] and [14] have 8 antenna elements. Consequently, in comparison to the other works (including our proposed beamformer) which have 4 antenna elements, they inherently have 6 dB more gain. Subtracting this excess gain shows that their gain performance is slightly better than our work. Second, in all three works that have higher gain and better (or comparable) noise performance (including [14, 41, 42]) the power efficiency FOM is at least 3 times worse than of our proposed circuit. Furthermore, in terms of chip area efficiency FOM, they show 2.5 to 28 times worse performance. Finally, to make a fair comparison between the amount of achieved phase range in different works, we introduced a new FOM which is named "Normalized Phase Range" (NPR) and can

Table 4.2: Comparison table with related research works.

	This work	**[42]**	**[40]**	**[41]**	**[14]**	**[43]**	**[58]**
Technology	**CMOS 65nm**	CMOS 65nm	CMOS 65nm	CMOS 65nm	CMOS 65nm	SiGe 120nm	CMOS 65nm
Frequency Range (GHz)	**21-23**	27.5-32	27-31	17.7-20.2	17.7-19.2	26-30	22-37
Architecture	**RX**	RX	RX	RX	RX	TRX	RX
RX Building Blocks	**LNA+PS$^{(a)}$+PCN$^{(b)}$**	LNA+PS+PCN	LNA+PS+PCN	LNA+PS+PCN	LNA+PS+PCN	LNA+PS+PCN	LNA+PS
$N_B^{(c)} \times N_E^{(d)}$	**2×4**	4×8	2×4	1×8	2×8	4×1	N/A
Gain (dB)	**18****	26.7	3	20.3	28	6.2-8.3	14.8
NF (dB)	**5.1***	3.7-4.5	10.8-11.7	1.7-2.1	3.2-4.1	4.9-7.3	2.5
P1dB (dBm)	**-18.5** **	-32.5	-22	-42	-27.4	-16.7	-22
Phase Range/Res. (deg)	**110/Cont.**	360/5.625	360/5.625	360/5.625	360/2.8125	360/11.25	174/Cont.
Power Consumption (mW)	**90**	1115.8	40	241.6	595.2	500	N/A
Area (mm^2)	**2.05**	21.2	10.4	57	12.88	8.7***	N/A
Power/($N_B \times N_E$) (mW)	**11.25**	34.9	5	30.2	37.2	125	21
Area/($N_B \times N_E$) (mm^2)	**0.256**	0.663	1.3	7.125	0.805	2.175 ***	0.48****
NPR ($degree/mm^2$)	**430**	543	277	50.5	447	166	362.5****

$^{(a)}$ Phase Shifter $^{(b)}$ Power Combining Network $^{(c)}$ Number of Beams $^{(d)}$ Number of Elements

* Simulation results

** Measurement at the mid-band

*** Including TX Power Amplifier

**** Power Combining Network is not included

be calculated as:

$$NPR = \frac{PhaseRange}{\frac{Area}{N_E \times N_B}} \ [\frac{degree}{mm^2}]. \tag{4.43}$$

The calculated values of NPR show that the proposed circuit takes third place after [42] and [14] while it provides a continuous phase shift (infinite resolution) with at least 3 times better power efficiency.

4.4.4 Discussion and Future Work

In the project's initial phase, the decision was made to utilize the unlicensed Industrial, Scientific, and Medical (ISM) band at 24 GHz for eventual testing of a complete phased array system with an antenna array. However, the realized beamformer functioned within the 21-23 GHz frequency range. Upon investigating this frequency deficiency, it was determined that the oversight of mutual coupling effects among output transmission line inductors led to this discrepancy. Our focus will be on the n258 channel within Frequency Range 2 of 5G New Radio (5G NR), encompassing the 24.25 – 27.50 GHz spectrum [59].

Additionally, by custom design of the array's antenna element impedance, we aim to alleviate the matching constraints between the antenna elements and the gain cells. It is anticipated that achieving this matching criterion will contribute to the enhanced

power efficiency and overall performance of the beamformer in terms of both power consumption and operational capabilities. Moreover, a marginal enhancement can be attained by refining the quality factor of fabricated varactors through their parallel integration with Wideband Negative Capacitors (WNC) [60].

Chapter 5

Conclusions and Future Work

5.1 Summary of Contributions

The rising demand for high-data-rate services has led to increased congestion in traditional low-GHz RF wireless communication channels. To alleviate this bandwidth shortage, higher-frequency bands, like millimeter-wave and sub-THz frequencies, are used. However, these higher-frequency signals suffer from greater path losses, limiting their communication range. Directional and phased array antennas have emerged as solutions to this challenge, enabling the focused transmission or reception of signals in specific directions to extend the communication range. Phased array systems, utilizing techniques known as beamforming, adjust phase shifts between antenna elements to create directional beams. Their advantages include faster response times, greater flexibility, and smaller form factors compared to mechanical alternatives, making them popular in various wireless applications. Moreover, there is a growing demand for energy-efficient and compact phased array systems to make them more suitable for use in applications in which battery life and device sizes are the main concerns, ranging from handheld 5G/6G devices to UAV and satellite communication equipment. This study proposes innovative circuit solutions to meet this demand, addressing RF analog beamforming and exploring methods to improve power efficiency and reduce chip size.

As the first contribution in this work, a Tapered TTL phase shifter is proposed that achieves a higher area efficiency than conventional TTL phase shifters while maintaining similar insertion loss and phase shift range. A systematic methodology is provided for the optimum design of the proposed phase shifter to maximize its area

efficiency while providing the desired phase shift range and satisfying the maximum allowed input/output return and insertion losses. To verify the efficacy of the proposed solution, an eleven-stage phase shifter is fabricated in a standard 65-nm CMOS technology and the measurement results are reported. The fabricated circuit provides 180 degree phase shift over the frequency range of 16.5 to 33 GHz with an average insertion loss of 7.2 dB. The proposed design presents 25 percent reduction in the chip area per unit delay in comparison to the conventional design with the same average insertion loss.

As the second contribution, we proposed an area and power-efficient Pseudo-DA beamforming architecture capable of supporting two simultaneous beams. The proposed beamformer is constructed by removing the input transmission line of a DA to directly connect the gain cells to the antenna elements of a phased array and utilizing Tunable-ATL cells of DA's output transmission line for creating the required progressive phase shifts. Using both ends of the output transmission line, two simultaneous beams can be obtained. The first beam can be steered independently while the other one is formed as an image of the first one. In this paper, the theory of operation and the design methodology of the proposed beamformer are presented. In addition, to verify the efficacy of the proposed solution a K-band four-element prototype is fabricated in a standard 65-nm CMOS technology and the measurement results are reported. The fabricated beamformer provides 110 degree beam steering over 21 to 23 GHz frequency range. The measured gain, Noise Figure, and 1dB compression point (P_{1dB}) are 18 dB, 5.1 dB, and -18.5 dBm, respectively, with 90-mW dc power consumption and a chip area of 2.05 mm^2.

5.2 Future Work

As future work, one could go one step further to construct a complete phased array system incorporating our new Pseudo-DA beamformer. In this work, the antenna elements (small dipoles) will be directly connected to the gain cells of the beamformer (Shown in Fig. 5.1). The proposed scheme provides the following benefits:

1. The input matching network is no longer required. Since it is assumed that the dipoles are small, the input impedance of the antenna elements can be estimated by a

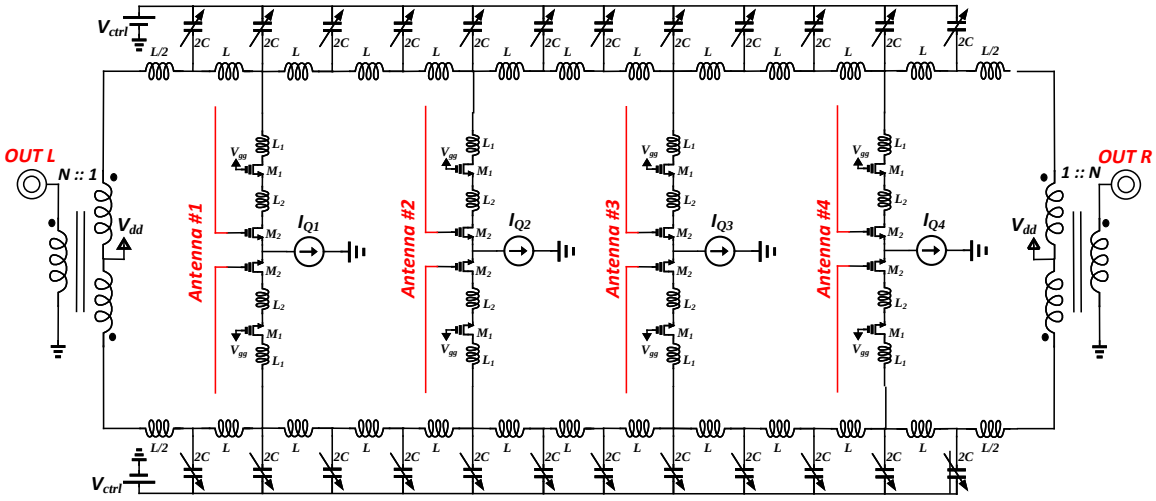


Figure 5.1: Proposed four-element phased array system

small capacitor. Consequently, the open circuit voltage (V_{OC}) induced by the receiving wave will be divided between this capacitance and C_{gg} of the input transistor. This pure capacitive voltage division will provide a wideband flat frequency response.

2. Since the input matching is no longer needed, the replacement of input configuration from common gate to the common source provides the capability of better noise performance and higher gain.

3. The differential architecture of the gain cells eliminates the need for an input balun for the antenna elements.

4. By choosing the proper turn ratio for the transformers, the characteristic impedance, and eventually the inductance value of the Tunable-ATL cells can be reduced. This could help to produce a more compact design and may improve the gain performance.

5. By independently controlling the tail current of the gain cells, the gain of each gain cell can be varied individually. This capability allows for the examination of nonuniform and uniform tapering as well as uniform tapering in the phased array system.

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