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THE UNIVERSITY OF ALBERTA

TECHNIQUES FOR THE REDUCTION OF DS-1 JITTER CAUSED BY SONET VT1.5 POINTER ADJUSTMENTS

BY

RICHARD GLENN KUSYK

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND RESEARCH IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

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29 August 1990

Date

To my family,

for their support, encouragement and patience.

ABSTRACT

In the past decade, fibre optical transmission systems have become common in telecommunication networks. Fibre has many advantages over coaxial cable and twisted pair transmission media, such as very low loss, large bandwidth, and no RF interference. Until recently, there has been no common signal format for optical fibre systems, resulting in the development of many different proprietary systems. SONET (Synchronous Optical NETwork) is a newly adopted signal format which exploits the advantages of optical fibre systems and allows transmission equipment from different vendors to be used interchangeably in a network. Synchronization in SONET is accomplished using payload pointers and envelope mechanisms. Both positive and negative pointer adjustments are used in the synchronization of VT1.5 payload envelopes.

This thesis examines the jitter impact of pointer adjustments occurring at the VT1.5 level on DS-1 signals carried in SONET. Theoretical analyses are developed and simulations are used to predict DS-1 jitter when pointer adjustments occur. Methods of reducing the DS-1 jitter caused by pointer adjustments are also examined. These jitter reduction techniques include fixed rate, variable rate, and feed forward pointer spreading, as well as stuff threshold modulation. For each of these techniques, theoretical analyses are developed and simulations are used to predict DS-1 jitter. Finally, these jitter reduction techniques are evaluated and compared based on jitter performance.

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LIST OF ABBREVIATIONS

ABBREVIATION	DESCRIPTION
+/0/-	Plus/zero/minus
CCITT	International Telephone and Telegraph Consultative Committee
D bits	Decrement bits
dB	Decibels
dc	Direct current
demap.	Demapper
desynch.	Desynchronizer
DS-1	Digital Signal level 1
ECSA	Exchange Carriers Standards Association
Eqn.	Equation
Fig.	Figure
HPF	High Pass Filter
Hz	Hertz
I bits	Increment bits
IIR	Infinite Impulse Response
kHz	Kilohertz
Mb/s	Megabits per second
μsec	Microseconds
NDF	New Data Flag
OC-N	Optical Carrier level N
PLL	Phase-Locked Loop
ppm	Parts per million
rad/s	Radians per second
RF	Radio Frequency

ABBREVIATION	DESCRIPTION

rms ..... Root mean squared

SONET..... Synchronous Optical Network

SPE..... Synchronous Payload Envelope

STM ..... Stuff Threshold Modulation

STS-N ..... Synchronous Transport Signal level N

synch..... Synchronizer

T ..... Stuff threshold

TDM..... Time Division Multiplexing

UI..... Unit Intervals

VTn ..... Virtual Tributary level n

LIST OF SYMBOLS

SYMBOL	DESCRIPTION
α	Leak period of fixed rate pointer spreader
β	Magnitude of fractional phase step
BRO(n)	Bit-reversed order of n
f_m	Stuff opportunity frequency
f_r	Read clock frequency
f_w	Write clock frequency
H(s)	Analog frequency response
H(z)	Digital frequency response
$H_{aps}(f)$	Equivalent transfer function of running average pointer spreader
$h_{aps}(t)$	Equivalent impulse response of running average pointer spreader
$H_{fps}(f)$	Equivalent transfer function of fixed rate pointer spreader
$h_{fps}(t)$	Equivalent impulse response of fixed rate pointer spreader
$H_{vps}(f)$	Equivalent transfer function of variable rate pointer spreader
$h_{vps}(t)$	Equivalent impulse response of variable rate pointer spreader
K	Magnitude of phase step
$\mu(t)$	t mod 1
N	Number of threshold levels in STM synchronizer
ν	VT1.5 offset frequency
ρ	Stuff ratio
p	Pointer value
t	Time
T_n	Threshold levels
τ_n	Time that the nth fractional phase step is leaked out
T_s	Time interval between samples

$\Phi_d(s)$ ..... Laplace transform of desynchronizer step response

$\phi_d(t)$ ..... Desynchronizer step response

$\Phi_{ffps}(f)$ ..... Fourier transform of waiting time jitter waveform with feed forward pointer spreading

$\phi_{ffps}(t)$ ..... Waiting time jitter waveform with feed forward pointer spreading

$\Phi_{fps}(f)$ ..... Fourier transform of waiting time jitter waveform with fixed rate pointer spreading

$\phi_{fps}(t)$ ..... Waiting time jitter waveform with fixed rate pointer spreading

$\Phi_s(f)$ ..... Fourier transform of waiting time jitter with +/0/- synchronizer

$\phi_s(t)$ ..... Waiting time jitter waveform with +/0/- synchronizer

$\Phi_{vps}(f)$ ..... Fourier transform of waiting time jitter waveform with variable rate pointer spreading

$\Phi_{vps}(f)$ ..... Fourier transform of waiting time jitter waveform with STM synchronizer

$\phi_{vps}(t)$ ..... Waiting time jitter waveform with STM synchronizer

$\phi_{vps}(t)$ ..... Waiting time jitter waveform with variable rate pointer spreading

x(n) ..... Input sample to digital filter

ω_c ..... 3 dB frequency in rad/s

Ω_c ..... 3 dB normalized digital frequency

ω_{HPF} ..... 3 dB frequency of HPF

ω_{PLL} ..... 3 dB frequency of PLL

y(n) ..... Output sample from digital filter

I. INTRODUCTION

In the past decade, fibre optical transmission systems have become much more common in telecommunication networks. Fibre has many advantages over coaxial cable and twisted pair transmission media, such as very low loss, large bandwidth, and no RF (radio frequency) interference. Until recently, there has been no signal standard for fibre systems and the result has been the development of many different proprietary systems. SONET (Synchronous Optical NETwork) is a newly adopted signal format [1-4] which uses the advantages of fibre systems, and allows transmission equipment from different vendors to be used interchangeably in a network. This thesis concentrates on the reduction of jitter caused by a synchronization technique referred to as pointer processing [5] which is exclusive to SONET. This Chapter provides a background on jitter, SONET, and pointers, along with a description of previous work done on jitter reduction techniques.

i. Waiting Time Jitter

Digital Time Division Multiplexing (TDM) is a technique of interleaving several low bit rate digital signals to produce one high bit rate signal, which can then be efficiently utilized on a high speed transmission facility [6]. In the transmitter, bits from each of the low bit rate signals, or tributaries, are sent out alternately on the high bit rate line. The receiver separates this high bit rate signal into the original low bit rate signals with the help of a framing pattern imbedded in the high bit rate signal. A considerable problem associated with TDM is the synchronization of plesiochronous, low bit rate signals before they are interleaved [6]. Plesiochronous signals have the same nominal bit rate, but because they are generated from different timing sources, their actual bit rates are not identical.

Variations between the actual bit rate and the nominal bit rate are maintained within a specified tolerance.

A common method of synchronization used in the existing North American digital hierarchy and in SONET is pulse stuffing [1-4,6]. A block diagram of a typical pulse stuffing synchronizer is shown in Fig. 1-1. The data from a low rate plesiochronous tributary is first written into an elastic store using a write clock derived from the low rate signal. The data is then read out from the elastic store using a read clock from the multiplexer, which operates at a slightly higher rate than the write clock. A phase comparator is used to measure the phase difference between the read and write clocks. Because the read clock operates at a higher rate than the write clock, the phase difference between the two clocks increases. To prevent the read clock from overtaking the write clock, the read clock is inhibited by stuffing control logic whenever the phase comparator output passes beyond a specified stuff threshold. This process results in an output data stream that contains occasional stuff, or dummy, bits. These stuff bits are only allowed at designated locations in the frame format, called stuff opportunities, to facilitate their identification and removal at the desynchronizer. Therefore, there is

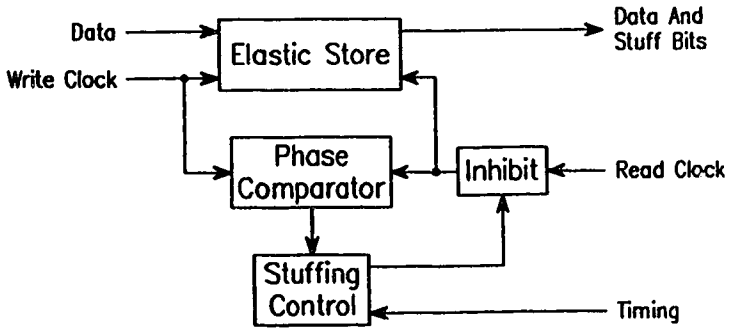

Fig. 1-1 Pulse stuffing synchronizer block diagram.

a delay, or waiting time, between the time that the phase comparator output passes the stuff threshold and the time that a pulse is stuffed. A timing signal from the multiplexer is used to signal the stuffing control logic when a stuff opportunity occurs. An example of a plesiochronous input pulse stream and the corresponding synchronized output stream containing stuffed pulses is shown in Fig. 1-2. Once all of the low rate signals have been synchronized in this manner to the common read clock, they can be interleaved in time to produce the high rate signal.

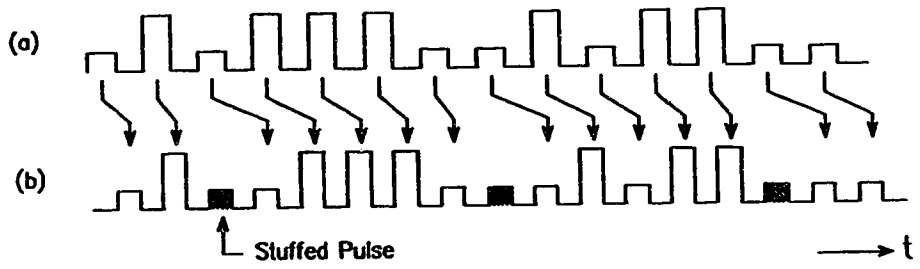

Fig. 1-2 Example of pulse stuffing synchronization.
(a) Original plesiochronous signal.
(b) Synchronous signal with stuffed pulses to be multiplexed.

A fundamental impairment that results from the use of pulse stuffing synchronization is jitter, which is defined as the variation of the significant instants of a clock from the significant instants of an ideal clock with the same average bit rate [6]. Pulse stuffing produces two forms of jitter. The first is the obvious one time slot of stuffing jitter which is produced each time a pulse is stuffed. The second is a more subtle form of jitter which is produced because pulse stuffing can only occur at stuff opportunities within the multiplexing frame format. In practice, there is no distinction made between these two forms and the total jitter is referred to as waiting time jitter. In this thesis we are concerned with the waiting

time jitter that arises because of a single multiplexing and demultiplexing operation, assuming a jitter free write clock at the synchronizer. This process is called jitter generation and the source of the jitter for this case is the pulse stuffing synchronizer. Jitter caused by the synchronization and desynchronization process is analyzed by studying the output waveform of the phase comparator at the synchronizer. This waveform is called the waiting time jitter waveform and a typical example is shown in Fig. 1-3 for the case of a jitter free write clock. The phase difference between the read and write clocks is shown by the solid line and the stuff threshold T is shown by the dotted line. By convention, the jitter waveform is defined as the read clock phase minus the write clock phase and is normalized to read clock Unit Intervals (UI). A UI of a particular clock is equal to the average period of that clock. Because the read clock operates at a slightly higher rate than the write clock, the phase difference between the read and write clocks increases linearly. After this phase difference passes the stuff threshold, a pulse is stuffed at the next available stuffing opportunity, causing the phase to decrease by one read clock UI.

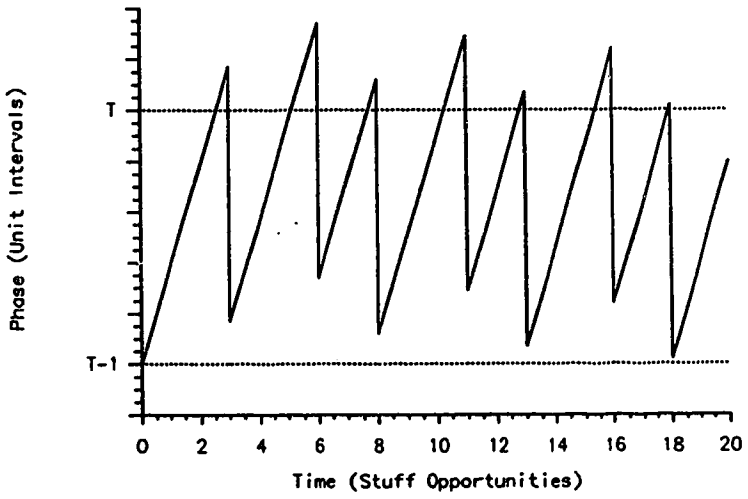

Fig. 1-3 Waiting time jitter waveform.

After the signals are synchronized, they are multiplexed and transmitted over the network to the receiver. At the receiver a desynchronizer is used after the demultiplexing operation in an attempt to recover the original tributary clock. A block diagram of a typical desynchronizer is shown in Fig. 1-4. At the demultiplexer, the high rate signal is first demultiplexed into the original synchronized low rate signals and then stuffing bits are removed, which causes gaps in their respective clock signals. The resulting gapped clock of any one tributary is used to write the data into the elastic store of the desynchronizer. A PLL (Phase-Locked Loop) is used to create a smoothed read clock that will have the same average bit rate as the original write clock at the synchronizer but the significant instances will contain some jitter. Under normal network conditions, the PLL operates linearly and therefore acts as a low pass filter on the waiting time jitter waveform [7-9] and therefore the output jitter on the read clock of the desynchronizer is a filtered version of the waiting time jitter waveform. Duttweiler [8] and Chow [9] have calculated the power spectral density and Fourier transform respectively of waiting time jitter. They found that the waiting time jitter waveform has arbitrarily low frequency components, making it impossible for all of the jitter to be removed by the PLL, which has a finite bandwidth. They also

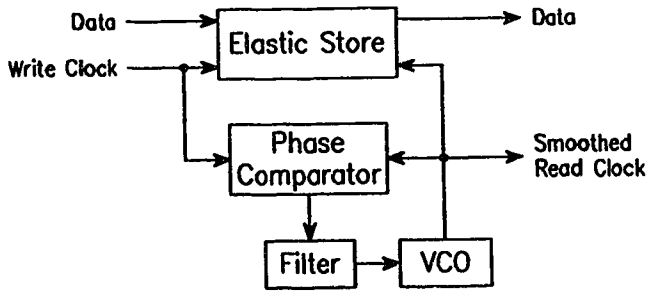

Fig. 1-4 Desynchronizer block diagram.

calculated waiting time jitter levels versus the stuff ratio, which they defined as the fraction of stuff opportunities that contain a dummy bit. From these results they found that the worst stuff ratios in terms of jitter performance occur near zero, one, and simple fractions such as one third.

ii. SONET

The Exchange Carriers Standards Association (ECSA) and the International Telephone and Telegraph Consultative Committee (CCITT) have adopted a new optical multiplex signal format known as SONET (Synchronous Optical Network) [1-4]. This new signal standard has many advantages [10,11] over the existing North American digital multiplex hierarchy, presently employed in Canada, United States, and Japan, such as flexibility to transport many different services. There is a desire in the industry to introduce SONET-based equipment into the network, but because of the large amount of capital invested in existing equipment it will take some time for the network to become fully SONET-based. Currently, there is a need for interface circuits that will allow signals from the existing multiplex hierarchy to be transported in SONET.

The SONET network is logically broken up into section, line, and path layers. A block diagram of a possible network configuration illustrating these layers is shown in Fig. 1-5. Each end of the network contains a muldem which contains both a multiplexer and demultiplexer and provides two-way communication. Services, such as a DS-1, are mapped into and out of a high rate SONET signal at these points. An add-drop muldem is also shown which is used access to specific services without terminating the high rate SONET section layer of the SONET network performs the transport of an OC-N al Carrier level N) across the physical medium and exists between all network elements including regenerators. The line layer performs the transport of

payloads and their overhead across the physical medium and exists between all network elements except for regenerators. The highest level layer is the path layer which transports services such as a DS-1 through the network. Each layer of the SONET network has overhead exclusively associated with it. Section overhead is used to provide framing, scrambling, and section error monitoring. Line overhead is used to provide synchronization and multiplexing functions. Path overhead is used to map services into payload formats.

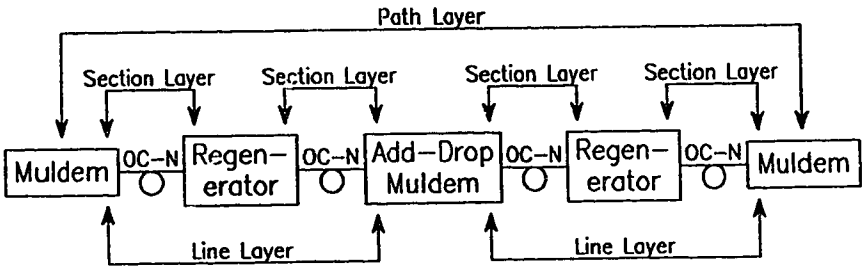

Fig. 1-5 SONET network example illustrating section, line, and path layers.

The OC-N optical signals in the SONET network have corresponding electrical signals referred to as STS-N (Synchronous Transport Signal Level N). The STS-1 [1] is the basic electrical signal in the SONET digital hierarchy which operates at a nominal bit rate of 51.84 Mb/s. The structure of this signal format, shown in Fig. 1-6, is based on a 90 column by 9 row frame of 8 bit bytes. Bytes are transmitted row by row from top to bottom, with each row being transmitted from left to right. Transport overhead is located in the first three columns of the STS-1 frame format and the remaining 87 columns form the Synchronous Payload Envelope (SPE) capacity. The first three rows of transport overhead are section overhead, and the remaining transport overhead is line overhead. Framing of the SPE in the STS-1 is accomplished by setting the payload pointer, part of the line

overhead, to the address of the first byte of the SPE frame. Valid pointer values range from 0 to 782, each of which corresponds to a specific byte within the SPE capacity of the STS-1 frame. By using this pointer, framing of the SPE can be accomplished immediately after framing of the STS-1 is established. Synchronization of the SPE to the STS-1 is accomplished with the use of the positive and negative stuff locations as well as the payload pointer. Synchronization using the payload pointer is described in the next section.

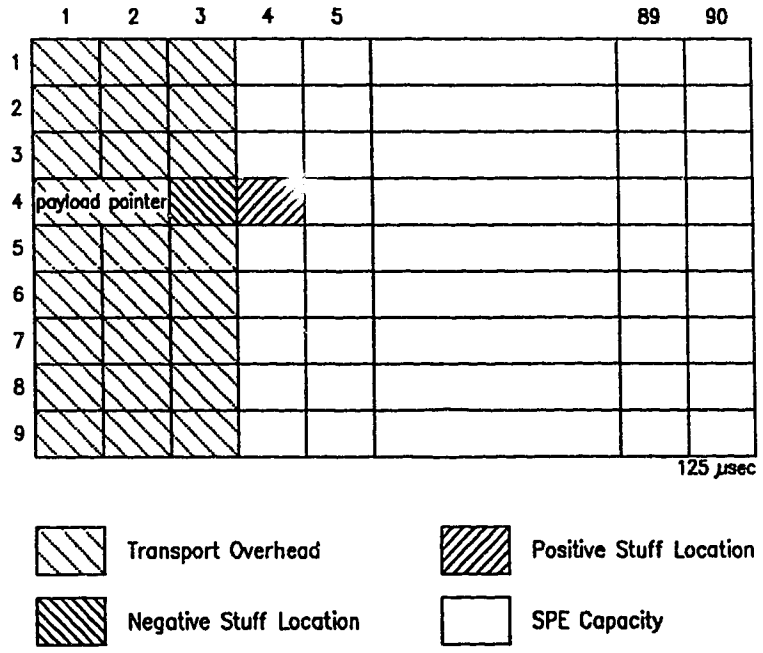

Fig. 1-6 STS-1 signal format.

Virtual tributaries (VT) were introduced into the SONET standard to accommodate signals with rates lower than the STS-1 SPE rate of 50.112 Mb/s. Standard VT sizes are the VT1.5, VT2, VT3, and VT6 which have equivalent transmission rates of 1.728 Mb/s, 2.304 Mb/s, 3.456 Mb/s, and 6.912 Mb/s respectively. In this thesis we are concerned with the VT1.5 which is used to

transport DS-1 signals in SONET. The VT1.5 signal format, as shown in Fig. 1-7, consists of a 27 column by 4 row frame with a period of 500 μsec. The first column of the frame consists of VT overhead, including a payload pointer analogous to the one used in the STS-1. The remaining columns are used to transmit the 26 column by 4 row VT1.5 SPE. The VT1.5 SPE is synchronized to the VT1.5 by both positive and negative byte stuffing and pointer processing analogous to that used in the STS-1.

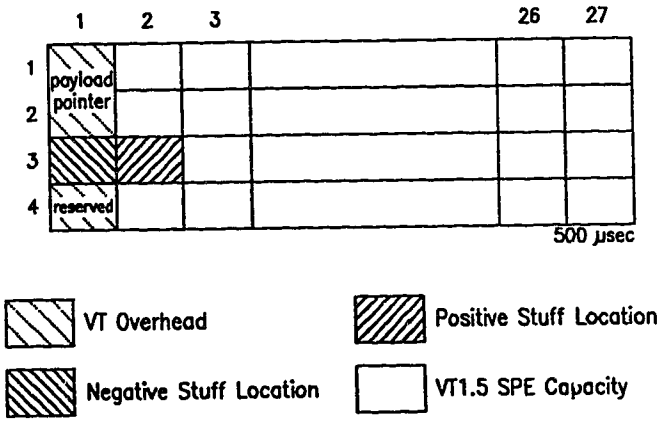

Fig. 1-7 VT1.5 signal format.

Bytes from 28 VT1.5 signals are interleaved along with STS-1 path overhead and fixed stuffs to form a VT structured STS-1 SPE, as shown in Fig. 1-8, which can then be transmitted via a STS-1. STS-1 path overhead is placed in the first column of the VT structured STS-1 SPE, and fixed stuffs are placed in columns 30 and 59. Each row of the STS-1 SPE contains three bytes from each of the VT1.5 signals. The first byte of the VT1.5 frame is placed in the first available byte of the STS-1 SPE allocated for that VT1.5. Using these VT1.5 signals, 28 DS-1 tributaries can be transmitted in a STS-1.

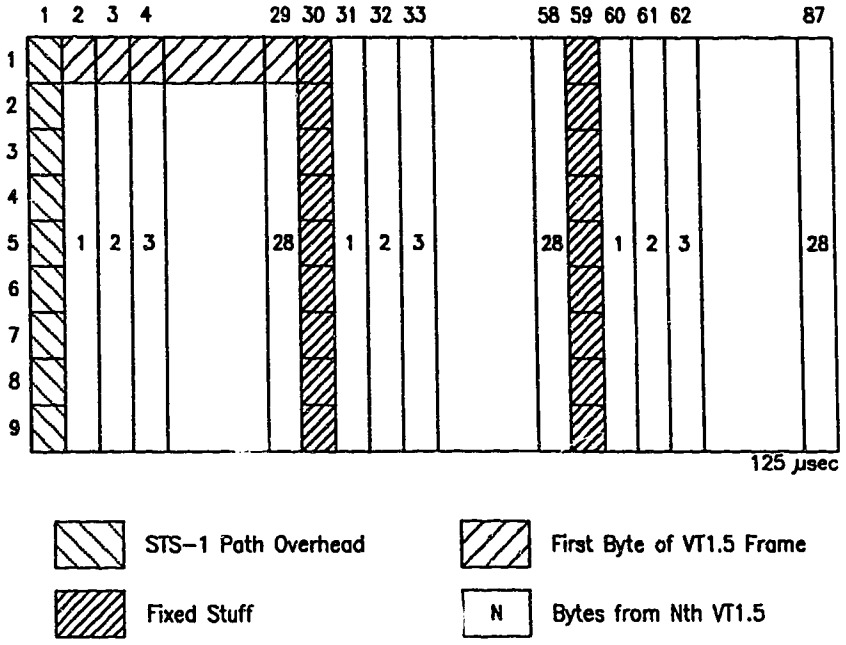

Fig. 1-8 VT structured STS-1 SPE with all VT1.5.

For our purposes, a DS-1 will be considered as a generic data stream, and therefore, the DS-1 signal format is not discussed here in detail. Important characteristics of the DS-1 signal format are the nominal bit rate which is 1.544 Mb/s and the bit rate tolerance which is ±130 ppm. Also important is the amount of jitter that is allowed on a DS-1 signal. A recommendation for maximum jitter generation has been issued by the CCITT which states that the jitter on a DS-1 signal after a single synchronization and desynchronization process be less than 1.0 UI peak to peak and 0.3 UI rms [12].

The format used for mapping a DS-1 into the SONET VT1.5 SPE, which consists of a 26 column by 4 row frame, is shown in Fig. 1-9. Path overhead and fixed stuffs are placed in the first column. The second column contains various bits including two stuff opportunity time slots and three DS-1 information bits. Two sets of stuff control bits are used in conjunction with the two stuff opportunity time slots to synchronize the DS-1 to the VT1.5 SPE. If the DS-1 is at the nominal

bit rate of 1.544 Mb/s, one stuff opportunity, S_1, will always contain a stuff bit and the other stuff opportunity, S_2, will always contain a data bit. This condition is referred to as a zero stuff ratio. When the DS-1 bit rate is higher than nominal, S_1 will occasionally contain a data bit. The stuff ratio for this case will be negative with a magnitude equal to the fraction of S_1 time slots that contain a data bit. Similarly, when the DS-1 bit rate is lower than nominal, S_2 will occasionally contain a stuff bit. For this case, the stuff ratio will be positive with a magnitude equal to the fraction of S_2 time slots that contain a dummy bit.

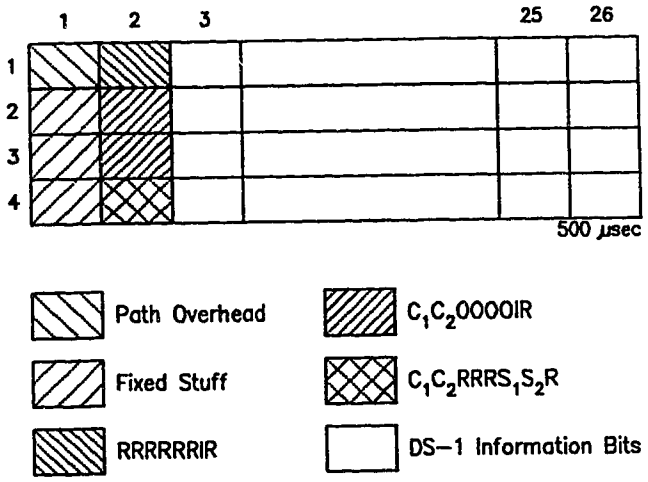

Fig. 1-9 Asynchronous mapping for DS-1 payload into VT1.5 SPE.
C - stuff control bit, I - DS-1 information bit,
O - overhead bit, R - fixed stuff bit,
S - stuff opportunity bit.

As described above, the nominal stuff ratio for DS-1 mapping into VT1.5 SPE is zero. As Duttweiler and Chow have found, stuff ratios near zero produce the worst case jitter. Stuff Threshold Modulation (STM) [13-15] is a technique which has been developed to reduce jitter when the stuff ratio is near zero and involves the manipulation of the stuff threshold level in the synchronizer. For the

mapping of DS-1 into a VT1.5 SPE, single sided STM is used. The stuff opportunity S_1 is set to a fixed pattern where one out of four stuff opportunities is a data bit. The other stuff opportunity S_2 is controlled by a modulated stuff threshold. The resulting waiting time jitter waveform is shown in Fig. 1-10 where the stuff threshold is shown by the dotted line and the output of the phase comparator is shown by the solid line. Positive phase jumps occur after every four stuff opportunities and are caused by the fixed pattern of S_1. The negative jumps are caused by a stuff bit in S_2 which occurs when the phase passes the stuff threshold. The waiting time jitter waveform that results when STM is used contains less power at low frequencies than the waiting time jitter waveform when STM is not used [13-15]. Therefore, after the desynchronizing PLL which acts as a low pass filter, the jitter with STM is less than the jitter without STM.

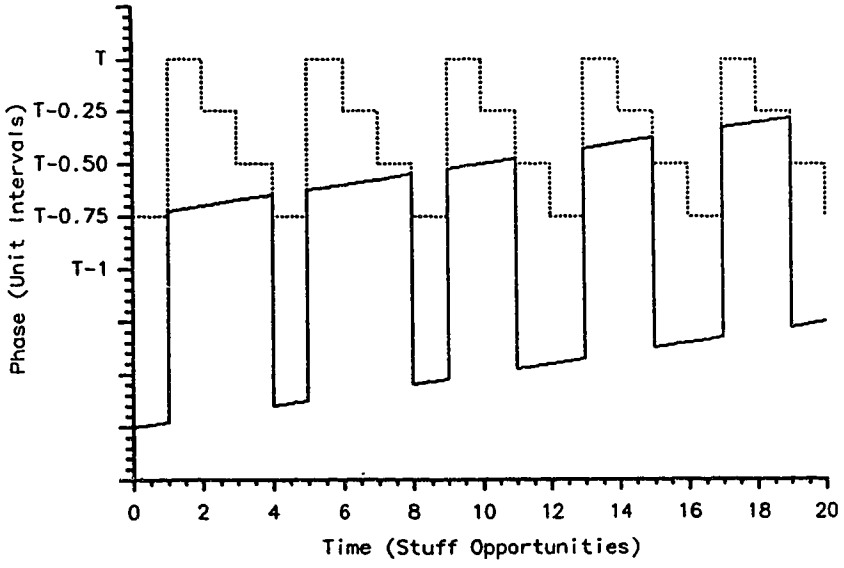

Fig. 1-10 Waiting time jitter waveform with single sided stuff threshold modulation.

III. Pointer Processing

Synchronization in SONET is accomplished using payload pointers and envelope mechanisms [5]. Synchronization is required between line layers in the SONET network when system clocks in each layer are plesiochronous. At the interface between line layers, the SONET SPE signals are removed from the originating layer and byte stuffed into signals in the terminating layer. Both positive and negative byte stuffing are used in the synchronization process, and pointers are used in the transport overhead to point to the beginning of the SPE frame. When a positive byte is stuffed, it is referred to as a positive pointer adjustment because the pointer must be incremented to point to the new beginning of the SPE frame. Similarly, when a negative byte is stuffed it is referred to as a negative pointer adjustment. Under normal conditions, system clocks from different line layers are synchronous. This condition is referred to as non-degraded synchronization mode and is associated with infrequent random pointer adjustments. The only cause of pointer adjustments in this mode is random, short term phase noise in the system clocks. Degraded synchronization mode refers to the condition where system clocks in the line layers are plesiochronous. The tolerance of system clocks in this mode can be as large as ±20 ppm [1]. This mode is associated with regular pointer adjustments. The network that is studied in this thesis consists of two line layers as in Fig. 1-5. Waiting time jitter is produced by the mapping of DS-1 signals into the SONET VT1.5 SPE at the muldem, and by positive and negative VT1.5 pointer adjustments that may occur between the two line layers. Jitter introduced by the regenerators is negligible compared to waiting time jitter [6]. Further more, pointer adjustments that occur at the STS-1 level are not considered because they will not contribute large amounts of jitter to the DS-1 signal [16]. This is because the SONET standard allows for a maximum peak to peak jitter amplitude of 1.5 STS-1 SPE UI on the

STS-1 SPE signal which corresponds to only 0.05 DS-1 UI. This amount of jitter is negligible compared to the jitter caused by VT1.5 pointer adjustments.

The pointer mechanism in SONET is used for framing of the SPE. The payload pointer consists of two bytes, or 16 bits, within the line overhead. The format of the VT1.5 payload pointer consisting of the two bytes V1 and V2 is shown in Fig. 1-11. The two bytes V1 and V2 correspond to the first and second bytes respectively in the first column of the VT1.5 signal format, shown in Fig. 1-7. The first four bits of the pointer are called the new data flag (NDF) and are used to indicate an arbitrarily new value for the pointer such as would occur when a new VT1.5 SPE is switched into the VT1.5. The fifth and sixth bits designate the size of the VT and are both set to one for the VT1.5. The remaining ten bits contain the value of the pointer with the most significant bit placed in the seventh bit location of the pointer and the least significant bit placed in the sixteenth bit location. Bits seven, nine, eleven, thirteen, and fifteen are designated increment bits and are used during the positive pointer adjustment operation. Bits eight, ten, twelve, fourteen, and sixteen are designated decrement bits and are used during the negative pointer adjustment operation.

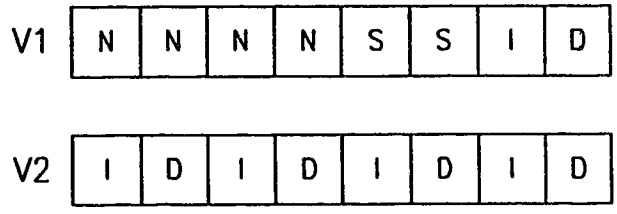

Fig. 1-11 VT payload pointer coding.
N - new data flag, S - VT size,
I - increment bit, D - decrement bit.

The value of the pointer indicates the location of the first byte of the VT1.5 SPE within the VT1.5 envelope capacity. The pointer values for each of the possible offsets are shown in Fig. 1-12. As an example, if the pointer value was 27, the first byte of the VT1.5 SPE would be placed in column 3 and row 3 of the VT1.5.

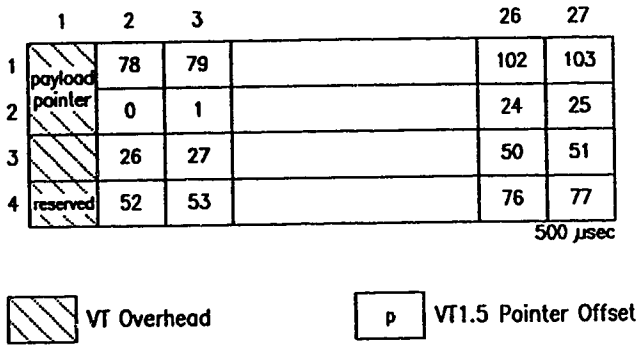

Fig. 1-12 VT1.5 pointer offset numbering.

Positive pointer adjustments occur when the frame rate of the VT1.5 SPE is slightly lower than the frame rate of the VT1.5. Three consecutive frames of the VT1.5 during a positive pointer adjustment are shown in Fig. 1-13. The first frame represents the VT1.5 before the pointer adjustment occurs where the pointer has some value p. The second frame represents the VT1.5 during the pointer adjustment operation. During this frame the I bits in the pointer are inverted to signal a positive pointer adjustment and the positive stuff location of the VT1.5 signal format contains a dummy byte. The last frame shown represents the VT1.5 after the pointer adjustment where the pointer is incremented so that it points to the new location of the VT1.5 SPE at p+1. Once a pointer adjustment has occurred, the pointer value must remain unchanged for the next three frames, or in other words, a pointer adjustment cannot occur for the next three frames.

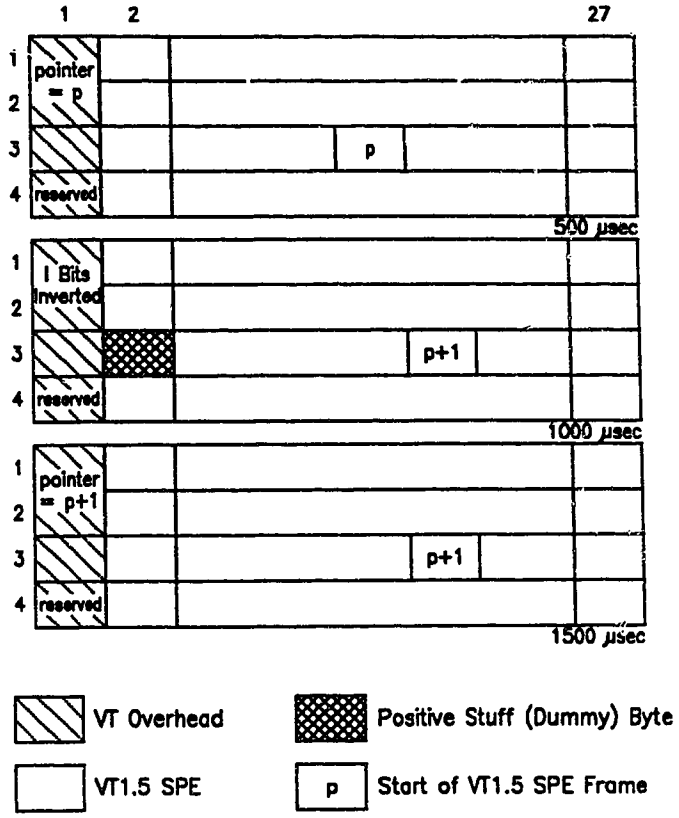

Fig. 1-13 Positive VT1.5 pointer adjustment operation.

The operation of a negative pointer adjustment in a VT1.5 is presented in Fig. 1-14 where three consecutive frames of the VT1.5 are shown. Negative pointer adjustments occur when the frame rate of the VT1.5 SPE is slightly higher than the frame rate of the VT1.5. As before the first frame represents the VT1.5 before the pointer adjustment occurs where the pointer has some value p. The second frame represents the VT1.5 during the pointer adjustment operation. During this frame the D bits in the pointer are inverted to signal a negative pointer adjustment and the negative stuff location of the VT1.5 signal format contains a data byte from the VT1.5 SPE. The last frame shown represents the VT1.5 after the pointer adjustment. The pointer is decremented so that it points to the new

location of the VT1.5 SPE at p-1. As before once a pointer adjustment has occurred, the pointer value must remain unchanged for the next three frames.

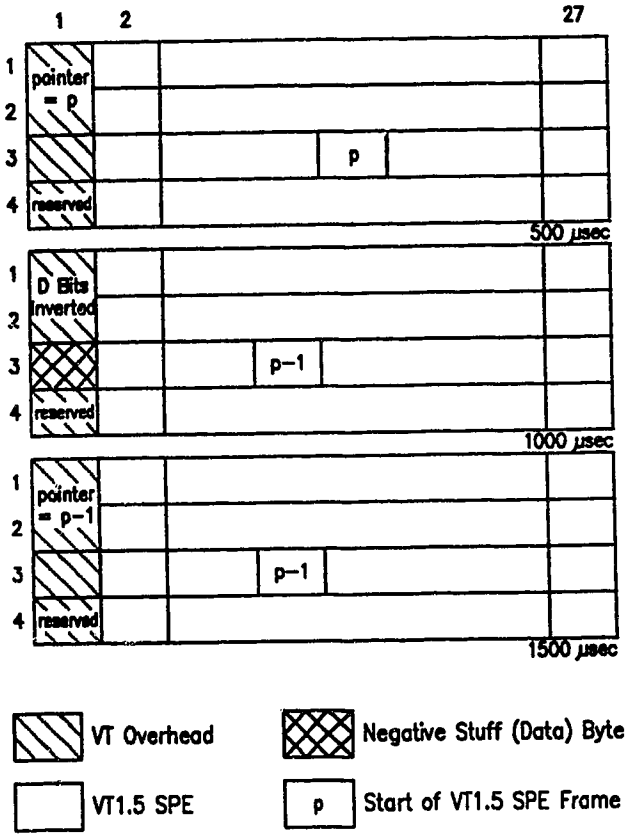

Fig. 1-14 Negative VT1.5 pointer adjustment operation.

Pointer adjustments used in SONET synchronizers introduces high peak to peak jitter levels for two reasons [17]. The first reason is because eight bits are stuffed at one time which corresponds to an eight UI phase step; the second reason is because the stuff ratio is close to zero. For our purposes jitter is defined as phase variations occurring in the pulse stream with frequency components higher than 10 Hz. Phase variations occurring with frequency components less than 10 Hz are defined as wander. A specification has been proposed by the

ECSA T1X1.6 working group which states that the payload output jitter from a network element in the absence of applied payload input jitter should not exceed 1.5 UI peak to peak as measured by a single pole 10 Hz high pass filter [18-20]. For the work done in this thesis, this jitter specification has been tightened to 1.0 UI peak to peak and 0.3 UI rms as measured with a 10 Hz high pass filter in order to meet the CCITT recommendations for maximum jitter generation. The purpose of this thesis is to analyze proposed techniques which reduce the jitter associated with pointer adjustments that occur at the VT1.5 level. These proposed techniques are described below.

iv. Previous Work

Several methods for the reduction of jitter caused by VT1.5 pointer adjustments have been proposed, which can be divided into two broad categories. The first category consists of pointer spreading techniques which are implemented during the desynchronization process, and the second category consists of STM techniques which are implemented at the VT1.5 SPE to VT1.5 synchronizer.

Pointer spreading methods are based on storing the phase step caused by a pointer adjustment in an elastic store and then leaking this stored phase out in small fractional phase steps at some rate. The pointer spreading techniques differ in the method and rate at which the fractional phase steps are leaked. A block diagram of a desynchronizer that uses pointer spreading is shown in Fig. 1-15. The difference between this desynchronizer and a conventional one is the additional pointer spreading elastic store and logic. When a pointer adjustment occurs, the resulting phase step is absorbed in the pointer spreading elastic store. The pointer spreading logic is responsible for leaking out this phase in small fractional phase steps. Three proposals of pointer spreading have been

studied in recent ECSA T1 contributions. These are (a) a fixed rate pointer spreader [21-23], (b) a feed forward pointer spreader [21,24], and (c) a variable rate pointer spreader [21,25,26].

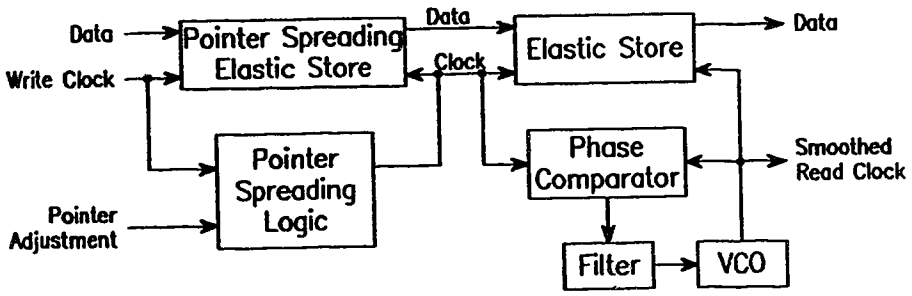

Fig. 1-15 Desynchronizer block diagram with added pointer spreading circuit.

A fixed rate pointer spreader leaks out constant magnitude, fractional phase steps at a fixed rate. The optimum choice of rate must be decided based upon the amount of jitter produced and the amount of time taken to completely leak out one pointer adjustment. This time is important because pointer adjustments must be leaked out at least as fast as they are occurring so that the elastic store does not spill. Fixed rate pointer spreading has been described in [21-23] and preliminary jitter levels have been estimated during a single pointer adjustment.

In a feed forward pointer spreader, all upstream equipment containing elastic stores continuously sends information to downstream equipment depending on the amount that its elastic store is filled. Prior to a pointer adjustment, downstream equipment leaks out fractional phase steps at the same rate that upstream elastic stores are filling. The design described in [21,24] requires a significant change in the SONET standard and would likely cause

international concern. For this design, a significant increase in the complexity of pointer processors and desynchronizers throughout the network would be necessary. No studies have been done on the networking aspects of this design.

A variable rate pointer spreader uses a digital phase lock loop in the pointer spreading logic to filter out pointer adjustments using a time constant well below 10 Hz. The phase lock loop associated with the pointer spreading elastic store is clocked at the frame rate which is much lower than the bit rate, and therefore allows a very low pass digital filter to be easily designed. The designs described in [21,25,26] can handle pointer adjustments associated with a ±20 ppm synchronization tolerance. No changes to the SONET standard are necessary. However, there is a marginal amount of additional hardware complexity required at the interface.

Stuff threshold modulation has been used in the mapping of DS-1 signals into VT1.5 SPE signals to successfully reduce waiting time jitter. It seems reasonable to try a similar method of jitter reduction in the VT1.5 SPE to VT1.5 mapping. This would involve a moderate increase in complexity of the synchronizers.

v. Outline

Chapter II describes the simulation technique [27,28] which is used in the remainder of this thesis to analyze the jitter associated with pointer adjustments in SONET. Chapter III describes the jitter that results when no pointer spreading or STM techniques are used to reduce jitter. These results are used as a benchmark for evaluating the effectiveness of jitter reduction schemes. Fixed rate pointer spreading and variable rate pointer spreading are discussed in Chapters IV and V, respectively. Stuff threshold modulation and feed forward pointer spreading are then discussed in Chapters VI and VII respectively. All of the jitter reduction

schemes are analyzed theoretically by calculating the Fourier transform of the waiting time jitter waveforms. Simulation results are also presented for each method. Chapter VII provides a summary of the work done in this thesis as well as conclusions and areas of possible future work.

II. SIMULATION TECHNIQUE

This Chapter describes the simulation technique used to analyze jitter associated with SONET pointer adjustments. This technique has been used successfully in the past to analyze waiting time jitter associated with other multiplexing formats [27]. Three different situations that occur in the SONET network are studied using this simulation technique. Source listings for all simulations used in this thesis are given in [28]. The first and second situations occur during non-degraded synchronization mode, in which case the VT1.5 SPE is synchronously mapped into the VT1.5. In the first of these situations, it is assumed that there are no pointer adjustments. The only source of jitter is the mapping of the DS-1 into the VT1.5 SPE. To analyze this situation, the DS-1 frequency is varied through its operating range of ±130 ppm [6], which corresponds to a DS-1 offset frequency of ±200 Hz. The second of these non-degraded situations analyses the effect of a random pointer adjustment. In this case there is a single isolated pointer adjustment which occurs at the beginning of the simulation. Again, the DS-1 offset frequency is varied through its operating range of ±200 Hz. The last set of circumstances occurs during degraded synchronization mode. In this mode, the VT1.5 offset frequency is allowed to vary through its maximum allowable range of ±20 ppm [1], which corresponds to ±35 Hz.

I. Basic Principle

Waiting time jitter characteristics for any multiplex format can be analyzed by examining the phase difference between the read and write clocks as a function of time in the synchronizer elastic store [8,9]. The synchronizer is the source of waiting time jitter and the desynchronizer behaves as a linear low pass

filter on the waiting time jitter spectrum. This principle is utilized in the simulation technique and is summarized in Fig. 2-1. The first step in the technique is the calculation of phase differences at discrete points in time between the read and write clocks of the synchronizer elastic store. These phase differences are referred to as phase samples. The second and third steps involve the application of appropriate time domain signal processing techniques to model the desynchronizer PLL and the jitter measuring instrument, respectively. Finally, statistical analyses are performed on the processed phase samples, to produce estimates of rms and peak to peak waiting time jitter characteristics.

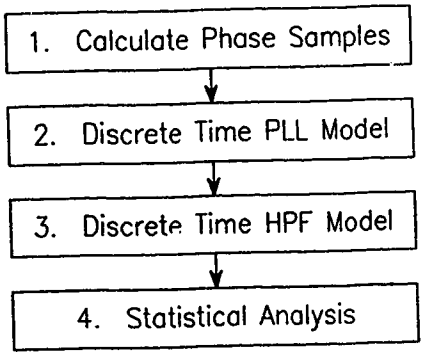

Fig. 2-1 Illustration of signal processing for time domain jitter analysis.

II. Phase Sample Calculation

Fig. 2-2 shows the methodology that was used in calculating the phase samples. For the case where DS-1 signals are transmitted in a VT1.5 signal there are two pulse stuffing synchronization steps. The first synchronization is the bit stuffing of the DS-1 into a VT1.5 SPE. It is assumed that the DS-1 frequency is at the nominal rate of 1.544 Mb/s plus some offset frequency in the range of ±200 Hz, and the VT1.5 SPE is at the nominal rate of 1.664 Mb/s. The second

synchronization is the byte stuffing of the VT1.5 SPE into a VT1.5. The VT1.5 is assumed to have an offset frequency in the range of ±35 Hz when in degraded synchronization mode, and 0 Hz when in non-degraded synchronization mode. The phases in the elastic stores of both of these synchronizers are monitored to obtain the stuffing pattern by using the generalized recursive relation described in [27]. The final step in the methodology is the removal of the DS-1 from the VT1.5 where the phase in the desynchronizer elastic store is calculated in VT1.5 read clock unit intervals using the knowledge of the stuffing pattern obtained from the two synchronization processes. For simulations involving pointer spreading circuits, the functionality of the pointer spreading logic and elastic store, see Fig. 1-15, were emulated and used to influence the phase samples. In order to calculate waiting time jitter characteristics correctly, it is necessary that the phase samples be calculated at times that are synchronous to the stuff opportunity frames [27]. For the DS-1 to VT1.5 mapping this means that the phase samples must be synchronized to the bit stuffing opportunities in the VT1.5 SPE as well as the byte stuffing opportunities in the VT1.5. In order to maintain this synchronization it is necessary and sufficient to calculate phase samples on a VT1.5 byte by byte basis. The time interval between samples is therefore approximately 4.63 μsec, which is the time required to transmit one VT1.5 byte.

For simulations involving pointer spreading techniques the phase samples were altered to simulate the pointer spreading circuit. The phase stored in the pointer spreading elastic store was subtracted from the input phase samples to the pointer spreading circuit. The functionality of the pointer spreading logic which controlled the amount of phase stored in the pointer spreading elastic store was modelled. Immediately after a pointer adjustment the phase in the pointer spreading elastic store was increased by 8.0 VT1.5 SPE UI with a polarity chosen based on whether a positive or negative pointer adjustment occurred. The phase

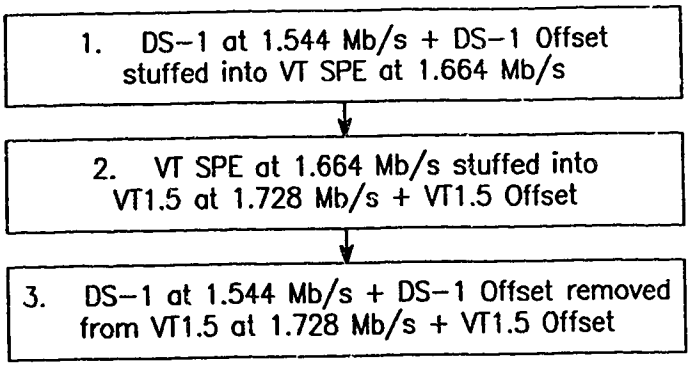

Fig. 2-2 Methodology for calculation of phase samples.

was then leaked out at times synchronous to the VT1.5 subframe rate of one per 125 μsec, and at a rate dependent on the type of pointer spreading logic modelled. The final phase samples represent the input phase at the desynchronizing PLL.

iii. Digital Filter Implementation

Once the phase samples have been calculated, they are filtered using time domain representations of digital filters to model the desynchronizer PLL and the jitter measuring equipment. Many different desynchronizer PLL models have been studied in the past, including some second order models with a cutoff frequency as low as 10 Hz [16]. The desynchronizer used in the analysis is assumed to have a second order Butterworth characteristic with a 25 Hz cutoff frequency. This PLL model has the transfer function

$$H(s) = \frac{\omega_c^2}{s^2 + \sqrt{2}s\omega_c + \omega_c^2}, \qquad (2\text{-}1)$$

where ω_c is the 3 dB frequency in rad/s. A digital filter can be found by using the bilinear transformation method where the poles and zeroes in the s-plane are

mapped into the z-plane. The bilinear transformation was chosen because it has the property of preserving the magnitude response of the piecewise constant analog filter [29]. By applying the bilinear transformation to Eqn. 2-1 the digital filter transfer function

$$H(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2}}{1 + b_1 z^{-1} + b_2 z^{-2}}, \qquad (2\text{-}2)$$

is obtained (see Appendix A), where

$$a_0 = \frac{\Omega_c^2}{\Omega_c^2 + \sqrt{2}\Omega_c + 1}, \qquad a_1 = 2a_0, \qquad a_2 = a_0,$$

$$b_1 = \frac{2\Omega_c^2 + 1}{\Omega_c^2 + \sqrt{2}\Omega_c + 1}, \qquad b_2 = \frac{\Omega_c^2 - \sqrt{2}\Omega_c + 1}{\Omega_c^2 + \sqrt{2}\Omega_c + 1},$$

and

$$\Omega_c = \tan\left(\frac{\omega_c T_s}{2}\right).$$

T_s is the time interval between samples which in our case is 4.63 μsec. Fig. 2-3 is a plot of the frequency response of the resulting digital system when the 3 dB frequency of the analog system is 25 Hz. Because the sampling frequency, which is 216 kHz, is so much higher than the 3 dB frequency, the frequency response of the digital system closely resembles that of the analog system.

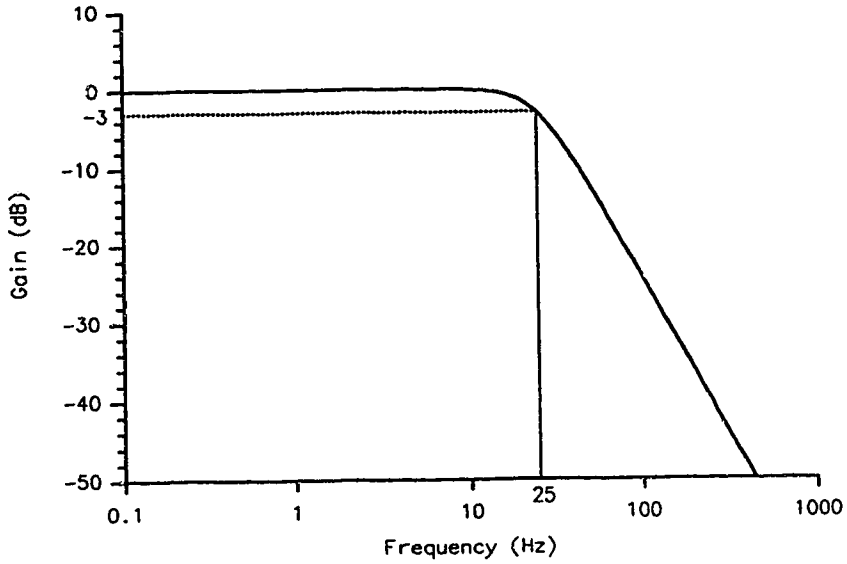

Fig. 2-3 Phase-lock loop frequency response.

The jitter measuring equipment is assumed to have a single pole at 10 Hz and a high pass characteristic. This response was chosen to agree with the T1X1.6 working group recommendation [18,24]. Therefore, the jitter measuring equipment is desired to have the frequency response

$$H(s) = \frac{s}{s + \omega_c}, \tag{2-3}$$

where ω_c is again the 3 dB frequency. Again, the bilinear transformation (see Appendix A) is applied to this filter to obtain

$$H(z) = \frac{a_0 + a_1 z^{-1}}{1 + b_1 z^{-1}}, \tag{2-4}$$

where

$$a_0 = \frac{1}{\Omega_c + 1}, \qquad a_1 = -a_0,$$

$$b_1 = \frac{\Omega_c - 1}{\Omega_c + 1},$$

and

$$\Omega_c = \tan\left(\frac{\omega_c T_s}{2}\right).$$

Fig. 2-4 is a plot of the frequency response of the resulting digital system for the jitter measuring equipment when the 3 dB frequency of the analog system is 10 Hz. Again, the analog and digital systems have very similar responses.

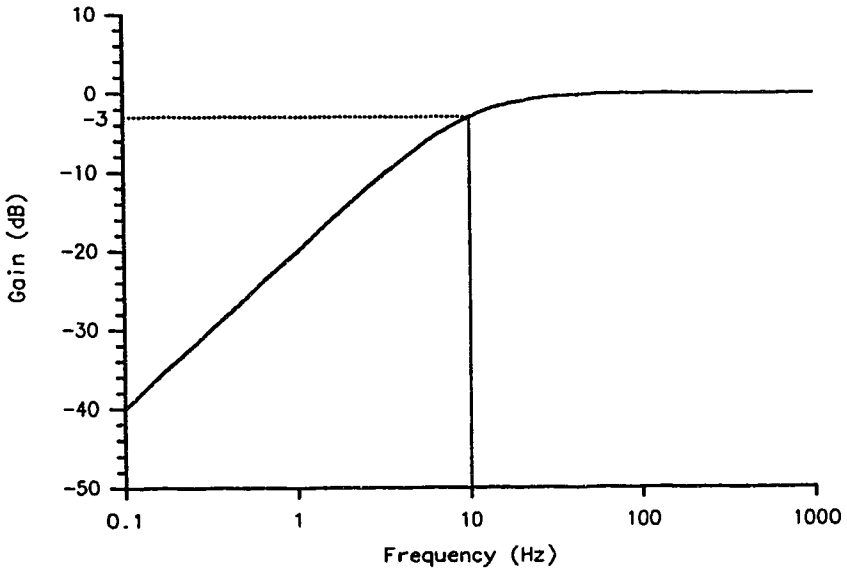

Fig. 2-4 Jitter measuring equipment frequency response.

The PLL and jitter measuring equipment digital filters are implemented using the Infinite Impulse Response (IIR) canonic realization [29] as shown in Fig. 2-5. The input phase samples are denoted as x(n) and the output filtered samples

are denoted as y(n). For the high pass filter, the coefficients a_2 and b_2 are set to zero.

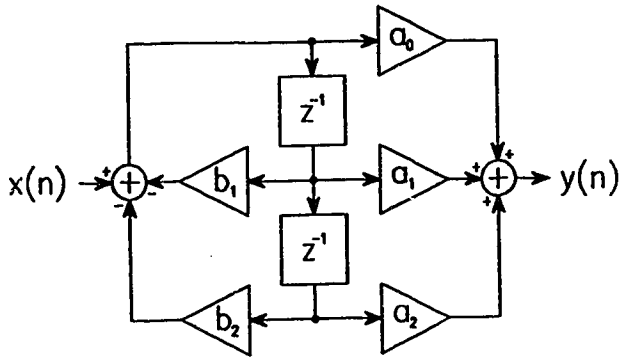

Fig. 2-5 Canonic realization of a second order Infinite Impulse Response digital filter.

Iv. Analysis

After the phase samples have been filtered they are used to calculate the rms and the peak to peak jitter estimates. It is desired to obtain the steady state rms and peak to peak jitter estimates, and therefore the simulation must contain a transient duration where the phase samples are calculated and filtered but are not used to obtain rms and peak to peak estimates. This is necessary to allow the transient responses of the digital filters to decay to a negligible level. After an appropriate transient duration, a sampling duration is invoked where the filtered samples are used to obtain jitter estimates. The rms jitter is calculated as the standard deviation of the filtered phase samples and the peak to peak jitter is calculated by finding the difference between the maximum and minimum filtered phase samples during the finite sampling duration. The jitter characteristics are then scaled by 1.544/1.728 to convert from VT1.5 read clock UI to DS-1 UI.

When examining non-degraded synchronization mode without pointer adjustments, the simulation is performed with the VT1.5 offset frequency set to 0 Hz and the DS-1 offset frequency varied from -200 Hz to 200 Hz in steps of 1 Hz. A single pointer adjustment is simulated in the same way except a single positive or negative pointer adjustment is forced to occur at the beginning of the sampling duration. Degraded synchronization mode is examined by setting the DS-1 offset frequency to 0 Hz and by varying the VT1.5 offset frequency from -35 Hz to 35 Hz in steps of 0.25 Hz.

v. Summary

The simulation technique described in this Chapter is used in this thesis to analyze jitter in SONET networks which include pointer adjustments. This technique, which has been used in the past to examine other multiplexing formats [27], is based on first calculating the phase difference between the read and write clocks of the synchronizer elastic store at discrete points in time. Discrete time representations of the PLL and of the measuring equipment are then applied to the discrete phase samples, and finally the filtered samples are used to derive the rms and peak to peak jitter. Complete source listings for all of the simulations used in this thesis are given in [28].

III. ANALYSIS WITHOUT JITTER REDUCTION TECHNIQUES

In this Chapter waiting time jitter is estimated when no methods are used to reduce the jitter caused by pointer adjustments. Results obtained in this Chapter are used as a benchmark for evaluating the effectiveness of pointer spreading and stuff threshold modulation techniques analyzed in later Chapters. The system without jitter reduction techniques is first described and then theoretically analyzed while in non-degraded and degraded synchronization mode. Simulation results are then discussed along with implementation considerations of the system.

I. Description

The system analyzed in this Chapter has a simple VT1.5 SPE to VT1.5 synchronizer, referred to as a plus/zero/minus synchronizer. This synchronizer has two fixed stuff thresholds, one which controls positive stuffing and one which controls negative stuffing. The positive and negative stuff thresholds are separated by more than eight VT1.5 SPE UI; the positive threshold is above the negative threshold on the waiting time jitter waveform. This type of synchronizer invokes a positive pointer adjustment if the phase is higher than the positive threshold and a negative pointer adjustment if the phase is lower than the negative threshold. If the phase is between the two thresholds, no pointer adjustment is invoked. In this system the DS-1 to VT1.5 SPE synchronizer uses single sided stuff threshold modulation for jitter reduction as described in section I.ii. At the desynchronizer, where the DS-1 is removed from the VT1.5, there is a 25 Hz second order PLL, and a 10 Hz high pass filter is used in the jitter measuring equipment. A block diagram of the system is given in Fig. 3-1. This system will perform very differently when in degraded synchronization mode as

compared to non-degraded synchronization mode. During non-degraded synchronization mode when there are no pointer adjustments, the jitter is expected to be very low. However when a pointer adjustment occurs, either randomly during non-degraded synchronization mode or frequently during degraded synchronization mode, the rms and peak to peak jitter levels are expected to be very high.

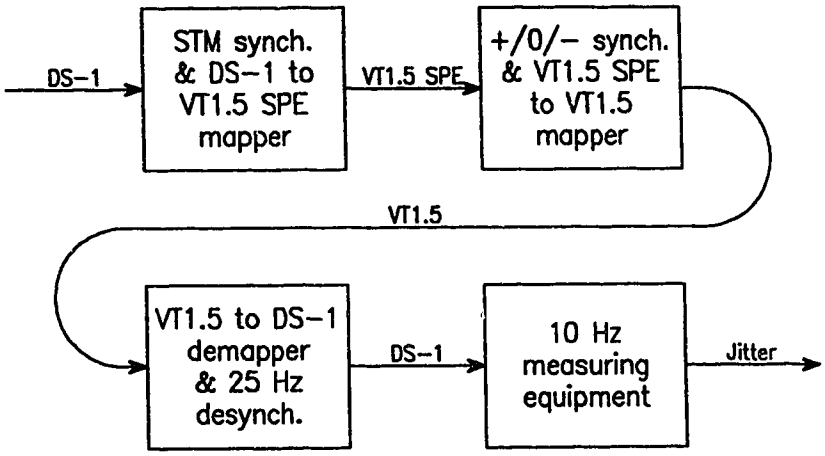

Fig. 3-1 System block diagram without jitter reduction techniques.

ii. Theoretical Analysis

Non-Degraded Synchronization Mode

During non-degraded synchronization mode, pointer adjustments will occur very infrequently [30-32] and each one can be considered as a single isolated pointer adjustment. The peak to peak jitter that results when a single isolated pointer adjustment occurs can be found by calculating the step response of the desynchronizer and jitter measuring equipment. A pointer adjustment causes a phase step to occur in the desynchronizer elastic store. The PLL and the jitter measuring equipment then respond to this phase step. The additional

jitter caused by the mapping of the DS-1 into the VT1.5 SPE is ignored for this analysis. From Eqns. 2-1 and 2-3, the transfer function of the desynchronizer and the jitter measuring equipment can be written as

$$H_d(s) = \frac{\omega_{PLL}^2 s}{\left(s^2 + \sqrt{2}s\omega_{PLL} + \omega_{PLL}^2\right)\left(s + \omega_{HPF}\right)}, \tag{3-1}$$

where ω_{PLL} is the 3 dB frequency of the PLL and ω_{HPF} is the 3 dB frequency of the jitter measuring equipment in rad/s. The input to the system is a phase step which has the Laplace transform

$$\Phi_s(s) = \frac{K}{s}, \tag{3-2}$$

where K is the magnitude of the phase step. The step response of the system to a single isolated pointer adjustment is therefore

$$\Phi_d(s) = \frac{K\omega_{PLL}^2}{\left(s^2 + \sqrt{2}s\omega_{PLL} + \omega_{PLL}^2\right)\left(s + \omega_{HPF}\right)}. \tag{3-3}$$

The inverse Laplace transform of $\Phi_d(s)$ is

$$\phi_d(t) = Ae^{-\sigma_1 t}\cos(\omega_1 t) + Be^{-\sigma_1 t}\sin(\omega_1 t) + Ce^{-\sigma_2 t}, \tag{3-4}$$

where

$$A = \frac{-K\omega_{PLL}^2}{\omega_{PLL}^2 - \sqrt{2}\omega_{PLL}\omega_{HPF} + \omega_{HPF}^2}, \qquad B = \frac{-K\omega_{PLL}^2 + \sqrt{2}K\omega_{PLL}\omega_{HPF}}{\omega_{PLL}^2 - \sqrt{2}\omega_{PLL}\omega_{HPF} + \omega_{HPF}^2},$$

$$C = \frac{K\omega_{PLL}^2}{\omega_{PLL}^2 - \sqrt{2}\omega_{PLL}\omega_{HPF} + \omega_{HPF}^2}, \qquad \omega_1 = \frac{\omega_{PLL}}{\sqrt{2}},$$

$$\sigma_1 = \frac{\omega_{PLL}}{\sqrt{2}}, \text{ and} \qquad \sigma_2 = \omega_{HPF}.$$

The peak to peak jitter that will be measured when a single pointer adjustment occurs is equal to the difference between the maximum value of $\phi_d(t)$ and the minimum value of $\phi_d(t)$. Numerical methods were used to find the maximum

value of $\phi_d(t)$ which occurs at 0.01645 seconds when the PLL's 3 dB frequency is 25 Hz and the jitter measuring equipment's 3 dB frequency is 10 Hz. For these values of cutoff frequencies the maximum value of $\phi_d(t)$ is 0.5535K and the minimum value is 0. Therefore the peak to peak jitter is 0.5535K. The response of the system normalized to K is shown in Fig. 3-2 which shows the maximum value that $\phi_d(t)$ reaches. For the system without pointer spreading or other jitter reduction techniques being employed, the phase step caused by a pointer adjustment will be 8.0 VT1.5 SPE UI. Therefore, using the results obtained above, the peak to peak jitter is expected to be 4.4280 VT1.5 SPE UI which corresponds to 4.1087 DS-1 UI.

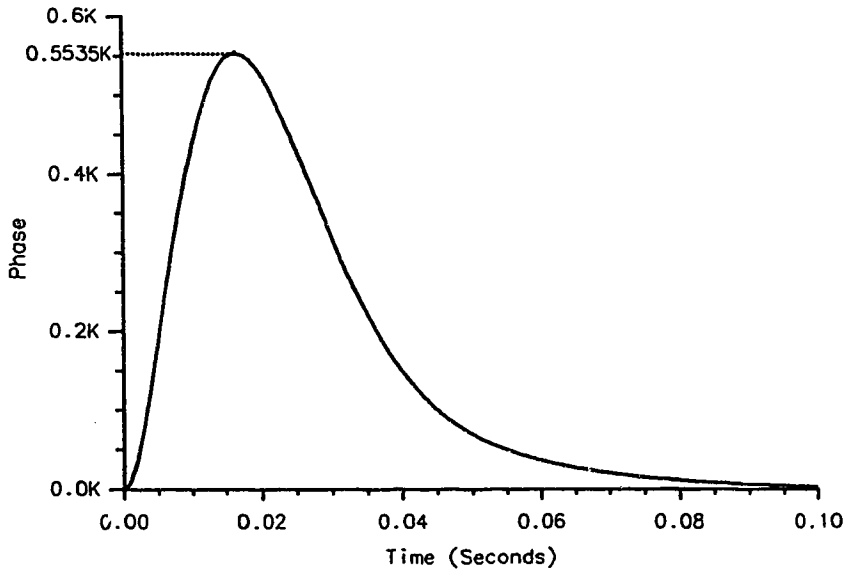

Fig. 3-2 System response to a single isolated phase step.

Degraded Synchronization Mode

When the system is in degraded synchronization mode, the Fourier transform can be used to determine the spectral components of the waiting time

jitter. The Fourier [illegible]n of the waiting time jitter waveform when there is no pointer spreading can be calculated using Chow's approach [9]. The jitter which is introduced by the DS-1 to VT1.5 SPE mapping is ignored for this analysis. Only the VT1.5 SPE to VT1.5 synchronization process is examined. Assuming a jitter free write clock, we get the time domain waiting time jitter waveform as shown in Fig. 3-3 for a positive VT1.5 offset frequency. The phase difference between the read and write clocks is given by the solid line, and the positive threshold is given by the dotted line. The negative threshold is not shown because for the assumed positive read minus write frequency difference it will not influence the process of pointer adjustments. The amplitude of the phase jump during a positive pointer adjustment is eight VT1.5 SPE UI and time is given in stuff opportunities of the VT1.5 signal format which are 500 μsec apart.

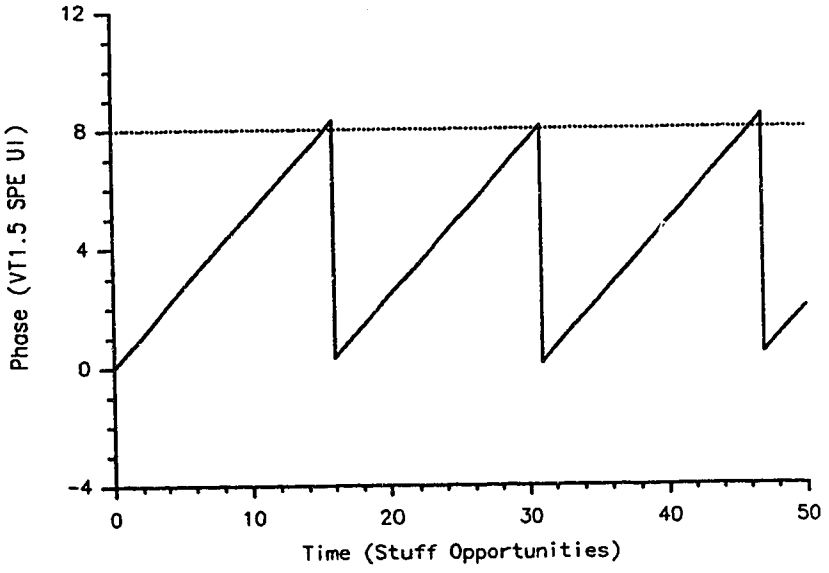

Fig. 3-3 Waiting time jitter waveform without jitter reduction techniques.

In order to calculate the Fourier transform of the waiting time jitter the stuff ratio is first defined as

$$\rho = \frac{(f_r - f_w)}{8f_m}, \tag{3-5}$$

where f_r is the frequency of the read clock, f_w is the frequency of the write clock, and f_m is the frequency of stuff opportunities. For VT1.5 SPE mapping into VT1.5 as shown in Fig. 1-6,

$$\rho = \frac{(1.728E6 + \nu)(26/27) - 1.664E6}{8(2000)} = \frac{13\nu}{216000} \tag{3-6}$$

where ν is the VT1.5 offset frequency in Hz. From Eqn. 3-6, it can be seen that the stuff ratio is nominally zero, and even with a large VT1.5 offset frequency such as 35 Hz the stuff ratio is small. Using the definition for the stuff ratio we can write the time domain equation for the waiting time jitter waveform as

$$\phi_s(t) = 8\left(\rho t - [\rho[t]]\right), \tag{3-7}$$

where $[x]$ denotes the greatest integer equal to or less than x, and time is normalized to the stuff opportunity period $1/f_m$ [8,9]. In order to calculate the Fourier transform of $\phi_s(t)$ we first define

$$\mu(x) = x - [x], \tag{3-8}$$

and then rewrite Eqn. 3-7 as

$$\phi_s(t) = 8\phi_{s1}(t) + 8\phi_{s2}(t), \tag{3-9}$$

where

$$\phi_{s1}(t) = \rho\mu(t), \tag{3-10}$$

$$\phi_{s2}(t) = \mu\left(\rho[t]\right). \tag{3-11}$$

Eqn. 3-10 represents a simple sawtooth waveform with period 1.0 and amplitude ρ, the Fourier transform of which is (see Appendix B)

$$\Phi_{s1}(f) = \frac{\rho}{2}\delta(f) + \sum_{k=1}^{\infty} \frac{j\rho}{2\pi k}\left[\delta(f-k) - \delta(f+k)\right]. \qquad (3\text{-}12)$$

The Fourier transform of $\phi_{s2}(t)$ may be calculated by first presenting it as (see Appendix B)

$$\phi_{s2}(t) = \left[U(t) - U(t-1)\right] * \left[\mu(\rho t) \cdot \sum_{m=-\infty}^{\infty} \delta(t-m)\right], \qquad (3\text{-}13)$$

where $U(t)$ is a unit step. The Fourier transform of Eqn. 3-13 is (see Appendix B)

$$\Phi_{s2}(f) = \frac{1}{2}\delta(f) + e^{-j\pi f}\,\frac{\sin(\pi f)}{\pi f} \sum_{k=1}^{\infty} \sum_{m=-\infty}^{\infty} \frac{j}{2\pi k}\left[\delta(f-\rho k-m) - \delta(f+\rho k-m)\right]. \qquad (3\text{-}14)$$

The complete Fourier transform of the waiting time jitter waveform is therefore

$$\Phi_s(f) = 8\Phi_{s1}(f) + 8\Phi_{s2}(f), \qquad (3\text{-}15)$$

where f is normalized to the stuff opportunity rate f_m. This result agrees with the one derived by Chow who calculated the Fourier transform for DS-1 to DS-2 multiplexing.

The unfiltered power spectral density of the waiting time jitter can be found by squaring the magnitudes of the Fourier transform terms. The power spectral density for unfiltered waiting time jitter with a VT1.5 offset of 35 Hz, which corresponds to a stuff ratio of 2.1065E-3, is shown in Fig. 3-4. The results are given in dB where 0 dB corresponds to 1 (DS-1 UI)^2/Hz. These results were found by calculating the first 125 terms of $\Phi_s(f)$. From Fig. 3-4 it is apparent that the jitter spectrum contains much of its power at low frequencies which will not be filtered out by the 25 Hz PLL. The magnitude of the power spectral density at these low frequencies is also very high.

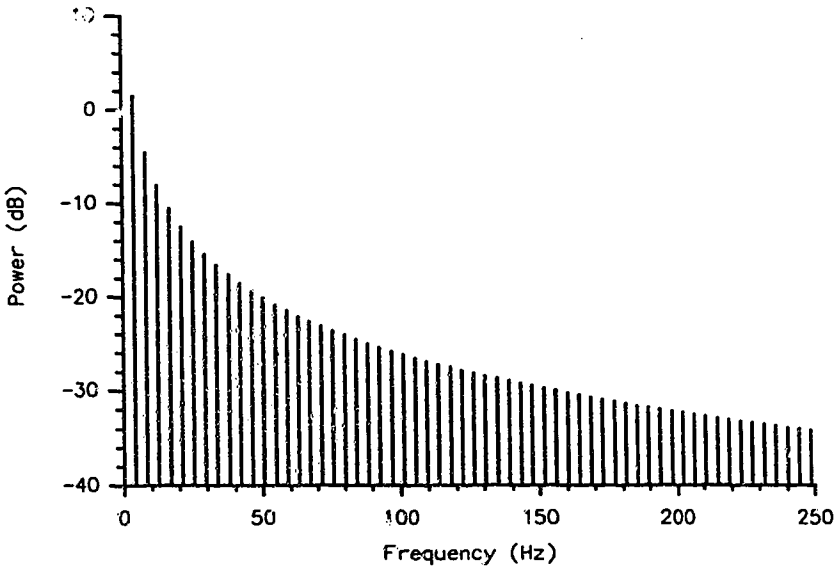

Fig. 3-4 Unfiltered power spectral density without jitter reduction techniques and a 35 Hz VT1.5 offset frequency.

Fig. 3-5 shows the rms jitter versus VT1.5 offset frequency for the VT SPE to VT1.5 mapping. This was calculated by integrating the filtered power spectral density. The response of the 25 Hz desynchronizer PLL and the 10 Hz jitter measuring equipment was implemented using Eqn. 3-1. Results were found by calculating the first 125 terms of $\Phi_{s2}(f)$, and by neglecting dc terms and $\Phi_{s1}(f)$. The jitter from $\Phi_{s1}(f)$ is negligible because its power is contained at frequencies much higher than the cutoff frequency of the PLL. As shown in Fig. 3-5 the rms jitter when no jitter reduction techniques are used is greater than 1.0 DS-1 UI for large VT1.5 offset frequencies.

iii. Simulation Results

Simulations were done for both degraded and non-degraded synchronization modes of operation. Transient durations of 1.0 second were used in all of the simulations to allow the PLL and high pass filters to reach steady

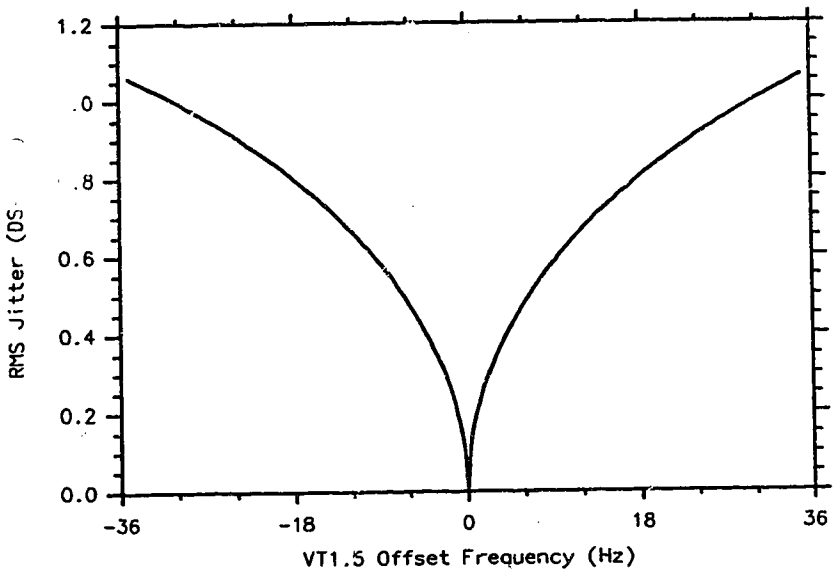

Fig. 3-5 Theoretical rms jitter versus VT1.5 offset frequency.

state conditions. Sampling durations of 1.0 second were used for the simulations of non-degraded synchronization mode. For the simulations of degraded synchronization mode, a 40.0 second sampling duration was used in order to assure that a pointer adjustment always occurred during the simulation. For a 0.25 Hz VT1.5 offset frequency, the time between successive pointer adjustments is approximately 33.2 seconds.

Non-Degraded Synchronization Mode

Fig. 3-6 shows the waiting time jitter versus DS-1 offset frequency when there are no pointer adjustments. The pointer value for this simulation was set to 0. All of the jitter is produced by the mapping of the DS-1 into the VT1.5 SPE. As expected, the jitter caused by the DS-1 to VT1.5 SPE mapping is low. The peak to peak jitter is always below 0.19 DS-1 UI and the rms jitter is always below 0.07 DS-1 UI. The asymmetry of the jitter versus DS-1 offset frequency is caused by the

stuff threshold modulation which is used in the DS-1 to VT1.5 SPE mapping. These results are well below the CCITT recommendations for maximum jitter generation of 1.0 DS-1 UI peak to peak and 0.3 DS-1 UI rms.

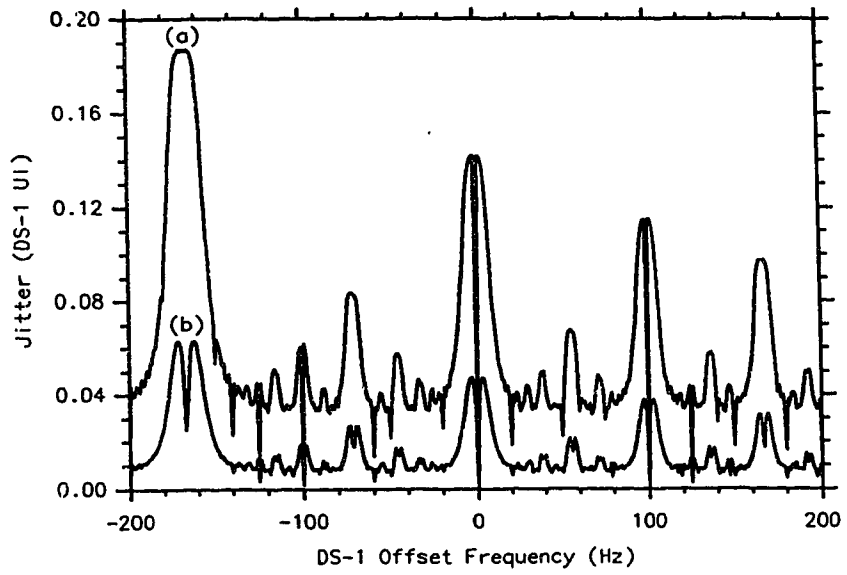

Fig. 3-6 Jitter without pointer adjustments.
(a) Peak to peak jitter.
(b) Rms jitter.

It has been assumed in the theoretical analysis that the phase step caused by pointer adjustment has a magnitude of 8.0 VT1.5 SPE UI. This assumption was tested in a simulation by calculating the mean phase before a pointer adjustment and comparing it to the mean phase after a pointer adjustment. This was done for different pointer values and for both positive and negative pointer adjustments. The results are summarized in Table 3-1. As shown, the phase step is close to 8.0 VT1.5 SPE UI for most pointer values and the average phase step over all pointer values is exactly 8.0 VT1.5 SPE UI. However, for some pointer values the phase step can be appreciably different. This result can be explained by the non-uniform distribution of overhead bits in the VT1.5 SPE frame format.

Consider what happens when the initial pointer value is 0 and a positive pointer adjustment occurs. As seen in Fig. 1-13, the DS-1 bits in columns 2 through 26 of the VT1.5 frame format after the pointer adjustment will be delayed by 1 VT1.5 byte, or 8 VT1.5 UI, as compared to before the pointer adjustment. The DS-1 bits in column 27 will be delayed by 2 VT1.5 bytes because of the overhead located in column 1 of the VT1.5 frame. By looking at a single row of the VT1.5 SPE inside of the VT1.5 as shown in Fig. 1-9 for a pointer value of 0, 185 DS-1 bits are delayed by 8 VT1.5 UI and 8 DS-1 bits are delayed by 16 VT1.5 UI. The average delay from a positive pointer adjustment for this case is therefore 8.3316 VT1.5 UI which corresponds to a -8.0230 VT1.5 SPE UI phase step. This value agrees with the simulation result shown in Table 3-1. For the same initial pointer value of 0 and a negative pointer adjustment, see Fig. 1-14, the DS-1 bits in columns 3 through 27 will be advanced by 8 VT1.5 UI and the DS-1 bits in column 2 will be advanced by 16 VT1.5 UI. When the pointer value is 0, there are no DS-1 information bits in column 2 as seen by the VT1.5 SPE frame format in Fig. 1-9. Therefore the average advance of phase is 8 VT1.5 UI which corresponds to a 7.7037 VT1.5 SPE UI phase step. Again, this value agrees with the simulation result shown in Table 3-1.

Table 3-1 Phase step as a function of initial pointer value and pointer adjustment direction.

Initial Pointer Value	Pointer Adjustment Direction	Phase Step (VT1.5 SPE UI)
25,51,77,103	Positive	-7.7037
24,50,76,102	Positive	-7.7436
0-23,26-49,52-75,78-101	Positive	-8.0230
0,26,52,78	Negative	7.7037
25,51,77,103	Negative	7.7436
1-24,27-50,53-76,79-102	Negative	8.0230

Simulations were done to calculate the peak to peak jitter when a single pointer adjustment occurs for various initial pointer values. For a positive pointer adjustment, the initial pointer values chosen were 0, 24, and 25 in order to study the effect of the three different magnitudes of phase steps. Fig. 3-7 shows the peak to peak jitter versus DS-1 offset frequency when there is a single positive pointer adjustment. As expected from the magnitudes of the phase steps shown in Table 3-1, the worst case initial pointer value is 0. Initial pointer values of 24 and 25 produce slightly less jitter because the size of the phase step caused by a pointer adjustment is smaller. The worst case peak to peak jitter for the system during a single isolated phase step is higher than 4.25 DS-1 UI.

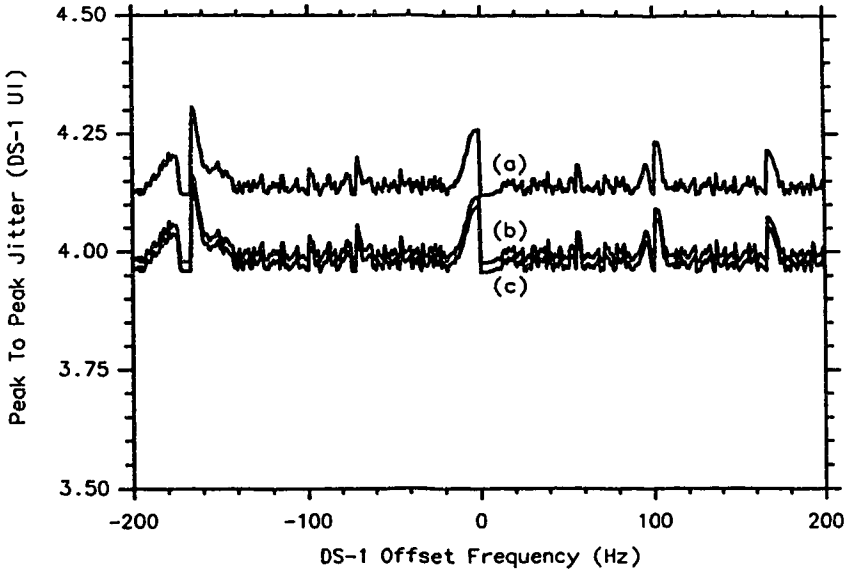

Fig. 3-7 Peak to peak jitter with a single positive pointer adjustment.
(a) Initial pointer value = 0.
(b) Initial pointer value = 24.
(c) Initial pointer value = 25.

Simulations were also performed during a single negative pointer adjustment. Initial pointer values for this case were chosen as 0, 1, and 25. Fig.

3-8 shows the simulation results for a single negative pointer adjustment. The worst case value of initial pointer for this case is 1 which agrees with the results of Table 3-1. Initial pointer values of 0 and 25 produce slightly less jitter. As with positive pointer adjustments, the worst case peak to peak jitter exceeds 4.25 DS-1 UI.

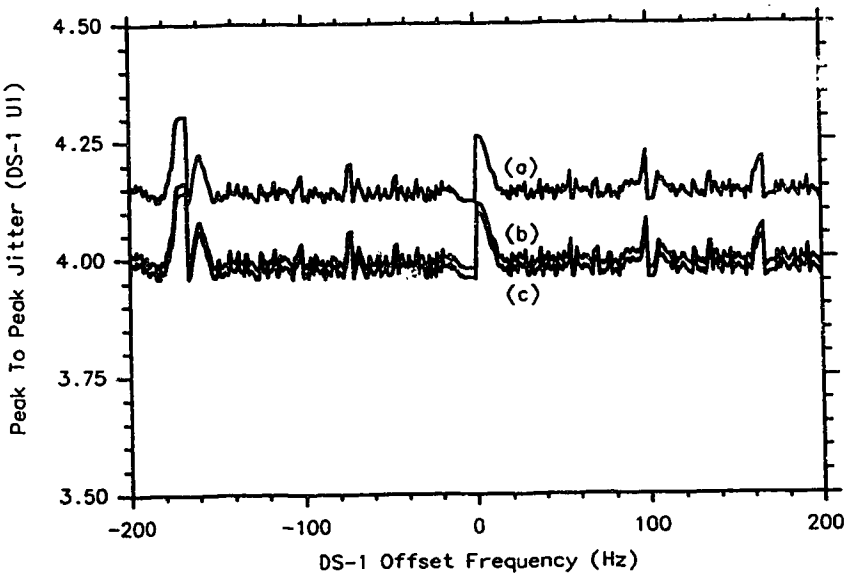

Fig. 3-8 Peak to peak jitter with a single negative pointer adjustment.
(a) Initial pointer value = 1.
(b) Initial pointer value = 25.
(c) Initial pointer value = 0.

Degraded Synchronization Mode

Simulations of the system operating in degraded synchronization mode were also performed. Fig. 3-9 shows the waiting time jitter during degraded synchronization mode versus VT1.5 offset frequency. The DS-1 offset frequency was set to zero and the initial pointer value was set to twelve. As in non-degraded synchronization mode with a single pointer adjustment, the jitter in this case is

very high. The peak to peak jitter is greater than 4.0 DS-1 UI for all VT1.5 frequency offsets, and the rms jitter is greater than 1.0 DS-1 UI for large VT1.5 offset frequencies.

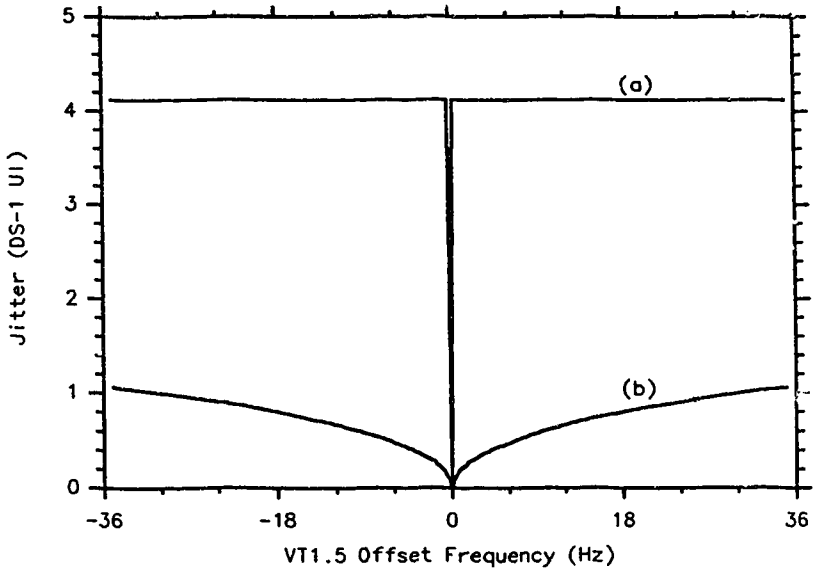

Fig. 3-9 Jitter versus VT1.5 offset frequency without jitter reduction techniques.
(a) Peak to peak jitter.
(b) Rms jitter.

Comparison to Theory

Peak to peak jitter results obtained by theoretical analysis and by simulation for both non-degraded synchronization mode and degraded synchronization mode are in close agreement. Table 3-2 summarizes the simulation results for peak to peak jitter during non-degraded synchronization mode with a single pointer adjustment. These results are given for a DS-1 offset frequency of 0 Hz. The theoretical prediction for peak to peak jitter with a single isolated pointer adjustment is 4.1087 DS-1 UI. The worst case relative error between this result and the simulation result is 3.7%. This error can be explained

by the assumption in the theoretical analysis that the phase step caused by a pointer adjustment is 8.0 VT1.5 SPE UI which is not exact. Rms results for degraded synchronization mode obtained by simulation and by theory are also in close agreement. The average absolute error between theoretical results and simulation results is less than 1%.

Table 3-2 Peak to peak jitter as a function of initial pointer value and pointer adjustment direction.

Initial Pointer Value	Pointer Adjustment Direction	Peak to peak jitter (DS-1 UI)
25,51,77,103	Positive	3.9564
24,50,76,102	Positive	3.9769
0-23,26-49,52-75,78-101	Positive	4.1203
0,26,52,78	Negative	3.9564
25,51,77,103	Negative	3.9769
1-24,27-50,53-76,79-102	Negative	4.1204

iv. Implementation Considerations

The system described and analyzed in this Chapter has the advantage of very simple synchronizers and desynchronizers. The system operates within the CCITT recommendations when in non-degraded synchronization mode when there are no pointer adjustments. However when pointer adjustments occur, either in non-degraded synchronization mode or in degraded synchronization mode, the jitter performance of the system no longer meets the CCITT recommendations. It has been shown that the peak to peak jitter in the presence of pointer adjustments exceeds 4.0 DS-1 UI, and the rms jitter can exceed 1.0 DS-1 UI. These jitter levels clearly do not meet the CCITT recommendation for maximum jitter generation of less than 1.0 DS-1 UI of peak to peak jitter and 0.3 DS-1 UI of rms jitter. For this system to meet jitter recommendations, it would be necessary to prevent pointer adjustments. Synchronization for this type of a

system would be performed by a slip buffer which would repeat a VT1.5 frame or delete a VT1.5 frame when necessary. This operation is referred to as slipping [6]. During non-degraded synchronization mode, the time between slips would be very long because the clocks in the network are synchronous. However, during degraded synchronization mode, the system would slip very often resulting in the loss of DS-1 data every time a slip occurs. All equipment receiving the corrupted DS-1 would then be effected.

v. Summary

In this Chapter it has been shown why the jitter resulting from pointer adjustments when no methods of jitter reduction are used in the system is higher than 4.0 DS-1 UI peak to peak and 1.0 DS-1 UI rms. The result for peak to peak jitter agrees with results given in recent ECSA contributions [17] which show that the system does not meet the CCITT recommendations for jitter generation. Theoretical analysis of the waiting time jitter was performed in this Chapter which showed that the spectral components of the jitter are highest at low frequencies and therefore cannot be filtered out by a conventional PLL. Simulation results have shown that the phase step caused by a pointer adjustment is not exactly 8.0 VT1.5 SPE UI, but is dependent on the initial pointer value and the pointer adjustment direction.

IV. FIXED RATE POINTER SPREADING

In this Chapter waiting time jitter is estimated when fixed rate pointer spreading is used to reduce jitter caused by pointer adjustments. Results are compared to those obtained when no methods are used to reduce jitter. The system with fixed rate pointer spreading is first described and then theoretically analyzed while in non-degraded and degraded synchronization mode. Simulation results are then discussed along with implementation considerations of the system.

I. Description

The system analyzed in this Chapter has the same plus/zero/minus VT1.5 SPE to VT1.5 synchronizer that was used in the previous Chapter. The DS-1 to VT1.5 SPE synchronizer is also the same. The differences between the system without jitter reduction techniques and the system with fixed rate pointer spreading occur at the desynchronizer. A block diagram of the system with fixed rate pointer spreading is shown in Fig. 4-1. After synchronization and transmission the received VT1.5 is first demapped and the VT1.5 SPE is removed. This VT1.5 SPE is then fed into a fixed rate pointer spreader consisting of a pointer spreading elastic store and associated control logic. During normal operation, the difference in phase between the read and write clocks of the pointer spreading elastic store is constant. When a pointer adjustment occurs, a phase step occurs on the incoming VT1.5 SPE which corresponds to a phase step on the write clock of the elastic store. At the same time, the fixed rate pointer spreading logic causes the phase step to be absorbed in the pointer spreading elastic store. Therefore, the VT1.5 SPE at the output of the pointer spreader does not contain a phase step. After the pointer adjustment the phase step that has

been absorbed in the elastic store is slowly leaked out in fractional phase steps at a fixed rate by the pointer spreading logic. The parameters of the fixed rate pointer spreader that will effect the jitter are the rate at which the phase step is leaked out and the magnitudes of the fractional phase steps. The final stage of the desynchronizing process as shown in Fig. 4-1 is the removal of the DS-1 from the VT1.5 SPE and the smoothing of the DS-1 by the desynchronizing PLL. As before, a second order 25 Hz PLL is used in the desynchronizer and a first order 10 Hz high pass filter is used in the jitter measuring equipment.

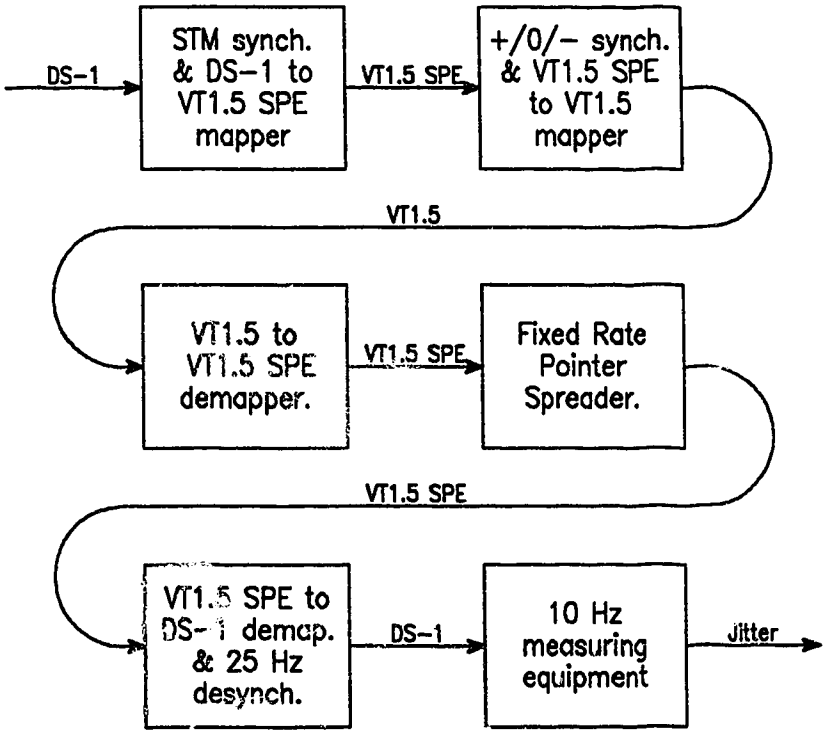

Fig. 4-1 System block diagram with fixed rate pointer spreading.

From the results in Chapter III, the phase step caused by a pointer adjustment is dependent on the initial pointer value. In order to keep the fixed rate pointer spreader implementation as general as possible, the phase step caused

by a pointer adjustment was assumed independent of the initial pointer value and equal to 8.0 VT1.5 SPE UI. Therefore, when a pointer adjustment occurs, the pointer spreading logic causes 8.0 VT1.5 SPE UI to be absorbed in the pointer spreading elastic store. The fixed rate pointer spreader analyzed in this Chapter has several possible magnitudes of fractional phase steps that can be leaked which are 1, 1/2, 1/4, 1/8, 1/16, and 1/32 VT1.5 SPE UI. A fractional phase step magnitude of 1/2 VT1.5 SPE UI means that the 8 VT1.5 SPE UI phase step caused by a pointer adjustment would be leaked out by 16 fractional phase steps spread out in time, each with a magnitude of 1/2 VT1.5 SPE UI. Another parameter necessary to characterize the fixed rate pointer spreader is the rate at which the phase is leaked out. The rate at which the fixed rate pointer spreader leaks out the fractional phase steps is specified in VT1.5 SPE UI per VT1.5 SPE frames. The higher this leak rate, the faster the phase is leaked out. A more convenient form of the leak rate is its inverse, referred to as the leak period which is specified in VT1.5 SPE frames per VT1.5 SPE UI. For degraded synchronization mode operation, the leak rate must be chosen such that the entire 8 VT1.5 SPE UI caused by a pointer adjustment is leaked out before the next pointer adjustment occurs. This is necessary to prevent spilling of the pointer spreading elastic store. The final parameter that is important for characterizing the pointer spreader is the time at which the first fractional phase step is leaked out after a pointer adjustment occurs. The pointer spreader analyzed in this Chapter leaks the first fractional phase step out immediately after the pointer adjustment occurs.

ii. Theoretical Analysis

Non-Degraded Synchronization Mode

Fixed rate pointer spreading can be analyzed for the system operating in non-degraded synchronization mode by considering special cases for the leak period. If the leak period is very small meaning that the pointer adjustment is leaked out quickly compared to the PLL and jitter measuring equipment responses, the fixed rate pointer spreader will not improve the peak to peak jitter performance. Therefore the theoretical peak to peak jitter with very small leak periods is the same as for the case without jitter reduction techniques which is 4.1087 DS-1 UI. As the leak rate is slowed down, or equivalently the leak period is increased, the peak to peak jitter should decrease. For very large leak periods, the peak to peak jitter will be entirely due to the individual fractional phase steps because each fractional phase step can be considered isolated. For this case the PLL and jitter measuring equipment will see an isolated fractional phase step and Eqn. 3-4 can therefore be applied with the magnitude of the fractional phase step used for the value of K. Table 4-1, summarizes the minimum theoretical peak to peak jitter using this assumption versus the magnitude of the fractional phase step.

Table 4-1 Theoretical minimum peak to peak jitter as a function of fractional phase step magnitude.

Fractional Phase Step Magnitude (VT1.5 SPE UI)	Peak To Peak Jitter (DS-1 UI)
1	0.5136
1/2	0.2568
1/4	0.1284
1/8	0.0642
1/16	0.0321
1/32	0.0161

Degraded Synchronization Mode

Fourier analysis can be used to obtain theoretical rms jitter estimates when the system is operating in degraded synchronization mode. Fixed rate pointer spreading will alter the waiting time jitter waveform as shown in Fig. 4-2. The dotted line represents the phase comparator output in the synchronizer and the solid line represents the phase comparator output in the desynchronizer after the fixed rate pointer spreader. For the example shown the magnitude of the fractional phase steps is 1 VT1.5 SPE UI and the leak period is 1 VT1.5 frame per VT1.5 UI.

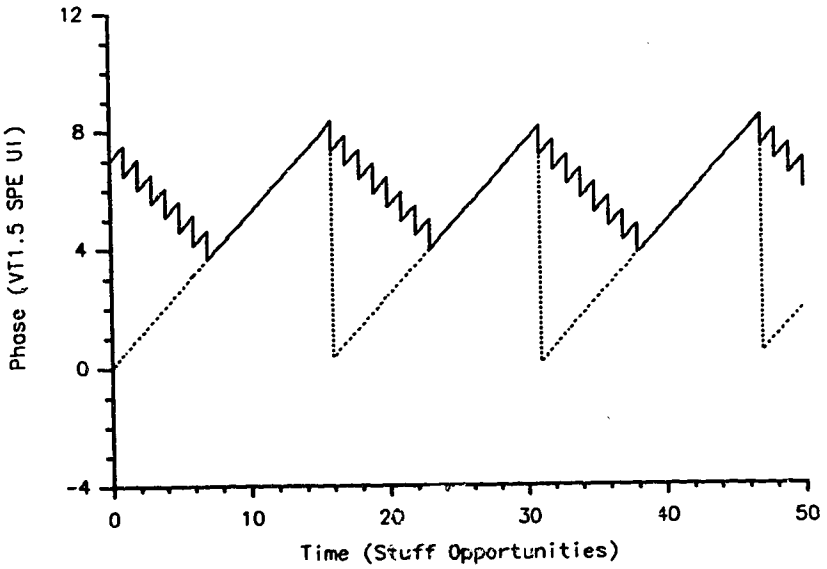

Fig. 4-2 Waiting time jitter waveform with fixed rate pointer spreading.

The waiting time jitter waveform in the synchronizer with or without fixed rate pointer spreading is the same because the same VT1.5 SPE to VT1.5 synchronizer is used in both systems. Therefore the waveform represented by the dotted line in Fig. 4-2 is the same as the waiting time jitter waveform, $\phi_s(t)$, as

calculated in Chapter III. To describe the fixed rate pointer spreader, α is defined as the leak period in VT1.5 SPE frames per VT1.5 SPE UI and β is defined as the magnitude of a fractional phase step in VT1.5 SPE UI. The desynchronizer waiting time jitter waveform as shown by the solid line in Fig. 4-2 can be presented as (see Appendix C)

$$\phi_{fps}(t) = \phi_s(t) * h_{fps}(t), \tag{4-1}$$

where $\phi_s(t)$ is the synchronizer waiting time jitter waveform given by Eqn. 3-7 and $h_{fps}(t)$ is the equivalent impulse response of the fixed rate pointer spreader and is given by (see Fig. 4-3)

$$h_{fps}(t) = \frac{\beta}{8} \sum_{n=1}^{8/\beta} \delta\left(t-(n-1)\alpha\beta\right). \tag{4-2}$$

The Fourier transform of $h_{fps}(t)$ is

$$H_{fps}(f) = \frac{\beta}{8} \sum_{n=1}^{8/\beta} e^{-j2\pi f(n-1)\alpha\beta}, \tag{4-3}$$

and therefore, the Fourier transform of the waiting time jitter waveform with fixed rate pointer spreading is

$$\Phi_{fps}(f) = \Phi_s(f) H_{fps}(f). \tag{4-4}$$

Eqn. 4-4 is valid as long as the distance between successive pointer adjustments is larger than the time taken to leak out a single pointer adjustment. From the definition of the stuff ratio, the time between successive pointer adjustments is approximately $1/|\rho|$. For the worst case offset frequency, this must be larger than the time taken to leak out 8 VT1.5 SPE UI which will be 8α. Therefore, the relation between the VT1.5 offset frequency, ν, and the maximum value of α can be found with the aid of Eqn. 3-6 as

$$8\alpha < \frac{1}{|\rho|}, \text{ or } \qquad \alpha < \frac{27000}{13|\nu|}. \qquad (4\text{-}5)$$

Using a maximum VT1.5 offset frequency of 35 Hz, the maximum value of α is approximately 59 VT1.5 SPE frames per VT1.5 SPE UI.

Fig. 4-3 shows the equivalent impulse response of a fixed rate pointer spreader with α equal to 25 VT1.5 SPE frames per VT1.5 SPE UI and β equal to 1 VT1.5 SPE UI, and Fig. 4-4 shows the corresponding frequency domain transfer function. The zeroes of the frequency domain transfer function can be found from Eqn. 4-3; they occur at multiples of $1/8\alpha$. The period of the transfer function, which is the distance between the frequencies where the magnitude of the gain goes to 0 dB, is equal to $1/\alpha\beta$. For the example shown, with α equal to 25 VT1.5 SPE frames per VT1.5 SPE UI and β equal to 1 VT1.5 SPE UI, the zeroes will occur at 0.005 cycles per stuff opportunity and the period is equal to 0.04 cycles per stuff opportunity. These frequencies can be de-normalized by multiplying them by the stuff opportunity rate of 2000 Hz. This calculation reveals that the zeroes are at 10 Hz, and the period is 80 Hz which agrees with the results plotted in Fig. 4-4. The unfiltered power spectral density which results when this fixed rate pointer spreader is used is shown in Fig. 4-5 for a VT1.5 offset frequency of 35 Hz. These results were calculated by applying the equivalent time domain transfer function of the fixed rate pointer spreader to the unfiltered power spectral density of the system without jitter reduction techniques. The resulting spectrum has less power in the low frequency components than the spectrum of the system without jitter reduction (see Fig. 3-4). The rms jitter with fixed rate pointer spreading should therefore be reduced.

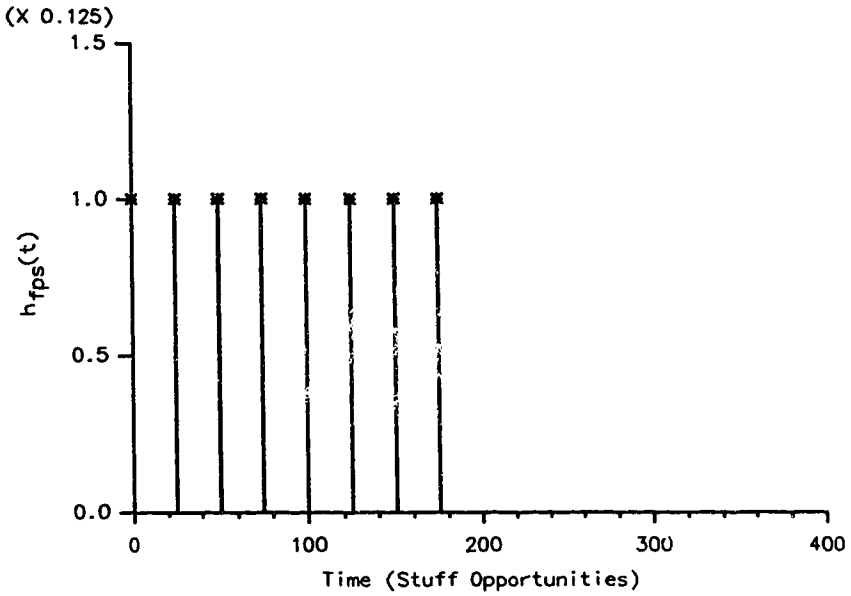

Fig. 4-3 Equivalent impulse response of fixed rate pointer spreader.
α = 25 VT1.5 SPE frames per VT1.5 SPE UI.
β = 1 VT1.5 SPE UI.

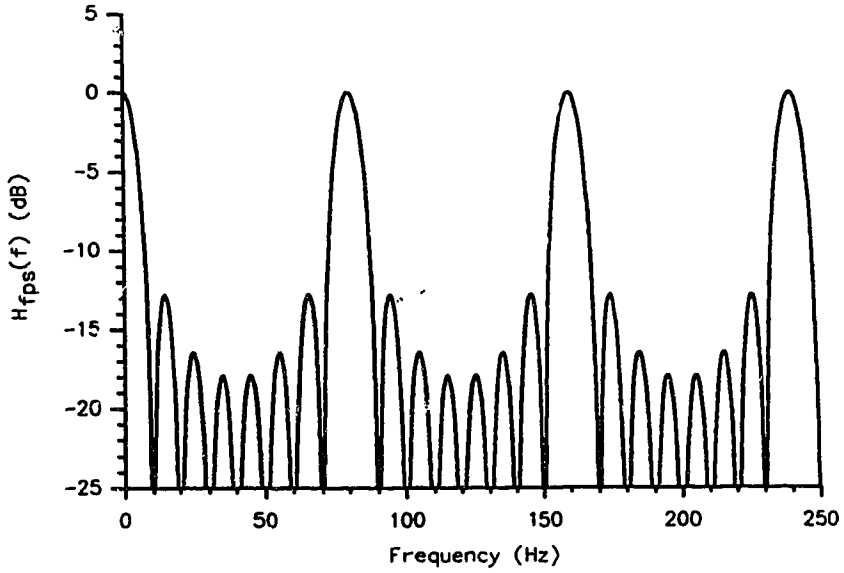

Fig. 4-4 Equivalent transfer function of fixed rate pointer spreader.
α = 25 VT1.5 SPE frames per VT1.5 SPE UI.
β = 1 VT1.5 SPE UI.

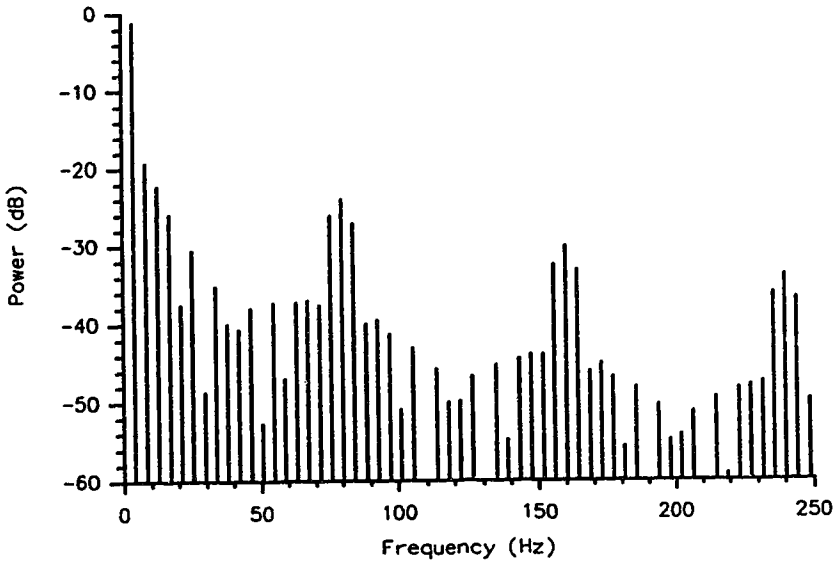

Fig. 4-5 Unfiltered power spectral density with fixed rate pointer spreading.
α = 25 VT1.5 SPE frames per VT1.5 SPE UI.
β = 1 VT1.5 SPE UI.

A possible improvement to the fixed rate pointer spreader described above is to decrease the magnitude of the fractional phase steps while keeping the leak rate the same. Fig. 4-6 shows the equivalent impulse response of a fixed rate pointer spreader with α equal to 25 VT1.5 SPE frames per VT1.5 SPE UI and β equal to 1/2 VT1.5 SPE UI, and Fig. 4-7 shows the resulting frequency domain transfer function. The effect of decreasing the magnitude of the fractional phase steps is to increase the period of the transfer function from 80 Hz to 160 Hz. The zeroes of the transfer function are only dependent on α and therefore remain at multiples of 10 Hz. The magnitude of the transfer function at the frequencies that will be passed by the 25 Hz PLL are also less when the fractional phase step is reduced. Therefore, the rms jitter should be reduced further by decreasing the fractional phase step magnitude. Fig. 4-8 is a plot of the unfiltered power spectral

density for this pointer spreader when the VT1.5 offset frequency is 35 Hz. As expected, the magnitude of the power spectral density at the frequencies that will be passed by the 25 Hz PLL have been slightly reduced as compared to the case with β equal to 1 VT1.5 SPE UI.

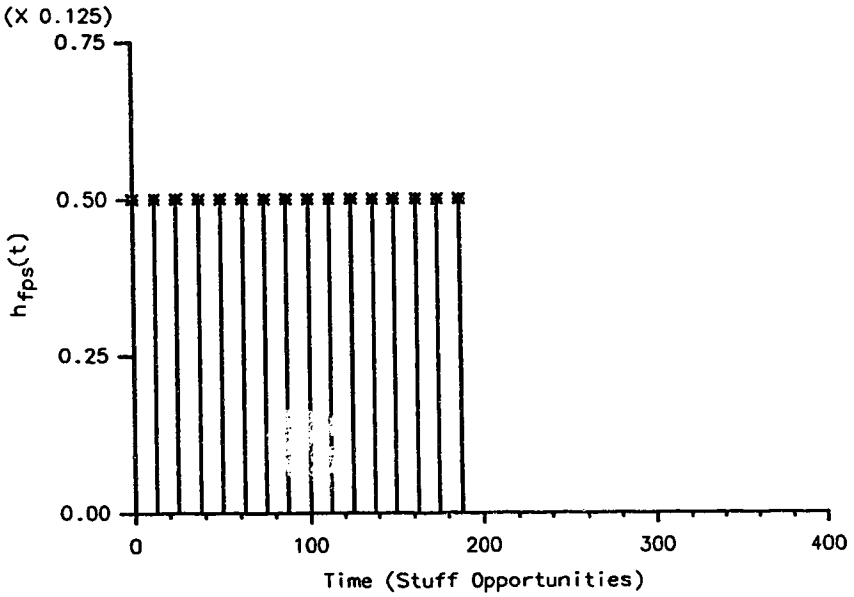

Fig. 4-6 Equivalent impulse response of fixed rate pointer spreader.
α = 25 VT1.5 SPE frames per VT1.5 SPE UI.
β = 1/2 VT1.5 SPE UI.

The rms jitter for a fixed rate pointer spreader was calculated for a system operating in degraded synchronization mode with a maximum VT1.5 offset frequency of ±35 Hz. The value of α was chosen as 56 VT1.5 SPE frames per VT1.5 SPE UI which was calculated assuming a maximum VT1.5 offset frequency of 35 Hz and including a small amount of margin. Rms jitter versus VT1.5 offset frequency for various values of β is shown in Fig. 4-9. The largest decrease in rms jitter that is obtained by decreasing the fractional phase magnitude occurs when β is decreased from 1 to 1/2 VT1.5 SPE UI. The maximum value of rms jitter with β

equal to 1 VT1.5 SPE UI is 0.26 DS-1 UI. When β is decreased to 1/2 VT1.5 SPE UI this maximum value of rms jitter decreases to 0.25 DS-1 UI. A more dramatic decrease in rms jitter occurs for large VT1.5 offset frequencies where the rms jitter is reduced from 0.12 DS-1 UI for β equal to 1 VT1.5 SPE UI to 0.07 DS-1 UI for β equal to 1/2 VT1.5 SPE UI. When β is reduced below 1/2 VT1.5 SPE UI the change in rms jitter is very minimal. These results suggest that the best value of the fractional phase step magnitude is 1/2 VT1.5 SPE UI because the increase in complexity associated with decreasing β below 1/2 VT1.5 SPE UI does not significantly improve the rms jitter performance. The results obtained for rms jitter also suggest that a system utilizing fixed rate pointer spreading would be able to meet the CCITT recommendations for maximum rms jitter generation of 0.3 DS-1 UI.

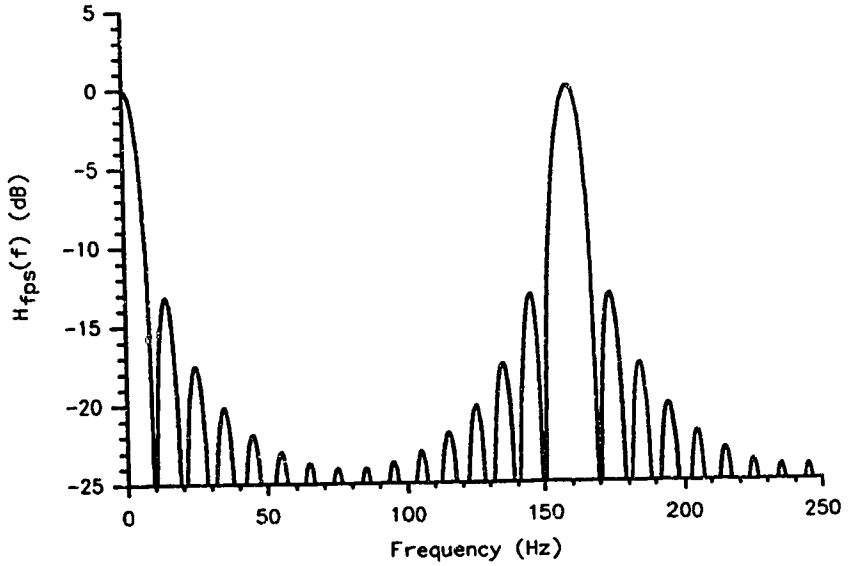

Fig. 4-7 Equivalent transfer function of fixed rate pointer spreader.
α = 25 VT1.5 SPE frames per VT1.5 SPE UI.
β = 1/2 VT1.5 SPE UI.

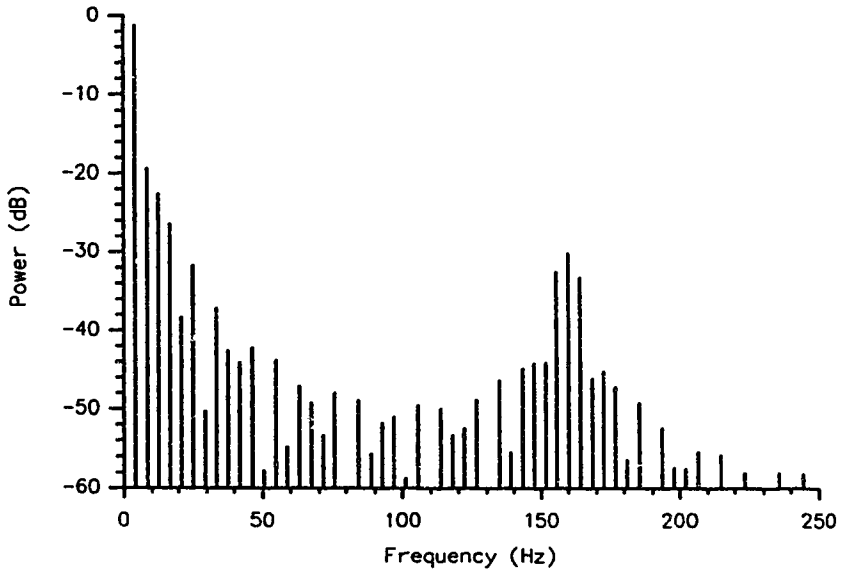

Fig. 4-8 Unfiltered power spectral density with fixed rate pointer spreading.
α = 25 VT1.5 SPE frames per VT1.5 SPE UI.
β = 1/2 VT1.5 SPE UI.

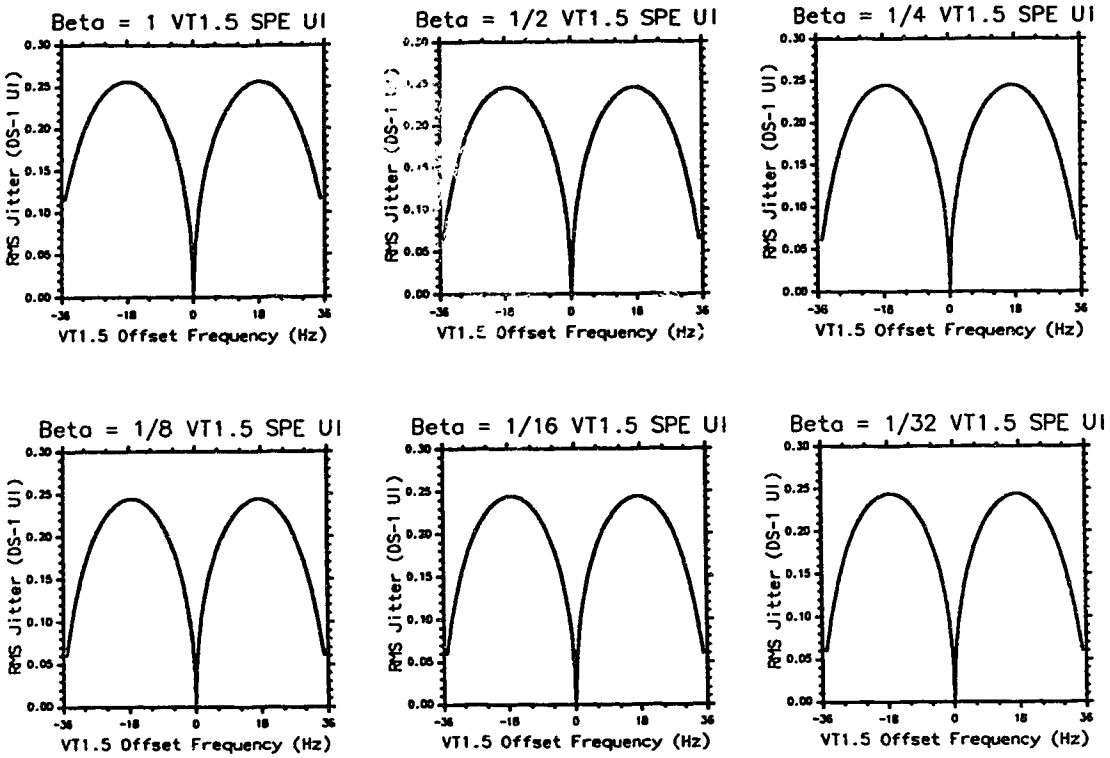

Fig. 4-9 Theoretical rms jitter versus VT1.5 offset frequency with fixed rate pointer spreading.
α = 56 VT1.5 SPE frames per VT1.5 SPE UI.

iii. Simulation Results

Simulations were done for both degraded and non-degraded synchronization modes of operation and are compared to the theoretical results obtained above. Transient durations of 1.0 second were used in all of the simulations to allow the PLL and high pass filters to reach steady state conditions. Non-degraded synchronization mode was studied with a single positive pointer adjustment and fixed rate pointer spreaders which had different leak rates and magnitudes of fractional phase steps. Sampling durations were 1.0 second longer than the time taken to leak out the entire pointer adjustment. For the simulations of degraded synchronization mode, the leak period was set to 56

VT1.5 SPE frames per VT1.5 SPE UI and a sampling duration of 40.0 seconds was used.

Non-Degraded Synchronization Mode

Simulations were done to calculate the peak to peak jitter when a single pointer adjustment occurs for various leak periods and fractional phase step magnitudes. For a positive pointer adjustment, the initial pointer values chosen were 0, 24, and 25 in order to study the effect of the three different magnitudes of phase steps caused by a pointer adjustment. Fig. 4-10 shows the peak to peak jitter versus leak period for the system with fixed rate pointer spreading. The initial pointer value for this simulation was 0. As expected the maximum value of peak to peak jitter for small leak periods is 4.11 DS-1 UI and as the leak period is increased the peak to peak jitter levels decrease. The minimum jitter that can be obtained is dependent on β as expected from theory.

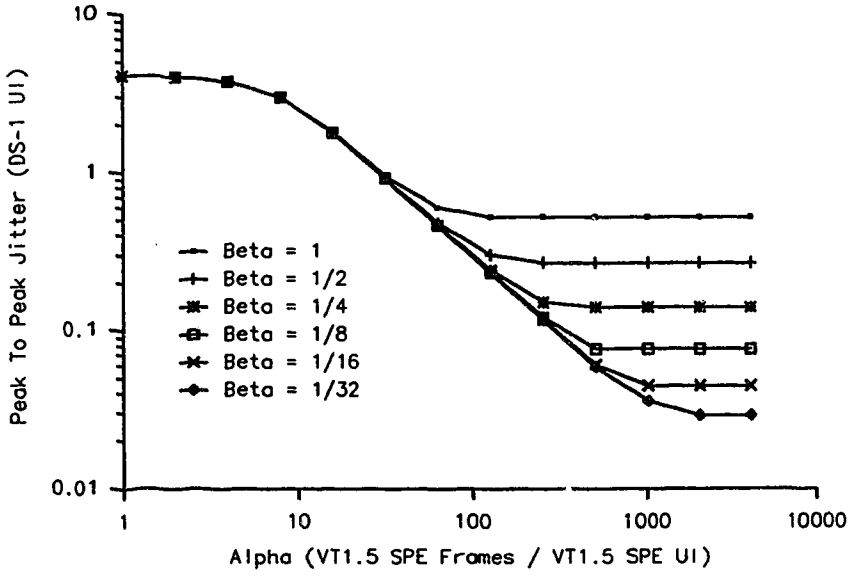

Fig. 4-10 Peak to peak jitter with a single positive pointer adjustment and an initial pointer value of 0.

Fig. 4-11 shows the peak to peak jitter versus leak period for the system with fixed rate pointer spreading when the initial value of the pointer is 25. Results for an initial pointer value of 24 are not shown because they are virtually identical to the results for an initial pointer value of 25. For these values of initial pointer, the minimum jitter that can be obtained for large leak periods is increased as compared to that for an initial pointer value of 0. Again, this is caused by the assumption of the fixed rate pointer spreader that the phase step caused by a pointer adjustment is 8.0 VT1.5 SPE UI. The results shown in Figs. 4-10 and 4-11 suggest that the best choice for β based on the minimum peak to peak jitter levels is 1/4 VT1.5 SPE UI. More importantly, for values of α near 56 VT1.5 SPE frames per VT1.5 SPE UI the best choice for β would appear to be 1/2 VT1.5 SPE UI. The improved jitter performance that is gained by further decreasing β, for this value of α, is not significant enough to justify the associated increase in circuit complexity.

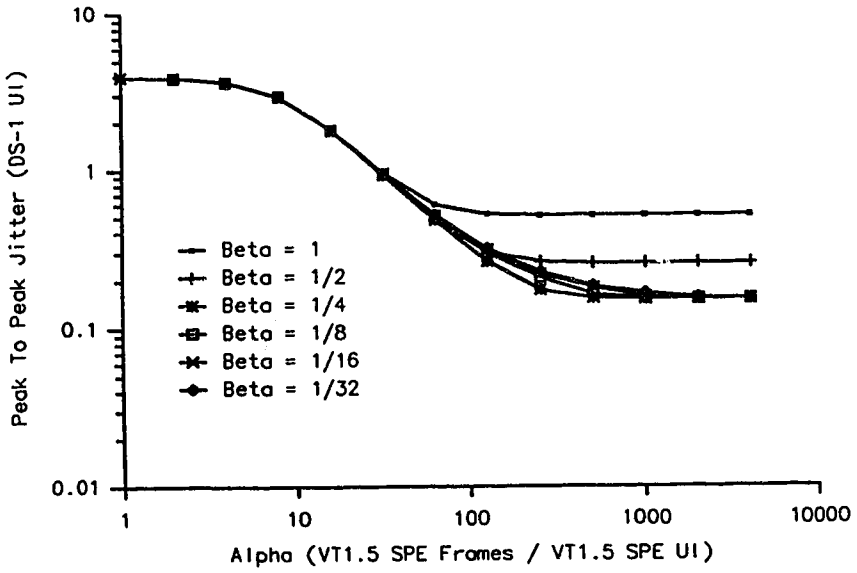

Fig. 4-11 Peak to peak jitter with a single positive pointer adjustment and an initial pointer value of 25.

Degraded Synchronization Mode

Simulations of the system operating in degraded synchronization mode were also performed. The value of α for this system was chosen as 56 VT1.5 SPE frames per VT1.5 SPE UI. The rms jitter and peak to peak results of these simulations for various values of β are shown in Figs. 4-12 and 4-13 respectively. As expected from theory, the best choice for the fractional phase step magnitude is 1/2 VT1.5 SPE UI. The results for the peak to peak jitter also support this claim. The minimum jitter is obtained when β is equal to 1/2 VT1.5 SPE UI. For the system with β equal to 1/2 VT1.5 SPE UI the maximum peak to peak jitter level would be less than 0.55 DS-1 UI and the maximum rms jitter level would be less than 0.25 DS-1 UI. Thus, this system meets the CCITT recommendations for maximum jitter generation.

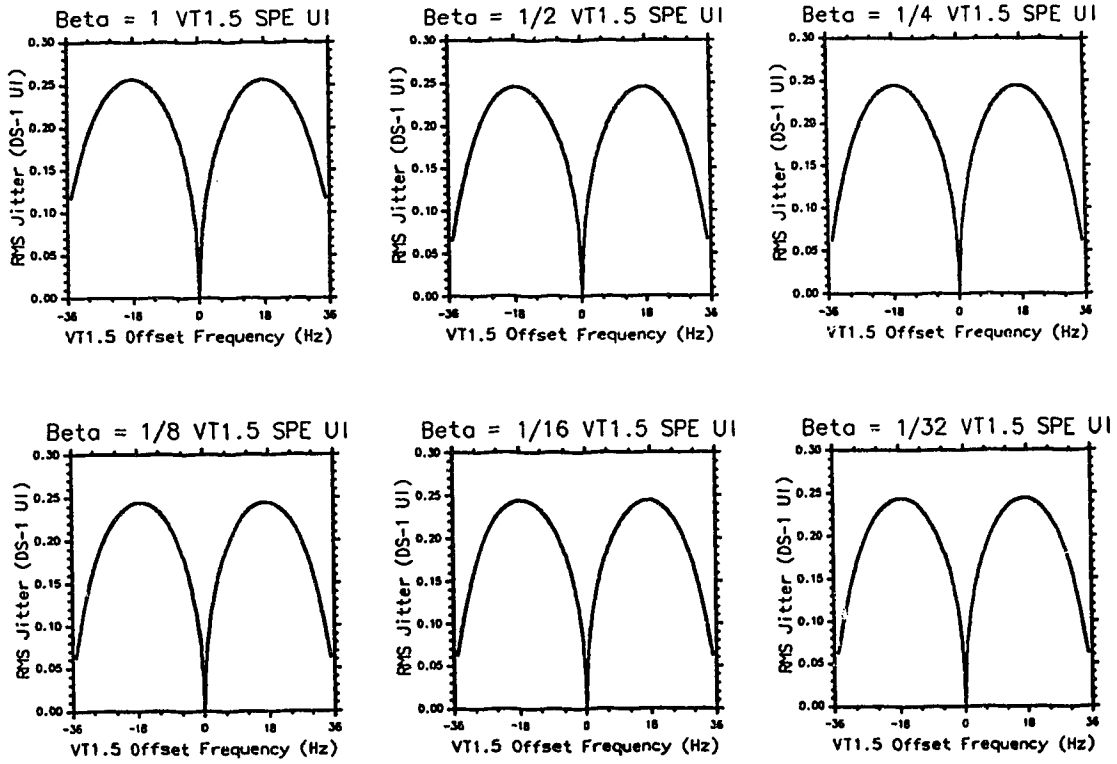

Fig. 4-12 Rms jitter with fixed rate pointer spreader.
α = 56 VT1.5 SPE frames per VT1.5 SPE UI.

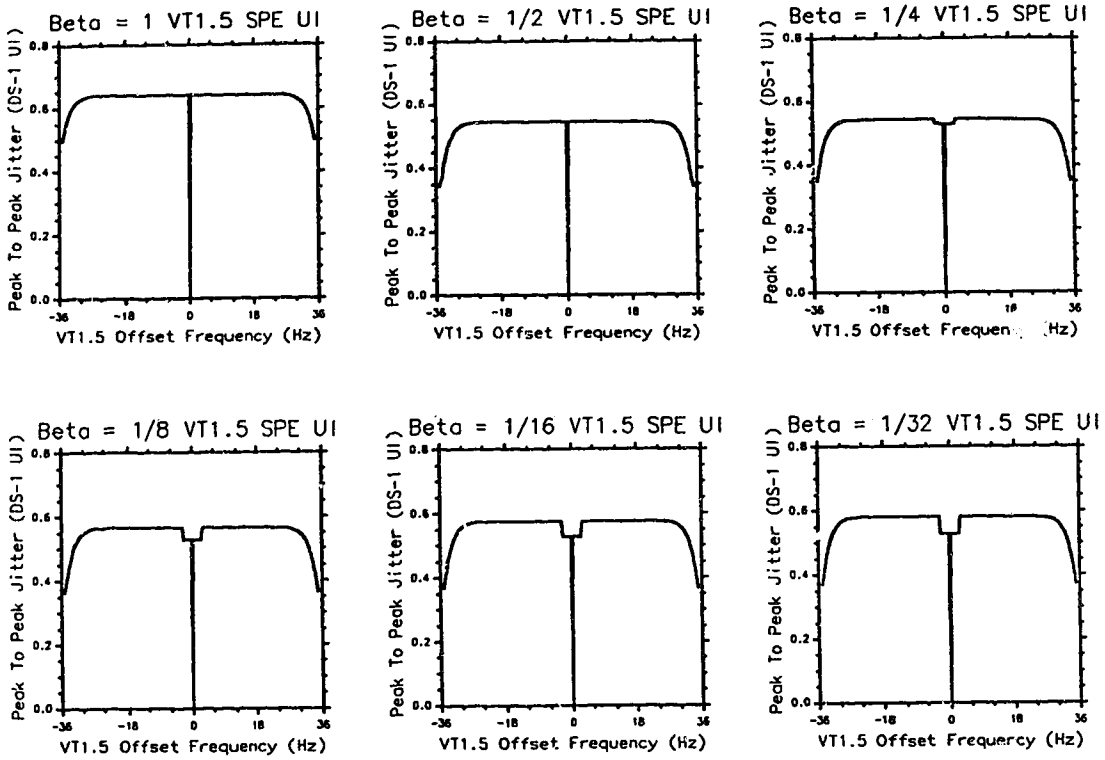

Fig. 4-13 Peak to peak jitter with fixed rate pointer spreader.
α = 56 VT1.5 SPE frames per VT1.5 SPE UI.

Comparison to Theory

Minimum values of peak to peak jitter as a function of the fractional phase step magnitudes were taken from the simulation results plotted in Fig. 4-10. The relative error between these results and the theoretical results shown in Table 4-1 ranged from a minimum of 2% when the fractional phase step magnitude was 1 VT1.5 SPE UI to a maximum of 45% when the fractional phase step magnitude was 1/32 VT1.5 SPE UI. The minimum values of jitter that were obtained by simulation are higher than the minimum values expected from theory. This can be explained by the fact that a positive pointer adjustment for an initial pointer value of 0 produces a phase hit of 8.023 VT1.5 SPE UI instead of the assumed 8.0 VT1.5 SPE UI. The fixed rate pointer spreading elastic store only absorbs 8.0

VT1.5 SPE UI and therefore there is an additional phase step of 0.023 VT1.5 SPE UI which is not included in the theoretical results. For degraded mode, the results of the rms jitter versus VT1.5 offset frequency obtained from simulations and from theory are in close agreement. The average absolute error between simulation and theoretical results for all values of β is less than 1%.

iv. Implementation Considerations

The system described and analyzed in this Chapter has the same advantage of very simple synchronizers and desynchronizers as the system without jitter reduction techniques. The fixed rate pointer spreader is the simplest of the pointer spreading methods for jitter reduction [21-23]. During non-degraded synchronization mode without pointer adjustments, the fixed rate pointer spreader will not effect the waiting time jitter waveform, and therefore the jitter performance versus DS-1 offset frequency will be the same as for the system without jitter reduction techniques. During pointer adjustments, it has been shown that the system meets the CCITT specifications for maximum jitter generation.

v. Summary

In this Chapter it has been shown that the jitter resulting from pointer adjustments when fixed rate pointer spreading is used in the system meets the CCITT recommendations for jitter generation. A system can be designed that will work with a maximum VT1.5 offset frequency of ±35 Hz and will have a maximum peak to peak and rms jitter levels of 0.54 DS-1 UI and 0.25 DS-1 UI respectively. Another important result obtained by this analysis is that the best magnitude for the magnitude of the fractional phase steps that are leaked out is 1/2 VT1.5 SPE UI when the maximum VT1.5 offset frequency is ±35 Hz.

V. VARIABLE RATE POINTER SPREADING

In this Chapter waiting time jitter is estimated when variable rate pointer spreading is used to reduce jitter caused by pointer adjustments. Results obtained are compared to those obtained when no methods are used to reduce jitter and when fixed rate pointer spreading is used. The system with variable rate pointer spreading is described and then theoretically analyzed while in non-degraded and degraded synchronization modes. Simulation results are then discussed along with implementation considerations of the system.

i. Description

The system analyzed in this Chapter is very similar to the system with fixed rate pointer spreading. Again, the DS-1 to VT1.5 SPE and the VT1.5 SPE to VT1.5 synchronization is done in the same way as in the system without jitter reduction techniques. A block diagram of the system with variable rate pointer spreading is shown in Fig. 5-1. The only difference between the system with variable rate pointer spreading and the system with fixed rate pointer spreading is the pointer spreading logic that is used to leak out the fractional phase steps. With the fixed rate pointer spreader this rate was constant, but with the variable rate pointer spreader, this rate is proportional to the fill of the pointer spreading elastic store. As before when a pointer adjustment occurs, the phase step caused by the pointer adjustment is absorbed in the pointer spreading elastic store. This phase is then leaked out in fractional phase steps at a rate which is proportional to the amount that the elastic store is filled. In this way it can be shown, (Appendix D), that the variable rate pointer spreader acts as a first order low pass filter on the phase of the VT1.5 SPE, and is characterized by the cutoff frequency of this filter. The pointer spreading logic can be designed as an all

digital PLL with a cutoff frequency much less than 1 Hz [21]. As with the fixed rate pointer spreader, the magnitude of the fractional phase steps that are leaked out must be specified along with the cutoff frequency to fully characterize the system. After the VT1.5 SPE has been filtered by the variable rate pointer spreader, the DS-1 is demapped out of the VT1.5 SPE and passed into the desynchronizer PLL. As before, a second order 25 Hz PLL is used in the desynchronizer and a first order 10 Hz high pass filter is used in the jitter measuring equipment.

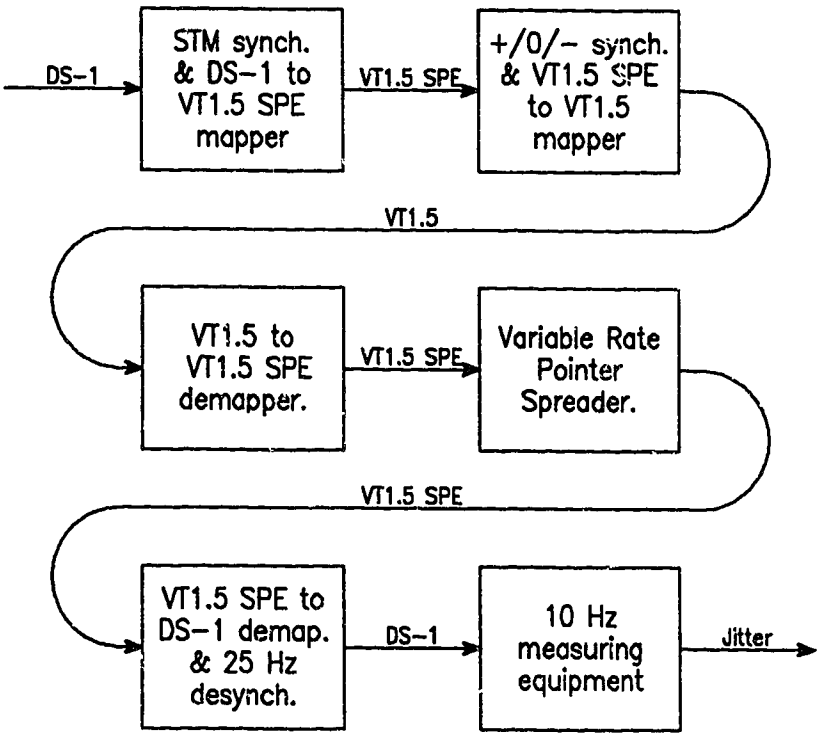

Fig. 5-1 System block diagram with variable rate pointer spreading.

As with the fixed rate pointer spreader, in order to keep the implementation of the variable rate pointer spreader as simple as possible, the phase step caused by a pointer adjustment was assumed independent of the initial pointer value and

equal to 8.0 VT1.5 SPE UI. Therefore, 8.0 VT1.5 SPE UI is absorbed in the pointer spreading elastic store when a pointer adjustment occurs. The fill of the elastic store is then reduced by leaking out fractional phase steps at a rate proportional to the fill. The variable rate pointer spreader analyzed in this Chapter is capable of leaking out a fractional phase step, which can have a magnitude of 1, 1/2, 1/4, 1/8, 1/16, or 1/32 VT1.5 SPE UI.

ii. Theoretical Analysis

Non-Degraded Synchronization Mode

Analysis of the system operating in non-degraded synchronization mode can be accomplished by considering special cases for the cutoff frequency of the variable rate pointer spreader. For cutoff frequencies much higher than the cutoff frequency of the DS-1 desynchronizing PLL, the variable rate pointer spreader is not expected to improve the peak to peak jitter performance because the phase in the pointer spreading elastic store will be leaked out very quickly. Therefore, the theoretical peak to peak jitter when the cutoff frequency is high is 4.1087 DS-1 UI which is the same as for a fixed rate pointer spreader with a fast leak rate. As the cutoff frequency of the variable rate pointer spreader is reduced, the peak to peak jitter is expected to decrease until the magnitude of the fractional phase step determines the minimum amount of jitter. For this case, each fractional phase step can be considered isolated and the magnitude of the fractional phase step can be used for the value of K in Eqn. 3-4 to determine the peak to peak jitter. Table 5-1, summarizes the minimum theoretical peak to peak jitter using this assumption versus the value of the fractional phase step which is in VT1.5 SPE UI. Because the jitter only depends on the magnitude of the fractional phase steps, this table is equivalent to Table 4-1 which gives the theoretical minimum peak to peak jitter for fixed rate pointer spreading.

Table 5-1 Theoretical minimum peak to peak jitter as a function of fractional phase step magnitude.

Fractional Phase Step Magnitude (VT1.5 SPE UI)	Peak To Peak Jitter (DS-1 UI)
1	0.5136
1/2	0.2568
1/4	0.1284
1/8	0.0642
1/16	0.0321
1/32	0.0161

Degraded Synchronization Mode

Fourier analysis is used to obtain theoretical rms jitter estimates when the system is operating in degraded synchronization mode. The variable rate pointer spreader will alter the waiting time jitter waveform as shown in Fig. 5-2. The dotted line represents the phase comparator output in the synchronizer and the solid line represents the phase comparator output in the desynchronizer after the

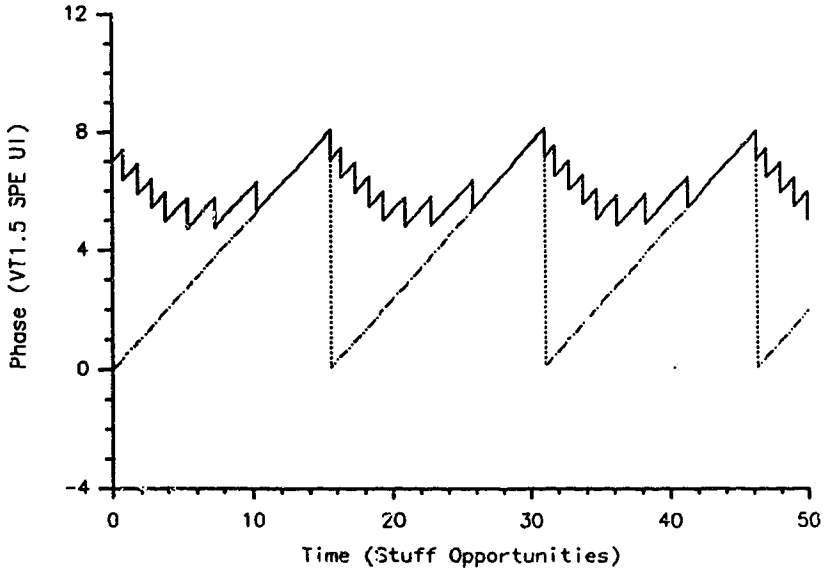

Fig. 5-2 Waiting time jitter waveform with variable rate pointer spreading.

variable rate pointer spreader. For the example shown the magnitude of the fractional phase step is 1 VT1.5 SPE and the cutoff frequency of the variable rate pointer spreader is 50 Hz.

The waiting time jitter waveforms in the synchronizers with and without variable rate pointer spreading are the same because the same plus/zero/minus VT1.5 SPE to VT1.5 synchronizer is used in both systems. Therefore the waveform represented by the dotted line in Fig. 5-2 is $\phi_s(t)$, as calculated in Chapter III. To describe the variable rate pointer spreader, f_{vps} is defined as the normalized cutoff frequency in cycles per stuff opportunity and β is defined as the magnitude of a fractional phase step in VT1.5 SPE UI. By analogy to fixed rate pointer spreading it is desired to approximate the waiting time jitter waveform with a time domain function of the form

$$\phi_{vps}(t) = \phi_s(t) * h_{vps}(t), \tag{5-1}$$

where $\phi_s(t)$ is the synchronizer waiting time jitter waveform given by Eqn. 3-7 and $h_{vps}(t)$ is the equivalent impulse response of the variable rate pointer spreader. This impulse response will be given by

$$h_{vps}(t) = \frac{\beta}{8} \sum_{n=1}^{8/\beta} \delta(t - \tau_n), \tag{5-2}$$

where an approximation for τ_n must be determined. In order to approximate the waiting time jitter waveform in this manner it is necessary to make two assumptions. The first assumption is that a pointer adjustment occurs every $1/|\rho|$ stuff opportunities, and the second assumption is that all 8.0 VT1.5 SPE UI will be leaked out between successive pointer adjustments. Using these assumptions and the cutoff frequency of the variable rate pointer spreader, the relation

$$\tau_n = \frac{-1}{2\pi f_{vps}} \ln\left[1 - \frac{(n-1)\beta}{8}\left[1 - e^{-j2\pi f_{vps}/|\rho|}\right]\right], \qquad (5\text{-}3)$$

can be derived. See Appendix D for this derivation. The Fourier transform of $h_{vps}(t)$ is

$$H_{vps}(f) = \frac{\beta}{8} \sum_{n=1}^{8/\beta} e^{-j2\pi f \tau_n}, \qquad (5\text{-}4)$$

and therefore, the Fourier transform of the waiting time jitter waveform with variable rate pointer spreading is

$$\Phi_{vps}(f) = \Phi_s(f) H_{vps}(f). \qquad (5\text{-}5)$$

Fig. 5-3 shows the equivalent impulse response of a variable rate pointer spreader with f_{vps} equal to 1 Hz, β equal to 1 VT1.5 SPE UI, and a VT1.5 offset frequency of 35 Hz. The leak rate is quickest just after the pointer adjustment and slows as the phase is leaked out. The delta function at time 0 causes the first fractional phase step to be leaked out immediately after the pointer adjustment occurs. For this case the time between successive pointer adjustments is approximately 475 stuff opportunities and from the impulse response, all 8.0 VT1.5 SPE UI will be leaked out in this time. The equivalent frequency domain transfer function for this impulse response is shown in Fig 5-4. The maximum attenuation of the waiting time jitter occurs at frequencies between approximately 5 and 25 Hz which is in the pass band of the PLL and the jitter measuring equipment. The behavior of the transfer function at higher frequencies is noise like with a minimum attenuation of approximately 4 dB. The unfiltered power spectral density of the waiting time jitter waveform for this example is shown in Fig. 5-5. These results were calculated by applying the equivalent time domain transfer function of the variable rate pointer spreader to the unfiltered power spectral density of the system without jitter reduction techniques. As expected from the equivalent transfer function of the variable rate pointer spreader, the

components of the power spectral density near the pass band of the PLL and the jitter measuring equipment are reduced. The rms jitter with variable rate pointer spreading should therefore be reduced.

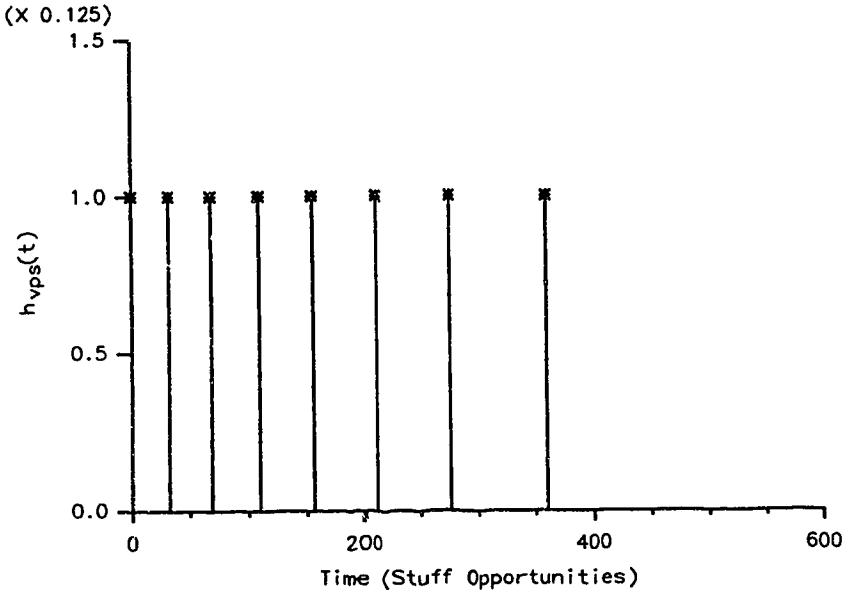

Fig. 5-3 Equivalent impulse response of variable rate pointer spreader.
f_{vps} = 1 Hz.
β = 1 VT1.5 SPE UI.
VT1.5 offset frequency = 35 Hz.

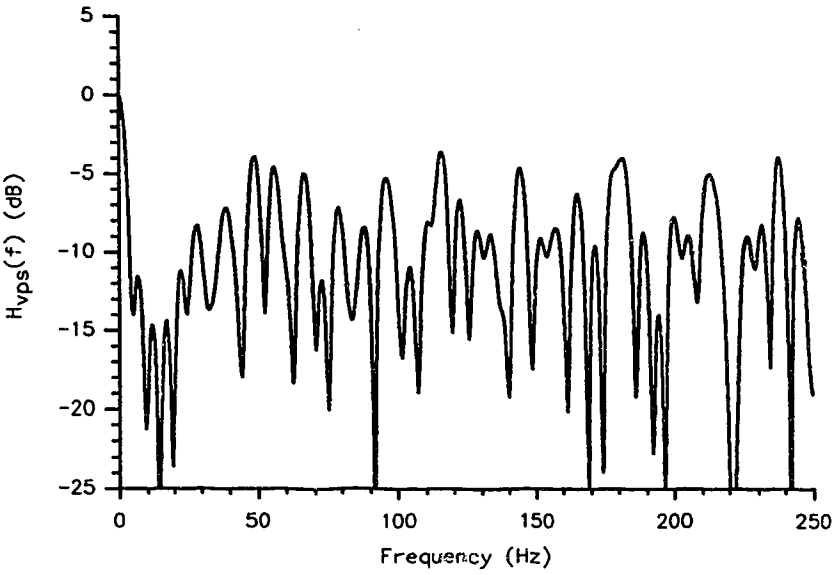

Fig. 5-4 Equivalent transfer function of variable rate pointer spreader.
f_{vps} = 1 Hz.
β = 1 VT1.5 SPE UI.
VT1.5 offset frequency = 35 Hz.

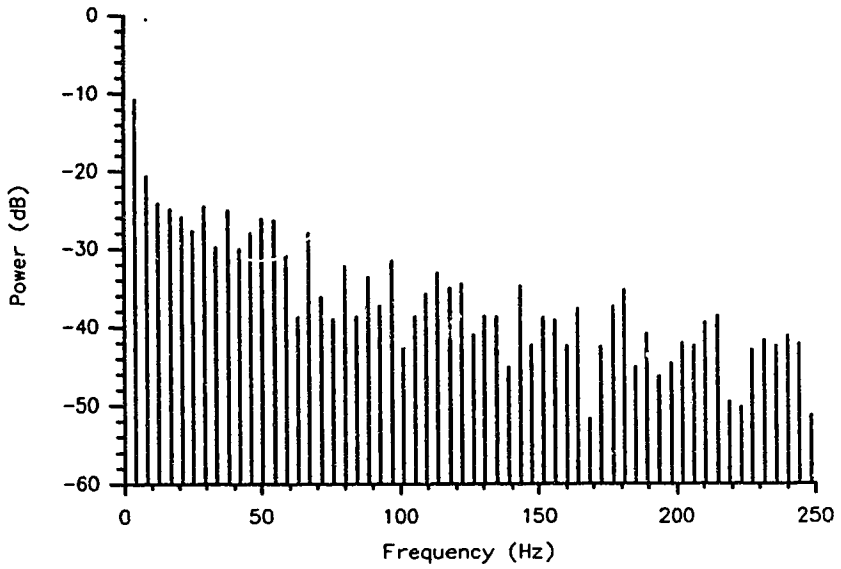

Fig. 5-5 Unfiltered power spectral density with variable rate pointer spreading.
f_{vps} = 1 Hz.
β = 1 VT1.5 SPE UI.
VT1.5 offset frequency = 35 Hz.

A possible improvement to the variable rate pointer spreader described above is to decrease the magnitude of the fractional phase steps while keeping the cutoff frequency the same. Fig. 5-6 shows the equivalent impulse response of a variable rate pointer spreader with f_{vps} equal to 1 Hz, β equal to 1/2 VT1.5 SPE UI, and a VT1.5 offset frequency of 35 Hz. As expected, the leak rate just after the pointer adjustment is the quickest and the entire pointer adjustment is leaked out in the required 475 stuff opportunities. The equivalent frequency domain transfer function for this case is shown in Fig. 5-7. The effect of decreasing the magnitude of the fractional phase steps was to increase the attenuation at low frequencies and to widen the bandwidth of maximum attenuation. The region of maximum attenuation now lies between approximately 5 and 40 Hz and the attenuation at higher frequencies has been increased to more than 6 dB. Fig. 5-8 is a plot of the

unfiltered power spectral density for this example. As expected, the magnitude of the power spectral density at the frequencies that will be passed by the 25 Hz PLL and the jitter measuring equipment has been reduced and therefore the rms jitter is expected to be reduced.

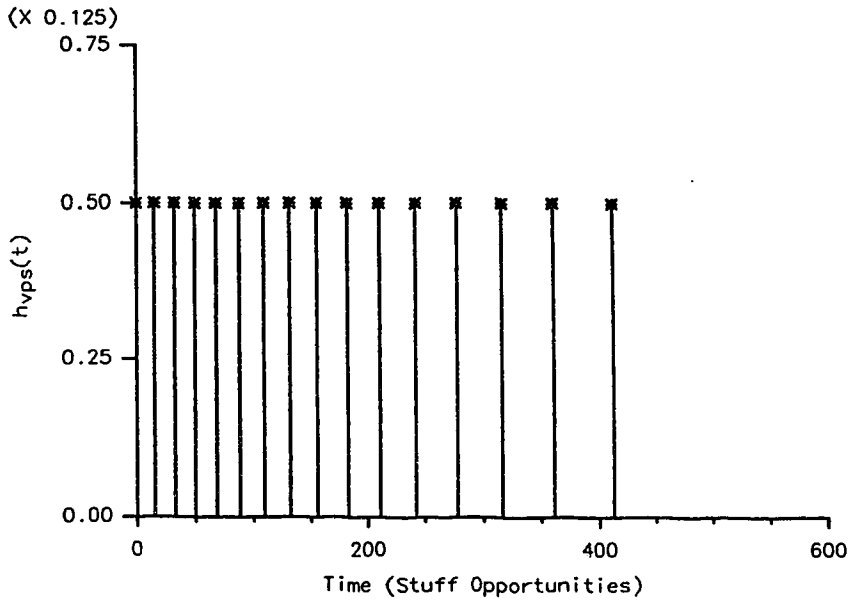

Fig. 5-6 Equivalent impulse response of variable rate pointer spreader.
f_{vps} = 1 Hz.
β = 1/2 VT1.5 SPE UI.
VT1.5 offset frequency = 35 Hz.

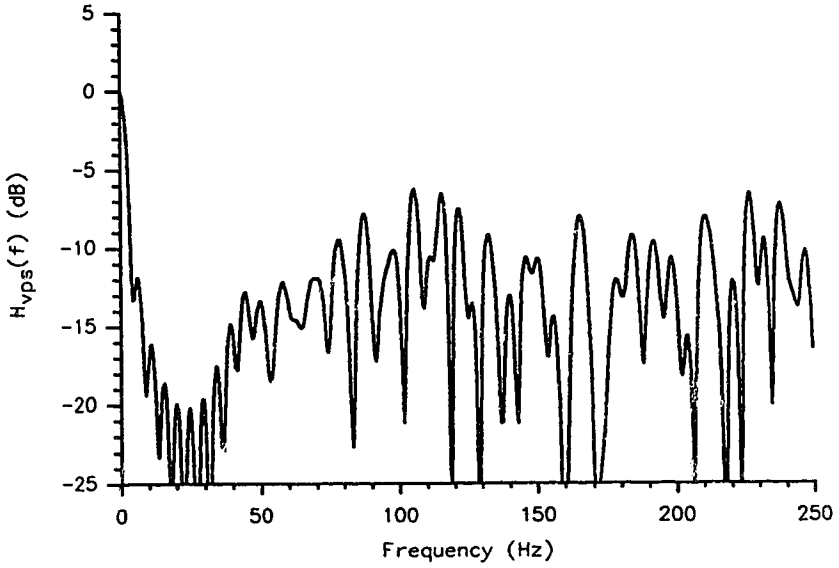

Fig. 5-7 Equivalent transfer function of variable rate pointer spreader.
f_{vps} = 1 Hz.
β = 1/2 VT1.5 SPE UI.
VT1.5 offset frequency = 35 Hz.

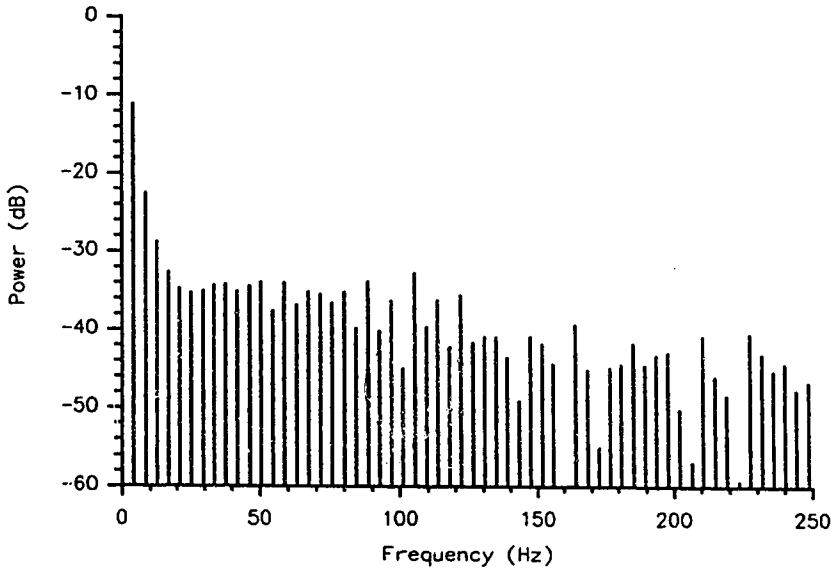

Fig. 5-8 Unfiltered power spectral density with variable rate pointer spreading.
f_{vps} = 1 Hz.
β = 1/2 VT1.5 SPE UI.
VT1.5 offset frequency = 35 Hz.

The rms jitter for a variable rate pointer spreader was calculated from theory for a system operating in degraded synchronization mode with a maximum VT1.5 offset frequency of ±35 Hz. The value of f_{vps} was chosen as 0.5 Hz. This value was chosen because it is well below the passband of the 10 Hz jitter measuring equipment and it is possible to implement a variable rate pointer spreader with this cutoff frequency [21]. The rms jitter versus VT1.5 offset frequency for this case with various values of β are shown in Fig. 5-9. The optimum choice for β with this system would appear to be 1/4 VT1.5 SPE UI. For this value of β the maximum value of rms jitter is approximately 0.1 DS-1 UI. The decrease in rms jitter that is obtained by further decreasing β is not significant. The results obtained for rms jitter suggest that a system utilizing variable rate

pointer spreading would be able to meet the CCITT recommendations for maximum rms jitter generation of 0.3 DS-1 UI.

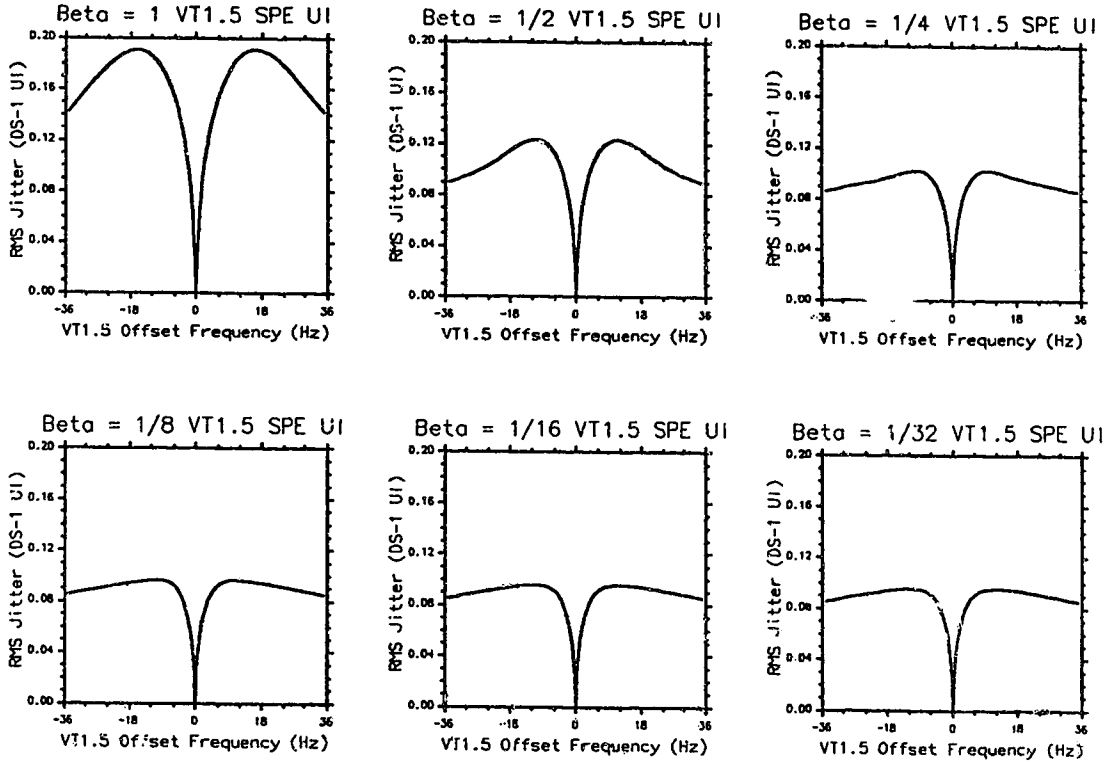

Fig. 5-9 Theoretical rms jitter versus VT1.5 offset frequency with variable rate pointer spreading.
f_{vps} = 0.5 Hz.

iii. Simulation Results

Simulations were done for both degraded and non-degraded synchronization modes of operation and are compared to the theoretical results obtained abcve. Non-degraded synchronization mode was studied with a variable rate pointer spreader with different cutoff frequencies and magnitudes of fractional phase steps during a single positive pointer adjustment. For these simulations, transient durations were set to 1.0 seconds and sampling durations were set to the inverse of the variable rate pointer spreaders cutoff frequency.

This sampling duration corresponds to over six time constants of the variable rate pointer spreader. Degraded synchronization mode was studied for a variable rate pointer spreader with a cutoff frequency of 0.5 Hz. Transient durations for these simulations were set to 2.0 seconds and sampling durations were 40.0 seconds.

Non-Degraded Synchronization Mode

Simulations were done to calculate the peak to peak jitter when a single pointer adjustment occurs for various cutoff frequencies and fractional phase steps. For a positive pointer adjustment, the initial pointer values chosen were 0, 24, and 25 in order to study the effect of the three different magnitudes of phase steps caused by a pointer adjustment. Fig. 5-10 shows the peak to peak jitter versus the cutoff frequency of the variable rate pointer spreader. The initial pointer value for this simulation was 0. As expected the maximum value of peak to peak jitter for large cutoff frequencies is 4.11 DS-1 UI and as the cutoff

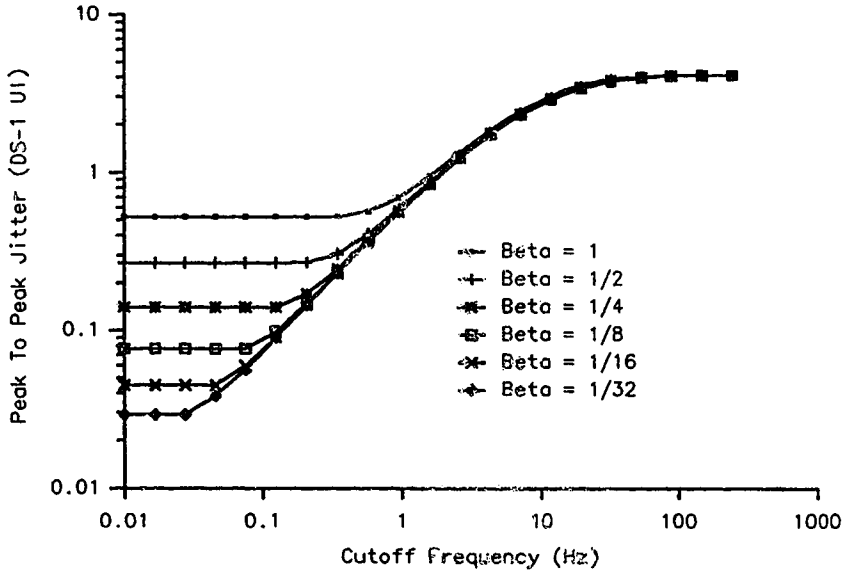

Fig. 5-10 Peak to peak jitter with a single positive pointer adjustment and an initial pointer value of 0.

frequency is decreased the peak to peak jitter levels decrease. The minimum jitter that can be obtained is dependent on β as expected from theory.

Fig. 5-11 shows the peak to peak jitter versus the cutoff frequency of the variable rate pointer spreader when the initial value of the pointer is 25. Results for an initial pointer value of 24 are virtually identical and therefore they are not plotted. For these initial pointer values, the minimum jitter that can be obtained with very low cutoff frequencies of the variable rate pointer spreader is higher than with an initial pointer value of 0. This is caused by the significant error between the actual phase step caused by a pointer adjustment and the assumed 8.0 VT1.5 SPE UI phase step. The results shown in Figs. 5-10 and 5-11 suggest that the best choice for β based on the minimum peak to peak jitter levels is 1/4 VT1.5 SPE UI. For a variable rate pointer spreader with a cutoff frequency of 0.5 Hz, the peak to peak jitter caused by a single pointer adjustment should be less than 0.6 DS-1 UI when the fractional phase step magnitude is 1 VT1.5 SPE UI. This clearly meets the CCITT jitter generation recommendations.

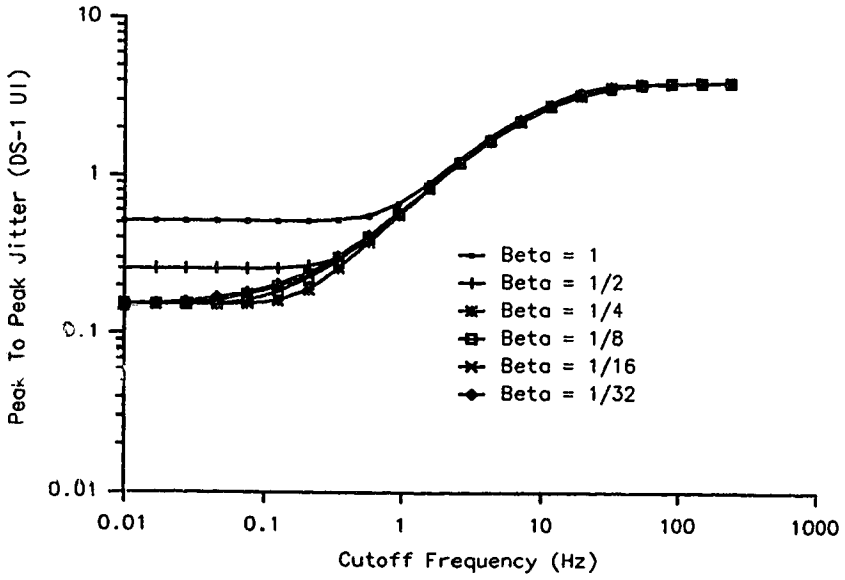

Fig. 5-11 Peak to peak jitter with a single positive pointer adjustment and an initial pointer value of 25.

Degraded Synchronization Mode

Simulations of the system operating in degraded synchronization mode were also performed with the cutoff frequency of the variable rate pointer spreader set to 0.5 Hz. The rms and peak to peak jitter results of these simulations for various values of β are shown in Figs. 5-12 and 5-13 respectively. As expected from theory, the best choice for the fractional phase step magnitude is 1/4 VT1.5 SPE UI based on the results of rms jitter. Results for peak to peak jitter also support this claim. Jitter results for values of β less than 1/4 VT1.5 SPE UI are not significantly less than for β equal to 1/4 VT1.5 SPE UI. For the system with β equal to 1/4 VT1.5 SPE UI the maximum peak to peak jitter level is less than 0.45 DS-1 UI and the maximum rms jitter level is less than 0.10 DS-1 UI. This system meets the CCITT recommendations for maximum jitter generation.

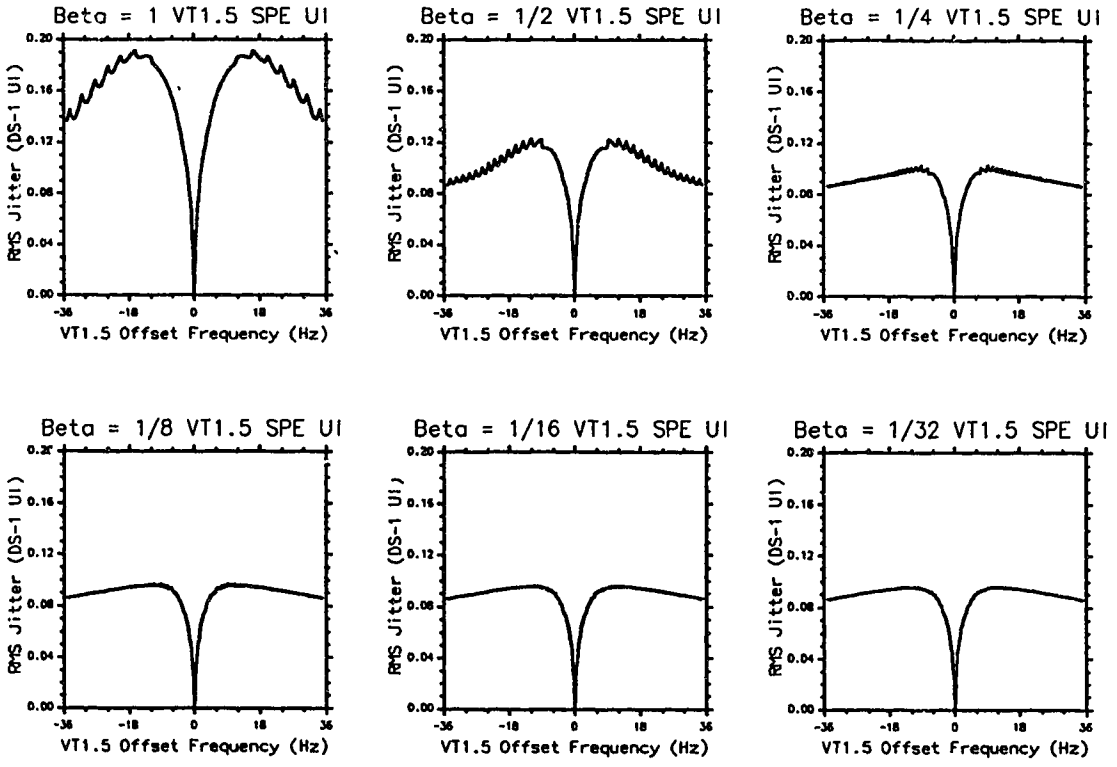

Fig. 5-12 Rms jitter with variable rate pointer spreader.
f_{vps} = 0.5 Hz.

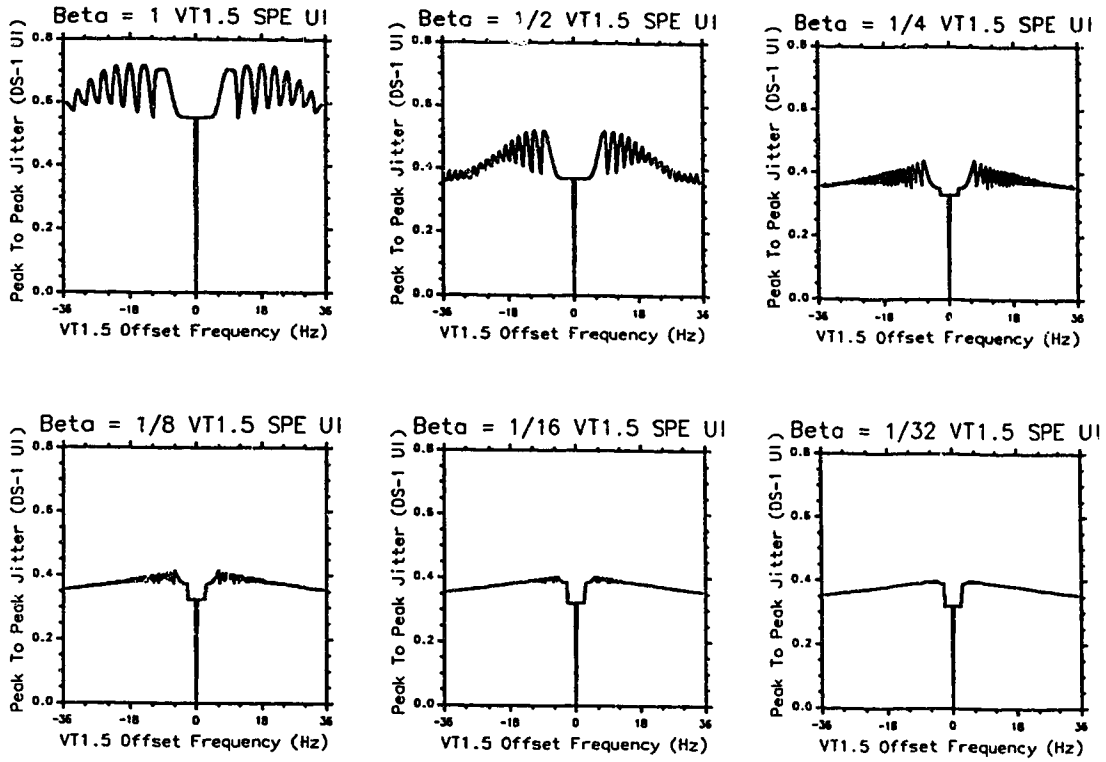

Fig. 5-13 Peak to peak jitter with variable rate pointer spreader. f_{vps} = 0.5 Hz.

Comparison to Theory

Minimum values of peak to peak jitter as a function of the fractional phase step magnitudes were taken from the simulation results plotted in Fig. 5-10. The relative error between these results and the theoretical ones shown in Table 5-1 ranged from a minimum of 2% when the fractional phase step magnitude was 1 VT1.5 SPE UI to a maximum of 45% when the fractional phase step magnitude was 1/32 VT1.5 SPE UI. The minimum values of jitter that were obtained by simulation are higher than the minimum values expected from theory. These errors are identical to those for the case with fixed rate pointer spreading and they can explained in the same way. A positive pointer adjustment for an initial pointer value of 0 produces a phase hit of 8.023 VT1.5 SPE UI instead of the assumed 8.0

VT1.5 SPE UI and therefore there is an additional 0.023 VT1.5 SPE UI phase step when a pointer adjustment occurs. For degraded mode, the results of the rms jitter versus VT1.5 offset frequency obtained from simulation and from theory are in close agreement. The average absolute error between simulation and theoretical results for all values of β is less than 3.5%.

iv. Implementation Considerations

The system described and analyzed in this Chapter has the same advantage of very simple synchronizers and desynchronizers as the system without jitter reduction techniques and the one with fixed rate pointer spreading. The variable rate pointer spreader is more complicated than the fixed rate pointer spreader, but the increase in complexity may be justified by the improved jitter performance that can be obtained. During non-degraded synchronization mode without pointer adjustments, the variable rate pointer spreader will not effect the waiting time jitter waveform, and therefore the jitter performance versus DS-1 offset frequency will be the same as for the system without jitter reduction techniques. During pointer adjustments, it has been shown that the system meets the CCITT specifications for maximum jitter generation.

v. Summary

In this Chapter it has been shown that the jitter resulting from pointer adjustments, when variable rate pointer spreading is used, meets the CCITT recommendations for jitter generation when the cutoff frequency of the variable rate pointer spreader is 0.5 Hz. This system will work with a maximum VT1.5 offset frequency of ±35 Hz and will have maximum peak to peak and rms jitter levels of 0.45 DS-1 UI and 0.10 DS-1 UI respectively. Another important result obtained by this analysis is that the best value for the magnitude of the fractional phase steps that are leaked out is 1/4 VT1.5 SPE UI when the cutoff frequency of

the variable rate pointer spreader is 0.5 Hz. A further decrease of the fractional phase step magnitude does not significantly improve the jitter performance.

VI. STUFF THRESHOLD MODULATION

In this Chapter waiting time jitter is estimated when stuff threshold modulation (STM) [13-15] is used in the VT1.5 SPE to VT1.5 synchronizer. Results obtained are compared to those obtained when no methods are used to control jitter and when pointer spreading techniques are used. The system with stuff threshold modulation is first described and then theoretically analyzed while in degraded synchronization mode. Simulation results are then discussed along with implementation considerations of the system.

i. Description

The system analyzed in this Chapter uses a different approach to reduce jitter caused by pointer adjustments. Pointer spreading methods concentrated on desynchronizer design in order to reduce jitter whereas STM concentrates on the synchronizer. The system analyzed in this Chapter uses double sided stuff threshold at the synchronizer in order to alter the waiting time jitter waveform by changing the stuffing pattern [13-15]. The desynchronizer used in this system does not use any methods to reduce jitter other than the usual 25 Hz PLL and 10 Hz jitter measuring equipment. A block diagram of the system is shown in Fig. 6-1. After the DS-1 is synchronized to and mapped into the VT1.5 SPE, the VT1.5 SPE is then synchronized to the VT1.5 using double sided STM. This synchronizer is a plus/zero/minus synchronizer which has both a positive and negative threshold that are always 8.0 VT1.5 SPE UI apart. These thresholds are varied frame by frame to produce a pattern called a threshold waveform, defined by specifying the negative threshold versus time. After synchronization and transmission the received VT1.5 is demapped and the DS-1 is removed and

passed through a 25 Hz PLL. Jitter is then measured using a first order 10 Hz high pass filter.

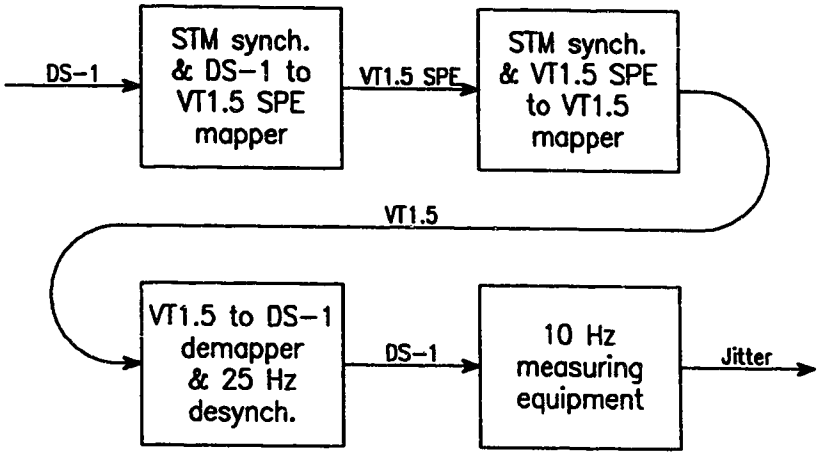

Fig. 6-1 System block diagram with stuff threshold modulation.

The system utilizing STM will have its performance during non-degraded synchronization mode altered as compared to the system using a simple plus/zero/minus synchronizer. Pointer adjustment occur very infrequently during non-degraded synchronization mode when STM is not used at the synchronizer. However with STM, pointer adjustments always occur frequently even during non-degraded synchronization mode. Hence there is no equivalent of a single isolated pointer adjustment during non-degraded synchronization mode. Non-degraded synchronization mode is analyzed by plotting the peak to peak and rms jitter versus DS-1 offset frequency when the VT1.5 offset frequency is 0 Hz. Degraded synchronization mode is analyzed in the usual way; peak to peak and rms jitter versus VT1.5 offset frequency with the DS-1 offset frequency set to 0 Hz.

In the STM synchronizer implemented in this analysis the positive and negative thresholds are separated by 8.0 VT1.5 SPE UI and the threshold

waveform has a period of N stuff opportunity frames with N different threshold levels, denoted as $T_0, T_1, \ldots, T_{N-1}$, which are allowed to take on values in the range of [0,8). The system analyzed in this Chapter uses a type of stuff threshold waveform referred to as a modified waveform [15]. For this waveform, the period is equal to a power of 2 and the values of T_n can be described by the equation

$$T_n = \frac{8BRO(n)}{N} \qquad (6\text{-}1)$$

where BRO(n) denotes the bit-reversed order of n [26]. The bit-reversal process involves first converting the values of n to their binary representation. These binary bit sequences are then reversed and converted into decimal values. Three different STM waveforms are studied which have periods of 8, 16, and 32 VT1.5 frames.

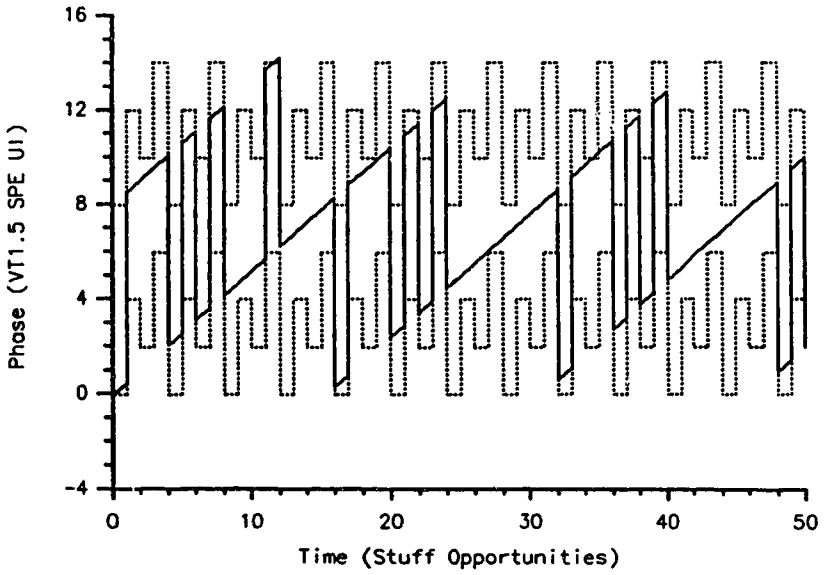

Fig. 6-2 Waiting time jitter waveform with four level modified stuff threshold modulation.

ii. Theoretical Analysis

Degraded Synchronization Mode

The system with STM can be studied while in degraded synchronization mode using Fourier analysis. An example of the time domain waiting time jitter waveform when STM is used at the synchronizer is shown in Fig. 6-2. For this example, four level STM is used which has threshold levels of 0, 4, 2, 6 as calculated using Eqn. 6-1. The positive and negative stuff thresholds are represented by the dotted lines, the positive threshold being the higher of the two. The waiting time jitter waveform is represented by the solid line.

For analytical purposes, introducing STM in conventional synchronizers may be considered analogous to adding input jitter consisting of the threshold waveform to the write clock. Applying this notion to Duttweiler's time domain equation for the waiting time jitter waveform including input jitter [8],

$$\phi_{stm}(t) = 8\left(\rho t - \left[\rho[t] - \frac{1}{8}T_{[t] \bmod N}\right]\right), \qquad (6\text{-}2)$$

where $[x]$ denotes the greatest integer equal to or less than x, and time is normalized to the stuff opportunity period $1/f_m$. Eqn. 6-2 reduces to the simple form of Eqn. 3-7 for a constant threshold. In order to calculate the Fourier transform of $\phi_{stm}(t)$, an auxiliary function $\mu(x)$ is first defined as

$$\mu(x) = x - [x], \qquad (6\text{-}3)$$

and Eqn. 6-2 is rewritten as

$$\phi_{stm}(t) = 8\phi_{stm1}(t) + 8\phi_{stm2}(t) + 8\phi_{stm3}(t), \qquad (6\text{-}4)$$

where

$$\phi_{stm1}(t) = \rho\mu(t), \qquad (6\text{-}5)$$

$$\phi_{stm2}(t) = \mu\left(\rho[t] - \frac{1}{8}T_{[t]\bmod N}\right), \tag{6-6}$$

$$\phi_{stm3}(t) = \frac{1}{8}T_{[t]\bmod N}. \tag{6-7}$$

Eqn. 6-5 represents a simple sawtooth waveform with period one and amplitude ρ, the Fourier transform of which is (see Appendix E)

$$\Phi_{stm1}(f) = \frac{\rho}{2}\delta(f) + \sum_{k=1}^{\infty}\frac{j\rho}{2\pi k}\left(\delta(f-k) - \delta(f+k)\right). \tag{6-8}$$

The Fourier transform of $\phi_{stm2}(t)$ may be calculated by first presenting it as (see Appendix E)

$$\phi_{stm2}(t) = \left[U(t) - U(t-1)\right] * \sum_{n=0}^{N-1}\left(\mu(\rho t - \frac{1}{8}T_n)\cdot\sum_{m=-\infty}^{\infty}\delta(t-n-mN)\right), \tag{6-9}$$

where U(t) is a unit step. The Fourier transform of Eqn. 6-9 is (see Appendix E)

$$\Phi_{stm2}(f) = \frac{1}{2}\delta(f) + e^{-j\pi f}\frac{\sin(\pi f)}{\pi f}\sum_{k=1}^{\infty}\sum_{m=-\infty}^{\infty}\frac{j}{2\pi k}\left(A_{k,m}\delta\left(f-\rho k-\frac{m}{N}\right) - B_{k,m}\delta\left(f+\rho k-\frac{m}{N}\right)\right), \tag{6-10}$$

where

$$A_{k,m} = \frac{1}{N}\sum_{n=0}^{N-1} e^{-j2\pi(kT_n/8 + mn/N)} \tag{6-11}$$

and

$$B_{k,m} = \frac{1}{N}\sum_{n=0}^{N-1} e^{j2\pi(kT_n/8 - mn/N)}. \tag{6-12}$$

In a similar manner the Fourier transform of $\phi_{stm3}(t)$ can be derived, and is given by (see Appendix E)

$$\Phi_{stm3}(f) = e^{-j\pi f} \frac{\sin(\pi f)}{\pi f} \sum_{m=-\infty}^{\infty} C_m \delta\left(f-\frac{m}{N}\right). \qquad (6\text{-}13)$$

where

$$C_m = \frac{1}{8N} \sum_{n=0}^{N-1} T_n e^{-j2\pi mn/N}. \qquad (6\text{-}14)$$

The complete Fourier transform of the waiting time jitter waveform including STM is therefore

$$\Phi_{stm}(f) = 8\Phi_{stm1}(f) + 8\Phi_{stm2}(f) + 8\Phi_{stm3}(f), \qquad (6\text{-}15)$$

where f is normalized to the stuff opportunity rate f_m. For a complete derivation of

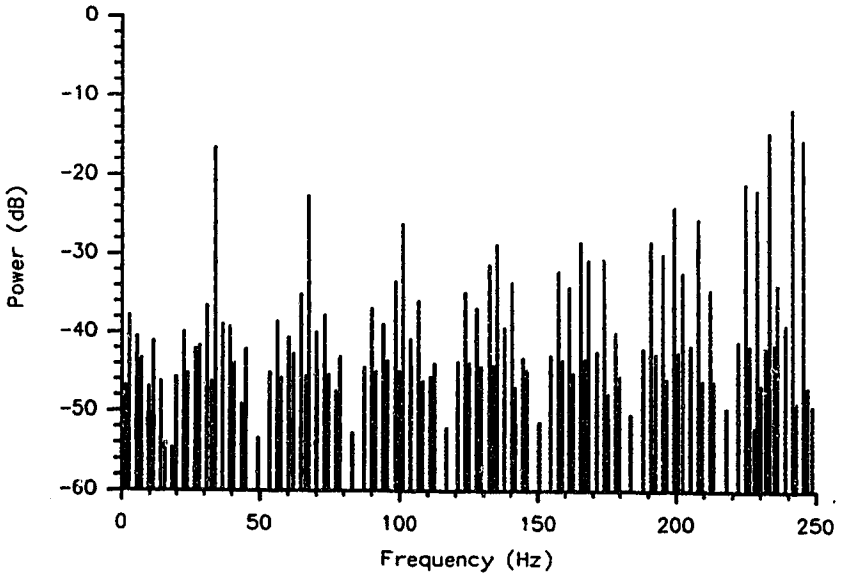

Fig. 6-3 Unfiltered power spectral density with 8 level modified stuff threshold modulation and a 35 Hz VT1.5 offset frequency.

Φ_{stm1}, Φ_{stm2}, and Φ_{stm3} see Appendix E. The Fourier transform described by Eqn. 6-15 reduces to the result given by Chow for constant thresholds. For this conventional case, N is equal to one and therefore the magnitudes of $A_{k,m}$ and $B_{k,m}$ of Eqn. 6-10 become unity and Eqn. 6-13 yields a dc term.

Fig. 6-3 shows the unfiltered power spectral density of a waiting time jitter waveform in the presence of a synchronizer utilizing 8 level modified STM. The VT1.5 offset frequency for this case was 35 Hz. This spectrum is very different than the one obtained when a plus/zero/minus synchronizer is used with fixed thresholds as shown in Fig. 3-4. More power is contained at higher frequencies in the STM case and less power is contained at lower frequencies. The largest frequency component that is within band of the PLL and jitter measuring equipment is the component at approximately 34 Hz. The rms jitter with STM is expected to be less than the rms jitter without STM because of the reduced power within band of the PLL and jitter measuring equipment.

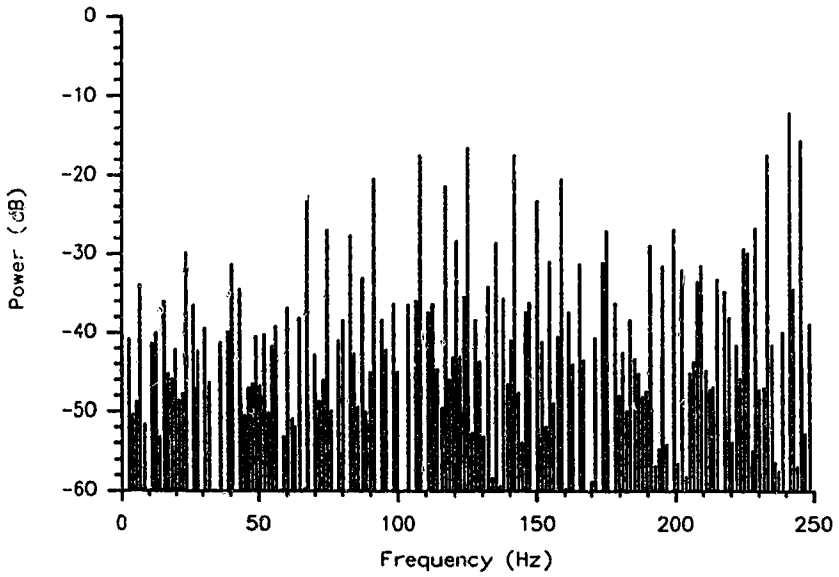

Fig. 6-4 Unfiltered power spectral density with 16 level modified stuff threshold modulation and a 35 Hz VT1.5 offset frequency.

A possible improvement to the STM synchronizer is to increase the value of N. Fig. 6-4 shows the unfiltered power spectral density of a waiting time jitter waveform in the presence of a synchronizer utilizing 16 level modified STM. Again, the VT1.5 offset frequency for this case was 35 Hz. The large component in the power spectral density at approximately 34 Hz is not present for this case. However, the number of components for this case is much larger than for 8 level STM. Hence, it is not obvious from the power spectral densities which level will produce lower rms jitter.

Fig. 6-5 shows the theoretical rms jitter versus the VT1.5 offset frequency during degraded mode. Eqn. 6-10 was calculated for the first 125 values of k with values of m chosen so that the frequency components calculated were within the band of 0 to 1 cycle per stuffing opportunity. From Fig. 6-5, altering the value of N

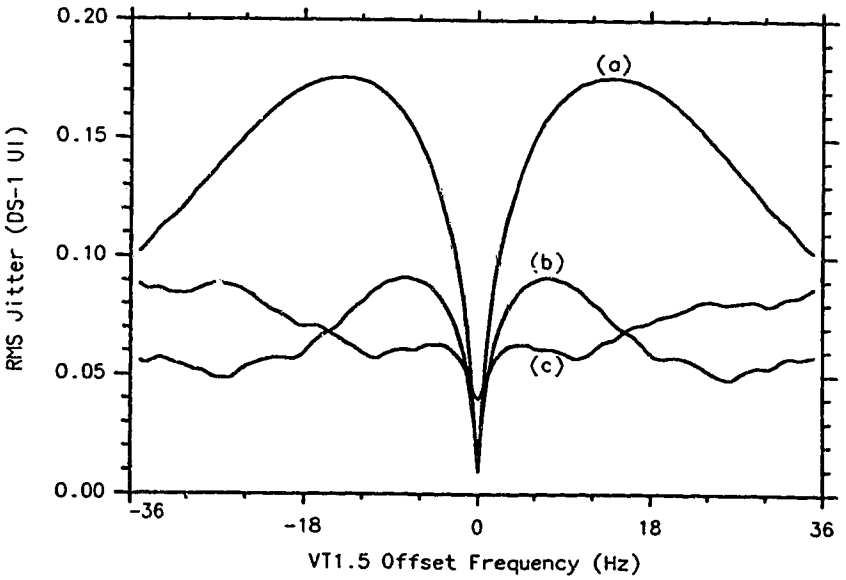

Fig. 6-5 Theoretical rms jitter versus VT1.5 offset frequency.
(a) 8 level STM.
(b) 16 level STM.
(c) 32 level STM.

changes both the level of the rms jitter and the shape of the rms jitter versus VT1.5 offset frequency curve. This non-linear interaction of N on the rms jitter was not seen for either fixed rate or variable rate pointer spreading. The rms jitter with STM employed at the synchronizer can be reduced below 0.1 DS-1 UI when the value of N is set to either 16 or 32.

iii. Simulation Results

Simulations were done for both degraded and non-degraded synchronization modes of operation. Results obtained for the rms jitter during degraded synchronization mode are compared with the theoretical results obtained above. Transient durations of 1.0 second were used in all of the simulations to allow the PLL and high pass filters to reach steady state conditions. Sampling durations were 1.0 second for the simulations of non-degraded synchronization mode and 10.0 seconds for the simulations of degraded synchronization mode. Non-degraded synchronization mode is not studied in the usual way because there is no equivalent of a single isolated pointer adjustment when STM is used at the synchronizer. Therefore, non-degraded synchronization mode was examined by simulating the jitter versus DS-1 offset for a 0 Hz VT1.5 offset. For these simulations the initial phase in the VT1.5 SPE to VT1.5 synchronizer was set halfway between the lowest threshold level and the second lowest threshold level. This was done to ensure that the synchronizer would force positive and negative pointer adjustments during the simulation. Results of these simulations are then compared to the case without STM which is shown in Fig. 3-6.

Non-Degraded Synchronization Mode

Simulation results for the rms jitter versus DS-1 offset in the presence of STM are shown in Fig. 6-6. Simulation results were not as sensitive to the initial

pointer value as those for the case without STM. Results are therefore only plotted in Fig. 6-6 for an initial pointer value of 0. From the results of Fig. 6-6, the frequent pointer adjustments in the presence of STM cause an increase in the amount of rms jitter that occurs during non-degraded synchronization mode as compared to the results for the case without STM shown in Fig. 3-6. As the value of N increases, the rms jitter increases and the rms jitter versus DS-1 offset frequency curve flattens out. The rms jitter as seen in Fig. 6-6 still meets the CCITT recommendations for jitter generation. The maximum values of rms jitter for N of 8, 16, and 32 are less than 0.065, 0.069, and 0.082 DS-1 UI respectively.

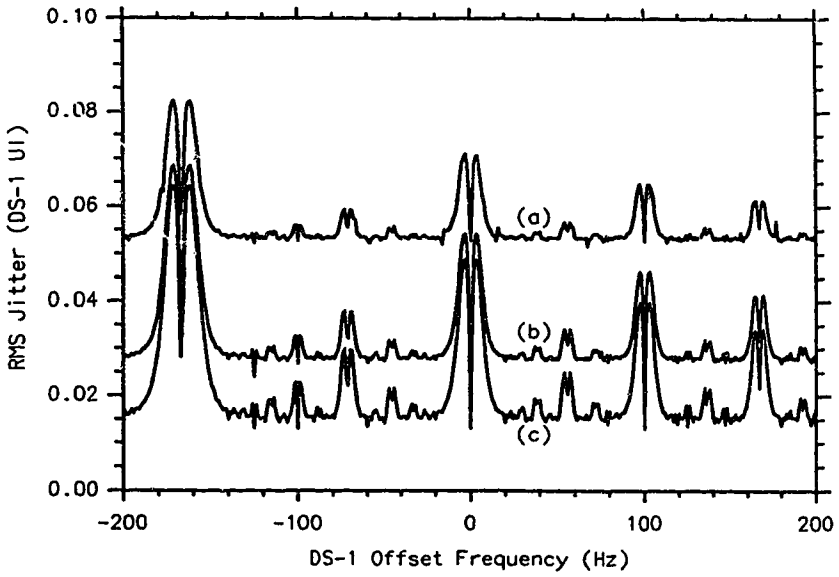

Fig. 6-6 Rms jitter during non-degraded synchronization mode with STM synchronizer.
(a) 32 level STM.
(b) 16 level STM.
(c) 8 level STM.

Fig. 6-7 shows the simulation results for the peak to peak jitter versus DS-1 offset during non-degraded synchronization mode. Again, the effect of the initial pointer value on the peak to peak jitter results is very small and therefore Fig. 6-7

only displays the results for an initial pointer value of 0. The frequent pointer adjustments in the presence of STM cause an increase in the amount of peak to peak jitter that occurs during non-degraded synchronization mode as compared to the case without STM. As N is increased, the peak to peak jitter increases, however the peak to peak jitter for all the values of N shown in Fig. 6-7 still meets the CCITT recommendations for peak to peak jitter generation. The peak to peak jitter for N of 8, 16, and 32 is less than 0.23, 0.27, and 0.35 DS-1 UI respectively.

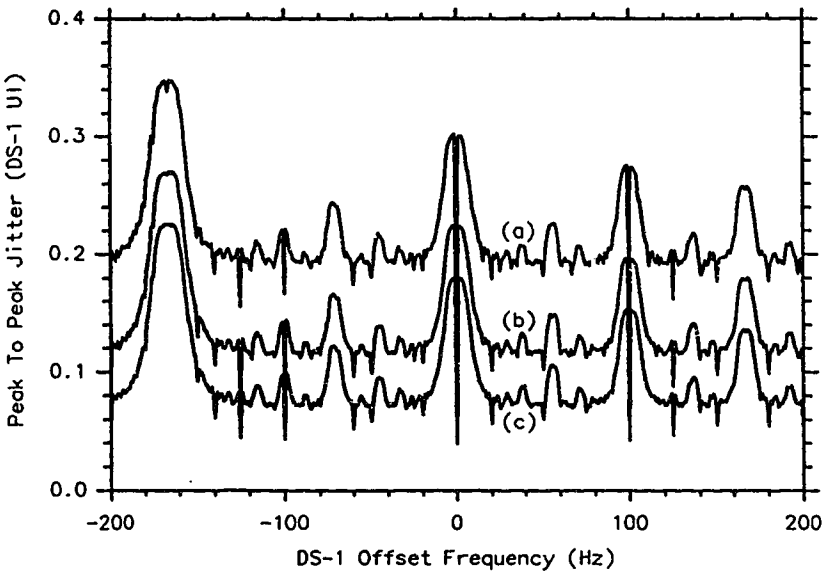

Fig. 6-7 Peak to peak jitter during non-degraded synchronization mode with STM synchronizer.
(a) 32 level STM.
(b) 16 level STM.
(c) 8 level STM.

Degraded Synchronization Mode

Simulation results for the rms jitter versus VT1.5 offset frequency during degraded synchronization mode are presented in Fig. 6-8. For the simulations in degraded synchronization mode, the initial pointer value was set to 12. For small

VT1.5 offset frequencies, the rms jitter decreases as N increases, and the best value for N is therefore 32. For large VT1.5 offset frequencies, the rms jitter is lowest for N equal to 16. Over the entire range of VT1.5 offset frequencies, the rms jitter is below 0.18, 0.093, and 0.091 for N of 8, 16, and 32 respectively. Based on this maximum rms jitter performance, the best value of N is 32. However, when N is changed from 16 to 32, there is only a marginal improvement in rms jitter performance.

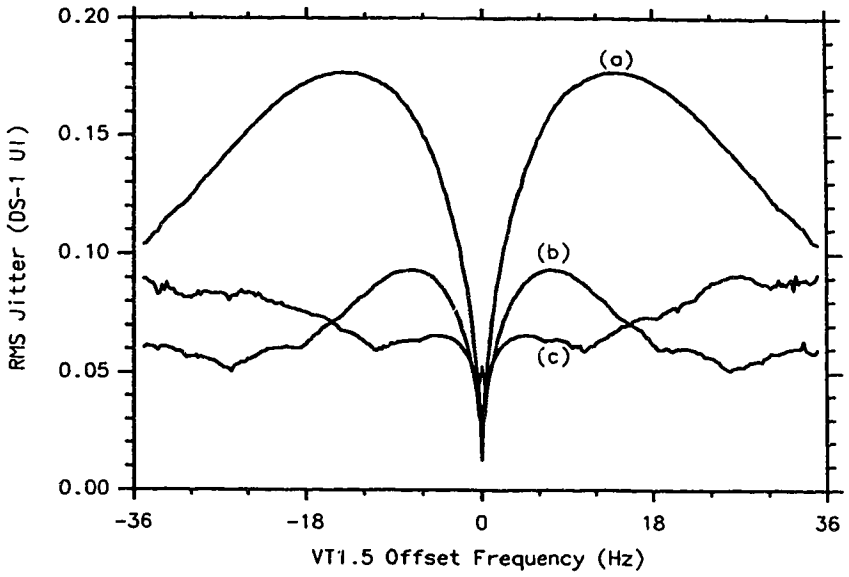

Fig. 6-8 Rms jitter during degraded synchronization mode with STM synchronizer.
(a) 8 level STM.
(b) 16 level STM.
(c) 32 level STM.

The peak to peak jitter versus VT1.5 offset frequency during degraded synchronization mode is shown in Fig. 6-9. For small VT1.5 offset frequencies, the peak to peak jitter decreases as the value of N increases with the largest decrease in peak to peak jitter occurring when N is increased from 8 to 16. The decrease in peak to peak jitter for small VT1.5 offset frequencies when N is

increased from 16 to 32 is not as dramatic. For large VT1.5 offset frequencies, the peak to peak jitter is lowest for N equal to 16. When N is increased to 32, the jitter increases. In the entire VT1.5 offset frequency range of ±35 Hz, the peak to peak jitter is below 0.573, 0.373, and 0.548 for values of N of 8, 16, and 32 respectively. Because the worst case rms jitter performance for N equal to 16 and 32 are comparable, the best value of N is 16 based on jitter performance.

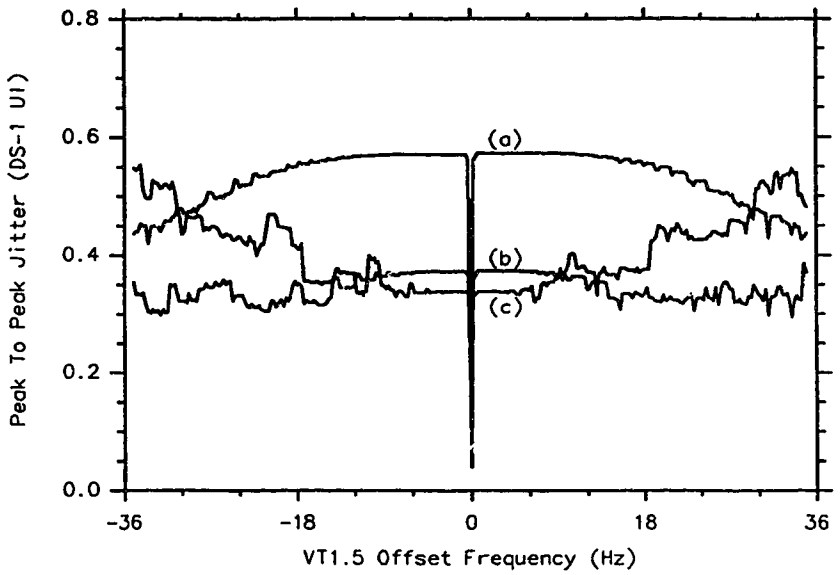

Fig. 6-9 Peak to peak jitter during degraded synchronization mode with STM synchronizer.
(a) 8 level STM.
(b) 16 level STM.
(c) 32 level STM.

Comparison to Theory

For degraded mode, the results of the rms jitter versus VT1.5 offset frequency obtained from simulation results and from theory are in close agreement. The average absolute error between simulation and theoretical results for all values of N is less than 5%.

iv. Implementation Considerations

The system utilizing STM which was analyzed in this Chapter has a slightly more complex VT1.5 SPE to VT1.5 synchronizer than the system utilizing fixed rate and variable rate pointer spreading which had a simple plus/zero/minus synchronizer. The advantage of the system which uses STM is in the simplicity of the desynchronizer. A very simple desynchronizing PLL is the only device necessary to ensure adequate jitter performance. Because there is no need for pointer spreading, the complexity of the desynchronizer is reduced. In the systems described in previous Chapters, non-degraded synchronization mode was not influenced by the pointer spreading desynchronizers when no pointer adjustments were occurring. This was because the waiting time jitter waveform was altered by the pointer spreader only when pointer adjustments were occurring. The synchronizer which was analyzed in this Chapter always causes frequent pointer adjustments even during non-degraded synchronization mode. The jitter performance during non-degraded synchronization mode is therefore impaired.

The STM synchronizer as analyzed in this Chapter can cause pointer adjustments to occur at a maximum frequency of once per VT1.5 frame. The current SONET standard allows for a maximum stuffing frequency of once per four VT1.5 frames [1]. There are two possibilities for the STM system meeting the SONET standard. The first obvious one is to change the SONET standard to allow a maximum of one pointer adjustment per VT1.5 frame. The second alternative would be to use every fourth stuffing opportunity in the STM synchronizer. This would effectively lower the stuffing opportunity frame rate and therefore the frequency of the components in the waiting time jitter spectrum would be reduced. In order to maintain reasonable performance of the system,

the PLL bandwidth would need to be reduced. This second alternative is more reasonable because it does not involve changes to the standard.

v. Summary

In this Chapter it has been shown that the jitter resulting from pointer adjustments when stuff threshold modulation is used in the VT1.5 SPE to VT1.5 synchronizer meets the CCITT recommendations for jitter generation. A system can be designed that will work with a maximum VT1.5 offset frequency of ±35 Hz and will have a maximum peak to peak and rms jitter levels of 0.37 DS-1 UI and 0.093 DS-1 UI respectively. An important result obtained by this analysis is that stuff threshold modulation is a valid method for reducing waiting time jitter caused by SONET pointer adjustments.

VII. FEED FORWARD POINTER SPREADING

In this Chapter waiting time jitter is estimated when feed forward pointer spreading is used to reduce waiting time jitter caused by pointer adjustments. Results obtained are compared to those obtained when other reduction techniques are used. The system with feed forward pointer spreading is first described and then theoretically analyzed while in degraded synchronization mode. Simulation results are then discussed along with implementation considerations of the system.

I. Description

The system analyzed in this Chapter utilizes both synchronizer and desynchronizer design in order to reduce jitter caused by SONET pointer adjustments. The phase difference in the VT1.5 SPE to VT1.5 elastic store is continuously transmitted to the desynchronizer along with the VT1.5. This information is then used to leak out fractional phase steps at the pointer spreading elastic store at the same rate as the phase is accumulating in the synchronizer. When a pointer adjustment finally occurs at the synchronizer, most of the phase step caused will have already been leaked out at the pointer spreader. The system analyzed in this Chapter uses stuff threshold modulation as a method of transmitting the synchronizer elastic store information. The stuffing pattern is dependent on the average phase in the synchronizer elastic store and therefore the pointer spreading logic can analyze this stuffing pattern to determine the synchronizer elastic store phase. The required amount of phase can then be leaked out. After the pointer spreader is used to smooth out the pointer adjustments, the usual 25 Hz PLL and 10 Hz jitter measuring equipment is used to smooth the DS-1 clock. A block diagram of the system is shown in Fig. 7-

1. After the DS-1 is synchronized to and mapped into the VT1.5 SPE, the VT1.5 SPE is synchronized to the VT1.5 using double sided STM. The STM in this system only uses one out of every four stuffing opportunities. This is done to ensure that any two stuff events are separated by at least four frames and thereby meet the SONET standard is adhered to. The stuff opportunity rate for this system is therefore once per 2000 μsec instead of the usual 500 μsec. After synchronization and transmission the received VT1.5 is demapped into a VT1.5 SPE which is passed through a feed forward pointer spreader. After pointer spreading, the VT1.5 SPE is demapped into a DS-1 and passed through a second order 25 Hz PLL. Jitter is then measured using a first order 10 Hz high pass filter.

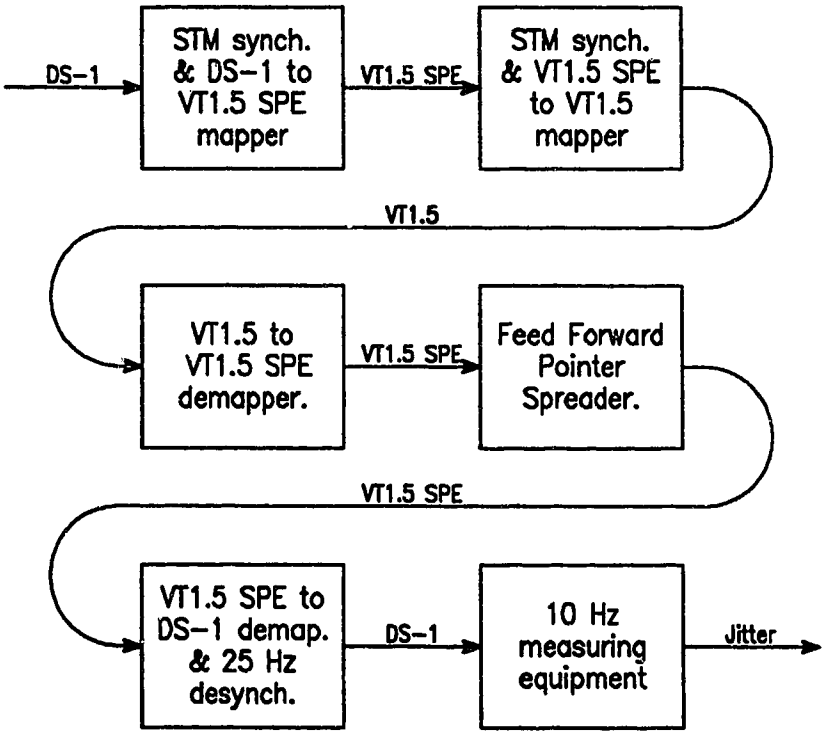

Fig. 7-1 System block diagram with feed forward pointer spreading.

A system using the feed forward pointer spreader described in this Chapter will have its performance affected during non-degraded synchronization mode because of the frequency of pointer adjustments. Because STM is used at the synchronizer, pointer adjustments will occur frequently even during non-degraded synchronization mode. Non-degraded synchronization mode is therefore analyzed by plotting the peak to peak and rms jitter versus DS-1 offset frequency when the VT1.5 offset frequency is 0 Hz. Degraded synchronization mode is analyzed in the usual way; peak to peak and rms jitter versus VT1.5 offset frequency with the DS-1 offset frequency set to 0 Hz.

The STM synchronizer is similar to the one used in the previous Chapter. The positive and negative thresholds are separated by 8.0 VT1.5 SPE UI and the threshold waveform has a period of N stuff opportunities with N different threshold levels, denoted as $T_0, T_1, \ldots, T_{N-1}$, which are allowed to take on values in the range of [0,3). The system analyzed in this Chapter uses a modified waveform [15] which has a period equal to a power of 2 and the values of T_n can be described by Eqn. 6-1. Three different waveforms are studied which have periods of 4, 8, and 16 stuff opportunities.

The pointer spreading logic can be designed to observe the stuffing pattern and leak out the required amount of phase. Immediately after a negative pointer adjustment the waiting time jitter waveform will be increased. This can be referred to as state 1. Similarly, immediately after a positive pointer adjustment, the waiting time jitter waveform will be decreased. This can be referred to as state 2. These two states can be seen in Fig. 7-2 on the dotted line waveform. To determine the amount of phase that must be leaked out the fraction of times that the system is in state 1 over the past N frames is multiplied by 8.0 VT1.5 SPE UI. For example if the system is in state 1 one half of the time, 4.0 VT1.5 SPE UI is leaked out.

ii. Theoretical Analysis

Degraded Synchronization Mode

The system with feed forward pointer spreading can be analyzed while in degraded synchronization mode using Fourier analysis. An example of the time domain waiting time jitter waveform when STM is used at the synchronizer is shown by the dotted line in Fig. 7-2. For this example, four level STM is used which has threshold levels of 0, 4, 2, 6 as calculated using Eqn. 6-1. The waiting time jitter waveform as shown by the solid line was calculated by taking the running average of the dotted line over the last 4 stuff opportunities. Therefore, the feed forward pointer spreading logic can be implemented by taking the running average of the VT1.5 SPE phase over the last N stuff opportunities when STM is used at the synchronizer. The resulting pointer spreading circuit is called a running average pointer spreader. For feed forward pointer spreading

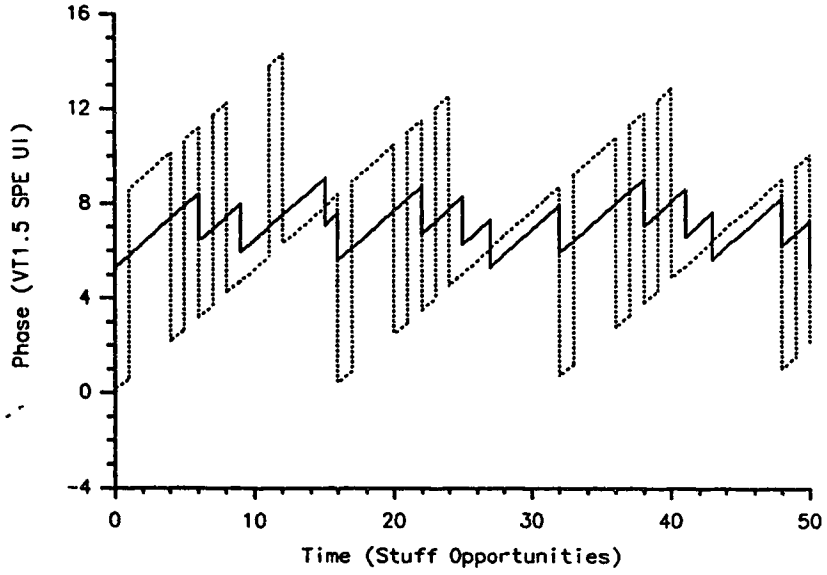

Fig. 7-2 Waiting time jitter waveform with feed forward pointer spreading.

implemented in this way the fractional phase steps have a magnitude of 8/N VT1.5 SPE UI. Therefore, for the example shown in Fig. 7-2, the fractional phase steps have a magnitude of 2 VT1.5 SPE UI.

For the system analyzed in this Chapter, the stuff opportunity rate was chosen to be once every 2000 μsec to ensure that the SONET standard is adhered to. Therefore, the stuff ratio must be recalculated using the definition

$$\rho = \frac{(f_r - f_w)}{8f_m}, \tag{7-1}$$

where f_r is the frequency of the read clock, f_w is the frequency of the write clock, and f_m is the frequency of stuff opportunities. Using the new stuff opportunity rate of 500 Hz, the stuff ratio can be recalculated in terms of the VT1.5 offset frequency as

$$\rho = \frac{(1.728E6 + \nu)(26/27) - 1.664E6}{8(500)} = \frac{13\nu}{54000} \tag{7-2}$$

where ν is the VT1.5 offset frequency in Hz.

The waiting time jitter waveform after feed forward pointer spreading will be given by

$$\phi_{ffps}(t) = \phi_{stm}(t) * h_{aps}(t), \tag{7-3}$$

where $\phi_{stm}(t)$ is the synchronizer waiting time jitter waveform utilizing STM as given by Eqn. 6-15 and $h_{aps}(t)$ is the equivalent impulse response of the running average pointer spreader. As described above, the pointer spreader takes the running average of the waiting time jitter waveform over the last N stuff opportunities and therefore $h_{aps}(t)$ can be represented as

$$h_{aps}(t) = \frac{1}{N}\sum_{n=0}^{N-1} \delta(t-n). \tag{7-4}$$

The Fourier transform of $h_{aps}(t)$ is

$$H_{aps}(f) = \frac{1}{N}\sum_{n=0}^{N-1} e^{-j2\pi fn}, \qquad (7\text{-}5)$$

and therefore, the Fourier transform of the waiting time jitter waveform with fixed rate pointer spreading is

$$\Phi_{ffps}(f) = \Phi_{stm}(f)H_{aps}(f), \qquad (7\text{-}6)$$

where f is normalized to the stuff opportunity rate f_m.

The equivalent transfer function of a running average pointer spreader when N is equal to 4 is shown in Fig. 7-3. This system is referred to as having 4 level pointer spreading. From Eqn. 7-5, this transfer function contains nulls at frequencies which are multiples of 1/N. These nulls occur at precisely the frequencies where Φ_{stm3} from Eqn. 6-13 contains its power. Therefore, the transfer function of the running average pointer spreader effectively removes all the power from the Φ_{stm3} term of Φ_{stm}. Fig. 7-4 shows the resulting unfiltered power spectral density of the waiting time jitter waveform for this case after feed forward pointer spreading with a VT1.5 offset frequency of 35 Hz. The largest frequency component that is within band of the PLL and jitter measuring equipment is the component at approximately 17 Hz. This component has a magnitude of -10.9 dB. The rms jitter with feed forward pointer spreading is expected to be less than the rms jitter without jitter reduction methods because of less power within the band of the PLL and jitter measuring equipment.

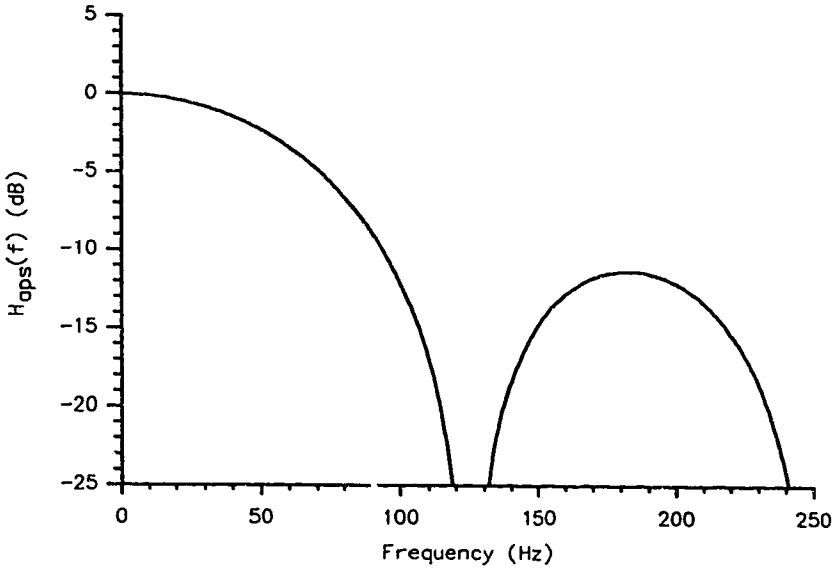

Fig. 7-3 Equivalent transfer function of 4 level running average pointer spreader.

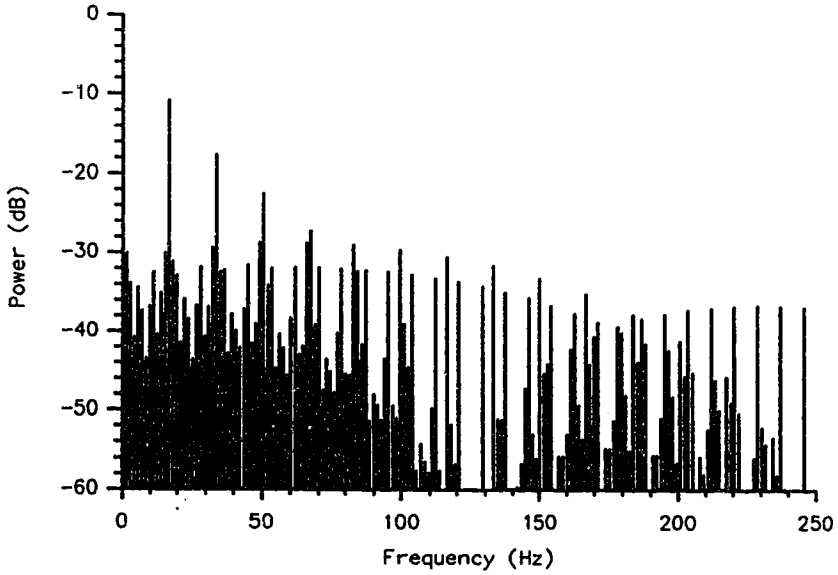

Fig. 7-4 Unfiltered power spectral density with 4 level feed forward pointer spreading and a 35 Hz VT1.5 offset frequency.

A possible improvement to the feed forward pointer spreader is to increase the value of N. Fig. 7-5 shows the equivalent transfer function of the running average pointer spreader for N equal to 8. Again nulls occurs at multiples of 1/N and the Φ_{stm3} will therefore be completely removed from the spectrum. The unfiltered power spectral density of the waiting time jitter waveform for this case with a 35 Hz VT1.5 Hz offset frequency is shown in Fig. 7-6. The largest component in the power spectral density occurs at approximately 34 Hz and has a magnitude of -21.3 dB. The magnitudes of the components in band of the 25 Hz PLL and the 10 Hz jitter measuring equipment are less than for the case of 4 level feed forward pointer spreading, and therefore the rms jitter should be further reduced.

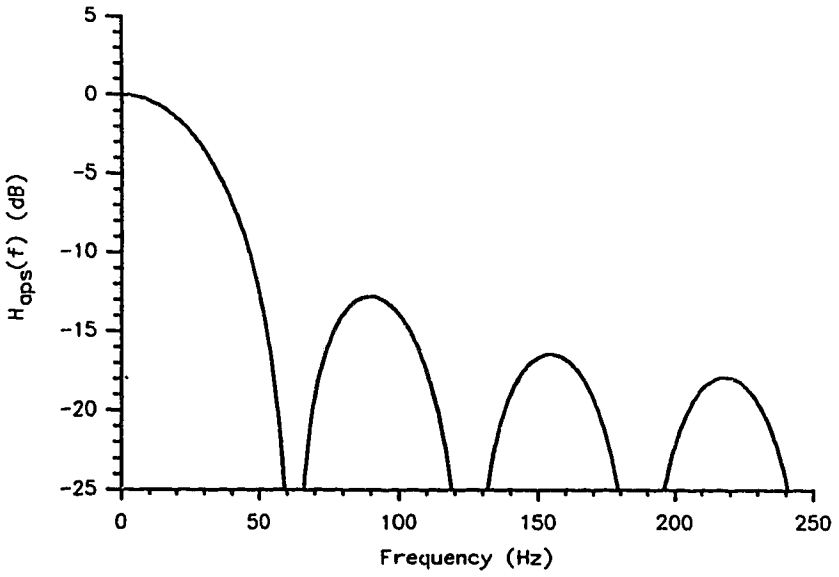

Fig. 7-5 Equivalent transfer function of 8 level running average pointer spreader.

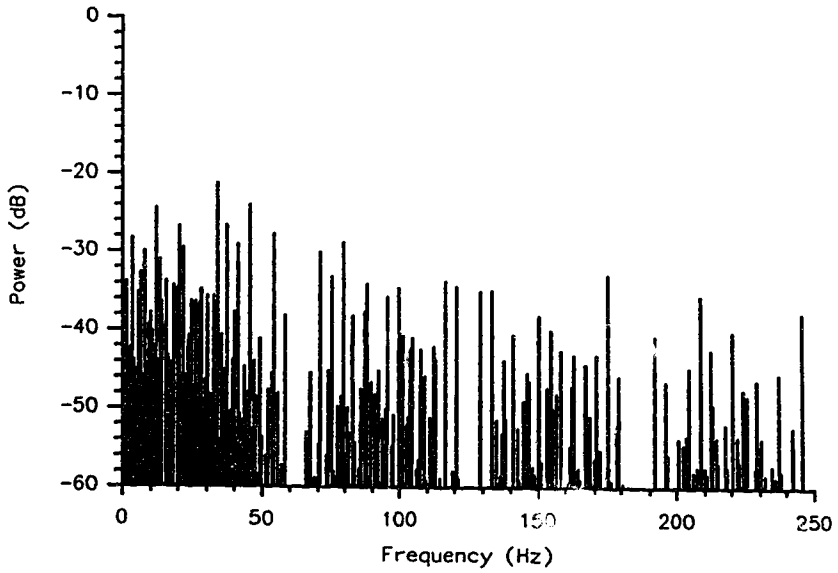

Fig. 7-6 Unfiltered power spectral density with 8 level feed forward pointer spreading and a 35 Hz VT1.5 offset frequency.

Fig. 7-7 shows the theoretical rms jitter that was obtained using Eqn. 7-6. Eqn. 6-10 was used to calculate Φ_{stm2} for the first 125 values of k with values of m chosen so that the frequency components calculated were within the band of 0 to 1 cycle per stuffing opportunity. From Fig. 7-7, altering the value of N changes both the level of the rms jitter and the shape of the rms jitter versus VT1.5 offset frequency. This non-linear interaction of N on the rms jitter was also seen for the system with only an STM synchronizer. The rms jitter with STM employed at the synchronizer and a running average pointer spreader at the desynchronizer can be reduced below 0.173 DS-1 UI when the value of N is 8 and below 0.140 DS-1 UI when the value of N is 16. For N equal to 4, the rms jitter exceeds the recommendation for maximum rms jitter generation of 0.3 DS-1 UI.

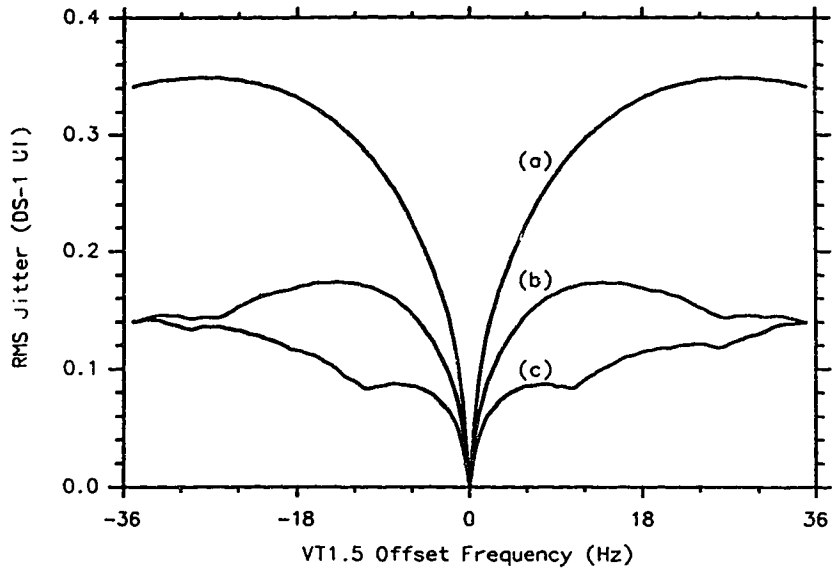

Fig. 7-7 Theoretical rms jitter versus VT1.5 offset frequency.
(a) 4 level feed forward pointer spreading.
(b) 8 level feed forward pointer spreading.
(c) 16 level feed forward pointer spreading.

iii. Simulation Results

Simulations were run for both degraded and non-degraded synchronization modes of operation. Results obtained for the rms jitter during degraded synchronization mode are compared with the theoretical results obtained above. Transient durations of 1.0 second were used in all of the simulations to allow the PLL and high pass filters to reach steady state conditions. Sampling durations were 1.0 second for the simulations of non-degraded synchronization mode and 10.0 seconds for the simulations of degraded synchronization mode. Non-degraded synchronization mode was studied by simulating the jitter versus DS-1 offset for a 0 Hz VT1.5 offset. Results are compared to the case without jitter reduction techniques as shown in Fig. 3-6

Non-Degraded Synchronization Mode

Fig. 7-8 shows the simulation results for peak to peak and rms jitter versus DS-1 offset during non-degraded synchronization mode and an initial pointer value of 0. For this simulation the initial phase in the VT1.5 SPE to VT1.5 synchronizer was set halfway between the lowest threshold level and the second lowest threshold level. For this initial pointer value the jitter was insensitive to the value of N and therefore the results are only plotted for N equal to 8. Comparing these results to the case without jitter reduction techniques as shown in Fig. 3-6, the feed forward pointer spreading method does not impair jitter performance during non-degraded synchronization mode for this value of initial pointer. From Fig. 7-8 the peak to peak jitter does not exceed 0.19 DS-1 UI and the rms jitter does not exceed 0.07 DS-1 UI. From these results it is clear that the CCITT

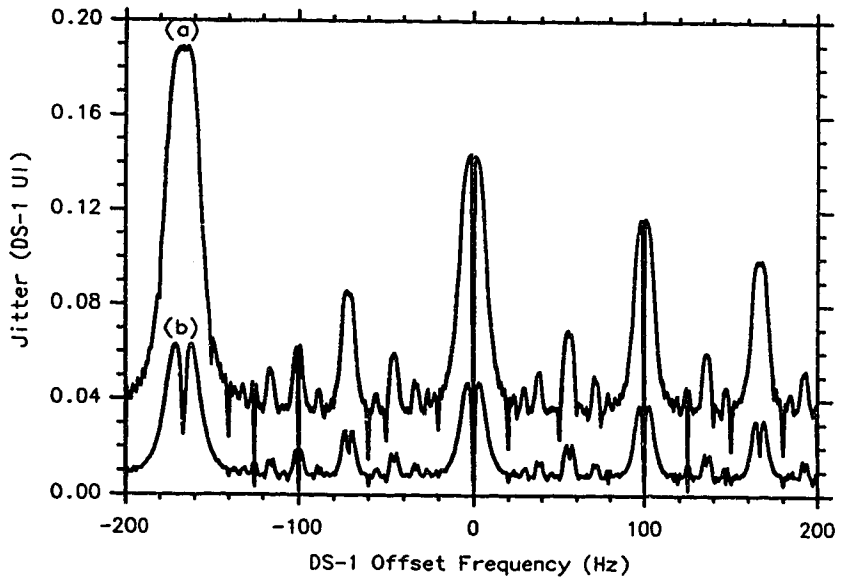

Fig. 7-8 Jitter during non-degraded synchronization mode with feed forward pointer spreading and an initial pointer value of 0.
(a) Peak to peak jitter.
(b) Rms jitter.

recommendations for maximum jitter generation are met for this case of initial pointer value.

Fig. 7-9 and Fig. 7-10 show the simulation results of non-degraded synchronization mode for rms and peak to peak jitter respectively for an initial pointer value of 25. Simulations with an initial pointer value of 24 also produces virtually the same results and are therefore not plotted. In these simulations, the initial phase in the VT1.5 SPE to VT1.5 synchronizer was set halfway between the lowest threshold level and the second lowest threshold level. Results are plotted for N equal to 8, 16, and 32. As seen from Figs. 7-9 and 7-10 the peak to peak jitter and rms jitter for this initial pointer value is sensitive to N. However, the sensitivity is significantly less than in the case with only STM used at the

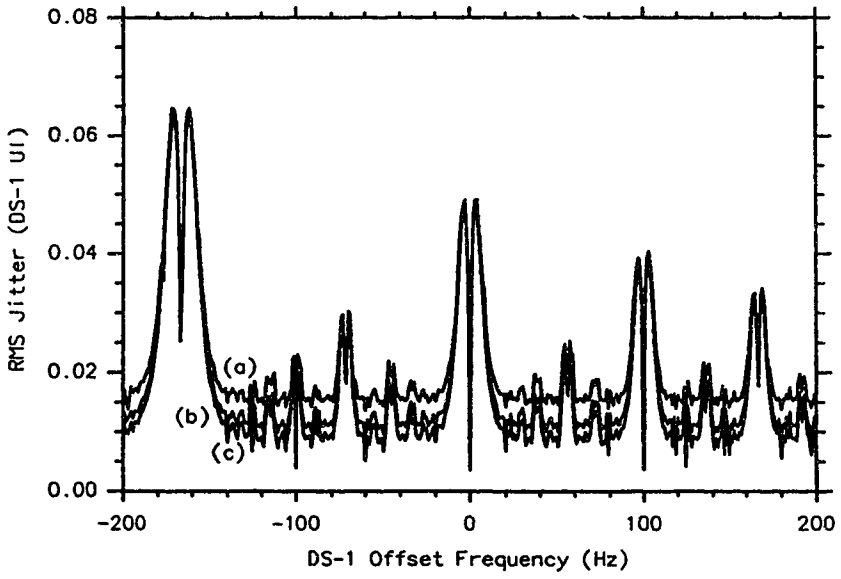

Fig. 7-9 Rms jitter during non-degraded synchronization mode with feed forward pointer spreading and an initial pointer value of 25.
(a) 16 level feed forward pointer spreading.
(b) 8 level feed forward pointer spreading.
(c) 4 level feed forward pointer spreading.

synchronizer as illustrated in Figs. 6-6 and 6-7. Comparing the results of Fig. 7-9 with that in case without jitter reduction techniques as shown in Fig. 3-6, the feed forward pointer spreading method moderately impairs the jitter during non-degraded synchronization mode for this value of initial pointer. However, the peak to peak jitter does not exceed 0.23 DS-1 UI and the rms jitter does not exceed 0.07 DS-1 UI and therefore the CCITT recommendations for maximum jitter generation are still met for this case of initial pointer value.

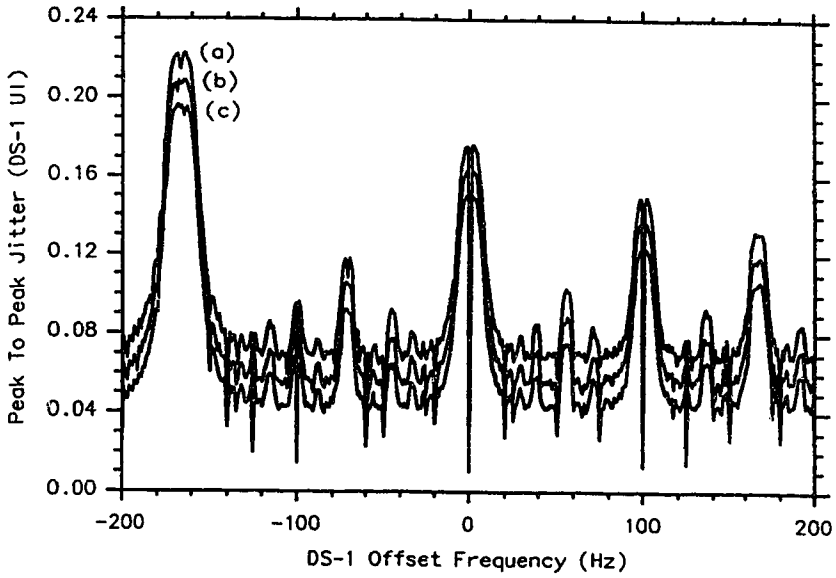

Fig. 7-10 Peak to peak jitter during non-degraded synchronization mode with feed forward pointer spreading and an initial pointer value of 25.
(a) 16 level feed forward pointer spreading.
(b) 8 level feed forward pointer spreading.
(c) 4 level feed forward pointer spreading.

Degraded Synchronization Mode

Simulation results for the rms jitter versus VT1.5 offset frequency during degraded synchronization mode are shown in Fig. 7-11. For the simulations of degraded synchronization mode, the initial pointer value was set to 12. For

almost all values of VT1.5 offset frequencies, the rms jitter decreases as N increases, and the best value for N is therefore 16. Over the entire range of VT1.5 offset frequencies, the rms jitter is below 0.351, 0.176, and 0.175 for N of 4, 8, and 16 respectively. Based on these results, the best value of N is 16. However, when N is changed from 8 to 16, there is only a marginal improvement in rms jitter performance.

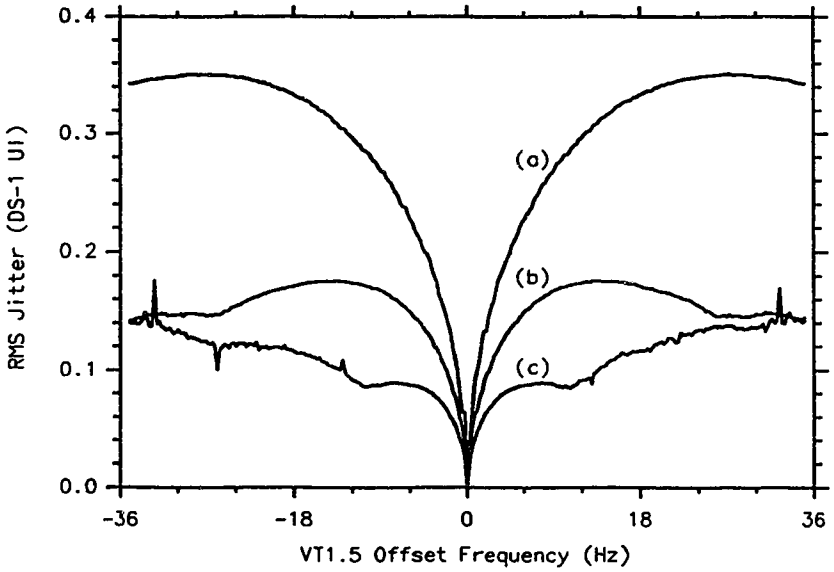

Fig. 7-11 Rms jitter during degraded synchronization mode with feed forward pointer spreading.
(a) 4 level feed forward pointer spreading.
(b) 8 level feed forward pointer spreading.
(c) 16 level feed forward pointer spreading.

The peak to peak jitter versus VT1.5 offset frequency during degraded synchronization mode is shown in Fig. 7-12. From Fig. 7-12, for small VT1.5 offset frequencies, the peak to peak jitter decreases as the value of N increases with the largest decrease in peak to peak jitter occurring when N is increased from 4 to 8. For large VT1.5 offset frequencies, the peak to peak jitter is lowest for N equal to 8. When N is increased to 16, the jitter increases slightly. In the entire

VT1.5 offset frequency range of ±35 Hz, the peak to peak jitter is below 1.04, 0.740, and 0.781 for values of N of 4, 8, and 16 respectively. Therefore, for this range of offset frequencies, the best value of N for the control of peak to peak jitter is 8. Based on both the peak to peak jitter performance and the rms jitter performance, the best value of N for this system is 8.

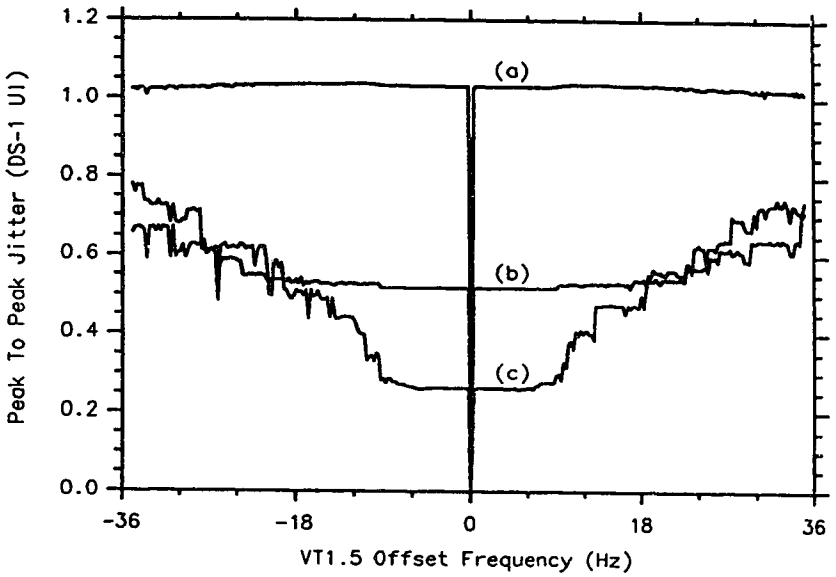

Fig. 7-12 Peak to peak jitter during degraded synchronization mode with feed forward pointer spreading.
(a) 4 level feed forward pointer spreading.
(b) 8 level feed forward pointer spreading.
(c) 16 level feed forward pointer spreading.

Comparison to Theory

For degraded mode, the results of the rms jitter versus VT1.5 offset frequency obtained from simulation results and from theory are in close agreement. The average absolute error between simulation and theoretical results for all values of N is less than 5.5%.

iv. Implementation Considerations

The system utilizing feed forward pointer spreading as was analyzed in this Chapter has a slightly more complex VT1.5 SPE to VT1.5 synchronizer than systems utilizing fixed rate or variable rate pointer spreading. The advantage of the system using feed forward pointer spreading over that of variable rate pointer spreading is that the desynchronizer is less complex and there is no need for a large pointer spreading elastic store. The advantage of feed forward pointer spreading over fixed rate pointer spreading is that the system cannot spill if the VT1.5 offset frequency exceeds the design tolerances. This spilling is possible with fixed rate pointer spreading if the leak rate is too slow. The STM synchronizer as analyzed in this Chapter causes pointer adjustments to occur at a maximum frequency of once per four VT1.5 frames. Therefore, unlike the STM system analyzed in Chapter VI, the system with feed forward pointer spreading meets the SONET standard which allows a maximum stuffing rate of once per four VT1.5 frames.

v. Summary

In this Chapter it has been shown that the jitter resulting from pointer adjustments when stuff threshold modulation is used in the VT1.5 SPE to VT1.5 synchronizer and a running average pointer spreader is used at the desynchronizer meets the CCITT recommendations for jitter generation. A system can be designed that will work with a maximum VT1.5 offset frequency of ±35 Hz and will have a maximum peak to peak and rms jitter levels of 0.740 DS-1 UI and 0.176 DS-1 UI respectively.

VIII CONCLUSIONS

I. Summary and Conclusions

This thesis has dealt with an analysis of techniques for reducing jitter on DS-1 signals caused by SONET VT1.5 pointer adjustments. Five different systems were analyzed. The first system did not use any jitter reduction techniques. From the results of the analysis of the system without jitter reduction, it was clear that its performance did not meet the CCITT recommendations for maximum jitter generation. Therefore some jitter reduction method is needed in the SONET network when DS-1 signals are transmitted in VT1.5 signals. Fixed rate pointer spreading and variable rate pointer spreading are jitter reduction techniques which are implemented as part of the desynchronization process. Stuff threshold modulation was also studied. It is implemented as part of the synchronization process. Finally, feed forward pointer spreading was analyzed which is implemented as part of both the synchronization and desynchronization process.

Each of the techniques for jitter reduction was analyzed in a similar manner. The Fourier transform of the waiting time jitter waveforms that result when each method is employed was first calculated. From this Fourier transform the rms jitter was calculated during the degraded mode. Simulations of the system were also performed which predicted the rms and peak to peak jitter performance of the system. The rms jitter results from the theory were compared with the results obtained from the simulations. In all cases, the results obtained from theory were found to be consistent with results obtained from the simulations.

Analysis of the system without jitter reduction techniques showed that the jitter resulting from pointer adjustments is higher than 4.0 DS-1 UI peak to peak and 1.0 DS-1 UI rms. These jitter levels are higher than the CCITT recommendations for maximum jitter levels of 1.0 DS-1 UI peak to peak and 0.3 DS-1 UI rms. Theoretical analysis of the waiting time jitter showed that the spectral components of the jitter are highest at low frequencies and therefore cannot be filtered out by a conventional PLL. An important result obtained from the analysis of this system was that the phase step caused by a pointer adjustment is not exactly 8.0 VT1.5 SPE UI, but is dependent on the initial pointer value and the pointer adjustment direction.

Analysis of the system employing fixed rate pointer spreading predicted jitter levels that were below the CCITT recommendations for maximum jitter generation. An important result obtained from this analysis was that the best value of the fractional phase step magnitude for this system was 1/2 VT1.5 SPE UI. The system with this value of fractional phase step magnitude and a leak period of 56 VT1.5 SPE frames per VT1.5 SPE UI was found to have maximum peak to peak jitter levels of 0.54 DS-1 UI and maximum rms jitter levels of 0.25 DS-1 UI over a ±35 Hz VT1.5 offset frequency range.

Variable rate pointer spreading was also analyzed and was found to reduce jitter below the CCITT recommendations. A system with a 0.5 Hz cutoff frequency for the variable rate pointer spreader was found to have maximum peak to peak and rms jitter levels of 0.45 DS-1 UI and 0.10 DS-1 UI respectively over a VT1.5 offset frequency range of ±35 Hz. The best value in terms of jitter performance for the magnitude of the fractional phase steps that are leaked out was found to be 1/4 VT1.5 SPE UI for this system.

Stuff threshold modulation was verified as a means of controlling jitter caused by pointer adjustments in SONET. A system with 16 level modified STM

was found to have maximum peak to peak and rms jitter levels of 0.37 DS-1 UI and 0.093 DS-1 UI respectively.

The final jitter reduction technique which was analyzed was feed forward pointer spreading. In this system, STM was used in the synchronizer as a method of transmitting the synchronizer elastic store phase to the desynchronizer. A system with 8 level modified STM used at the synchronizer and a running average pointer spreader at the desynchronizer was found to have maximum peak to peak and rms jitter levels of 0.740 DS-1 UI and 0.176 DS-1 UI respectively.

A summary of the maximum rms and peak to peak jitter levels of the five systems described above is shown in Table 8-1. From this table it can be seen that the best waiting time jitter performance is achieved using STM at the synchronizer. It must be noted that these results are for a 0 Hz DS-1 offset frequency. If the DS-1 offset frequency is varied, the peak to peak and rms jitter will increase. The maximum peak to peak and rms jitter caused by the DS-1 to VT1.5 SPE synchronization is 0.19 DS-1 UI and 0.07 DS-1 UI respectively (see Fig. 3-6). The worst case peak to peak jitter including the DS-1 to VT1.5 SPE synchronization process can be found by adding 0.19 DS-1 UI to the results in Table 8-1. The worst case rms jitter can be found by the addition of 0.07 DS-1 UI on a power basis to the results in Table 8-1. If this is done it is observed that the systems with jitter reduction techniques still meet the CCITT recommendation by a reasonable margin. However this margin is reduced in all cases as compared to the case without considering the DS-1 to VT1.5 SPE synchronization.

Table 8-1 Maximum jitter levels of systems analyzed during degraded mode operation.

Jitter Reduction Technique	Peak To Peak Jitter	RMS Jitter
None	4.120	1.060
Fixed Rate	0.524	0.236
Variable Rate	0.438	0.103
STM	0.373	0.093
Feed Forward	0.740	0.176

From the analysis contained of this thesis, it is clear that some jitter reduction method is required in SONET networks to reduce the jitter caused by VT1.5 pointer adjustments. The best method found of the four jitter reduction techniques studied in terms of jitter performance was 16 level modified stuff threshold modulation. This technique has the advantage of needing only very simple desynchronizers. The jitter reduction is obtained through a modest increase in complexity at the synchronizer. The disadvantage of this method is that it requires a change to the SONET rates and formats specification. This is so because the STM technique described can cause a maximum pointer adjustment frequency of one in every VT1.5 frame. The SONET standard however, limits the maximum number of pointer adjustments to one in every four VT1.5 frames. The best method in terms of jitter performance that does not require a change to the SONET standard is variable rate pointer spreading.

ii. Future Work

The magnitude of the elastic store in a variable rate pointer spreader is dependent on the cutoff frequency and on the implementation of the pointer spreader. The design of variable rate pointer spreading logic is similar to the design of all digital PLL circuits which can be designed so that they have steady state phase offsets of zero. It seems reasonable to attempt to implement a variable rate pointer spreading circuit which has a zero steady state error and

therefore does not require an extremely large elastic store even when the cutoff frequency is very low. Further work should be done in this area in the future.

Stuff threshold modulation has been shown in this thesis to be a valid method of reducing waiting time jitter caused by SONET pointer adjustments. An STM synchronizer that uses every fourth stuff opportunity should meet the SONET standard which allows a maximum pointer adjustment frequency of one per four frames. A system utilizing this type of STM synchronizer along with a desynchronizer which has a bandwidth tighter than 25 Hz should be studied to determine its jitter performance.

Feed forward pointer spreading requires information about the synchronizer elastic store phase to be transmitted to the desynchronizer. In the work done in this thesis, this information was sent by using STM at the synchronizer. Another possibility that would not require a significant change to the SONET standard would be to use the negative stuff location of the VT1.5 to transmit the synchronizer elastic store phase. This is possible because the negative stuff location normally contains a dummy byte which is ignored by the desynchronizer. Future work should be done on the implementation considerations and on the jitter performance of a system using this type of feed forward pointer spreading.

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APPENDIX A

i. Bilinear Transformation of PLL Transfer Function

The PLL transfer function is of the form

$$H(s) = \frac{\omega_c^2}{s^2 + \sqrt{2}s\omega_c + \omega_c^2}, \qquad \text{(A-1)}$$

where ω_c is the 3 dB frequency in rad/s. The bilinear transformation of this transfer function can be obtained by making the substitutions

$$\Omega_c \rightarrow \omega_c, \text{ and } \qquad \frac{z-1}{z+1} \rightarrow s$$

where Ω_c is the 3 dB frequency of the digital filter. Making these substitutions in Eqn. A-1 and multiplying the numerator and denominator by $(z+1)^2$, the transfer function

$$H(z) = \frac{\Omega_c^2(z+1)^2}{(z-1)^2 + \sqrt{2}\Omega_c(z-1)(z+1) + \Omega_c^2(z+1)^2}, \qquad \text{(A-2)}$$

is obtained. Rearranging Eqn. A-2 by grouping like terms, this transfer function is simplified to

$$H(z) = \frac{z^2\left(\Omega_c^2\right) + z\left(2\Omega_c^2\right) + \left(\Omega_c^2\right)}{z^2\left(\Omega_c^2+\sqrt{2}\Omega_c+1\right) + z\left(2\Omega_c+1\right) + \left(\Omega_c^2+\sqrt{2}\Omega_c+1\right)}. \qquad \text{(A-3)}$$

Finally, the transfer function is normalized by dividing the numerator and denominator by

$$z^2\left(\Omega_c^2+\sqrt{2}\Omega_c+1\right).$$

This produces the final result

$$H(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2}}{1 + b_1 z^{-1} + b_2 z^{-2}}, \qquad \text{(A-4)}$$

where

$$a_0 = \frac{\Omega_c^2}{\Omega_c^2 + \sqrt{2}\Omega_c + 1}, \qquad a_1 = 2a_0, \qquad a_2 = a_0,$$

$$b_1 = \frac{2\Omega_c^2 + 1}{\Omega_c^2 + \sqrt{2}\Omega_c + 1}, \text{ and } b_2 = \frac{\Omega_c^2 - \sqrt{2}\Omega_c + 1}{\Omega_c^2 + \sqrt{2}\Omega_c + 1}.$$

The final step in the bilinear transformation process is to prewarp the 3 dB frequency ω_c of the analog prototype filter into the normalized frequency Ω_c of the digital filter. This is achieved using the relation

$$\Omega_c = \tan\left(\frac{\omega_c T_s}{2}\right), \qquad \text{(A-5)}$$

where T_s is the time in seconds between successive sample points.

ii. Bilinear Transformation of Jitter Measuring Equipment

The transfer function of the jitter measuring equipment is of the form

$$H(s) = \frac{s}{s + \omega_c}, \qquad \text{(A-6)}$$

where ω_c is the 3 dB frequency in rad/s. The bilinear transformation of this transfer function can be obtained by making the substitutions

$$\Omega_c \rightarrow \omega_c, \text{ and} \qquad \frac{z-1}{z+1} \rightarrow s$$

where Ω_c is the 3 dB frequency of the digital filter. Making these substitutions in Eqn. A-6 and multiplying the numerator and denominator by $(z+1)$, the transfer function

$$H(z) = \frac{(z-1)}{(z-1) + \Omega_c(z+1)}, \qquad \text{(A-7)}$$

is obtained. Rearranging Eqn. A-7 by grouping like terms, this transfer function is simplified to

$$H(z) = \frac{z[1] + [-1]}{z[\Omega_c+1] + [\Omega_c-1]}. \qquad \text{(A-8)}$$

Finally, the transfer function is normalized by dividing the numerator and denominator by

$z[\Omega_c+1]$.

This produces the final result

$$H(z) = \frac{a_0 + a_1 z^{-1}}{1 + b_1 z^{-1}}, \qquad \text{(A-9)}$$

where

$$a_0 = \frac{1}{\Omega_c + 1}, \qquad a_1 = -a_0, \text{ and}$$

$$b_1 = \frac{\Omega_c - 1}{\Omega_c + 1}.$$

The final step in the bilinear transformation process is to prewarp the frequency ω_c of the prototype analog filter into the normalized frequency Ω_c of the digital filter. This is done using the relation

$$\Omega_c = \tan\left(\frac{\omega_c T_s}{2}\right), \qquad \text{(A-10)}$$

where T_s is the time in seconds between successive sample points.

APPENDIX B

i. Fourier Transform of $\phi_{s1}(t)$

The first term of $\phi_s(t)$ is

$$\phi_{s1}(t) = \rho\mu(t). \tag{B-1}$$

To calculate the Fourier transform of $\phi_{s1}(t)$, it is first represented as a Fourier series expansion. The exponential Fourier series of $\mu(t)$ is of the form

$$\mu(t) = \sum_{k=-\infty}^{\infty} X_k e^{jk\omega_0 t}, \tag{B-2}$$

where

$$\omega_0 = \frac{2\pi}{T_0}, \text{ and} \qquad X_k = \frac{1}{T_0}\int_{t_0}^{t_0+T_0} \mu(t) e^{-jk\omega_0 t}\, dt.$$

The function $\mu(t)$ is a unity amplitude sawtooth waveform with a period of 1.0. The Fourier coefficients can therefore be calculated from

$$X_k = \int_0^1 te^{-j2\pi kt}\, dt. \tag{B-3}$$

This produces the Fourier coefficients

$$X_k = \frac{j}{2\pi k}, \text{ for } k \neq 0, \text{ and} \qquad X_0 = \frac{1}{2},$$

and the function $\mu(t)$ can therefore be written as

$$\mu(t) = \frac{1}{2} + \sum_{k=1}^{\infty} \frac{j}{2\pi k}(e^{j2\pi kt} - e^{-j2\pi kt}). \tag{B-4}$$

The term $\phi_{s1}(t)$ is equal to $\mu(t)$ multiplied by ρ and is therefore equal to

$$\phi_{s1}(t) = \frac{\rho}{2} + \sum_{k=1}^{\infty} \frac{j\rho}{2\pi k}(e^{j2\pi kt} - e^{-j2\pi kt}). \qquad \text{(B-5)}$$

The Fourier transform of $\phi_{s1}(t)$ can now be taken and is equal to

$$\Phi_{s1}(f) = \frac{\rho}{2}\delta(f) + \sum_{k=1}^{\infty} \frac{j\rho}{2\pi k}\left[\delta(f-k) - \delta(f+k)\right]. \qquad \text{(B-6)}$$

ii. Fourier Transform of $\phi_{s2}(t)$

The second term of $\phi_s(t)$ is

$$\phi_{s2}(t) = \mu\big(\rho[t]\big). \tag{B-7}$$

The function $\phi_{s2}(t)$ is a staircase function because its magnitude can only change when t is an integer. Therefore, $\phi_{s2}(t)$ can be written as a sample and hold waveform. The function can be sampled using a train of delta functions, and the hold operation can be performed by convolving the resulting sampled function with a square pulse. The resulting sample and hold waveform is

$$\mu\big(\rho[t]\big) = \big(U(t) - U(t-1)\big)*\Big(\mu\big(\rho[t]\big)\cdot\sum_{m=-\infty}^{\infty}\delta(t-m)\Big). \tag{B-8}$$

This can be simplified by noting that

$$\mu\big(\rho[t]\big)\cdot\delta(t-m) = \mu(\rho t)\cdot\delta(t-m), \text{ for } m = 0, \pm1, \pm2, \ldots$$

The function $\phi_{s2}(t)$ can therefore be written as

$$\phi_{s2}(t) = \big(U(t) - U(t-1)\big)*\Big(\mu(\rho t)\cdot\sum_{m=-\infty}^{\infty}\delta(t-m)\Big). \tag{B-9}$$

In order to take the Fourier transform of $\phi_{s2}(t)$ it is written as

$$\phi_{s2}(t) = \phi_{s2a}(t)*\big(\phi_{s2b}(t)\cdot\phi_{s2c}(t)\big), \tag{B-10}$$

where

$$\phi_{s2a}(t) = U(t) - U(t-1), \qquad \phi_{s2b}(t) = \mu(\rho t), \text{ and}$$

$$\phi_{s2c}(t) = \sum_{m=-\infty}^{\infty}\delta(t-m),$$

and the Fourier transforms of the terms $\phi_{s2a}(t)$, $\phi_{s2b}(t)$, and $\phi_{s2c}(t)$ are taken separately.

The first term in the expansion of $\phi_{s2}(t)$ is

$$\phi_{s2a}(t) = U(t) - U(t-1). \tag{B-11}$$

This term is equal to unity over the range between 0 and 1, and is equal to zero elsewhere. The Fourier transform can therefore be calculated from

$$\Phi_{s2a}(f) = \int_0^1 e^{-j2\pi ft}\, dt. \tag{B-12}$$

This produces the result for the Fourier transform of $\phi_{s2a}(t)$ which is

$$\Phi_{s2a}(f) = e^{-j\pi f}\,\frac{\sin(\pi f)}{\pi f}. \tag{B-13}$$

The second term in the expansion of $\phi_{s2}(t)$ is

$$\phi_{s2b}(t) = \mu(\rho t). \tag{B-14}$$

To calculate the Fourier transform of $\phi_{s2b}(t)$, it is first represented as a Fourier series expansion. The exponential Fourier series of $\phi_{s2b}(t)$ is of the form

$$\phi_{s2b}(t) = \sum_{k=-\infty}^{\infty} X_k e^{jk\omega_0 t}, \tag{B-15}$$

where

$$\omega_0 = \frac{2\pi}{T_0}, \text{ and} \qquad X_k = \frac{1}{T_0}\int_{t_0}^{t_0+T_0} \mu(t) e^{-jk\omega_0 t}\, dt.$$

The function $\phi_{s2b}(t)$ is a unity amplitude sawtooth waveform with a period of $1/\rho$. The Fourier coefficients can therefore be calculated from

$$X_k = \rho\int_0^{1/\rho} \rho t e^{-j2\pi\rho kt}\, dt. \tag{B-16}$$

This produces the Fourier coefficients

$$X_k = \frac{j}{2\pi k}, \text{ for } k \neq 0, \text{ and} \qquad X_0 = \frac{1}{2}.$$

The function $\phi_{s2b}(t)$ can therefore be written as

$$\phi_{s2b}(t) = \frac{1}{2} + \sum_{k=1}^{\infty} \frac{j}{2\pi k}\left(e^{j2\pi\rho kt} - e^{-j2\pi\rho kt}\right), \qquad \text{(B-17)}$$

and the Fourier transform of $\phi_{s2b}(t)$ is

$$\Phi_{s2b}(f) = \frac{1}{2}\delta(f) + \sum_{k=1}^{\infty} \frac{j}{2\pi k}\left[\delta(f-\rho k) - \delta(f+\rho k)\right]. \qquad \text{(B-18)}$$

The final term in the expansion of $\phi_{s2}(t)$ is

$$\phi_{s2c}(t) = \sum_{m=-\infty}^{\infty} \delta(t-m). \qquad \text{(B-19)}$$

The Fourier transform of this term is found from tables and is equal to

$$\Phi_{s2c}(f) = \sum_{m=-\infty}^{\infty} \delta(f-m). \qquad \text{(B-20)}$$

The Fourier transform of $\phi_s(t)$ can be found using some of the properties of Fourier transforms. Multiplication in the time domain is replaced by convolution in the frequency domain, and convolution in the time domain is replaced by multiplication in the frequency domain. This produces the result

$$\Phi_{s2}(f) = \Phi_{s2a}(f) \cdot \left[\Phi_{s2b}(f) * \Phi_{s2c}(f)\right]. \qquad \text{(B-21)}$$

Applying this relationship to Eqns. B-13, B-18, and B-20 the Fourier transform of $\phi_{s2}(t)$ is found after some simplification to be

$$\Phi_{s2}(f) = \frac{1}{2}\delta(f) + e^{-j\pi f}\,\frac{\sin(\pi f)}{\pi f} \sum_{k=1}^{\infty} \sum_{m=-\infty}^{\infty} \frac{j}{2\pi k}\left[\delta(f-\rho k-m) - \delta(f+\rho k-m)\right]. \qquad \text{(B-22)}$$

APPENDIX C

I. Mathematical Description of Pointer Spreading

It is claimed that the waiting time jitter waveform after pointer spreading, $\phi_{ps}(t)$, can be described by the equation

$$\phi_{ps}(t) = \phi_s(t) * h_{ps}(t). \tag{C-1}$$

The term $\phi_s(t)$ is the waiting time jitter waveform with a plus/zero/minus synchronizer and $h_{ps}(t)$ is the equivalent impulse response of the pointer spreader given by

$$h_{ps}(t) = \frac{\beta}{8} \sum_{n=1}^{8/\beta} \delta\left(t - \tau_n\right). \tag{C-2}$$

The term τ_n is the interval of time from a pointer adjustment to the moment when the nth fractional phase step is leaked out.

To understand this description of pointer spreading, consider the simple case shown in Fig. C-1. For this example, the solid line represents $\phi_{ps}(t)$ and the dotted line represents $\phi_s(t)$. For this case, β is equal to 4, τ_1 is equal to 0, and τ_2 is equal to 1 stuff opportunity. Therefore,

$$h_{ps}(t) = \frac{1}{2}\left(\delta(t) + \delta(t-1)\right), \tag{C-3}$$

which gives

$$\phi_{ps}(t) = \frac{1}{2}\phi_s(t) * \left(\delta(t) + \delta(t-1)\right). \tag{C-4}$$

This equation can be simplified to

$$\phi_{ps}(t) = \frac{1}{2}\phi_s(t) + \frac{1}{2}\phi_s(t-1). \qquad (C\text{-}5)$$

In order to show that this equation gives the waveform as shown by the solid line in Fig. C-1, two conditions must be satisfied. The first condition is that the slope of $\phi_{ps}(t)$ is equal to the slope of $\phi_s(t)$. The second condition is that the magnitude of the discontinuities of $\phi_{ps}(t)$ are exactly equal to one half of the magnitude of the discontinuities of $\phi_s(t)$. By geometry, see Fig. C-1, if these two conditions are met, Eqn. C-5 will give the correct waiting time jitter waveform.

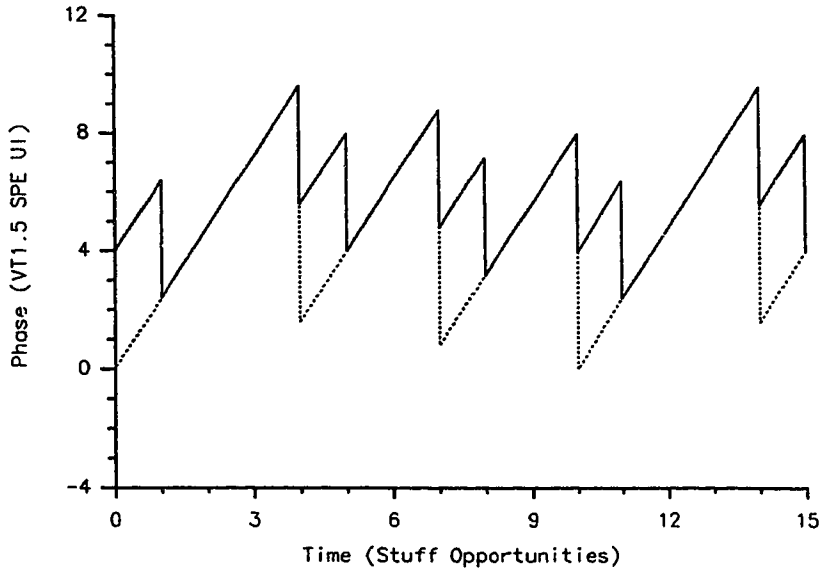

Fig. C-1 Waiting time jitter waveform with pointer spreading.

To show that the slope of $\phi_{ps}(t)$ is equal to the slope of $\phi_s(t)$, the derivative of Eqn. C-5 is taken and is equal to

$$\frac{d}{dt}\phi_{ps}(t) = \frac{1}{2}\frac{d}{dt}\phi_s(t) + \frac{1}{2}\frac{d}{dt}\phi_s(t-1). \qquad (C\text{-}6)$$

Because the slope of $\phi_s(t)$ is constant except for discontinuities

$$\frac{d}{dt}\phi_s(t) = \frac{d}{dt}\phi_s(t-1), \qquad (C\text{-}7)$$

and therefore

$$\frac{d}{dt}\phi_{ps}(t) = \frac{d}{dt}\phi_{s}(t). \qquad (C\text{-}8)$$

The physical reason for the equality of slopes of $\phi_{ps}(t)$ and $\phi_{s}(t)$ is that they both represent the rate of phase change determined by the fixed frequency difference between the read and write clocks at the synchronizer.

From Eqn. C-5, $\phi_{ps}(t)$ is the sum of one half of $\phi_{s}(t)$ and one half of a delayed version of $\phi_{s}(t)$. From this result, any discontinuity of $\phi_{s}(t)$ will cause two discontinuities of $\phi_{ps}(t)$ separated by 1 stuff opportunity, each with a magnitude of one half of the magnitude of discontinuities of $\phi_{s}(t)$.

Hence, we have demonstrated that for the simple case shown in Fig. C-1, Eqn. C-1 produces the proper waiting time jitter waveform with pointer spreading. The reasoning used in this case can be extended to include both fixed rate and variable rate pointer spreading by applying the appropriate values of β and τ_n. The maximum value of τ_n must be less than the minimum distance between successive pointer adjustments.

APPENDIX D

i. Description of Variable Rate Pointer Spreader

The rate at which a variable rate pointer spreading elastic store is emptied is proportional to the fill of the elastic store. This process can be represented by the function

$$\frac{dB}{dt} = -\alpha B, \tag{D-1}$$

where α is a constant which determines the cutoff frequency of the variable rate pointer spreader and B is the amount of phase difference with which the elastic store is filled. The term αB determines the instantaneous leak rate of the pointer spreader. Eqn. D-1 can be rewritten as

$$\frac{-1}{\alpha B}\, dB = dt, \tag{D-2}$$

and the terms on both sides can be integrated to produce the function

$$-\frac{1}{\alpha} \ln(B) = t + a, \tag{D-3}$$

where a is a constant. This can be rewritten as

$$B = Ce^{-\alpha t}, \tag{D-4}$$

where C is a constant. This expression demonstrates that the amount that the pointer spreading elastic store is filled follows an exponential curve. By analogy, a first order filter also follows an exponential curve. By making the substitution

$$\alpha = 2\pi f_{vps}, \tag{D-5}$$

the amount of fill of the elastic store can be expressed as

$$B = Ce^{-2\pi f_{vps} t}, \tag{D-6}$$

where f_{vps} is the normalized cutoff frequency of the variable rate pointer spreader.

The value of the constant c can be determined by assuming that 8.0 VT1.5 SPE UI will be leaked out in a time equal to $1/|\rho|$. The fill of the elastic store immediately after the pointer adjustment, at time equal to 0, is c. At a time equal to $1/|\rho|$, the fill of the elastic store will be equal to $c - 8$. Substituting this time and fill of elastic store into Eqn. D-6, the equality

$$Ce^{-2\pi f_{vps}/|\rho|} = c - 8, \tag{D-7}$$

is obtained. This equality can be used to determine the value of the constant c which is

$$c = \frac{8}{1 - e^{-2\pi f_{vps}/|\rho|}}. \tag{D-8}$$

The times at which a variable rate pointer spreader will leak out fractional phase steps can be determined once the value of c is known. The first fractional phase step is leaked out at a time equal to 0 which occurs when the fill of the elastic store is c. When next fractional phase step is leaked out the fill of the elastic store is reduced to $c - \beta$, where β is the magnitude of the fractional phase step. Using this reasoning, the equality

$$c - (n-1)\beta = Ce^{-2\pi f_{vps}\tau_n}, \tag{D-9}$$

is obtained where τ_n is the time that the nth fractional phase step is leaked out. This equality can be used to determine the values of τ_n with the aid of Eqn. D-8, generating the relationship for τ_n given by

$$\tau_n = \frac{-1}{2\pi f_{vps}} \ln\left[1 - \frac{(n-1)\beta}{8}\left[1 - e^{-j2\pi f_{vps}/|\rho|}\right]\right]. \tag{D-10}$$

APPENDIX E

i. Fourier Transform of $\phi_{stm1}(t)$

The first term of $\phi_{stm}(t)$ is

$$\phi_{stm1}(t) = \rho\mu(t). \tag{E-1}$$

From the results of Appendix B.i, the Fourier transform of this function is

$$\Phi_{stm1}(f) = \frac{\rho}{2}\delta(f) + \sum_{k=1}^{\infty} \frac{j\rho}{2\pi k}\left(\delta(f-k) - \delta(f+k)\right). \tag{E-2}$$

ii. Fourier Transform of $\phi_{stm2}(t)$

The second term of $\phi_{stm}(t)$ is

$$\phi_{stm2}(t) = \mu\left(\rho[t] - \frac{1}{8}T_{[t]\bmod N}\right), \tag{E-3}$$

The function $\phi_{stm2}(t)$ is a staircase function because its magnitude can only change when t is an integer. Therefore, $\phi_{stm2}(t)$ can be written as a sample and hold waveform. The function can be sampled using a train of delta functions, and the hold operation can be performed by convolving the resulting sampled function with a square pulse. The resulting sample and hold waveform is

$$\phi_{stm2}(t) = \left(U(t) - U(t-1)\right) * \left(\mu\left(\rho[t] - \frac{1}{8}T_{[t]\bmod N}\right) \cdot \sum_{m=-\infty}^{\infty} \delta(t-m)\right). \tag{E-4}$$

This equation is expanded by making the substitution

$$\sum_{m=-\infty}^{\infty} \delta(t-m) = \sum_{n=0}^{N-1} \sum_{m=-\infty}^{\infty} \delta(t-n-mN), \tag{E-5}$$

which after some rearrangement gives

$$\phi_{stm2}(t) = \left(U(t) - U(t-1)\right) * \sum_{n=0}^{N-1} \left(\mu\left(\rho[t] - \frac{1}{8}T_{[t]\bmod N}\right) \cdot \sum_{m=-\infty}^{\infty} \delta(t-n-mN)\right). \tag{E-6}$$

This can be simplified by noting that

$$\mu\left(\rho[t] - \frac{1}{8}T_{[t]\bmod N}\right) \cdot \delta(t-n-mN) = \mu(\rho t - \frac{1}{8}T_n) \cdot \delta(t-n-mN), \tag{E-7}$$

which allows the function $\phi_{stm2}(t)$ to be written as

$$\phi_{stm2}(t) = \left(U(t) - U(t-1)\right) * \sum_{n=0}^{N-1} \left(\mu(\rho t - \frac{1}{8}T_n) \cdot \sum_{m=-\infty}^{\infty} \delta(t-n-mN)\right). \tag{E-8}$$

In order to take the Fourier transform of $\phi_{stm2}(t)$ it is written as

$$\phi_{stm2}(t) = \phi_{stm2a}(t) * \sum_{n=0}^{N-1} \left[\phi_{stm2b}(t) \cdot \phi_{stm2c}(t)\right], \qquad \text{(E-9)}$$

where

$$\phi_{stm2a}(t) = U(t) - U(t-1), \qquad \phi_{stm2b}(t) = \mu(\rho t - \tfrac{1}{8}T_n), \text{ and}$$

$$\phi_{stm2c}(t) = \sum_{m=-\infty}^{\infty} \delta(t-n-mN),$$

and the Fourier transforms of the terms $\phi_{stm2a}(t)$, $\phi_{stm2b}(t)$, and $\phi_{stm2c}(t)$ are taken separately.

The first term in the expansion of $\phi_{stm2}(t)$ is

$$\phi_{stm2a}(t) = U(t) - U(t-1). \qquad \text{(E-10)}$$

From Appendix B.ii, the Fourier transform of this is

$$\Phi_{stm2a}(f) = e^{-j\pi f} \frac{\sin(\pi f)}{\pi f}. \qquad \text{(E-11)}$$

The second term in the expansion of $\phi_{stm2}(t)$ is

$$\phi_{stm2b}(t) = \mu(\rho t - \tfrac{1}{8}T_n). \qquad \text{(E-12)}$$

To calculate the Fourier transform of $\phi_{stm2b}(t)$, it is first represented as a Fourier series expansion. The exponential Fourier series of $\phi_{stm2b}(t)$ is of the form

$$\phi_{stm2b}(t) = \sum_{k=-\infty}^{\infty} X_k e^{jk\omega_0 t}, \qquad \text{(E-13)}$$

where

$$\omega_0 = \frac{2\pi}{T_0}, \text{ and} \qquad X_k = \frac{1}{T_0} \int_{t_0}^{t_0+T_0} \mu(\rho t - \tfrac{1}{8}T_n) e^{-jk\omega_0 t}\, dt.$$

The function $\phi_{stm2b}(t)$ is a unity amplitude sawtooth waveform with a period of $1/\rho$. Its Fourier coefficients can therefore be calculated from

$$X_k = \rho\int_{T_n/8\rho}^{(T_n+8)/8\rho} (\rho t - \frac{1}{8}T_n)e^{-j2\pi\rho kt}\, dt. \qquad \text{(E-14)}$$

This produces the Fourier coefficients

$$X_k = e^{-j2\pi kT_n/8}\,\frac{j}{2\pi k}, \text{ for } k \neq 0, \text{ and } \quad X_0 = \frac{1}{2}.$$

The function $\phi_{stm2b}(t)$ can therefore be written as

$$\phi_{stm2b}(t) = \frac{1}{2} + \sum_{k=1}^{\infty} \frac{j}{2\pi k}(e^{-j2\pi kT_n/8}\, e^{j2\pi\rho kt} - e^{j2\pi kT_n/8}\, e^{-j2\pi\rho kt}), \qquad \text{(E-15)}$$

and the Fourier transform of $\phi_{stm2b}(t)$ is

$$\Phi_{stm2b}(f) = \frac{1}{2}\delta(f) + \sum_{k=1}^{\infty} \frac{j}{2\pi k}\left(e^{-j2\pi kT_n/8}\, \delta(f-\rho k) - e^{j2\pi kT_n/8}\, \delta(f+\rho k)\right). \qquad \text{(E-16)}$$

The final term in the expansion of $\phi_{stm2}(t)$ is

$$\phi_{stm2c}(t) = \sum_{m=-\infty}^{\infty} \delta(t-n-mN). \qquad \text{(E-17)}$$

The Fourier transform of this term is found from tables and is equal to

$$\Phi_{stm2c}(f) = \frac{1}{N}\sum_{m=-\infty}^{\infty} e^{-j2\pi nm/N}\, \delta\left(f-\frac{m}{N}\right). \qquad \text{(E-18)}$$

The Fourier transform of $\phi_{stm}(t)$ can be found using some of the properties of Fourier transforms. Multiplication in the time domain is replaced by convolution in the frequency domain, and convolution in the time domain is replaced by multiplication in the frequency domain. This produces the result

$$\Phi_{stm2}(f) = \Phi_{stm2a}(f)\cdot\sum_{n=0}^{N-1} \left(\Phi_{stm2b}(f)*\Phi_{stm2c}(f)\right). \qquad \text{(E-19)}$$

Applying this relationship to Eqns. E-11, E-16, and E-18 the Fourier transform of $\phi_{stm2}(t)$ is found after some simplification to be

$$\Phi_{stm2}(f) = \frac{1}{2}\delta(f) + e^{-j\pi f}\frac{\sin(\pi f)}{\pi f}\sum_{k=1}^{\infty}\sum_{m=-\infty}^{\infty}\frac{j}{2\pi k}\left(A_{k,m}\delta\left(f-\rho k-\frac{m}{N}\right) - B_{k,m}\delta\left(f+\rho k-\frac{m}{N}\right)\right), \tag{E-20}$$

where

$$A_{k,m} = \frac{1}{N}\sum_{n=0}^{N-1} e^{-j2\pi(kT_n/8 + mn/N)},$$

and

$$B_{k,m} = \frac{1}{N}\sum_{n=0}^{N-1} e^{j2\pi(kT_n/8 - mn/N)}.$$

iii. Fourier Transform of $\phi_{stm3}(t)$

The third term of $\phi_{stm}(t)$ is

$$\phi_{stm3}(t) = \frac{1}{8}T_{[t]\bmod N}. \tag{E-21}$$

The function $\phi_{stm3}(t)$ is a staircase function because its magnitude can only change when t is an integer. Therefore, $\phi_{stm3}(t)$ can be written as a sample and hold waveform. The function can be sampled using a train of delta functions, and the hold operation can be performed by convolving the resulting sampled function with a square pulse. The resulting sample and hold waveform is

$$\phi_{stm3}(t) = \big[U(t) - U(t-1)\big] * \left[\frac{1}{8}T_{[t]\bmod N} \cdot \sum_{m=-\infty}^{\infty} \delta(t-m)\right]. \tag{E-22}$$

This equation is expanded by making the substitution

$$\sum_{m=-\infty}^{\infty} \delta(t-m) = \sum_{n=0}^{N-1} \sum_{m=-\infty}^{\infty} \delta(t-n-mN), \tag{E-23}$$

which after some rearrangement gives

$$\phi_{stm3}(t) = \big[U(t) - U(t-1)\big] * \sum_{n=0}^{N-1} \left[\frac{1}{8}T_{[t]\bmod N} \cdot \sum_{m=-\infty}^{\infty} \delta(t-n-mN)\right]. \tag{E-24}$$

This can be simplified by noting that

$$\frac{1}{8}T_{[t]\bmod N} \cdot \delta(t-n-mN) = \frac{1}{8}T_n \cdot \delta(t-n-mN), \tag{E-25}$$

which allows the function $\phi_{stm3}(t)$ to be written as

$$\phi_{stm3}(t) = \big[U(t) - U(t-1)\big] * \sum_{n=0}^{N-1} \left[\sum_{m=-\infty}^{\infty} \frac{1}{8}T_n \delta(t-n-mN)\right]. \tag{E-26}$$

In order to take the Fourier transform of $\phi_{stm3}(t)$ it is written as

$$\phi_{stm3}(t) = \phi_{stm3a}(t) * \sum_{n=0}^{N-1} \left(\phi_{stm3b}(t)\right), \qquad \text{(E-27)}$$

where

$$\phi_{stm3a}(t) = U(t) - U(t-1), \text{ and} \qquad \phi_{stm3b}(t) = \sum_{m=-\infty}^{\infty} \frac{1}{8} T_n \delta(t-n-mN),$$

and the Fourier transforms of the terms $\phi_{stm3a}(t)$ and $\phi_{stm3b}(t)$ are taken separately.

The first term in the expansion of $\phi_{stm3}(t)$ is

$$\phi_{stm3a}(t) = U(t) - U(t-1). \qquad \text{(E-28)}$$

From Appendix B.ii, the Fourier transform of this is

$$\Phi_{stm3a}(f) = e^{-j\pi f} \frac{\sin(\pi f)}{\pi f}. \qquad \text{(E-29)}$$

The second term in the expansion of $\phi_{stm3}(t)$ is

$$\phi_{stm3b}(t) = \sum_{m=-\infty}^{\infty} \frac{1}{8} T_n \delta(t-n-mN). \qquad \text{(E-30)}$$

From the results of Appendix E.ii, the Fourier transform of this term is

$$\Phi_{stm3b}(f) = \frac{T_n}{8N} \sum_{m=-\infty}^{\infty} e^{-j2\pi nm/N} \, \delta\left(f - \frac{m}{N}\right). \qquad \text{(E-31)}$$

The Fourier transform of $\phi_{stm3}(t)$ can be found using some of the properties of Fourier transforms. Convolution in the time domain is replaced by multiplication in the frequency domain. This produces the result

$$\Phi_{stm3}(f) = \Phi_{stm3a}(f) \cdot \sum_{n=0}^{N-1} \left(\Phi_{stm3b}(f)\right). \qquad \text{(E-32)}$$

Applying this relationship to Eqns. E-29 and E-31, the Fourier transform of $\phi_{stm3}(t)$ is found after some simplification to be

$$\Phi_{stm3}(f) = e^{-j\pi z}\,\frac{\sin(\pi f)}{\pi f}\sum_{m=-\infty}^{\infty} C_m \delta\left(f-\frac{m}{N}\right), \qquad \text{(E-33)}$$

where

$$C_m = \frac{1}{8N}\sum_{n=0}^{N-1} e^{-j2\pi mn/N}.$$

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