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Non-linear behavioural modelling of device-level transients for complex power electronic converter circuit hardware realisation on FPGA

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Abstract: Detailed device-level models of the insulated-gate-bipolar-transistor (IGBT) and diode are essential for power converter design evaluation for providing insight into circuit and device behaviours, as well as to shorten the design cycle and reduce costs. In this study, the non-linear behavioural models of IGBT and power diode are utilised for emulating the modular multilevel converter (MMC) on the field programmable gate array. For digital hardware-in-the-loop (HIL) emulation, these time-domain continuous models are discretised and linearised prior to being designed into the corresponding hardware modules using the hardware description language VHDL that features a fully paralleled and pipelined implementation. A circuit partitioning approach is adopted according to the MMC structure to enhance computation efficiency and then, detailed information from the system-level performance to the specific features of individual switches is available. HIL emulation and the subsequent comparison with results from the commercial off-line simulation tools prove that the complex IGBT and diode models can be involved in the efficient simulation of large-scale power converters.

1 Introduction

Detailed physics-based analytical device-level models for IGBTs are available in the literature, which are among the most prevalent models [1, 2]. Highly exact numerical models based on finite-element methods [3] and hybrid models [4] combining the analytical and numerical concepts also exist. Nevertheless, all these insulated-gate-bipolar-transistor (IGBT) models are seldom used for time-domain simulation of power converters even though high accuracy is preferred and demanded [5, 6] since they involve many non-linear physical phenomena and employing them would contribute to very long computational time even with a few devices, at a moderate switching frequency, and for a fraction of the simulation interval [7]. On the other hand, parameter exaction is not instantly feasible, even for the lumped-charge model [8] that is simpler than the Hefner model; an experimental set-up is still required. The situation is similar in power diode modelling where the aforementioned methods are also adopted [9–11].

Behavioural models reveal the necessary device static and dynamic characteristics in circuit simulation while omitting excessive device physics. Therefore, they gain computational advantages over the aforementioned models and are better in accuracy and details than system-level models such as the ideal model and the averaged value model. There are a number of variants, e.g. the macro-model [12], the Hammerstein configuration [13], all of which have an order >5. A considerably simpler first-order model was proposed in [14]; however, custom experiments and curve-fitting were used for parameter determination. An improved behavioural model was presented in [15] to accurately capture the device behaviour, and the data-sheet-driven feature that exempts itself from acquiring a long list of inaccessible device-correlated parameters as in the analytical or numerical models makes it more applicable.

FPGAs have been successfully deployed for detailed modelling of complex power system equipment [16–20]. While the hardware emulation of power converters mainly aims at validating functions of the converter and its control strategies, non-linear IGBT and diode models were rarely included due to their complexity even though they have long been in existence. On the contrary, simpler switch models prevail. The two-node model having a resistance in parallel to a current source [21] showed its effectiveness in two-level voltage sourced converters. Also, the ideal switch model claimed dominance in various circuit simulation occasions. Nevertheless, those IGBT and diode models merely reflect the on- and off-state characteristics and are incapable of providing further details for converter evaluation. Typical switching transients were recorded in a curve-fitting based linear switch model [22] and the look-up table (LUT) method [23]. The accuracy of the former was compromised due to the omission of non-linearities, and they both lack versatility as the waveform shapes stored in the field programmable gate array (FPGA) ROM cannot change along with the electromagnetic environment, typically the gate driver circuit conditions, underlining the importance of adaptive models.

The purpose of this study is to propose FPGA-based hardware emulation of power converters containing non-linear behavioural switch models, which are first derived by discretisation and linearisation. Then, parallelism is featured in the process of hardware design by VHDL under Xilinx® Vivado®. Furthermore, the detailed device-level models are applied to a modular multilevel converter (MMC) for medium-voltage direct-current (MVDC) system hardware emulation to testify that the complex switch models can be used in large circuit occasions which off-line simulation tools could hardly achieve.

The paper is organised as follows: Section 2 elaborates device-level behavioural modelling of the power diode and IGBT and their hardware design. The methodology for efficient power converter emulation on FPGA is narrated in Section 3. Section 4 presents comparison and analysis of hardware-in-the-loop (HIL) emulation results, and Section 5 provides the conclusions.

2 Non-linear behavioural device model

2.1 Power diode non-linear behavioural model

The power diode is simplified with only static features and the reverse recovery dynamics preserved while other negligible components in the original full behavioural model [24] are omitted, as shown in Fig. 1*a*.

2.1.1 Model description: The diode static characteristics represented by the symbol *NLD* reflects an exponential relationship

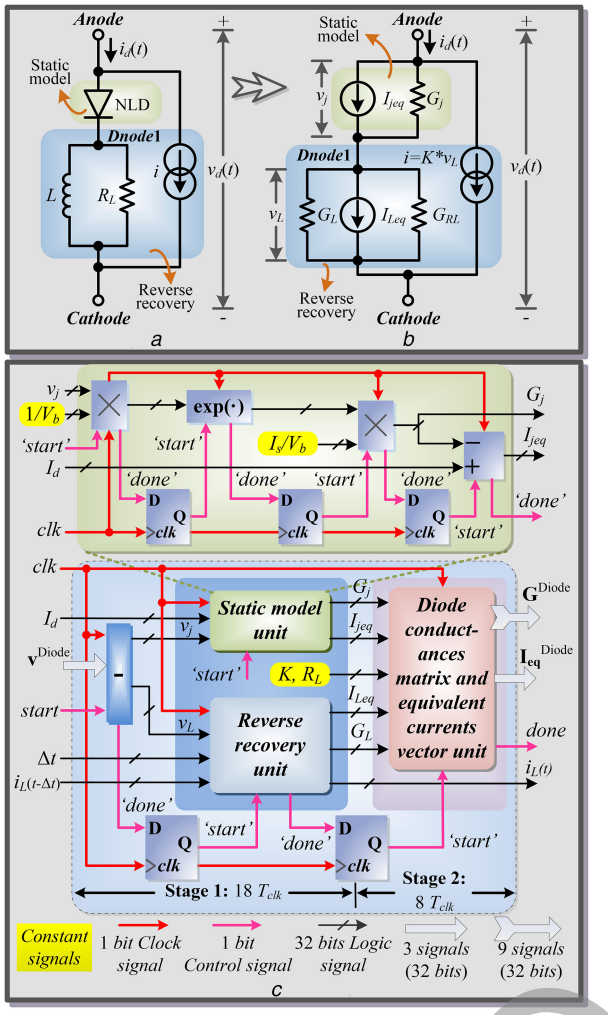

Fig. 1 *Power diode model for HIL emulation*
(a) Simplified power diode model, ***(b)*** Linearised discrete-time equivalent circuit, ***(c)*** Architecture of hardware module

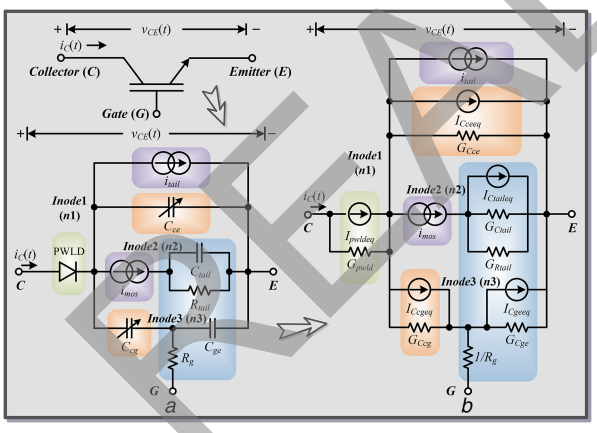

Fig. 2 *IGBT EMT model*
(a) IGBT non-linear continuous-time behavioural model, ***(b)*** Linearised discrete-time equivalent circuit

between the static current I_d and the junction voltage V_j, as expressed by

$$I_d = I_s(e^{(V_j/V_b)} - 1), \tag{1}$$

where I_s is the leakage current and V_b the junction barrier potential. Its discrete-time Norton equivalent circuit, which is shown in Fig. 1*b*, becomes available by taking the partial derivative and subsequent linearisation, as expressed by

$$G_j = \frac{\partial I_d}{\partial V_j} = \frac{I_s}{V_b} e^{(V_j/V_b)}, \tag{2}$$

$$I_{jeq} = I_d - G_j \cdot V_j, \tag{3}$$

respectively, where G_j and I_{jeq} are the conductance and equivalent current contribution of *NLD*.

The reverse recovery phenomenon is attained by the $R_L - L$ pair and the voltage controlled current source with a coefficient of K. Backward Euler integration is adopted due to its lower latency in hardware implementation compared with other integration methods. The Norton equivalent circuit of the linear inductor L is derived by the following equations:

$$G_L = \frac{L}{\Delta t}, \tag{4}$$

$$I_{Leq}(t) = i_L(t - \Delta t), \tag{5}$$

where Δt is the simulation time-step and the iterative inductor current $i_L(t)$ takes the form of

$$i_L(t) = I_{Leq}(t) + G_L \cdot v_L(t). \tag{6}$$

Hence, the matrix equation of the simplified diode model is

$$\boldsymbol{G}^{\text{Diode}} \cdot \boldsymbol{v}^{\text{Diode}} = \boldsymbol{I}_{\text{eq}}^{\text{Diode}}, \tag{7}$$

where the 3×3 admittance matrix is given by

$$\boldsymbol{G}^{\text{Diode}} = \begin{bmatrix} G_j & K - G_j & -K \\ -G_j & G_j + G_L + G_{RL} & -G_L - G_{RL} \\ 0 & -G_L - G_{RL} - K & G_L + G_{RL} + K \end{bmatrix}, \tag{8}$$

$\boldsymbol{v}^{\text{Diode}}$ is a vector of diode nodal voltages, and the equivalent current source contribution vector is

$$\boldsymbol{I}_{\text{eq}}^{\text{Diode}} = [-I_{jeq}, \quad I_{jeq} - I_{Leq}, \quad I_{Leq}]^{\text{T}}. \tag{9}$$

2.1.2 Hardware architecture design: The hardware design conforms to the parallelism and pipelined structure. Fig. 1*c* shows the architecture of the proposed simplified diode hardware module which is composed of four subunits with each enclosing a controllable *start* input port and a *done* signal output port. The structure of the static model unit is taken for instance to illustrate the way mathematical models are being materialised as hardware modules by algebraic operators and registers on the FPGA. For the entire diode module, once the outer *start* command is received by the subtracter, at *Stage 1* voltages of internal components are first calculated, followed by the concurrent calculation of the static model and reverse recovery unit. Then, formations of the diode's admittance matrix and current contribution vector begin simultaneously at *Stage 2*. This strictly organised execution sequence is realised by two-dimensional flip-flops, which, as part of the finite state machine, translate the internal *done* signals to *start* orders in one clock cycle for subsequent hardware modules.

2.2 IGBT non-linear behavioural model

2.2.1 Model description: The IGBT behavioural model is shown in Fig. 2*a*, where PWLD denotes a piecewise linear diode, R_g is the resistance to the gate, and elements such as voltage controlled current sources i_{mos} and i_{tail} as well as inter-electrode capacitors C_{ce} and C_{cg} are non-linear.

The basic operation can be summarised as when the collector-emitter voltage v_{CE} is less than the threshold voltage V_{on}, PWLD remains off and the collector current i_C is zero; when the value of v_{CE} is between V_{on} and the saturation voltage V_{sat}, the device is represented by i_{mos} in the quasi-linear region; then, when v_{CE} is

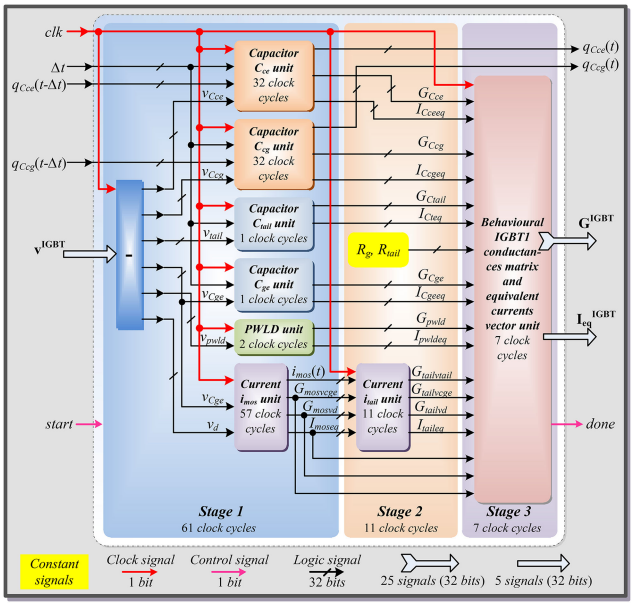

Fig. 3 *Hardware architecture of IGBT non-linear behavioural model*

greater than V_{sat}, i_C will mainly depend on the gate-emitter voltage v_{ge} and v_{ce} [15]. The tail current i_{tail}, which is controlled by the internal parallel $R_{tail} - C_{tail}$ pair, only emerges during the turn-off process. Using the IGBT tool in SaberRD®, the static and dynamic parameters can be determined based on the corresponding characteristics and curves provided by the device data-sheet [25].

The *PWLD* can be deemed as a binary conductor whose on- and off-state conductances are g_{on} and g_{off}, respectively. Thus, its Norton equivalent model for electromagnetic transient (EMT) simulation is

$$G_{pwld} = \begin{cases} g_{on} & (v_{pn} > V_{on}), \\ g_{off} & (v_{pn} \le V_{on}), \end{cases} \tag{10}$$

$$I_{pwldeq} = -G_{pwld} \cdot V_{on}, \tag{11}$$

where v_{pn} is the voltage across PWLD, V_{on} is its forward threshold voltage.

Using a similar procedure illustrated in the diode section, all internal components can be turned into their EMT models, and the outcome is shown in Fig. 2*b*, in which linearly passive elements are calculated by

$$G_{Cx} = \frac{C_x}{\Delta t}, \tag{12}$$

$$I_{Cxeq} = -G_{Cx} \cdot v_{Cx}(t - \Delta t), \tag{13}$$

where C_x is referred to either C_{tail} or C_{ge}. With regard to non-linear capacitors C_{ce} and C_{cg}, they are treated in the same fashion as taking C_{cg} for example

$$G_{Ccg} = \begin{cases} \dfrac{\left(ccgo\left(1 + (v_{Ccg}/vcgo)\right)^{-M}\right)}{\Delta t} & (v_{Ccg} > 0), \\ \dfrac{ccgo}{\Delta t} & (v_{Ccg} \le 0), \end{cases} \tag{14}$$

$$i_{Ccgeq} = \frac{q_{Ccg}(t) - q_{Ccg}(t - \Delta t)}{\Delta t} - G_{Ccg} \cdot v_{Ccg}(t), \tag{15}$$

where M is the Miller capacitance exponent coefficient that affects the current rise and fall time.

Since i_{mos} and i_{tail} are dependent on voltages over other components, their EMT models are taken as a combination of equivalent current sources and conductance or transconductance. The voltage controlled current source i_{mos} reflecting the turn-on and -off behaviours is the most complicated component, as expressed by

$$i_{mos} = \begin{cases} 0, & (v_{Cge} < V_t) \,||\, (v_d \le 0) \\ a_2 \cdot v_d^{(z+1)} - b_2 \cdot v_d^{(z+2)}, & v_d < (y(v_{Cge} - V_t))^{(1/x)}, \\ \dfrac{(v_{Cge} - V_t)^2}{a_1 + b_1 \cdot (v_{Cge} - V_t)}, & (\text{others}), \end{cases} \tag{16}$$

where a_1, b_1, a_2, b_2, x, y, and z are internal parameters, V_t is the channel threshold voltage, and v_d the potential difference between *Inode*1 and *Inode*2. It indicates that i_{mos} can branch off conductance G_{mosvd} and transconductance $G_{mosvcge}$ derived by taking partial derivatives with respect to v_d and v_{Cge}, i.e. $(\partial i_{mos}/\partial v_d)$ and $(\partial i_{mos}/\partial v_{Cge})$.

Thus, its equivalent current I_{moseq} takes the form of

$$I_{moseq} = i_{mos} - G_{mosvd} \cdot v_d - G_{mosvcge} \cdot v_{Cge}. \tag{17}$$

Similarly, the equivalent current contribution from the i_{tail} unit can also be found as an expression of transconductance

$$I_{taileq} = i_{tail} - G_{tailvd} v_d - G_{tailvcge} v_{Cge} - G_{tailvtail} v_{tail}, \tag{18}$$

A 5×5 admittance matrix $\boldsymbol{G}^{IGBT}$ and current source contribution vector $\boldsymbol{I}_{eq}^{IGBT}$ can be constructed according to the discrete model, and the IGBT nodal voltage vector $\boldsymbol{v}^{IGBT}$ is obtained by

$$\boldsymbol{v}^{IGBT} = \left(\boldsymbol{G}^{IGBT}\right)^{-1} \cdot \boldsymbol{I}_{eq}^{IGBT}, \tag{19}$$

2.2.2 Hardware architecture design: As shown in Fig. 3 where all subunits are horizontally scaled with respect to latency, the overall process is completed within three stages. At the first stage are the simultaneous start and implementation of the six independent subunits. *Stage 2* which commences only when *Stage 1* is completed is set up particularly for i_{tail}, since it has a sequential relationship with i_{mos}. At the last stage, all calculated conductances and current contributions are grouped according to their positions to form $\boldsymbol{G}^{IGBT}$ and $\boldsymbol{I}_{eq}^{IGBT}$. Then, the *done* signal indicating the completion of one cycle is issued and the IGBT module remains idle until a new start order arrives.

To sum up, the total latency is about 79 clock cycles according to its critical path. Circuit nodal voltages are the inputs to the IGBT hardware module, and so are two history signals $q_{Cce}(t - \Delta t)$ and $q_{Ccg}(t - \Delta t)$. After the Newton–Raphson (N–R) iteration converges in the current time interval, $q_{Cce}(t)$, $q_{Ccg}(t)$ can be correctly calculated and all history values should be updated for the next time-step.

3 Power converter HIL emulation

Device-level IGBT and diode models are commonly seen in the simulation of simple power converters. However, they are rarely involved in large-scale circuits due to low computational efficiency and numerical divergence. Therefore, the HIL emulation of the MMC is carried out as an instance on the Xilinx® Virtex®-7 VC707 XC7VX485T FPGA platform. Table 1 lists the FPGA resource utilisation of the designed IGBT and diode hardware modules, respectively.

Fig. 4*a* shows the topology of a three-phase MMC, and Fig. 4*b* shows the structure of a sub-module (SM) consisting of one direct current (DC) capacitor and two switches S_1 and S_2, each of which may consist of a number of identical IGBTs and diodes in parallel to enhance the current capacity. The instant consequence is a dramatic rise in the number of nodes which leads to inefficient EMT simulation. However, that numerical solution always yields a wanted well-balanced condition meaning that all the corresponding nodes can be deemed as connected and consequently, the total node

Table 1 FPGA resource utilisation of IGBT and diode hardware modules

Resources	IGBT	Diode	Total available
LUT	29,064 (9.57%)	5555 (1.83%)	303,600
LUTRAM	168 (0.13%)	20 (0.02%)	130,800
FF	21,070 (3.47%)	4722 (0.78%)	607,200
BRAM	6.50 (0.63%)	2.50 (0.24%)	1030
DSP48	518 (18.5%)	100 (3.57%)	2800
I/O	98 (14.0%)	98 (14.0%)	700
BUFG	1 (3.12%)	1 (3.12%)	32

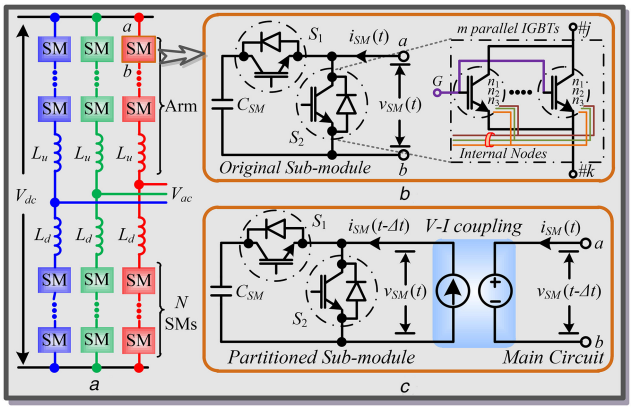

Fig. 4 *MMC SM architecture*
(a) Configuration of an MMC, ***(b)*** SM with behavioural switch models, ***(c)*** Partitioned SM

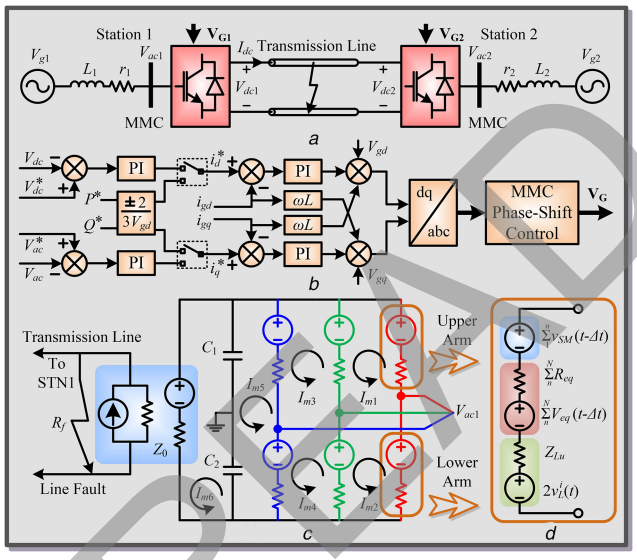

Fig. 5 *MMC-based MVDC system*
(a) System configuration, ***(b)*** Station control scheme, ***(c)*** EMT model of MMC, ***(d)*** Equivalent circuit for an arm

number remains the same, as demonstrated by the IGBT in Fig. 4*b*. All terminal nodes tagged as j and k, as well as three internal nodes abbreviated by $n_{1,2,3}$, are connected. Thus, for m parallel IGBTs, their equivalent admittance and current matrices are simply multiplied by that coefficient, i.e. $m \cdot G^{\text{IGBT}}$ and $m \cdot I_{\text{eq}}^{\text{IGBT}}$, and the matrix equation for the IGBT portion is established as

$$\left(m\boldsymbol{G}^{\text{IGBT}} + \begin{bmatrix} G_{j1} & \cdots & 0 \\ 0 & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & G_{k5} \end{bmatrix} \right) \boldsymbol{U} = m\boldsymbol{I}_{\text{eq}}^{\text{IGBT}} + \begin{bmatrix} J_{\text{eq1}} \\ 0 \\ 0 \\ 0 \\ J_{\text{eq5}} \end{bmatrix}, \tag{20}$$

where G_{j1}, G_{k5}, J_{eq1}, and J_{eq5} are conductances and current contributions from the external circuit. The benefits are the hardware resource requirement for m parallel switches is the same to a single switch, and the computational time is greatly shortened compared with solving each device individually.

Meanwhile, the many SMs connecting to each other also introduce plenty of meshes and nodes, making the direct computation of the converter still impractical. One solution is illustrated in Fig. 4*c*, where a coupled voltage–current source pair is inserted between each SM and the remaining circuit – named as the *main circuit* – so that a group of independent sub-circuits can be constructed [26]. Therefore, the original large admittance matrix for the MMC is split into a number of smaller matrices and parallel computation can be achieved on the FPGA to accelerate HIL emulation.

The difference between the original SM and its partitioned counterpart lies in that for the latter, a unit mismatch on both sides of the $V-I$ coupling is introduced. Nevertheless, it has a negligible impact on the accuracy of simulation due to the fact that the change of i_{SM} in one time-step is so small that can be deemed constant. For a single phase $(N+1)$-level MMC, $2N$ sub-circuits and one main circuit will be formed, which are computed in parallel. The main circuit can be solved by a single calculation since non-linearities are excluded after partitioning, and the SM is decisive on the latency of the hardware design since it is more sophisticated. Therefore, the speed remains the same even though only one SM contains behavioural models while others employ ideal switches considering that the FPGA board has limited resources. Once the N–R iteration converges, this SM exchanges information with the main circuit for the next time step.

A two-terminal MVDC system is configured in Fig. 5*a*. The specific parameters of the system are listed in the Appendix and the control strategy is carried out in the d–q frame, as shown in Fig. 5*b*. Station 1 is in charge of power flow regulation, while Station 2 controls DC voltage. The driving pulses denoted by vector $\boldsymbol{V}_{\text{G}}$ are produced in the MMC controller, whose corresponding hardware module designed with Vivado HLS® has a latency of 116 clock cycles if the phase-shift strategy [27] is adopted. The EMT model of Station 2 is shown in Fig. 5*c*, where all MMC arms are merged and represented by one voltage source and one resistor. The equivalent circuit of an arm is shown in Fig. 5*d*, which assumes an arbitrary number of partitioned SMs containing non-linear behavioural models, whose coupling on the arm side is merged. Meanwhile, for an ideal SM, it can be simplified as [28]

$$R_{\text{eq}} = \frac{R_1 R_2 + R_2 Z_{\text{CSM}}}{R_1 + R_2 + Z_{\text{CSM}}}, \tag{21}$$

$$V_{\text{eq}}(t-\Delta t) = \frac{R_2 V_{\text{CSM}}(t-\Delta t)}{R_1 + R_2 + Z_{\text{CSM}}}, \tag{22}$$

where Z_{CSM} is the equivalent resistance of the SM capacitor, and V_{CSM} is the voltage contribution in its EMT model. Therefore, the remaining ideal SMs can also be added together. Z_{Lu} and v_{L}^{i} represents the transmission line stub model [29] of an arm inductor so that a Thévenin equivalent circuit based main circuit can be constructed. The transmission line can be replaced by its hybrid Thévenin–Norton equivalent model, which brings one benefit to system solution, i.e. the two converters can be calculated independently as they are physically separated but electrically linked. Thus, as denoted by currents I_{m1-6}, a three-phase converter contains only six meshes.

In Fig. 6, the iterative HIL emulation process of the MMC SM containing non-linear behavioural IGBT and diode models is depicted. It should be noted that the V–I coupling module is designed specifically for the converter part with circuit partitioning.

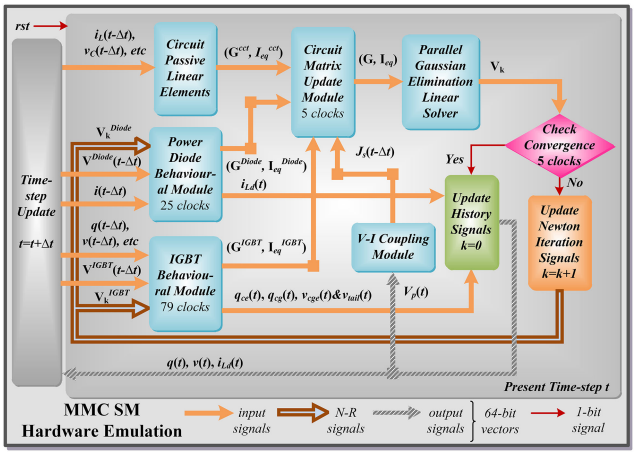

Fig. 6 *Hardware architecture and its signal flow routes for the MMC SM with non-linear behavioural switch models*

Table 2 Simulation execution times from EMT simulators and HIL systems

		Execution time, s			
Tool	m	Diode	IGBT	5L-MMC	11L-MMC
SaberRD®	$m_1 = 1$	2.96	4.2	340	715
	$m_2 = 2$	4.15	6.5	528	1060
	$m_3 = 3$	5.10	8.6	620	1430
PSCAD/EMTDC®	1	0.3	0.3	4.5	17.5
HIL system	$m_{1,2,3}$	0.68	2.2	5.2	5.2
Speed-up SP1	$m_1/m_2/m_3$	4.3/6.1/7.5	1.9/2.9/3.9	65/101/119	137/204/275
Speed-up SP2	$m_{1,2,3}$	0.44	0.13	0.87	3.37

4 HIL emulation results and validation

To showcase the versatility of non-linear behavioural models, HIL emulation results from the device level to the system level captured by the Tektronix DPO 7054 Digital Phosphor Oscilloscope are validated by off-line simulation tools running under 64-bit Windows® 7 Enterprise SP1 operating system with 3.40 GHz Intel® Core™ i7 CPU and 8.00 GB RAM. The employed IGBT and power diode models have been experimentally verified and are available in SaberRD® [30], as also listed in the Appendix.

4.1 Islanded MMC performance

The MMC topology in Fig. 4*a* is used as an inverter with DC link voltage $V_{dc} = 3$ kV and alternating current (AC) side inductive load $5\,\Omega - 6$ mH for demonstrating the performance of non-linear behavioural IGBT and diode models. In the device-level simulation, the selection of a switch type should consider the device's capacity. The BSM300GA160D IGBT (1600 V/400 A) [31] is suitable for this DC voltage rating and thus is chosen. The frequencies of switches and AC output are 2.0 kHz and 60 Hz, respectively.

Due to the non-linearities in a SM, a minimum of five N–R iterations are needed for convergent results, and each iteration has a latency of 209 clock cycles. The HIL emulation time-step is set as 200 ns and FPGA clock frequency is 100 MHz. Table 2 summarises the time some EMT simulators and the HIL system need to conduct the computation of a number of circuits for a 100 ms period. To achieve high fidelity, multiple switches are considered. The time SaberRD® needs to complete simulation of simple circuits, e.g. a single diode and IGBT, is acceptable, and the hardware speedup is medium. However, it rises dramatically along with the circuit scale and the number of parallel switches. Thus, the speed-up SP1 for a three-phase five-level MMC is 65 times while it reaches 275 for 11-level MMC. Meanwhile, the HIL system has a similar, or even faster simulation speed than PSCAD/EMTDC® in single three-phase MMC cases even though the time-step in the latter tool is 20 μs. Thus, it can be inferred that with higher voltage levels, more converters, or parallel devices, the speed-up becomes more significant because the MMC latency remains the same.

The oscilloscope results in Figs. 7*a–c* show starting of the five-level MMC. Slightly irregular in the first two cycles, the output voltage later stabilises with an evident level of 5. DC capacitor overcharge is observed in all SMs, with those in the lower arm having larger amplitudes to around 1200 V, but finally, all of them manage to maintain around 750 V, as shown in Fig. 7*b*, indicating proper functioning of the controller. Fig. 7*c* shows two arm currents, the opposite phase relation explains the SM capacitor voltages in the upper and lower arms reaching their peaks alternately. Moreover, a momentary current surge at the beginning explains the overcharge in DC capacitors. The impact of the number of behavioural SMs in an MMC is also tested by setting all of them non-linear, and the results are given in the middle, which are verified by SaberRD® using the same configuration in the bottom. The ideal switch model leads to some minor differences in the output voltage around the third cycle; other than that, its outcomes are virtually the same to the other two rows, indicating that the proposed MMC arm structure has a high fidelity.

From the perspective of a real converter design, switching dead-time is always set to protect switches in a SM, and the gate driver circuit also affects their safe operation. Fig. 8*a* shows the turn-on waveforms of an IGBT without dead-time, and a gate voltage $V_G = +15\,V/0\,V$ exerted on the device via a gate resistance of $10\,\Omega$. A collector current surge up to over 1200 A appears due to the overlapped conduction of the two complementary switches and consequently, the energy stored in the DC capacitor discharges dramatically through that path. To avoid the hazardous current which may damage the switches, as well as to demonstrate the versatility of the behavioural model, different gate driving conditions are set. As depicted in Figs. 8*b* and *c*, the current surge, caused by diode reverse recovery, witnesses a remarkable mitigation to about two times the amplitude of the steady-state current by simply setting a sufficient dead-time to 5 μs. Reducing the off-state gate voltage V_G^{off} would lose the requirement on dead-time, as shown in Figs. 8*d* and *e*. By setting a 2 μs dead-time and $V_G^{off} = 0$, a current surge up to 1000 A can still be observed. In

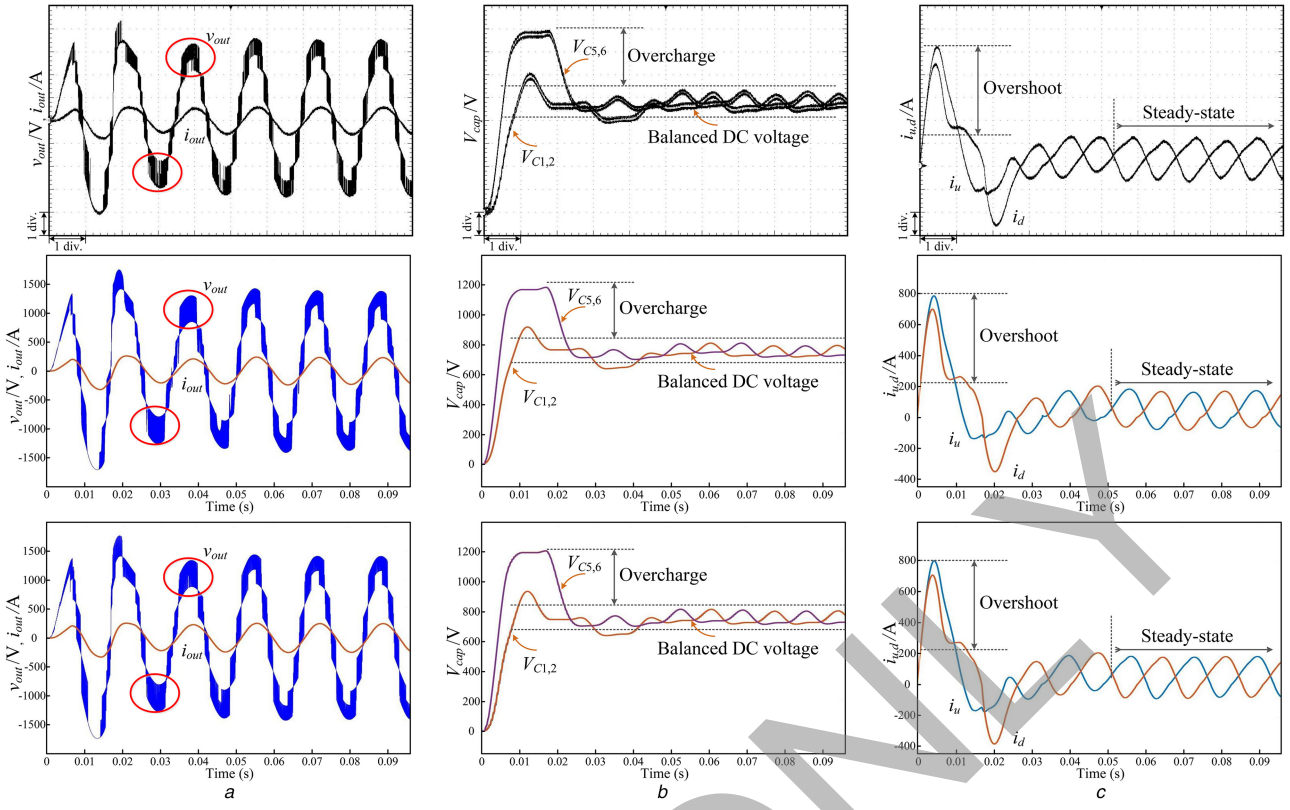

Fig. 7 *System-level performance of MMC with non-linear behavioural models from proposed models (top, middle) and SaberRD® simulation (bottom). Oscilloscope y-axis: (a) 396 V(A)/div., (b) 155 V/div., (c) 155 A/div.; x-axis: 50 ms/div*
(a) Output voltage, ***(b)*** Capacitor voltages, ***(c)*** Arm currents

contrast, it disappears when $V_G^{off} = -10\,V$. Fig. 8*f* shows the overview of switching waveforms of the upper and lower IGBT-diode pairs in a SM. During Stage 1, the arm current is positive and consequently, the upper diode conducts to charge the DC capacitor, as can be noticed from the rising envelopes of v_{CE1} and v_{CE2}. Reverse recovery accompanies the diode operation, and correspondingly, current overshoot is induced to the lower IGBT. At Stage 2, the arm current becomes negative so the upper IGBT is ordered to turn on repeatedly, and the lower diode acts in concert to discharge energy stored in the DC capacitor. These device-level results prove that the non-linear behavioural model has a high versatility to variations of electromagnetic environment since its switching waveforms can change accordingly along with external circuits without any adjustment on its parameters once they are obtained; on the contrary, the ideal switch model and the averaged value model do not exhibit transients. It is also impractical to enable the curve-fitting model to have that capability because potentially there could be numerous switching cases, and selection of an appropriate case is difficult. Moreover, it is also restricted by the availability of hardware resources when implemented on the FPGA.

In Table 3, some static and dynamic features of IGBT and diode models are validated by SaberRD® simulation. It shows that the reverse recovery time of diode lasts up to 2 μs, much longer than IGBT's turn-on and -off period, which are around 200 and 640 ns, respectively. The conduction power loss distinguished by subscript "cond" is measured at a collector current of 300 A. The error with respect to SaberRD® is negligible because essentially, it is a comparison of the static *I–V* characteristics, which is easy to model. The transient power dissipation covers the overall switching period, i.e. from the time prior to the process to the switch's re-entry into steady-state. Thus, the power loss is calculated by the consumed energy E_{Tr} over T_{Tr} – the duration of switching period

$$P_{Tr} = \frac{E_{Tr}}{T_{Tr}} = \frac{1}{T_{Tr}} \int_0^{T_{Tr}} (v \cdot i)\, dt, \tag{23}$$

In HIL emulation, the forward Euler integration method is applied to the above equation, leading to

$$P_{Tr} = \frac{\sum_{i=1}^{N_{Tr}} (v_i \cdot i_i \Delta t)}{T_{Tr}}, \tag{24}$$

where the entire duration T_{Tr} is divided into $N_{Tr} = T_{Tr}/\Delta t$ intervals. Though the mathematical model for the switching transients is more complex, the power loss from HIL emulation is still precise, with diode reverse recovery power dissipation having the largest error of 5.4% and IGBT turn-off loss next to it, at 3.4%. Moreover, the numerical results explicitly illustrate that transient power losses are much higher, underlining the importance of device-level non-linear switch models for evaluation of the safe operation of a converter.

4.2 MMC-MVDC performance

To enable a higher DC voltage with the same five-level MMC configuration, IGBTs with a larger capacity, such as the 5SNA 2000K450300 StakPak IGBT Module (4500 V/2000 A) [32], are used in this case study. HIL emulation of a 10 kV/0.8 kA MVDC system is conducted while result validation relied on PSCAD/EMTDC® as SaberRD® was unable to simulate such a large system for a long period. In Fig. 9*a*, the system start is conducted, after a few oscillations at the beginning, the DC voltages stabilise at around 1 s, with the rectifier station slightly over 10 kV. At $t = 2$ s, pole-to-pole fault lasting 5 ms occurred at the centre of the transmission line, as Fig. 9*b* depicts, the DC voltages fall immediately, and the transmission line sees a large current, from the initial 500 A to ~1 kA. In Fig. 9*c*, power reversal is carried out. The power reference in the rectifier station is ordered to ramp down from −5 to 3 MW in a time interval of 10 s, and consequently, the DC line current I_{dc} declines from ~+500 to −300 A. Therefore, before $t_1 = 10$ s, the energy is transferred to the inverter side, and the DC voltage at rectifier station V_{dc1} is slightly higher than V_{dc2} at the inverter station to ensure energy flow. Then,

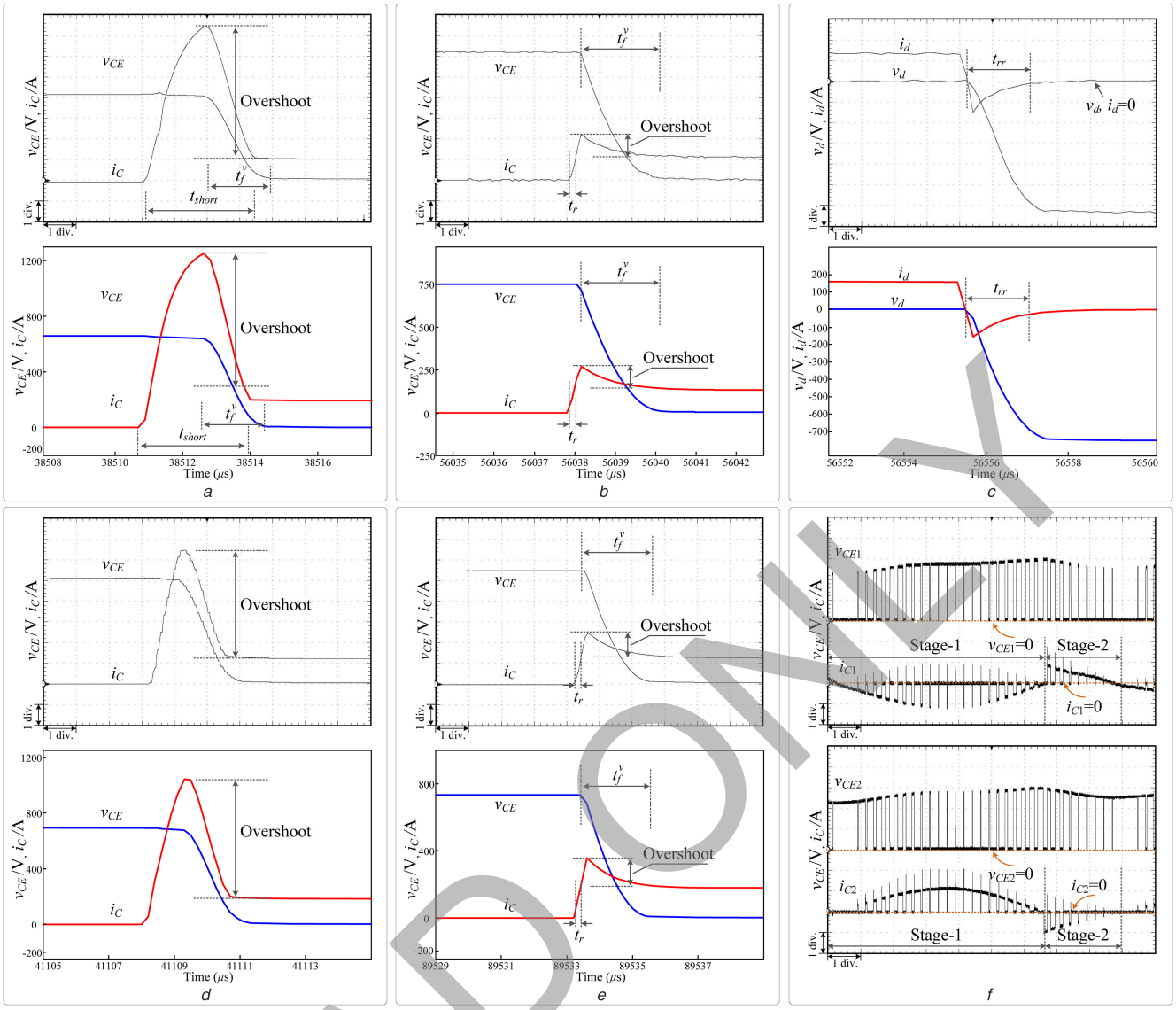

Fig. 8 *Performance of MMC with non-linear behavioural models from HIL emulation (top) and SaberRD® simulation (bottom). Oscilloscope y-axis: (a) 156 V(A)/div., (b)–(e) 130 V(A)/div., (f) 255 V(A)/div.; x-axis: (a)–(e) 5 μs/div., (f) 10 ms/div*

(a) IGBT turn-on without dead-time, ***(b)***,***(c)*** Switching transients with 5 μs dead-time, ***(d)***, ***(e)*** Switching transients with 2 μs dead-time, ***(f)*** Operation of complementary switches in a SM from HIL emulation

Table 3 Validation of IGBT and power diode non-linear behavioural models by SaberRD® simulation

	SaberRD®	FPGA	Error, %
	transient time		
t_{rr}^{Diode}	2080 ns	1970 ns	5.2
t_{r}^{IGBT}	200 ns	205 ns	2.5
t_{f}^{IGBT}	640 ns	600 ns	6.6
	power dissipation		
P_{rr}^{Diode}	3572 W	3378 W	5.4
P_{cond}^{Diode}	1117 W	1119 W	0.2
P_{r}^{IGBT}	16.53 kW	16.46 kW	0.4
P_{f}^{IGBT}	94.08 kW	90.87 kW	3.4
P_{cond}^{IGBT}	1012 W	1012 W	<0.1

I_{dc} starts ramping down, accompanied by a minor decrease of DC voltages at both terminals. At $t_2 = 20$ s, the process is ceased and noticeably, the numerical relationship between the two DC voltages has also reversed. These results prove that the decoupled hardware modules of the non-linear behavioural switch models can be effectively employed for system-level studies when the fully iterative solution provides the same results as a transient simulation tool PSCAD/EMTDC® performing a non-iterative solution using ideal switch models, particularly when an obvious speed advantage is witnessed, i.e. it takes around 752 s for the latter tool to simulate a 10 s interval with a much larger time-step of 20 μs, while the HIL system only requires 520 s even though its time-step is 100 times smaller.

5 Conclusion

This study presented the hardware emulation of device-level non-linear behavioural IGBT and power diode models, which can be applied to various power converters to obtain their precise performance for circuit design evaluation that otherwise cannot be achieved by ideal switch models. Also, compared with curve-fitting methods, the non-linear behavioural models are more versatile to electromagnetic environment variation. Meanwhile, approaches for simulating power converters containing these models are specified. Based on the circuit partitioning methodology, the hardware design is carried out. The consistency between HIL emulation results and those from off-line simulation tools indicates that the proposed non-linear behavioural IGBT and diode modules have a wide application prospect ranging from device-level behaviour evaluation to system-level performance

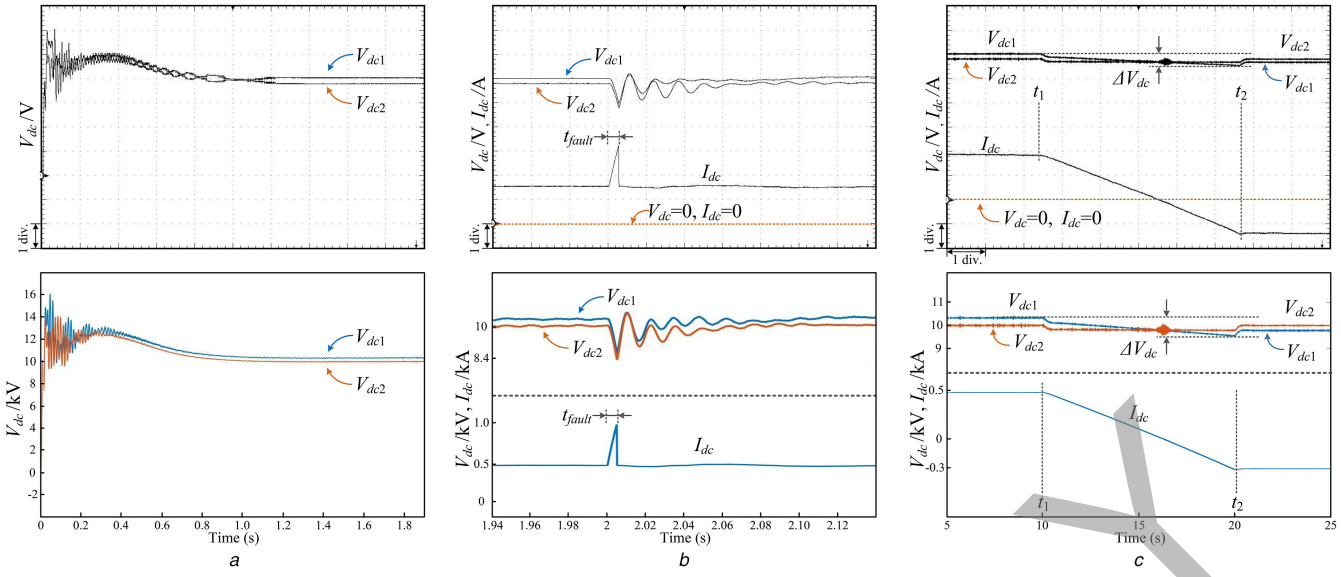

Fig. 9 *MVDC system-level performance from HIL emulation (top) and PSCAD/EMTDC® (bottom). Oscilloscope y-axis: (a) 2.58 kV/div., (b) 1.73 kV/div., 272 A/div., (c) 1.72 kV/div., 246 A/div.; x-axis: (a) 1 s/div., (b) 100 ms/div., (c) 10 s/div*

(a) System start, ***(b)*** Line-to-line fault response, ***(c)*** Power reversal

preview. Significant speed-ups are obtained over commercial device-level simulation tools, and the HIL emulation is also faster than system-level simulation tools even when the emulation time-step is much smaller.

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7 References

[1] Hefner, A.R., Diebolt, D.M.: 'An experimentally verified IGBT model implemented in the Saber circuit simulator', *IEEE Trans. Power Electron.*, 1994, **9**, (5), pp. 532–542

[2] Yang, X., Otsuki, M., Palmer, P.R.: 'Physics-based insulated-gate bipolar transistor model with input capacitance correction', *IET Power Electron.*, 2015, **8**, (3), pp. 417–427

[3] Chibante, R., Araújo, A., Carvalho, A.: 'Finite-element modeling and optimization-based parameter extraction algorithm for NPT-IGBTs', *IEEE Trans. Power Electron.*, 2009, **24**, (5), pp. 1417–1427

[4] Sheng, K., Williams, B.W., Finney, S.J.: 'A review of IGBT models', *IEEE Trans. Power Electron.*, 2000, **15**, (6), pp. 1250–1266

[5] Miyake, M., Ueno, M., Feldmann, U., *et al.*: 'Modeling of SiC IGBT turn-off behavior valid for over 5-kV circuit simulation', *IEEE Trans. Electron Dev.*, 2013, **60**, (2), pp. 622–629

[6] Rodrigues, S., Papadopoulos, A., Kontos, E., *et al.*: 'Steady-state loss model of half-bridge modular multilevel converters', *IEEE Trans. Ind. Appl.*, 2016, **52**, (3), pp. 2415–2425

[7] Wang, W., Shen, Z., Dinavahi, V.: 'Physics-based device-level power electronic circuit hardware emulation on FPGA', *IEEE Trans. Ind. Inf.*, 2014, **10**, (4), pp. 2166–2179

[8] Lauritzen, P.O., Andersen, G.K., Helsper, M.: 'A basic IGBT model with easy parameter extraction'. IEEE PESC'01, Vancouver, Canada, June 2001, pp. 2160–2165

[9] Fu, R., Grekov, A.E., Peng, K., *et al.*: 'Parameter extraction procedure for a physics-based power SiC Schottky diode model', *IEEE Trans. Ind. Appl.*, 2014, **50**, (5), pp. 3558–3568

[10] Shaker, A., Abouelatta, M., Sayah, G.T., *et al.*: 'Comprehensive physically based modelling and simulation of power diodes with parameter extraction using MATLAB', *IET Power Electron.*, 2014, **7**, (10), pp. 2464–2471

[11] Xue, P., Fu, G., Zhang, D.: 'Physics-based compact model for the EMCON p-i-n diode using Matlab and Simulink', *IET Power Electron.*, 2016, **9**, (12), pp. 2416–2424

[12] Bazzano, G., Cavallaro, D.G., Greco, G.: 'An analog behavioral thermal macro-model aimed at representing an elementary portion of a discrete IGBT power device'. THERMINIC'11, Paris, France, September 2011, pp. 1–6

[13] Hsu, J.T., Ngo, K.D.T.: 'Behavioral modeling of the IGBT using the Hammerstein configuration', *IEEE Trans. Power Electron.*, 1996, **11**, (6), pp. 746–754

[14] Tichenor, J.L., Sudhoff, S.D., Drewniak, J.L.: 'Behavioral IGBT modeling for predicting high frequency effects in motor drives', *IEEE Trans. Power Electron.*, 2000, **15**, (2), pp. 354–360

[15] Zhang, M., Courtay, A., Yang, Z.: 'An improved behavioral IGBT model and its characterization tool'. IEEE Proc. Electron Devices Meeting, Hong Kong, China, June 2000, pp. 142–145

[16] Chen, Y., Dinavahi, V.: 'Hardware emulation building blocks for large-scale real-time simulation of power grids', *IEEE Trans. Ind. Inf.*, 2014, **10**, (1), pp. 373–381

[17] Liu, J., Dinavahi, V.: 'A real-time nonlinear hysteretic transformer transient model on FPGA', *IEEE Trans. Ind. Electron.*, 2014, **61**, (7), pp. 3587–3597

[18] Tavana, N.R., Dinavahi, V.: 'A general framework for real-time simulation of electrical machines on FPGA for HIL applications', *IEEE Trans. Ind. Electron.*, 2015, **62**, (4), pp. 2041–2053

[19] Liu, J., Dinavahi, V.: 'Detailed magnetic equivalent circuit based real-time nonlinear power transformer model on FPGA for electromagnetic transient studies', *IEEE Trans. Ind. Electron.*, 2016, **63**, (2), pp. 1191–1202

[20] Tavana, N.R., Dinavahi, V.: 'Real-time nonlinear magnetic equivalent circuit model of induction machine on FPGA for hardware-in-the-loop simulation', *IEEE Trans. Energy Convers.*, 2016, **31**, (2), pp. 520–530

[21] Herrera, L., Li, C., Yao, X., *et al.*: 'FPGA-based detailed real-time simulation of power converters and electric machines for EV HIL applications', *IEEE Trans. Ind. Appl.*, 2015, **51**, (2), pp. 1702–1712

[22] Shen, Z., Dinavahi, V.: 'Real-time device-level transient electrothermal model for modular multilevel converter on FPGA', *IEEE Trans. Power Electron.*, 2016, **31**, (9), pp. 6155–6168

[23] Wong, C.: 'EMTP modeling of IGBT dynamic performance for power dissipation estimation', *IEEE Trans. Ind. Appl.*, 1997, **33**, (1), pp. 64–71

[24] Courtay, A.: 'MAST power diode and thyristor models including automatic parameter extraction'. SABER User Group Meeting, Brighton, UK, September 1995, pp. 1–10

[25] Synopsys, Inc.: 'Saber model architect tool user guide', USA, September 2009

[26] Kato, T., Inoue, K., Fukutani, T., *et al.*: 'Multirate analysis method for a power electronic system by circuit partitioning', *IEEE Trans. Power Electron.*, 2009, **24**, (12), pp. 2791–2802

[27] Hagiwara, M., Akagi, H.: 'Control and experiment of pulsewidth-modulated modular multilevel converters', *IEEE Trans. Power Electron.*, 2009, **24**, (7), pp. 1737–1746

[28] Gnanarathna, U.N., Gole, A.M., Jayasinghe, R.P.: 'Efficient modeling of modular multilevel HVDC converters (MMC) on electromagnetic transient simulation programs', *IEEE Trans. Power Deliv.*, 2011, **26**, (1), pp. 316–324

[29] Selhi, H., Christopoulos, C., Howe, A.F., *et al.*: 'The application of transmission-line modelling to the simulation of an induction motor drive', *IEEE Trans. Energy Convers.*, 1996, **11**, (2), pp. 287–297

[30] Synopsys, Inc.: 'Saber user guide', USA, September 2011

[31] 'Siemens BSM300GA160D IGBT Module'. Available at http://www.datashe-etlib.com/datasheet/839054/bsm300ga160d_siemens-semiconductor. html, accessed 26 February 2018

[32] 'ABB 5SNA 2000K450400 StakPak IGBT Module'. Available at http://new.abb.com/semiconductors/stakpak, accessed October 2016

8 Appendix

The MVDC system parameters are $V_{dc} = 10$ kV, $P_{dc} = 8$ MW, $C_{SM} = 1$ mF, $L_{u,d} = 20$ mH, $V_{g1,2} = 5.5$ kV/60 Hz, feed-in resistor $r_{1,2} = 0.4\ \Omega$, feed-in inductor $L_{1,2} = 1$ mH (Table 4).

Table 4 Behavioural IGBT and diode parameters provided by SaberRD®

Siemens® BSM300GA160D model parameters
$r_{off} = 10^9\,\Omega$, $g_{off} = 10^{-12}\,S$, $g_{on} = 10^6\,S$, $r_g = 5\,\Omega$, $vce1 = 4.8\,V$, $vge1 = 9\,V$, $ic1 = 225\,A$, $vce2 = 1.8\,V$, $vge2 = 7\,V$, $ic2 = 20\,A$, $vce3 = 4\,V$, $vge3 = 17\,V$, $ic3 = 400\,A$, $V_t = 6.3\,V$, $V_{on} = 0.8\,V$, $vce4 = 10\,V$, $vce5 = 4\,V$, $vce6 = 800\,V$, $vge4 = 10\,V$, $vge5 = 20\,V$, $itrat = 20$, $crss1 = 30\,nF$, $crss2 = 1.6\,nF$, $coss1 = 42\,nF$, $coss2 = 5\,nF$, $q1 = 400\,nC$, $q2 = 2000\,nC$, $q3 = 3500\,nC$, $\tau = 10\,\mu s$, $M = 0.5$, $R_{tail} = 1\,\mu\Omega$, $C_{tail} = 10\,F$, $a1 = 0.0217$, $a3 = 91.705$, $b1 = 0.00395$, $b3 = 3.221$, $x = 0.973$, $y = 1.428$, $z = 0.369$, $icsat3 = 1.789\,kA$, $cceo = 12\,nF$, $ccgo = 110\,nF$, $cgeo = 40\,nF$, $vceo = 0.873\,V$, $vcgo = 0.0189\,V$

ABB® 5SNA 2000K450300 StakPak IGBT model parameters
$r_{off} = 10^9\,\Omega$, $g_{off} = 10^{-12}\,S$, $g_{on} = 10^6\,S$, $r_g = 1.2\,\Omega$, $V_t = 7.71\,V$, $V_{on} = 0.43\,V$, $itrat = 4$, $a = 0.00514$, $b = 445.6\,\mu m$, $x = 1.32$, $y = 1.45$, $z = 1.04$, $ittau = 1\,\mu$, $cres0 = 30\,nF$, $cres1 = 25\,nF$, $cres2 = 4\,nF$, $coes0 = 40\,nF$, $coes1 = 32\,nF$, $coes2 = 10\,nF$, $cies0 = 40\,nF$, $M = 0.5$, $V_1 = 12\,V$, $V_2 = 20\,V$

Behavioural diode model parameters
$r_{on} = 10\,m\Omega$, $r_{off} = 100\,k\Omega$, $V_{on} = 0.7\,V$, $I_{Fo} = 10\,A$, $\frac{dI_r}{dt} = 50 \times 10^6$, $I_{rrm} = 10\,A$, $t_{rr} = 2\,\mu s$, $K = 9.883 \times 10^4$, $L = 10 \times 10^{-12}\,H$, $R_L = 1.279 \times 10^{-5}\,\Omega$