# Energy-Efficient Wireless Transceivers Powered by Radio Frequency Energy Harvesting

by

Mohammadamin Karami

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Department of Electrical and Computer Engineering
University of Alberta

# Abstract

RF energy harvesting, the process of scavenging energy from ambient electromagnetic waves, is becoming a feasible option for powering low-power electronic devices such as Internet of Things (IoT) devices, biomedical implants, and harsh environment sensors in which traditional wiring solutions or using batteries is costly or infeasible. However, RF energy density is limited because of its fast attenuation over distance and the constraints on the maximum power that can be transmitted over a channel, as set by the regularity bodies. To enable the operation of these nodes solely powered by RF energy with maximum range possible, the first part of this Ph.D work has focused on enhancing the efficiency and sensitivity of an RF Energy Harvester (RFEH) to increase the amount of the harvested energy from the available RF power. The second part is dedicated to lowering the power consumption and the required DC supply voltage of the wireless transceivers to finally arrive at a highly-sensitive RF-powered wireless transceiver.

In the first part of this dissertation, first, a systematic methodology is presented for the co-design of a matching network and a rectifier for RFEHs that results in maximum power conversion efficiency (PCE) for a given available power. This method is based on a newly developed rectifier model capable of calculating the CMOS Dickson's rectifier's input/output voltages at a given input power developed for low/high input power regimes. The proposed model allows for the co-design of the matching network and rectifier in a fraction of the time that takes for the design of a RFEH using previously developed models that rely on the knowledge of rectifier's input voltage levels, where a computationally extensive iterative design procedure must be performed be-

cause of the interdependency of the rectifier's input voltage, the input power, and the matching network's and rectifier's parameters. Second, a highly-efficient RFEH that utilizes an extra matching network to produce a passively-amplified adaptive compensation voltage is presented. The compensation voltage produced on the gate of the transistors reduces the transistors' conduction loss by increasing the gate-source voltage when transistors are on and reduces the leakage current by producing a negative gate-source voltage when the transistors are off. This is the first work that produces an adaptive compensation voltage without using active components, resulting in a significantly higher conversion efficiency if passive components of high quality are utilized.

For the second part of the dissertation, first, an ultra-low-power low-voltage wake-up transmitter (WuTx) is proposed that is capable of transmitting simultaneously the analog outputs of two sensors using short pulses that modulates their LOW and HIGH time with the analog inputs. The minimalist design of the proposed transmitter significantly reduces the overall power consumption by avoiding power-hungry data converters for sensor readout circuitry and modulation, short pulses at the output that enable the power amplifier for only a short time, during transmission along with operation in the subthreshold region. Second, to achieve the primary goal of the dissertation, a fully RF-powered wireless transceiver that integrates an efficient RFEH, a wake-up receiver (WuRx), and a wake-up transmitter (WuTx) on a single CMOS chip is introduced. The capability of the WuRx to operate without using a power management unit (PMU) enhances the sensitivity and overall conversion efficiency of the RFEH system. Utilizing an ultra-low-power ultra-low-voltage envelope detector that produces its required signal levels using passive amplification instead of an active low-noise amplifier, the transceiver's input sensitivity has been improved significantly compared to that of other previously reported RF-powered transceivers. The proposed transmitter consists of a fast start-up oscillator and an efficient class E power amplifier, which can be externally tuned for different output powers.

# Preface

I, Mohammadamin Karami, am the principal contributor to all seven chapters in this thesis. Chapter 3 of this dissertation is based on my work on the co-design of matching networks and rectifiers for optimizing the RFEH's efficiency published as publication no. 1. My supervisor, Dr. Kambiz Moez, assisted me with the formation of the concept, chip layout, measurements, and improving the manuscript quality. Chapter 4 is based on my work on increasing the efficiency of CMOS rectifiers, this same chapter was the basis of article no . 3 that has been submitted to IEEE TCAS1. The idea, chip design, layout, and measurements were done by myself. Dr. Moez provided valuable suggestions and feedback for improving the idea and manuscript quality. Chapter 5 of this work is based on the journal publicatio 2 and describes my proposed low-power wake-up transmitter. I used valuable suggestions from Dr. Moez regarding the concept, design, layout of the chip. He also assisted me in the measurement of the chip and improving the manuscript quality. Chapter 6 of this dissertation is based on article no. 4, submitted to TCAS1, and is based on my work on the design and fabrication of a completely RF-powered wireless transceiver, which is the main purpose of this thesis. The idea, chip design, layout, and measurement have been done by myself. During the process, Dr. Moez provided suggestions to the research and improving the manuscript quality.

## Journal Publications:

1. Mohammad Amin Karami and Kambiz Moez, "Systematic co-design of matching networks and rectifiers for CMOS radio frequency energy harvesters," IEEE

Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 8, pp. 3238–3251, 2019.

2. Mohammad Amin Karami and Kambiz Moez, "An ultra-low-power low-voltage WuTx with built-in analog sensing for self-powered WSN," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 7, pp. 2274–2287, 2020.

3. Mohammad Amin Karami and Kambiz Moez, "A Highly-Efficient RF Energy Harvester Using Passively-Produced Adaptive Threshold Voltage Compensation," IEEE Transactions on Circuits and Systems I: Regular Papers, (Manuscript : TCAS-I-01601-2020, submitted in Nov. 2020, 14 pages) .

4. Mohammad Amin Karami and Kambiz Moez, "An Integrated RF-powered Wireless Transceiver with -26 dBm Sensitivity," IEEE Transactions on Circuits and Systems I: Regular Papers, (Manuscript : TCAS-I-01560-2020, submitted in Nov. 2020, 12 pages).

# Table of Contents

# List of Tables

# List of Figures

# Abbreviations

**ADC** Analog-to-digital converter.

**ADS** Advanced design system.

**BAW** Bulk acoustic wave.

**CP** Charge pump.

**DAC** Digital-to-analog converter.

**DC** Direct current.

**ED** Envelope detector.

**EM** Electromagnetic.

**FCC** Federal Communication Commission.

**FPGA** Field-programmable gate array.

**FSK** Frequency-shift keying.

**IC** Integrated circuit.

**ILFD** Injection-locked frequency divider.

**ISM** Industrial, scientific, and medical.

**MIM** Metal-insulator-metal.

**OOK** On-off keying.

**OPAMP** Operational amplifier.

**PA** Power amplifier.

**PC** Personal computer.

**PCB** Printed circuit board.

**PCE** Power conversion efficiency.

**PGA** Programmable gain amplifier.

**PIL** Pulse-inject loop.

**PLL** Phase-locked loop.

**PMU** Power management unit.

**PPM** Pulse-position modulation.

**PWM** Pulse width modulation.

**QFN** Quad flat no-leads.

**RF** Radio frequency.

**RFEH** Radio-frequency energy harvesting.

**SMT** Surface mount technology.

**SMU** Source measure unit.

**SU** start-up.

**UWB** Ultra wide band.

**VCO** Voltage-Controlled Oscillator.

**VNA** Vector network analyzer.

**WPT** Wireless power transfer.

**WSN** Wireless Sensor Network.

# Chapter 1

# Introduction

## 1.1 Motivation

In many applications, such as biomedical implants, IoT and harsh environment sensors, it is costly or sometimes infeasible to power the electronic devices using traditional ways, such as wiring or using batteries. In biomedical implants, as the implant is placed inside the body, it is not practical to use wires while utilizing batteries requires follow-up surgeries for their replacements. In addition to that, in IoT applications, powering millions of nodes by traditional wiring requires a highly complex and expensive infrastructure while, on the other hand, using batteries necessitates future replacement or recharging, which is often quite impractical. Using wiring or batteries becomes impractical or very expensive if not impossible when the sensor/-transceiver is deployed in a harsh environment with high temperature and pressure.

Energy harvesting, the process of scavenging energy from the ambient environment, is a promising method to power electronic devices in the aforementioned scenarios when traditional methods cannot be used [1, 2]. The energy required for the operation of these low-power devices can be harvested from a variety of possible sources: radio frequency [3], kinetic or vibration [4], thermal [5], and solar [6]. However, systems that rely on ambient sources makes them unpredictable and uncontrollable sources of energy.

Radio frequency (RF) energy harvesting, the process of scavenging energy from am-

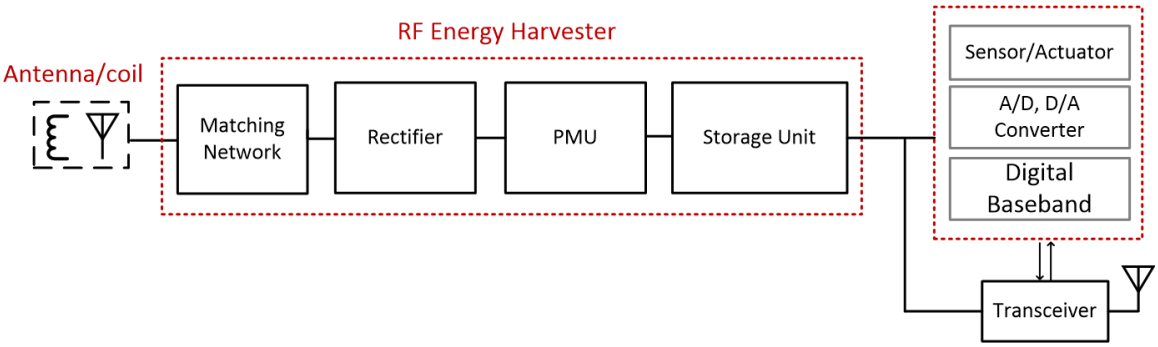



Figure 1.1: Block diagram of the general RF-powered transceiver.

bient electromagnetic waves, has been considered as one of the most viable options because of the ability to control the RF power intentionally by using a power radiator in the environment and the ability to share components of wireless transceivers and RF energy harvester to arrive at a low-cost solution. However, because of the often low-power density of RF energy, it is critically important to enhance the efficiency of the RF energy harvester (RFEH) to maximize the amount of energy harvested and minimize the power consumption of the wireless transceivers, enabling the development of self-powered/RF-powered wireless transceivers with enhanced performance.

## 1.2 RF-Powered Wireless Transceivers

The block diagram of a conventional self-powered/RF-powered transceiver is shown in Fig. 1.1. A general RF-powered transceiver is composed of an RF energy harvester, a digital baseband core, a sensor/actuator, and its interface, and finally an RF transceiver. The energy harvester, consisting of a matching network, rectifier, PMU, and a storage unit, captures the received RF energy at its antenna/coil and converts it to the DC energy required for the rest of the transceiver. The digital baseband core is responsible for communicating with the sensor/actuator interface, consisting of an Analog-to-Digital (ADC) and a Digital-to-Analog Converters (DAC), to acquire the sensor's data or activate a mechanism. In addition to that, the digital baseband core interprets the packets received by the transceiver and prepares the

data that is needed to be sent by the transceiver. The RF transceiver is responsible for managing the RF communications to the base station or other nodes. The transmission of the transceiver can be realized by an active or passive transmission. In active transmission, which is utilized mostly for relatively long distances, an antenna is required to send the RF signal. On the other hand, for short distances, the transmission can be done passively using backscattering. In backscattering, instead of using an active transmitter, the data is sent back to the base station by making a perturbation in the input impedance matching.

## 1.3 RF Energy Harvesting

As illustrated in Fig. 1.2, an RFEH consists of an antenna or coil for converting electromagnetic energy of wireless waves to electrical energy, a matching network to maximize the power transfer to the next stage, an RF-to-DC power converter (also known as RF rectifier or rectifier) to convert the RF energy into a DC source, and an energy storage element along with required power management circuitry capable of powering downstream electronic circuits. The overall efficiency of a RFEH system is defined as [7]:

$$\eta_{system} = \frac{P_{output,dc}}{P_{available,RF}} = G_A \, \Gamma \, \eta_{rec} \tag{1.1}$$

where $G_A$ is the matching network power gain, which is always lower than 0 dB due to resistive loss, $\Gamma$ is the power transfer coefficient at the interface of the matching network and the rectifier, and $\eta_{rec}$ is the rectifier's efficiency [7]. Therefore, to maximize the overall efficiency, the matching network must be designed to maximize the power transfer from the antenna/coil to the rectifier. Furthermore, the rectifier's efficiency must be maximized, usually obtained by using circuit techniques.

The required components for power transfer can be chosen based on the type of transmission and the distance between the receiver and transmitter. Based on the

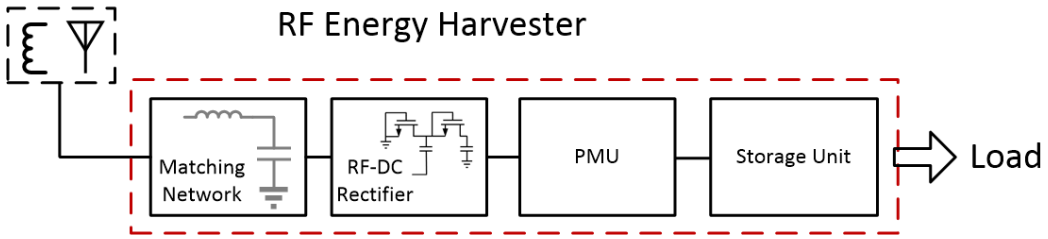



Figure 1.2: Radio Frequency Energy Harvester.

receiver and transmitter distance, RF power transfer is divided into near-field and far-field categories. In near-field transmission, energy is transferred through a magnetic or inductive link, usually realized by a coil. This method is usually used for transmitting high power densities in relatively short distances and at low RF frequencies [8–11]. On the other hand, far-field energy transfer requires a receiving antenna and is used for relatively long distances. Another important factor for transmitting power wirelessly is the operating frequency. Unlicensed portions of the frequency spectrum have been set aside for Industrial, Scientific, and Medical (ISM) purposes and is a good candidate for the operating frequency of RFEH systems as it can be used without requiring a license from regulatory bodies. As the operating frequency increases, the component sizes, including the matching network and antenna, reduce; however, the path loss increases [12]. Therefore, most of the reported far-field RFEH systems chosen the 915 MHz and 2.4 GHz ISM band frequencies as a compromise between area and path loss [7, 13–18]. In [18] quantitative research is described, and 2.4 GHz was chosen considering transmitter power consumption, tissue losses, and antenna efficiency. In this P.h.D work, 915 MHz and 2.4 GHz were also chosen as the operating frequencies.

### 1.3.1 Limitations of RFEH

Although RFEH is a promising method for powering up a wireless transceiver, the amount of the harvested energy is limited because of the low density of RF power in the environment. This is because, first, for RF power transfer, the maximum energy that can be transmitted over a frequency channel is limited by regulatory bodies such

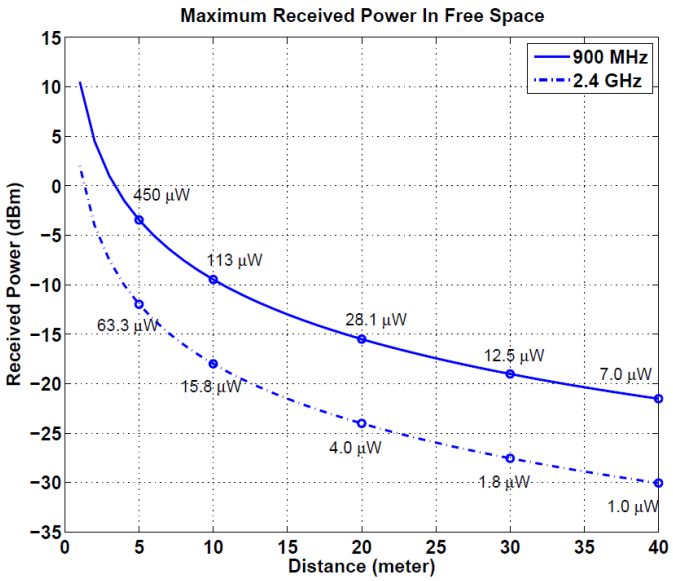



Figure 1.3: Maximum received power over distance when the transmitter power is the maximum FCC allows [12].

as the FCC [19]. Second, RF power is attenuated rapidly over the distance due to the path loss, which in free space is given by Friis' equation as [20]

$$L = (\frac{4\pi R}{\lambda})^2 \tag{1.2}$$

where $R$ is the distance between the transmitter and receiver, and $\lambda$ is the RF signal wavelength. In addition to that, the path loss increases in different environments due to multi-path fading and destructive signal interference. Fig. 1.3 shows the maximum power that can be received over various distances at different ISM band frequencies when the transmitted power is the maximum power that regulatory bodies allow with the path loss model of an office environment [12]. As can be seen, the maximum power of 28.1 $\mu W$ is received at a frequency of 900 MHz while the transmitter and receiver are 20 meters apart. However, at the same distance, 4 $\mu W$ is received at 2.4 GHz. Therefore, as the received power is limited, for achieving long powering ranges in the RF-powered transceiver, it is necessary to increase the efficiency of the RFEH so that more of the received power is converted to DC. Additionally, as will be discussed in detail in Chapter 3, at low input power levels, the output DC voltage and the

power of the RFEH will be limited and cannot be indefinitely increased by changing the topology of the RFEH such as number of stages in the rectifier. Therefore, the wireless transceiver should operate with low supply voltages and powers to be powered up by the limited received RF power.

## 1.4 Ultra-Low-Power Ultra-Low-Voltage Wireless Transceivers

The conventional receivers and transmitters consume a large amount of power and operate with the process' standard supply voltage. However, at the expense of inferior performance and speed, their power consumption and the required supply voltage can be reduced. The techniques to reduce the power consumption and supply voltage of the wireless transceiver can be categorized into system and circuit-level techniques.

### 1.4.1 System-Level Techniques

System-level approaches try to reduce the energy consumption by intermittent operation of the wireless transceivers in which the RF energy is stored for a long period of time to supply the required power for operation of wireless transceiver over a short period of time [2, 13, 18, 21]. The intermittent operation can be done by utilizing a charge and burst mechanism in which a PMU monitors the stored voltage on the capacitor/battery and activates the receiver and transmitter when the stored voltage exceeds a pre-defined level, and deactivates them when the capacitor/battery is discharged enough that it cannot operate the transceiver anymore. Furthermore, intermittent operation can be realized by using a wake-up scheme in which an ultra-low-power receiver listens to the incoming data and activates the rest of the transceiver when a pre-defined packet is detected. The wake-up receiver can be supplied using a small battery or by using RF energy harvesting. The ability to wake up the transceiver when a pre-defined packet is sent by the base station makes this scheme preferable in large-scale deployment as the transceiver is activated on-

demand, avoiding unnecessary activation of the transceiver. Inherently intermittent wireless communication systems, such as UWB modulation in which the transmitter is on in a fraction of period, can be considered as part of this category [22, 23]. By decreasing the on-time of the transmitter in communication a significant power reduction can be achieved. For shorter transmission range applications, back-scattering techniques can be utilized to reflect part of transmission energy back to the reader, obviating the need for power-hungry power amplifiers of active transmitters [16].

### 1.4.2 Circuit-Level Techniques

In order to reduce the power consumption and supply voltage of the transceiver, low-power circuit design techniques, such as operation in the subthreshold region, can be utilized [13, 24, 25]. Transistors work in the subthreshold region when their gate-source voltage is below their threshold voltage so that the supply voltage can be lower than the nominal supply voltage of the process as lower voltages are required for the operation of the transistors. Although when working in the subthreshold region, transistors require a lower supply voltage and consume lower power, their speed is reduced limiting the baseband operation speed. In addition to working in the subthreshold region, utilizing low-efficiency circuitry, such as linear regulators, must be avoided in the transceiver to use most of the harvested power just for the operation of the primary transceiver. Finally, using power-hungry circuitry, such as PLL, ADC, DAC, must be avoided. These circuits are required for complex and high-speed communications, however, their power consumption is high and their output needs a long time to settle requiring the transceiver to stay on for a long amount of time making their deployment in an intermittent scheme less appealing.

## 1.5 Thesis Overview

The objective of this dissertation is to develop a highly-sensitive RF-powered wireless transceiver by first increasing the efficiency of the RFEH and, second, decreasing the

required supply power and voltage of the transceiver. This dissertation is organized as follows:

Chapter 2 is dedicated to the literature review. The first part of Chapter 2 reviews the literature on the design of RFEHs and the existing methods for optimizing their performance for maximum power efficiency. In the second part of the chapter, the existing circuit-level techniques to increase the rectifier's efficiency are reviewed. Third, the existing techniques for reducing the power consumption of wireless transceivers are explored. Finally, previously introduced RF-powered transceivers are investigated.

Chapter 3 introduces a systematic method for the co-design of matching networks and rectifiers for RFEHs, which is a newly developed method for optimizing Dickson based RFEHs based on the input power. Dickson rectifiers are inherently non-linear because the rectifier's transistors operate in different regions during the input voltage period, which complicates the analysis of such rectifiers when RFEH is connected to a power source (antenna) via a matching network and therefore its input voltage is unknown. We present an analytical method that accurately and rapidly calculates the input resistance of the rectifier, its input voltage and output voltage based on the input power. The proposed method eliminates the need for extensive simulations that were previously done for optimizing these rectifiers. In the derived model, first, it is assumed that the matching network inductor is lossless, which although it is not realistic, provides intuition to the designers on the effect of the number of stages, the width of the transistors and the load on the efficiency. The model is further improved by considering the losses caused by the matching network inductor. The presented model can accurately calculate the rectifier properties and the matching network based on the input power. In the last part, using the developed model, contour plots of the efficiency based on the rectifier's properties are obtained. Finally, for validating the proposed model, a one-stage rectifier is fabricated in a standard 130-nm CMOS process, and measurement and simulation results are confirmed to be in good agreement validating the proposed model.

In Chapter 4, a novel technique is proposed that produces an adaptive compensation voltage for the first time without using any active components (transistors), eliminating the power consumption associated with the generation of the compensation voltage. The proposed technique produces the adaptive compensation voltage by passively amplifying the input voltages of the rectifier using a secondary matching network and feeding it to the gate of the transistors in a way that increases the transistors' $V_{gs}$, and hence their conduction current, when they are on, and reduces their leakage current when they are off by making $V_{gs}$ negative. Simulation and measurement results show that the proposed rectifier can increase the efficiency significantly compared to the conventional rectifiers for any input power level and number of rectifier's stages.

Chapter 5 presents an ultra-low-power transmitter capable of sensing and transmitting analog outputs of two sensors using PWM modulation. The transmitter consists of an ultra-low-power relaxation oscillator that its output pulse on and off time is modulated with the two analog inputs, a ring oscillator that produces the high-frequency carrier signal and upconverts the output of the relaxation oscillator to the ISM band frequency and a highly efficient class E power amplifier. The chapter describes the implementation of the transmitter and each block and the related circuit techniques that led to low power consumption. The transmitter was fabricated in a 65-nm CMOS general process and simulations and measurement results were found to be in good agreement.

In Chapter 6, an integrated RF-powered wireless transceiver consisting of an RFEH, WuRx and WuTx is proposed to complete them main goal of the thesis. The WuRx consists of an ultra-low-voltage ultra-low-power envelope detector that is made by utilizing a common source amplifier biased in subthreshold region, a low kick-back strong-Arm comparator and an ultra-low-power ring oscillator. RFEH harvests energy from the input signal to power up the WuRx while the WuRx simultaneously demodulates the input signal to baseband and waits until a pre-defined packet is re-

ceived to activate the rest of the transceiver. By removing the low-efficiency PMU, the entire generated DC output power of RFEH is used to power up the WuRx. As the WuRx consumes a very low amount of power, the excess of harvested energy is stored on a large capacitor for supplying the energy required for the transmitter to work for a short amount of time. To balance the consumed power with the harvested power that enables the operation of the self-efficient node, in addition to enhancing each building block's performance separately, the co-design of RFEH and wireless transceiver can open up unprecedented possibilities. For example, the RFEH sensitivity, the input power level at which the RFEH produces the required DC supply voltage, can not be improved indefinitely by enhancing the circuit topology (increasing the number of stages for a Dickson based RF rectifiers). Therefore, if a wireless transceiver can operate with a lower supply voltage, the sensitivity of the RFEH, and the range of the operation can be significantly increased. In addition, the required voltage regulator (or PMU), often exhibiting low efficiencies at these extremely low power levels, has been eliminated by designing wireless transceiver circuitry that can operate with a range of supply voltages rather than a fixed supply voltage, so that the input sensitivity of the entire system is further improved. The WuTx is constructed using a fast start-up oscillator and an efficient class E power amplifier that can be tuned to output different input power levels. The proposed WuRx can be deployed solely in the applications where a power-hungry transceiver is used and it needs to be activated on-demand when a pre-defined packet is detected to increase its battery life-time. The WuRx also can be used to enable the WuTx when a pre-defined packet is received achieving a complete RF-powered wireless transceiver.

Chapter 7 concludes the dissertation by summarizing the motivation, contributions and future work.

# Chapter 2

# Literature Review

In this chapter, first, previously introduced methods for optimizing RFEH are reviewed. Then, circuits techniques for increasing the efficiency of RFEH implemented in CMOS are investigated. Finally, existing methods and circuit techniques for implementing low-power and RF-powered transceivers are described.

## 2.1 RFEH Optimization and Efficiency Enhancing

In this section, existing methods for optimizing and increasing the efficiency of RFEH is reviewed. As stated in (1.1) the overall efficiency of an RFEH system depends on the design of the matching network and rectifier's efficiency. Therefore, for increasing the overall RFEH system efficiency, the matching network and rectifier must be co-designed to maximize the power transfer and rectifier's efficiency. In addition to that, circuit techniques can be applied to increase the rectifier's efficiency further. In this section, first we investigate the methods for analytically modelling and optimizing the rectifiers and matching networks and then review the previously introduced circuit techniques for increasing the efficiency of the rectifiers.

### 2.1.1 Existing RFEH Models and Optimization Methods

The Modified Dickson's charge pump, as shown in Fig. 2.1, is extensively used in the design of RF-to-DC power converters for RF energy harvesting applications because

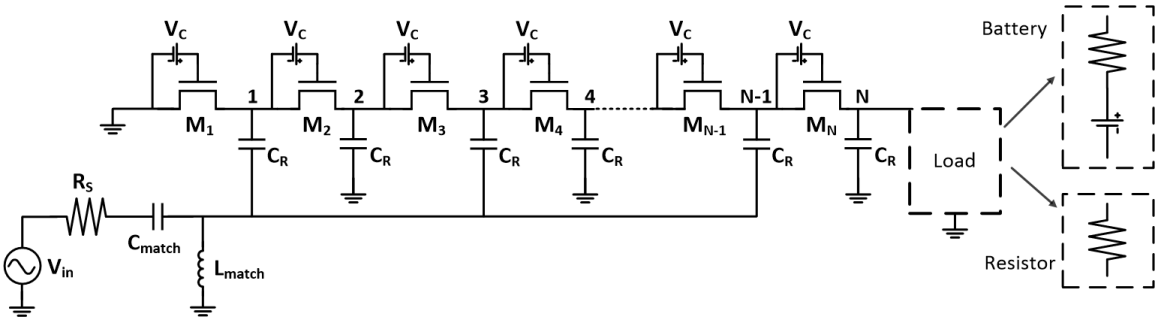



Figure 2.1: Threshold-compensated Dickson rectifier.

both rectification of received RF signal and boosting of the DC output voltage levels can be achieved by a single circuit. These are the two functions that are required for converting RF energy to DC for supplying the electronic circuits [14, 26–28]. The analysis and design of RF-to-DC Dickson's power converters are difficult because of the inherently nonlinear behavior of these rectifiers. The design parameters of an RFEH include the matching network topology and component sizes, the number of rectifier stages, the transistor and capacitor sizes, and the compensation voltage if a threshold voltage compensation is applied. These parameters are required to be determined to achieve the design goal, which is often maximizing the power conversion efficiency of the RFEH. The simulation of these circuits is computationally expensive as the transient simulation's maximum time step selected by the circuit simulators is determined by the frequency of the RF signal often resulting in millions of simulation steps to allow for the rectifier output to settle at its final values.

The stand-alone design of the rectifier for maximum efficiency, without the inclusion of the matching network, is not possible as the input voltage of the rectifier depends on the design of the preceding matching network and input power levels in addition to the rectifier's own design parameters because of the dependency of the input resistance of the rectifier to these parameters. At the same time, the design of the matching network for maximum power transfer depends on the rectifier's parameters, which are the function of rectifier's input voltage level (which is a function of input power levels itself). This will require a time-consuming iterative process that

the designer has to go through to find the optimum matching network and rectifier design parameters. Therefore, it is necessary to design the matching network and rectifier simultaneously to achieve the design goal (maximum power efficiency).

To understand the effect of design parameters on the performance of an RF harvester, and to facilitate and accelerate the design process, several analytical models have been developed that rely on the knowledge of input voltage levels as discussed below. However, in real-world RF energy harvesting applications, the input voltage level of the rectifiers is not a known design input because it is a function of the available input power, matching network design, and rectifier's parameters. The true design input of the RFEH is the available input power from the antenna/coil that can be determined based on the Friis equation taking into account the transmitted power levels and the distance of the source of power among other factors [7]. In [29], an analytical model of the rectifier is presented when the input voltage is higher than $V_{th}$. The presented equations are

$$\begin{aligned} V_o &= N[V_a' - V_{th} - V_{ov} + V_c] = NV_{boost}, \\ V_{ov} &= \left(\frac{15\pi I'_{oeff}\sqrt{2V_a'}}{8\mu_n C_{ox}\frac{W}{L}}\right)^{\frac{2}{5}}, V_a' = \frac{C_c}{C_c + C_{par}}V_a, \\ I'_{oeff} &= I_o + \frac{I_{s0}W}{\pi L}(e^{\frac{-V_c}{nV_T}})(1 - e^{\frac{-V_a'}{nV_T}})(1 + \lambda_{sub}V_a'). \end{aligned} \tag{2.1}$$

Here $V_a$ is the input voltage amplitude, $I_o$ is the output current, $V_c$ is the compensation voltage applied between gate and source of the transistors and $C_{par}$ is the transistor parasitic capacitor. In addition to that, a method is proposed for designing the rectifier's parameters for achieving maximum-efficiency. The developed maximum-efficiency design strategy assumes a given voltage level at the input of the rectifier to find the optimum rectifier's design parameters. However, it does not develop a design methodology that maximizes the overall efficiency of the energy harvester for a given input power. Furthermore, the above analysis cannot be used for an RF rectifier operating in the subthreshold regime (low input power levels). Similarly, [30] produced a model to predict the behavior of the charge pump rectifiers implemented with

Schottky diodes at a given input voltage level. The proposed method for calculating the input impedance of the rectifier at different input voltage levels does not lead to a proper design strategy because of the aforementioned reasons. In [31], the authors presented an analysis for Dickson's charge pumps in the low-power mode where the transistors operate in the subthreshold region. The output voltage equation for when the input amplitude is lower than $V_{th}$, but high enough to turn on the transistors in the subthreshold region, can be obtained as [31]:

$$V_o = NnV_T ln\left(\frac{I_0\left(\frac{V_a}{nV_T}\right)}{I_{Load}/\left(I_S\frac{W}{L}e^{\frac{V_c}{nV_T}}\right)+1}\right) \tag{2.2}$$

where $I_0$ is the zero-order modified Bessel function of the first kind, $V_a$ is the rectifier input voltage amplitude, $V_o$ is the output voltage of the rectifier, $V_c$ is the compensation voltage, and $N$ is the number of transistors in the rectifier chain consisting of $N/2$ stages.

This model also has been developed based on the level of the input voltage for the calculation of the input impedance. Therefore, it does not lead to the development of a non-iterative design strategy for the co-design of the matching network and rectifier for a given input power although it significantly reduces the time required for each iteration when compared to the simulation.

In [32], a self threshold-compensated Dickson's charge pump based on the input voltage is investigated and the optimum rectifier parameters are determined. However, the effect and design of the matching network on the overall RFEH efficiency are not considered. Although in [33], a new circuit technique for producing a constant compensation voltage for the rectifier is presented and the optimum value of the compensation voltage is determined using simulation based on the input voltage, the authors did not investigate the effect of the matching network and passive amplification. In other articles, computationally expensive simulations are used to determine the input impedance of the rectifier, and iterative design of the matching network [14, 34–36].

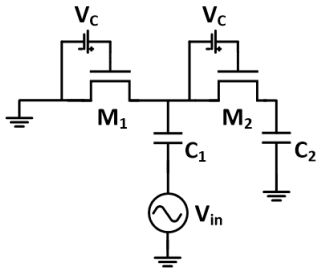



Figure 2.2: Single-stage Dickson's rectifier.

As the input voltage of a CMOS-based Dickson's charge pump rectifier changes substantially during each period of the input signal, small signal models for the transistors cannot be used as they work with a large signal at their input and their properties changes significantly over a period. Therefore it is necessary to drive a mathematical equation to facilitate the design process of such rectifiers.

In Chapter 3, we first analytically investigate RFEH operation and then introduce a method that makes the co-design of RFEH based on the input power much faster and easier compared to previously used methods.

### 2.1.2 Threshold Voltage Compensation: Operating Principles and Existing Techniques

One of the drawbacks of implementing Dickson's rectifiers in CMOS is the increased forward conduction loss caused by the large threshold voltage of MOSFETs compared with rectifiers that use diodes with extremely low threshold voltages. This problem can be addressed by adding a compensation voltage to the gate-source voltage ($V_{gs}$) of the transistors in the rectifier chain to increase their forward conduction current. The threshold-compensated CMOS Dickson's rectifier is illustrated in Fig. 2.1. This rectifier is structured by cascading N single-stage rectifiers as shown in Fig. 2.2. Briefly, the operation principle of a one-stage rectifier, shown in Fig. 2.2, when working at high input power levels is as follows: when the input voltage is negative, and its amplitude is larger than the $V_{th}$ of the MOSFET, $M_1$ turn on, and a charge is stored in $C_1$ while $M_2$ is biased reversely drawing some leakage current. When $V_{in} > 0$

and its amplitude is larger than $V_{th}$, $M_2$ starts conducting while $M_1$ draws a leakage current, which can be determined by the subthreshold current equation of MOSFETs.

As can be seen in (2.1), (2.2), the output voltage, and therefore the output power and efficiency, depends directly to the compensation voltage ($V_C$) that is applied between the gate and source of the transistor. $V_C$ reduces the forward power loss by decreasing the forward drop voltage from $V_{th}$ to $V_{th} - V_C$. However, this reduction comes at the cost of increasing the leakage loss, which will decrease the efficiency if $V_C$ is larger than its optimum value. Therefore, applying a constant DC voltage of $V_C$ between the gate and source of the transistor can increase the efficiency to certain levels and is limited. The efficiency can be improved by producing an adaptive $V_C$ for each transistor at each phase of conduction. For example, $V_C$ can be set positive when the transistor is conducting and negative when the transistor is in a leakage region so that its leakage current reduces. It is important that the added power consumption of the extra circuitry to produce the compensation voltage does not exceed the the extra power harvested as the result of their utilization. Also, the efficacy of the generated compensation voltages must be examined over the desired input power range.

Several works have been reported for making the compensation voltage using circuit techniques. In [27, 37], a compensation voltage is added to the gate-source voltage of each transistor generated by a diode-connected voltage reference, as shown in Fig. 2.4. As can be seen in Fig. 2.4 (a) a compensation voltage is generated using a diode-connected transistor biased in the subthreshold region and then it is distributed over main rectifier's transistors by storing it on a capacitor connected between source and gate of the transistor. As illustrated in Fig. 2.4 (b), in order to reduce the area, a ferroelectric capacitor is used to store the generated compensation voltage. However, these methods produce a constant compensation voltage, and as mentioned above, this voltage cannot exceed a certain level as it will increase the leakage current, and therefore the maximum efficiency of the rectifier is limited. In [38], the authors used a chain of resistors to make the compensation voltage, as illustrated in Fig. 2.5. In this

scheme, biasing resistors are used to produce a compensation voltage at the gate of the transistors from the output voltage thus reducing the forward conduction loss. This approach suffers from two main drawbacks. First, required off-chip resistors increase the area as they are required to be high to not consume large amount of power, and as mentioned above, as the compensation voltage is constant over the input period, the maximum achievable efficiency is limited. The authors of [17] propose a new circuit for producing the compensation voltage. However, still as the generated compensation voltage in [17] is a constant DC voltage, it can improve the efficiency to some extent where the added leakage current of the transistors starts degrading the efficiency of the rectifier. In [7, 14], as illustrated in Fig. 2.6, the gate of the transistors is connected to the corresponding Nth next/previous stage in the rectifier chain, which adds a DC bias voltage to the gate of the transistor increasing its conduction current. However, this method also increases the leakage current degrading the efficiency of the rectifier. Furthermore, the compensation voltage is not constant for different input power levels, making the efficiency dependent on input power. In [39], a control loop is utilized to produce a compensation voltage that keeps the output voltage of the rectifier as high as possible, as illustrated in Fig. 2.3. However, this method cannot effectively decrease the leakage current of the transistors as the produced compensation voltage does not change based on the input voltage and requires a power-consuming digital circuitry.

Trying to address the trade-off between the reduced conduction loss and increased reversed leakage, several techniques have been reported [15, 40, 41]. In [40], as illustrated in Fig. 2.7 (a), a differential structure is used, and the transistors' gate in the negative rectifier is connected to the middle point of the positive rectifier to produce an adaptive compensation voltage that increases the conduction current and decreases leakage current simultaneously. Although this method improves the rectifier's efficiency, it requires a differential input that may not be available when a single-ended antenna is used. In [41], body biasing is added to to the differential $V_{th}$

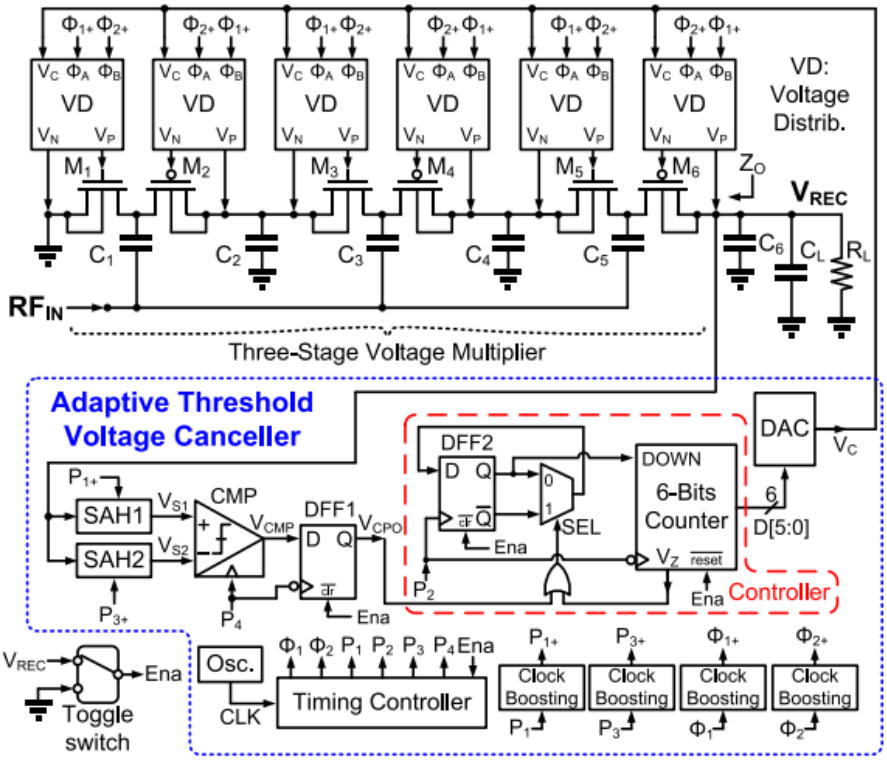



Figure 2.3: Control loop proposed in [39] ©IEEE.

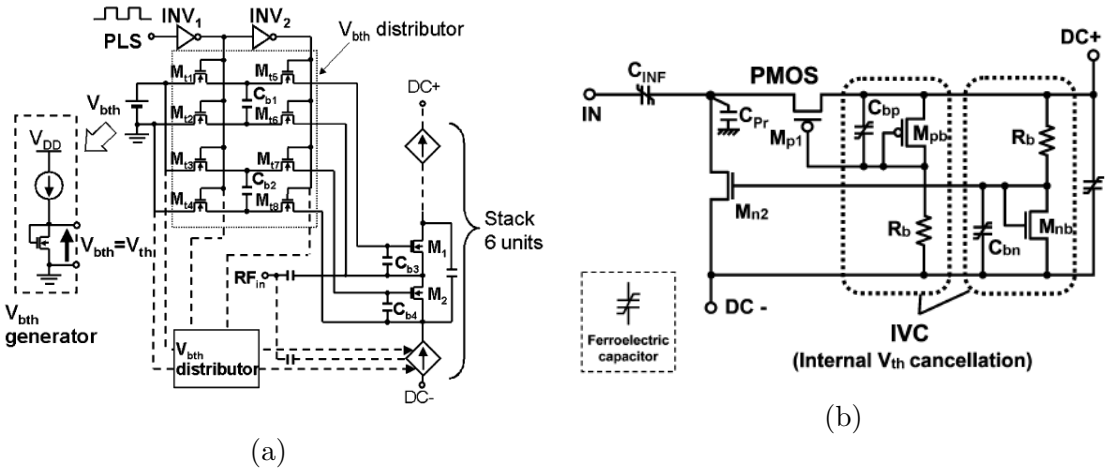



Figure 2.4: $V_{th}$ cancellation scheme proposed in (a) [27] (b) [37] ©IEEE.

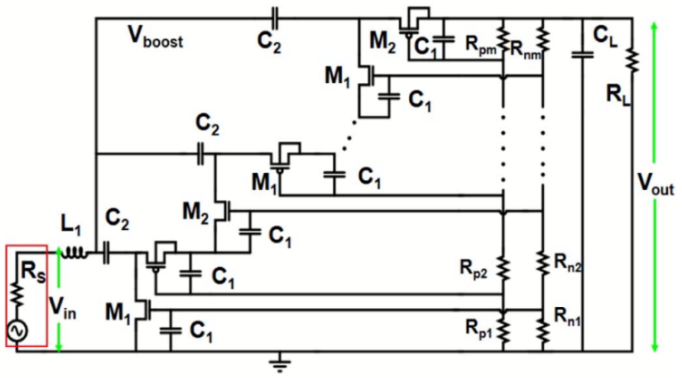
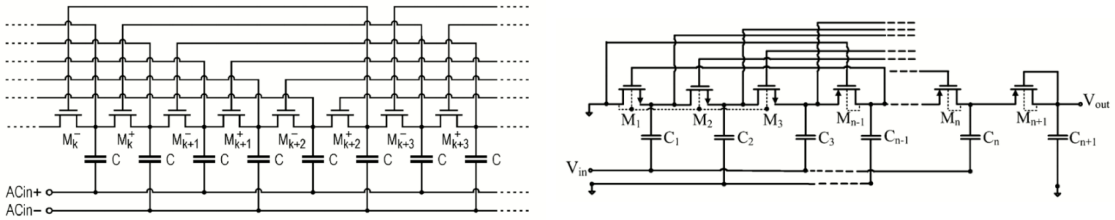



Figure 2.5: $V_{th}$ cancellation technique proposed in [38] ©IEEE.




(a) (b)

Figure 2.6: $V_{th}$ cancellation scheme proposed in (a) [7] (b) [14] ©IEEE.

cancellation method introduced in [40] to change the threshold voltage of the transistors in the rectifier chain, increasing their forward conduction current. However, this method requires differential RF input and triple-well CMOS process as the body of NMOS transistors should be connected to different voltages. In addition to that, as the threshold voltage is a function of the square root of $V_{sb}$ (source-bulk voltage), threshold voltage change will be limited. In [15], an adaptive compensation voltage is generated by dynamically connecting the transistors' gate to the suitable nodes in a rectifier chain as shown in Fig. 2.7 (c). However, this adaptive method cannot produce a suitable compensation voltage for a wide input power range as the amount of the compensation voltages changes drastically for different input power levels.

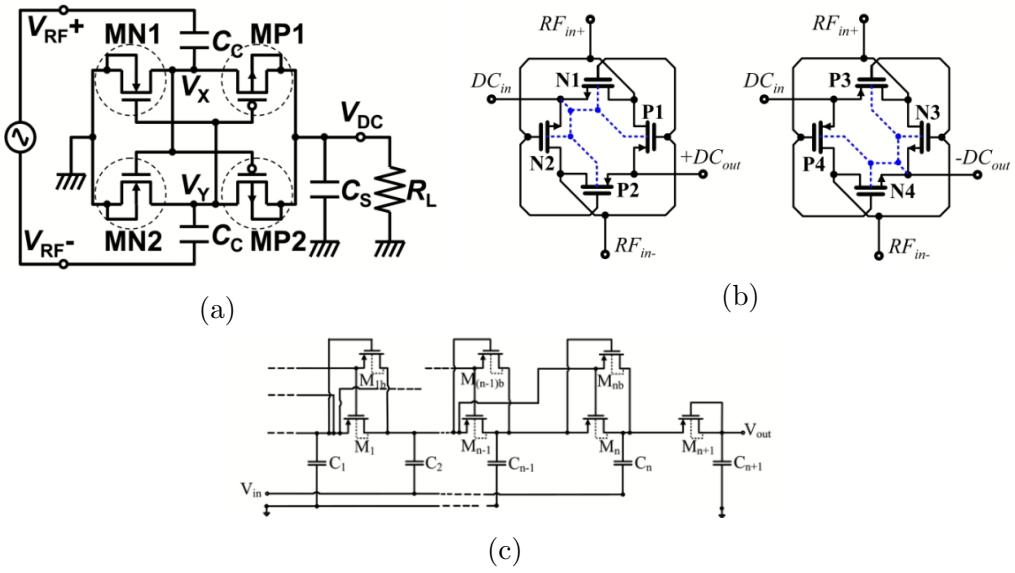


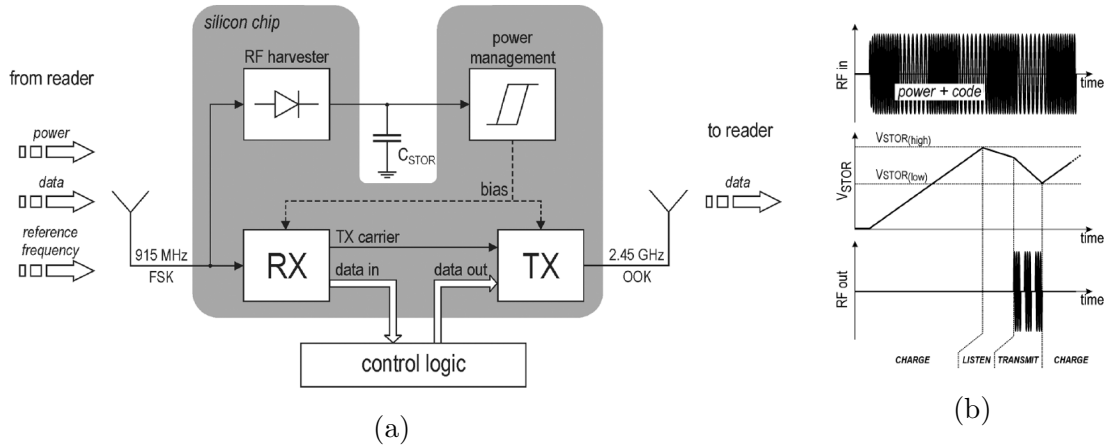

Figure 2.7: $V_{th}$ cancellation scheme proposed in (a) [40] (b) [41] (c) [15] ©IEEE.

## 2.2 Existing Low-Power and RF-powered Transceivers

As mentioned in Chapter 1, for a given input power, the RFEH output voltage cannot indefinitely increase. Usually, to increase the output voltage in Dickson's rectifiers, the number of stages must be increased. However, as analytically described in Chapter 3, as the rectifier's number of stages increases, its input resistance reduces, which will lower the passive amplification at its input leading to a lower input voltage amplitude. Therefore, for a given input power, by increasing the number of stages, the rectifier's output voltage increases up to an optimum point and starts decreasing after that. Therefore, for achieving a highly-sensitive RF-powered wireless transceiver, its minimum required supply voltage and power consumption must be reduced. Co-design of RFEH and wireless transceiver and eliminating low-efficiency PMU can lead to a lower required supply voltage for the transceiver thereby opening unprecedented possibilities in the design of RF-powered transceivers. In recent years, several works have been done to reduce wireless transceiver power consumption to arrive at an RF-powered scheme. The works can be categorized as follows:

### 2.2.1 Low-Power Intermittent Operation

The majority of the power consumed by wireless transceivers is consumed during the transmission time by the power amplifier and the preceding blocks driving it. However, as many IoT applications do not require continuous signal transmission and/or fast data rates, one way to reduce the power consumption of the transceiver is to turn it on for a short amount of time in a long period, so-called duty-cycled operation or intermittent operation. In this scheme, the transmitter and receiver are off and the RF energy harvester is charging the battery/capacitor until it stores enough energy to power on the transceiver for the required transmission time ([2, 13, 21]). The battery/capacitor voltage is being monitored using a power management unit and a voltage sensor. This method proves efficient at reducing the active power consumption of the transceiver by turning it on whenever required. However, in this method the power management unit, which is made by several amplifiers and voltage references, may consume a noticeably large amount of power when the battery/capacitor is getting charged and while the transmitter and receiver are off. In [13], an RF-powered transceiver based on the charge and discharge scheme, is proposed as illustrated in Fig. 2.8(a). As shown in Fig. 2.8(b) in the charging phase, both the receiver and transmitter are off and the harvested energy is stored on a capacitor. After the capacitor voltage reaches a certain level, the receiver is turned on listening to the incoming packets while its energy is providing by the capacitor. When the receiver detects a pre-defined code it activates the transmitter discharging the capacitor faster until the capacitor voltage reduces to a certain level so that the PMU turns off both receiver and transmitter and a new charging phase begins. Thanks to the proposed duty-cycled operation, the transceiver can work with input power levels as low as -17.1 dBm (input sensitivity). However, as the PMU requires 80 nA constantly, the input sensitivity of this transceiver cannot be further improved. In addition to that, the required supply voltage of 1.75 V for the operation of the transceiver cannot be




(a) (b)

Figure 2.8: (a) RF-powered wireless transceiver and (b) power management strategy (charge & burst) proposed in [13] ©IEEE.

achieved at the RFEH's output at very low input power levels, decreasing the input sensitivity. Furthermore, as mentioned in Section 2.2.3, the receiver utilized in this transceiver requires a power-hungry Phase-Locked Loop (PLL) so that the input sensitivity will be limited when it is utilized in schemes that only a wake-up receiver is required to turn on the main transceiver.

In [2], an RF-powered wireless transmitter is proposed as shown in Fig. 2.9. As can be seen, the RFEH charges the output capacitor until its voltage reaches 3 V and then activates the transmitter. The proposed transmitter consumes 190 nW when it is idle, leading to an input sensitivity of -19.7 dBm; however, as it requires a monitoring unit, the input sensitivity cannot be further improved. In Section 2.2.3, more information is provided regarding this transmitter.

Another method of reducing the power consumption of these wireless transceivers is to use wake-up schemes that transmit the data on demand. Typically, in a wake-up scheme, a wake-up receiver that consumes a very low amount of power listens to the input packets sent by the interrogator and waits for the predefined wake-up packet to activate the sensor circuitry and its transmitter ([42]). In addition to avoiding the power consumption associated with the transmission of the data at regular intervals, this scheme eliminates the power consumption of a power manager

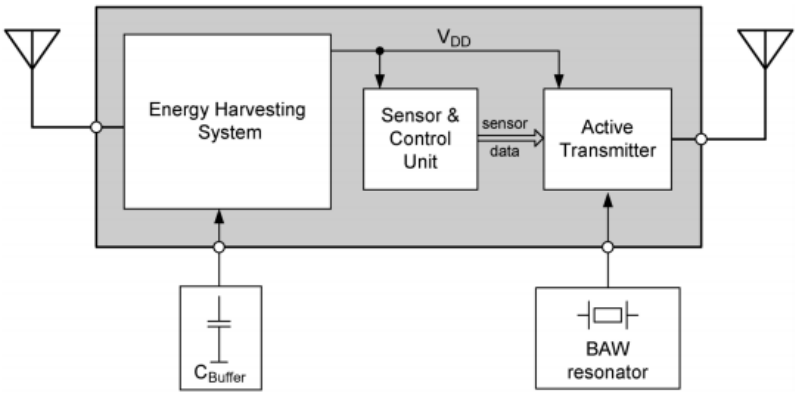



Figure 2.9: RF-powered wireless transceiver proposed in [2] ©IEEE.

and voltage supervisor or a low-frequency oscillator. However this topology has its own drawbacks; for instance, the wake up scheme needs a proper waking timing which requires related logic and state machines plus a decision maker making the circuit more complex ([43]). Recently, several near-zero wake-up receivers with good sensitivity have been reported promoting the investigation of wake-up schemes for the development of RF-powered wireless nodes [44–46].

In cases where real-time operation is required, the energy needed for the transceiver to work properly should be directly obtained from the RFEH. Therefore, the RFEH requires higher input power levels to provide the transceiver's energy, and these methods cannot achieve high input sensitivities [47, 48]. In [47], a TSPC frequency divider is used to generate a 457.5-MHz carrier frequency for the output power amplifier. On–Off Keying (OOK) modulation is utilized to transmit the data back to the base station. However, because of the non-intermittent operation, the input sensitivity 0f -10 dBm is achieved. In addition to that, because of using low-efficiency regulators, some of the harvested energy is wasted reducing the input sensitivity.

### 2.2.2 Low-Power Passive and Active Transmission

Backscattering transmission, reflecting back a portion of the incoming RF energy by making a disturbance in the input matching network connecting the antenna to the

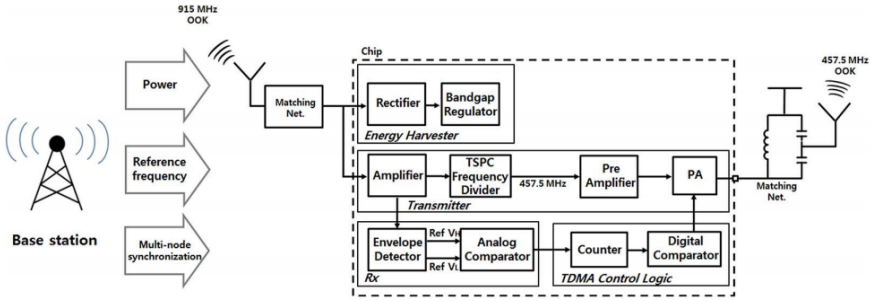



Figure 2.10: RF-powered wireless transceiver proposed in [47] ©IEEE.

rest of the system, has been reported in several papers [16, 49]. In [16], as illustrated in Fig. 2.11, a RF-to-DC rectifier is used to harvest energy from the incoming RF signal to turn on the sensor circuitry and transmitter. The designed ring oscillator, which acts as a temperature sensor, modulates the input of a backscattering switch to reflect back the input RF signal to the base station with a frequency that depends on the temperature. Although this method is a promising way of lowering the power consumption of the transmission as it does not need a dedicated wireless transmitter, its application is limited to very short-range communications because of the limited energy of the reflected signal.

Active power transmission is mostly realized by using a power amplifier at the output whose output power can be tuned for different transmission ranges. As mentioned, the significant portion of the transceiver power consumption is consumed during transmission time when the power amplifier is on, making duty-cycled narrowband transmissions a favorite technique to reduce the power consumption. Alternatively, inherently pulse-like transmission, like Ultra Wideband (UWB), can be used for low-power transmission. UWB modulation is a great candidate as it provides high energy efficiency by sending the signal in a fraction of the period [22, 23, 50–52]. However, the range of UWB pulses is hard to control and the pulse energy is limited by supply voltage and, so multiple pulses often must be sent for each symbol [53]. In [53], the authors increased the bandwidth efficiency and distance control by introducing pulses that are longer than a typical UWB pulse. This architecture is superior to tradition

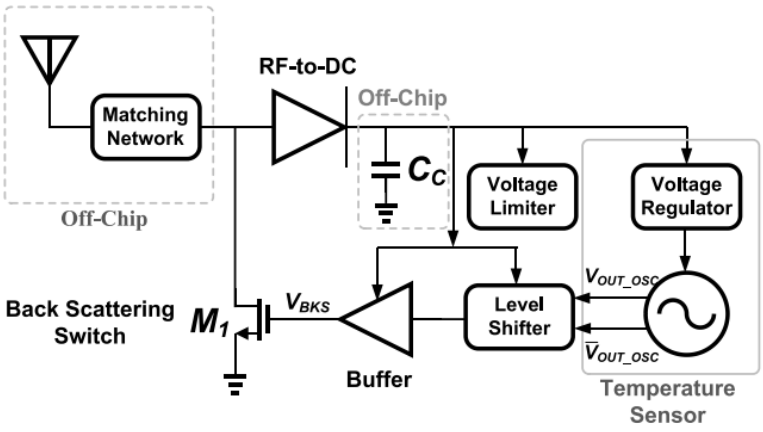



Figure 2.11: RF-powered temperature sensor proposed in [16] ©IEEE.

UWB transmission as it offers lower power consumption and less complexity in the design of the transceiver.

### 2.2.3 Idle and Active Power Reduction

As described earlier, RF-powered wireless transceivers are typically duty-cycled to reduce the total power consumption. While duty-cycled operation is effective at lowering the power consumption, it is essential that the transceiver consumes a very low amount of power while it is off as well. In [18] the authors reduced the off power consumption by inserting a high-Vt switch in the supply path of the circuit; however, one problem with using a switch is prolonging the start-up time which can increase the active power consumption.

For reducing the power consumption of the transceiver when it is on, power-hungry circuits must be avoided in favor of less complex transmitter and receiver designs, and power amplifier efficiency must be increased. In [18] to increase the efficiency in the transmission power and to overcome the low-quality factor of the printed antenna, a power oscillator is proposed as illustrated in Fig 2.12. In this architecture, the antenna is directly connected to the oscillator as the load and its internal resistance is compensated by the negative-gm of the power oscillator. Although this scheme is innovative in increasing the quality factor of the antenna, its carrier frequency

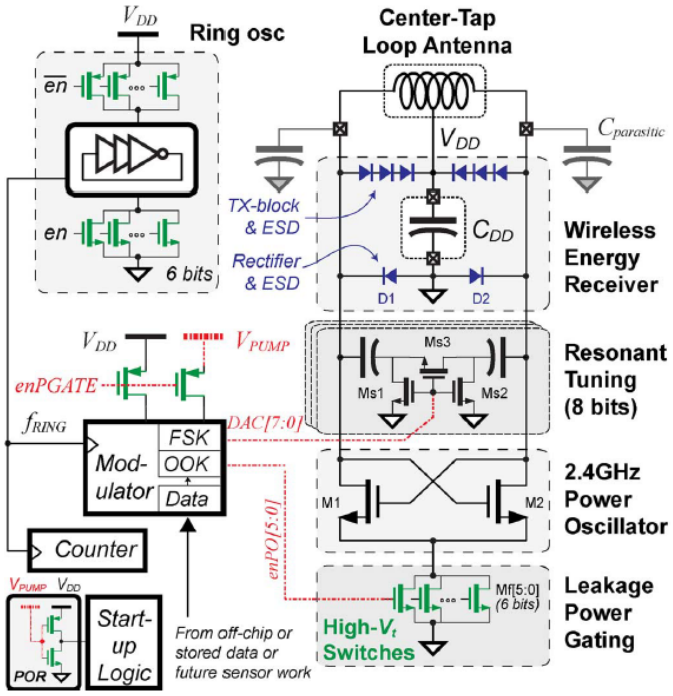



Figure 2.12: Power oscillator proposed in [18] ©IEEE.

can shift significantly in real applications from environmental factors. In addition its output power is not tunable, whereas, by using power amplifiers, the designer can tune the output power for specific applications. On the other hand, the authors in [13] used a frequency divider and phase-locked loop (PLL) as the receiver and an OOK transmitter that consumes large active power. Moreover, the output of a PLL takes a long time to settle, which will increase the activation time. On the transmitter side, power should be transmitted for a long time when a '1' code must be transmitted. Therefore, for a transmission power of $-12.5\ dBm$ they reported 860 $\mu A$ current consumption. Using a PLL in the transmitter can have the benefits of having a more accurate carrier frequency and reduction in sideband spurs, however, it is power-hungry and its long settling time wastes energy in the transceiver.

In [54], a low-energy crystal-less transceiver is presented that uses a divider-based transmitter that uses a dual-FSK modulator that is power-hungry and degrades the power efficiency of the circuit in the active mode. The authors in [2] report a sensor

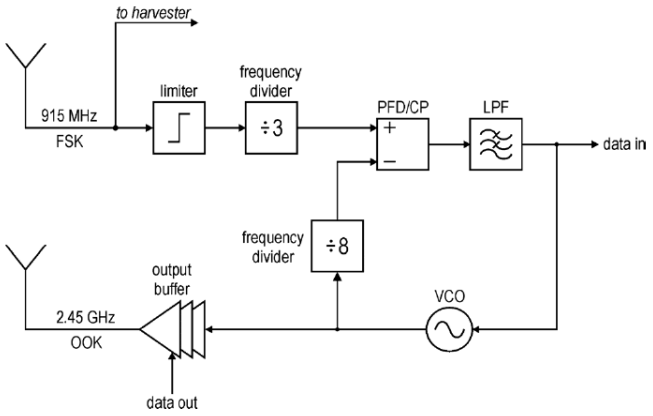



Figure 2.13: RF-powered transceiver proposed in [13] ©IEEE.

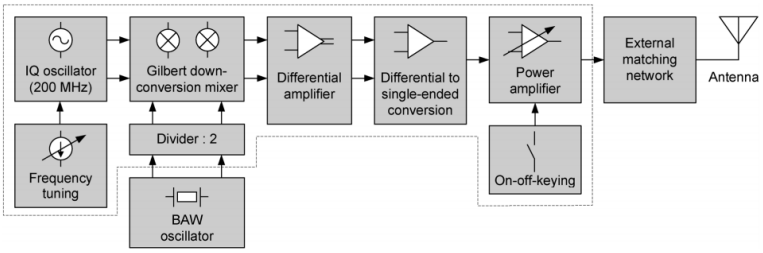



Figure 2.14: Active transmitter proposed in [2] ©IEEE.

transmitter that uses a Bulk Acoustic Wave (BAW) resonator which has significantly lowered start-up time compared to conventional crystal oscillators. However, their proposed transmitter suffers from large active power consumption mainly because of the complex structure consisting of a Gilbert cell, differential amplifier, and oscillator as shown in Fig. 2.14.

In [55], a near-field RF-powered transmitter is presented that uses an injection-locked frequency divider (ILFD). The ILFD circuit divides the received signal frequency by three and then re-uses it to transmit back the data by an open-drain driver using OOK modulation. This method eliminates the complexity of RFID readers by changing the transmitter frequency as it reuses the received frequency. However, the power amplifier used in the circuit draws static current and, therefore, it will drain the battery fast when it is used in a battery-powered scheme. To reduce the idle power consumption, which is the power when there is no signal to transmit and the

transmitter output is ZERO, it is desirable to use a power amplifier that does not consume static current. As mentioned earlier, because of the limited power for operating these types of sensors, using an ADC or microprocessor in the transmitter for interfacing with the sensor is not practical. Therefore, the transmitter should be designed in such a way that an analog signal value can be sent with the minimum amount of power and then interpreted at the base station, receiver where there are no constraints on power consumption.

# Chapter 3

# Systematic Co-Design of Matching Networks and Rectifiers for RF Energy Harvesters

As stated in Chapters. 1 and 2, the lack of a proper analytical model for calculating the RF rectifier characteristics based on their input power has made the design of such systems time-consuming. Without having a direct analytical method for finding the rectifier output voltage based on its input power, time-consuming simulation is required to design the matching network before finding the rectifier output. Furthermore, as the rectifier design variables, such as transistor width, length, and the number of stages, are changed, then the matching network must be designed once more, and this is why for optimizing the performance of such rectifiers, designers previously used time-consuming extensive simulations.

This chapter[1] presents a non-iterative method for the co-design of the matching network and rectifier of the RFEH to maximize the power conversion efficiency at a given input power level. The design methodology is based on a newly developed analytical model that calculates the output voltage, input impedance, and power conversion efficiency of RFEHs for a given input power. The model is developed for the scenario when conducting transistors operate in the subthreshold and above-threshold

[1]This chapter is based on a manuscript published in IEEE Transactions on Circuits and Systems I: Regular Papers [56].

regions. For the first time, the losses of the matching network, constructed of finite-quality passive components, have been taken into account in the analysis and design process of RFEHs. Considering the losses of the matching network components, the design of the matching network is modified to yield significantly smaller return losses when compared to the designs that do not consider the loss form the beginning.

## 3.1 Power-Based Rectifier Model

A modified multi-stage Dickson rectifier along with its input matching network is shown in Fig. 2.1. The objective of this section is to find the output power (or output voltage for a resistive load) of the energy harvester as a function of the available power from the antenna. The developed model then will be used for the non-iterative co-design of the matching network and rectifier by finding the design parameters that maximize the power conversion efficiency, a task that was not previously possible with voltage-based models.

Dickson's rectifiers are inherently nonlinear because of the switching behavior of their rectifying elements. However, in steady-state, we can assume that the input voltage of the rectifier is sinusoidal ($V_i = V_a cos(\omega t)$) with reasonable approximation especially for low input powers ($P_{in} < -10dBm$) if the energy harvester is driven by a sinusoidal input power source modeled as a $V_{source} = V_s cos(\omega t)$ in series with its output resistance $R_s$. In this case, the input impedance of the rectifier can be modeled with a resistor ($R_{in}$) in parallel with a capacitor ($C_{in}$). A matching network is essential to maximize the power transfer from the power source (antenna) to the rectifier, as shown in Fig. 3.1. Based on the maximum power theorem, the source impedance must be the complex conjugate of the input impedance at the input of the matching network ($Z_s = Z_m^*$ as shown in Fig 3.1). Assuming that a lossless matching network can be designed to maximize the power transfer from the source to the rectifier, for a purely real source impedance ($R_s$), the input impedance of the matching network must be equal to $R_s$. In this case, all of the available power will be

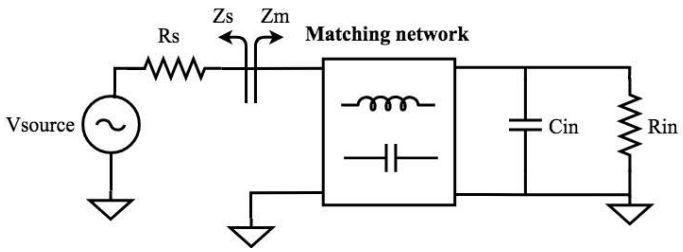



Figure 3.1: Equivalent circuit for the RFEH

delivered to the rectifier. The amount of the power that is delivered to the rectifier and the amount of the power that is consumed by $R_S$ are given by [57]

$$P_{in} = \frac{V_a^2}{2R_{in}} \text{ and } P_{source} = \frac{Vs^2}{8R_s}, \tag{3.1}$$

respectively. By equating $P_{source}$ and $P_{in}$, $V_a$ can be determined as the following:

$$V_a = \frac{V_s}{2}\sqrt{\frac{R_{in}}{R_s}} \tag{3.2}$$

which shows that $V_a$ can be larger than $V_s/2$ depending on the ratio of $R_{in}$ and $R_S$. This effect usually is called passive amplification. Passive amplification in Dickson converters is beneficial because it increases the ac signal amplitude before going to the rectifier and, hence, it increases the output voltage of the rectifier and also helps the rectifier to overcome the threshold voltage. The level of the output voltage of an energy harvester is determined based on the the ac-to-ac passive amplification of the matching network (multiplication of the RF signal amplitude by the matching network) and ac-to-dc voltage rectification and the multiplication of the multi-stage Dickson charge pump. For example, a rectifier with a small number of stages exhibits higher input resistance that in turn leads to higher passive amplification by the matching network whereas rectifier with a large number of stages exhibits lower input resistance leading to smaller passive amplification but higher dc voltage multiplication because of the rectifier with a large number of stages. A critical design decision is thus how to split the voltage multiplication between the matching network and the rectifier to achieve maximum power efficiency.

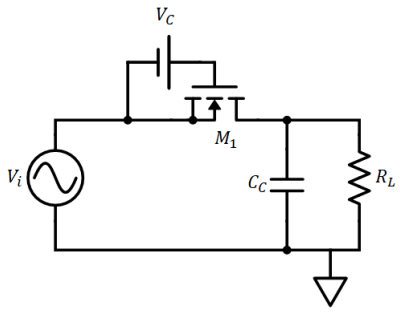



Figure 3.2: Half-stage (single transistor) rectifier

Therefore, the amount of passive amplification and the rectifier's input voltage level are not known at a given input power because $R_{in}$ is a function of the number of stages (N), $I_{Load}$, input power and $W/L$ i.e.,

$$R_{in} = f(P_{in}, N, I_{Load}, \frac{W}{L}) \tag{3.3}$$

Consequently, it is not possible to optimize the rectifier performance using models that rely on knowing the input voltage of the rectifier. In the following subsection, we derive a model that can predict $R_{in}$ for a given input power starting with the analysis of a single-transistor rectifier (a half-stage rectifier, as shown in Fig. 3.2) and then generalizing the result to N/2-stage rectifiers. Based on the level of the input power, it is necessary to separately analyze the rectifier behavior depending on the operating region of the transistors during the conduction phase.

### 3.1.1 Analysis for Low Input Power Levels

Considering the half-stage rectifier shown in Fig. 3.2, it is assumed that the output capacitor ($C_c$) is large enough that the ripple on the output voltage can be neglected. Assuming $V_i = V_a\ cos(\omega t)$, if $V_a < V_{th} + V_o$ the rectifier never conducts in the strong-inversion regime. The transistor's current in the weak-inversion regime is [58]

$$I_{sub} = I_S \frac{W}{L} e^{\frac{V_{gs}}{nV_T}} (1 - e^{-\frac{V_{ds}}{V_T}})(1 + \lambda_{sub} V_{ds}) \tag{3.4}$$

where $V_T$ is the thermal voltage, $n$ is the subthreshold slope factor, and $\lambda_{sub}$ demonstrates channel-length modulation in the subthreshold region. $I_S = I_{s0} e^{-V_{th}/nV_T}$ de-

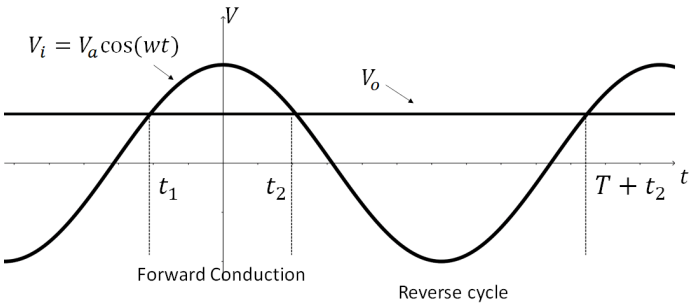



Figure 3.3: Half-stage rectifier waveform working in weak inversion.

pends on the process parameters and it can be obtained directly from the process simulation models or extracted from the simulation results of a single transistor. However, if the latter method is chosen, according to [59], the extracted parameters may not be very accurate if the simulation accuracy is reduced by circuit simulator methods that are used to speed up the simulation time.

Fig. 3.3 depicts the input and output voltage waveform of a half-stage rectifier. Between $t_1$ and $t_2$, the output voltage is smaller than the input voltage so that the output capacitor is charged via transistor conduction in the subthreshold region. In the time between $t_2$ and $t_1 + T$, the input voltage is smaller than the output voltage so that the output capacitor is discharged via the output current and the leakage caused by the transistor. According to the charge conservation principle, the amount of charge that is stored on the output capacitor during the forward conduction should be equal to the charge of the load and the one caused by the leakage

$$\Delta Q_{forward} = \Delta Q_{leakage} + \Delta Q_{load}. \tag{3.5}$$

Solving the integral in (3.5) for one period, the following equation set can be obtained as a function of input signal amplitude ($V_a$) and load current ($I_{Load}$) [31]

$$\begin{cases} V_o = NnV_T ln\left(\dfrac{I_0\left(\frac{V_a}{nV_T}\right)}{I_{Load}/\left(I_S\frac{W}{L}e^{\frac{V_c}{nV_T}}\right)+1}\right) \\ P_{in} = N\left(I_{Load} + I_S\dfrac{W}{L}e^{\frac{V_c}{nV_T}}\right)V_a\dfrac{I_1\left(\frac{V_a}{nV_T}\right)}{I_0\left(\frac{V_a}{nV_T}\right)} \end{cases} \tag{3.6}$$

where $I_0$ and $I_1$ are the zeroth and first-order modified Bessel functions of the first kind, $V_a$ is the rectifier input voltage, $V_o$ is the output voltage, $V_c$ is the compensation voltage, and $N$ is the number of transistors in the rectifier chain consisting of $N/2$ stages. The unknown parameters in this equation set are $V_a$ and $V_o$ considering the input power ($P_{in}$) as the design input, which can be found by solving the two equations simultaneously. In the following, we further simplify the equations to obtain a closed-form relation for $V_o$ as a function of $P_{in}$ and the rectifier's parameters. Equation set (3.6) can be simplified by using the following approximation for the modified Bessel functions [60]

$$I_k(x) \approx \frac{1}{\sqrt{2\pi x}} e^x \quad x >> k. \tag{3.7}$$

This approximation does not produce large errors for large $x$ values ( $x > 5k$). Therefore, if $V_a > 5nV_T$, the second equation of (3.6) can be simplified to

$$\begin{aligned} P_{in} &= N(I_{Load} + I_S \frac{W}{L} e^{\frac{V_c}{nV_T}})(V_a) \\ \Rightarrow V_a &= (\frac{P_{in}}{N}) \frac{1}{I_{Load} + \alpha_c} \end{aligned} \tag{3.8}$$

where $\alpha_c = I_S \frac{W}{L} e^{\frac{V_c}{nV_T}}$ is called the compensation coefficient. By using (3.7) as the approximation of $I_0$, an equation for $V_o$ can be derived as

$$V_o = \frac{NnV_T}{2} ln \frac{nV_T e^{\frac{2V_a}{nV_T}}}{2\pi V_a (\frac{I_{Load}}{\alpha_c} + 1)^2} \tag{3.9}$$

If $I_{Load}$ does not depend on the output voltage, a closed-form equation for the output voltage based on the input power can be obtained using

$$V_o = \frac{NnV_T}{2} ln \left( \frac{(I_{Load} + \alpha_c) NnV_T e^{\frac{2P_{in}}{(I_{Load}+\alpha_c)NnV_T}}}{2\pi P_{in} (\frac{I_{Load}}{\alpha_c} + 1)^2} \right). \tag{3.10}$$

### 3.1.2 Analysis for High Input Power Levels

The voltage waveform of the rectifier for high input powers, where $V_a > V_o + V_{th}$, is shown in Fig. 3.4.

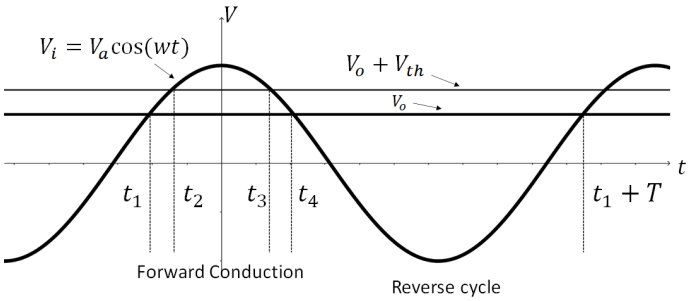



Figure 3.4: Half-stage rectifier waveform working in strong inversion.

The transistor's current equations for intervals $[t_1, t_2]$,$[t_3, t_4]$ and $[t_1, t_1 + T]$ are similar to the previous analysis, however the transistor's current equation for $[t_2, t_3]$ must be replaced with the transistor's current equation in the strong inversion region because in that interval the input voltage is higher than $V_o + V_{th}$. As the transistor is diode-connected, it operates in the saturation region, where the current of a long-channel transistor is given by

$$I_{sat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2. \tag{3.11}$$

Integrating over the charge conservation equation (3.5) for one period, the following equation set is obtained by including the effect of the compensation voltage ($V_c$) in the results obtained in [29]

$$\begin{cases} V_o = N[V_a' - V_{th} - V_{ov} + V_c] = NV_{boost}, \\ P_{in} = V_o I_{Load} + N \times I'_{oeff}\left[V_{th} - V_c + \frac{6}{7}\left(\frac{15\pi I'_{oeff}\sqrt{2V_a'}}{8\mu_n C_{ox}\frac{W}{L}}\right)^{\frac{2}{5}}\right] \\ + I_{s0}\frac{W}{L}\left[\frac{V_{boost}}{2} + \frac{V_a'}{\pi}\right. \\ \left. + \lambda_{sub}\left(\frac{V_{boost}^2}{2} + \frac{V_a'^2}{4} + \frac{2V_{boost}V_a'}{\pi}\right)\right] \end{cases} \tag{3.12}$$

where

$$\begin{aligned} V_{ov} &= \left(\frac{15\pi I'_{oeff}\sqrt{2V_a'}}{8\mu_n C_{ox}\frac{W}{L}}\right)^{\frac{2}{5}}, V_a' = \frac{C_c}{C_c + C_{par}}V_a, \\ I'_{oeff} &= I_{Load} + \frac{I_{s0}W}{\pi L}(e^{\frac{V_c}{nV_T}})(1 - e^{\frac{-V_a'}{nV_T}})(1 + \lambda_{sub}V_a'). \end{aligned} \tag{3.13}$$

and $C_{par}$ is the transistor parasitic capacitor. The equation set (3.12) must be solved to obtain $V_a$ and $V_o$ as a function of $P_{in}$.

### 3.1.3 Analysis of Converter for Resistive Load Based on Input Power

The equation sets of (3.6) and (3.12), or their simplified versions, can be used to model the rectifier behavior. By solving these equations, one can find the input voltage amplitude of the rectifier $V_a$ and the rectifier's output voltage $V_o$ for a given rectifier's input power $P_{in}$, the rectifier's parameters, and load condition. For instance, for a resistive load, the load current $I_{Load}$ can be placed by $V_o/R_L$ leaving only two unknowns in the equation sets if $P_{in}$ and rectifier's parameters are known. By solving the above equation sets, $V_a$, which is the input voltage of the rectifier, can be found. Solving these sets of equations can be done simply by available mathematical tools or numerical methods. For the purpose of this work, Matlab's fslove function has been used for solving the equation sets. Solving a non-linear equation numerically requires a proper initial guess that accelerates convergence to the final results. Assuming that the matching network between the antenna and the rectifier does not amplify the voltage (no passive amplification) for a given input power, an initial guess for $V_a$ can be found by replacing $R_{in}$ in (3.2) with $R_s$. In this case, $V_a$ will be half of the source voltage and can be used as the initial guess for $V_a$. An initial guess for $V_o$ can be found by assuming a typical rectifier efficiency (e.g. 30%) and, therefore, an initial guess for $V_o$ is $\sqrt{P_{in} \times 0.3 \times R_L}$. The estimate of 30% for the rectifier efficiency is a rough estimate based on experience and it can be fine-tuned by the designer. Nonetheless, the fsolve function can find the answer of the equation accurately even if initial guesses are not close to the final results. It should be mentioned that solving the equation systems takes only a few seconds on a conventional PC.

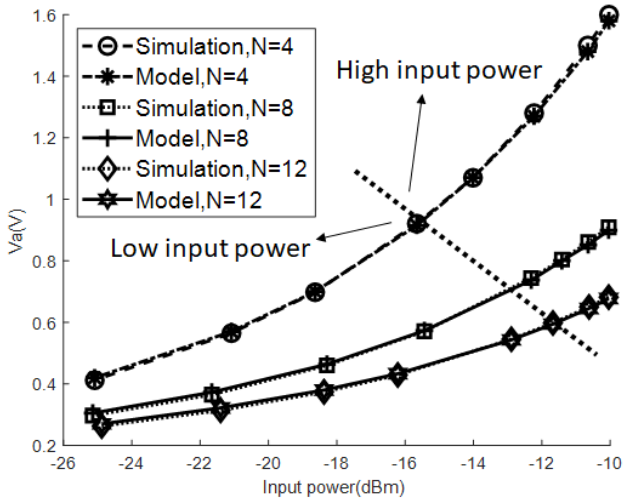
As noted, two different equation sets are presented for modeling the rectifier behavior depending on the input power levels. The decision to use the valid equation set for

a given input power level can be made by the following process: For a given $P_{in}$, both equation sets are solved to find $V_a$ and $V_o$. Then, the obtained $V_a$ and $V_o$ for each set is tested against the corresponding assumptions of the equation set ($V_a < V_o/N + V_{th}$ for low input power levels or high input power levels $V_a > V_o/N + V_{th}$). The results that comply with the corresponding assumption are valid indicating the correct region of operation for transistors,

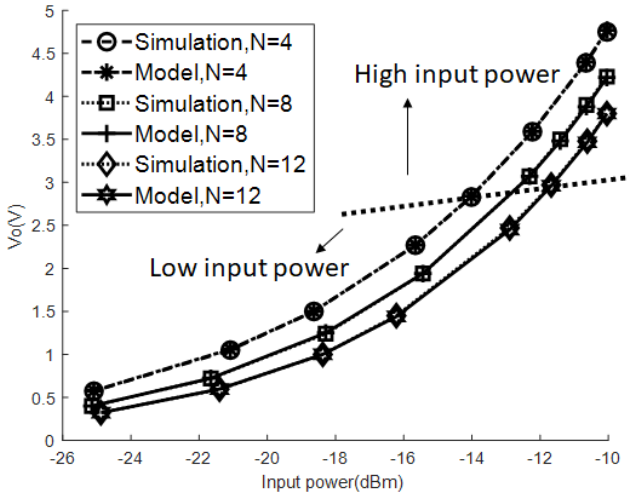
Simulation results and the proposed analytical model results for different rectifier input powers and parameters for a $130nm$ process are illustrated in Fig. 3.5. As can be seen, the proposed model and the simulation results show very good agreement (e.g. less than 5% error for the 2-stage ($N = 4$) rectifier) confirming the validity of the model. As can be seen in Fig. 3.5, the 2-stage rectifier's transistors work in the strong-inversion region when the rectifier input power is higher than -15.5dBm, therefore, the answers from (3.12) must be used for predicting the rectifier input and output voltage. Conversely, for input power levels lower than -15.5 dBm, because the rectifier's transistors never work in the strong-inversion region, the answers from (3.6) are valid. The border line in Fig. 3.5 separates the low and high input power level regions. On this line $V_a = V_o/N + V_{th}$ and the rectifier's transistors are operating at the boundary of the subthreshold and saturation regions.

## 3.2 Design of Lossless Matching Network for a Given Input Power

An impedance matching network between the antenna and the RF rectifier is required to maximize the power transfer to the rectifier, as shown in Fig. 3.1. The maximum power transfer happens when $Z_m = Z_s^*$. The matching network also increases the amplitude of the input voltage of the rectifier, i.e. $V_a$, via passive amplification. The typical design procedure for input matching networks starts with knowing the input impedance of the network. However, the input impedance of the rectifiers depends on the input power, the rectifier's load, the number of stages, and transistor sizes.




(a)




(b)

Figure 3.5: Simulation and model results versus input power for $N$=4, 8, and 12, W=10 $\mu$m, L=130 $nm$ and $R_L = 300\ K\Omega$ (a) Va and (b) Vo.

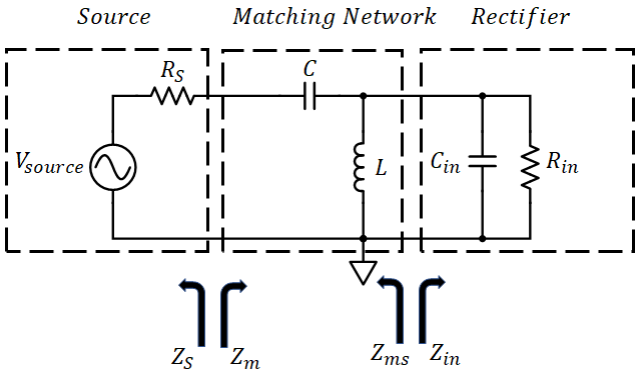



Figure 3.6: Equivalent circuit of RFEH using L-section for matching network.

To find the input power of the rectifier, we first assume that if a proper lossless matching network can be designed, half of the power received by the antenna goes to the rectifier. Therefore, when we know the rectifier's input power, load and rectifier's parameters we can use equation sets of (3.6) and (3.12) to solve numerically for the output voltage ($V_o$) and input voltage of ($V_a$) of the rectifier. Once we have calculated $V_a$, the input resistance and the input capacitance of the rectifier can be calculated as described in Subsection. 3.2.1. Knowing the input resistance and capacitance of the rectifier at a given input power, now we can design the assumed matching network that transfers half of the power by transforming the rectifier input impedance to be the conjugate match of source resistance. Although we first assume that the matching network is lossless, for practical cases, the matching network can only be constructed of passive elements with limited quality factors. The design of lossy matching networks is discussed in the next section.

Several matching network topology are possible for the circuit of Fig. 3.1 as investigated in [7, 30, 36]. In this work, the design of widely used L-section matching topology, as shown in Fig. 3.6, is described. The first step in the design of the matching network is to find the input impedance of the rectifier for a given input power, as discussed in Subsection 3.2.1. Then, closed-form equations for designing the matching network based on the derived input impedance are obtained in Subsection. 3.2.2.

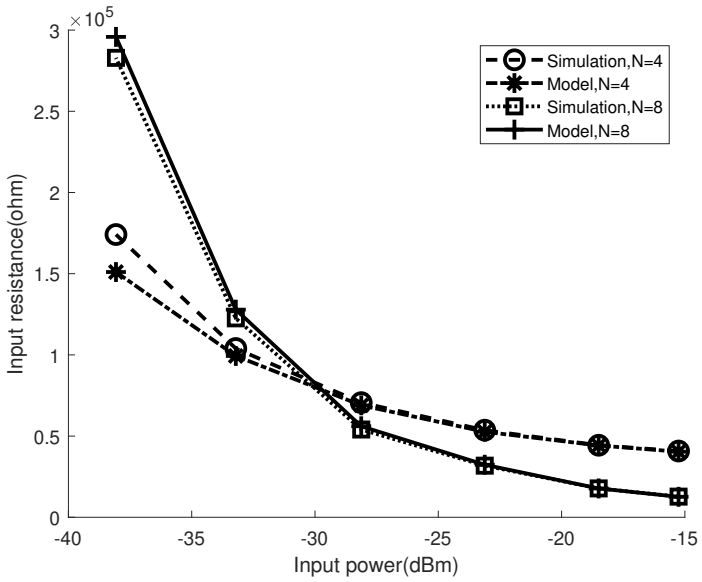



Figure 3.7: Simulation and model results for the rectifier's input resistance versus input power for $N = 4$ and 8, $W = 10\ \mu$m, $L = 130\ nm$ and $R_L = 1\ M\Omega$.

### 3.2.1 Input Impedance

#### Input Resistance

As a lossless matching network does not dissipate any power, the input power of the matching network is equal to its output power, the power that is delivered to the rectifier i.e. the rectifier's input power. As mentioned previously, by solving (3.6) or (3.12) for a given rectifier input power, $V_a$ and $V_o$ can be determined. Hence, the rectifier input resistance can be obtained using $R_{in} = V_a^2/2P_{in}$, where $P_{in} = P_{available}$. Fig. 3.7 compares the input resistance obtained by the model and simulation for different input power levels. As can be seen, the input resistance calculated by the model is close to the simulation results implying that the presented model predicts the input resistance with good accuracy at a given input power. The developed model only takes a fraction of the time to compute the rectifier's input resistance compared to the computationally expensive simulation that would be required to determine input resistance at each input power level. Furthermore, in previous methods that are based on the knowledge of rectifier's input voltage levels, an iterative process was required to find $V_a$ for a given input power.

**Input capacitance**

If the coupling capacitors are large enough, exhibiting much smaller reactances than those of parasitic capacitors of the transistors, the rectifier's input capacitance can be considered as $N$ parallel input capacitors of the half-stage rectifiers due to their transistor parasitic capacitors. As can be seen in Fig. 3.8 (a), in the positive cycle, $C_{GS}$ and $C_{SB}$ lie between the input RF signal and the ground, where $C_{GS}$ is the parasitic capacitor between gate and source of the transistor and $C_{SB}$ is the source-bulk junction capacitor. Whereas in the negative cycle, $C_{GD}$ and $C_{DB}$ are the parasitic capacitors seen by the input as the drain and source of the MOSFET change places. In both the negative and positive cycles, $C_{DB}$ and $C_{SB}$ are

$$C_{DB} = C_{SB} = WEC_j + 2(W + E)C_{jsw} \tag{3.14}$$

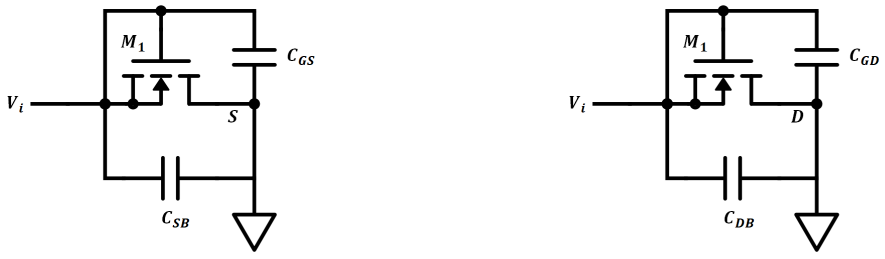
in which $C_j = C_{j0}/[1 + V_R/(\phi_B)]^m$ and $C_{jsw} = C_{jsw0}/[1 + V_R/(\phi_B)]^m$ where $V_R$ is the reverse voltage across the junction, $\phi_B$ is the junction built-in potential and m is a power related to the process [61]. In the case of low input power level that transistors never operate in the strong-inversion region,the gate-source capacitance and gate-drain capacitance are equal and can be determined as follows:

$$C_{GS} = C_{GD} = WC_{ov}. \tag{3.15}$$

However, for high input power levels, if the transistor operates in the strong-inversion region in the positive cycle, $C_{GS}$ increases to

$$C_{GS} = \frac{2}{3}WLC_{ox} + WC_{ov}. \tag{3.16}$$

However, in the negative cycle, $C_{GD}$ is equal to $WC_{ov}$ because the transistor is working in the weak-inversion region. As can be seen, all parasitic capacitors are voltage-dependent so that for a large-signal input, their value changes over a period. The change in the input capacitance of the rectifier, creates distortion on the rectifier current waveform, hence making the analysis difficult. Assuming constant junction




(a) (b)

Figure 3.8: Equivalent circuit of half-stage rectifier for calculating the input capacitor (a) positive cycle (b) negative cycle.

capacitors for simplicity, for high input power levels, average of $C_{GS}$ can be obtained for the positive cycle as

$$C_{GS} = \alpha\frac{2}{3}WLC_{ox} + WC_{ov} \tag{3.17}$$

where $\alpha$ is the ratio of the time that transistor is in strong-inversion region to the period. As illustrated in Fig. 3.4, the transistor operates in the saturation region in $[t_2,t_3]$ so $\alpha = (t_3 - t_2)/T$ where, $t_2$ and $t_3$ are the answers to $V_a cos(\omega t) + V_c - V_{th} = V_o$ where $t = t_2$ and $t = t_3$. If the ripple of the output voltage is small, $\alpha$ can be obtained as $(1/\pi)cos^{-1}((V_o + V_{th} - V_c)/V_a)$.

Using (3.14) and (3.15), in low input power levels, the rectifier input capacitance can be determined as follows:

$$C_{in} = N(WEC_j + 2(W + E)C_{jsw} + WC_{ov}) \tag{3.18}$$

and for high input power levels by summing the capacitors the following is obtained

$$\begin{aligned} C_{in} =& N\Big(\Big[\frac{1}{\pi}cos^{-1}(\frac{V_o + V_{th} - V_c}{V_a})\Big]\frac{2}{3}WLC_{ox} \\ &+ WC_{ov} + WEC_j + 2(W + E)C_{jsw}\Big). \end{aligned} \tag{3.19}$$

Although by using the above approximation the matching network can be designed with reasonable accuracy, there will be some errors due to the transistor parasitic capacitor's dependence on the voltage and the introduction of the layout parasitic capacitors. Hence, some final tuning may be needed in the matching network to acquire the exact matching values.

### 3.2.2 Lossless Matching Network Design

Assuming that the source impedance is purely resistive, the matching circuit of Fig. 3.6 should transform the rectifier input impedance to $R_s$ ( $R_m = R_s$ and $X_m = 0$). Converting the parallel impedance of $L_{eq} = Lw/(1 - LC_{in}w^2)$ and $R_{in}$ to series

$$Z_1 = \frac{R_{in}}{(1+Q^2)} + (\frac{jL\omega}{1 - LC_{in}\omega^2})(\frac{Q^2}{1+Q^2}) \tag{3.20}$$

where

$$Q = \frac{Im(R_{in} + jL_{eq}\omega)}{Re(R_{in} + jL_{eq}\omega)} = \frac{R_{in}}{\omega L} - \omega C_{in}R_{in}. \tag{3.21}$$

The value of Q also can be obtained by equating the matching network input resistance to the source resistance so

$$\frac{R_{in}}{(1+Q^2)} = R_s \quad \Rightarrow Q = \sqrt{\frac{R_{in}}{R_s} - 1}. \tag{3.22}$$

By substituting (3.22) in (3.21) the following closed-form equation for the matching network inductor can be obtained

$$L = \frac{R_{in}}{\omega(Q + \omega R_{in}C_{in})}. \tag{3.23}$$

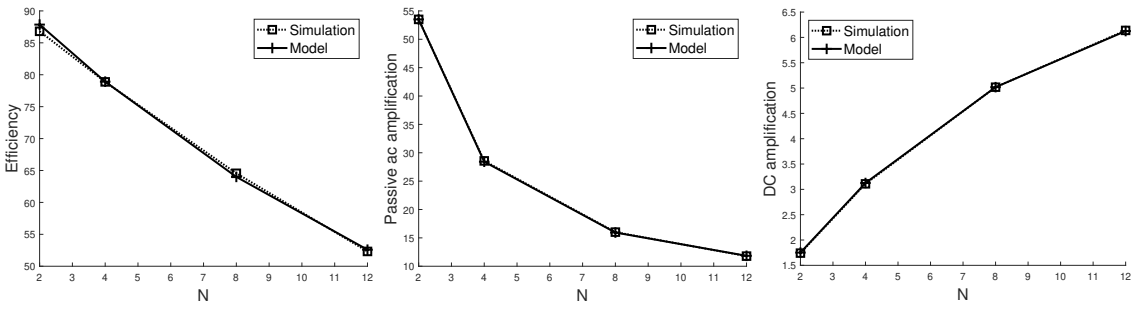
$C$ can be obtained by setting $Im(Z_m)$ to zero

$$\begin{aligned} &\frac{jL\omega}{1 - LC_{in}\omega^2}(\frac{Q^2}{Q^2+1}) + \frac{1}{jC\omega} = 0 \\ &\Rightarrow C = \frac{(1 - LC_{in}\omega^2)(Q^2+1)}{L\omega^2(Q^2)}. \end{aligned} \tag{3.24}$$

A comparison of the matching network for different parameters and the operating frequency of 915 MHz that is obtained from the simulation using iterative methods with the one that is predicted via model for different rectifier parameters and input power levels is shown in Table. 3.1. It can be seen the simulation and model results are close.

Table 3.1: Comparison of matching network component values obtained by model and simulation for different parameters. L=130 $nm$ and input power=-15 dBm.

| | | | Simulation | | Model | |
|---|---|---|---|---|---|---|
| $Vc$ (mV) | $N$ | $W(um)$ | $L(nH)$ | $C(fF)$ | $L(nH)$ | $C(fF)$ |
| 0 | 2 | 10 | 266 | 88 | 279 | 65 |
| 0 | 4 | 10 | 169 | 120 | 166 | 122 |
| 0 | 8 | 10 | 78 | 267 | 77 | 218 |
| 100 | 8 | 10 | 74 | 280 | 74 | 238 |
| 200 | 8 | 10 | 64 | 350 | 63 | 308 |
| 0 | 4 | 1 | 243 | 118 | 243 | 119 |
| 0 | 4 | 20 | 124 | 133 | 124 | 124 |




(a) (b) (c)

Figure 3.9: Effect of the number of stages on RFEH when $W = 10\ \mu m$, $L = 130\ nm$, $V_c = 0$, $P_{in}$ = -15 dBm and $R_L = 1\ M\Omega$ (a) efficiency (b) passive amplification and (c) dc amplification.

## 3.3 Design for Maximum-Efficiency for a Given Input Power - Lossless Matching Network

The common objective in the design of RFEHs is to maximize their power conversion efficiency in order to scavenge the maximum energy from a given input power. The power conversion efficiency ($\eta$) of energy harvester is

$$\eta = \frac{P_{out}}{P_{available}} = \frac{V_o^2/R_L}{P_{in} + P_{ref} + P_{match} + P_{rect}} \tag{3.25}$$

where $P_{in}$ is the rectifier input power, $P_{ref}$ is the reflected power to the antenna because of the impedance mismatch, $P_{match}$ is the matching network loss and $P_{rect}$ is the power loss due to leakage and conduction loss of the rectifier.

Now that we have developed a model capable of calculating the rectifier's input/output voltage for a given input power, and consequently find the optimum matching network based on the method shown in Subsection 3.2.2, we can proceed to maximize the overall power conversion efficiency of the energy harvester assuming a lossless matching network can be designed ($P_{ref} = P_{match\,loss} = 0$). As opposed to the previous methods that rely on extensive search and optimization algorithms to find matching optimum network components and rectifier parameters, our proposed method can quickly find the rectifier's input/output voltage and input impedance at a given input power that can be used to determine the values of the matching network's components based on (3.23) and (3.24) if the rectifier's parameters are known. Excluding the matching network's components will reduce the search domain significantly as the design parameters will be limited to only the rectifier's parameters. The following subsection investigates the effects of the rectifier's parameters (number of stages, transistor width, and compensation voltage) on the efficiency of the energy harvester. It is noteworthy that the produced results are only valid if the matching network components do exhibit extremely high-quality factors; nevertheless, it predicts how the rectifier's parameters affect the energy harvester' efficiency.

### 3.3.1 Effect of the Number of Stages

To investigate the effect of the number of stages on the rectifier efficiency, $N$ is swept while the other parameters are kept constant. The effect of the number of stages on the rectifier efficiency, shown in Fig. 3.9 (a), indicates that for a given input power, the efficiency of the rectifier decreases when the number of stages increases. This is due to the large passive amplification in rectifiers with a smaller number of stages (Fig. 3.9 (b)). As the rectifier number of stages decreases, the input resistance of the rectifier becomes larger leading to a larger passive amplification. Therefore, in the case that $N$ is equal to 2 (one-stage rectifier), most of the amplification comes from the ac amplification produced by the matching network. Conversely, for rectifiers with a larger number of stages, DC amplification (Fig. 3.9 (c))) caused by Dickson's charge pump becomes more dominant. DC amplification is defined to be the ratio of the output voltage to the input voltage amplitude. Having such a large passive amplification needs extremely high-Q components in the matching network. Hence, not only using very high-Q components is not feasible in real applications but also leads to a very narrow band RFEH [62]. Therefore, in practice, it is not possible to obtain efficiency values reported in Fig. 3.9 (a) because of the limited quality factor of the matching network components.

### 3.3.2 Effect of the Transistor Widths

The efficiency plot of a 4-stage rectifier for different input powers and transistor's width produced by the model is shown in Fig. 3.10. As the input voltage of the rectifier is divided between $C_c$ and parasitic capacitors of the transistors, the gate-source voltage of the transistors drops for larger transistors affecting the overall efficiency. Therefore, as it can be seen in Fig. 3.10, the efficiency reaches the maximum value for some optimum transistor size. It is worth mentioning that as the width of the transistors increases, the transistor's parasitic capacitor becomes larger so that at some point the magnitude of the imaginary part of the input impedance becomes

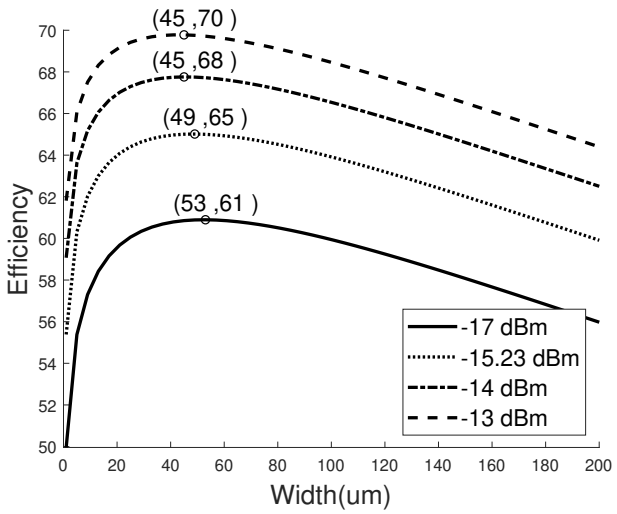



Figure 3.10: Effect of transistors widths on efficiency where $L = 130\ nm$, $N = 8$, $V_c = 0$, and $R_L = 1\ M\Omega$.

comparable to the input resistance. Therefore, other topologies other than the L-section matching network may be required. The effect of the transistors width in real applications when the matching network is lossy, will be discussed in Section 3.4.2

### 3.3.3 Effect of the Compensation Voltage

Choosing the right threshold compensation voltage, $V_c$, can lead to an improvement in rectifier efficiency. As previously mentioned, $V_c$ reduces the input voltage level needed by the transistor for turning on, resembling usage of a MOSFET with a lower threshold voltage in the rectifier. Using devices with lower threshold voltages in Dickson's charge pumps increases each stage dc voltage amplification and also reduces conduction loss as it decreases transistor ON resistance. However, in the negative cycle, the reduced threshold voltage leads to an increase in the leakage current as it can be seen in (3.4) which leads to a higher leakage loss. Model prediction and simulation results of sweeping $V_c$ between 0 to 0.25 for -15dBm input power level, $N = 8$ (4-stage rectifier), $L = 130\ nm$ and $W = 10\ \mu m$ is shown in Fig. 3.11. As can be seen for the given parameters the best efficiency is obtained when $V_c = 150\ mV$ meaning that if $V_c > 150\ mV$, the increased leakage loss overcomes the

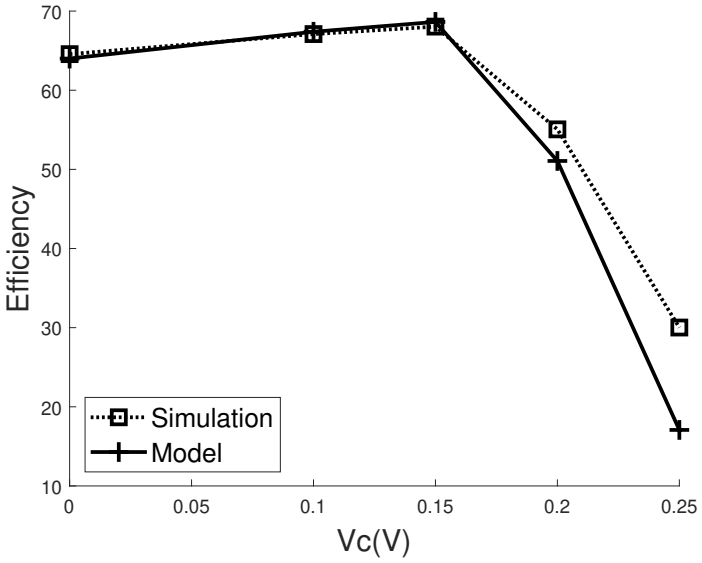



Figure 3.11: Effect of $V_c$ on efficiency where $L = 130\ nm$, $N = 8$, $R_L = 1\ M\Omega$, $W = 10\ \mu m$ and $P_{in}$= -15 dBm.

reduced conduction loss so that the efficiency decreases. It is worth noting that the compensation voltage can be generated off-chip using an external voltage source or one-chip using threshold self-compensation schemes [7, 14] or using a diode-connected MOS working in weak-inversion regime[27].

## 3.4 Co-Design of Lossy Matching Network and Rectifier for Given Input Power

In the previous analysis, we assumed that the matching network components exhibit extremely high quality factors ($Q$), so the input power of the matching network is equal to the input power of the rectifier for this lossless matching network. However, the on-chip and off-chip inductors and capacitors often exhibit limited $Q$. For instance, inductors implemented on-chip show quality factor of only 5-10 ([57]) while off-chip inductors often show a quality factor in the range of 20-100. On-chip and off-chip capacitors usually show a higher $Q$ than inductors, therefore, the effect of a limited-$Q$ capacitor in the matching network is neglected in this work. The loss of the matching network not only depends on its components' sizes and their quality factors

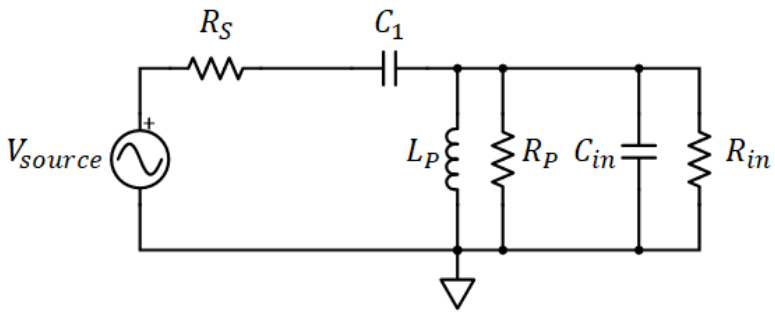



Figure 3.12: Equivalent circuit with lossy matching network.

but also on the rectifier parameters and the input power. Consequently co-design of the rectifier parameters and matching network is essential to maximize the efficiency of the overall energy harvester. In this section, the design of an RFEH for maximum efficiency is discussed taking the losses of the matching network into account. Compared to the previous analysis, the matching network power loss (inductor's power loss) must be deducted from the rectifier input power in order to find the optimum values of the matching components that satisfy the matching conditions for maximum power transfer($Z_s = Z_m^*$).

An inductor ($L_1$) with a finite quality factor can be modeled with an ideal inductor in series with a resistor where $R_{L1} = L_1 w/Q_{ind}$. The series representation of the lossy inductor can be converted into a parallel configuration, as shown in Fig. 3.12.

$$\begin{aligned} R_P &= R_{L1}(1+Q_{ind}^2) = \frac{L_1\omega}{Q_{ind}}(1+Q_{ind}^2) \\ L_P &= L_1(\frac{1+Q_{ind}^2}{Q_{ind}^2}). \end{aligned} \tag{3.26}$$

Two modifications to (3.6) and (3.12) are needed so that the effect of the lossy matching network is taken into account. First, the loss caused by $R_P$, which is $V_a^2/2R_P$, should be considered and deducted from the rectifier input power so that $P_{in} = P_{available} - V_a^2/2R_P$. Second, a third equation must be added to the equation sets of (3.6) and (3.12) that enforces the maximum power transfer condition. The new equations for designing the matching network can be obtained by replacing $R_{in}$ with $R'_{in}||R_P$ in (3.22) and (3.24) where $R'_{in}$ is the input resistance of the rectifier

in the presence of the lossy matching network. By adding the third equation and modifying (3.6), the following can be obtained for low input power regime as

$$\begin{cases} V_o = NnV_T ln\left(\dfrac{I_0\left(\frac{V_a}{nV_T}\right)}{\frac{I_{Load}}{\left(I_S\frac{W}{L}e^{\frac{V_c}{nV_T}}\right)}+1}\right), \\ P_{in}-\dfrac{V_a^2}{2R_P} = N\left(I_{Load}+I_S\dfrac{W}{L}e^{\frac{V_c}{nV_T}}\right)V_a\dfrac{I_1\left(\frac{V_a}{nV_T}\right)}{I_0\left(\frac{V_a}{nV_T}\right)}, \\ L_p = \dfrac{R'_{in}||R_P}{\omega(Q+\omega(R'_{in}||R_P)C_{in})}. \end{cases} \tag{3.27}$$

In case of high input power level, the equation set of (3.12) is extended to

$$\begin{cases} V_{oN} = N[V'_a - V_{th} - V_{ov} + V'_c] = NV_{boost}, \\ P_{in}-\dfrac{V_a^2}{2R_P} = V_oI_{Load} \\ +N\times I'_{oeff}\left[V_{th}-V_c+\dfrac{6}{7}\left(\dfrac{15\pi I'_{oeff}\sqrt{2V'_a}}{8\mu_nC_{ox}\frac{W}{L}}\right)^{\frac{2}{5}}\right] \\ +I_{s0}\dfrac{W}{L}\left[\dfrac{V_{boost}}{2}+\dfrac{V'_a}{\pi}+\right. \\ \left.\lambda_{sub}\left(\dfrac{V_{boost}^2}{2}+\dfrac{V_a'^2}{4}+\dfrac{2V_{boost}V'_a}{\pi}\right)\right], \\ L_p = \dfrac{R'_{in}||R_P}{\omega(Q+\omega(R'_{in}||R_P)C_{in})} \end{cases} \tag{3.28}$$

where $Q=\sqrt{(R'_{in}||R_P)/R_s-1}$, $L_P$ and $R_P$ are the same as in (3.26) and $R'_{in}=V_a^2/2P_{in}$. As mentioned previously, (3.27) and (3.28) can be solved numerically using mathematical tools. For verification purposes, the input voltage, $V_a$, and the output voltage of the rectifier for different inductor quality factors obtained by simulation and the model for a 2-stage rectifier with $W=10\ \mu m$, $L=130\ nm$ and input power of -15 dBm are depicted in Fig. 3.13. Table. 3.2 compares the size of the matching network's components obtained from the extensive search simulation and our proposed model verifying that the model can accurately predict the components' size in a fraction of time. The proposed model finds the matching network's inductor value with less

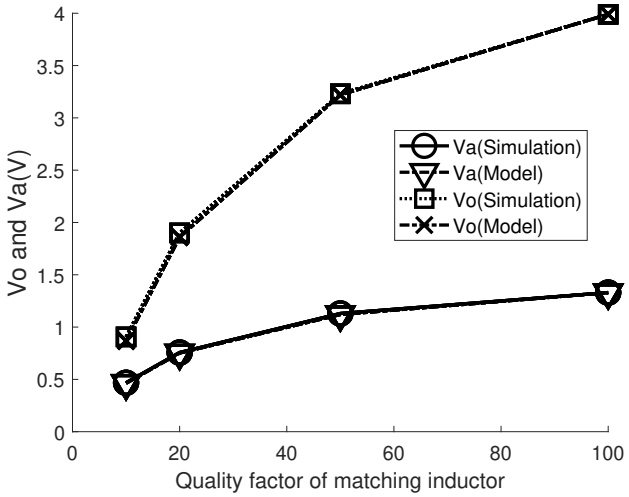
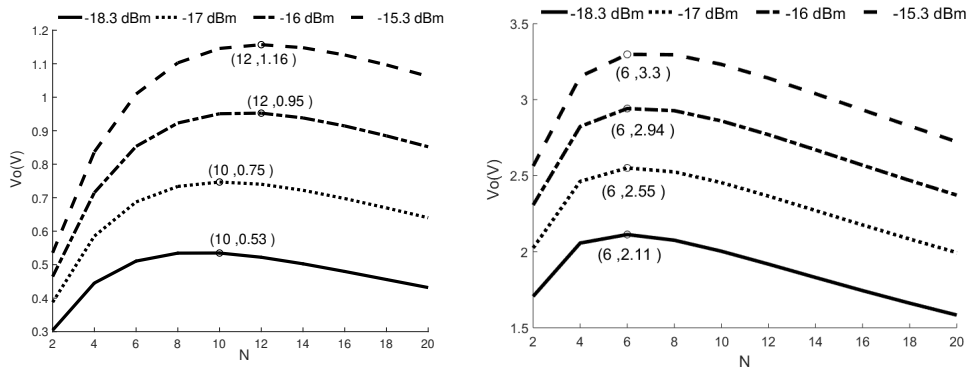


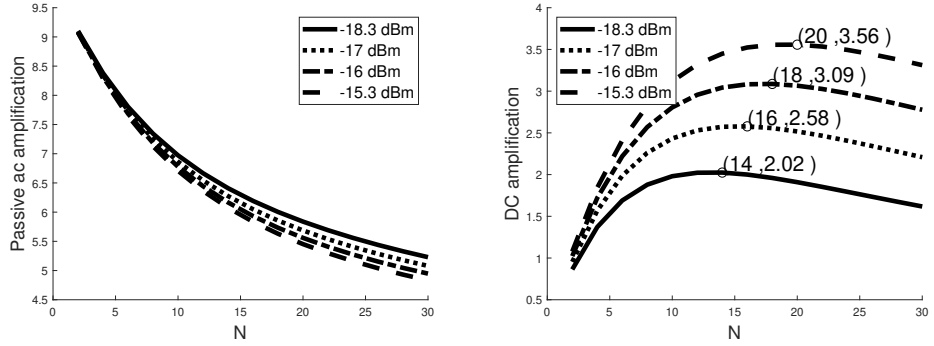

Figure 3.13: $V_o$ and $V_a$ simulation and model results versus $Q$ for $N$=4, $W$=10 $\mu$m, $L$=130 $nm$, $R_L = 1\ M\Omega$, and $P_{in}$=-15 dBm.

than 1% error and the capacitor value with a worst-case error of 21%. The large error in the predicted capacitor value comes from assuming that the input capacitance of the rectifier is constant in a cycle, however, as mentioned previously, the input capacitance of the rectifier depends on the input voltage of the rectifier. The error in the calculation of input capacitance affects the matching network's capacitor value more than its inductor so the error in the calculated matching network's capacitor provided by the model is larger than its inductor. One can find the exact value of the matching network's capacitor value by simulation. The amount of time required to find the matching network's component values using iterative methods can be extended to weeks in rectifiers with a large number of stages. Using the proposed novel method, the matching network inductor value can be calculated with good accuracy (1% error) in a few seconds by using a conventional PC. Although finding the exact value of matching network's capacitor cannot be done by the proposed method, the search domain is reduced significantly as it is restricted to $[0.75\,C_{model}, 1.25\,C_{model}]$.



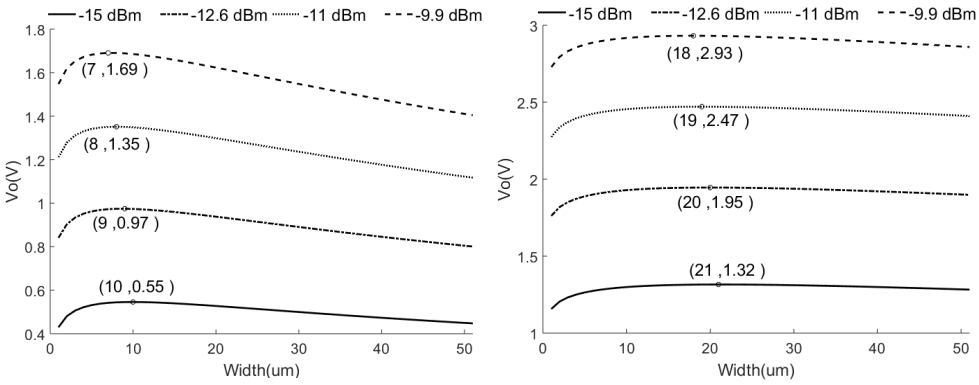

(a) (b)

Figure 3.14: Effect of number of stages on $V_o$ where $W = 10\ \mu m$, $L$=130 $nm$, and $R_L = 1\ M\Omega$ for different input powers (a) $Q = 10$ and (b) $Q = 50$.




(a) (b)

Figure 3.15: Effect of number of stages on passive amplification and dc amplification where $W = 10\ \mu m$, $L = 130\ nm$, $Q = 10$ for different input powers (a) passive amplification, and (b) dc amplification.




(a) (b)

Figure 3.16: Effect of transistors width on output voltage where $V_c = 0$, $L = 130\ nm$ and $N = 8$ for different input powers and $R_L = 200\ K\Omega$ (a) $Q = 10$, and (b) $Q = 50$.

Table 3.2: Matching network for
$N = 4$, $W = 10\ \mu m$, $L = 130\ nm$, and input power = -15 dBm.

| | Simulation | | Model | |
|---|---|---|---|---|
| Q | L1(nH) | C1(fF) | L1(nH) | C1(fF) |
| 10 | 63 | 420 | 63 | 330 |
| 20 | 95 | 250 | 95 | 217 |
| 50 | 130 | 174 | 130 | 150 |
| 100 | 146 | 149 | 146 | 128 |

### 3.4.1 Effect of Number of Stages - Lossy Matching Network

The effect of the number of stages on the output voltage for different input power levels for $Q$ of 10 and 50 (typical values for quality factors of on-chip and off-chip inductors, respectively) is shown in Fig. 3.14. As can be seen, in the RFEH with a lossy matching network, the efficiency is not always better for a rectifier with a smaller number of stages as it was the case for the lossless matching network. In case of the lossless matching network, the rectifier's input voltage, and in turn its efficiency, increases with the reduced number of stages as the passive amplification increases because of the larger input resistance of the rectifier with a lower number of stages. In the case of the lossy matching network, the matching networks with larger passive amplification exhibit higher power losses because of the increased inductor sizes and associated losses. If the inductor quality factor is 10, at the input power of -18.3 dBm, the best efficiency can be acquired using 5-stage ($N = 10$) rectifier whereas if the input power of the rectifier is -15.3 dBm the best efficiency can be obtained by using a 6-stage rectifier. As can be seen in Fig. 3.15 (a), passive amplification in the case of using a lossy matching network shows a similar behavior compared to the lossless one as a function of the number of stages. As the number of stages increases, the passive amplification reduces as the rectifier's input resistance decreases. DC amplification (Fig. 3.15 (b)), however, starts to reduce after some point. This is the point that the reduced passive amplification (the reduced rectifier's input voltage)

leads to a small DC boosting at each stage so that adding stages no longer increases the output voltage.

### 3.4.2 Effect of Transistor Width - Lossy Matching Network

Also, the model can be used to optimize the transistor's width to achieve the best efficiency for a given input power level and inductor quality factor. The effect of the transistor's width on the output voltage for various input powers is shown in Fig. 3.16. As shown, the efficiency relationship to the width of transistors is not the same as when the matching network is lossless. Width of the transistors should be narrower than the ones that work with a lossless matching network. According to Fig. 3.16 (a), for a 4-stage(N=8) rectifier terminated with $200K\Omega$ resistor as the load, when inductor quality factor is 10 and the rectifier input power is -15dBm the rectifier reaches its best efficiency when the rectifier transistors are $10\mu m$ wide.

### 3.4.3 Contour Plots

Design for maximum efficiency, at a given input power and matching network quality factor using the proposed method, can be done very quickly by constructing contour plots at those specifications. Simulation and model results show that for the compensation voltage of 150 $mV$ the rectifier achieves its best efficiency (Section 3.3.3) in our $130nm$ CMOS process independent of the number of stages and the transistor width. Therefore, after fixing the compensation voltage, for a given input power and matching network quality factor, contour plots of the efficiency versus the number of stages and transistors width can be used to find optimum rectifier's parameters. Contour plots of the overall harvester efficiency for different numbers of stages and transistor widths for the input power level of -15 dBm, $V_c = 150mV$, and different quality factors are shown in Fig. 3.17 (a) and (b). A comparison between two contour plots shows that when the loss of the matching network increases (from $Q = 50$ to $Q = 10$), the maximum efficiency can be obtained at a larger number of stages due

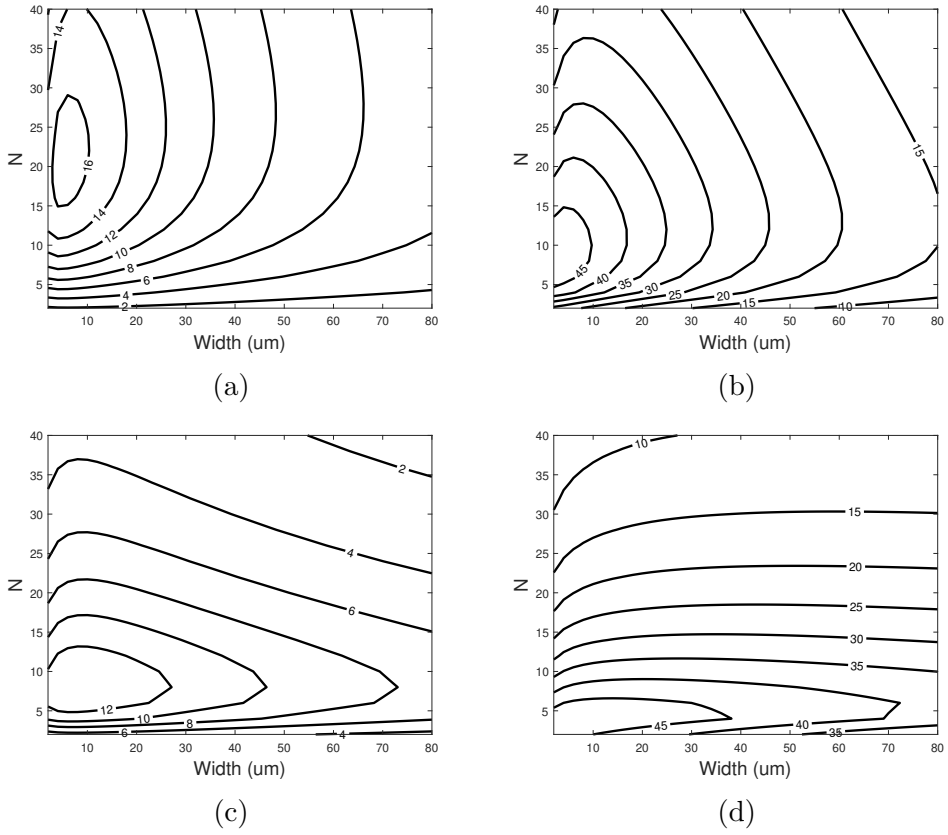
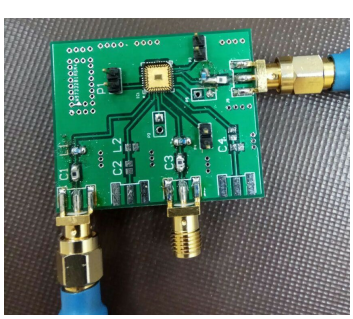



Figure 3.17: Contour plots of RFEH efficiency (a) $Q$=10, $V_c = 150\ mV$, $R_L = 1\ M\Omega$, $P_{in} = -15\ dBm$ (b) $Q$=50, $V_c = 150\ mV$, $R_L = 1\ M\Omega$, $P_{in} = -15\ dBm$ (c) $Q$=10, $V_c = 0$, $R_L = 200\ K\Omega$, $P_{in} = -10\ dBm$ (d) $Q$=50, $V_c = 0$, $R_L = 200\ K\Omega$, $P_{in} = -10\ dBm$

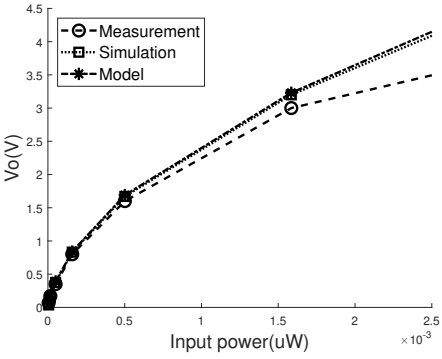
to the reduction in the passive amplification. The contour plots in 3.17(c) and (d) depict the efficiency relationship to transistors width and the number of stages in the case that compensated voltage is 0 ($V_c = 0$).

It is noteworthy to mention that previously for investigating the effect of the matching network's and rectifier's parameters on the overall harvester efficiency, one had to find the matching network's components' values using iterative methods for each set of rectifier's parameters. However, producing these contour plots using this novel method takes a fraction of the time required to produce the same results with the previously known computationally-intensive methods.

To quantify how the proposed methodology accelerates the design process of an RFEH for maximum efficiency, consider the following design example. In our simulation environment, a 4-stage rectifier reaches steady state after $60\mu s$ and the time needed for simulating the circuit using Cadence on a server that has a 32 processing cores is 6 minutes. Assuming that the designer's initial guess for matching network values is very close to the real ones, the search space can be limited to five different capacitor and inductor values. If the designer uses the iterative search method for finding optimum matching network's parameter, 25 simulations are required to find the optimum matching network values that transfers the maximum power which takes 150 minutes in total. This procedure must be repeated for each set of rectifier's parameters to produce the contour plot of Fig. 3.17(a). Assuming 20 different stages and 80 transistors sizes are tested, the process of optimum matching network design must be repeated 1,600 times which takes 240,000 minutes. Whereas in a conventional PC, the contour plot of Fig. 3.17 (a) can be calculated using the proposed model in approximately 16 minutes for the overall design process. Therefore, finding the optimum rectifier's parameters for a given input power using the proposed model is 15,000 times faster than previously used iterative search methods. In conclusion, design for maximum efficiency for a given input power, inductor quality factor and load as the design parameters can be achieved by generating a contour plot of the




(a)




(b)

Figure 3.18: (a) Experiment setup, (b) measurement results for $V_o$ for $N = 2, W = 200\ \mu m, L = 130\ nm$ , and $R_L = 10\ K\Omega$ vs. input power.

efficiency to find the optimum rectifier's parameters $(W, N)$ that produce the highest efficiency (assuming $L$ to be the minimum channel length of the process).

## 3.5 Model Validation with Experimental Results

For verifying the proposed model, a single-stage NMOS rectifier with transistor size of $200\mu m$ / $130nm$ was fabricated in TSMC's $130nm$ process. The chip is packaged in a QFN 36-pin package to reduce the parasitic effects of pins and mounted on a PCB with an FR-4 substrate as shown in Fig. 3.18 (a). The matching network inductors are chosen from CoilCraft ceramic chip inductors that typically show a quality factor range of 40 to 98 for the inductor value range of 1.8nH to 380nH at 900 MHz, which makes them suitable for achieving a narrowband matching network with high passive amplification. The circuit's input is connected to a Vector Network Analyzer via a 50Ω SMA connector and stimulated with the operating frequency of 915 MHz in order to measure $S_{11}$ and the output voltage simultaneously. Although the matching network was first designed considering pad, pin, wire bond and track parasitic effects, the final matching network inductor and capacitor values were fine-tuned for each power level to get less than 5% reflected power. The plot of the output voltage versus different input power levels is depicted in Fig. 3.18 (b). As

can be seen, the error between the predicted output voltage by the proposed model and the measurement results is less than 6% for input powers of lower than 5 dBm, indicating that the proposed model can accurately predict the RFEH performance. The difference between model, simulation, and the measurement results partly come from parasitic capacitors, especially the bottom plate capacitor of MIM capacitors, gate poly-silicon resistance, and interconnection parasitic resistance.

## 3.6 Summary

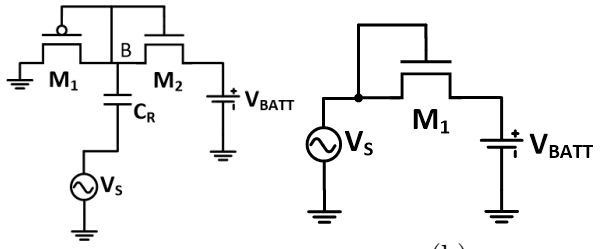
In this chapter, a new analytic model is developed for Dickson's charge pump rectifiers that is capable of predicting the rectifier's input/output voltage levels based on the rectifier's input power. The model is developed for both low and high input power regimes resulting in corresponding equation sets to be solved using mathematical tools for finding rectifier' input/output voltages. Simulation and measurement results for a $130nm$ process are in good agreement with the model. The model can determine the passive amplification produced by the lossless and lossy matching networks for a given input power allowing the matching network's and rectifier's optimum design parameters for maximum efficiency (matching network's components sizes, compensation voltage, transistor width, and the number of stages) to be found quickly and accurately. Capable of finding the rectifier's input voltage as a function of available input power, the proposed co-design methodology simplifies the design process of RFEHs and significantly reduces the time that is required to optimize design parameters for maximum power conversion efficiency compared to the previous methods that use an extensive iterative search to find the optimum design values.

# Chapter 4

# A Highly-Efficient RF Energy Harvester Using a Passively-Produced Adaptive Threshold Voltage Compensation

As mentioned in Chapter 2, adding a compensation voltage between the gate and source of the transistors in the rectifier chain can increase the rectifier's efficiency. In this chapter[1], we propose a novel scheme for creating an adaptive compensation voltage that increases the efficiency by increasing the forward conduction current and decreasing the leakage current of the rectifier's transistors. The impact of the compensation voltage for resistively loaded applications has already been described in detail in [29, 31] and Chapter 3. To highlight the impact of the proposed idea on efficiency, first, an analysis of a battery-loaded RFEH is derived, and then the proposed idea is presented. Finally, the presented idea is mathematically analyzed to highlight its effect on efficiency. The proposed idea successfully increases the forward conduction current and reduces the leakage current when transistors are off by adding an adaptive compensation voltage leading to significant improvement in the rectifier's efficiency.

[1]This chapter is based on a manuscript submitted to IEEE Transactions on Circuits and Systems I: Regular Papers [63].




(a) (b)

Figure 4.1: (a) Modified battery-loaded Dickson's rectifier. (b) Single-transistor rectifier.

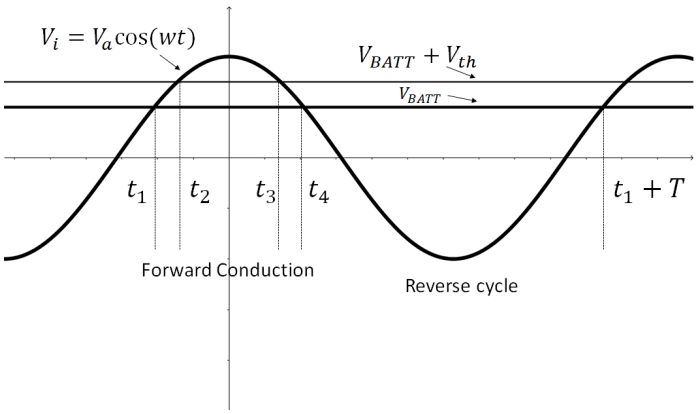



Figure 4.2: Voltage waveform of the rectifier.

## 4.1 Proposed Adaptive Compensation Voltage

In this work, another topology of Dickson's rectifiers, as shown in Fig. 4.1 (a) is used that utilizes a PMOS as the first transistor in the rectifier, and it is assumed that the battery can be modeled by a voltage source neglecting the battery internal resistance for simplicity. It will be described later that this topology is preferable to use if a compensation voltage is to be added as the gates of both transistors are tied together.

In this section, a mathematical model that can predict the output current of a battery loaded rectifier for a given input voltage is derived, starting with the analysis of a single-transistor rectifier shown in Fig. 4.1 (b) and generalizing it to a complete $N$-transistor rectifier. Assuming the input voltage is sinusoidal, $V_{in} = V_a cos(\omega t)$, the voltage waveform of the rectifier over one period is shown in Fig. 4.2. At $t_1$, the input voltage becomes larger than the battery voltage, and the transistor starts conducting in the subthreshold region until $t_2$ when it enters the saturation region. The transistor stays in the saturation region from $t_2$ to $t_3$. Between $t_3$ and $t_4$, the transistor is in forward conduction and operates in the subthreshold region. Finally, after $t_4$ and until the next cycle, the transistor is in reversed conduction, and its current is determined by the subthreshold current equation of the MOSFET transistor. The transistor drain current equations in the subthreshold and saturation regions is [58]:

$$\begin{aligned} I_{sub} &= I_S \frac{W}{L} e^{\frac{V_{gs}}{nV_T}} (1 - e^{-\frac{V_{ds}}{V_T}})(1 + \lambda_{sub} V_{ds}) \\ I_{sat} &= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 \end{aligned} \tag{4.1}$$

where $n$ is the subthreshold slope factor, $\lambda_{sub}$ is the channel-length modulation factor in the subthreshold region, $V_T$ is the thermal voltage, and $I_S$ is a process-dependent parameter.

For determining the average output current over one period, the charge conserva-

tion principle must be applied which can be obtained as follows:

$$\int_{t_1}^{t_2} I_{sub}\, dt + \int_{t_2}^{t_3} I_{sat}\, dt + \int_{t_3}^{t_4} I_{sub}\, dt - \int_{t_4}^{T+t_1} I_{sub,reversed}\, dt = \int_{t_1}^{T+t_1} I_{load}\, dt. \tag{4.2}$$

Assuming the input voltage is high, the duration of $t_1$ to $t_2$ and $t_3$ to $t_4$ is very small and the subthreshold current in that region is much lower that the saturation current in the region from $t_2$ to $t_3$, (4.2) can be simplified to:

$$\int_{t_2}^{t_3} I_{sat}\, dt - \int_{t_4}^{T+t_1} I_{sub,reversed}\, dt = \int_{t_1}^{T+t_1} I_{load}\, dt. \tag{4.3}$$

For $t_2$ to $t_3$ the following must be solved:

$$\int_{t_2}^{t_3} I_{sat}\, dt = \int_{t_2}^{t_3} \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{BATT} - V_{th})^2\, dt. \tag{4.4}$$

For $t_4$ to $T + t_1$, when the transistors are off, their current is determined by the transistor leakage current equation. The following needs to be solved determining the leakage average current over one period:

$$\int_{t_4}^{T+t_1} I_{sub}\, dt = \int_{t_4}^{T+t_1} I_S\frac{W}{L}(1 - e^{-\frac{V_{ds}}{V_T}})(1 + \lambda_{sub}V_{ds})\, dt. \tag{4.5}$$

Using the same procedure in [29], $I_{load}$ can be obtained as follows:

$$I_{load} = \frac{(8\mu_n C_{OX} W/L)(V_a - V_{TH} - V_{BATT})^{\frac{5}{2}}}{15\pi\sqrt{2V_a}} - \frac{I_S}{\pi}\frac{W}{L}(1 - e^{\frac{-V_a}{V_{TH}}})(1 + \lambda_{sub}V_a). \tag{4.6}$$

As can be seen, the first part of (4.6) is related to the conduction cycle and increases as the input voltage increases; however, the second term, which is for the transistor leakage, also increases as $V_a$ increases which has a negative effect on $I_{load}$. Another critical thing to consider in (4.6) is the fact that $V_a - V_{TH}$ should be larger than $V_{BATT}$ in order for the rectifier to start conducting current and for the transistors to turn on. For a single transistor rectifier shown in Fig. 4.1 (b), the above analysis will lead to the same result if the input node and the ground node are interchanged. Therefore,

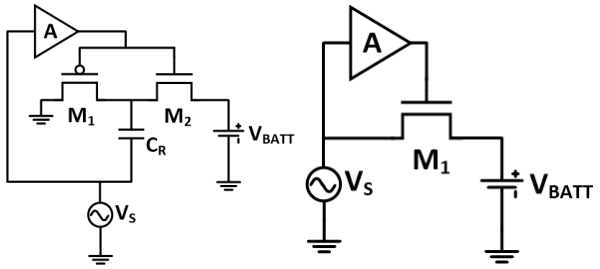
for an $N$-transistor rectifier ($N/2$ stages), the output current will be obtained by dividing $V_{BATT}$ by $N$ as follows:

$$I_{load} = \frac{(8\mu_n C_{OX} W/L)(V_a - V_{TH} - V_{BATT}/N)^{\frac{5}{2}}}{15\pi\sqrt{2V_a}} - \frac{I_S}{\pi}\frac{W}{L}(1 - e^{\frac{-V_a}{V_{TH}}})(1 + \lambda_{sub}V_a). \tag{4.7}$$

As can be seen in (4.7), by increasing the number of stages, the output current increases. Furthermore, for an $N$-transistor rectifier, $V_a - V_{TH}$ should be larger than $V_{BATT}/N$ for the rectifier to start charging the battery so for improving the sensitivity of the rectifier, one must use a greater number of stages. However, in real-world applications where the rectifier is connected to a power source instead of a voltage source, increasing the number of stages reduces the passive amplification at the input of the rectifier and may not necessarily increase the efficiency and sensitivity of rectifiers as stated in Chapter 3.

Now, first, the proposed idea for increasing the rectifier efficiency is introduced, and then $I_{load}$ for the proposed idea is derived, and finally, a circuit that implements the proposed idea is introduced and analyzed. The proposed idea increases the efficiency by increasing the forward conduction current and reducing the leakage current. For increasing the current of the transistor in the forward conduction, $V_{gs}$ must become larger compared to the conventional rectifier, and since the source of the transistor in the forward conduction is tied to the battery, the gate voltage is the only terminal whose voltage can be amplified. In contrast to that, in the negative cycle that the transistor is drawing leakage current, the gate voltage should be smaller than the source which is tied to the input to reduce the leakage current. Therefore, an adaptive voltage which is in-phase with the input voltage and is larger than it is required to be applied to the gate of the transistor, as shown in Fig. 4.3 (a).

In Fig. 4.3 (a), the rectifier's input is amplified by A and is fed back to the rectifier's transistors gate. For analyzing the rectifier, a single-transistor rectifier can be used once more, as shown in Fig. 4.3 (b) before generalizing the results to $N$-transistor




(a) (b)

Figure 4.3: (a) proposed modified battery-loaded Dickson's rectifier (b) proposed single-transistor rectifier.

rectifiers. As can be seen, in the forward conduction cycle, $V_g = AV_{in}$ and $V_s = V_{BATT}$ while $V_d = V_{in}$ meaning that the forward conduction current of the transistors is larger compared to the conventional rectifier increasing the overall efficiency. In the negative cycle, $V_g = AV_{in}$ and $V_s = V_{in}$ while $V_d = V_{BATT}$, therefore, $V_{gs} = (A-1)V_{in}$ which is a negative value reducing the leakage current compared to the conventional rectifier that in the negative cycle $V_{gs} = 0$.

As mentioned earlier, finding the exact closed-form equations for the rectifiers leads to complex formulas that cannot be used for design purposes. Therefore, some approximations must be applied to the equations to achieve more simplified result. For finding the average output current of the transistor over one period, the approximations utilized in [29] can be used. Between $t_2$ and $t_3$, $V_{gs} = AV_{in} - V_{BATT}$ and $V_{ds} = V_{in} - V_{BATT}$, therefore, transistors enter the triode region. The drain current of the transistors in the triode region is as follows:

$$I_{triode} = \mu_n C_{ox} \frac{W}{L}[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2]. \tag{4.8}$$

Assuming that the transistors enter the deep triode region ($V_{ds}$ is very small), the second term of (4.8) i.e. $1/2V_{ds}^2$ is negligible. Therefore, (4.4) will be

$$\int_{t_2}^{t_3} I_{triode}\, dt = \int_{t_2}^{t_3} \mu_n C_{ox} \frac{W}{L}(AV_{in} - V_{BATT} - V_{TH})(V_{in} - V_{BATT})\, dt. \tag{4.9}$$

As can be seen, as the transistors enter the triode region, their on resistance reduces compared to when they work in the saturation region and therefore the forward

conduction current increases. In the negative cycle the leakage current must be multiplied by $exp((A-1)V_{in}/nV_T)$ as $V_g = AV_{in}$ and $V_s = V_{in}$. Therefore the following is obtained:

$$I_{load,new} = \frac{\sqrt{2}\mu_n C_{OX} W/L\sqrt{V_a - V_{TH} - V_{BATT}}}{15\pi\sqrt{V_a}}$$
$$\times (8AV_a^2 - V_a(10V_{TH} + 10V_o + 6AV_o - 4AV_{TH} + V_o^2(10-2A) + V_{TH}(AV_o + 5V_o) + 3AV_{TH}^2)$$
$$- \frac{I_S}{\pi}\frac{W}{L}e^{\frac{(1-A)V_a}{nV_T}}(1 - e^{\frac{-V_a}{V_{TH}}})(1 + \lambda_{sub}V_a). \tag{4.10}$$

This equation is complex and cannot be used for qualitative investigation. Qualitatively, first, in the conduction cycle $V_g$ is increased by a factor of A and the transistors enter the triode region. Therefore, the transistors' on resistance reduces compared to when they were working in the saturation region as they act as a small resistor. Therefore, forward conduction current increases benefiting efficiency. Second, the leakage current of transistors is suppressed by a factor of $exp((1-A)V_a/nV_T)$. As the leakage current of the transistors reduces, the second term of 4.10 reduces, increasing $I_{load}$ and hence the efficiency. Therefore, by increasing A, the efficiency of the rectifier increases without any limitations. In this chapter, we propose a novel circuit implementation of the adaptive compensation voltage by utilizing passive amplification. The proposed circuit introduces a small power overhead and significantly increases the rectifier efficiency compared to the conventional one.

### 4.1.1 Passive Amplification

In RFEH, the power is captured via an antenna/coil, which can be modeled as a voltage source in series with an internal input resistance ($R_S$) that in typical applications it is set to 50 Ω. Based on the maximum power transfer theorem, a matching network between the antenna (power source) and the rectifier is needed to transfer the input impedance of the rectifier to the conjugate complex of the input impedance ($Z_s = Z_m^*$) as shown in Fig. 4.4. In Fig. 4.4, it is assumed that a capacitor and resistor in parallel can model the rectifier. Assuming that the matching network is lossless

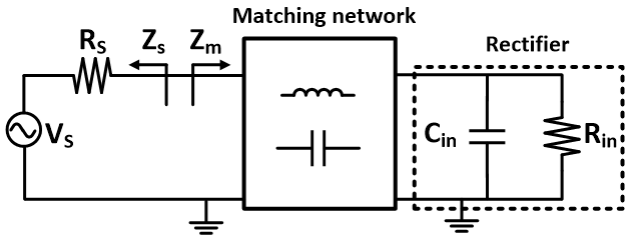



Figure 4.4: Equivalent circuit of RFEH.

and the output impedance of the source is purely resistive (real), and the source voltage is a sinusoidal wave ($V_s cos(\omega t)$), all of the available power will be transferred to the rectifier .i.e. $R_{in}$ if $Z_m = R_m = R_S$. Therefore, the amount of power delivered to the $R_{in}$ will be

$$P_{in} = \frac{V_a^2}{2R_{in}} \tag{4.11}$$

where $V_a$ is the amplitude of the signal at the input of the rectifier after the matching network. If $R_m = R_S$, the power consumed by $R_S$ ($P_{source}$) is obtained by: [57]

$$P_{source} = \frac{Vs^2}{8R_s}. \tag{4.12}$$

By equating $P_{source}$ and $P_{in}$ one can find $V_a$ as:

$$V_a = \frac{V_s}{2}\sqrt{\frac{R_{in}}{R_s}}. \tag{4.13}$$

As can be seen, if the input resistance of the circuit ($R_{in}$) is larger than $R_S$, $V_a$ can be larger than $V_s$. This phenomenon is called passive amplification and plays an important role in RFEH circuits that use Dickson's rectifiers. Finding a closed-form equation for $R_{in}$ of Dickson's rectifiers is quite complex as the rectifier is inherently non-linear, and $R_{in}$ depends on the input power, transistors' sizes, and the load as stated in chapter 3. However, it can be said that, with the appropriate design of the rectifier, $R_{in}$ is larger than $R_S$ so that $V_a$ is larger than $V_s$. As shown in (2.1), a larger $V_a$ can increase the rectifier efficiency as the rectifier efficiency depends on its input amplitude.

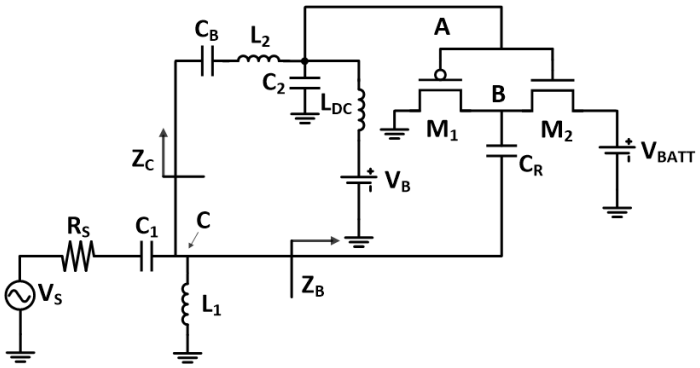



Figure 4.5: Proposed modified Dickson's rectifier.

### 4.1.2 Implementation of the Proposed Circuit

The proposed circuit, producing the adaptive compensation voltage, is shown in Fig. 4.5. $L_1$ and $C_1$ are the matching network for the rectifier. The matching network consisting of $L_2$ and $C_2$ is a secondary matching network for converting the impedance seen at the gate of the transistors closer to the power source impedance for transferring a ratio of the input power to the gate of the transistors. The large input resistance seen at A is converted to a smaller value of $Z_C$ after the matching network, causing some of the input power coming from the source to be transferred to the gate of the transistors.

Assuming that the resistive part of $Z_C$ is $R_C$, the impedance at node B is $R_B$, and $C_R$ is large enough that in the operating frequency it can be assumed as a short-circuit, the input power is divided between C and B is as follows:

$$\begin{aligned} \frac{P_B}{P_{IN}} &= \frac{R_C}{R_C + R_B} \\ \frac{P_C}{P_{IN}} &= \frac{R_B}{R_C + R_B} \end{aligned} \tag{4.14}$$

where $P_B$ is the power transferred to the rectifier, $P_C$ is the power transferred to $R_C$, and $P_{IN}$ is the total input power coming from the input source. If the matching network of $L_2$ and $C_2$ is lossless, $P_C$ is completely transferred to the resistance seen

at node A . i.e $P_C = P_A$. Therefore:

$$\begin{aligned} V_A &= \sqrt{2P_C R_A} \\ V_B = V_C = \sqrt{2P_B R_B} &= \sqrt{2P_C R_C} \\ \Rightarrow \frac{V_A}{V_B} &= \sqrt{\frac{R_A}{R_C}} \end{aligned} \tag{4.15}$$

where $V_A$ is voltage amplitude at node A, $V_B$ is voltage amplitude at node B, and $V_C$ is the voltage amplitude at node C which is equal to $V_B$ in RF frequency where $C_R$ is short-circuited (designers ser $C_R$ large enough to act as short-circuit in the operating frequency). The power division between $Z_B$ and $Z_C$ determines the voltage at nodes A and B. The input power coming from the source is divided between $Z_C$ and $Z_B$. As the rectifier is charging the battery, most of the power should be transmitted to $Z_B$. It can be assumed that $P_C = xP_B$ in which $x$ is small so that $P_B >> P_C$. Therefore:

$$\begin{aligned} V_A &= \sqrt{2P_C R_A} \\ V_B &= \sqrt{2P_B R_B} = \\ \Rightarrow \frac{V_A}{V_B} &= \sqrt{\frac{xR_A}{R_B}}. \end{aligned} \tag{4.16}$$

(4.16) shows an interesting result. If $xR_A > R_B$, the voltage at node A is amplified compared to node B. As $R_A$ is the resistance seen at the gate of transistors, it is reasonable to assume that it is higher than the rectifier input resistance and simulation results approve it. By utilizing this technique, an adaptive compensation voltage can be obtained that enhances the efficiency of the rectifier by making the amplifier with the gain of A shown in Fig. 4.3 (a). The amplified voltage still is in sinusoidal form, meaning that no switching power will be consumed at node A and therefore, the power consumption overhead is minimized. For quantifying the voltage amplification, it is imperative to find $R_B$ and $R_A$ based on the input power levels. However, as the rectifiers are inherently non-linear, and their input voltage is large-signal and changes drastically over one period, small-signal analysis cannot be applied to find the rectifier input resistance. The rectifier input resistance based on the input power can be obtained using the method described in Chapter 3 requiring numerical tools for each

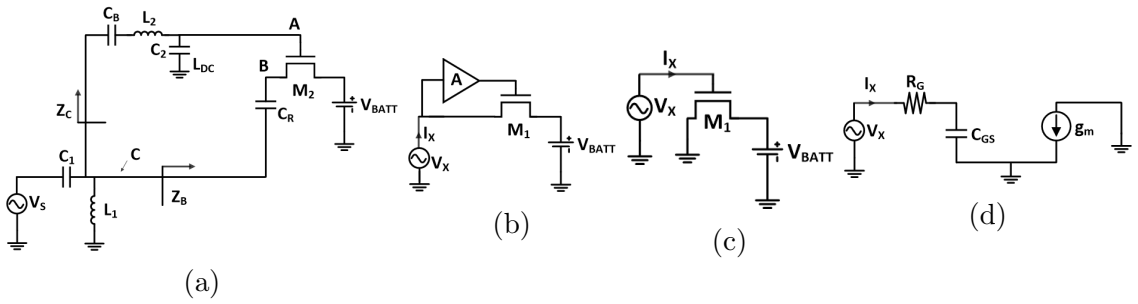



Figure 4.6: (a) single-transistor rectifier, (b) input impedance of rectifier, (c) impedance seen at gate of transistor, (d) small-signal equivalent of Fig. 4.6(c).

input power level. Nevertheless, to get insight into the rectifier's design, $R_A$ and $R_B$ of the proposed rectifier are obtained in an operating point, and small-signal analysis is applied to find the gain i.e., A.

For finding the input resistance of the rectifier, a single-transistor rectifier shown in Fig. 4.6 (a) is used as the results can be generalized to find the main rectifier's input resistance shown in Fig. 4.5. First, we derive an equation for the input impedance of the rectifier, i.e. $Z_A$ in Fig. 4.5. As shown in Fig. 4.6 (b), assuming that the compensation voltage on the gate of the transistor can be modeled by an amplifier with a gain of A and neglecting the parasitic capacitors except for $C_{gs}$ for simplicity, for long-channel transistors input impedance of the rectifier is

$$Z_{in} = \frac{1}{g_m A} \tag{4.17}$$

where $g_m$ is the transconductance of $M_1$.

Now for calculating the input impedance seen at the gate of the transistor, the voltage source is applied to the gate of the transistor, as illustrated in Fig. 4.6(c). Neglecting all the parasitic capacitors except for $C_{gs}$, the small-signal equivalent of Fig. 4.6 (c) is shown in Fig. 4.6 (d) where $R_g$ is the resistance seen at the gate of the transistors. As can be seen, the input impedance of the transistors is $R_g + C_{gs}$. Using a series-to-parallel impedance transformation, the parallel input resistance at

the gate of transistor is

$$R_P = R_g(Q_S^2 + 1) \tag{4.18}$$

where $Q_S = 1/(\omega R_g C_{gs})$. Therefore, using (4.16), $V_A/V_B$ can be obtained:

$$\begin{aligned} A = \frac{V_A}{V_B} &= \sqrt{\frac{xR_A}{R_B}} = \sqrt{xg_m A(\frac{1}{C_{gs}^2\omega^2 R_g} + R_g)} \\ \Rightarrow A &= xg_m(\frac{1}{C_{gs}^2\omega^2 R_g} + R_g). \end{aligned} \tag{4.19}$$

In reality, the lossy components in the matching network limit the maximum voltage gain that can be achieved. As the quality factor of off-chip inductors is lower than that of off-chip capacitors, most of the matching network's loss is due to the inductor. Assuming that each matching network's inductor has a quality factor of $Q_L$, (4.19) will be

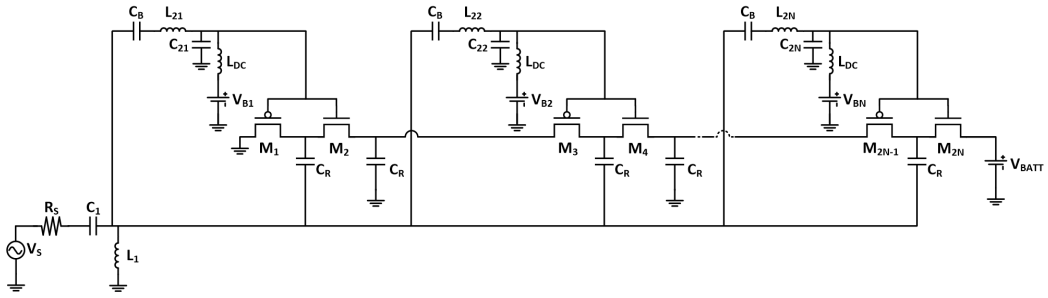
$$A = \frac{V_A}{V_B} = \sqrt{\frac{x(R_A||R_{EQ2})}{(R_B||R_{EQ1})}} \tag{4.20}$$

where $R_{EQi} = L_i * w * Q_L$ is a resistor in parallel with $L_i$ modeling its finite quality factor. $R_A$ is the resistance seen at the gate of the transistors and usually is quite large. Therefore, it can be assumed that $R_A >> R_{EQ2}$ , and so $R_A||R_{EQ2} \approx R_{EQ2}$. Therefore, assuming $R_{EQ1}Ag_m >> 1$, (4.20) simplifies to

$$\begin{aligned} A &= \sqrt{x\frac{R_{EQ2}}{R_{EQ1}}(R_{EQ1}Ag_m + 1)} \\ \Rightarrow A &\approx xR_{EQ2}g_m. \end{aligned} \tag{4.21}$$

As can be seen, for achieving high gain, $R_{EQ2}$ should be maximized requiring high-Q inductors.

Another essential thing to consider is that as the rectifier is connected to a battery, the voltage at point B is clipped to $V_{BATT}$ when the $M_2$ is on. The voltage of A will be clipped at $V_{BATT}$ if a conventional rectifier is used in which points A and B are connected. However, in the proposed rectifier, A and B are not connected, and voltage at point A is independent of the battery voltage; therefore, the voltage at point A can be much larger than the voltage of point B when $M_2$ is on. Therefore $V_{gs}$ of $M_2$ can be further increased, improving the rectifier's efficiency.




(a)

Figure 4.7: Proposed $N$-stage Dickson's rectifier.

### 4.1.3 $N$-stage Proposed Rectifier

As discussed in Sec. 4.1, the rectifier's sensitivity i.e., the minimum input power level that in which the rectifier starts charging the battery, can be improved by increasing the number of stages in the rectifier chain. However, as the number of stages in the rectifier increases, the rectifier's efficiency reduces since the input resistance of the rectifier is reduced. As shown in (4.13), if the input resistance of the rectifier is reduced, the passive amplification at the input of it is reduced, causing a lower input voltage and lower efficiency for the rectifier. Like a single-stage rectifier, the proposed idea can be utilized to increase the efficiency of an $N$-stage Dickson's rectifier by adding a matching network for each stage to enhance the voltage of the transistors' gates as illustrated in Fig. 4.7 (a). The proposed $N$-stage rectifier enhances the voltage at the transistors' gates passively using the secondary matching networks and significantly increases efficiency.

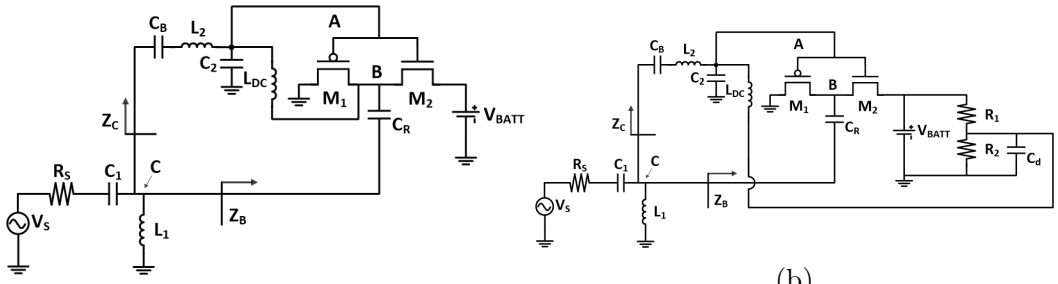
### 4.1.4 Biasing Voltage

In a two-transistor Dickson's rectifier shown in Fig. 4.1 (a), $M_1$ conducts as the voltage of middle point (B) goes below zero. This conduction will make a path to connect H to the ground. As the voltage of H goes higher than $V_{BATT}$, $M_2$ starts conducting connecting node H to the battery. Therefore, in a one-stage rectifier, the voltage of H has a DC offset that is approximately half of the $V_{BATT}$. Using the

same analysis, in an $N$-transistor rectifier ($N/2$ stage) shown in Fig. 2.1, DC offset of the point 1,2, and 3 in the rectifier chain are approximately equal to $V_{BATT}/N$, $2V_{BATT}/N$, and $3V_{BATT}/N$ respectively. Therefore, the DC offset of point k in the rectifier chain is approximately equal to $kV_{BATT}/N$, where $k \in [0, N-1]$. In the proposed one-stage Dickson's rectifier shown in Fig. 4.5, DC voltage at node B is equal to $V_{BATT}/2$, and for the rectifier to work correctly, a DC voltage must be added to node A which is equal to $V_{BATT}/2$ to equalize the DC offset of node A and B. $V_B$ and $L_{DC}$ are added for biasing the gate of transistors with a DC voltage required for the rectifier to work correctly. $L_{DC}$ is a large RF choke to pass the DC offset voltage and block the high frequencies signals. Likewise, in an N-transistor rectifier shown in Fig. 4.7, $V_{Bk}$ should be set to $kV_{BATT}/N$ for the rectifier to work. Adding $V_B$ which can be tuned individually, gives the designer ability to tune the DC voltage of the gates of the transistors, adding a degree of freedom in the design of the rectifiers to increase the efficiency and sensitivity of the rectifier. $V_B$ can be fine-tuned in the simulation or measurements to increase the efficiency and sensitivity as it will act as a constant compensation voltage. In this chapter, we explore two ways of producing $V_B$ as follows:

**Middle point**

In Fig. 4.5 the DC offset can be generated by connecting $L_{DC}$ to point B, as illustrated in Fig. 4.8 (a). Connecting $L_{DC}$ between node A and B makes their DC voltages equal while blocking the RF power of B going to A. This method does not consume any power for generating $V_B$, however, in this method as DC voltage of A is equal to B, it can not be tuned separately to increase the sensitivity and efficiency of the proposed rectifier.




(a) (b)

Figure 4.8: Producing $V_B$ (a) $L_{DC}$ connected to B, and (b) resistive divider connected to battery.

**Resistive divider**

Simulation results show that for a one-stage rectifier with battery load of 1.2 V, the best efficiency occurs at $V_B = 690\,mV$ instead of $V_{BATT}/2 = 600m\,V$. This compensation voltage can be produced using a resistive voltage divider connected to the battery, as shown in Fig. 4.8 (b). $R_1$ and $R_2$ can be chosen large enough to minimize the power consumption of the voltage divider. For instance, standard size $100M\,\Omega$ and $130M\,\Omega$ resistors can be chosen to produce $V_B = 680\,mV$ from the 1.2 V battery. The power consumption of the voltage divider in this manner is $6.3nW$ that will be added to the leakage of the transistors draining the battery when no power exists at the input.

## 4.2 Design Procedure of the Proposed Rectifier

The design of rectifiers and matching networks can be a time-consuming job as rectifiers are inherently non-linear, and their characteristics depend on their input power. In this section, a design procedure for the proposed rectifier is developed. The proposed rectifier's design variables assuming known transistor sizes are the first matching network consisting of $L_1$ and $C_1$ and the second matching network consisting of $L_2$, $C_2$. One way to design the proposed rectifier is using iterative methods to find the optimum matching network for the rectifier by iterating $C_1$, $L_1$, $C_2$, and $L_2$ until an optimal input matching and efficiency is obtained. However, this method can be very

time-consuming as each parameter change requires simulation, and each simulation requires thousands of cycles to reach the steady-state. Therefore, for reducing the design time, a design guideline is necessary, and the search space must be made as small as possible for fastening the design time. In order to find optimum $C_1$, $L_1$, $C_2$, and $L_2$ for a given input power level, the two matching networks can be designed separately and then fined-tuned. The first rectifier's matching network .i.e $L_1$ and $C_1$ can be obtained using iterative simulations or analytically methods for a conventional rectifier shown in Fig. 4.1 (a) . To further simplify the design, the second matching network can be simplified and instead of using both capacitor and inductor in it, only an inductor can be used as shown in Fig. 4.9. A matching network consisting of only an inductor will never result to perfect matching network conditions. However, as only a small percent of the input power must flow to the transistors' gates, a perfect matching condition is not required. Therefore, using an matching network with an inductor, the only remaining search variable is $L_2$. As in this new structure, $L_2$ is in series with the rectifier's transistors gate, a DC block capacitor of $C_B$ is added to decouple the DC values of the gate and the input voltages. Two critical observations are required before designing $L_2$. First, according to (4.17), the input impedance of the rectifier depends on its gate voltage. As the power transfer to the gate of the transistor increases (x in (4.19)), the voltage on the gate of the transistor also increases, leading to a lower rectifier's input impedance which will reduce the passive amplification at the input of the rectifier. This reduction on the rectifier's input voltage after some point may lead to a low input voltage level at the rectifier's input so that the rectifier is turned on, but the input voltage is lower than the battery voltage, and a current starts flowing from the battery to the input draining the battery. Secondly, x should not be very large as it gets larger the input power of the rectifier reduces lowering the output power. As the input resistance of the transistors' gates is much higher than the rectifier's input impedance, x is always a small value. Therefore, the second requirement will not be problematic in the design. However, the first condition can be

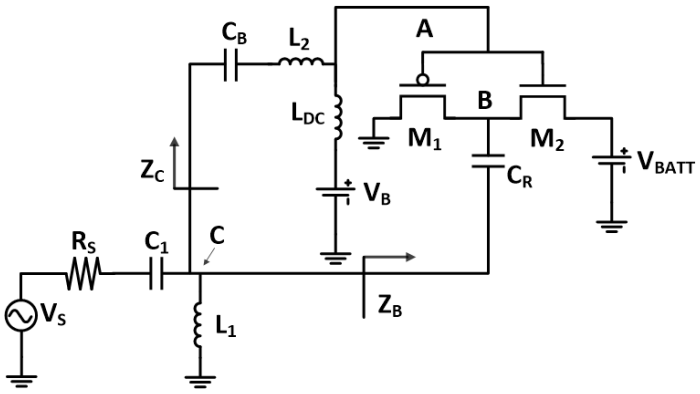



Figure 4.9: Simplified version of the proposed modified Dickson's rectifier.

troublesome if not designed carefully. If the transistor gate voltage gets high enough, the input impedance of the rectifier and so the input voltage of the rectifier reduces significantly leading to a current flowing from the battery to the rectifier draining the battery as the gate of the transistor is high enough to turn on the transistors in the rectifier chain. The optimum value of $L_2$ can be obtained by the iterative transient simulation to find the point that the best efficiency occurs. As the voltage gain (A) increases, the conduction current of the transistor increases, meaning that the input resistance of the rectifier is reduced. Therefore, when $L_2$ is iterated to the point that the best efficiency occurs, the rectifier's matching condition changes and after $L_2$ is chosen, the rectifier's matching network must be fine-tuned to find $L_1$ and $C_1$ that transfer the maximum power from the input power source to the rectifier.

## 4.3 Simulation Results

Dickson's rectifiers' design parameters are the optimum number of stages and the transistors' sizes. These parameters should be designed so that the rectifier achieves the best efficiency at the desired input power range as the optimum of the rectifier's parameters are different for each input power level. Generally, for high input power levels that the transistors conduction current is much higher than their leakage, transistors should be large to reduce the conduction loss. However, as the rectifier's transistors'

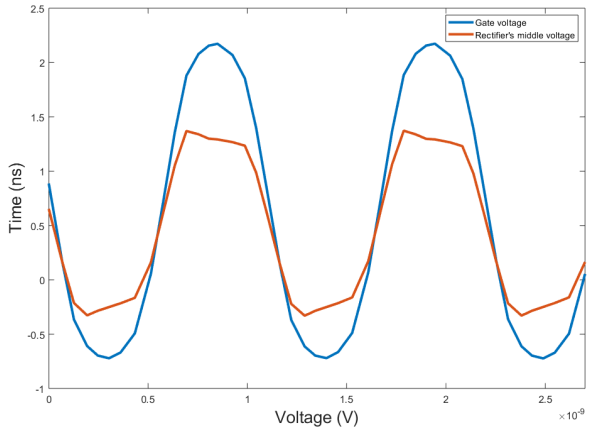



Figure 4.10: Transistors gate and rectifier's middle voltage wave forms for a battery load of 1.2 V where $\frac{W_p}{L_p} = \frac{200\mu m}{130nm}$, $\frac{W_n}{L_n} = \frac{100\mu m}{130nm}$, and $V_B = 690\,mV$.

sizes increase, the passive amplification at the input of the rectifier reduces because the input resistance of the rectifier reduces. Hence, rectifiers with large devices show lower sensitivities and efficiencies at low input power levels. Therefore, as there are not an optimum number of stages and rectifier's transistors' sizes that cause the best efficiency over a broad input power range, in the design of rectifiers first the minimum and maximum input power levels must be determined and then device's sizes and the number of stages must be selected. In this section, several rectifiers with different matching conditions and number of stages are explored to highlight the ability of the proposed rectifier for enhancing the efficiency under any circumstances. First rectifier is designed with $W_p/L_p = 200\,\mu m/130\,nm$, and $W_n/L_n = 100\,\mu m/130\,nm$ and has one stage. It is designed to work with the input power levels of $-10\,dBm$ to $5\,dBm$ and the battery load of 1.2 V and 1.5 V. The large devices are chosen as the rectifier is designed to work with high input power levels. The matching network is designed for the input power level of $5\,dBm$ and the operating frequency of 915 MHz. After simulations based on the design procedure mentioned in Sec. 4.2, $L1$, $C_1$, and $L_2$ are obtained 14.2 nH, 2.6 pF, 60 nH respectively for 5 $dBm$ input power level. $V_B$ is made by connecting a large RF choke between the rectifier's middle point and transistors' gates, as illustrated in Fig. 4.8. The voltage waveform of the rectifier's middle voltage

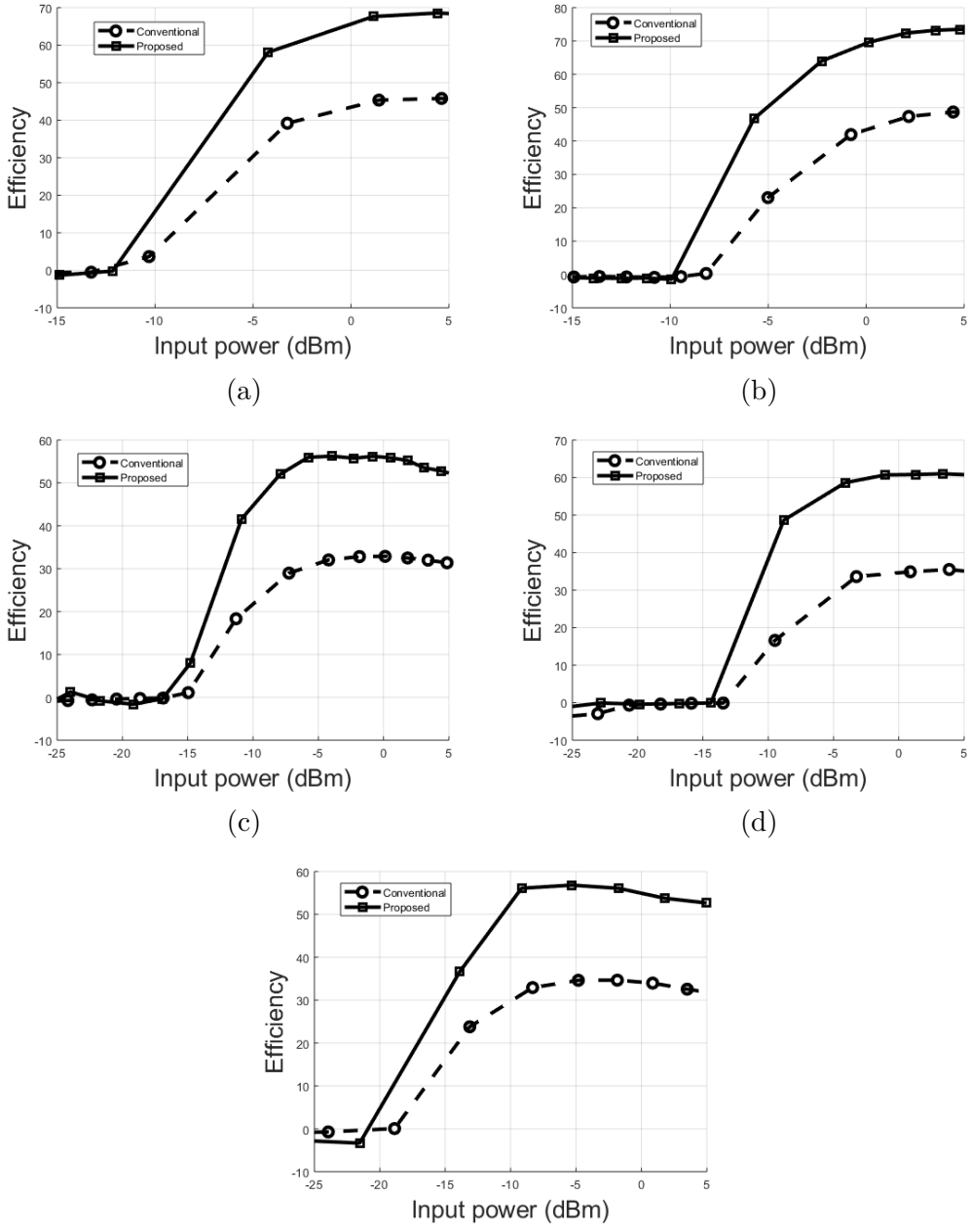
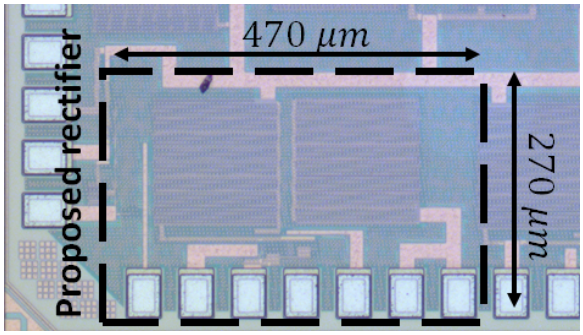


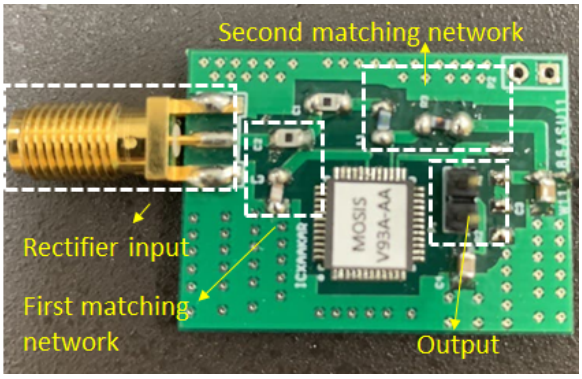

Figure 4.11: Efficiency plot of proposed vs. conventional rectifier, size1: $W_p/L_p = 200\ \mu m/130\ nm$, and $W_n/L_n = 100\ \mu m/130\ nm$, size2: $W_p/L_p = 100\ \mu m/130\ nm$, and $W_n/L_n = 50\ \mu m/130\ nm$, matching: $5\ dBm$ (a) one-stage, size1, for 1.2 V battery load, matching: $5\,dBm$ (b) one-stage, size1, for 1.5 V battery load, matching: $5\,dBm$, (c) two-stage, size2, for 1.2 V battery, matching: $0\,dBm$ (d) two-stage, size2, ,1.5 V battery load, matching: $0\,dBm$ . (e) two stage, size2, 1.2 V battery, matching: $-10\,dBm$.

(node B in Fig. 4.5) and rectifier's transistors' gates voltage (node A in Fig. 4.5) is shown in Fig. 4.10. As can be seen, the maximum of the rectifier's middle point voltage is clipped by the battery at 1.2 V. The maximum of transistors' gates voltage reached 2.17 V showing a 970 $mV$ voltage difference between the source and gate of the transistors and gain of 1.81. The input power coming from the source is 3.1 mW (5 $dBm$), and only 66 $\mu W$ of this power is transferred to the gate of transistors for producing this large voltage gain. The efficiency plot of the proposed rectifier compared to the conventional one with the same specifications for 1.2 V battery load is shown in Fig. 4.11 (a). For generating the plot, first the matching network is designed for 5 $dBm$ input power level and the operating frequency of 915 MHz, and then the input power is changed from $-15$ $dBm$ to 5 $dBm$. It should be mentioned that in all the simulations, inductors with quality factors of 50 are used which is a typical value in the off-chip CoilCraft inductors used for the measurement. As can be seen, the maximum efficiency of the proposed rectifier is 70.7% compared to the maximum efficiency of the conventional one, which is 46.12%. Likewise, the efficiency plot of conventional and proposed rectifiers for 1.5 V battery is shown in Fig. 4.11 (b). As can be seen, the maximum efficiency of the rectifier has changed from 49% to 74% showing significant improvement on the rectifier's efficiency.

For improving the sensitivity of the rectifier, the number of stages should be increased. In addition to that, for increasing the passive amplification at the input of the rectifier, smaller transistors are better as the input resistance of the rectifier increases. The proposed $N$-stage rectifier can be used to enhance the efficiency of conventional N-stage rectifiers. The second rectifier is designed with $W_p/L_p = 100\,\mu m/130\,nm$, and $W_n/L_n = 50\,\mu m/130\,nm$ and has two stages for increasing the sensitivity. The matching network components are designed for $0\,dBm$ input power level, and then the input power is swept from $-25$ $dBm$ to 5 $dBm$. The efficiency plots of the proposed two-stage rectifier for battery load of 1.2 V and 1.5 V are shown in Fig. 4.11 (c) and (d), respectively. As can be seen, compared to the one-stage rectifier, the sensitivity




(a)




(b)

Figure 4.12: (a) Die microphotograph of fabricated chip, (b) prototype PCB.

of the proposed rectifier has improved 4.74 $dBm$ and 5 $dBm$ for battery load of 1.2 V and 1.5 V battery, respectively.

Finally, the second rectifier's matching network is designed for $-10\,dBm$ and battery load of 1.2 V to increase the sensitivity further. As illustrated in Fig. 4.11 (e), the sensitivity has improved to $-20\,dBm$. It can be seen that at low input power levels also the proposed rectifier significantly improves the rectifier efficiency so that the maximum of efficiency changes from 34% to 57%.

## 4.4 Experiment Results

To verify the functionality of the proposed Dickson's rectifier, a single-stage rectifier with transistors' sizes of $W_p/L_p = 200\,\mu m/130\,nm$, and $W_n/L_n = 100\,\mu m/130\,nm$ was fabricated. The proposed rectifier was fabricated in TSMC 130-nm standard CMOS process with eight layers of metallization. Fig. 4.12 (a) shows the microphoto-

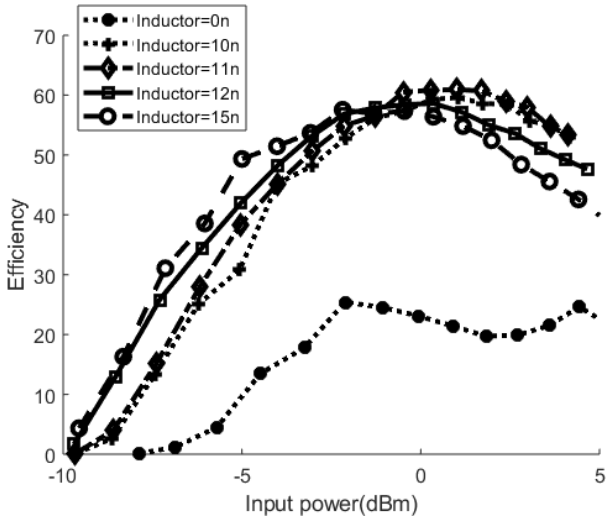



Figure 4.13: Measured efficiency of the rectifier for 1.2 V battery load.

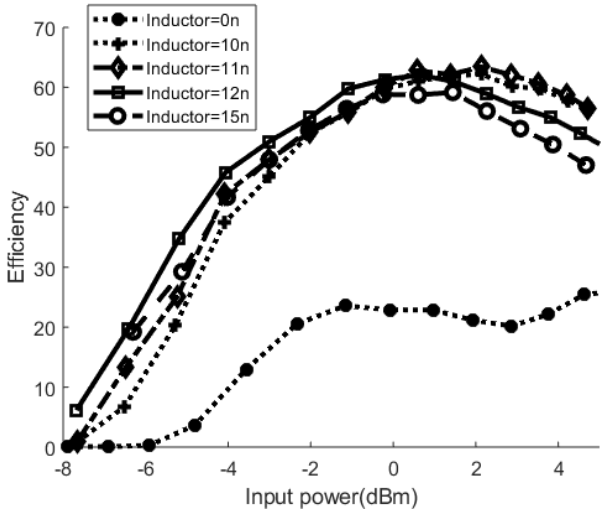



Figure 4.14: Measured efficiency of the rectifier for 1.5 V battery load.

Table 4.1: Performance summary and comparison of the proposed rectifier

| Reference | This work | [39] '17 JSSC | [41] '17 TCAS I | [27] '07 JSSC | [47] '15 TCAS II |
|---|---|---|---|---|---|
| Technology | 130 nm | 180 nm | 130 nm | 0.3 $\mu$m | 180 nm |
| Frequency | 915 MHz | 402 MHz | 953 MHz | 950 MHz | 915 MHz |
| Chip Area | 0.127 $mm^2$ | 1.44 $mm^2$ | 0.029 $mm^2$ | 0.64 $mm^2$ | - |
| Loading | Battery | 30 kΩ | 2 kΩ | Battery | 21.6 kΩ |
| Peak Efficiency | 61 % @ 1 dBm for 1.2 V 63.4 % @ 2.12 dBm for 1.5 V | 31.9 % @ -1 dBm | 69.5 % @ 5.2 dBm | 11 % @ -6 dBm | 32.5 % @ 0 dBm |
| Sensitivity[1] | -10 dBm for 1.2 V -8.5 dBm for 1.5 V | -12 dBm @ $R_L = 1M\Omega$, $V_{REC} = 1.38\ V$ | 0 dBm @ $R_L = 2k\Omega$, $V_{REC} = 1.0\ V$ [2] | -16 dBm @ $V_{REC} = 1.22\ V$ | -10 dBm @ $R_L = 1M\Omega$, $V_{REC} = 1.3\ V$ |
| Requirements | Secondary matching network | Control loop | Differential input, triple-well process | Battery | Native MOSFET |

[1]Sensitivity depends on the required output voltage, matching network and number of stages.

[2]Estimated from the figure.

graph of the fabricated chip. The die is wire bonded in a QFN package as this package has lower parasitics compared to other SMT packages. The output efficiency of the proposed rectifier for 1.2 V and 1.5 V output voltages is measured with KEITHLEY 236 Source Measure Unit (SMU) capable of measuring the current with nano ampere accuracy. As the output of the proposed rectifier is connected to the pin of the package by a high-Q bond wire, the sharp voltage change when the SMU output is turned on will result in oscillation at the output of the rectifier. This oscillation can damage the rectifier's transistors as the output voltage can reach to high voltages like 10 V. Therefore, a 20 $\Omega$ resistor is added between the SMU and output pin of the rectifier to lower the overall quality factor dampening the oscillation. As discussed in Sec. 4.1, as passive amplification plays a vital role in boosting the voltage of the input source before the rectifier and rectifier's transistors' gate, for increasing the overall efficiency, the matching network losses should be minimized. For the measurements, high-Q off-chip inductors are chosen from CoilCraft 0603CS series that typically show quality factors in the range of 40 to 98 for inductor values of 1.8 nH to 180 nH at 900 MHz making them suitable for the narrow-band matching networks used in the proposed rectifier to achieve high passive amplification. The chip is mounted on an FR-4 PCB as illustrated in Fig. 4.12 (b), and the PCB tracks are characterized using EM simulation done by Keysight Advanced Design System (ADS). These losses, along with the cable losses, are deducted from the input power of the proposed rectifier in calculation of the efficiency. The matching network presented in Fig. 4.9 is used for the measurement, and the input of the proposed rectifier is connected to a Vector Network Analyzer (VNA) to measure the S11 of the rectifier. As discussed in Sec. 4.2, first $L_2$ is set to zero and $L_1$ and $C_1$ are tuned to achieve a good matching condition at the operating frequency of 915 MHz. Then $L_2$ is changed to achieve the maximum efficiency. Finally, $L_1$ and $C_1$ are fine-tuned to obtain a good matching condition at 915 MHz. The efficiency of the proposed rectifier is measured for 1.2 V and 1.5 V battery voltages for different $L_2$ values. The measured efficiency plots of

the implemented rectifier for different $L_2$ values and the output voltage of 1.2 V is shown in Fig. 4.13. The matching network is designed at 915 MHz, and 3 $dBm$ input power level and the input power is then swept from $-10\,dBm$ to $5\,dBm$. The bias voltage is generated by a resistive divider consisting of 10 $M\Omega$ and 13 $M\Omega$ resistors connected to 1.2 V to produce approximately 680 $mV$. As can be seen, the rectifier achieves the maximum efficiency of 61% when $L_2$ is 11 nH, which is 40% higher of when $L_2 = 0$. In addition to that, the sensitivity of the rectifier for battery load of 1.2 V is $-10\,dBm$ which is close to the simulation results. Efficiency plot of the proposed rectifier for the output voltage of 1.5 V and different $L_2$ values is illustrated in Fig. 4.14. The maximum efficiency is measured 63.4% when $L_2$ is 11 nH which is 42% higher of when $L_2 = 0$.

Several factors can cause the discrepancy between simulation and measurement results. First, in the simulations, all the inductors are assumed to have a quality factor of 50. However, the quality factor of off-chip inductors used in the measurements varies and can be lower than 50. Secondly, the on-chip capacitors see a large parasitic capacitor between their bottom plate and substrate [57] lowering the input power reaching the rectifier. This parasitic capacitor is not modelled in the simulation. Table 4.1 summarizes the performance parameters of the proposed RFEH and compares them with those of the prior state-of-the-art works. As can be seen, the peak efficiency of the proposed rectifier is superior than other reported works except for [41] that requires a differential input generated by a balun or dipole antenna. As described in Sec. 4.1, the sensitivity of the rectifier can be further improved by increasing the number of stages at the expense of lowering the efficiency. Therefore, number of stages is mostly determined by the minimum sensitivity required for the intended application. As the fabricated prototype was designed to charge batteries with RF input power range of -10 to 5 dBm, a one-stage rectifier is utilized to achieve the highest efficiency. However, as shown in Fig. 4.11 (e), a two-stage rectifier can achieve a sensitivity of -20 dBm and peak efficiency of 57%.

## 4.5 Summary

A highly efficient RF energy harvester is proposed by passively producing an adaptive compensation voltage. The adaptive compensation voltage increases the $V_{gs}$ of transistors when they are conducting and makes the $V_{gs}$ negative when they are off. Therefore, the conduction and leakage loss are minimized simultaneously. The compensation voltage is produced by a secondary matching network that passively amplifies the input voltage of the rectifier and feeds it to the gate of transistors. Simulation and measurement results show that the proposed rectifier can increase the efficiency of the rectifier by at least 20% compared to that of the conventional Dickson's rectifier. For improving the input sensitivity, the proposed idea is generalized to an $N$-stage rectifier and simulation results show that the proposed idea can be used at different input power levels and numbers of stages to improve the efficiency over that of the conventional rectifiers. Finally, for verifying the efficacy of the proposed idea, a single-stage rectifier is fabricated in TSMC's standard 130-nm CMOS. The measurement results are in good agreement with the simulation results.

# Chapter 5

# Ultra-Low-Power WuTX with Built-In Analog Sensing Capabilities for Self-Powered WSN

This chapter[1] presents an ultra-low-power transmitter that simultaneously transmits the analog outputs of two sensors by generating short pulses at the output without using any power-hungry circuitry. The built-in sensing capability, along with the ultra-low power consumption of the presented transmitter, makes it ideal for self-powered schemes where the amount of available power for powering up the sensor is limited and, as stated in Chapters. 1 and 2, the operation of the transceiver must be intermittent (wake-up).

The OFF and ON times of the proposed transmitter output pulse are controlled by the two analog input signals. The generated pulse is then fed to a ring oscillator input to turn it on and then multiplied to a carrier frequency that upconverts the produced pulse frequency to ISM band frequencies. The NAND gate at the input of the ring oscillator turns on the oscillator when the baseband output pulse is ONE, which lowers the power consumption of the transmitter by keeping the oscillator off when there is no pulse to transmit. The carrier generator ring oscillator is designed in such a way that its frequency is 915 MHz when $V_{DD} = 600\ mV$ and 2.4 GHz when

[1]This chapter is based on a manuscript published in IEEE Transactions on Circuits and Systems I: Regular Papers [64].

$V_{DD} = 1\ V$, which adds a degree of freedom in the transmitter design by transmitting the modulated data at two different ISM band frequencies. After the multiplication of the baseband pulse with the carrier frequency, the generated signal is fed to a class E power amplifier with a high efficiency that transmits the signal via the output antenna. The generated short sinusoidal pulses at the output activate the power amplifier, which is the most power-consuming component in a portion of the transmission period leading to a significant reduction of the active power consumption of the circuit. In addition to that, using a ring oscillator, with a NAND gate at the input stage, eliminates the need for a power-hungry mixer and the ring oscillator does not oscillate if the pulse generator is off, which will reduce both idle and active power consumption.

## 5.1 Proposed Ultra-Low-Power Transmitter

The proposed transmitter is realized by an ultra-low-power relaxation oscillator consisting of a comparator biased in subthreshold followed by an inverter chain to produce a delay between the comparator output and $S_1$ switch. The voltage references used to bias the comparator are designed to consume a very low amount of power (nW). The proposed architecture eliminates the need for complex circuits, such as ADC or DAC modulators, by incorporating variable capacitors (varactors) to modulate the LOW and HIGH time of the generated pulse according to the two analog input signals. As shown in Fig. 5.1, in the relaxation oscillator, variable capacitor (varactor) of $C_1$ is charged by $I_{REF}$ until it reaches $V_{REF1}$ then it will be discharged by $S_1$. The frequency and the pulse width of the generated pulses depend on the value of $C_1$ and the delay of the inverter chain connecting the output of the comparator to switch $S_1$, respectively. Then the generated pulse incorporating the information of two analog sensor signals is multiplied by the ring oscillator output to be transmitted in the allocated ISM band.

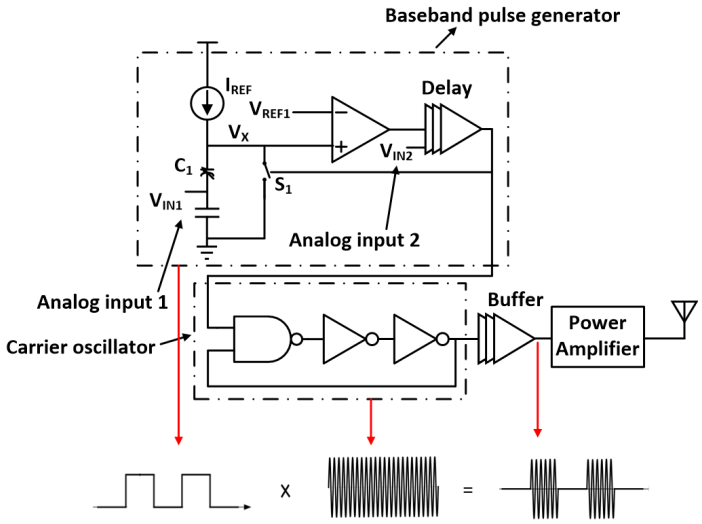



Figure 5.1: Proposed ultra-low-power transmitter.

### 5.1.1 Baseband Pulse Generator

#### Amplitude to Time Modulation

As it is possible to transmit the data of two sensors simultaneously using a single transmission signal, a pulse is produced with its LOW time, the time that the output pulse is ZERO, and the HIGH time, the time that the output pulse ONE, modulated with the corresponding analog sensor outputs. The pulse generator consisting of a variable capacitor, a current source, a comparator and two inverters working as a delay line is shown in Fig. 5.1. Assuming a zero initial voltage for the variable capacitor ($C_1$) and the output, $C_1$ starts charging by $I_{REF}$ until $V_X$ reaches $V_{REF1}$ when the comparator positive terminal voltage will be larger than its negative terminal voltage producing $V_{DD}$ at its output. The time that it takes for $V_X$ to reach $V_{REF1}$ is proportional to the value of $C_1$ and $I_{REF}$ and is called $T_{SENSE1}$. At this point, $S_1$ switch will be turned on after a delay, ($T_{SENSE2}$), discharging $C_1$. Therefore, the generated pulse outputs ZERO during $T_{SENSE1}+T_{SENSE2}$ consisting of the time that the capacitor is charging and $V_X$ is less than $V_{REF1}$ which is named $T_{SENSE1}$, and the delay it takes the comparator output to reach to the pulse generator output to make it ONE ($T_{SENSE2}$). After the output voltage of the pulse generator becomes ONE, $S_1$

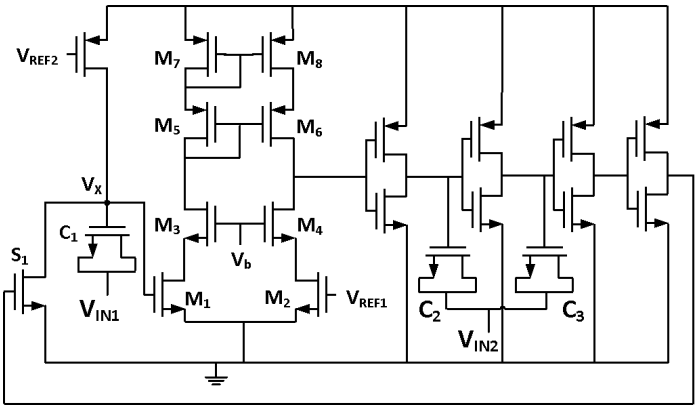



Figure 5.2: Implementation of the pulse generator circuit.

will be activated discharging $C_1$ and making the comparator output ZERO so that after a delay of ($T_{SENSE2}$) which again is the delay between when the comparator output and the output voltage of the pulse generator output become ZERO, so

$$\begin{aligned} T_{LOW} &= T_{SENSE1} + T_{SENSE2}, \\ T_{HIGH} &= T_{SENSE2}, \\ T &= T_{SENSE1} + 2\,T_{SENSE2} \end{aligned} \tag{5.1}$$

where $T$ is the output pulse period. $T_{SENSE1}$, the time that is required for $V_X$ to reach $V_{REF1}$ depends on the value of $C_1$ and $I_{REF}$. Assuming that $I_{REF}$ does not change in the charging cycle,

$$\begin{aligned} I_{REF} &= C_1 \frac{dV_X}{dt}, \\ \Rightarrow T_{SENSE1} &= \frac{C_1 V_{REF1}}{I_{REF}}. \end{aligned} \tag{5.2}$$

where $C_1$ is the capacitance seen at node $V_X$ to ground. $T_{SENSE2}$, the time that is required for the pulse generator output to change from ONE to ZERO after $S_1$ is activated is determined by the delay line. For making the $C_1$ as a function of $V_{IN1}$, it has been realized as a MOS varactor with its drain-source terminal connected to the sensor output so that $T_{SENSE1}$ can be changed linearly via the sensor output voltage. The circuit implementation of the pulse generator is shown in Fig. 5.2. $C_1$, $C_2$, and $C_3$ are "accumulation-mode" MOS varactors which their capacitance can be obtained

by ([57])

$$C_{var}(V_{GS}) = \frac{C_{max} - C_{min}}{2} tanh(a + \frac{V_{GS}}{V_0}) + \frac{C_{max} + C_{min}}{2} \tag{5.3}$$

where $a$ and $V_0$ are fitting slope, and $C_{min}$ and $C_{max}$ include the gate-drain and gate-source overlap capacitance. According to (5.2), by connecting a sensor's analog output voltage to $V_{IN1}$ (source-drain terminal of $C_1$ varactor), $T_{SENSE1}$ of the pulse, and therefore its frequency, can be changed as $C_1$ changes. However, as $C_1$ is charging by $I_{REF}$, its gate voltage is increasing so that its $V_{GS}$ and capacitance changes during the charging cycle. For calculating $T_{SENSE1}$, instead of using (5.3) that complicates the calculation, it can be assumed that $C_1$ varactor changes linearly from $C_{min}$ to $C_{max}$ when $V_{GS}$ changes from $-V_M$ to $V_M$ so that the varactor value as a function of its $V_{GS}$ will be

$$C_{var}(V_{GS}) = A(V_{GS}) + D \tag{5.4}$$

where $A = (C_{max} - C_{min})/2V_M$ and $D = (C_{max} + C_{min})/2$.

To calculate $T_{SENSE1}$, the linear approximation approximation for the varactor must be inserted in (5.2).

$$I_{REF}dt = [A(V_X - V_{IN1}) + D]\ d(V_X - V_{IN1}) \tag{5.5}$$

Integrating from both sides, when $V_X$ changes from 0 to $V_{REF1}$, $T_{SENSE1}$ can be obtained as follows:

$$T_{SENSE1} = \Big[\frac{AV_{REF1}^2}{2I_{REF}} + \frac{DV_{REF1}}{I_{REF}} - \frac{AV_{REF1}V_{IN1}}{I_{REF}}\Big] \tag{5.6}$$

As can be seen, $T_{SENSE1}$ will be reduced as $V_{IN1}$ increases. The capacitance reduces as $V_{IN1}$ increases so that it takes less time for the capacitor to charge up to $V_{REF1}$. $T_{SENSE1}$ as a function of $V_{IN1}$ obtained by post-layout simulation is shown in Fig. 5.3. As can be seen, by changing $V_{IN1}$ from 0 to 1.2 V, $T_{SENSE1}$ changes from 139 ns to 94 ns. Affected by nonlinearity of the varactor value, $T_{SENSE1}$ does not change linearly with $V_{IN1}$, as shown in (5.6). In order to convert back $T_{SENSE1}$ of the received signal at the base station to its corresponding amplitude, it is imperative to find $V_{IN1}$ as

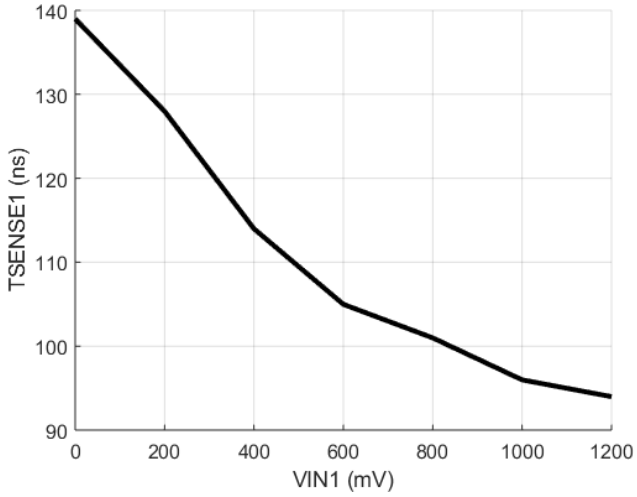



Figure 5.3: $T_{SENSE1}$ vs. $V_{IN1}$.

a function of $T_{SENSE1}$. Using the curve Fitting Tool in Matlab and the simulation results, $V_{IN1}$ is calculated as an order 5 polynomial function of $T_{SENSE1}$:

$$\begin{aligned} V_{IN1} = & -5.022e-8*(T_{SENSE1})^5 + 2.92e-5*(T_{SENSE1})^4 \\ & - 6.78e-3*(T_{SENSE1})^3 + 0.7864*(T_{SENSE1})^2 \\ & - 45.61*(T_{SENSE1}) + 1060 \end{aligned} \tag{5.7}$$

where $V_{IN1}$ is in Volts and $T_{SENSE1}$ in nanoseconds and $R^2$ of the fitted curve is 0.9974. Eq. (5.7) can be used at the receiver to find the sensor's output voltage, $V_{IN1}$, based on the measured $T_{SENSE1}$ easily using a microprocessor. Assuming that $I_{REF}$ does not depend on $V_{DD}$, $T_{SENSE1}$ is independent of the supply voltage, therefore, it is not required to measure its value for different supply voltages.

In the proposed baseband generator, after $V_X$ reaches $V_{REF1}$, the comparator output becomes ONE. Then, after a delay resulted from the inverter chain the output of the pulse generator becomes ONE and switch $S_1$ will be activated to discharge $C_1$ capacitor and make $V_X$ equal to ZERO. After $V_X$ becomes ZERO, the comparator output changes from ONE to ZERO and after a delay, the baseband generator output will be ZERO. So, the width of the generated pulse ($T_{SENSE2}$) is equal to the delay from the comparator input to the pulse generator output. By tuning the delay of the inverter chain, the pulse width ($T_{SENSE2}$) can be controlled. In the proposed trans-

mitter, variable capacitors of $C_2$ and $C_3$ are used to change the delay of the inverters by tuning its RC time constant. Therefore, by connecting the second sensor's output to the controlling voltage of $C_2$ and $C_3$, the analog input can be converted to the $T_{HIGH}$ of the generated which is equal to $T_{SENSE2}$. The simplicity of the proposed circuit can be received and demodulated simply by using a power detector which is discussed in section 5.2. In the proposed circuit, the buffer line is made by connecting four inverters in series that are loaded by $C_2$ and $C_3$ which their capacitance is tuned by $V_{IN2}$. For understanding the delay of the buffer line first it is needed to calculate the RC time constant of a single inverter which is

$$\tau = R_{on}C \tag{5.8}$$

where $R_{on} = 1/(\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH}))$ is the transistor on resistance when it is working in triode region and $C = C_L + C_{DB}$ is the capacitance seen at the output of the inverter which is the drain capacitances plus load capacitance. For controlling the delay of the line, $C_2$ and $C_3$ are used to change the output capacitance of the inverter and therefore its RC time constant. $C_2$ and $C_3$ decrease with increasing $V_{IN2}$ leading to a lower RC time constant and lower delay. MOSFETs in the inverter chain work in the triode region and their input switches from 0 to $V_{DD}$. Therefore, their on resistance depends on the supply voltage and it is essential to determine $T_{SENSE2}$ for $V_{DD} = 600\ mV$ and $V_{DD} = 1\ V$. The pulse width ($T_{SENSE2}$) versus $V_{IN2}$ for different supply voltages obtained by the post-layout simulation is shown in Fig. 5.4(a) and (b), respectively.

Similarly, for finding the relationship between $V_{IN2}$ and $T_{SENSE2}$, the Curve Fitting tool has been used and $V_{IN2}$ as a function of pulse width ($T_{SENSE2}$) for $V_{DD} = 600\ mV$ is obtained:

$$\begin{aligned} V_{IN2} = {} & -2.754e-9*(T_{SENSE2})^5 + 1.23e-6*(T_{SENSE2})^4 \\ & - 2.173e-4*(T_{SENSE2})^3 + 1.902e-2*(T_{SENSE2})^2 \\ & - 0.8354*(T_{SENSE2}) + 15.38 \end{aligned} \tag{5.9}$$

where $V_{IN2}$ is in Volts and $T_{SENSE2}$ in nanoseconds and $R^2$ of the fitted curve is 0.9991.

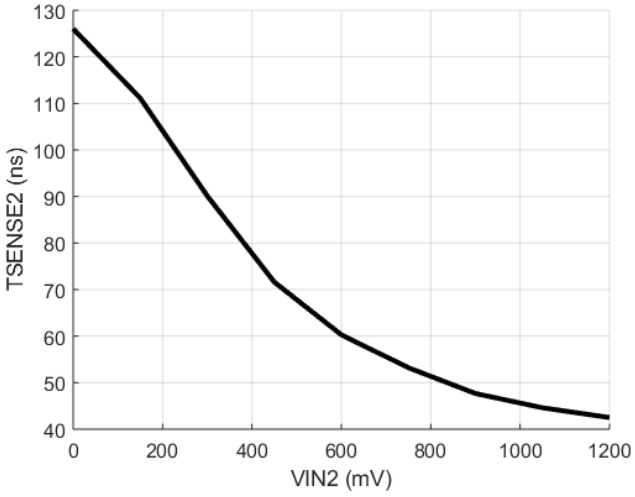
The output waveform of the pulse generator for different $V_{IN1}$ obtained by the simulation is illustrated in Fig. 5.5. As will be discussed in the following part, a carrier frequency is multiplied by the generated pulse to upconvert the generated signal to the required frequency band for communication.

**Direct Capacitive Sensing**

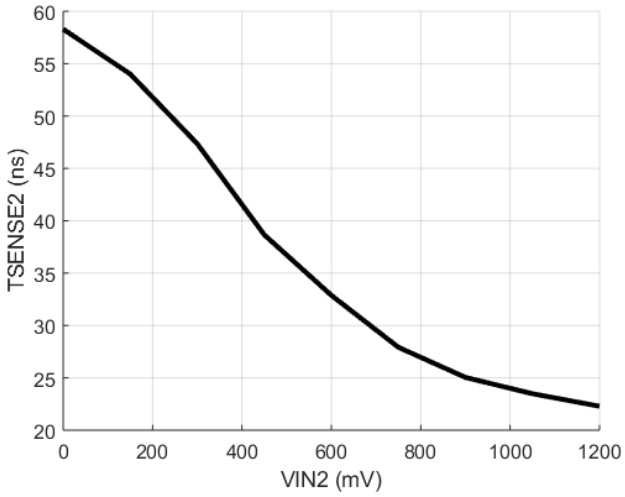
Capacitive sensors are widely used for measuring parameters such as pressure, displacement, force, humidity, fluid levels, acceleration and many others [65]. Usually, capacitive sensors need auxiliary circuitry to read the value of the capacitor and convert it to a digital signal before it can be sent by a transmitter. The proposed transmitter can transmit the value of a capacitive sensor without requiring any auxiliary circuit by directly connecting the sensor between the ground and $V_X$, in Fig. 5.1. As illustrated in Eq. 5.2, $T_{SENSE1}$ depends on the value of the capacitance seen from $V_X$ to the ground. By connecting the capacitive sensor between $V_X$ and ground, $T_{SENSE1}$ of the generated pulse will directly be related to the capacitive sensor value and therefore transmits its value to the base station receiver without requiring other circuitry like ADC or DAC.

**Comparator**

$M_1$-$M_7$ construct a telescopic differential amplifier working in the sub-threshold region which does not use a bias current produced by a tail current source. $V_{REF1}$ is made by an nW voltage reference and is set to be 300 mV. N-channel MOSFETs in the CMOS technology which has been used have a threshold voltage of near 350 $mV$. Therefore, $M_2$ that its $V_{GS}$ is 300 mV work in the subthreshold region. When $V_X$ becomes higher than $V_{REF1}$, because $V_{GS}$ of $M_1$ becomes larger than $M_2$, the output of the comparator becomes $V_{DD}$ because of the high gain of the comparator. For

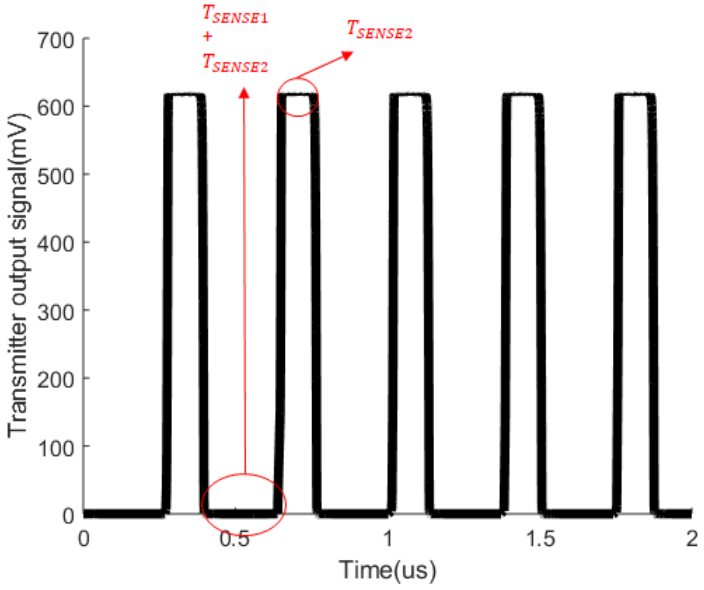



(a)

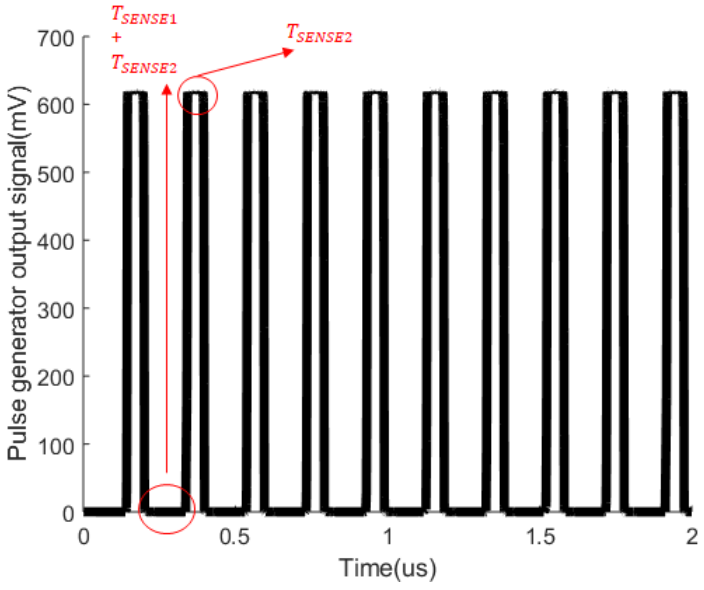



(b)

Figure 5.4: $T_{SENSE2}$ vs. $V_{IN2}$ for (a) $V_{DD} = 600\,mV$ and (b) $V_{DD} = 1\,V$ obtained by simulation.




(a)




(b)

Figure 5.5: Pulse generator output voltage when $V_{DD} = 600\ mV$ and (a) $V_{IN2} = 0$ (b) $V_{IN2} = 600\ mV$ obtained by simulation.

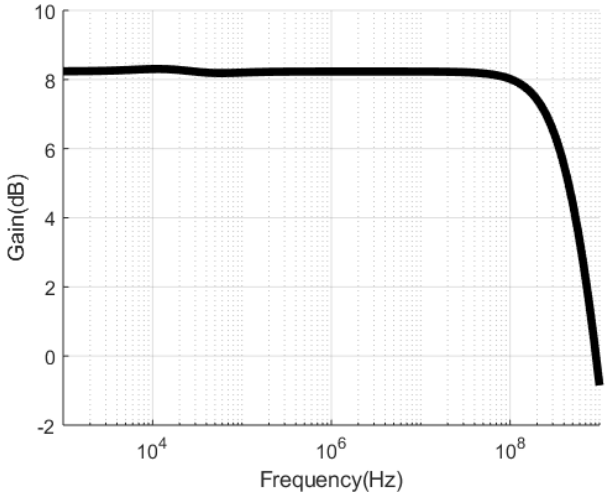



Figure 5.6: Comparator frequency response when $V_{DD} = 600\ mV$.

understanding the behavior of the comparator it is essential to find its characteristics. For finding the gain of the comparator its drain current must be obtained. The drain current of a transistor working in the subthreshold region can be obtained from Eq. (3.4). Therefore, transconductance and output resistance of a MOSFET working in subthreshold region will be

$$\begin{aligned} gm &= \frac{\partial I_D}{\partial V_{GS}} = \frac{I_d}{nV_T}, \\ r_o &= \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\lambda_{sub} I_d} \end{aligned} \tag{5.10}$$

Assuming $V_X = V_{REF1} + \Delta V_{in}$, $\Delta V_{out}$ is:

$$\Delta V_{out} = g_{m1,2} R_o \Delta V_{in} \tag{5.11}$$

where $g_{m1,2}$ is the transconductance of the transistors biased with $V_{REF1}$ and $R_o \approx (g_{m4} r_{o2} r_{o4}) || (g_{m6} r_{o6} r_{o8})$.

The frequency response of the comparator obtained by simulation when $V_{DD} = 600\ mV$ is shown in Fig. 5.6. The comparator shows a gain of 8.24 dB with -3 dB cutoff frequency of 427MHz in a 65 nm CMOS process. The gain of the comparator is further improved by inverters after the comparator.

When $V_X = 0$, the current path through $M_2$ and $M_4$ discharges the capacitors at

the output of the comparator making the output 0 and as $M_1$, $M_3$, $M_5$, $M_7$, $M_8$ and $M_6$ are off, no current path exist between $V_{DD}$ and the ground except for the leakage currents. Therefore, comparator current when $V_X = 0$ and $V_{REF1} = 300\ mV$ and $V_{DD} = 600\ mV$, obtained by simulation is 7.74 $nA$ that is caused by the leakage currents.

**Voltage reference**

To reduce the idle power consumption of the circuit, biasing circuitry and voltage references must consume very low power. Throughout the years several configurations for making a voltage reference have been introduced. For instance, in the bandgap voltage references, using bipolar transistors, a temperature voltage-independent voltage can be achieved which is approximately 1.2 V. Although bandgap voltage references show good behavior against temperature variation, they cannot be used in low-voltage and low-power applications as the supply voltage cannot be below 1.8 V ([66]). One interesting approach to achieve a low-voltage and low-power voltage reference is using MOSFETs in the subthreshold region. In addition to that, these references can be implemented resistorless which makes them appropriate for on-chip designs with a budget on the area.

In the proposed transmitter a SBSCM voltage reference introduced in [66] is used to create an ultra-low-power CMOS resistorless voltage reference for generating $V_{REF1}$ and $V_{REF2}$ as shown in Fig. 5.7 where $M_1, M_2, M_4$ are high-Vt transistors. $V_{REF1}$ is obtained by

$$\begin{aligned} V_{REF1} = \frac{V_{T2}(T_0) - V_{T3}(T_0)}{n_3\epsilon} + \big(\frac{n_3 - n_2}{n_1 n_3 \epsilon}\big) V_{T1}(T_0) \\ + T_0 \big(\frac{n_1(\alpha_{T2} - \alpha_{T3}) - (n_2 - n_3)\alpha_{T1}}{n_1 n_3 \epsilon}\big) \end{aligned} \tag{5.12}$$

where $V_{T2}$ and $V_{T3}$ are the threshold voltages of $M_2$ and $M_3$ respectively, $n_x$ is the subthreshold slope factor of $M_x$ transistor, $\alpha_T$ is the first derivative of the thershold voltage with respect to temperature, $\epsilon = 1 - (n_2 - n_3)/(n_1 n_3)$.

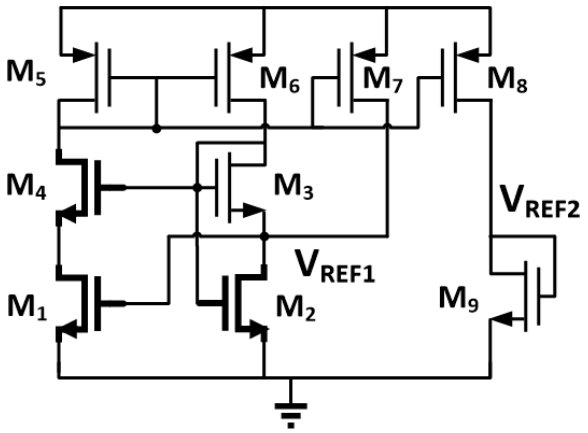



Figure 5.7: Reference voltage generator.

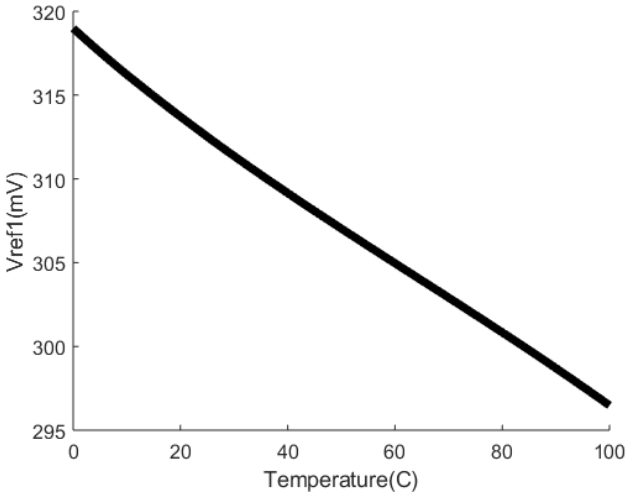



Figure 5.8: $V_{REF1}$ vs. temperature.

$V_{REF1}$ for different working temperatures is shown in Fig. 5.8. As can be seen, the voltage reference temperature changes from 319 $mV$ to 297 $mV$ as the temperature changes from 0 to 100 centigrade degrees. 22 $mV$ is low enough that makes the sensor suitable to be placed even in harsh environments that temperature may change drastically while the transmitter is working. The simulated power consumption of the voltage reference generator is 2.4 $nW$.

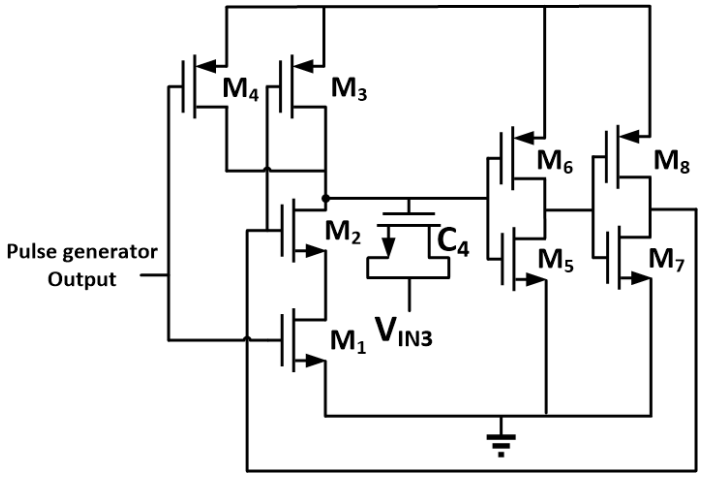
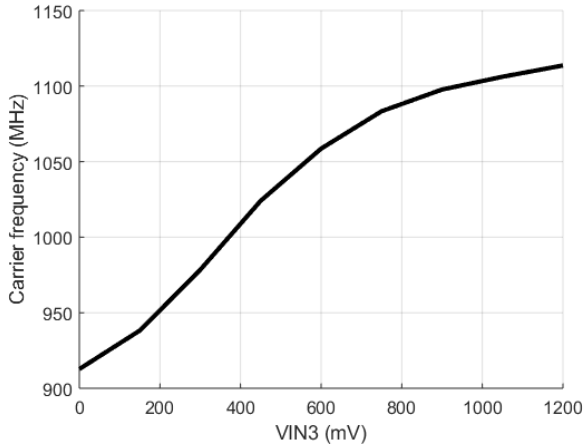



Figure 5.9: Carrier oscillator.

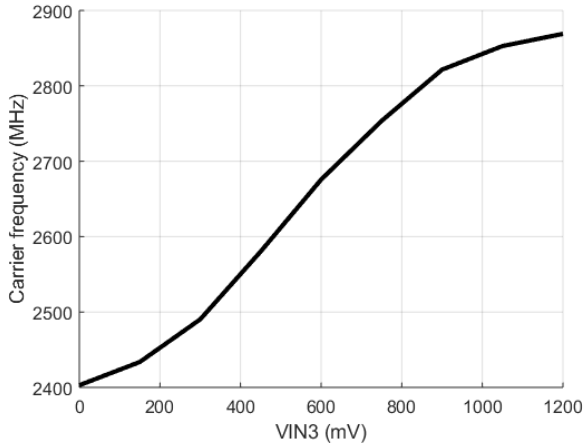
### 5.1.2 Carrier Clock Generator

In the proposed transmitter a simple ring oscillator consisting of two inverters and a NAND gate is used, as can be seen in Figs. 5.1 and 5.9, to generate the carrier frequency. The generated pulse made in the previous stage is fed to one of the NAND inputs for turning on the oscillator when a pulse must be transmitted. Leveraged the NAND gate in the input of the carrier generator oscillator turns off the oscillator when the pulse generator output is ZERO to minimize the power consumption as it shuts down a high-frequency oscillator that consumes large dynamic power. To accurately tune the carrier frequency after fabrication, a MOS varactor ($C_4$) has been used as the load of the NAND gate in the ring oscillator as can be seen in Fig. 5.9. The simulation results of the carrier generator output frequency for different tuning voltages($V_{IN3}$) and $V_{DD}$ has been shown in Fig. 5.10. As can be seen, the output frequency changes from 912 $MHz$ when $V_{IN3} = 0\ V$ to 1.113 $GHz$ when $V_{IN3} = 1.2\ V$ at supply voltage of $V_{DD} = 600\ mV$ and from 2.4029 $GHz$ when $V_{IN3} = 0\ V$ to 2.869 $GHz$ when $V_{IN3} = 1.2\ V$ at supply voltage of $V_{DD} = 1\ V$.

The final output waveform of the created signal, which is the product of the carrier frequency and the narrow pulse, is illustrated in Fig. 5.11.




(a)




(b)

Figure 5.10: Carrier frequency for different tuning voltages ($V_{IN3}$) when (a) $V_{DD} = 600\ mV$ (b) $V_{DD} = 1\ V$ .

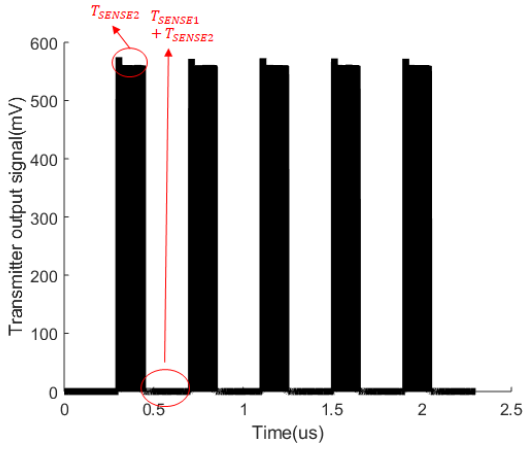



Figure 5.11: Output voltage of the signal generator when $V_{DD} = 600\ mV$, $V_{IN1} = 0\ V$, and $V_{IN2} = 0\ V$ obtained by simulation.

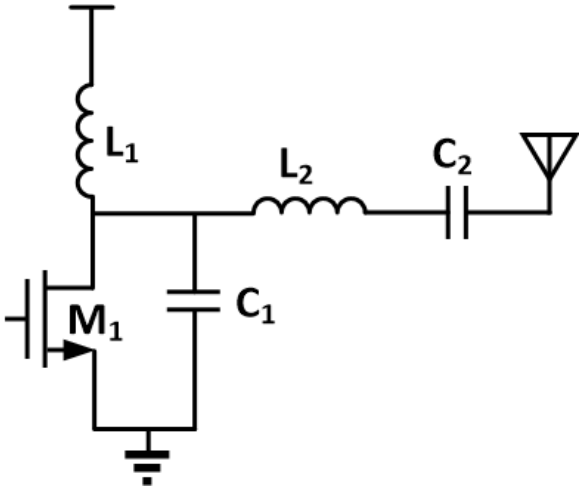



Figure 5.12: Class E power amplifier.

### 5.1.3 Power Amplifier

Output power, gain, efficiency, and linearity are the most important factors in the design of RF power amplifiers [67]. An RF power amplifier can be realized by transconductance amplifiers, like class-A and B amplifiers, in which there are voltage-controlled current sources that convert an input voltage to the current required for the output. Transconductance amplifiers need biasing and consume static current and their efficiency is limited but show good linearity compared to switching amplifiers([57]). In recent years, due to simplicity and high-efficiency, Class E power amplifiers have gained popularity. In a Class E amplifier, the transistor operates as an on/off switch and the overlap of high voltage and current is avoided by tuning the reactive components in the output matching circuit [68]. In the proposed transmitter, a parallel-circuit class E amplifier is leveraged at the output to eliminate the biasing need for the output amplifier and to increase the efficiency of active power consumption. Using a power amplifier at the output gives the ability to tune the output power to gain different working ranges and power consumption which is not feasible when a power oscillator or backscattering method is used. A typical Class E amplifier is shown in Fig. 5.12. The load network includes a finite dc-feed inductance $L_1$, a parallel capacitance $C_1$, and a series resonator consists of $L_2$ and $C_2$ tuned to

the fundamental frequency that passes current at the desired frequency to the load and inhibits it at other ones and the load resistor R. Assuming a signal with a 50% duty cycle on the input, that is on till $wt = \pi$ and is off till $wt = 2\pi$, for a lossless operation it is essential to apply the following conditions prior to the start of the switch to eliminate power loss [69]:

$$\begin{cases} v(wt)\Big|_{wt=2\pi} = 0 \\ \dfrac{dv(wt)}{dwt}\Big|_{wt=2\pi} = 0 \end{cases} \tag{5.13}$$

where $v_{wt}$ is the voltage across the switch.

Using (5.13) and an additional equation defining the supply voltage $V_{DD}$ from Fourier series expansion, the design of a class E amplifier can be done by ([69, 70]):

$$\begin{cases} R_{Loptimum} = 1.365\ \dfrac{V_{DD}^2}{P_{out}} \\ L1 = 0.732\ \dfrac{R_{Loptimum}}{\omega} \\ C1 = \dfrac{0.685}{\omega R_{Loptimum}} \end{cases} \tag{5.14}$$

where $R_{Loptimum}$ is the optimum load resistance for the specified values of $V_{DD}$ and output power. The output resonator used to attenuate harmonics at the output can be designed by specifying the loaded quality factor of the load. In this work, the power amplifier output must be connected to a 50 Ω load; however, as $R_{Loptimum}$ is different from the required 50 Ω, a matching network is required which can be combined with the resonator to obtain the circuit shown in Fig. 5.13.

$C_2$, $C_3$ and $L_2$ must be designed so that the load of 50 Ω is transferred to $R_{Loptimum}$ by the matching network. The mentioned equations assume the transistor to be an ideal switch, however, the transistor on resistance ($R_{on}$) affects the efficiency and must be minimized by increasing the width of the transistor. On the other hand, increasing the width of the power amplifier increases the parasitic capacitance seen at its gate causing a large buffer at its input to amplify the transmitter output before

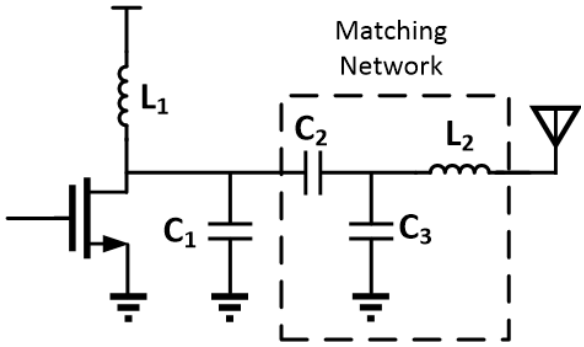



Figure 5.13: Class E power amplifier with matching network.

the power amplifier. Having a large buffer before the power amplifier will increase the active power consumption, because of switching loss, due to the added leakage caused by large transistors. In the proposed transmitter, a tapered inverter before the power amplifier has been used. The tradeoff between the size of the buffer's and power amplifier's transistor, efficiency and power consumption mainly depends on the required output power and was optimized by parametric simulations. In the proposed amplifier, high output power wanted to be tested so that the output power amplifier is designed to have the output of -1 dBm. Simulation results show that the designed power amplifier has 70.63% at the desired output power when $V_{DD} = 600\ mV$. The power amplifier could further be improved if the switching transistor is wider imposing extra leakage current.

## 5.2 Decoding Generated Signal

For demodulating the transmitter output signal, an envelope detector as shown in Fig. 5.14 can be used. An envelope detector can detect the input energy by passing the received signal through a non-linear element and then a low-pass filter to eliminate high-frequency components. After the envelope detector, the baseband pulse is received which is at low frequency and can be decoded by using a low-cost microprocessor with a moderate accuracy timer. For detecting the pulse frequency, the timer waits until RF power is reached the antenna and detected by the power detector and

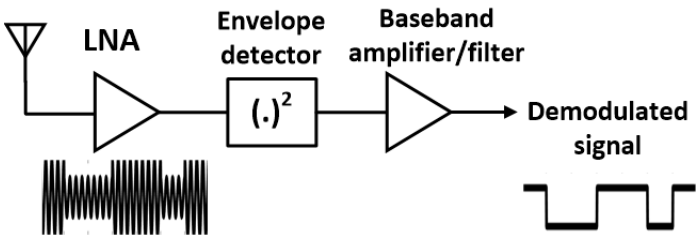



Figure 5.14: Power detector at the receiver.

starts counting until another pulse is received. The time difference between two consecutive pulses can be mapped easily to the pulse frequency and the sensor voltage. Similarly, the other sensor output which is coded in the pulse width can be detected by a second timer that counts the duration of the received power when it is larger than a certain threshold. By having the pulse frequency and pulse width, $T_{SENSE1}$ also can be calculated using Eq. (5.1).

After $T_{SENSE1}$ and $T_{SENSE2}$ are calculated, the sensors' output voltages can be obtained by using Eqs. (5.7) and (5.9). The simplicity of the demodulator of the transmitter's output waveform allows the receiver to be less complex hence consuming very low power.

## 5.3 Off, Active and Idle Power Consumption of the Proposed Transmitter

The total power consumption of the transmitter comprises of its leakage power when the transmitter is turned off by high-Vt switches, the power consumption of the pulse generator and high-frequency ring oscillator, and power amplifier drivers (signal generator) that generate the signal that is fed to the power amplifier, and the power consumption of the power amplifier. Moreover, in the proposed transmitter, because of the short pulses at the output, the total power consumption is a function of $T_{SENSE1}$ and $T_{SENSE2}$:

$$\begin{aligned} P_{TX,total} &= P_{TX,off} + P_{signalgenerator}\left(T_{SENSE1}, T_{SENSE2}\right) \\ &+ D \times P_{poweramplifier} \end{aligned} \tag{5.15}$$

where D is the duty cycle of the generated pulse and is equal to $T_{SENSE2}/(T_{SENSE1} + 2\ T_{SENSE2})$. Therefore, in the proposed transmitter, by increasing $T_{SENSE1}$ and decreasing $T_{SENSE2}$, the final signal's duty cycle can be reduced which will lower the total power consumption of the proposed transmitter leading to significant power reduction compared to other work that use other modulation techniques as the short pulses at the output will reduce the power amplifier operation time. The designed power amplifier has a 70.63 % efficiency while consuming a total power of 1.113 $mW$ for the output power of $-1\ dBm$. The power consumption of the signal generator like power amplifier also depends on $T_{SENSE1}$ and $T_{SENSE2}$ as only in the $T_{SENSE1}$ the high-frequency oscillator is activated. In the LOW time, as the high-frequency oscillator is turned off the power consumption will be equal to the idle power consumption which is the time the output pulse is ZERO and only the comparator is on. In the HIGH time, when the output of the pulse generator is ONE, the high-frequency oscillator and the power amplifier driving buffers consume most of the power. The plot of the signal generator power consumption including the power amplifier driving buffers versus $V_{IN1}$ and $V_{IN2}$ when $V_{DD} = 600\ mV$ and $I_{REF} = 8.2\ \mu A$ is shown in Fig. 5.15. As can be seen, the highest power consumption of 30 $\mu W$ occurs when $V_{IN1}$ is maximum ($T_{SENSE1}$ is minimum) and $V_{IN2}$ is minimum ($T_{SENSE2}$ is maximum) whereas the lowest power consumption of $10.8\mu W$ occurs when $V_{IN1}$ is minimum ($T_{SENSE1}$ is maximum) and $V_{IN2}$ is maximum ($T_{SENSE2}$ is minimum).

Finally, the total power consumption of the transmitter including the power amplifier with the output power of -1dBm when $V_{DD} = 600mV$ and $I_{REF} = 8.2\mu A$ is 271.46 $\mu W$ when $V_{IN1} = 0$ and $V_{IN2} = 1.2V$, and the 667 $\mu W$ when $V_{IN1} = 1.2V$ and $V_{IN2} = 0$.

The total power consumption of the proposed transmitter can be reduced further by decreasing the output pulse duty-cycle to extreme limits. This can be done by increasing $T_{SENSE1}$ or decreasing $T_{SENSE2}$. In the proposed transmitter, $T_{SENSE1}$ can be increased by decreasing the charging current ($I_{REF}$) so that the capacitor charging

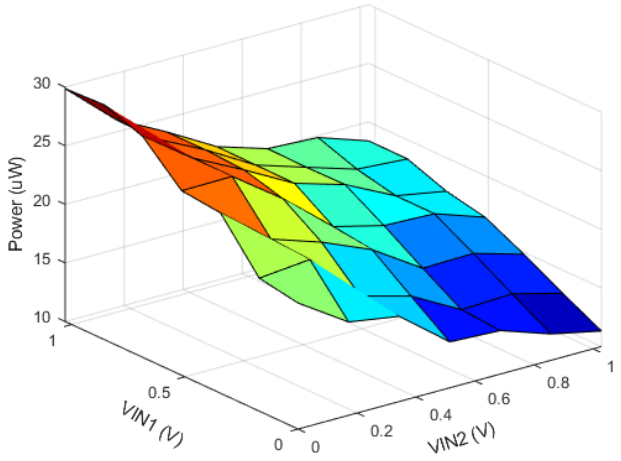



Figure 5.15: Transmitter active power vs. $V_{IN1}$ and $V_{IN2}$ without considering power amplifier.

time until it reaches $V_{REF1}$ increases. However, as $T_{SENSE1}$ increases, the generated output pulse period increases which lowers the data rate. Simulation results show that by reducing $I_{REF}$ from its original value of 8.2 $\mu A$ to 27 $nA$, makes the minimum average power consumption equal to 5.41 $\mu W(V_{IN1} = 0, V_{IN2} = 1.2V)$ and maximum of 94.12 $\mu W(V_{IN1} = 1.2V, V_{IN2} = 0)$, however, at the expense of prolonging $T_{SENSE1}$ to 6.57 $\mu s$.

To reduce the power consumption of the presented wake-up transmitter when it is completely off, two high-Vt switches are inserted in the path of $V_{DD}$ and GND. Switches are sized so that $R_{ds}$ does not affect the efficiency and operation of the transmitter when on. The power consumption of the proposed transmitter is 7 $nW$ when it is off.

## 5.4 Experimental Results

The proposed ultra-low-power transmitter is fabricated in a standard TSMC 65nm CMOS process. The transmitter occupies a die area of 320 $\mu m \times 365$ $\mu m$. The power amplifier inductors and capacitors are realized off-chip to increase the efficiency and tuneability of the power amplifier. Inductors are chosen from CoilCraft ceramic chip

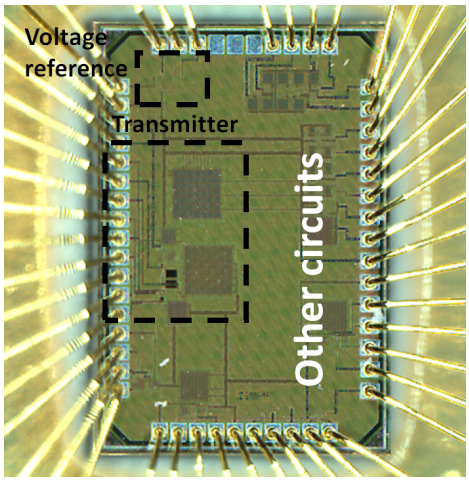



Figure 5.16: Chip microphotograph.

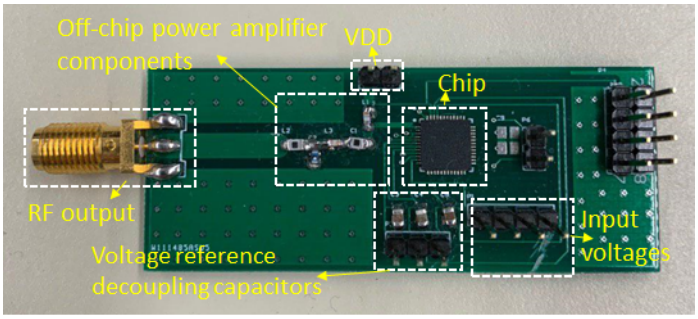



Figure 5.17: Chip mounted on a PCB.

inductors that show a quality factor range of 40 to 98 for the inductor value range of 1.8 nH to 380 nH at 900 MHz as opposed to on-chip inductors that show a quality factor of around 10 [57]. The chip die photo is shown in Fig. 5.16.

The chip is encapsulated in a QFN package for reducing the parasitic effects imposed by packaging and is mounted on a 2-layer FR-4 PCB and is tested using a Keysight Infiniium S-Series 8 GHz oscilloscope that is connected to the PCB using an SMA connector. The final PCB is illustrated in Fig. 5.17. The chip is tested at two carrier frequencies of 915 MHz and 2.4 GHz, which are both in the ISM band, by changing the $V_{DD}$ from 600 $mV$ to 1 $V$. The measured output waveform of the proposed transmitter when $V_{IN1} = 0, V_{IN2} = 0, V_{DD} = 600\ mV$, and $I_{REF} = 8.2\ \mu A$ is shown in Fig. 5.18. $T_{SENSE1}$ and $T_{SENSE2}$ are shown in the figure. As can be seen, $T_{SENSE1}$ is equal to 148 ns and $T_{SENSE2}$ is equal to 131 ns and in good agreement

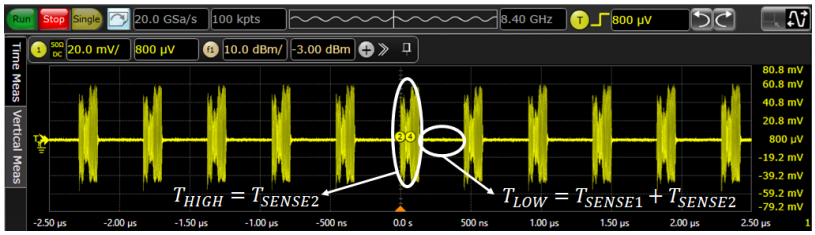



Figure 5.18: Chip output waveform when $V_{IN1} = 0, V_{IN2} = 0, V_{DD} = 600\ mV$, and $I_{REF} = 8.2\ \mu A$.

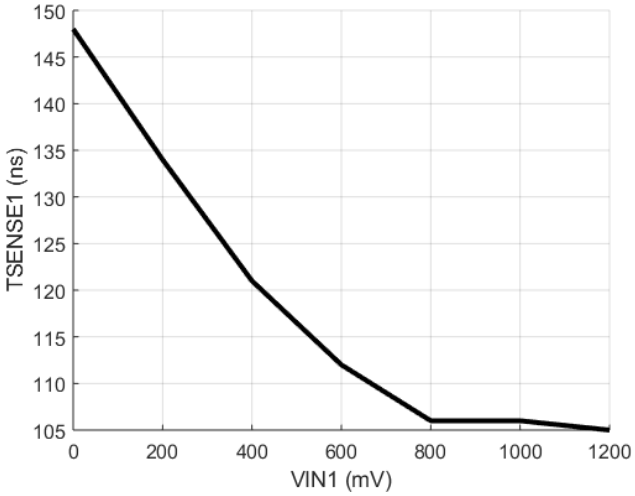



Figure 5.19: Measured $T_{SENSE1}$ vs. $V_{IN1}$.

with the measurement results.

$V_X$ in Fig. 5.1 is connected to a pad in the chip and so that a capacitive sensor can be directly connected to this node and ground and change the output pulse $T_{SENSE1}$. However, the added pad capacitance on this node increases the parasitic capacitance and reduces the tuning range of $T_{SENSE1}$. The measured $T_{SENSE1}$ of the output waveform that is obtained by changing $V_{IN1}$ from 0 to 1.2 V for $V_{DD} = 600\ mV$ is shown in Fig. 5.19 . The difference between the post-layout simulation and measurement results mainly comes from the added parasitic to node $V_X$ from pad and pin parasitic and bond wires that are not modeled properly.

Similarly, $T_{SENSE2}$ is measured by changing $V_{IN2}$ from 0 to 1.2 V which is illustrated in Fig. 5.20.

As can be seen, the measured results are in good agreement with the post-layout

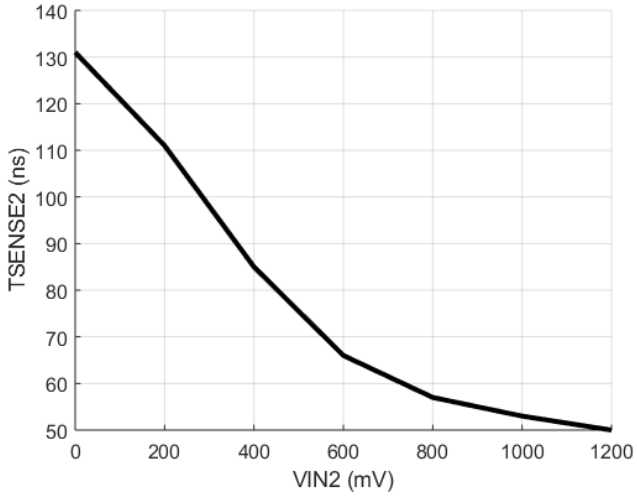



Figure 5.20: Measured $T_{SENSE2}$ vs. $V_{IN2}$.

simulations. For accurately measuring the idle current (the pulse generator output is ZERO), a Keithley picoammeter/voltage source is used. 2.9 $\mu A$ is measured as the idle current when $V_{DD} = 600\ mV$,$V_{IN1} = 0$, $V_{IN2} = 0$ .i.e $P_{IDLE} = 1.74\ \mu W$. The post-layout simulation results predict this power to be 1.721 $\mu W$ which is 20 $nW$ lower than the measured results.

As discussed in Section 5.3, active and total power consumption can be reduced by decreasing $I_{REF}$ which will increase $T_{SENSE1}$ and decreases the output duty cycle. For testing this effect, the basing voltage of the PMOS producing $I_{REF}$ ($V_{REF2}$) is changed from it original value of 8.2 $\mu A$ to 1.5 $\mu A$ by connecting an external voltage source to $V_{REF2}$ instead of the on-chip voltage reference output. The output measured waveform when $V_{IN1} = 0, V_{IN2} = 0, V_{DD} = 600\ mV$, and $I_{REF} = 1.64\ \mu A$ is shown in Fig. 5.21. As can be seen, $T_{SENSE2}$ has not changed but $T_{SENSE1}$ has become 100 $ns$ longer.

**Power amplifier optimization and measurement**

For testing the transmitter's power amplifier, $V_X$ is connected to $V_{DD}$ which will set the output of the pulse generator to $V_{DD}$ (bypassing the relaxation oscillator) enabling the carrier generator ring oscillator all the time so that the output changes

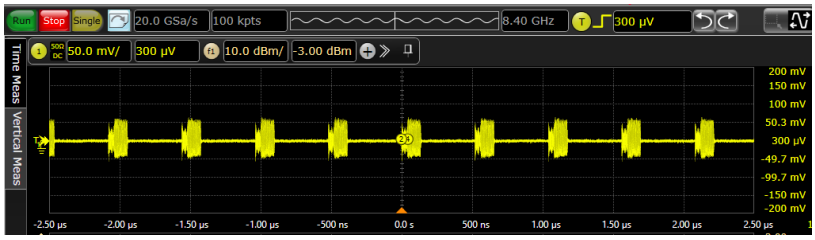



Figure 5.21: Chip output waveform when $V_{IN1} = 0, V_{IN2} = 0, V_{DD} = 600mV$, and $I_{REF} = 1.5\ \mu A$.

from a pulse to a sinusoidal wave, making tuning easier. The output of the power amplifier then is connected to the spectrum analyzer via PE343-48 N-type cable and the output power is measured. The PCB track loss obtained from EM simulation and cable insertion loss are added to the measured power to find the accurate output power levels. By tuning the power amplifier external components, the output power is measured -2 dBm in $V_{DD} = 600\ mV$ which is 1 dB lower than the output power obtained by post-layout simulation.

Table 5.1 summarizes the performance of the proposed transmitter and compares it to the recently published low-power transmitters. The work in [2, 43, 71, 72] report both receiver and transmitter that have been designed for a system-on-chip low-power sensor node, however, for a fair comparison, only the transmitter parts have been compared with our work. As can be seen, the average active and off power consumption of the proposed transmitter is the lowest among all the reported work while delivering the output power of -1 dBm which is highest except for [2]. All other previously reported designs, use power-hungry circuitry such as ADC and microprocessors, to read the sensor output and modulate the signal as opposed to our work that the signal is modulated with an ultra-low-power pulse generator. Moreover, the proposed transmitter is capable of transmitting two sensors' output simultaneously whereas prior work can only transmit one. The voltage supply of the proposed transmitter is lower than other reported work except for [71] that is 0.56 V.

Table 5.1: Performance summary and comparison of the proposed transmitter

| Parameter | This work | [43] '16 JSSC | [2] '11 JSSC | [71] '14 JSSC | [72] '14 JSSC |
|---|---|---|---|---|---|
| Technology | 65nm | 180nm | 130nm | 65nm | 350nm |
| Frequency | 915MHz and 2.4GHz | 112MHz | 868MHz | 402MHz | 403MHz |
| Built-in sensing | Y | Y(ADC) | Y(ADC) | Y(ADC) | Y(ADC) |
| Wireless | PWM | PPM | FSK | OOK | OOK |
| Blocks[1] | Osc, Comp, PA | Osc, $SU$, Comp, Amp, $PIL$ | ADC, $CP$, Amp | ADC, PA, Osc | ADC, PGA, Processor |
| Supply voltage | 0.6V | 4.1V | 1.5V | 0.56V | 1.8V |
| Active power | $5.41\mu W \sim 94.12\mu W$[4] | $43.5\mu W$ | $8.55mW \sim 14.4mW$[2] | $215\mu W$ | $762\mu W$ |
| Off power | $7nW$ | $22nW$ | $190nW$ | $< 1\mu W$ | $226.3\mu W$[3] |
| Output power levels | $-40dBm \sim -1dBm$ | $-78dBm$@$50cm$ | $-6.4dBm \sim 5.4dBm$ | $-18 \sim -16dBm$ | $-18dBm$ |
| Tx channels | 2 | 1 | 1 | 1 | 1 |
| Output stage | PA | Osc | Osc | PA | PA |

[1] Osc: oscillator, Comp: comparator, PA: power amplifier, SU: start-up circuit, PIL: pulse inject loop, CP: charge pump

[1]PGA: programmable gain amplifier.

[2]Transmitter total power consumption for $I_{REF} = 27nA$.

[3]Alarm mode.

## 5.5 Summary

In this chapter, an ultra-low-power wake-up transmitter is presented that is capable of transmitting simultaneously two sensors' analog outputs. The idle power consumption of the proposed transmitter is reduced by eliminating all the static current paths between ground and $V_{DD}$, a comparator biased in the subthreshold region, by using two ring oscillators and a voltage reference working in the deep subthreshold region and a zero-bias switching power amplifier. By introducing a new modulation technique that modulates the LOW and HIGH time of the transmission signal according to two input analog sensor voltages, the active power consumption of the transmitter is significantly reduced as the power amplifier is activated in a portion of the transmission period. In addition to its high power efficiency, utilizing a class E switching power amplifier at the output with external components allows for the tuning of the transmitter output power by enabling different transmission ranges depending on the desired application. Finally, for reducing the power consumption of the transmitter when it is completely off, two high-Vt switches have been used to cut off the supply voltage. The proposed transmitter was fabricated in standard TSMC's 65-nm CMOS process. The measurement results show that the transmitter consumes less than 7 $nW$ when it is completely off and consumes less than 30 $\mu W$ without considering

the power amplifier power consumption at the output.

# Chapter 6

# An Integrated RF-powered Wireless Transceiver with -26 dBm Sensitivity

This chapter presents[1] a self-sufficient wireless node by integrating an RF energy harvester powering up a wake-up receiver and wireless data transmitter on a single chip. An ultra-low-power (nW) RF-powered WuRx is designed to operate with supply voltages as low as 300 mV that can be continuously powered up by a highly efficient RF energy harvester. The excess harvested energy is stored on a large buffer capacitor to power up the WuTx after the WuRx detects a pre-defined packet. In addition to operating with a supply voltage as low as 300 mV, an ultra-low-power ultra-low-voltage envelope detect (ED) with a high input sensitivity is designed using passive amplification of a matching network to amplify the input RF signal without requiring a low-noise amplifier. To increase the input sensitivity of the WuRx, RFEH and ED are co-designed so that most of the power goes to the RFEH while ED can still detect the received packets. Furthermore, instead of using a voltage regulator with limited efficiency in the proposed transceiver, the RFEH is directly connected to the ED, avoiding power converters' loss. The proposed WuTx is designed to work with a supply voltage as low as 600 mV. The transmitter employs a highly efficient

[1]This chapter is based on a manuscript submitted to IEEE Transactions on Circuits and Systems I: Regular Papers [73].

class E amplifier, and it is designed so that it does not consume static power while transmitting zero increasing the overall efficiency. Furthermore, by introducing asymmetry in the transmitter's cross-coupled oscillator, the start-up time has decreased, increasing the maximum transmitter data rate.

## 6.1 RFEH and Wake-up Receiver

In this section, the working principle and circuit implementation for each building block of the proposed transceiver shown in Fig. 6.1 is described. As can be seen in Fig. 6.1, an OOK modulated signal is captured via the receiver antenna and is passively amplified by the high-Q L-section matching network and is fed to the receiver in which the envelope detector and RF energy harvester are connected to the input simultaneously. The RF energy harvester is designed to have $R_{in}$ much less than the envelope detector so that most of the received power is transferred to the harvester to be converted to DC power. As before receiving the predefined wake-up packet, the transmitter is off, the output DC voltage of the harvester is stored in a large buffer capacitor. The RFEH output simultaneously supplies the WuRx consisting of the envelope detector, comparator and ring oscillator. Therefore, the WuRx is designed to consume an ultra-low amount of power.

The proposed transceiver utilizes an OOK ultra-low-voltage ultra-low-power wake-up scheme with high input sensitivity while consuming an ultra-low amount of power, reducing the total power consumption of the WuRx. Therefore, the input power required for the harvester to produce the voltage required for the WuRx is reduced, leading to the increased overall sensitivity.

### 6.1.1 Passive Amplification

The receiver antenna can be modelled by a voltage source with an internal impedance of $Z_s$. Assuming that the input impedances of the receiver before and after the matching network are $Z_r$ and $Z_m$ respectively (shown in Fig. 6.1), in order to transfer

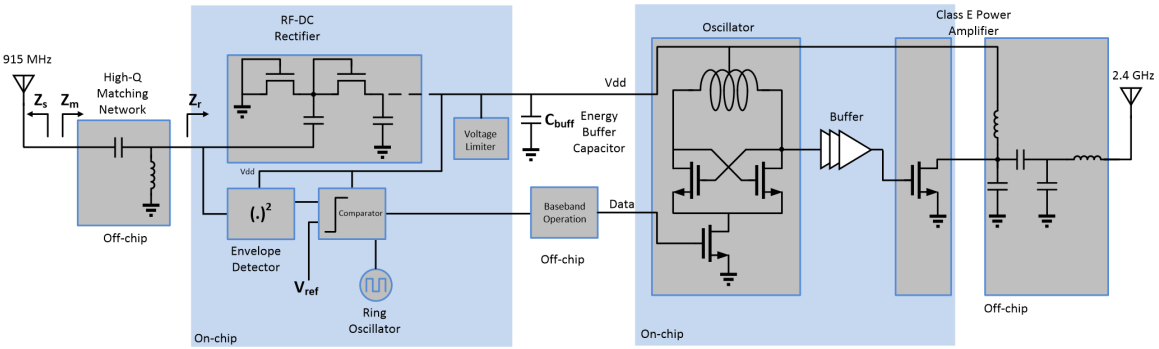



Figure 6.1: Proposed self-powered transceiver.

the maximum power from the antenna to the receiver, the matching network must be designed so that $Z_s = Z_m^*$. If the matching network is lossless and the $Z_s$ is purely resistive and equal to $R_s$, assuming that the input voltage is in the sinusoidal form $(V_a cos(\omega t))$

$$P_s = P_r = \frac{V_a^2}{2R_s} = \frac{V_a^2}{2R_r} \tag{6.1}$$

where $P_s$ is the power of the source, $P_r$ is the receiver's power, $V_a$ is the input voltage of the receiver and $R_r$ is the input resistance of the receiver (parallel of WuRx and RFEH input impedance). On the other hand, the power consumed by $R_s$ or $P_s$ can be obtained by [57]

$$P_s = \frac{V_s^2}{8R_s} \tag{6.2}$$

where $V_s$ is the source voltage. Therefore, by equating (6.1) and (6.2) the input voltage of the receiver is obtained as

$$V_a = \frac{V_s}{2}\sqrt{\frac{R_{in}}{R_s}}. \tag{6.3}$$

As can be seen, if $R_{in}$ is larger than $R_s$, for a lossless network, the source voltage is passively amplified. This is beneficial in increasing the overall receiver sensitivity as the matching network amplifies the voltage at the receiver input without consuming any amount of power. In reality, on-chip and off-chip inductors and capacitors show a limited quality factor. Therefore, the matching network cannot be assumed to be lossless. Therefore some of the input power coming from the source (antenna) is

lost in the matching network. As having a high passive amplification in operation of RFEH and WuRx is essential, most of the time the matching network is realized off-chip to reduce the losses as on-chip inductors show lower quality factors compared to off-chip ones in frequencies lower than 2 GHz [57]. In addition to that, capacitors often show a higher quality factor than inductors at the targeted 915 MHz frequency; therefore, their loss can be neglected in the design process. The matching network's lossy inductor can be modelled with an inductor ($L_{match}$) in parallel with a resistor ($R_{match}$). As $R_{match}$ is in parallel with the receiver input resistance, the maximum passive amplification can be obtained as

$$A = \frac{1}{2}\sqrt{\frac{R_{in}||R_{match}}{R_s}} \tag{6.4}$$

where $R_{match} = QL_{match}\omega$, and Q is the matching network's inductor quality factor. Therefore, for higher input sensitivity levels, the input resistance of the receiver which is parallel of WuRx and RFEH impedance must be designed as large as possible, and the matching network must be high-Q. In this work, L-section matching network is used that is implemented by utilizing high-Q off-chip inductors and capacitors. That is why passive amplification has been the foundation of the most recent introduced wake-up receivers [24, 25, 44, 45, 74] and RFEHs [14, 15, 17] as the high-Q matching network amplifies the receiver's input signal without consuming power making it popular for ultra-low-power designs.

### 6.1.2 RFEH

In order to make wireless transceivers RF-powered an RFEH which is mostly realized by an RF-DC rectifier needs to be implemented. However, integrating RFEH in conjunction with a WuRx arises several problems that need to be addressed:

1. As powering up the wireless transceiver is RFEH's responsibility, most of the input power coming from the antenna should go to the RFEH. Therefore, the input resistance of the rectifier must be much lower than the input resistance of the envelope

detector. If $R_{ED}$ is the input resistance of the envelope detector and $R_{REC}$ is the input resistance of the rectifier, the power division at the input of the receiver is:

$$\begin{aligned} \frac{P_{ED}}{P_r} &= \frac{R_{REC}}{R_{REC}+R_{ED}}, \\ \frac{P_{REC}}{P_r} &= \frac{R_{ED}}{R_{REC}+R_{ED}}. \end{aligned} \tag{6.5}$$

Therefore, in order to transfer most the input power to RFEH, $R_{ED} >> R_{REC}$.

2. The overall receiver's input resistance is equal to $R_r = R_{ED}||R_{REC}$ and because $R_{ED} >> R_{REC}$, $R_r \approx R_{REC}$. As shown in Eq. (6.3), the passive amplification depends on the value of WuRx input resistance .i.e $R_r$. Therefore, as $R_{REC}$ reduces, the passive amplification at the input of the receiver reduces hence lowering the input voltage ($V_a$). Therefore, in order to get a large passive amplification at the input of the receiver, $R_{REC}$ should be large and $R_{ED} >> R_{REC}$. Input sensitivity of the transceiver is defined as the minimum input power in which RFEH can produce the supply voltage required for the transceiver to work properly. In this design the minimum supply voltage required for the proposed WuRx and WuTx to work properly are 300 mV and 600 mV respectively. As discussed in chapter 3, as the number of stages in the rectifier chain increases, the rectifier's input resistance is reduced, leading to a lower passive amplification at the rectifier's input. This is because more stages become in parallel with each other lowering the input resistance. Therefore, for a fixed input power level, by increasing the number of stages the output voltage increases up to the point that the input voltage becomes very low at the rectifier's input so that more number of stages cannot increase the output voltage. In addition to that, transistors' sizes also play an important role in determining the passive amplification and the RFEH's efficiency. As the transistors' sizes increase the input resistance of the RFEH is lowered but the conduction current of transistors increases that overally leads to a better efficiency up to an optimum point. Therefore, as the transistors' sizes increase, the efficiency and the output voltage of RFEH increases up to a point that the passive amplification at the input becomes very low so that

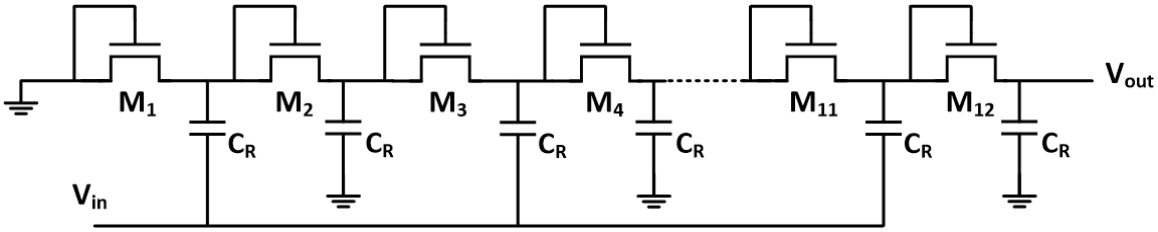



Figure 6.2: RF Energy Harvester.

the efficiency is degraded and output voltage is lowered. Therefore, the main goal is to find the lowest number of stages and transistors' sizes required for producing 300 mV or 600 mV output voltage so that the maximum passive amplification is achieved at the receiver's input. This can be done by using iterative simulations for a fixed input power level: for a certain number of stages the input matching network must be designed using iterative simulations, and this process must be repeated for each number of stages. However, this process is very time consuming and not practical. Therefore, to address the issues mentioned above, in this chapter, the analytic method introduced in chapter 3 is used to find the optimum number of stages required for the rectifier to produce the proper supply voltages for the transmitter and receiver to work correctly. Considering all the requirements, a six-stage Dickson's rectifier utilizing low-Vt transistors with size of $1.2\mu m/130nm$ is used as shown in Fig. 6.2 . Simulation results show that the RFEH output reaches 300 mV (voltage required for the WuRx to operate properly) for the input power level of -29.3 dBm and reaches 600 mV (voltage required for the WuTx to work) for the input power level of -24.8 dBm considering the leakage current of the transmitter. The rectifier's input impedance at these power levels and at a 915-MHz operating frequency is approximately equal to $35.7 - 595j$ which in fact is a $10 - K\Omega$ resistor in parallel with a $291 - fF$ capacitor showing a high input resistance.

### 6.1.3 Envelope Detector

Recently, several envelope detectors have been presented that achieve high sensitivities while consuming a few nanowatts [24, 25, 44, 45, 74]. Envelope detector circuits can be categorized into the wo categories of active and passive. The active circuits are realized by passing the signal from a non-linear device (a transistor working in subthreshold) and adding a low-pass filter at the output to extract the signal's low-frequency envelope [24, 45]. Passive EDs can be realized by using a rectifier as the ED. However, the passive envelope detectors show a lower input resistance compared to the active ones as a high number of stages must be in parallel with each other to achieve a high input sensitivity. Furthermore, a passive envelope detector is usually accompanied by a baseband amplifier to enhance the extracted signal amplitude. For input power levels lower than the RFEH sensitivity, the RFEH will not produce a proper output DC voltage to power up the rest of the transceiver. Therefore, the proposed RF-powered transceiver input sensitivity is mainly determined by the input sensitivity of RFEH. Also, as the RFEH is responsible for powering up the entire transceiver, its input power must be maximized as much as possible. This can be done by increasing the input resistance of ED. Although using N-stage passive EDs which do not consume DC power and have better 1/f noise performance seem a better choice, achieving very high input resistance with them is difficult as N resistors are in parallel with each other. In order to maximize the input resistance of the ED so that most of the input power transfers to the RFEH, in this work a common-source stage with the self-biased active load shown in Fig. 6.3 is used as the ED. The bias current of the active load is provided by connecting its gate and drain to each other with a large resistor, i.e. $R_G$ so that it acts as a diode-connected transistor at DC. $C_G$ is used to stabilize the DC biasing voltage at the transistor's gate and eliminate high-frequency signals by acting as a short-circuit in RF. Body of $M_1$ is connected to its gate to enhance the gain of the amplifier. The transistor is biased in the

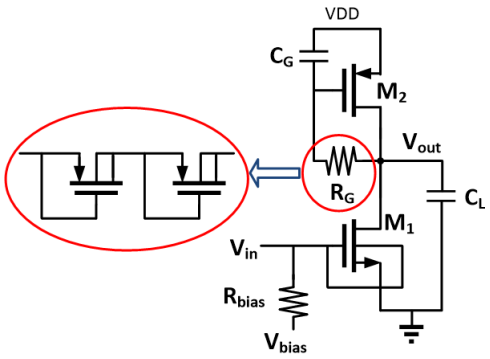



Figure 6.3: Common-source with self-biased active load envelope detector.

subthreshold region to have low power consumption and exponential drain current and input voltage dependency. $C_L$ and $r_o$ at the ED's output constitute a low pass filter eliminating high-frequency signals from the extracted envelope. $M_1$ is designed to have 6 nA DC bias current.

The normalized gain of the common-source ED is obtained by [24]

$$A = (g_{m2} + g_{mb2})R_o = [1 + (n-1)^2]\frac{I_d}{2(nV_T)^2}R_o \tag{6.6}$$

where $I_d$ is the bias current determined by $M_8$, $V_T$ is thermal voltage, $R_o = r_{o1}||r_{o2}||R_G$, and n is the subthreshold slope factor. As can be seen, the gain of the envelope detector can be increased by increasing the bias current at the expense of more power consumption. Furthermore, for increasing the gain of the envelope detector, $R_G$ must be maximized. Therefore a MOS-bipolar-pseudoresistor is used [75] to generate a high resistance in a small area, as shown in Fig. 6.3. Assuming $R_G$ to be very large so that it is an open circuit in RF analysis, the input admittance of the common-source envelope detector is obtained as [57]

$$\begin{aligned} R(Y_{in}) &= R_D C_{GD1}\omega^2 \frac{C_{GD1} + G_m R_D(C_L + C_{GD1})}{R_D^2(C_L + C_{GD1})^2\omega^2 + 1}, \\ Im(Y_{in}) &= C_{GD1}\omega \frac{R_D^2 C_L(C_L + C_{GD1})\omega^2 + 1 + G_m R_D}{R_D^2(C_L + C_{GD1})^2\omega^2 + 1} \\ &+ C_{GS1}\omega \end{aligned} \tag{6.7}$$

where $R_D = r_{o1}||r_{o2}$, $G_m = g_{m1} + g_{mb1}$. $C_L$ is used at the output of the envelope detector to create a low-pass filter to extract the envelope of the signal so that

$C_{GD1} << C_L$, therefore, $R(Y_{in})$ is simplified to

$$R(Y_{in}) \approx R_D C_{GD1} \omega^2 \frac{G_m R_D C_L}{R_D^2 C_L^2 \omega^2 + 1}. \tag{6.8}$$

(6.8) can be simplified further at high frequencies that $R_D^2 C_L^2 w^2 > 10$:

$$R(Y_{in}) \approx \frac{C_{GD1} G_m}{C_L}. \tag{6.9}$$

Therefore the input resistance of the envelope detector approximately is

$$R_{ED} \approx \frac{C_L}{C_{GD1} G_m}. \tag{6.10}$$

As can be seen in (6.10), $R_{ED}$ is inversely proportional to $G_m$ while the envelope detector gain is proportional to it. As $g_m = I_d/nV_T$ and $g_{mb} = (n-1)I_d/nV_T$ in subthreshold region, $G_m = I_d/V_T$. Therefore, as the required power consumption determines the bias current of the envelope detector, $C_{GD1}$ must be minimized to increase the envelope detector's input resistance. This can be done by decreasing $W_1$ as in the subthreshold region $C_{GD} = WC_{ov}$, where $C_{ov}$ is the gate-drain overlap capacitance. In this design $M_1$ size is set to $W_1/L_1 = 1.2\mu m/350nm$. The designed ED input resistance obtained by simulation is 2.51 M $\Omega$ . The designed ED shows an input sensitivity of -70 dBm.

### 6.1.4 Comparator and Oscillator

The output of ED is not in a digital format and cannot drive large capacitors as the ED is biased with a low bias current. Hence it is fed to a comparator with $V_{ref}$ as the reference voltage to digitize the envelope detector's output. The comparator illustrated in Fig. 6.4 is utilized in the proposed transceiver [59, 76]. The comparator works as follows. As illustrated in Fig. 6.5 when clock is zero, $M_8$, and $M_{10}$ are turned on, connecting X and Y to $V_{DD}$ turning on $M_3$ and $M_4$. In this phase, A, B, C and D are discharged by $M_1$ and $M_2$, and as $M_5$ and $M_6$ are not on, the positive feedback loop is not closed. In the next phase at the rising edge of the clock, $M_5$ and $M_6$ turn

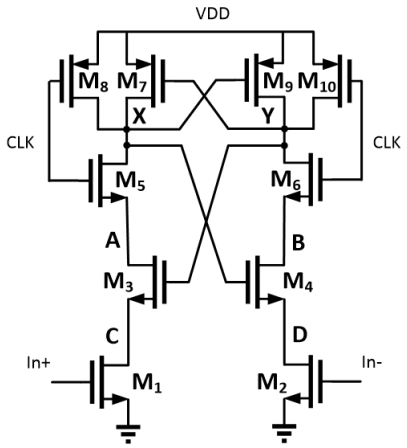



Figure 6.4: Comparator.

on making a current path between A, C, and X, and D, B, and Y that creates a spike at A, C, B, C voltages. Meanwhile, currents of $M_1$ and $M_2$ flow from these points discharging their capacitors. The different discharging rate determined by In- ($M_2$ current) and In+ ($M_1$ current) creates an imbalance on C, D voltages which is then amplified by the positive feedback until the positive feedback turn on one of the $M_3$, $M_9$ or $M_4$, $M_7$ pairs completely while turning the other off producing a rail to rail voltage at X and Y. As the drain of the input transistors is clocked, this comparator has a low kickback noise; therefore, the envelope detector's output is not affected by the comparator. This is beneficial because the envelope detector's bias current is very low and its output can be significantly affected by the comparator's kickback noise producing error at the final detected output.

The clock of comparator is generated by a 5-stage ring oscillator that is based on constant energy-per-cycle cell illustrated in Fig. 6.6 [77]. For $V_{DD}$= 300 mV (only WuRx is deployed), the oscillator's frequency range is 2.5 KHz to 753 KHz while consuming 690 pW to 103 nW. Similarly, for $V_{DD}$= 600 mV (both WuRx and WuTx are deployed), the oscillator's frequency varies from 2.9 KHz to 8.7 MHz while consuming 1.5 nW to 7.2 $\mu$W. The oscillator's tuning voltage should be set based on the minimum desired data rate of the WuRx. For instance, when $V_{DD}$= 300 mV and $V_{tune}$ = 0 V, the maximum data rate of WuRx of 1.2 KHz can be achieved (2×

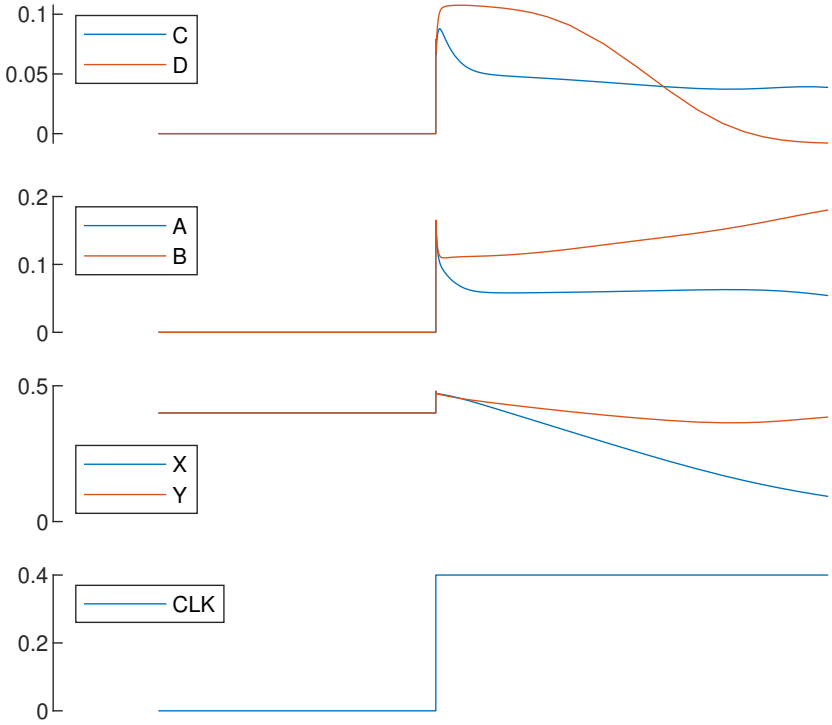



Figure 6.5: Comparator's voltage waveform.

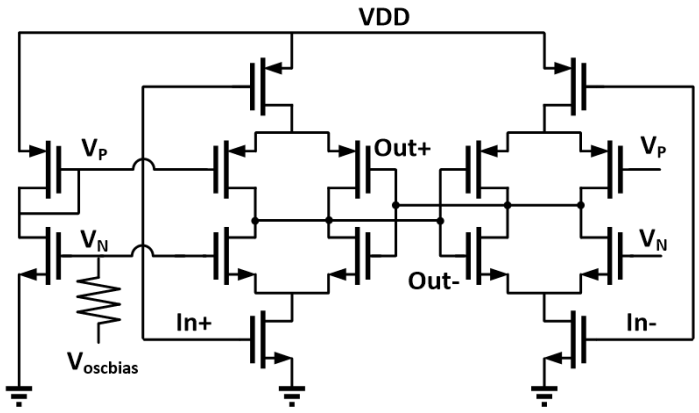



Figure 6.6: Current starved ring oscillator.


(a) (b)

Figure 6.7: (a) $S_{11}$ vs. frequency, (b) passive amplification vs. frequency.

oversampling rate).

### 6.1.5 RFEH and WuRx Simulation Results

In measurements, off-chip inductors are chosen from CoilCraft 0603 inductors with Q of 40 to 98 for the inductor range of 1.8 nH to 380 nH at 900 MHz. Therefore, in simulations, the matching network is designed by assuming its inductor to have a Q of 50. Fig. 6.7 shows the simulated $S_{11}$ and passive amplification for the matching network that is designed for -25 dBm input power level. As illustrated in Fig. 6.7, $S_{11}$ reaches -33.4 dB and the passive amplification of 22.4 dB at 915 MHz . The simulated power consumption of the entire WuRx for $V_{DD}$ of 300 mV is 5.7 nW.

The simulation result of the proposed RF-powered WuRx for an input power of -25 dBm is illustrated in Fig. 6.8. To reduce the ripple on supply voltage, in the simulations, $C_{buff}$ is set to 500 pF. The oscillator tuning voltage is set to zero to set its frequency to the minimum. As can be seen, the oscillator starts working for supply voltages as low as 200 mV. Using the comparator helps to reduce the ED's output voltage noise. The comparator also acts as a voltage buffer for driving the baseband digital circuitry. Otherwise, as ED is biased with low bias current, a small amount of parasitic capacitance on its output will result error. For detecting the pre-defined wake-up bit sequence, an ultra-low-power digital correlator can be used [24, 25]. For instance, in [24], a 16-bit digital correlator is designed that consumes 770 pW. In this prototype, in order to increase the testing flexibility, digital circuitry is realized by

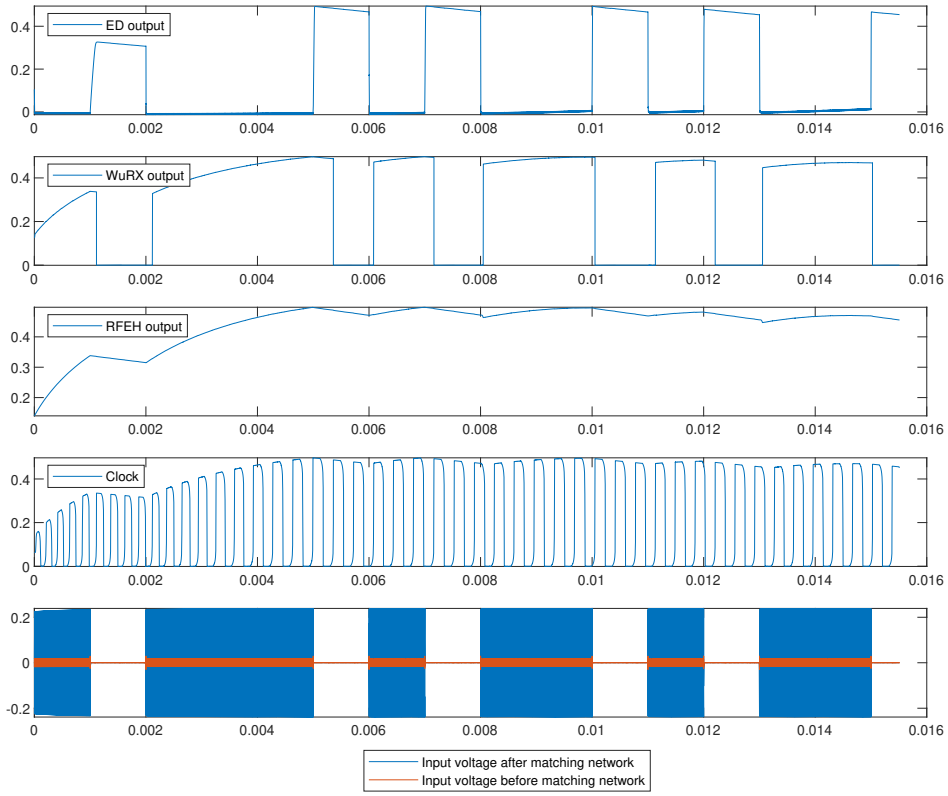



Figure 6.8: WuRx simulation results. Y axis scale is Volts and X axis demonstrates time in seconds.

using an external FPGA.

## 6.2 Wake-up Transmitter

In the proposed self-powered transceiver, the energy of the received RF signal is stored on a capacitor which is used for powering the WuRx and WuTx. As the WuTx draws a large current while transmitting, the buffer capacitor, .i.e $C_{buff}$ should be large enough to provide a large current for a short amount of time that the transmitter is sending data. Therefore, $C_{buff}$ is realized off-chip using a ceramic SMT capacitor. A cross-coupled oscillator is used as the VCO to generate the target carrier frequency of 2.45 GHz, as shown in Fig. 6.1. In the proposed wireless transceiver, OOK modulation is chosen as it does not consume power for transmitting zeros. Therefore, all the circuit blocks in the transmitter are designed so that they do not consume power when transmitting zero. As illustrated in Fig. 6.9, OOK modulation is generated by feeding the data to an NMOS at the tail of the oscillator providing the current needed for the oscillator to work. To buffer the oscillator signal before feeding it to the Class E amplifier, two inverter-based buffers have been used. As the first buffer's input signal (output of the oscillator) has a DC offset of $V_{DD}$ a decoupling capacitor is used and the inverter's bias current is provided by an NMOS transistor controlled by the input data turning of the buffer when zero is getting transmitted. In this way, the second buffer's input voltage is zero when transmitting zero so that a simple inverter is used. The limiting factor in the maximum achievable data rate of the transmitter is the oscillator start up time. The start-up time of the oscillator can be increased by introducing asymmetry in the cross-coupled oscillator so that in the presence of the thermal noise one output can reach to a rail voltage faster [78]. Therefore, to increase the maximum data rate of the transmitter, $C_2$ is sized twice as large as $C_1$. The simulated VCO tuning range is 2.39 GHz to 2.66 GHz covering the targeted center frequency of 2.45 GHz. The VCO phase noise obtained by simulation is -116 dBc/Hz at 1 MHz offset. By introducing the asymmetry between the varactors, a start-up

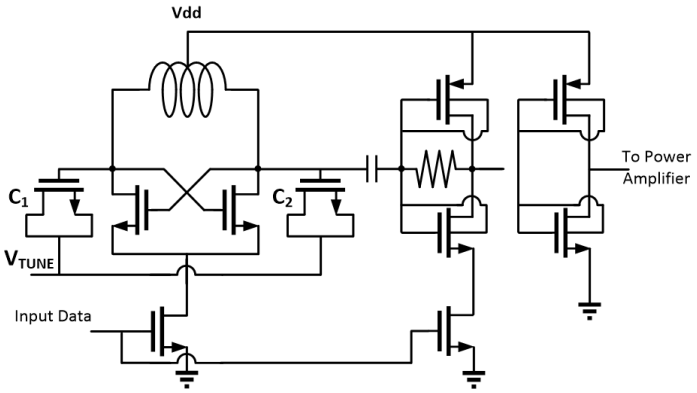



Figure 6.9: Circuit implementation of the OOK transmitter.

time of 2.5 ns is achieved, which sets the maximum data rate to 200 Mb/s considering 4× safety margin.

### 6.2.1 Power Amplifier

To eliminate static power consumption when transmitting zero, and increase the power conversion efficiency, a switching Class E power amplifier with finite DC-feed inductance is utilized in the proposed transceiver as illustrated in Fig. 6.10. By knowing the supply voltage ($V_{DD}$) and the required output power ($P_{out}$), the power amplifier's components ($L_1$ and $C_1$) can be designed by using [69]:

$$\begin{cases} R_L = 1.365\dfrac{V_{DD}^2}{P_{out}}, \\ L1 = 0.732\dfrac{R_L}{\omega}, \\ C1 = \dfrac{0.685}{\omega R_L} \end{cases} \tag{6.11}$$

where $R_L$ is the optimum load resistance. As the output of the power amplifier is connected to an antenna which often is designed with the impedance of 50Ω, a matching network must be used to convert $R_L$ to 50Ω. Therefore, a matching network consisting of $C_2$, $C_3$, and $L_2$ is utilized. In order to have the flexibility to tune the output power externally, power amplifier inductors and capacitors are realized off-chip. As the utilized off-chip inductors are capacitors are high-Q, the efficiency of the power amplifier is also improved. The power amplifier of the proposed transceiver is

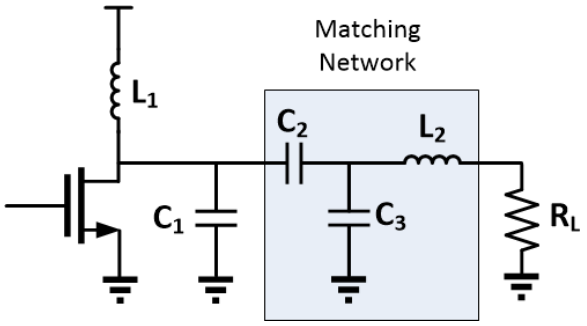



Figure 6.10: Class E power amplifier.

designed to have the output power level of -10 dBm. Simulation results show that the power amplifier output power is 95 $\mu W$ (-10.2 dBm) while consuming 150.3 $\mu W$ from $V_{DD}$ of 600 mV. Therefore, the efficiency of 63.2% is achieved.

## 6.3 Design of Buffer Capacitor

The buffer capacitor value ($C_{buff}$) plays an important role in the start-up time of the proposed transceiver and the maximum on-time of the transmitter. The proposed transceiver can be deployed in two modes and $C_{buff}$ design procedure is different for each mode. In the following, design procedure of $C_{buff}$ is explored for each mode:
(a) In order to increase the battery life time of a transceiver, the proposed RFEH and WuRx can be deployed in radios to wake up the power consuming transceiver only when a pre-defined packet is received. In this way, the proposed WuRx is powered by RFEH and the primary transceiver is off until a wake-up sequence is detected. Utilizing this technique, no power is drawn from the battery when transceiver is off and the operation is duty-cycled expanding the battery life time. As the WuRx draws low current when its on, $C_{buff}$ should be small and used to reduce the supply ripple. Assuming $C_{buff}$= 10 pF, for the input power level of -24 dBm, simulation results show that RFEH average output current is 170 nA. Therefore, the start-up time can be obtained as follows:

$$\Delta t = \frac{C\Delta v}{i} = \frac{10\ pF \times 300\ mV}{170\ nA} = 17.65\ \mu s. \tag{6.12}$$

The start-up time is decreased by reducing $C_{buff}$ at the expense of more ripple on the supply voltage. The start-up time also decreases for higher RF input power levels as the RFEH output current increases.

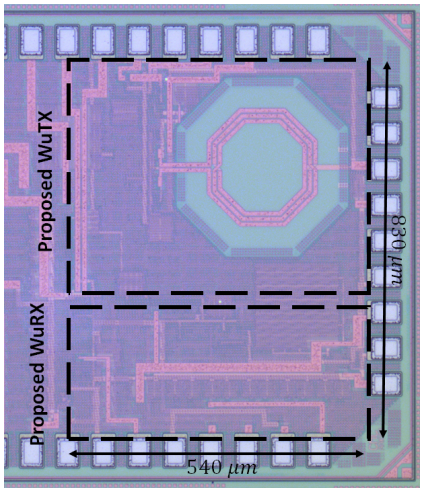
(b) In the case that both transmitter and receiver must be RF powered, the proposed transceiver consisting of RFEH, WuRx and WuTx can be deployed. In this scenario, WuRx demodulates the input signal, and RFEH charges $C_{buff}$. After a pre-defined sequence is detected, the WuRx wakes up the rest of the transceiver including the sensors and WuTx. However, in order to increase the input sensitivity as much as possible in this scenario, the operation must be heavily duty-cycled. For example, for the WuTx's data rate of 10 Mb/s, to send 20 bits out WuTx must stay on for 2 $\mu s$ while drawing 2 mA average current from a 600 mV supply. During this time, $C_{buff}$ provides the energy WuTx requires and discharges rapidly. Simulation results show that the WuTx can work properly for supply voltages as low as 560 mV. Therefore $C_{buff}$ voltage drop for 2 $\mu s$ should be 40 mV so that

$$C = i\frac{\Delta t}{\Delta v} = 2\ mA \times \frac{2\ \mu s}{40\ mV} = 100\ nF. \tag{6.13}$$

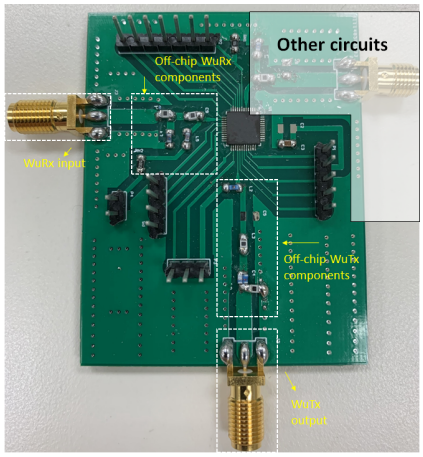
In order to charge $C_{buff}$= 100 nF to 600 mV with -24 dBm RF input power (extreme case) the following must be calculated as this

$$\Delta t = \frac{C\Delta v}{i} = \frac{100\ nF \times 600\ mV}{170\ nA} = 353\ ms. \tag{6.14}$$

As can be seen in (6.14), for the input power level of -24 dBm, the start-up time of the transceiver for 2 $\mu s$ operation time will be 353 ms. The start-up time is reduced for higher input power levels. Furthermore, the transmitter power consumption can be reduced so that a smaller $C_{buff}$ is required. For instance, the low-power transmitter introduced in Chapter 5 can be used in cases that the sensor output voltage is in the analog domain.




(a)




(b)

Figure 6.11: (a) Die micrograph, (b) PCB.

## 6.4 Measurement Results

The proposed transceiver is fabricated in standard TSMC 130 nm CMOS process. A micrograph of the proposed transceiver is shown in Fig. 6.11(a). The proposed RF-powered transceiver occupies a die area of 830 $\mu m \times 540$ $\mu m$. The chip is packaged in a QFN package to reduce the package parasitic and is mounted on a two-layer FR-4 PCB, as illustrated in Fig. 6.11(b). High-Q CoilCraft 0603 inductors and AVX 0805 capacitors are used for measurement. As the input impedance of the receiver depends on its input power level (non-linearity of RFEH and envelope detector), the matching network cannot be designed using conventional methods like measuring s-parameters with a VNA. The following procedure is used to design the matching network:

1. First, in the post-layout simulation, a matching network is designed for the receiver consisting of RFEH and WuRx at -20 dBm and working frequency of 915 MHz using iterative simulations.

2. After finding the proper matching network, the input impedance of the receiver can be calculated at -20 dBm input power level.

3. All the PCB tracks are modelled using Electro Magnetic (EM) simulations in Advanced Design System (ADS).

4. Using the input impedance of the receiver and PCB tracks models, the matching network is designed in ADS using ideal components.

5. Ideal components are replaced with real components (s-parameters of AVX capacitors and Coil Craft are available) using iterative simulations.

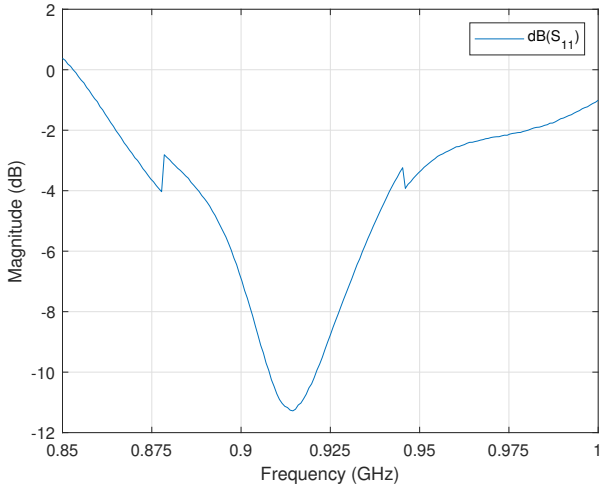



Figure 6.12: Measured $S_{11}$.

Measured $S_{11}$ of the proposed transceiver is illustrated in Fig. 6.12. As can be seen, $S_{11}$ reaches -11.22 dB at 915 MHz. As the RFEH output current at low RF input power levels is low and biasing currents in the proposed transceiver are in nano amperes scale, probing the RFEH and WuRx voltages cannot be done using conventional methods such as using an oscilloscope or a multimeter as their input resistance usually is set to 1 $M\Omega$ and they may load the point they are probing. For measurement purpose, a buffer amplifier is designed using AD8602 OPAMP from Analog Devices with a gain of 2 to solve the loading problem. The designed amplifier is placed between the oscilloscope and the point being probe. As AD8602's input bias current is in order of few pico amperes, it will not load the point that its voltage is being probed. As the designed amplifier stage has a gain of two, the measured voltages are doubled. For creating the input modulated OOK signal, PXIe-5652 RF signal generator from National Instrument is used. The PCB tracks are characterized with EM simulation, and their loss along with the loss of discrete components and cables are deducted from the main input power. For measurements, a 1 $\mu F$ 0805 SMT buffer capacitor is used that can provide energy for the transmitter for 20 $\mu s$. WuRx's performance is

Table 6.1: Performance summary and comparison of the proposed transceiver

| Parameter | This work | [13] '13 JSSC | [16] '18 TCAS I | [52] '09 ISSCC | [2] '11 JSSC |
|---|---|---|---|---|---|
| Technology | 130 nm | 90 nm | 130nm | 180 nm | 130 nm |
| Sensitivity | -26 dBm WuRx<br>-23 dBm both WuRx and WuTx | -17.1 dBm | -16 dBm | -18.5 dBm | -19.7 dBm |
| Minimum supply voltage | 300 mV for WuRx<br>600 mV for both WuRx and WuTx | 1.75 V | 800 mV | 2.75 V | 3 V |
| RX frequency | 915 MHz | 902-928 MHz | 915 MHz | 900 MHz | - |
| TX frequency | 2.45 GHz | 2.405-2.475 GHz | 915 MHz [4] | 3.1-10.6 GHz | 868 MHz |
| RX data rate | 1 Kb/s [1] | 5 Mb/s | - | 40-160 Kb/s | - |
| TX data rate | 20 Mb/s [2] | 5 Mb/s | - | 10 Mb/s | 256 Kb/s |
| Tx power | -11 dBm [3] | -12.5 dBm | - | - | 5.4 dBm |
| Current consumption | 19 nA (WuRx)<br>2.28 mA (WuTx) | 80 nA (idle)<br>860 $\mu$A (active) | 1.05 [5,6] | 1.5 $\mu$A (idle)<br>510 $\mu$A (active) | 9.6 mA |

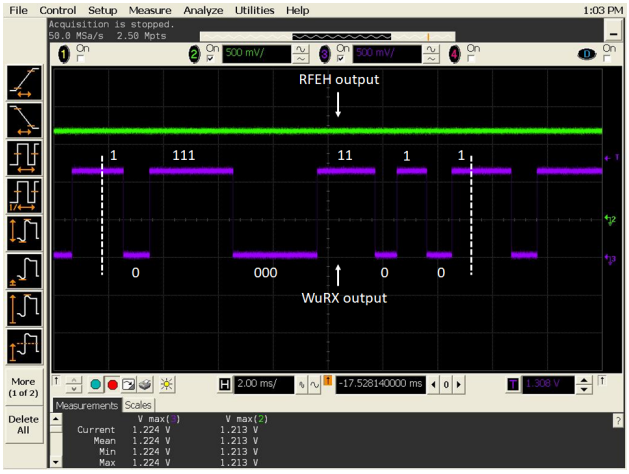
[1]Can go up to 1 Mb/s in the expense of lower input sensitivity.
[2]Can go up to 200 Mb/s.
[2]Can go up to 0 dBm.
[4]Backscattering.
[5]Measurement supply voltage is not reported.
[6]This includes the temperature sensor consumption.

tested for different input power levels for the input data sequence of 10111000110101 with 1 Kb/s data rate. The measured demodulated signal and RFEH output voltage are shown in Fig. 6.13. As can be seen in Fig. 6.13 (a), RFEH output reaches 606 mV for the input power level of -23 dBm (voltage required for the operation of WuTx). Also, as illustrated in 6.13 (b), WuRx can work properly with supply voltages as low as 300 mV that is achieved when the input power level is -26 dBm.

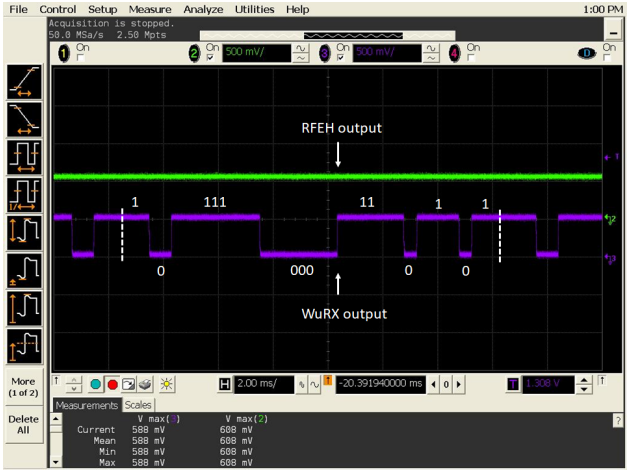
The digital baseband operation is required to detect the pre-defined sequence to turn on the WuTx. In this prototype, digital baseband operation is done by utilizing an Alchitry Au that features a Xilinx Artix 7 FPGA.

Fig. 6.14 shows the simulated and measured frequency range of the VCO when $V_{TUNE}$ varies from 0 to 600 mV.

As can be seen, the VCO frequency changes from 2.29 GHz to 2.58 GHz. To set the transmitter output frequency to 2.45 GHz, $V_{TUNE}$ is set to 420 mV. WuTx output voltage is probed by the MXR608A Infiniium MXR-Series oscilloscope from Keysight while the input data is fed to the transmitter by the FPGA. The output voltage of the WuTx for 1010110010 data stream and data rate of 20 MHz and 10 Mb/s is illustrated in Fig. 6.15 (a) and (b) respectively. As can be seen, the transmitter can




(a)




(b)

Figure 6.13: Measured demodulated output voltage of WuRx for $f_{in}$ = 915 MHz and (a) $P_{in}$ = -23 dBm (b) $P_{in}$ = -26 dBm.

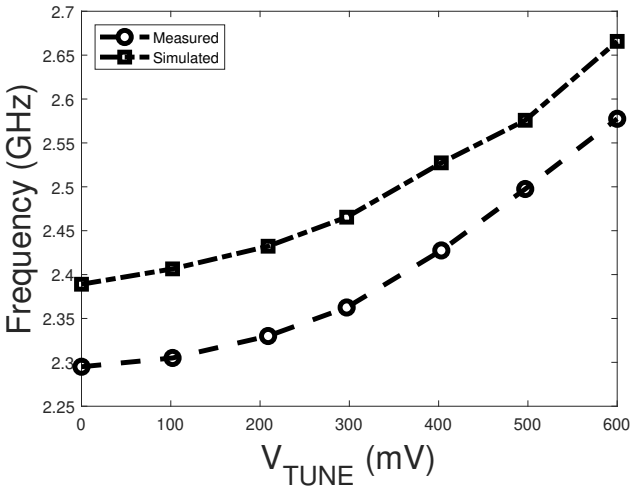
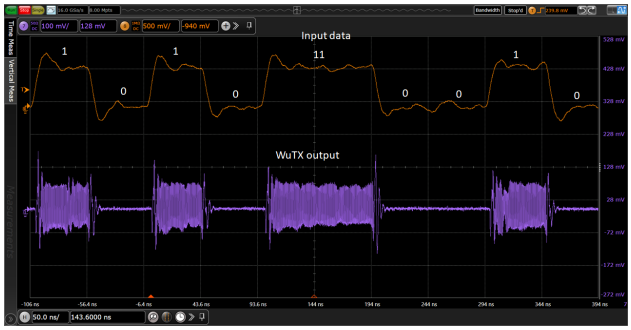



Figure 6.14: Measured and simulated transmitter frequency range.

successfully produce a modulated OOK output signal at a high data rate of 20 MHz. VCO consumes an average current of 2.2 $mA$ (50 % duty cycle), and the output power amplifier delivers -11 dBm to a 50 Ω load with the efficiency of 51 % (cable and track losses are added to the measured output power). Table 6.1 summarizes the performance of the proposed RF powered transceiver with the prior state of the art. As can be seen, thanks to the co-design of low-voltage ultra-low-power WuRx and RFEH, the input sensitivity of -26 dBm for WuRx and -23 dBm for both WuRx and WuTx is achieved that is significantly higher than other previously introduced works even from [16] that uses backscattering instead of active transmission. In addition to that, because of the utilized wide tuning range ring oscillator, the input data rate of 1 Mb/s can be achieved for the proposed wireless transceiver (in the expense of lower input sensitivity). Finally, because of the asymmetric VCO, the maximum data rate of 200 Mb/s is achieved.

## 6.5 Summary

In this chapter, an ultra-low-power wireless transceiver is proposed consisting of a WuRx and a WuTx entirely powered by harvesting RF energy. The co-design of




(a)


(b)

Figure 6.15: (a) The output voltage of the transmitter for data rate (a) 20 Mb/s (b) 10 Mb/s.

RFEH and WuRx opened up the possibility of achieving receiver sensitivities significantly higher than those reported previously. The ultra-low-power WuRx is designed to work with supply voltages as low as 300 mV eliminating the need for power converters that are often inefficient at low power levels. Moreover, it utilizes passive amplification, instead of using an active LNA, and an ultra-low-power envelope detector to minimize its power consumption. Consuming only 5.7 nW at 300 mV, the WuRx can be continuously powered up by RF input power levels as low as -26 dBm. The complete transceiver consisting of WuRx and WuTx can work with a 600-mV supply voltage requiring a minimum RF input power level of -23 dBm. The utilized class E power amplifier in the transmitter outputs -11 dBm with a 51% efficiency at the operating frequency of 2.45 GHz and can be externally tuned for other output power levels.

# Chapter 7

# Conclusions, Recommendations, and Future Work

## 7.1 Conclusions

To develop an RF-powered wireless transceiver, this dissertation focuses on enhancing the efficiency and sensitivity of the RFEH to increase the amount of the harvested energy from the available RF power, and lowering the power consumption and/or the required DC supply voltage of the wireless transceivers and its peripheral circuitry.

The basics of RFEH and RF-powered transceivers are described in Chapter 1. In Chapter 2, the previously introduced methods for increasing the efficiency of RFEH and reducing the power consumption of wireless transceivers are reviewed.

In Chapter 3 a novel analytical model for the design of Dickson rectifiers is presented. The model predicts the rectifier's input and output voltages based on the rectifier's input power. The proposed model can accurately predict the behavior of the rectifier in both the low-power and high-power regimes. As a prototype, a one-stage rectifier is fabricated in TSMC 130-nm CMOS process. Simulation and measurement results are in good agreement with the model. The model can accurately predict passive amplification produced by the lossless and lossy matching network based on the input power level, enabling the designers to find the optimum rectifier's design parameters and matching network quickly. The proposed method co-design methodology reduces the design time required to find RFEH optimum design parameters

for maximum power efficiency compared to the previous methods that use iterative simulations to find the optimum design variables.

In chapter 4, a highly efficient RFEH is proposed by producing an adaptive compensation voltage using a secondary matching network. The secondary matching network passively amplifies the input voltage of the rectifier and feeds it to the transistor gates producing an adaptive compensation voltage. The produced compensation voltage reduces the forward conduction loss of the transistors in the rectifier chain by increasing the $V_{gs}$ of transistors when they are conducting, and reduces the leakage loss by reducing the transistors' $V_{gs}$ when they are off. Simulation and measurement results show that the proposed rectifier's efficiency is 20% higher compared to the conventional ones showing a significant improvement in the efficiency. To verify the proposed rectifier's efficacy, a single-stage rectifier was fabricated in TSMC 130-nm CMOS process, and simulation and measurement results are in good agreement.

In Chapter 5, an ultra-low-power WuTx capable of simultaneously transmitting two analog sensor signals is introduced. The WuTx comprises a comparator, a relaxation oscillator, a ring oscillator, and voltage references working in the subthreshold region. By eliminating the paths between the ground and $V_{DD}$, and using a switching power amplifier, the idle power consumption of the WuTx is reduced significantly. By using a relaxation oscillator and a delay path, a pulse is generated with its HIGH and LOW times that are modulated by the two input signals coming from the sensors. Therefore, using the proposed modulation technique, the power amplifier is activated only in a portion of the transmission period, lowering the average active power consumption of WuTx. In addition to increasing the transmission efficiency using the proposed modulation, a class E power amplifier is utilized at the output with external components that allow tuning of the transmitter output power, enabling different transmission ranges depending on the application. Finally, to reduce the power consumption of the proposed WuTx when it is completely off, high-Vt switches have been used to cut off the connections to the supply voltages. The proposed WuTX

is fabricated in TSMC's 65-nm CMOS process. The measurement results show that the transmitter consumes less than $7nW$ when it is completely off, and it consumes less than $30\mu W$ without considering the power amplifier power consumption at the output.

In Chapter 6, an integrated wireless transceiver is proposed consisting of a WuRx and a WuTx powered by harvesting RF energy. The co-design of RFEH and WuRx, and eliminating the low-efficiency PMU, has opened the possibility of achieving receiver sensitivities significantly higher than previously reported works. The ultra-low-power, ultra-low-voltage WuRX can work with supply voltages as low as 300 mV. Furthermore, instead of using an active LNA, an ultra-low-power envelope detector, constructed by a common-source amplifier working in the subthreshold region, has been utilized to minimize the receiver power consumption. Fabricated in TSMC's 130-nm CMOS process, the proposed WuRx consumes only 5.7 nW at 300 mV and can be continuously powered up by RF input power levels as low as -26 dBm. The complete WuRX and WuTX can work with a 600-mV supply voltage requiring a minimum RF input power level of -23 dBm. The utilized class E power amplifier in the transmitter outputs -11 dBm with 51% efficiency operating at a 2.45 GHz frequency and can be externally tuned for other output power levels.

## 7.2 Future Work

As described in Chapter 3, the rectifier's input impedance depends on its input power level. Therefore, if a matching network is designed for a certain input power level, as the input power changes there will be a mismatch between the antenna and the rectifier, reducing the overall efficiency of RFEH. To maintain the proper matching condition, an adaptive matching network can be used that changes based on the input power level to achieve the highest possible efficiency. An adaptive matching network can be realized by using capacitor banks for rough tuning and variable capacitors (varactors) for fine-tuning. An analog or digital control loop can be activated in

a time span to change the matching network capacitors until the best efficiency is achieved.

The RF-powered wireless transceiver proposed in this dissertation does not include integrated digital or sensor circuitry. In the future, it would be interesting to integrate all the required digital baseband and sensor circuitry inside one chip to arrive at a complete integrated solution. In addition to that, the matching network and antennas can be integrated inside the chip to save the area which can be done by using higher operating frequencies requiring smaller antenna and inductor sizes.

## 7.3 Related Publications

The following is a summary of major contributions from this work:

### Journal Publications:

1. Mohammad Amin Karami and Kambiz Moez, "Systematic co-design of matching networks and rectifiers for CMOS radio frequency energy harvesters," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 8, pp. 3238–3251, 2019.

2. Mohammad Amin Karami and Kambiz Moez, "An ultra-low-power low-voltage WuTx with built-in analog sensing for self-powered WSN," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 7, pp. 2274–2287, 2020.

3. Mohammad Amin Karami and Kambiz Moez, "A Highly-Efficient RF Energy Harvester Using Passively-Produced Adaptive Threshold Voltage Compensation," IEEE Transactions on Circuits and Systems I: Regular Papers, (Manuscript : TCAS-I-01601-2020, submitted in Nov 2020, 14 pages) .

4. Mohammad Amin Karami and Kambiz Moez, "An Integrated RF-powered Wireless Transceiver with -26 dBm Sensitivity," IEEE Transactions on Circuits

and Systems I: Regular Papers, (Manuscript : TCAS-I-01560-2020, submitted in Nov 2020, 12 pages).

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