University of Alberta

VERTICALLY-INTEGRATED CMOS TECHNOLOGY FOR THIRD-GENERATION IMAGE SENSORS

by

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Abstract

Over the past four decades, CCDs and CMOS active-pixel sensors have defined the first and second generations of electronic image sensors, respectively. They are the core components of digital still and video cameras. However, despite significant progress, visible-band digital cameras do not rival the human eye entirely. For example, most CCD and CMOS image sensors suffer from low image quality in dim scenes and low dynamic range relative to human perception. To realize a third-generation of image sensors with superior capabilities, vertical integration is a promising approach. A process flow to support research of this nature in Canada was developed with CMC Microsystems. Using the flow, a vertically-integrated (VI) CMOS image sensor with competitive dark limit and dynamic range was presented. Silicon CMOS dies and hydrogenated amorphous-silicon photodetector dies are first designed and fabricated separately, and are then assembled with solder bumps by flip-chip bonding. The CMOS circuits include an electronic feedback that maintains a constant potential across each photodetector, which means the light-sensitive film need not be patterned. Methods to ensure stability of the feedback loop are presented. Using semiconductor physics for a simplified photodetector structure, a mathematical model that employs intuitive boundary conditions is proposed. Analytical and numerical solutions are used to explain and calculate the optimal thickness of the light-sensitive film. In this fashion, efforts to establish a third generation of image sensors through VI-CMOS technology are advanced.

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List of Abbreviations

ADC	Analog-to-Digital Converter
APS	Active Pixel Sensor
ASIC	Application-Specific Integrated Circuit
BL	Bright Limit
C	Capacitance
CCD	Charge Coupled Device
CDS	Correlated Double-Sampling
CMC	Canadian Microelectronics Corporation
CMOS	Complementary Metal-Oxide-Semiconductor
CNT	Carbon Nanotube
CSF	Contrast Sensitivity Function
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapour Deposition
DL	Dark Limit
DPS	Digital Pixel Sensor
DR	Dynamic Range
ENIG	Electroless Nickel and Immersion Gold
FOM	Figure of Merit
FPA	Focal Plane Array
FPGA	Field-Programmable Gate Array
FPN	Fixed Pattern Noise
HVS	Human Visual System
IC	Integrated Circuit
IR	Infrared
L	Inductance
MEMS	Micro-Electro-Mechanical System
MLF	Most Limiting Factor
MSM	Metal-Semiconductor-Metal
MTF	Modulation Transfer Function
PC	Power Consumption
PCB	Printed Circuit Board
PECVD	Plasma-Enhanced Chemical Vapour Deposition
PM	Phase Margin
PPS	Passive Pixel Sensor
PVD	Physical Vapour Deposition
QE	Quantum Efficiency
R	Resistance

RF	Radio Frequency
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SOI	Silicon on Insulator
SR	Spatial Resolution
SRH	Shockley-Read-Hall
SWCNT	Single-Walled Carbon Nanotube
SWE	Steabler-Wronski Effect
TCO	Transparent Conductive Oxide
TCP	Transparent Conductive Polymer
TFA	Thin Film on ASIC
TFT	Thin Film Transistor
TR	Temporal Resolution
TSM	Top Surface Metallurgy
TSV	Through-Substrate Via
UBM	Under-Bump Metalization
USB	Universal Serial Bus
VASE	Variable Angle Spectroscopic Ellipsometry
VF	Visual Field
VI	Vertically-Integrated

Chapter 1

Introduction

At present, there is an extraordinarily wide range of applications for digital cameras, such as machine vision systems, space research, medical imaging, defense, and consumer-use cameras. For these applications, engineers are required to design cameras that can capture scenes at high video rate, and that are able to produce high quality images. Furthermore, in visible-band imaging, digital cameras are often expected to compete with the human eye. However, high performance on all imaging parameters cannot be achieved simultaneously with current image sensors [1]. Consequently, today's digital cameras do not rival the human eye [2].

CCDs and CMOS active-pixel sensors (APSs), which define the first and second generations of electronic image sensors, respectively, are both planar technologies. Performance of digital cameras can be improved with additional pixel circuits. But integration of photodetectors with electronics in CCDs is impossible. With CMOS APSs, more pixel-level electronics results in a large pixel area or requires design in a nanoscale process, which may be unsuitable for photodetection. Instead, fabrication of image sensors by vertical stacking of active devices, a method that has long been used for imaging in invisible bands, holds great promise for visible-band imaging.

The semiconductor industry, which has so far been driven by Moore's Law, introduced a dual-trend roadmap in 2010. In addition to the traditional trend, which focuses on device miniaturization, the roadmap now includes technologies for 3D integrated circuits (ICs), which target heterogeneous microsystems, such as electronic image sensors. Vertical integration offers several advantages over planar technologies. First, only one package is required for several dies, which makes it possible to build lighter and more compact systems [3]. Second, because the long traces on a printed circuit board (PCB) are replaced by much shorter connections between dies, the resistance (R) and capacitance (C) of interconnects are significantly lowered. This results in a notable reduction in transmission power loss. Moreover, RC delays become smaller and, therefore, the interconnect bandwidth increases [4]. In addition, the information flow between dies may be raised substantially with vertical integration because the number of connections between dies is area limited, not perimeter limited as with planar technologies.

Electronic imaging is a key field that can benefit from vertical integration. Thus, the focus of this thesis is on advancing vertically-integrated (VI) CMOS technology for image sensors in order to enhance performance of digital cameras. With the boost to performance VI-CMOS technology can provide to digital cameras, it is likely to define the third generation of image sensors.

1.1 Third-Generation Image Sensors

The first electronic image sensors were presented in the 1960s. They were fabricated in MOS technology, and the photodetector readout was based on the passive pixel sensor (PPS) configuration. CCD technology emerged in the early 1970s, and became the dominant technology in electronic imaging for the following three decades. Therefore, it defines the first generation of electronic image sensors. CMOS image sensors could not compete with CCD sensors at that time because they used to have larger pixel dimensions, higher noise levels, and lower sensitivity. In general, CMOS PPS performance was poorer relative to that of CCDs [5].

CMOS image sensors re-emerged in the early 1990s due to the invention of the active pixel sensor. CMOS APS technology launched the second generation of electronic image sensors. Its main advantage over CCD is on-chip functionality. CMOS image sensors are fabricated in standard CMOS processes, allowing analog and digital signal processing circuits to be integrated on the same die as the sensor array. These circuits, which can be placed at chip, column, and pixel level can be used for operations such as timing and addressing, and can also assist in improving image quality and overall performance. With standard CCD technology, however, CMOS circuits may not be integrated either in the pixel or elsewhere on the chip.

For vision applications, image sensors should have features such as high spatial and temporal resolution, high signal-to-noise ratio, high dynamic range, and low dark limit. Advanced pixel-level circuitry, such as digital pixel sensors (DPS), may be used to address these competing requirements. With CCD technology, however, standard CMOS circuits may not be integrated either in the pixel or elsewhere on the chip. Although DPS is possible with CMOS technology, in-pixel circuits and photodetectors must be laterally integrated. Thus, it is impossible to use advanced circuitry without either having impractical pixel dimensions or using a nanoscale CMOS process, which is less suitable for photodetection. Scaling down of the CMOS process involves shallower diffusion layers and increased levels of channel doping. This results in increased dark noise, which degrades photodetection in the dark [6].

Image sensors are likely to benefit from vertical integration because each tier can be fabricated in a technology optimized for the type of devices it contains. Image sensors require photodetectors for sensing, analog circuits for amplification and pre-processing, and digital circuits for control and post-processing. While digital circuits may exploit the advantages of a nanoscale CMOS process, photodetectors may be fabricated in a larger scale process. Analog circuits may be fabricated in an intermediate scale process or, with robust design methods, in the same process as the digital ones. Furthermore, in some fabrication methods, the photodetector tier need not use crystalline silicon, which makes it easier to target invisible bands of the electromagnetic spectrum.

VI-CMOS technology allows distribution of semiconductor devices across overlapping tiers. In theory, it enables small pixels for high spatial resolution and also advanced pixel-level circuitry to address other important measures of imaging performance. Therefore, the capabilities of VI-CMOS image sensors are likely to surpass those of image sensors made by planar technologies. The VI-CMOS technology is expected to define a third generation in electronic imaging.

There are published works from as early 1980 that describe VI image sensors for the infrared (IR) band, where readout is done using silicon CCDs [7]. These VI-CCD image sensors were made either by direct deposition of IR photodetectors on silicon CCDs or by bonding a substrate with IR photodetectors to a substrate with CCDs using solder bumps. Following the emergence of the CMOS APS technology, CMOS readout circuits increasingly were used in VI image sensors that targeted invisible bands. For example, Bajaj describes VI-CMOS image sensors for the IR band in 2000 [8].

Although the motivation for VI-CMOS image sensors started with imaging in invisible bands, where the optoelectronic properties of crystalline silicon make it unsuitable for photodetection, the advantages offered by vertical integration have attracted international research groups since the late 1990s to use this approach also for imaging in the visible band. Examples include: (1) the work done by Benthien *et al.* [9], who used the direct deposition method, which they named "thin film on ASIC" (TFA); (2) image sensors presented by Rockwell Scientific (now a part of Teledyne) [10] that were fabricated using the solder bump or flip-chip bonding method; and (3) the image sensor shown by Lincoln Laboratories in MIT [11] that was based on the through-substrate-via (TSV) approach. Despite demonstrating functioning VI-CMOS image sensors for imaging in the visible band, these works do not explain how the area of electronic imaging can be advanced by a transition to vertical integration.

This thesis identifies the most limiting factors with current electronic image sensors that are fabricated in planar technologies, and elaborates on ways to address them by VI-CMOS technologies. Moreover, this thesis presents methods that allow design engineers to take advantage of the increased degrees of freedom offered by vertical integration to improve performance.

To conclude, the first and second generations of electronic image sensors are defined by CCD and CMOS APS technologies, respectively. Both are planar technologies, where performance is limited as all devices must be fabricated in the same process on the same tier. Making a transition to VI-CMOS technologies is a promising way to advance the field. Although VI image sensors have been fabricated since the early days of CCDs, no trials have been made to overcome the weakness of planar image sensors by exploiting VI-CMOS technologies. Addressing this deficiency is the main contribution of this thesis to the area of electronic imaging.

1.2 Vertically-Integrated CMOS Technology

The advantages of VI-CMOS technologies are not limited to image sensors. In fact, most heterogeneous microsystems are likely to benefit from these technologies. In 2010, the International Technology Roadmap for Semiconductors (ITRS) has officially announced that technologies for 3D ICs now define a new trend in the industry roadmap. The status of technologies for vertical integration at international and national levels is discussed in the following sections.

1.2.1 3D Integration Roadmap

In 1965, Moore [12] was the first to propose a technology roadmap for the semiconductor industry. After analysing market data that relates manufacturing cost of a single component to component density, he forecast that the number of components per substrate area is likely to increase "at a rate of roughly a factor of two per year" for at least 10 years. This statement, which is now known as "Moore's Law", had a great impact for more than forty years. Increase in device densities as gate electric-field values are maintained constant results in higher-speed and lower-power MOS circuits. The latter two parameters, along with reduction in minimum feature size, have became the main driving forces of the semiconductor industry.

A white paper that was released by the ITRS in 2010 presents a dual-trend roadmap for the semiconductor industry [13]. The first trend for future development has been labeled as "More Moore". It focuses on device miniaturization and mainly applies to digital applications, such as memory and logic circuits. The "More Moore" trend simply continues the traditional approach of Moore's Law. The second trend, which has been labeled as "More than Moore", focuses on functional diversification of semiconductor devices. It has evolved from systems that include

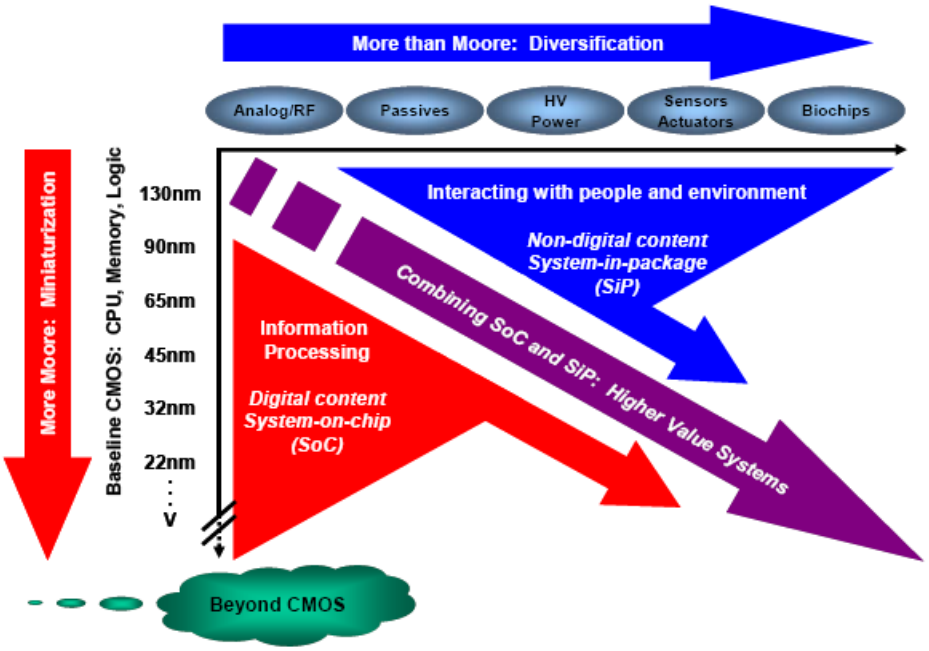


Figure 1.1: Diagram taken from a white paper of the ITRS that was released in 2010 [13]. The dual trend of the ITRS includes device miniaturization, or "More Moore", as well as functional diversification, or "More than Moore".

both digital and non-digital functionalities, such as radio frequency (RF) circuits and biochips. A diagram of the dual-trend roadmap is shown in Fig. 1.1.

While "More Moore" devices fulfill roles in the digital signal processing and storage components of a system, and might be considered as constituting the system's brain, "More than Moore" devices employ heterogeneous integration to form microsystems that are able to interact with the external world. This includes applications where transducers, i.e., sensors and actuators, are used, as well as subsystems for power generation and management. There is a wide variety of fields where there is a demand for "More than Moore" devices, e.g., communication, health care, and security.

Yole Développment, a market research and strategy consulting company based in Europe, is expecting a rapid growth of the 3D TSV market in the near future [14]. Electronic image sensors nicely fit into the "More than Moore" trend because this trend emphasizes heterogeneous integration of functionalities into compact systems, and Yole Développment forecasts a significant portion of the market to be based on applications related to CMOS image sensors, as shown in Fig. 1.2.

1.2.2 3D IC Technologies

Technologies for 3D integration of ICs can be divided into three groups, as shown in Fig. 1.3: 3D IC packaging, 3D IC integration, and 3D silicon (Si) integration [15]. Unlike 3D IC packaging, the other two technologies are based on TSVs. With 3D IC packaging, each chip or die has only one active side. With TSVs, however, the circuits are accessible from both sides of the chip and, practically, there is no more distinction between the front side and the back side. Among the three technology groups, only 3D IC integration and 3D Si integration are incorporated in the "More

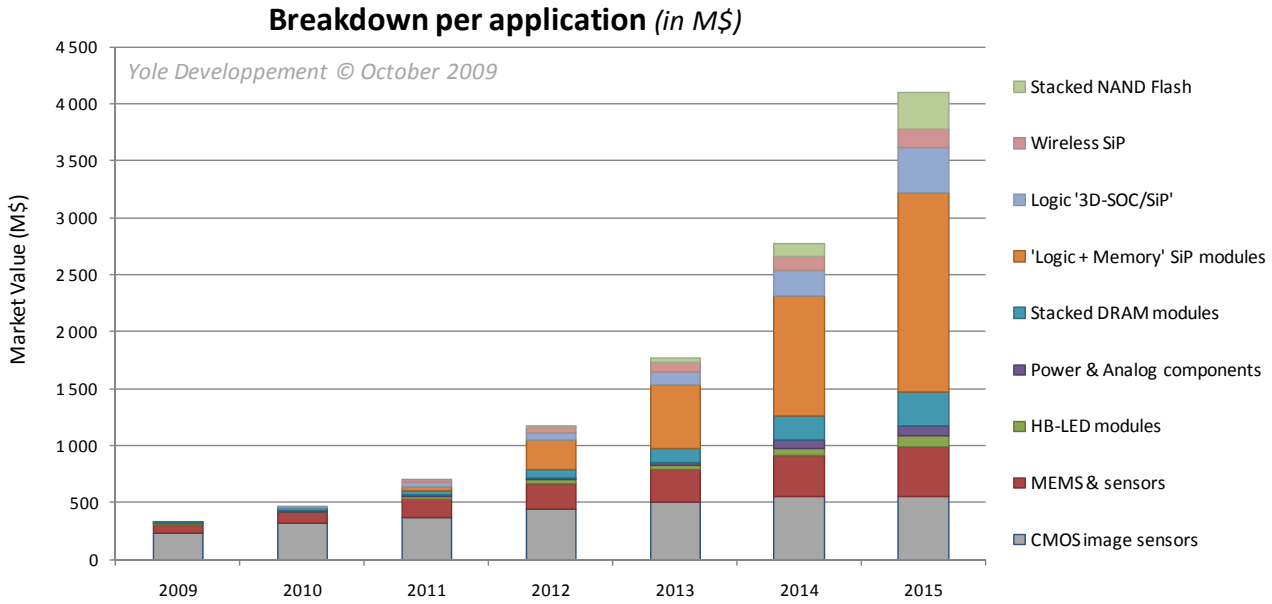


Figure 1.2: Market value forecast of 3D TSV packaging, from a report by Yole Développment [14]. The market is expected to show a rapid growth in the coming years. Applications related to CMOS image sensors are anticipated to hold a significant portion of the 3D TSV market.

than Moore" trend.

3D IC packaging: The microsystems are composed of two or more chips that are stacked vertically using conventional packaging methods, such as wire bonds, solder bumps, gold stud bumps, and conductive adhesives. Examples include 3D memory stacking, such as Samsung's multi-chip-package (MCP) memory [16], and package-on-package (PoP) microsystems [17]. The 3D IC packaging technologies are considered mature.

3D IC integration: The difference between 3D IC integration and 3D Si integration (below) is that, in the former, chips are bonded using bumps, e.g., solder, gold, or conductive adhesive, whereas the latter is based on bumpless bonding. The stacking in 3D IC integration can be done at three different levels: chip-to-chip (C2C), chip-to-wafer (C2W), and wafer-to-wafer (W2W). Kurita *et al.* [18], for example, present a stacked DRAM made by a process that includes etching of TSVs in the silicon substrate and Cu/Sn-Ag solder bumps. 3D IC integration technologies are currently in the phase of industrialization.

3D Si integration: The vertical stacking is based on pad-to-pad bonding, mainly Cu-to-Cu bonding [19] and oxide-to-oxide bonding [11]. These technologies are expected to have better performance than 3D IC integration technologies. Power consumption, profile, weight, and manufacturing cost of microsystems made by 3D Si integration are expected to be lower than those of microsystems made by 3D IC integration. However, 3D Si integration lags behind 3D IC integration because of lower yield and serious problems related to heat dissipation. Bonding can be done only at the wafer-to-wafer (W2W) level, which results in reduced yield because one cannot avoid bonding of nonfunctional dies to good ones. Moreover, surface pre-treatment is done under more rigorous conditions because 3D Si integration requires

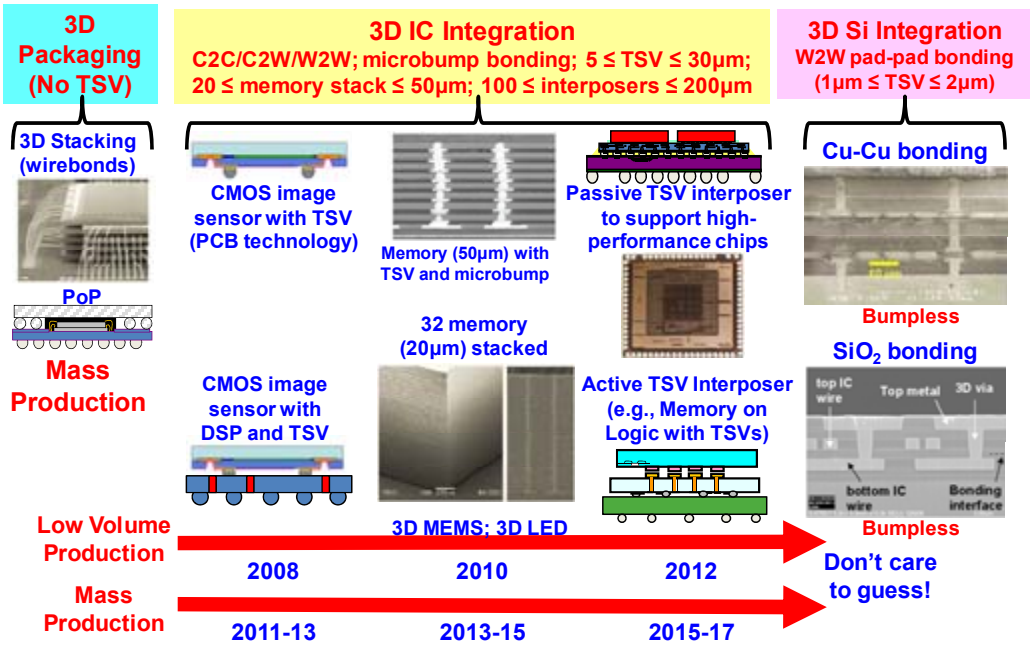


Figure 1.3: The 3D integration roadmap, taken from Lau [15]. *Low Volume Production* implies that only a small number of companies are shipping products, while *Mass Production* refers to a significant number of suppliers.

higher levels of surface cleanness and flatness than 3D IC integration. Thermal management is a major problem because the pad-to-pad bonding essentially leaves no gap between the stacked tiers. Although 3D Si integration technologies have been studied for more than 25 years [20], they are still far from being suitable for mass production.

To increase the reliability of "More than Moore" microsystems, there is plenty of room for research and development in areas starting with the design process and ending with proper functionality of finished microsystems.

So far, tools used for design of "More than Moore" microsystems were based on standard design tools inteneded for 2D ICs. Such ad hoc techniques were sufficient as long as the designs were small and simple. However, with an increased level of complexity and a transition from testing of small prototypes to commercial production, the improvised approach is no longer acceptable, and one needs to develop "true-3D" tools [21]. A true-3D tool needs, for example, to be able to handle 3D hierarchy, i.e., it is required to work with functional blocks that are spread over several tiers, and which possibly include devices fabricated by different technologies. Moreover, the effect of the TSVs on mechanical and thermal stress, as well as their electrical RLC models, need to be incorporated into the design tools.

The fabrication process of "More than Moore" microsystems requires improvement in the accuracy level of the equipment used for alignment [22]. Also, mass production tools for TSVs are needed as well as better techniques for wafer thinning and handling of thin wafers. Furthermore, one needs to develop a process that ensures high yield in the preparation of TSVs with high aspect ratio.

Inspection methods for 3D microsystems need to be developed. Testing methods for known-good-dies at wafer level are no longer sufficient [21]. Process steps that involve wafer thinning, metalization, and stacking cannot guarantee that a die that was found functional at wafer level is also functional upon completion of the assembly process. Test structures that can determine the functionality of the assembled microsystem need to be integrated in each tier.

Lastly, for a proper functionality of "More than Moore" microsystems over reasonable periods of time, efforts are currently being made to develop methods for power delivery and distribution, as well as for heat dissipation [23]. For example, VI microsystems need to have adequate density of power and ground vias to prevent significant voltage swings during operation. Thermal management is a major problem in "More than Moore" microsystems because the die stacking results in a substantial increase in the total power generated per unit area, and the small gap between the tiers turns placement of cooling channels into a difficult task. Also, differences in thermal coefficients of expansion (TCEs) cause stress and deformation that may lead to microsystem failure.

1.2.3 CMC Microsystems

Although the research presented in this thesis is concerned with vertical integration of active devices, it does not focus on the practical aspects related to development of 3D IC technologies. Instead, the research needs to rely on outsourcing of work to external service providers. This can only be done through the available national infrastructure, which, therefore, is an important factor for a work of this nature. The Canadian Microelectronics Corporation (CMC), operating as CMC Microsystems, is the organization that connects academic institutions in Canada with third-party companies that provide services, such as fabrication and packaging, to the semiconductor industry. CMC clients have access to both national and international suppliers.

Apart from the work presented in this thesis, Canadian research institutions have developed and demonstrated microsystems that are based on vertical integration of a sensor array and a readout circuit array. Aziz *et al.* [24] presented a 3D microsystem for multi-site extra-cellular neural recording that is composed of a CMOS die and an electrode die, where the two are flip-chip bonded using gold stud-bumps. Izadi *et al.* [25] presented an image sensor for medical X-ray imaging. It is composed of amorphous-selenium photodetectors deposited on amorphous-silicon thin film transistors (TFT) that are used for readout. INO, a Quebec firm, has integrated uncooled bolometric sensors, which are micro-electro-mechanical systems (MEMS), and CMOS readout circuits. These VI-CMOS image sensors are designated for the IR and THz bands [26, 27].

Flip-chip bonding is categorized under 3D IC packaging technologies. It is not based on TSVs and, therefore, it is not a part of the "More than Moore" trend. However, this was the chosen fabrication method for the VI-CMOS image sensor prototype that was fabricated during the course of this thesis because, by the time the project was at its design stage, it was the only method for a microsystem of this nature that could be supported by CMC. Nonetheless, the design principles presented here are applicable also for VI-CMOS image sensors that are fabricated in "More than Moore" technologies. Today, CMC does offer access to a TSV-based process; this change was partly motivated by the work done for this thesis.

1.3 Scope of Thesis

To advance electronic imaging, vertical integration is exploited in this thesis. First, the work presents an evaluation method for design engineers to assess the limitations of a digital camera with respect to the human eye and vice versa. General principles related to design and fabrication

of VI-CMOS image sensors by flip-chip bonding are discussed next. A VI-CMOS prototype that was realized during the work is described as a specific example. Lastly, the thesis covers topics related to the design, modeling and simulation of devices and circuits that are unique to VI-CMOS image sensors. Modeling and simulation is an integral part of the design process; it is needed to ensure proper and optimal functionality.

Chapter 2 presents an evaluation method for digital cameras. It is a tool to measure the performance gap between a digital camera and the human eye. Eight properties of imaging performance are considered: power consumption, temporal resolution, visual field, spatial resolution, signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR), dynamic range (DR), and dark limit. Experimental work done with human observers and cadavers is reviewed to assess the properties for the human eye, and assessment methods are also given for digital cameras. The method is applied to 26 electronic image sensors of various types and sources, where an ideal thin lens is assumed to complete a digital camera. Results show that modern digital cameras, which are based on image sensors fabricated in planar technologies, do not rival the human eye. The DR and dark limit are shown to be the two most-limiting factors. Technologies for 3D ICs are promising to boost the performance of image sensors, and lead to a digital camera that rivals the human eye.

Principles in the design and fabrication of VI-CMOS image sensors by flip-chip bonding are discussed in Chapter 3. These image sensors are composed of two dies: a CMOS die that is prepared in a commercial process, and a photodetector die that is prepared in a custom process. After fabrication, preparation of bond pads, and deposition of solder bumps on the smaller die, the two dies are aligned precisely and finally bonded in a flip-chip process. Chapter 3 also describes a specific prototype that was designed at the University of Alberta (UofA) and fabricated via CMC Microsystems, the UofA Nanofab, and Micralyne Inc. A digital camera was developed to test the prototype. It communicates in real time with a PC through a USB port. Experimental results obtained with the VI-CMOS prototype show that it has a low SNDR, which is expected as the data conversion is done at board level. However, the prototype demonstrates a high DR, thanks to a logarithmic response of the CMOS circuits, and its dark limit is one order of magnitude lower (better) that that achieved with conventional image sensors.

Chapter 4 discusses design principles of feedback active pixels. These circuits can be used to improve photodetector performance by avoiding pixel-level patterning of the photodetector array. This situation is unique to VI-CMOS image sensors. In CMOS image sensors, physical borders must be defined for the photodetectors because the pixel area is shared with other CMOS devices. In an unpatterned photodetector array, crosstalk may be reduced by maintenance of a constant electric potential at all photodetectors in the array. This is achieved using an operational amplifier with a negative feedback in each pixel. Unlike with conventional CMOS image sensors, the photodetector current defines the input signal as voltage must be fixed. The chapter presents several topologies that can be used to implement a logarithmic feedback, and indicates the one that has the lowest power consumption. Issues related to stability and compensation are also considered because changes in the phase of signals traveling in the feedback loop might result in an oscillating response. Simulation and experimental results obtained with the VI-CMOS prototype are presented.

Chapter 5 presents a mathematical model for photodetectors in VI-CMOS image sensors. This model is a useful tool for design and optimization of such devices when prepared in a custom process. The model is used here for optimization of the thickness of the light-sensitive semiconductor for a low dark limit. Moreover, it treats the case of sensors with logarithmic response. An analytical solution and a numerical solution have been derived, which are shown to be comparable. Experimental results obtained with two VI-CMOS image sensor prototypes that differ only in the

thickness of the a-Si:H layer show a good agreement with simulation results.

Chapter 6 concludes the work, first by summarizing the contributions of this thesis. It also discusses several directions by which principles developed in this thesis can be further extended and implemented. One promising direction is lens-less X-ray imaging for medical applications.

Chapter 2

Rivaling the Human Eye

Despite significant progress in the area of electronic imaging since the invention of the CCD more than 40 years ago, digital cameras still do not rival the human eye. Consider that, in his keynote address to the 2010 International Solid-State Circuits Conference, Tomoyuki Suzuki, the Senior Vice-President of Sony, said "In developing the CMOS image sensor, the goal is exceeding human vision" [2]. Toward that end, this work introduces a method to evaluate the performance gap between a digital camera and the human eye. A clear definition and quantification of limiting factors will help design engineers realize a digital camera to rival the human eye.

The large diversity in design and fabrication technologies for electronic image sensors encouraged many research groups worldwide to develop performance evaluation methodologies for digital cameras or image sensors. Franz *et al.* [28], for example, suggested a method that mainly considers the modulation transfer function (MTF) and the signal-to-noise ratio (SNR). Rodricks *et al.* [29] introduced a method that includes metrics such as dark noise, linearity, SNR, and MTF, and compared the response of a camera with a CCD sensor to that of a camera with a CMOS sensor at various integration time and ISO speed values. The European Machine Vision Association (EMVA) developed the EMVA Standard 1288 [30], for "Characterization and Presentation of Specification Data for Image Sensors and Cameras", to unify the way image sensors are tested and evaluated. Spivak *et al.* [31] analyzed high dynamic range image sensors, while focusing on SNR, dynamic range (DR), and sensitivity. Janesick [32] compared the performance of a back-illuminated CCD image sensor to that of linear CMOS image sensors with photodiode and pinned-photodiode configurations. Unlike the other works, he does define a figure of merit for an image sensor, which is determined by the SNR. This approach, however, is limited because it discounts other important factors, such as sensor dimensions and power consumption, that also affect the overall performance. Most importantly, none of the above methods uses a benchmark to evaluate electronic image sensors or imaging systems.

In research on image quality assessment, rendering techniques, and display technology, a benchmark is very well defined. Systems have always been evaluated according to how they match the characteristics of the human visual system (HVS) [33]. Brémond *et al.* [34], for example, presented a method for evaluation of still images that is composed of three indices of HVS image quality metrics: visual performance, visual appearance, and visual attention. Ma *et al.* [35] proposed a method for quality assessment of still images and video frames that is based on human visual attention. With any non-artificial image that is displayed in a digital format, the process starts when a scene is captured by an electronic imaging system. This is followed by digital signal processing (DSP), which includes steps such as tone mapping and compression. If the performance of the imaging system is such that a large amount of information is lost, even

when sophisticated DSP algorithms are used, a high quality reconstruction of the original scene is infeasible.

In this work, digital cameras are evaluated with respect to the human eye. A demand for a digital camera that can successfully compete with the human eye exists in a large range of applications, varying from consumer electronics to machine vision systems for robotic modules. The work reviews the structure and operating principles of the human eye, and discusses performance measures and testing techniques that are used with human observers. For each one of the identified parameters, the work specifies the performance of the eye in healthy adults. This value is used as the performance benchmark for digital cameras. To fairly compare between imaging systems of different types, the evaluation is always referred to the scene, i.e., the imaging system input. The process is concluded with a single figure-of-merit (FOM), which is given in dB for an easy representation of large numbers.

Section 2.1 discusses considerations in the selection of parameters for the evaluation process. It also explains how each one of the chosen parameters is assessed for the human eye and for digital cameras. Section 2.2 presents the results obtained after the proposed method was applied to 26 modern electronic image sensors of diverse types and sources, assuming an ideal thin lens is used to form a complete digital camera. Section 2.3 discusses past trends in the area of electronic imaging, using them to predict which current trends are likely to boost the performance of digital cameras, by overcoming their most limiting factors, and to become a future trend in electronic imaging. Finally, Section 2.4 concludes the work.

2.1 Method

Various parameters can be used for characterization of imaging systems. They include cost, physical properties like weight and size, power consumption, visual field, spatial resolution, temporal resolution, parameters related to signal and noise power, and colour mapping. The performance evaluation presented here considers only some of these properties, but the method may be readily extended in future.

Cost is excluded because it is not fixed for a digital camera. The price varies (usually drops) with time and also depends on the place of purchase. Moreover, the human eye is priceless, and so all digital cameras are infinitely cheaper by comparison. Weight and size are excluded because they depend on the design of the camera body and on the lens used. There are too many optional combinations for a given image sensor, and so these physical properties are excluded for simplicity. To narrow the scope of this work further, colour mapping is not included in the performance evaluation method. All image sensors are treated as monochrome ones, i.e., they are evaluated according to their response to a varying intensity of white light. In general, colour mapping of a digital camera depends not only on the image sensor, but also on the algorithm used for image processing and display. Therefore, various options can be applied to the same image sensor.

The eight parameters that are considered for performance evaluation are: power consumption (PC), visual field (VF), spatial resolution (SR), temporal resolution (TR), signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR), dynamic range (DR), and dark limit (DL). Two parameters, VF and SR, are related to the geometry of the imaging system, and the last four parameters are related to signal and noise power. To guarantee that performance is not limited by lens imperfections, and for simplicity, an ideal thin lens is assumed to complete the digital camera. In cases where the imaging system includes digital signal processing (DSP), the properties of the image that is read after the DSP is applied are considered for the evaluation.

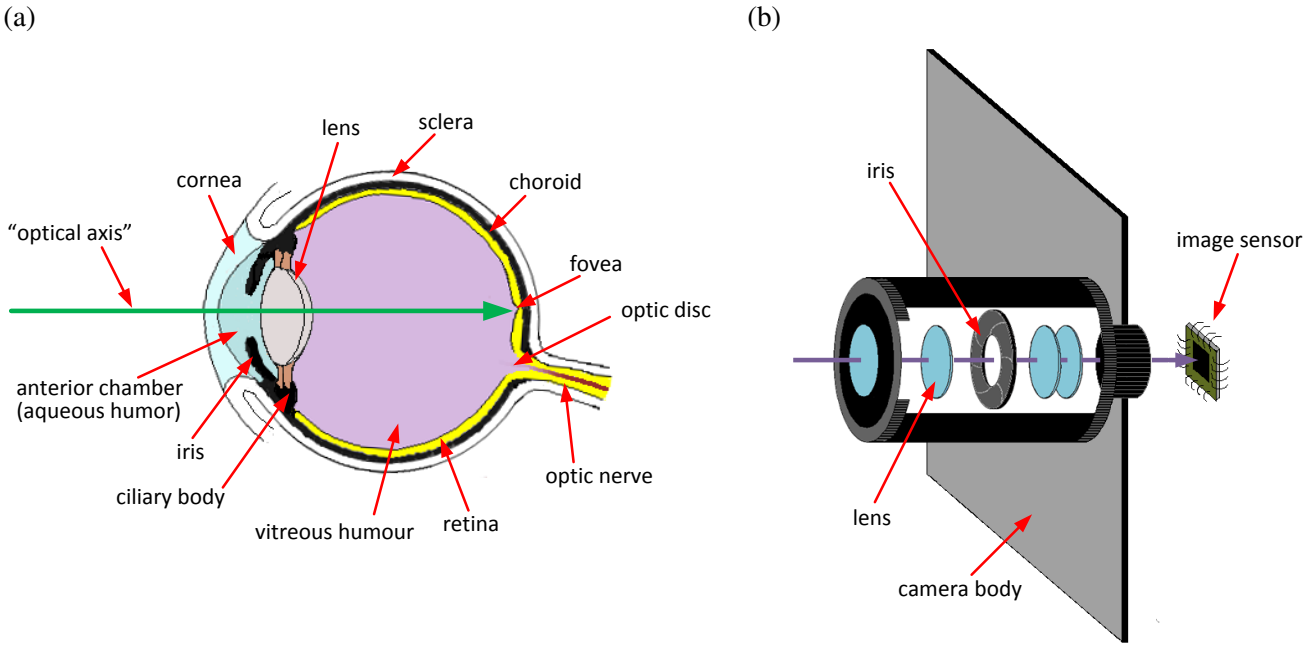


Figure 2.1: (a) Horizontal cross-section of the right eye (top view). Light enters the eye through the iris aperture (the pupil). It is refracted by the cornea and the lens before reaching the retina, which is a light-sensitive tissue. The fovea is rich in cone photoreceptors; it is responsible for sharp central vision. (b) In digital cameras, light enters the camera body through the aperture in the iris diaphragm. It is refracted by a system of lenses before reaching an image sensor located in the focal plane.

The evaluation process involves mathematical operations and, most importantly, calculation of ratios. Therefore, it requires explicit values to be defined for the parameters of all imaging systems, including the human eye. Consequently, the performance of the human eye is reviewed below, with reference to experiments done using human cadavers and observers.

2.1.1 Power Consumption (PC)

Fig. 2.1 shows diagrams of (a) the human eye and (b) a digital camera. There are many similarities between the two systems. Both include an iris with an aperture, which is called a pupil. The sclera and the camera body prevent light from entering the imaging system from any direction other than the pupil. Refraction of light in the human eye is performed by the cornea and the lens. While the cornea has a fixed focal length, the focal distance of the lens can be varied by muscles that change its shape. In digital cameras, refraction of light is done by a system of lenses. The retina is a light sensitive tissue; it is composed of a complex layered structure. Optics of the eye form an image that appears upside down on the retina. The retina converts the image into electrical signals that are sent to the brain through the optic nerve. The image sensor plays an equivalent role in digital cameras. It converts photons into electrical signals, which are then read out through electrical wires.

Comparison between the power consumption of a biological system and an electronic system that serve similar roles is established in electronic engineering. It is noteworthy when biological

Table 2.1: Approximate basal metabolic rates of different tissues that compose the human eye [37].

Type	Tissues	Metabolic rate $[\mathrm{W/m^3}]$
Passive	cornea, lens, sclera, choroid, vitreous humor, aqueous humor	0
Muscular	lens zonules, scleral muscle, ciliary muscle, iris dilator muscle, iris sphincter muscle	690
Neural	retina (including fovea)	10,000

systems can fulfill the same function while consuming less power. Carver Mead, who did extensive research on biologically-inspired electronics, emphasizes a comparison of power consumption in his book "Analog VLSI and Neural Systems" [36]. He went on to found Foveon, a digital camera company.

The power consumption of the human eye can be estimated using the basal metabolic rate of the different tissues from which it is composed. Some of the tissues, such as the sclera and the lens, have a very low metabolic rate and, therefore, can be categorized as "passive". There are also muscles that take part in the functionality of the eye, such as those that control the pupil and the lens. Their metabolic rate can be taken as that of typical muscle tissue in the human body. The retina is the most "power hungry" tissue in the human eye. Its metabolic rate is considered to be equal to that of brain gray matter. The metabolic rates of various tissues in the human eye are shown in Table 2.1, as reported by DeMarco *et al.* [37].

To estimate the power consumption of the human eye, one needs to assess the volume of the different tissues. Straatsma *et al.* [38] report statistical details about the dimensions of the retina based on measurements done with 200 eyes from human cadavers. A mean value of $1340\,\mathrm{mm}^2$ was calculated for the internal surface area of the retina from the reported data. The retinal thickness in healthy adults is $220\,\mu\mathrm{m}$ [39, 40]. This gives that the volume of the retina is approximately $295\,\mathrm{mm}^3$. Therefore, the power consumption of the retina is approximately $3\,\mathrm{mW}$. The metabolic rate of the muscle tissue is about one tenth of the retinal metabolic rate. Assuming the overall volume of muscle tissue in the human eye is less than 30 times the retinal volume, the power consumption of the eye is less than $10\,\mathrm{mW}$.

The power consumption of image sensors depends on the technology used for device fabrication and on the circuit design. In general, it increases with frame size and frame rate because more power is consumed with an increase in capacitance that needs (dis)charging and with an increase in cycle frequency. The power consumption of image sensors is obtained from datasheets or other publications for one or more frame rates chosen by the manufacturer or author.

2.1.2 Visual Field (VF)

The visual field of an imaging system is the overall volume "viewed" by the system. The clinical method used to evaluate the human visual field is called *perimetry*. Various techniques and instruments have been developed for this purpose; they can be categorized in several ways. The Goldmann perimeter is an example of an instrument for manual perimetry, while the Octopus perimeter and the Humphery visual-field analyzer are examples of computer-controlled instruments. In kinetic perimetry, a stimulus of a known and constant luminance moves at a steady speed from an area outside the patient's visual field to an area inside. The patient is asked to report when the stimulus has been perceived. In static perimetry, there are multiple stimuli with fixed locations. However, the luminance may be either constant or varied [41]. Threshold strategies determine the threshold luminance of the patient at different locations by gradually increasing the luminance intensity at fixed points until they are perceived. In suprathreshold strategies, the patient is presented with stimuli luminance above normal threshold values at various locations in his or her visual field [42].

The monocular visual field of a healthy adult extends approximately 50–60° superiorly and 70–75° inferiorly in the vertical direction [42, 41], as shown in Fig. 2.2(a). Horizontally, it extends about 60° nasally and 90–100° temporally, as shown in Fig. 2.2(b). The optic disc, which is the exit point of the optic nerve from the eye to the brain (see Fig. 2.1(a)), lacks photoreceptors. This causes a "blind spot" in the visual field that is located between 10° and 20° temporally. The binocular visual field extends about 200° horizontally because each eye covers about 100° temporally, which includes the nasal visual field of the other eye. Vertical extent of binocular vision is similar to that of monocular vision.

To allow a fair comparison between the visual field of imaging systems of different types, the solid angle subtended by the imaging system is calculated. Moreover, expression of the visual field as a solid angle emphasizes the fact that an imaging system captures a 3D spatial volume and not a 2D area. To simplify the calculations, which are required to estimate the solid angle subtended by the human eye, its visual field is treated as a right elliptical cone (see Fig. 2.2(c)). The solid angle subtended by an elliptical cone with opening angles $\theta_\perp$ and $\theta_\parallel$ ($\theta_\perp \geq \theta_\parallel$) is given by [43]

$$\Omega = 2\pi \left(1 - \Lambda_0(\varphi, \alpha)\right), \tag{2.1}$$

where

$$\varphi \equiv \frac{1}{2}\left(\pi - \theta_\parallel\right), \tag{2.2}$$

$$(\sin\alpha)^2 \equiv 1 - \left(\frac{\cos\left(\theta_\perp/2\right)}{\cos\left(\theta_\parallel/2\right)}\right)^2. \tag{2.3}$$

Λ_0 is Heuman's lambda function, which is given by [44]

$$\begin{aligned}\Lambda_0(\varphi, \alpha) =& \frac{2}{\pi} K(\alpha) E\left(\varphi, \pi/2 - \alpha\right) - \\ & \frac{2}{\pi}\left(K(\alpha) - E(\alpha)\right) F\left(\varphi, \pi/2 - \alpha\right),\end{aligned} \tag{2.4}$$

where $K(\alpha)$ and $E(\alpha)$ are complete elliptic integrals of the first and second kind, respectively, and $F(\varphi, \phi)$ and $E(\varphi, \phi)$ are incomplete elliptic integrals of the first and second kind, respectively.

To estimate the solid angle subtended by the monocular visual field of the human eye, the vertical opening angle, $\theta_\parallel$, is taken as 127.5°, and the horizontal opening angle, $\theta_\perp$, is taken as 155°.

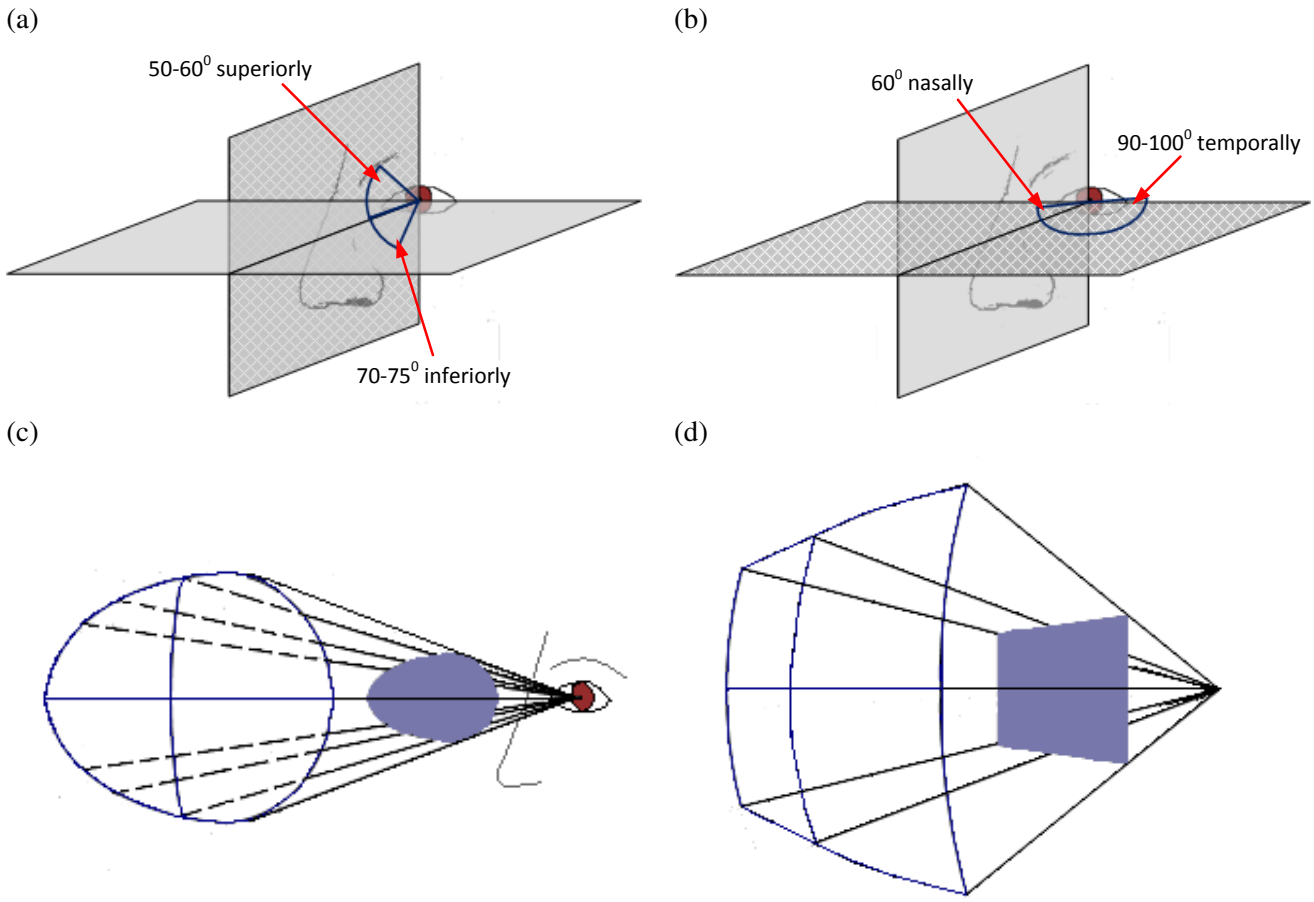


Figure 2.2: (a) The visual field of a healthy adult extends, in the vertical direction, approximately 50–60° superiorly and 70–75° inferiorly. (b) It extends, in the horizontal direction, about 60° nasally and 90–100° temporally. (c) For simplicity, the solid angle viewed by the human eye is taken as the one seen by a right elliptical cone. (d) The solid angle viewed by a digital camera is the one seen by a right rectangular pyramid. It varies with image sensor dimensions and lens focal length.

The blind spot in the visual field is ignored. A calculation performed using MATLABfunctions for the elliptic integrals shows that the human eye captures a solid angle of $4.123\,\mathrm{sr}$, i.e., $\Omega_{\mathrm{eye}} \approx 4.1\,\mathrm{sr}$.

Conventional image sensors are rectangularly shaped. Therefore, a digital camera views a solid angle of a right rectangular pyramid, as shown in Fig. 2.2(d). Its visual field depends on the width, w, and length, ℓ, of the sensor array, and on the focal length of the lens, f_ℓ. In this pyramid, the image sensor is considered as the base, and the apex is located at a distance f_ℓ from the centre of the base. The solid angle subtended by the image sensor, Ω_s, is given by [45]

$$\Omega_s = 4 \arcsin\left(\sin(\alpha_w/2) \cdot \sin(\alpha_\ell/2)\right), \tag{2.5}$$

where $\alpha_w = 2\arctan\left(w/(2f_\ell)\right)$ and $\alpha_\ell = 2\arctan\left(\ell/(2f_\ell)\right)$ are the apex angles of the right rectangular pyramid.

2.1.3 Spatial Resolution (SR)

The spatial resolution of an imaging system represents the finest detail or the highest spatial frequency that can be perceived by the system. It may be derived from the system's response to varying spatial frequency. For simplicity, the spatial resolution is examined here only for 1D patterns. The spatial response, for each spatial frequency, is defined through the Michelson contrast ratio, C, which is given by

$$C = \frac{I_{\max} - I_{\min}}{I_{\max} + I_{\min}}. \tag{2.6}$$

This is a general definition, where the term I can refer to various quantities. Although the spatial response is defined for sinusoidal-wave spatial patterns, testing is often performed with square-wave spatial patterns.

The spatial resolution of the eye is not uniform across the whole visual field. It is sharpest at the centre and gradually declines toward the periphery or, as described by Traquair, it is "an island of vision or hill of vision surrounded by a sea of blindness" [46]. This evolves from the non-uniformity of the retina. The fovea is the retinal area that is responsible for sharp central vision. Sharp vision of the whole visual field is obtained thanks to saccades, which are constant fast eye movements that bring different portions of the scene to the fovea.

A test pattern to characterize the spatial response of human observers is shown in Fig. 2.3(a), where L_0 is the adaptation luminance and $\Delta L = L_{\max} - L_{\min}$ is the tone difference. For a central pattern with a constant spatial frequency, $f_{\text{x-sc}}$, the examiner varies ΔL and the observer is asked to specify whether the tone difference is perceived. This is repeated until a threshold value, ΔL_{th}, usually defined as the level with 50% probability of detection, can be determined. For a comprehensive characterization of an observer's spatial response, tests need to be repeated with different $f_{\text{x-sc}}$ and L_0 conditions.

The threshold values can be used to construct a plot of the contrast sensitivity function (CSF), which is the inverse of the threshold contrast, C_{th}, as given by

$$CSF = \frac{1}{C_{\text{th}}} = \frac{L_{\max} + L_{\min}}{\Delta L_{\text{th}}}. \tag{2.7}$$

Fig. 2.3(b) shows the CSF of a young adult observer at four different adaptation levels. The spatial frequency is given in units of cycles per degree (cpd). The plot was constructed according to data presented by Patel [47]. The experiment was performed with an artificial pupil, whose diameter was smaller than the natural pupil diameter even at very bright conditions. Although original results were given in Td (Trolands), they were converted to cd/m^2. One Td, which represents the retinal illuminance, equals the scene luminance in cd/m^2 multiplied by the area of the pupil's aperture in mm^2. Conversion was done according to interpolation of data presented by De Groot and Gebhard [48] on the relationship between pupil diameter and scene luminance. The retinal illuminance (Td) was calculated from the expected pupil diameter (mm) at the corresponding scene luminance (cd/m^2). Fig. 2.3(b) shows that spatial response of the human eye improves with increasing L_0.

To define a benchmark for the spatial response of the HVS, Snellen visual acuity charts are considered. These charts have been used since the 19^{th} century as an evaluation standard for spatial response of human observers. During examination, the observer is asked to identify letters, or other patterns, of different sizes from a distance of 20 feet (or 6 meters). Those who can clearly perceive the letters in the row that matches visual acuity of $20/20$ are considered to have good acuity. The letter E in that row corresponds to a spatial frequency of $30\,\text{cpd}$. One may conclude from Fig. 2.3(b) that, at $30\,\text{cpd}$, the spatial response of the HVS in typical office luminance, i.e.,

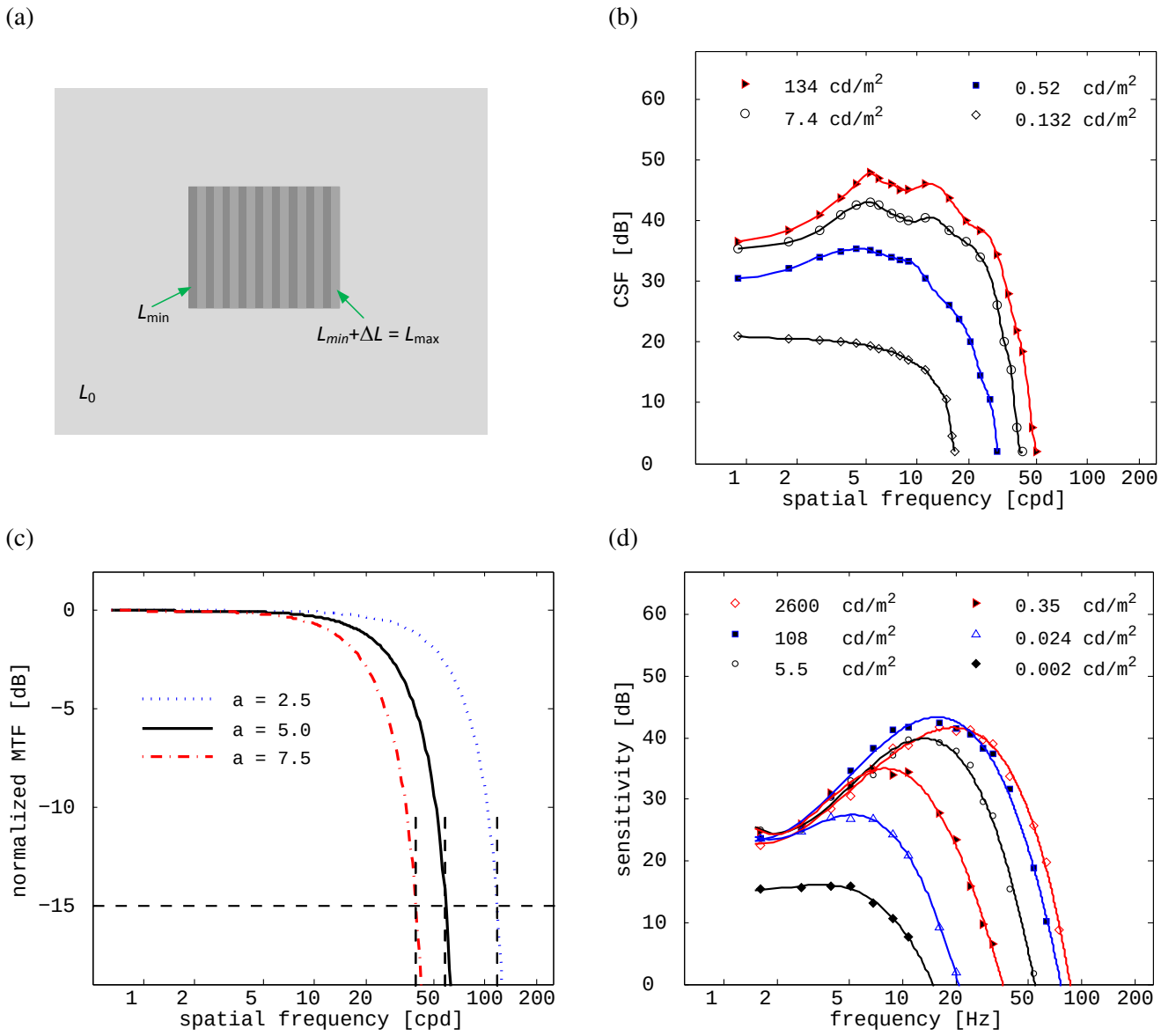


Figure 2.3: (a) A pattern to test the spatial response of human observers. L_0 is the adaptation luminance. The examiner varies ΔL until a threshold level, $\Delta L_{\rm th}$, can be determined. (b) The CSF of an observer with good vision at four adaptation levels [47]. (c) The normalized MTF of a digital camera with $f_\ell = 20\,\mathrm{mm}$, $p = 10\,\mu\mathrm{m}$, and $a = 2.5$, 5, and $7.5\,\mu\mathrm{m}$. Spatial frequencies at $15\,\mathrm{dB}$ deterioration are indicated. (d) The temporal response of an observer with good vision, using data from Kelly [49].

about $100\,\mathrm{cd/m^2}$, is about $15\,\mathrm{dB}$ lower than its maximal value. Therefore, for the performance evaluation, the spatial frequency at which the spatial response of a digital camera deteriorates by $15\,\mathrm{dB}$ is compared to the HVS benchmark of $30\,\mathrm{cpd}$.

Unlike testing methods with human observers, which have to be based on threshold values, with digital cameras one may gradually change the spatial frequency of the scene stimulus and measure the system response directly. However, as results of such measurements are often not published, the spatial response is estimated here by calculations based on system geometry. The overall spatial response of a digital camera is affected by the response of the image sensor and the response of each component that is placed in the path of the light, such as lenses and filters.

The image sensor is usually composed of a 2D array of rectangularly shaped pixels. The pattern of light formed on the image plane is sampled in each pixel by the photodetector. Because image sensors may be considered as linear and space-invariant (isoplanatic) systems [50], the sampled image is a two-dimensional convolution of the pattern on the image plane with the impulse response of the array, also called the point spread function (PSF). The impulse response is derived from the sampling pattern of the array.

The Fourier transform of the impulse response is called the optical transfer function (OTF). It defines the image sensor response to varying spatial frequencies along the x and y axes on the image plane, f_x and f_y, respectively, which are expressed in units of line-pairs per mm ($\mathrm{lp/mm}$). The modulation transfer function (MTF) is the magnitude of the OTF.

To simplify calculations, the MTF is given here for 1D patterns and does not consider aliasing. Yadid-Pecht [51] shows that, for an array with pixel pitch p and photodetector pitch a, the 1D MTF is given by

$$\mathrm{MTF}(f_\mathrm{x}) = \frac{a}{p}\,\mathrm{sinc}(af_\mathrm{x}), \tag{2.8}$$

where

$$\mathrm{sinc}(x) = \begin{cases} \sin(\pi x)/(\pi x), & x \neq 0; \\ 1, & x = 0. \end{cases} \tag{2.9}$$

The lens MTF needs to be multiplied by the MTF of the image sensor to calculate the spatial response of the digital camera. However, the lens is considered here to have an ideal spatial response, i.e., to have a unity MTF. While this is a simplification, the actual spatial resolution of the digital camera would not surpass the value taken here for the performance evaluation.

To refer the spatial response of the digital camera to the scene, the spatial frequency f_x in $\mathrm{lp/mm}$ on the image plane needs to be converted to $f_\text{x-sc}$ in cpd of the scene. Because an opening angle of 1° corresponds to a length of $d = 2f_\ell \tan 0.5^\circ$ on the image plane, $f_\text{x-sc} = f_\mathrm{x} d$.

The MTF is often normalized in order to represent the contrast ratio, C, of the frequency response. Theoretically, one concludes from (2.8) that the bandwidth of the spatial response improves without limit as the photodetector pitch diminishes. However, practically, the photodetector must be large enough to absorb an adequate number of photons to generate a detectable electrical signal. Fig. 2.3(c) shows the normalized MTF as calculated for a digital camera, where the sensor has a pixel pitch of $p = 10\,\mu\mathrm{m}$ and the lens has a focal length of $f_\ell = 20\,\mathrm{mm}$. Calculations were performed for three values of photodetector pitch. The spatial frequency at $15\,\mathrm{dB}$ deterioration, which is considered here as the spatial resolution, is shown for each case.

To conclude, the spatial response of the HVS can be extracted from experiments performed with human observers. The benchmark is determined using a commonly used standard—the $20/20$ row of the Snellen chart. With digital cameras, although the spatial response can be measured directly, experimental results are usually not provided. Therefore, it is estimated here according to the image sensor geometry and the given focal length.

2.1.4 Temporal Resolution (TR)

The temporal response of the human eye has been tested by different groups worldwide, who have experimented with human observers. In general, the published works agree that the response improves with retinal illuminance, and that temporal changes with frequencies greater than 80–$90\,\mathrm{Hz}$ cannot be detected even at high luminance levels.

The method used to test the temporal response somewhat resembles the one used to test the spatial response of human observers. The main difference is that instead of working with spatial variations in frequency and contrast, these factors are now required to vary with time. Kelly [49], for example, performed experiments using an apparatus that generates a stimulus in the form of

$$L(t) = L_0(1 + m \cdot \cos(2\pi f t)), \tag{2.10}$$

where L_0 is the adaptation luminance, m is the modulation amplitude, and f is the frequency. The modulation amplitude is an example of the Michelson contrast ratio defined in (2.6), i.e.,

$$m = \frac{L_{\max} - L_{\min}}{L_{\max} + L_{\min}}, \tag{2.11}$$

where $L_{\max}$ and $L_{\min}$ are the maximum and minimum of $L(t)$, respectively.

During the experiment, while L_0 and f are kept constant, the observer is asked to report whether temporal changes can be detected for different m values. The threshold modulation amplitude, m_{th}, is defined as the minimal m that the observer requires to be able to notice temporal changes in the scene, and the ratio between L_0 and m_{th} defines the sensitivity. Experiment results are shown in Fig. 2.3(d). As before, the original data was given in Td and was converted to $\mathrm{cd/m^2}$ based on the dimensions of the artificial pupil used in the experiment. Results show that, in typical office conditions, the human eye can detect temporal changes up to frequencies of $65\,\mathrm{Hz}$. This value is used in the performance evaluation.

The temporal resolution of a digital camera is proportional to the frame rate of its image sensor, as indicated by the manufacturer. According to the Nyquist theorem, in order to reconstruct a signal, the sampling rate needs to be at least two times higher than the highest frequency it contains. Therefore, the highest temporal frequency that can be properly captured by a digital camera, and which determines its temporal resolution, equals half the frame rate of its image sensor in the best case.

2.1.5 Signal and Noise Power (SNR, SNDR, DR, and DL)

The signal and noise power of an imaging system determines four important measures: the signal-to-noise ratio (SNR), the signal-to-noise-and-distortion ratio (SNDR), the dynamic range (DR), and the dark limit (DL). Noise sources can be found in the imaging system and in the scene. For a fair comparison, all the noise is referred to the scene, i.e., the input of the imaging system.

Two types of noise affect the performance of imaging systems: temporal noise and fixed pattern noise (FPN). In this paper, the SNR considers only the temporal noise. The SNDR considers both temporal noise and FPN, where the two are assumed to be uncorrelated. In some works [52, 31], both temporal noise and FPN are included in the definition of SNR, i.e., their definition of SNR is equivalent to SNDR here. The SNDR of an imaging system cannot be greater than its SNR under the same operating conditions.

FPN exists in any array of analog or mixed-signal sensors due to inherent variability. With digital cameras, it is reduced by methods such as correlated double-sampling (CDS) and/or calibration. However, the residual FPN causes distortion. With the human eye, FPN is avoided

because the retina is sensitive to the temporal derivative of the stimulus intensity and not to the intensity itself [53]. One proof of this mechanism is that static images formed on the retina without saccadic influence fade away to the observer. Although the best way to represent the ratio between signal and noise power is through the SNDR, both SNR and SNDR are considered here because only the temporal noise is specified for some image sensors.

The dark limit is the lowest luminance level at which the SNDR begins to exceed $0\,\mathrm{dB}$. At this operating point, the signal and noise power are equal. The dynamic range is the maximal range of luminances that the imaging system can safely capture with SNDR greater than $0\,\mathrm{dB}$. Therefore, it is limited by the DL at one end. The bright limit (BL) of the DR is determined by the luminance level that causes the SNDR to drop abruptly to zero, or that damages the imaging system, or that causes other undesirable conditions, such as a sudden increase in distortion.

An intra-scene DR and an inter-scene DR can be defined for every imaging system, including the human eye. The intra-scene DR is the maximal luminance range that the imaging system can capture using fixed operating conditions. It may depend on an adaptation point. With the human eye, the pupil size should be constant and, with digital cameras, parameters such as gain and exposure time should be constant. The inter-scene DR is the maximal luminance range that the imaging system can capture with adaptation included. With the human eye, time may be allowed for adjustment to new luminance conditions and, with digital cameras, operating parameters may be likewise varied. Only the intra-scene DR is considered here for performance evaluation. Nonetheless, the inter-scene response of the human eye is explained below because it is needed to explain the intra-scene response.

Measures related to signal and noise power of the human eye may be assessed using contrast-sensitivity test patterns. The test pattern shown in Fig. 2.4(a) can be used to examine the inter-scene response of human observers [54]. The observer is first given enough time to adapt to a new background luminance level, L_0, and is then asked to indicate whether the scene looks uniform or whether the central pattern is perceived. The test pattern shown in Fig. 2.4(b) may be used to examine the intra-scene response of human observers. In this test, while L_0 and L are kept constant, ΔL is varied. The observer is asked to indicate whether the central pattern looks uniform or whether the tone difference between the two sections is perceived. Reported results are the threshold levels.

Assuming that a signal cannot be detected as long as its power is smaller than the noise power, the threshold luminance, ΔL_{th}, represents the luminance level for which the signal power and the noise power are equal. Therefore, the SNDR may be written as

$$SNDR_{\text{inter-scene}} = 20 \log \left(\frac{L_0}{\Delta L_{\mathrm{th}}} \right) \tag{2.12}$$

for the inter-scene response, and as

$$SNDR_{\text{intra-scene}} = 20 \log \left(\frac{L}{\Delta L_{\mathrm{th}}} \right) \tag{2.13}$$

for the intra-scene response.

Hecht [55] presents results of experiments done with human observers according to data reported by Koenig and Brodhun in 1889. The goal of these experiments was to find the inter-scene response of the human eye. The response was tested at luminance levels that cover the whole range in which the eye can function, from the dimmest perceptible luminance to intense levels that cause temporary blindness. The results, presented in Fig. 2.5(a), show that the inter-scene DR of the human eye extends at least $170\,\mathrm{dB}$. They also show that the peak SNDR of the human eye

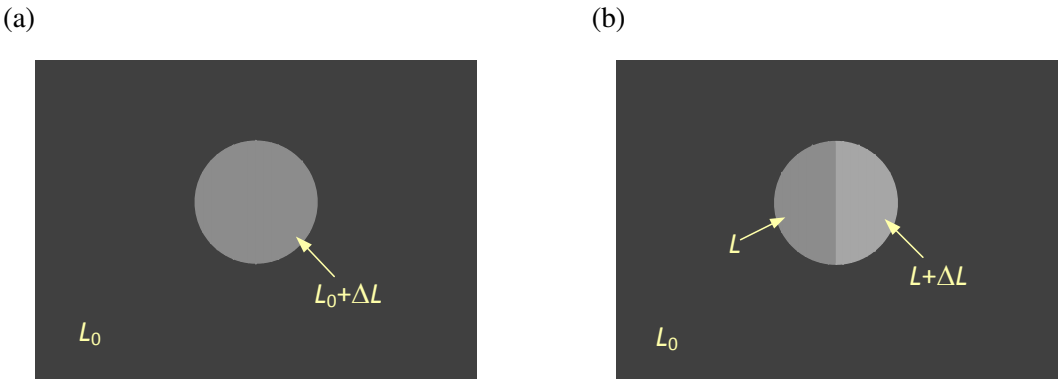


Figure 2.4: Test patterns to examine (a) the inter-scene, and (b) the intra-scene response of human observers. L_0 is the adaptation luminance. In both cases, ΔL_{th}, the minimum increment an observer requires to distinguish two luminances, is determined. Assuming that signal power equals total noise power at the threshold level, SNDR may be calculated.

equals $36\,\mathrm{dB}$, which is reached in typical office luminance. This value is used for both peak SNR and peak SNDR benchmarks in the evaluation process.

The retina includes two types of photoreceptors: cones and rods. Cones are responsible for colour vision and operate in bright light; they are mostly concentrated in the fovea. Rods are responsible for vision in dim light. The inter-scene response of the human eye is composed of three regions of operation [56]. Colour vision, or photopic vision, occurs at luminances greater than $3\,\mathrm{cd/m^2}$. Mesopic vision occurs at luminances between 3 and $.001\,\mathrm{cd/m^2}$. In this range, the response of the eye to colour gradually deteriorates. Finally, vision at luminances lower than $.001\,\mathrm{cd/m^2}$, in which only rods are operative, is called dark vision, or scotopic vision. As the human eye can detect colour until the luminance drops to $.001\,\mathrm{cd/m^2}$, this value is considered as its dark limit in the performance evaluation.

The intra-scene response was calculated according to a mathematical model developed by Barten [57], based on experimental work performed by Rogers and Carel [58]. It expresses the effect of background luminance on the CSF as a Gaussian function of the logarithm of L_0 divided by L. Although originally developed for the CSF, this model may be used to estimate the intra-scene SNDR because SNDR tests are equivalent to CSF tests at low spatial frequencies. In general, the performance of the eye is best when the background luminance is similar or somewhat lower than the object luminance. Calculation of the intra-scene response was performed at two adaptation levels. Results are shown in Fig. 2.5(a), along with the inter-scene response. The response around $100\,\mathrm{cd/m^2}$ is blocked by the BL of the human eye. The DL of the intra-scene response around $.1\,\mathrm{cd/m^2}$ corresponds to the DL of the mesopic region. The intra-scene DR at this adaptation luminance covers $126\,\mathrm{dB}$, and this value is used in the performance evaluation.

To estimate the dark limit of a digital camera, one needs to refer scene luminance, L_{sc}, which is expressed in $\mathrm{cd/m^2}$, to image plane illuminance, E_{im}, which is expressed in lux, as shown in Fig. 2.5(b). The two measures are related as follows:

$$L_{\mathrm{sc}} = \frac{E_{\mathrm{im}}}{T}\frac{1}{\pi}\left(\frac{2f_\ell}{D}\right)^2 = \frac{E_{\mathrm{im}}}{T}\frac{4f_\#^2}{\pi}, \tag{2.14}$$

where T is the lens transmission, D is the aperture diameter, and $f_\# = f_\ell/D$ is the f-number of

the lens. This formula is derived from Smith [59]. The dark limit of an image sensor, $E_{\text{im-DL}}$, may be calculated for integrating sensors if the sensitivity, the dark signal, and the dark noise are given, as explained in Section 3.3.B.

CMOS image sensors with logarithmic pixel circuits are characterized by a high DR but low SNR. Their response is somewhat similar to the inter-scene response of the human eye (see Fig. 2.5(b)). The BL of logarithmic image sensors is determined by the image plane illuminance that generates photocurrent that causes a non-logarithmic response of the pixel circuit. Above such an illuminance, residual FPN would increase substantially. With an ideal lens model, image plane illuminance (lux) may be referred to scene luminance ($\mathrm{cd/m^2}$), using (2.14), for comparison with the human eye.

Although CMOS image sensors with linear pixel circuits, as well as CCD image sensors, achieve high SNDR, they have a low DR. Their BL is determined by the image plane illuminance that causes a saturating response because the charge generated during the integration time is greater than the well capacity. At this point, the SNDR drops abruptly to zero. There are several methods to increase the DR of low DR image sensors. Those based on multiple readouts of each pixel to construct one frame are characterized by a sawtooth SNDR in the region where the bright limit of the DR is extended. Such methods include multi-mode sensors and multiple-capture methods, which can be based on either global or local control of integration time [31]. Fig. 2.5(c) compares the response of linear CMOS image sensors, with and without extension of DR, to the intra-scene response of the human eye around $100\,\mathrm{cd/m^2}$.

Although SNR and SNDR should be represented as a curve that covers the whole DR of an image sensor, a single value is usually given in datasheets. This value is either the peak SNR or the SNR at a certain operating point chosen by the manufacturer. Similarly, data for the photo-response non-uniformity (PRNU), which allows calculation of SNDR, is normally specified only for certain operating conditions. Assuming an ideal lens, the peak SNR, peak SNDR, and DR of an image sensor are equal to those of the digital camera that accommodates it.

2.1.6 Figure of Merit (FOM)

The performance evaluation method considers eight parameters: power consumption (PC), visual field (VF), spatial resolution (SR), temporal resolution (TR), signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR), dynamic range (DR), and dark limit (DL). For a digital camera, each parameter is evaluated and compared to the corresponding benchmark of the human eye. The figure of merit (FOM) is defined as the performance ratio, expressed in decibels, of the parameter that proves to be the weakest one according to such ratios. To rival the human eye, a digital camera needs to demonstrate performance that is equivalent to or better than that of the human eye at every single measure. If the FOM of a digital camera is negative, there is at least one parameter for which the performance of the human eye exceeds that of the digital camera. If the FOM is positive, the digital camera is superior to the human eye in all eight parameters.

To refer the VF, SR, and DL to the scene, the focal length, f_ℓ, and f-number, $f_\#$, of the lens need to be specified. For simplicity, the calculations are done using a thin-lens model, which means only the image sensor specifications are required. Moreover, to eliminate the effect of lens imperfections on overall performance, the lens is assumed to be ideal, i.e., with unity transmission and unity MTF.

There is a trade-off between VF and SR, which depends on the focal length of the lens. When f_ℓ is short, as with wide angle lenses, a large volume is captured by the imaging system. However, small details would not be distinguished. Therefore, short f_ℓ results in high VF but low SR. Similarly, when f_ℓ is long, as with telephoto lenses, one can clearly see small details but the

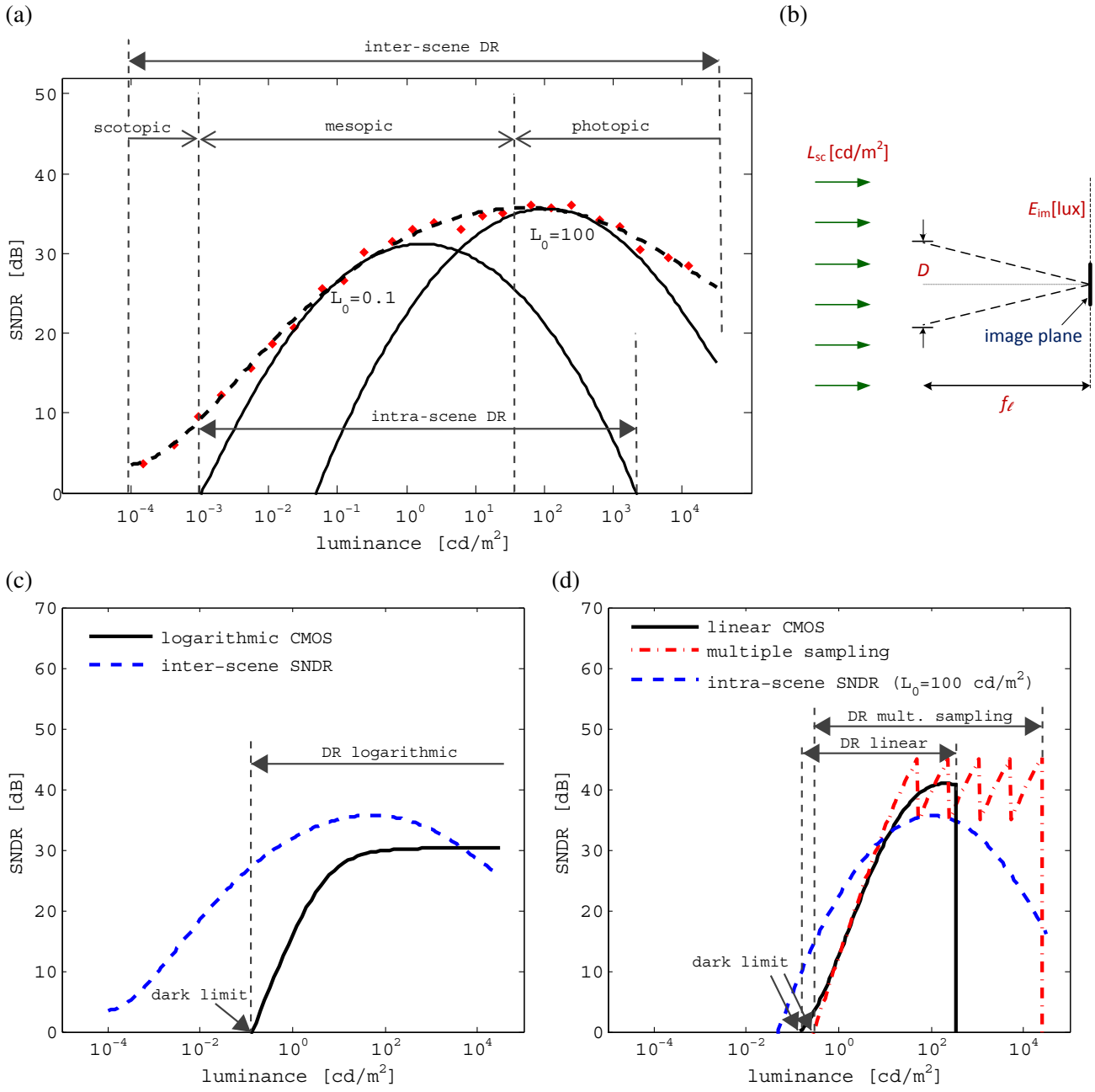


Figure 2.5: (a) The inter-scene response obtained from experiments with human observers [55]. Using a model developed by Barten [57], the intra-scene response was calculated at adaptation levels of 0.1 and $100\,\mathrm{cd/m^2}$ for a $4^\circ \times 4^\circ$ visual field. (b) A simplified model of an imaging system that is used to refer the scene luminance, L_{sc}, to the image plane illuminance, E_{im}. (c) The inter-scene response of the human eye exhibits a high DR but a low SNDR, and resembles the intra-scene response of logarithmic CMOS image sensors. (d) The intra-scene response of CCD and linear CMOS image sensors is characterized by a low DR but a high SNDR. It is compared to the intra-scene response of the human eye. When multiple sampling is used to increase the DR, the SNDR has a sawtooth pattern.

volume captured is very limited. To compare digital cameras having the same lens model, the same f_ℓ and $f_\#$ values are used with all image sensors in the performance evaluation.

The reduced eye model treats the refracting surfaces in the human eye, i.e., the cornea and the lens, as a single equivalent lens [60]. Considering refractive indices and other physical properties, one concludes that the power of the equivalent lens is 60 diopters. This gives a focal length of $17\,\mathrm{mm}$. In film cameras based on the full-frame format ($24 \times 36\,\mathrm{mm}^2$), lenses with focal lengths of 35 to $70\,\mathrm{mm}$ are considered "normal" lenses, i.e., neither wide angle nor telephoto [61]. Electronic image sensors are usually smaller than the full-frame format. Therefore, lenses with shorter focal lengths are typically used to achieve a similar VF. A focal length of $17\,\mathrm{mm}$, the equivalent focal length of the human eye, is in the range of "normal" lenses for electronic image sensors. Therefore, it does not give priority to the VF over the SR, or vice versa, and is taken as f_ℓ in the performance evaluation.

At the DL benchmark ($.001\,\mathrm{cd/m}^2$) the pupil diameter of the human eye is $6.5\,\mathrm{mm}$ [48]. This value, along with $f_\ell = 17\,\mathrm{mm}$, results in $f_\# = 2.6$. This f-number, which lies in the 2–16 range that is typical for photography, is used in the performance evaluation.

2.2 Results

The performance of 26 modern image sensors combined with an ideal lens is evaluated with respect to the human eye. The evaluation was based on data provided in commercial datasheets or academic publications that describe the image sensors. Therefore, the main criteria in the selection of image sensors for the survey was the sufficiency of details provided in the documentation. Example calculations are shown for two image sensors, and a summary of the FOM and the two most limiting factors for each sensor is presented in a table.

2.2.1 Modern Image Sensors

A list of the surveyed image sensors is presented in Table 2.2. The zeroth row of the table is dedicated to the human eye, which sets the benchmark for the performance evaluation. Data given for frame size and pixel pitch in this row refers to the number of cone photoreceptors and their diameter, respectively. Values are taken from Wyszecki and Stiles [62].

Table 2.2 includes raw data that characterizes the image sensors. Some of the details, such as pixel size and fill factor, are required for calculations related to the performance evaluation. Parameters that do not require any complicated processing for the evaluation, such as power consumption and frame rate, are not shown in the table because they are presented in a figure. Details related to control and operation of an image sensor are excluded because they are not considered in the evaluation. Raw data for calculations of signal and noise power are also excluded because there is no uniformity in the way data was measured or reported, even for image sensors of similar types. Moreover, not all parameters are relevant to all image sensors. For example, the term "full well capacity" is meaningful for CCD and linear CMOS image sensors, but not for logarithmic ones.

The image sensors included in the survey are divided into three groups. Image sensors 1–7 were fabricated in CCD technology. They include full-frame, frame-transfer, and interline-transfer CCD image sensors. Image sensors 8–16 are commercial CMOS ones, where all are based on linear integration. Image sensors 17–24 are called academic CMOS image sensors because they were described in scientific publications rather than commercial ones. Image sensors 25–26 were designed at the University of Alberta. Although their performance is summarized here, they are

Table 2.2: The 26 image sensors included in the performance evaluation: 1–7 are commercial CCD, 8–16 are commercial CMOS, 17–24 are academic (VI) CMOS image sensors, and 25–26 are UofA (VI) CMOS image sensors. The zeroth row refers to the retina and fovea of the human eye.

Image sensor	Technology (Supply voltage)	Data conversion (ADC bits)	Sensor size (Frame size)	Pixel pitch (Fill factor)
	(V)		mm^2 (Mp)	μm (%)
0. Human retina	organic	pixel level	1341.5 (5–6.5)	4.5–9
Human fovea	organic	pixel level	1.77 (0.11–0.115)	1–4
1. Kodak [63] KAF-50100, 2010	CCD full frame (15)	board level	49.1×36.8 (50)	6
2. Dalsa [64] FTF2021M, 2009	CCD full frame (24)	board level	24.5×24.4 (4.2)	12 (94)
3. Kodak [65] KAI-02050, 2008	CCD interline (15)	board level	8.8×6.6 (1.9)	5.5
4. Atmel [66] AT71200M, 2003	CCD full frame (15)	board level	35×23 (8.1)	10
5. Sony [67] ICX285AL, 2003	CCD interline (15)	board level	8.8×6.6 (1.4)	6.45
6. Texas Instruments [68] TC237B, 2001	CCD frame tr. (26)	board level	4.9×3.7 (0.3)	7.4
7. Philips [69] FXA 1012, 2000	CCD frame tr. (24)	board level	8.2×6.6 (2.1)	5.1
8. Hynix [70] YACD5B1S, 2010	CMOS linear (2.8)	chip level (10)	2.8×2.1 (1.9)	1.75
9. Samsung [71] S5K4E1GA(EVT3), 2010	CMOS linear (2.8)	column level (10)	3.7×2.7 (5.1)	1.4
10. Cypress [72] Lupa-4000, 2009	CMOS linear (3.5)	chip level (10)	24.6×24.6 (4.2)	12 (37.5)
11. Aptina Imaging [73] MT9P031, 2006	CMOS linear (2.8)	chip level (12)	5.7×4.3 (5)	2.2
12. Aptina Imaging [74] MT9M001C12STM, 2004	CMOS linear (3.3)	chip level (10)	6.7×5.3 (1.3)	5.2

Image sensor	Technology (Supply voltage)	Data conversion (ADC bits)	Sensor size (Frame size)	Pixel pitch (Fill factor)
	(V)		mm^2 (Mp)	μm (%)
13. Samsung [75] S5K3A1EA, 2004	CMOS linear (2.8)	column level (10)	4.9×3.9 (1.3)	3.8
14. STMicroelectronics [76] VS6502, 2004	CMOS linear (3.3)	chip level (10)	3.6×2.7 (0.3)	5.6
15. National Semiconductor [77] LM9638, 2002	CMOS linear (3)	chip level (10)	6.2×7.7 (1.3)	6 (49)
16. Hynix [78] HV7141D, 2001	CMOS linear (3.3)	chip level (8)	6.4×4.8 (0.5)	8 (30)
17. Lim *et al.* [79], 2009	CMOS linear (2.8)	column level (10)	1.8×1.3 (0.1)	5.6
18. Matsuo *et al.* [80], 2009	CMOS linear (3.3)	column level (14)	17.3×9.1 (8.9)	4.2
19. Dubois *et al.* [81], 2008	CMOS linear (3.3)	board level	2.2×2.2 (0.004)	35 (25)
20. Hoefflinger [82] VGAy, 2007	CMOS log. (3.3)	chip level (10)	7.7×5.0 (0.4)	10 (40)
21. Storm *et al.* [83], 2006	CMOS lin-log (3.6)	column level	2.0×1.6 (0.1)	5.6 (33)
22. Kitchen *et al.* [84], 2005	CMOS linear (3.3)	pixel level (8)	2.9×2.9 (0.004)	45 (20)
23. Mase *et al.* [85], 2005	CMOS linear (3.3)	column level (12)	6.6×4.9 (0.3)	10 (54.5)
24. Lulé *et al.* [86], 2000	VI-CMOS linear (5)	board level (12)	14.1×10.2 (0.1)	40 (100)
25. Mahmoodi [87], 2011	CMOS log. (1.8)	pixel level (11)	1.8× 2.4 (0.003)	38 (1.7)
26. Skorka (Chapter 3), 2011	VI-CMOS log. (5)	board level (16)	2.2×2.6 (0.00048)	110 (100)

discussed in Chapter 3. In each group, the image sensors are presented in chronological order, which was determined by the publication date.

The design of each academic image sensor focuses on boosting one or more performance measures. Lim *et al.* [79] and Dubois *et al.* [81] target temporal resolution. Matsuo *et al.* [80] aimed to achieve low temporal noise by using pixel circuits based on the pinned-photodiode configuration. Kitchen *et al.* [84] show a digital pixel sensor with pulse-width-modulation control that is used to improve the DR. Hoefflinger [82] and Storm *et al.* [83] use logarithmic pixel circuits to achieve high DR image sensors. Mase *et al.* [85] and Lulé *et al.* [86] also target the DR. However, they use methods that are based on multiple integration times to construct a single frame. The image sensor described by Lulé *et al.* [86] is a vertically-integrated (VI) CMOS image sensor, in which hydrogenated amorphous-silicon photodetectors were deposited on top of CMOS circuits.

2.2.2 Example Calculations

Calculation examples for the signal and noise power parameters are presented here for two image sensors: a commercial CCD sensor and an academic CMOS sensor that uses two modes of operation to construct a single frame.

Image sensor 6 (Texas Instruments, TC237B [68]) is a CCD sensor. With linear sensors, changes in the response are proportional to changes in the scene luminance. The DR of sensor 6 with CDS is $64\,\mathrm{dB}$, and its typical full-well capacity, v_{sat}, is $30\,\mathrm{k}$ electrons. Therefore, the RMS voltage of the temporal noise in the dark, $N_{\text{dark-RMS}}$, may be derived from

$$DR = 20\log\left(\frac{v_{\mathrm{sat}}}{N_{\text{dark-RMS}}}\right), \tag{2.15}$$

i.e.,

$$64 = 20\log\left(\frac{30000}{N_{\text{dark-RMS}}}\right), \tag{2.16}$$

which results in $N_{\text{dark-RMS}} = 19\,\mathrm{e}^-$ or $0.246\,\mathrm{mV}$ when using the charge conversion factor $13\,\mu\mathrm{V/e}^-$.

With image sensors that are based on integration time, i.e., CCD and linear CMOS ones, $E_{\text{im-DL}}$ may be calculated as follows:

$$S \cdot T_{\mathrm{int}} \cdot E_{\text{im-DL}} - DS \cdot T_{\mathrm{int}} = N_{\text{dark-RMS}}, \tag{2.17}$$

where S is the sensitivity, given in $\mathrm{V/(lux\,s)}$, T_{int} is the integration time, and DS is the dark signal, which is expressed in $\mathrm{V/s}$. This equation shows that if $DS \cdot T_{\mathrm{int}} \gg N_{\text{dark-RMS}}$, which can be achieved with long integration times, $E_{\text{im-DL}} \approx DS/S$. Therefore, the DL cannot be improved beyond a certain limit even when T_{int} is increased.

The sensitivity of sensor 6 with an infrared (IR) filter is $32\,\mathrm{mV/lux}$, and its dark signal is $1\,\mathrm{mV}$. Since S and DS are expressed in $\mathrm{mV/lux}$ and mV, respectively, the integration time is, actually, not required for calculation of the dark limit. The datasheet does specify that a $16.67\,\mathrm{ms}$ exposure time was used to estimate the smear. However, it is not clear whether a similar integration time was also used to find S and DS. The minimum detectable image plane illuminance is calculated by

$$(32\,\mathrm{mV/\,lux}) \cdot E_{\text{im-DL}} - 1\,\mathrm{mV} = 0.246\,\mathrm{mV}, \tag{2.18}$$

which gives $E_{\text{im-DL}} = 0.039\,\mathrm{lux}$ and results in $L_{\text{sc-DL}} = 0.336\,\mathrm{cd/m^2}$.

RMS value of the distortion, σ_v^d, and RMS value of the temporal noise, σ_v^t, are needed to calculate the SNDR. The datasheet specifies that the spurious nonuniformity under illumination

(usually called PRNU) is 15%. No data is given for the temporal noise under illumination. Therefore, the value of $N_{\text{dark-RMS}}$ is used instead, which gives:

$$\begin{aligned} \text{SNDR} &= 20\log\left(\frac{v_{\text{sat}}}{\sqrt{(\sigma_v^d)^2+(\sigma_v^t)^2}}\right) \\ &= 20\log\left(\frac{30000}{\sqrt{4500^2+19^2}}\right) \\ &= 16.5\,\text{dB}. \end{aligned} \tag{2.19}$$

Image sensor 21 (Storm *et al.* [83]) has two modes of operation: linear and logarithmic. At the beginning of each readout cycle, the photodiode capacitance is precharged, and the pixels are set to work in linear mode. Afterward, the pixels are switched to operate in logarithmic mode. Therefore, the linear mode targets dim scenes, whereas the logarithmic mode targets increased DR in bright scenes.

Storm *et al.* report that the sensitivity of the image sensor is $S = 726\text{mV}/(\text{lux}\,\text{s})$, and its dark noise is $N_{\text{dark-RMS}} = 0.95\,\text{mV}$. The pixel dark current is $0.388\,\text{fA}$. Using the specified conversion factor of $15.35\,\mu\text{V}/\text{e}^-$, the dark signal is $DS = 37.173\,\text{mV/s}$. According to the description of the sensor activation, one may conclude that at a frame rate of 26 Hz, the integration time in linear mode is $T_{\text{int}} = 50\,\mu\text{s}$. Using (2.14) and (2.17), one may find that the DL equals $226\,\text{cd}/\text{m}^2$.

However, this DL, which is very high, is inconsistent with the plot shown in Fig. 22 of Storm *et al.* [83] that presents SNR against image plane illuminance. A halogen light source is used for the measurement, and the light intensity is given in units of mW/m^2. Assuming a colour temperature of 3200 K, which is typical for this type of light source, the luminous efficacy is $28\,\text{lm}/\text{W}$ [88]. One may conclude from this plot that a digital camera with this image sensor can detect luminance levels of at least $3.4\,\text{cd}/\text{m}^2$, and this value is used for performance evaluation. However, it is not clear whether the measurement was done at a frame rate of 26 Hz. If T_{int} is large enough, so that $E_{\text{im-DL}} \approx DS/S$, the DL is $0.43\,\text{cd}/\text{m}^2$, which is comparable to that of the other image sensors included in the survey.

The plot in Fig. 22 of Storm *et al.* [83] shows that peak SNR is achieved when the sensor is activated in linear mode and equals $44.5\,\text{dB}$. This value defines the SNR for the performance evaluation. Data regarding distortion is provided only for the logarithmic mode, and it is referred to the sensor response. Therefore, the SNDR may be calculated only for logarithmic operation. The plot also shows that peak SNR in logarithmic mode equals $32.5\,\text{dB}$.

In logarithmic sensors, changes in the response are proportional to the changes in the logarithm of the scene luminance. The response y of a pixel operating in logarithmic mode to stimulus x is [89]:

$$y \approx a + b\cdot\ln x + \epsilon, \tag{2.20}$$

where a and b are temporally-constant spatially-varying parameters, and ϵ is temporally-varying noise with spatially-constant statistics.

The RMS value of the temporal noise in the scene, σ_x^t, is calculated as follows:

$$\text{SNR} = 20\log\left(\frac{x}{\sigma_x^t}\right) = 32.5\,\text{dB}. \tag{2.21}$$

Therefore, σ_x^t is 2.37% of the scene luminance.

Storm *et al.* report that, after 2-parameter calibration, the FPN is 2% of the logarithmic response, i.e., $b\cdot\ln(10)$, which equals $77\,\text{mV}$ per decade. To refer the RMS value of the distortion in

the sensor response, σ_y^d, to the RMS value of the distortion in the scene, σ_x^d, one needs to express changes in the stimulus in terms of changes in the response, which may be done with a derivative:

$$\frac{dy}{dx} = \frac{b \cdot \ln(10)}{x \cdot \ln(10)} = \frac{\sigma_y}{\sigma_x}. \tag{2.22}$$

Therefore,

$$\frac{\sigma_x^d}{x} = \frac{\sigma_y^d}{b} = 0.02 \cdot \ln(10) = 0.046, \tag{2.23}$$

or σ_x^d is 4.6% of the scene luminance.

The SNDR of sensor 21 may now be calculated as follows:

$$\begin{aligned} \mathrm{SNDR} &= 20 \log \left(\frac{x}{\sqrt{(\sigma_x^d)^2 + (\sigma_x^t)^2}} \right) \\ &= 20 \log \left(\frac{1}{\sqrt{0.046^2 + 0.0237^2}} \right) \\ &= 25.7 \, \mathrm{dB}. \end{aligned} \tag{2.24}$$

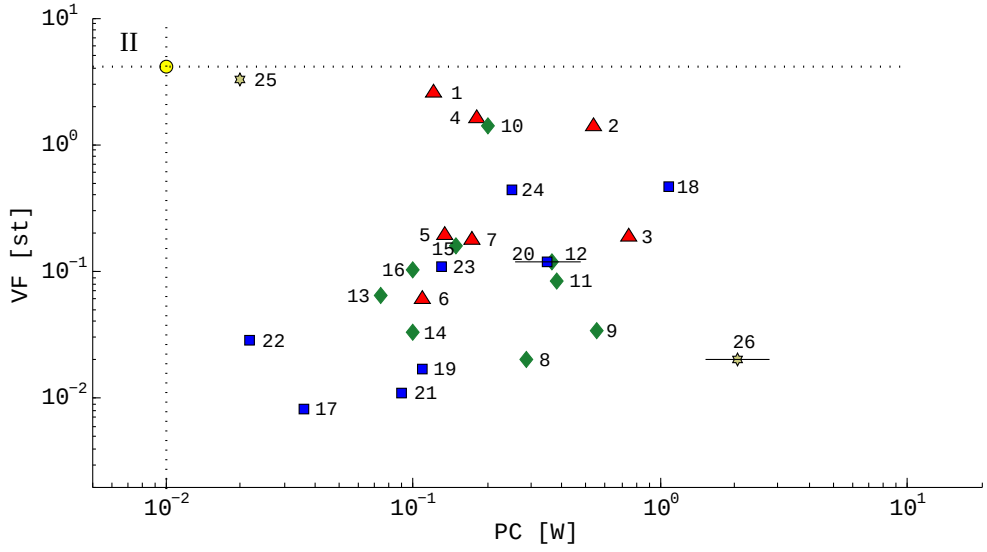
This section presented example calculations of the signal and noise power properties for two modern image sensors. These sensors differ by their technology and by their operating principles. The first example considered a CCD sensor, which is linear, and its calculation process was straightforward. The second example considered a CMOS image sensor that operates in two modes, linear and logarithmic, to construct a single frame. It required a more complicated calculation process. Therefore, this section demonstrates how the performance evaluation method of Section 2.1 can be applied to extract performance properties in a unified way that makes it possible to compare two significantly different imaging systems.

2.2.3 Performance Evaluation

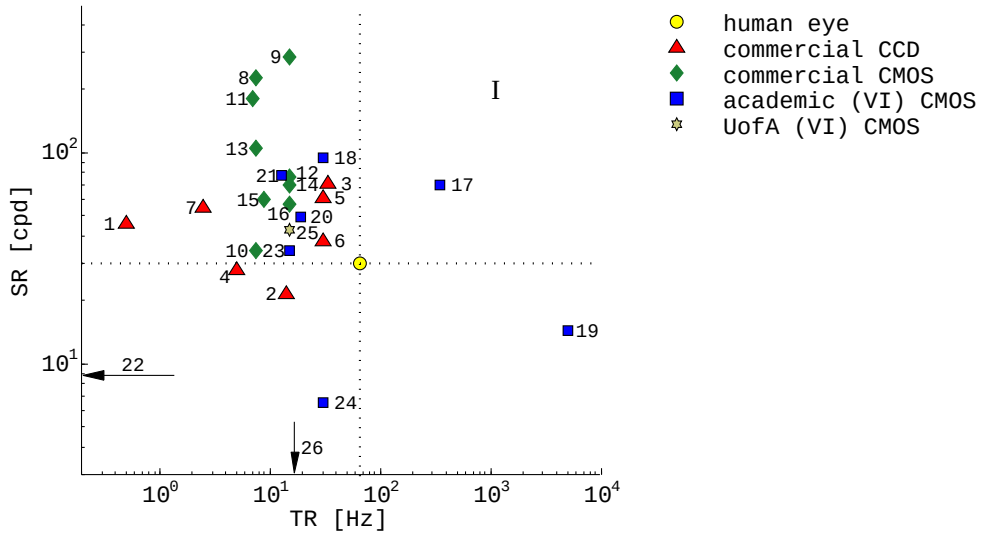
Results obtained for all the parameters considered in the performance evaluation are shown in Fig. 2.6. Image sensors located in the second quadrant of plot (a), first quadrant of the plots (b) and (c), and fourth quadrant of plot (d) perform better than the human eye in both parameters shown. In cases where information was not available for a certain parameter, the FOM was used instead of the missing parameter to determine the point in the plot, and a line is drawn parallel to the missing parameter axis. For example, image sensor 20 in Fig. 2.6(a) is missing information regarding power consumption. If the actual point is located to the right, the missing parameter is the most limiting factor (MLF) and determines the FOM, which would be lower. If the actual point is to the left, it would not change the FOM.

Fig. 2.6(a) shows that, with an ideal lens, none of the surveyed image sensors is superior to the human eye in terms of PC and VF. The VF depends on sensor dimensions. In general, one sees a deterioration in the PC with improvement in the VF. However, this does not apply to all cases because there are other factors that affect the PC, such as frame rate and circuit design. This plot also shows that commercial CCD and CMOS image sensors with similar dimensions have comparable power consumption. However, one should consider that CCD sensors operate under higher voltage levels (see Table 2.2), and also require more complicated power systems to activate the charge transfer mechanism. Although these issues are significant from a camera cost and complexity perspective, they are outside the scope of this paper.

(a)


II
VF [st]
PC [W]
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-2}
10^{-1}
10^{0}
10^{1}
25
1
4
10
2
24
18
5
15
7
3
20
12
16
23
11
13
6
22
14
9
26
8
19
21
17

(b)


I
SR [cpd]
TR [Hz]
human eye
commercial CCD
commercial CMOS
academic (VI) CMOS
UofA (VI) CMOS
10^{2}
10^{1}
10^{0}
10^{1}
10^{2}
10^{3}
10^{4}
9
8
11
13
18
21
12
14
3
17
7
15
5
1
16
20
25
10
23
6
4
2
19
22
24
26

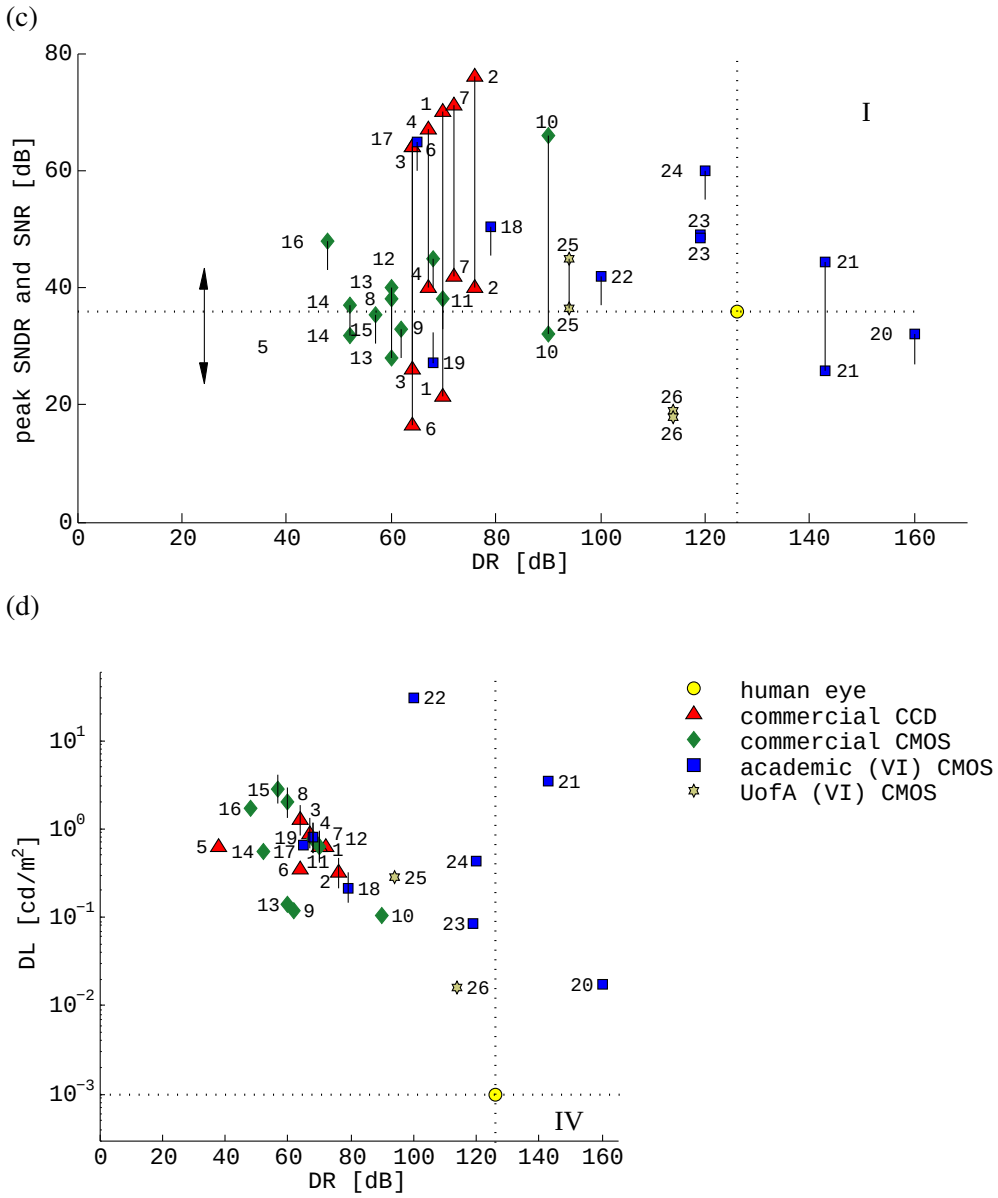


Figure 2.6: Performance evaluation results: (a) visual field versus power consumption, (b) spatial resolution versus temporal resolution, (c) peak SNDR and SNR versus dynamic range, and (d) dark limit versus dynamic range. The quadrant in which performance is superior to the human eye is indicated by the quadrant label.

The PC might be misleading for image sensors with off-chip ADCs. ADCs are an integral part of any digital camera, and the actual PC of a system that includes such an image sensor and an external ADC is higher. Likewise, the very low VF of several academic CMOS image sensors might underestimate their potential. These image sensors were designed to prove a concept and, therefore, only a small array was fabricated to save resources.

The TR is shown in Fig. 2.6(b) along with the SR. While the TR obtained for CCD image sensors ranges from 0.5 to $34\,\mathrm{Hz}$, the TR of commercial CMOS image sensors lies in a much narrower band that ranges from 7 to $15\,\mathrm{Hz}$. The academic CMOS image sensors have, in general, higher TR than commercial ones, and sensors 17 and 19 perform even better than the human eye at this measure. All this may indicate that commercial CMOS image sensors are targeting video applications rather than still imaging, and that high video rate imaging is one of the current trends in CMOS image sensors. Sensor 22 is represented by an arrow because no data was specified for its frame rate, and using its FOM resulted in a point located out of the range of the plot.

The SR depends on pixel pitch and fill factor. In cases where the fill factor was not mentioned (see Table 2.2), reasonable values were assumed for the calculation. Full frame and frame transfer CCDs can have a fill factor as high as 100%, while interline transfer CCDs can have a fill factor as low as 20% [90]. To estimate the SR, fill factors of 80% and 40% were assumed for the frame transfer and interline transfer CCDs, respecitively, in Table 2.2. A fill factor of 40% was also assumed for the CMOS image sensors missing this data. This value is close to the average fill factor of the other CMOS image sensors in Table 2.2, excluding the vertically-integrated one.

The pixel pitch of sensor 24 is relatively large because of a bond pad for vertical integration and a complicated circuit that are placed in the pixel to increase the DR. This manifests in a low SR. In general, Fig. 2.6(b) shows that the SR that can be achieved with modern electronic image sensors is at least comparable to that of the human eye, even when a normal focal-length lens, rather than a long focal-length one, is used.

Fig. 2.6(c) shows the peak SNDR and SNR of the surveyed image sensors versus their DR. If the specifications were given with and without an IR-cut filter, the performance with the filter is considered. With some of the linear CMOS image sensors, e.g., sensor 16, the magnitude of the temporal noise was specified only for dark conditions. This value was used to calculate the peak SNR, which resulted in this measure being equal to the sensor's DR. However, the actual peak SNR would be lower. Image sensors for which both SNR and SNDR data was provided are represented by a line with two end points. The top one refers to the SNR, and the bottom to the SNDR. Cases where only the SNR could be calculated, such as sensor 18, are represented by a downward line with one end point, and cases where only the SNDR could be calculated, such as sensor 19, are represented by an upward line with one end point. Sensor 5 is represented by a double arrow because its datasheet does not provide any information related to noise, and use of its FOM resulted in a negative value.

Commercial CCD image sensors can have better SNR than CMOS ones. However, the DR of both is comparable and rarely exceeds $70\,\mathrm{dB}$. Sensor 10 has an operating mode that allows an increased DR by multiple exposure times. Five of the academic CMOS image sensors have a DR of at least $100\,\mathrm{dB}$, among which sensors 20 and 21 demonstrate a DR that is superior to the benchmark defined by the human eye. This indicates that a current trend in electronic imaging is improved DR. Image sensor 24 achieves both high DR and high SNR. However, this comes at the expense of large pixels (see Fig. 2.6(b)).

Fig. 2.6(d) presents the DL versus the DR. The DL could not be extracted for image sensors 1, 3, 8, 11, 12, 15, 18, and 19. The FOM is used instead with a line parallel to the DL axis. The documentation of sensor 20 specifies $E_{\text{im-DL}}$ in lux. For sensor 22, $E_{\text{im-DL}}$ was determined from

a plot (Fig.11(a) of Kitchen *et al.* [84]) for the longest integration time shown. The figure shows that none of the image sensors has a DL that is lower than the benchmark set by the human eye. The DL of commercial CCD image sensors is somewhat better than that of CMOS ones.

Table 2.3 summarizes the performance evaluation results for each image sensor. The number of entries is out of the eight parameters considered for the evaluation. Also included are the first MLF, which determines the FOM, and the second MLF. The table shows that with each one of the surveyed image sensors, at least one parameter is significantly weak, even with the benefit of an ideal lens. The DR proved to be the most limiting factor in most cases, and it is followed by the DL and the VF. Currently, no digital camera rivals the human eye.

2.3 Discussion

The previous section demonstrated not only the room for improvement but also the large variability in electronic image sensors. They differ by properties such as fabrication technology, readout mechanism, architecture, and pixel design. Past trends in the area of electronic imaging may suggest which of the present trends will lead to a significant improvement in performance and, therefore, have the potential to become dominant in the future.

The first electronic image sensors were based on MOS devices. Various configurations fabricated in NMOS, PMOS, and bipolar technologies were demonstrated in the 1960s [91]. However, their image quality was poor, mainly due to a high FPN. The invention of the CCD by Willard Boyle and George Smith in the late 1960s, for which they were granted the Nobel Prize in Physics in 2009, enabled the first generation of electronic image sensors. CCD technology created the image sensor market because it showed a significant improvement in image quality when compared to MOS technology. CCD image sensors were almost free of FPN, and achieved a higher spatial resolution because CCD technology allowed fabrication of smaller pixel dimensions than MOS technology. For three decades, CCD was the dominant technology in the area of electronic image sensors.

The second generation of electronic image sensors emerged in the 1990s when various groups around the world, and mainly the NASA Jet Propulsion Laboratory [92], decided to put more effort into the development and improvement of CMOS active pixel sensors (APS). The advantages of these image sensors over CCD devices included increased chip-level functionality, lower cost, and the ability to operate with a simple power system. These advantages made CMOS image sensors suitable for mobile applications, where there was a demand for compact systems that are also low power. Other properties, which prevented CMOS image sensors from competing with CCD in the early days, improved with developments in the CMOS industry and, particularly, in the area of CMOS image sensors.

As they still do not rival the human eye, further work needs to be done to improve modern digital cameras. Using a design approach that is inspired by biological systems too literally is not the best way to accomplish comparable functionality. A better approach is to develop methods that use available technologies for implementation of systems that can compete with natural ones. Nonetheless, one should examine how structural differences between the human retina and electronic image sensors lead to a functional gap between the two. For example, the retina has a multi-layered structure, whereas electronic image sensors are usually fabricated in single-tier technologies.

A schematic cross-section of the human retina is shown in Fig. 2.7(a). The retinal pigment epithelium delivers nutrients to the retina and disposes of the metabolic waste. It also prevents reflections of light rays that are not absorbed by photoreceptors [62]. Rod and cone cells absorb light,

Table 2.3: Summary of results for the 26 image sensors in Table 2.2. "Entries" refers to how many of the eight parameters in the performance evaluation could be determined. The FOM is the performance gap of the most limiting factor (MLF) of a digital camera, composed of the corresponding image sensor and an ideal lens, with respect to the human eye.

Sensor	Entries	FOM [dB]	1st MLF	2nd MLF
1.	7	−56	DR	TR
2.	8	−50	DR	DL
3.	7	−62	DR	PC
4.	8	−59	DR	DL
5.	6	−88	DR	DL
6.	8	−62	DR	DL
7.	8	−56	DL	DR
8.	6	−66	DR	VF
9.	7	−64	DR	DL
10.	8	−40	DL	DR
11.	6	−56	DR	VF
12.	6	−58	DR	PC
13.	8	−66	DR	DL
14.	8	−74	DR	DL
15.	6	−69	DR	VF
16.	7	−78	DR	DL
17.	7	−61	DR	DL
18.	6	−47	DR	PC
19.	6	−58	DR	VF
20.	6	−31	VF	DL
21.	8	−71	DL	VF
22.	6	−90	DL	VF
23.	8	−39	DL	VF
24.	7	−53	DL	PC
25.	8	−49	DL	VF
26.	7	−46	VF	DL

and convert it into a neural response in the form of impulses. The human retina contains about 115–120 million rods and 5–6.5 million cones, which are not distributed uniformly. Impulses travel vertically through the bipolar cells and finally reach the ganglion cells. Each ganglion cell transmits the impulses through its nerve fiber (an axon) to the brain.

Both horizontal and amacrine cells form lateral connections between bipolar cells, the former at the receptor-bipolar synapse (a "node" where cells are connected electrically and chemically), and the latter at the bipolar-ganglion synapse. Horizontal cells have a role in retinal processing, which possibly involves chromatic interaction between photoreceptors. Amacrine cells play a role in modulation of signals that are transmitted to the ganglion cells [93].

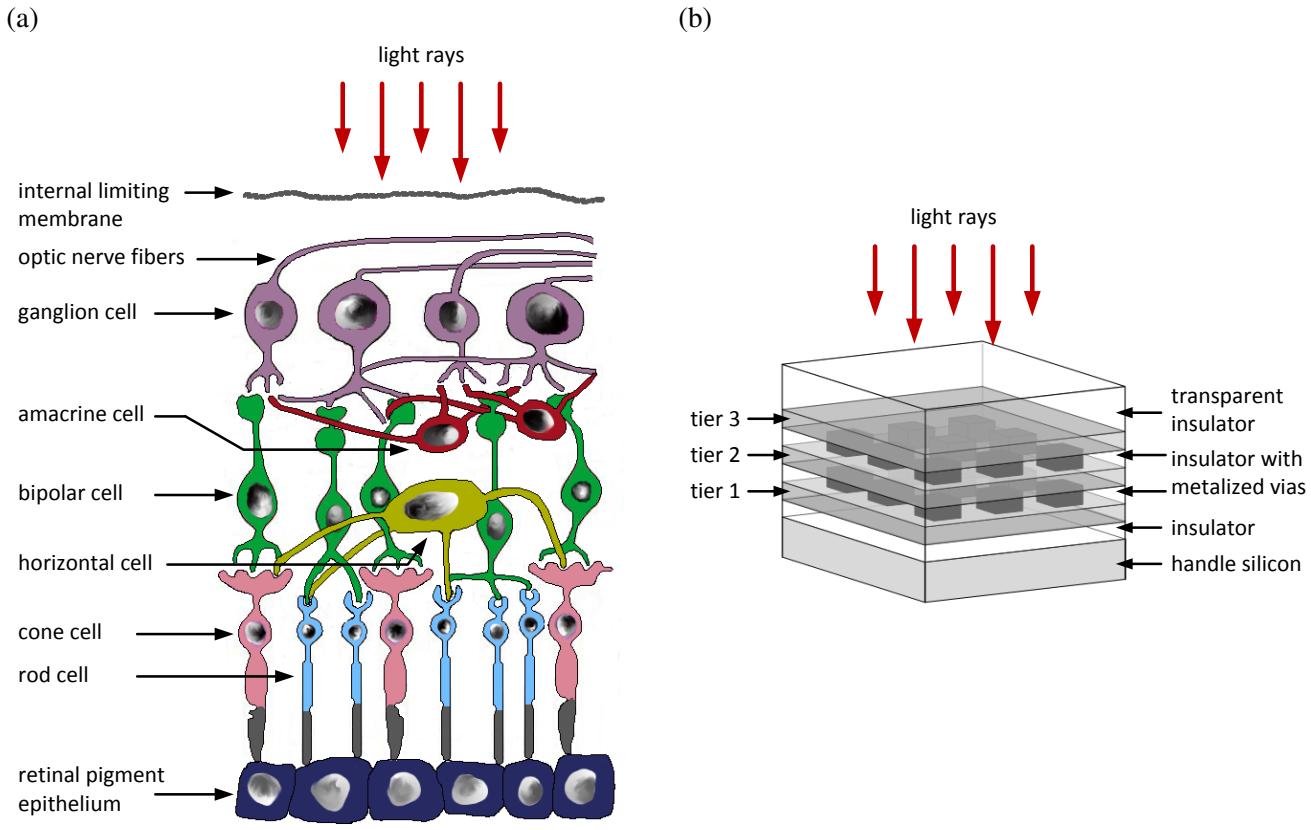


Figure 2.7: (a) The human retina has a vertically-integrated structure. Photoreceptors absorb light and generate electric pulses, which are transmitted to bipolar and ganglion cells, and then to optic nerve fibers. The retina also has horizontal and amacrine cells that form lateral connections. (b) A vertically-integrated CMOS image sensor, made by through-substrate-via (TSV) technology, has multiple tiers. For example, photodetectors, analog circuits, and digital circuits may be optimized independently with three tiers.

Conversion of light into impulses by the retinal photoreceptors is equivalent to data conversion that is done at pixel level. In image sensors, digitization of the analog signals generated by the photodetectors can be done at four different levels: board level, chip level, column level, and pixel level. The level of data conversion is mentioned in Table 2.2 for each of the image sensors. In CCD image sensors, where integration of electronics with photodetectors is, at large, impossible, the data conversion must be done at board level. In almost all CMOS image sensors in the table,

the ADCs are integrated with the sensor array. The benefits of this integration include reduction in system size, power consumption, and noise. Noise reduction is essential for improvement of performance in parameters related to signal and noise power.

The longer the path an analog signal needs to travel to reach an ADC, the greater the noise power it accumulates. The travel distance is minimal when the data conversion is done at pixel level. Digital pixel sensors have been demonstrated [94, 95, 96]. However, ADCs are composed of a large number of transistors. In planar technologies, the pixel area is shared between photodetector and electronics. Working with deep submicron CMOS processes, which allows increased device density, is undesirable for image sensors due to poor optical performance [97]. Therefore, implementation of more circuits in the pixel area results in large pixel dimensions, which degrades the SR. See, for example, sensor 24 in Section 3.3.

Fabrication of ICs in 3D structures, where two or more dies are stacked to form a multiple-tier device, allows more pixel-level circuitry while reasonable pixel dimensions are maintained. Moreover, each tier can be fabricated in a process that best suits the type of devices it contains. Therefore, digital circuits can be fabricated in a high-density nanoscale CMOS process, while photodetectors are prepared in a large scale processes. Analog circuits can be either fabricated in the same process as the digital ones or in an intermediate scale process. Furthermore, vertical integration allows more degrees of freedom in the design of the photodetectors. In some fabrication methods, it is feasible to use materials that are other than crystalline silicon.

The DL, which proved to be an important limiting factor in modern digital cameras can be improved by photodetector optimization. Image sensors fabricated by planar technologies that include avalanche photodiodes for photodetection in dim light have been presented [98]. However, this architecture requires a large pixel area and, therefore, suffers from low SR.

The horizontal connections between the retinal cells allow mechanisms of feedback and control. A processed image rather than "raw data" is sent from the retina to the brain. This is equivalent to DSP that is used for image enhancement in camera systems. Image sensors that include analog circuits for implementation of image enhancement features have been demonstrated in planar technologies [99]. However, also in this case, the additional circuitry came at the expense of an enlarged pixel area and reduced SR. In general, the DSP is done at board level in modern digital cameras.

Among the various technologies for vertical integration of IC devices [4], through-substrate via (TSV) technologies [100] are the only ones that allow fabrication of multiple-tier ICs with vertical integration at pixel level. In TSV technologies, via holes are etched through the substrate, and then filled with metal to form electrical connections between tiers. The process also requires alignment and attachment at either die or wafer level. A VI-CMOS image sensor has been demonstrated in stacked-SOI technology [11], which is one of the TSV methods. Fig. 2.7(b) shows a schematic of a multiple-tier image sensor fabricated by this technology.

There are issues that need to be overcome before technologies for vertical stacking of ICs can be widely used. For example, alignment of small features at die or wafer level is a mechanical challenge. Moreover, heat dissipation is a major problem in such structures because of the increase in volumetric device density. Lastly, to make these devices affordable for consumers, fabrication costs need to drop. Nonetheless, the interest in fabrication of 3D ICs has increased in recent years because these devices have widespread advantages [3].

2.4 Conclusion

The human factor has been widely considered for evaluation of digital displays. However, it is rarely used as a reference point in the design and evaluation of digital cameras and electronic image sensors, although these are fundamental systems at the heart of every process of digital recording of scenes. This work introduces a method that evaluates performance of digital cameras with respect to the human eye. It is motivated by a wide range of applications in which digital cameras are expected to observe scenes the same way they are perceived by the human eye and, therefore, to rival the human eye.

After considering various parameters that can be used to characterize an imaging system, eight are taken for the evaluation. The process is concluded with a figure of merit, which represents the performance gap for the parameter that appears to be the weakest when compared to the human eye. Assessment methods for the eight parameters are covered for the human eye and for digital cameras. Experiments performed with human observers and cadavers are reviewed to determine and justify benchmark values for the human eye. Information given in datasheets or other detailed publications is needed to assess the performance of digital cameras.

The performance evaluation method has been applied to 26 modern CCD and CMOS image sensors, both commercial and academic ones, where an ideal lens is assumed to complete the electronic imaging system. In the majority of cases the dynamic range proved to be the most limiting factor with respect to the human visual system, and this parameter was followed by the dark limit. Overall, the evaluation concludes that modern digital cameras do not rival the human eye. The functional gap ranges from 31 to $90\,\mathrm{dB}$, or from 1.6 to 4.5 orders of magnitude.

Past trends in the area of electronic imaging were initially concerned with image quality of low dynamic range scenes. This was succeeded by image sensors more suitable for mobile devices. Image sensor capabilities can be improved by photodetector optimization and increased pixel-level data processing. But implementations in planar technologies result in degradation of the spatial resolution. Although more effort needs to be put into the development of reliable and economical fabrication methods, vertical stacking of pixel components is promising for boosting the performance of image sensors and digital cameras.

Chapter 3

Design and Fabrication

The work covered in this chapter describes the first process flow for VI-CMOS image sensors made by flip-chip bonding through CMC Microsystems. It discusses general design guidelines for such image sensors, and focuses on the VI-CMOS prototype that was prepared as a part of the research work presented in this thesis. The chapter also refers to the electronic imaging system, i.e., the digital camera, that was developed to test the prototype, and presents results obtained form prototype characterization, which shows competitive dark limit and dynamic range.

Fig. 3.1 shows a VI-CMOS image sensor, made by flip-chip bonding, next to a CMOS image sensor. Both were designed at the University of Alberta (UofA) and fabricated via the Canadian Microelectronics Corporation (CMC). The CMOS sensor was fabricated in a $0.35\,\mu\mathrm{m}$ TSMC process. Each pixel contains a photodetector integrated laterally with CMOS transistors. The VI-CMOS sensor comprises a CMOS die (bottom) and a photodetector die (top) that were assembled by flip-chip bonding. Whereas the CMOS die was fabricated in a standard $0.8\,\mu\mathrm{m}$ DALSA process, the photodetector die was fabricated in a custom process via Micralyne Inc and the UofA Nanofab. Each pixel contains a photodetector integrated vertically with CMOS transistors.

The chapter is organized as follows. Section 3.1 discusses optional fabrication methods for VI-CMOS image sensors, and focuses on general principles in the design of those made by flip-chip bonding. It includes a detailed review on various choices for the photodetector die. Section 3.2 presents, as a specific example, the design and fabrication of the VI-CMOS image sensor prototype shown in Fig. 3.1(b). Finally, Section 3.3 presents results of experimental work.

3.1 Principles of Design and Fabrication

VI-CMOS image sensors may be designed for different fabrication methods, as shown in Fig. 3.2. With thinned substrate technology [101], after CMOS circuits are formed on one side, photodetectors are formed on the other side of a silicon substrate that is also thinned. With TFA technology, thin films that define photodetectors are deposited and patterned directly on a silicon substrate with CMOS circuits, i.e., an ASIC. In these two technologies, semiconductor devices are vertically integrated on one die, enabling monolithic VI-CMOS image sensors.

With flip-chip technology, VI-CMOS image sensors are composed of two dies: a silicon die with CMOS circuits and a transparent die with photodetectors. After separate fabrication, the two are precisely aligned and attached face-to-face using metallic interconnects. TSV technologies may be used to vertically integrate two or more dies. Front-to-back electrical connections between dies are possible by etching holes through substrates and metalizing them. Burns *et al.* [11] demonstrated a TSV image sensor with three tiers using stacked silicon-on-insulator (SOI) tech-

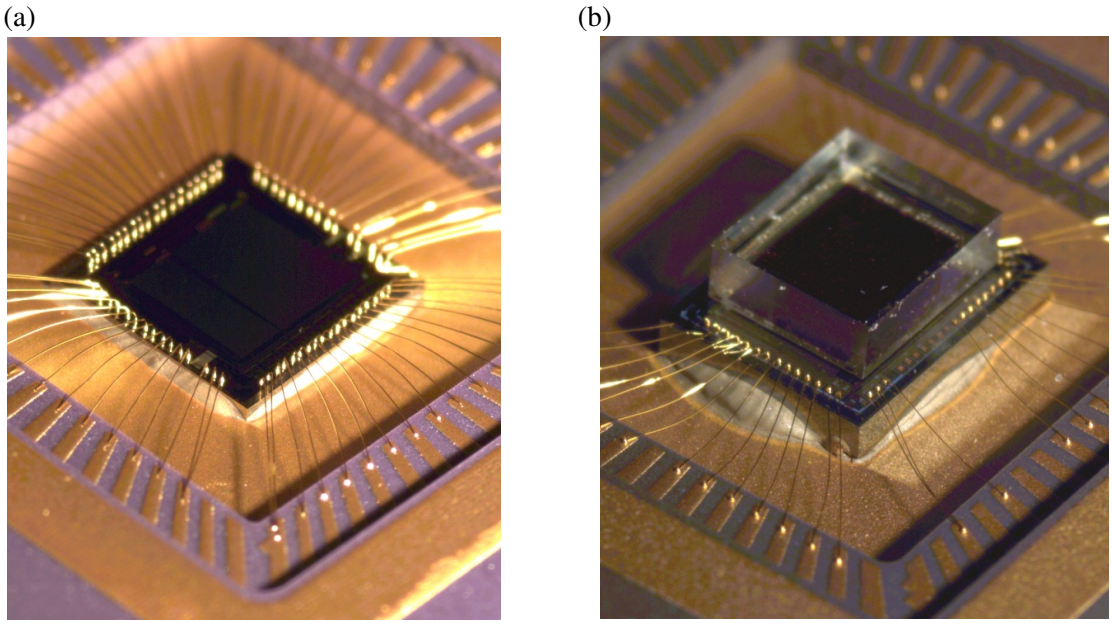


Figure 3.1: (a) CMOS and (b) VI-CMOS image sensors designed at the University of Alberta and fabricated via CMC Microsystems. With the CMOS sensor, each pixel includes a photodetector integrated laterally with CMOS transistors. With the VI-CMOS sensor, a CMOS die (bottom), which includes an active pixel sensor array, is vertically integrated with a photodetector die (top), which includes a photodetector array fabricated on a glass substrate.

nology. Top, middle, and bottom tiers were dedicated to photodetectors, analog circuits, and digital circuits, respectively. While all tiers were fabricated using SOI substrates, each tier had its own process scale.

Our first efforts toward a prototype concerned TFA technology. However, TFA involves extensive post-processing of finished CMOS substrates, including surface planarization and film deposition. Process development requires whole CMOS wafers but we could obtain only tens of CMOS dies at a relatively low cost using a multi-project wafer service through CMC. Furthermore, because the CMOS dies were fabricated in a commercial process, the exact materials and dimensions used were trade secrets, which made it more difficult to develop compatible post-processing.

In 2007, we switched to flip-chip technology because it was the only way to make a VI-CMOS image sensor with the support of CMC. At the time, TSV technologies were still in development – there were no TSV services available through CMC. Flip-chip technology required the design and fabrication of a CMOS die (Section 3.1.1) and a photodetector die (Section 3.1.2), which are then bonded (Section 3.1.3) to assemble a VI-CMOS image sensor.

3.1.1 CMOS Die

The CMOS die in Fig. 3.3(a) was designed for a standard CMOS process. Design of a CMOS die for a VI-CMOS image sensor is similar to the design of a CMOS image sensor, but there are some important differences.

Typical CMOS image sensors are composed of: active pixels, which amplify photodetector signals; row and column address decoders, which select pixel signals for readout; column and out-

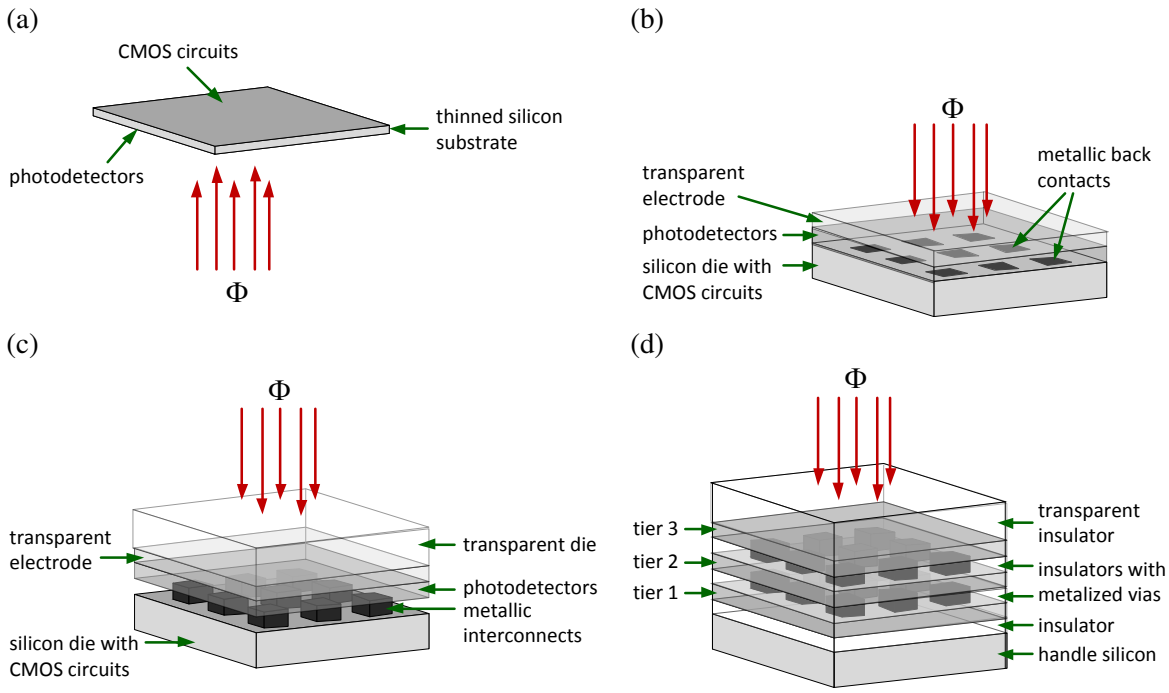


Figure 3.2: VI-CMOS image sensors fabricated by (a) thinned substrate, (b) thin-film-on-ASIC (TFA), (c) flip-chip, and (d) through-substrate via (TSV) technologies.

put buffers, which route selected signals to output buses; and analog-to-digital converters (ADC), which transform the output signals. In addition to the photodetectors, these readout circuits define how photogenerated charge carriers are interpreted. In general, the digital response is a linear or logarithmic function of the light stimulus. Usually, a few ADCs are included for all pixels. However, designs that include one or two ADCs per column, or column-level ADCs, are increasingly common. Further details on CMOS image sensor design may be found in the literature [5, 52, 102].

As with a CMOS image sensor, the floor plan of a CMOS die designed for a VI-CMOS image sensor also requires an active pixel array, address decoders, buffers, and one or more ADCs. However, unlike CMOS image sensors, there is no photodetector in the pixel layout. Instead, each pixel has a bond pad to form an electrical contact with a vertically-integrated photodetector after flip-chip bonding. This makes a bond-pad array of photodetector back-contacts. Surrounding bond pads mate to a transparent conductive oxide (TCO), which defines a front contact on the photodetectors. Like typical CMOS chips, a VI-CMOS image sensor also requires peripheral bond pads for wire bonding to a package that can be soldered onto a PCB.

For visible-band image sensors, the motivation for VI-CMOS over CMOS technology is to facilitate one ADC per pixel. With conventional CMOS image sensors, analog signals must travel outside the pixel array for conversion to digital signals. While traveling, they accumulate noise. Because digital signals are far more immune to noise than analog ones, the signal-to-noise ratio is expected to improve with pixel-level ADCs. However, as ADCs require complex circuits, building them in a CMOS technology suitable for visible-band imaging implies a relatively low spatial resolution. Further details on pixel-level ADCs may be found in the literature [103, 94].

In CMOS image sensors, borders of each photodetector are defined in the pixel layout. In VI-CMOS image sensors, however, there are good reasons to avoid physical borders between adjacent

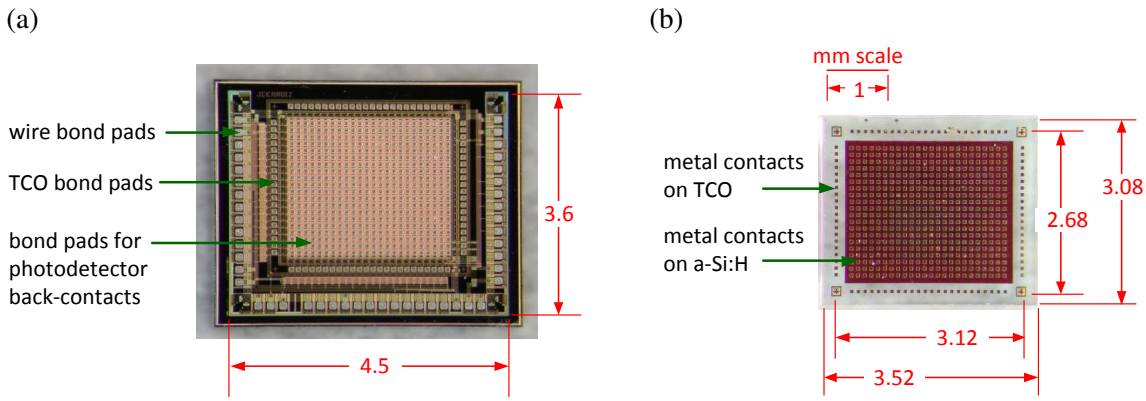


Figure 3.3: The VI-CMOS prototype in Fig. 3.1(b) is composed of a CMOS die and a photodetector die. (a) The central area of the CMOS die contains a circuit array for readout purposes, which mates to back contacts on the photodetectors. Surrounding bond pads mate to a transparent conductive oxide (TCO), which defines a front contact on the photodetectors. Peripheral bond pads are required to wire the image sensor to a package. (b) The central area of the photodetector die has an array of bond pads on a light-sensitive semiconductor. Surrounding bond pads are on the TCO.

photodetectors. The manufacturing cost of the photodetector die may be reduced by avoiding the lithography steps required to pattern the borders. Moreover, edges of patterned devices introduce defect states and other imperfections that degrade performance, for example, by increasing the dark currents of photodetectors.

Without physical borders between adjacent photodetectors, lateral currents may flow due to drift and diffusion. This would cause photogenerated charge carriers to enter the "wrong" pixels of the CMOS die, a condition known as "crosstalk". The crosstalk may be made negligible if a vertical electric field of sufficient uniformity and magnitude is applied on all photodetectors by the CMOS circuits. Schneider *et al.* [104] used a feedback active pixel to introduce this approach in a VI-CMOS image sensor made by TFA technology. Chapter 4 elaborates on the design of such pixels, especially in terms of stability and compensation.

3.1.2 Photodetector Die

The photodetector die in Fig. 3.3(b) was fabricated in a custom process. Its central area has an array of bond pads on a light-sensitive semiconductor; the surrounding bond pads are on the TCO. Unlike with the CMOS die, the challenge with designing this die has to do with its cross-section, and not its floor plan. One must specify the material layers, their ordering, and their thicknesses. Usually, the electric field in the photodetectors is oriented parallel to the incident light flux, i.e., parallel to Φ in Fig. 3.2(c). Otherwise, each pixel requires two bond pads.

Handle Substrate

The handle substrate of the photodetector die must be transparent for the electromagnetic band targeted by the application. For better imaging performance, a large percentage of photons must reach the light-sensitive devices. There is always some loss of photons due to reflections at interfaces formed in the path of the light. However, loss of photons due to absorption in the handle

Table 3.1: Coefficients of thermal expansion (CTEs) of silicon and substrates that are transparent in the visible band [105].

Substrate material	CTE [$10^{-6}\,\mathrm{K}^{-1}$]		
	@ 200 K	@ 293 K	@ 500 K
Silicon	1.5	2.6	3.5
Glass, borosilicate	2.7	2.8	3.3
Glass, fused-silica	0.1	0.5	0.6
Glass, soda-lime	-	7.5	-
Quartz, single crystal, $\parallel$ c-axis	5.2	6.8	11.4
Quartz, single crystal, $\perp$ c-axis	10.3	12.2	19.5
Sapphire, single crystal, $\parallel$ c-axis	4.1	4.8	7.9
Sapphire, single crystal, $\perp$ c-axis	6.6	7.4	8.3

substrate should be minimized.

Handle substrates of the photodetector and CMOS dies should have similar coefficients of thermal expansion (CTEs). Large CTE differences cause mechanical stress when the temperature of the assembled device varies from the temperature of assembly. Temperature changes are also expected when the device is powered up or down. Mechanical stress results in distortion of features, which may affect functionality, especially with nanoscale CMOS. Table 3.1 gives three CTEs of silicon, which is the handle substrate of standard CMOS dies, and of substrates suitable for visible-band applications. Borosilicate glass, which is sold commercially under brand names such as Pyrex and Borofloat, has CTEs closest to those of silicon.

When selecting a handle substrate, properties of other substrate materials in the photodetector die should be considered. Amorphous materials may, in general, be deposited on any handle substrate. However, crystalline materials require handle substrates with matching lattice constants. Moreover, the handle substrate must withstand all process steps required to make the photodetector die. For example, polysilicon films, which are suitable for photodetection, may be deposited using low-pressure chemical vapour deposition (LPCVD) at over $600^{\circ}\mathrm{C}$. If the films are doped, they require annealing at 900–$1000^{\circ}\mathrm{C}$ for dopant activation. Borosilicate glass, although transparent and with CTEs close to those of silicon, cannot be used with polysilicon photodetectors because it cannot withstand these temperatures. Fused silica, quartz, or sapphire should be used in this case.

Transparent Electrode

The first layer on the handle substrate must be a transparent conductor. It forms the front contact of all photodetectors, and is an essential electrode to realize a vertical electric field. In some cases, it is possible to use a heavily-doped section of the handle substrate or the light-sensitive devices (subsequent layers) for this purpose. In other cases, one deposits a film based on thin metals, transparent conductive oxides (TCOs), transparent conductive polymers (TCPs), or carbon nanotubes (CNTs). These materials are described below.

Table 3.2: Optoelectronic properties of widely used transparent-conductive oxides.

Material	Band Gap [eV]	Conductivity $[\Omega^{-1}\mathrm{cm}^{-1}]$	Carrier Concentration $[\mathrm{cm}^{-3}]$	Mobility $[\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}]$
ZnO [111]	3.3	10^3	$2 \cdot 10^{20}$	20
AZO [112, 113]	3.8	2100–3300	$6.5 \cdot 10^{20}$	30
SnO_2 [114]	3.95	10–50	$3.5 \cdot 10^{19}$	5
In_2O_3 [115, 116]	2.6–3.6	50–5000	10^{19}–10^{21}	1–30
ITO [117, 118, 119]	3.5–4.3	2500–7000	10^{20}–10^{21}	20–30

Thin metals: Metals are very good conductors but are opaque to visible light. Metal films, however, transmit some visible light if they are very thin. Aluminum (Al), silver (Ag), and gold (Au), are attractive choices because they have a relatively high transmittance in the visible band. These metals must be less than $20\,\mathrm{nm}$ thick to have at least 10% transmission [106, 107]. Unfortunately, thin films are much less conductive than thick ones, and their conductivity is much more sensitive to thickness variation. Hence, it may be difficult to achieve a satisfactory combination of transparency, conductivity, and uniformity with thin metals [108].

Transparent conductive oxides: TCOs are semiconductors, usually polycrystalline or amorphous, that have high optical transparency and high electrical conductivity, properties normally considered mutually exclusive [109]. To be used as a TCO, a semiconductor needs a high band gap ($\gtrsim 3.1\,\mathrm{eV}$), a high concentration of free carriers ($\gtrsim 10^{19}\,\mathrm{cm}^{-3}$) – i.e., it needs to be a degenerated semiconductor [110] – and a good mobility ($\gtrsim 1\,\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$). Popular TCOs are indium oxide (In_2O_3), tin oxide (SnO_2), and zinc oxide (ZnO), which are all n-type semiconductors. Table 3.2 presents their optoelectronic properties. Although TCOs are more conductive than typical semiconductors, they are much less conductive than metals.

Often, TCOs are doped with impurities. Widely used examples are tin-doped indium oxide (In_2O_3:Sn or ITO) and aluminum-doped zinc oxide (ZnO:Al or AZO). ITO has been used for many years in applications where transparent electrodes were needed. However, because indium and tin are expensive metals, while zinc is cheap and non-toxic, AZO films have been getting more attention in recent years [120].

Transparent conductive polymers: Organic electronic devices are based on polymers such as those listed in Table 3.3. Mass production of organic devices is expected to be cheaper than that of inorganic devices. Moreover, polymers are ideal for realizing flexible devices. Currently, ITO is widely used as a transparent electrode in organic optoelectronic devices [121]. However, ITO is brittle, which makes it unsuitable for flexible devices. PEDOT:PSS is a flexible TCP that has been touted as a suitable replacement [122].

At present, the conductivity of TCPs is about an order of magnitude lower than that of ITO [123], and TCPs are less transparent to visible light than ITO [122]. Moreover, when a device includes polymers, the maximum temperature that it can withstand during fabrication

Table 3.3: Abbreviations and full names of polymers commonly used in organic electronic devices.

Abbreviation	Full Name
CuPc	copper(II) phthalocyanine
$PC_{60}BM$	(6,6)-phenyl-C61-butyric acid methyl ester
PDDTT	poly(5,7-bis(4-decanyl-2-thienyl)-thieno (3,4-b)diathiazole-thiophene-2,5)
PEDOT	poly(3,4-ethylenedioxythiophene)
PSS	poly(styrenesulfonate)
P3HT	poly(3-hexylthiophene)

and operation is more limited. Therefore, the advantages of working with TCPs are relevant mainly when the whole device is organic.

Carbon nanotubes: Researchers have shown recently that thin films of CNTs, mainly single-walled CNTs (SWCNTs), may be used as transparent electrodes [124, 125]. SWCNTs are attractive because they can be deposited on almost any substrate [126], and because their mechanical properties make them suitable for use in flexible devices. Whereas indium prices are rising due to the increasing depletion of indium sources worldwide, carbon remains an abundant element. Hence, SWCNTs have a promising future.

Similar to the difficulties faced with polymers, the transparency and conductivity of SWCNTs are inferior to those of ITO. Sangeeth *et al.* [122] compared experimentally the performance of ITO, PEDOT:PSS, and SWCNTs. When SWCNT films have a transparency comparable to that of ITO films, for light at $550\,\mathrm{nm}$ (i.e., the middle of the visible band), their conductivity is almost two orders of magnitude lower. Nonetheless, researchers are working on methods to improve the conductivity of CNT films [126, 127].

Light-Sensitive Devices

Electronic photodetectors are mainly constructed from a light-sensitive semiconductor, which must have high absorption coefficients for the targeted wavelengths. Hence, for visible-band imaging, the semiconductor band gap must be smaller than the energy of red photons. In addition, absorbed photons must change the electrical properties of the semiconductor sufficiently so that the change is detectable by a CMOS circuit.

With VI-CMOS image sensors, there may be more degrees of freedom in photodetector design than with CMOS image sensors. For example, the depth of lateral photodetectors in a CMOS image sensor is largely fixed by the doping profiles of the CMOS process. However, the depth of vertical photodetectors in a flip-chip image sensor is largely variable. On the photodetector die, the thickness of the light-sensitive semiconductor may be chosen to optimize a performance measure, such as the ratio between photocurrent and dark current, as discussed in Chapter 5.

In addition to layer thicknesses, a photodetector design must specify the device type and the layer materials. In general, light-sensitive devices may be categorized as photoconductors, photodiodes, or phototransistors [128]. Traditionally, photodetector layers were based on inorganic

semiconductors, either crystalline or amorphous ones, but organic semiconductors may also be used. Further details are given below.

A list of optional device structures for photodetectors is given below. Devices are categorized according to the number of junctions they include.

Photoconductors: A photoconductor (or photoresistor) consists of a uniformly-doped semiconductor sandwiched between ohmic contacts. Device conductivity increases with increasing illumination. With an applied electric field, photogenerated electrons and holes are collected by opposite contacts. For good performance, the charge carriers should have long lifetimes and high mobilities. Otherwise, most of the excess electron-hole pairs recombine on their way to the contacts, and do not contribute to the photocurrent. The semiconductor should have a low noise current in the dark, with respect to photocurrent, for the device to have an acceptable response in dim illumination.

Photodiodes: Photodiodes are commonly used in CMOS image sensors. They incorporate either p-n junctions between p-doped and n-doped semiconductors or Schottky junctions between semiconductors and metals. Under reverse bias, photodiodes usually have lower dark currents than comparable photoconductors because of a depletion layer. An electric field accelerates photogenerated charge carriers toward the contacts, where they contribute to photocurrent. To increase the thickness of the depletion layer, an intrinsic layer (undoped or lightly doped) may be inserted between the p and n regions. This makes a p-i-n photodiode.

Avalanche photodiodes permit the detection of single photons. These devices realize high gains by accelerating photogenerated charge carriers, using a high electric field, so as to generate secondary electron-hole pairs in the depletion layer. Lately, there has been an increased interest in avalanche photodiodes [129], which have applications also in lens-less imaging systems, e.g., in microfluidic devices (lab on a chip).

Phototransistors: The term phototransistor is normally used for two back-to-back p-n junctions, i.e., light-sensitive devices that resemble bipolar transistors. When two Schottky junctions are used, the device is often called a metal-semiconductor-metal (MSM) photodetector. In either case, one junction is reverse biased while the other is forward biased when a voltage is applied. The floating-base configuration is often used.

A list of optional material families of light-sensitive semiconductors is given below. Material families are categorized as crystalline and amorphous inorganic semiconductors or as organic semiconductors.

Crystalline semiconductors: Crystalline silicon is the material used to make photodetectors in standard CMOS and CCD image sensors. Other crystalline semiconductors that are suitable for photodetection in the visible band are alloys like gallium arsenide [130] (GaAs) and indium gallium nitride [131] (InGaN). Common deposition methods for these materials are molecular beam epitaxy (MBE) and metal-organic chemical vapour deposition (MOCVD). Mercury cadmium telluride (HgCdTe or MCT) has long been used for infrared photodetection. The band gap of this alloy may be varied by changing the element proportions [132]. The main drawback with crystalline materials is that they can be deposited only on substrates with similar lattice constants. Moreover, the deposition needs to be done at relatively high temperatures.

Amorphous semiconductors: Hydrogenated amorphous silicon (a-Si:H) is an amorphous semiconductor commonly used for photodetection in the visible band. It is a relatively cheap material, has a high absorption coefficient for visible light, and can be deposited on various substrates. Popular deposition methods for a-Si:H optoelectronic devices are sputtering and plasma-enhanced chemical vapour deposition (PECVD). The deposition is done at relatively low temperatures, i.e., at 200–250°C. Amorphous selenium (a-Se) is another amorphous semiconductor that is used for photodetection. Its properties make it ideal for detecting X-rays [133]. However, a-Se photodetectors for the visible band have also been demonstrated [134].

Organic semiconductors: Although organic semiconductors have been studied for 60 years, their use in optoelectronic devices, e.g., LCD displays, is quite recent. The breakthrough was the discovery that some organic semiconductors are photoconductive under visible light [135]. Initially, organic semiconductors were unstable and had a low carrier mobility. However, their properties have improved in recent years thanks to extensive research. They are attractive for use in optoelectronic devices, as an alternative to inorganic semiconductors, because of their low cost, low deposition temperature, and flexibility. Organic photodetectors for the visible band have been demonstrated using materials such as pentacene [136], a blend of PDDTT and $PC_{60}BM$ [137], and a structure composed of P3HT and CuPc thin films [138]. Deposition methods for organic semiconductors include thermal evaporation, organic molecular beam deposition (OMBD), and spin coating. In some cases, deposition may be done at or just above room temperature.

3.1.3 Flip-Chip Bonding

CMOS dies and photodetector dies need to undergo a few more process steps before they can be flip-chip bonded. The process performed on the CMOS dies includes etching of the native oxide layer from the aluminum bond pads and deposition of a metal stack, called top surface metallurgy (TSM), that has a good wettability to the solder material used in the flip-chip bonding. Photodetector dies are processed to form two sets of bond pads, which are also metal stacks, called under bump metallization (UBM). These bond pads form back contacts on the photodetectors, and also connect to the transparent electrode, which makes the front contact of the photodetectors. The UBM must have a good adhesion to non-metallic materials, such as semiconductors and conductive oxides, as well as good wettability to the solder material. Solder bumps are then formed on the UBM, as illustrated in Fig. 3.4. Having the solder bumps on the smaller die facilitates the assembly process. Further details are given in Appendix A.

3.2 Design and Fabrication of a Prototype

The previous section focused on general principles in the design and fabrication of a VI-CMOS image sensor. This section focuses on the design and fabrication of a specific prototype.

CMOS dies were fabricated in a standard CMOS process. Therefore, the challenging part with these dies was the circuit design, mainly the pixel layout, and not the fabrication. Photodetector dies, however, were fabricated in a custom process. In terms of manufacturability and performance, these dies are not the best that could be designed for the visible band (400–700 nm), which was targeted for simplicity. However, they are the best that could be made with the available materials and equipment. A new process was developed at the UofA Nanofab to realize the photodetector dies. Process development requires that all materials used, e.g., etching gases and

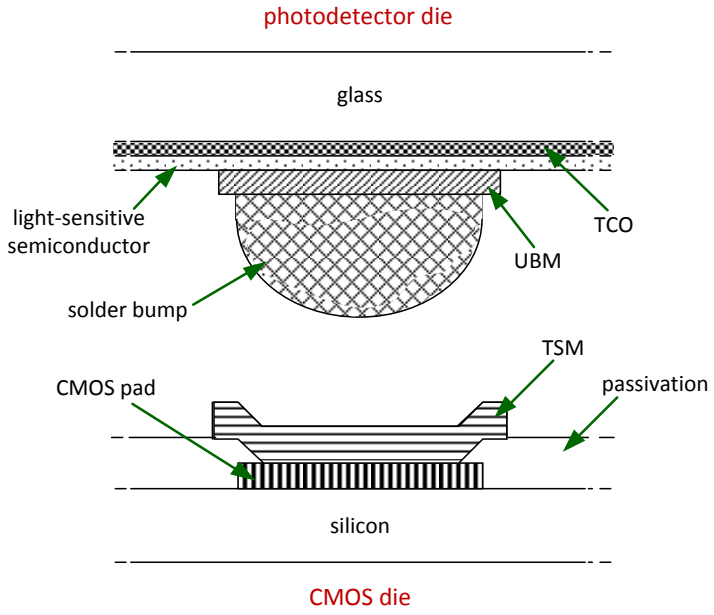


Figure 3.4: Pre-processing required for flip-chip bonding (not drawn to scale). TSM is deposited on the CMOS die, and UBM is deposited on the photodetector die. Solder bumps, tens of microns thick, are fabricated on the UBM.

solutions, and all conditions reached, e.g., maximum temperature, work without any undesirable side effects.

3.2.1 CMOS Die

The CMOS die was designed for a $0.8\,\mu\mathrm{m}$ DALSA process, which has three metal layers. In this process, CMOS devices are fabricated in a large N well. Therefore, NMOS transistors require a P well, whereas PMOS transistors are fabricated in the substrate. The supply voltage V_{dd} is $5\,\mathrm{V}$.

A floor plan of the design is shown in Fig. 3.5(a). It includes a 20×24 array of active pixels (AP), row and column address decoders (AD), buffers (BF), extra circuits (EC) for test purposes, and alignment marks (AM). ADCs were not included for simplicity. Schematic and layout designs were done with Cadence. The schematic was verified using DC, AC, and transient simulations. The layout was verified using design rule check (DRC) and layout versus schematic (LVS) tests. Dies were fabricated through CMC.

Layout of the active pixel is shown in Fig. 3.5(b). Each pixel has a bond pad (BP) for integration with a vertical photodetector and a lateral photodiode (LP). It also includes a feedback logarithmic-response (FL) circuit, a standard logarithmic-response (SL) circuit, and a switch (SW) that configures the output. Although electrostatic discharge protection is recommended for all bond pads, such circuits were only included in wire bond pads. Interior bond pads are inaccessible after flip-chip bonding.

Pixels are $110 \times 110\,\mu\mathrm{m}^2$, which is quite large for visible-band applications. When the project was at the design stage, CMC could guarantee flip-chip bonding only for bond pads of at least $55\,\mu\mathrm{m}$ pitch and $110\,\mu\mathrm{m}$ spacing from centre to centre. However, pixel dimension of $10 \times 10\,\mu\mathrm{m}^2$, i.e., small enough for imaging in the visible band, have been demonstrated elsewhere with VI-

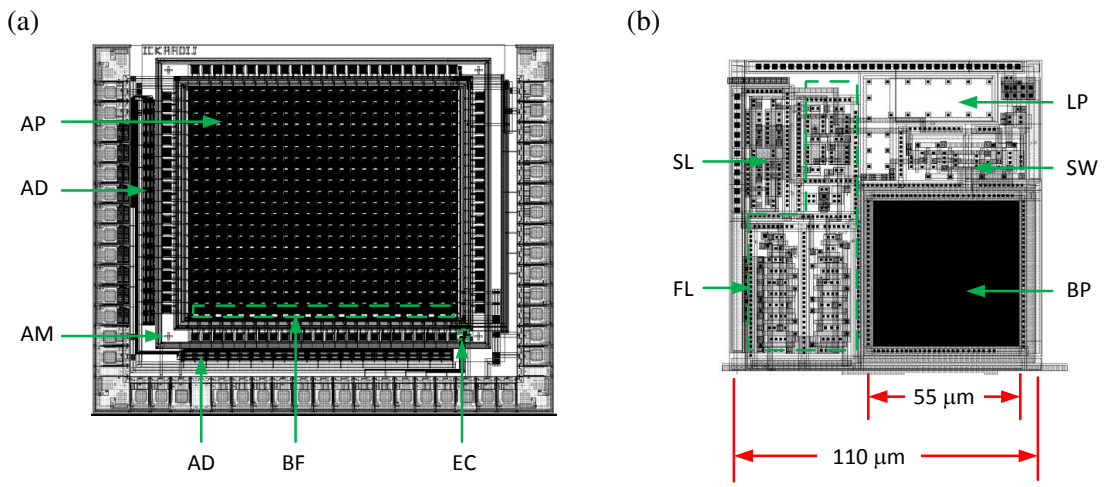


Figure 3.5: (a) Floor plan of the CMOS die. As with a CMOS image sensor, the CMOS die of a VI-CMOS image sensor requires active pixels (AP), row and column address decoders (AD), and buffers (BF). Extra circuits (EC) and alignment marks (AM) are added for test purposes and flip-chip bonding, respectively. (b) Layout of an active pixel. It includes a bond pad (BP) for a vertical photodetector and a feedback logarithmic-response circuit (FL), as well as a lateral photodiode (LP) and a standard logarithmic-response circuit (SL). A switch (SW) configures the output.

CMOS image sensors made by flip-chip bonding [139].

In general, design rules of CMOS processes do not allow placement of devices underneath bond pads, and require bond pads to connect to all metal layers. However, researchers are working to change this. For example, Ker *et al.* [140] designed and tested NMOS transistors underneath wire bond pads. Their bond pads used all metal layers except the lowest, which was used for the transistors. Even after wire bonding, there was little difference between the characteristics of these transistors and standard ones, located far from the bond pads.

Fig. 3.6 shows principle schematics of the different circuit blocks in the active pixel. Substrates of all NMOS transistors are connected to ground, and substrates of all PMOS transistors are connected to the supply voltage (V_{dd}). Fig. 3.6(a) presents the switch. It has its two input lines, which are always connected to the bond pad and to the lateral CMOS photodiode. Fig. 3.6(b) shows the standard logarithmic-response circuit, and Fig. 3.6(c) shows the feedback logarithmic-response circuit. Each of them is connected to two of four switch outputs. However, only one output of each pair is active at a time, as explained below. Width-to-length ratios are given for all transistors, except for those in the operational amplifier, which is detailed in Chapter 4.

A logarithmic response to light stimulus was chosen over a linear one because it can capture a higher dynamic range. Because the light-sensitive semiconductor in the photodetector die is unpatterned, active pixels in the CMOS die employ feedback circuits to reduce crosstalk, as explained in Chapter 4. The FL circuit maintains a constant voltage at the photodetector back contacts and, therefore, uses current as its input signal. A lateral photodiode and a standard logarithmic-response circuit are included in each pixel so that the functionality of the CMOS die could be tested independently of flip-chip bonding and feedback.

The switch in each pixel is configured externally through the control line S. In one configuration, the lateral photodiode is connected to the input node of the standard logarithmic circuit, $V_{\text{in SL}}$, and the vertical photodetector is connected to the input node of the feedback logarithmic

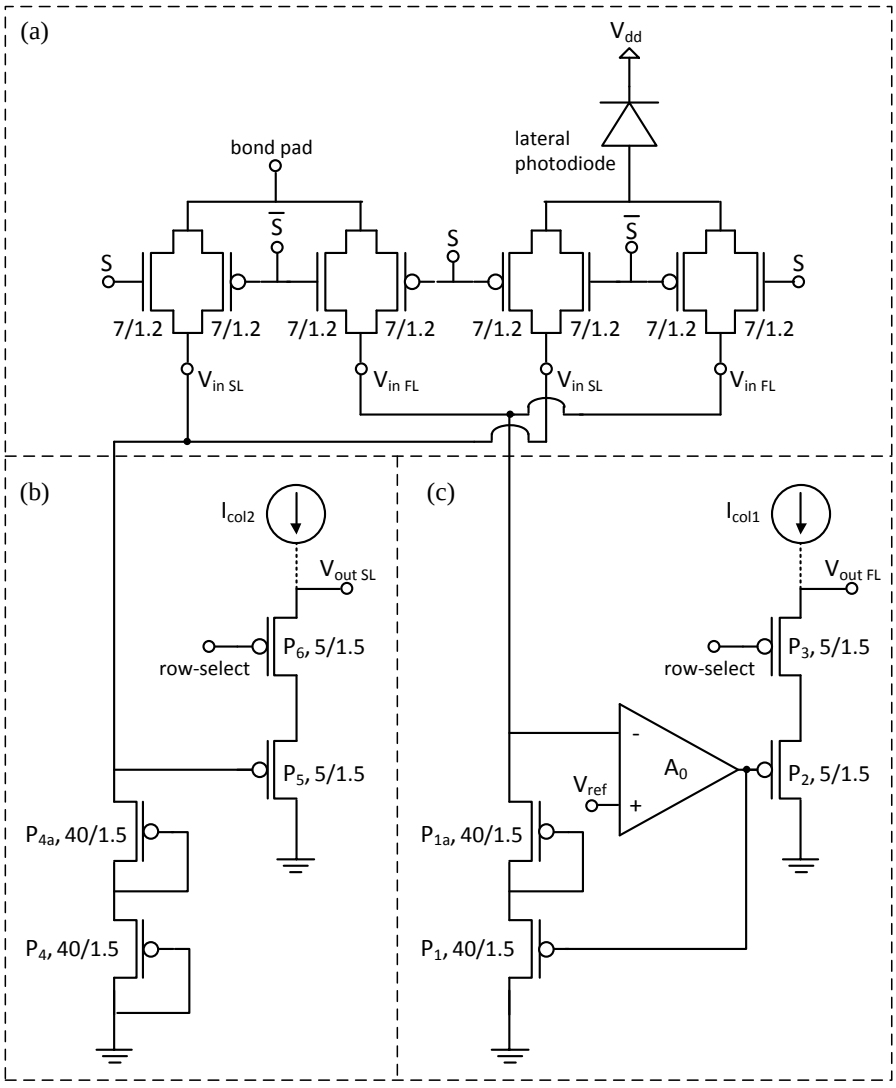


Figure 3.6: Principal schematics of the active pixel: (a) the switch (SW); (b) the standard logarithmic-response (SL) circuit; and (c) the feedback logarithmic-response (FL) circuit. The control signal S configures transmission gates connected to a bond pad (BP), which is used for integration with a vertical photodetector, and to a lateral photodiode (LP).

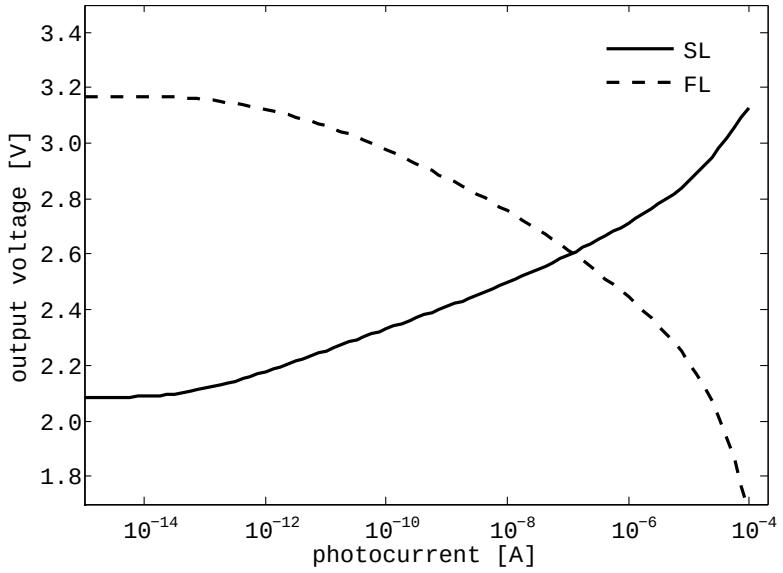


Figure 3.7: A DC simulation of the output voltage of the SL and FL circuits versus photocurrent.

circuit, $V_{\text{in FL}}$. Connections are swapped in the second configuration. The switch acts as a multiplexer to analog signals; it is composed of transmission gates, which support rail-to-rail operation. When a transmission gate is activated, the gate terminals of the NMOS and PMOS transistors are connected to $\mathrm{V_{dd}}$ and ground, respectively. Therefore, they are always in the linear region.

Results of a DC simulation that tested the output voltage of the SL and FL circuits as a function of photocurrent are shown in Fig. 3.7. The output voltage of the SL circuit increases with photocurrent because the voltage across the photodetector decreases as the incident illuminance increases. The output voltage of the FL circuit decreases with photocurrent because the feedback mechanism increases V_{gs} of $\mathrm{P_1}$ to allow conduction of a higher drain current through this transistor. The presence of the switch does not affect the DC response of these two circuits for current levels smaller than $10\,\mu\mathrm{A}$, i.e., the switch affects the response only for current levels that are well above the maximal expected photocurrent. AC simulation was performed only on the FL circuit, as it includes a feedback loop. Chapter 4 presents the result and elaborates on it.

Readout of the FL and SL circuits is activated when the *row-select* signal is logic low. In this case, transistors $\mathrm{P_3}$ and $\mathrm{P_6}$ are conducting, and column bias currents, I_{col1} and I_{col2}, flow through the source-follower transistors, $\mathrm{P_2}$ and $\mathrm{P_5}$, respectively. Each pixel has two output lines, where one is for the FL circuit, $V_{\text{out FL}}$, and the other is for the SL circuit, $V_{\text{out SL}}$.

3.2.2 Photodetector Die

The design of the photodetector die was mainly determined by the light-sensitive semiconductor that we could use. There was no equipment for GaAs deposition in the Nanofab. Moreover, GaAs films must be deposited on GaAs substrates, which are opaque to visible light. Some options, such as HgCdTe, were ruled out because of their toxicity. Other options, such as organic films, did not have good enough performance at the time. After a careful review, the only semiconductor we could work with productively was a-Si:H.

In general, a-Si:H can be deposited either by sputtering or by PECVD. The latter method tends to yield higher quality films than the former method. Sputtering must be done at 200–$250^{\circ}\mathrm{C}$ as

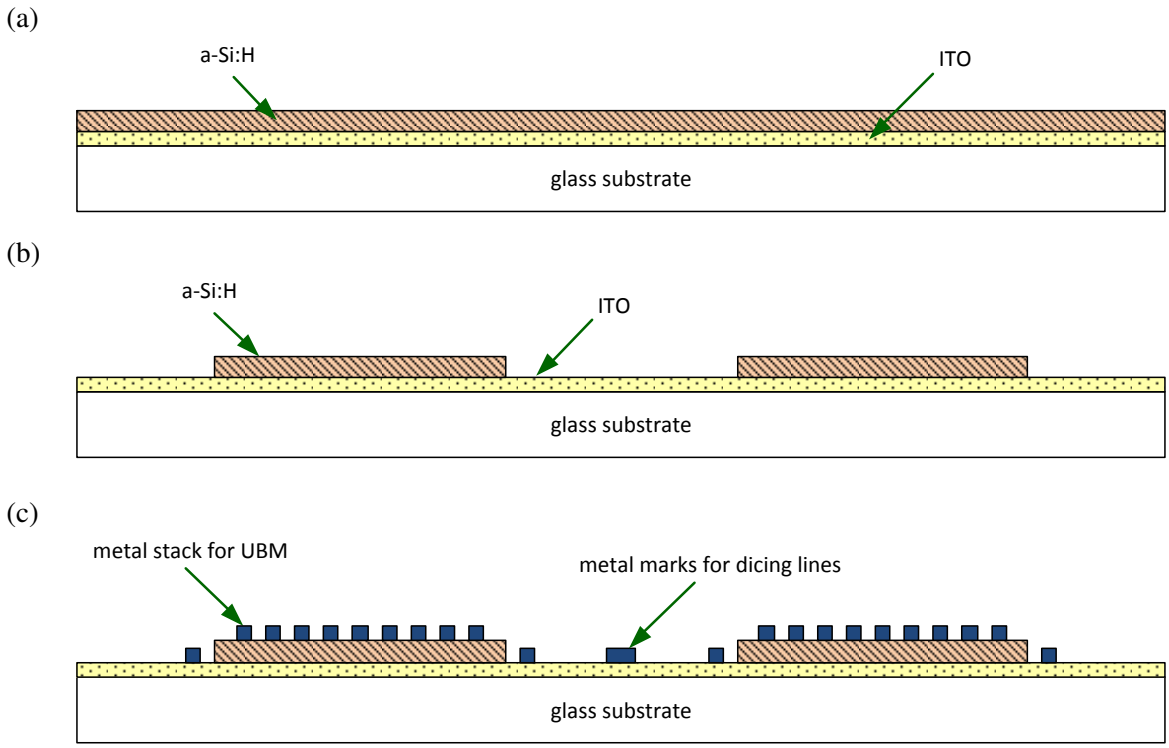


Figure 3.8: Fabrication process of the designed photodetector die. (a) ITO is sputter deposited and then annealed. An a-Si:H film is deposited by PECVD on the ITO. (b) The first lithography step uses reactive ion etching to expose ITO at the periphery of a-Si:H rectangles. (c) An array of bond pads is formed on the a-Si:H rectangles, with further bond pads on the surrounding ITO. A metal grid is deposited with the bond pads to mark dicing lines on the coated glass substrate.

a reactive process using hydrogen. Although the Nanofab has sputtering machines, none of them had a hydrogen supply. Fortunately, Micralyne Inc, an Edmonton company, agreed to deposit a-Si:H films with their PECVD machine. Micralyne's process, however, did not support dopant gases. Therefore, our devices had to be based on intrinsic films, and so p-n or p-i-n photodiodes could not be implemented. Consequently, we designed an MSM device, in which an intrinsic a-Si:H layer is sandwiched between two conductive layers.

Fig. 3.8 illustrates the fabrication process of the photodetectors. ITO and a-Si:H were deposited on the handle substrate by sputtering and PECVD, respectively. The purpose of the first lithography step was to selectively etch the a-Si:H layer. One needs to expose the ITO layer because, in the VI-CMOS image sensor, an electric potential must be applied to it. The a-Si:H was dry etched using the Plasma Lab μEtch machine in the Nanofab. The chamber was pumped down prior to the process. Etching was done in an atmosphere created by $40\,\mathrm{sccm}$ flow of carbon tetrafluoride (CF_4) and $10\,\mathrm{sccm}$ flow of oxygen (O_2). The CF_4/O_2 plasma also serves as surface treatment to improve performance of the ITO film [141]. An RF power of $100\,\mathrm{W}$ was applied, and the chamber pressure was $63\,\mathrm{mTorr}$. A chrome mask was used for the dry etch because earlier trials with a photoresist mask showed that the etchant gases consumed the photoresist at a higher rate than the a-Si:H.

The final photodetector design was a Cr/a-Si:H/ITO stack on glass. Chrome was used as the back contact because it has good adhesion to non-metal substrates, including a-Si:H. To get a

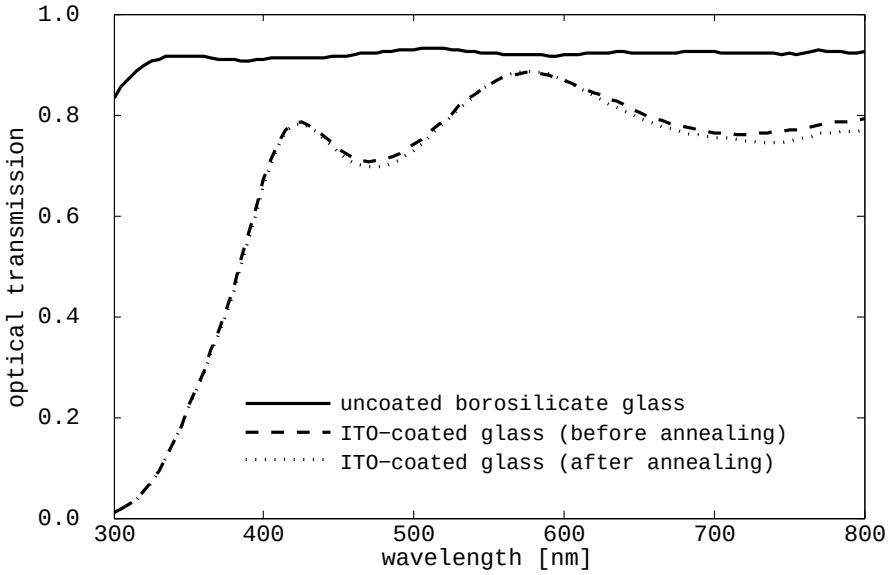


Figure 3.9: Optical transmission of a borosilicate glass substrate before and after ITO deposition. Transmission of the coated glass was measured before and after the ITO was annealed.

higher photocurrent to dark current ratio with this MSM device, the CMOS die connects the ITO electrode to a higher voltage than the chrome electrode due to the relative size of potential barriers at the two Schottky junctions [142].

Handle Substrate

We used borosilicate glass (Borofloat) as the handle substrate for the photodetectors. Although thinner substrates were available, we used $1\,\mathrm{mm}$ thick ones because they were in stock at the Nanofab. Substrates were cleaned using a Piranha solution (sulfuric acid and hydrogen peroxide). Using the Woollam VASE ellipsometer in the Nanofab, we measured the optical transmission of a naked substrate. Results are presented in Fig. 3.9. They show that 90% of visible light is transmitted.

Transparent Electrode

Equipment and materials available in the Nanofab meant we could use either a thin metal or TCO film as the transparent electrode. The layer could be realized by physical vapour deposition (PVD), i.e., either sputtering or e-beam evaporation. We preferred the TCO option because our first sputtering trials of ITO were successful, despite a brittle ITO target. Moreover, if a metal film is used, it must be less than $20\,\mathrm{nm}$ thick. Although the substrate is rotated during the deposition, there are still non-uniformities in film thickness. With thin metals, small variations in thickness result in large variations in transparency and conductivity.

For photodetectors based on a-Si:H, in which an a-Si:H film is deposited on a TCO substrate, ZnO is preferable to ITO as the TCO material. The a-Si:H is normally deposited using a PECVD process, during which the TCO surface is exposed to hydrogen plasma. When ITO is exposed to hydrogen plasma, hydrogen radicals react with the oxygen in the ITO, and reduce some of the oxide into metals, i.e., indium and tin [143, 144]. This decreases the transparency of the ITO to

visible light, and also changes the electrical properties of the a-Si:H/ITO contact. ZnO, on the contrary, is non-reactive under these conditions [145].

Although ZnO (and AZO) targets are available commercially, we were not allowed to work with zinc in the multi-user machines of the Nanofab because zinc has a high vapour pressure at low temperatures. Usage of zinc in the vacuum chambers would mean that, for a long time, future users of the machine would have zinc contamination in their depositions. Therefore, we had to work with ITO.

The ITO films were deposited in a Lesker magnetron sputtering machine with a Lesker ITO target. Prior to deposition, the chamber was pumped down to a pressure of $2\,\mu\mathrm{Torr}$. The deposition was done at room temperature in a pure argon environment with a gas flow of $50\,\mathrm{sccm}$, and under pressure of $5.3\,\mathrm{mTorr}$. Each deposition lasted for $50\,\mathrm{min}$. An RF power of $80\,\mathrm{W}$ was used during the process. Under these conditions, the mean deposition rate of the ITO was $5.5\,\mathrm{nm/min}$. Film resistivity was measured immediately after deposition using a four-point probe. The average value was $5.83 \cdot 10^{-4}\,\Omega\,\mathrm{cm}$. Deposition of ITO films in a reactive process, where the chamber atmosphere was 1% oxygen, resulted in films that were about twice as resistive (or half as conductive).

After deposition, the ITO films were annealed for two hours in air at 150–$175^{\circ}\mathrm{C}$. The average resistivity after annealing was $5.45 \cdot 10^{-4}\,\Omega\mathrm{cm}$. Annealing trials that were performed at 250–$325^{\circ}\mathrm{C}$ instead resulted in increased resistivity. As shown in Fig. 3.9, annealing had negligible impact on film transparency. ITO films show high optical transmission for wavelengths longer than $400\,\mathrm{nm}$, and this makes them suitable for photodetection in the visible and near IR bands.

Light-Sensitive Devices

Micralyne deposited two sets of a-Si:H films for us by PECVD. Both depositions were done at $200^{\circ}\mathrm{C}$. In the first set, a-Si:H was deposited on two thermal-oxide silicon wafers. One film was $50\,\mathrm{nm}$ thick, and the other was $1000\,\mathrm{nm}$ thick. The purpose was to characterize the films, and to determine their suitability for the VI-CMOS image sensor prototype. In the second set, a-Si:H was deposited on four ITO-coated Borofloat wafers. Film thicknesses were 250, 500, 750, and $1000\,\mathrm{nm}$. These depositions were used to fabricate the photodetector dies. The $1000\,\mathrm{nm}$ film in this second set, however, was not uniform over the substrate. "Bald" areas could be seen. We asked for multiple thicknesses to experimentally determine the optimal photodetector thickness.

The thin Micralyne film on the thermal oxide substrate was used for characterization of optical properties in the visible band. Measurement was performed with the Woollam variable angle spectroscopic ellipsometry (VASE) system in the UofA Nanofab. Ellipsometry is a non-destructive characterization method. Because this method is based on reflected light, the a-Si:H film had to be thin to ensure that not all the light reaching this layer is absorbed.

Linearly polarized light is incident at the surface of a sample. The light is reflected at the different interfaces of the sample and some of it is absorbed. In the general case, the light reflected from the sample is elliptically polarized. It has a component that is parallel to the plane of incidence, r_p, and a component that is perpendicular to this plane, r_s. The reflected light reaches a detector that measures the magnitude of the two components and their phase difference for each wavelength. Ellipsometry is an indirect characterization method. One needs to perform a model analysis to extract the refractive index and the thickness of the different layers. The analysis is done by an iterative process, and a good initial guess is needed for a successful construction of a model. More details about ellipsometry are available from Woollam [146].

Model analysis for the Micralyne a-Si:H film was performed using the software included as a part of the Woollam VASE system. The initial guess was a structure composed of a crystalline

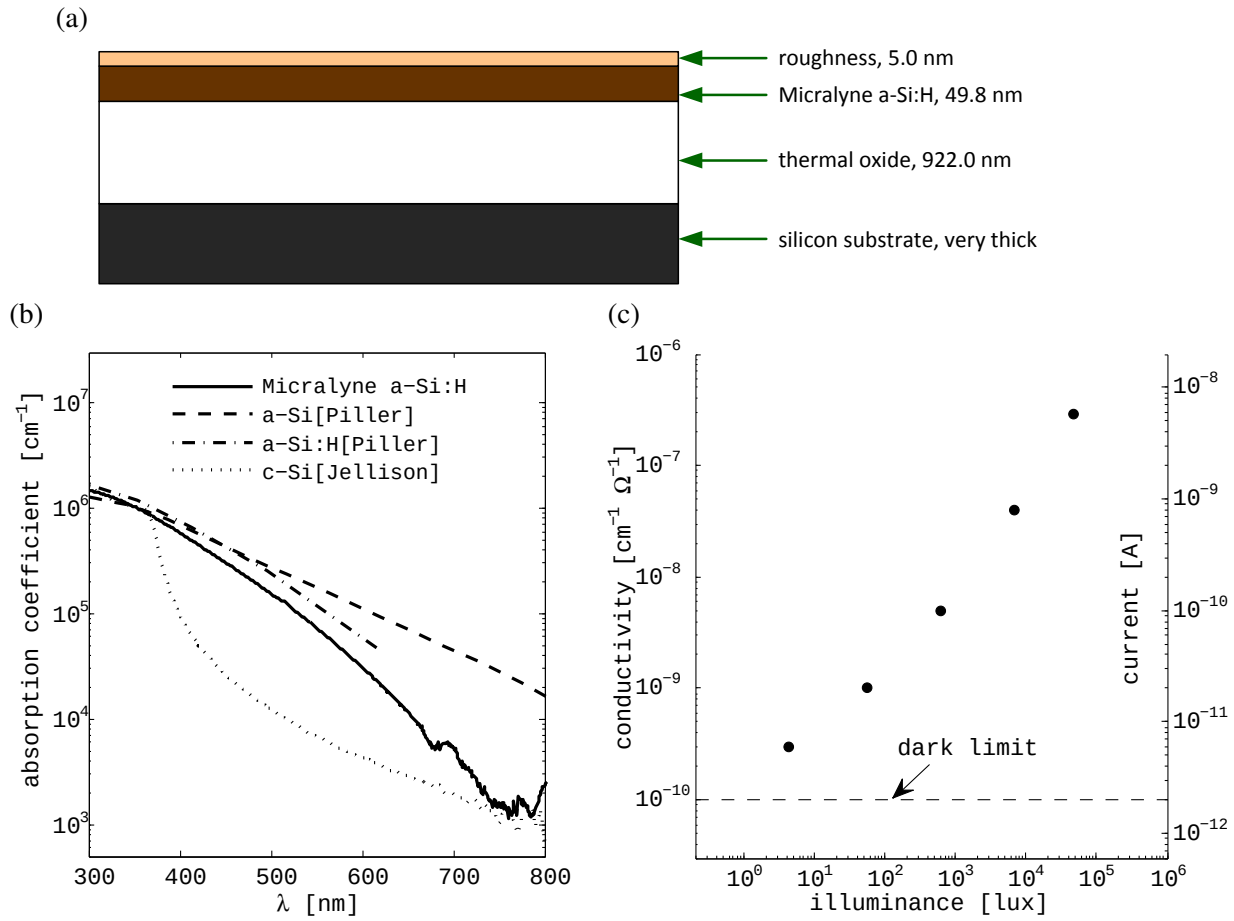


Figure 3.10: Optoelectronic properties of Micralyne a-Si:H films: (a) the best-fit structure obtained for ellipsometry measurement done with a thin ($\approx 50\,\mathrm{nm}$) a-Si:H film deposited on a thermal oxide substrate; (b) absorption coefficient as obtained by ellipsometry in comparison to literature values; and (c) film conductivity and estimated pixel current for varying surface illuminance.

silicon substrate, a $1000\,\mathrm{nm}$ thermal oxide layer, a $50\,\mathrm{nm}$ a-Si:H layer, and a $10\,\mathrm{nm}$ surface roughness layer (a mixture of void and a-Si:H). The refractive index of the handle substrate was based on Jellison's model [147]. This layer is much thicker than the other and assumed to absorb all light that enters it. The refractive index of the thermal oxide layer was taken from tabulated values provided by the software, and the initial guess for the refractive index of the a-Si:H layer was the tabulated value of non-hydrogenated a-Si, also provided by the software. The thicknesses of the thermal oxide, the a-Si:H, and the roughness layers were varied during simulation, as well as the refractive index of the a-Si:H layer. The best-fit structure that was obtained by the end of the process is shown in Fig. 3.10(a).

The absorption coefficient, $\alpha(\lambda)$, of the a-Si:H film was calculated from the refractive index, $n(\lambda)$, obtained for this layer in the best-fit model. Results are shown in Fig. 3.10(b). The plot compares the absorption coefficient of the Micralyne film to reported values for crystalline silicon [147], as well as hydrogenated and non-hydrogenated amorphous silicon [148]. In most of the visible band, the Micralyne film absorbs about ten times as much light as does crystalline silicon.

The thick Micralyne film on the second thermal oxide substrate was used for optoelectronic

characterization. Because the thermal oxide is an insulator, electrical properties of the film could only be tested with surface contacts. The transmission line model (TLM) method [149] was used to extract sheet resistance. This method requires long contacts with variable spacing to be patterned. Aluminum was deposited on the a-Si:H to form the contacts, and this was followed by a single lithography step. Aluminum interacts with a-Si:H to form ohmic contacts even at low temperatures [150]. Given film thickness, the material conductivity may be extracted.

Measurements with the patterned Micralyne film were repeated for several levels of surface illuminance. The light source was a halogen light bulb with a $3050\,\mathrm{K}$ correlated colour temperature and a cold fiber waveguide. Electrical measurements were performed using a probe station and a HP 4156 parameter analyzer. To estimate surface illuminance, luminance was measured with a meter from light reflected off white paper that was illuminated under identical conditions to the sample. Results are shown in Fig. 3.10(c).

Conductivity of the Micralyne film changes by about four orders of magnitude in response to a similar change in surface illuminance. Fig. 3.10(c) shows that the dark conductivity is $10^{-10}\,\mathrm{cm}^{-1}\,\Omega^{-1}$. In general, a-Si:H films with dark conductivity from 10^{-9} to $10^{-11}\,\mathrm{cm}^{-1}\,\Omega^{-1}$ are of good quality [151]. A second y-axis gives the estimated current for a $10 \times 10\,\mu\mathrm{m}^2$ pixel, i.e., for pixel dimensions more suitable for imaging than the ones actually used ($110 \times 110\,\mu\mathrm{m}^2$), assuming $1\mathrm{V}$ is applied across a $500\,\mathrm{nm}$ film. Currents in this range may be easily sensed by CMOS circuits. Fig. 3.10(c) proves that the Micralyne a-Si:H films are suitable for imaging in the visible band with readout done using conventional CMOS circuits.

There is one more factor to note. Steabler and Wronski [152] found that, when exposed to light, there is a gradual decrease in the photocurrent and dark current of a-Si:H films. This change can be reversed by annealing the films in a temperature that is slightly lower than their deposition temperature. Extensive research has been done on the Steabler-Wronski effect (SWE) by various groups around the world, such as Stutzmann *et al.* [153]. We are not certain to what extent our VI-CMOS image sensor is affected by the SWE. However, our main purpose is prototype fabrication and proof of functionality. Different light-sensitive devices may be used in future.

3.2.3 Flip-Chip Bonding

Fig. 3.3 shows finished CMOS and photodetector dies. UBM bond pads were fabricated on the photodetector dies, both on the a-Si:H surface, where they are arranged in a 20×24 array, and on the exposed ITO at the array periphery. Design and fabrication of these bond pads are discussed in Appendix A. The finished dies were sent to a flip-chip contractor, who deposited TSM on the interior bond pads of the CMOS dies, formed indium-based solder bumps on the UBM bond pads, and assembled several prototypes by flip-chip bonding.

Difficulties encountered by the contractor suggest that, for future projects of a similar nature, it is preferred that the UBM bond pads be prepared at the contractor's facility. The process developed there for the UBM includes deposition of a titanium adhesion layer and a thick aluminum layer. This is followed by electroless-nickel immersion-gold plating. It is also preferred that undiced glass substrates with photodetector arrays are sent rather than photodetector dies. Some dies were damaged as they were too small to handle. After formation of the solder bumps, the flip-chip contractor can dice the substrates into dies at his facility.

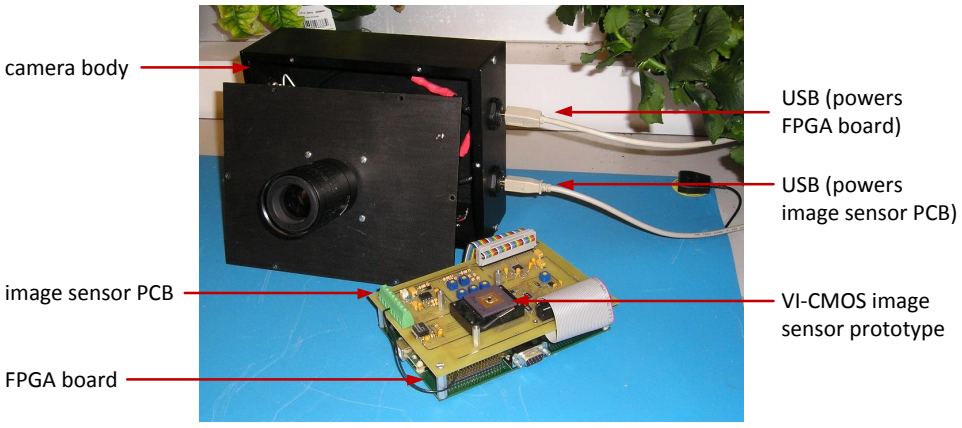


Figure 3.11: Digital camera that was designed and built to test the VI-CMOS prototype. The camera body accommodates a commercial board with an FPGA and a custom-made board that includes the image sensor. Board powering and data transfer between the FPGA and a PC are done through two USB ports.

3.3 Experimental Results

A PCB was designed to test the VI-CMOS image sensor prototype. For data conversion, the PCB includes a 16-bit commercial ADC (Texas Instruments ADS8411). Activation of the image sensor and the ADC is accomplished with an Altera Cyclone II FPGA board, which communicates with a PC through a QuickUSB board from Bitwise Systems. The FPGA is programmed to scan the array using the row and column address decoders. After a new address is placed, control signals are sent to the ADC to sample the analog output line of the image sensor. Data placed on the ADC output bus is read at video rate by the FPGA and sent to a PC.

In the PC, an application has been developed in MATLAB and C++ to process the data in real time and display it on the screen. To capture scenes, the image sensor PCB is placed on the top of the FPGA board, and the two are accommodated in a camera body that was designed for this purpose. The two boards are powered by universal serial bus (USB) ports of the PC. A photo of the disassembled camera is shown in Fig. 3.11.

The main drawback of the VI-CMOS prototype is its low spatial resolution. To demonstrate the effect of working with large pixels, the same scene was photographed with a commercial CCD camera (an Olympus D-575 with 3.2 megapixels and a 1/2.5" sensor) and with the prototype. The original photo taken with the CCD camera is shown in Fig. 3.12(a). Fig. 3.12(b) shows the image obtained after the original photo has been processed to match the resolution of the VI-CMOS prototype, i.e., an array of 20×24 pixels with $110\,\mu\mathrm{m}$ pitch. A photo of the mug as taken with the prototype is shown in Fig. 3.12(c). The shape of the mug, including the handle, is clear in both Fig. 3.12(b) and (c). Also, in both cases one may detect the central line and the dots of the dark pattern on the mug.

Signal and noise properties of a digital camera define four important measures that affect the overall image quality: the signal-to-noise ratio (SNR), the signal-to-noise-and-distortion ratio (SNDR), the dynamic range (DR), and the dark limit (DL). Noise sources exist in the imaging system and in the scene. They can be divided into two types: temporal noise and fixed-pattern noise (FPN). The SNR considers only the temporal noise, whereas the SNDR considers both temporal and fixed-pattern noise, which are assumed to be uncorrelated. The DL is the luminance

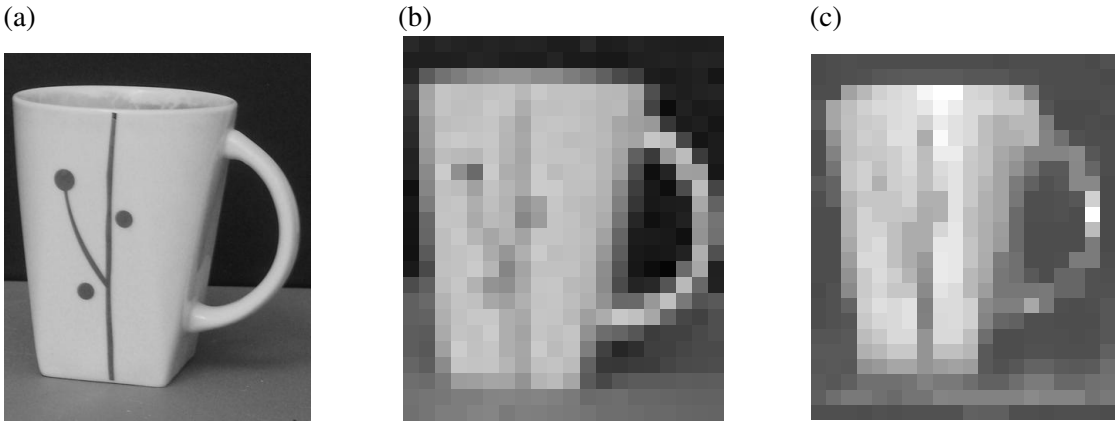


Figure 3.12: Example images: (a) taken with a commercial CCD camera; (b) same as previous but with the resolution changed to match that of the prototype; and (c) taken with the VI-CMOS prototype.

level for which the SNDR is $0\,\mathrm{dB}$. At this operating point, the signal and noise power are equal. The DR is the range of luminances that the imaging system can capture in a single frame with SNDR greater than $0\,\mathrm{dB}$.

To characterize the signal and noise properties obtained with the VI-CMOS prototype, the camera was pointed at a uniformly illuminated scene. A light bulb with colour temperature of $2700\,\mathrm{K}$ was used as the light source. The image plane illuminance was varied by changing the aperture diameter (or the f-number) of the pupil. Nine calibrated values are defined on the lens (Fujinon CF25HA-1) that is used with the camera. A neutral density filter (Hoya ND400) with attenuation ratio of 400 was used in combination with the pupil. The scene luminance captured by the camera was measured with a light meter (Sekonic L-758CINE) in $\mathrm{cd/m^2}$.

For these measurements, the image sensor was configured to connect the vertical photodetectors to the input nodes of the standard logarithmic-response circuits, and data was read through the output lines of those circuits. 20 frames sampled at a frame rate of $70\,\mathrm{Hz}$ were read and recorded at each luminance level. The data was used for statistical calculations, i.e., calculations of means and standard deviations, that are needed to determine the signal and noise properties. The average response of each pixel is used as calibration data for a real-time FPN-correction algorithm.

Fig. 3.13 shows SNDR curves of the human eye and conventional CMOS APS cameras. It also shows the SNDR curve obtained with the VI-CMOS prototype. When enough time is given for adaptation, the DR of the human eye extends at least $170\,\mathrm{dB}$. The peak SNDR of the human eye is $36\,\mathrm{dB}$, which is reached in typical office luminance [55]. Human vision has three regions of operation [56]. Scotopic vision, or dark vision, occurs for luminances lower than $10^{-3}\,\mathrm{cd/m^2}$, and photopic vision, or color vision, occurs for luminances higher than $3\,\mathrm{cd/m^2}$. For luminances between these thresholds, the human eye operates in a transition mode called mesopic vision. In this region, the response to colour gradually deteriorates as luminance decreases.

Cameras with a linear CMOS APS or a CCD sensor can achieve high SNDR but have a low DR, whereas a logarithmic CMOS APS is characterized by a high DR but low SNDR [31]. Janesick [32] and Hoefflinger [82], for example, reported values obtained experimentally with linear and logarithmic CMOS APS cameras, respectively. Assuming parameters of a conventional lens, data provided for the image plane illuminance at which the SNDR of an image sensor is

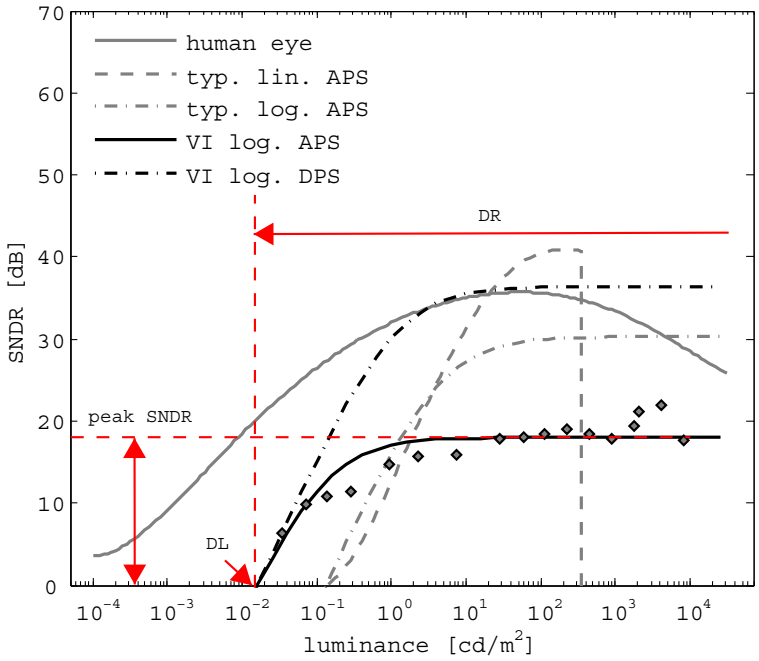


Figure 3.13: SNDR curves of the human eye, digital cameras with typical linear and logarithmic CMOS APS, and with the logarithmic VI-CMOS APS prototype. The expected curve from a digital camera with a logarithmic VI-CMOS DPS is also shown. The DR, peak SNDR, and DL of the VI-CMOS prototype are annotated.

0 dB can be used to estimate the DL of a digital camera built with that sensor. One may conclude from Fig. 3.13 that the prototype has a better (lower) DL than a typical CMOS APS, and a better (higher) DR than a linear CMOS APS. However, its peak SNDR is low.

In electronic image sensors, conversion of analog signals generated by photodetectors into digital signals can be done at four different levels. At board level, one or more ADCs are placed on the PCB. At chip level, one or more ADCs are fabricated on the same chip as the sensor array. At column level, there are one or two ADCs at the edge of each column and, at pixel level, each pixel contains an ADC to make a digital pixel sensor (DPS). In general, the longer the path an analog signal needs to travel to reach an ADC, the greater the noise it accumulates. Increased noise translates into poorer performance in terms of SNR, SNDR, DR, and DL.

Although chip and column level data conversion are typically used in a commercial CMOS APS, data conversion was done at board level here with the VI-CMOS prototype. In a parallel project, Mahmoodi designed, built, and tested a logarithmic CMOS DPS, where each pixel includes a delta-sigma ADC [87]. Characterization of this image sensor shows that its DL is comparable to that of a conventional CMOS APS, and its DR is comparable to that of a logarithmic CMOS APS. However, thanks to the pixel-level data conversion, the SNDR is significantly improved when compared to a logarithmic CMOS APS. Mahmoodi's data indicates a peak SNDR of at least 36 dB. Therefore, Fig. 3.13 also shows the expected SNDR curve from a VI-CMOS image sensor that has a photodetector optimized for low DL, a logarithmic response that achieves high DR, and pixel-level data conversion for high SNDR.

3.4 Conclusion

Image sensors include photodetectors and mixed-signal circuits, which involve devices with different requirements. Vertical integration of these devices means each tier may be fabricated in a different process. This enables advanced circuits in each pixel without sacrificing spatial resolution. Advanced pixel-level circuitry is essential for improving the overall performance of image sensors. This chapter focuses on VI-CMOS image sensors made by flip-chip bonding; they are composed of a CMOS die and a photodetector die. Other fabrication methods for VI-CMOS image sensors are possible.

The main difference between a CMOS die of a VI-CMOS image sensor and a CMOS image sensor is that, with the former, each pixel needs a bond pad for a vertical photodetector and does not need a lateral photodetector. It is desirable to leave the light-sensitive semiconductor unpatterned in the photodetector die of a VI-CMOS image sensor. This results in a preference for feedback active pixels in the CMOS die, whereby potential differences between adjacent photodetector contacts are attenuated to reduce pixel crosstalk.

The design of photodetectors for VI-CMOS image sensors, especially those fabricated by flip-chip bonding, has many more degrees of freedom than the design of photodetectors for CMOS image sensors. Choices need to be made regarding materials used for the handle substrate, the transparent electrode, and the light-sensitive devices. One must also choose the light-sensitive device type, which may be a photoconductor, photodiode, or phototransistor. With all this freedom, photodetectors may be optimized for various applications.

In addition to general design and fabrication principles, supported by extensive references, this chapter presents a specific VI-CMOS image sensor prototype. To make the prototype, a CMOS die was designed for a commercial process, and a photodetector die was designed for a custom process. The CMOS die was fabricated by DALSA through CMC Microsystems, and the photodetector die was fabricated at the University of Alberta Nanofab and Micralyne Inc. Finally, the two dies were assembled by a flip-chip contractor through CMC.

The VI-CMOS prototype includes two sets of CMOS circuits in each pixel. The first is a feedback logarithmic-response circuit, and the second is a standard logarithmic-response circuit. Each pixel also includes both a vertical MSM photodetector, which uses an unpatterned a-Si:H film, and a lateral CMOS photodiode. Optoelectronic properties of the Micralyne a-Si:H films were reported. The films proved excellent for visible-band imaging.

An imaging system has been developed to test the prototype. It is based on a QuickUSB Altera FPGA board that communicates with a PC in real-time. Characterization results of the signal and noise properties at video rates show that the prototype has a lower dark limit and a higher dynamic range than a conventional CMOS APS. The SNDR, however, is low. While data conversion with the VI-CMOS prototype is done at board level, a logarithmic CMOS DPS has recently shown a high SNDR. Therefore, a logarithmic VI-CMOS DPS would have superior signal and noise properties.

The main drawback with the prototype is a low spatial resolution due to large pixels. Even if fine-pitch flip-chip bonding cannot be accessed by Canadian researchers in the near future, there are applications where large pixels are acceptable. For example, in medical X-ray imaging, which is a lens-less imaging technique, pixel pitches are of several tens of microns [154, 155]. Low dark limit facilitates low-dose X-ray imaging. Another advantage of the presented approach is its robustness. As long as contact dimensions and electrical interfaces are preserved, the same CMOS die may be bonded to various sensor dies, which are not limited to photodetector dies.

Chapter 4

Feedback Active Pixels

This chapter discusses pixel circuits that can be used to reduce crosstalk in vertically-integrated (VI) CMOS image sensors with an unpatterned photodetector array. In standard CMOS image sensors (not VI devices), a definition of a clear border to the photodetector cannot be avoided because it shares the pixel area with other CMOS devices. The problem presented here is, therefore, unique to VI-CMOS image sensors. The design methodology of the feedback active pixels strives to maintain a constant potential at the interface nodes, which connect the readout circuits to the photodetector array to create a vertical electric field that is uniform and strong enough to overcome lateral drift and diffusion currents. To support a high DR, the pixel circuit is also designed to have a logarithmic response to light.

Schneider *et al.* [104], who fabricated a VI-CMOS image sensor by the thin-film-on-ASIC (TFA) method, have also encountered the problem of lateral currents, and addressed it with a pixel circuit that kept a constant voltage across the photodetector interfaces. They used an inverter stage for amplification, and a source-follower transistor for feedback. The image sensor was designed to have a linear response. As with typical linear CMOS image sensors, a capacitor is charged before the beginning of a new integration time, and then discharged by the photocurrent. The output signal is the voltage read across the capacitor at the end of the integration time.

Storm *et al.* [83] use a logarithmic amplifier with feedback in their image sensor. However, they work with a standard (not VI) CMOS image sensor, and the purpose of the amplifier is to allow the image sensor to operate in two modes: linear and logarithmic. Also, because their application does not require a constant potential to be maintained at all photodetectors simultaneously, they use a complex operational amplifier (op-amp), which is placed at column level. While both works describe the operating principles of their image sensors, neither of them discuss important considerations in the design process of the feedback amplifier, such as stability and compensation.

Section 4.1 presents a structure of a VI-CMOS image sensor with an unpatterned photodetector array, as well as the requirements from a circuit that can be used to reduce crosstalk in this structure. Section 4.2 presents several principal configurations for pixel circuits that meet the requirements set out in Section 4.1. It elaborates on the power consumption needed for a proper operation of each possible configuration. A small-signal model, which is required for stability analysis, is presented for the configuration with the lowest power consumption. Section 4.3 presents experimental results obtained with a VI-CMOS image sensor, having hydrogenated amorphous silicon (a-Si:H) photodetectors, for different levels of scene luminance. It also analyzes the frequency response and discusses compensation methods to ensure stability of the feedback loop.

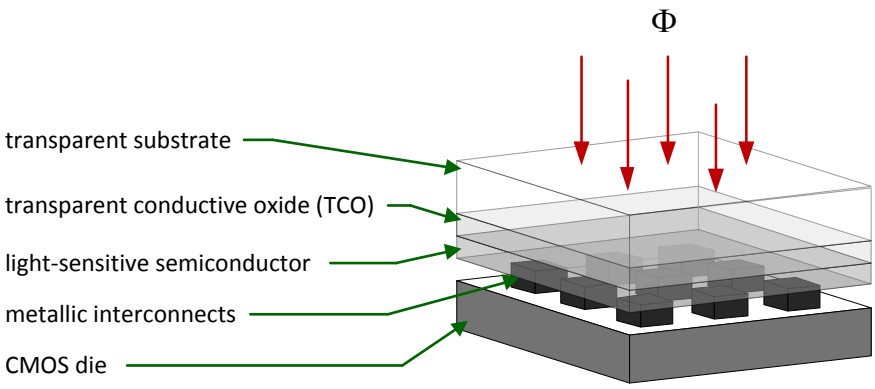


Figure 4.1: Central area of a VI-CMOS image sensor. The CMOS die also contains peripheral circuits and bond pads for wire bonding, which are intended for communication with the external world. Φ refers to the incident illuminance. The TCO layer is connected to a constant potential supplied through the CMOS die by peripheral metallic interconnects (not shown).

4.1 Background

There are several methods for fabrication of VI-CMOS image sensors, as shown in Chapter 3. However, this chapter considers a VI-CMOS design that is fabricated by flip-chip bonding, and whose structure is similar to that of the prototype described in the previous chapter. Nonetheless, the operating principles and design methodology that are presented here are also valid for other fabrication methods.

4.1.1 Device Structure

With flip-chip bonding, the VI-CMOS image sensor is composed of a CMOS die and a photodetector die. The two are processed independently and, after a precise alignment, are attached through metallic interconnects. A drawing of the central area of the structure considered here is shown in Fig. 4.1.

This work treats a case where each photodetector is composed of three layers deposited in the following order: a transparent conductive film, a light-sensitive semiconductor, and a metallic contact. The transparent conductive layer forms a common front contact to all photodetectors in the array. For applications in the visible band, indium-doped tin oxide (ITO) and aluminum-doped zinc oxide (ZnO:Al) are commonly used as transparent conductive oxides (TCOs). Hydrogenated amorphous silicon (a-Si:H) is considered here as the light-sensitive semiconductor. This material has a high absorption coefficient in the visible band ($\alpha \approx 10^5\,\mathrm{cm}^{-1}$). It has been widely used in optoelectronic devices, such as photovolatic cells and photodetectors. The last fabrication stage of the photodetector die includes placement of metallic bond pads on the semiconductor. The bond pads are composed of a metal stack, and the first metal deposited on the a-Si:H needs to have a good adhesion to non-metallic substrates (Appendix A). Titanium and chrome are commonly used for this purpose. In this work, the photodetector structure is assumed to be ITO/a-Si:H/Cr.

4.1.2 Reduction of Crosstalk

Crosstalk is a situation where signals reach destinations other than their intended ones. In the VI-CMOS image sensor considered here, crosstalk is caused by flow of lateral currents in the die with the photodetectors. These currents might result in collection of photo-generated charge carriers in the "wrong" pixels, which degrade the image quality. One way to prevent lateral currents is by formation of physical borders between the photodetectors using lithography steps such as material etching and doping. However, this type of solution introduces defect states and other imperfections, such as dangling bonds, at the edges of the patterned devices. Moreover, the additional lithography steps required to create the borders increase the overall manufacturing cost of the device.

Lateral currents evolve from two different mechanisms: drift and diffusion. Diffusion of charge carriers is a result of concentration gradients, which arise from variations in the illuminance over the array. The number of generated free charge carriers in each pixel is proportional to the number of photons incident on its surface. Therefore, there is a diffusion of charge carriers from the pixels where more photons are absorbed to the darker pixels in the same frame.

Drift of charge carriers is a result of variations in the electric potential applied at the different pixel contacts. Potential differences cause flow of currents (net positive charge) from the pixel contacts where the potential is high to the pixel contacts with lower potentials. Conventional circuits used in CMOS image sensors, both linear and logarithmic, sense the photodetector voltage, which varies from one pixel to another in accordance with the amount of photons absorbed in each pixel. If such circuits are used in a VI-CMOS image sensor, where the light sensitive semiconductor layer is left unpatterned, potential differences between adjacent pixels result in flow of lateral currents toward the pixel contacts with lower potentials, as shown in Fig. 4.2(a). "Node a" in the figure refers to the node where the photodetector is electrically connected through a metallic interconnect to a pixel circuit in the CMOS array. The TCO front contact of the photodetector, which is connected to one of the power rails (i.e., vdd or ground) is referred to as "node b".

Crosstalk caused by lateral drift currents in the semiconductor can be reduced by maintenance of a constant electric potential at all pixels. The applied electric field should be strong enough in the vertical direction to ensure that the currents caused by diffusion become negligible. The currents in the unpatterned semiconductor layer for the case where a uniform potential is applied at all pixels are illustrated in Fig. 4.2(b).

4.1.3 Primary Circuit Requirements

In VI-CMOS image sensors with an unpatterned photodetector array, the photodetector voltage must remain constant at all illuminance levels. Therefore, these image sensors require a new design for the pixel circuit, where photodetector current is used as the input signal. The number of generated free charge carriers in the light-sensitive semiconductor is proportional to the image-plane illuminance. Excess free charge carriers increase the conductivity of the film, and so, under a constant voltage, the pixel current increases proportionally with illuminance.

To design an efficient readout circuit, one is required to know the expected range of the photodetector resistance, R_{ph}. The overall DR of an image sensor, DR, is defined as the ratio between the brightest illuminance that can be captured without causing a saturating response, $\Phi_{\max}$, to the dimmest detectable illuminance in the same frame, $\Phi_{\min}$. It is bounded by the performance of the photodetector and that of the readout circuit. The readout circuit needs to be designed to handle the full range of R_{ph}. Under a constant voltage drop, this value is inversely proportional to the photocurrent, I_{pd}.

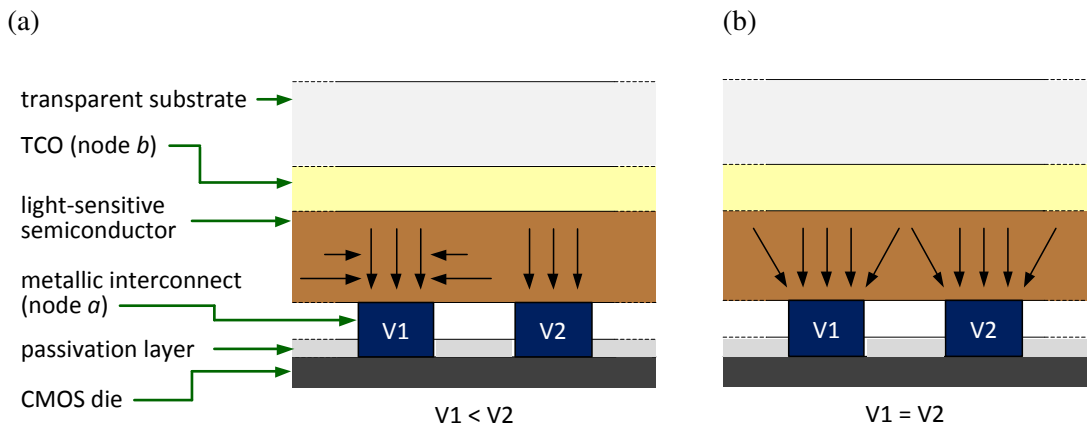


Figure 4.2: Cross section of the structure shown in Fig. 4.1. (a) When the light-sensitive semiconductor layer is unpatterned, potential differences between adjacent pixels results in flow of lateral currents toward pixels with lower potentials. (b) Lateral currents can be reduced by maintenance of a constant potential at all pixels. The electric field needs to be strong enough to overcome diffusion of charge carriers due to concentration gradients.

Fig. 4.3 shows the conductivity, σ, of an a-Si:H film versus image-plane illuminance, which was obtained experimentally, as explained in Chapter 3. The figure also shows the estimated photodetector current for a $1\,\mathrm{V}$ drop, film thickness of $500\,\mathrm{nm}$, and pixel area of $110\,\mu\mathrm{m} \times 110\,\mu\mathrm{m}$, as used with the VI-CMOS prototype of Chapter 3. Photodetector resistance is expected to vary by four orders of magnitude when the image-plane illuminance is varied by six orders of magnitude, i.e., by a DR of $120\,\mathrm{dB}$.

Conventional circuits used in CMOS image sensors can have either a linear or a logarithmic response to the image-plane illuminance. The logarithmic response is the preferred one in this work because the DR that can be captured with logarithmic circuits is significantly higher than that of linear ones. Consider that optical preamplifiers are, in many cases, based on logarithmic amplifiers [156, 157].

To conclude, the pixel circuit of the VI-CMOS image sensor considered here should maintain a constant voltage over the photodetector, sense the photodetector current as its input signal, and have a logarithmic response to image-plane illuminance.

4.2 Design Principles

This section discusses principles in the design of pixel circuits that fulfill the above requirements. These circuits are based on a feedback mechanism, where there are several options to implement a logarithmic feedback element. When a feedback is involved, the system is susceptible to stability problems. Therefore, the small signal model of the loop-gain in the feedback active pixel is presented here and analyzed.

4.2.1 Feedback Circuit Overview

A constant potential needs to be applied at node a in each one of the pixels in the array. This can be implemented by an appropriate pixel circuit, which controls the voltage at this node. The

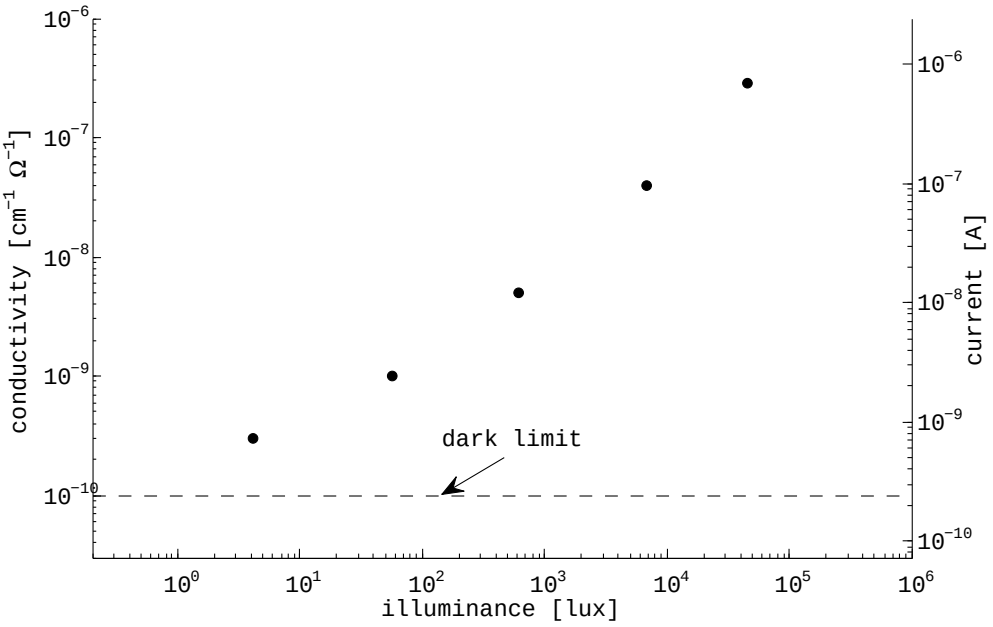


Figure 4.3: Conductivity of an a-Si:H film as measured for varying image plane illuminance. The right y-axis shows the estimated photodetector current for a $1\,\mathrm{V}$ drop, film thickness of $500\,\mathrm{nm}$, and pixel area of $110\,\mu\mathrm{m} \times 110\,\mu\mathrm{m}$, as used in a VI-CMOS prototype

pixel circuit proposed here is based on a differential-input op-amp, where a feedback element and the photodetector are both connected to the negative input node of the amplifier. This circuit is referred to as a "feedback active pixel". A schematic of the feedback active pixel is shown in Fig. 4.4(a). This model is used to describe the large-signal response of the circuit.

A constant reference voltage, V_{ref}, is connected to the positive input node of the amplifier. The amplifier senses the voltage at node a and generates an output signal, V_{out}. Recall that the photodetector resistance, R_{ph}, is inversely-proportional to the pixel illuminance. The feedback loop contains a voltage controlled current source (VCCS), which generates a current, I_{pd}, that depends on V_{out}. In general, I_{pd} may be either a linear or logarithmic function of V_{out}. In a proper design, when the voltage at node a is too high, the generated V_{out} should cause the VCCS to lower its current, which leads to a decrease in the voltage at node a.

A conventional differential stage with an active current-mirror load, as shown in Fig. 4.4(b), is used here as the op-amp. Fig. 4.4(c) shows the output stage of the pixel circuit, which is based on a source-follower (or a buffer) amplifier, a configuration that is commonly used in CMOS image sensors. Transistor T_6 operates as a source-follower, and transistor T_7 operates as a switch that is activated by the control signal *row-select*. When T_7 is on, the column bias current, I_{col}, flows through the stage and V_{pixel} can be read.

4.2.2 Optional Circuit Topologies

To achieve a logarithmic response to image-plane illuminance, the element placed in the feedback loop needs to have a logarithmic relationship between its current and voltage. CMOS transistors operating in weak-inversion, i.e., with their gate-source voltage smaller than their threshold voltage, or $V_{\mathrm{gs}} < V_{\mathrm{th}}$, can be used for this purpose.

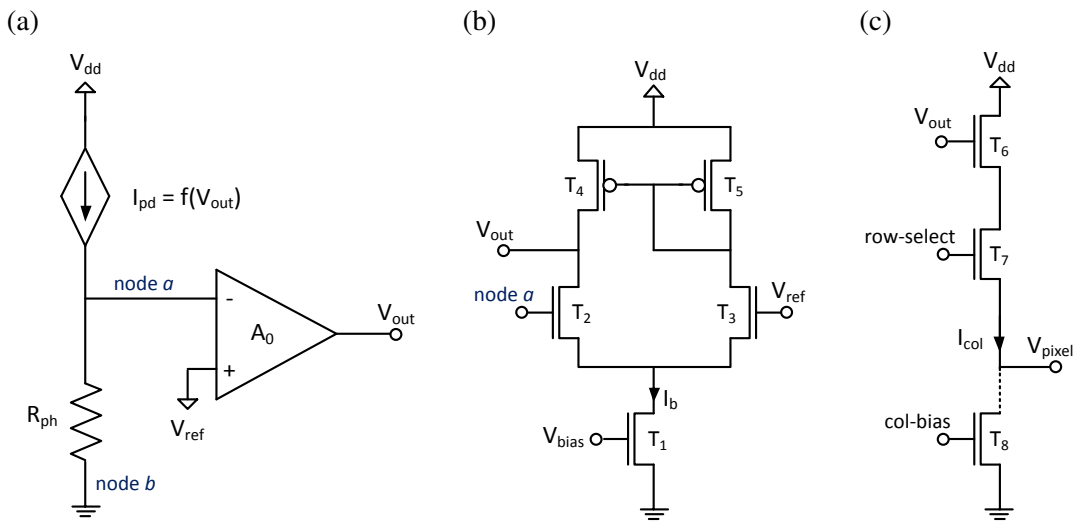


Figure 4.4: (a) Schematic of a feedback active pixel. A constant potential, V_{ref}, is maintained at node a using an op-amp with a negative feedback loop. A voltage-controlled current source (VCCS) generates a current, I_{pd}, that varies as a function of V_{out}. (b) The amplifier may be implemented using a differential-input op-amp with an active current-mirror load. (c) The output stage of the pixel circuit.

There are three principal feedback topologies to choose from: the common-drain (CD), the common-gate (CG), and the "diode-connected" transistor (DCT). Since either an NMOS or a PMOS transistor can be used in each of them, there are six options in total. The three topologies with an NMOS transistor are illustrated in Fig. 4.5. Among the six options, the diode-connected NMOS transistor is the one often used in logarithmic CMOS image sensors, as in the work done by Scheffer *et al.* [158]. In this work, however, all the three configurations are initially examined before selecting the best one for a megapixel image sensor.

In the CD configuration (Fig. 4.5(a)), the output voltage from the amplifier is sensed by the gate of a transistor. In the CG configuration (Fig. 4.5(b)), the source of the transistor is connected to the output of the amplifier. The gate voltage, V_{g}, should be set to a level that ensures that the transistor operates in the weak-inversion region for the whole current range. In the DCT configuration (Fig. 4.5(c)), both the gate and the drain of the transistor are connected to the output of the amplifier. A diode-connected transistor can operate either in weak-inversion or in saturation. In general, the voltage swing of the pixel's output can be increased by adding a second diode-connected transistor in series with the first, which is connected to the amplifier's output, as also mentioned by Basu *et al.* [159].

Although the photodetector is treated as a photoresistor, it is actually an asymmetric metal-semiconductor-metal (MSM) device in this work. Such a device is composed of two back-to-back Schottky junctions. The first is an ITO/a-Si:H junction, which has a barrier height of $0.93\,\mathrm{eV}$. The second is a Cr/a-Si:H junction, which has a barrier height of $0.84\,\mathrm{eV}$. Due to the differences in barrier heights, the dark current is significantly lower when the ITO/a-Si:H junction is reverse biased [142]. However, the photocurrent has the same order of magnitude in both polarities. Given such a photodetector, node b should be connected to the higher potential, i.e., to $\mathrm{V_{dd}}$. A different device structure, which is commonly used for photodetection, is the p-i-n photodiode. In these devices, the polarity should also be set so that the diode is reverse-biased. In each of the three

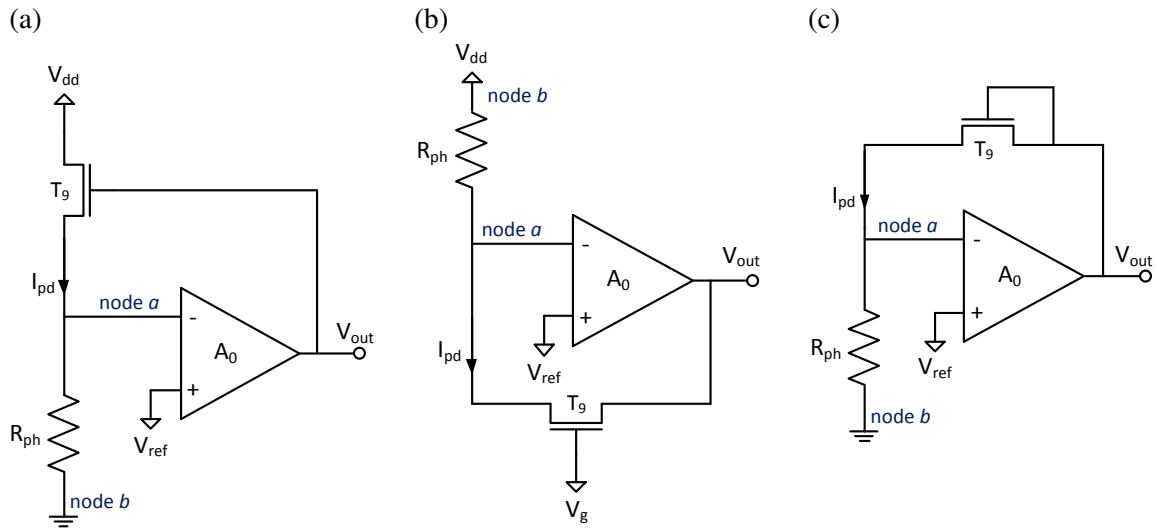


Figure 4.5: A logarithmic response can be achieved by placing a MOS transistor, which operates in the sub-threshold region, in the feedback loop. This work considers three optional configurations: (a) the common-drain, (b) the common-gate, and (c) the "diode-connected" transistor.

configurations shown in Fig. 4.5, the polarity of the photodetector can be inverted by using a PMOS transistor in the feedback loop instead of an NMOS one.

4.2.3 Bias Point Analysis

The first stages in the design process of the pixel circuit need to ensure that it operates properly for the entire expected range of R_{ph}. In a proper design, the voltage at node a should be as much as possible close to V_{ref}, and V_{out} should vary logarithmically with I_{pd}. One may conclude from Fig. 4.3 that I_{pd} is is not likely to exceed $1\,\mu$A in real scenes, especially with smaller pixels.

The bias point analysis of the pixel circuit is also important for estimation of the pixel power consumption. Solid-state image sensors usually contain megapixel arrays, which, in many applications, are designated for portable battery-powered devices. Therefore, the power consumption of each individual pixel plays an important role in the design considerations. By targeting the power consumption of a megapixel array to the order of 1 W, the power consumption of a single pixel would be on the order of $1\,\mu$W. CMOS processes that are commonly used image sensors need to show good analog performance. In such processes, the supply voltage is on the order of 3–5 V. Therefore, to fulfill the power consumption requirements, the pixel current should be limited to about $1\,\mu$A.

Among the three main configurations, the CD is the only one in which the feedback loop does not draw current from the amplifier. In this topology, a transistor's gate is connected to the output node of the amplifier, and I_{pd} is drawn directly from the power supply. In the CG and DCT topologies, however, either a source or a drain of a transistor is connected to V_{out}. Therefore, the current that flows through the feedback loop is drawn from the amplifier. Consequently, to ensure a proper operation of the op-amp over the full illuminance range, including high levels, where R_{ph} is low and I_{pd} is high, its bias current, I_{b}, should be significantly higher than the maximum current required by the feedback loop, or $I_{\mathrm{b}} \gg \max(I_{\mathrm{pd}})$. Basu *et al.* [159] have reached a similar conclusion in a detailed work that investigates CD and CG topologies in a different context.

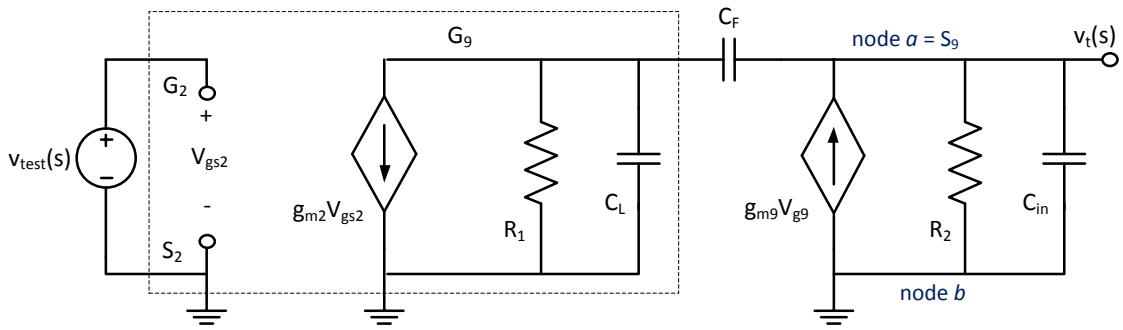


Figure 4.6: Small-signal model of the loop-gain for an active pixel with a common-drain feedback. The simplified small-signal model of the amplifier is shown in the dashed box. If both sides of the amplifier are perfectly matched, the node connecting the sources of T_2 and T_3 is an "AC ground". C_L, C_in, and C_F represent the load, input, and feedback capacitances of the amplifier, respectively. R_1 and R_2 represent the net ohmic resistance connected at the output and input nodes of the amplifier, respectively.

The CG and DCT topologies require each pixel to consume high power at any given moment in order to be ready for the worst-case scenario, in which an extremely high level of illuminance is incident at its surface. This makes these topologies very inefficient because, in typical scenes, most pixels are not exposed to bright light most of the time. On the contrary, in the CD topology, power consumption of a pixel is not constant, but increases with illuminance. Even at high illuminance levels, where I_pd is on the order of 1 μA, the pixel power consumption is still significantly lower than the power consumed constantly by pixels with the other two topologies. This makes the CD topology (also called a source-follower feedback) the most suitable one for a megapixel array. Therefore, the next parts of the work focus on this configuration.

4.2.4 Stability and Compensation

The pixel circuits presented here might encounter stability problems because they are based on a system with a feedback loop. Changes in the phase of the signal traveling through the feedback loop might result in an oscillating response due to positive feedback, although the system was originally designed to have negative feedback. Therefore, the stability of the feedback circuit also needs to be examined in order to ensure a proper design. The DC response is not influenced by the capacitive components of the circuit. However, these devices do affect its frequency response, and play an important role in stability-related issues.

The pixel circuit is designed to cover a high DR of illuminance. A large change in the incident illuminance is translated into a large change in V_out of the amplifier and I_pd in the feedback loop, where transistor T_9 always operates in the subthreshold region. This results in a gradual change in the bias point of the pixel circuit with illuminance. The system's stability should, therefore, be tested for the different bias points, around which the pixel circuit operates, for the full range of expected R_ph values.

In order to test the pixel circuit for stability, its loop gain needs to be examined. The small-signal model of the loop gain is shown in Fig. 4.6. The figure refers to the CD configuration. The simplified small-signal model of the op-amp is shown in the dashed box. This model is based on the assumption that both sides of this differential stage are perfectly matched [160]. Although

the current-mirror load actually results in non-identical drain loads in transistors T_2 and T_3, the simplified model is sufficient for low frequencies.

The transconductance of a MOS transistor, g_m, is given by $g_\mathrm{m} = \partial i_\mathrm{d}/\partial v_\mathrm{gs}$. R_1 is the total resistance connected to the output node, i.e., $R_1 = (g_\mathrm{ds2} + g_\mathrm{ds4})^{-1}$, where g_ds is the output conductance of a MOS transistor, i.e., $g_\mathrm{ds} = \partial i_\mathrm{d}/\partial v_\mathrm{ds}$. C_L consists of all the capacitance connected at the output of the amplifier, which includes C_bd2, C_bd4, C_ds2, C_gd9, and the input capacitance of the source-follower stage (Fig. 4.4). C_in is the input capacitance, which is mainly composed of the photodetector capacitance, C_ph. C_F is the feedback capacitance, which consists of C_gs9 and any compensation capacitor, C_C. Lastly, R_2 is the total resistance connected to the input node, i.e., $R_2 = (R_\mathrm{ph}^{-1} + g_\mathrm{ds9} + g_\mathrm{m9})^{-1}$.

The loop gain, βA_OL is given by [160]

$$\beta A_\mathrm{OL} = \frac{v_t(s)}{v_\mathrm{test}(s)} = -g_\mathrm{m2} g_\mathrm{m9} R_1 R_2 \frac{1 + cs}{as^2 + bs + 1}, \tag{4.1}$$

where

$$a = R_1 R_2 (C_\mathrm{L} C_\mathrm{in} + C_\mathrm{F} C_\mathrm{L} + C_\mathrm{in} C_\mathrm{F}), \tag{4.2}$$

$$b = R_1 (C_\mathrm{L} + C_\mathrm{F}) + R_2 (C_\mathrm{in} + C_\mathrm{F}) - g_\mathrm{m9} R_1 R_2 C_\mathrm{F}, \tag{4.3}$$

$$c = C_\mathrm{F}/g_\mathrm{m9}. \tag{4.4}$$

This expression contains two poles and one finite zero, which are located at

$$p_1 \cong \frac{1}{g_\mathrm{m9} R_1 R_2 C_\mathrm{F}}, \tag{4.5}$$

$$p_2 \cong \frac{g_\mathrm{m9} C_\mathrm{F}}{C_\mathrm{L} C_\mathrm{in} + C_\mathrm{F} C_\mathrm{L} + C_\mathrm{in} C_\mathrm{F}}, \tag{4.6}$$

$$z_1 = \frac{-g_\mathrm{m9}}{C_\mathrm{F}}. \tag{4.7}$$

If the poles are located too close to each other, a phase change of 180° occurs while $\beta A_\mathrm{OL} > 0\,\mathrm{dB}$, and this results in instability. This problem can be solved by adding a compensation capacitor, C_C, between the input and the output of the amplifier, i.e., node a and V_out. The additional capacitance increases the distance between the two poles, but the payment for the increased stability is a smaller bandwidth. In this work the capacitance of C_C is taken to realize a 45° phase margin (PM) based on the simplified model. This is usually the PM a feedback system is required to have in order to prevent oscillating transitions [161].

4.3 Results

Simulation and experimental results are presented in this section for a $0.8\,\mu\mathrm{m}$ DALSA process, where $\mathrm{V}_\mathrm{dd} = 5\,\mathrm{V}$. This is the process used for fabrication of the CMOS die in the VI-CMOS image sensor prototype described in Chapter 3. Circuit schematics indicating transistor sizes that were used in simulations and in the actual design are shown in Fig. 4.7. Simulation results are given for the DC response of six optional circuit configurations. Simulation and experimental results showing the transient response of the feedback active pixel under different luminance conditions are also provided. As the circuit oscillates at some operating conditions, simulations of its frequency response are presented and analyzed. Suggestions are given for improved performance with the current design and with designs of similar nature.

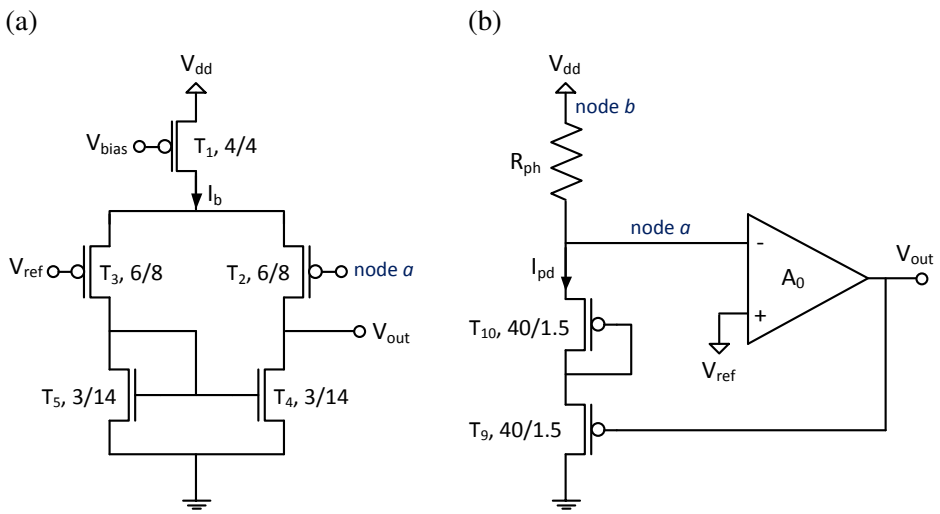


Figure 4.7: Schematics of (a) the op-amp and (b) the entire feedback active pixel. These circuits were used for simulations and were implemented in the CMOS die of a fabricated VI-CMOS prototype.

4.3.1 Power Consumption

The output voltage of the op-amp as a function of $I_{\rm pd}$ for the six optional pixel circuits is shown in Fig. 4.8. Similar sizes were used with all the feedback transistors. The voltage drop over $R_{\rm ph}$ was $1.5\,{\rm V}$ for the CD cases and $2.5\,{\rm V}$ for the rest. The same op-amp was used in all cases, notwithstanding the width of transistor ${\rm T}_1$ in Fig. 4.4(b), which acts as a current source. A ten times wider transistor was needed with the CG and DCT topologies to achieve a similar performance as with the CD topology. In terms of bias current, using the CD topology, the op-amp operated with $I_{\rm b} \approx 1\,\mu{\rm A}$. A bias current of about $36\,\mu{\rm A}$ was required for the other four pixel circuits, which use the CG and the DCT topologies.

Photodetector pitch in the prototype is $110\,\mu{\rm m}$. Based on its expected resistance, the simulation considers a photocurrent range corresponding to Fig. 4.3. Fig. 4.8 shows that the logarithmic response can support a high DR. When the drain current is above $1\,\mu{\rm A}$, the transistor enters saturation mode, where the relation between $I_{\rm ds}$ and $V_{\rm gs}$ is no longer logarithmic.

The feedback active pixel in the prototype was designed with the CD configuration, which is the most power efficient. Because node b needs to connect to ${\rm V}_{\rm dd}$, as explained in Section 4.2.2, the PMOS version is chosen. To increase the voltage swing at the output, a diode-connected PMOS transistor is added to the feedback loop, as shown in Fig. 4.7(b).

4.3.2 Experimental Results

Measurements were performed with the digital camera that was developed to accommodate and activate the VI-CMOS prototype, as described in Chapter 3. The camera was pointed at a uniformly illuminated scene, where a compact fluorescent bulb with a colour temperature of $2700\,{\rm K}$ was used as the light source. A single pixel was sampled at a frequency of $.75\,{\rm MHz}$ with a 16-bit commercial ADC (Texas Instruments ADS8411) that was placed on the same PCB as the image sensor. Image-plane illuminance was varied by changing the lens aperture.

Results of the temporal response are shown in Fig. 4.9(a). One may conclude that starting

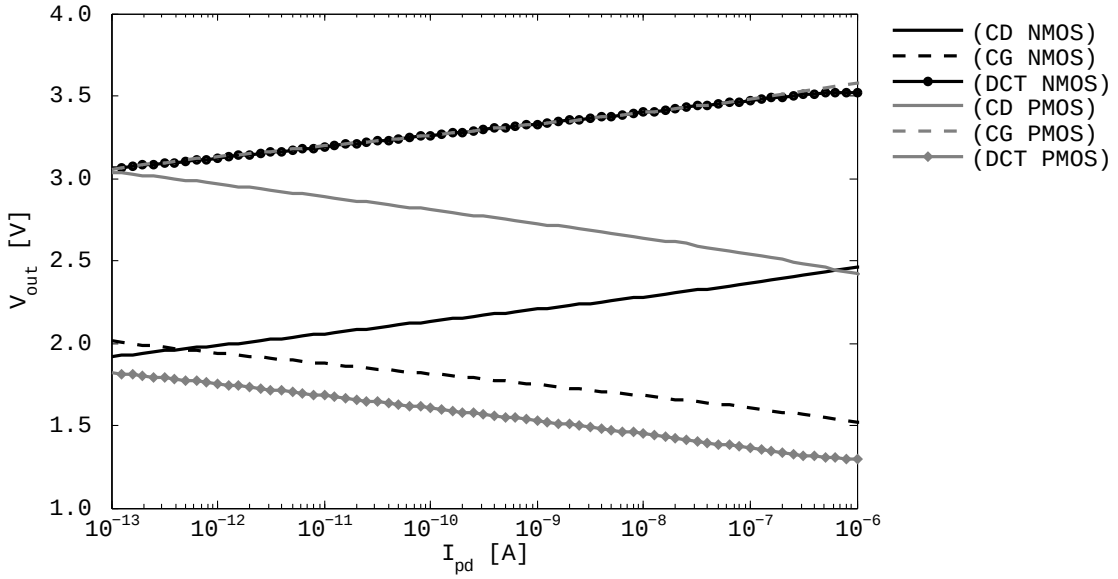


Figure 4.8: The output voltage of the amplifier as a function of the photodetector current is shown here for the different feedback configurations: common-drain (CD), common-gate (CG), and diode-connected transistor (DCT). Each case is examined once with an NMOS and once with a PMOS transistor in the feedback loop.

from a luminance level of about $100\,\mathrm{cd/m^2}$, which is typical office luminance, the circuit suffers from stability problems, and this manifests in an oscillating response. The spectral composition of the transient response was analyzed using tools available in the Signal Processing Toolbox of MATLAB. Fig. 4.9(b) shows that the peak frequency increases logarithmically with luminance. This is an expected result as the transconductance of the elements in the feedback loop changes in a similar manner.

Bias conditions used in the design process turned out to result in unstable conditions in actual operation. Input and output nodes of the pixel amplifiers are not accessible so compensation is impossible after fabrication. However, it is possible to improve the response by changing the bias voltages of the pixel amplifiers, mainly V_{bias}. The transient responses obtained when T_1 was activated with a lower $|V_{\mathrm{gs}}|$ are shown in Fig. 4.9(c).

With the new bias conditions, oscillations start to occur at luminance levels that are about one order of magnitude higher than before. Although the circuit is still unstable for the whole range of luminance, it is stable for a higher range.

There is a trade-off between gain and bandwidth with op-amps. By reducing $|V_{\mathrm{gs}}|$ of T_1, βA_{OL} increases. However, the bandwidth of the feedback circuit diminishes because of the increase in the resistance R_1. Stability is achieved because the bandwidth becomes smaller, and the loop-gain reaches $0\,\mathrm{dB}$ at a lower frequency, where its phase is high enough. The magnitude and phase of the loop-gain are shown in Fig. 4.10 for the original bias conditions and for those used to increase stability. Simulations were performed in Cadence with $R_{\mathrm{ph}} = 10\,\mathrm{M\Omega}$.

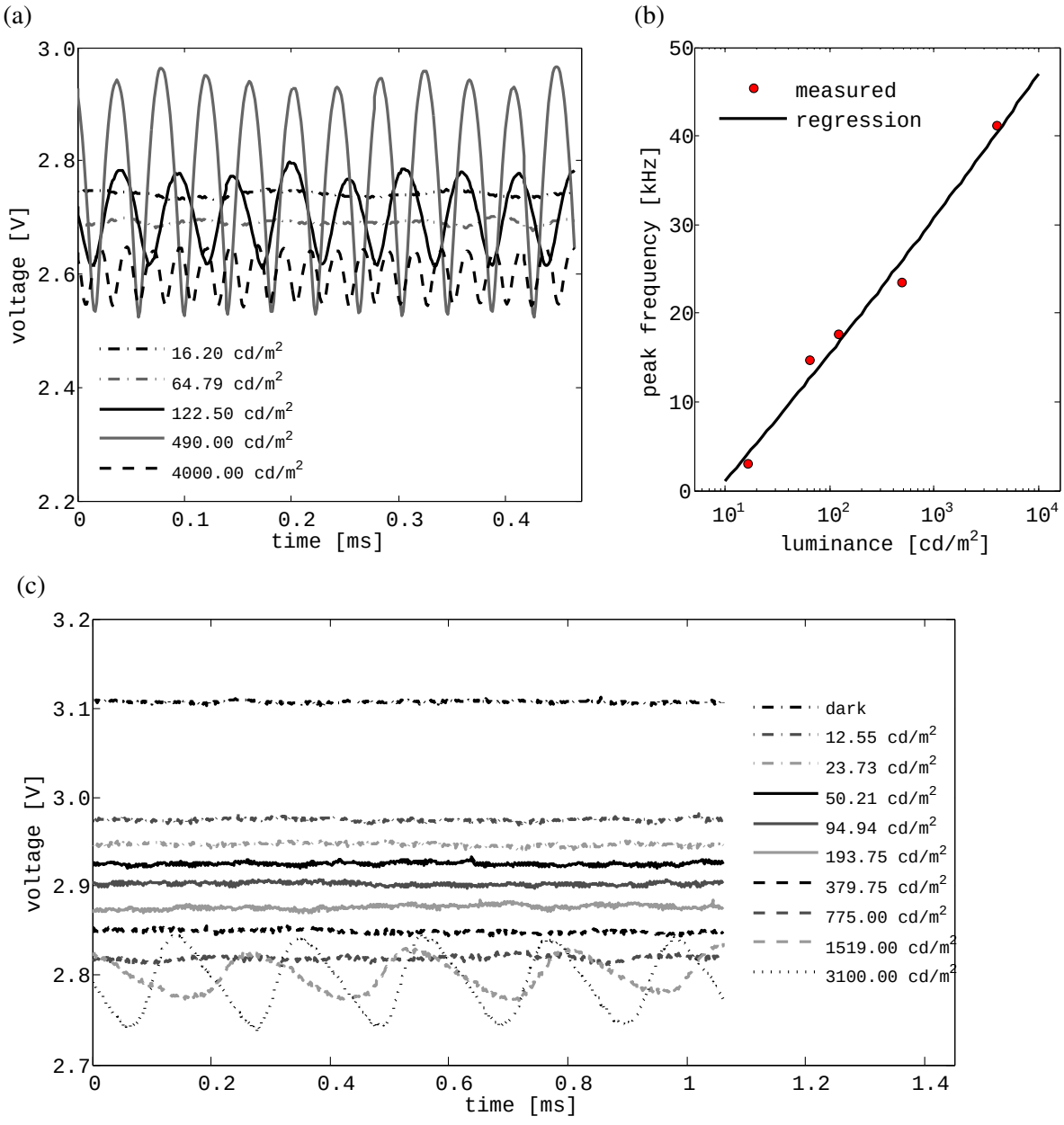


Figure 4.9: Experimental results obtained with the feedback active pixel of the VI-CMOS prototype. (a) The transient response shows oscillation at several levels of luminance. (b) Using signal processing, peak frequency versus luminance is shown. (c) Stability of the feedback active pixel in the VI-CMOS prototype is improved after changing the bias conditions.

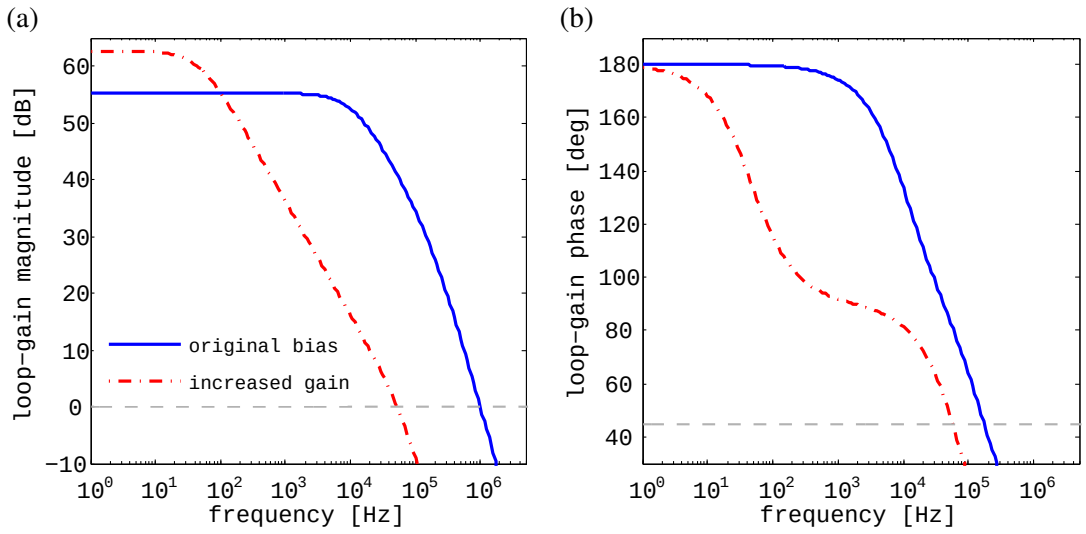


Figure 4.10: Comparison of the (a) magnitude and (b) phase of the loop-gain between two bias conditions. The original biasing results in an unstable response. By changing the bias, the gain is increased and the bandwidth is reduced. This is used to improve stability.

4.3.3 Stability and Compensation

No compensation capacitor was included in the feedback active pixels of the prototype because transient simulations done in Cadence, using default numerical tolerances, indicated that there was no need for additional capacitance. However, as experimental results show, the circuit becomes unstable at luminance levels that fall in its normal range of operation. The problem could have been solved by including a compensation capacitor in each pixel between node a and V_{out}, as explained in Section 4.2.4, that ensures $\text{PM} \geq 45^\circ$ for the whole luminance range.

To determine the minimal compensation capacitance, i.e., the one that results in a 45° PM, one has to solve two equations with two unknowns:

$$|\beta A_{\text{OL}}(f_{0\text{dB}}, C_{\text{C}})| = 1, \tag{4.8}$$

$$\angle \beta A_{\text{OL}}(f_{0\text{dB}}, C_{\text{C}}) = 45^\circ, \tag{4.9}$$

where $f_{0\text{dB}}$ is the unity-gain frequency of βA_{OL}. For simplicity, calculations are performed for a single PMOS transistor in the feedback loop, as per the model presented in Section 4.2.4. The compensation capacitance for the case of two transistors in the feedback loop is found later by simulation. The additional capacitance required for stability is lower in the latter case because the second transistor adds its own capacitance to the feedback loop.

When referring to the magnitude of βA_{OL}, as determined from (4.1), R_2 is approximately $1/g_{m9}$ for the whole illuminance range and, therefore, $g_{\text{m9}}R_2$ is approximately 1. However, as the scene becomes brighter, changes in the bias point of the amplifier result in a significant increase in the value of g_{ds2} and a slight decrease in the value of g_{m2}. Hence, the overall magnitude of the loop gain decreases with illuminance. The 3 dB frequency of the poles and the finite zero increases with illuminance, and this results in an increased bandwidth. The PM, however, becomes smaller with illuminance. To ensure that the pixel circuit is stable in the "worst case", C_{C} needs to be determined for the highest expected illuminance level, i.e., the bias point obtained when $R_{\text{ph}} = 1\,\text{M}\Omega$.

For a photodetector with $110\,\mu\mathrm{m}$ pitch, given $\epsilon_r = 8$ in a-Si:H, one finds that $C_{\mathrm{ph}} \approx 1.7\,\mathrm{pF}$. Using relevant process parameters, the solution gives $f_{0\mathrm{dB}} \approx .8\,\mathrm{MHz}$ and $C_{\mathrm{C}} \approx 1.5\,\mathrm{pF}$. After adding $C_{\mathrm{C}} = 1.5\,\mathrm{pF}$ to the pixel circuit, its loop gain was calculated once according to the simplified small-signal model (Fig. 4.6), and once by running a stability simulation in Cadence. The magnitude and phase of the complex transfer function, as obtained by both methods, are shown in Fig. 4.11. Cadence considers the full circuit, including poles and zeros that arise from the current mirror of the amplifier that were ignored by the simplified analysis. As well, it uses more sophisticated transistor models. Nevertheless, both calculations show very similar results in the low frequency region, which is the region of interest since the loop gain there is high.

Simulation results show that when the actual pixel circuit, which has two PMOS transistors in the feedback loop, is considered, a compensation capacitor with capacitance of $.80\,\mathrm{pF}$ is needed. In the $0.8\,\mu\mathrm{m}$ DALSA process, implementation of this capacitor occupies an area of $592\,\mu\mathrm{m}^2$, or requires a $24.3\,\mu\mathrm{m}$ pitch for a square shape. This is less than 5% of the pixel area.

4.3.4 Large-Signal Transitions

Lastly, simulation of the transient response to a large signal input is essential because it is possible that although a system is designed to have sufficient phase margin at $0\,\mathrm{dB}$ gain, its transient response to a large signal input still oscillates. This is a result of non-linear changes in the voltages and currents of the system during the transition, which affect the location of poles and zeros, and adds a degree of complication to the transient response [161].

The feedback active pixels discussed here are to be used not only for still imaging, but also for video applications, where very fast transitions between luminance levels at each pixel are likely to occur. A large overshoot or a long response time, which result from too low or too high capacitance, respectively, are both not desirable because they also affect the voltage at node a. A large deviation of the voltage at this node from V_{ref}, or a transient deviation that occurs for a long time, results in temporary lateral currents within the photodetector array.

Fig. 4.12 shows the transient response of the feedback active pixel when it is powered up. Simulations were performed for two bias conditions. Fig. 4.12(a) and (b) refer to the original bias conditions used in the design, which correspond to the experimental results that were presented in Fig. 4.9(a), and Fig. 4.12(c) and (d) refer to the bias conditions that correspond to Fig. 4.9(c), where $|V_{\mathrm{gs}}|$ of T_1 is lowered. The simulations show that the oscillation frequency and amplitude are reduced in the latter bias conditions.

Logarithmic circuits are known to have asymmetric transition times to abrupt changes in illuminance, a behavior recognized by Basu *et al.* [162]. With linear circuits, the load capacitor is charged (or discharged) to the dark level at the beginning of each integration cycle, then discharged (or charged) by the photocurrent during integration time and, finally, at the end of the integration cycle, the charge is read as voltage over the load capacitor. Conventional logarithmic image sensors, however, do not have an integration time. Therefore, the photodetector is never precharged electronically to its dark level. All changes in the charge stored in the different capacitors are made by the photocurrent. When the scene becomes brighter, the photocurrent is increased. A large current means that less time is required to charge or discharge the capacitors. With the opposite transition, I_{pd} abruptly decreases, which results in a longer transition time. In the feedback circuit discussed here, the light-to-dark transition time for large changes can be made shorter if I_b is made larger [162] at the cost of a higher power consumption. Another way to make this transition time shorter is to precharge the capacitances to their dark level, similar to the way linear image sensors are operated. The cost in this case is an increased complexity of the circuit.

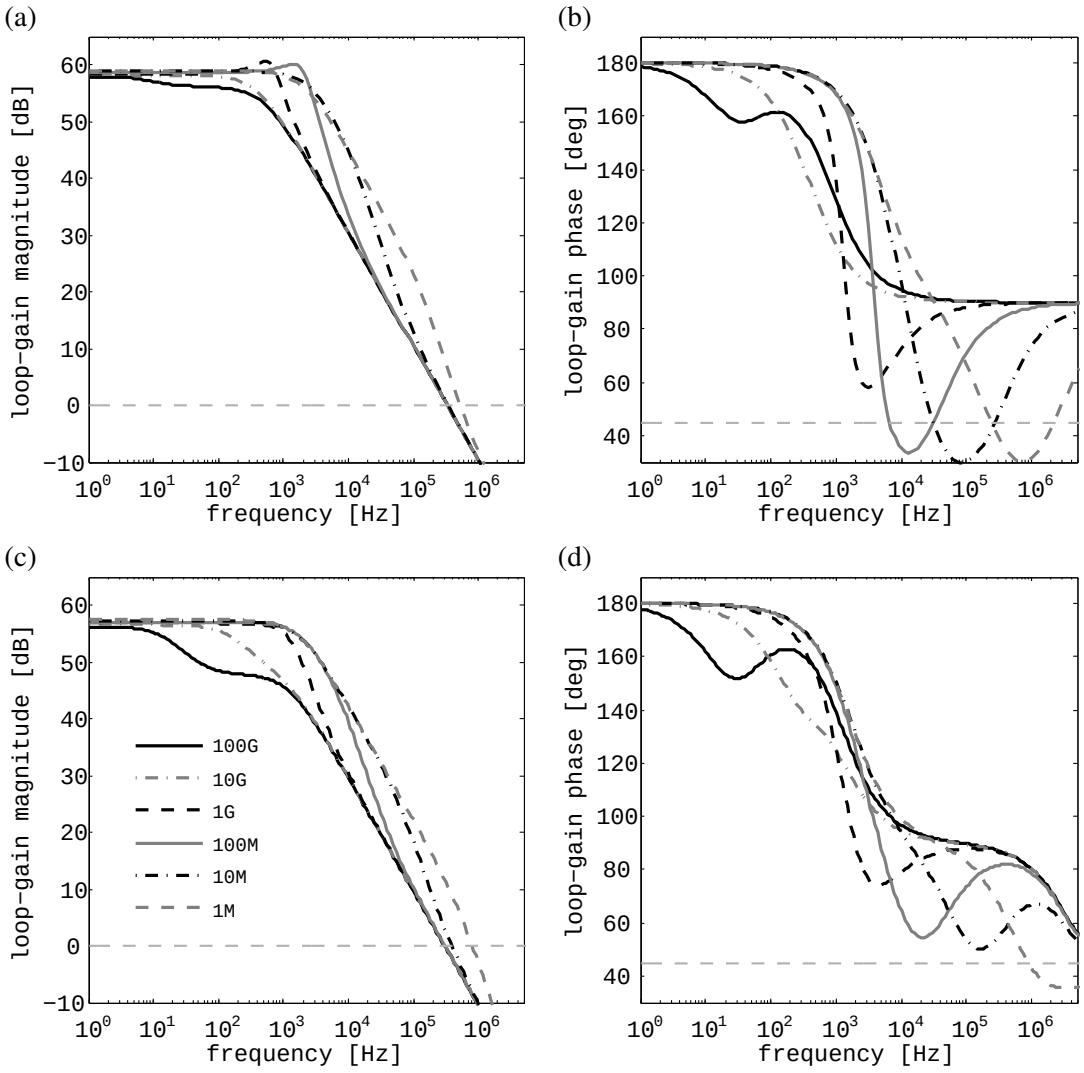


Figure 4.11: Loop gain of the pixel circuit with the feedback configuration based on a PMOS transistor in common-drain for several levels of R_{ph}. The (a) magnitude and (b) phase of the loop gain is obtained from calculation according to the simplified small-signal model. The (c) magnitude and (d) phase of the loop gain is also obtained from Cadence. A capacitance of $C_{\mathrm{C}} = 1.5\,\mathrm{pF}$ was added between the input and output of the amplifier in all cases.

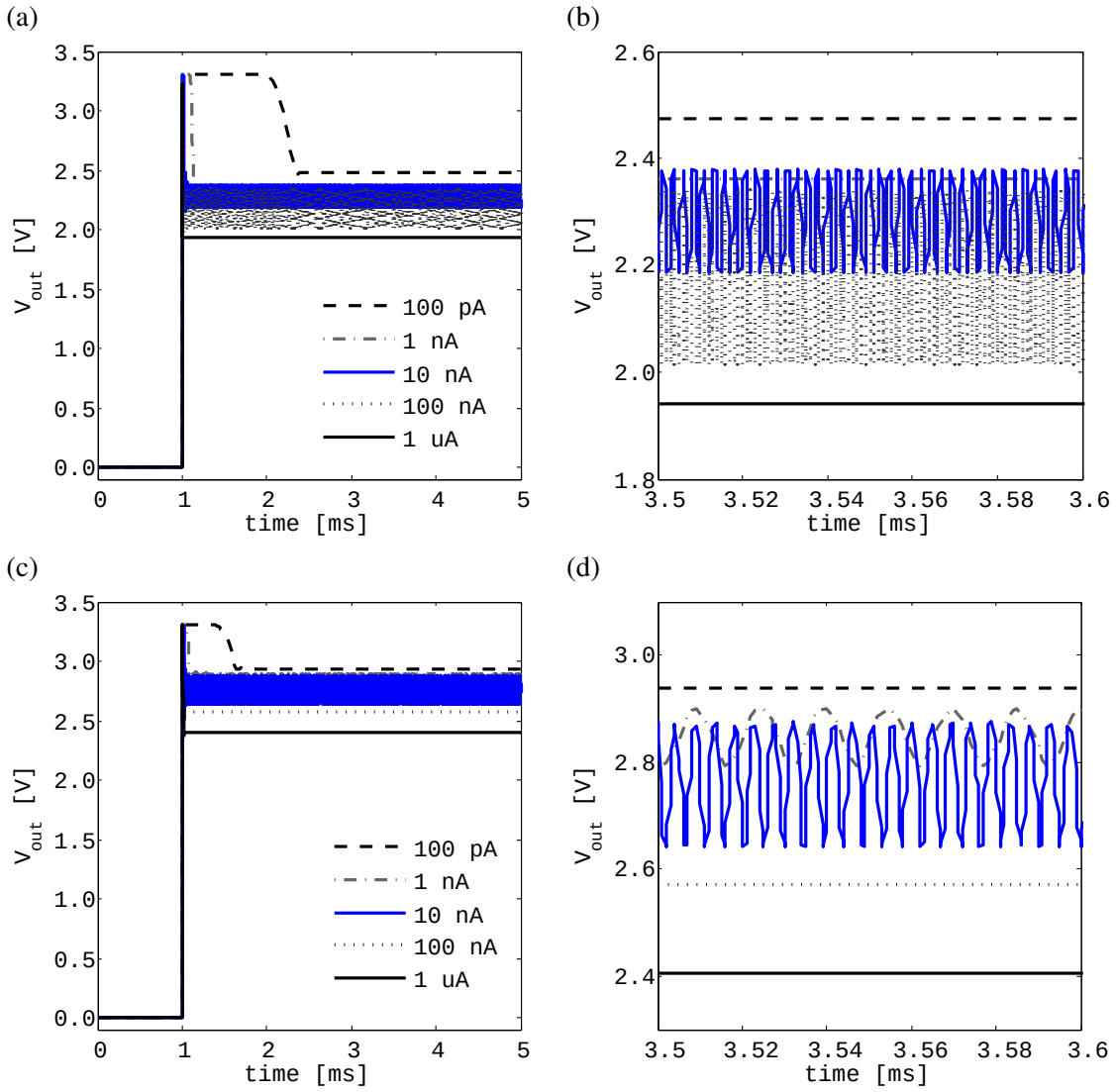


Figure 4.12: Transient response of the feedback circuit when it is powered up. (a) Simulation results with the original bias conditions are shown. (b) A magnified time period of $0.1\,\mathrm{ms}$ in (a) is shown. (c) Simulation results when $|V_{\mathrm{gs}}|$ of T_1 is lowered to the level used in Fig. 4.9(c) are shown. (d) A magnified time period of $0.1\,\mathrm{ms}$ in (c) is shown.

4.4 Conclusion

This chapter discusses pixel circuits that can be used in VI-CMOS image sensors with an unpatterned photodetector array. The main challenge with these image sensors is flow of lateral currents in the photodetector array due to the absence of physical borders. Lateral currents can be reduced by maintenance of a constant electric potential at all pixels in the unpatterned array. This can be implemented with pixel circuits that include an op-amp with a feedback mechanism. Photodetector current is used as the input signal because the voltage must remain constant. To achieve a high dynamic range, the pixel circuit is designed to have a logarithmic response to image-plane illuminance.

Among several optional circuit configurations, the common-drain feedback is found to be the most suitable one for applications involving megapixel arrays as it is the most power efficient. Because of the feedback, these types of circuits are susceptible to stability problems. A simplified small-signal model of the circuit loop-gain is presented to investigate stability. The bias point changes with image-plane illuminance, and the circuit is likely to encounter stability problems at high illuminance levels.

Simulation results performed in a $0.8\,\mu\mathrm{m}$ DALSA process and experimental results obtained with a prototype are presented. The work discusses methods to improve stability in these pixel circuits. A compensation capacitor should be added during the design process. After fabrication, stability can be improved by changing externally controlled bias voltages.

Chapter 5

Photodetector Thickness

In vertically-integrated (VI) CMOS image sensors that are prepared by flip-chip bonding, such as the prototype presented in Chapter 3, the CMOS die is fabricated in a commercial process, whereas the photodetector die is fabricated in a custom process. With the CMOS die, the manufacturer characterizes the devices, and provides design engineers with models that can be used for simulation. With the photodetector die, the designer has more degrees of freedom in choices of materials and film thicknesses. However, no models are available. The ability to predict the behavior of a semiconductor device under various operating conditions is essential to ensure proper functionality and, more importantly, for optimization of devices and systems.

Gopal and Warrier [163] elaborate on the optimal thickness of the $0.1\,\mathrm{eV}$ HgCdTe layer in infrared (IR) photodetectors. They examine the effect of thickness variation on the voltage responsivity, the generation-recombination noise, and the specific detectivity, which is the ratio between the former two. They conclude that the optimal thickness should be within one diffusion length of the minority charge carriers. However, their presented optimization method is rather limited. The expressions used for calculations are given in a final form. They treat only photoresistors with doped semiconductor films and discount contacts.

Yang *et al.* [164] study the influence on photocurrent of thickness variations of $\mathrm{Pb}_{1-x}\mathrm{Sr}_x\mathrm{Se}$ thin films in IR photodetectors. They calculate the photocurrent spectra and the overall photocurrent as a function of film thickness. Calculations are repeated for different film compositions. Like before, the model is limited to this type of photodetectors. Furthermore, an optimum thickness is obtained in each case for the photocurrent. However, the effect of thickness variations on other properties of photodetector performance, such as the dark current, is not considered.

This chapter presents a mathematical model for photodetectors in VI-CMOS image sensors. To develop the model, a finite-differences method is used to solve a system of equations derived from Kirchoff's laws and charge transport equations in semiconductors. The model is applied for thickness optimization of the light-sensitive semiconductor film in the photodetector. Both numerical and analytical solutions are presented. The model is developed for the general case and, later, parameters of a-Si:H films are used for specific calculations. This work considers performance properties of logarithmic CMOS image sensors for optimization, rather than photodetector performance.

Section 5.1 describes the simplified model of the photodetector. Section 5.2 presents the mathematical method that is used to solve the problem. Section 5.3 elaborates on the solution process and presents simulation results. It also presents results obtained experimentally with the VI-CMOS prototype, and reviews layer thicknesses of a-Si:H films in photodetectors reported in the literature.

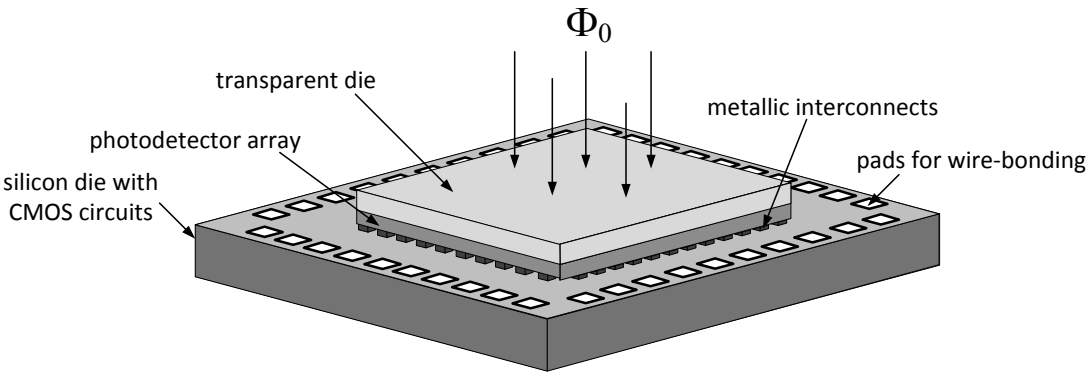


Figure 5.1: Schematic of a VI-CMOS image sensor fabricated by flip-chip bonding. A transparent die with an array of photodetectors is bonded through metallic interconnects to an array of readout circuits on a CMOS die. The CMOS die, which is prepared in a standard CMOS process, also contains peripheral circuits and bond pads for external communication. Φ_0 refers to the incident illumination.

5.1 Photodetector Model

A schematic of a VI-CMOS image sensor made by flip-chip bonding is shown in Fig. 5.1. The image sensor is composed of a CMOS die with an array of readout circuits, and a photodetector die. Each die is processed independently, to optimize performance, and as the last step they are aligned precisely and finally attached through metallic interconnects. Although this chapter refers to this structure, for development of a mathematical model for the photodetector, principles presented here are valid for other fabrication methods of VI-CMOS image sensors.

This section presents a simplified model of the photodetector to estimate its response to varying optical and electrical conditions. The model uses a set of equations that are based on Kirchhoff's laws and charge-transport in semiconductors. An optimization method to obtain a low dark limit (DL) with logarithmic pixel circuits is developed using this model.

5.1.1 Three-Resistor Model

To simplify the analysis, a one-dimensional approach is taken, where the device is assumed to be uniform in the other two dimensions. The schematic of the structure of this photodetector is shown in Fig. 5.2(a). [1] It is composed of three layers, which are deposited in the following order on a transparent substrate, such as glass: a thin film of transparent-conductive oxide (TCO), a semiconductor layer with thickness ℓ, and a thin film of metal. The TCO forms the front contact, while allowing the illumination, Φ_0, to pass to the semiconductor, and the metal layer forms the electrical contact between the semiconductor and the CMOS pixel circuit. The semiconductor is the light-sensitive layer. The voltage across the photodetector is kept constant at V_{ab}, and J represents the current density through the device.

To work with a linear system, which simplifies the modeling and analysis, the two Schottky contacts between the semiconductor and the conductors are replaced with the equivalent resistance

[1] The polarity of the photodetector voltage in this chapter is opposite to that used with the actual prototype, as discussed in Chapter 4. Nonetheless, the analysis presented in the following sections is still valid.

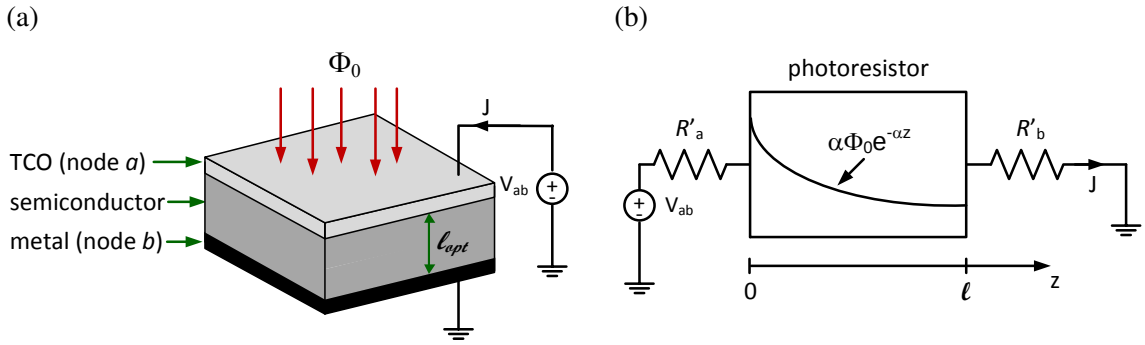


Figure 5.2: (a) In the photodetector, a semiconductor layer with thickness ℓ is sandwiched between two conductive layers: a transparent conductive oxide (TCO) (node a) and a metal (node b). $V_{\rm ab}$ is the applied voltage, and J is the current density. (b) The photodetector can be represented as three resistors in series. $R'_{\rm a}$ and $R'_{\rm b}$ are the scaled contact resistances (in $\Omega\,{\rm cm}^2$) between the semiconductor and the conductive layers. In the semiconductor, light intensity decays exponentially as it is absorbed in the film, while generating free charge carriers that improve conductivity. Therefore, it is referred to simply as a *photoresistor*.

of these diodes around a nominal bias point. Therefore, the photodetector can be treated as a network of three serially-connected resistors, as shown in Fig. 5.2(b).

$R'_{\rm a}$ and $R'_{\rm b}$ stand for the equivalent resistance, in $\Omega\,{\rm cm}^2$, of the junction between the semiconductor and the TCO and the junction between the semiconductor and the metal, respectively. The resistance of the bulk semiconductor decreases with the intensity of the illumination, Φ_0, because the absorbed light generates free charge carriers. This layer can therefore be referred to as a *photoresistor*. If a constant voltage, $V_{\rm ab}$, is applied to the three-resistor network, the current density, J, will increase with increasing Φ_0.

5.1.2 Kirchhoff's Law and Electric Field

Kirchhoff's voltage law for the three-resistor network can be written as

$$V_{\rm ab} = J\cdot(R'_{\rm a}+R'_{\rm b}) + V(0) - V(\ell) = J\cdot(R'_{\rm a}+R'_{\rm b}) + \int_0^\ell E(z)dz, \tag{5.1}$$

where E is the electric-field profile of the photoresistor. It depends on V, the potential inside the photoresistor, in the following way:

$$E(z) = -\frac{dV(z)}{dz}. \tag{5.2}$$

At each point along the z axis, E can be presented as a sum of its average value, $E_{\rm ext}$, and a local perturbation, $E_{\rm int}$, i.e.,

$$E(z) = E_{\rm ext} + E_{\rm int}(z), \tag{5.3}$$

where

$$E_{\rm ext} = \frac{1}{\ell}\int_0^\ell E(z)dz, \tag{5.4}$$

and

$$\int_0^{\ell} E_{\text{int}}(z)dz = 0. \tag{5.5}$$

Consequently, (5.1) may be rewritten as

$$V_{\text{ab}} = J \cdot ({R'}_{\text{a}} + {R'}_{\text{b}}) + \ell \cdot E_{\text{ext}}. \tag{5.6}$$

The total electric field in the semiconductor is a result of two factors: (i) the external applied voltage; and (ii) local differences in the concentration of charge carriers, which arise partly because charge particles travel with different mobilities. E_{ext} comes from the former factor, and E_{int} comes from the latter one. In general, the internal field is expected to be much smaller than the external one and, therefore, is often neglected in hand calculations [165]. Later, the expressions for both fields are developed according to semiconductor physics and the problem is solved both analytically and numerically. For the analytical solution only E_{ext} is considered, and for the numerical solution E_{int} is also calculated. The simulation results show that E_{int} can indeed be neglected. Nonetheless, the approach we take to solve for E_{ext} and E_{int}, e.g., using Kirchhoff's voltage law as a boundary condition, is different from the literature.

5.1.3 Charge Carrier Equations

Several processes occur simultaneously in the light-sensitive semiconductor. During their lifetime between generation and recombination, free charge carriers are subject to electric field, which drifts them to the contacts, and diffusion that forces them to overcome differences in concentration. To fully determine the steady state of the semiconductor layer under different conditions, one needs to solve a set of simultaneous equations. This set includes Poisson's equation, i.e.,

$$\frac{dE(z)}{dz} = \frac{q}{\epsilon}\left(p(z) - n(z) + N_{\text{D}}^{+}(z) - N_{\text{A}}^{-}(z)\right), \tag{5.7}$$

and the continuity equations for holes and electrons, i.e.,

$$\frac{dJ_{\text{p}}(z)}{dz} = q\left(g(z) - r(z)\right), \tag{5.8}$$

$$\frac{dJ_{\text{n}}(z)}{dz} = -q\left(g(z) - r(z)\right), \tag{5.9}$$

where $\epsilon = \epsilon_0\epsilon_{\text{r}}$ is the dielectric constant of the semiconductor, q is the fundamental charge, p and n are the concentrations of holes and electrons, respectively, N_{D}^{+} and N_{A}^{-} are the densities of ionized donors and acceptors, respectively, and g and r are the generation and recombination rates of charge carriers in the semiconductor. The hole and electron current densities, J_{p} and J_{n}, are given by the drift-diffusion equations, i.e.,

$$J_{\text{p}}(z) = q\mu_{\text{p}}p(z)E(z) - qD_{\text{p}}\frac{dp(z)}{dz}, \tag{5.10}$$

$$J_{\text{n}}(z) = q\mu_{\text{n}}n(z)E(z) + qD_{\text{n}}\frac{dn(z)}{dz}, \tag{5.11}$$

where μ_{p} and μ_{n} are hole and electron mobilities in the semiconductor, and D_{p} and D_{n} are the corresponding diffusion coefficients.

Considering only direct recombination at this stage, we have

$$r(z) = \alpha_{\mathrm{r}} p(z) n(z), \tag{5.12}$$

where α_{r} is the bimolecular recombination coefficient. The generation includes both an optical generation process, g_{opt}, and a thermal generation process, g_{th}. The overall generation rate is given by

$$g(z) = g_{\mathrm{opt}}(z) + g_{\mathrm{th}}(z) = \int_0^\infty \alpha(\lambda)\Phi_0(\lambda)T(\lambda)e^{-\alpha(\lambda)z}d\lambda + \alpha_{\mathrm{r}} p_0 n_0, \tag{5.13}$$

where p_0 and n_0 are the hole and electron concentrations in the dark, respectively, α is the absorption coefficient of the semiconductor at wavelength λ, and T is the transmission factor. Reflections from the metal contact are ignored for simplicity. For monochromatic light, (5.13) reduces to

$$g(z) = \alpha\Phi_0 T e^{-\alpha z} + \alpha_r p_0 n_0, \tag{5.14}$$

where $\Phi_0(\lambda)$ and Φ_0 in (5.13) and (5.14) have different units ($\mathrm{cm}^{-2}\,\mathrm{s}^{-1}\mathrm{nm}^{-1}$ and $\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, respectively).

5.1.4 Photodetector Optimization

Chapter 2 concluded that the two most-limiting factors with image sensors fabricated by planar technologies are the dynamic range (DR) and the DL. While high DR can be achieved with logarithmic circuits, as demonstrated in Chapter 3 with the VI-CMOS prototype, the photodetector can be optimized for low DL.

The logarithmic response is given by [89]:

$$y = a + b\ln(c + x) + \epsilon, \tag{5.15}$$

where y is the digital response of a pixel to luminance x, where a, b, and c are temporally-constant spatially-varying parameters, and where ϵ is temporally-varying noise with spatially-constant statistics. The signal-to-noise and distortion ratio (SNDR) is defined as

$$SNDR = \frac{x}{\sigma_x} = \frac{x}{dx/dy \cdot \sigma_y} = \frac{x}{\sigma_\epsilon} \cdot \frac{dy}{dx}, \tag{5.16}$$

where σ_x is the RMS value of the noise in the scene, and $\sigma_y = \sigma_\epsilon$ is the RMS value of the noise in the pixel output, which can be considered as constant and independent of x. By including the derivative of y with respect to x, the SNDR may be written as

$$SNDR = \frac{x}{c + x} \cdot \frac{b}{\sigma_\epsilon}. \tag{5.17}$$

When $x \gg c$, the SNDR is b/σ_ϵ, and when $x \ll c$, the SNDR is 0. A general shape of the SNDR of a logarithmic pixel is shown in Fig. 5.3. The luminance level of unity (or $0\,\mathrm{dB}$) SNDR is represented by x_0, which may be written as

$$x_0 = \frac{c}{b/\sigma_\epsilon - 1}. \tag{5.18}$$

The relation between the pixel photocurrent, I_{p}, and the scene luminance is given by

$$I_{\mathrm{p}} = Gx, \tag{5.19}$$

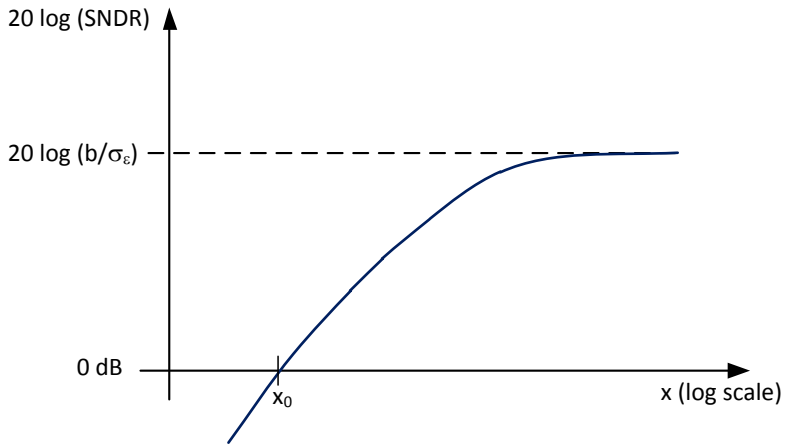


Figure 5.3: The general shape of the SNDR of a logarithmic pixel. Peak SNDR is achieved when $x \gg c$, and equals b/σ_ϵ. The luminance x_0, at which the SNDR is $0\,\mathrm{dB}$, is the dark limit.

where G is a conversion factor that is affected by the opening aperture and transmission of the lens, and by the quantum efficiency and area of the photodetector. The photocurrent at unity SNDR, I_{p0}, is

$$I_{\mathrm{p0}} = Gx_0 = G\frac{c}{b/\sigma_\epsilon - 1}. \tag{5.20}$$

Joseph and Collins [89] show that $c = I_{\mathrm{dk}}/G$, where I_{dk} is the pixel dark current. The ratio between I_{p0} and I_{dk} is constant and equals

$$\beta = \frac{I_{\mathrm{p0}}}{I_{\mathrm{dk}}} = \frac{J_{\mathrm{p0}}}{J_{\mathrm{dk}}} = \frac{1}{b/\sigma_\epsilon - 1}, \tag{5.21}$$

where J_{p0} and J_{dk} are the current densities at x_0 and in the dark, respectively.

Chapter 2 showed that the peak SNDR of the human eye is $36\,\mathrm{dB}$. Therefore, a $40\,\mathrm{dB}$ peak SNDR is sufficient for an image sensor to rival the human eye on this parameter and, in this case, $b/\sigma_\epsilon = 100$. The optimal thickness for the photodetector, ℓ_{opt}, is defined as the thickness for which a minimum value for I_{p0} is obtained, i.e., when $\beta = 1/99$.

5.2 Mathematical Method

The solution process is based on the mean values of the different variables in the semiconductor, and on the deviation of the local quantity from its mean value, which is similar to the way the electric field was treated in Section 5.1.2.

5.2.1 Excess Charge Carriers

The local concentration of either holes or electrons can be presented as a summation of its concentration in the dark, p_0 or n_0, and the concentration of excess charge carriers, δp or δn, due to light absorption, i.e.,

$$p(z) = p_0 + \delta p(z), \tag{5.22}$$

$$n(z) = n_0 + \delta n(z). \tag{5.23}$$

Furthermore, the excess charge carriers can be presented as a sum of an average value, $\overline{\delta p}$ and $\overline{\delta n}$, and a local perturbation, γ_{p} and γ_{n}, for holes and electrons, respectively, i.e.,

$$\delta p(z) = \overline{\delta p} + \gamma_{\mathrm{p}}(z), \tag{5.24}$$

$$\delta n(z) = \overline{\delta n} + \gamma_{\mathrm{n}}(z), \tag{5.25}$$

where

$$\overline{\delta p} = \frac{1}{\ell}\int_0^{\ell} \delta p(z)dz, \tag{5.26}$$

$$\overline{\delta n} = \frac{1}{\ell}\int_0^{\ell} \delta n(z)dz, \tag{5.27}$$

and

$$\int_0^{\ell} \gamma_{\mathrm{p}}(z)dz = 0, \tag{5.28}$$

$$\int_0^{\ell} \gamma_{\mathrm{n}}(z)dz = 0. \tag{5.29}$$

Consequently, one can derive the following:

$$\overline{p} = \frac{1}{\ell}\int_0^{\ell} p(z)dz = p_0 + \overline{\delta p}, \tag{5.30}$$

$$\overline{n} = \frac{1}{\ell}\int_0^{\ell} n(z)dz = n_0 + \overline{\delta n}, \tag{5.31}$$

which leads to the formulations:

$$p(z) = \overline{p} + \gamma_{\mathrm{p}}(z), \tag{5.32}$$

$$n(z) = \overline{n} + \gamma_{\mathrm{n}}(z). \tag{5.33}$$

While hole and electron concentrations are typically expressed as in (5.22) and (5.23), we have reformulated them in terms of local perturbations because we found that it simplifies analysis and proves more robust numerically.

5.2.2 Conductivity and Current Density

The local conductivity of the semiconductor, σ, is given by

$$\sigma(z) = q\left(\mu_{\mathrm{p}} p(z) + \mu_{\mathrm{n}} n(z)\right). \tag{5.34}$$

Therefore, its mean value, $\overline{\sigma}$, can be written as

$$\overline{\sigma} = \frac{1}{\ell}\int_0^{\ell} \sigma(z)dz = q(\mu_{\mathrm{p}}\overline{p} + \mu_{\mathrm{n}}\overline{n}). \tag{5.35}$$

Furthermore, $\overline{\sigma}$ may be expressed as a sum of the dark conductivity, σ_{dk}, and the mean value, $\overline{\sigma}_{\mathrm{ph}}$, of the change in conductivity when the photoresistor is illuminated ($\Phi_0 > 0$), i.e.,

$$\overline{\sigma} = \sigma_{\mathrm{dk}} + \overline{\sigma}_{\mathrm{ph}}, \tag{5.36}$$

where

$$\sigma_{\rm dk} = q(\mu_{\rm p} p_0 + \mu_{\rm n} n_0), \tag{5.37}$$

and

$$\overline{\sigma}_{\rm ph} = q(\mu_{\rm p}\overline{\delta p} + \mu_{\rm n}\overline{\delta n}). \tag{5.38}$$

According to Kirchhoff's current law, the current inside the semiconductor must be constant for all z and must equal J. Since this current density is composed of hole and electron contributions, i.e., $J_{\rm p}$ and $J_{\rm n}$, one can write

$$J_{\rm p}(z) + J_{\rm n}(z) = J. \tag{5.39}$$

Therefore, J may be expressed as a mean value, i.e.,

$$J = \frac{1}{\ell}\int_0^{\ell} (J_{\rm p}(z) + J_{\rm n}(z))dz. \tag{5.40}$$

By applying (5.10) to (5.40), one can rewrite J as

$$J = J_{\rm ext} + J_{\rm int}, \tag{5.41}$$

where

$$J_{\rm ext} = \overline{\sigma} E_{\rm ext}, \tag{5.42}$$

and

$$J_{\rm int} = \frac{q}{\ell}\int_0^{\ell} \left\{ \big(\mu_{\rm p}\gamma_{\rm p}(z) + \mu_{\rm n}\gamma_{\rm n}(z)\big) E_{\rm int}(z) - D_{\rm p}\frac{d\gamma_{\rm p}(z)}{dz} + D_{\rm n}\frac{d\gamma_{\rm n}(z)}{dz} \right\} dz \tag{5.43}$$

or

$$J_{\rm int} = \frac{q}{\ell}\left\{ \int_0^{\ell} \big(\mu_{\rm p}\gamma_{\rm p}(z) + \mu_{\rm n}\gamma_{\rm n}(z)\big) E_{\rm int}(z)dz - D_{\rm p}\big(\gamma_{\rm p}(\ell) - \gamma_{\rm p}(0)\big) + D_{\rm n}\big(\gamma_{\rm n}(\ell) - \gamma_{\rm n}(0)\big) \right\}. \tag{5.44}$$

By applying (5.41) and (5.42) to (5.6), i.e., Kirchhoff's voltage law in Fig. 5.2(b), J can be written as

$$J = \frac{V_{\rm ab} + J_{\rm int}\cdot \ell/\overline{\sigma}}{R'_{\rm a} + R'_{\rm b} + \ell/\overline{\sigma}}, \tag{5.45}$$

where $\ell/\overline{\sigma}$ is basically the scaled resistance of the photoresistor. One can conclude from (5.45) that the system actually has two voltage sources. The first is the applied voltage, $V_{\rm ab}$, and the second is a voltage developed due to optical excitation of the semiconductor, i.e., $J_{\rm int}\cdot \ell/\overline{\sigma}$.

5.2.3 Boundary Conditions

To solve the system of charge carrier equations, which was presented in Section 5.1.3, one has to provide appropriate boundary conditions. In the literature, boundary conditions are often defined in terms of the concentration of charge carriers and current densities on the boundaries, such as in the works done by De Mari [166] and Gummel [167]. We found these boundary conditions did not work for our photodetector model and so developed new ones that not only work but also have a simpler interpretation.

The first boundary condition, presented in integral form in (5.1), is Kirchhoff's voltage law. It incorporates the applied voltage, V_{ab}. The second boundary condition is charge neutrality. The material is initially neutral, and each generation or recombination process involves two particles: a hole and an electron. Therefore, the sum of excess charge carriers in the semiconductor must be zero, i.e.,

$$\int_0^\ell \left(\delta p(z) - \delta n(z)\right) dz = 0. \tag{5.46}$$

Since $p_0 = N_{\mathrm{A}}^-$ and $n_0 = N_{\mathrm{D}}^+$, (5.7) reduces to

$$\frac{dE_{\mathrm{int}}(z)}{dz} = \frac{q}{\epsilon}\left(\delta p(z) - \delta n(z)\right), \tag{5.47}$$

and so charge neutrality implies

$$E_{\mathrm{int}}(0) = E_{\mathrm{int}}(\ell). \tag{5.48}$$

Considering (5.24) to (5.29), charge neutrality also implies

$$\overline{\delta p} = \overline{\delta n}, \tag{5.49}$$

which means (5.47) can be reduced to

$$\frac{dE_{\mathrm{int}}(z)}{dz} = \frac{q}{\epsilon}\left(\gamma_{\mathrm{p}}(z) - \gamma_{\mathrm{n}}(z)\right). \tag{5.50}$$

For a more complex recombination process, (5.46) becomes more complicated (for example, it might include trapped charge carriers). However, the overall charge neutrality must be maintained.

The third boundary condition is generation-recombination balance. In the steady state, every electron-hole pair generation must be offset by an electron-hole pair recombination. This is achieved by the condition

$$\int_0^\ell \left(g(z) - r(z)\right) dz = 0. \tag{5.51}$$

Considering (5.12), (5.14), and (5.30) to (5.33), generation-recombination balance implies

$$\int_0^\ell \left\{\alpha\Phi_0 T e^{-\alpha z} + \alpha_{\mathrm{r}} p_0 n_0 - \alpha_{\mathrm{r}}\left(p_0 + \overline{\delta p} + \gamma_{\mathrm{p}}(z)\right)\cdot\left(n_0 + \overline{\delta n} + \gamma_{\mathrm{n}}(z)\right)\right\} dz = 0. \tag{5.52}$$

When (5.49) is used, (5.52) can be rewritten in the following way:

$$\alpha_{\mathrm{r}}\overline{\delta n}^{\,2} + \alpha_{\mathrm{r}}(p_0 + n_0)\overline{\delta n} - \frac{\Phi_0 T(1 - e^{-\alpha\ell})}{\ell} + \frac{\alpha_{\mathrm{r}}}{\ell}\int_0^\ell \gamma_{\mathrm{p}}(z)\gamma_{\mathrm{n}}(z) dz = 0. \tag{5.53}$$

If $\gamma_{\mathrm{p}}(z)$ and $\gamma_{\mathrm{n}}(z)$ are known, (5.53) becomes a quadratic equation, from which $\overline{\delta n}$ can be derived. E_{int} can then be obtained from (5.5) and (5.50), J_{int} is deducible from (5.44), and so on for the rest of the variables.

5.3 Optimization of Thickness

This section presents the analytical and numerical solutions that were derived from the photodetector model. Comparison of results indicates that the error of the incomplete analytical solution is very small. The section also presents simulation results performed to find the optimal thickness, and experimental results that were obtained with two VI-CMOS image sensor prototypes.

5.3.1 Analytical and Numerical Solutions

For the analytical solution, it is assumed that the concentration of charge carriers in the semiconductor is uniform along the z axis, or in other words there is no perturbation, i.e., $\gamma_{\mathrm{p}} = \gamma_{\mathrm{n}} = 0$. In this case (5.53) has a single unknown, $\overline{\delta n}$, and E_{int} and J_{int} both vanish. In the dark ($\Phi_0 = 0$) there are no excess charge carriers and so $\overline{\delta n} = 0$ by (5.53), which means $\overline{\sigma}_{\mathrm{ph}} = 0$ and the current density is given by

$$J_{\mathrm{dk}} = J(\Phi_0 = 0) = \frac{V_{\mathrm{ab}}}{R'_{\mathrm{a}} + R'_{\mathrm{b}} + \ell/\sigma_{\mathrm{dk}}}. \tag{5.54}$$

The photocurrent is defined as the difference between the current under illumination and the current in the dark, i.e.,

$$J_{\mathrm{ph}} = J - J_{\mathrm{dk}}. \tag{5.55}$$

If all material parameters and operating conditions are given, $\overline{\sigma}_{\mathrm{ph}}$ and J can be readily calculated for any $\Phi_0 > 0$, and one can finally calculate the contrast, β, as defined in (5.21).

A numerical solution was also developed based on a finite-differences method [168]. It calculates γ_{p} and γ_{n} in an iterative way. The numerical solution is initialized with the quantities of the different variables when γ_{p} and γ_{n} are taken to be zero, i.e., the analytical solution. The overall results of the numerical solution are very similar to those that are obtained by the analytical one, which shows that the latter is very good. However, the numerical solution also allows calculation of the perturbation in the charge carrier concentrations, γ_{p} and γ_{n}, as well as the internal field, E_{int}, and the internal current density, J_{int}.

5.3.2 Shockley-Read-Hall Recombination

In a-Si:H films, which were used in the VI-CMOS prototype, the recombination is dominated by the Shockley-Read-Hall (SRH) process. To improve the simulation, this recombination mechanism needed to be included in the photodetector model. Although the actual SRH recombination process in a-Si:H is best described by a multi-level trap model, we use a simplified single-level trap SRH mechanism as presented by Sakata *et al.* [169]. The rest of the solution process proceeds in a manner similar to that already described for direct recombination. With SRH, instead of (5.12), the recombination rate of the free charge carriers is given by

$$r(z) = \alpha_{\mathrm{r}} p(z) n(z) + \frac{p(z)n(z) - n_{\mathrm{i}}^2}{\tau_{\mathrm{p}}\left(n(z) + n_{\mathrm{i}}\right) + \tau_{\mathrm{n}}\left(p(z) + n_{\mathrm{i}}\right)}, \tag{5.56}$$

where τ_{p} and τ_{n} are the recombination lifetimes of holes and electrons, respectively, and n_{i} is the intrinsic carrier concentration ($n_{\mathrm{i}}^2 = p_0 n_0$).

Table 5.1: Operating conditions and material parameters used for the simulation.

Constant	Symbol	Value	Units
applied voltage	V_{ab}	1.5	V
photon flux	Φ_0	$1.23 \cdot 10^{15}$	$\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$
wavelength	λ	555	nm
light transmission factor	T	0.1	
scaled contact resistances	R'_{a}, R'_{b}	10	$\Omega\,\mathrm{cm}^2$
a-Si:H absorption coefficient @ 555 nm	α	10^5	cm^{-1}
a-Si:H bimolecular recombination coefficient	α_{r}	$5 \cdot 10^{-10}$	$\mathrm{cm}^3\,\mathrm{s}^{-1}$
a-Si:H dielectric constant	ϵ_{r}	8	
a-Si:H carrier concentrations	n_{i}, n_0, p_0	$6.26 \cdot 10^7$	cm^{-3}
a-Si:H carrier mobilities	μ_{n}, μ_{p}	10, 1	$\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$
a-Si:H diffusion coefficients	D_{n}, D_{p}	0.26, 0.026	$\mathrm{cm}^2\,\mathrm{s}^{-1}$
a-Si:H recombination lifetimes	τ_{n}, τ_{p}	$4 \cdot 10^{-8}$, $3 \cdot 10^{-7}$	s
lens f-number	$f_{\#}$	2.6	

5.3.3 Simulation Results

Simulations were performed with material parameters of an intrinsic hydrogenated amorphous-silicon (a-Si:H) film deposited by plasma-enhanced chemical-vapor-deposition (PECVD). Operating conditions and material parameters are given in Table 5.1. The incident light was assumed to be monochromatic with $\lambda = 555\,\mathrm{nm}$ (green light). This wavelength represents the point where the photopic (color) vision of the human eye has maximum sensitivity, and it allows easy relation of Φ_0 to units commonly used to specify image-plane illuminance and scene luminance.

The photodetector model was developed according to a system of seven equations taken from principles of electromagnetics and charge transport in semiconductors. The analytical solution satisfies all the equations except for the continuity equation, whereas the numerical solution is a complete solution, which satisfies all the equations. This is indicated in Table 5.2. The analytical solution does not satisfy the continuity equation because it includes a derivative of the perturbation. Perturbation is zero with the analytical solution. This is demonstrated in Fig. 5.4(a) and (b).

A profile of the perturbation in the bulk concentration of charge carriers is presented in Fig. 5.4(c), and the internal electric field, which is developed because of these perturbations, is shown in Fig. 5.4(d). These quantities were calculated by the iterative numerical method for a $0.5\,\mu\mathrm{m}$ thick a-Si:H layer. The mean value of the free charge carriers for these conditions is $\overline{\delta n} = 8.3176 \cdot 10^{11}\,\mathrm{cm}^{-3}$, and the external field is $E_{\mathrm{ext}} = 1.8911 \cdot 10^4\,\mathrm{V/cm}$. Therefore, $\gamma_{\mathrm{p}}, \gamma_{\mathrm{n}} \ll \overline{\delta n}$ and $E_{\mathrm{int}} \ll E_{\mathrm{ext}}$. This confirms that the analytical solution, although incomplete, is comparable to the numerical one.

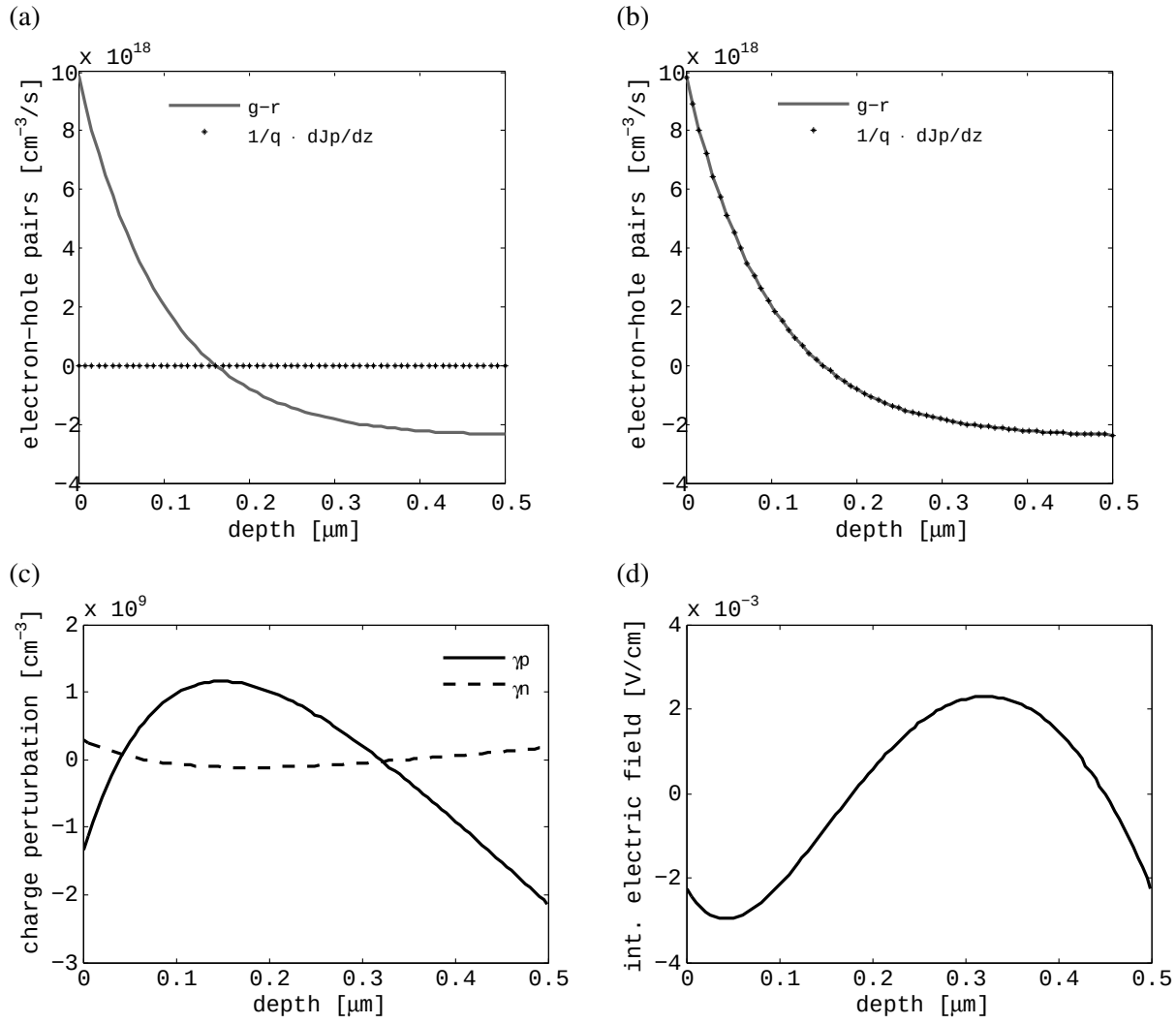


Figure 5.4: The continuity equation is not satisfied by (a) the analytical solution, but is satisfied by (b) the numerical one. (c) The profile of the perturbation in the concentration of free charge carriers. (d) The profile of the internal electric field, E_{int}. Both (c) and (d) are calculated for a photodetector with a $0.5\,\mu\text{m}$ thick a-Si:H layer, and image-plane illuminance of $3000\,\text{lux}$. The rest of the operating conditions and material parameters are given in Table 5.1.

Table 5.2: A comparison between the analytical and the numerical solutions shows that the continuity equation is the only one not satisfied by the analytical solution.

Eq.	Description	Analytical	Numerical
(5.7)	Poisson's equation	yes	yes
(5.8), (5.9)	Continuity equations	no	yes
(5.10), (5.11)	Drift-diffusion equations	yes	yes
(5.1)	Kirchhoff's voltage law	yes	yes
(5.40)	Kirchhoff's current law	yes	yes
(5.46)	Charge neutrality	yes	yes
(5.51),	Generation-recombination balance	yes	yes

Fig. 5.5 shows the mean conductivity, $\overline{\sigma}$, of the a-Si:H layer versus illuminance. The calculation was performed for a $0.5\,\mu\mathrm{m}$ thick photoresistor. The actual conductivities for the range where $\overline{\sigma}$ increases linearly with the illuminance (above $1\,\mathrm{lux}$) are expected to be lower because, in a-Si:H, most excess charge carriers are trapped in the bulk [170] and, therefore, do not contribute to the photoconductivity. A better approximation is expected once the multi-level trap model is incorporated into the recombination process. This agrees with experimental results obtained with Micralyne a-Si:H films that were presented in Chapter 3.

A plot of the DL versus length is shown in Fig. 5.6(a). The DL is expressed in $\mathrm{cd/m^2}$ as results were referred to the scene assuming a lens with f-number as given in Table 5.1. Simulation results show that the DL is expected to improve as the film becomes thinner. They also show that there is a final limit to the DL. The DL with this type of photodetectors cannot be smaller than $4\text{–}5 \cdot 10^{-3}\,\mathrm{cd/m^2}$.

Although it seems that the a-Si:H film needs to be as thin as possible, the ratio between the photocurrent in a bright scene and the dark current was also evaluated. Simulation results for the contrast ratio, $J_{\mathrm{ph}}/J_{\mathrm{dk}}$, as obtained for illuminance of $3000\,\mathrm{lux}$ (green light) are shown in Fig. 5.6(b). Maximum contrast ratio is obtained for $\ell = 0.4\,\mu\mathrm{m}$. At this thickness, the DL is only two times greater than its minimal theoretical value. Therefore, this thickness is considered here as the recommended one.

5.3.4 Experimental Results

VI-CMOS prototypes and the digital camera that was developed to test them were described in Chapter 3. Two prototypes were characterized. The thickness of the a-Si:H film in the photodetector die was $500\,\mathrm{nm}$ in one of the prototypes and $750\,\mathrm{nm}$ in the other.

Twenty frames were recorded at each luminance while the array was scanned at a frequency of $70\,\mathrm{Hz}$. The average response of the pixels is shown in Fig. 5.6(c). Spatially-varying constants a, b, and c could be extracted from this image data for each prototype.

The SNDR of the two prototypes is shown in Fig. 5.6(d). Results were obtained after fixed-pattern-noise (FPN) correction. The peak SNDR is lower than required. However, it can be significantly improved with on-chip analog-to-digital converters (ADCs). Mahmoodi has demonstrated

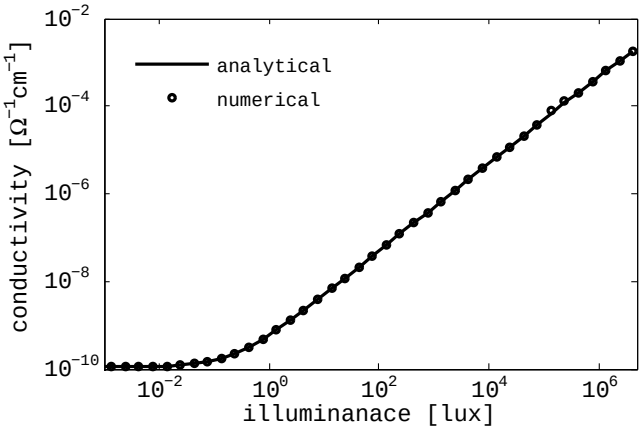


Figure 5.5: The mean conductivity, $\overline{\sigma}$, of an a-Si:H photoresistor versus illuminance, a simulation done for a $0.5\,\mu\mathrm{m}$ thick photoresistor ($\ell = 0.5\,\mu\mathrm{m}$). The illumination is composed of monochromatic light with photon wavelength of $\lambda = 555\,\mathrm{nm}$ (green light). $\overline{\sigma}$ increases linearly with illuminance for levels greater than $1\,\mathrm{lux}$.

peak SNDR of at least $36\,\mathrm{dB}$ with logarithmic CMOS image sensors with pixel-level ADCs [87]. Results show that the prototype with the $500\,\mathrm{nm}$ a-Si:H film has a lower DL than the one with the $750\,\mathrm{nm}$ film. This agrees with simulation results. Moreover, the DL levels are in the same order of magnitude as the values obtained by simulation.

Lastly, it was essential to compare values obtained here theoretically to thicknesses typically used in photodetectors that are based on a-Si:H. We were only interested in designs similar to the configuration given in this work, i.e., where the electric field was parallel to the direction of illumination. Table 5.3 gives details on the thicknesses of different layers for several a-Si:H photodetectors, which were fabricated by different groups worldwide. All the devices were either designed or tested in the visible band.

The processes of generation and transportation of free charge carriers, which are later collected in the contacts, mainly occur in the intrinsic layer. Table 5.3 shows that the thickness of the intrinsic layer used in literature ranges from 0.25 to $2\,\mu\mathrm{m}$. Ng *et al.* [173] are the only ones among the five groups included in the table who reported a trial to reach optimization. They tested films with 600 and $1200\,\mathrm{nm}$ thick intrinsic layers, and concluded that even though the thinner ones had the same density of defects as the thicker ones, the probability of recombination of free charge carriers due to these defects was smaller with the thinner intrinsic layers.

5.4 Conclusion

This chapter presented a new approach to solve the governing equations of charge carriers in a semiconductor. Analytical and numerical solutions have been derived; they are based on different boundary conditions than those found in the literature. The boundary conditions follow simply from Kirchhoff's voltage law, charge neutrality, and generation-recombination balance. Excess charge carrier concentrations are formulated using local perturbation, which leads to efficiencies in the solution process. The approach is applied to optimize the thickness of the light-sensitive semiconductor film in photodetectors for logarithmic VI-CMOS image sensors.

Simulations were performed with film parameters of a-Si:H. They show that the differences

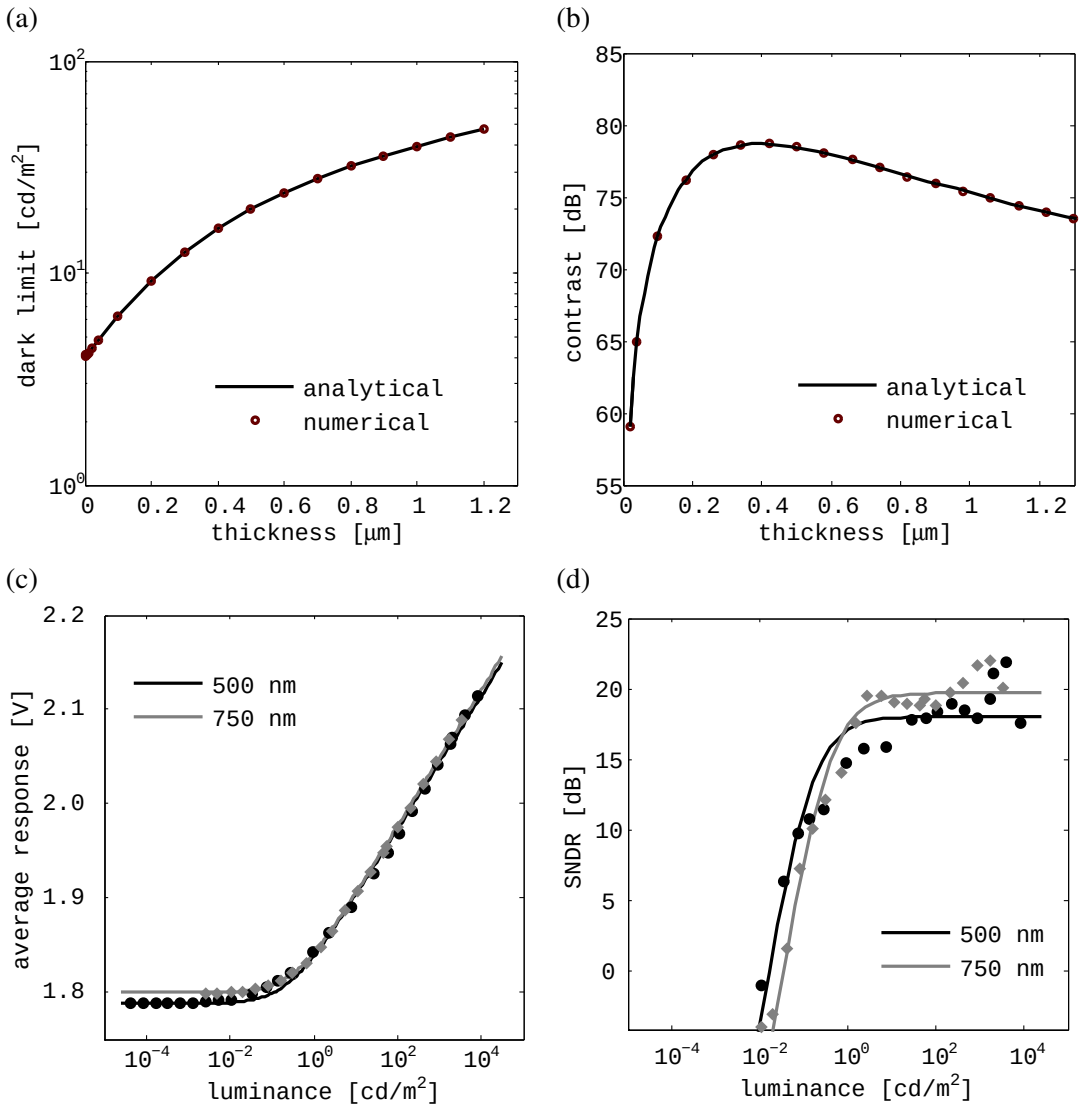


Figure 5.6: (a) Dark limit versus film thickness. (b) Ratio of photocurrent to dark current (contrast ratio) versus thickness. A maximum is obtained at $\ell = 0.4\,\mu\mathrm{m}$. Raw data and best-fit curves of experimental results obtained with two VI-CMOS prototypes having 500 and $750\,\mathrm{nm}$ thick a-Si:H films: (c) the average response of the pixels in the array versus luminance; and (d) the SNDR after FPN correction versus luminance.

Table 5.3: Layer thickness of PECVD a-Si:H in other published works. All devices were used or tested in the visible range. The thickness of the intrinsic layer, which is the most important layer for the conversion of light into electrical signals, ranges between 0.25 and $2\,\mu\mathrm{m}$.

Reference	Device	Thickness of Layers		
		p	i	n
Lulé *et al.* [171]	n-i-p TCO structure deposited on CMOS die for image sensor built in TFA technology	$20\,\mathrm{nm}$	$1350\,\mathrm{nm}$	$30\,\mathrm{nm}$
Hayama [172]	metal i-p TCO structure deposited on glass substrate for detection of light at $570\,\mathrm{nm}$ in stripe-type contact image sensor	$10\,\mathrm{nm}$	$2000\,\mathrm{nm}$	
Ng *et al.* [173]	metal n-i-p TCO structure deposited on polyethylene naphthalate substrate for thin-film-transistor flexible image sensor	$10\,\mathrm{nm}$	$\geq 600\,\mathrm{nm}$	$70\,\mathrm{nm}$
Caputo *et al.* [174]	TCO n-i-p metal structure deposited on glass substrate for detection of light at $514\,\mathrm{nm}$ in chromatography system	$20\,\mathrm{nm}$	$250\,\mathrm{nm}$	$70\,\mathrm{nm}$
Vygranenko *et al.* [175]	metal n-i-p TCO structure deposited on glass and stainless-steel foil substrate for flexible image sensor	$30\,\mathrm{nm}$	$500\,\mathrm{nm}$	$30\,\mathrm{nm}$

between the analytical and numerical solutions are very small, where the continuity equation is the only one not satisfied by the analytical solution. According to simulations, the a-Si:H films need to be as thin as possible to achieve a lower DL, but even with very thin films the DL cannot be smaller than $4\text{–}5 \cdot 10^{-3}\,\mathrm{cd/m^2}$. With very thin films it is more difficult to fulfill the SNDR requirements. Contrast ratio simulations show that it is preferred to work with films that are about $0.4\,\mu\mathrm{m}$ thick. Dark limit levels obtained experimentally with two VI-CMOS prototypes that have 500 and $750\,\mathrm{nm}$ a-Si:H films correlate with simulation results.

Chapter 6

Conclusion

CCD technology, invented in the late 1960s, defines the first generation of electronic image sensors. It was the dominant technology in the market for three decades because it could offer low-noise high-resolution image sensors. CMOS APS technology, which emerged in the 1990s, defines the second generation of electronic image sensors. Its main advantages over CCD include on-chip integration with CMOS circuits, which are essential to improve performance, and a simple power supply, which makes CMOS APS technology more suitable for mobile devices than CCD technology.

Despite significant development in the area of electronic imaging since the early days of CCD, digital cameras do not truly rival the human eye. Performance can be improved by integration of more electronics at pixel-level and by device optimization. However, with CCD technology, although the process is optimized for high quality photodetectors, integration of on-chip electronics is impossible. With CMOS technology, having more pixel-level circuitry either results in impractically large pixels or requires use of a nanoscale CMOS process, where shallow and highly-doped diffusion layers degrade from the imaging performance. Therefore, overall performance of electronic image sensors cannot be substantially improved with planar technologies.

Fabrication of image sensors by vertical integration of dies has been demonstrated since the 1970s with devices that targeted invisible bands. Initially, CCD arrays were used for the readout to form VI-CCD image sensors. They were later replaced by CMOS arrays. The advantages offered by vertical integration make VI-CMOS technology attractive also for the visible band.

The current roadmap of the semiconductor industry introduces a trend that is concerned with technologies for fabrication of 3D ICs. This trend, the "More than Moore" trend, targets microsystems that require heterogeneous integration. There are three technology groups for fabrication of 3D ICs. The 3D IC packaging is based on long-established integration methods, whereas 3D IC integration and 3D Si integration are based on emerging through-substrate-via (TSV) methods. The latter two, which are the only ones included in the "More than Moore" trend are not yet well developed. More needs to be done in the areas of "true-3D" design tools, mass production equipment for TSV devices, and heat dissipation.

With CMOS APS technology, image sensors are heterogeneous microsystems. They are composed of photodetectors, analog circuits, and digital circuits. Technologies for 3D ICs are promising for electronic imaging as they allow device optimization and increased pixel-level functionality, while high spatial resolution can be preserved. The purpose of this thesis is to advance the field of electronic imaging by addressing the limitations of current planar technologies, and by exploiting technologies for vertical integration of active devices. VI-CMOS technology is expected to define a third generation of image sensors. Section 6.1 covers the main contributions of the

thesis, and Section 6.2 discusses ways the work presented here can be extended and used in future applications.

6.1 Contributions

The contributions of this thesis are highlighted in the following sections. Section 6.1.1 discusses a method that can be used by design engineers to evaluate the gap between the performance of an electronic imaging system and that of the human visual system (HVS). This work was published in a journal [176]. Section 6.1.2 discusses a process flow, for fabrication of VI-CMOS image sensors by flip-chip bonding, that was developed with CMC Microsystems. It also presents experimental results obtained from characterization of a VI-CMOS prototype. Part of this work was published as a CMC application note [177], and was later extended into a journal publication [178]. The digital camera that was developed to test the prototype was presented at CMC TEXPO 2010 [179]. Appendix A presents a related work that focuses on preparation of bond pads on custom dies. This work was also published as a CMC application note [180].

The second half of this thesis covered aspects related to design and modeling of circuits and devices for VI-CMOS image sensors. Section 6.1.3 discusses the feedback active pixels. These circuits allow the light-sensitive semiconductor layer in the photodetector array to be left unpatterned, which is benign to the photodetector performance. This work, excluding experimental results, was presented at SPIE/IS&T Electronic Imaging 2010, and published in the conference proceedings [181]. Lastly, Section 6.1.4 discusses a new approach to photodetector modeling, and its use for device optimization. A part of this work was presented at SPIE/IS&T Electronic Imaging 2009, and published in the conference proceedings [182].

6.1.1 Rivaling the Human Eye

Chapter 2 introduced a method to evaluate the gap between the performance of a digital camera and that of the human eye. This is useful for design engineers who try to develop a digital camera to rival the human eye. There are numerous evaluation methods for visible-band digital cameras and image sensors. Franz *et al.* [28], for example, consider the modulation transfer function (MTF) and the signal-to-noise ratio (SNR) as parameters for evaluation, whereas Spivak *et al.* [31] consider SNR, dynamic range (DR), and sensitivity. Janesick [32] treats the SNR as the figure of merit. None of these works use human performance as a benchmark. On the other hand, in the areas of image quality assessment and display technology, systems are always evaluated with regard to the HVS. The method presented in this thesis sets the benchmark for evaluation at the performance of the human eye.

The evaluation considers eight parameters: power consumption (PC), temporal resolution (TR), visual field (VF), spatial resolution (SR), SNR, signal-to-noise and distortion ratio (SNDR), DR, and dark limit (DL). While visual field and spatial resolution relate to geometric properties of the image sensor, i.e., photodetector size and array area, the last four parameters relate to its signal and noise power characteristics. The evaluation process is concluded with a figure of merit, which is taken as the performance gap of the weakest parameter. To rival the human eye truly, a digital camera must equal or surpass the human eye on every parameter.

Experimental work done with observers and cadavers is reviewed to assess the measures for the human eye. Assessment techniques are also covered for digital cameras. Some of the properties for digital cameras can be extracted directly from their documentation, such as power consumption

and temporal resolution, whereas others need to be calculated. To be able to compare between imaging systems of different types, the evaluation is always referred to the scene.

The performance evaluation method was applied to 25 modern image sensors of various types and manufacturers, e.g., CCD and CMOS sensors from both commercial and academic sources, including three sensors based on logarithmic response. Image sensors are considered rather than digital cameras because datasheets of digital cameras are not detailed enough for the evaluation. To ensure that the performance is not limited due to lens imperfections, an ideal lens is assumed to complete a digital camera. Results show that neither of the image sensors included in the survey can be used to rival the human eye. They also indicate that DR and DL are the most limiting factors.

The substantial functional gap between the human eye and digital cameras may arise from architectural differences between the human retina, arranged in a multiple-layer structure, and image sensors, mostly fabricated in planar technologies. Functionality of image sensors is likely to be significantly improved by exploiting technologies that allow vertical stacking of active tiers.

6.1.2 Design and Fabrication

Chapter 3 and Appendix A describe the process flow that was developed with CMC Microsystems for fabrication of VI-CMOS image sensors. They elaborate on general design principles for such microsystems, and then focus on the prototype developed for this thesis.

Flip-chip bonding was the only method for VI microsystems available through CMC when the project was at its design stage. VI-CMOS image sensors prepared by flip-chip bonding are composed of a CMOS die and a photodetector die. While the CMOS die is prepared in a commercialized process, the photodetector die is made in a customized process, which leaves the designer with many degrees of freedom. After fabrication, the two dies are aligned precisely and finally attached with solder bumps.

The CMOS die should include an active pixel array, where each pixel has a bond pad to form an electrical contact with a vertically-integrated photodetector after flip-chip bonding, and flip-chip bond pads that connect to the front contact of the photodetectors. It also requires bond-pads for flip-chip bonding on the periphery to communicate with the external world. The photodetector die includes an array of bond pads on the photodetector array, which are surrounded by bond pads placed on the transparent conductor that makes the front contact of the photodetectors. As a part of the design process of the photodetector dies, one needs to select the substrate material, the transparent conductor, and the light-sensitive semiconductor film. All process steps must be compatible with all materials involved. One also needs to decide about the type of devices used for photodetection, which may include zero to a few junctions.

The VI-CMOS image sensor prototype was designed at the University of Alberta, and fabricated with the help of CMC Microsystems and Micralyne Inc. CMOS dies were prepared in a $0.8\,\mu\mathrm{m}$ DALSA process. They include a 20×24 array of $110\,\mu\mathrm{m}$ pitch active pixels with logarithmic response. Photodetector dies include a borosilicate glass substrate, an ITO transparent electrode, and a PECVD a-Si:H light-sensitive semiconductor. The photodetectors are ITO/a-Si:H/Cr MSM devices. To realize prototypes, the two dies are flip-chip bonded with indium-based (In/Ag) solder bumps.

A PCB with a 16-bit ADC was designed to test the VI-CMOS prototype. Activation of the image sensor and the ADC is accomplished with an Altera Cyclone II FPGA board. A camera body was designed to accommodate the two boards, which are connected to USB ports of a PC for power and real-time data transfer.

The signal-and-noise power properties of the prototype were measured. Its peak SNDR is rather low, 20–25 dB, which is expected as the data conversion is done at board level. Thanks to the logarithmic response, the prototype has high DR, which extends at least 6 decades. Furthermore, its DL is one order of magnitude lower (better) than that of conventional CCD and CMOS image sensors. High SNDR, high DR, and low DL are anticipated if digital pixel sensor (DPS) circuits are used with a microsystem of a similar structure.

To conclude, a general process flow for VI-CMOS image sensors made by flip-chip bonding, and a specific process flow developed for a prototype, were presented. The prototype was tested with a custom digital camera. Characterization results show that it has better DR and DL than conventional image sensors. Performance can be further improved with DPS circuits.

6.1.3 Feedback Active Pixels

Chapter 4 elaborated on the approach of using a feedback mechanism in the CMOS array of a VI-CMOS image sensor. Schneider *et al.* [104] have presented feedback active pixels with a linear response for a VI-CMOS image sensor that was fabricated by thin-film-on-ASIC technology. However, they do not discuss considerations in the design process of the feedback amplifier, including issues related to stability and compensation, which are covered in Chapter 4.

To avoid defect states at photodetector boundaries, which add to the overall noise, it is desirable to leave the light-sensitive semiconductor layer in the photodetector array unpatterned. But without a physical border between adjacent photodetectors, flow of lateral currents results in undesirable crosstalk. Crosstalk can be reduced by maintenance of a constant electric potential at all nodes where the photodetector array connects to the readout circuit array. The feedback mechanism may be implemented using a circuit with an operational amplifier and a negative feedback loop.

With conventional CMOS APS technology, the readout is based on the voltage drop over the photodetector. With the feedback active pixels, the current flowing through the photodetector is sensed as the input signal because the photodetector potential must remain constant. To achieve a high DR, a logarithmic feedback is used in the design presented in this thesis. There are three optional principal configurations for the feedback loop, and the common-drain is the most power efficient one because the feedback is sent to a gate of a transistor and does not draw current from the operational amplifier.

A simplified small-signal model of the pixel circuit is derived to analyze its frequency response. The bias point of the feedback circuit changes with luminance, and it is more susceptible to stability problems as luminance is increased. The feedback pixel circuits of the VI-CMOS prototype oscillate at typical office luminance levels. The chapter elaborates on two methods to improve stability. The first is by adding a compensation capacitor during the design stage, as the amplifier nodes are inaccessible after fabrication. The second is by changing externally-controlled bias voltages. With this method, which was successfully applied to the VI-CMOS prototype, stability is improved at the cost of reduced bandwidth.

To conclude, feedback active pixels can be used to improve performance of photodetectors in VI-CMOS image sensors. However, with these circuits the designer needs to model and simulate the frequency response in order to ensure stability for the full range of expected luminance levels.

6.1.4 Photodetector Thickness

Chapter 5 presented a mathematical model for photodetectors in VI-CMOS image sensors, which are usually fabricated in a custom process. The model is used to find the optimal thickness of the

light-sensitive semiconductor film. Although Gopal and Warrier [163] and Yang *et al.* [164] have presented optimization methods for film thickness in photodetectors, their methods are specific to the materials they used, and cannot be applied in the general case.

The model was developed for a simplified 1D photodetector structure, and the photodetector is treated as a three-resistor network. It is based on principles of electromagnetics and charge transport in semiconductors. The thickness is optimized to achieve low DR in sensors with logarithmic pixels. The typical logarithmic response is used to derive an expression for the optimal thickness. It depends on the ratio between the photocurrent at unity SNDR and the dark current.

The model uses a smaller number of boundary conditions than are usually used with similar semiconductor devices. Nevertheless, the boundary conditions are sufficient to solve the problem without inconsistency. The solution approach is based on mean values of the variables and on the deviation of the local quantity from the mean value. Analytical and numerical solutions have been developed. The analytical solution is based on mean values and does not consider perturbations. The numerical solution is based on the finite differences method, and uses an iterative process to solve the problem. It provides a consistent and complete solution. Nonetheless, the analytical and the numerical solutions are shown to be comparable.

Properties of a-Si:H are used for the simulation. Simulation results show that the DL improves as the thickness of the film is reduced. However, even with very thin films, the DL cannot be smaller than $4\text{–}5 \cdot 10^{-3}\,\mathrm{cd/m^2}$. Having layers too thin makes it difficult, if not impossible, to meet the minimum SNDR requirements, as the signal is very weak. One may conclude from simulation of contrast ratio that the optimal thickness is $0.4\,\mu\mathrm{m}$. At this thickness, the DL is greater only by a factor of 2 than the theoretical minimum.

Experimental results of the average response and the SNDR as obtained with two VI-CMOS prototypes that have 500 and $750\,\mathrm{nm}$ a-Si:H films are presented. The DL levels agree with values obtained by simulation. Survey of other works with a-Si:H photodetectors shows that the thicknesses discussed in this part of the work are within the range of values used by others. The survey also concludes that this parameter is often not optimized.

To conclude, a mathematical model for photodetectors in VI-CMOS image sensors has been developed. It is used for thickness optimization of the light-sensitive semiconductor to achieve low DL in sensors with logarithmic response. DL values obtained experimentally with two prototypes agree with simulations.

6.2 Future Work

The work presented in this thesis can be extended in different directions; several options are discussed in the following sections. Crosstalk can be further investigated by including electromagnetic simulations to model lateral currents in the photodetector arrays. A more comprehensive experimental work can be done to verify results obtained from photodetector modeling. An improved version of the VI-CMOS prototype should include DPS pixels. Technologies for fine pitch vertical-integration may be explored, and the photodetectors can be designed to target invisible bands.

6.2.1 Crosstalk Modeling

Chapter 4 presented the feedback active pixel. Its design methodology strives to improve performance of photodetectors and, mainly, to lower their dark noise, by leaving the light-sensitive semiconductor layer in the photodetector array unpatterned. The chapter describes the operating

principle of these circuits, and also covers optional design configurations and issues related to stability and compensation.

The 1D photodetector model presented in Chapter 5 may be extended into a 2D or, preferably, a 3D model of the photodetector array. The availability of a comprehensive electromagnetic simulation of the array can assist in testing the effectiveness of the feedback circuits in reducing crosstalk. Moreover, this model can also be used to define specifications for the feedback amplifier, such as maximum offset voltage and minimum photodetector voltage.

Transport of charge carriers in the light-sensitive semiconductor is affected by drift and diffusion. The model can be used to ensure that even in situations where there are very large differences between illuminance levels of two adjacent pixels, i.e., when diffusion currents are relatively high, the signal power of the lateral currents due to drift and diffusion does not affect performance. Therefore, one may use the model to define conditions that guarantee that crosstalk can never cause the SNDR to drop below $40\,\mathrm{dB}$, a value that is slightly above the $36\,\mathrm{dB}$ benchmark set by the human eye. In this case, the overall lateral current at each pixel needs to be at least 100 times smaller than the vertical current.

6.2.2 Photodetector Optimization

Chapter 5 presented a mathematical model for photodetectors in VI-CMOS image sensors. The model was used to find the optimal thickness of the light-sensitive semiconductor layer in sensors with logarithmic response, such as the VI-CMOS prototype. This work can be extended in two directions.

The mathematical model of the photodetector can be extended to treat more complicated structures that include junctions. The recombination model may be improved by adding multiple-trap processes that describe a-Si:H films in a more accurate way. Also, the model used in the simulations assumed monochromatic green light. It may be extended to treat spectrum from black-body radiation, which is a better approximation to natural light sources. However, multiple wavelengths may result in a significant increase in the run time of the simulation, especially with the iterative process that is required for the numerical solution, as the calculation process may need to be repeated multiple times.

Experimental results are presented for two thicknesses of a-Si:H films. Although our initial plan was to test four thicknesses (250, 500, 750, and $1000\,\mathrm{nm}$), while assembling the VI-CMOS prototypes the flip-chip supplier encountered difficulties during the bonding process, which resulted in low yield. However, it is desirable to test more thicknesses to validate results obtained by simulations. More prototypes with a-Si:H photodetectors can be prepared, and the bond pads can be deposited in the facility of the flip-chip supplier, who has a well-developed process for bond pads on non-metallic substrates. Furthermore, testing can be done with materials other than a-Si:H, which are not limited to imaging in the visible band. In this case, recombination processes and material parameters in the mathematical model need to be modified according to the properties of the chosen light-sensitive semiconductor.

6.2.3 X-ray Image Sensors

The spatial resolution of the VI-CMOS image sensor prototype, whose pixel pitch is $110\,\mu\mathrm{m}$, is too low for conventional digital cameras, where light is diffracted by a system of lenses to form a demagnified image of the scene on the image plane. However, this was the smallest pitch available through CMC for a microsystem of this nature when the project was at its design stage. Although

a similar microsystem could be fabricated through CMC today with pitch that is half the size used for the prototype, it remains too large for conventional digital cameras.

Nevertheless, VI-CMOS image sensors may be fabricated with smaller pitch to allow conventional imaging systems to benefit from the advantages offered by VI technologies. Teledyne Imaging Sensors, a US company, has demonstrated a VI-CMOS image sensor made by flip-chip bonding with $10\,\mu\mathrm{m}$ pitch [139], which provides adequate spatial resolution for typical digital cameras. FLip-chip bonding aside, CMC offers its users the access to a fine-pitch TSV process, a capability that was partially motivated by this thesis. This process is based only on silicon devices.

Furthermore, there are lens-less imaging applications where pixel pitch of several tens of microns are typical. Examples include X-ray [183] and terahertz (THz) imaging [184], which are both invisible-band applications, and imagers used in lab-on-chip microsystems [185], where imaging is done with visible light.

Flip-chip bonding is a traditional fabrication method for 3D ICs, which is considered a 3D IC packaging technology and is not a part of the "More than Moore" trend. Still, it is a reliable method that is also robust and suitable for hybrid integration. The same CMOS die can be assembled with various types of sensors, which are actually not limited to photodetectors.

The VI-CMOS prototype was shown to have high DR, thanks to the logarithmic response, and low DL, thanks to the vertical integration. However, data conversion that is done at board level results in 20–25 dB peak SNDR after FPN correction algorithms are used. This value is low when compared to other image sensors and to the human eye. Mahmoodi has designed and tested a logarithmic CMOS image sensor with digital pixel circuits [87], which had a peak SNDR of at least $36\,\mathrm{dB}$. Therefore, integration of ADCs on the image sensor chip, preferably at column or pixel level, is necessary to improve the SNDR. High SNDR, which manifests in high image quality, is desirable for any imaging application.

Design principles used for the VI-CMOS prototype can be used with a VI-CMOS image sensor for medical X-ray imaging. In this case, the photodetectors need to be based on materials such as amorphous selenium (a-Se) or cadmium telluride (CdTe), which are direct converters of X-ray photons. Photodetector optimization for low DL and DPS circuits that improve SNDR can allow detection of a small number of X-ray photons. At present, there is an increasing pressure to reduce the amount of ionizing radiation to which both patients and medical staff are exposed during treatments done using X-ray imaging systems [186]. Therefore, an X-ray image sensor with high DR, high SNDR, and low DL is very desirable for medical imaging applications.

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Appendix A

Flip-Chip Bond Pads

The VI-CMOS image sensor prototype is composed of two dies: a die with an array of CMOS circuits that were fabricated on a silicon substrate, and a die with a photodetector array that was prepared on a glass substrate. Flip-chip bonding provides both electrical and mechanical connection between the two. The CMOS die has been fabricated using a standard CMOS process at DALSA. Whereas, the photodetector die has been fabricated using a custom process, involving the University of Alberta Nanofab and also Micralyne. With flip-chip bonding, the two dies are aligned precisely and attached with metallic interconnects.

Cross-sections of the assembled prototype and the photodetector die are shown in Fig. A.1(a) and (b), respectively. Light enters from the back of the flipped photodetector die and travels through the glass before reaching an array of photodetectors. Thinner glass substrates and wider image sensors are possible but the drawing shows relative dimensions of an actual prototype. The photodetectors are based on hydrogenated amorphous silicon (a-Si:H), a semiconductor that is sensitive to visible light. Indium-doped tin oxide (ITO), which is a transparent conductive oxide, forms the common front contact of the photodetectors. The a-Si:H is etched at the periphery of the array to expose the ITO to allow formation of bond pads on this film.

To assemble the prototype, both dies described above required pre-processing for flip-chip bonding. As the CMOS die had been processed in a standard way, it could also be pre-processed in a standard way for flip-chip bonding. Indeed, this task was outsourced by CMC to a third party. However, the photodetector die had been processed in a custom way and, therefore, it was not clear what was the best way to pre-process it for flip-chip bonding.

This appendix begins with general design principles of bond pads for custom dies. It covers deposition methods that can be used for the different layers in the metal stack, and focuses on wet plating. This is followed by presenting the approach used to form the bond pads on the photodetector dies that were prepared for the VI-CMOS image sensor prototype, which was described in Chapter 3.

A.1 Design of Bond Pads

There are several approaches to flip-chip bonding of two dies. Bonding can be done using solder bumps, gold stud bumps, or conductive adhesives (polymer films that contain metallic particles) [187, 188]. This appendix focuses on flip-chip bonding using solder bumps.

Flip-chip bonding of two dies using solder bumps requires pre-processing of both dies, as illustrated in Chapter 3. Under bump metallization (UBM), also called ball-limiting metallurgy (BLM), is required on the bond pads of one die, which may be called “the main die”. This

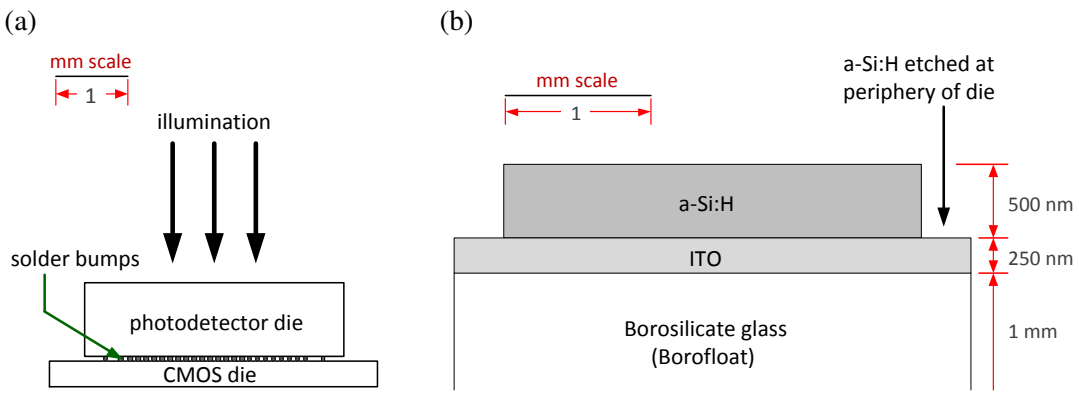

Figure A.1: (a) The VI-CMOS image sensor prototype is composed of a CMOS die and a photodetector die. It is assembled by flip-chip bonding. (b) To prepare the photodetector die, ITO is deposited on a borosilicate glass substrate, and a-Si:H film is deposited on the ITO and then etched from the periphery. To enable flip-chip bonding to the CMOS die, bond pads need to be formed on the a-Si:H and ITO regions.

is followed by the fabrication of solder bumps on the UBM. Top surface metallurgy (TSM) is required on the bond pads of the other die, which is usually called "the substrate". Although this appendix focuses on the UBM, similar principles apply to the TSM.

The quality of the bonding depends on the solder material and the bond pad metallurgy. We describe the soldering process and commonly used solders below. Thereafter, we explain the metallurgical principles essential for proper design of the UBM, focusing on the vertical profile of the bond pads. Horizontal profiles are not discussed here, except to say that the minimum pad footprint and the minimum distance between adjacent pads are specified by the flip-chip bonding supplier.

A.1.1 Solder Material

In soldering, a molten filler wets two mating surfaces in order to form a metallurgical bond [189]. This process must sometimes be preceded by cleaning of the surfaces with flux. Unlike in welding, the parts joined by soldering are expected to remain solid during the bonding process. Therefore, the melting temperature of the filler metal or alloy must be lower than that of the parts to be assembled.

Most of the fillers, or solders, used for flip-chip bonding are tin-based or indium-based alloys [187]. Mixtures of tin or indium with lead are commonly used although, recently, there has been a tendency to minimize or eliminate the lead in solders [190]. Nonetheless, lead-tin solders have superior wetting and spreading characteristics in comparison to most other solders, including indium-based ones. Both tin and lead are relatively cheap metals, and the mechanical properties of lead-tin solders are satisfactory. However, tin-based solders form brittle compounds with copper and gold, which are metals commonly used with semiconductor devices [189]. These compounds may crack, leading to joint failure [187].

Indium-based solders are recommended when bonding substrates coated with gold because the solubility of gold in these solders is much lower than the solubility of gold in lead-tin solders [189]. Furthermore, the formation of a gold-indium alloy suppresses any further reactions between these two metals. The low melting point of solder alloys with high indium composition

makes them suitable for applications where exposure to high temperature is not desired (e.g., when using organic substrates). In addition, lead-indium joints are more susceptible to humidity than lead-tin joints [191]. Therefore, they need to be better protected from the environment to prevent corrosion.

A.1.2 Under Bump Metallization

Bond pads may be designed for metal or nonmetal substrates. Nonmetals, such as semiconductors, ceramics, and polymers, are usually chemically stable. These materials normally do not bond well with molten solder, unless the solder is tailored to react with negatively charged particles, such as oxygen and nitrogen ions, found in the nonmetal substrate or its surface [189]. In general, when standard solders are used, nonmetal substrates must be metallized with UBM, which provides a wettable surface for the solder. Metal substrates that cannot be wetted by the molten solder also require UBM.

Other than having a low resistance, the UBM needs to adhere well to the substrate while providing good wettability to the solder. For nonmetal substrates, which we focus on below, no single metal layer can meet both these requirements. Therefore, the UBM is composed of several metal layers.

Foundation layer

For good adhesion of the UBM to a nonmetal substrate, the foundation (or adhesion) layer, which is in direct contact with the substrate, must be a reactive metal [189]. Reactive metals have a strong affinity to oxygen. They form strong bonds with clean surfaces of nonmetals that contain oxygen or that have surface oxides. Chromium and titanium are successful choices for many substrates.

In choosing the foundation layer, one must also consider diffusion rates of the metal atoms into the nonmetal substrate, and the influence of the former on the latter. For example, iron has a strong affinity to oxygen and, therefore, a good adhesion to nonmetal substrates [192]. However, iron should not be used as a foundation layer for silicon devices. Iron (as well as gold, silver, nickel, and copper) is a middle band-gap dopant in silicon [193]. Such dopants are not desirable because they form trap states in the semiconductor, which increase leakage currents and degrade device performance.

Barrier layer

In some cases, the UBM may require a barrier layer to prevent metallurgical reaction between the foundation layer and the wettable layer. Gold, which is a popular choice for the wettable layer, diffuses into some reactive metals, including chromium [194] and titanium [195], to form intermetallic compounds [196]. Presence of gold in the foundation layer can result in the diffusion of gold atoms into the nonmetal substrate, which may be undesirable (see above). Furthermore, the formation of an alloy between the foundation and wettable layers may decrease the overall wettability of the UBM to solder.

The barrier layer may be either a pure metal or an alloy. Platinum, nickel, copper, titanium-tungsten alloy, and titanium nitride are commonly used for this purpose [189]. The barrier layer must be thick enough to survive flip-chip bonding. It should also block the unwanted diffusion of UBM atoms sufficiently, while maintaining a good conductivity, for the lifetime of the assembled device.

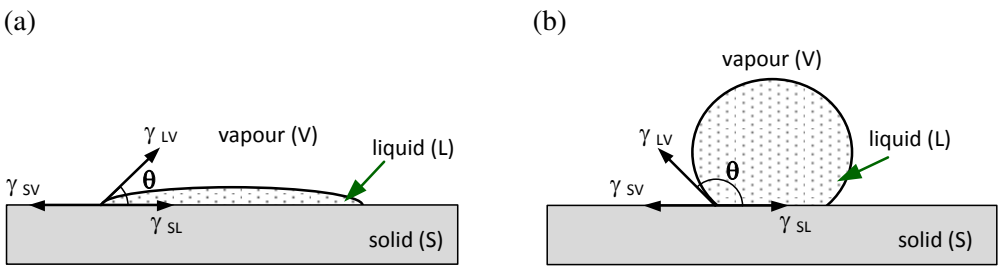

Figure A.2: (a) When $\theta < 90°$, the surface is wetted by the liquid. (b) When $90° < \theta < 180°$, the liquid does not spread on the surface. Formation of a thin oxide layer on a metal surface reduces the surface free energy. The small γ_{SV} forces large θ, and this prevents molten solder from wetting the oxidized surface.

Wetting layer

There are two thermodynamic principles that determine whether the surface of a solid substrate can be wetted by a droplet of liquid solder. They are the Young-Dupre law and the Gibbs function [197].

According to Young-Dupre, a liquid droplet spreads on a solid substrate until three surface tension forces are in balance: the tension γ_{SL} between the solid substrate and the liquid droplet; the tension γ_{LV} between the liquid droplet and the (vapour) atmosphere; and the tension γ_{SV} between the substrate and the atmosphere. The relationship between these forces and the contact angle, θ, is expressed by the Young-Dupre law,

$$\cos\theta = \frac{\gamma_{SV} - \gamma_{SL}}{\gamma_{LV}}, \tag{A.1}$$

which is also known as the wetting equation. When $90° < \theta < 180°$, the liquid does not spread on the surface, although there is contact between the droplet and substrate. When $\theta < 90°$, the liquid spreads on the surface, and the substrate is said to be wetted by the liquid [189]. The two cases are illustrated in Fig. A.2.

Gibbs function implies that when a spontaneous change occurs on a surface, the surface free energy is lowered. Consequently, surface oxidation would decrease γ_{SV} and increase θ, which would reduce the liquid's ability to wet the substrate [197]. For this reason, the reactive metal in the foundation layer of the UBM would lose its wettability once exposed to the atmosphere. To overcome this problem, a more noble metal, which offers good wettability to the solder, must be deposited on the foundation layer. This wettable layer must be sufficiently thick to protect the underlying metal layers from corrosion, and to maintain wettability of the component over a reasonable shelf life prior to soldering [189].

Since gold resists oxidation, it is commonly used as the outermost layer in the UBM for fluxless soldering [197]. Gold can be used as a protective coating to the wettable layer or it can be used as the wettable layer itself. In the first case, a thin gold layer is required, and the solder is a material into which gold quickly dissolves so as to expose the underlying wettable layer to the solder. Materials that are commonly used here are nickel, as the wettable layer underneath the gold, and a tin-based solder, usually lead-tin. In the second case, one desires a very low solubility of gold in the solder material. Indium-based solders, usually lead-indium, are commonly used for this case.

A.2 Fabrication of Bond Pads

Bond pad fabrication can either be done in house, as additional steps to the preparation of custom dies, or be outsourced to an external supplier. With outsourcing, bond pad design remains important, especially for custom dies, and some understanding of fabrication is essential for successful design. Due to our proximity to the University of Alberta Nanofab, it was convenient for us to explore some design choices by fabricating the bond pads ourselves. This experience helped us to understand the engineering principles involved, which have been summarized in this appendix.

There are basically four methods to deposit metal layers on metallic and nonmetallic substrates: physical vapour deposition (PVD), chemical vapour deposition (CVD), wet plating, and thick-film metallization. This section covers only two of the above—PVD and wet plating—because they are the only metal deposition methods currently available at the Nanofab and at CMC.

Although flip-chip bonding is done in this application with dies, it is easier and cheaper to fabricate the bond pads on whole wafers, and to dice them as the last step before the flip-chip bonding.

A.2.1 Physical Vapour Deposition

In PVD, material particles are brought into the vapour phase prior to deposition on a nearby substrate surface. The relatively slow deposition rate of PVD limits its usefulness mainly to thin film fabrication, with thicknesses up to a few hundred nanometers. PVD processes are described here only briefly because these methods are well-covered in micro/nano-fabrication courses at university level.

Evaporation

The material to be deposited is thermally vapourized under high vacuum conditions. Common methods to achieve the vapourization are resistance heating and electron beam bombardment.

Sputtering

A target made of the material to be deposited is bombarded with ions of an inert gas, usually argon. As a result of momentum transfer between the ions and the target, atoms are released from the latter. Sputter guns with magnetrons enhance ion generation close to the target. This increases the deposition rate of atoms on the nearby substrate and, in general, makes the process more efficient.

Using the Lesker magnetron sputtering machines at the University of Alberta Nanofab, we tried to deposit thick films ($500\,\mathrm{nm}$ or more) of aluminum and nickel to serve as metal layers for bond pads. However, the films were of poor quality. The aluminum looked cloudy or white instead of the usual shiny metallic colour, which could be obtained by sputtering thin films instead. As for the nickel, its surface was cracked and it could not be etched by conventional nickel etchants.

We suspect that during a long deposition time, which is required for thick films, the sputter chamber warms up, resulting in excessive outgassing. Gases trapped within surfaces inside the chamber, which is initially at room temperature, may not be pumped out during a pump-down step that is done prior to deposition. As the temperature rises during a long deposition, the gases may obtain enough energy to escape into the chamber while the deposition is proceeding. These

outgassed particles are impurities that would contaminate the deposited films, thereby changing their characteristics.

A.2.2 Wet Plating

In wet plating, a metal layer is deposited by immersion of the substrate in a liquid, which contains the appropriate metallic ions. Electroless plating and electroplating have a relatively high deposition rate, and are therefore suitable for thick film fabrication, with thicknesses up to a few microns. However, control on the thickness of the deposited film is less precise than with PVD.

Wet plating methods, which are discussed below, all use the electrochemical mechanisms of oxidation and reduction. Both reactions involve the transfer of electrons between reacting substances. Oxidation is characterized by a loss of electrons or "de-electronation", while reduction is characterized by a gain of electrons or "electronation" [198]. Electroplating requires an external power source. However, electroless plating and immersion plating do not require any electrical circuitry.

Electroplating

Electroplating uses an electrolytic cell, which consists of two electrodes submerged in a solution that contains ions. A current is passed between the anode and cathode. Unlike electronic circuits, which use electrons to carry a current, the electrolytic cell uses ions to carry a current.

The sample or piece to be plated is connected to the cathode. There are two types of anodes: sacrificial anodes and permanent anodes [198]. Sacrificial anodes are made of the metal to be deposited. They supply the solution with fresh ions of the metal to replace the ions consumed during the plating. Permanent anodes serve only to complete the electrical circuit. In this case, the anode is not consumed during electroplating and the amount of ions in the solution decreases with time.

When a DC current is passed between the electrodes, metal ions in the solution, which are positively charged, are attracted to the sample at the cathode, which is negatively charged. The metal ions absorb electrons from the cathode, undergoing a reduction process that transforms them into metal atoms. These atoms are deposited on the sample surface and, in this manner, form the plated film. Non-uniformity of the current density over the sample leads to non-uniformity in the thickness of the deposited film. Current density is higher at or near the edges and corners of the sample.

To ensure the electroplated metal adheres well to a substrate surface, a good seed layer is required. The seed layer is usually a thin metal layer (100 to $200\,\mathrm{nm}$ thick) that does not oxidize easily. Gold, copper, and nickel are commonly used for this purpose. Fig. A.3 depicts the result of an early electroplating trial. We tried to electroplate nickel onto glass substrates coated with a sputtered layer of chrome. Since chrome oxidizes easily in standard room conditions, it proved unsuitable as a seed layer. The electroplated nickel did not adhere to the substrate surface and could be peeled off easily.

Electroless plating

With electroless plating, or autocatalytic plating, a chemical reducing agent is placed in the solution with ions of the metal to be deposited. The deposition only occurs on catalytic surfaces. Therefore, the deposited metal must itself form a catalytic surface for the deposition process to continue.

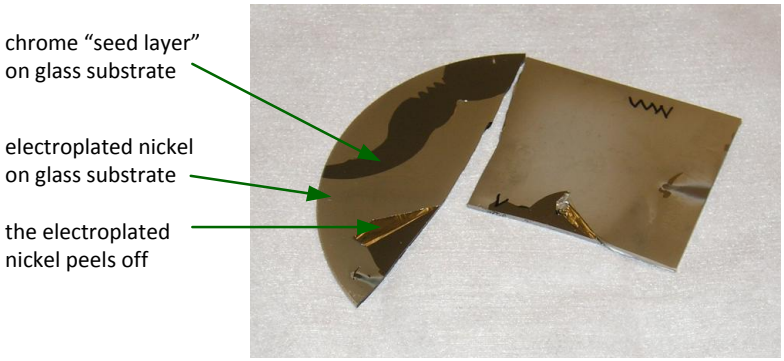

Figure A.3: In an early electroplating trial, we electroplated nickel onto glass substrates that were coated with sputtered chrome. Although the chrome had a good adhesion to the glass, it proved to be an unsuitable seed layer for the electroplated nickel. In the photo, one can see that the nickel layer peels off easily.

In comparison to electroplating, electroless plating may be done on surfaces of non-conductive materials, although the surfaces may need pre-processing to make them catalytic for the reaction. Another advantage of electroless plating is that metal is deposited uniformly. There is no excessive buildup at or near edges and corners. The main disadvantage of electroless plating is that the reducing agents are usually more expensive as electron sources compared to electron currents [198].

Immersion plating

Like electroless plating, immersion plating does not require an external circuit. However, unlike electroless plating, there is no reducing agent in the solution. Instead, metal atoms from the original surface of the immersed sample undergo an oxidation process, which releases them as ions into the solution. These atoms are replaced by other ions in the solution that undergo a reduction process, which deposits them on the sample as metal atoms. The process works only if the metal to be deposited is more noble (i.e., has a lower oxidation potential) than the original metal on the sample surface [199].

A combination of electroless nickel and immersion gold (ENIG) is commonly used to fabricate bond pads for soldering. Surface nickel atoms from the electroless plating are replaced with gold atoms during the immersion plating. Deposition proceeds until a thin layer of gold covers the nickel.

A.3 Bond Pads on Coated Glass

The previous sections discussed general principles related to the design and fabrication of bond pads for flip-chip bonding of custom dies to CMOS dies. We revisit them here for a specific case study, namely the development of a prototype vertically-integrated (VI) CMOS image sensor (Fig. A.1). The custom die is a photodetector die on which a photodetector array has been fabricated. To complete the VI-CMOS image sensor, it must be flip-chip bonded to a CMOS die containing CMOS read-out circuits.

Bond pads are required on the custom die, which is actually not a glass substrate. To make the photodetector array, the glass has been coated with ITO and a-Si:H. Since the a-Si:H is not itself

patterned, the array of photodetectors is actually defined by the array of bond pads fabricated on the a-Si:H. These bond pads form the back electrical contacts of all photodetectors, with respect to light entering the image sensor. Bond pads must also be fabricated on the ITO, at the periphery of the photodetector array, to establish a connection between the front electrical contact and the CMOS die.

A.3.1 Design of Bond Pads

Our application required the design of bond pads for a-Si:H and ITO substrates. Due to the capabilities, at the time of our initial design, of the flip-chip bonding suppliers to whom we had access, our pads have a footprint of $55 \times 55\,\mu\mathrm{m}^2$ and a centre-to-centre spacing of $110\,\mu\mathrm{m}$. These dimensions determine the horizontal profiles of both the TSM, on the CMOS dies, and the UBM, on the photodetector dies (Chapter 3). Because the standard CMOS dies were to be pre-processed for flip-chip bonding by a third party, we focused on the pre-processing of the custom photodetector dies, in other words on the UBM.

We chose to use a $100\,\mathrm{nm}$ sputter-deposited layer of chromium as the foundation layer of the UBM. Chrome was preferred over titanium because our titanium etchant contained hydroflouric acid (HF). Since HF also etched glass, it was not advisable to use it with coated glass substrates. The chrome showed good adhesion to the a-Si:H and ITO substrates, as well as the naked glass substrates.

As for the wettable layer of the UBM, we considered the following three options:

1. Electroless nickel/immersion gold: In this case, the nickel is the wettable layer for soldering, and the gold is there to prevent oxidation of the nickel when the UBM is heated as a preparation for bonding. Lead-tin solder would be used here. This process cannot be done in the University of Alberta Nanofab, but it was available through CMC. We were asked to prepare bond pads with aluminum layers several microns thick to serve as the initial catalyst for the electroless nickel. Currently, aluminum deposition in the Nanofab can be done only by sputtering. Since thick films of sputtered aluminum proved to be of poor quality, this option was not suitable for us.

2. Electroplated nickel/electroplated gold: A thick nickel layer (several microns) and a thin gold layer (several hundred nanometers) would be deposited by electroplating in this case. The roles of the nickel and gold layers here are as described above. Similarly, lead-tin solder would be used. To ensure adhesion of the electroplated nickel (see Fig. A.3), a seed layer needed to be deposited on the chrome foundation layer. Moreover, two stages of electroplating were required, which increased the process complexity. We abandoned this option in favour of a simpler one.

3. Electroplated gold: In this case, a thick layer of electroplated gold (about $1.5\,\mu\mathrm{m}$) is used as the wettable layer. Indium-based solder bumps would therefore be used (lead-indium was available from the flip-chip supplier). Compared to the previous option, it might seem that using a thick gold layer would cost more. However, the economics of electroplating at the Nanofab, and the small scale of our prototype, meant that this was not so. This was our preferred option.

In summary, we decided to go with chrome as the foundation layer and with gold as the wettable layer. We used nickel as a seed layer for the electroplating of gold. A thin nickel layer can be deposited by sputtering immediately after the sputter deposition of chrome, and nickel can

be etched with chemicals that are available in the Nanofab. Unlike sputtered platinum or gold, which can also be used as a seed layer for electroplated gold, nickel is a relatively cheap metal. Also, nickel serves as a good barrier layer between gold and chrome. The final design of the bond pads was a $100\,\mathrm{nm}$ foundation layer of chrome, a $200\,\mathrm{nm}$ barrier/seed layer of nickel, and a $1.5\,\mu\mathrm{m}$ wettable layer of gold.

A.3.2 Fabrication of Bond Pads

Fig. A.4 illustrates the main process steps in the fabrication of bond pads on the a-Si:H and ITO regions of glass substrates. These bond pads enable our custom dies to be flip-chip bonded with CMOS dies. All steps were done at the University of Alberta Nanofab. Further details are given below:

1. Sputtering of chrome and nickel: This step was done in a Lesker DC magnetron sputtering machine. Both materials were sputtered at $300\,\mathrm{W}$, in an argon atmosphere at $7\,\mathrm{mTorr}$.

2. Lithography: After this step, the whole substrate was covered with photoresist, except for the $55 \times 55\,\mu\mathrm{m}^2$ squares that would define the bond pads. Only one mask was required.

3. Electroplating of gold: Using a Techni Gold 25 E S solution, deposition was done at $40\,^{\circ}\mathrm{C}$. The current density was about $0.1\,\mathrm{ASD}$ (Amperes per square decimeter), and the deposition rate was about $65\,\mathrm{nm/min}$. Fig. A.5 depicts the Nanofab station developed through this work.

4. Stripping of the photoresist: After washing residues of the electroplating solution from the sample, the photoresist was stripped using acetone and IPA (isopropyl alcohol).

5. Etching of the nickel and chrome: First, the nickel was etched using a diluted solution of $FeCl_3$. Next, the chrome was etched using a chrome etchant solution. The gold acted as a mask.

Photos of the finished photodetector dies, prior to dicing, are given in Fig. A.6. The size of each bond pad is $55 \times 55\,\mu\mathrm{m}^2$. In the a-Si:H photodetector array, the distance between the centres of two adjacent bond pads is $110\,\mu\mathrm{m}$. The size of each die, excluding the dicing lines, is $3.7 \times 3.3\,\mathrm{mm}^2$. Our next step was to complete the VI-CMOS image sensor prototype through flip-chip bonding, as reported in Chapter 3.

A.4 Conclusion

This appendix describes the design and fabrication of bond pads on custom dies so that they can be flip-chip bonded to CMOS dies. Design of bond pads entails top surface metallurgy and solder materials. With nonmetal substrates, such as semiconductors, the bond pads have to be composed of several metal layers. The foundation layer must be reactive but the wettable layer must resist oxidation. Fabrication of bond pads involves wet plating and physical vapour deposition. Electroplating and electroless plating are suitable ways to make thick metal layers; whereas, sputtering and immersion plating are suitable for making thin metal layers.

We used sputtering and electroplating to fabricate bond pads on the photodetector dies that were prepared for the VI-CMOS image sensor prototype. The metal stack included a chromium foundation layer and a gold wettable layer.

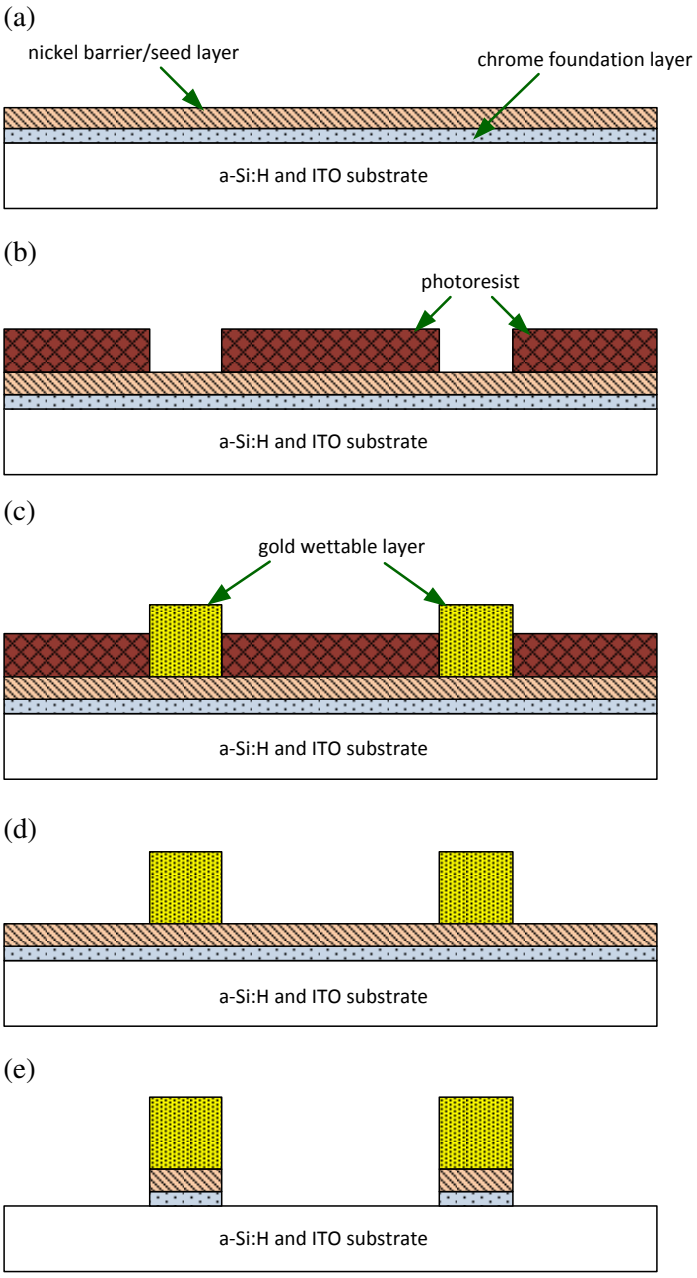

Figure A.4: Fabrication of bond pads: (a) Sputtering of a $100\,\mathrm{nm}$ foundation layer of chrome and a $200\,\mathrm{nm}$ barrier/seed layer of nickel. (b) Lithography—only the areas that will be bond pads are exposed. (c) Electroplating of a $1.5\,\mu\mathrm{m}$ wettable layer of gold. Deposition occurs only on the exposed nickel, which is connected to the cathode. (d) Stripping of the photoresist. (e) Etching of the nickel and chrome, except from underneath the gold.

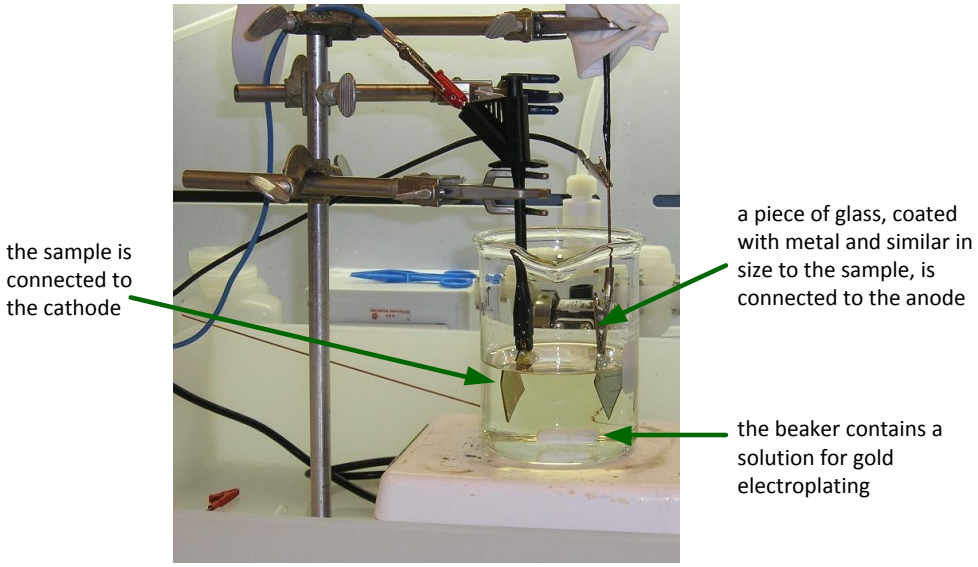

Figure A.5: The gold electroplating station: A beaker filled with a gold electroplating solution is placed on a hot plate that also provides stirring. The solution is heated to about $40\,^{\circ}\mathrm{C}$. The sample, on which the gold is to be deposited, is connected to the cathode. A comparable piece of glass with a conductive coating is connected to the anode. A power supply keeps a constant current between the electrodes while monitoring the voltage.

(a) (b)

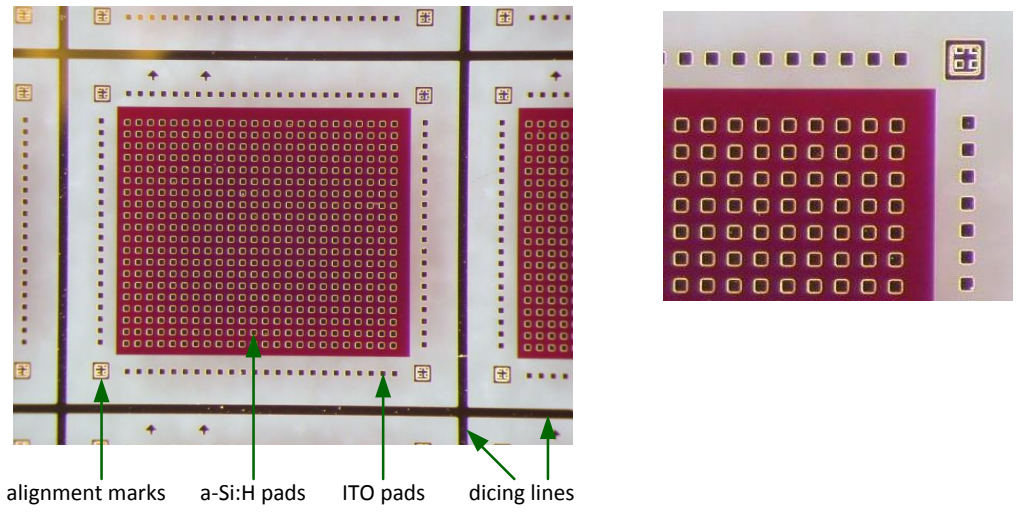

Figure A.6: (a) Photodetector dies with photodetectors for a prototype VI-CMOS image sensor. (b) A closer look at a photodetector array. Bond pads, i.e., the UBM for flip-chip bonding, are visible on the a-Si:H and ITO regions.