# Fault Tolerant Control of a Grid Interfacing Converter for Bipolar DC Distribution

by

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# Abstract

Recent research on electric power conversion has focused on multiport power electronic converter topologies, in which a single converter can transfer power between more than two ports. These ports interface with alternating current (AC) and/or direct current (DC) systems, and exchange power between them for various applications, such as grid integration of wind and solar power and the fast charging of electric vehicles. In general, by multitasking certain components, these multiport converters have the advantage of fewer switching devices, smaller footprints, and reduced cost.

However, many existing multiport converter designs have diminished reliability since internal components are typically shared between different power conversion stages. Consequently, a single switch failure in a multiport converter can end up rendering an entire system inoperative. This complete loss of power transfer on all ports presents an unacceptable level of risk to system reliability and operational resiliency. In comparison, conventional multi-converter systems do not suffer to the same degree from single points of failure. To address this gap, this work pursues new control strategies to allow a multiport converter topology to re-task healthy phase legs such that power transfer to all ports may continue during internal component failures.

Focusing on a grid interfacing converter for bipolar DC distribution with the ability to handle unbalanced DC side power flows, a converter model and constraints are developed that allow for continued operation during single and dual phase leg faults. Controls are then developed to meet these constraints while realizing appropriate transient responses to faults and load changes. The system is tested using a new controller hardware-in-the-loop environment built using a NovaCor Real-Time Digital Simulator and Imperix Boombox controller, with communication achieved using the Aurora protocol over fibre.

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# List of Abbreviations

| | |
|---|---|
| Alpha-Beta | Alpha-Beta (Stationary) Reference Frame |
| AC | Alternating Current |
| BGIC | Bipolar DC Grid Interfacing Converter |
| BJT | Bipolar Junction Transistor |
| DDSRF | Decoupled Dual Synchronous Reference Frame |
| DC | Direct Current |
| DQ | Direct-Quadrature (Synchronous) Reference Frame |
| EOF | End of Frame |
| FPGA | Field Programmable Gate Array |
| HDL | Hardware Description Language |
| HVDC | High Voltage DC |
| IGBT | Insulated Gate Bipolar Transistor |
| KCL | Kirchhoff's Current Law |
| KVL | Kirchhoff's Voltage Law |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| PV | Photovoltaic (Solar) |
| PCC | Point of Common Connection |
| PI | Proportional Integral |
| PIR | Proportional Integral Resonant |
| PWM | Pulse Width Modulation |
| RTDS | Real Time Digital Simulator |
| SBI | Sandbox Input |
| SBO | Sandbox Output |
| SFP | Small Form-Factor Pluggable (Fibre Optic Data Port) |
| SOF | Start of Frame |
| 2L-VSC | Two Level Voltage Source Converter |
| VFD | Variable Frequency Drive |

# Symbol Convention

Throughout this work, the symbol convention for mixed AC/DC signals from Sedra & Smith [1] is used. That is,

$$I_g(t) = I_G + i_g(t)$$

Where $I_G$ is the DC portion and $i_g$ is the AC portion of the signal. For brevity, the signals are all assumed to be time-varying; therefore (t) is omitted. To differentiate signals in the time domain from those in the Laplace (frequency) domain, signals in the Laplace domain are bolded. Therefore, a typical set of current, voltage, and modulating signals is represented in the time domain as:

$$I_g = I_g(t) = I_G + i_g(t) = I_G + i_g$$
$$V_g = V_g(t) = V_G + i_g(t) = V_G + v_g$$
$$M_g = M_g(t) = M_G + m_g(t) = M_G + m_g$$

The same set of signals is represented in the Laplace domain as:

$$\boldsymbol{i_g} = i_g(s)$$
$$\boldsymbol{v_g} = v_g(s)$$
$$\boldsymbol{m_g} = m_g(s)$$

Time derivatives are represented using dot notation, where:

$$\frac{dv_g}{dt} = \dot{v_g}$$

Complex quantities may be expressed in phasor notation, such that:

$$\bar{A} = \alpha + \beta j = |A|e^{j\theta} = A\angle\theta$$

# 1. Introduction

Power electronic converters, capable of converting power between AC and DC forms, have become ubiquitous – appearing in motor drives (VFDs), electric vehicles, consumer electronics, and high-voltage DC (HVDC) transmission systems. One area with substantial growth is distributed generation – where small generating units, often utilizing renewable energy sources (wind or solar), are located throughout a power grid, as opposed to large units in remotely located plants. Growth is driven by the increased usage of renewable energy sources, reduced capital outlay for smaller units, and increased supply reliability, along with the avoidance of constructing new transmission lines [2].

In an effort to reduce costs & switching losses, while improving the interface between renewable sources and the grid, multiport power converters, capable of transferring power between 3 or more AC and/or DC ports, are being developed [3]. Many of the advantages of multiport power converters come as a result of shared power stages and decreased switching device counts; however, this can lead to reduced resiliency in the face of converter faults. With the increased penetration of distributed generation, converters "tripping" offline (shutting down due to fault conditions) can exacerbate under-frequency conditions leading to grid instability [2].

In distributed generation units, converters are considered a weak link from a reliability standpoint – they have a high failure rate, lower lifetime, and higher maintenance costs, compared to other components [3]. In one solar (PV) installation, over a 5-year period, 156 unscheduled maintenance events occurred where generation capacity was lost; 37% of these events were related to the converters, and the converter-related events constituted 59% of the total outage expenditure [4]. In another installation (wind), 13% of failures and 18.4% of downtime was converter related [5].

Overall, in wind farms, converter-related failure rates fall between 0.12 – 0.39 events per turbine, per year [6].

One of the main sources of converter failure is the phase module, which is responsible for 22% of failures [7]. Insulated Gate Bipolar Transistors (IGBTs), a type of semiconductor power device, are the building blocks of the phase modules of voltage-source converters, being able to be switched on and off while current is flowing. Industry surveys and studies have found semiconductor power devices to be the most failure prone and fragile component of a converter [8, 9], while converter modules analyzed after failure found that 75% had non-switching IGBTs [6].

IGBT failure has a variety of causes, including bond-wire lift-off, gate drive failure, high-voltage breakdown & latch-up, and can lead to either short-circuit or open-circuit conditions [10]. Ongoing work focuses on detecting and mitigating IGBT faults, including through the use of additional (backup) phase modules and cascaded inverters [11].

When an IGBT in a phase module of a grid-interfacing voltage-source converter fails in the absence of fault-tolerant controls, it generally causes unbalanced AC grid currents. As the grid is unable to tolerate these unbalanced conditions, protection systems will quickly trip the converter offline, resulting in the complete loss of power transfer. If protection systems fail to trip the converter offline, the harmonics caused by the unbalanced operation can lead to damage to other equipment connected to the AC grid. In addition, large ripple on the DC link during a fault condition can cause damage to the connected DC equipment.

## 1.1. Two-Level Voltage Source Converters

During the 1990's, Insulated Gate Bipolar Transistors (IGBTs), a combination between a Bi-polar Junction Transistor (BJT) and a Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET), began to see use in HVDC converters in a two-level topology, referred to as Voltage Source Converters (VSCs or 2L-VSCs). Compared to thyristors used in Line-Commutated Converters (LCCs), the IGBT is able to be switched off while current is flowing, allowing switching to be independent of the line current. As the IGBT is a unidirectional device (current flow in one direction only), it is paired with diode to provide current flow in the opposite direction (antiparallel), to allow bidirectional current flow.

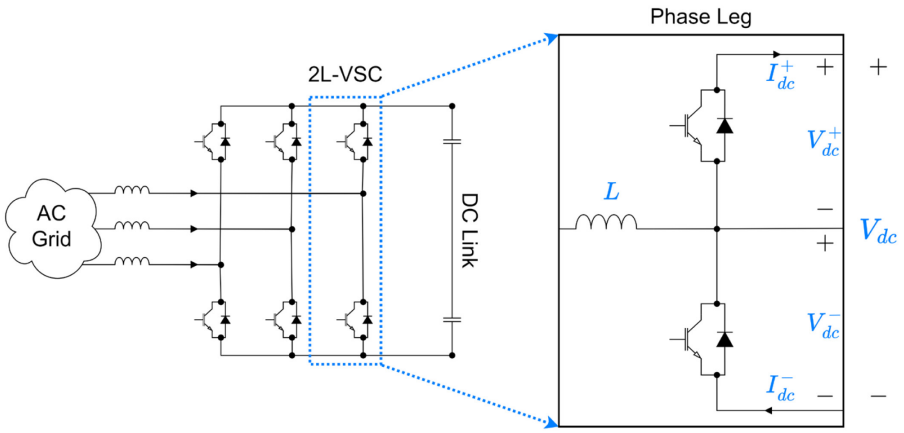



*Figure 1 - 2L-VSC Phase Leg*

A phase leg is created by stacking two IGBTs, each with an antiparallel diode, as shown in Figure 1. When an IGBT is commanded to conduct, it is considered "on", whereas when it is commanded to open, it is considered "off". The midpoint is connected, through its respective inductor, to the AC phase output, while the upper and low points are connected to the positive and negative rails of the DC link, respectively. This allows the midpoint to be switched between $V_{DC}^{+}$ (by turning the upper IGBT on and the lower IGBT off) and $V_{DC}^{-}$ (by turning the upper IGBT off and the lower IGBT on). If both IGBTs are on, a shoot-through condition (short circuit of the DC link) is created

– this is to be avoided at all times. If neither IGBT is on, the converter acts as a line-commutated converter due to the antiparallel diodes.

Under normal operation, if the upper IGBT is on, the lower IGBT is off, and vice-versa. The percentage of time that the upper IGBT is turned on, relative to the switching period, is referred to as the duty cycle, and this determines the time-averaged voltage at the midpoint (which can be set to any value between $V_{DC}^{+}$ and $V_{DC}^{-}$).

A modulating signal is created, of the form:

$$M_a = M_A + m_a = M + m\,sin(\omega_e t + \theta_a) \tag{1}$$

where $M_a \in [-1,1]$, and $M$ / m are the AC and DC modulation indexes, respectively. This modulating signal can then be compared to a triangular carrier wave, with a frequency much higher than the fundamental frequency, to generate a pulse width modulation (PWM) signal. The PWM signal varies the duty cycle of the phase arm over time, resulting in a midpoint voltage that has a fundamental frequency component with amplitude $m\left[\frac{V_{DC}^{+}+V_{DC}^{-}}{2}\right] = m\frac{V_{DC}}{2}$. Due to the high frequency switching, the frequency spectrum has substantial components at and around the switching frequency as well. However, if the interface inductor is sized appropriately, it will largely filter out these high-frequency components, resulting in a (mostly) noise-free fundamental frequency voltage at the AC connection point. An example of this process is shown in Figure 2, where the AC modulation index has been set at 0.8 (DC modulation index at 0), the modulation frequency at 60Hz ($\omega_e = 2\pi 60$), the carrier frequency at 3000Hz, and the DC link voltage ($V_{dc} = V_{dc}^{+} + V_{dc}^{-}$) at 300V. The resulting midpoint voltage 60Hz component is therefore $\frac{300}{2} \cdot 0.8 = 120$V.

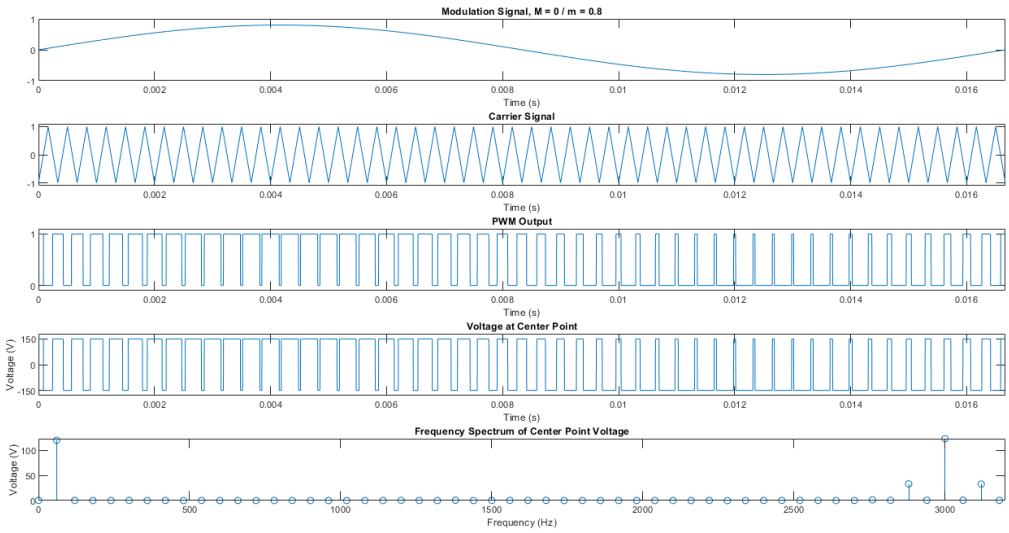



*Figure 2 – PWM Example with M=0, m = 0.8*

In high voltage applications, it is common for the DC link voltage to greatly exceed the voltage blocking capabilities of commercially-available IGBTs, which are typically in the range of a few thousand volts. Therefore, while a valve is represented as a single IGBT, it is commonly built as a number of IGBTs connected in series with a complex gate drive circuit that balances the voltage drop across each IGBT. The current rating of IGBTs used in converters is generally in the hundreds of amps; due to this, there may also be IGBTs in parallel to increase the current capacity of the converter. In the case where there are no parallel IGBTs, an open-circuit fault arises in the phase arm if any single IGBT fails to conduct; this may be a result of failure of the IGBT itself, such as in the case of bond wire lift-off, or the failure of a gate drive circuit. For converters with parallel IGBTs in each phase arm, it requires multiple IGBTs directly in parallel with each other to be faulted, reducing the likelihood of device failure causing phase arm failure, but increasing the complexity of the gate drive circuit, potentially increasing its failure rate.

## 1.2. Multiport Power Converters

Multiport power electronic converter topologies are typically single converter structures that can exchange power between three or more ports, often explored in the pursuit of achieving smaller, more efficient converter systems [3]. Compared to conventional, independent multi-converter systems (Figure 3(a)), multiport systems (Figure 3(b)) share internal components between power conversion stages, resulting in fewer switching devices and a smaller footprint [13].

In a multi-converter system, in order to transfer power between ports that separated by converter stages, it is necessary for power to flow through another (external) component. For example, in Figure 3, if power is to flow from DC port 1 to DC port 2, it must pass through the upper AC transformer, the AC grid connections, and the lower AC transformer. In comparison, in the multiport converter setup, power can flow directly from DC port 1 to DC port 2 without involving either the transformer or the AC grid connection. This allows the AC side to be sized appropriately for the required AC power transfer, rather than the AC and DC power transfer combined. In addition, losses are reduced as redundant stages (DC-DC vs DC-AC/AC-DC) are removed.

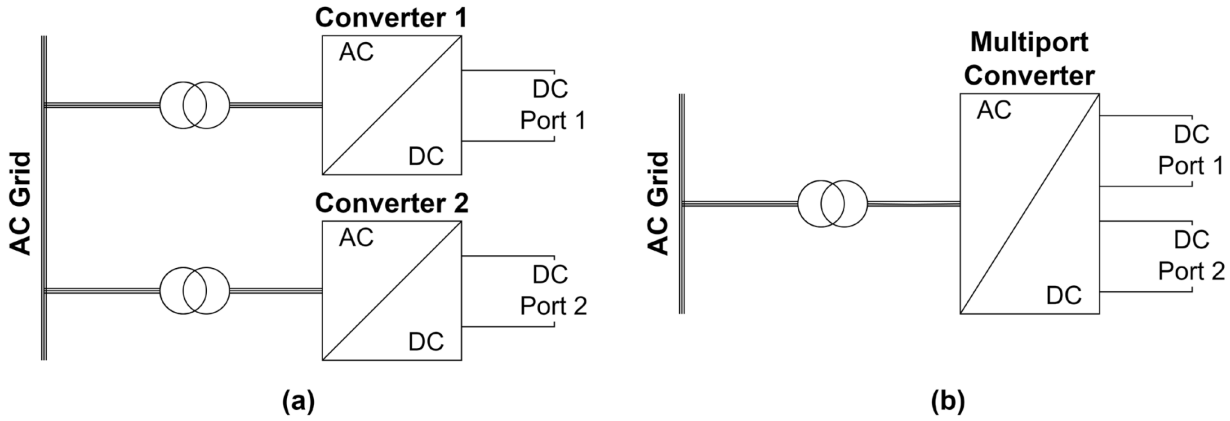



*Figure 3 - (a) Multiconverter System (b) Multiport System*

However, assuming the converters have no fault-tolerance, any single fault in the multiport converter setup will stop all power transfer, whereas a single fault in the multi-converter setup will

only impact power transfer to/from one DC port. This is considered a major caveat of multiport converter deployments.

## 1.3. Fault Tolerance in Multiport Converters

A significant amount of work has been done on detecting switching faults in 2L-VSCs and the similar Neutral Point Clamped (NPC) 3-level converter using a variety of approaches – including observers, discrete wavelet transforms, and change rate of current residual. For examples, see [14, 15, 16, 17]. Work has then followed on to fault-tolerant control of 2L-VSCs, often using additional switches (e.g., TRIACs) to intentionally overload fuses placed in front of the converter on the AC connections to remove the faulty leg from the circuit while connecting the faulted phase to the neutral point of the DC link [18, 19], as shown in Figure 4. This allows the converter to continue operating with balanced grid currents but introduces unwanted fundamental frequency ripples on the DC link midpoint.

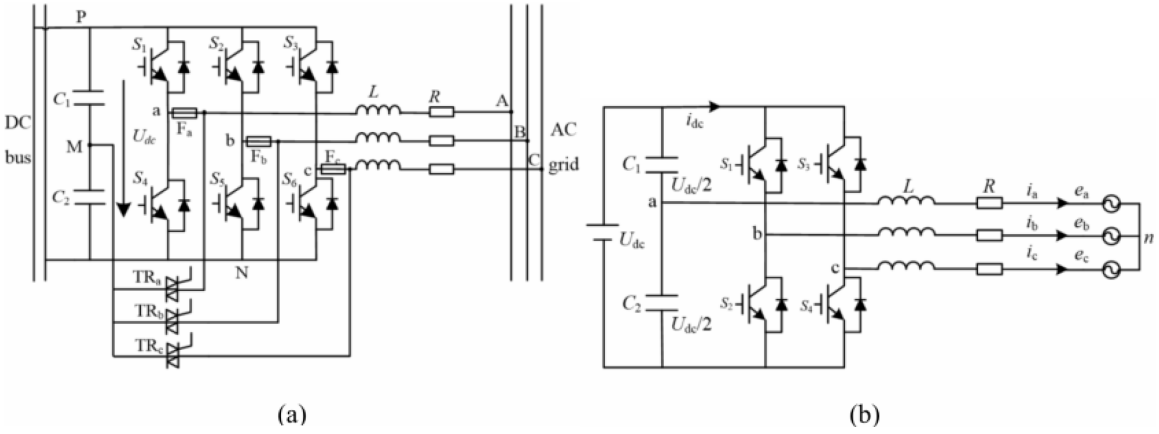
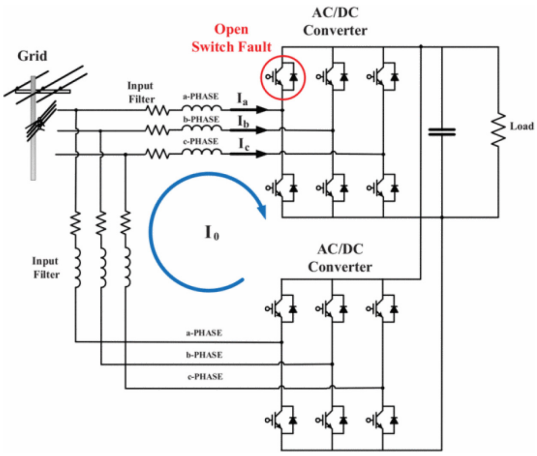



*Figure 4 - Fault Tolerant Approach using TRIACs / Fuses [19]*

*(a) Fault Tolerant Structure, (b) Equivalent Circuit during Phase A Fault*

In [20], a multi-converter approach to connecting a DC load to an AC grid explored fault-tolerant operation by having the healthy inverter modify its operation. In this strategy, the faulted converter produces an unbalanced AC current, which is unacceptable to the grid, so the AC current in the healthy inverter is intentionally unbalanced in order to compensate. This requires coordination

between two independent converters while producing a circulating current that must be tolerated by the grid connections, shown in Figure 5. This converter system also only has a single DC port and thus is unable to balance the poles of a bipolar DC connection.



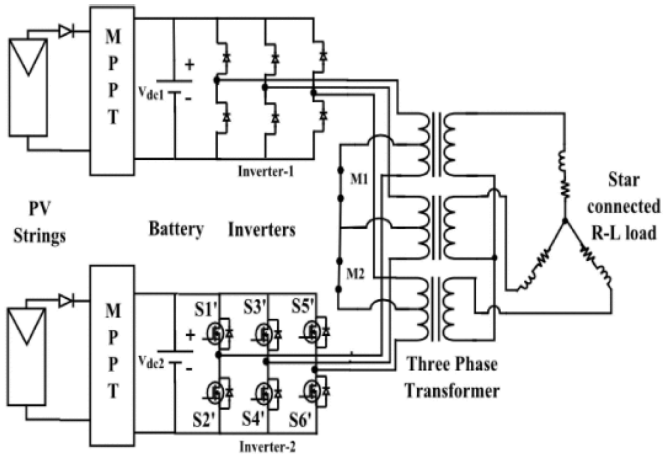




*Figure 5 (left) - Parallel AC/DC Converters Under Fault Conditions, with Circulating Current [20]*

*Figure 6 (right) - Fault Tolerant Multiport Converter Approach [21]*

A multiport converter topology, with two separate DC links and a centre-tapped transformer was used in [21], shown in Figure 6. Under normal controls, a switching fault causes overall system failure, while it is noted that "the healthy inverter … is still capable of supplying half of the total power" [21]. The approach taken was to cease power transfer to the DC link on the faulted side, while connecting the three centre-taps on the transformer (enabled by closing switches M1 and M2). This allows the healthy side to continue to transfer power, albeit at a reduced maximum (0.5PU). In addition, it is not possible to transfer power from one of the DC links during the fault.

## 1.4. Motivation

In 2021, a multiport converter topology was proposed in [12], shown in Figure 7, which consists of two, two-level voltage source converters (2L-VSCs) arranged around a centre-tapped transformer. A single AC port is used to connect to the grid, while the two DC ports are tied together at the midpoint to create a bi-polar DC link with the ability to balance the pole voltages while transferring power independently to or from each pole. Thus, it is an implementation of the multi (three) port converter system in Figure 3b. Though it allows AC/DC and DC/DC conversion within a single converter structure, while also reducing the transformer requirements compared to a conventional, multi-converter setup, it suffers from reduced resiliency during phase module faults, as tripping offline results in losing power transfer capability from both DC sources. However, as will be demonstrated in this thesis, the topology itself supports fault-tolerant operation, allowing for continued power transfer during multiple phase module faults (with power level restrictions) with balanced AC grid currents and independent power transfer from each DC source. It is only the originally proposed controls in [12] that limit the fault-tolerant abilities of the converter.

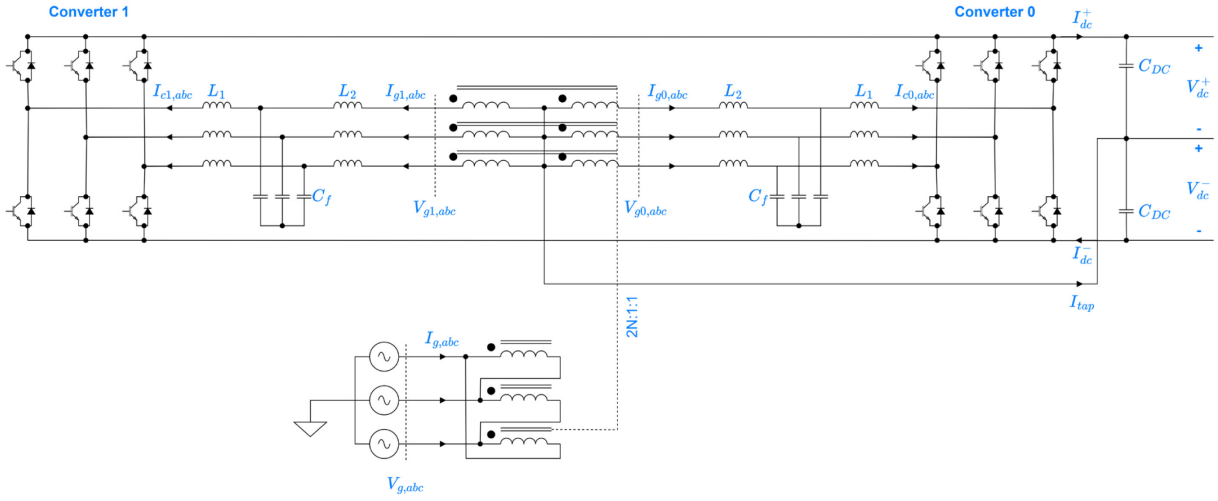



*Figure 7 - Bipolar Grid Interfacing Converter (BGIC) under study in this work [12]*

The Bipolar DC Grid Interfacing Converter (BGIC) shown in Figure 7 provides the ability to independently exchange power between an AC grid and each pole of a bi-polar DC link, while retaining the advantages of a multiport power converter. However, its operation under IGBT failure, a prevalent cause of failure in power converters, is insufficient for continued connection to the power grid.

Previous approaches to creating a more fault-tolerant AC/DC/DC converter have focused on separating the DC links [21, 22], allowing for continued operation during a switching / IGBT fault in one phase arm. This is achieved either by shifting the modulating index towards the healthy inverter, as in [22], or by connecting the centre-taps of the grid connection transformer and disabling the entire 2L-VSC affected by the switching fault, as in [21]. In both cases, it is not possible to exchange power with one of the DC links, and a second switching / IGBT fault can render the entire converter inoperable.

The motivation of this work is to determine the constraints and conditions required in order for the BGIC from [12] to continue operation, possibly with reduced maximum power transfer, under a variety of switching / IGBT faults, and then develop controls that enable balanced AC grid operation with acceptable DC link power quality during normal system events while the converter is faulted. As the BGIC from [12] is built upon the 2L-VSC topology, this work focuses on fault tolerance for two-level-type converters; while the same topology can be built with modular, multilevel converters (MMCs), the failure mode in an MMC-type converter is different due to the additional current path through the phase arm. Therefore, open-circuit IGBT failures have a different reliability threat and require a different fault response.

## 1.5. Thesis Scope

A new control strategy for the BGIC from [12], shown in Figure 7, is presented in this thesis, with two implementations – one which controls the converter currents in the ABC frame, the other which controls them in the synchronous (DQ) frame. Both control implementations allow the converter to continue operating, at reduced power levels, during single and dual IGBT open-circuit failures (provided the dual failures do not occur on the same phase), while maintaining the ability to balance the DC link voltage between the two poles during load changes. Crucially, the controls maintain balanced AC grid currents despite the permanently applied faults.

The ABC frame controls are tested in a pure simulation environment, using the NovaCor Real Time Digital Simulator (RTDS), while the DQ frame controls are tested using a controller hardware-in-the-loop (C-HIL) environment built with an Imperix Boombox and the RTDS. In order to accommodate the number of input signals to the controller, a fibre-optic link (utilizing the Aurora 8b10b protocol) was established between the Boombox and RTDS. This link was developed for this thesis and implemented in FPGA using the Verilog Hardware Description Language (HDL).

The thesis is laid out as follows:

- Chapter 2 introduces the Bipolar DC Grid Interfacing Converter topology under study and its operating principle. Operating conditions are explored under healthy conditions as well as single & dual IGBT open-circuit failures.
- Chapter 3 introduces the proposed fault tolerant control implementations and validates them using simulation and C-HIL experiments.
- Chapter 4 provides a summary.

# 2. Bipolar DC Grid Interfacing Converter Operation

In 2021, a three-port converter with 1 AC port and 2 DC ports, capable of balancing the DC voltage between the two DC ports, was proposed [12], shown in Figure 8. The Bipolar DC Grid Interfacing Converter (BGIC) allows for AC/DC and DC/DC conversion, with the ability to transfer power between ports with no restrictions, other than total power transfer.

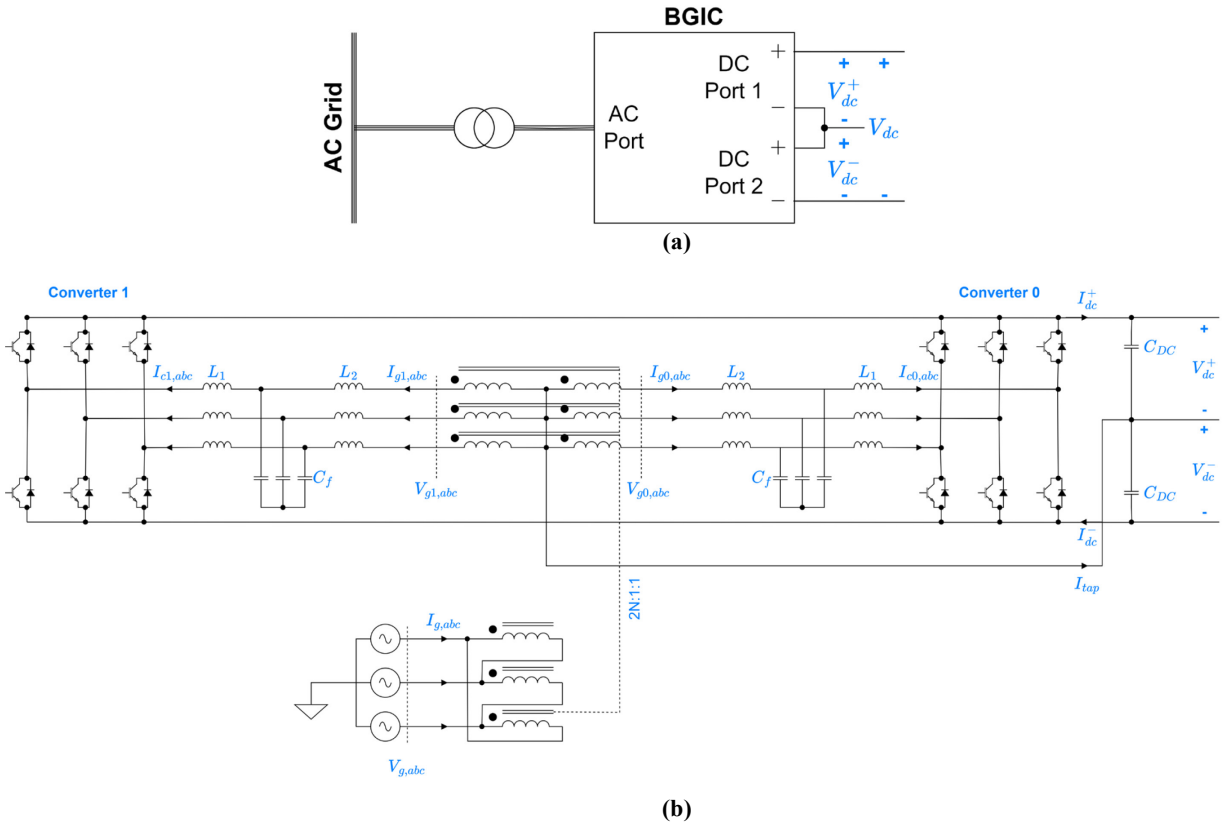



*Figure 8 - Bipolar Grid Interfacing Converter (BGIC)*
*(a) Port Arrangement, (b) Topology*

Under healthy operating conditions, it is capable of rapid response to step changes in the power transfer from either of the DC ports, yielding a quick return to a balanced voltage condition. However, with the originally proposed controls from [12], the AC grid current is unbalanced and the DC port voltage exhibits large ripples during a fault condition. As an example, Figure 9 shows the response of the BGIC under the controls proposed in [12] to an upper switching fault on phase

A of the right converter (converter 0). The steady-state three-phase grid currents under the fault are unbalanced, with the magnitude of the phase C current being nearly twice the magnitude of the remaining phases. In addition, a large zero sequence current is present and the DC link has substantial ripple at twice the fundamental (grid) frequency.

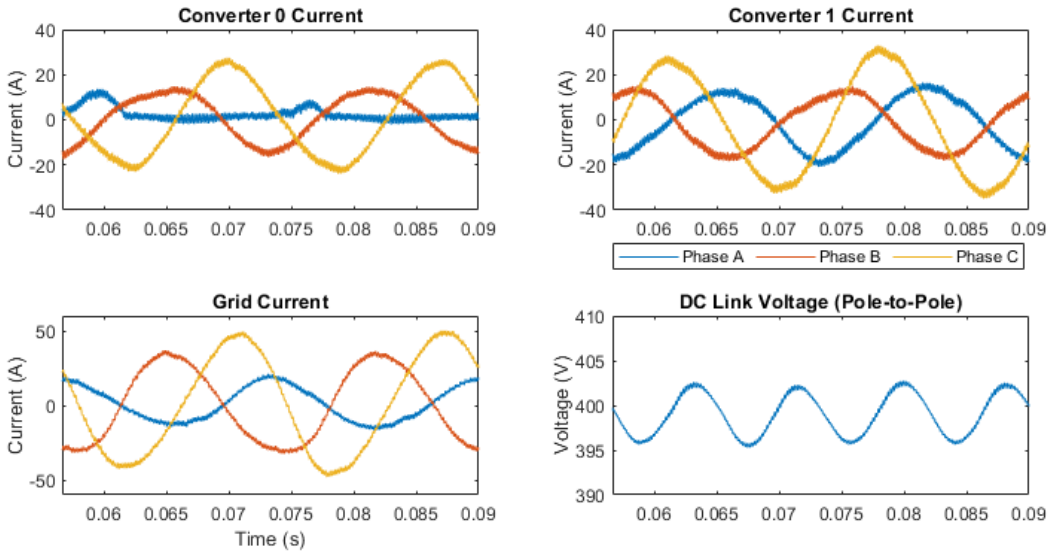



*Figure 9 – Original BGIC Controls Under Single Switch Failure*

## 2.1. Operating Principle and Model of BGIC

Under healthy operating conditions, the BGIC operates all six phase legs such that each 2L-VSC is producing / consuming balanced AC current, and the DC current carried by the centre-tap transformer is equal on all 6 windings. This allows the DC flux to cancel within the transformer, avoiding core saturation. The PCC sees no DC current and AC currents are balanced. DC current flows through the centre-taps ($I_{TAP}$) to balance the capacitor voltages such that $V_{DC}^{+} = V_{DC}^{-}$.

For the following analysis, the phase A grid voltage is taken as the zero degree reference and the grid voltages are assumed to be ideal, such that:

$$V_a = V_{ln}\cos(\omega_e t) \tag{2}$$

$$V_b = V_{ln}\cos(\omega_e t - 120^o) \tag{3}$$

$$V_b = V_{ln}\cos(\omega_e t + 120^o) \tag{4}$$

The AC grid currents are then given as (neglecting harmonics):

$$I_{ga} = I_{GA} + i_{ga} = I_G + i_g\cos\left(\omega_e t + \theta_{i_g}\right) \tag{5}$$

$$I_{gc} = I_{GB} + i_{gb} = I_G + i_g\cos\left(\omega_e t + \theta_{i_g} - 120^o\right) \tag{6}$$

$$I_{gc} = I_{GC} + i_{gc} = I_G + i_g\cos\left(\omega_e t + \theta_{i_g} + 120^o\right) \tag{7}$$

Note that DC current ($I_G$) exists here for pole balancing purposes and must cancel such that no DC current is present at the PCC. The AC port currents of converter 0 are given as:

$$I_{g0a} = I_{G0A} + i_{g0a} = \frac{I_{TAP}}{6} + \frac{i_g}{2}\cos\left(\omega_e t + \theta_{i_g}\right) \tag{8}$$

$$I_{g0b} = I_{G0B} + i_{g0b} = \frac{I_{TAP}}{6} + \frac{i_g}{2}\cos\left(\omega_e t + \theta_{i_g} - 120^o\right) \tag{9}$$

$$I_{g0c} = I_{G0C} + i_{g0c} = \frac{I_{TAP}}{6} + \frac{i_g}{2}\cos\left(\omega_e t + \theta_{i_g} + 120^o\right) \tag{10}$$

The modulating signals are composed of a fundamental frequency sinusoid with a DC bias, as:

$$M_a = M_A + m_a = M + m\cos(\omega_e t + \theta_m) \tag{11}$$

$$M_b = M_B + m_b = M + m\cos(\omega_e t + \theta_m - 120^o) \tag{12}$$

$$M_c = M_C + m_c = M + m\cos(\omega_e t + \theta_m + 120^o) \tag{13}$$

Assuming that the system is operated such that the pole-to-pole DC link voltage is kept constant, a fundamental frequency analysis can be carried out on the "AC" side of a single phase of one of the 2L-VSCs. The resulting circuit model, given in Figure 10, yields two differential equations for the currents,

$$v_a = L_2 \frac{di_{g0a}}{dt} + R_2 i_{g0a} + L_1 \frac{di_{c0a}}{dt} + R_1 i_{c0a} + m_a \frac{V_{dc}}{2} \tag{14}$$

$$v_a = L_2 \frac{di_{g0a}}{dt} + R_2 i_{g0a} + R_f i_{f0a} + \frac{1}{Cf} \int i_{f0a} dt \tag{15}$$

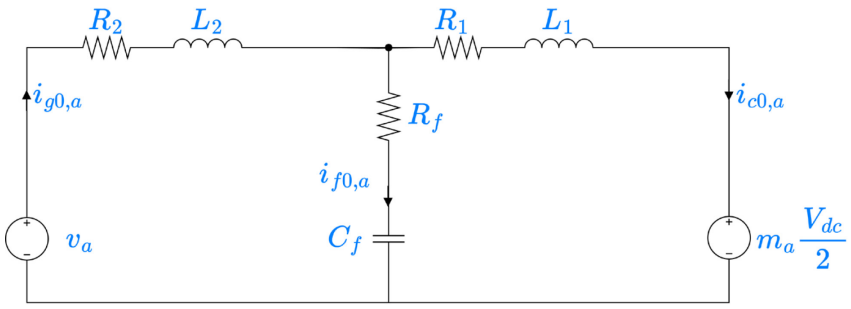



*Figure 10 – 2L-VSC Fundamental Frequency Time Averaged Model of "AC" Side*

Transforming these into the Laplace domain gives:

$$\boldsymbol{v_a} = (L_2 s + R_2)\boldsymbol{i_{g0a}} + (L_1 s + R_1)\boldsymbol{i_{c0a}} + \boldsymbol{m_a} \frac{V_{dc}}{2} \tag{16}$$

$$\boldsymbol{v_a} = (L_2 s + R_2)\boldsymbol{i_{g0a}} + \left(R_f + \frac{1}{C_f s}\right)\boldsymbol{i_{f0a}} \tag{17}$$

Since the converter AC port currents are equal to the converter current plus the filter current ($i_{g0a} = i_{c0a} + i_{f0a}$), equations (16) and (17) can be solved into one equation with a single unknown, the AC converter port current, as follows:

$$\boldsymbol{v_a} = (L_2 s + R_2)\boldsymbol{i_{g0a}} + \frac{L_1 s + R_1}{L_1 s + R_1 + R_f + \frac{1}{C_f s}} \left( \left( R_f + \frac{1}{C_f s} \right) \boldsymbol{i_{g0a}} - \boldsymbol{m_a} \frac{V_{dc}}{2} \right) + \boldsymbol{m_a} \frac{V_{dc}}{2} \tag{18}$$

The following approximations can be made when considering the fundamental frequency response:

$$L_1\omega_e \gg R_1 \qquad \frac{1}{C_f\omega_e} \gg L_1\omega_e$$

$$L_2\omega_e \gg R_2 \qquad L_1C_f\omega_e^2 \ll 1$$

$$\frac{1}{C_f\omega_e} \gg R_f$$

Equation (18) can then be approximated as:

$$\boldsymbol{v_a} \cong (L_1 + L_2)j\omega_e\boldsymbol{i_{g0a}} + \boldsymbol{m_a}\frac{V_{dc}}{2} \tag{19}$$

And the modulation index can be solved as:

$$\boldsymbol{m_a} \cong \frac{\boldsymbol{v_a} - (L_2 + L_1)j\omega_e\boldsymbol{i_{g0a}}}{\frac{V_{dc}}{2}} \tag{20}$$

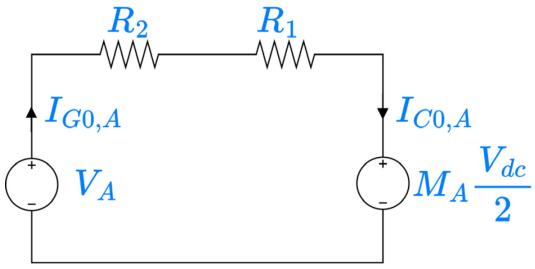



*Figure 11 - 2L-VSC DC Time Averaged Model of "AC" Side*

Conducting a similar analysis for DC conditions yields the circuit model in Figure 11, which can be used to derive an equation:

$$I_{G0A} = I_{C0A} = \frac{V_A - M_A\frac{V_{dc}}{2}}{R_1 + R_2} = -\frac{M_AV_{dc}}{2(R_1 + R_2)}, \tag{21}$$

where the grid is assumed to have no DC voltage bias present; i.e., $V_A = 0$.

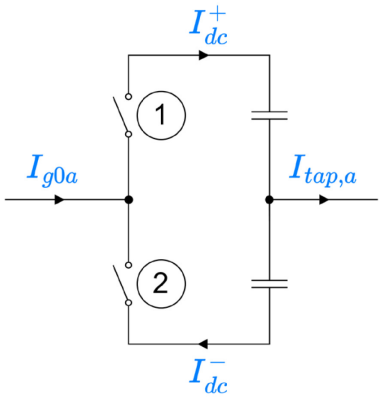



*Figure 12 – 2L-VSC Single Phase Leg "DC" Side Model*

Looking at the "DC" side of a single 2L-VSC, considering a single phase leg as in Figure 12, the DC pole currents are given as:

$$I_{dc}^{+} = I_{g0a}$$

$$I_{dc}^{-} = 0$$

when switch 1 is closed and switch 2 is open, and

$$I_{dc}^{+} = 0$$

$$I_{dc}^{-} = I_{g0a}$$

when switch 1 is open and switch 2 is closed. Taking the time-average across all three phases gives:

$$I_{dc}^{+} = \sum_{i=a,b,c} \frac{M_i + 1}{2} I_{gi} \tag{22}$$

$$I_{dc}^{-} = \sum_{i=a,b,c} \frac{M_i - 1}{2} I_{gi} \tag{23}$$

Looking at the A phase contribution of (22),

$$I_{dc,a}^{+} = \frac{M + m\cos(\omega_e t + \theta_m) + 1}{2} \cdot \left(\frac{I_{TAP}}{6} + \frac{i_g}{2}\cos\left(\omega_e t + \theta_{i_g}\right)\right) \tag{24}$$

this can be rewritten as:

$$I_{dc,a}^{+} = \frac{1}{4}\Bigg[m\cos\left(2\omega_e t + \theta_m + \theta_{i_g}\right) + m\cos\left(\theta_m - \theta_{i_g}\right) + \frac{I_{TAP}}{6}m\cos(\omega_e t + \theta_m)$$
$$+ (M+1)\frac{i_g}{2}\cos\left(\omega_e t + \theta_{i_g}\right) + 2(M+1)\frac{I_{TAP}}{6}\Bigg]$$

Although the fundamental and second harmonic components sum to zero across the 3 phases, the component of (24) corresponding to the AC power transfer (for a single phase) is given by:

$$i_{dc,a}^{+} = \frac{m\cos\left(\theta_m - \theta_{i_g}\right)}{4}, \tag{25}$$

and the DC power transfer for a single phase contribution is given by:

$$I_{DC,A}^{+} = \frac{(M+1)\frac{I_{TAP}}{6}}{2} \tag{26}$$

For the negative "DC side" pole current, while the fundamental and second harmonic components again sum to zero across the 3 phases, the AC power transfer term remains unchanged, and the DC power transfer term becomes:

$$I_{DC,A}^{-} = \frac{(M-1)\frac{I_{TAP}}{6}}{2} \tag{27}$$

Thus the contribution from a single phase to the tap current is given as:

$$I_{tap,a} = I_{dc,a}^{+} - I_{dc,a}^{-} = \frac{I_{TAP}}{6} \tag{28}$$

## 2.2. Operation & Modeling Under Single Switch Fault

When a single switch fault occurs (IGBT fails to open-circuit) in the considered BGIC, one 2L-VSC is capable of full operation while the other cannot maintain balanced 3-phase current. An example case is shown in Figure 13, where the fault occurs in the upper switch of the B-phase of converter 0.

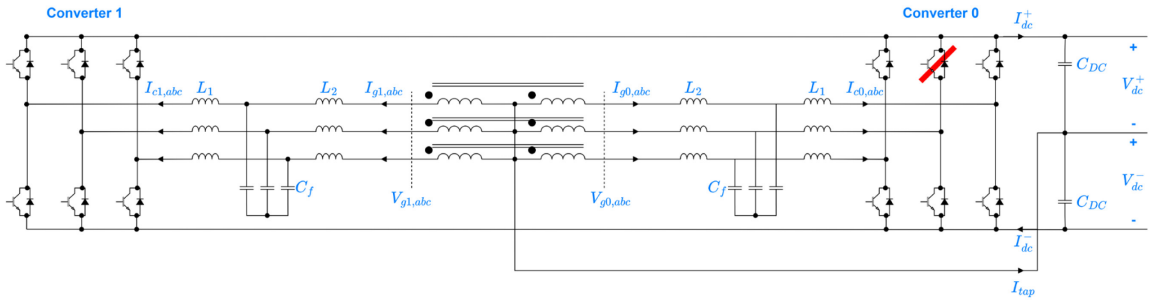



*Figure 13 - BGIC Under Single Switch Fault*

Under the proposed control strategy, the healthy converter (converter 1) maintains normal operation, required only to force the DC current of the faulty phase to zero. This is required in order to prevent transformer core saturation – since the faulted converter (converter 0) cannot produce DC current on the secondary winding of the affected phase (phase B), the healthy converter (converter 1) must also stop producing DC current on the secondary winding of the affected phase (phase B).

The faulted converter (converter 0) stops AC power transfer, since it is not capable of producing balanced three-phase AC current. However, it can continue to process DC current on the unaffected phases (phases A & C) to maintain pole balancing. The faulty arm is completely disabled, with all gating signals blocked to both the upper and lower IGBTs, to ensure no current is processed by this phase.

The time-averaged model for the "AC" port of the BGIC under the fault scenario of Figure 13, is given in Figure 14. Here, all three phases must be considered in the circuit as the three-phase operation is no longer balanced. Based on this circuit, KVL and KCL can be used to derive the following equations:

$$\boldsymbol{V_a} = \boldsymbol{I_{g0a}}Z_2 + \boldsymbol{I_{c0a}}Z_1 + \boldsymbol{M_a}\frac{V_{dc}}{2} \quad (29)$$

$$\boldsymbol{V_c} = \boldsymbol{I_{g0c}}Z_2 + \boldsymbol{I_{c0c}}Z_1 + \boldsymbol{M_c}\frac{V_{dc}}{2} \quad (30)$$

$$\boldsymbol{V_a} - \boldsymbol{V_b} = \boldsymbol{I_{g0a}}Z_2 + \boldsymbol{I_{f0a}}Z_f - \boldsymbol{I_{g0b}}Z_f - \boldsymbol{I_{g0b}}Z_2 \quad (31)$$

$$\boldsymbol{V_c} - \boldsymbol{V_b} = \boldsymbol{I_{g0c}}Z_2 + \boldsymbol{I_{f0c}}Z_f - \boldsymbol{I_{g0b}}Z_f - \boldsymbol{I_{g0b}}Z_2 \quad (32)$$

$$\boldsymbol{I_{f0a}} + \boldsymbol{I_{g0b}} + \boldsymbol{I_{f0c}} = 0 \quad (33)$$

$$\boldsymbol{I_{g0a}} + \boldsymbol{I_{g0b}} + \boldsymbol{I_{g0c}} = \boldsymbol{I_{c0a}} + \boldsymbol{I_{c0c}} \quad (34)$$

$$\boldsymbol{I_{g0a}} = \boldsymbol{I_{c0a}} + \boldsymbol{I_{f0a}} \quad (35)$$

$$\boldsymbol{I_{g0c}} = \boldsymbol{I_{c0c}} + \boldsymbol{I_{f0c}} \quad (36)$$

Solving equations (29) through (36), with the approximation that the filter impedance, $Z_f$, is larger than either the interface or converter impedances, $Z_1$ and $Z_2$ respectively, and neglecting harmonics, yields an equation for the approximate current on the disabled phase:

$$\boldsymbol{I_{g0b}} \cong \frac{\boldsymbol{v_b}(3Z_1 + 2Z_2) + \boldsymbol{m_b}\frac{V_{dc}}{2}}{3(Z_1 + Z_2)Z_f} \quad (37)$$

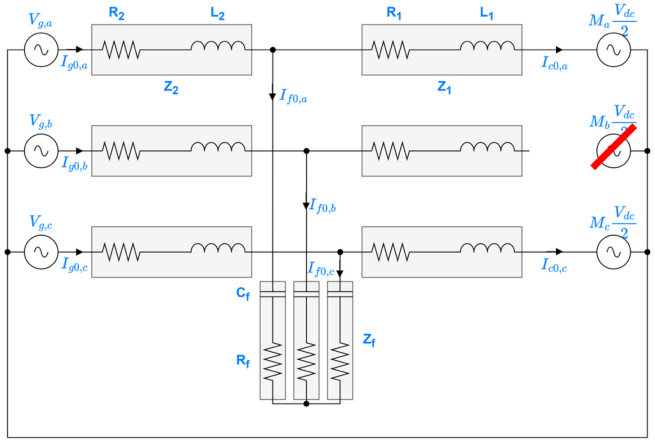



*Figure 14 - Time-Averaged Circuit Model with Disabled Leg (Phase B) on Converter 0*

Under healthy operation, the power transfer is limited by the peak current in the phase legs. The current in phase A of converter 1 is given as:

$$I_{c1a} \cong I_{g1a} = \frac{I_{TAP}}{6} - \frac{i_g}{2}\cos\left(\omega_e t + \theta_{i_g}\right) \tag{38}$$

This results in the healthy operation limiting equation:

$$\frac{I_{TAP}}{6} + \frac{i_g}{2} \leq I_{max} \tag{39}$$

Under single switch fault operation, the total tap current is split between 4 phase legs instead of 6, and, for each phase, the grid current is processed by a single phase leg, instead of 2. The current in phase A of converter 1 is then given as:

$$I_{c1a} \cong I_{g1a} = \frac{I_{TAP}}{4} - i_g\cos\left(\omega_e t + \theta_{i_g}\right) \tag{40}$$

This results in the single switch fault operation limiting equation:

$$\frac{I_{TAP}}{4} + i_g \leq I_{max} \tag{41}$$

The operating region under healthy and single switch fault operation are shown in Figure 15; the maximum power transfer during a single switch fault is limited to approximately 0.5PU.

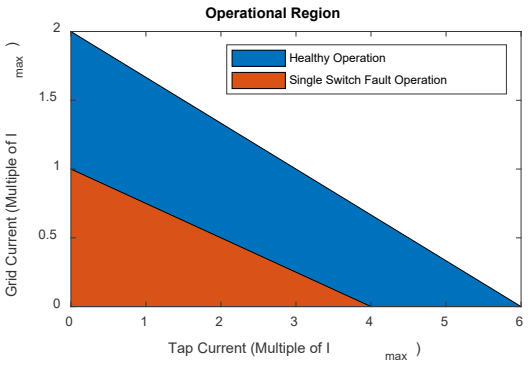



*Figure 15 - Operating Region Under Single Switch Fault*

## 2.3. Operation & Model Under Dual Switch Fault

When a dual switch fault occurs where the two faults are in different converters and on different phases, neither 2L-VSC is capable of maintaining balanced 3-phase current by itself. It is therefore necessary to run unbalanced AC current through both converters, such that balanced AC currents result at the PCC, while processing DC current through the single remaining healthy phase in both converters to avoid transformer saturation. An example is shown in Figure 16 where phase A of converter 0 and phase B of converter 1 are both faulted.

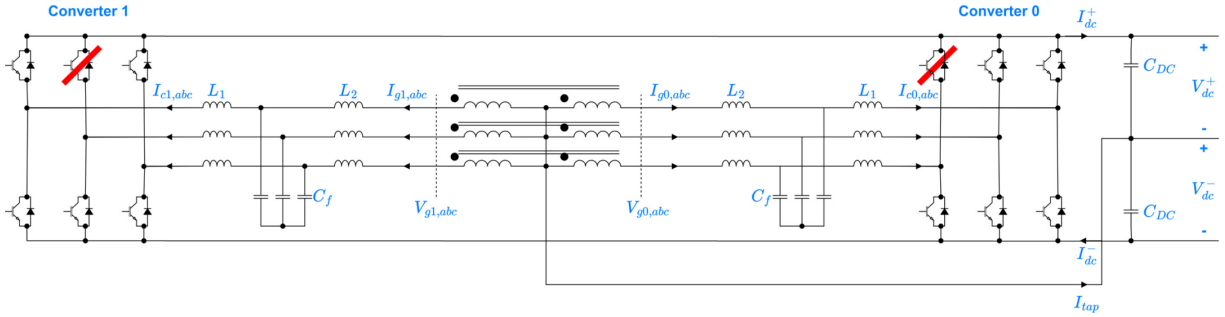



*Figure 16 - BGIC Under Dual Switch Fault, Different Phases*

The windings configuration of the three phase, centre-tapped transformer is shown in Figure 17. The grid current ($I_{g,abc}$) must be balanced and free of DC and low-order harmonics in order to maintain acceptable power quality. That is:

$$I_{ga} = i_g \cos\left(\omega_e t + \theta_{i_g}\right) \tag{42}$$

$$I_{gb} = i_g \cos\left(\omega_e t + \theta_{i_g} - 120^o\right) \tag{43}$$

$$I_{gc} = i_g \cos\left(\omega_e t + \theta_{i_g} + 120^o\right) \tag{44}$$

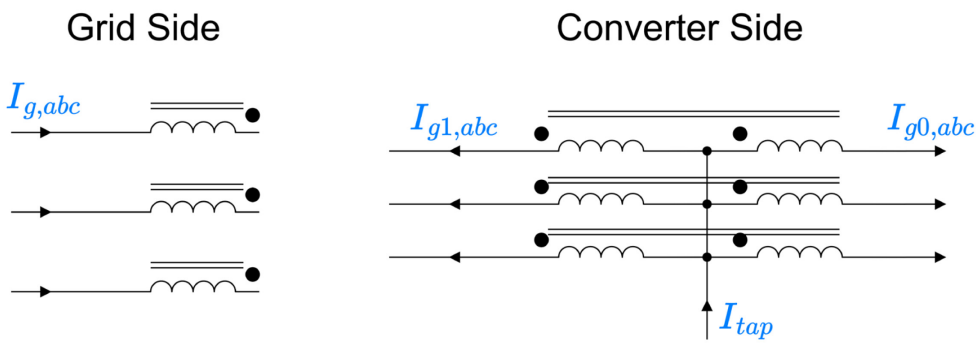



*Figure 17 - Centre-tapped Transformer Winding Configuration*

In addition, to avoid a large fundamental frequency AC component on the DC link, the common centre-tap point (connected to the DC link midpoint) must be a virtual ground – that is, all AC currents into this node must sum to zero – while the total tap current ($I_{tap}$) must be free of fundamental frequency AC.

The transformer current relationships are given by:

$$NI_{ga} = I_{g0a} - I_{g1a} \tag{45}$$

$$NI_{gb} = I_{g0b} - I_{g1b} \tag{46}$$

$$NI_{gc} = I_{g0c} - I_{g1c} \tag{47}$$

Where N is the ratio of turns on the primary winding to each secondary winding (2N:1:1 transformer). Here, the transformer magnetizing current has been neglected.

Imposing the restrictions in (45-47) to equations (42-44) yields

$$Ni_g \cos(\omega_e t + \theta_{ig}) = I_{g0a} - I_{g1a} \tag{48}$$

$$Ni_g \cos(\omega_e t + \theta_{ig} - 120^o) = I_{g0b} - I_{g1b} \tag{49}$$

$$Ni_g \cos(\omega_e t + \theta_{ig} + 120^o) = I_{g0c} - I_{g1c} \tag{50}$$

$$\sum_{i=a,b,c} (i_{g0i} + i_{g1i}) = 0 \tag{51}$$

In addition, in order to avoid transformer core saturation, the DC current must sum to zero in each set of secondary windings:

$$I_{G0A} = I_{G1A} \tag{52}$$

$$I_{G0B} = I_{G1B} \tag{53}$$

$$I_{G0C} = I_{G1C} \tag{54}$$

Solving equations (48) through (54) yields the operating constraints for the example configuration, setting N = 1, as:

$$I_{g0a} = 0 \tag{55}$$

$$I_{g0c} = i_g \cos\left(\omega_e t + \theta_{i_g} - 120^o\right) \tag{56}$$

$$I_{g0c} = I_G - i_g \cos\left(\omega_e t + \theta_{i_g} - 120^o\right) \tag{57}$$

$$I_{g1a} = -i_g \cos\left(\omega_e t + \theta_{i_g}\right) \tag{58}$$

$$I_{g1c} = 0 \tag{59}$$

$$I_{g1c} = I_G + i_g \cos\left(\omega_e t + \theta_{i_g}\right) \tag{60}$$

Where the DC current is calculated as:

$$I_G = \frac{I_{TAP}}{2} \tag{61}$$

The positive DC link current is expressed by:

$$I_{dc}^{+} = \sum_{i=0a,0b,0c,1a,1b,1c} \frac{M_i + 1}{2} I_{gi} \tag{62}$$

Equation (62) can be expanded as:

$$
\begin{aligned}
I_{dc}^{+} = &-\frac{m_{1a} i_g}{4}\left[\cos\left(2\omega_e t + \theta_{m1a} + \theta_{ig}\right) + \cos\left(\theta_{m1a} - \theta_{ig}\right)\right] \\
&+\frac{m_{0b} i_g}{4}\left[\cos\left(2\omega_e t + \theta_{m0b} + \theta_{ig} - 120^o\right) + \cos\left(\theta_{m0b} - \theta_{ig} + 120^o\right)\right] \\
&+\frac{m_{1c} i_g}{4}\left[\cos\left(2\omega_e t + \theta_{m1c} + \theta_{ig}\right) + \cos\left(\theta_{m1c} - \theta_{ig}\right)\right] \\
&-\frac{m_{0c} i_g}{4}\left[\cos\left(2\omega_e t + \theta_{m0c} + \theta_{ig} - 120^o\right) + \cos\left(\theta_{m0c} - \theta_{ig} + 120^o\right)\right] \\
&-\frac{i_g}{2}\cos\left(\omega_e t + \theta_{ig}\right) + \frac{i_g}{2}\cos\left(\omega_e t + \theta_{ig} - 120^o\right) + \frac{i_g}{2}\cos\left(\omega_e t + \theta_{ig}\right) \\
&-\frac{i_g}{2}\cos\left(\omega_e t + \theta_{ig} - 120^o\right) + \frac{M_{1C}}{2}\left[i_g \cos\left(\omega_e t + \theta_{ig}\right) + I_G\right] \\
&+\frac{M_{OC}}{2}\left[-i_g \cos\left(\omega_e t + \theta_{ig} - 120^o\right] + I_G\right) \\
&+\frac{I_G}{2}\left[2 + m_{0c}\cos(\omega_e t + \theta_{m0c}) + m_{1c}\cos(\omega_e t + \theta_{m1c})\right]
\end{aligned}
\tag{63}
$$

When operating near unity power factor, the grid current is nearly in phase with the grid voltage, which is taken as the 0-degree reference; therefore:

$$\theta_{ig} \cong 0 \tag{64}$$

In comparison to the AC portion of the modulation signal, which tends around 1, the DC portion, from equation (18), is very small:

$$M_x = \frac{2(R_1 + R_2) I_{GX}}{V_{dc}} \ll 1 \quad x = a, b, c \tag{65}$$

Thus, the fundamental frequency components resulting from these cross terms can be neglected.

Applying approximations (64) and (65) to (63) yields:

$$I_{dc}^{+} \cong \frac{i_g}{4} \sum_{i=1a,0b,1c,0c} S_i m_i \cos(2\omega_e t + \theta_{mi} + \theta_i) + \frac{i_g}{4} \sum_{i=1a,0b,1c,0c} S_i m_i \cos(\theta_{mi} + \theta_i)$$

$$+ \frac{I_G}{2} [m_{1c} \cos(\omega_e t + \theta_{m1c}) + m_{0c} \cos(\omega_e t + \theta_{m0c})] + I_G \quad (66)$$

Where:

$$S_{1a} = -1$$

$$S_{0b} = 1$$

$$S_{1c} = 1$$

$$S_{0c} = -1$$

$$\theta_{1a} = \theta_{1c} = 0^o$$

$$\theta_{0b} = \theta_{0c} = 120^o$$

The first summation in (66) is the second harmonic ripple (undesired), the second summation is the DC current produced by AC->DC power transfer (desired), while the remaining two terms are fundamental frequency ripple (undesired) and DC current produced by DC->DC power transfer (desired).

Looking at the fundamental frequency ripple current,

$$i_{60Hz} \cong \frac{I_G}{2}\left[m_{1c}\cos(\omega_e t + \theta_{m1c}) + m_{0c}\cos(\omega_e t + \theta_{m0c})\right] \tag{67}$$

It depends on the AC and DC currents, as well as the modulation indexes of the entirely healthy arm pair. These can be calculated as:

$$\bar{m}_{0c} \cong \frac{\bar{v}_{0c} - (L_2 + L_1)j\omega_e \bar{\imath}_{g0c}}{\frac{V_{dc}}{2}} = \frac{v_{ln}\angle 120^o - (L_2 + L_1)\omega_e \angle 90^o \cdot (-1) i_g \angle -120^o}{\frac{V_{dc}}{2}} \tag{68}$$

$$\bar{m}_{1c} \cong \frac{\bar{v}_{1c} - (L_2 + L_1)j\omega_e \bar{\imath}_{g1c}}{\frac{V_{dc}}{2}} = \frac{-v_{ln}\angle 120^o - (L_2 + L_1)\omega_e \angle 90^o \cdot i_g \angle 0^o}{\frac{V_{dc}}{2}} \tag{69}$$

$$|\bar{m}_{0c} + \bar{m}_{1c}| \cong \frac{2(L_1 + L_2)}{\frac{V_{dc}}{2}}\omega_e i_g \tag{70}$$

Substituting (70) into (67) yields an upper limit on the magnitude of the fundamental frequency ripple:

$$|i_{60Hz}| \leq \frac{I_G}{2}\left(\frac{(L_1 + L_2)}{V_{dc}}\omega_e i_g\right) = I_G \frac{(L_1 + L_2)\omega_e}{V_{dc}} i_g \tag{71}$$

Thus, the fundamental frequency ripple is proportional to both the AC grid current and the DC tap current. A similar analysis on the second harmonic ripple current shows that it is proportional to the AC grid current and not the DC tap current.

Taking the same approach for calculating maximum power transfer as in equations (38) through (41) for the single switch fault operation, under dual switch fault operation, the tap current is split between 2 phase legs instead of 6, and the grid current is supported by a single phase leg, instead of 2. The current in the healthy phase of both converters is then given as:

$$I_{c1a} \cong I_{g1a} = \frac{I_{TAP}}{2} - i_g \cos\left(\omega_e t + \theta_{i_g}\right) \tag{72}$$

This results in the dual switch fault operation limiting equation:

$$\frac{I_{TAP}}{2} + i_g \leq I_{max} \tag{73}$$

The operating region under healthy and dual switch fault operation are shown in Figure 18; the maximum power transfer during a dual switch fault is limited to between 0.33PU and 0.5PU.

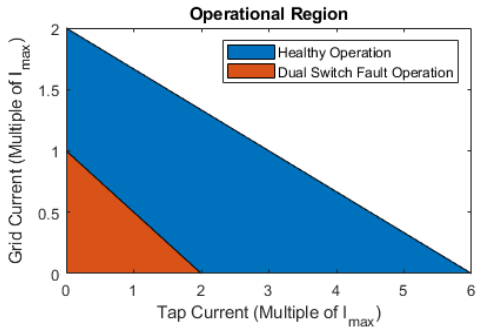



*Figure 18 - Operating Region Under Single Switch Fault*

## 2.4. Operational States of the BGIC

Compared to the original controls in [12], using the constraints developed in this section, the BGIC is capable of continued operation under single and dual switch faults, provided that the dual faults do not occur within the same phase. Table 1 provides a summary of the states in which the BGIC can operate under the original controls and under the constraints proposed in this chapter.

Table 1 - Operating Abilities Under Open-Circuit Switching Faults

| Converter Condition | Original Controls | | | Proposed Constraints | | |
|---|---|---|---|---|---|---|
| | Balanced AC Grid Current | Maximum Power Transfer | DC Link Pole Balancing | Balanced AC Grid Current | Maximum Power Transfer | DC Link Pole Balancing |
| No Fault | Yes | 1.0PU | Yes | Yes | 1.0PU | Yes |
| Single Fault | No | - | - | Yes | 0.5PU | Yes |
| Dual Fault – Same Converter | No | - | - | Yes | 0.5PU | Yes |
| Triple Fault – Same Converter | No | - | - | Yes | 0.5PU | No |
| Dual Fault, Different Converter, Same Phase | No | - | - | No | - | - |
| Dual Fault, Different Converter, Different Phase | No | - | - | Yes | 0.33-0.5PU | Yes |
| Triple Fault, Differenct Converters | No | - | - | No | - | - |

## 2.5. Magnetic Model of Three-Phase Centre-Tap Transformer

A key consideration in the BGIC operation is that the centre-tapped transformer must not be subjected to DC flux in any limb – if it is, the transformer can become saturated and no longer effectively carry the AC current. In the original controls presented in [12], the DC current through every secondary winding was equal in magnitude, with all of the current flowing either into the centre point or out of the centre point. In this way, the DC current cancelled at the midpoint, and saturation was avoided.

This work however removes the constraint that all three phases need to carry DC current of the same magnitude – at times, it is necessary for a single phase to carry no DC current, or for a single phase to carry all of the DC current. Using the magnetic modelling techniques in [23], a five-limb, three-phase centre-tapped transformer, such as shown in Figure 19, is modelled as a magnetic circuit in Figure 20. The AC and DC components of the flux are separated, in accordance with the superposition principle, to provide clarity on the cancellation.

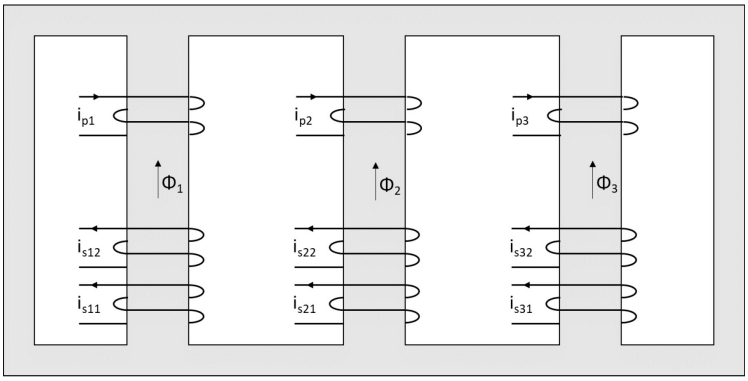



*Figure 19 - Five-Limb, Three-Phase Centre-Tapped Transformer Winding Arrangement*

The magnetomotive force resulting from the current on each winding is represented by $F_{xyz}$ where X is the winding designation (primary or secondary), Y is the winding location (upper or lower for

secondary), and Z is the limb number. The magnetic flux resulting in each limb is represented by $\Phi_z$. Provided that the constraint:

$$F_{slz,dc} = -F_{suz,dc} \tag{74}$$

Holds for each limb (z = 1,2,3) individually, the magnetic flux in the limb is a result of only the magnetomotive force resulting from the AC current. Therefore, the constraint on the DC currents can be written as:

$$I_{G0A} = -I_{G1A} \tag{75}$$

$$I_{G0B} = -I_{G1B} \tag{76}$$

$$I_{G0C} = -I_{G1C} \tag{77}$$

This presents a unique advantage of the BGIC over balancing bipolar DC converters that use a zig-zag transformer, such as in [24], as the zig-zag winding arrangement requires equal DC current to flow in all three phases to avoid core DC flux saturation.

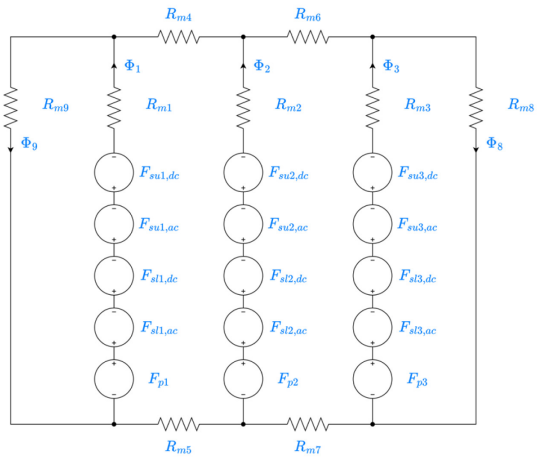



*Figure 20 - Magnetic Model of Transformer*

## 2.6. Summary

The Bipolar DC Grid Interfacing Converter proposed in [12], a multiport (AC-DC-DC) converter topology comprising two, 2-level VSCs, has been introduced. A time averaged model of the converter has been used to derive equations for the fundamental frequency grid currents as well as the DC link current under healthy operation and single & dual open-circuit switch faults. Constraints to ensure balanced AC grid currents as well as reduced ripples on the DC link have been derived for single and dual fault operation. A magnetic model has been analyzed to confirm transformer saturation due to DC flux bias is prevented during faulted operation.

# 3. Control Strategy

In order to control both the transient and steady-state response of the BGIC, it is first necessary to develop models and derive transfer functions, linking the input (generally a current or voltage reference) to the output (a measured voltage or current, respectively). Two implementations are developed here, differing on which reference frame is used for the current level control of the individual 2L-VSCs. The first operates in the ABC frame, using a reference current calculated in a stationary (αβ) frame, while the second operates in a synchronous (DQ) reference frame, with the reference current calculated in the same reference frame. As the control loops are tuned to have a closed-loop bandwidth in the neighborhood of the grid frequency and the switching is done at a substantially higher frequency, time-averaged models are developed that neglect the switching harmonics.

## 3.1. ABC Frame Control

Under ABC frame control, a current control loop is implemented for each phase of each 2L-VSC (a total of 6 inner controllers for the BGIC), using a proportional-integral-resonant (PIR) controller which is capable of tracking both DC and fundamental frequency reference commands. Two outer loop voltage controllers determine the AC grid current and DC tap current references, respectively, based on the sum and difference of the two DC link capacitor voltages. These reference signals are modified by the fault control supervisor in order to generate the required converter current references. An additional outer loop controller is implemented during a single fault event, modifying the AC converter current reference of the healthy phase legs in the faulted converter to drive the AC portion of the current to zero.

### 3.1.1. Converter Plant Modelling

In order to control the DC link voltage, the DC side of the BGIC in Figure 8 is modelled by the circuit in Figure 21, with the load currents being treated as disturbances (that is, the load current is taken as zero for the purpose of determining the plant transfer function). As the load currents are nominally DC, aside from moments of switching, they are expected to be constant when considering a short time period (that is, they may change, but it is expected to be a slow enough change that from the control system perspective, it is a constant). From this circuit, KCL are used to derive equations for the DC currents, as:

$$I_{DC}^{+} = C_{DC}\dot{V}_{DC}^{+} + I_{LOAD}^{+} \tag{78}$$

$$I_{DC}^{-} = C_{DC}\dot{V}_{DC}^{-} + I_{LOAD}^{-} \tag{79}$$

$$I_{TAP} = I_{DC}^{+} - I_{DC}^{-} - I_{LOAD}^{+} + I_{LOAD}^{-} \tag{80}$$

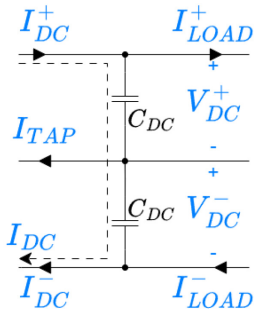



*Figure 21 - DC Link Plant Circuit*

Rearranging (78-80) and transforming into the Laplace domain yields:

$$\boldsymbol{V_{DC}} = \frac{\boldsymbol{I_{DC}^{+} + I_{DC}^{-}}}{sC_{DC}} = \frac{2\boldsymbol{I_{DC}}}{sC_{DC}} \tag{81}$$

$$\boldsymbol{V_{DIFF}} = \frac{\boldsymbol{I_{DC}^{+} - I_{DC}^{-}}}{sC_{DC}} = \frac{\boldsymbol{I_{TAP}}}{sC_{DC}} \tag{82}$$

Where $V_{DIFF}$ is the pole-to-pole voltage difference, $V_{DC}$ is the combined DC link voltage, $I_{DC}$ is the common mode DC current, and $I_{TAP}$ is the differential mode DC current. The two DC link plant models are then given by the following transfer functions:

$$\boldsymbol{G_{DC}} = \frac{\boldsymbol{V_{DC}}}{\boldsymbol{I_{DC}}} = \frac{2}{sC_{DC}} \qquad (83) \qquad\qquad \boldsymbol{G_{DIFF}} = \frac{\boldsymbol{V_{DIFF}}}{\boldsymbol{I_{TAP}}} = \frac{1}{sC_{DC}} \qquad (84)$$

The common mode DC current ($I_{DC} = \frac{I_{DC}^{+} + I_{DC}^{-}}{2}$) is used to calculate the AC grid current reference, through the power balance equation (assuming unity power factor operation):

$$P_{AC} = \frac{3V_{LL}}{\sqrt{3}} \frac{\hat{\imath}_g}{\sqrt{2}} = P_{DC} = V_{DC} I_{DC} \qquad (85)$$

The differential mode DC current ($I_{TAP} = I_{DC}^{+} - I_{DC}^{-}$) is directly used as the tap current.

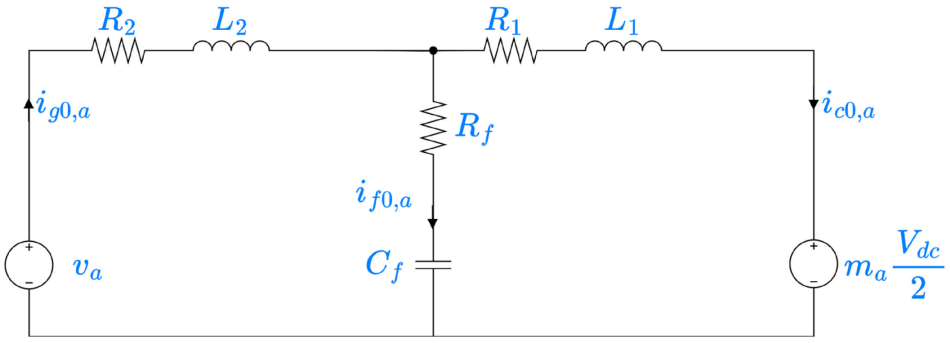



*Figure 22 - 2L-VSC Time Averaged Model, ABC Frame*

Each 2L-VSC is then modelled independently on the AC side using a time averaged approach – presented in chapter 2, shown again in Figure 22. The converter current is solved from (18), as:

$$\boldsymbol{I_{g0,a}} = -\left[\frac{Z_f + Z_1}{Z_f}\boldsymbol{V_a} - \frac{\boldsymbol{M_a} V_{DC}}{2}\right] \frac{-Z_f}{Z_1 Z_2 + Z_f(Z_1 + Z_2)} \qquad (86)$$

With:

$$Z_f = R_f + \frac{1}{sC_f} \qquad (87)$$

$$Z_1 = R_1 + sL_1 \qquad (88)$$

$$Z_2 = R_2 + s_{L_2} \qquad (89)$$

The plant model transfer function for the AC converter current is then extracted as:

$$\boldsymbol{G_I} = \frac{\boldsymbol{I_{g0}}}{\boldsymbol{U}} = -\frac{Z_f}{Z_1 Z_2 + Z_f(Z_1 + Z_2)} \qquad (90)$$

Where U is the virtual input, defined as:

$$\boldsymbol{U} = -\frac{Z_f + Z_1}{Z_f}\boldsymbol{V_a} + \frac{V_{DC}}{2}\boldsymbol{M_a} \tag{91}$$

The controller / plant arrangement is then as shown in Figure 23, where the virtual control signal U is generated by the compensator and transformed to the modulating signal **M** prior to being passed to the converter in the form of a PWM signal.

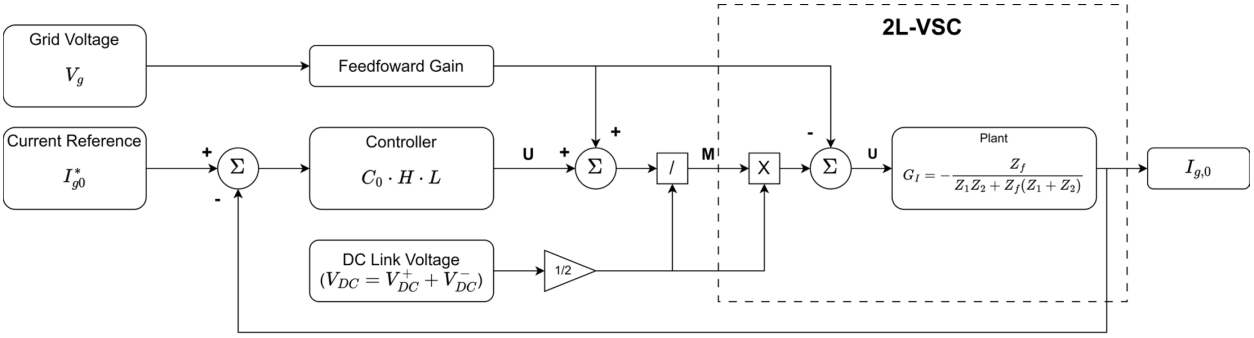



*Figure 23 - ABC Frame Current Controller Arrangement*

## 3.1.2. Converter Current Control Loop

The current control loop, shown in Figure 23, employs a Proportional Integral Resonant (PIR) compensator, designed using the method in [25]. That is, the plant can be written as:

$$\boldsymbol{G_I} = \frac{\boldsymbol{I_{g0}}}{\boldsymbol{U}} = \frac{K_G(s + z_1)}{(s + p_1)(s + p_2)(s + p_3)} \tag{92}$$

Since all poles are located in the open left-half plane and are thus stable, they can be cancelled by zeros in the controller. This allows for more arbitrary shaping of the closed loop transfer function and therefore the time-domain response of the system. The initial controller is then given as:

$$\boldsymbol{C_0} = \frac{(s + p_1)(s + p_2)(s + p_3)}{(s^2 + 0.2\omega_e s + \omega_e^2)s} \tag{93}$$

It is augmented by a 2nd order Butterworth low-pass filter with a cutoff frequency of $0.1 \cdot f_s$ which helps the system reject the switching noise, of the form:

$$\boldsymbol{H} = \frac{K_h}{s^2 + h_1 s + h_2} \tag{94}$$

Finally, a lead compensator is added to increase the phase margin at crossover to ensure stability, of the form:

$$\boldsymbol{L} = \left( \frac{s + \frac{p_l}{\alpha}}{s + p_l} \right)^{n_l} \tag{95}$$

The system is tuned to have an open-loop magnitude of 0dB and a phase margin greater than 60° at a crossover frequency near $0.1 \cdot f_s$. The final controller has the form:

$$\boldsymbol{C_I} = \boldsymbol{C_0} \cdot \boldsymbol{H} \cdot \boldsymbol{L} = k \frac{(s + p_1)(s + p_2)(s + p_3)}{(s^2 + 0.2\omega_e s + \omega_e^2)s} \cdot \frac{K_h}{(s^2 + h_1 s + h_2)} \cdot \left( \frac{s + \frac{p_l}{\alpha}}{s + p_l} \right)^{n_l} \tag{96}$$

For the system used in this work, the resulting parameters are listed in Table *2*. The Bode plot of the controller ($C_I$) and system closed loop $\left(\frac{C_I G_I}{1 + C_I G_I}\right)$ are shown in Figure 24.

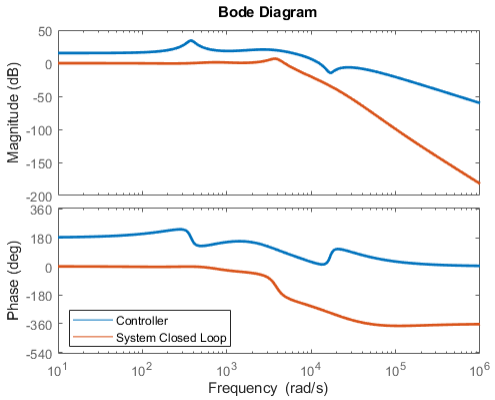



*Figure 24 - Bode Plot for Current Controller, Current Closed Loop System*

Table 2 - Control System Parameters, ABC Implementation

| Current Control Loop | |
|---|---|
| **Parameter** | **Value** |
| $k$ | 98.522 |
| $p_1$ | -1400+16675j |
| $p_2$ | -1400-16675j |
| $p_3$ | -0.3143 |
| $\omega_e$ | $2\pi 60$ |
| $K_h$ | $9.87 \cdot 10^6$ |
| $h_1$ | 4443 |
| $h_2$ | $9.87 \cdot 10^6$ |
| $p_l$ | 17817 |
| $\alpha$ | 32.163 |
| $n_l$ | 3 |

| Voltage Control Loop | |
|---|---|
| **Parameter** | **Value** |
| $k_{dc}$ | 0.7502 |
| $z_{dc}$ | 37.699 |
| $k_{diff}$ | 0.7502 |
| $z_{diff}$ | 37.699 |
| $k_{dc,f}$ | 0.1232 |
| $z_{dc,f}$ | 37.7 |
| $\omega_f$ | $\frac{\omega_e}{2} = \pi 60$ |

### 3.1.3. DC Link Voltage Control Loop

For the purposes of controlling the DC link voltage ($V_{DC} = V_{DC}^{+} + V_{DC}^{-}$) and voltage difference ($V_{diff} = V_{DC}^{+} - V_{DC}^{-}$), it is assumed that the current control loop acts sufficiently faster than the voltage control loop, and therefore the dynamics of the current control loop are negligible.

For control under healthy conditions, the same approach as used in [12] is used – that is, the controllers have the form:

$$\boldsymbol{C_{DC}} = k_{dc}\frac{(s + z_{dc})}{s} \tag{97}$$

$$\boldsymbol{C_{diff}} = k_{diff}\frac{(s + z_{diff})}{s} \tag{98}$$

The controller layout is shown in Figure 25.

Each loop is tuned such that the open-loop gain is unity at the crossover frequency ($\omega_c$), which is set equal to the fundamental grid frequency ($\omega_e$). The zero is chosen as one-tenth the crossover frequency. This provides fast response to changes in DC load without causing large disturbances to the grid current.

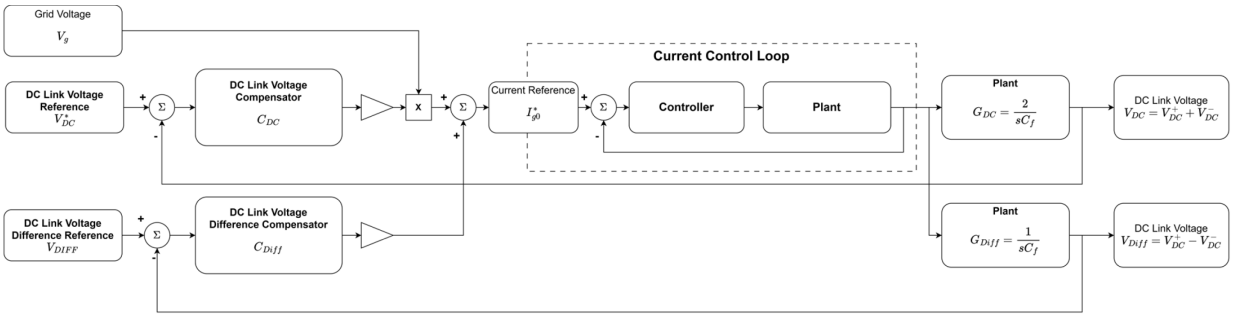



*Figure 25 – ABC Frame Voltage Controller Arrangement*

However, for faulted conditions, the DC link voltages are expected to have both fundamental and second harmonic frequency ripples due to the unbalanced operation of the individual 2L-VSCs, as explored in Chapter 2.3. These ripples should be treated as noise by the voltage control loops; therefore, the loops need to be slowed down during faulted operation, in addition to having high-frequency roll-off terms to attenuate the ripples. After a fault has occurred, the voltage compensators have the form:

$$\boldsymbol{C_{DC,FAULT}} = k_{dc,f}\frac{\left(s + z_{dc,f}\right)\omega_f^2}{s\left(s + \omega_f\right)^2} \tag{99}$$

Where the zero is still chosen as one-tenth the crossover frequency, but the crossover frequency is reduced to 1/5$^{th}$ the fundamental frequency. The filter frequency is chosen to be equal to ½ the fundamental frequency. Controller parameters for the system under test are given in Table *2*.

As seen in the closed-loop frequency response plot, Figure 26, the closed loop system with the healthy controller ($C_{DC}$) has little attenuation of fundamental and 2$^{nd}$ harmonic frequencies (-2dB and -7db, respectively), while with the faulted controller ($C_{DC,FAULT}$) it has significantly better attenuation (-32dB and -43dB, respectively).

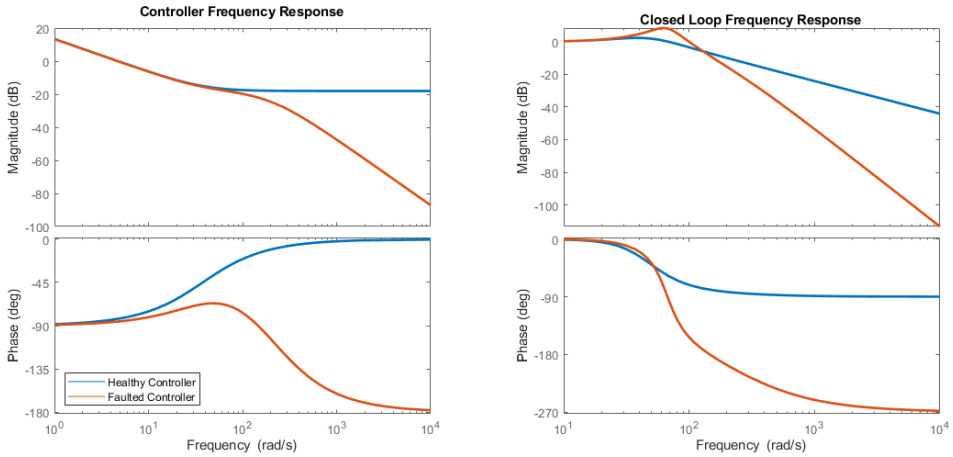



*Figure 26 – Bode Plots for Voltage Control Loop under Healthy and Faulted Operation*

The step response of the faulted controller is compared to that of the original controller in Figure 27, while the steady-state response of the two controllers to fundamental and second harmonic ripples is shown in Figure 28. While the faulted controller is substantially better at rejecting the ripples, it is significantly slower and more oscillatory when responding to step changes.

Figure 27 shows the step response of the two closed loops – the fast controller response is noticeably faster, with less oscillation. However, Figure 28 provides a comparison of the response to fundamental frequency and second harmonic frequency input – the healthy system is unable to reject the first and second order terms, while the faulted system is able to attenuate both to prevent DC link ripple from impacting control action. Due to this, it is necessary to use the faster, original controller during large transient changes and switch to the slower, fault controller once the system has stabilized, in order to have optimal steady-state performance.

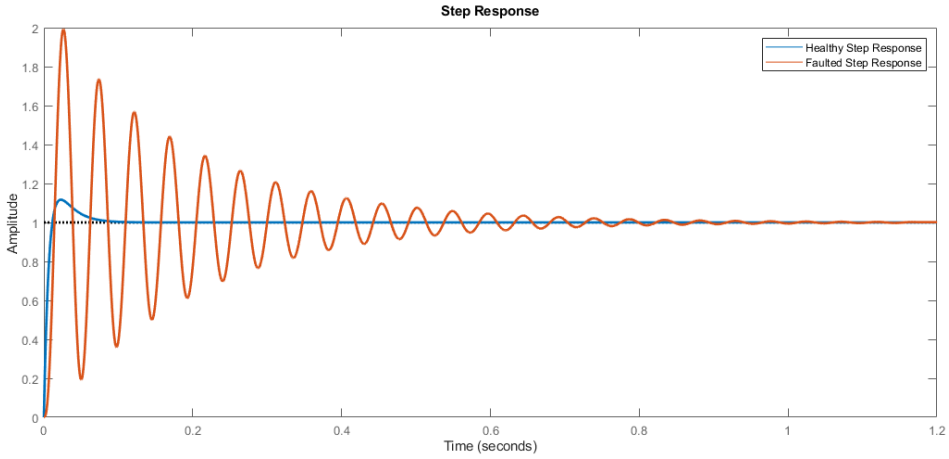



*Figure 27 - Step Response of Healthy and Faulted Closed-Loop Voltage Control*

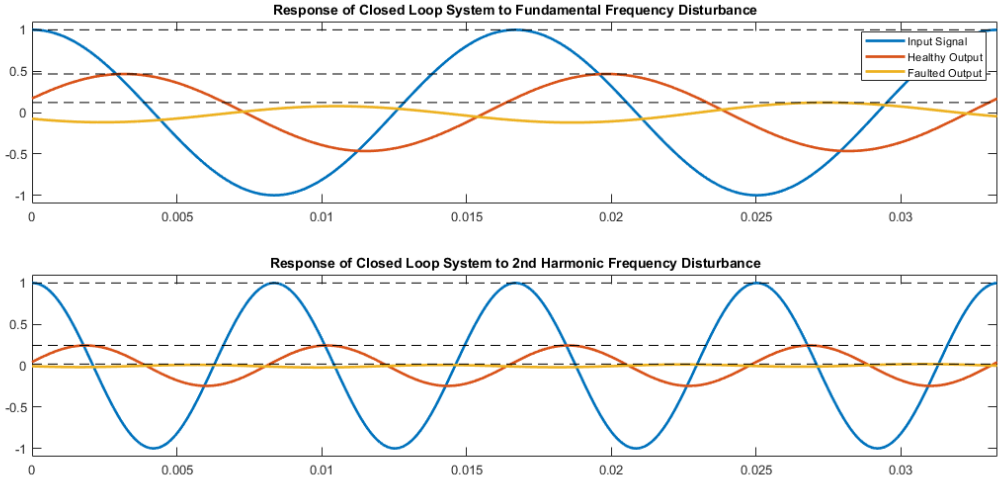



*Figure 28 - Response of Closed-Loop Voltage Control to Fundamental and 2nd Harmonic Noise*

In order to enable switching between the two controllers, they are each converted to the form:

$$\boldsymbol{C = A\frac{1}{s} + H} \tag{100}$$

This allows the integrator to be shared between the two controllers, with a variable input gain (A). Through this, when the switch occurs from one controller to the other, the integrator state is kept constant and there is no large jump in control output. The final controller arrangement is shown in Figure 29; note that the fault signal comes from the fault control supervisor. The entirety of Figure 29 replaces the DC link voltage compensator block in Figure 25. The same process is repeated for the DC link voltage difference compensator.

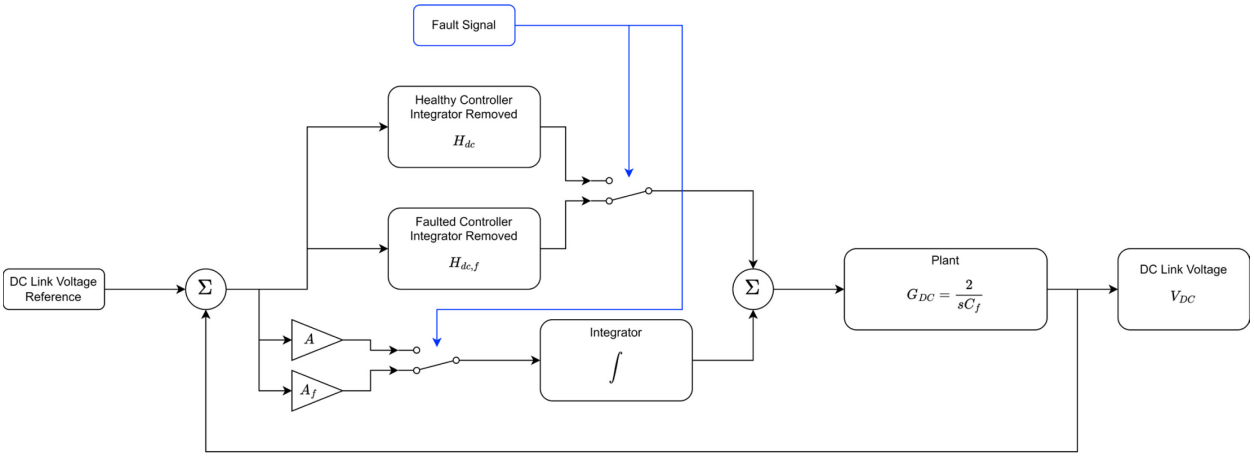



*Figure 29 - Variable Voltage Compensator Setup*

Finally, an additional outer loop control is implemented for the healthy phase legs of the faulted converter in a single-fault condition. Normally, the AC reference current is driven by the voltage controller, which compensates for any modelling errors (component variances, unmodelled dynamics, signal noise, etc) by adjusting the reference current based on the resulting DC voltage. However, when a single fault occurs and the AC current in one converter is reduced to zero, the reference current for that converter is no longer linked to the DC link voltage – it is instead fixed at zero. In order to ensure that the resulting AC current is indeed zero, an FFT is taken of each healthy leg current in the faulty converter, the fundamental component is isolated, and the magnitude is used as the input to an integral controller. The output of the integrator becomes the AC reference current for the leg.

### 3.1.4. Fault Control Supervisor

A fault control supervisor was built to oversee the operation of the BGIC and all compensators. Its purpose is to:

- Receive status signals for each phase leg (generated by a fault detection system, external to this work),
- Generate current reference signals (both AC and DC tap) for each phase leg, given the fault status and the constraints in Chapter 2,
- Determine the mode of operation of the variable voltage compensators, and
- Modify the gating signals to prevent signals being sent to faulted phase legs.

The AC reference current for each phase is determined according to a lookup table, based on the fault condition (Table *3*). The DC reference current is the desired tap current, generated by the DC voltage difference control loop, divided by the number of phase legs that are healthy in both

converters (e.g.., if phase leg 0A is faulted, 2 legs are healthy in both converters (B & C), while if phase leg 0A and 1B are faulted, there is 1 healthy leg in both converters (C)).

Table 3: AC Reference Current Lookup Table

| | Phase Leg Status | | | | | | Reference Current Output | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Converter 0 | | | Converter 1 | | |
| | 0A | 0B | 0C | 1A | 1B | 1C | A | B | C | A | B | C |
| *Single Fault* | | | | | | | $½ I_{ga}$ | $½ I_{gb}$ | $½ I_{gc}$ | $-½ I_{ga}$ | $-½ I_{gb}$ | $-½ I_{gc}$ |
| | X | | | | | | 0 | 0 | 0 | $-I_{ga}$ | $-I_{gb}$ | $-I_{gc}$ |
| | | X | | | | | 0 | 0 | 0 | $-I_{ga}$ | $-I_{gb}$ | $-I_{gc}$ |
| | | | X | | | | 0 | 0 | 0 | $-I_{ga}$ | $-I_{gb}$ | $-I_{gc}$ |
| | | | | X | | | $I_{ga}$ | $I_{gb}$ | $I_{gc}$ | 0 | 0 | 0 |
| | | | | | X | | $I_{ga}$ | $I_{gb}$ | $I_{gc}$ | 0 | 0 | 0 |
| | | | | | | X | $I_{ga}$ | $I_{gb}$ | $I_{gc}$ | 0 | 0 | 0 |
| *Dual Fault Same Converter* | X | X | | | | | 0 | 0 | 0 | $-I_{ga}$ | $-I_{gb}$ | $-I_{gc}$ |
| | X | | X | | | | 0 | 0 | 0 | $-I_{ga}$ | $-I_{gb}$ | $-I_{gc}$ |
| | | X | X | | | | 0 | 0 | 0 | $-I_{ga}$ | $-I_{gb}$ | $-I_{gc}$ |
| | | | | X | X | | $I_{ga}$ | $I_{gb}$ | $I_{gc}$ | 0 | 0 | 0 |
| | | | | X | | X | $I_{ga}$ | $I_{gb}$ | $I_{gc}$ | 0 | 0 | 0 |
| | | | | | X | X | $I_{ga}$ | $I_{gb}$ | $I_{gc}$ | 0 | 0 | 0 |
| *Dual Fault Different Converter* | X | | | | X | | 0 | $I_{gb}$ | $-I_{gb}$ | $-I_{ga}$ | 0 | $I_{ga}$ |
| | X | | | | | X | 0 | $-I_{gc}$ | $I_{gc}$ | $-I_{ga}$ | $I_{ga}$ | 0 |
| | | X | | X | | | $I_{ga}$ | 0 | $-I_{ga}$ | 0 | $-I_{gb}$ | $I_{gn}$ |
| | | X | | | | X | $-I_{gc}$ | 0 | $I_{gc}$ | $I_{gn}$ | $-I_{gn}$ | 0 |
| | | | X | X | | | $I_{ga}$ | $-I_{ga}$ | 0 | 0 | $I_{gc}$ | $-I_{gc}$ |
| | | | X | | X | | $-I_{gb}$ | $I_{gb}$ | 0 | $I_{gc}$ | 0 | $-I_{gc}$ |

The mode of operation of the variable voltage compensators is determined according to the following rules:

- If there is no fault active in either converter, the healthy compensator is used.
- If there is a fault active in either converter and the DC link voltage is stable, the faulted compensator is used.
- If there is a fault active in either converter and the DC link voltage is not stable, the healthy compensator is used.

Stable in terms of the DC link voltage is defined here as being within a tolerance of the reference value ($V_{tol}$) for the past $t_{tol}$ seconds. This allows the system to use the faster, healthy compensator to quickly return the DC voltage to the reference value while ensuring that DC voltage ripples do not cause low-order harmonics on the AC grid current during steady-state. The time requirement is to ensure that hysteresis does not occur when switching between the two compensators. Tuning these two parameters allows for a trade-off between the length and magnitude of transients on the DC link and the stability of the AC grid current during load changes, as seen in Figure 30. A tolerance of 10V was selected, as it allows for a rapid return to stable DC link voltage while maintaining AC grid current power quality.

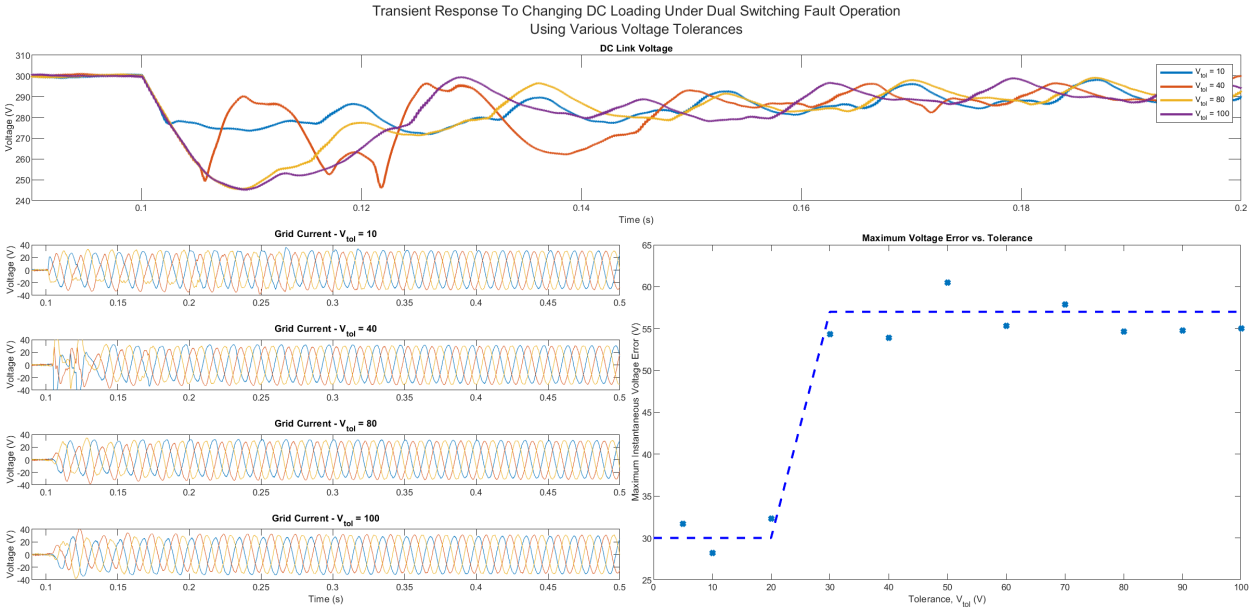



*Figure 30 - Transient Response of DC Link Voltage to Step Change in DC Load Under Various Switching Tolerances*

Finally, the fault supervisor blocks all gating pulses to phase legs that have a fault, to ensure that neither IGBT is switched on. Since each DC pole has a voltage in excess of the peak grid voltage, the antiparallel diodes will be reverse biased under steady-state conditions; therefore, the only current through the faulted phase leg will result from the filter capacitance. This was calculated in (34) and is negligible in comparison to the AC grid current.

### 3.1.5. Simulation Results

The ABC control implementation is tested in simulation using a NovaCor Real Time Digital Simulator (RTDS) and the BGIC parameters from [12], summarized in Table *4*.

Table 4: Test Systems Parameters

| Parameter | Symbol | Value |
|---|---|---|
| Grid RMS Line Voltage | $v_{grid,rms,line}$ | 160V |
| Grid Frequency | $f_{grid}$ | 60Hz |
| Transformer Turns Ratio | 1:1:2N | 1:1:2 |
| DC Link Voltage | $v_{dc}$ | 300V |
| DC Link Capacitance per Pole | $C_{dc}$ | 4mF |
| Rated AC Current per Valve | $I_{max}$ | 30A |
| Switching Frequency | $f_{sw}$ | 5kHz |
| Converter Side LCL Filter Inductance | $L_1$ | 2.5mH |
| Transformer Side LCL Filter Inductance | $L_2$ | 1mH |
| Converter Side LCL Filter Resistance (includes on-resistance of valves) | $R_1$ | 0.1mΩ |
| Transformer Side LCL Filter Resistance | $R_2$ | 0.1mΩ |
| LCL Filter Capacitance | $C_f$ | 5μF |
| LCL Filter Damping Resistance | $R_f$ | 2Ω |

Due to the real-time nature of the RTDS, initial conditions at controller startup are not easily implemented. Instead, a pre-charge system was built into the controllers – consisting of a grid connect breaker, a set of pre-charge resistors & bypass breakers, and a control routine. A breaker connecting the converter to the grid is closed at a particular point in the voltage waveform (to ensure repeatability), following which the converter acts as an LCC (due to the antiparallel diodes). The DC link voltage increases, while the current is limited by the pre-charge resistors. Once the DC link voltage has reached a percentage of its normal operating range, the pre-charge resistors are bypassed and the normal controls are activated. This startup routine is shown in Figure 31, with both poles set to consume 0.5PU power. While the grid current experiences significant harmonics during startup, it is a brief window and the maximum current is limited to ensure the semiconductor switches are not damaged.

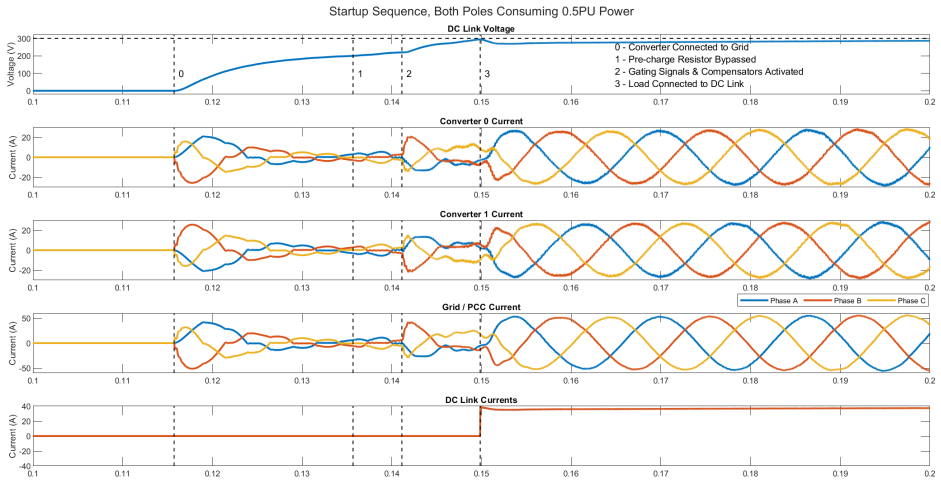



*Figure 31 – Startup Sequence*

Once the BGIC is energized, three main scenarios are considered:

- **(A)** Both DC poles consuming 0.25PU power (therefore the AC and DC power transfers are 0.5PU and 0PU, respectively). This is the highest AC power transfer that can be sustained under fault conditions.
- **(B)** One DC pole consuming 0.25PU power, the other producing 0.25PU power (therefore the AC and DC power transfers are 0PU and 0.5PU, respectively). This is the highest DC power transfer that can be sustained under fault conditions.
- **(C)** One DC pole consuming 0.375PU power, the other producing 0.125PU power (therefore the AC and DC power transfers are 0.25PU and 0.25PU, respectively). This is the worst-case scenario for DC link capacitor voltage ripple, as both AC and DC power transfers are maximized.

Under each scenario, the transient and steady-state response is analyzed under several conditions:

- No fault (healthy operation)
- A single fault occurring (no fault to single fault)
- A second fault occurring (single fault to dual fault)

Figure 32 identifies the AC and DC power transfers within the BGIC, for clarity.

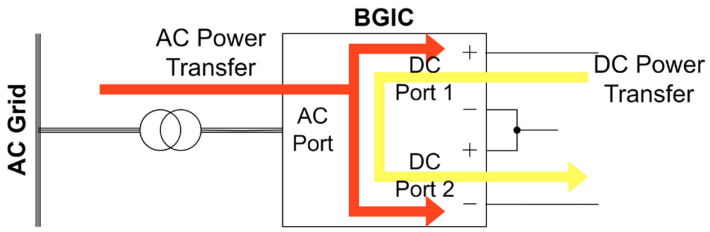



*Figure 32 – AC / DC Power Transfer in BGIC*

Figure 33 and Figure 34 show the transient and steady-state response for scenario A with a single switching fault occurring at t = 0.1s. The DC link voltage falls rapidly due to the loss of AC power transfer from the faulted converter (here, converter 0). The voltage controller attempts to compensate, resulting in the spike in the grid current. Since the system is already operating near the maximum AC power transfer, there is little room for the controller to increase the grid current, and the DC link voltage remains depressed until the healthy converter (here, converter 1) can increase its current flow to compensate. However, once the controls compensate, the DC link voltage is stable and free of ripple while the grid current is balanced and free of low-order harmonics.

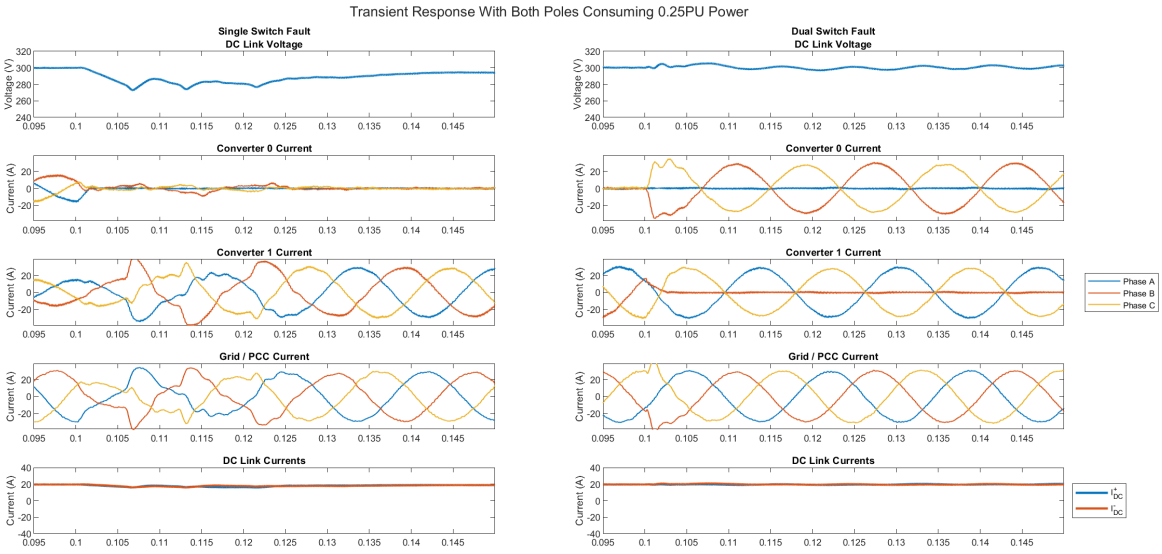



*Figure 33 - Transient Response to Faults, Both Poles Consuming 0.25PU Power (Scenario A)*

For the dual switch fault case, a single switch fault has previously occurred (phase A of converter 0) and the system has reached steady-state operation. At t = 0.1s, a second switch fault occurs (phase B of converter 1); the change for the previously healthy inverter (here, converter 1) is minimal (a phase shift of one phase, no change to the remaining phases). This helps to reduce the transient spike in the DC link voltage. At steady-state, the DC link voltage is stable with a relatively small 2nd harmonic ripple while the grid current is balanced and free of low-order harmonics.

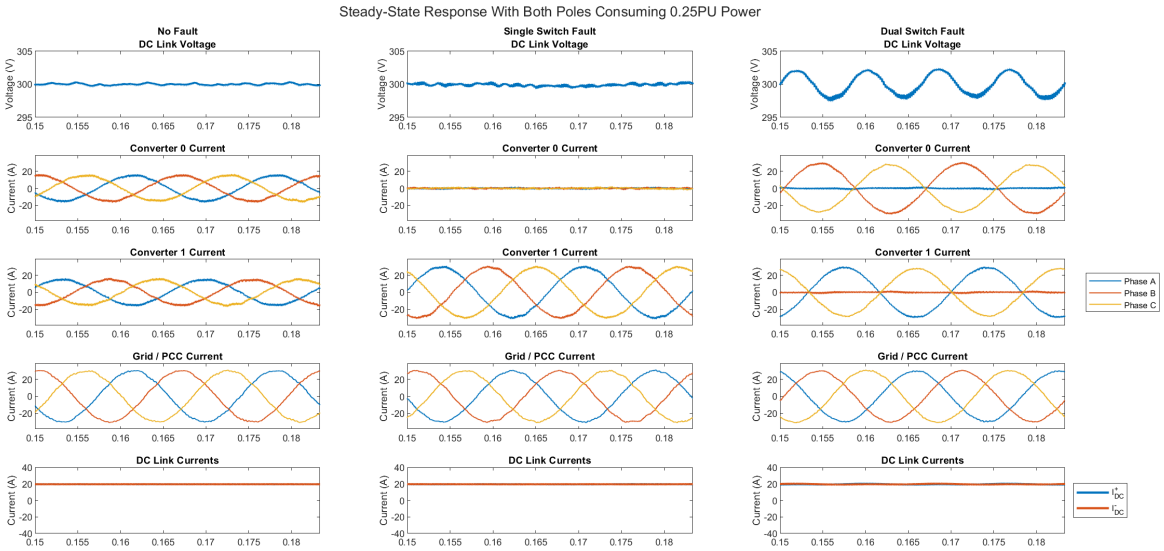



*Figure 34 - Steady State Response with Both Poles Consuming 0.25PU Power (Scenario A)*

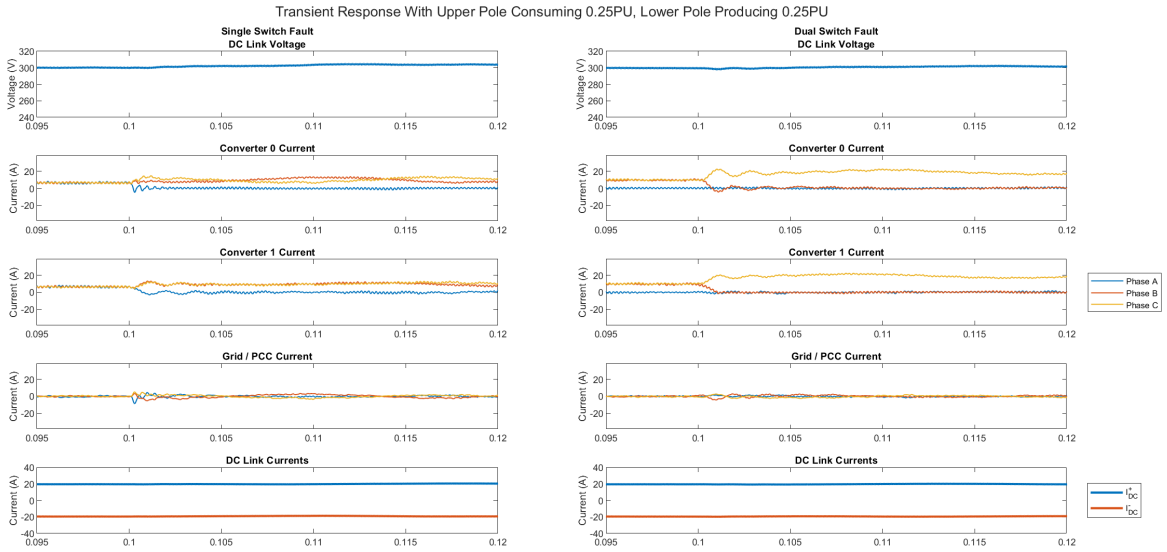



*Figure 35 - Transient Response with One Pole Consuming, One Pole Producing Power (Scenario B)*

Figure 35 and Figure 36 show the same responses for maximum DC power transfer. As there is no change in the AC power transfer due to the fault, the impact on the DC link voltage is minimal, and the system quickly compensates for the imbalance between the two pole voltages.

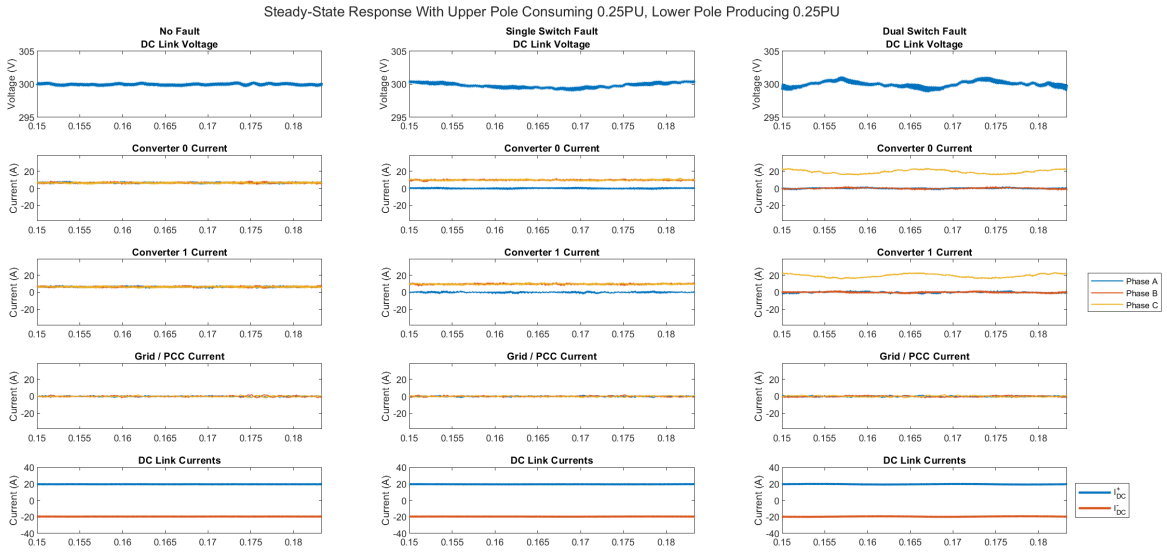



*Figure 36 - Steady State Response with One Pole Consuming, One Pole Producing Power (Scenario B)*

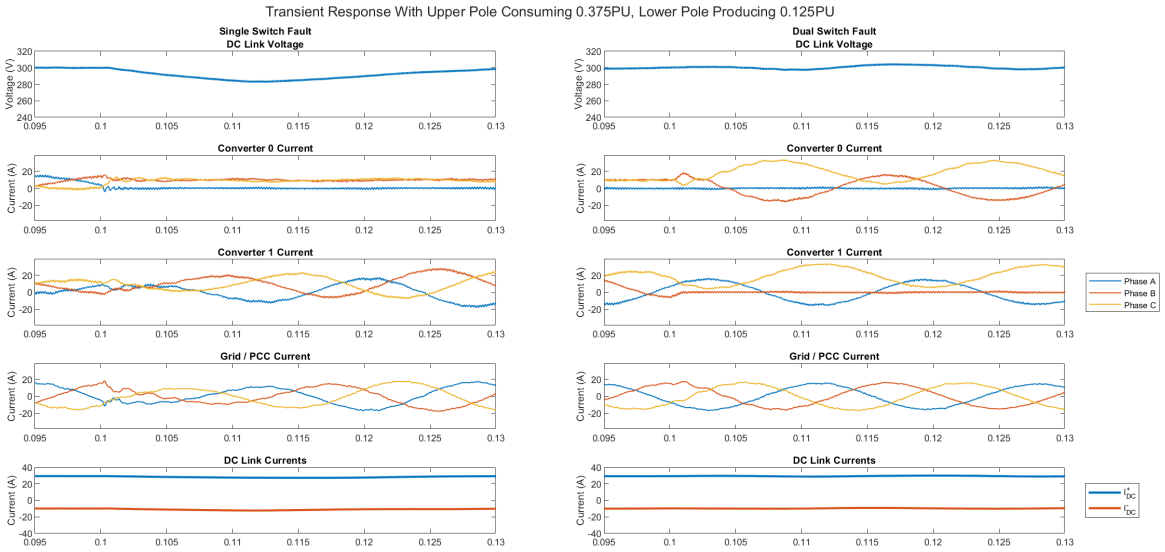



*Figure 37 - Transient Response with AC and DC Power Transfer (Scenario C)*

Figure 37 and Figure 38 show the same response when the AC and DC power transfers are both at maximum. Again the system responds quickly, though the change in AC power transfer as a result of the fault causes a slight sag in the DC link voltage during the single switch fault event.

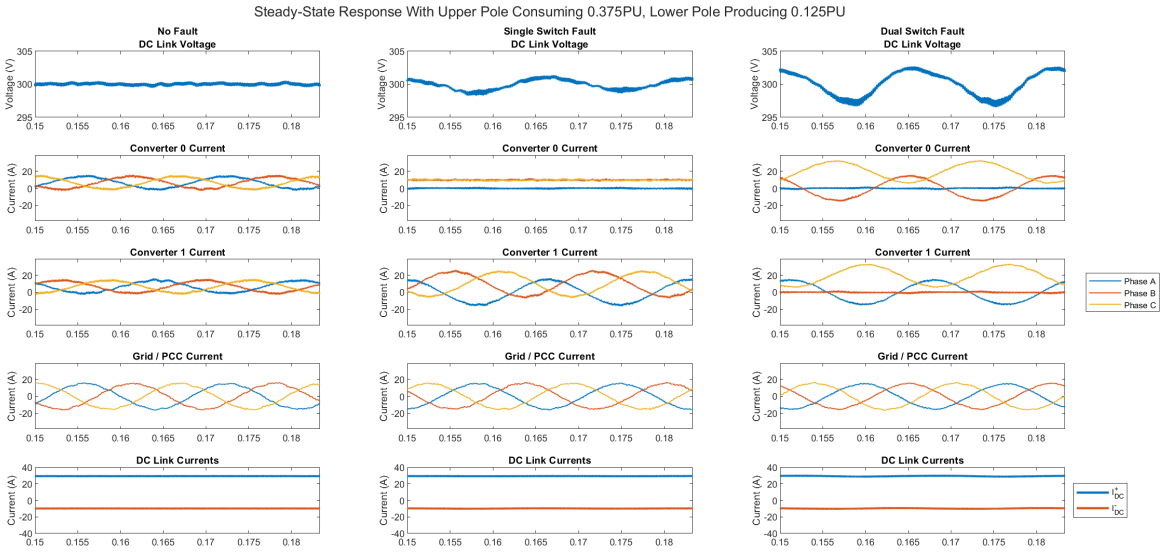



*Figure 38 - Steady State Response with AC and DC Power Transfer (Scenario C)*

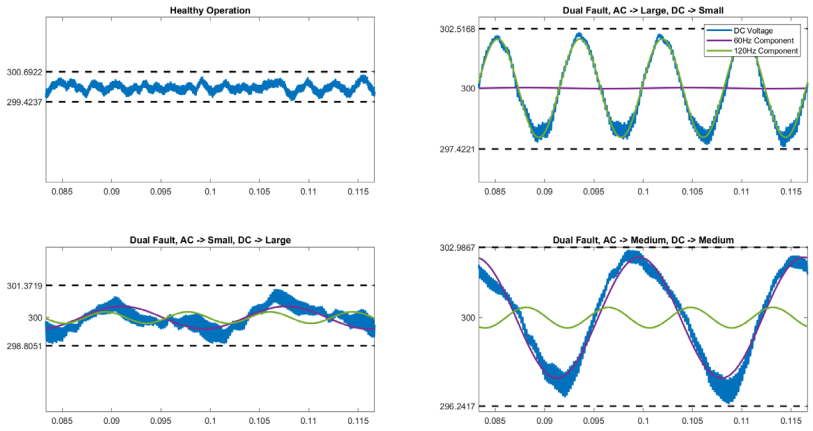



*Figure 39 - Comparison of DC Link Ripple Under Dual Fault Conditions for Various Power Transfers*

As shown in (71), the DC link ripple is proportional to the magnitude of both the AC and DC converter current. The 120Hz ripple is primarily driven by the AC power transfer, while the 60Hz is driven by the product of the AC and DC power transfers. This is elucidated in Figure 39, where under healthy operation, no low-order ripple is seen (upper left). When the AC and DC power transfers are high and low, respectively (upper right), the 120Hz component dominates the ripple. When the AC and DC power transfers are low and high, respectively (lower left), neither component dominates. When the AC and DC power transfers are both significant (lower right), the 60Hz component dominates.

Finally, the system is exposed to load changes on one DC pole – small and large changes in DC current magnitude without a change in direction, as well as a change from consuming DC power to producing DC power – under healthy conditions, single switch fault, and dual switch fault. Figure 40 shows the transient response under healthy conditions, while Figure 41 and Figure 42 show the response under single and dual fault conditions, respectively. The healthy condition DC link voltage is superimposed on the fault graphs, as a baseline. It is seen that the initial sag/spike of the DC link voltage is worsened under fault conditions and ripple is introduced. However, the grid current returns to balanced, clean sinusoids rapidly after the load change.

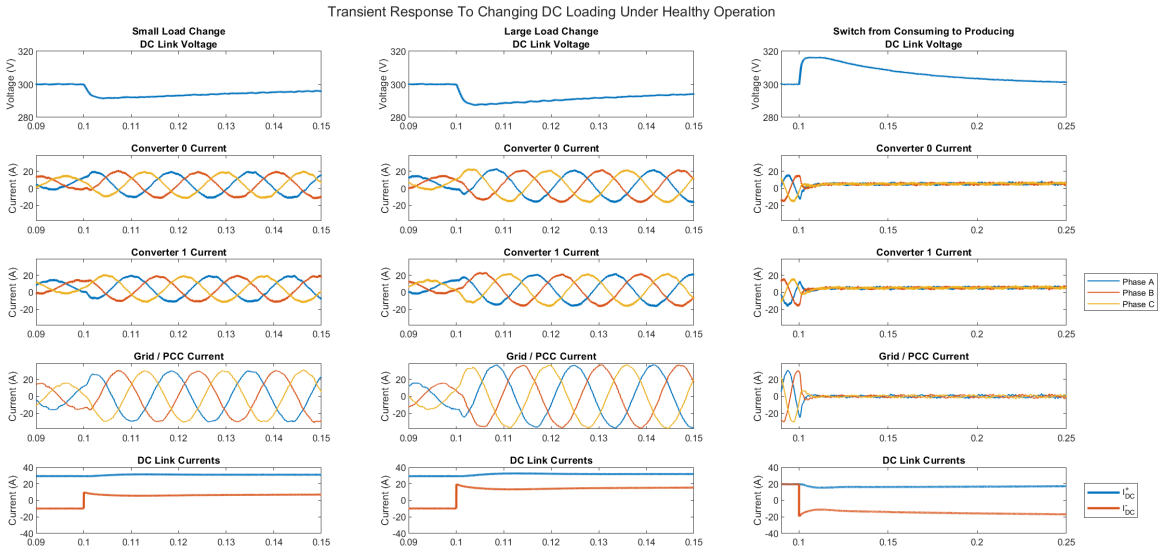



*Figure 40 - Transient Response to DC Load Changes Under Healthy Operation*

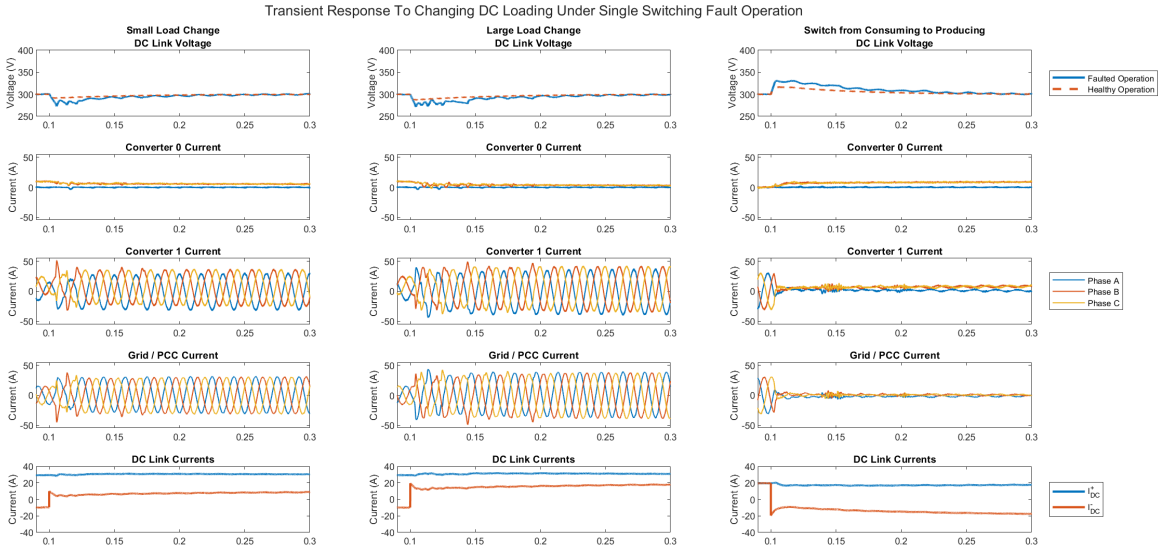



*Figure 41 - Transient Response to DC Load Changes Under Single Fault Operation*

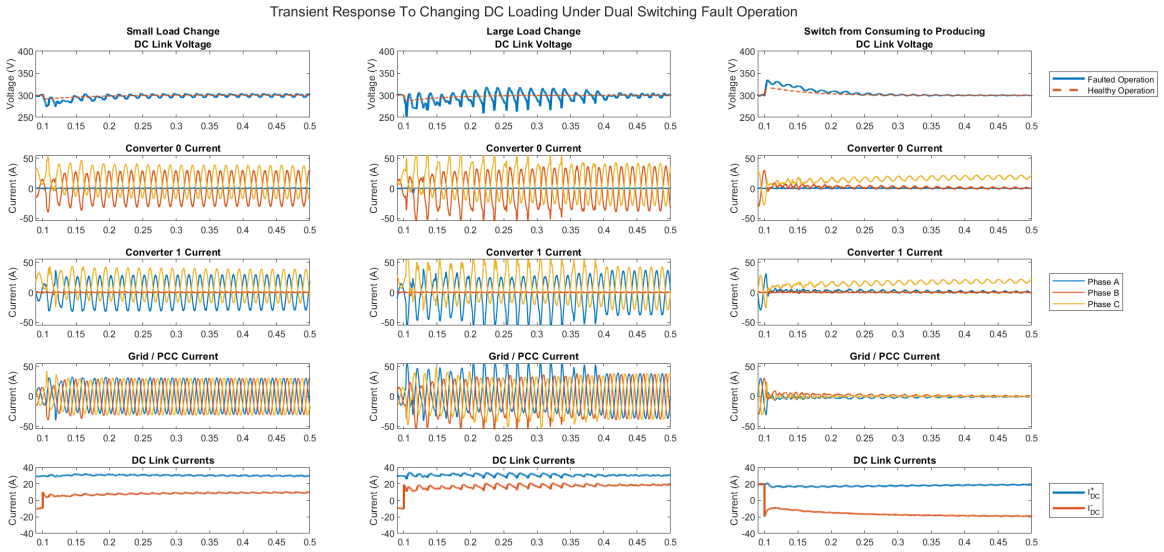



*Figure 42 - Transient Response to DC Load Changes Under Dual Fault Operation*

Table *5* summarizes the maximum deviation and time to return to within 3% of the DC link voltage as well as the total demand distortion (TDD) for the grid current, under each of the scenarios above.

Total demand distortion is defined as:

$$TDD = \sqrt{\sum_{h=2}^{\infty} \frac{I_h^2}{I_L^2}} \cdot 100\% \tag{101}$$

Where $I_h$ is the harmonic current and $I_L$ is the maximum load current. IEEE 519 limits the TDD for a system rated 120V to 69kV to 5% (in the most restrictive case [26]). As can be seen in Table *5*, the system is able to remain under this steady-state limit in all cases.

For the DC side, while significant effort has been put into developing standards for DC power quality [27, 28, 29], currently there is no well adopted result. However, in some applications, such as DC systems aboard ships and in railway systems, standards have been implemented. Currently they limit the DC ripple to 10% and 15%, respectively [30, 31].

Table 5: Response to Fault Conditions / DC Load Changes

| | Scenario | Maximum DC Link Deviation (% of nominal) | Time to Return to Normal (ms) | Total Demand Distortion at Steady State (%) |
|---|---|---|---|---|
| (A) | Healthy Operation -> Single Fault | 9.1 | 36 | 0.87 |
| | Single Fault -> Dual Fault | 1.8 | - | 1.59 |
| (B) | Healthy Operation -> Single Fault | 1.5 | - | 0.99 |
| | Single Fault -> Dual Fault | 0.8 | - | 1.1 |
| (C) | Healthy Operation -> Single Fault | 5.7 | 21.2 | 0.93 |
| | Single Fault -> Dual Fault | 1.4 | - | 1.24 |
| Healthy | Small Load Change | 4.3 | 27.7 | |
| | Large Load Change | 2.9 | - | |
| | Switch from Consuming to Producing | 5.5 | 48.1 | |
| Single Fault | Small Load Change | 9.5 | 94.4 | |
| | Large Load Change | 9.1 | 56.0 | |
| | Switch from Consuming to Producing | 10.3 | 102.2 | |
| Dual Fault | Small Load Change | 16.2 | 304.1 | |
| | Large Load Change | 8.9 | 125.5 | |
| | Switch from Consuming to Producing | 11.7 | 123.0 | |

## 3.2. Dual Decoupled Synchronous Reference Frame Control

In the dual decoupled synchronous reference frame (DDSRF) control implementation, a decoupling approach is used to allow independent control of the positive- and negative-sequence current in each 2L-VSC in the synchronous (DQ) frame. A number of approaches have been taken in the literature to decoupling the positive- and negative-sequence current, including the use of filters and delays [32, 33]. A more recent approach uses a decoupling network to allow a faster system response during transients [34]. By transforming the system into the DQ frame, the three-phase sinusoidal currents transform into DC signals at steady-state, which are then controlled using Proportional Integral (PI) controllers, eliminating the need for a resonant term in the controller compensator. The reference signals for each of the 2L-VSCs are determined by an outer loop controller, based on the capacitor voltages, similar to the ABC frame implementation – however, here these loops operate in the DQ frame, allowing direct control of the reactive power. A similar fault control supervisor is used to modify the reference signals based on the current fault status.

### 3.2.1. Converter Plant Modeling

Each 2L-VSC, along with its LCL filter, is modelled in the DQ frame using the method in [35], resulting in the circuit model in Figure 43, where the top circuit is for the DQ components while the bottom circuit is for the zero sequence component. Assuming the current through the filter branch is dominated by the capacitor current, thus the current source is negligible, this yields four differential equations governing the system DQ dynamics, shown in Laplace domain:

$$\boldsymbol{v_D} = \boldsymbol{i_{GD}}(R_2 + L_2 s) - L_2\omega_e \boldsymbol{i_{GQ}} + \boldsymbol{i_{CD}}(R_1 + L_1 s) - L_1\omega_e \boldsymbol{i_{CQ}} + \boldsymbol{m_D}\frac{V_{DC}}{2} \tag{102}$$

$$\boldsymbol{v_D} = \boldsymbol{i_{GD}}(R_2 + L_2 s) - L_2\omega_e \boldsymbol{i_{GQ}} + (\boldsymbol{i_{GD}} - \boldsymbol{i_{CD}})\left(\mathrm{R_f} + \frac{1}{\mathrm{C_f s}}\right) \tag{103}$$

$$\boldsymbol{v_Q} = \boldsymbol{i_{GQ}}(R_2 + L_2 s) + L_2\omega_e \boldsymbol{i_{GD}} + \boldsymbol{i_{CQ}}(R_1 + L_1 s) + L_1\omega_e \boldsymbol{i_{CD}} + \boldsymbol{m_{DQ}}\frac{V_{DC}}{2} \tag{104}$$

$$\boldsymbol{v_Q} = \boldsymbol{i_{GQ}}(R_2 + L_2 s) + L_2\omega_e \boldsymbol{i_{GD}} + (\boldsymbol{i_{GQ}} - \boldsymbol{i_{CQ}})\left(\mathrm{R_f} + \frac{1}{\mathrm{C_f s}}\right) \tag{105}$$

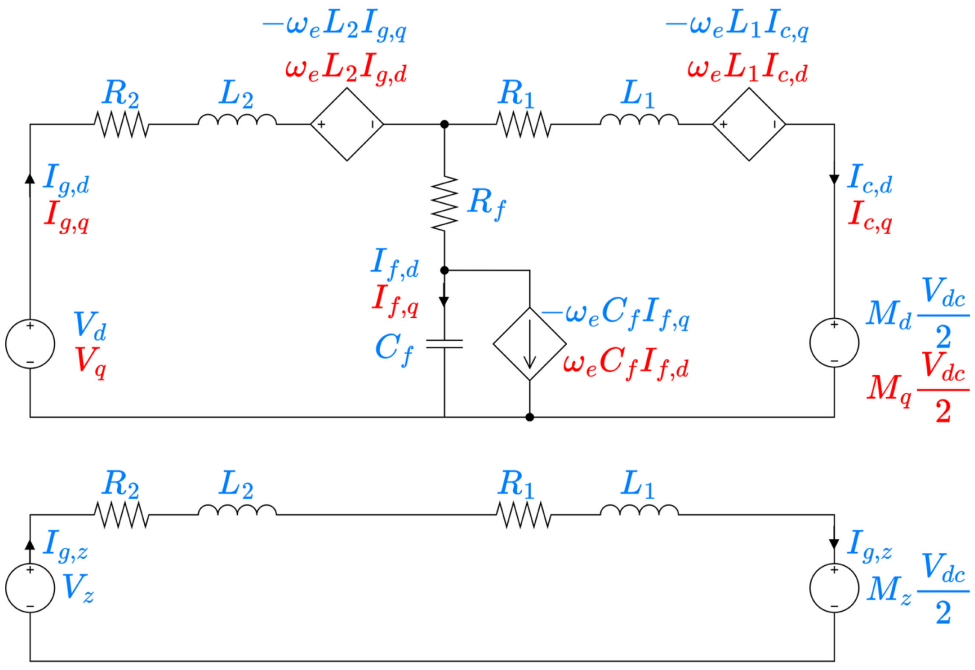



*Figure 43 – DQ Equivalent Circuit*

Solving for the grid current, applying the same assumptions as in section 2.2, yields,

$$\boldsymbol{i_{GD}}(R_2 + L_2 s) \cong \boldsymbol{v_D} + L_2\omega_e \boldsymbol{i_{GQ}} + L_1\omega_e \boldsymbol{i_{CQ}} - \boldsymbol{m_D}\frac{V_{DC}}{2} \tag{106}$$

$$\boldsymbol{i_{GQ}}(R_2 + L_2 s) \cong \boldsymbol{v_Q} - L_2\omega_e \boldsymbol{i_{GD}} - L_1\omega_e \boldsymbol{i_{CD}} - \boldsymbol{m_Q}\frac{V_{DC}}{2} \tag{107}$$

And defining the plant virtual input (u) as:

$$\boldsymbol{u_D} = \boldsymbol{v_D} + L_2\omega_e \boldsymbol{i_{GQ}} + L_1\omega_e \boldsymbol{i_{CQ}} - \boldsymbol{m_D}\frac{V_{DC}}{2} \tag{108}$$

$$\boldsymbol{u_Q} = \boldsymbol{v_Q} - L_2\omega_e \boldsymbol{i_{GD}} - L_1\omega_e \boldsymbol{i_{CD}} - \boldsymbol{m_Q}\frac{V_{DC}}{2} \tag{109}$$

Allows the plant to be written as:

$$\boldsymbol{P_D} = \frac{\boldsymbol{i_D}}{\boldsymbol{u_D}} = \frac{1}{R_2 + L_2 s} \tag{110}$$

$$\boldsymbol{P_Q} = \frac{\boldsymbol{i_Q}}{\boldsymbol{u_Q}} = \frac{1}{R_2 + L_2 s} \tag{111}$$

Where the converter current and grid voltage are treated as feedforward terms, as in the block diagram in Figure 44.

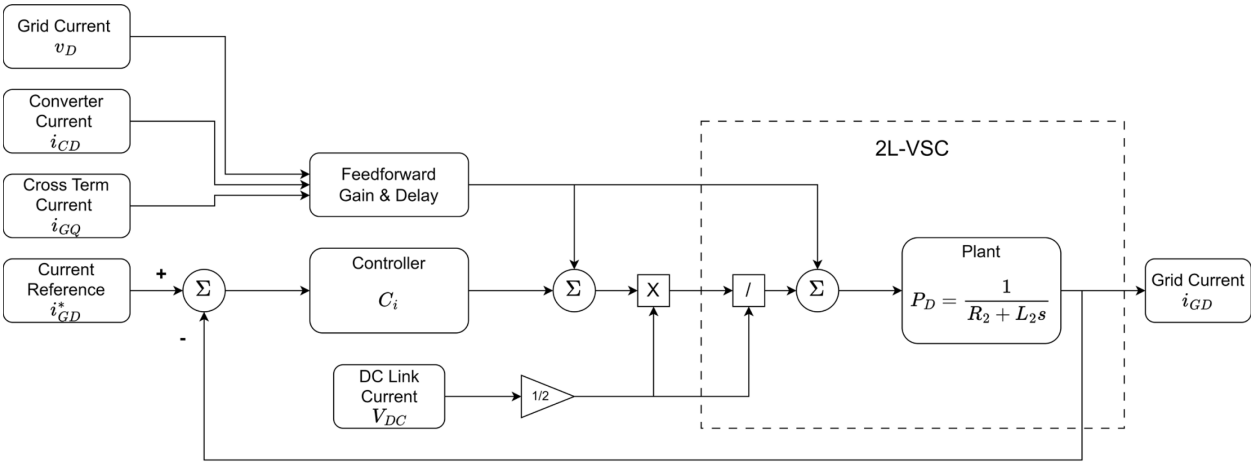



*Figure 44 - DQ Plant Block Diagram for each 2L-VSC within the BGIC*

### 3.2.2. Decoupling Methodology

Three phase values, both balanced and unbalanced, can be broken down into three balanced symmetrical components – that is, a balanced positive sequence component, a balanced negative sequence component, and a zero-sequence component. Therefore, by controlling all three, it is possible to generate any arbitrary output. The positive and negative sequence components can be transformed into the synchronous (DQ) reference frame, resulting in steady-state DC signals, while the zero sequence component is treated separately, having a simpler plant model. However, this requires separating the signal into its symmetrical components, a process that introduces significant delay into the control loop.

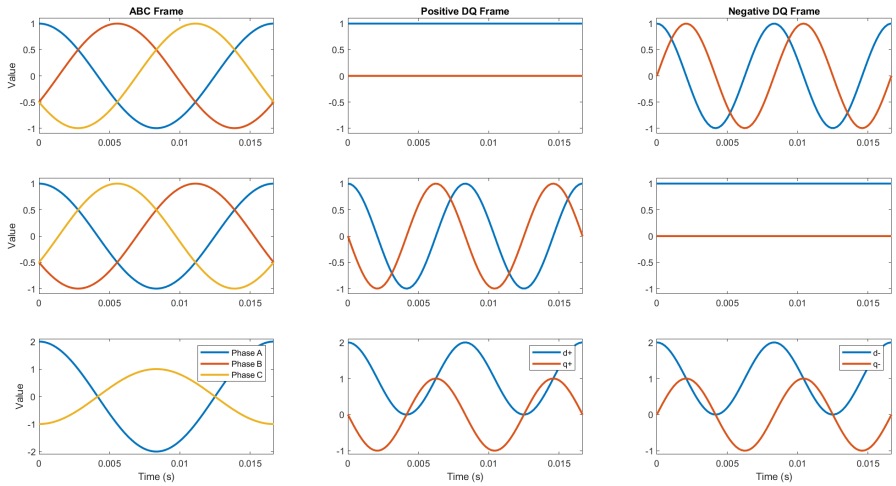



*Figure 45 - Positive and Negative Sequence Values in DQ Frames*

An alternative approach was proposed in [34], termed the "Enhanced Decoupled Dual Synchronous Reference Frame" (DDSRF). As seen in Figure 45, when a positive sequence, three-phase signal is transformed to the positive synchronous reference frame, it results in a DC signal. However, transforming it into the negative synchronous reference frame yields a time-varying signal at twice the fundamental frequency, with an amplitude equal to the DC signal in the positive DQ frame (as in the upper subplots in Figure 45). The opposite occurs when transforming a

negative sequence, three-phase signal into the synchronous frames (as in the middle subplots in Figure 45). If a three-phase signal containing both positive- and negative-sequence components is transformed into the synchronous reference frames, the result is a DC component as well as a sinusoid of twice fundamental frequency whose amplitude is given by the magnitude of the DC component in the opposite direction synchronous frame (as in the lower subplots in Figure 45).

Therefore, instead of separating the symmetrical components in the ABC frame using delays, [34] uses the reference current of the opposite frame, combined with the control loop error in that frame (filtered to isolate the DC component), to predict the second harmonic portion of the DQ frame signal. This is then subtracted from the measured signal, resulting in a (relatively) DC value in each synchronous reference frame.

In this work the decoupling methodology from [34] is extended to include the DC component of each individual phase, by converting the decoupling signals back into the ABC frame and subtracting them from the measured current. The DC reference current for each phase is also subtracted from the input to the DDSRF system. The resulting decoupling network is shown in Figure 46, where the filters are first-order low pass filters tuned as in [34].

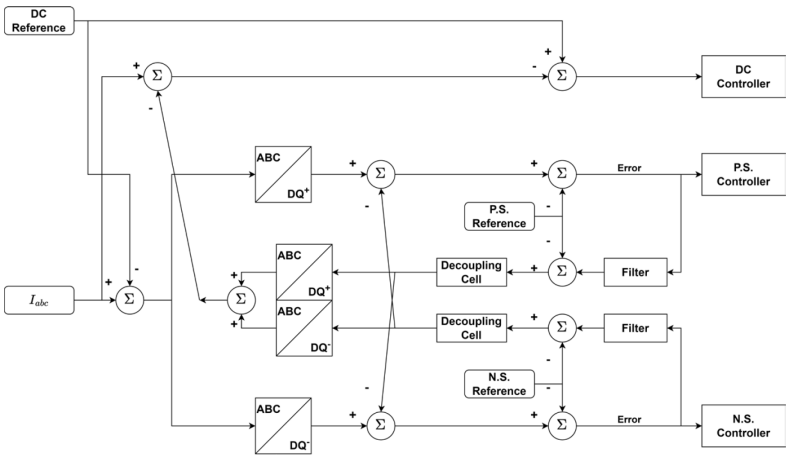



*Figure 46 – Proposed Extended DDSRF Decoupling Network*

### 3.2.3. Converter Current Control Loop

The inner controls again control the current of the individual 2L-VSCs, but due to the transformation into the synchronous (DQ) frame, the reference signal is now DC, as opposed to a fundamental-frequency sinusoid. This allows a Proportional Integral (PI) controller to be used, without need for a resonance term. The controller takes the form:

$$\boldsymbol{C_i} = K_p + K_i \frac{1}{s} \tag{112}$$

Where the gains are chosen such that the controller has a crossover frequency around 1/10$^{th}$ of the switching (sampling) frequency and a phase margin in excess of 60° at the crossover point. The frequency response plot of the open and closed loops is shown in Figure 47. The parameters used for the system under test are shown in Table *6*.

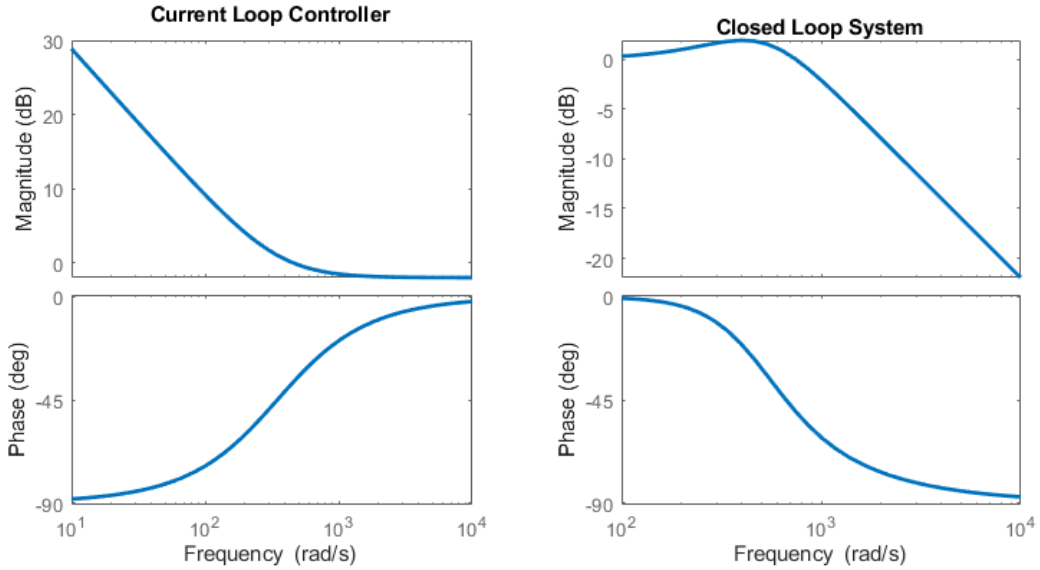



*Figure 47 - Frequency Response of Inner Loop Controller*

### 3.2.4. DC Link Voltage Control Loop

Under healthy operating conditions, the outer loop controller takes the form of a PI controller, tuned for a crossover frequency near the fundamental grid frequency.

$$\boldsymbol{C_v} = K_v \frac{(s + z_f)}{s} \tag{113}$$

Using the same methodology as in section 3.1.3, a slower controller is used under fault conditions to prevent DC link ripple from affecting the control action. The controllers are slowed to 1/5$^{th}$ of the fundamental grid frequency, and a second order low-pass filter is added to help remove first and second order ripple. Thus the controller takes the form:

$$\boldsymbol{C_{vf}} = K_{vf} \frac{s + z_{vf}}{s} \cdot \frac{w_f^2}{(s + wf)^2} \tag{114}$$

The parameters used for the system under test are shown in Table *6*.

Table 6 - Control System Parameters, DDSRF Implementation

| Current Control Loop | |
|---|---|
| **Parameter** | **Value** |
| $K_p$ | 0.797 |
| $K_i$ | 277.22 |

| Voltage Control Loop | |
|---|---|
| **Parameter** | **Value** |
| $K_v$ | 0.750 |
| $z_v$ | 37.7 |
| $K_{vf}$ | 0.296 |
| $z_{vf}$ | 15.1 |
| $\omega_f$ | 75.4 |

### 3.2.5. Fault Control Supervisor

As with the ABC control strategy, the fault control supervisor oversees the operation of the converter and all compensators. The AC reference current lookup table, shown in Table *3*, remains in effect; however, the supervisor converts these reference currents into positive and negative components in the synchronous (DQ) reference frame. The balance of the supervisor remains the same.

## 3.3. Controller Hardware-in-the-Loop Testing

Simulations are relied on heavily in the design of control systems for power electronic converters, as they provide the opportunity to test control loops and system responses with reduced infrastructure needs in a shorter period of time. In addition, they offer the ability to test conditions that are not feasible in fully-built systems, such as cases that would lead to equipment damage or require excessive power levels [36].

The IEEE Standard for the Testing of Microgrid Controllers [37] provides definitions on the implementation of different controller testing strategies involving simulation. Simulation fidelity refers to how closely the simulated system response matches the real response of the built system; it is impacted by the use of time-average models in place of switched models, as well as computational limitations requiring larger than optimal step sizes. Coverage refers to the ability to test a variety of conditions – under simulation, it is generally possible to subject the system to arbitrary conditions without regard for equipment damage, power requirements, or safety. If a component is damaged in simulation, it is simply reset to a working state prior to executing the next simulation. However, when physical hardware is involved, expected grid conditions that would lead to equipment failure cannot easily be tested due to the expense and time involved in replacing damaged components. Similarly, lab environments often have limitations on the voltage and current levels available, both due to infrastructure and safety concerns.

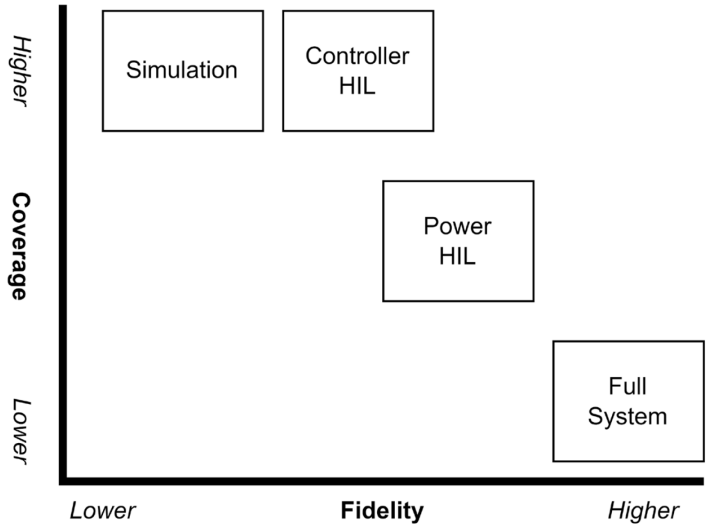



*Figure 48 - Relative coverage and fidelity of controller testing methods, adapted from [37]*

There are four main levels of controller testing, with a comparison of the relative coverage and fidelity provided in Figure 48:

- Simulation, where both the system under test (grid, converter, and load(s)) and the controller are entirely simulated, generally in the same system. This may be an online (real-time) or offline simulation (Figure 49). This is the approach used in section 3.1.5 to test the ABC implementation of the BGIC control.

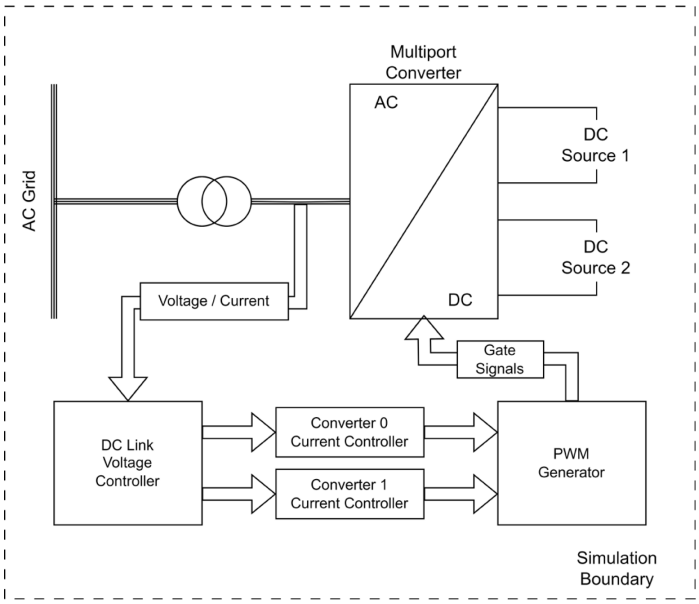



*Figure 49 - Simulation Testing Method Employed for the ABC-frame Control Implementation*

- Controller Hardware-in-the-Loop (C-HIL), where the system under test (grid, converter, and load(s)) are simulated, but the system outputs and control inputs are generated by a physically separate controller (generally, the same hardware that would be deployed to a field installation). Signals are passed between the controller and the simulation environment either through analog / digital voltage signals or through some communication protocol (ethernet, MODBUS, etc). This is generally done as an online (real-time) simulation (Figure 50).

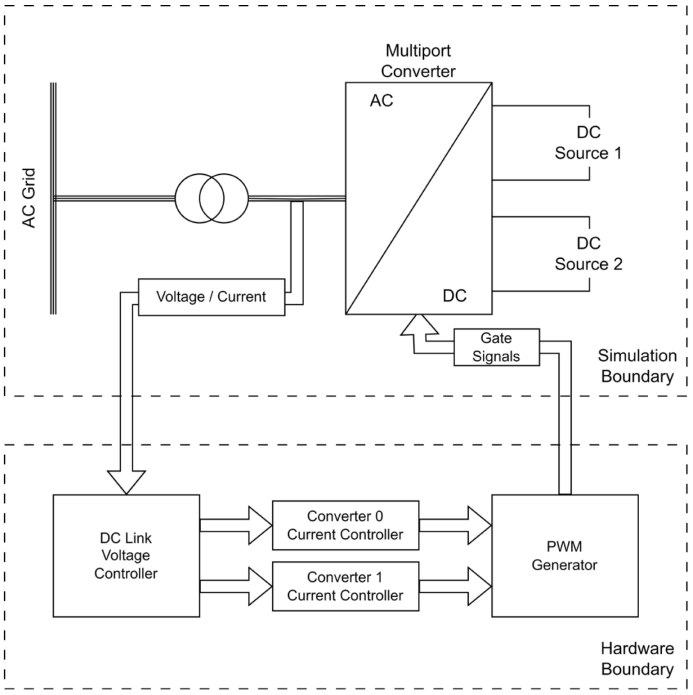



*Figure 50 – Controller Hardware-in-the-Loop (C-HIL) Testing Method Employed for the DQ-frame Control Implementation*

Power hardware-in-the-loop and full system testing are not used in this work.

C-HIL allows for the actual control algorithm to run on the expected control platform, as opposed to being adapted to a simulation environment. This can eliminate issues relating to implementation differences – for example, the phase-locked loop (PLL) component in Simulink behaves slightly differently than the similarly configured component for the Imperix Boombox; running a simulation in Simulink may verify that the control system works as intended, only for the system

to fail when implemented on the Boombox for hardware verification due to the differences. Compared to full hardware implementation, it has the additional benefits of creating repeatable, standards test cases that can help speed up the development cycle [36].

A limitation with C-HIL, however, is that the interface between the controller and the simulation must be validated due to the large impact it can have on the test results [36]. One proposed option is to run a benchmark test on full hardware and then repeat the same test on the C-HIL environment, to ensure the output is the same. If a simulation environment that is already validated exists, then it is possible to run this benchmark case on the simulation instead of in physical hardware.

A number of options exist for the interface between the controller and the simulator, though they fall into one of two categories – electrical analog or digital signals, generally produced/read using special interface cards for the simulator, or digital communication protocols, such as ethernet or MODBUS. Examples of both systems are widely available:

- A system-on-a-chip (SoC) from the Xilinx Zynq family was used in [38] to implement a DC-DC buck converter controller on the SoC's FPGA, communicating with the plant through the AXI bus.
- A commercial power plant controller was connected via MODBUS (over ethernet) with a NovaCor Real-Time Digital Simulator (RTDS) in [38].
- Multiple solar (PV) systems have been tested using Typhoon hardware specifically designed for C-HIL testing, such as in [40, 41].
- Offshore wind power controllers were connected via analog / digital input / output cards to a NovaCor RTDS in [42].
- An OPAL-RT OP5700 real time simulator platform was connected to a controller via Aurora 8b/10b for C-HIL testing in [43].

### 3.3.1. Conventional C-HIL Setup

The PEPST lab at the University of Alberta is equipped with a NovaCor RTDS and several Imperix Boombox's, which have been used for C-HIL testing.

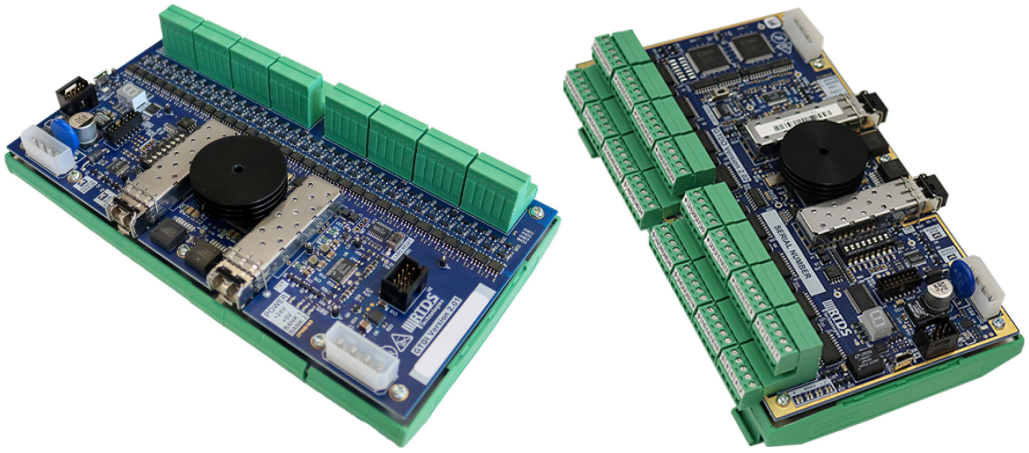


*Figure 51 - NovaCor Analog Output (GTAO, left) and Digital Input (GTDI, right) Cards*

The NovaCor is equipped with an analog output (GTAO) card providing 12 analog outputs ranging from -10V to +10V, a digital input (GTDI card) providing 64 digital inputs, and a front panel interface (GTFP) providing an additional 16 digital inputs and 16 digital outputs. Additional cards may be daisy-chained allow for increased IO capability but come at substantial cost.


*Figure 52 - Imperix Boombox Controller*

The Boombox is equipped with 16 analog inputs, 4 analog outputs, 16 digital inputs, and 48 digital outputs. An additional 36 digital pins can be configured as either input or output. Of the 48 digital output pins, 32 are capable of pulse-width modulation (PWM). Additional Boomboxes can be connected via fibre optic cables to allow access to additional IO capability, but again come at a substantial cost.

The original C-HIL testing setup used the GTAO card on the RTDS to generate analog signals, which were then read using the analog inputs on the Boombox. PWM signals were generated using the FPGA on the Boombox, output via electrical (digital) outputs, and read into the RTDS using the GTDI card. While this works well for small converter topologies, it is limited (by hardware availability) to 12 measured signals in simulation. For the full implementation of the BGIC controls in the decoupled, dual synchronous reference frame, a total of 20 signals are required – grid voltage (x3), grid-side current (x3), and converter-side current (x3) for each of the two 2L-VSCs, in addition to the DC pole voltages (x2). To overcome this limitation, the fibre ports on the RTDS and Boombox were connected via the Aurora protocol, allowing for substantially more measured signals in simulation.

### 3.3.2. Aurora Protocol Overview

The Aurora 8B/10B protocol is a low-resource, fully duplex link-layer protocol for serial communication. It is generally implemented in Field-Programmable Gate Arrays (FPGAs) and provides general-purpose data channels capable of up to 84.48Gb/s data transfer. It was originally developed by Xilinx and is now maintained by AMD as an "open standard… available for implementation by anyone without restriction". [44]

The RTDS natively supports Aurora communication, offering both a mainstep and a substep component. The Imperix Boombox is capable of Aurora communication, and Aurora is used for connecting multiple Boomboxes together; however, support for arbitrary data transfer is not available. Imperix has provided a modified IP for FPGA development in which the SFP ports are left available for the user application.

Additional information on the Aurora link implementation can be found in Appendix A.

### 3.3.3. Aurora C-HIL Environment Validation

Prior to using the Aurora C-HIL environment to test the DDSRF controls, it is necessary to validate that it is working correctly. This is done by running the same circuit and controller in three different environments - simulation only, conventional C-HIL environment, and Aurora C-HIL environment - and comparing the results. Provided that there are no unexplained discrepancies, the environment can then be considered validated. It is expected that there will be minor differences in timing and transient response due to the loss of synchronization – in the pure simulation environment, the controller and simulation run at the same sampling frequency with the control outputs generated in the same simulation timestep that produced the control inputs. However, when the controller is moved to the Boombox, this synchronization is lost and some clock jitter is expected. This may result in the simulation not receiving the output of the controller until the next timestep, which can appear as an additional zero-order hold. The hardware used for communication, either the Aurora transceivers or the input/output cards on the RTDS, can also introduce slight delays.

Figure 53 shows the startup sequence in the 3 environments; while the high-frequency transient response varies slightly, this can be attributed to the additional delays as well as the noise introduced by the hardware links.

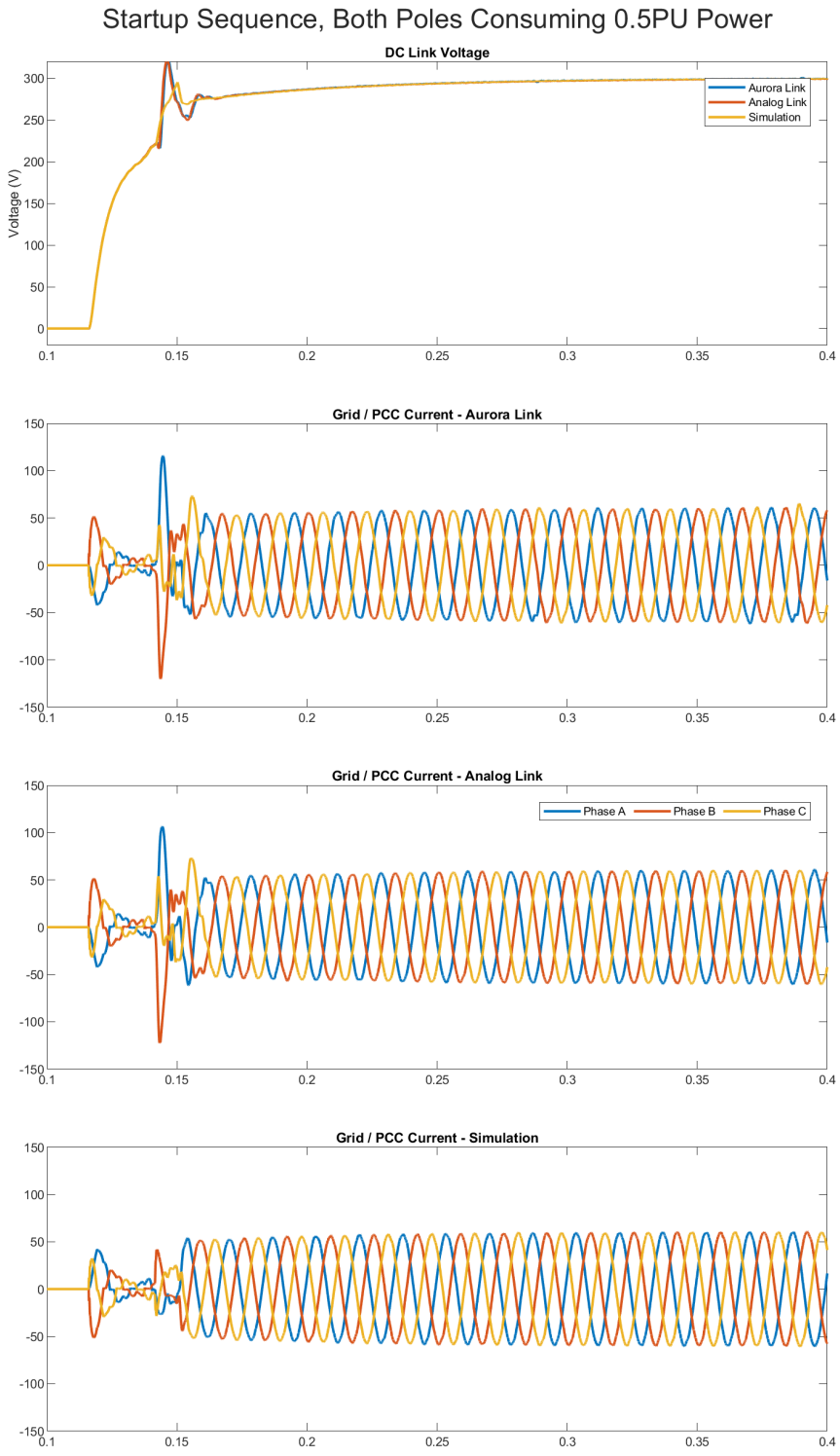



*Figure 53 - Comparison of BGIC Operation Using Hardware and Aurora IO for C-HIL, Startup*

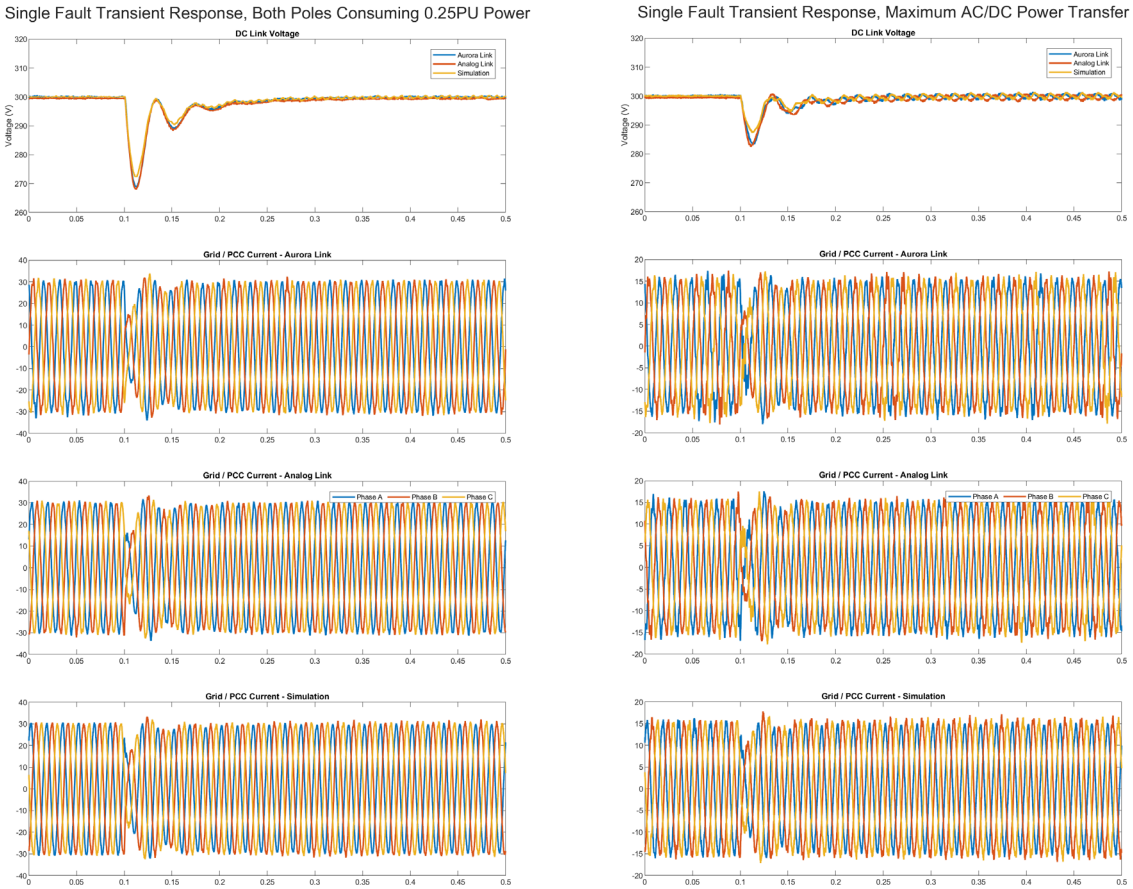



*Figure 54 - Comparison of BGIC Operation Using Hardware and Aurora IO for C-HIL, Single Fault*

Figure 54 provides a comparison of the transient response under the 3 environments to a single switching fault, under two different load configurations. Figure 55 provides a comparison of the transient response for a load change during a fault. Under all three scenarios, the hardware and Aurora link C-HIL environments closely match the simulation results, validating the C-HIL environments. Note that these validation tests were completed prior to final tuning of the compensators and therefore do not match the response of the final system; their purposes is only to show that, under the same compensator parameters, the three environments have the same response.

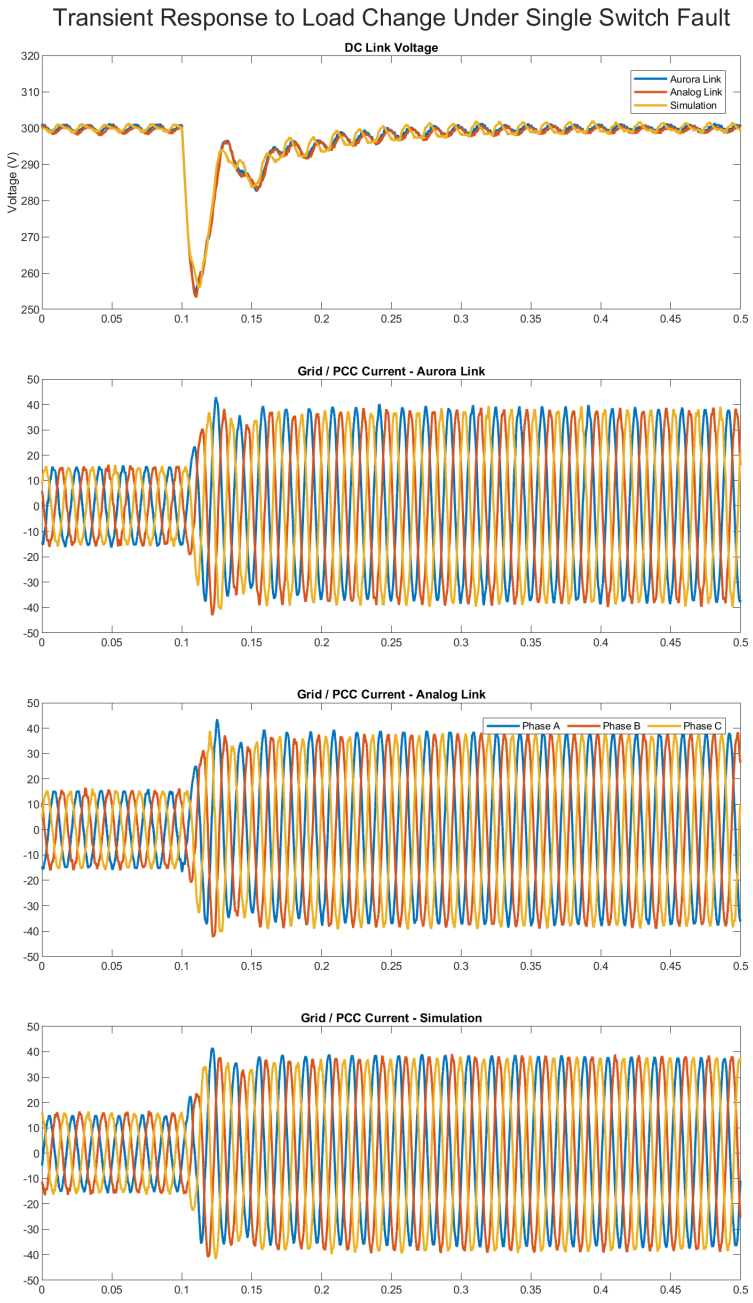



*Figure 55 - Comparison of BGIC Operation Using Hardware and Aurora IO for C-HIL, Load Change During Fault*

### 3.3.4. C-HIL Experiment Results

The control system is tested under the C-HIL methodology validated above; that is, an Imperix Boombox controller receiving measurements from a NovaCor RTDS via the Aurora link and transmitting PWM gating signals via hardware IO. The system parameters are kept the same as for the ABC control strategy, presented in Table *4*.

As with the ABC control strategy, three scenarios are considered:

- **(A)** Both DC poles consuming 0.25PU power (therefore the AC and DC power transfers are 0.5PU and 0PU, respectively). This is the highest AC power transfer that can be sustained under fault conditions.
- **(B)** One DC pole consuming 0.25PU power, the other producing 0.25PU power (therefore the AC and DC power transfers are 0PU and 0.5PU, respectively). This is the highest DC power transfer that can be sustained under fault conditions.
- **(C)** One DC pole consuming 0.375PU power, the other producing 0.125PU power (therefore the AC and DC power transfers are 0.5PU and 0.5PU, respectively). This is the worst-case scenario for DC ripple, as both AC and DC power transfers are maximized.

Transient response to a fault as well as steady-state response after the fault are presented.

Figure 56 identifies the AC and DC power transfer for the BGIC and is repeated here for clarity.

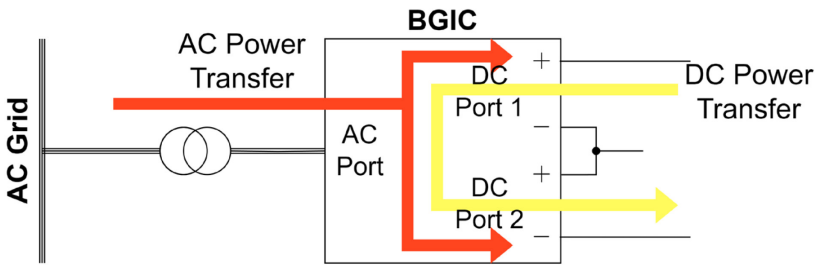



*Figure 56 - AC / DC Power Transfer for BGIC*

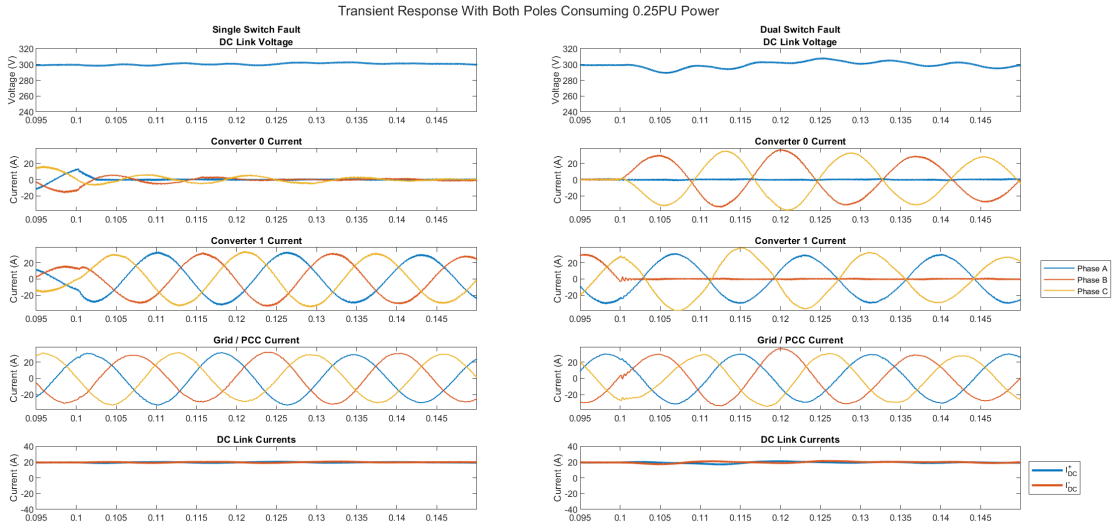



*Figure 57 - Transient Response with Both Poles Consuming 0.25PU Power (Scenario A)*

Figure 57 and Figure 58 show the transient and steady state response, respectively, under scenario (A). As with the ABC control strategy, for a single fault, the faulted converter switches to DC power transfer only while the AC power transfer of the healthy inverter is doubled. The DQ controllers react faster than the ABC controllers, resulting in very little voltage sag/spike on the DC link. For the dual fault, the previously faulted controller resumes partial AC power transfer rapidly, resulting in a grid current that is relatively free of disruption.

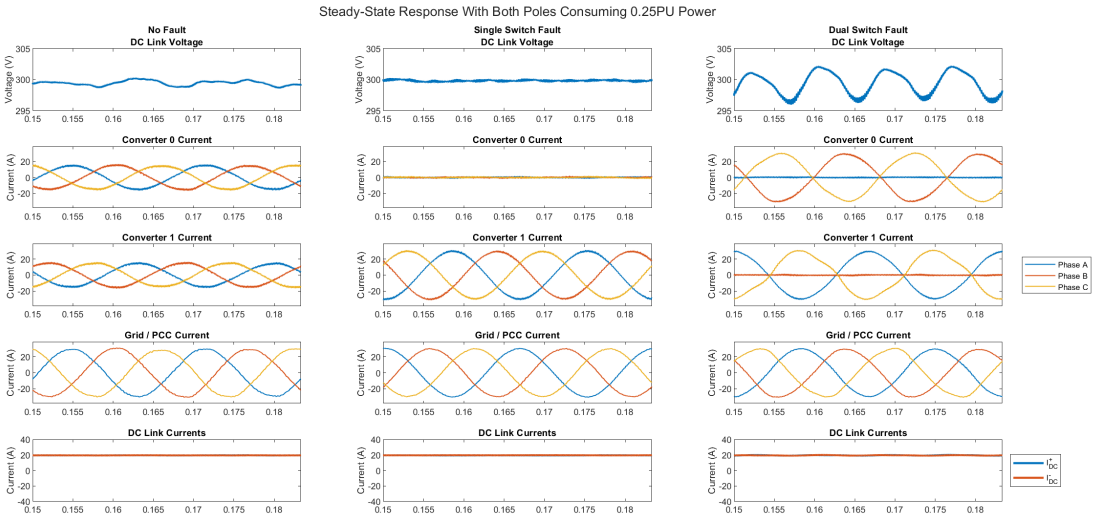



*Figure 58 - Steady State Response with Both Poles Consuming 0.25PU Power (Scenario A)*

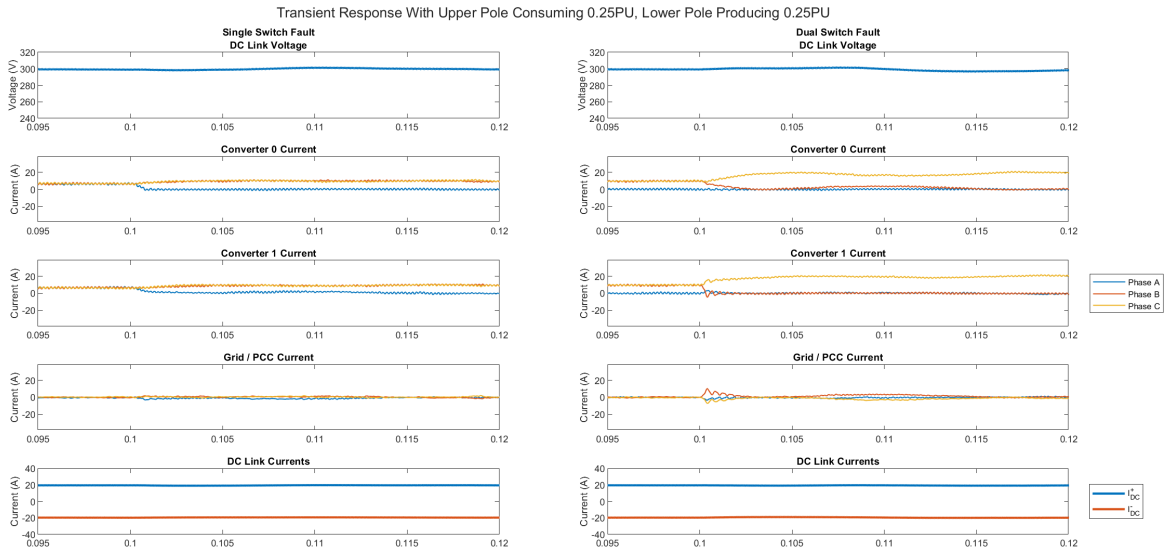



*Figure 59 - Transient Response with One Pole Consuming, One Pole Producing Power (Scenario B)*

Figure 59 and Figure 60 show the transient and steady state responses under scenario (B). Due to the lack of AC power transfer, the grid current sees little disruption during either fault.

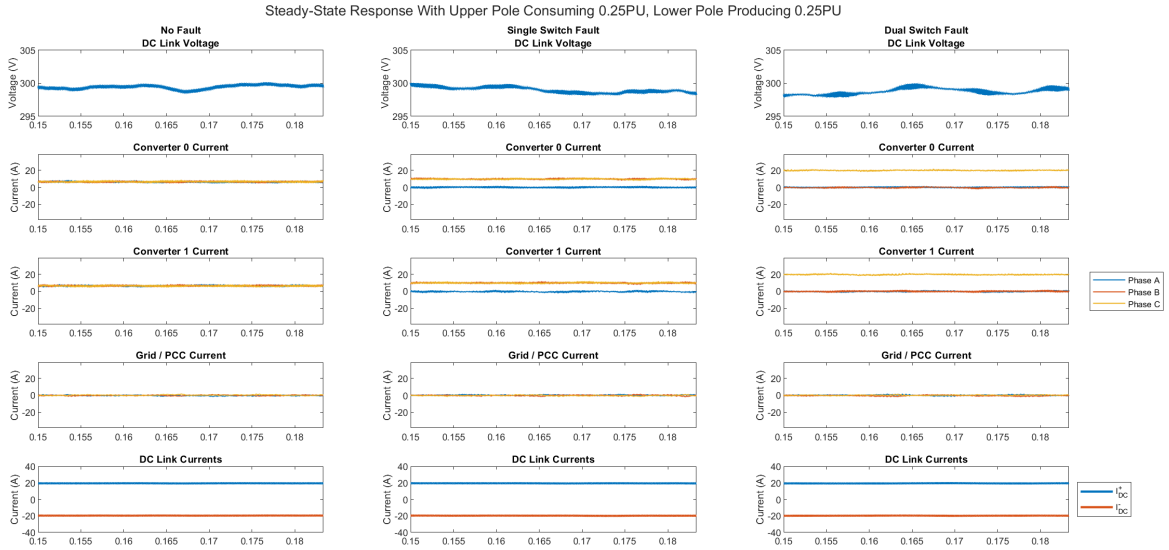



*Figure 60 - Steady State Response with One Pole Consuming, One Pole Producing Power (Scenario B)*

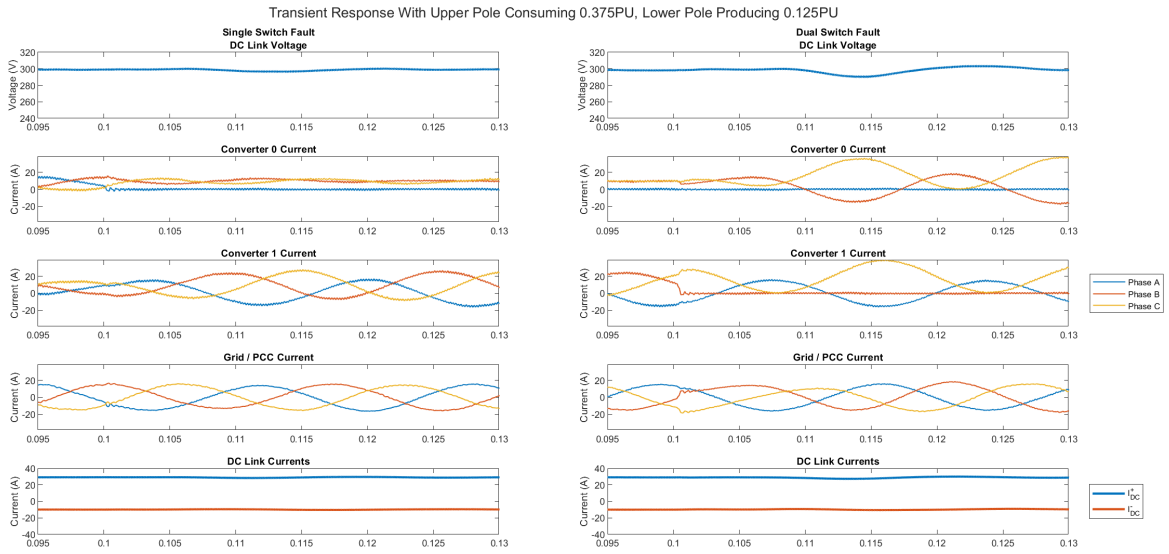



*Figure 61 - Transient Response with both AC and DC Power Transfer (Scenario C)*

Figure 61 and Figure 62 show the transient and steady state responses under scenario (C).

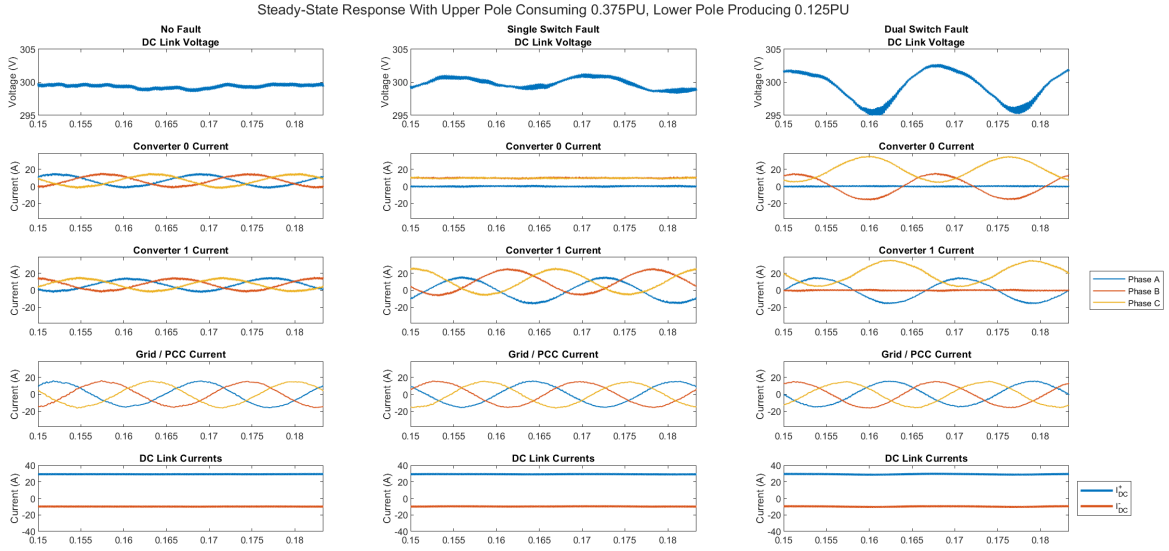



*Figure 62 - Steady State Response with both AC and DC Power Transfer (Scenario C)*

The transient response to DC load changes is shown alongside the ABC control strategy response in the following section.

## 3.4. Comparison of Control Strategies

Figure 63 and Figure 64 provide a high-level overview of the ABC and DDSRF control strategies, respectively. Each strategy uses two PI controllers, with variable coefficients, for the voltage / outer control loop, to generate DC link reference currents. This is followed by a power calculation stage, which converts the DC reference current into an AC reference current. In the ABC control strategy, this is done using the $\alpha\beta$ frame representation of the grid current, whereas the DDSRF control strategy uses the DQ frame representation. The fault control supervisor then takes this reference current and generates current references for each 2L-VSC.

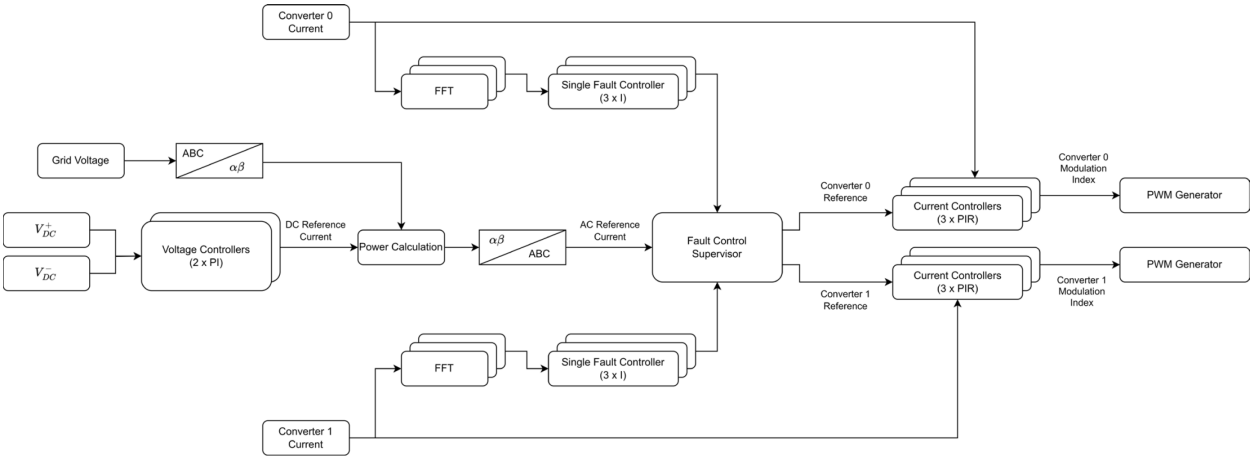



*Figure 63 - ABC Control Strategy Overview*

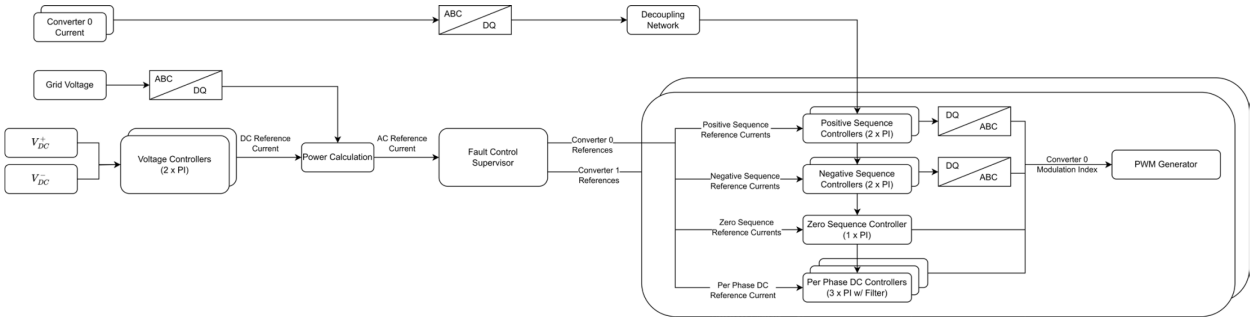



*Figure 64 - DDSRF Control Strategy Overview*

For the ABC control strategy, the inner loop consists of 3 PIR compensators for each 2L-VSC, along with 3 FFT & integral compensators (for driving the AC current to zero during single fault

conditions). For the DQ control implementation, the inner loop consists of 2 positive sequence PI compensators, 2 negative sequence PI compensators, a zero sequence PI compensators, and 3 per-phase DC PI compensators for each 2L-VSC. In total, the ABC control strategy requires 14 compensators (2 x PI, 6 x PIR, and 6 x FFT&I) and 2 Clarke transformations, while the DQ control strategy requires 18 compensators (all PI), 1 PLL, 18 Clarke transformations, and 30 Park transformations.

Table 7 – Required Control Elements for Each Control Implementation

| Component | Required Number | |
|---|---|---|
| | ABC Implementation | DQ Implementation |
| PI Compensator | 2 | 18 |
| PIR Compensator | 6 | - |
| FFT / I Compensator | 6 | - |
| PLL | - | 1 |
| Clarke Transformation | 2 | 18 |
| Park Transformation | - | 30 |

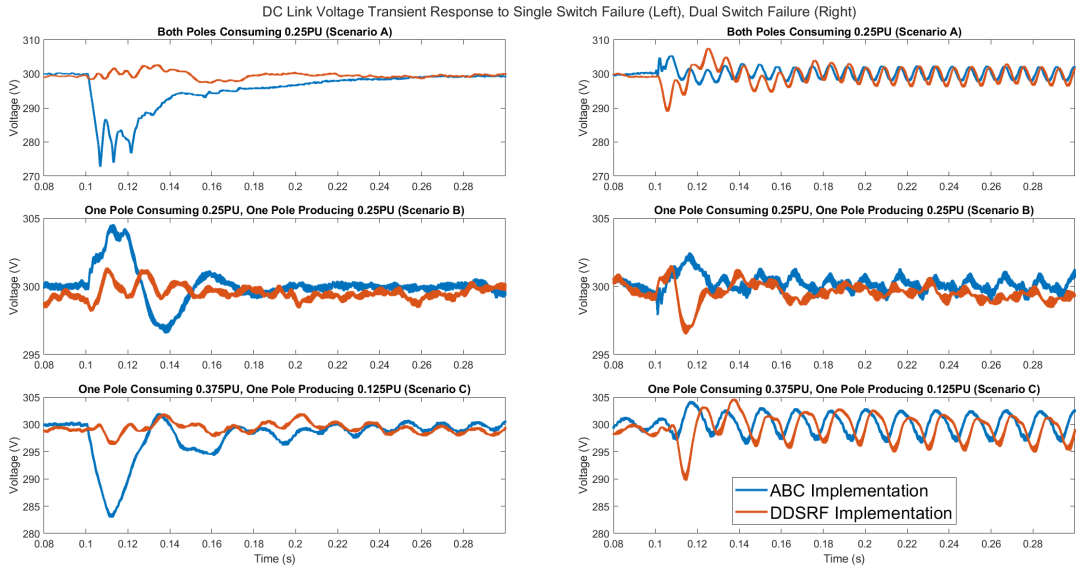



*Figure 65 - DC Link Voltage Transient Response to Failure under Both Control Strategies*

The DDSRF control strategy generally responds faster to faults, as shown in Figure 65, due to the higher crossover frequency of the inner loop controllers. However, it responds substantially slower to changes in the DC link load, as shown in Figure 66, in particular when one pole changes

suddenly from consuming to producing power (such as in the case where a large load is shut off quickly or a generating resource is returned to service). This is largely due to the decoupling of the positive, negative, and DC portions of the measured converter current and the interaction of the various controllers. If the decoupling was perfect, all controllers would be able to operate at a high crossover frequency, selected just low enough to treat the DC link ripple as a disturbance. However, since the decoupling is imperfect and also introduces some phase lag due to the filtering, the controllers act against each other during transients, delaying a return to steady state operation.

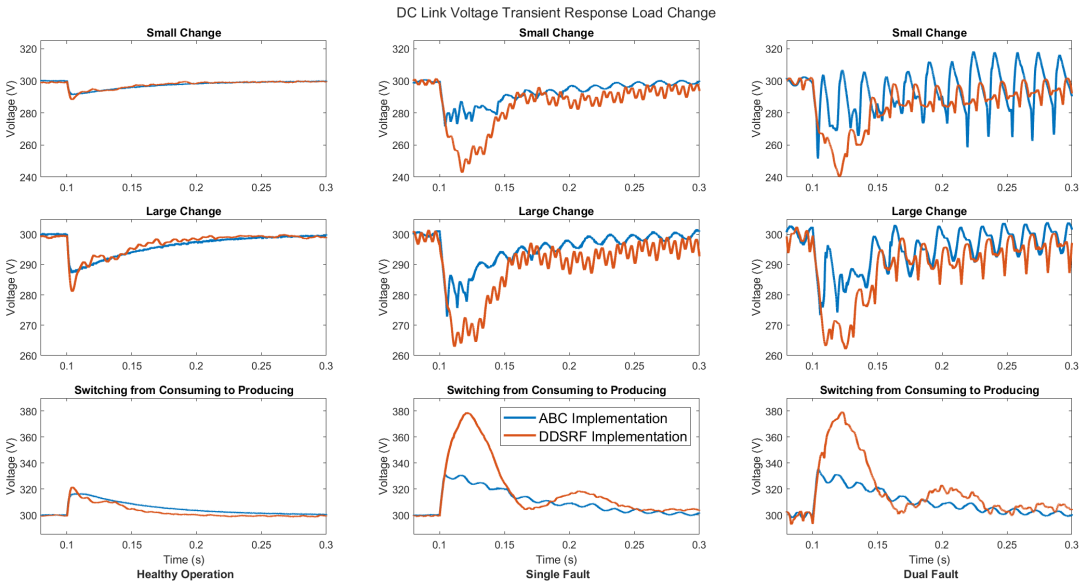



*Figure 66 - DC Link Voltage Transient Response to DC Load Change under Both Control Strategies*

# 4. Conclusion & Future Works

In this thesis, a novel strategy for the fault tolerant control of a multiport converter topology was proposed that allows for continued operation while ensuring balanced AC grid currents during single and dual switch fault events. Two implementations of the control strategy were presented – the first in the ABC frame, the second in an enhanced, decoupled dual synchronous reference frame (DDSRF). Simulation results are provided to validate the ABC frame controls under healthy operation and single & dual IGBT open-circuit failure, while controller hardware-in-the-loop experiments using the NovaCor Real Time Digital Simulator, Imperix Boombox controller, and a custom Aurora communications link are provided to validate the DDSRF controls. A summary of the results and possible future works are presented in this section.

## 4.1. Summary and Contributions

The Bipolar Grid Interfacing Converter, proposed in [12], is a multiport converter topology capable of converting between a single AC port and two DC ports. Normally, it is configured with the DC links tied together at the midpoint, allowing for a bi-polar DC connection with the capability of balancing the DC voltages. Through this, it is possible to arbitrarily transfer power between either DC pole and the AC grid or between the DC poles, with the only limitation being total power transfer. In the controls proposed in [12], the system had balanced AC grid currents during steady state and a rapid return to balanced conditions during transients such as load changes. However, they did not allow for continued operation should any open circuit fault occur, instead producing unbalanced AC grid current.

Detailed electrical and magnetic modelling of the BGIC was conducted in this work, with the aim of determining under what fault conditions the converter could maintain acceptable power quality

and balanced AC grid currents. This analysis determined that operation can be sustained under single and dual open-circuit IGBT failures, provided that, in the case of dual failure, the failures are not on the same phase. Power balanced equations were derived which provide an upper limit for the fundamental frequency and second harmonic ripple current on the DC link during faults. Modelling of the converters in the ABC frame as well as a rotating (DQ) frame was conducted in order to design effective controllers.

A new control strategy was proposed that intentionally produces unbalanced AC currents in each of the two, two-level voltage source converters that make up the BGIC. While in some scenarios there is fundamental frequency and second harmonic ripple on the DC link as a result, it is shown to be small in comparison to the DC current and can largely be mitigated by normal DC link capacitance. A detailed analysis of the fundamental frequency ripple is presented, determining it is proportional to both the AC grid current and the DC tap current, while the second harmonic ripple is proportional only to the AC grid current. This insight is leveraged to set operational limits on the DC tap current, used to balance the two poles, to further mitigate the fundamental frequency ripple.

Two implementations of the control strategy were then proposed. The first implementation controls the current in the ABC frame, using Proportional-Integral-Resonant controllers to allow for input tracking of both fundamental frequency AC current as well as DC tap current. The power required from each pole is calculated from the DC link capacitor voltages and used to generate the current reference in the stationary ($\alpha\beta$) frame. Additional controls are in place to assist with driving the current to zero during single faults as well as allowing for pre-charging of the DC link capacitors during startup. A fault control supervisor modifies the reference commands as required to handle the current phase arm statuses.

Simulation results validate that the controls work during healthy operation as well as during single & dual open-circuit IGBT failures. Transient response to failures as well as load changes while in a failed state are suitable for DC grids used in rail and ship applications, while the AC grid current remains under the total demand distortion limits given in IEEE 519.

The second implementation controls the AC current in two rotating (DQ) reference frames – one positive, one negative – alongside a zero-sequence component. The reference frames are decoupled based on a method proposed in [34], expanded in this work to include a decoupled ABC frame for control of the DC tap currents during faults. By working in the rotating reference frame, the AC current references become DC signals. This simplifies the control requirements, allowing Proportional-Integral controllers without need for resonant terms. The power required is again calculated from the DC link capacitor voltages and used to generate the current reference in the rotating (DQ) frame. A similar fault control supervisor again modifies the reference commands as required to handle the current phase arm statuses.

Due to laboratory hardware limitations, the conventional controller hardware-in-the-loop setup did not provide enough outputs from the simulator in order to run the DDSRF controls (due to extra feedforward terms resulting from the use of the LCL filter). Therefore, a custom FPGA bitstream was written for the Imperix Boombox, implementing an Aurora link over the fibre optic connection between the RTDS and Boombox. This C-HIL environment was validated using the ABC control implementation, comparing the Aurora C-HIL results to the conventional, hardware IO results as well as the pure simulation results.

C-HIL experiments were then used to show that the DDSRF controls work during both healthy and faulted operation. Steady-state response largely matches the steady-state response of the ABC implementation, while transient response to failures is improved, due to the higher bandwidth of

the dq frame current controls. However, transient response to load changes, in particular large step changes, is slower and includes more disruption on both the DC link voltage and the AC grid currents. This is a result of the imperfect decoupling of the positive- and negative-sequence controls and the delay introduced by the decoupling network. However, the system is still able to meet the DC grid requirements for rail and ship applications.

In conclusion, both control implementations are suitable for continued operation of the BGIC during single and dual open-circuit IGBT failures, with the ABC implementation being preferable where the transient response to large, sudden load changes is a priority, while the DDSRF implementation is preferable where the transient response during a fault is a higher priority.

## 4.2. Future Works

There are multiple directions this work can be expanded upon, including:

- The current implementation of the Aurora link in the Imperix Boombox FPGA uses the sandbox inputs/outputs provided by Imperix to communicate between the user code (running on the CPU) and the FPGA. This interface is limited in the amount of data transferred per clock cycle, requiring the data transfer be split over 2 or more clock cycles. This introduces delay in the closed loop system, which impacts the transient response. A better method of transferring data could eliminate this.
- Further, while the Aurora implementation works adequately for transferring voltage and current readings from the RTDS to the Boombox, it suffers from small timing issues between the various components. These timing issues cause occasional data points to be received incorrectly. As this occurs infrequently, the control loops filter out this noise effectively. However, when attempting to use the Aurora link to transfer PWM gate signals

from the Boombox to the RTDS, this noise causes unpredictable behavior of the converter. This has been avoided in this work by using hardware IO to transmit the PWM signals but is a potential improvement opportunity for further work.

- This work has focused on open-circuit IGBT failure; however, the control strategy is able to handle the loss of a phase arm for any reason provided that the uncontrollable portion of the arm fails to open. Short-circuit failure of the IGBT can be converted to open-circuit failure by adding fuses to the arms and intentionally overloading them through temporary control action once a fault has been detected. Exploring this would allow the same control strategy to work during short-circuit IGBT failures.

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# Appendix A: Aurora Link Implementation

## A.1 Aurora Protocol Overview

The Aurora 8B/10B protocol is a low-resource, fully duplex link-layer protocol for serial communication. It is generally implemented in Field-Programmable Gate Arrays (FPGAs) and provides general-purpose data channels capable of up to 84.48Gb/s data transfer. It was originally developed by Xilinx and is now maintained by AMD as an "open standard… available for implementation by anyone without restriction". [42]

The RTDS natively supports Aurora communication, offering both a mainstep and a substep component for transferring up to 128 data points (64 in substep) over each of 4 available SFP ports. The Imperix Boombox is capable of Aurora communication, and Aurora is used for connecting multiple Boomboxes together; however, support for arbitrary data transfer is not supported. Imperix has provided a modified IP for FPGA development in which the SFP ports are left available for the user application.

Aurora uses a framing-based interface, in which both a start-of-frame (SOF) and end-of-frame (EOF) are asserted in order to control data transmission / reception. In order to transmit data, it must be broken into packets that are the same width as the channel; in this case, RTDS has defined the channel to be 16 bits.

All signals for the transmission of data are synchronized to the user_clk. Provided the channel has already been established, tx_ready being asserted indicates that the channel is ready to receive data. When data is ready, tx_valid is asserted by the user code. At the next positive-edge of user_clk, provided that both tx_ready and tx_valid are asserted, the data is read from tx_data and added to the transmission buffer. When the last data packet is presented, tx_last is asserted and tx_keep is

set to indicate the number of valid bits (to account for cases where the total number of bytes to be transferred is not divisible by the channel size).

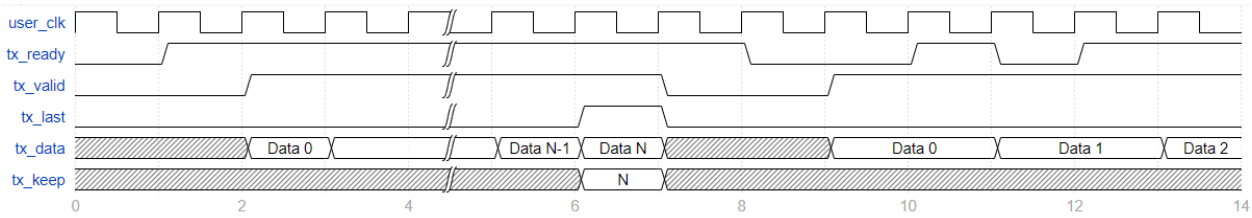


*Figure 67 - Example Waveform for Data Transmission*

Figure 67 provides two examples of this process. At t = 1, the channel is ready (tx_ready asserted). At t = 2, the first portion of the data is loaded onto tx_data and tx_valid is asserted. Since tx_ready remains asserted, at each clock cycle, the next portion of the data is presented. At t = 6, the final portion of the data is presented, and tx_last is asserted. At the next clock cycle, both tx_valid and tx_last are de-asserted. This is the normal transmission process with no interruptions.

At t = 9, a new frame is begun by asserting tx_valid. However, since tx_ready is not asserted, the second piece of data is not presented at the next clock cycle; instead, Data 0 is held until tx_ready and tx_valid have both been asserted at a clock edge. This is the case where the user code presents data prior to the channel being able to accept data (either due to recovering from a reset, error, or a pause due to clock synchronization).

At t = 11, Data 1 is presented, but since tx_ready has been de-asserted, it is held until tx_ready is asserted. This is the case where an error or clock synchronization occurs in the middle of a frame.

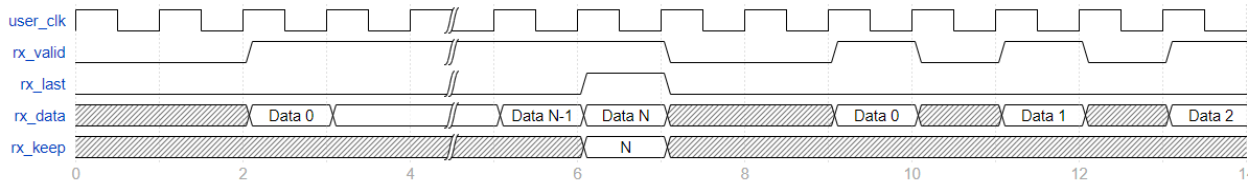


*Figure 68 - Example Waveform for Data Reception*

Receiving data follows a very similar process, except that there is no buffer and therefore no rx_ready signal. When data is received, rx_valid is asserted by the Aurora IP, and the user code must store the value of rx_data at the next positive clock edge. When the last portion of the data is received, the Aurora IP asserts rx_last and indicates the number of valid bits via rx_keep.

Figure 68 shows two examples of this process; first without any interruptions and then with a pause between each segment of data. At t = 2, rx_valid is asserted and Data 0 is presented on rx_data. At every clock cycle, the next piece of data is presented, until t = 6 where rx_last is asserted, rx_keep is set to N, and the final piece of data is presented. At t = 9, a new frame is begun, but since rx_valid is de-asserted after Data 0 is presented, at the next clock edge, rx_data is in an unknown state and cannot be stored.

## A.2 Imperix Boombox Communication Methodology

The Imperix IP, which provides all of the necessary FPGA functionality to support the Simulink model being executed on the CPU, provides two interfaces for data transfer – SandBox In (SBI) and SandBox Out (SBO). Each of these interfaces consists of 64, 16-bit registers, of which the first 32 are generally made available to the user code. SBI registers are used to transfer data from the FPGA to the CPU, whereas SBO registers are used to transfer data from the CPU to the FPGA.

There are 3 essential clock domains within the Imperix system – Clock0, the Imperix clock, and the User Clock. The Imperix clock is fixed at 250MHz, and all signals coming from / going to the Imperix IP are synchronized to this clock. Clock0 is the main clock for the Simulink model, and is

generally much slower than the Imperix clock – on the order of 1-100kHz. Analog inputs are sampled in reference to this clock; it defines the sampling frequency of the system. The User clock is determined by the Aurora channel, and for the RTDS link, is set to 100MHz. All signals coming from / going to the Aurora IP are synchronized to this clock.

The SBO/SBI registers are updated once per Clock0 period; when stable, valid data is available on the SBO registers, data_valid_pulse is asserted (synchronized to the Imperix clock) for 1 clock cycle. The SBI registers are sampled immediately after sampling_pulse is asserted. Sampling occurs at the beginning of each Clock0 period, while data is written to the SBO registers near the end of the period (Fig X., provided by Imperix). It is sufficient to write data to the SBI registers in user code shortly after data_valid_pulse is asserted; this provides sufficient time for the data to propagate through all latches and stabilize, prior to being read.

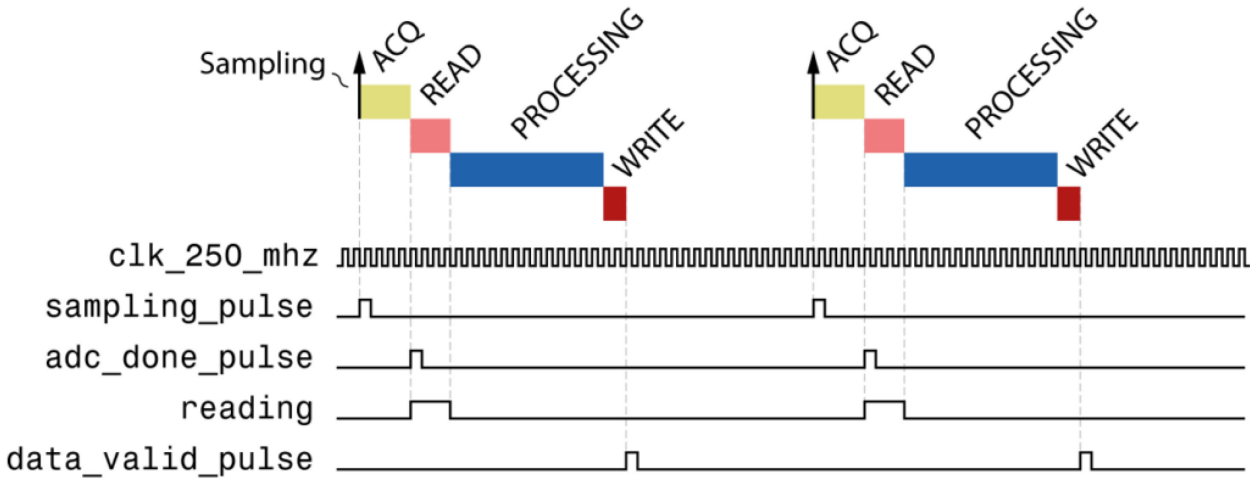


*Figure 69 - Boombox Timing*

Since the RTDS is capable of receiving up to 128, 32-bit data points via the Aurora channel, and the SBI/SBO interfaces only provide 16, 32-bit data points, it was decided to split the data transmission from the CPU to the FPGA over multiple Clock0 periods. Since some data also needs to be passed as control / status signals, 8 32-bit data points are transferred each Clock0 period.

Table *8* outlines which SBI/SBO registers are used for data transfer and control, while Table *9* defines the bits of the two control words. Figure 70 provides a block diagram overview of the system.

Table 8: Imperix FPGA Register Identification

| Register Number | SBI Use | SBO Use |
|---|---|---|
| *0/1* | *Data_Out[0]* | *Data_In[0]* |
| *2/3* | *Data_Out[1]* | *Data_In[1]* |
| *4/5* | *Data_Out[2]* | *Data_In[2]* |
| *6/7* | *Data_Out[3]* | *Data_In[3]* |
| *8/9* | *Data_Out[4]* | *Data_In[4]* |
| *10/11* | *Data_Out[5]* | *Data_In[5]* |
| *12/13* | *Data_Out[6]* | *Data_In[6]* |
| *14/15* | *Data_Out[7]* | *Data_In[7]* |
| *16/17* | *Control_Out* | *Control_In* |

Table 9: Control Word Bit Maps

| Bit Range | Control_In Name | Control_In Purpose |
|---|---|---|
| *0* | *RESET* | *Asynchronous Reset Signal* |
| *1:7* | *RX_Max* | *Total number of points to receive from RTDS* |
| *8:15* | *RX_Request* | *Index of first word to read back next clock cycle* |
| *16:23* | *TX_Max* | *Total number of points to transmit to RTDS* |
| *24:31* | *TX_Index* | *First word presented to FPGA this clock cycle* |

| Bit Range | Control_Out Name | Control_Out Purpose |
|---|---|---|
| *0* | *Channel_Up* | *Status bit; 1 indicates channel is established* |
| *1* | *XFRIP* | *Status bit; 1 indicates data is being transferred to CPU and new packets will be ignored* |
| *8:15* | *RX_Index* | *Index of first word presented to CPU this clock cycle* |
| *16:23* | *Soft_Count* | *Number of soft errors since last reset* |
| *24:31* | *Hard_Count* | *Number of hard errors since last reset* |

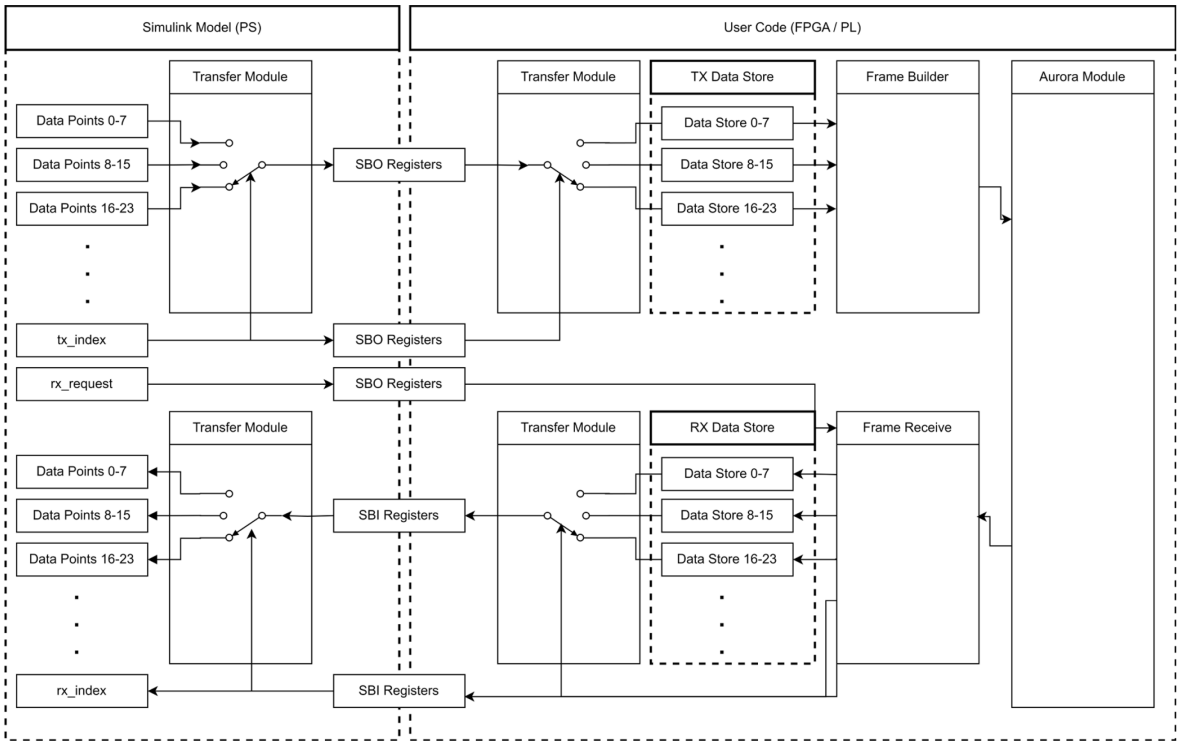


*Figure 70 - Boombox Data Transfer Block Diagram*

Figure 71 demonstrates the typical process for transferring data from the CPU to the FPGA. In this example, 16 data points are transferred, with Data X representing 8 data points. TX_Max is set to 16 and held constant for the duration of the process. At t = 9, data_valid_pulse is asserted by the Imperix IP. At this point, the Simulink model presents the first 8 data points (Data 0) on the SBO registers, along with TX_Index = 0. The user code reads the value of TX_Index from the SBO registers, and sets the Data_Read_Next flag. At the next Imperix clock edge, Data 0 will be transferred from the SBO registers to the data store, using TX_Index to locate it properly starting at word 0. This delay allows all assignments to remain non-blocking.

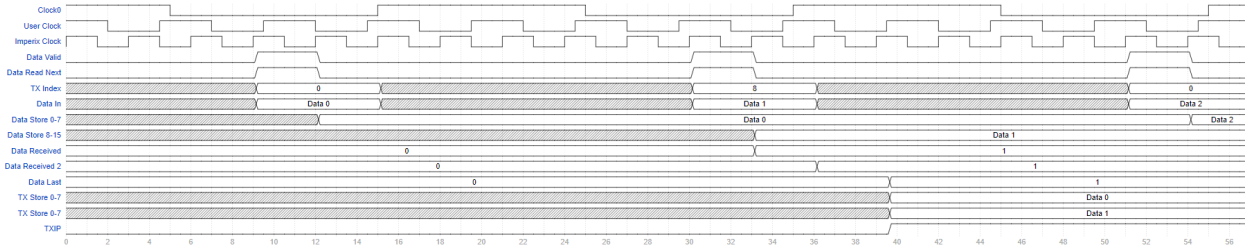


*Figure 71 - Example Waveform for CPU to FPGA Data Transfer*

At t = 30, the data_valid_pulse is again asserted, this time with the second set of 8 data points (Data 1) on the SBO registers and TX_Index = 8. This block of data is stored to words 8-15 of the data store. As TX_Index has reached its maximum value (TX_Max – 8), the user code recognizes that a full data set has been received and can now be transmitted to the Aurora channel. The Data_Received counter is incremented at the Imperix clock edge, to signal that a new set of data has been received. At the next edge of the User clock, Data_Received is compared to the last captured value (Data_Last); since the two do not agree, new data has been received. After a one period delay (to avoid data instability, see below), the data store is copied into the transmission store (TX_Store) and the transmission in progress (TXIP) flag is asserted, to begin the transmission process.

If a full set of data points is received prior to the transmission process finishing (TXIP being de-asserted), it will be discarded. However, provided the last portion of the data is received after TXIP is de-asserted, the full packet is kept intact due to the use of the data store. In addition, copying the data into a transmission store rather than sending from the data store ensures that data is kept synchronized (i.e., the first 8 words and the last 8 words of a transmission are from the same data set transferred to the FPGA).

The process of transferring data from the FPGA to the CPU is similar, and an example is shown in Figure 72. RX_Request is set by the Simulink model, and determines the starting index of the data presented to the CPU on the next Clock0 cycle. RX_Index presents the starting index of the data currently presented to the CPU, and should always be used by the Simulink model for processing the data. Again, a data store is used to ensure that data is synchronized and new data will be rejected if received while the transfer of the previous data is still in progress. Receiving is considered concluded when the last 8 data words have been requested and presented to the CPU.

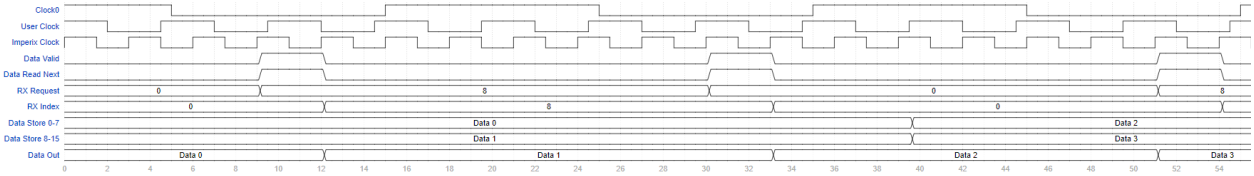


*Figure 72 - Example Waveform for FPGA to CPU Data Transfer*

Due to the lack of synchronization between Clock0 (which is synchronized to the Imperix clock) and the User clock, there exists the possibility for unstable data to be read. This can cause unpredictable results.

Data synchronized to a clock in a hardware description language (HDL), such as Verilog (used here for the user code), is latched at either the positive or negative clock edge. This latching occurs using flip-flops; due to propagation delays in logic circuitry, including the flip-flops themselves, there is a period of time prior to the clock edge where the data must be valid and held constant (setup time) as well as a period of time after the clock edge where the data must remain constant (hold time). If either of these conditions is not met, the output may latch to an unknown value – it may be 0, 1, or Z, which can be read by some logic as a 0 and other logic as a 1.

Such a violation can occur due to the lack of synchronization between clocks; in the example in Figure 73, the output is latched at the positive edge of User clock at t = 7, and is switching from 0 to 1. For some small period of time after the clock edge, the output is not guaranteed to be 1 – as the latches transition from 0 to 1, propagation delays mean that the signal may remain at 0, or may even oscillate briefly between 0 and 1. If the next positive edge of the Imperix clock occurs shortly after this clock edge, such as occurs at t = 8, the input that it latches may have the wrong value, as the output has not yet settled. Since there is no way to ensure that clock edges do not occur in close proximity to each other, a delay is instead used to ensure data integrity. Since data is being received synchronously with Clock0, which is very slow in comparison to either User or Imperix clocks, it changes very rarely from the perspective of the user code. Therefore, each time a change occurs in a signal that crosses clock domains, a delay is introduced before acting on the data, ensuring stability.

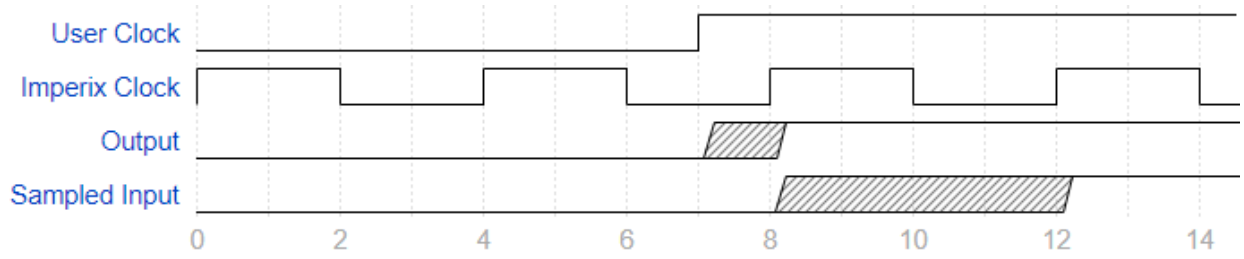


*Figure 73 - Waveform Demonstrating Clock Domain Crossing*

## A.3 Delay Measurement

The delay introduced as a result of the Aurora link is primarily due to the transfer process between the FPGA and the CPU, which takes multiple Clock0 cycles. Figure 74 shows a signal that was generated in the Boombox, sent to the RTDS and then looped back to the Boombox, all through hardware IO. The delay, measured from the perspective of the Boombox, is approximately 0.5ms, equal to the sampling time of the Boombox for this test. The same process was repeated using the Aurora link to transmit data from the RTDS to the Boombox, shown in Figure 75, and shows a delay of four times the Clock0 sampling time.

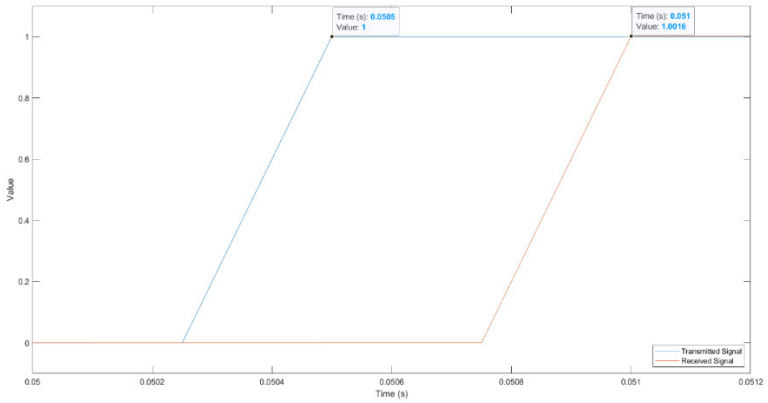


*Figure 74 - Delay Measurement, Hardware IO*

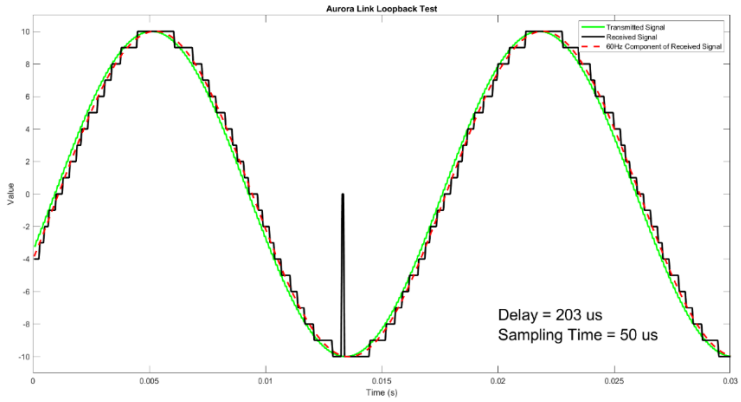


*Figure 75 - Delay Measurement, Aurora IO*