# High Mobility MIS Interfaces with Wide Bandgap Semiconductors

Eric Milburn

A thesis submitted in partial fulfillment of the requirements for the degree of

Masters of Science

in

Microsystems and Nanodevices

Department of Electrical and Computer Engineering

University of Alberta

***Abstract***

*As communications technologies continue to grow, the role of gallium nitride (GaN) transistors for high-frequency applications continues to grow as the speed requirements of more and more applications exceed the abilities of silicon. Today the vast majority of commercial GaN devices use HEMT architectures which are far more complicated to manufacture and have inferior off-state performance in comparison to standard MOSFET architecture. The primary cause for this is the lack of dielectric materials capable of forming an interface with GaN that does not dramatically degrade carrier mobility due to interface traps. In this research I demonstrate that atomic layer deposited (ALD) silicon nitride (SiN) forms an interface with GaN that bypasses any deleterious effects of interface traps and allows for high mobility of carriers within a simple three-layer MOSCAP device. The GaN-SiN-ruthenium system used in these MOSCAPs is analyzed through materials and electronic characterization to describe the chemical makeup and band structure of the system. These findings suggest a promising path of research for developing architecturally simple lateral GaN MOSFETs with speeds comparable to commercial HEMTs with superior off-state performance.*

## Preface

I, Eric Milburn, am the principal contributor to all chapters of this thesis. Chapter 4 of this thesis is based substantially off of Conference Proceeding #1.

Triratna Muneshwar and Alex Ma assisted with the deposition of all ruthenium contacts and SiN ALD films in throughout Chapters 4 and 5.

***Conference Proceedings Resulting from This Thesis Work***

Plasma Enhanced Atomic Layer Deposited Silicon Nitride on GaN MISCAPs with High Charge and Mobility, *CS Mantech 2020 Digital Digest*.

## Acknowledgements

One of the greatest lessons I learned in undertaking this research was the value of great advisors, mentors, collaborators, and supporters. I have been incredibly lucky to have had many amazing people fill these roles around me, and they have made the experience all the richer.

My gratitude to my supervisor Doug Barlage is immeasurable. His willingness to answer my endless stream of questions made the transition from a Materials Engineering undergraduate degree to an Electrical Engineering Masters program seamless. Under his mentorship I have watched myself develop from someone who was simply looking for an interesting research topic into a truly confident researcher with a strong understanding of the limits of knowledge and how they can be pushed.

Without the help of my colleagues my research would not have progressed nearly as far as it did. Alex Ma's experience with lithography and etching processes, Triratna Muneshwar's expertise in ALD, Ken Cadien for his ALD lab (which provided the SiN films which were a cornerstone of this research), and Gem Shoute's help with data analysis and modelling were all invaluable to this thesis. An honorable mention is also mandatory for the staff in Nanofab, whose friendliness and endless knowledgeability have allowed me to attain a high level of proficiency in a vast array of fabrication techniques.

I owe eternal thanks to my friends and family for all their support, which during the tumultuous months during which this thesis was completed kept me grounded and focused when the world was bleak. My mother, father, and sister's endless curiosity in my work forced me to understand it better myself, and inspired me to continue asking the hard questions of my findings. Finally, to my love Lindsay, the welcoming set of arms there for me at the end of every day, and the set of eyes that meticulously proofread everything within these pages, I am perpetually grateful.

# Table of Contents

## List of Figures and Tables

# 1 – Wide Bandgap Semiconductors: Foundation of Future Electronics

## *1.0 – The Wide Bandgap Advantage*

As the demands of modern semiconductor devices continue to drift upwards, the incumbent material of choice in nearly all spheres of electronics – silicon – has over the past 20 years begun to stagnate as physical limits restrict the size and performance of devices[1]. In extremely small devices such as complementary metal oxide semiconductor (CMOS) circuits, electric fields in the channel become high and the low critical field ($E_c$) of silicon allows sub-threshold conduction through the channel. A similar challenge arises in high-frequency and high-power devices where high voltages – rather than small dimensions – are responsible for the high electric fields necessary to drive high frequency switching or high power outputs. With a small bandgap of 1.1 electron volts (eV), silicon inherently generates a relatively large concentration of intrinsic charge carriers, particularly at elevated temperatures, which can lead to high off currents and poor high temperature performance[2]. Low thermal conductivity exacerbates this issue, particularly in high-frequency devices where power dissipation generates heat that must be removed from the circuit, requiring extensive dedicated cooling systems to boost switching frequency.

In order to meet these challenges, wide bandgap semiconductors have been investigated since the middle of the 20$^{th}$ century as potential replacements for electronic components where smaller device footprint, higher frequency operation, higher power output, higher temperature operation, or any combination of these specifications are desired. Evaluation of an arbitrary semiconductor to perform well in these categories is typically achieved by aggregating the semiconductor's material properties into various figures of merit. For power applications, the Baliga Figure of Merit (BFOM) expresses the inherent tradeoff between a vertical power transistor's power usage (due to ON resistance $r_{on}$) and the transistor's breakdown voltage ($V_{bd}$)[3]; materials that can minimize a transistor's power use while maximizing breakdown voltage have a high BFOM.

$$BFOM = \epsilon \cdot \mu \cdot E_g^3$$

The Johnson Figure of Merit (JFOM) expresses the product of two parameters relevant to high-frequency transistors, the critical electric field ($E_c$) and the saturation velocity of carriers in the semiconductor[4] to evaluate theoretical switching speed limits.

$$JFOM = \frac{E_c \cdot v_s}{2\pi}$$

Another popular figure of merit for high-frequency switching applications is the Baliga High Frequency Figure of Merit (BHFFOM)[5], which assigns a characteristic frequency (not to be mistaken for the true switching frequency limit[6]) to a given semiconductor.

$$BHFFOM = \mu \cdot E_c^2$$

Finally, a figure of merit that evaluates the suitability of a semiconductor for high frequency applications that also considers the material's ability to dissipate heat is the Keyes Figure of Merit (KFOM)[7], which includes the material's thermal conductivity ($\Phi_k$).

$$KFOM = \lambda \cdot \sqrt{\frac{c \cdot v_s}{4\pi\epsilon}}$$

When comparing all figures of merit for several semiconductors and normalizing the results to silicon using values from literature[8–17] as shown in Figure 1.1, popular wide bandgap semiconductors 4H-SiC and GaN clearly outperform silicon in suitability for high-frequency and high-power applications, additionally ZnO, which is considerably less developed than SiC and GaN in high voltage electronics research can also be seen to show potential for similar application areas.

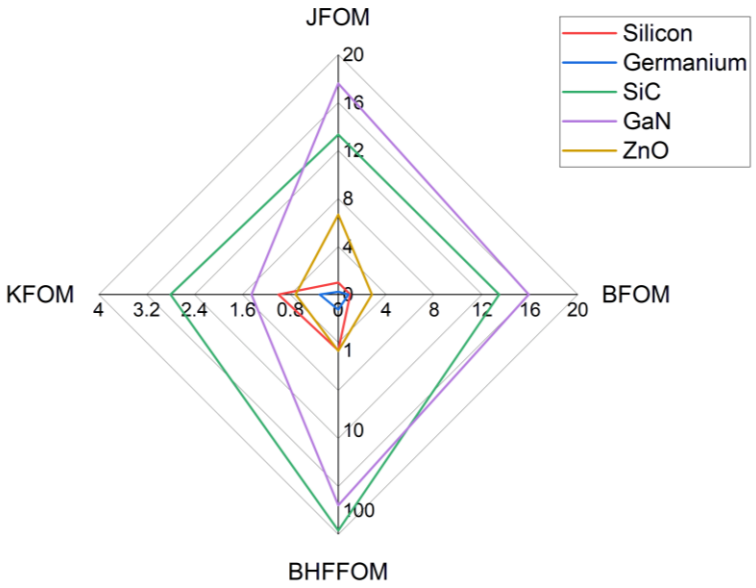


**Figure 1.1** – Comparison of common Figures of Merit for various semiconductors.

It is also worth noting that although the figures of merit described above provide a good rough guideline on the suitability of various semiconductors for use in high voltage applications, they are less useful in guiding the actual design of high-frequency and high-power devices[6]. Just as Dennard scaling drove the development of CMOS devices to achieve higher device densities and performance, more consequential device performance metrics have been proposed to drive the development of high voltage transistors. These parameters are the quality factor ($Q_{F2}$)[18], the gate charge ($Q_G$), and the maximum junction temperature between the device substrate and the packaging it is assembled with ($T_{j,max}$). $Q_{f2}$ can be calculated from the device material's thermal conductivity ($\lambda$), specific conductivity ($\sigma$), and $E_c$ while $T_{j,max}$ can be calculated from the case temperature ($T_c$), on current/resistance, and thermal resistance between the substrate and casing ($R_{jc}$).

$$Q_{f2} = \lambda \cdot \sigma_{sp,ON} \cdot E_c$$

$$T_{j,max} = T_c + I_{ON}^2 R_{ON} R_{jc}$$

The formulation for $T_{j,max}$ demonstrates that devices with lower ON resistance will have lower device-case junction temperatures due to lower power dissipation ($I_{ON}^2R_{ON}$), and that materials with strong thermal conductivity will have similar performance due to a decrease in $R_{jc}$.

In recent years, the motivation for development of wide bandgap semiconductor electronics has begun to shift away from prototyping and towards competitive commercial goals as wide bandgap devices begin to challenge traditional materials in power and radio frequency (RF) applications. As wide bandgap technologies mature, silicon based power devices are being replaced by 4H-SiC equivalents (market share projected as 27.3% by 2024)[19,20] while GaN RF devices are increasingly being used in favor of common GaAs components (market share projected as 7.5% by 2025)[21,22]. Several markets are responsible for the recent growth in the wide bandgap market, primarily energy and utility (power devices), communication technology and consumer electronics (RF, LEDs, and power devices), automotive technology (power devices) and aerospace/defense (RF, optical, and power devices[23]). As these markets adopt wide bandgap technologies – particularly with the advent of high frequency 5G cellular technology and electric vehicles (EVs) – the total wide bandgap market has increased from $210M in 2015[19] to around $600M in 2019 with a compound annual growth rate (CAGR) of ~30% and is expected to continue growing with an average CAGR of ~22% to nearly $3B by 2027[23].

### *1.1 – Wide Bandgap Semiconductor Materials Throughout History*

The history of wide bandgap semiconductor materials is diverse, ranging from ancient minerals that grew into electronic materials to space age inventions grown specifically for electronic uses. Of the popular wide bandgap semiconductors popular in research today (SiC, GaN, ZnO), the oldest is ZnO which occurs naturally as a white, powdery mineral that saw use in antiquity as a wound dressing, for skin treatment, and in the production of brass, paints, enamels, and rubbers. In 1890 the discovery of SiC crystals would be made by Edward Goodrich Acheson while passing a current through a graphite rod embedded in silica sand. Scaled up, this Acheson process[24] would be applied to the mass manufacture of SiC crystals for the abrasives industry. The early 1900s would see ZnO expand into new uses in cosmetics and pharmaceuticals[25], meanwhile a relatively new field of scientists investigating the interaction of crystals with electricity would yield some of the most groundbreaking discoveries of the 20$^{th}$ century. In 1906 Henry Dunwoody would invent a crystal radio using SiC[26] and in 1907 English engineer Henry Joseph Round would inadvertently create the first reported light emitting diode[27] when he passed a current through a crystal of SiC and observed luminescence at the anode. That same year, American physicist George Pierce would conduct similar research, developing a SiC rectifier[28] which he would patent two years later[29]. These discoveries would kickstart scientific interest in SiC and its crystal properties, and in 1915 German mineralogist Heinrich Baumhauer would coin the term "*polytypie*" to refer to the various lattice stacking patterns, or *polytypes* displayed by SiC crystals[30], polytypes of SiC would be found to have drastically different properties and would be investigated thoroughly later in the century. In 1931 James Bayard Parsons would synthesize the first GaN powder at the University of Chicago[31] by passing ammonia gas over liquid gallium (this technique would be repeated by Harry von Hahn at the University of Gdansk in 1940[32]). Compound semiconductor development would slow to a halt during World War II as focus shifted to more established technologies that could be rapidly developed for wartime technologies, however it is worth noting that SiC crystal radios saw heavy use during the war due to their resistance to interference from external vibration, ZnO also saw some use in the War as a component of zinc chloride smokescreen mixtures.

Interest in compound semiconductors would begin again in earnest in the 1950s. Research on the physical properties of GaN including conductivity[33], dielectric constant[34], magnetic susceptibility, band gap[35], emission and photoluminescence[36,37], and crystal parameters[38] would be conducted between 1956 and 1964. Fabrication technology for SiC would also receive a big boost in 1958

with the invention of the Lely sublimation method for SiC crystal formation[39], developed by Jan Lely at Phillips. With higher quality material, the development of SiC devices was rapid, with the development of the first SiC bipolar junction transistor (BJT) in 1959 by Robert Hall at General Electric[40] and the first SiC FET at Westinghouse[41]. The interest in SiC around this time would be bookmarked in particular by the holding of the first International Conference on Silicon Carbide[42], which featured sessions focused on the silicon-carbon binary system, crystal growth, crystal structure, solid-state physics, and SiC devices, and which featured esteemed presenters such as the aforementioned Robert Hall as well as William Shockley. In the frenzy of research on all semiconductors around this time it should come as no surprise that ZnO also saw heavy development, with research on optical, band, and transport properties being conducted starting in 1959 and stretching into the 1960s[43–45]. The early 1960's would also see developments in less prominent compound semiconductors with the development of the first intentionally designed optical spectrum LED by Nick Holonyak in 1962, which was made out of gallium arsenide and gallium phosphide and produced red light[46]. The late 1960s would see a number of further developments in LED technology, the first ZnO LED was built in 1967 and used copper (I) oxide as the p-type semiconductor of the junction[47]. In 1968 Herbert Maruska (who would later pioneer the use of Mg as a p-type dopant in GaN), would synthesize the first GaN crystals using halide vapor phase epitaxy while working at RCA labs[48]. These crystals had lower defect concentrations than those produced using previous processes and would result in the first GaN blue LEDs produced in 1971[48]. No significant milestones during this period would be achieved in SiC technology, although the material began to see use in UV detection systems[49]. So little work was being done on SiC that in 1982 the essay "Whatever Happened to SiC?" was published in IEEE Transactions[50], lamenting the fact that interest in high temperature SiC devices had tapered off over the previous decades. This lack of interest was attributed to the advent of integrated circuits and the scaling race taking place in silicon technology, as well as difficulty in SiC fabrication and the conclusion of many government programs that had been aimed at the exploration of SiC technologies. However, SiC would see a resurgence in the late 1980s as interest in SiC FETs using the 3C and 6H polytypes would surge[51–53] and the search for the superior SiC polytype for electronics would commence. The 1980s would also see one of the most critical processes in the development of GaN in 1983 when metal organic chemical vapour deposition (MOCVD) (which

was pioneered in the early 1970s by Harold Manasevit[54]) would be used to create high purity GaN crystals that would serve as a basis for GaN development in the following decades.

The 1990s would mark the beginning of the modern age of wide bandgap transistor technology. Transistor technology using GaN would be spearheaded largely by M. Asif Khan at APA Optics of Infineon, with documented demonstrations of both metal semiconductor FETs (MESFETs )and heterojunction FETs (HFETs) in 1993[55–57]. The following year would see the first SiC MESFET using the 4H-SiC polytype[58] which has become the contemporary standard for all SiC commercial devices, as well as J. Bayant Baliga filing patent for the SiC vertical power MISFET[59], an architecture that has driven a significant portion of SiC's modern market share in the power electronics industry. Work done in 1995 at Naval Research Labs would also yield the first work on GaN MISFETs, which used $Si_3N_4$ as the gate dielectric[60], integration of p-GaN would be achieved at Sandia National Lab in 2000 with the demonstration of a GaN junction FET (JFET)[61]. The first ZnO thin film transistors (TFTs) would be published in 2001[62], giving new life to the ZnO field that had focused primarily on optoelectronic devices for the previous several decades. The remainder of the 2000s would be focused on refinement of new wide bandgap technologies, and further material studies on polytypes[63] and electronic architectures such as the integration of JFET structures into power MISFETs (aka the "Baliga Pair"[64]) and self-alignment techniques[65] would carry wide bandgap semiconductors to the current state-of-the-art.

### *1.2 – State of the Art Wide Bandgap Technology*

While silicon carbide continues to undergo considerable research, it is in general a more mature materials system than GaN and ZnO[66]. Several material properties pertaining to quality of semiconductor material, quality of semiconductor-oxide interfaces, and full device characteristics serve as good benchmarks to assess the current state-of-the-art with respect to GaN and ZnO material technologies.

When depositing wide bandgap semiconductors the primary factors that will affect material performance are the crystal quality and dopant activation fractions. Crystal quality is critical for ensuring the minimization of defects that can scatter charge carriers, lowering their mobility, as well as allowing for uniform distribution of electric potential throughout the material, maximizing

breakdown strength. Single crystal growth of GaN is relatively well explored, and various deposition methods have been developed for different applications. High nitrogen pressure solution growth (HNPS) produces the highest quality films with dislocation densities as low as $2.2x10^2$ $cm^{-2}$, however it is an extremely slow process, growing around 1 μm/h[67]. Ammonothermal growth and sodium-flux methods provide similar dislocation densities but also have very low growth rates[67], leaving a need for methods of deposition for device grade (dislocation densities $<10^5$ $cm^{-2}$) GaN at more scalable deposition rates. Deposition of ZnO is still a highly debated area of research, and no one technology has emerged as dominant for producing high quality ZnO; among current research approaches which include epitaxial growth, sputtering methods, and solution processing, the current benchmark for dislocation density in ZnO comes from a deposition technology that hasn't traditionally been known for crystallinity: atomic layer deposition (ALD). Paired with rapid thermal annealing (RTA), ALD ZnO has reached dislocation densities as low as $5.2x10^9$ $cm^{-2}$, which while much higher than current GaN technologies is a big step forward for ZnO[68]. Dopant activation in semiconductors is important for reasons similar to high crystallinity, low dopant activation requires higher concentrations of dopant atoms to be added to the semiconductor, each of which serves as a scattering center for charge carriers. A considerable engineering problem in both GaN and ZnO over the past two decades has been finding p-type dopants that activate sufficiently to provide both high p-type mobility and conductivity. In particular, GaN p-doping with magnesium has only reached around 8% activation, and studies on the activation energy required for Mg dopants suggest that the theoretical maximum activation of Mg in GaN is only 8.2%[69]. Clearly further efforts into alternative p-doping strategies in GaN are required to maximize p-type or bipolar GaN device performance. A promising new doping strategy being applied to produce p-type ZnO is co-doping. This approach uses multiple dopants to simultaneously suppress native n-type defects in the ZnO while introuducing acceptor type states to provide hole conductivity. This approach using AlN co-doping has allowed for p-type activation up to 56.8%[70].

In order to assess material combinations suitable for device fabrication, several benchmarks measure a semiconductor's ability to interact favorably with other materials. Interface state density ($D_{it}$) is one of the most critical measures of the quality at a semiconductor-insulator interface. In GaN systems, ALD $Al_2O_3$ has shown the lowest $D_{it}$ at $1x10^{10}$ $cm^{-2}$ $eV^{-1}$, although interfaces with high-κ dielectrics have shown $D_{it}$ values on the same order of magnitude[71,72]. Studies on interfaces

between ZnO and dielectrics has been limited relative to GaN, the current $D_{it}$ benchmark in ZnO systems is between ZnO and plasma enhanced chemical vapour deposition (PECVD) $SiO_2$, with a value of $8.37x10^{11}$ $cm^{-2}$ $eV^{-1}$, which is almost 2 orders of magnitude higher than for GaN[73]. Next, of all semiconductor properties, carrier mobility ($\mu$) is arguably one of the most important, and pursuit of ever higher values of mobility (along with device scaling) has been one of the top drivers of faster devices in the semiconductor industry. Although mobility is typically cited as an inherent material property, it is quite often dependent on the architecture of the structure it is being measured in (except for Hall effect mobility, but even this can depend on metal-semiconductor contacts). In heterostructure devices like high electron mobility transistors (HEMTs), the mobility is a property of the 2D electron gas (2DEG) at the semiconductor-semiconductor interface, in metal insulator semiconductor (MIS) devices the field effect mobility is strongly affected by interface states. The highest GaN mobilities are seen in 2DEGs at GaN/AlGaN interfaces, with the room temperature benchmark at 3215 $cm^2$ $V^{-1}$ $s^{-1}$, while the benchmark for field-effect mobility is lower at 375 $cm^2$ $V^{-1}$ $s^{-1}$ with a $HfO_2$-GaN MIS structure[74,75]. In ZnO systems, bulk mobilities as high as 245 $cm^2$ $V^{-1}$ $s^{-1}$ have been achieved through boron doped melt growth[76], while field effect mobilities have been limited to 110 $cm^2$ $V^{-1}$ $s^{-1}$ in $SiO_2$ based TFTs[77]. Finally, gate capacitance in MIS structures is clearly dependent on the dielectric used. As such, both gate capacitance benchmarks for GaN and ZnO are from MIS structures using HfO2, which has a high dielectric constant of around 25. The benchmarks are 6.49 µF $cm^{-2}$ and 1.75 µF $cm^{-2}$ for GaN and ZnO respectively[72,78].

Finally, some benchmarks are properties of full devices, and demonstrate the state of the material technology in addressing particular applications. The unity-current-gain frequency ($f_t$) for transistors is a good measure of the ability of a material to fill high speed applications. High speed GaN transistors are already commercially viable, so it is no surprise that highly scaled GaN HEMTs have managed to achieve incredibly high $f_t$ values up to 454 GHz[79]. On the other hand, ZnO TFTs have shown promising results given their relative immaturity, and $f_t$ values up to 2.45 GHz[80] have been reported, suggesting ZnO TFTs may find space in the high frequency applications space. In the power electronics industry where high voltages are a requirement, another device benchmark defines the ability of a material system to hold up under strong potentials, the critical breakdown field ($E_c$). Once again, the more developed technology GaN devices have achieved the higher $E_c$ between GaN and ZnO with a value of 2.3 MV $cm^{-1}$ in high quality GaN epilayers[81],

however in recent years ZnO vertical devices have begun to benefit from better voltage distribution strategies, and critical field values up to 800 kV $cm^{-1}$ have been achieved[82]. Theoretical calculations place the maximum $E_c$ of both GaN and ZnO around 5 MV $cm^{-1}$, so the following decades of research may yet see many breakthroughs in these benchmarks.

**Table 1I –** Summary of GaN and ZnO material benchmarks.

| **Material/Device Property:** | **GaN:** | **ZnO:** |
|---|---|---|
| Defect density ($V^{-1}$ $cm^{-2}$) | $2.2x10^2$ | $5.2x10^9$ |
| Activation of p-dopants (%) | 8 | 57 |
| Interface state density ($cm^{-2}$ $eV^{-1}$) | $1.0x10^{10}$ | $8.37x10^{11}$ |
| Mobility ($cm^2$ $V^{-1}s^{-1}$) | 3215 ($\mu_{2DEG}$) | 245 ($\mu_{bulk}$) |
| | 375 ($\mu_{eff}$) | 110 ($\mu_{eff}$) |
| Gate capacitance ($\mu F$ $cm^{-2}$) | 6.49 | 1.75 |
| $f_t$ (GHz) | 454 | 2.45 |
| Critical electric field (MV $cm^{-1}$) | 2.3 | 0.8 |

# 2 – Theory of Interfaces in MIS Structures

## *2.0 – Structural Considerations*

### *2.0.0 – Interface Topography*

When depositing thin films of materials on top of one another, one of the most basic variables to consider when evaluating the quality of the interface is the interface topography. Irregular topography at the interface between two materials can have a number of consequences. The effect of surface roughness on breakdown behavior in MIS structures has been studied thoroughly both experimentally[83,84] as well as through simulation[85], and it is generally accepted that the field enhancements caused by surface roughness at the oxide-semiconductor interface can cause significant variance in the breakdown of the dielectric in MIS structures. Studies on sputtered $HfO_2$ dielectric films have also shown a correlation between topological roughness and the density of interface states and oxide charges, with higher sputtering voltages resulting in higher surface roughness and a shift in the flatband voltage of the MISCAP corresponding to traps in the oxide and at the interface[86]. This phenomenon is intuitive, since the majority of traps result from structural defects it is easy to imagine how a surface with irregular topology would increase the likelihood of material discontinuities that could manifest as electronic traps. Similarly, high surface roughness has been linked to high leakage currents through dielectric layers[86].

Evaluation of surface roughness is generally carried out using atomic force microscopy (AFM) which will be described in detail in Chapter 3. In order to truly measure the roughness of the oxide-semiconductor interface the measurements should be made on the bottom material, depending on deposition order, since the top material may either reduce the measured roughness as it fills the dips in the surface or enhance the measured roughness due to factors like high deposition rate which reduce uniformity. Usually to extract the most representative measure of surface roughness the AFM is scanned over a small area and the surface roughness is calculated as the root-mean-square (RMS) of the AFM tip position.

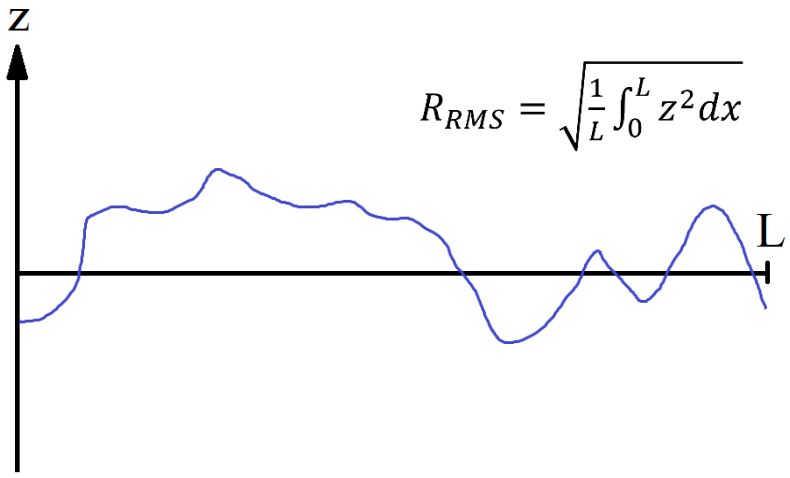


**Figure 2.1** – Representation of RMS roughness.

*2.0.1 – Interfacial Stress and Strain*

When two materials are in contact with one another, shear stresses and strains can develop at the interface between the two materials. Stress and strain at material interfaces in semiconductor devices are of interest for two different reasons. Firstly, excessive strain at material interfaces can degrade the quality of the interface, leading to dislocations and other defects that can affect breakdown behavior, increased trap densities, and increased leakage current. Secondly, interfacial strain can lead to polarization and an induced piezoelectric voltage due to the separation of positive and negative nuclei near the interface. This is the operating principle of GaN/AlGaN HEMTs, where piezoelectric voltages lead to a well of electrons known as a 2DEG, which demonstrates very high electron mobilities allowing for very fast devices. Interfacial stress and strain can be caused by a number of factors. In epitaxially grown layers such as AlGaN on GaN lattice mismatch between the two crystal structures generates the strain that leads to polarization. The other most common source of strain, particularly in films deposited by non-epitaxial methods is thermal expansion during deposition. Thermal stresses arise from a mismatch in the thermal expansion coefficient between the substrate material and the deposited material. If the deposited film is formed at elevated temperatures, both the film and substrate will undergo contraction upon cooling, but if the thermal expansion coefficients of the two materials are considerably different

this contraction will introduce strain at the material interface. For example, if a feature of length $L_f$ with thermal expansion coefficient $\alpha_f$ is deposited on a substrate with expansion coefficient $\alpha_{sub}$ at some temperature $T_{dep}$ before cooling down to room temperature (298 K) the feature will contract to a new length given as:

$$L_f' = L_f\left(1 + \alpha_f\left(298 - T_{dep}\right)\right)$$

Simultaneously, the substrate under the feature will contract in a similar fashion, but with a different thermal expansion coefficient:

$$L_{sub}' = L_f\left(1 + \alpha_{sub}\left(298 - T_{dep}\right)\right)$$

Taking the difference between the two equilibrium lengths and assuming the substrate will remain undeformed by the film, the strain introduced by the contraction $\varepsilon$ can be derived:

$$\Delta L = L_f' - L_{sub}' = L_f(\alpha_f - \alpha_{sub})(298 - T_{dep})$$

$$\varepsilon = \frac{\Delta L}{L_{sub}'} = \frac{(\alpha_f - \alpha_{sub})(298 - T_{dep})}{1 + \alpha_{sub}(298 - T_{dep})}$$

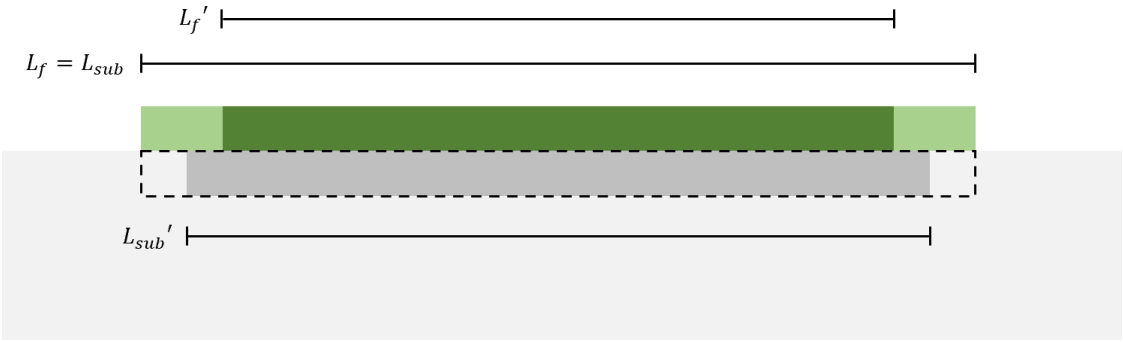


**Figure 2.2 –** Visualization of basic thermal contraction strain for the case where $\alpha_f > \alpha_{sub}$.

## *2.1 – Electronic Considerations*

### *2.1.0 – Band Structure*

Easily the strongest tool in evaluating electronic thin film devices is the band diagram, which gives an intuitive picture of the electron energy levels within the device.

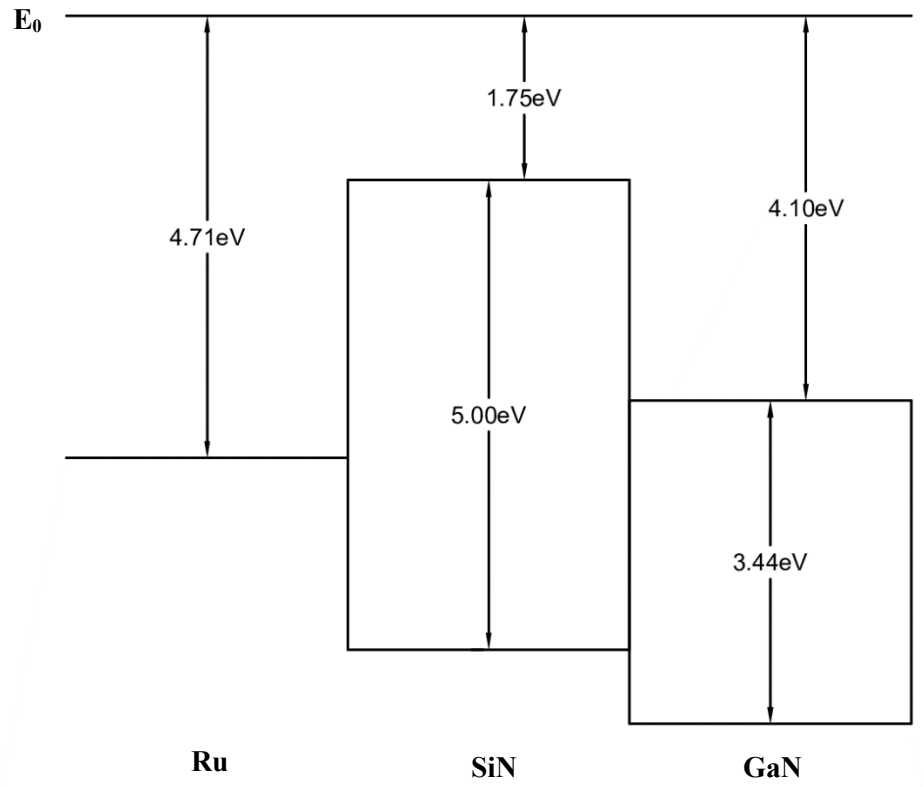


**Figure 2.3 –** Theoretical band diagram of a Ru-SiN-GaN MISCAP under flat-band conditions.

In Figure 2.3 above, the theoretical band diagram for a Ru-SiN-GaN MISCAP is constructed from literature values for the work function ($\varphi_m$), bandgap ($E_g$), and electron affinity ($\chi$) relative to the vacuum level $E_0$ for each material[8,87]. The diagram reveals a theoretical 2.35 eV electron barrier from the GaN to the Ru, this barrier is the primary controller of tunneling current which will be analyzed later. The diagram also reveals the fact that at flat-band conditions and at zero-bias conditions there is no barrier to hole-flow from GaN to Ru, however since all devices in this thesis are fabricated on n-type GaN substrates, and since GaN has an extremely small intrinsic carrier concentration to begin with (~$10^{-19}$ $cm^{-3}$), there will be virtually no holes present in the GaN and hole conduction will be negligible.

As will be investigated in this thesis, there are several non-idealities that can exist in MIS devices that cause deviation from the ideal band diagram. These include interface states or traps, as well as band-bending which can arise from several sources.

*2.1.1 – Interface States and Traps*

An unavoidable non-ideality in thin film structures is the presence of intrinsic and extrinsic defects at the interfaces between materials. Intrinsic defects form as a result of the termination of the material crystal structure, which results in a distribution of energy states within the material's (either semiconductor or insulator) bandgap, extrinsic defects result from dislocations, impurities, and other crystal defects near the surface, and result in a similar distribution of states. Depending on the exact position of these states they can be either positively charged (donor states) when empty or negatively charged (acceptor states) when occupied. This leads to an equilibrium point at which the charge from negatively charged acceptor states is equal to the positive charge from positively charged donor states, the Fermi level at the material surface will fix itself to this point provided there are sufficient carriers to fill the acceptor states. This fixation of the Fermi level is known as Fermi level "pinning" and results in energy barriers within thin film devices that deviate strongly from theory. Figure 2.4 below shows the band diagram from Figure 2.3 with the Fermi level pinned, leading to a different electron barrier from GaN to Ru.

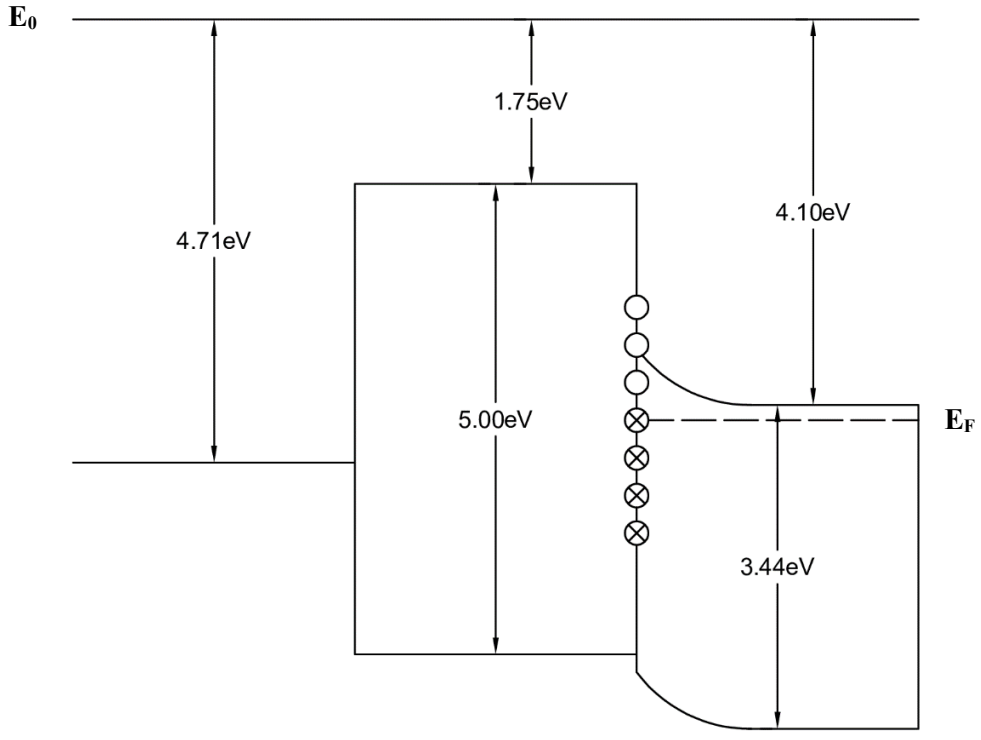


**Figure 2.4 –** Modified band diagram including Fermi level pinning from interface traps.

*2.1.2 – Interface Polarization and Band Bending*

Many factors can lead to bending of the energy bands in an MIS device. Some of these factors occur in all devices, for example all real devices will experience band bending at zero bias due to the difference in work functions between the metal contact and the semiconductor. Other causes, such as the Fermi level pinning described earlier are non-ideal and more difficult to predict. One particularly important factor, and an inherent factor in GaN devices that can further enhance this bending is polarization charge. Polarization charge occurs when the strain in a III-V semiconductor forms displaced regions of charge leading to a piezoelectric potential. This polarization charge leads to band bending at each side of the semiconductor interface, and in cases where this band bending creates a potential well that reaches below the Fermi level under equilibrium conditions, leads to the formation of a 2DEG. This 2DEG is the fundamental characteristic of GaN/AlGaN HFETs discussed in Chapter 1. Polarization in GaN can take two forms, spontaneous and piezoelectric polarization. Spontaneous polarization occurs naturally even on unprocessed GaN surfaces and arises directly from the equilibrium surface structure of the GaN crystal. Piezoelectric polarization occurs at GaN interfaces as a result of interfacial strain, and depending on whether the strain is compressive or tensile can enhance or dampen the spontaneous polarization already present at the GaN surface. A strong tool for evaluating band bending in equilibrium devices is the use of x-ray photoelectron spectroscopy (XPS), a simple method for this evaluation is given in Chapter 3.

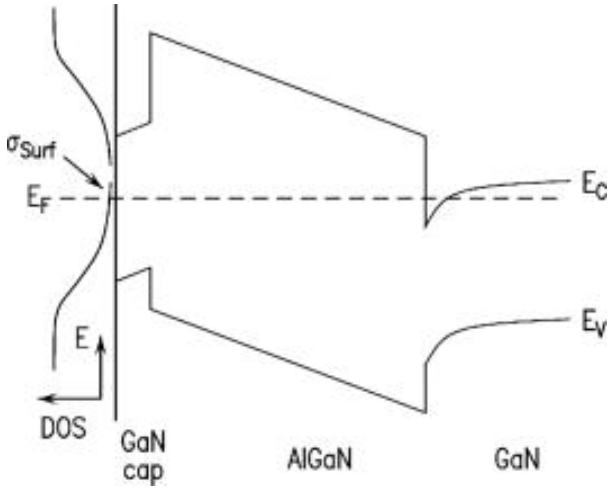


**Figure 2.5 –** Polarization induced band bending at an AlGaN/GaN interface[88].

# 3 – Fabrication and Materials Characterization of MIS Structures

## *3.0 – Sputtering of Metals*

Deposition of ruthenium and any other metals deposited in these studies was performed using standard sputtering techniques. The sputtering chamber used for deposition uses argon as the sputtering gas which is ionized and accelerated with a basic RF capacitively coupled circuit, the bombarding ions are confined near the target surface using a standard magnetron source. The chamber pressure, RF power, and sputtering time used are all provided in the fabrication section of Chapter 4.

## *3.1 – Atomic Layer Deposition*

### *3.1.0 – Deposition process*

The defining characteristic of ALD processing when compared to other similar methods such as chemical vapor deposition (CVD) is the use of precursors that undergo self-limiting reactions with the deposition surface to ensure that only one atomic layer is deposited at a time. The exact precursors used in this thesis for SiN films are covered in Chapter 4. By choosing ALD as the deposition method for this thesis, common thin film issues such as pin holing which can lead to excess leakage through the dielectric can ideally be avoided. ALD should also enable better control over the film thickness, allowing for more accurate analysis of dimension dependent quantities such as electric field.

### *3.1.1 – Plasma Enhanced ALD*

The films fabricated in this thesis take advantage of another technique in ALD: the use of a remote plasma source to provide the energetic nitrogen atoms required for the nitride films. The reactor used was set up with an inductively coupled plasma (ICP) source to produce these species. A remote plasma is a plasma set up such that the target is not within or in the vicinity of the discharge, which can prevent damage from high energy particles ejected from the plasma. Inductively coupled plasmas are also referred to as transformer coupled plasmas (TCP) because the mechanism of energy transfer from the external circuit to the plasma within the discharge chamber can be

modelled very accurately as a transformer circuit where and external inductive circuit couples to the inductance of charged carriers within the plasma discharge itself as shown in Figure 3.1 below.

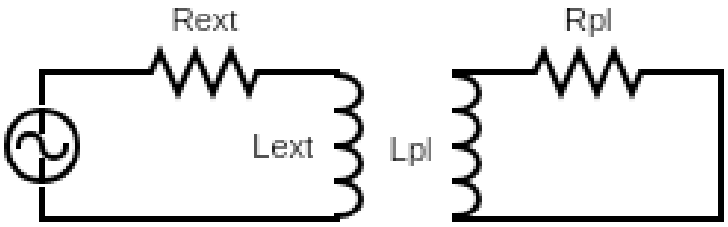


**Figure 3.1 –** Circuit representation of ICP discharge source.

This circuit can be used to design the necessary driving circuit based on the desired plasma discharge size. To begin it is necessary to know the rate of electron-neutral collisions ($\nu_e$), the density of charged species in the plasma sheath ($n_{sh}$), as well as the desired discharge radius ($\rho$) and length ($\lambda$). The measurement of the collision rate and sheath concentration is outside the scope of this project, but they can be found in basic plasma characterization literature. Once these parameters have been determined, the plasma skin layer where current flows ($\delta$) can be calculated as[89]:

$$\delta = \sqrt{\frac{m_e}{e^2 \mu_0 n_{sh}}}$$

And the plasma resistance ($R_{pl}$) and capacitance ($L_{pl}$) can be found as:

$$R_{pl} = \frac{2\pi\rho}{\lambda\delta}\frac{m_e \nu_e}{e^2 n_{sh}}$$

$$L_{pl} = \frac{\mu_0 \pi \rho^2}{\lambda}$$

Where $m_e$ is the electron mass. The external circuit characteristics can be calculated from these values as long as the number of inductive windings ($N_{wind}$) and the radius of the external windings ($R_{wind}$) (different than the radius of the discharge) are known, and the external resistance ($R_{ext}$) and inductance ($L_{ext}$) are given as:

$$R_{ext} = N_{wind}^2 R_{pl}$$

$$L_{ext} = \left(\frac{R_{ext}^2}{\rho^2} - 1\right) N_{wind}^2 L_{pl}$$

Which fully describes the necessary circuit for achieving the plasma, the required input currents ($I_{ext}$) and voltages ($V_{ext}$) are then given as:

$$I_{ext} = \sqrt{\frac{2P_{abs}}{R_{ext}}}$$

$$V_{ext} = I_{ext}\sqrt{R_{ext}^2 + \omega^2 L_{ext}^2}$$

Where $P_{abs}$ is the desired power absorption within the plasma, and is a design choice made based on the desired performance of the discharge in terms of plasma temperature, plasma energy distribution function, and other considerations.

*3.1.2 – Film Thickness Monitoring*

In-situ monitoring of the ALD film thickness was achieved using a fixed angle J. A. Woolam ellipsometer. By placing a reference substrate (silicon) in the middle of the deposition platen during deposition, and training the ellipsometer's source on this reference substrate, the film thickness and deposition rate can be determined for all substrates within the reactor. Ellipsometry works through the application of a beam of linearly polarized light onto a thin film deposited on a substrate. A model predicting the amplitude and phase of the reflected signal is used to fit the measured signal which can then be used to estimate film thickness and permittivity, among other parameters. This starts with calculating the reflectance and transmittance at each material barrier using Fresnel's equations, as well as the "phase distance" ($\beta$) of the film given as[90]:

$$\beta = 2\pi\left(\frac{d_1}{\lambda}\right) n_1 \cos(\theta_1)$$

Where $d_1$ is the film thickness, $\lambda$ is the wavelength of the incident light, $n_1$ is the refractive index of the film and $\theta_1$ is the angle of refraction into the film. Using these equations for the repeated internal reflections and transmissions leads to the model for total reflected amplitude and phase, which can be fitted to experimental data to determine film qualities.

### *3.2 – Lift-Off Processing*

Patterning of all metal layers in this thesis was performed using lift-off processing. Lift-off processing involves the use of an image reversal photoresist during lithography, this exposes only the regions of the substrate where metal deposition is desired after development. Metal is sputtered as described previously and when the photoresist is dissolved in acetone the metal deposited on top of the photoresist is released, leaving only the patterned metal on the substrate. Lift-off processing has a number of advantages, the most important of these is it avoids use of etchants, so consideration of the substrate chemistry in any chemical agents is not required.

### *3.3 – Characterization*

#### *3.3.0 – Atomic Force Microscopy*

In order to ensure material surfaces were sufficiently smooth, and to analyze step heights on fabricated devices, atomic force microscopy (AFM) was employed. The working principle of AFM is the use of a laser which is reflected off a cantilever with a probe tip on the bottom. This tip is placed atomically close to the surface and a potential is applied to it which causes it to oscillate with a characteristic frequency which is detected in the movement of the reflected laser. As the tip is moved across the sample surface changes in distance between the tip and the surface cause changes in the vibrational frequency of the cantilever and measured signal, this information is transformed into a profile of the surface. This profile can be applied in a straight line to measure step heights of thin film features or can be applied to an area of a film to find the surface roughness as explained in Chapter 2.

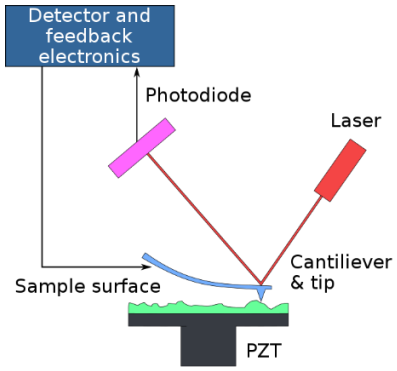


**Figure 3.2 –** Schematic of AFM mode of operation.

*3.3.1 – X-Ray Photoelectron Spectroscopy*

Elemental and energy level analysis of thin film devices can be carried out using XPS. When completing low level elemental analysis, use of XPS is quite straightforward, as only a simple qualitative picture is needed. More advanced analysis and in-depth knowledge of the XPS system setup is required to transform the raw counts-per-second (cps) data into accurate composition% data. Approximate depth profiling however is quite simple and a suitable method to confirm that all expected components of each film are present. Limitations on depth-resolution in XPS – which are only capable of being lowered to approximately 5 nm – are the primary limiting factor of depth profiling, although deconvolution of the data can be performed to estimate values with greater resolution, as will be explained below.

XPS can also be used as a tool to evaluate the band structure of thin film devices, and in this thesis XPS data will be used to make inferences about band bending behaviour near the GaN-SiN interface. In Zhao et al.[91] angle resolved XPS is used to estimate the band bending near the surface of plain GaN substrates as shown in Figure 3.3 (where the GaN surface is the left boundary of the diagram), where it is assumed that a glancing angle incident signal will probe mostly the GaN surface while more normal angle signals will probe deeper into the sample. This result is improved in the reference by modelling the detected signal as the integral of a continuum of signals coming from differing depths into the sample, by fitting the experimental data to this model they were able to estimate more accurately what the true value of $(E_{CL} - E_V)_{surface}$ is for $Ga_{3d}$ orbitals. In this thesis this technique will be used in the more approximate form and using a slightly different method. Since samples in this thesis will consist of three material layers, measurement of the GaN-SiN interface is not possible directly. However, since the samples were sputtered to achieve depth profiling, the measured signal as the probe depth approaches the GaN-SiN interface will begin to represent the interface and then eventually pass through the interface once the metal layer and some of the SiN layer has been sputtered away. With this under consideration it becomes clear that as the material is sputtered away the GaN energy bands at the interface will relax, and the difference in measured values (which correspond to $(E_{CL} - E_V)_{surface}$) will represent the surface band bending induced by the SiN interface with GaN.

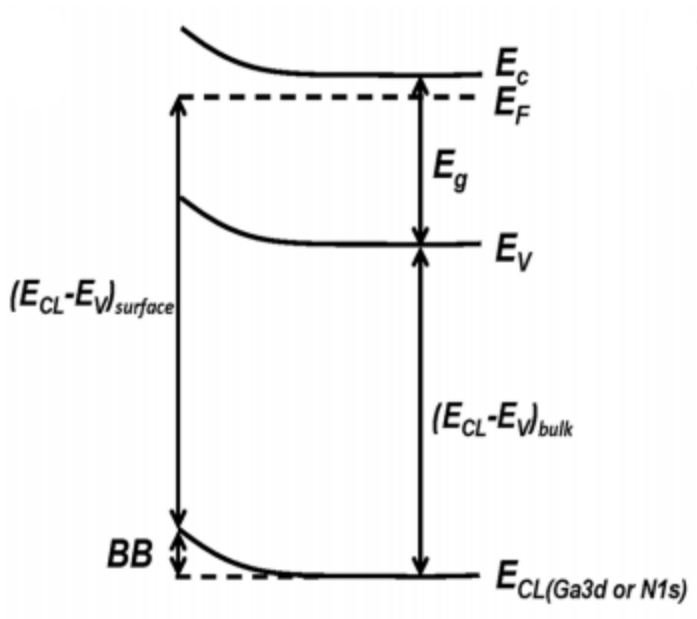


**Figure 3.3 –** Schematic from Zhao et al.[91] showing the energy levels associated with measuring band bending.

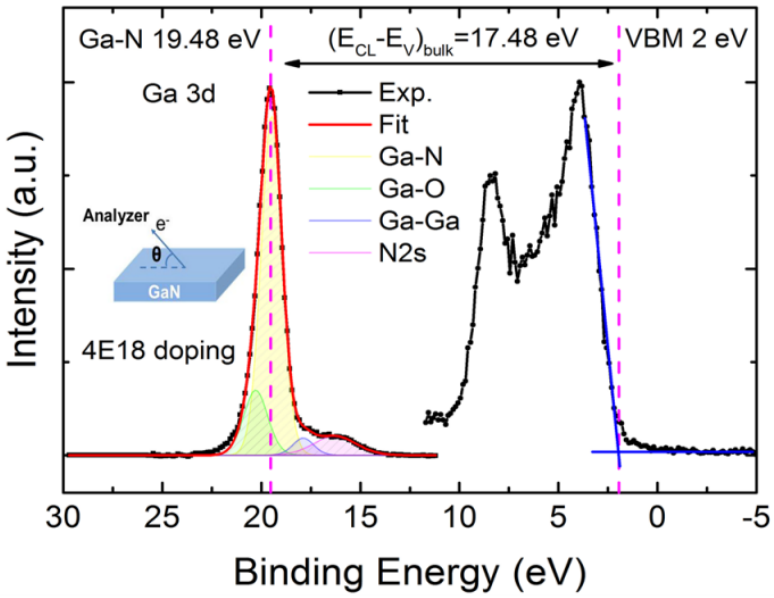


**Figure 3.4 –** Position of VBM from XPS data[91].

The reference gives the band bending equation as:

$$BB = (E_{cl} - E_V)_{bulk} + E_g - E_c - (E_{cl} - E_V)_{surface}$$

$$= \Delta(E_{cl} - E_V) + E_g - E_c$$

Where $(E_{cl} - E_V)_{bulk}$ is the energetic distance of the peak of interest (either $Ga_{3d}$ or $N_{1s}$) with respect to the valence band minimum (VBM) as shown in Figure 4.4, $E_g$ is GaN's bandgap, and $E_c$ is the conduction band position relative to the Fermi level ($E_F$). This distance can be found through the relation:

$$E_c = -kTln\left(\frac{n}{N_c}\right)$$

Where $n$ is the dopant concentration in the GaN and $N_c$ is the conduction band edge density of electron states in GaN[8].

# 4 – Oxide-Semiconductor Interfaces in Crystalline GaN MISCAPs

Parts of this chapter are adapted from an extended conference abstract which was published in the CS Mantech 2020 Digital Digest.

### *4.0 – Device Fabrication and Physical Characterization*

Identical MISCAPs were fabricated on three different types of GaN wafers which included $n^+$ and $n^-$ wafers from Kyma as well as $n^{++}$ wafers from University Wafer. All wafers were cleaned with piranha etch solution consisting of a 3:1 ratio of sulphuric acid to hydrogen peroxide to remove any organic matter or metallic contaminants on the surface[92]. Silicon nitride was deposited as the dielectric layer via ALD and was deposited without patterning on top of the GaN wafer, electronic methods of breaking the outer contacts of the devices are discussed in Section 4.1 to compensate for the un-patterned SiN at the outer contacts. Silicon nitride films were deposited using ALD with tris(dimethylamino)silane as the precursor for silicon and a forming gas ICP plasma consisting of 95% $N_2$ and 5% $H_2$ as the precursor for nitrogen. Further information on the ALD process as well as the ICP plasma can be found in a related study by Triratna Muneshwar[93], the fabrication parameters used during the deposition are listed in Table 4I below.

**Table 4I -** ALD parameters used for deposition of SiN films.

| Parameter: | Value: |
|---|---|
| Substrate temperature | 100 ˚C |
| Reactor pressure | ~1 Torr |
| 3DMAS pulse time | 0.1 s |
| 3DMAS purge time | 10 s |
| Forming gas plasma time | 10 s |
| Forming gas purge time | 10 s |
| GPC | ~0.35 Å |

The device contacts were patterned using a lift-off process along with sputtered ruthenium. For lift-off, the negative photoresist AZ5214E was used as it possesses a tendency to form a slight undercut during exposure which enhances the lift-off process. The photoresist was spun, baked,

and exposed according to the parameters outlined in Table 4II and the ruthenium contacts were then sputtered using inputs described in Table 4III.

**Table 4II –** Processing steps for AZ5214E.

| Process Step: | Description: |
|---|---|
| Spin coat | 10 s @ 500 rpm + 40 s @ 4000 rpm |
| Soft bake | 90 s @ 90 ˚C |
| Pattern exposure | 1.0 s @ 60.7 mW/s$^2$ |
| Hard bake | 120 s @ 110 ˚C |
| Flood exposure | 60 s @ 60.7 mW/s$^2$ |
| Development | Submersion and agitation in MF CD 319 x 35 s |

**Table 4III –** Ruthenium sputtering parameters.

| Parameter: | Value: |
|---|---|
| Sputter input power | 200 W |
| Chamber pressure | 1.8 mTorr |
| Sputter time | 500 s |

Finally, the lift-off step was completed by sonicating the samples in an acetone bath, taking care to not use too high a power setting to avoid damaging both the ruthenium and underlying SiN films. The full process flow is illustrated in Figure 4.1, starting from clean GaN wafers.

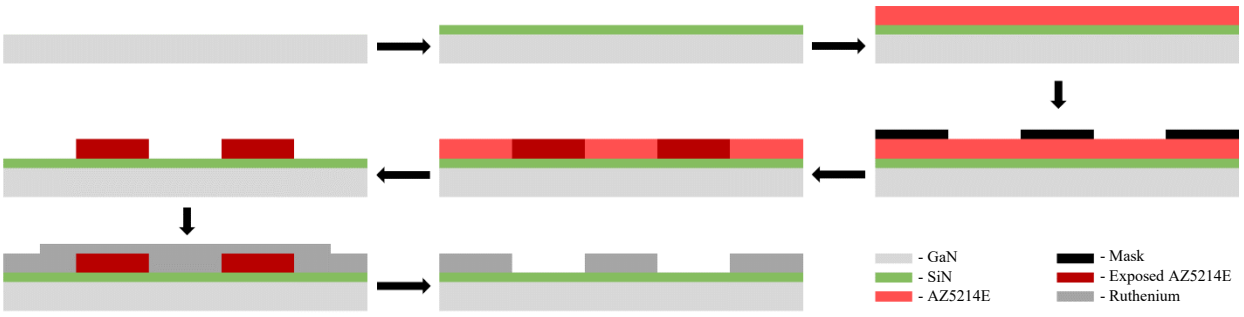


**Figure 4.1 –** Process flow for fabrication of SiN/GaN MISCAPs.

During fabrication and after electronic testing, physical characterization methods were used to gain insight into the quality of the fabricated devices. During fabrication, AFM was employed to monitor the surface roughness and topology of the deposited films since high surface roughness can enhance electrical breakdown effects and otherwise contribute to inconsistent device behaviour as discussed in Chapter 2. Images taken from AFM scans on top of the SiN and ruthenium films during fabrication of the Kyma $n^+$ devices are shown in Figure 4.2, AFM data also allows for direct measurement of the RMS roughness which was measured as 1.92 nm and 2.17 nm for the SiN and ruthenium films respectively. These values are low enough that surface roughness was not considered to be a significant factor in the electronic performance of the devices.

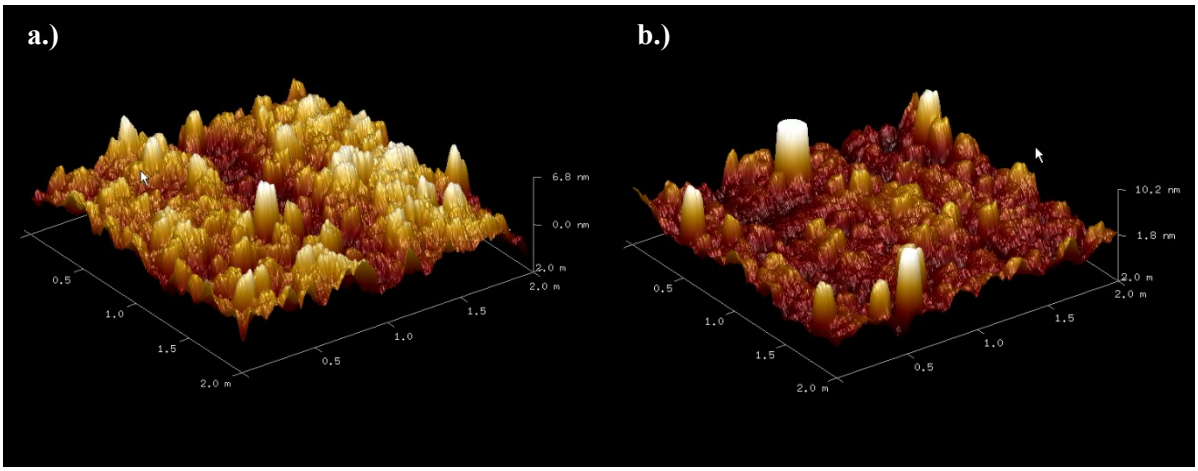


**Figure 4.2 –** AFM images of **a.)** SiN and **b.)** ruthenium film topology.

After full electronic characterization of the Kyma $n^+$ MISCAPs, they were subjected to XPS depth profiling to analyze the film composition as well as investigate the electronic band structure of the MISCAPs. In Figure 4.3 the expected depth profile is seen, with the ruthenium contact showing little oxidation while the SiN film at the interface between the ruthenium contact and GaN substrate shows substantial oxidation with a distinct hump in the oxygen signal. This result makes a clear case that the thin SiN films are oxidizing considerably after deposition, and hence for electronic analysis the dielectric will be treated as a silicon oxynitride (SiON) rather than pure SiN.

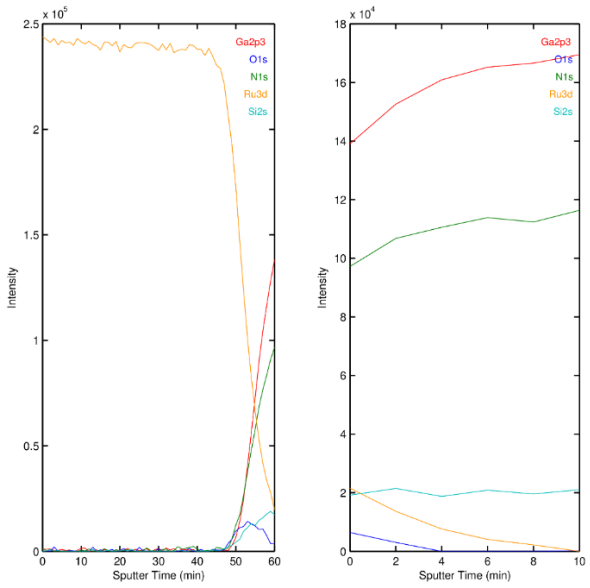


**Figure 4.3 –** XPS Depth profiling of Kyma $n^+$ SiN/GaN MISCAPs.

Full spectra results for several elements of interest were also measured using XPS, and Figure 4.4 includes the spectra for gallium, silicon, nitrogen, and oxygen. Peaks in the gallium 2p3 and nitrogen 1s XPS spectra appear at the expected positions for GaN crystals. Silicon 2s orbital peaks appear at the theoretical locations corresponding to Si dopants in GaN as well as Si-O and Si-N bonds in the 150-152.6 eV range, and 2p peaks corresponding to elemental Si and Si-O bonds. Surprisingly, the oxygen 1s peaks showed up around 530.7 eV, far from the 534.5 eV expected for Si-O bonds. This peak location is actually likely to result from Ga-O bonds[94], suggesting a degree of oxidation of the GaN wafer surface. The sequential peaks in Figure 4.4 result from repeat measurements as material is sputtered away, and using techniques described in Chapter 3 it is possible to make some hypotheses about the electronic band structure near the dielectric-semiconductor interface. The band-bending near the SiON-GaN interface is calculated to be approximately 1.81 eV. This result could suggest some degree of polarization, induced by the SiON film, by the natural polarity of the GaN surface, or by a combination of both.

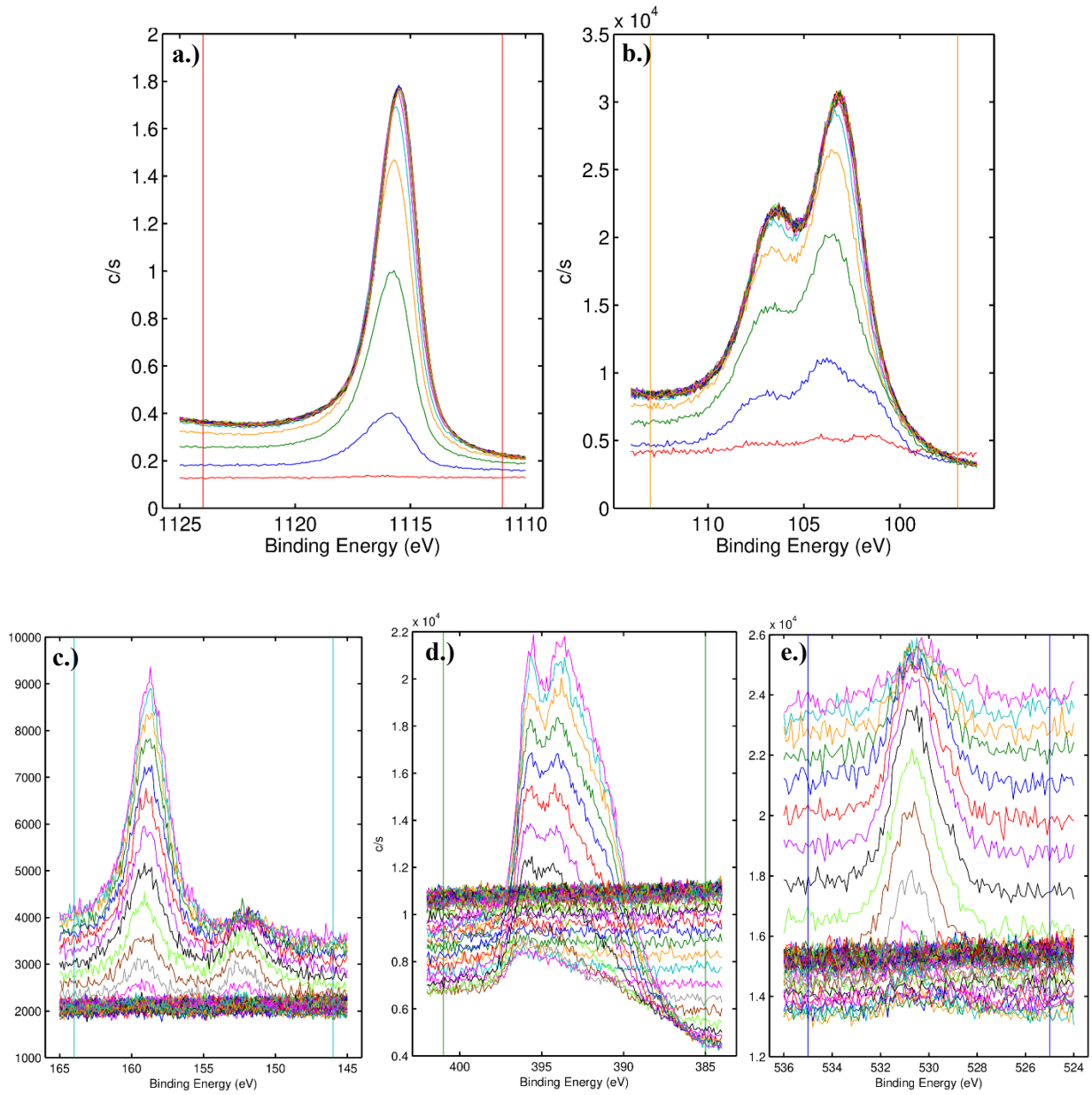


**Figure 4.4 –** Elemental XPS spectra for **a.)** gallium 2p3, **b.)** silicon 2p **c.)** silicon 2s **d.)** nitrogen 1s and **e.)** oxygen 1s taken from Kyma $n^+$ SiN/GaN MISCAPs.

### *4.1 – Electronic Characterization*

Current-voltage analysis was carried out on the MISCAPs to evaluate their behaviour as well as to investigate conduction mechanisms throughout the device. Prior to measurement, breaking of the SiON films under the outer contacts of the devices was required in order to remove the current

barrier and series capacitance that would otherwise arise from the MIS structure. Various methods for breaking this film were employed, with the most common methods involving either using large voltage pulses with very short ramp-up time or applying high voltages up to 100 V across adjacent outer contacts until avalanche breakdown occurred.

From standard IV curves (See Appendix A) a variety of curves were observed which complicated the analysis of which conduction mechanisms were dominating the device behaviour. Some devices showed nearly ideal diode behaviour with current switching from negative to positive at 0 V while many other devices transitioned from negative to positive current at a *negative* voltage before plateauing at voltages around 0 V and rising again at higher voltages. In order to gain a clearer understanding of the conduction mechanisms taking place in the devices, the current-voltage data was transformed to the form of a Fowler-Nordheim plot. The Fowler-Nordheim equation, under the famous Wentzel-Kramers-Brillouin approximations for tunneling current through a triangular barrier, takes the exponential form:

$$J = AE^2 \cdot e^{-\frac{4}{3}\frac{\sqrt{2qm^*}}{\hbar}\frac{\phi_b^{\frac{3}{2}}}{E}}$$

This equation can then be modified into a linear equation in logarithmic scale as:

$$\ln\left(\frac{J}{E^2}\right) = \ln(A) - \frac{4}{3}\frac{\sqrt{2qm^*}}{\hbar}\frac{\phi_b^{\frac{3}{2}}}{E}$$

This form allows for the simple identification of Fowler-Nordheim tunneling current regimes by normalizing the current by area into the current density (*J*), normalizing the voltage across the dielectric barrier into the electric field (*E*), and plotting $\ln\left(\frac{J}{E^2}\right)$ against $\frac{1}{E}$. If Fowler-Nordheim tunneling occurs, there will be a region of this plot with a distinct linear form with negative slope. This slope can then be used to calculate the tunneling barrier height ($\phi_b$) using experimental values of the electron effective mass ($m^*$) in SiON. When formulating these plots, it is also important to consider the distribution of potential throughout the device as only the potential difference across the dielectric is considered in the Fowler-Nordheim equation. In Figure 4.5 Fowler-Nordheim plots for devices fabricated on University Wafer $n^{++}$ wafers are shown. Away from the high $\frac{1}{E}$ region discrepancies in the shape of several of the $\ln\left(\frac{J}{E^2}\right)$ curves (primarily in the 3 nm devices of 4.5a

and all devices in 4.5b) continue to suggest that other conductivity mechanisms such as trap assisted tunneling are responsible for the variance in standard current-voltage characteristics observed across all samples. It is also worth making note of the distinctly lower values of $\ln\left(\frac{J}{E^2}\right)$ for the 5 nm SiON samples vs the 3 nm samples, which should be similar since the electric field normalizes film thickness. This can be explained if one considers that most defects in a deposited film occur close to the interfaces; if defects contributed conductivity in parallel to other tunneling mechanisms it is expected that as the SiON film becomes thicker, a better current barrier will begin to form and lower current will flow even at similar values of *E*. Ambiguity over the primary conduction mechanism disappears, however, at low values of $\frac{1}{E}$ as a consistent pattern begins to emerge and most samples demonstrate the expected negative-slope linear behaviour characteristic of Fowler-Nordheim tunneling. Moreover, the slopes in these linear regimes appear to be remarkably similar, suggesting a consistent tunneling barrier across all devices, even for different thicknesses of SiON.

In order to quantitatively analyze this observed pattern, we can numerically calculate the slopes in the linear regime after making suitable corrections to the voltage across the dielectric. For these devices, the high doping of the substrate removes most series resistance in the device, and the voltage distribution can then be established by treating the system as two capacitors in series, one corresponding to the oxide capacitance ($C_{ox}$) and the other corresponding to the capacitance across the electron layer immediately adjacent to the oxide in the semiconductor ($C_D$), which has a characteristic thickness of the Debye length ($\lambda_D$). Since the total charge held by both the oxide and the electron layer are equal, the potential distribution can be given as:

$$V_a = V_{ox} + V_D$$

$$V_a = \frac{Q t_{ox}}{\epsilon_{ox}} + \frac{Q \lambda_D}{\epsilon_s}$$

Where $V_a$ is the applied voltage, $t_{ox}$ is the oxide thickness, and $\epsilon_{ox}, \epsilon_s$ are the permittivity values for SiON and GaN, respectively. Taking the ratio of $V_{ox}$ to $V_D$ we get:

$$V_D = \frac{\lambda_D \epsilon_{ox}}{t_{ox} \epsilon_s} \cdot V_{ox}$$

Substituting into the first equation for $V_a$ the relation between $V_a$ and $V_{ox}$ becomes:

$$V_a = \left(1 + \frac{\lambda_D \epsilon_{ox}}{t_{ox}\epsilon_s}\right) V_{ox}$$

The Debye length for GaN can be calculated using the classical formula:

$$\lambda_D = \sqrt{\frac{\epsilon_s kT}{N_d q^2}}$$

Where $N_d$ is the dopant density which is extracted from the capacitance analysis later in this chapter to be approximately $10^{19}$ $cm^{-3}$ for the University Wafer $n^{++}$ wafers. Alternatively, a quantized capacitance where $\lambda_D$ is replaced with the centroid of the electron wave function away from the barrier can also be used, this value has previously been calculated to be approximately 2 nm[95]. A calculated $\lambda_D$ value of 1.11 nm was used in combination with literature values for the permittivity of GaN and SiON (8.9 and 5 respectively for SiON with approximately 50% oxidation[8,96]) and values of SiON thickness determined during deposition to calculate the correction factor for $V_{ox}$.

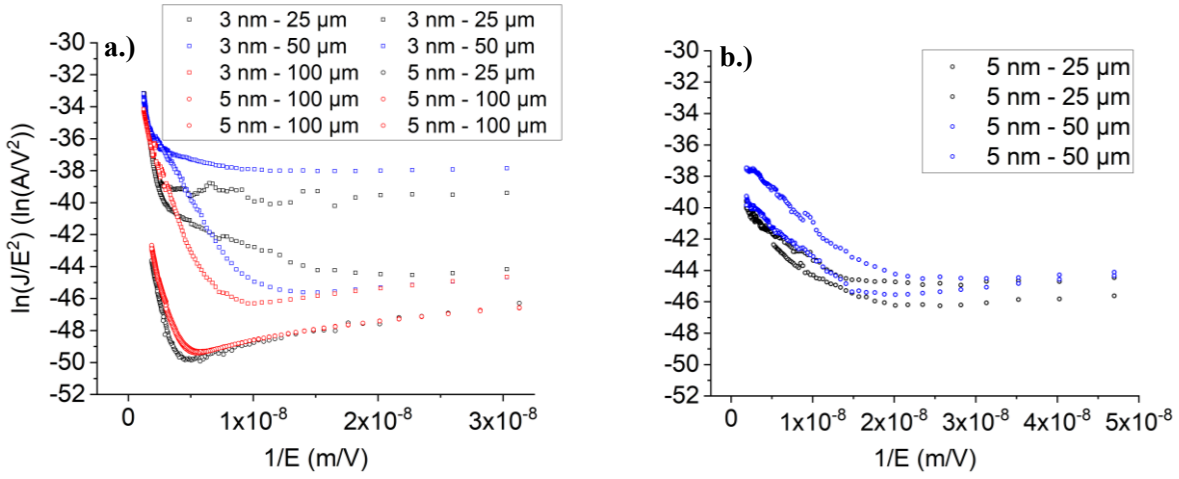


**Figure 4.5 –** Fowler-Nordheim plots demonstrating the two most common slopes.

With $V_{ox}$ and therefore $E$ corrected, the slope ($S$) of the Fowler-Nordheim plots can be converted to a value of barrier height ($\phi_b$) using:

$$\phi_b = \left(-\frac{3}{4}\frac{\hbar}{\sqrt{2qm^*}} S\right)^{\frac{2}{3}}$$

Where $q$ is the elementary charge and $m^*$ for SiON is taken as $0.4m_e$[96]. Calculating these values for all curves shown in Figure 4.5, three classes of barrier height are found. Within the samples displayed in Figure 4.5a nearly all curves have the same slope and therefore barrier height within the linear regime, with the exception of the 3 nm thick, 25 μm radius devices and one of the 3 nm thick, 50 μm radius devices which demonstrated a slightly higher barrier height. Within samples from Figure 4.5b a lower barrier height is determined, this may be a sign of a barrier that has been lowered through some physical process, but considering these curves' lower degree of convergence and linearity compared to the devices in Figure 4.5a it is more likely that these slopes are an artifact of other competing conduction mechanisms. It is also worth noting that the slopes in Figure 4.5b are very similar to the secondary slope (corresponding barrier of 0.206 eV) of the lower 3 nm thick, 25 μm radius data in Figure 4.5a, further suggesting that these slopes come from a conduction mechanism other than classical Fowler-Nordheim tunneling or a much lower barrier height.

**Table 4IV –** Three regimes of barrier heights with standard deviations.

| Number of Samples: | Barrier Height (meV): | σ (meV): |
|---|---|---|
| 4 | 222 | 12.32 |
| 7 | 953 | 6.95 |
| 3 | 1184 | 42.42 |

The testing of MISCAPs typically focuses primarily on assessing a material system's suitability for use in MISFETs. The primary characteristics that can be extracted from MISCAPs that translate to MISFETs are capacitance density, which dictates how much charge can be held under a device gate and consequently how much current can be generated from source to drain, as well as effective mobility which limits the operating frequency of the device. Capacitance measurements were carried out on the MISCAP structures to ascertain these properties from devices with outer contacts with broken SiON films as described prior in this chapter.

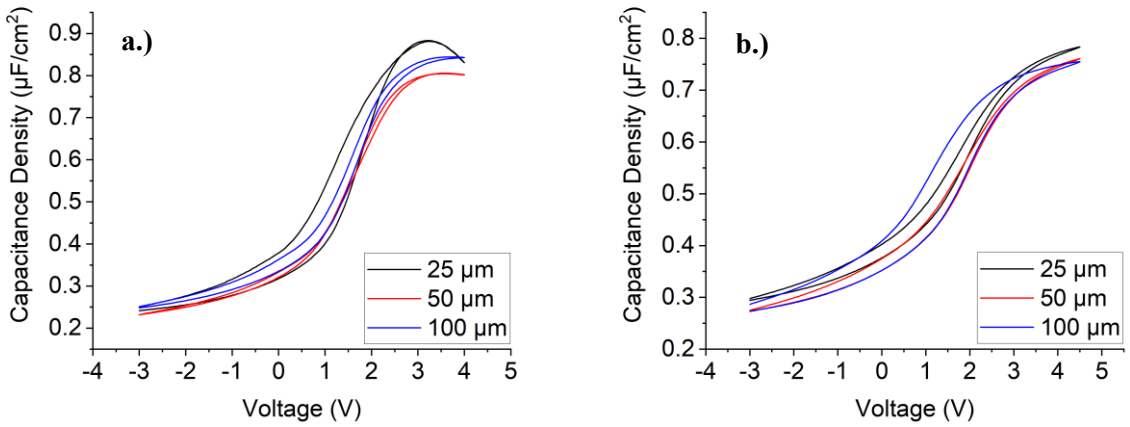


**Figure 4.6 –** Normalized capacitance-voltage plots for **a.)** 3 nm and **b.)** 5 nm SiON films.

Capacitance-voltage measurements were taken from test structures with inner contact radii of 25, 50 and 100 μm and outer contacts with varying area in order to verify that the outer contacts were not having any appreciable effect on the capacitance measurements. Measurements were made at a variety of frequencies to get a picture of the frequency dependence prior to full spectrum capacitance-frequency measurements. Dual sweep measurements were also taken to measure the degree of hysteresis in the devices. The measurements were normalized by the inner radius area to extract the capacitance density in common units of μF/cm$^2$, normalized curves from devices with SiON thickness of 3 nm and 5 nm on University Wafer n$^{++}$ wafers are shown in Figure 4.6. For both thicknesses the normalized curves align nicely with each other, demonstrating that the inner contact area is the primary source of the capacitance rather than the outer contact.

The good area dependence is also observed over larger sample sizes, Figure 4.7 shows averaged capacitance values from all devices with 3 nm and 5 nm SiON thicknesses vs. their inner contact area. The capacitance vs. area trend is linear, which once again demonstrates the good area dependence of the devices, as well as allowing extraction of the average capacitance density through linear regression of the series. Using this method the capacitance densities for both the 3 nm and 5 nm devices were found to be 0.827 μF/cm$^2$ and 0.757 μF/cm$^2$ respectively. It is worth noting that the capacitance density doesn't scale exactly as would be expected, since the oxide capacitance should scale inversely proportional to SiON thickness ($C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$) the capacitance density for the 3 nm films should in theory be $\frac{5}{3}$ times greater than the capacitance density of the 5

nm films, but in reality the ratio $\frac{C_{ox,3nm}}{C_{ox,5nm}}$ is calculated to be 1.092, considerably lower. However, this can be explained through consideration of leakage effects in the 3 nm films, which reach leakage current densities of 1 A/cm$^2$ where these effects become important[97] (the 5 nm films do not reach this current density). It has been demonstrated[97] that as gate length (which in a planar MISCAP structure is equivalent to the inner radius) shrinks the leakage correction factor is significantly reduced. Therefore, the 3 nm data with inner radius 25 μm and the lowest qualitative "droop" of the capacitance-voltage curve at high voltages (>2 V) is considered the best representation of capacitance density for the 3 nm films. This data is presented in Appendix B and it is seen that the data fulfilling the above criteria shows capacitance density of around 1.2 μF/cm$^2$.

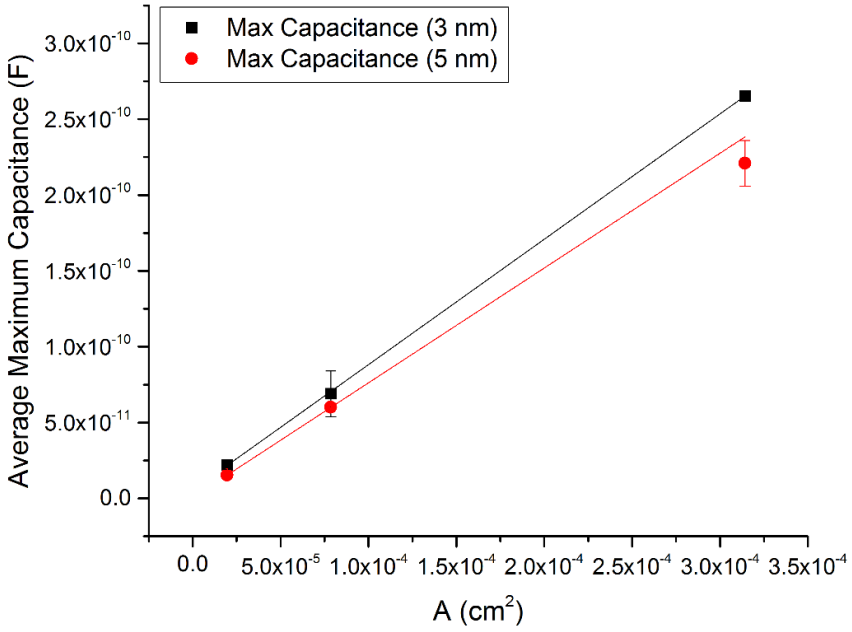


**Figure 4.7** – Capacitance vs. area plot for 3 nm and 5 nm films.

A key piece of material characterization that can be performed using capacitance-voltage data is the calculation of dopant density plots. The relevant equations from Schroder[98] are as follows:

$$N_d(W_{dep}) = \frac{2}{q\epsilon_s A^2 \frac{d\left(\frac{1}{C^2}\right)}{dV}}$$

$$W_{dep} = \frac{\epsilon_s A}{C}$$

However, it is also worth correcting the capacitance term in the depletion width to reflect only the depletion capacitance. The total measured capacitance in an ideal MISCAP is given by:

$$\frac{1}{C_{meas}} = \frac{t_{ox}}{\epsilon_{ox}} + \frac{\lambda_D}{\epsilon_s} + \frac{1}{C_{dep}}$$

Using this breakdown $W_{dep}$ can be reformulated as:

$$W_{dep} = \epsilon_s A \left( \frac{1}{C_{meas}} - \frac{t_{ox}}{\epsilon_{ox}} - \frac{\lambda_D}{\epsilon_s} \right)$$

Using the same values for the material constants as in the previous current-voltage analysis. This correction is unnecessary in the formula for $N_D$ because the differential operator removes the constant contribution from the oxide and Debye capacitances. Using these formulae the doping concentrations of the Kyma $n^+/n^-$ as well as the University Wafer $n^{++}$ wafers were all determined as a function of depth into the wafer and are illustrated in Figure 4.8 below. As expected the $n^+$ wafers are approximately an order of magnitude greater than the $n^-$, and the $n^{++}$ are two orders of magnitude greater than the $n^+$ wafers.

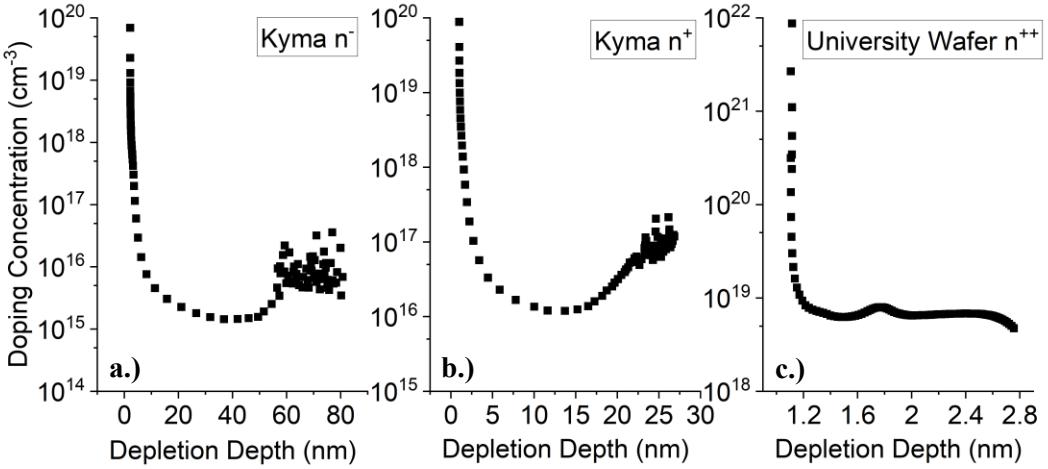


**Figure 4.8** – Extracted dopant density profiles from **a.)** Kyma $n^+$, **b.)** Kyma $n^-$, and **c.)** University $n^{++}$ wafers.

Another key insight provided by capacitance-voltage plots pertains tothe band structure of the device through the behaviour of the flat-band voltage. The flat band voltage is traditionally calculated at the point where the depletion capacitance disappears and the measured capacitance becomes the flat-band capacitance ($C_{fb}$), that is:

$$C_{fb} = \left(\frac{t_{ox}}{\epsilon_{ox}} + \frac{\lambda_D}{\epsilon_s}\right)^{-1}$$

Which can be calculated as 1.21 μF/cm$^2$ and 0.79 μF/cm$^2$ for 3 nm and 5 nm film thicknesses respectively. However, in practice the normalized capacitance values rarely reached these values, which requires some analysis. Three explanations are possible for why the measured capacitance density does not reach the theoretical flat-band capacitance: a.) the assumed SiON dielectric constant of 5 is higher than in reality, artificially increasing $C_{fb}$, b.) the film thickness calculated during deposition is lower than in reality, leading to the same outcome as a.), or c.) there is some other series capacitance ($C_s$) within the MISCAP system which is leading to a lower measured capacitance than would otherwise be seen. In order to investigate these possibilities an approximate method of extracting the flat-band capacitance was employed by taking the capacitance at the inflection point of the capacitance-voltage curve. This capacitance value was then used in conjunction with the flat-band capacitance formula to calculate what values of $t_{ox}$ or $\epsilon_{ox}$ would be required to achieve the extracted value of $C_{fb}$ assuming the other was close to theoretical/measured ($\epsilon_{ox}$ = 5 for variable $t_{ox}$ and $t_{ox}$ = 3 nm, 5 nm for variable $\epsilon_{ox}$). The results for approaches a.) and b.) are shown in Figure 4.5.

The results of analyses a.) and b.) do not provide a satisfactory explanation for the discrepancy between theoretical and measured capacitance density. If a larger than expected value of $t_{ox}$ was responsible it would be expected that the fitted values of $t_{ox}$ would be constant, it would also be expected that even if the expected $t_{ox}$ values of 3 nm and 5 nm were inaccurate, the 5 nm sample would still be thicker than the 3 nm sample, however in the results above the fitted $t_{ox}$ values between the two samples cross over one another. The fitted dielectric constant results encounter different issues, although they appear relatively constant with contact size the value itself is unphysical.

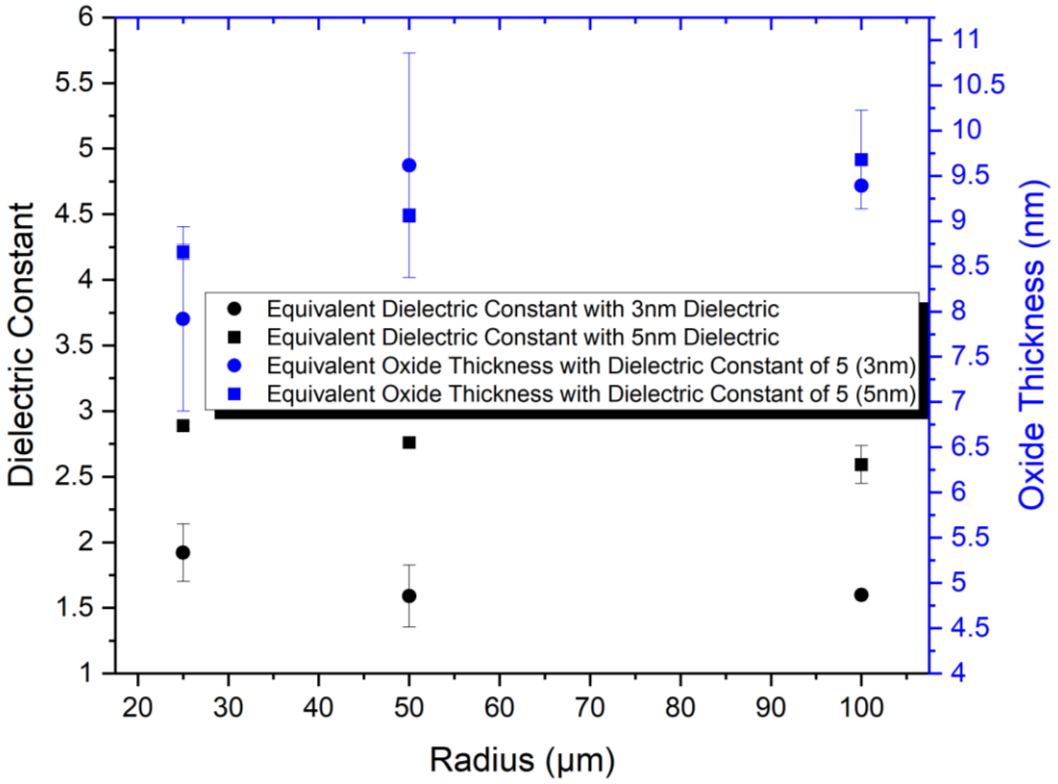


**Figure 4.9 –** Dielectric constant assuming accurate dielectric thickness and dielectric thickness assuming theoretical dielectric constant of SiON.

Even if complete oxidation of the SiN film to the point that it behaves like $SiO_2$ is assumed, a minimum dielectric constant of 3.9 would be expected, higher than every value for the fitted dielectric constant found here. Therefore, it is clear that a more robust model is needed to determine the composition of the devices fabricated. A third model is constructed assuming a partially oxidized film where *x* is the film oxidation fraction, it includes the Debye capacitance described earlier as well as another series capacitance in the form of a thin gallium oxide layer at the GaN substrate interface.

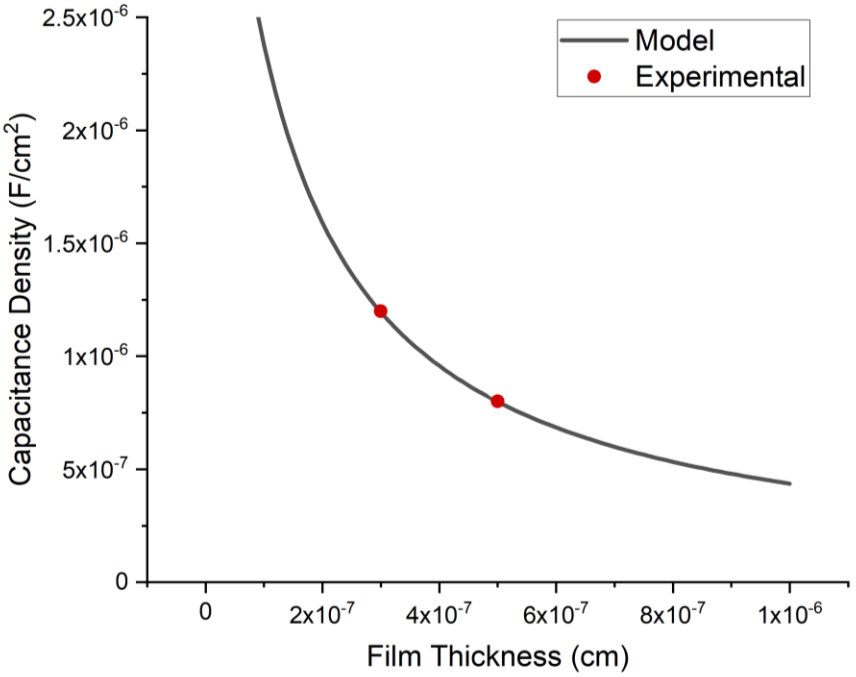


**Figure 4.10 –** Fitted capacitance data based off series capacitance model.

Suggested by XPS measurements, $Ga_2O_3$ has been known to act both as a semiconductor and as an insulator, the dielectric constant of $Ga_2O_3$ has been found experimentally to be between 10 and 15[99], since the $Ga_2O_3$ in our samples results from oxidized GaN it is expected that the dielectric constant would be closer to GaN at 8.9, so the lower literature value of 10 is used. This model results in an expression for the measured capacitance of:

$$C_{meas} = \left( \frac{t_{GaO}}{\varepsilon_{GaO}} + \frac{\lambda_D}{\varepsilon_{GaN}} + \frac{t_{ox}}{x\varepsilon_{SiO_2} + (1-x)\varepsilon_{SiN}} \right)^{-1}$$

By fitting this model to the corrected capacitance data for 3 nm films and the standard data for 5 nm films as shown in Figure 4.10, the fitting parameters of the model were determined as shown in Table 4V below.

**Table 4V –** Fitted parameters from MISCAP capacitance model.

| System Characteristic: | Value: |
|---|---|
| Gallium oxide thickness $t_{GaO}$ | 0.45 nm |
| Dielectric oxidation fraction $x$ | 0.60 |

The treatment of $Ga_2O_3$ as semi-insulating can be justified by comparing the diffusivity of silicon, known to dope both GaN and $Ga_2O_3$, within the two materials. Studies on silicon diffusivity have found the value to be around $4.5 \cdot 10^{-12}$ $cm^2/s$ for $Ga_2O_3$ and in the range of $1 \cdot 10^{-14}$ – $1 \cdot 10^{-12}$ $cm^2/s$ for GaN, measured around 1100 ˚C[100,101]. While these high temperatures are considerably higher than the ~100 ˚C used during ALD processing, it is still notable that silicon has higher diffusivity in $Ga_2O_3$ than in GaN, the effect of this over time or at elevated temperatures is that silicon will tend to segregate from $Ga_2O_3$ to GaN, since once it moves into regions of lower diffusivity it will slow down and necessarily accumulate. This mechanism effectively removes dopants from the $Ga_2O_3$ layer, causing it to act as a semi-insulator.

Taking the same approach as for the flat-band capacitance, the flat-band voltages of each capacitance-voltage curve was determined as shown in Figure 4.11 below. The values are seen to be almost constant for the 5 nm samples while there is a negative dependence on device area for the 3 nm devices. The values can be compared to the theoretical flat-band voltage for a ruthenium-GaN device, which can be calculated using the theory in Chapter 2 to be 0.65 V for GaN with doping concentration $10^{19}$ $cm^{-3}$, which is lower than the measured values. This value can be attributed to interface states, which can be calculated theoretically through the relation:

$$V_{FB} = V_{FB,0} + \frac{qD_{it}}{C_{ox}}$$

Where $V_{FB,0}$ is the theoretical flat-band voltage given above.

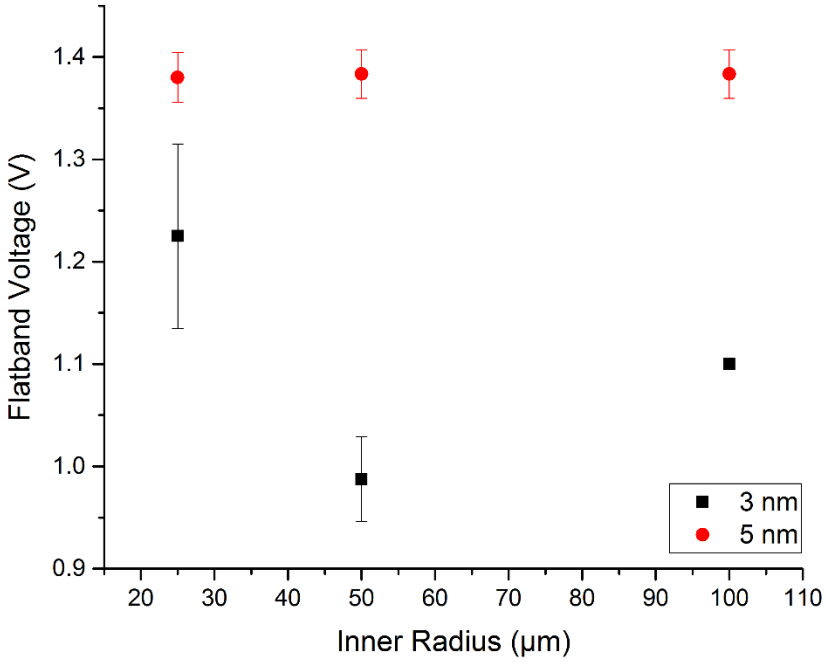


**Figure 4.11 –** Change in flatband voltage with contact size.

Solving for $D_{it}$ using this method and using the corrected dielectric constant of the 5 nm films found above, the 5 nm samples which each have $V_{FB}$ equal to about 1.375 V are found to have $D_{it}$ equal to $5.12 \cdot 10^{12}$ $V^{-1}$ $cm^{-2}$. Repeating the process for the 3 nm samples results in $D_{it}$ values of $5.3 \cdot 10^{12}$ $V^{-1}$ $cm^{-2}$ ($V_{FB}$ = 1.225 V), $3.04 \cdot 10^{12}$ $V^{-1}$ $cm^{-2}$ ($V_{FB}$ = 0.980 V) and $4.15 \cdot 10^{12}$ $V^{-1}$ $cm^{-2}$ ($V_{FB}$ = 1.100 V).

In order to confirm these values, interface state densities were analyzed further from conductance-frequency measurements using the technique described in Schroder[98]. In this technique the conductance can be related to the density of interface states through the relation:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln(1 + (\omega\tau_{it})^2)$$

Where $\tau_{it}$ is the interface trap recombination time constant, $\omega$ is the measurement frequency multiplied by $2\pi$, and $G_p$ is the measured conductance density. By plotting $G_p/\omega$ vs. $\omega$ it is observed that at some frequency there is a peak in $Gp/\omega$, this peak can be used to calculate the density of interface states with a basic scaling factor:

$$D_{it} = \frac{2}{q}\left(\frac{G_p}{\omega}\right)_{max}$$

Using this methodology $D_{it}$ was calculated for each device at each measurement voltage point and at 1 MHz (although any frequency could have been used due to the frequency independence of the capacitance-frequency measurements), resulting in Figure 4.12 which shows $D_{it}$ as a function of voltage for the 25 µm, 50 µm, and 100 µm radius devices respectively. Some immediate observations can be made in that the plots, particularly those for the 25 µm radius devices, appear remarkably similar to the capacitance-voltage curves seen in Figure 4.6, it is also notable that there is no real trend of interface trap density with capacitor area with all values remaining within the same ($10^{13}$ $V^{-1}$ $cm^{-2}$) order of magnitude. It also appears that the 3 nm devices on average had higher trap densities, which may be attributed to their reduced residence time in the ALD reactor, where elevated temperatures could help relax defects that would act as traps. Another trend across these data is the increasing disorder in values when moving from the 25 µm to the 100 µm devices. This could be a result of the increased series resistance influencing the measured conductance in unpredictable ways.

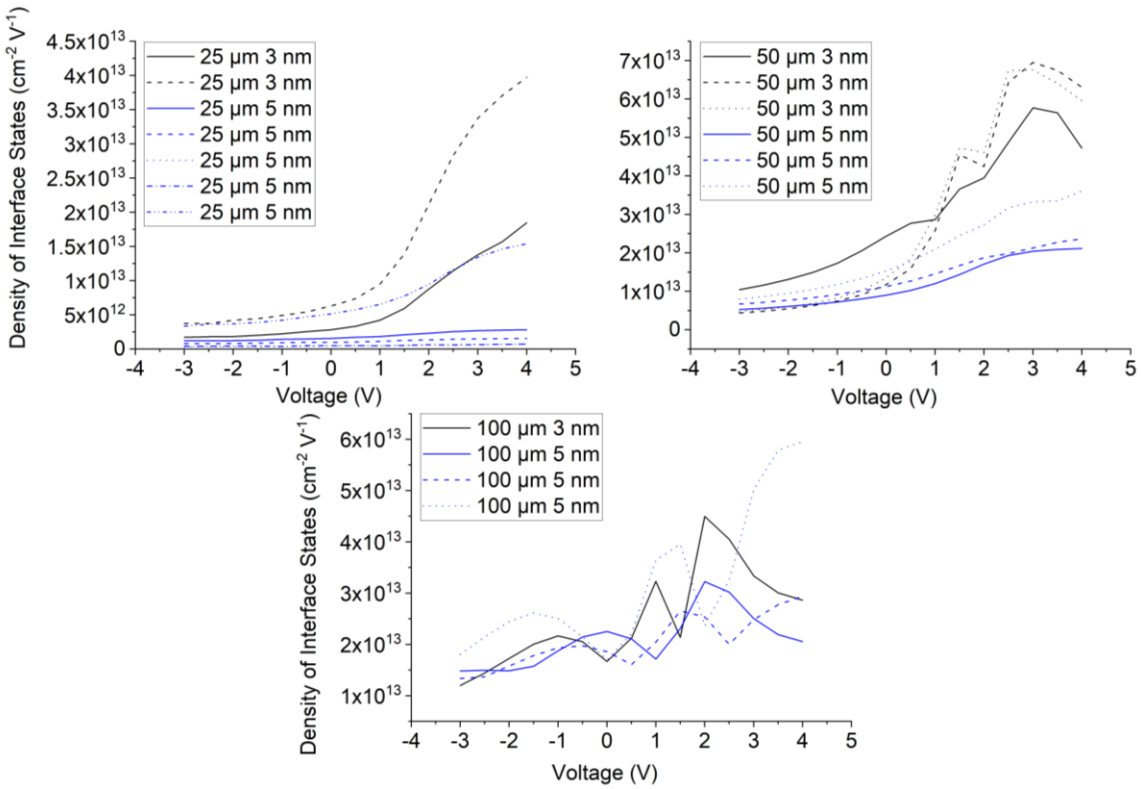


**Figure 4.12 –** Trap density vs. voltage for each device size.

The conductance method for interface trap density was also used to compare trap densities with capacitance-frequency characteristics. Figure 4.13 demonstrates how the frequency of peak trap density correlates to an unexpected rise in capacitance density at high frequencies, where the expectation would be to see a roll-off in capacitance as the frequency becomes faster than carriers can move with. This suggests that some sort of high-frequency traps are responsible for this rise in capacitance density. Finally, it is important to note that the trap densities measured through the conductance method are on average about one order of magnitude higher than the values calculated from the flat-band method. This suggests that the approximate method used to determine the flat-band voltage may have underestimated the flat-band voltages, leading to a lower-than-expected shift in $V_{FB}$ and lower interface state density.

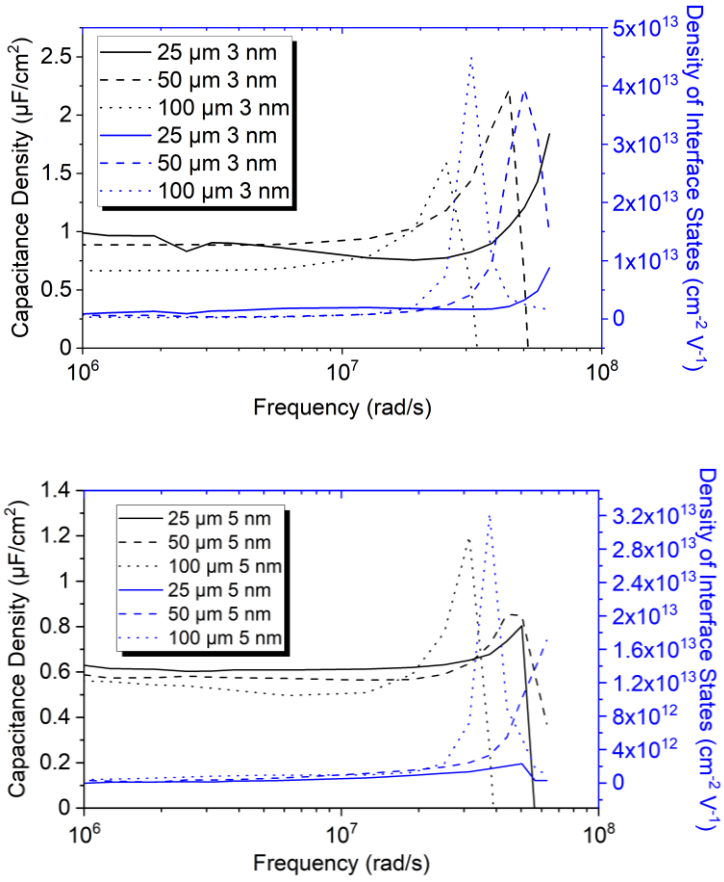


**Figure 4.13 –** Correlation between frequency dependence of traps and frequency dependence of capacitance for 3 nm and 5 nm devices.

In order to characterize the nature of these measured traps and investigate their role in conduction through the dielectric layer, current-voltage characteristics were measured at four temperatures ranging from 25 ˚C to 100 ˚C. These measurements were used to calculate the position of traps relative to the GaN conduction band edge. This is achieved by assuming tunneling is independent of temperature (which is generally true) and that any increase in current is proportional to an increase in carrier concentration due to shallow traps accumulating sufficient activation energy to be excited into the conduction band, resulting in the relation[72]:

$$E_A = \frac{d(\ln(J))}{d\left(\frac{1}{kT}\right)}$$

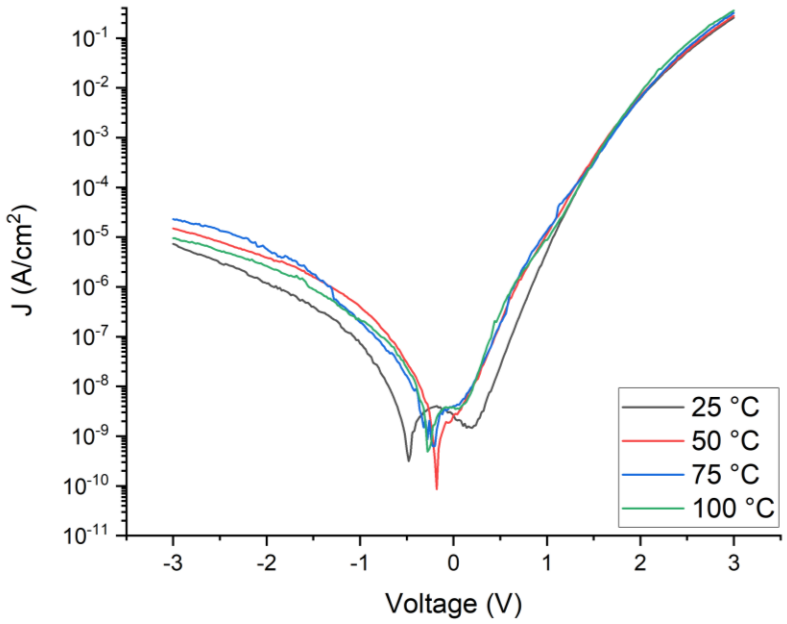


**Figure 4.14 –** Change of IV characteristic with temperature for a 3 nm $n^{++}$ MISCAP.

Using this relation, the slope of each current-temperature series shown in Figure 4.15a was used to calculate the activation energy at each voltage, resulting in Figure 4.15b.

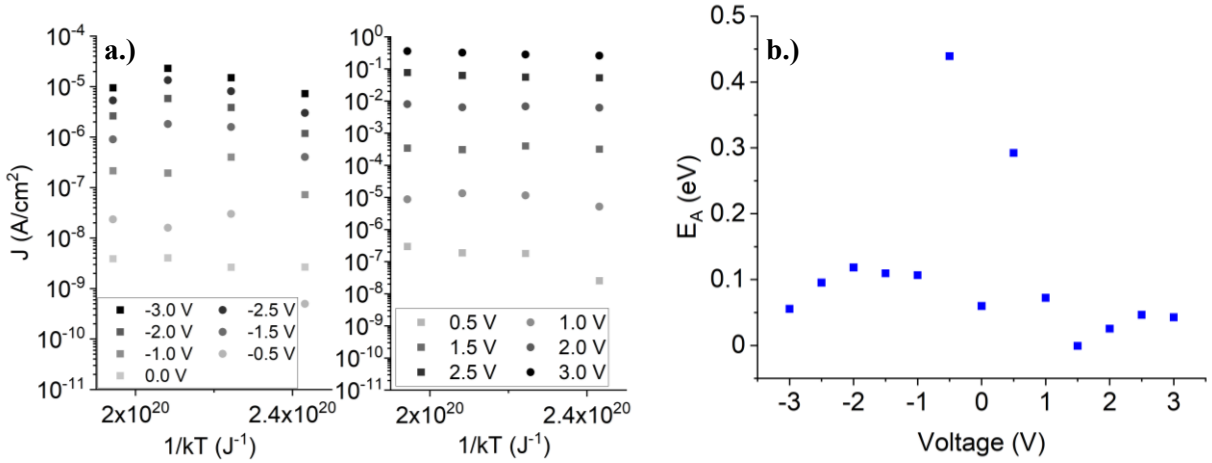


**Figure 4.15 – a.)** Current vs. 1/kT in depletion and accumulation, **b.)** calculated activation energy vs. bias voltage.

The results in 4.15b can be described as three regimes: depletion at or below -1 V, accumulation at or above 1 V, and neutral conditions around 0 V. In depletion the measured activation energies are generally around 100 meV and correspond to traps in the bulk GaN, while in accumulation the activation energies are around 50 meV and could correspond to shallow traps/dopants[102] in the GaN or alternatively to thermally assisted field emission, from the accumulation layer to conductive traps above the GaN conduction band in the SiON film. It is noteworthy that the accumulation activation energies are very low due to a relative insensitivity of current density to temperature in this regime. This suggests that in accumulation current is almost exclusively direct/Fowler-Nordheim tunneling limited, with very little contribution from trap assisted (Frenkel-Poole) tunneling.

### *4.2 – Extraction of Capacitance Density and Effective Mobility*

Further exploration of the properties of the GaN-SiON MISCAPs was carried out using techniques developed by Kyle Bothe for extracting the capacitance density and effective mobility from the roll-off behaviour of the capacitance-frequency curve using a distributed model[103]. The model is based on application of tapered transmission line theory and theory of small reflections to construct an expected capacitance model from the distributed system shown below.

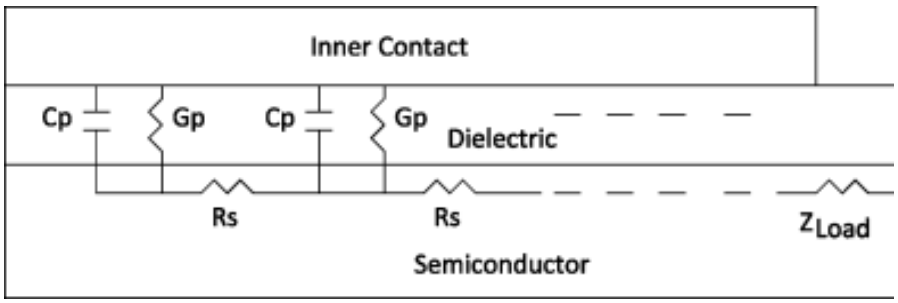


**Figure 4.16 –** Distributed model of planar capacitor[103].

This approach results in a model of measured capacitance ($C_m$) of the form:

$$C_m = f(f_m, C_p, G_p, R_s, Z_L)$$

Which can be applied to capacitance-frequency data that demonstrates a distinctive roll-off behaviour. This model was used to fit data from 100 µm inner contact radius devices fabricated on Kyma $n^+$ wafers as shown in Figure 4.17 below for several bias voltages. By performing this fitting for the full range of voltages measured a theoretical "true" capacitance can be extracted for each voltage and an extracted capacitance-voltage characteristic can be constructed, for the data in Figure 4.17 the extracted capacitance-voltage curve is shown in Figure 4.18 where it is compared with the leakage current through the dielectric layer.

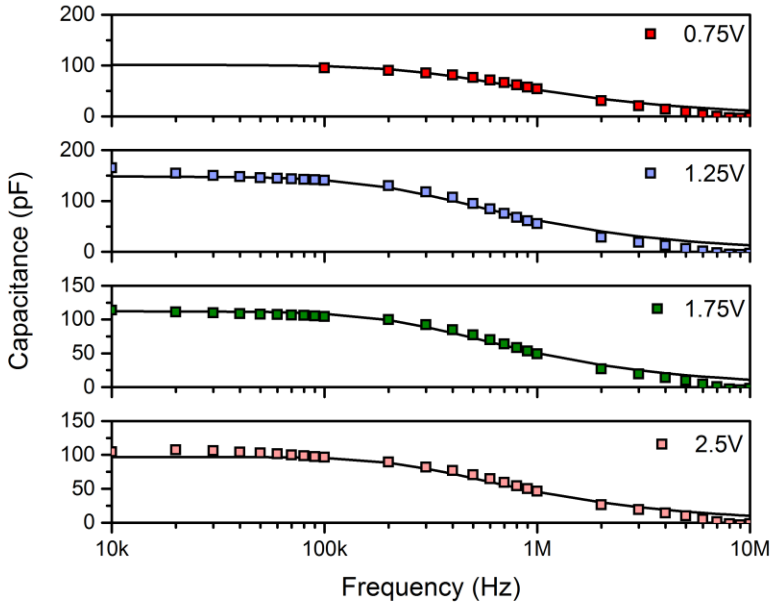


**Figure 4.17 –** Cf curves fitted according to distributed model.

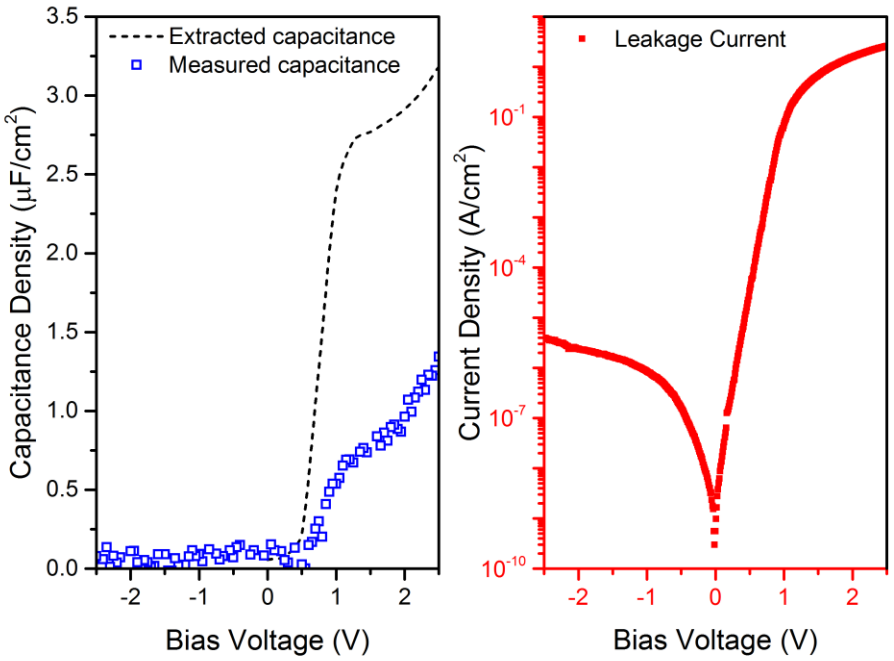


**Figure 4.18** – Extracted CV curve.

Even when taking into account that capacitance measurements typically become less reliable once current density through a film passes the 0.1 A/cm$^2$ point, the extracted capacitance density of over 2.5 μF/cm$^2$ is still very impressive and, even assuming a pure SiN film with a dielectric constant of 7.4, correlates to a very thin film thickness of 2.62 nm. Once the capacitance has been extracted it is also possible to calculate the theoretical effective carrier mobility using the extracted capacitance and extracted series resistance using the following:

$$\mu_{eff} = \frac{1}{R_s * Q_{acc}(C_p, V_A)}$$

$$Q_{acc} = \int_{V_{FB}}^{V_A} C_p dV$$

Applying these formulae to the same data and using the assumed dielectric thickness of 2.62 nm a mobility vs. electric field plot can be constructed. The characteristic follows a commonly seen trend, increasing as electric field decreases. The extracted mobility values are very high, and it is worth examining the extraction model to ensure that nothing is being miscalculated, however upon

inspecting the model it is found that any parameters that lower the extracted mobility increase the extracted capacitance. Attempting to increase $R_s$ lowers the model capacitance-frequency curve

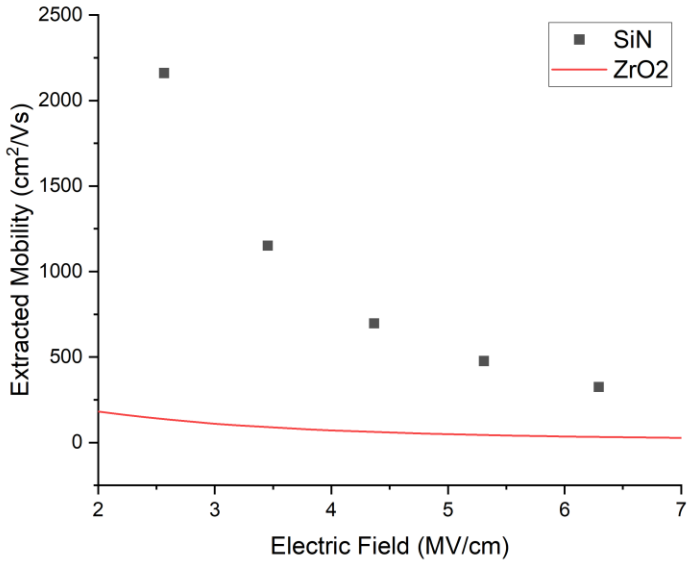


**Figure 4.19 –** Extracted effective mobility vs. electric field compared with values from $ZrO_2$[72].

below the experimental data, and the only way to properly fit it is by increasing $C_p$, which – while boosting $Q_{acc}$ and subsequently lowering mobility even further – requires more unreasonable values of dielectric thickness to explain the very high capacitance densities, thicknesses which are incompatible with the comparably low leakage currents. To put it succinctly, the data suggests either very high values of capacitance density or very high values of mobility. Data from devices fabricated on the University Wafer $n^{++}$ wafers suggest the latter. As shown in Figure 4.20 below, the devices fabricated on highly doped wafers, which will inherently have very low series resistance, show comparable capacitance density to the devices fabricated on the Kyma $n^{+}$ wafers, however their high-frequency performance improves markedly, with capacitance densities that are stable up to the upper limits of the Keithley 4200 SCS which was used to make the measurements, suggesting potentially even *higher* mobility values for these devices. It can also be seen that the capacitance-voltage characteristics are nearly independent of frequency. This data strongly suggests that the primary benefit of SiON-GaN structures lies in their potential for high-speed operation.

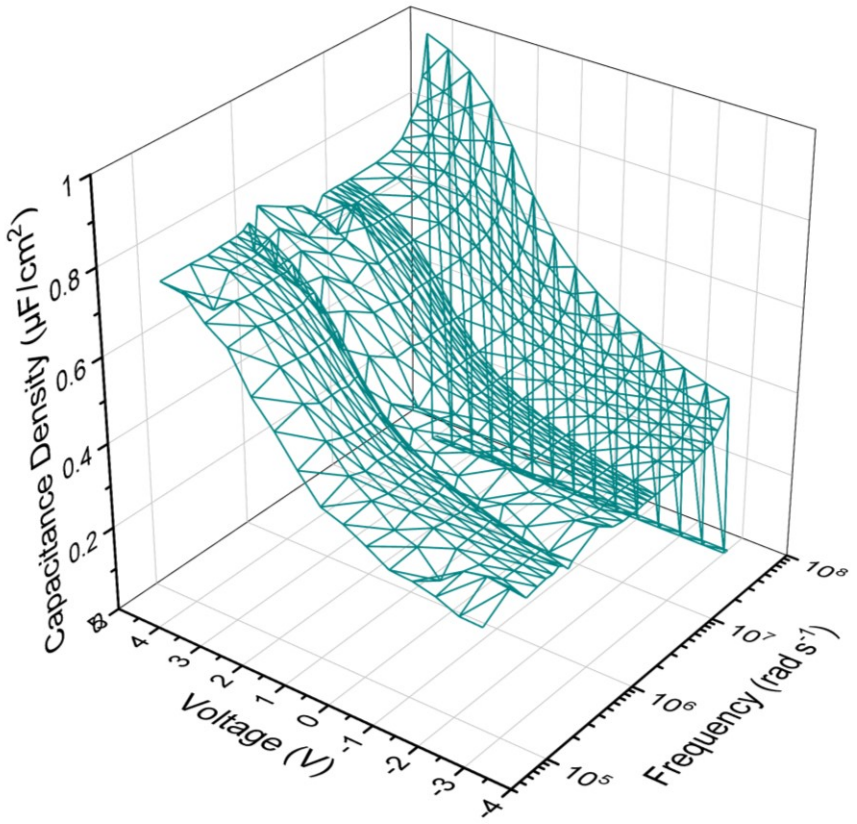


**Figure 4.20 –** Capacitance-frequency curves for $n^{++}$ 5 nm MISCAPs at different voltages.

One theory for why this system could provide such high mobility comes from the quantum mechanical considerations introduced earlier when considering the electron wave function centroid for evaluating capacitance. Both SiON and $Ga_2O_3$, which the experimental data suggests are the materials at the substrate-dielectric interface, have relatively high values of effective mass ($0.4m_e$, and $\sim 0.3m_e$ respectively[96,104]). The effect this would have on the electron wave function within GaN would be to push the centroid further into the GaN itself, providing the highly desired benefit of moving the electrons away from defects and other scattering centers at the substrate-dielectric interface, which can have deleterious effects on the mobility.

### *4.3 – Discussion of Results*

The analyses above present a rather complex picture which warrants summarization. Beginning with the physical structure, the primary differences between the theoretical device and what is observed experimentally are the compositional differences of the substrate and the deposited SiN

film. The substrate, from XPS data as well as unexpectedly degraded capacitance-voltage characteristics, is found not to be pure GaN but rather to have a thin region of semi-insulating $Ga_2O_3$ at the surface. This $Ga_2O_3$ layer is proposed to manifest itself as a series capacitance which is responsible for the degraded capacitance density displayed in the $n^{++}$ MISCAPs. The SiN film, through XPS data is found not to consist of pure SiN but rather a graded SiON film where regions closer to the surface are more highly oxidized. The relative capacitance density enhancement of the 5 nm MISCAPs suggests that this oxidized layer has a finite thickness, beyond which the film is closer to a pure SiN.

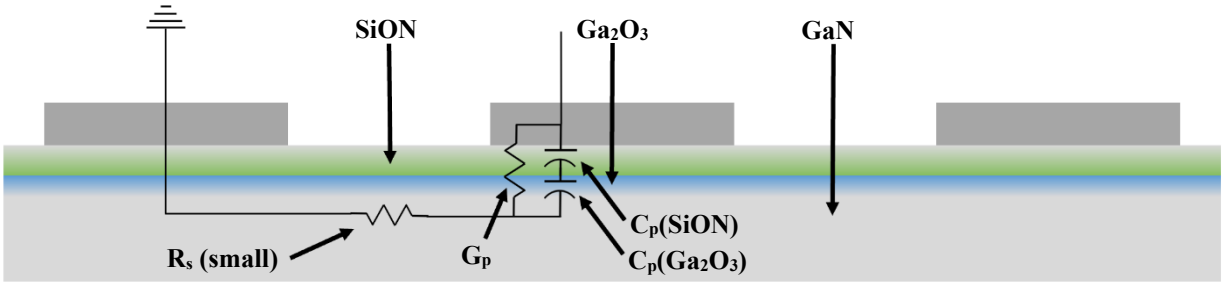


**Figure 4.21 –** Summary of GaN-SiON MISCAP structure including all experimentally supported features.

Considering the devices from a band theoretical perspective, the non-ideal device structure suggested by the experimental data can be used to paint a self-consistent picture of the band structure of the devices as well as explaining the current-voltage behaviour discussed earlier. Including a graded SiON (SiN to $SiO_2$[105]) film as well as a thin $Ga_2O_3$[106] layer at the GaN substrate surface results in the band diagram shown in Figure 4.22. As mentioned previously, surface band bending at the GaN/$Ga_2O_3$-SiON interface was suggested by XPS measurements. This band bending, in combination with interface states measured from conductance-frequency measurements (which can lead to Fermi level pinning) results in a smaller than theoretical Fowler-Nordheim tunneling barrier of around 1 eV. Dispersion in the ideality of Fowler-Nordheim tunneling behaviour between devices can be explained by considering the graded SiON band structure. It can be seen in Figure 4.22 that a SiON film which is purely SiN at the GaN/$Ga_2O_3$ surface and fully oxidized (pure $SiO_2$) at the exposed surface has a sloped conduction band even at flat band conditions. Since Fowler-Nordheim tunneling requires a triangular barrier, this conduction band offset would be the determining factor for what bias voltage is required to enter the Fowler-Nordheim regime and the ideality of the transition. Therefore, variations in the

oxidation profile of the SiON films would result in variations in the ideality of Fowler-Nordheim tunneling behaviour, ranging from highly ideal as seen in the 5 nm – 100 μm radius devices in Figure 4.5a, to non-ideal as seen in the devices of Figure 4.5b. Finally, it is worth noting that both deviation of the tunneling barrier height and dispersion of the tunneling ideality further hinge on the silicon content of the SiON film. It has been shown that excess silicon in SiN films can reduce the dielectric's bandgap to 2 eV and below[107]. The exact composition of the films is unknown, so the possibility of high silicon content in the films remains, both from during deposition as well as diffusion of silicon impurities out of the GaN substrate.

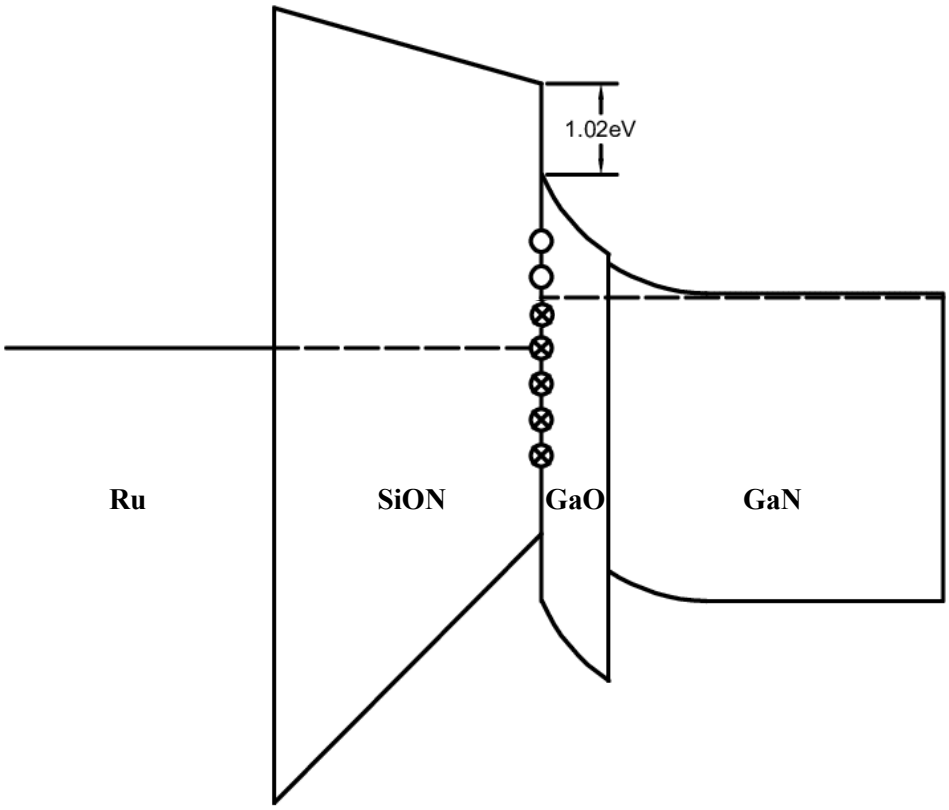


**Figure 4.22 –** Band diagram of GaN-SiON MISCAP including experimentally supported features under flat-band conditions.

Finally, it is worth discussing potential issues with the analyses presented throughout this chapter. Primarily at the root of these issues is the chosen architecture, where the SiON is deposited as a blanket layer on the substrate and various techniques (primarily high-voltage and fast-ramp voltage pulses) are used to "break" the dielectric between the outer contacts and the substrate. Ideally this dielectric breakdown is consistent and results in outer contacts that are effectively shorted to the

substrate. However, in practice this approach produces some inconsistencies which could have undesired effects on the final device measurements. Capacitance measurements between adjacent outer contacts (on $n^{++}$ devices where the resistance between the contacts is negligible) yielded capacitances one or two orders of magnitude below those measured at the center contact, and while the capacitance densities measured at the center contact had proper area dependence, it is unknown if the outer contacts could have influenced the measurements without running comparison experiments where the SiON is patterned. Attempts to pattern the SiON using buffered oxide etch (BOE) and lift-off processes have been unsuccessful, so points of comparison are currently unavailable. The second and more tangible issue with this architecture comes from the process of breaking the outer contacts. When using high voltages to break the contacts a trend was observed between devices depending on if the outer contact had the high (negative) voltage applied to it during the breaking process. As shown in Figure 4.23, when the voltage was applied to an outer contact during the breaking process, the measured capacitance was higher and the current-voltage behaviour is considerably more diode-like than the devices whose outer contacts acted as the ground during the breaking process. This suggests some asymmetry is created during the breaking process which has some effect on the device characteristics. Considering that during the breaking process the outer contacts act as back-to-back MISCAPs, the contact with the voltage applied to it would be reverse biased while the grounded contact would be forward biased. This means that the voltage would be developed across only the dielectric for the grounded contact while it would be applied across both the dielectric and the depletion region in the electrified contact. Therefore, it is possible that this method introduces some sort of further breakdown within the semiconductor itself surrounding the electrified contact, and further uncertainty to the measurements.

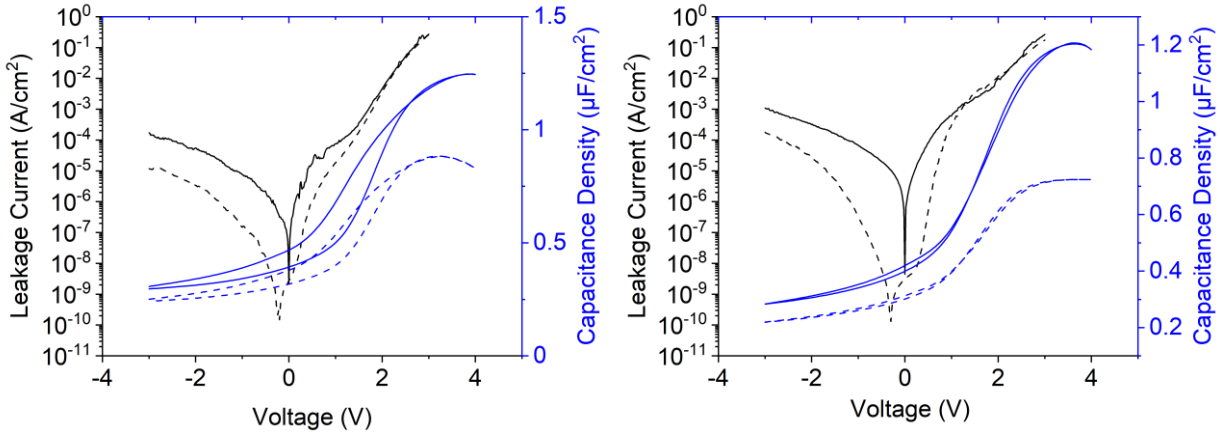


**Figure 4.23 –** Comparison of IV and CV curves for 3 nm SiON film 25 µm and 50 µm samples with differing contact preparation, solid lines correspond to samples where the breaking voltage was applied to the contact, dotted lines correspond to samples where the contact was grounded.

# 5 – GaN MISFETs with SiON Gate Dielectrics

## *5.0 – Device Fabrication*

The MISFETs were fabricated using the same processes as described in Chapter 4, where Ru was sputtered and SiON was deposited through atomic layer deposition. Patterning for the Ru layers was performed with standard liftoff techniques. Patterning of SiON proved challenging, due to the very low thickness of the film (~3 nm) attempts to wet etch with buffered oxide etch (BOE) resulted in rapid undercut, completely wiping the film even when only submerging for seconds at a time. Lift-off techniques, which have been used to pattern other difficult-to-etch dielectrics such as $HfO_2$ in the past[72,103] also proved unsuccessful. Although the exact reasons have not been investigated, the lack of any remaining SiON film on the wafer after liftoff suggests that the ALD SiON has poor adhesion to the GaN surface, so that when the lift-off step was performed the entire SiON film released along with the photoresist. Finally, plasma dry etching (RIE) was attempted, since the etch rate control and anisotropic nature of the process were predicted to help avoid over-etching and undercut issues from before. A low etch rate (~30 nm/min) recipe was developed on an Oxford NGP80 RIE with the help of Nanofab personnel and is described in Table 5I below.

**Table 5I –** Process parameters for slow SiON anisotropic etch.

| Parameter: | Value: |
|---|---|
| Chuck temperature | 10 ˚C |
| $O_2$ flow rate | 4 ccps |
| $SF_6$ flow rate | 0 ccps |
| $CHF_3$ flow rate | 25 ccps |
| $CF_4$ flow rate | 40 ccps |
| Pressure | 30 mTorr |
| RF Power | 50 W |

These deposition and patterning processes were applied as illustrated in Figure 5.1 to fabricate four-layer MISFETs in a circular configuration. As shown in Figure 5.2 this configuration consists of a center dot drain, an outer ring as the source, and a middle ring as the gate. For the experiments

in this chapter the design choice was made not to include any overlap between the source/drain and the gate to avoid any shorts induced by pinholing in the SiON film.

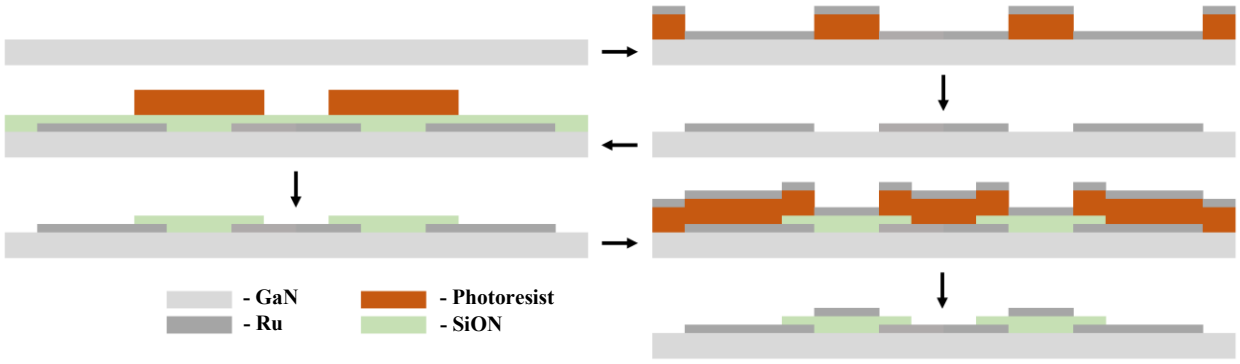


**Figure 5.1 –** Process flow for fabrication of GaN-SiON MISFETs.

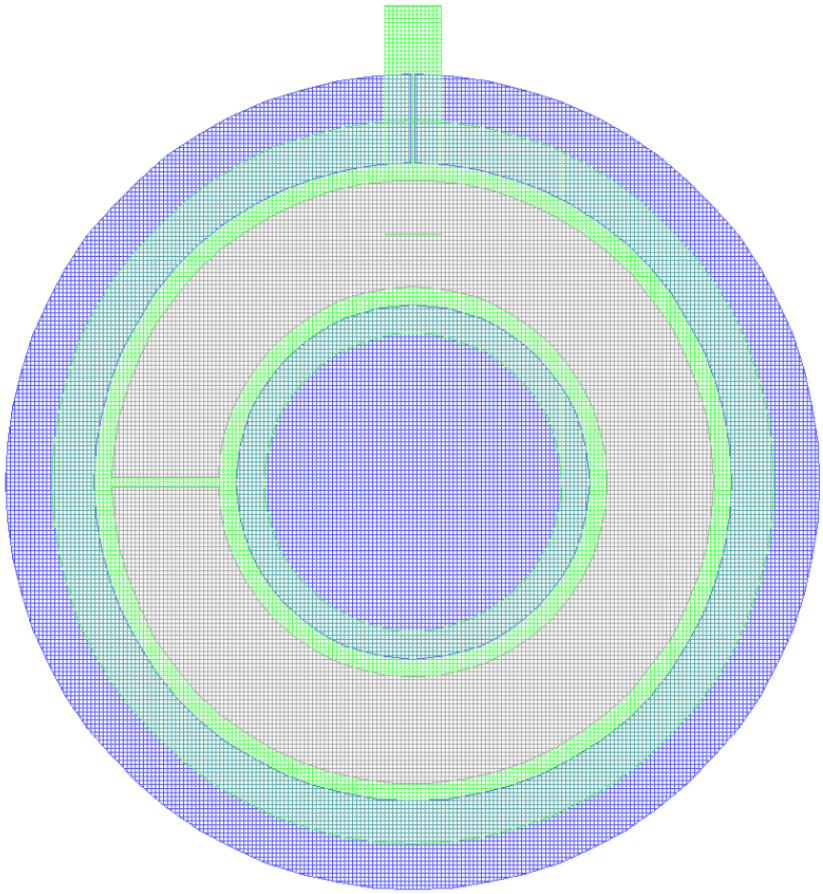

**Figure 5.2 –** Top down schematic of MISFET. The ruthenium source/drain is given in blue, the SiON film is given in green, and the ruthenium gate is given in grey.

### *5.1 – Mobility Analysis Theory*

Analysis of the fabricated MISFETs for mobility requires $I_{DS}$ vs. $V_{DS}$ data at given $V_{GS}$ values as well as CV data taken from the device gate at the same values of $V_{GS}$. The theory behind the analysis starts from the standard MISFET current equation in the linear regime given as:

$$I_{DS} = \mu_{FE} C_{ox} \frac{W}{L} \left( (V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

At low $V_{DS}$, $V_{DS}^2$ is negligible provided $(V_{GS} - V_t) \gg \frac{V_{DS}}{2}$, allowing this to be simplified, the capacitance and voltage in the equation are equivalent to the accumulation charge under the gate. By combining these and using the definition for the linear regime channel resistance ($R_{DS}$) we can come up with an expression relating the field effect mobility ($\mu_{FE}$) with the accumulation charge under the gate, the dimensions of the device, and the channel resistance.

$$I_{DS} = \mu_{FE} C_{ox} \frac{W}{L} (V_{GS} - V_t) V_{DS}$$

$$C_{ox}(V_{GS} - V_t) = Q_{ox}$$

$$\frac{1}{R_{DS}} = \frac{dI_{DS}}{dV_{DS}} = \mu_{FE} \frac{W}{L} Q_{ox}$$

It is also important to remember that the previous definition for the accumulation charge under the gate is an approximation which assumes the CV profile of the gate is a step function, that is there is no charge under the gate below the threshold voltage, which does not hold in reality. In order to account for the fact that $C_{ox}$ isn't a step function one candefine the charge more generally in its integral form and complete the expression for extracting mobility.

$$Q_{ox} = \int_{-\infty}^{V_{GS}} C_{ox} dV_{GS}$$

$$\mu_{FE} = \frac{1}{\left(\frac{W}{L}\right) R_{DS} \int_{-\infty}^{V_{GS}} C_{ox}\, dV_{GS}}$$

Where for a circular FET architecture the width-length ratio is given as:

$$\frac{W}{L} = \frac{2\pi}{\ln\left(\frac{R_{in}+L}{R_{in}}\right)}$$

### *5.2 – Mobility Analysis*

In order to make use of the theory outlined in the previous section, measurements of the family of curves ($I_{DS}$ vs. $V_{DS}$ at several $V_{GS}$ values), transfer curves ($I_{DS}$ vs. $V_{GS}$ at constant values of $V_{DS}$), and CV data were measured on a MISFET with inner contact radius of 25 µm and channel length of 70 µm. The family of curves shown in Figure 5.3a does not look like a typical set of curves due to the high doping of the substrate (measured as 2-5·$10^{16}$ $cm^{-3}$ from CV data), and in fact behaves more like a varistor. However, the resistance ($R_{DS}$) extracted from 5.3a and shown vs. $V_{GS}$ in Figure 5.3b is sufficient for the calculations necessary for mobility estimation. The linear reduction in resistance with $V_{GS}$ suggest a constant accumulation of carriers under the gate which is confirmed by the CV data further on.

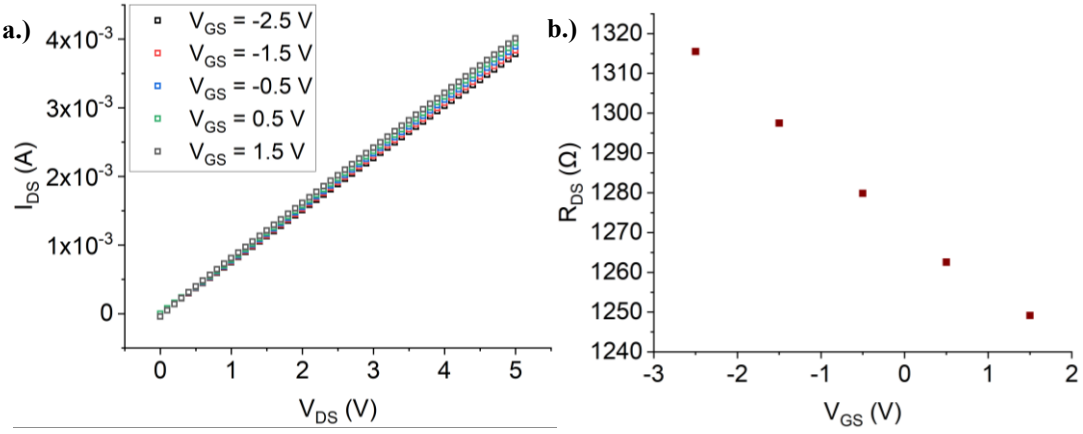


**Figure 5.3 –** Variable resistor behaviour of MISFET under varying gate voltages.

Due to the non-ideal nature of the devices, analysis of the CV and transfer curve data were required to determine where the devices behaved most like a standard transistor. In this context this refers to the amount of control the gate voltage has on the accumulation charge in the channel. In Figure 5.4 below, the gate capacitance and accumulation charge are plotted in comparison to the transfer curve of the device taken at $V_{DS}$ of 3 V. It can be seen that the gate dielectric in these devices is considerably leakier than the devices in Chapter 4, this was due to a growth problem which occurred during the ALD process, which interrupted the deposition and required two separate depositions to complete. This likely resulted in oxidation throughout the film which reduces the

film density and introduces a higher concentration of traps. As a result the gate behaves less like like a true capacitor and more like an MIS diode, where the capacitance drops off once the diode "switches on" which in this case occurs around 1.25 V. However since capacitance is the rate of change in accumulation charge with respect to voltage, charge continues to accumulate until the leakage current through the dielectric becomes significant enough for the capacitance to reach zero, which occurs at approximately 2.25 V. By comparing the accumulation charge profile to the transfer curve it is seen that the peak in accumulation charge coincides with the peak in channel current at this same voltage, confirming that the gate induced accumulation charge is controlling the channel current. It can be further observed that the beginning of the channel current peak is around 1.5 V, therefore it is assumed that in the $V_{GS}$ range from 1.5 V to 2.5 V the theory presented in the previous section holds.

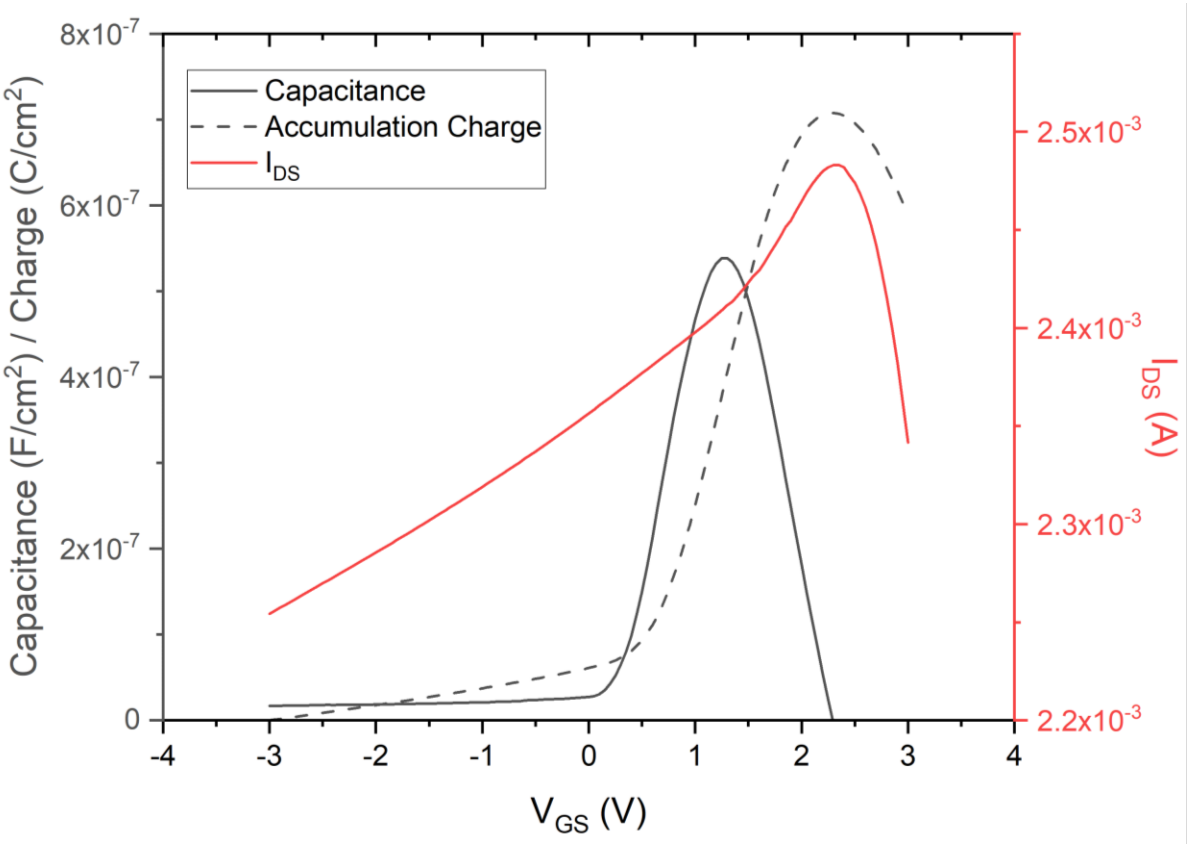


**Figure 5.4 –** Comparison of the gate capacitance, gate charge, and channel current vs. gate voltage.

Applying the arithmetic described earlier to the data collected, we obtain the results tabulated in Table 5II below.

**Table 5II –** Results of MISFET mobility analysis.

| Parameter: | Value: |
|---|---|
| $V_{DS}$ | 3.00 V |
| $V_{GS}$ | 1.50 V |
| $R_{DS}$ | 1.25 kΩ |
| W/L | 4.71 |
| $\int_{-\infty}^{V_{GS}} C_{ox}\, dV_{GS}$ | 509 C/cm$^2$ |
| $\mu_{FE}$ | 334 cm$^2$/Vs |

This value of mobility is of great interest because it is very close to the value extracted from MISCAPs using the transmission line model in Chapter 4, which resulted in an effective mobility of 325 cm$^2$/Vs at 2.5 V. The fact that both these methods have produced a similar result under comparable (but not equal) voltage conditions suggests that for interfaces between Kyma n$^+$ wafers and ALD SiON films the true electron mobility is likely within the 300-400 cm$^2$/Vs range. Comparing this with data from MISFETs fabricated on GaN in the last decade, we see that for enhancement mode devices it is rare to see mobilities over 200 cm$^2$/Vs (Table 5III) in GaN MISFETs fabricated with other gate dielectrics such as $SiO_2$ or $Al_2O_3$. That the minimum extracted mobilities from SiN devices are higher than those extracted in other materials systems is very encouraging for future research.

**Table 5III –** Comparison with literature mobility values.

| Dielectric Material [Reference] | Field Effect Mobility (cm$^2$/Vs) |
|---|---|
| $Al_2O_3$ [108] | 251 |
| $SiO_2$ [109] | 123 |
| $SiO_2$ [110] | 173 |
| $SiO_2$ [111] | 159 |
| $Al_2O_3$ [112] | 207 |
| $SiN_x$ (this work) | 334 |

# 6 – Conclusions and Future Work

## *6.0 – Conclusions*

In this research I set out to determine if ALD SiN could be used to form an interface with GaN that would allow for the fabrication of standard lateral GaN MISFETs with mobility high enough to compete with the current preferred architecture for high speed GaN transistors: the HEMT. The Ru-SiN-GaN materials system was investigated through fabrication of MISCAPs and MISFETs. In investigating the materials system, XPS data suggested that many of the oxygen bonds throughout the system were Ga-O bonds, therefore it was concluded that a thin layer of $Ga_2O_3$ was present at the surface of the GaN wafers used in the thesis. The XPS data also suggested oxidation of the SiN film during or after ALD deposition. The presence of $Ga_2O_3$ and oxidation of the SiN were incorporated into the capacitance model which was used to explain the trend in capacitance between the 3 nm and 5 nm dielectric films. In fitting this model to the capacitance data it was also concluded that high tunneling leakage in the 3 nm SiON films (evidenced by the coincidence of current densities in excess of 0.1 A/cm$^2$ with a visible "droop" in capacitance) resulted in a reduction of the measured capacitance, this "droop" was observed to be lowest in the 25 μm capacitors and so they were treated as most accurate. Applying a series capacitance model to this system suggested a $Ga_2O_3$ thickness of 6.1 Å and an oxidation fraction of 0.67 for the SiON films. The band structure of the Ru-SiN-GaN system was investigated using XPS depth profiling data as well as applying the Fowler-Nordheim model for tunneling through a triangular barrier. XPS data taken as the system was sputtered away was used to infer that band bending on the order of 1.8 eV at the SiN-GaN interface, Fowler-Nordheim analysis of the current-voltage data of the devices suggested a probable barrier height of around 0.953 V from GaN to SiN. Finally, and most importantly, the electron mobility under the dielectric layer was investigated using frequency dependent capacitance measurements as well as measurements from MISFETs. Using a transmission line model the mobility was extracted from the MISCAPs as 325 cm$^2$/Vs at a gate voltage of 2.5 V while a similar mobility of 334 cm$^2$/Vs was extracted from MISFET data. The similarity of these values suggests that the mobility of carriers at the SiN-GaN interface is at least in the 300 cm$^2$/Vs range, which suggests it could easily be a candidate for high speed lateral MISFETs fabricated on GaN.

## *6.1 – Future Work*

There are several avenues of further research that could be explored to continue developing the materials system covered in this thesis. The most pertinent of these for molding the SiN-GaN material system into a commercially viable transistor are as follows:

### *6.1.0 – Conversion of Highly Doped Wafers to Semi-Insulating GaN*

The substrates used in most experiments in this thesis were highly doped, with dopant concentrations typically in the $10^{17}$ $cm^{-3}$ or $10^{19}$ $cm^{-3}$ range depending on the producer of the substrate. This high background concentration of electrons increases the rate of electron scattering during transport under the gate, and prevents the system from achieving the highest mobilities possible. Additionally, the high concentration introduces very high off-state current for any transistors fabricated on such substrates. In order to maximize the potential of the materials system it should be replicated using semi-insulating substrates. These substrates will likely come with their own set of challenges however, the biggest of which comes in optimizing the metal-GaN contact.

### *6.1.1 – Optimization of Contacts to Semi-Insulating GaN*

In theory ruthenium forms a very strong Schottky barrier with semi-insulating GaN, with a theoretical Schottky barrier height of ~1.6 V (this is a small issue with highly doped GaN due to the very thin potential barrier formed between metals and highly doped semiconductors). Therefore, if a device is to be fabricated without considerable impact of the metal-semiconductor contact on performance, improvements must be made to the contact to reduce its rectifying nature. One of the more promising avenues of research in this area is the investigation of forming a metal-silicide at the metal-GaN interface. This investigation would involve deposition of a thin layer of silicon between the metal contact and GaN substrate, and subsequent high temperature annealing of the system to form a graded solid solution from metal to semiconductor. This experiment could be repeated with many different silicon thicknesses, annealing temperatures, and contact metals to determine the optimal contact on GaN for lateral MISFETs.

### *6.1.2 – Improvement of ALD SiN Films*

While the electronic performance of the ALD SiN films in this research was highly promising, it was seen throughout various tests that the current ALD process requires optimization. It has been noted that with the current recipe, the GPC of SiN inexplicably begins to reduce once the film reaches 3 nm, which caused difficulties during fabrication of thicker films in this research. This may also be related to the difficulty that has been found in forming reliable metal-insulator-metal structures with ALD SiN. Structures involving ALD SiN deposited both on flat metal surfaces as well as over metal step structures such as the edge of contacts have been found to consistently short out. The cause of these shorts have not yet been investigated, it is likely there is some amount of pinholing occurring as a result of the rough surfaces these films are being deposited on, as well as the low thickness of the films due to the GPC issue discussed earlier. A possible solution to this problem could also include using a dielectric stack of SiN and a high-κ dielectric, to achieve the good electronic interface of SiN-GaN while taking advantage of the more reliable high-κ insulators in order to avoid shorts between the MISFET contacts and the gate. However, long term it could also be beneficial to investigate the issues with the current SiN ALD recipe.

### *6.1.3 – Investigation of Role of $Ga_2O_3$ in GaN MIS Interfaces*

It has been tentatively concluded that a thin $Ga_2O_3$ layer at the GaN-SiN interface may play a role in the good characteristics observed throughout this thesis research. However, the exact role it plays is currently unclear and would benefit from further investigation. Numerical simulations of the SiN-$Ga_2O_3$-GaN system as well as experiments making use of thin ALD $Ga_2O_3$ layers or simple thermal oxidation of GaN could be beneficial for determining if $Ga_2O_3$ could play a role in pushing the spatial electron probability distribution away from the interface, and hence improving not just SiN-GaN, but any dielectric-GaN interface.

## References


1. Kish LB. End of Moore's law: thermal (noise) death of integration in micro and nano electronics. *Phys Lett A*. 2002;305(3):144-149. doi:https://doi.org/10.1016/S0375-9601(02)01365-8

2. Sproul AB, Green MA. Improved value for the silicon intrinsic carrier concentration from 275 to 375 K. *J Appl Phys*. 1991;70(2):846-854. doi:10.1063/1.349645

3. Baliga BJ. Semiconductors for high-voltage, vertical channel field-effect transistors. *J Appl Phys*. 1982;53(3):1759-1764. doi:10.1063/1.331646

4. Johnson E. Physical limitations on frequency and power parameters of transistors. In: *1958 IRE International Convention Record*. Vol 13. ; 1965:27-34. doi:10.1109/IRECON.1965.1147520

5. Baliga BJ. Power semiconductor device figure of merit for high-frequency applications. *IEEE Electron Device Lett*. 1989;10(10):455-457. doi:10.1109/55.43098

6. Shenai K. The Figure of Merit of a Semiconductor Power Electronics Switch. *IEEE Trans Electron Devices*. 2018;65(10):4216-4224. doi:10.1109/TED.2018.2866360

7. Keyes RW. Figure of merit for semiconductors for high-speed switches. *Proc IEEE*. 1972;60(2):225. doi:10.1109/PROC.1972.8593

8. Electronic archive New Semiconductor Materials. Characteristics and Properties. http://www.ioffe.ru/SVA/NSM/Semicond/. Accessed September 8, 2020.

9. Mnatsakanov TT, Levinshtein ME, Pomortseva LI, Yurkov SN. Carrier mobility model for simulation of SiC-based electronic devices. *Semicond Sci Technol*. 2002;17(9):974-977. doi:10.1088/0268-1242/17/9/313

10. Jacoboni C, Canali C, Ottaviani G, Alberigi Quaranta A. A review of some charge transport properties of silicon. *Solid State Electron*. 1977;20(2):77-89. doi:https://doi.org/10.1016/0038-1101(77)90054-5

11. Jacoboni C, Nava F, Canali C, Ottaviani G. Electron drift velocity and diffusivity in germanium. *Phys Rev B*. 1981;24(2):1014-1026. doi:10.1103/PhysRevB.24.1014

12. Crisler DF, Cupal JJ, Moore AR. Dielectric, piezoelectric, and electromechanical coupling constants of zinc oxide crystals. *Proc IEEE*. 1968;56(2):225-226. doi:10.1109/PROC.1968.6246

13. Kolník J, Oğuzman IH, Brennan KF, Wang R, Ruden PP, Wang Y. Electronic transport studies of bulk zincblende and wurtzite phases of GaN based on an ensemble Monte Carlo calculation including a full zone band structure . *J Appl Phys* . 1995;78(2):1033-1038. doi:10.1063/1.360405

14. Gaskill DK, Brandt CD, Nemanich RJ. *III-Nitride, SiC and Diamond Materials for Electronic Devices. Symposium Held April 8-12 1996, San Francisco, California, U.S.A. Volume 423.* Vol 423.; 1996. https://apps.dtic.mil/docs/citations/ADA319390.

15. Patrick L, Choyke WJ. Static Dielectric Constant of SiC. *Phys Rev B*. 1970;2(6):2255-2256. doi:10.1103/PhysRevB.2.2255

16. Srikant V, Clarke DR. On the optical band gap of zinc oxide. *J Appl Phys*. 1998;83(10):5447-5451. doi:10.1063/1.367375

17. Vassilevski K V, Zekentes K, Zorenko A V, Romanov LP. Experimental determination of electron drift velocity in 4H-SiC p/sup +/-n-n/sup +/ avalanche diodes. *IEEE Electron Device Lett*. 2000;21(10):485-487. doi:10.1109/55.870609

18. Shenai K, Scott RS, Baliga BJ. Optimum semiconductors for high-power electronics. *IEEE Trans Electron Devices*. 1989;36(9):1811-1823. doi:10.1109/16.34247

19. Silicon carbide power device market growing at 29% CAGR to $1.93bn in 2024, driven by EV market. Semiconductor Today. http://www.semiconductor-today.com/news_items/2019/jul/yole-190719.shtml. Published 2019. Accessed September 8, 2020.

20. Power Semiconductor Switches Market Growth 2020 to 2024: Analysed by Vendor Landscape, Regional Trends, Up Stream and Down Stream Fundamentals. MarketWatch. https://www.marketwatch.com/press-release/power-semiconductor-switches-market-growth-2020-to-2024-analysed-by-vendor-landscape-regional-trends-up-stream-and-down-stream-fundamentals-2020-07-15. Published 2020. Accessed September 8, 2020.

21. GaN RF Semiconductor Devices Market - Growth, Trends, and Forecast (2020 - 2025). Mordor Intelligence. https://www.mordorintelligence.com/industry-reports/gan-rf-semiconductor-devices-market. Published 2019. Accessed September 8, 2020.

22. The global RF semiconductor market size is expected to grow from USD 17.4 billion in 2020 to USD 26.2 billion by 2025, at a CAGR of 8.5%. PRNewswire. https://www.prnewswire.com/news-releases/the-global-rf-semiconductor-market-size-is-expected-to-grow-from-usd-17-4-billion-in-2020-to-usd-26-2-billion-by-2025--at-a-cagr-of-8-5-301022857.html. Published 2020. Accessed September 8, 2020.

23. *Transparency Market Research. Wide Bandgap Semiconductor Market.*; 2019. https://www.transparencymarketresearch.com/wide-band-gap-semiconductor-market.html.

24. Weimer AW. *Carbide, Nitride and Boride Materials Synthesis and Processing*. Chapman & Hall; 1997.

25. Litton CW, Reynolds DC, Collins TC. *Zinc Oxide Materials for Electronic and Optoelectronic Device Applications*.; 2011. doi:10.1002/9781119991038

26. Heilig ML. Henry H. C. Dunwoody. May 1906. doi:10.1145/178951.178972

27. Schubert F, Jong KK. Light-emitting diodes hit the centenary milestone. *Compd Semicond*. 2007;13(9):20-22.

28. Pierce GW. Crystal Rectifiers for Electric Currents and Electric Oscillations. Part I. Carborundum. *Phys Rev (Series I)*. 1907;25(1):31-60. doi:10.1103/PhysRevSeriesI.25.31

29. Pierce GW. Rectifier. 1909.

30. Baumhauer H. XII. Über die verschiedenen Modifikationen des Carborundums und die Erscheinung der Polytypie. *Zeitschrift für Krist - Cryst Mater*. 1915;55(1-6):249-259. doi:10.1524/zkri.1915.55.1.249

31. Parsons JB. The Preparation and Study of the Halides and a Nitride of Gallium. 1931. http://storage.lib.uchicago.edu/pres/2020/pres2020-0090.pdf.

32. Hahn H, Juza R. Untersuchungen über die Nitride von Cadmium, Gallium, Indium und Germanium. Metallamide und Metallnitride. VIII. Mitteilung. *Zeitschrift für Anorg und Allg Chemie*. 1940;244(2):111-124. doi:10.1002/zaac.19402440203

33. Juza R, Rabenau A. Das elektrische Leitvermögen einiger Metallnitride. *Zeitschrift für Anorg und Allg Chemie*. 1956;285(3-6):212-220. doi:10.1002/zaac.19562850314

34. Lagrenaudie J. Propriétés électroniques du nitrure d'aluminium. *J Chim Phys*. 1956;53:222-225. https://doi.org/10.1051/jcp/1956530222.

35. Kauer E, Rabenau A. Notizen: Über den Bandabstand von Galliumnitrid und Aluminiumnitrid. *Zeitschrift für Naturforsch A*. 1957;12(11):942-943. doi:10.1515/zna-1957-1112

36. Grimmeiss HG, Koelmans H. Über die Kantenemission und andere Emissionen des GaN. *Zeitschrift für Naturforsch A*. 1959;14(3):264-271. doi:10.1515/zna-1959-0309

37. Lorenz MR, Binkowski BB. Preparation, Stability, and Luminescence of Gallium Nitride. *J Electrochem Soc*. 1962;109(1):24. doi:10.1149/1.2425318

38. Perdok WG. Crystal data. Determinative tables edited by J. D. H. Donnay (General Editor). *Acta Crystallogr*. 1964;17(1):73. doi:10.1107/S0365110X6400024X

39. Jan Anthony Lely. Sublimation Process for Manufacturing Silicon Carbide Crystals. 1958.

40. Hall RN. Silicon Carbide Semiconductor Devices and Method of Preparation Thereof. 1959.

41. Lorant M. Silicon Carbide Transistor. *Wirel World*. 1962:7.

42. O'Connor JR. International Conference on Silicon Carbide Boston, Mass. *Phys Today*. 1959;12(11):14-17. doi:10.1063/1.3060563

43. Feng ZC. *Zinc Oxide and Materials*.; 2012.

44. Damen TC, Porto SPS, Tell B. Raman Effect in Zinc Oxide. *Phys Rev*. 1966;142(2):570-574. doi:10.1103/PhysRev.142.570

45. Thomas DG. The exciton spectrum of zinc oxide. *J Phys Chem Solids*. 1960;15(1):86-96. doi:https://doi.org/10.1016/0022-3697(60)90104-9

46. Holonyak N, Bevacqua SF. COHERENT (VISIBLE) LIGHT EMISSION FROM Ga(As1−xPx) JUNCTIONS. *Appl Phys Lett*. 1962;1(4):82-83. doi:10.1063/1.1753706

47. Drapak IT. Visible luminescence of a ZnO-Cu2O heterojunction. *Sov Phys Semicond*. 1968;2(4):513.

48. Maruska HP, Rhines WC. A modern perspective on the history of semiconductor nitride blue light sources. *Solid State Electron*. 2015;111:32-41. doi:https://doi.org/10.1016/j.sse.2015.04.010

49. Chi H, Robert, Chang, Crull ML. Silicon Carbide Solid State Ultraviolet Radiation Detector. 1970.

50. Campbell RB. Whatever Happened to Silicon Carbide. *IEEE Trans Ind Electron*. 1982;IE-29(2):124-128. doi:10.1109/TIE.1982.356648

51. K. Shibahara , T. Saito, S. Nishino and HM. No Title. In: *Extended Abstracts of the Eighteenth International Conference on Solid State Device and Materials*. ; 1986:717-718.

52. Kondo Y, Takahashi T, Ishii K, et al. High-Temperature Operation of Silicon Carbide MOSFET. *Jpn J Appl Phys*. 1987;26(Part 1, No. 2):310-311. doi:10.1143/jjap.26.310

53. Dmitriev VA, Ivanov PA, D N, Syrkin AL, Tsarenkov B V. High-temperature SiC-6H field-effect transistor with p-n gate. *Sov Tech Phys Lett*. 1988;14(April):127-128.

54. Feigelson RS. *50 Years Progress in Crystal Growth : A Reprint Collection*. Amsterdam, the Netherlands: Elsevier Science; 2004. https://login.ezproxy.library.ualberta.ca/login?url=https://search.ebscohost.com/login.aspx?direct=true&db=e000xna&AN=195055&site=ehost-live&scope=site.

55. Asif Khan M, Kuznia JN, Bhattarai AR, Olson DT. Metal semiconductor field effect transistor based on single crystal GaN. *Appl Phys Lett*. 1993;62(15):1786-1787. doi:10.1063/1.109549

56. Asif Khan M, Bhattarai A, Kuznia JN, Olson DT. High electron mobility transistor based on a GaN-AlxGa1−xN heterojunction. *Appl Phys Lett*. 1993;63(9):1214-1215. doi:10.1063/1.109775

57. Khan, M. A.;VanHove, James M.; Kuznia, Jon N.; Olson DT. High Electron Mobility Transistor. 1993.

58. Weitzel CE, Palmour JW, Carter CH, Nordquist KJ. 4H-SiC MESFET with 2.8 W/mm power density at 1.8 GHz. *IEEE Electron Device Lett*. 1994;15(10):406-408. doi:10.1109/55.320983

59. Baliga, Bantval J., Bhatnagar M. Silicon Carbide Field Effect Transistor. 1994.

60. Binari SC, Ren F, Buckley DN, et al. GaN FETs for high-temperature and microwave applications. *Proc Electrochem Soc*. 1995;95:21.

61. Zolper, John C.; Shul RJ. Gallium Nitride Junction Field Effect Transistor. 1999.

62. Ohya Y, Niwa T, Ban T, Takahashi Y. Thin Film Transistor of ZnO Fabricated by Chemical Solution Deposition. *Jpn J Appl Phys*. 2001;40(Part 1, No. 1):297-298. doi:10.1143/jjap.40.297

63. Chang K-C, Porter LM, Bentley J, Lu C-Y, Cooper J. Electrical, structural, and chemical analysis of silicon carbide-based metal-oxide-semiconductor field-effect-transistors. *J Appl Phys*. 2004;95(12):8252-8257. doi:10.1063/1.1737801

64. Stephani D, Friedrichs P. Silicon Carbide Junction Field Effect Transistors. *Int J High Speed Electron Syst*. 2006;16(03):825-854. doi:10.1142/S012915640600403X

65. Ranbir Singh; Anant K. AS-HR. Self-aligned Bipolar Junction Silicon Carbide Transistors. 2001.

66. Silicon Carbide (SiC) vs. Gallium Nitride (GaN). *Arrow*. 2020. https://www.arrow.com/en/research-and-events/articles/silicon-carbide-and-gallium-nitride-compared.

67. Mokhov EN, Wolfson AA. 12 - Growth of AlN and GaN crystals by sublimation. In: Fornari RBT-SC of EM, ed. *Woodhead Publishing Series in Electronic and Optical Materials*. Woodhead Publishing; 2019:401-445. doi:https://doi.org/10.1016/B978-0-08-102096-8.00012-4

68. Chen HC, Chen MJ, Liu TC, Yang JR, Shiojiri M. Structure and stimulated emission of a high-quality zinc oxide epilayer grown by atomic layer deposition on the sapphire substrate. *Thin Solid Films*. 2010;519(1):536-540. doi:https://doi.org/10.1016/j.tsf.2010.07.069

69. Anderson TJ, Feigelson BN, Kub FJ, et al. Activation of Mg implanted in GaN by multicycle rapid thermal annealing. *Electron Lett*. 2014;50(3):197-198. doi:10.1049/el.2013.3214

70. Balakrishnan L, Gowrishankar S, Premchander P, Gopalakrishnan N. Dual codoping for the fabrication of low resistive p-ZnO. *J Alloys Compd*. 2012;512(1):235-240. doi:https://doi.org/10.1016/j.jallcom.2011.09.072

71. Hashizume T, Kaneki S, Oyobiki T, Ando Y, Sasaki S, Nishiguchi K. Effects of postmetallization annealing on interface properties of Al2O3/GaN structures. *Appl Phys Express*. 2018;11(12):124102. doi:10.7567/apex.11.124102

72. Hauff P Von. Metal Oxide Processing on Gallium Nitride and Silicon. 2012. doi:10.1227/00006123-197907010-00116

73. Nandi SK. Origin of Hysteresis in Zinc Oxide Based Metal Oxide Semiconductor Films. *Int J Eng Sci Math*. 2018;7(4):17-27.

74. Selvaraj SL, Watanabe A, Egawa T. Enhanced mobility for MOCVD grown AlGaN/GaN HEMTs on Si substrate. In: *69th Device Research Conference*. ; 2011:221-222. doi:10.1109/DRC.2011.5994507

75. Bothe KM, Hauff PA von, Afshar A, Foroughi-Abari A, Cadien KC, Barlage DW. Electrical Comparison of $HfO_2$ and $ZrO_2$ Gate Dielectrics on GaN. *IEEE Trans Electron Devices*. 2013;60(12):4119-4124. doi:10.1109/TED.2013.2283802

76. Feng ZC, ed. *Handbook of Zinc Oxide and Related Materials*. CRC Press; 2012. doi:10.1201/b13072

77. Bayraktaroglu B, Leedy K, Neidhard R. Microwave ZnO Thin-Film Transistors. *IEEE Electron Device Lett*. 2008;29(9):1024-1026. doi:10.1109/LED.2008.2001635

78. Shoute G, Afshar A, Muneshwar T, Cadien K, Barlage D. Sustained hole inversion layer in a wide-bandgap metal-oxide semiconductor with enhanced tunnel current. *Nat Commun*. 2016;7(1):10632. doi:10.1038/ncomms10632

79. Tang Y, Shinohara K, Regan D, et al. Ultrahigh-Speed GaN High-Electron-Mobility Transistors With $f_{T}/f_{\mathrm {max}}$ of 454/444 GHz. *IEEE Electron Device Lett*. 2015;36(6):549-551. doi:10.1109/LED.2015.2421311

80. Bayraktaroglu B, Leedy K, Neidhard R. High-Frequency ZnO Thin-Film Transistors on Si Substrates. *IEEE Electron Device Lett*. 2009;30(9):946-948. doi:10.1109/LED.2009.2025672

81. Rowena IB, Selvaraj SL, Egawa T. Buffer Thickness Contribution to Suppress Vertical Leakage Current With High Breakdown Field (2.3 MV/cm) for GaN on Si. *IEEE Electron Device Lett*. 2011;32(11):1534-1536. doi:10.1109/LED.2011.2166052

82. Benlamri M, Wiltshire BD, Zhang Y, Mahdi N, Shankar K, Barlage DW. High Breakdown Strength Schottky Diodes Made from Electrodeposited ZnO for Power Electronics Applications. *ACS Appl Electron Mater*. 2019;1(1):13-17. doi:10.1021/acsaelm.8b00053

83. Lannoo M. Theoretical Calculations of the Electronic Structure in the Si-$SiO_2$ Systems BT - The Physics and Chemistry of $SiO_2$ and the Si-$SiO_2$ Interface. In: Helms CR, Deal BE, eds. Boston, MA: Springer US; 1988:259-269. doi:10.1007/978-1-4899-0774-5_29

84. Carim AH, Bhattacharyya A. Si/$SiO_2$ interface roughness: Structural observations and electrical consequences. *Appl Phys Lett*. 1985;46(9):872-874. doi:10.1063/1.95870

85. Lopes MC V, dos Santos Fo. SG, Hasenack CM, Baranauskas V. Si - SiO2 Electronic Interface Roughness as a Consequence of Si - $SiO_2$ Topographic Interface Roughness. *J Electrochem Soc*. 1996;143(3):1021-1025. doi:10.1149/1.1836575

86. Nahar RK, Singh V, Sharma A. Study of electrical and microstructure properties of high dielectric hafnium oxide thin film for MOS devices. *J Mater Sci Mater Electron*. 2007;18(6):615-619. doi:10.1007/s10854-006-9111-6

87. Tsai S-J, Wang C-L, Lee H-C, et al. Approaching Defect-free Amorphous Silicon Nitride by Plasma-assisted Atomic Beam Deposition for High Performance Gate Dielectric. *Sci Rep*. 2016;6(1):28326. doi:10.1038/srep28326

88. Dong Y, Feenstra RM, Northrup JE. Electronic states of oxidized GaN(0001) surfaces. *Appl Phys Lett*. 2006;89(17):171920. doi:10.1063/1.2370519

89. Lieberman MA, Gottscho RA. *Design of High-Density Plasma Sources for Materials Processing*. Vol 18. ACADEMIC PRESS, INC.; 1994. doi:10.1016/b978-0-08-092513-4.50006-4

90. J. A. Woolam. Ellipsometry.

91. Zhao Y, Gao H, Huang R, et al. Precise determination of surface band bending in Ga-polar n-GaN films by angular dependent X-Ray photoemission spectroscopy. *Sci Rep*. 2019;9(1):1-7. doi:10.1038/s41598-019-53236-9

92. *University of Alberta Nanofab - Piranha Cleaning SOP*.; 2009.

93. Muneshwar T, Cadien K. Resolving self-limiting growth in silicon nitride plasma enhanced atomic layer deposition with tris-dimethylamino silane precursor. *J Vac Sci Technol A*. 2020;38(6):62406. doi:10.1116/6.0000493

94. Huang L, Feng Q, Han G, et al. Comparison Study of β-$Ga_2O_3$ Photodetectors Grown on Sapphire at Different Oxygen Pressures. *IEEE Photonics J*. 2017;9(4):1-8. doi:10.1109/JPHOT.2017.2731625

95. Bothe KM, Barlage DW. Underlying design advantages for GaN MOSFETs compared with GaN HFETs for power applications. *J Comput Electron*. 2014;13(1):217-223. doi:10.1007/s10825-013-0502-7

96. Muraoka K, Kurihara K, Yasuda N, Satake H. Optimum structure of deposited ultrathin silicon oxynitride film to minimize leakage current. *J Appl Phys*. 2003;94(3):2038-2045. doi:10.1063/1.1588354

97. Barlage DW, O'Keeffe JT, Kavalieros JT, Nguyen MM, Chau RS. Inversion MOS Capacitance Extraction for High-Leakage Dielectrics Using a Transmission Line Equivalent Circuit. *IEEE Electron Device Lett*. 2000;21(9):454-456. doi:10.1109/55.863109

98. Schroder DK. *Semiconductor Material and Device Characterization Third Edition*. 3rd ed. John Wiley & Sons, Inc.; 1990.

99. Paskaleva A, Spassov D, Terziyska P. Electric, dielectric and optical properties of $Ga_2O_3$ grown by metal organic chemical vapour deposition. *J Phys Conf Ser*. 2017;794:12017. doi:10.1088/1742-6596/794/1/012017

100. Sharma R, Law ME, Fares C, et al. The role of annealing ambient on diffusion of implanted Si in β-$Ga_2O_3$. *AIP Adv*. 2019;9(8):85111. doi:10.1063/1.5115149

101. Jakiela R, Barcz A, Dumiszewska E, Jagoda A. Si diffusion in epitaxial GaN. *Phys status solidi c*. 2006;3(6):1416-1419. doi:https://doi.org/10.1002/pssc.200565112

102. Götz W, Johnson NM, Chen C, Liu H, Kuo C, Imler W. Activation energies of Si donors in GaN. *Appl Phys Lett*. 1996;68(22):3144-3146. doi:10.1063/1.115805

103. Bothe KM. Enhancement-mode Polar Sourced Gallium Nitride MOSFET. 2015.

104. Peelaers H, Van de Walle CG. Sub-band-gap absorption in $Ga_2O_3$. *Appl Phys Lett*. 2017;111(18):182104. doi:10.1063/1.5001323

105. Ballarotto VW, Breban M, Siegrist K, Phaneuf RJ, Williams ED. Photoelectron emission microscopy of ultrathin oxide covered devices. *J Vac Sci Technol B Microelectron Nanom Struct Process Meas Phenom*. 2002;20(6):2514-2518. doi:10.1116/1.1525007

106. Huan Y-W, Sun S-M, Gu C-J, et al. Recent Advances in β-Ga2O3–Metal Contacts. *Nanoscale Res Lett*. 2018;13(1):246. doi:10.1186/s11671-018-2667-2

107. Cheng Q, Xu S, Ostrikov K (Ken). Controlled-bandgap silicon nitride nanomaterials: deterministic nitrogenation in high-density plasmas. *J Mater Chem*. 2010;20(28):5853-5859. doi:10.1039/C0JM01060J

108. Wang Y, Wang M, Xie B, et al. High-Performance Normally-Off $Al_2O_3$-GaN MOSFET Using a Wet Etching-Based Gate Recess Technique. *IEEE Electron Device Lett*. 2013;34(11):1370-1372. doi:10.1109/LED.2013.2279844

109. Takashima S, Ueno K, Matsuyama H, et al. Control of the inversion-channel MOS properties by Mg doping in homoepitaxial p-GaN layers. *Appl Phys Express*. 2017;10(12):121004. doi:10.7567/apex.10.121004

110. Tanaka R, Takashima S, Ueno K, Matsuyama H, Edo M, Nakagawa K. Mg implantation dose dependence of MOS channel characteristics in GaN double-implanted MOSFETs. *Appl Phys Express*. 2019;12(5):54001. doi:10.7567/1882-0786/ab0c2c

111. Tanaka R, Takashima S, Ueno K, Matsuyama H, Edo M. Demonstration of 1200 V/1.4 mΩ cm2 vertical GaN planar MOSFET fabricated by an all ion implantation process. *Jpn J Appl Phys*. 2020;59(SG):SGGD02. doi:10.7567/1347-4065/ab6347

112. Ando Y, Nagamatsu K, Deki M, et al. Electrical properties of GaN metal-insulator-semiconductor field-effect transistors with $Al_2O_3$/GaN interfaces formed on vicinal Ga-polar and nonpolar surfaces. *Appl Phys Lett*. 2020;117(24):242104. doi:10.1063/5.0028516

## Appendix A: JV Data

Raw current density vs. voltage plots for various devices with 3 nm and 5 nm SiON films are shown in Figure A.1 below. The JV characteristics take three distinct forms: devices such as the 25 µm and 50 µm 3 nm film devices seen at the top of Figure A.1 show almost pure diode behaviour centered around 0 V, the remainder of the 3 nm film devices found in the middle show a mix of diode and insulator behaviour with a short plateau in current before returning to diode-like gain, the 5 nm devices seen at the bottom behave solely as insulators with a long plateau in current before Fowler-Nordheim tunneling takes over around 1 V. The 5 nm film devices showed the most standard F-N plots of all devices, suggesting that they demonstrated the simplest energy barrier structure and likely the most consistent film composition of all the devices.

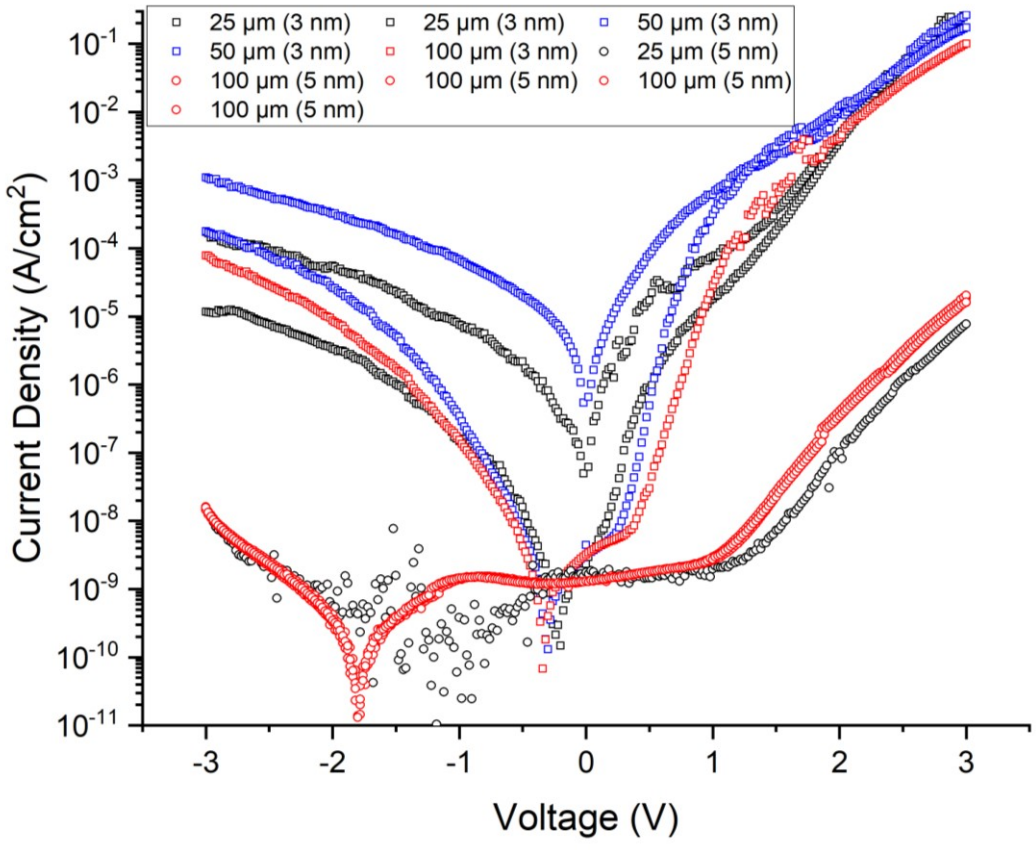


**Figure A.1 –** JV curves used to generate Fowler-Nordheim plots in Figure 4.5a.

## Appendix B: CV Data and Comparison of Leakage Current

As described in Chapter 4, the CV characteristics of the 3 nm film MISCAPs fell into two categories, the devices with high tunneling leakage current saw a noticeable "droop" in their peak capacitance.

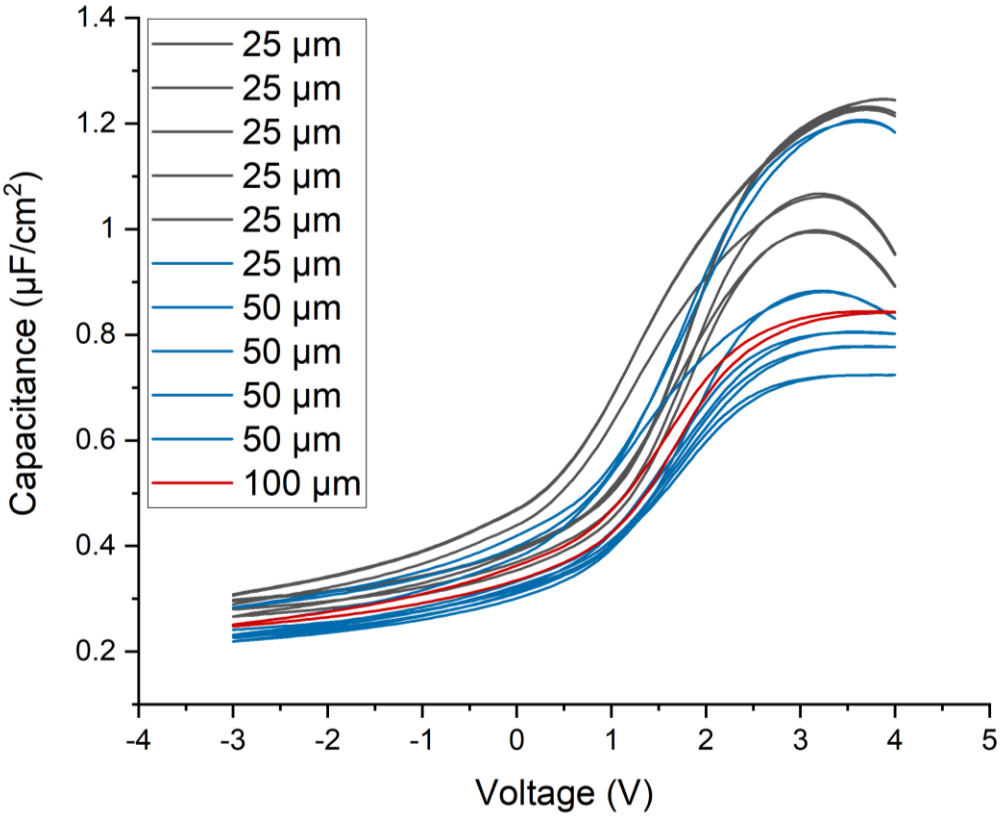


**Figure B.1 –** Demonstration of higher droop likelihood with increasing capacitor size.

It was noted that as the size of the capacitor increased, this tendency of the capacitance to "droop" increased. This increased tendency is clearly visible in Figure B.1 above, where all but two of the 25 µm devices show little to no droop, and all but one of the 50 µm devices demonstrate droop. Based on these observations it was decided to use the devices with the least droop as representatives of the true capacitance density of the 3 nm SiON films.