Microstructure-based Direct Digital Capacitive Pressure Sensor

By

Carson R. Dick

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Department of Electrical and Computer Engineering

University of Alberta

Abstract

Pressure sensors are important in many applications, from medical hyperbaric oxygen chambers to precision pressure monitoring in vacuum setups of semiconductor manufacturing. With their simple design and high precision, capacitive pressure sensors are one of the best designs of pressure sensors. In this thesis, we proposed a new class of microstructure-based direct digital capacitive pressure sensor, including the microstructured pressure-to-capacitance transducer and its capacitance-to-frequency digital conversion circuitry. The microstructured transducer design provides ease of fabrication and long-term durability. The novel sensor circuit using digital phase-locked-loop (PLL) enables highly sensitive detection of capacitance. For proof of concept, we fabricated the microstructured transducer and constructed the digital PLL using discrete parts. The experimental results and analysis show the viability of implementing such sensors in the future.

Preface

This thesis is submitted for the degree of the Master of Science at University of Alberta. This thesis contains results of the research undertaken in the Department of Electrical and Computer Engineering, University of Alberta, from January 2018 to August 2020, under the supervision of Professor Xihua Wang and Professor Masum Hossain. The results and discussion in chapter 2 and 3 of this thesis will be used in the preparation of a journal publication.

Acknowledgments

I would like to express my sincere gratitude to my supervisors Dr. Xihua Wang and Dr. Masum Hossain, for all their help with both my research and the creation of this document. Their help was invaluable and taught me more about circuits and electrical engineering than I could ever do on my own. I am also thankful to the members of the lab Shovon Dey, Aurangozeb, Lingju Meng and countless graduate peers who helped me in my studies and research. The support from family and friends was invaluable, as was that of the University of Alberta faculty and staff.

Finally, this is also dedicated to Kevin P. May you rest in peace.

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1.1 Overview of capacitive pressure sensors

1.1.1 Introduction to pressure sensors

As the consumer market for electronics continues to grow, so does the market for sensors. [*1, 2*]. With more devices being interconnected than ever before and with the rise of the Internet-of-Things (IoT), the use of devices to sense the environment has become both commonplace and necessary.

One class of common sensors is the pressure sensor. Pressure is defined as the ratio between a force and the area which it is applied over, and the unit of pressure is N/m^2. The ability to detect pressure can be useful in many ways, from sensing the pressure applied to a touchscreen to sensing the ambient air pressure for weather monitoring. Pressure sensors can be found in almost all areas of life, such as clinics, cars, flights, ships, industry, and consumer markets. Fundamentally, most pressure sensors work on the mechanism that the applied pressure will either deform or displace a functional material inside the sensor, and different types of pressure sensors are designed to utilize this mechanism in different ways.

When subject to a pressure, all materials deform, some more than others. The percentage of deformation in a material relative to its original geometry before the pressure is applied is known as the strain. More formally, strain can be defined as:

$$\varepsilon = \frac{l - L}{L} \quad (1.1)$$

Where ε is the strain value (unitless), L is the original length along one axis of the material, and l is the final length. Fundamentally it can be viewed as a percentage change in one axis of a material. Utilizing this property, several types of sensors can be constructed for the purpose of measuring pressure, either by

changing the electrical properties of a sensing material in response to strain, or the physical geometrical displacement of the sensor material.

1.1.2 Types of pressure sensors

Pressure sensors come in many forms, using various transduction methods such as strain-induced resistance change [*3*], piezoresistive [*4*], piezoelectric [*5*], and capacitive [*6*] techniques.

Strain-induced resistance change pressure sensors are constructed by forming metal-based resistors on a non-conducting substrate. When the substrate is stretched or deformed due to an applied pressure, the patterned metal resistor will have the same strain as the substrate, and its resistance will change due to its changed geometry (strain). This change in resistance is measured using circuitry to determine the amount of strain, then the strain can be used to calculate the applied pressure considering the mechanical property of the substrate. This type of pressure sensors is also called the strain gauge. The working principle of the strain gauge relies on the common definition of resistance *R*:

$$R = \frac{\rho L}{A} (1.2)$$

Where ρ is the resistivity, *L* is the length, and *A* is the cross-sectional area of the pattern metal. The strain in the patterned metal resistor will cause its length to increase and the cross-sectional area to decrease due to stretching, similar to stretching an elastic band.

For piezoresistive pressure sensors, a special semiconductor (piezoresistive) material is used instead of metal. The sensitivity in piezoresistive pressure sensor tends to be greater than metal due to the larger change in its resistance being caused by changing semiconductor properties in response to pressure.

For piezoelectric pressure sensors, a voltage is produced in the piezoelectric material, another class of semiconductors, in response to strain using the piezoelectric effect. The piezoelectric effect refers

to electric field changes inside the sensing material in response to generated strain by applied pressure [*7*]. This piezoelectric property can be useful as energy is produced from the deformation itself versus being supplied externally, thus the piezoelectric properties of some semiconductors are consistent over many environmental conditions which makes for robust sensors [*5*].

1.1.3 Capacitive pressure sensors

Unlike the previously discussed pressure sensors, the capacitive sensor does not utilize a change in resistance of the sensing material. Instead, as their name implies, capacitive sensors use a change in capacitance (*C*) to measure pressure. And the capacitance is defined as the amount of charge (*Q*) stored in a device in response to a change in applied voltage (*V*).

While there are many configurations for capacitive sensors, the most common design of capacitive pressure sensors consists of two conductive plates that act as electrical terminals separated by a flexible dielectric or airgap. The capacitance for a two-parallel-plate capacitor can be written as:

$$C = \frac{\varepsilon A}{D} \quad (1.3)$$

Where *A* is the area of overlap between the two plates,

D is the distance between them,

ε is the permittivity between the two plates.

If the distance *D* between the two plates is changed or the area of overlap between the two plates is changed, a change in capacitance will be observed. Thus, we can link position of the two plates to the value of capacitance. If this displacement is caused by pressure, we can relate the capacitance value directly to pressure, and form a capacitive pressure sensor. This concept is illustrated in Figure 1.1.

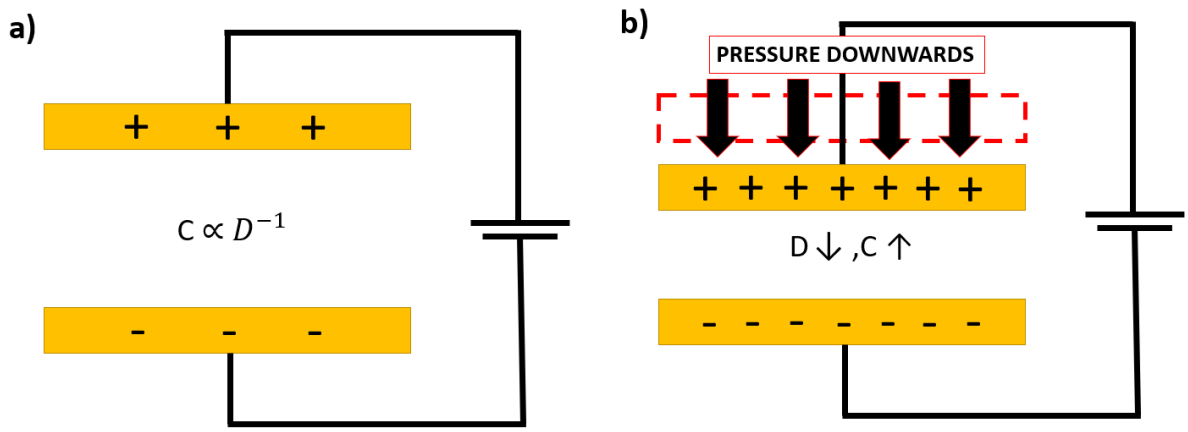

Figure 1.1: Illustration showing the working principle behind capacitive pressure sensors. in a) a cut-away side view of a double plate capacitor with distance D between the plates is shown, with positive and negative charge on both plates, which is supplied by an external voltage source. b) when pressure is applied to the top-plate, the decreasing distance D between them causes an increase in charge stored due to an increase in capacitance.

There are several advantages to capacitive pressure sensors that make them ideal candidates for precision pressure sensing. First, the design is relatively simple, and the sensor can be constructed using standard silicon etching techniques[*8*]. Second, as the conductive plates do not have to be strained or stretched but only have their position change relative to one another, the sensor can be made more rugged and last longer. Finally, the capacitive sensor can be made small and with low mass while retaining its sensitivity [*9*].

Capacitive pressure sensors have lots of applications in industry and academia [*10-13*]. For example, they are used in flexible sensors for tactile response for bio-medical devices and touch screens. They are also used for more static applications such as pressure detection in aerospace airfoils [*14*].

Another famous application of capacitive pressure sensors is the precision positioning sensors used in photolithography machines that have to be nanometer accurate [*15*]. Without the use of capacitive sensors in lithography machines, the mask alignment necessary to construct modern chips is not feasible. In disc-drive technology, hardware discs require tight requirements due to their data density and high-

speed operation, capacitive sensors are required to detect the runout of a disc, which is the amount of angular deviation the platter spins as compared to an ideal perfect platter [*16*].

1.2 Circuitry of capacitive sensors

Sensor circuitry is very important for sensor-connected full electronic systems, and it converts the detected electrical signals from the sensor to digital codes for further processing in computers and instruments. Typical capacitive sensor circuits are designed to convert capacitance to voltage for read-out. Then the analog value of voltage is converted to the digital code using an analog-to-digital converter (ADC) for further processing. This type of circuits is called the voltage domain circuitry.

For a capacitor, the charge-current-voltage relation is:

$$C * V = \int_0^t i(t)\, dt \quad (1.4)$$

Where *C* is the capacitance value,

V is the voltage between both terminals of the capacitor,

i(t) is the instantaneous current,

t is the integration time.

As the integral of current over time for a capacitor is equivalent to the amount of charge stored on the capacitor, equation (1.4) can be simplified to:

$$C * V = Q \quad (1.5)$$

Combining equation (1.4) and (1.5) with charge conservation tells us several things. First, it shows that if one knows the voltage *V* and the charge *Q* in a capacitor, one can determine the capacitance value *C* of the sensor capacitor. Second, if the capacitance value *C* changes, we will either see a change in voltage *V*

if charge *Q* is held constant, or we will see a change in charge *Q* if voltage *V* is held constant. From this, one can measure a change in capacitance of a capacitive sensor capacitor by measuring the resulting change in charge Q or voltage V of the capacitor.

Although voltage domain circuitry has been used broadly for capacitive sensors, its sensitivity is limited by the resolution of ADC to read the analog voltage. In recent years, researchers proposed to convert capacitance to frequency of the resonant circuit, and the ADC can provide better sensitivity to deal with the frequency. This type of circuits is called the time/frequency domain circuitry. These time/frequency domain circuits can only contain passive elements, such as inductors and capacitors, without loss compensation. They can also include resistors with loss compensation using active elements. For the latter case, circuits can be either open loop or closed loop. The closed loop active time/frequency domain circuits provide best performance among all types of circuits and they are the focus of my thesis work. The details of time/frequency domain circuitry and comparison of different types of time/frequency domain circuits will be discussed in Chapter 3. In this section, I will show the development and limitations of the voltage domain circuitry.

1.2.1 Current-to-voltage digital conversion techniques

The first type of voltage domain circuitry is developed using current-to-voltage digital conversion. As shown in reference [*17*], a simple method of converting capacitance to voltage is achieved by injecting a fixed amount of current over a specified period and measure the resulting voltage, otherwise known as a Current-to-Voltage capacitance-to-digital technique. If, for example, 1 mA of current is injected into a sensor capacitor with the value of 1 nF over a period of 1µs, the resulting voltage will be 1 V.

Using this principle, one could measure the value of a capacitive sensor C_{sens} by injecting a fixed amount of current I_{Sens} over a fixed time interval and converting the produced voltage V_{sens} to a digital value by measuring it with an ADC. Thus, capacitance can be converted to voltage using current, and this

voltage is converted into a digital value, digitizing the capacitance of the capacitive sensor. A simple implementation can be illustrated in Figure 1.2.

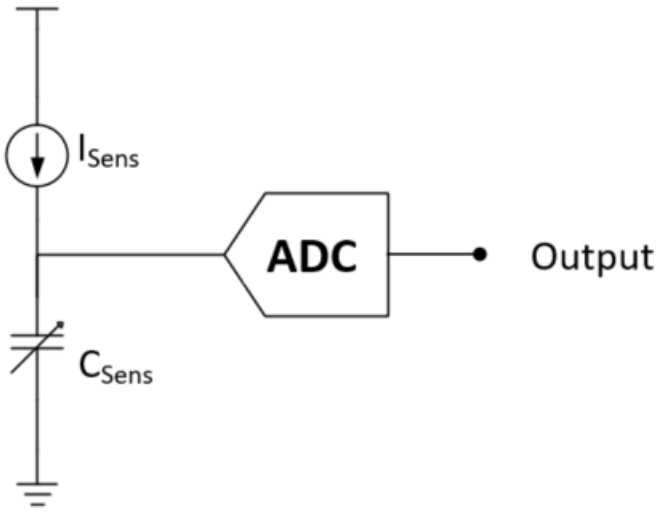

Figure 1.2: A simple implementation of the current-to-Voltage capacitance-to-digital techniques. A current I_{Sens} is injected into a variable capacitive sensor C_{Sens} over a fixed time Ts. The voltage V_{Sens} of the capacitor node is measured with an ADC, and this value can be used to determine the value of the capacitor C_{Sens+}. A transmission gate connected between the capacitor and GND would then be used to discharge the capacitor so it could be tested again, not shown.

However, there are issues with the simplistic Current-to-Voltage Capacitance-to-Digital technique just described. First, if the amount of current that is injected into the capacitor or the amount of time the current is injected into the capacitor is not constant due to noise, then the resulting measured voltage will contain this noise too and be less accurate. Second, the loading of the ADC, current source, and other parts of the circuit will contribute parasitic capacitance, resistance, and inductance which will change how much of the current I_{Sens} is actually injected into the capacitor C_{Sens}. Finally, there could be capacitor leakage that would lead to charge being dissipated before it can be measured.

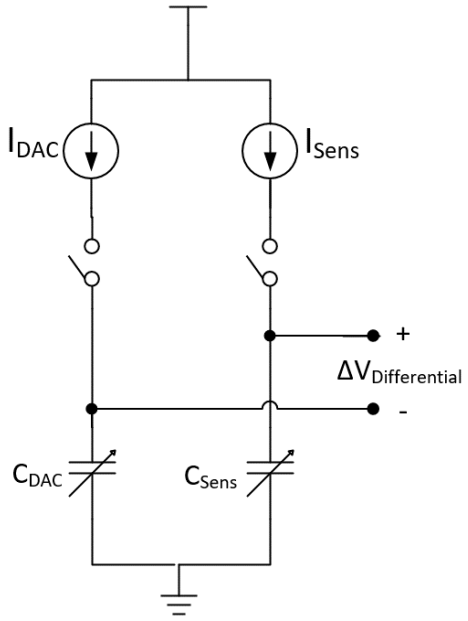

Figure 1.3: A simplified diagram of the circuit used in [16], where currents I_{DAC} and I_{Sens} are injected into C_{DAC} and C_{Sens}, respectively. If I_{DAC} and I_{Sens} are the same, then the differential voltage $\Delta V_{Differential}$ will output 0 or 1 depenidng on whether C_{DAC} is greater in value than C_{Sens}

To eliminate these discrepancies, in reference [*18*], another approach is taken as shown in Figure 1.3. First, to solve the issues of current and timing noise for the current sources, two current sources inject currents I_{Sens} and I_{DAC} into two capacitors, C_{Sens} and C_{DAC} respectively, for a fixed time interval T_{Sens} and T_{DAC}, respectively. C_{Sens} is the variable capacitive sensor, while C_{DAC} is a digitally controlled capacitor with known capacitance values. The two voltages produced, V_{Sens} and V_{DAC}, produce a differential voltage $\Delta V_{Differential}$ between the two nodes.

The differential voltage $\Delta V_{Differential}$ is given by:

$$\Delta V_{differential} = V_{sensor} - V_{Dac} = \frac{I_{sens} * T_{sens}}{C_{sens}} - \frac{I_{Dac} * T_{Dac}}{C_{DAC}} \quad (1.6)$$

If the two current sources are set to be the same so that $I_{Sens} = I_{DAC}$, and they also receive the same fixed time interval so that $T_{Sens} = T_{DAC}$, then the equation (1.5) is changed to

$$\Delta V_{differential} = V_{sensor} - V_{Dac} = I_{sens} * T_{sens} * \left(\frac{1}{C_{sens}} - \frac{1}{C_{DAC}}\right) (1.7)$$

Thus, in equation (1.7), if C_{Sens} is larger than C_{DAC}, then $\Delta V_{Differential}$ will be negative, and if C_{Sens} is smaller than C_{DAC}, $\Delta V_{Differential}$ will be positive. By inputting the differential voltage into a comparator, a binary output can be produced indicating if C_{Sens} is larger or smaller than C_{DAC} by outputting a 0 or a 1. Then. through successive operations we change C_{DAC}'s value to get closer and closer to C_{Sens}'s value by changing each bit of the capacitor bank on or off given the comparator output, starting at the MSB capacitor bit of the C_{DAC} to the LSB capacitor of the C_{DAC} bit, effectively doing a binary search in hardware to determine C_{Sens} value in a process known as Successive-Approximation-Register (SAR) technique.

To deal with the parasitic capacitances, a calibration can be done using the following method. Given that the C_{Sensor} node will have parasitic capacitance denoted as $C_{ParSens}$ and the C_{DAC} node will have parasitic capacitance denoted by C_{ParDAC} , by adding a second capacitor DAC C_{Offset} to the C_{DAC} node we are able to tune so that $C_{ParDAC} + C_{Offset} = C_{ParSens}$.

Thus, the equation (1.7) becomes:

$$\Delta V_{differential} = V_{sensor} - V_{Dac} = I_{sens} * T_{sens} * \left(\frac{1}{C_{sens} + C_{ParSens}} - \frac{1}{C_{DAC} + C_{ParSens}}\right) (1.8)$$

So while the addition of parasitics leads to a reduction in sensitivity, the fundamental principle remains and we can still determine if C_{Sens} is smaller or larger than the selected C_{DAC}, even if our current supply or time interval the current is injected is variable, and thus we can digitize our capacitance value using a binary search SAR-Algorithm, as described before.

1.2.2 Voltage charge-redistribution digital conversion techniques.

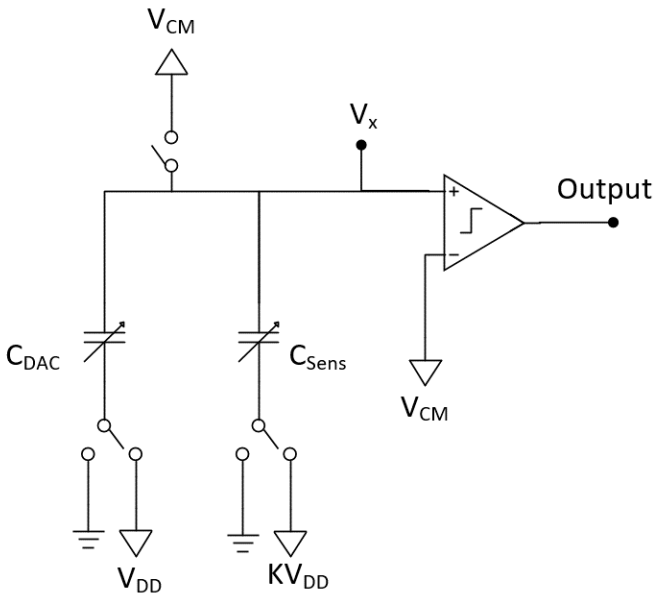

Figure 1.4: A simplified representation of the circuit used in [17]. By first charging C_{Sens} to a value KV_{DD}, and then charging C_{DAC} to the value VDD afterwards, the comparator output will output a 0 or 1 depending on whether Vx is greater than VCM, which is determined by whether C_{DAC} is greater than C_{DAC}

To further improve the performance of voltage domain circuitry, another approach is proposed to convert capacitance to voltage without using injected currents, but instead using voltage-charge-redistribution techniques [*19*]. In reference [*18*], just like in [17], the capacitance of the capacitive sensor C_{Sens} and the capacitance of a controllable capacitor C_{DAC} are compared by converting their relative capacitances to voltage values and digitizing the result with a voltage-comparator. As stated in equation (1.4), if a voltage is applied to a capacitor, the amount of charge stored is directly related to the value of the capacitance of the capacitor. Given this, if C_{Sens} and C_{DAC} are charged up with the same voltage but of opposite polarity, we will have positive charge in C_{Sens} and negative charge stored in C_{DAC}. By making a circuit that effectively sums the two charges together, we can use the polarity (positive or negative, relative to a reference voltage) of the result to determine which capacitor is bigger, and then use the same SAR technique as described before

An improved version of this method was reported in reference [*17*]. As illustrated in Figure 1.4, a DAC capacitor bank and the sensing capacitor are connected to a voltage comparator. Different from the basic method discussed above, this time the DAC capacitor bank and sensing capacitor are both attached to the + sign of the comparator, called node *Vx*, while a static DC offset voltage V_{CM} is applied to the – terminal. This circuit operates in 2 cycles. The first cycle is the sampling phase, where the node *Vx* is connected to an offset voltage V_{CM} and the other terminal of the sensing capacitor is connected to V_{DD}. The amount of charge stored on the node will then be (ignoring parasitics):

$$Q_{Vx} = (V_{CM} - V_{DD}) * C_{sens} \quad (1.9)$$

In the second cycle, called the conversion phase, we then disconnect node *Vx* from the voltage V_{CM}, and connect the – terminals of our activated capacitors of our capacitor bank (whose total value will be C_{DAC}). Due to conservation of charge, the voltage on the node *Vx* will be:

$$V_x = V_{CM} + V_{DD} * \frac{C_{DAC} - C_{Sens}}{C_{DAC} + C_{Sens}} \quad (1.10)$$

If we rewrite the equation (1.8) in terms of the differential voltage applied to the comparator and reduce some terms, we can rewrite equation (1.9) as:

$$V_x - V_{CM} = m * (C_{DAC} - C_{Sensor}) \quad (1.11)$$

$$m = \frac{V_{DD}}{C_{DAC} + C_{Sensor}} \quad (1.12)$$

From equation (1.9), we can see that the polarity of the differential voltage is based solely on which capacitor is larger, C_{DAC} or C_{Sensor}. If C_{DAC} is larger, than the comparator will output a 1. If C_{Sensor} is smaller, the comparator will output a 0. Thus, by using the same SAR technique described in [*17*] doing a binary search over N cycles, we can quantize the value of C_{Sensor} to N bits of resolution.

1.2.3 Limitations of capacitance-to-voltage digital conversion

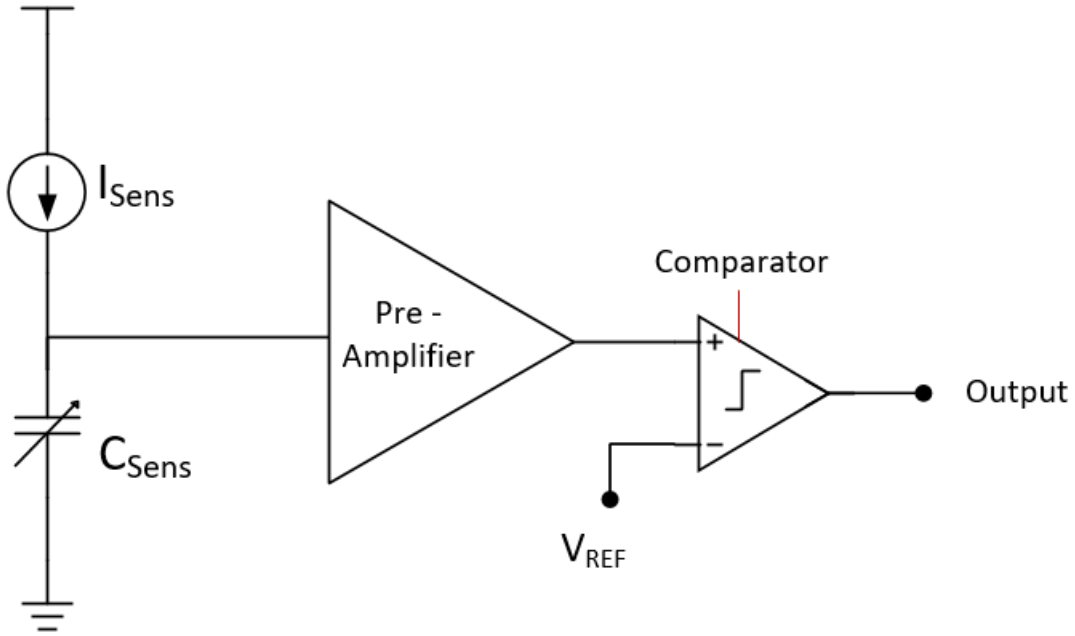

Figure 1.5: A more detailed representation of the capacitance-to-voltage digital conversion circuit, showing how the pre-amplifier amplifies the signal of the capacitive sensor, which is then digitized by a comparator.

As shown in Figure 1.5, a more detailed representation of the ADC conversion of voltage is performed by first amplifying the voltage with a pre-amplifier, and then using a comparator to digitize the value with a reference V_{REF}. The front-end pre-amplifier noise consists of thermal and flicker noise, with flicker noise being the major contribution to noise. To solve this issue, techniques such as chopper amplifiers can be used, but this leads to significant power costs[*20, 21*]. An alternative is to use those amplifiers with lower gain and larger integrating capacitors, as shown in Figure 1.6, but this also leads to lower bandwidth and larger IC area with higher cost [*22*].

For the comparator, due to mismatch between the inputs, the actual comparison is not ideal – there will be an offset in the V_{REF} node as shown in Figure 1.5 that will lead to an inherent inaccuracy[*23*]. While this can be reduced using trimming circuits, this leads to more complex circuitry, increased cost,

and a reduction in performance due to the parasitic and noise introduced by the trimming circuitry. Additionally, a single bit error using the SAR algorithm described above can lead to a significant error.

Finally, both the pre-amplifier and the comparator based ADC suffers from increased challenges in the analog circuit design as IC technology nodes get smaller. This comes from increased mismatch, lower voltage headroom, susceptibility to noise, high circuit complexity due to the use of various signal generators and reference circuits, [24].

As transistors become smaller, digital techniques become more attractive versus analog techniques, due to increased digital speed and the fact that voltage references are less stable than frequency references at smaller technology nodes [25]. Thus, in this we proposed that capacitance-to-frequency and time domain sensing techniques are a more sensible design approach for future Capacitance-to-digital techniques.

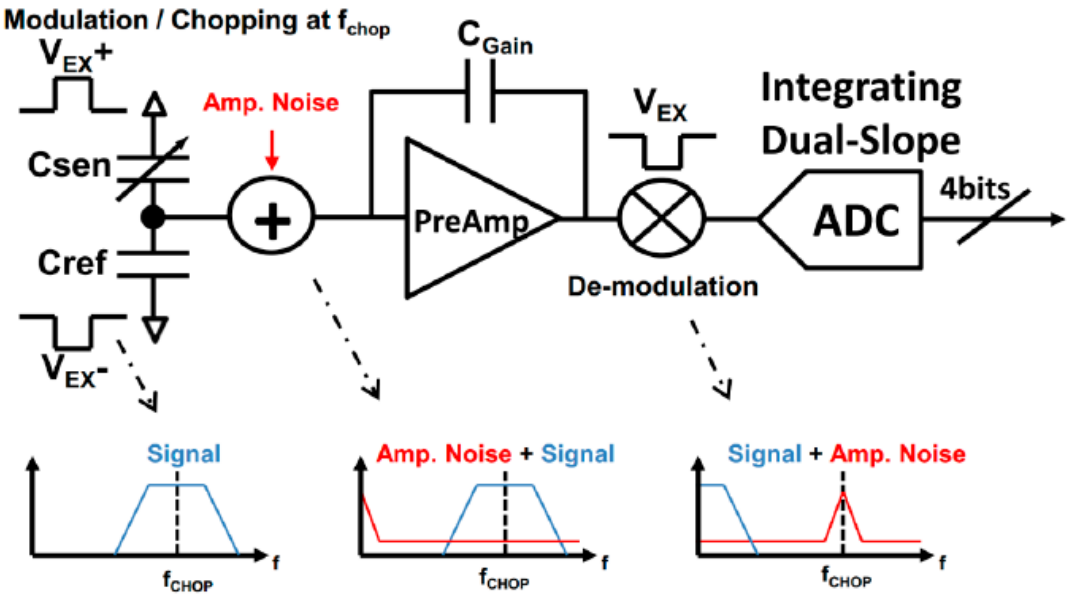

Figure 1.6: An example of a traditional Capacitance-to-Digital circuit using voltage domain techniques, using a pre-amplifier with an integrating C_{GAIN} capacitor, and a comparator based ADC. Note that C_{GAIN} will limit speed and become more expensive if it is made bigger to lower noise impact. Reprinted from [22], MDPI journal with permission MDPI ©, 2017.

1.3 Objectives and outline of the thesis

As mentioned above, pressure sensors are important in many applications. With their simple design and high precision, capacitive pressure sensors are one of the best designs of pressure sensors. In this thesis, we proposed a new class of microstructure-based direct digital capacitive pressure sensor, including the microstructured pressure-to-capacitance transducer and its capacitance-to-frequency digital conversion circuit. The microstructured transducer design provides ease of fabrication and long-term durability. The novel sensor circuit using digital phase-locked-loop (PLL) enables highly sensitive detection of capacitance. Full implementation of the proposed sensor system, including taped out circuits and system-on-chip integration, requires years of tedious works and I am not able to finish within my master study. Thus, I carried out proof-of-concept demonstration of the proposed sensor system. I first fabricated and characterized the microstructured transducer, and then constructed the digital PLL using

discrete parts. The experimental results and analysis show the viability of implementing such sensor system in the future.

In this thesis, I first gave an overview of various pressure sensors, including capacitive pressure sensors, in Chapter 1. In this chapter, I also talked about various types of circuitry people designed for capacitive sensors. The development and limitations of voltage domain circuitry was discussed in detail. This motivates people to develop the time/frequency domain circuitry for capacitance measurement. In the end of this chapter, objectives and outline of the thesis were given.

In Chapter 2, I explained the working principle behind our microstructured sensor design. In the microstructured sensor (or called transducer), both its variable capacitance and parasitic capacitance, as well as inductance are present in its circuit model. The values of these circuit parameters are needed for the sensor-reading circuit discussed in Chapter 3. For retrieving values of these circuit parameters, we constructed and measured several different sensors using various design parameters. For those values that could not be measured using our current set-up, I used COMSOL simulation software to calculate them. To validate my simulation results, I showed that the simulation results matched those values that can be measured experimentally.

In Chapter 3, the use of resonators for the purpose of capacitance detection is argued, followed by the need for phase-locked loop control systems to decrease the noise and therefore enhance the resolution of digitized results if used in capacitance-to-digital circuitry design. Then, it is explained the mathematics and specifics of the digital phase-locked-loop design and their relation to traditional analog phase-locked-loop (PLL) design, showing the advantages of digital design on noise reduction. Using Cadence simulation software, a 65 nm-technology-based digitally-controlled-oscillator that the capacitive sensor discussed in Chapter 2 could be connected to was simulated, showing how a change in capacitance leads to a change in frequency. From these results, the viability of integrating the capacitive pressure

sensor from Chapter 2 into a digital PLL system shown in Chapter 3 for the purposes of digitization and sensor reading is shown to be practical. Finally, to show that a digital PLL system can be used as a ADC for the purposes of sensor reading, a real-word digital PLL using discrete parts was constructed and shown that the sensing circuit constructed was able to accurately sense and digitize applied frequency disturbances, thus demonstrating the viability of the digital-PLL ADC design.

In Chapter 4, the thesis work is summarized. In order to fully implement the proposed microstructure-based direct digital capacitive pressure sensor, several projects were proposed as future works.

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25. D. Koscielnik and M. Miskowicz, “Designing time-to-digital converter for asynchronous ADCs”. Paper presented at IEEE Design and Diagnostics of Electronic Circuits and Systems 2007.

Chapter 2: Microstructure-based capacitive pressure sensor

In order to construct a working prototype using our novel capacitance measurement technique discussed in Chapter 3, we changed the previously developed microelectromechanical sensor [*1*] to a microstructure-based capacitive pressure sensor, and aim to integrate this sensor to our capacitance measurement circuit for a complete sensor system. In this chapter, we built a capacitive sensor that can detect pressure applied vertically to the sensor. We measured the capacitance of the sensor in response to pressure, and we also used the measured capacitance to validate an equivalent circuit model we developed to simulate its performance. We then used this equivalent model to study the influence of resistance and inductance on the sensor performance. This circuit model will be used to simulate how the capacitor sensor interacts with our digital conversion circuit in Chapter 3.

2.1 Working principle

2.1.1 Device structure

As illustrated in Figure 2.1, the microstructure-based capacitive sensor is similar to a classical double plate capacitor except that it uses three plates instead of two. Effectively, the sensor consists of two thin patterned gold electrodes parallel to each other patterned onto a glass substrate. A polydimethylsiloxane (PDMS) 'bridge' with two piers is positioned on the glass substrate so that the bottom of the 'bridge' is above the gold electrodes, separated by a small micron-sized air gap (30 µm to 120 µm). The bottom of this bridge is coated with a thin layer of gold, and this metal plate is suspended above the two gold electrodes attached to the glass substrate, as shown in Figure 2.1.

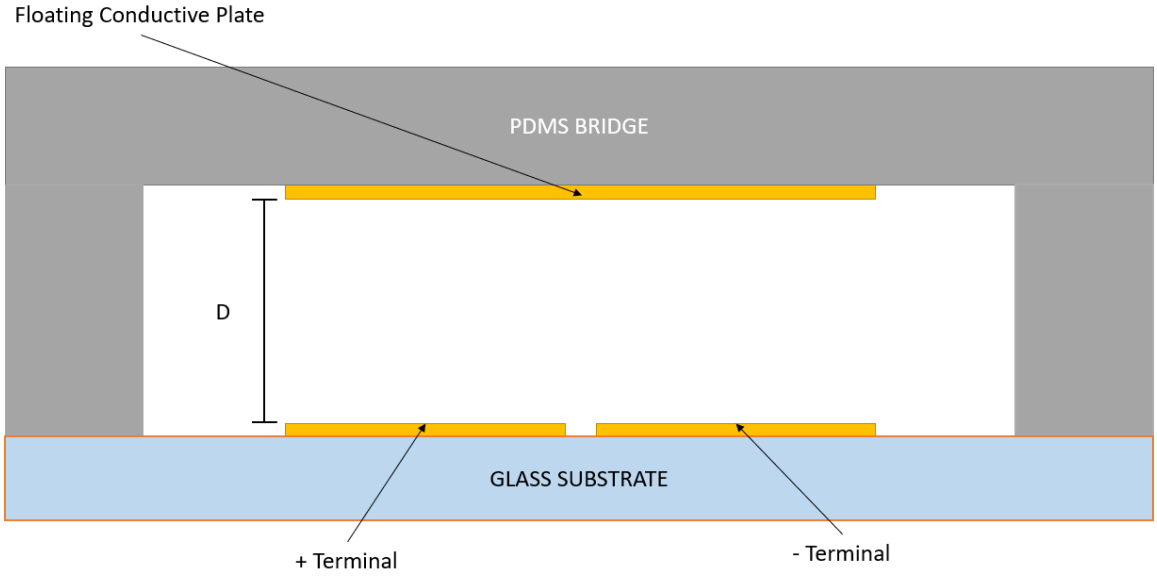

Figure 2.1: Sideview of the capacitive sensor in the static state with no pressure applied to the bridge. The + and - terminals shown in the diagram form the two terminals of our two-terminal variable capacitive sensor.

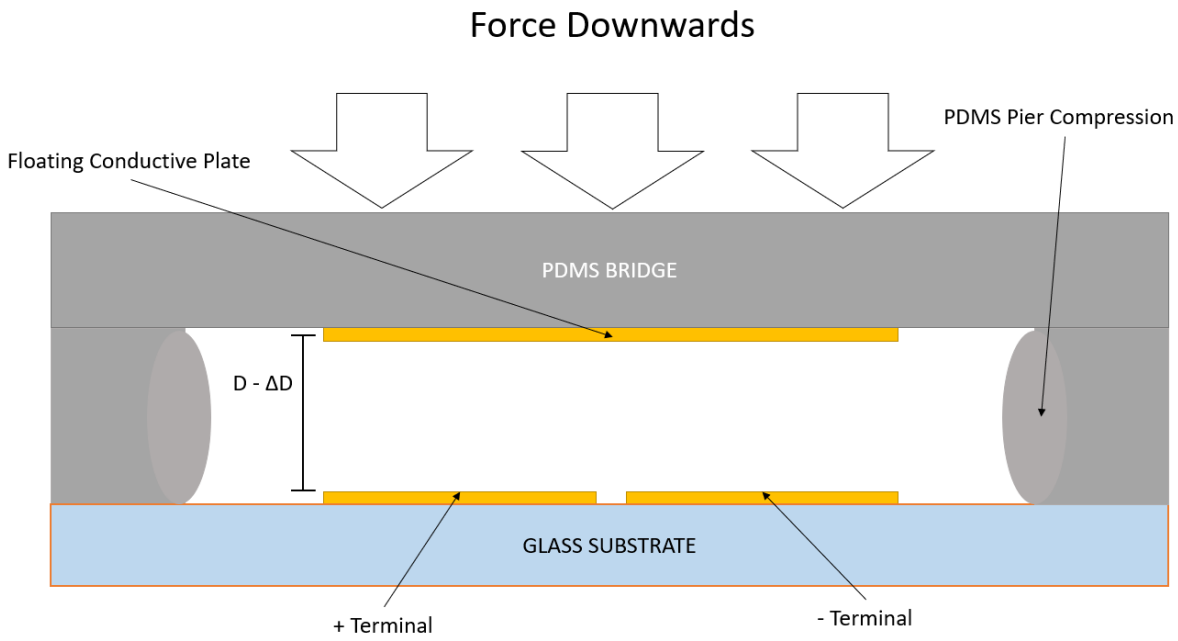

Figure 2.2: Sideview of the capacitive sensor when pressure is applied to the top of the bridge. The change in gap height D between the floating conductive plate and the terminals causes a change in capacitance.

PDMS is a flexible material which is widely used in industry that is easy to produce, flexible, reliable, and non-toxic to people and organisms [*2*], making it a great material to use in sensor applications from industrial to bio-medical. If pressure is applied to the top of the PDMS bridge, the bridge will compress in the vertical direction and the distance between the conductive underside of the bridge and the golden electrodes on the glass substrate will decrease, causing a change in capacitance which is explained further in Section 2.1.2. This decrease of the gap height is due to the low Young's modulus of the bridge (1.32–2.97MPa)[*1, 3*] and the shape change in glass in negligible for its large Young's modulus (50-90 GPa). As the Young's modulus of a material indicates how the material will compress in response to pressure, the capacitance between two gold electrodes will change due to decrease of the gap height This concept can be seen in Figure 2.2.

The benefits of this design are its simple construction and the ability for the device geometry to be easily tuned. Unlike other strain gauges that use resistive or piezoresistive effects, degradation of the metal electrodes does not change the signal and is only limited by the structural integrity of the PDMS, which can have stable long-term characteristics.

2.1.2 Model of the variable sensing capacitor caused by the floating conductive plate and fringe capacitance

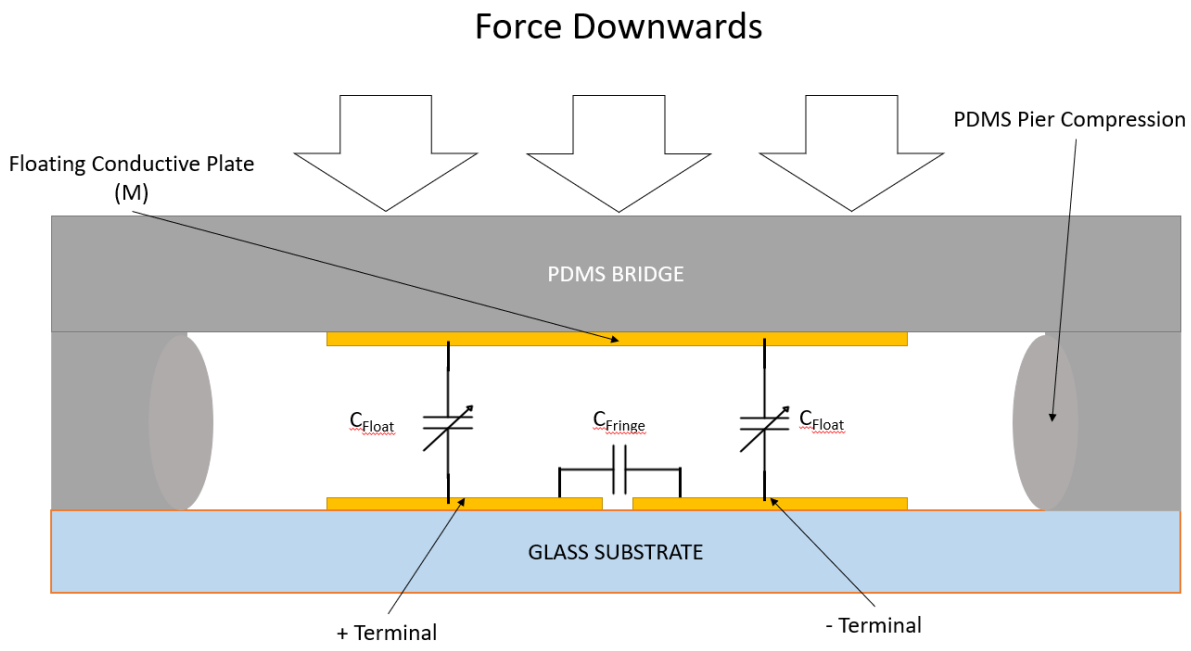

Figure 2.3: The variable capacitance C_{Float} and the static capacitance C_{Fringe} are shown placed on the sideview of the capacitive sensor, to illustrate their positions.

In Figure 2.3, we illustrate the model of our capacitive sensor. A variable sensing capacitor is formed between the two terminals of the gold electrodes patterned on the glass when the floating conductive plate is suspended above the gold electrodes patterned on the glass. Unlike traditional metal capacitors that consist of two layers of metal separated by a dielectric, this device works as a two terminal device where the two terminals have a third floating terminal between them, which effectively forms two variable capacitors in series. The use of a third floating terminal in capacitor based transducers has been used in other sensor designs, and is useful in reducing the complexity that may arise from requiring only two plates [*4, 5*].

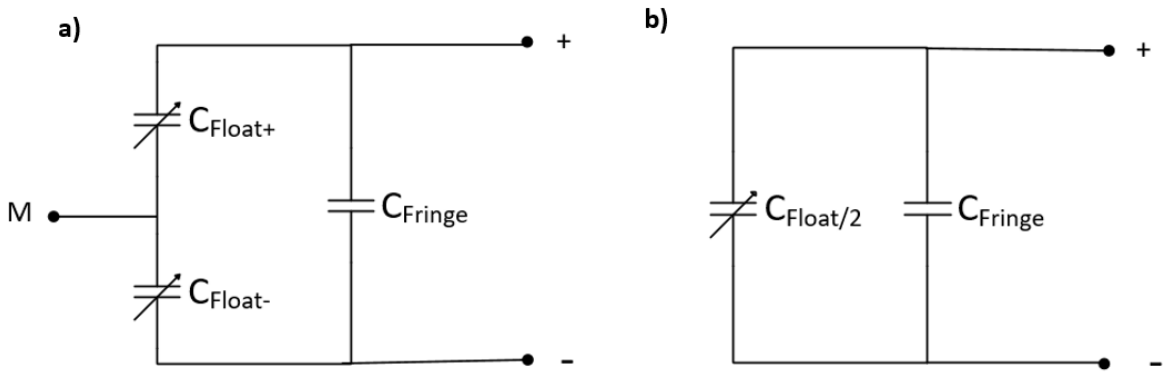

Figure 2.4: a) The capacitance circuit model, showing how the middle floating plate 'M' forms two variable capacitances between the + and - terminal, as well as the static capacitance between the + and - terminal directly. b) the model in a) can be reduced to a single variable capacitor.

As seen in Figure 2.3 and Figure 2.4, the static fringe capacitance, denoted by C_{Fringe}, represents capacitance between the + and - electrodes that occurs when there is no PDMS bridge present. While this would appear to be a simple capacitance to calculate, the analytical solutions are quite complex to derive due to non-traditional geometry [*6*]. Thus, measurement and simulation were used to obtain this value, as shown in Sections 2.2 and 2.3.

The second capacitance component to consider is the capacitance between the two electrodes and the floating middle plate. We can model this as two capacitors in series of with capacitance denoted as $C_{Float+-}$, with one variable C_{Float+} capacitor being between the + terminal and the middle plate, and the second C_{Float-} capacitor being between the middle plate and the terminal, resulting in an effective capacitance of $C_{Float}/2$ (assuming C_{Float+} and C_{Float-} are equal). The total capacitance is then given by:

$$C_{Total} = \frac{C_{Float}}{2} + C_{Fringe} \quad (2.1)$$

2.1.3 Other considerations

More components of the device need to be considered to create an accurate circuit model of this microstructure based capacitive sensor. An actual designed sensor would be connected to pads designed for either probe measurement connections (large pads, 2 mm x 2 mm in area) or bond-wire pads (small pads, with 60 µm x 30 µm area). The bond-wire pads would be used for a final integrated product using bond-wire technology to connect directly to a sensing IC so as to reduce parasitic capacitance and size, while the sensors with probe pads would be used to characterize the capacitive sensor itself using simple probe instruments that would not require advanced precision to connect to measuring equipment – these would be the sensors we could measure using the facilities in the nanoFAB at the University of Alberta.

Finally, we assumed that the electrode pads would be connected to the connection pads via narrow metal traces. While we could have the pads connected to the sensing electrodes, or even have the connections attached directly to the electrodes themselves, by placing the contacts further away from the electrodes we isolate the electrode-bridge capacitance from the pad-probe capacitance, and allow more space to position the bridge over the electrodes without obstructing or contacting the pad connections. These three components can be seen in Figure 2.4 above which illustrates the basic structure of all sensors simulated or constructed.

First, like all real devices, we will have inherent resistance. The resistance of a rectangular block of material is given by

$$R = \rho * \frac{l}{A} \quad (2.2)$$

Where ρ is the resistivity of the material involved,

l is the length of the conductor from one end to the other

A is the cross-sectional area.

From equation (2.2), we can surmise that resistance of our sensor can be decreased by increasing the thickness layer or increasing the width of the electrode. Given the materials and geometry used, parasitic resistance was not considered a major factor.

As discussed further in Chapter 3, the inductance of this sensor must be kept at a reasonably low level on the order of a few nanohenries if it is to be used in a high-frequency design. From [*7*] we can approximate the self inductance of a straight conductor of rectangular geometry as:

$$L_{flat} = 2 * 10^{-4} l * \left[\ln\left(\frac{2l}{w+t} + 0.5 + 0.2235 \left(\frac{w+t}{l} \right) \right) \right] [\mu H] \quad (2.3)$$

Where *l* is the length of the conductor from one end to another,

w is the width of the conductor,

t is the thickness of the conductor.

Using Equation (2.3), and if each electrode we have has dimensions of 1 mm x 1 mm and thickness 1 µm, we have an approximate inductance of 0.283 nH for each electrode. For two electrodes, this should equal 0.566 nH total. However, while the self-inductance of this should equal 0.566 nH, we should have even more inductance due to the floating plate and the mutual inductance between all the conductors forming a current loop. Thus, without considering these effects the magnitude of the parasitic inductance of our sensor is unknown. To solve this, simulation of the sensor was done in COMSOL. These induction

parameters are important to consider in Chapter 3 of this thesis, at the very least for putting an upper bound on the assumed inductance.

2.2 Fabrication and characterization

Several steps are required to fabricate our capacitive sensors proposed in Section 2.1. First, a photomask for patterning the electrodes was designed and constructed using the pattern generator (Heidelberg DWL-200) in the nanoFAB at the University of Alberta. Then, using this photomask the electrodes were patterned with gold onto a soda-lime 5 inch glass wafer using the lift-off pattern-transfer method. Finally, the PDMS bridges were constructed using a molding process, with a deposited metal circle on the bottom. These steps are described in full below.

2.2.1 Electrode and mask construction

Probe-pad, bond-wire, and magnetic loop construction

The construction of our capacitive sensors is a multi-step process, which begins with the construction of the photomask. Using L-Edit – a mask creating software, several variations of the sensor's geometry were constructed.

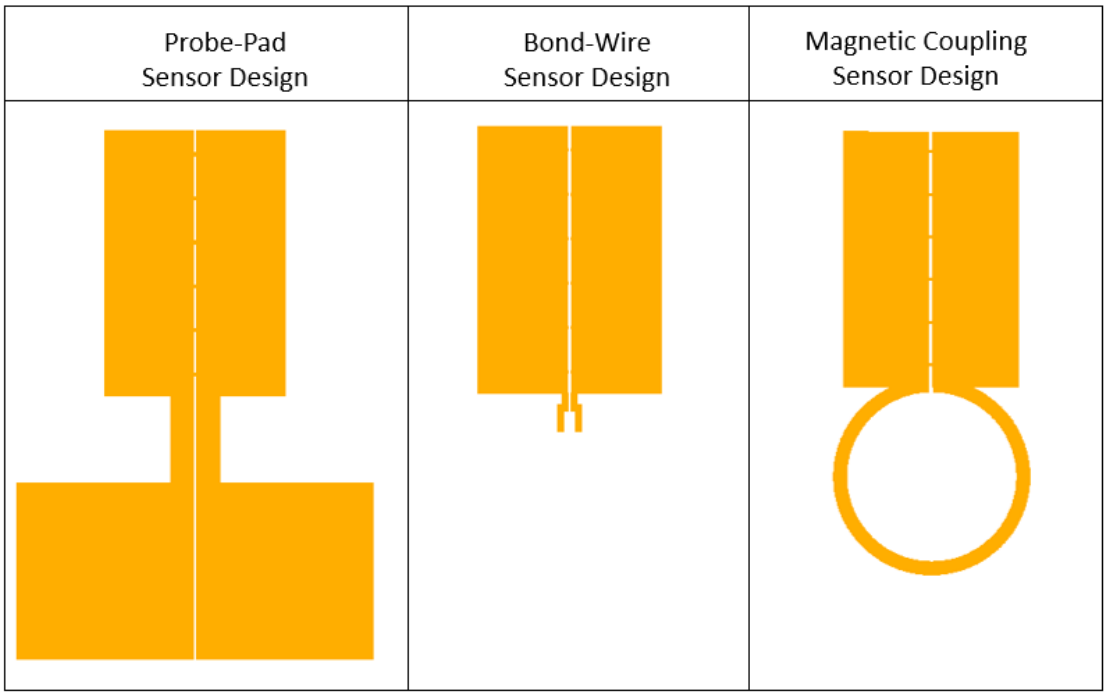

Figure 2.5: The three types of sensors fabricated onto the soda-lime glass wafer, showing the probe-pad design, the bond-wire pad design, and the magnetic loop design. Variations of these three types of sensors were made General structure of capacitive sensors

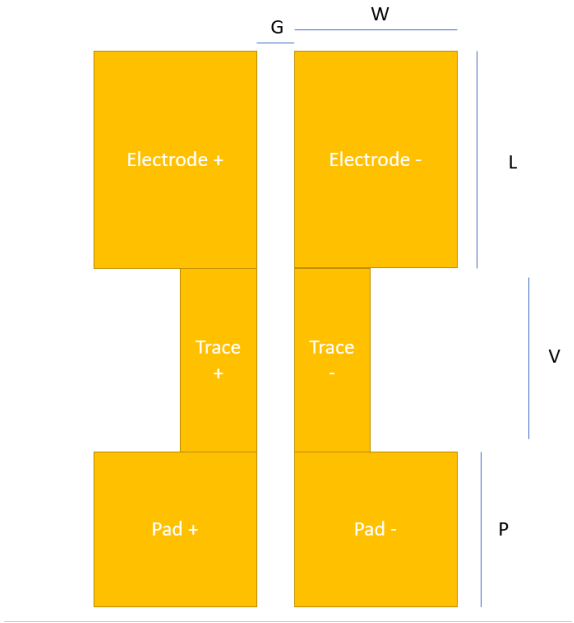

Figure 2.6: General structure of the capacitive sensor. G represents the gap distance between electrodes, W represents the width of the electrodes, L represents the length of the electrodes, V represents the trace length between the electrodes and the pads, and P represents the pad dimensions.

The general structure and dimensions of all sensors made can be modified by changing the geometric variables shown in Figure 2.6, other than the addition of a magnetic coupled sensor, which have a single loop ring, not shown in the diagram. In Figure 2.7, all variations of the sensors that were produced are shown.

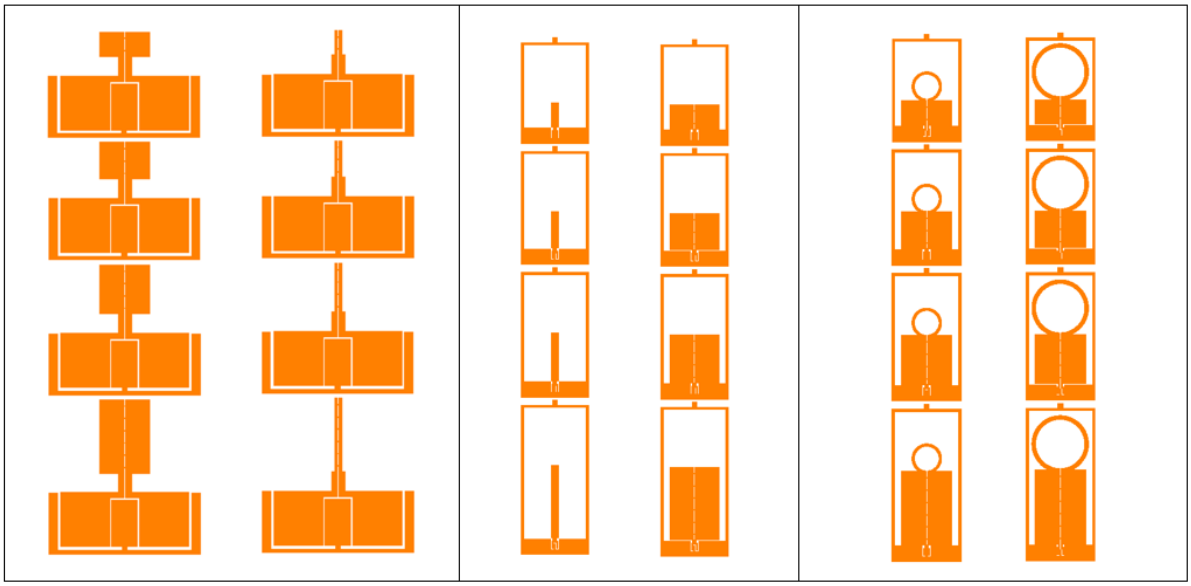

Figure 2.7: The variations of the probe-pad, bond-wire, and magnetic loop sensors that were fabricated, showing how the electrode size and magnetic loop radii is varied.

Type 1: Probe-pad sensors

The first type of sensors we made consisted of electrodes connected to large 2 mm x 2 mm probe pads. This group of sensors was designed to be compatible with standard tungsten needle probes so they could be characterized and measured using the Keithley 4200 Semiconductor Characterization System available in the nanoFAB at the University of Alberta. The downside to this is the introduction of more fringe capacitance and inductance, as well as area size. As shown in Figure 2.6, 8 types of sensors with using this design were made. 4 sensors consisted of 'skinny' electrodes with gap width G of width W of 125 µm and length L of 1000 µm, 1500 µm, 2000 µm, and 3000 µm. The other 4 sensors consisted of 'wide' electrodes with width W of 1000 µm and length 1000 µm, 1500 µm, 2000 µm, and 3000 µm. These

different electrode widths and lengths was done so that we could test how capacitance changed for different electrode sizes, but also for additional inductance introduced by increasing the length of the electrode. For all 8 sensors, the electrodes were spaced 1 mm away from the pads by a via, given as value *V* in Figure 2.6.

For these devices, a third electrode (GND pad) could be placed between the + and – terminal. This electrode was intended to be used as a ground shield if the sensors were tested at high frequency (> 1 GHz) [*8*]. This work was not carried out in the thesis, and only sensors (with width of 1000 µm and length of 1000 µm and 3000 µm, respectively) without the GND pad were made and characterized.

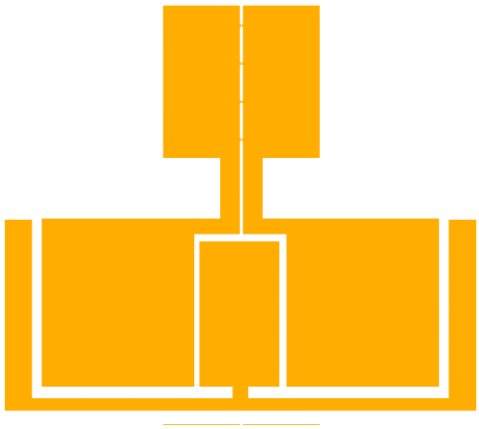

Figure 2.8: Probe-pad sensor with additional GND shield pad added, to reduce noise in a high-frequency design.

Type 2: Bond-wire sensors

The second set of sensors consist of the same 8 electrode sizes used in the probe-pad sensors, but this time a 60 µm x 300 µm pad to be attached with bond-wire was used as shown in Figure 2.8. Given the much smaller pads, we expect this should decrease parasitic inductance and fringe capacitance as compared to the sensors with the probe pads and is the design that would be used in a final integrated

system. The pad-pitch was sized for 60 µm x 300 µm, which is within the size parameters allowed for wire-bonding of 65 nm circuits, which is discussed further in Chapter 3. [*9*]

Type 3: Magnetic loop sensors

Finally, the last group of sensors consisted of 8 sensors that were given a simple single turn induction loop, allowing for potential magnetic coupling to an IC circuit, vs using a direct metal connection. 4 of the sensors had electrode width (*W*) of 1 mm and electrode length (*L*) of 1000 µm, 1500 µm, 2000 µm and 3000 µm, and a magnetic induction loop of 1 mm in diameter. The other 4 sensors had the same electrode sizes, but with an induction loop of diameter 2 mm.

2.2.2 Fabrication of capacitive sensors

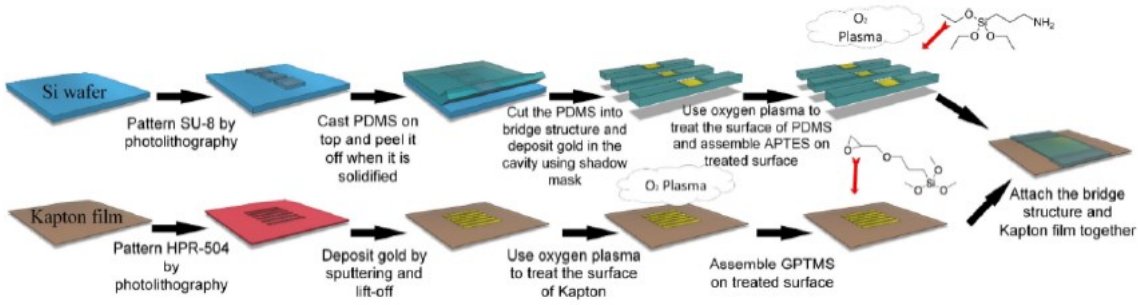

Figure 2.9: From [1], a figure showing the procedure for fabricating the PDMS Bridge-Electrode sensor. ***Reprinted from Nanoscale*** *"L. Meng, Fan, Shicheng Mahpeykar, Seyed, Wang, Xihua. , Digital microelectromechanical sensor with an engineered polydimethylsiloxane (PDMS) bridge structure.* Nanoscale." ***with permission from Nanoscale.***

The sensors were made using previous techniques developed in [*1*], as shown in Figure 2.9. The steps are as follows:

Lift-off of gold on glass

First, a 4" soda-lime glass wafer was cleaned using piranha etch to remove any surface contaminants. Then, the wafer was spin coated with HPR 504 positive photoresist and patterned using the previous discussed mask using photolithography. A gold layer was then sputtered onto the surface.

The lift-off process was then done by soaking the glass wafer in acetone for two hours, and rubbing off the gold, leaving only the gold-patterned electrodes on the glass wafer.

The layer thickness of the gold electrodes was approximately 200nm – as the relative thickness of the electrode is much smaller than the dimensions of the bridge and electrode size, exact knowledge of the thickness was not required and was estimated using resistivity of a rectangular test spot and Equation (2). A profilometer could be used for more accurate information but was not necessary for this project.

PDMS bridge construction

For the PDMS bridge, we used a method of nanostamp imprinting, where a material is solidified in a nano-mould, and the resulting structure removed after. Using SU-8 as a template, we made the negative of the bridge, using a mask-set previously produced in [*1*]. The height of the negative bridge was 90um, leading to a gap distance of 90um for the produced bridges.

Once the negative stamp was made, 10ml of PDMS solution was prepared using the SYLGARD 184 Elastomer Kit [*10*] and poured over top of it. After drying over 24 hours, the PDMS layer had solidified around the negative stamp.

After this step, a precision knife was used to carefully carve the bridges out of the PDMS layer, and peel them off the aluminum substrate. The bridges were approximately 8mmx18mm in size.

Then, using a simple mask constructed from a piece of Kapton plastic with holes punched out with a standard holepunch, gold is deposited in a thin layer, so as to give the bottom of the bridge a conductive circular region without any metal being attached to the piers.

Placement of bridge and testing

While we could attach the PDMS bridge to the glass substrate permanently to make a more secure sensor[*11*], in this paper it was decided to have the bridge simply rest on it's piers without permanently attaching it to the substrate. While a final version would be attached to the substrate for stability, we found it prudent to allow it to simply rest on the wafer so we could use a single bridge and position it as necessary over the sensor electrodes.

2.2.3: Characterization of capacitive sensors

One set of sensors were fabricated and characterized in this project. The largest sensor was chosen, with an electrode area of 1 mm x 3 mm with 2 mm x 2 mm sensor probe pads.

Resistance

Using a standard multimeter, the resistance of the sensor from probe-pad to probe-pad with the bridge compressed till it contacts the electrodes was 10.6 ohms. Given the thin layer of gold, this is to be expected. By increasing the thickness of the gold layer, we could reduce this resistance without changing the capacitance characteristics significantly – instead of a 200 nm layer, a 2 µm layer could be deposited instead. However, this was not done due to the high cost of gold.

Pressure measurement set-up

To apply pressure to the sensor, we simply apply weight on top of the sensor. Given that the Earth's gravity force downwards is relatively constant, by placing weight on top of the sensor a known force can be applied. As pressure is force divided by area, if we know the dimensions of the sensor, we can calculate the pressure being placed on top of it.

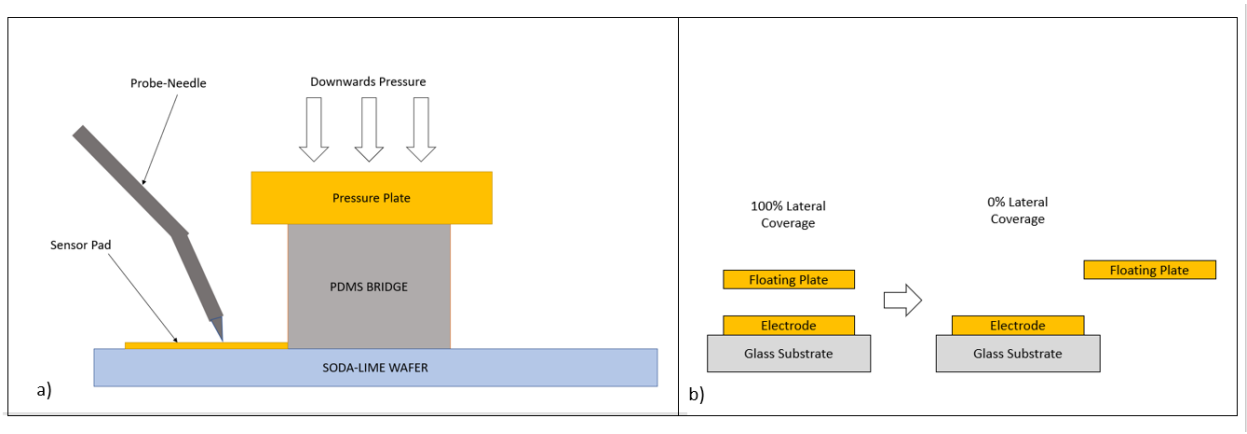

Figure 2.10: a): Diagram showing how the use of a pressure plate was used to apply vertical pressure (and thus vertical displacement) on top of the PDMS bridge without touching the probe needles. b) The second variable we varied and tested was the lateral position of the bridge over the electrodes, which should also affect the capacitance values we measure.

However, while the simple solution would be to balance several weights on top of the sensor using a platter, due to the design of the sensor this approach didn't give reliable results. The proximity of the large needle probes to the sensor means that a very small pressure plate must be used when characterizing the sensor, and not much weight could safely be balanced on it. As well, the probe-station we used had a confined space with limited room. This is illustrated in Figure 2.10a).

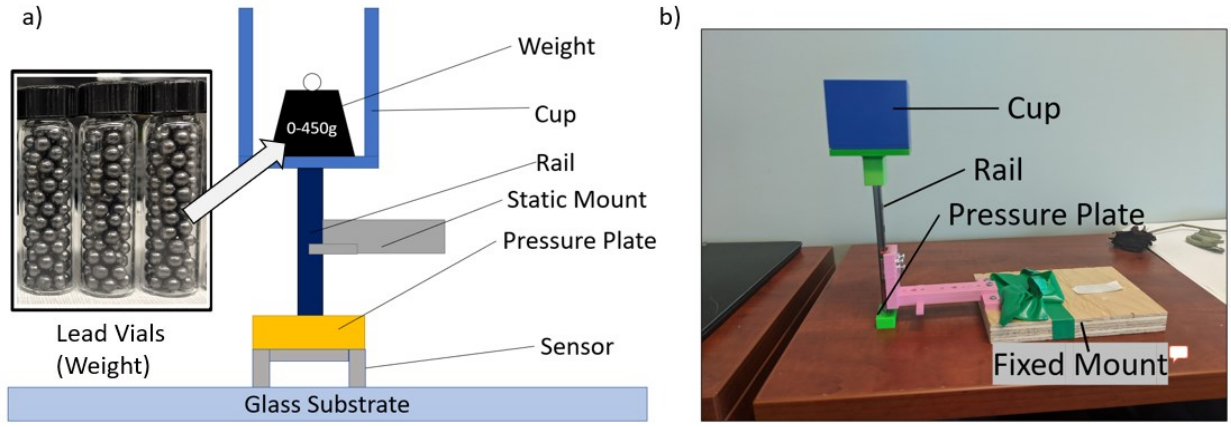

Figure 2.11: a): A basic diagram showing the basic set-up, where a pressure plate is affixed to a linear rail that can only move in the lateral direction. On top of the rail is a cup where weight can be placed, which will apply pressure to the pressure plate. Vials filled with lead were used as weights, as shown. b): Implementation of the pressure plate applicator using 3D printed parts and a ball-bearing linear rail.

To resolve this issue, a pressure applicator was designed. It consisted of a 3D Printed rectangular "pressure plate" of a size that was able to apply pressure across the entire sensor area equally, but without touching or interfering with the sensor probes. Then, so as to balance a significant amount of weight directly on the pressure plate without touching the probes, a linear ball-bearing rail guide was used, specifically a LML9B Miniature Linear Rail Guide [*12*]. On-top of the rail guide, a 3D printed 'cup' was attached that could hold weight. To increase the amount of weight while having the pressure applicator fit within the Keithley 4200 test setup, 9 vials filled with lead-pellets were used as weights, with each vial weighting approximately 50 g. Combining the weight of the pressure applicator and the lead vials a total of 605 g weight was applied to the sensor.

As pressure is related to pressure by:

$$P = \frac{F}{A} \quad (2.4)$$

Where F = force in newtons, and A = area in m^2. Using Equation (2.4) and knowing the mass of the weight being placed into the cup, we can calculate that the maximum force applied to the sensor should be 5.935 newtons. Given a sensor area of 8 mm x 15 mm, this equals a max pressure of 49 kPa approximately. The pressure-applicator setup can be seen in Figure 2.11.

Keithley 4200 and capacitance measurement

To measure the capacitance change of our sensor in response to pressure, we used the Keithley 4200 Semiconductor Characterization System [*13*]. The system can measure the capacitance by measuring the phase angle between current and voltage at certain test frequencies to determine the impedance and thus the capacitance. Testing capacitors of known values was done before all measurements to verify the set-up was working properly.

Experimental procedure:

First, two tungsten probes connected to the Keithley 4200 SCS analyzer were positioned onto the probe-pads of our device. Then, the PDMS bridge was positioned so that the bottom of the bridge was overtop the electrodes, at 3 different overlap positions. Once positioned, the pressure applicator was secured to the probe station, so the pressure plate could freely rest on top of the sensor without touching the probe pads. Then, 5 measurements with different forces acting on the sensor were taken. These measurements were done for the sensor without any weight applied, the sensor with the pressure plate applied and no weight in the cup, and 3 measurements with 3, 6, or 9 vials of lead in the cup, respectively.

This was repeated 9 times for every pressure point, and then averaged. Error bars were given by standard deviation, which is defined as:

$$s = \sqrt{\frac{\sum_{i=1}^{N}(x_{i-}\bar{x})^2}{N-1}} \quad (2.5)$$

Where *S* equals the standard deviation for each test set, *N* equals the amount of samples, x_i equals the value of each data point, and $\bar{x}$ equals the average of all data points of the sample. Equation (2.5) was used to calculate the standard deviation of each data point.

The bridge was also moved in the lateral direction from approximately 100% coverage to less coverage, in two different positions, leading to 3 trendlines. As the bridge is moved laterally and less of the bridge is suspended over the electrodes, we expect the capacitance to decrease. The results from these experiments are shown in Section 2.4. The testing setup can be shown in Figure 2.12 below.

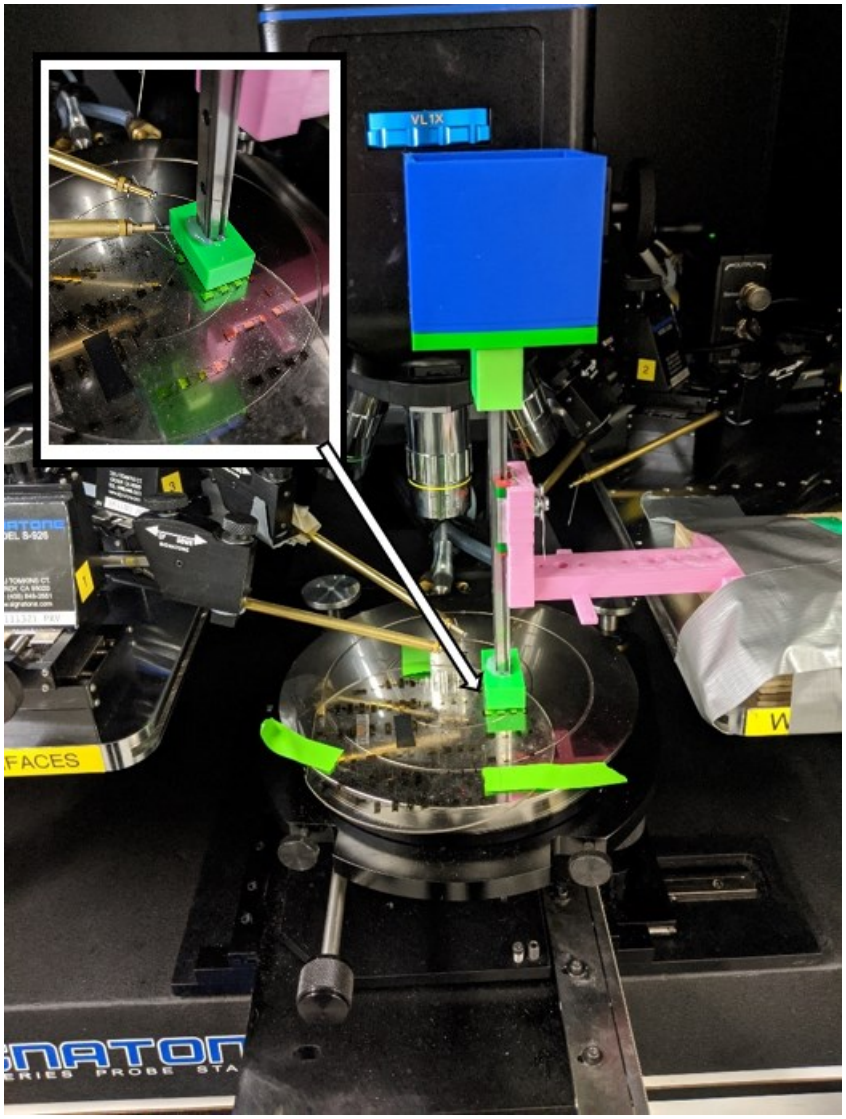

Figure 2.12: The capacitance testing setup used to measure the change in capacitance in response to pressure. A Keithley 4200 SCS analyzer with two probes was connected to the two terminals of our device. Weights were added to the cup in different intervals, and the capacitance at these different pressures was measured. As can be seen in the zoom-in, the pressure plate is big enough to apply pressure to the whole sensor without touching the probe needles.

2.3 Simulation

Using the COMSOL Multiphysics, we simulated the capacitance of the sensor, in order to verify the results we measured. The results confirmed our model and analysis of the sensor are correct.

Additionally, we simulated the inductance we expected to see from our sensors, as we were unable to measure this value directly in the low frequency measurement.

2.3.1 Simulation model

Two types of sensors were simulated in our COMSOL simulation. This included a model of the sensor with electrode width value of 1 mm and length value of 3 mm which was the sensor electrode size we tested. By comparing the simulations, we could estimate the effect that the large pads had on the capacitance-pressure relation versus the smaller bond-wire pads. Given the smaller size of the bond-wire pads, there should be less static fringe capacitance for the bond-wire sensors and a greater change in capacitance to a change in pressure.

The two models were made by importing their .GDS file shape constructed from the mask-layout, converting the mask file into a 3D file effectively. Thickness of the sensors was modeled at 30um due to the limitations of the software, and a square slab of glass with dielectric constant 5 was modelled underneath it. Both electrode and pad configurations can be seen in Figure 2.13.

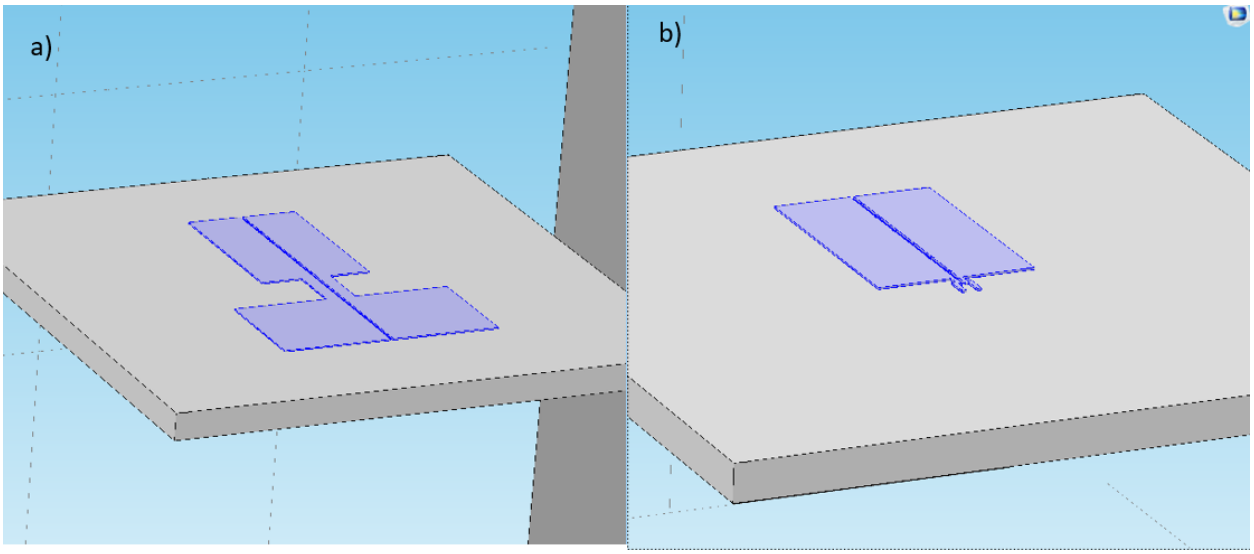

Figure 2.13: The two electrodes tested in COMSOL simulation software. a): The model with the 1 mm x 3 mm electrodes with 2 mm x 2 mm probe-pads. b): The model of the same electrodes, but with 60 µm x 300 µm bond-wire pads.

For simulating the bridge, the bridge was simply modeled as a rectangular slab of PDMS 1cmx1cm, with a thin circular coating of gold underneath it 5mm in diameter, and thickness 30um. The slab was given a dielectric constant of 2.67, which is the dielectric constant given for the PDMS solution we used for the fabrication, discussed in Section 2.2. The reason for the circular shape of the underside was to replicate the circular shape fabricated in Section 2.2.

2.3.2 Simulation environment

To simulate the devices in the COMSOL environment, the AC/DC Electrostatics COMSOL module was used. Using this model, the DC capacitance of a two terminal device can be simulated. For this simulation, the surface of one of the electrodes was modeled as the + terminal with a voltage of 1 V, the other electrode was modeled as the – terminal being connected to GND, and the conductive circular portion of the bottom of the bridge was modeled as a free-floating conductive potential. Thus, from this the DC capacitance can be simulated and calculated.

2.3.3 Simulation tests

Fringe capacitance

For the fringe and pad capacitance, to simulate this value the floating plate is removed from the simulation, and any capacitance measured should be between the two terminals. The factors that will affect this value will be the size of the electrodes, the distance between the electrodes in the lateral direction, the thickness of the electrodes, and the dielectric permittivity value of the substrate beneath them.

Floating plate: lateral movement

As discussed in Section 2.2, we expect that if either the electrode area changes or the lateral overlap of the floating bridge plate relative to the glass-electrodes changes, so should the capacitance. This simulation data should show that the placement of the bridge can be used to change the variable capacitance factor C_{Float} if needed to tune a device without changing the inductance or resistivity of the sensor. We also changed this lateral movement in experiment to demonstrate this effect, as previously discussed.

To test this, we added the floating plate to the simulation at a gap distance height of 90um, and simulated it at 100% lateral coverage (the floating plate is suspended above the two electrodes with 100% coverage), 50% lateral coverage (the floating plate is suspended over 50% of the electrode), and 0% lateral coverage (the floating plate is not directly over the electrodes at all.

Instead of simulating the amount the bridge would compress in response to pressure, we simplified the model and simply changed the gap distance *D* from Figure 1 between the conductive bottom of the bridge and the gold electrodes in the range of 90 µm to 10 µm, in 10 µm increments. This gap distance corresponds to the range of distance we expect the gap to exist in, from 90 µm being the static distance with no pressure applied, and 10 µm being the closest reliable distance the bridge could compress. While this means we do not know the exact response of how pressure relates to a change in capacitance, if future simulation or experimental work can find the relation between pressure and gap distance then the simulation work can link capacitance to pressure. This vertical simulation was done at the 100%, 50%, and 0% lateral coverage previously simulated.

Induction simulation approximation

Finally, the induction of the sensor is important to the operation of our capacitance-to-digital converter in Chapter 3. While ideally, we would like to simulate the inductance with the floating plate and

electrodes in the time and frequency domain, we found this very difficult to do in COMSOL. For COMSOL to simulate inductance, we found that the current had to flow from the + terminal to the – terminal of the electrode in a continuous path. As our circuit is inherently open circuit from + to – terminal, we decided to connect the two electrodes at the end farthest away from the pads, and simulate the current going around in a loop to get an estimate of inductance without considering the floating middle plate. This can be shown in Figure 2.14.

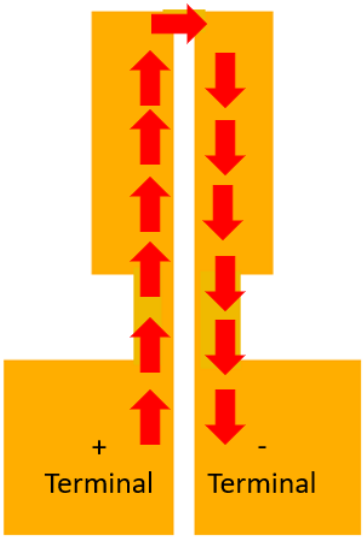

Figure 2.14: The model used to estimate the inductance of our sensor. In simulation a current was injected from the + terminal to the - terminal through the longest path between them at the ends of the electrode. This gives us an order of magnitude estimation of the inductance the device should have.

2.4 Results and discussion:

2.4.1 Experimental results

The results from the experimental data are shown in Figure 2.15 below. The linear response of the sensor indicates that it's a good candidate for pressure sensing. The slop of the curves gives the sensitivity of our capacitive pressure sensors, which is 4.6 fF/kPa for the device with 100% coverage.

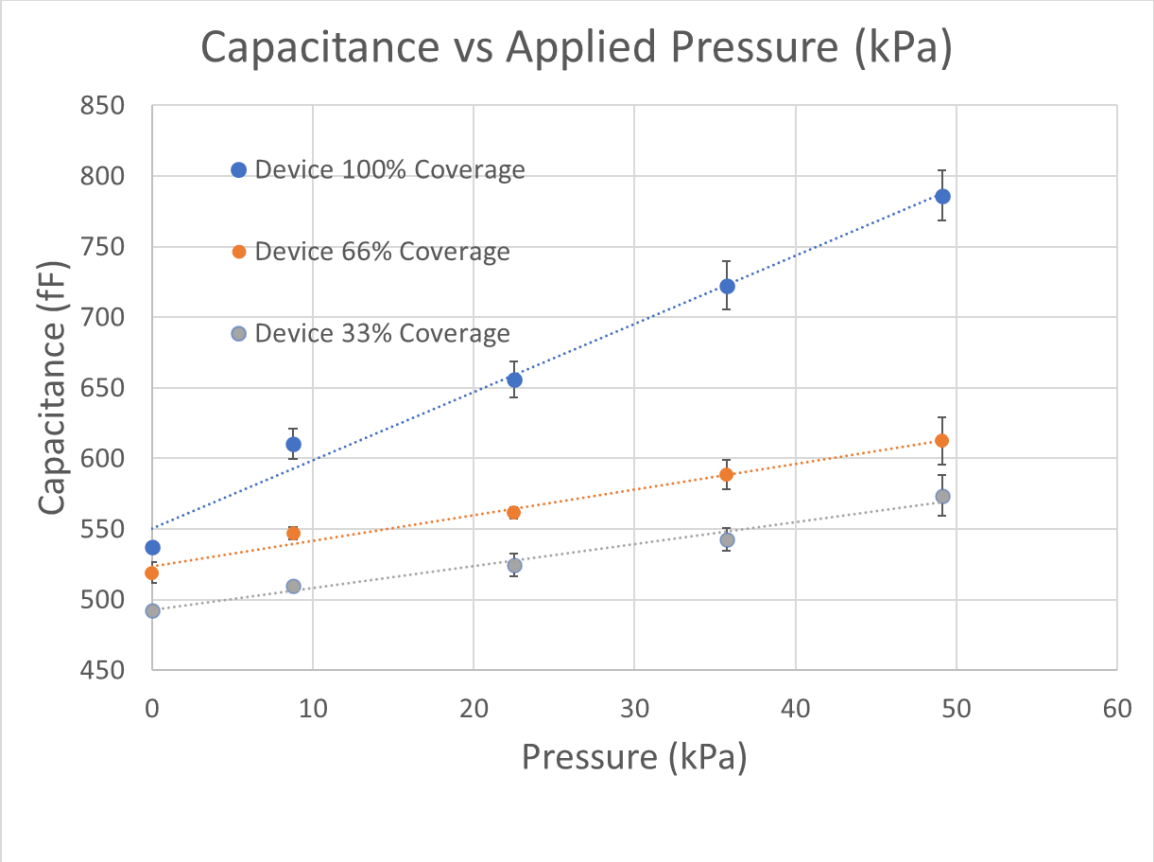

Figure 2.15: Capacitance vs Pressure for 3 different lateral positions. 9 samples were taken at each pressure point from which error bars were calculated. As less of the bridge is overtop the electrodes, capacitance goes down.

2.4.2 Simulation results

Capacitance simulation results

The simulation results are shown below in Figure 2.16, for both the probe-pad sensors and the bond-wire sensors at 100% lateral coverage, 50% lateral coverage, and 0% lateral coverage, with a downwards ΔD displacement between 0-80 µm in 10 µm increments (or in other words, simulated at a gap height D between 90 µm to 10 µm in 10 µm increments).

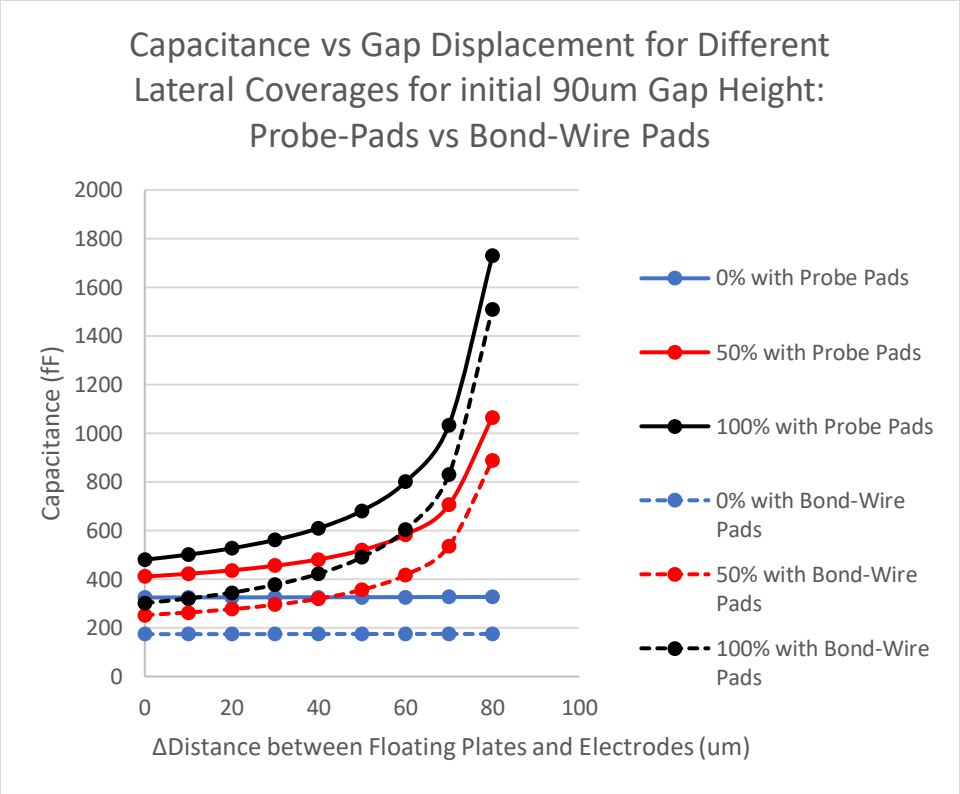

Figure 2.16: Simulation results for gap decrease from 0 to 80 µm (initially starting at 90 µm) for three different overlaps, with two types of devices.

Inductance simulation results

From our inductance simulation, we found that our electrode design should have an inductance of 1.89 nH if the current is forced to loop around the electrodes over the longest path. While this is only an estimate, we can reasonably conclude that the sensor can have an inductance between 1-10 nH, which is low enough for the sensor in Chapter 3.

2.4.3 Simulation vs experimental

Comparing the static fringe capacitance for the probe pad sensors with the bridge and without, the simulation and experimental results are compared in Table 2.1 below.

Sensor Type	Capacitance of Experimental	Capacitance of Simulation	% Error
With Bridge	537fF	480fF	10.6%
Without Bridge	465.2fF	327fF	29.4%

Table 2.1: Comparing the capacitance results between experimental results and simulation results for the 1mmx3mm sensor, both with and without the bridge over-top.

As can also be seen from Figures 2.15 and Figures 2.16, both in simulation and from experiment the capacitance changes with pressure or decreasing gap size. However, as we could not measure the gap size for each pressure point, we cannot compare the curves directly.

As can be seen from Table 2.1, there is a slight difference in measured amounts for the static capacitance with and without the bridge, at 10.6% difference between measured and simulated with the bridge overtop the electrodes, and 29.4% with just the electrodes alone. Two possible reasons are discussed below.

Instrument offset

First, if there was a static capacitance introduced by the instrument that was not properly calibrated for, we should expect slightly more capacitance in our measured results, as we'd be measuring the instruments and sensors capacitance.

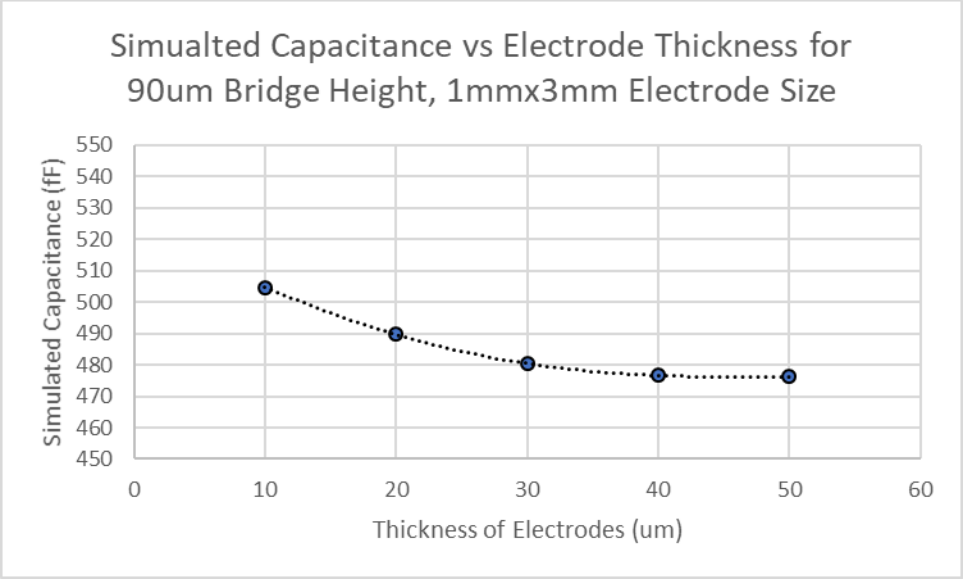

Figure 2.17: A plot showing the capacitance vs the thickness of the electrodes modelled. As the simulation thickness decreases, the capacitance values increase.

Second, in COMSOL, doing simulation of thin-film 3D structures can be challenging if the thinness of the device is much smaller than the width or length due to the mesh-construction. In this case, we found that simulating the electrodes below 10 µm led to COMSOL being unable to make a mesh or requiring more computer power than could be provided to finish the simulation. Thus, while our real-devices would be expected to have electrodes thinner than 1 µm, our simulations were forced to simulate the gold-electrodes on the glass and the conductive bridge bottom plate as having a minimum thickness of 10um, and for efficient simulations a thickness 3x larger of 30 µm was used.

Given that our simulation was using a thickness 10-30x thicker than the devices we actually tested, we did a sweep of our models at several thicknesses and noted how the capacitance and other measured values changed as the thicknesses approached the 1 µm thickness. From this graph, shown in Figure 2.17, we can see how as the thickness approaches the actual thickness of 200 nm, the capacitance changes significantly. This too could also be a reason for the difference in measurement and simulation – our simulation would need to be much thinner to accurately model our sensor.

2.5 Conclusion

In this work, we fabricated and characterized a microstructure based capacitive pressure sensor. Based on experimental data and simulation results, we believe that we have demonstrated a capacitive pressure sensor with a tunable capacitance range that could be connected to the closed-loop PLL circuits developed and discussed in Chapter 3.

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Chapter 3: Time-domain capacitance sensing

3.1 Passive resonator

3.1.1 Passive LC resonator

There are several ways of designing a capacitance-to-digital circuit using time-domain properties, with one of the most common ways being converting a capacitance change to a frequency difference through the use of a resonator. From electrical point of view a resonator is a combination of inductor and capacitor. Usually they are often placed in parallel as shown in Figure 3.1.

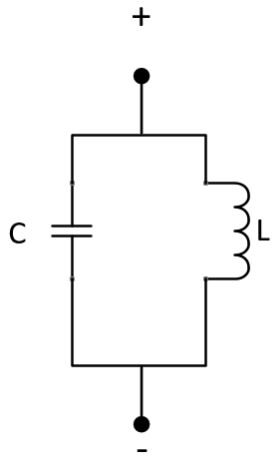

Figure 3.1: An Ideal LC Resonator

If the reactance for an inductor is given by:

$$XL = 2\pi fL \quad (3.1)$$

And the reactance for a capacitor is given by:

$$XC = \frac{1}{2\pi fC} \quad (3.2)$$

Then, equating them to find the f_0 resonance frequency where there impedances are the same we find the resonant frequency is

$$2\pi f_0 L = \frac{1}{2\pi f_0 C} \rightarrow f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (3.3)$$

As well, we can qualitatively see how changing the capacitance of the capacitor in the resonator will change the intersection between its reactance and the inductor's reactance, thus changing the resonant frequency. If this resonance frequency can be measured, the capacitance value can be discovered. This can be shown in Figure 3.2.

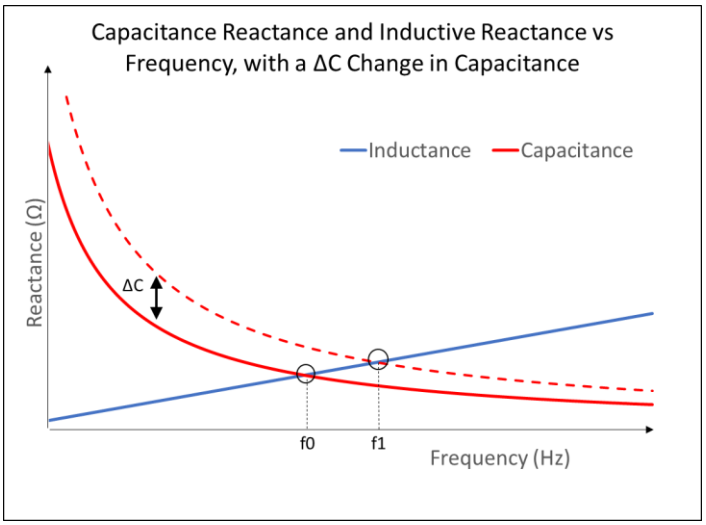

Figure 3.2: A delta C leads to a change in resonance frequency from f0 to f1

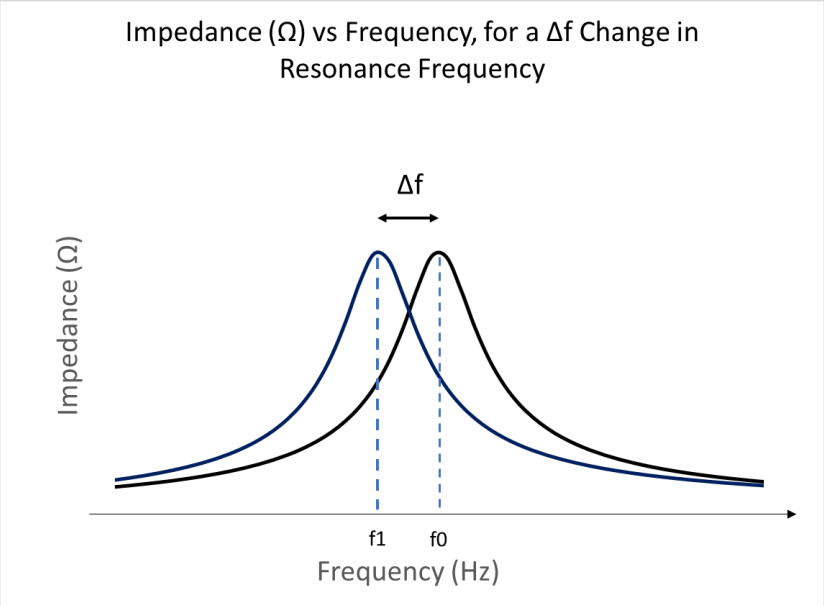

Figure 3.3: A delta f caused by a change in capacitance will lead to a change in resonance frequency, but if the Q is too low the frequency may not be distinguishable due to frequency spread.

Note that in microwave passive sensors this principle is often adopted where the resonator is built as a combination of transmission-line based inductors and capacitors [*1, 2*]. Regardless of the implementation, their measurement suffers from two main issues. First, there is no simple way to determine the shift in the resonant frequency – in most cases the VNA is used to sweep the frequency to generate the impedance profile. Obviously, such approaches are not cost-effective portable solutions. Second, the loss mechanism makes shift in the peak hard to determine, as shown in Figure 3.3. Below we explain how the loss mechanism affects the sensing.

While it may seem arbitrarily easy to form a capacitance-to-frequency converter using ideal capacitors and inductors as shown in the previous section, in the real-case the capacitor and inductor will have unavoidable parasitic resistances. Primarily, given current manufacturing technology for silicon

semiconductor circuits, the inductor unfortunately has considerable resistance that cannot be avoided. Thus, a real-world resonator will more resemble the LCR circuit shown in Figure 3.4 below:

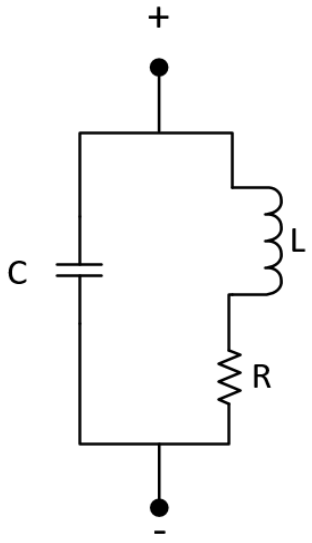

Figure 3.4: An RLC circuit that represents the parasitic resistance that is present in the inductor, which affects QL and performance of the oscillating circuit.

For purposes of analysis, this resistance can equate to a resistor in parallel with the capacitor and inductor, as shown in Figure 3.5:

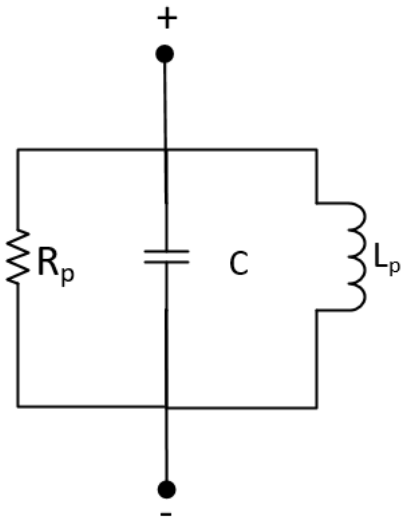

Figure 3.5: Equivalent RLC parallel model for a real-world LC resonant circuit.

Where R_p is the equivalent parallel resistance, and L_p is the equivalent parallel inductor. If we define quality factor Q_L as:

$$Q_L = \frac{\omega L}{R} \quad (3.4)$$

And define ω as:

$$\omega = \frac{f_0}{2\pi} = \frac{1}{\sqrt{LC}} \quad (3.5)$$

We can then define R_p and L_p as:

$$R_p = \left({Q_L}^2 + 1\right) * R \quad (3.6)$$

$$L_p = \left(\frac{1}{{Q_L}^2} + 1\right) * L \approx L \quad (3.7)$$

Qualitatively, this tells us that if our inductor is designed well and has low resistance (giving us a higher quality factor), the equivalent parallel resistance should be much larger than the series resistance, and vise-versa.

Quality factor, as described above, is very important in LC resonator and oscillator design. While it is a way of describing the quality of the inductor used and resistance, it can also be defined as the amount of energy lost per cycle compared to the amount of total energy per resonant cycle. This is important for the discussion of continued oscillation and phase noise in section 3.2 and 3.3.

For the resonator, it also affects the spread of the resonance frequency. While an ideal LC oscillator should resonate at a single frequency, with the addition of a resistor the power is absorbed by it leads to a resonation at different frequencies. The Bandwidth of this spread is given by:

$$BW = \frac{f_0}{Q_L} \quad (3.8)$$

Where BW is the frequency is the range of frequencies over which at least half of the maximum power and current is as compared to the peak amplitude at the resonance frequency (assuming a current source is provided to the resonator). Alternatively, it is the range of frequencies where the impedance is 70.7% of the peak impedance, as shown in Figure 3.6 below:

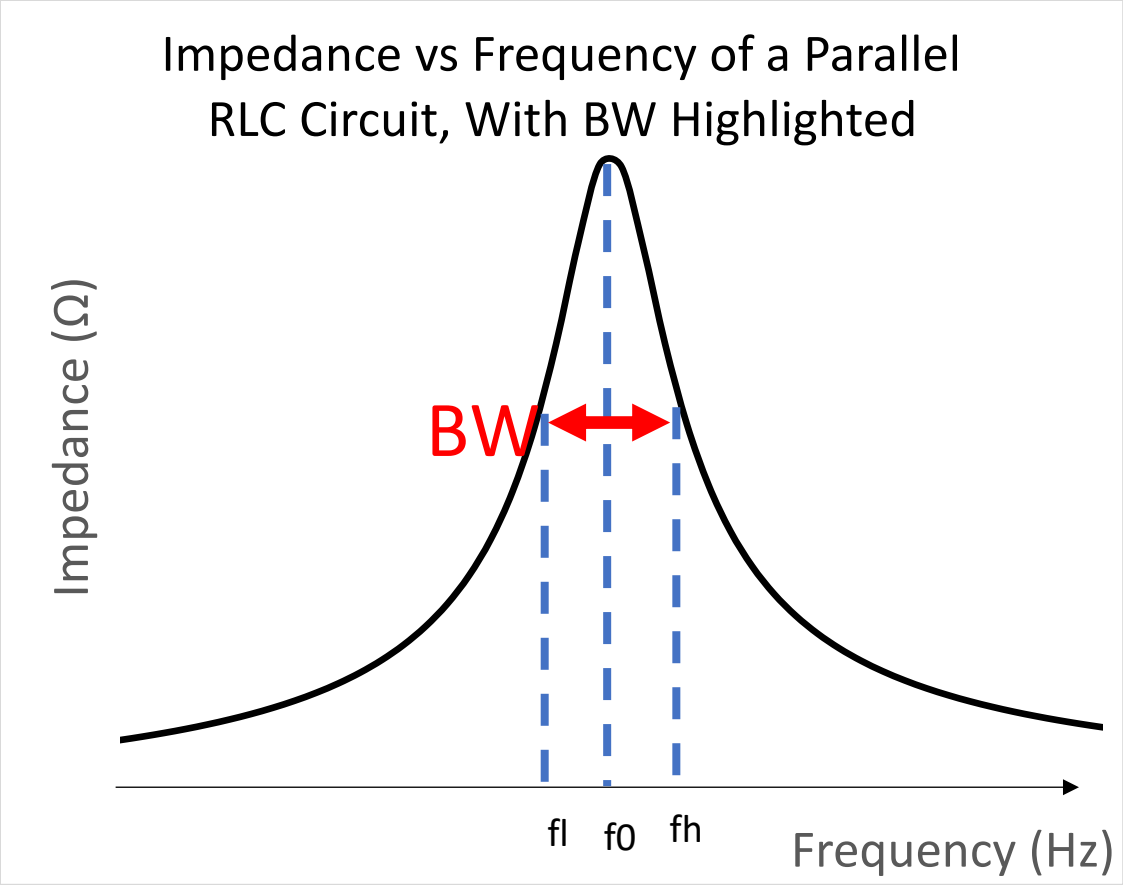

Figure 3.6: Impedance vs Frequency of a Parallel RLC Circuit, showing how the BW is defined between the corner frequencies fl and fh, around center frequency f0.

Thus, with increased resistance the BW of our resonator increases, and the ability for us to differentiate between two different frequencies for two different capacitance values decreases.

Another issue introduced by the parasitic resistance in an LCR resonator is that if we initially charge the capacitor and let the LCR circuit oscillate, the resistance will bleed off energy over time and cause the oscillation to stop, like a ticking grandfather clock losing energy due to friction, as shown below in Figure 3.7.

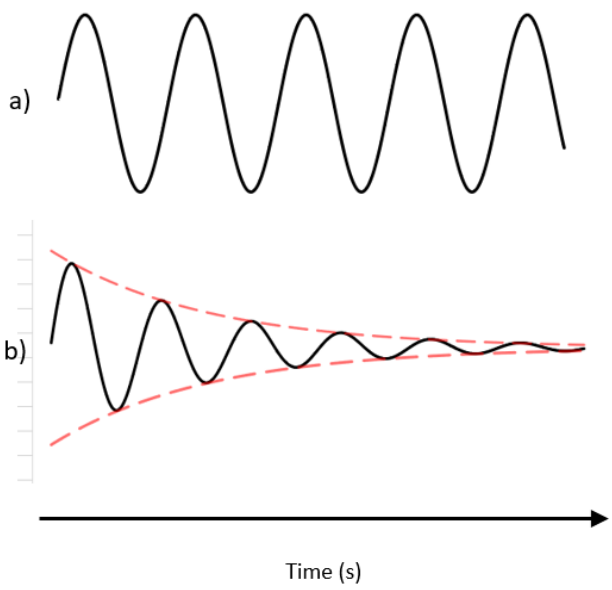

Figure 3.7: Voltage output over time for: a) an ideal LC resonator oscillating with no resistance given an initial charge b) a real-world LC resonator with resistance, causing the oscillation to die out overtime. The dashed lines represent the exponential decay.

Thus, from a practical viewpoint any frequency signal we wish to measure will eventually disappear as it dies out, and if a circuit is developed to 'recharge' this circuit continuously, power consumption will increase as resistance does.

3.2 Active LC resonator loss compensation

3.2.1 Negative resistance and sustained oscillation

To counter the decay in oscillation caused by the resistor and to keep the oscillator oscillating, while also improving the Q factor by increasing power at the resonance frequency, negative resistance must be added to the LC circuit to remove the resistance. As passive negative resistors do not exist in the real-world as that would imply infinite energy, active circuits that replicate negative resistance must be used instead. In a typical LC Tank Oscillator, negative resistance is supplied by a negative differential cross-coupled CMOS pair, showed in 3.8 and it is assumed that power is supplied through a tapped inductor connected to VDD. When energy is lost as current passes through the capacitor or inductor the cross-

coupled NMOS transistor pair supplies 'extra' energy from the VDD power supply and replaces the lost LC energy, thus sustaining the oscillation.

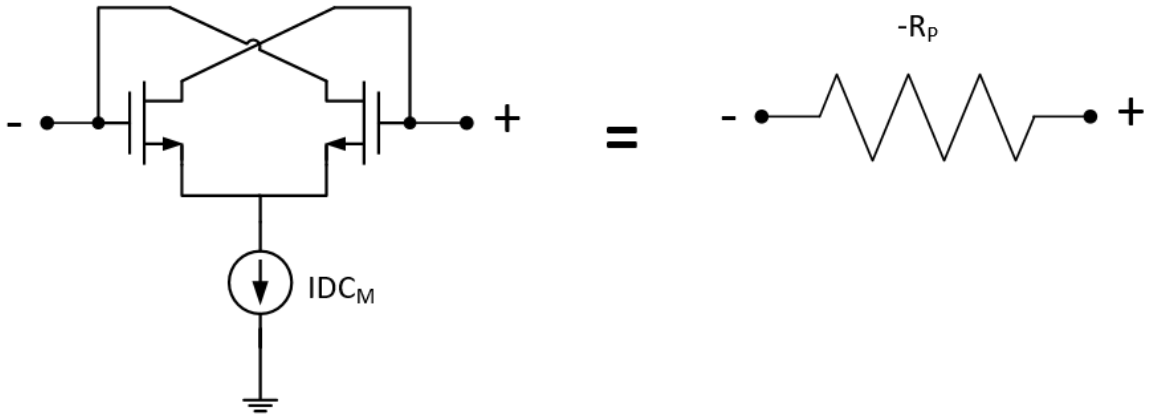

Figure 3.8: A cross-coupled transistor pair with a current source is equivalent to a negative resistor from node to node. The value of negative resistance will be determined by both the gm of the transistors and the current source IDCM .

Thus, by adding a cross-coupled NMOS pair to the LC tank, we can effectively add negative resistance, where the energy lost to the resistor is replaced by that of the cross-coupled NMOS transistor pair. The equation for what the value of the negative resistance is given by:

$$-\frac{2}{g_m} \quad (3.9)$$

Where g_m is the transconductance of the transistor.

Adding the negative resistance, we can now visualize the LC oscillator tank as being all parallel components, as shown in Figure 3.9.

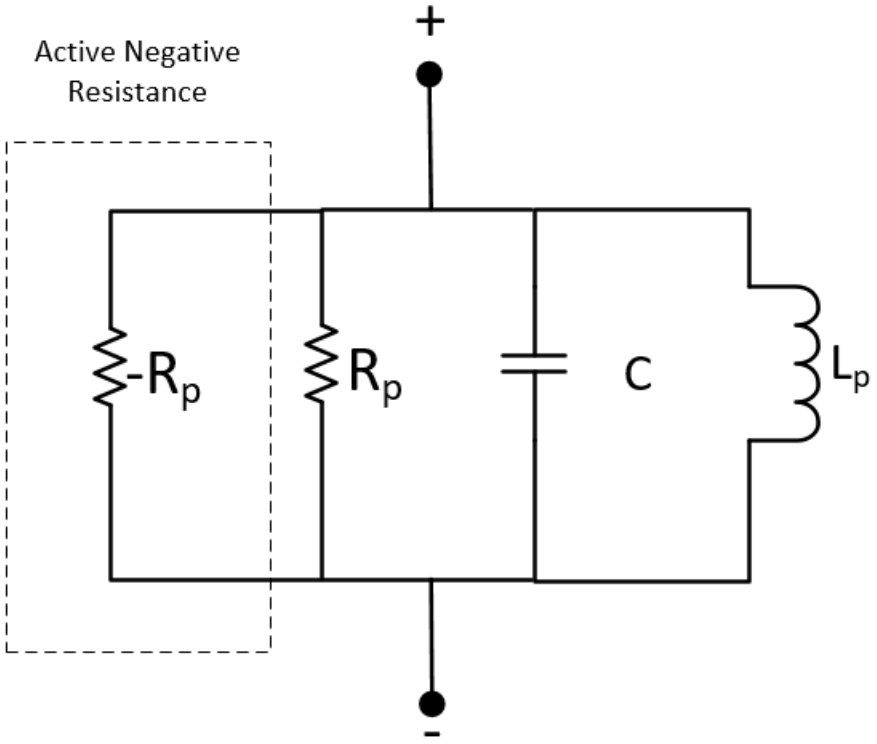

Figure 3.9: LCR oscillator with negative resistance added, to sustain oscillation.

Once the active negative resistance exceeds the resistance R_P, which requires sizing the cross-coupled transistors sufficiently wide enough so as to increase gm, the circuit not only can sustain oscillation but will naturally begin to oscillate on it's own at approximately the frequency given by equation (8). Thus, an oscillator is formed.

3.3 Open loop LC oscillator

Negative resistance and phase noise

The second major disadvantage to a high inductor resistance and a low Q_L quality factor is that of the introduction of phase noise, which is the more fundamental disadvantage. As the electrons in a resistor essentially do a 'random walk' at all times, producing thermal noise even when no power is

applied to a resistor, it will produce thermal electrical noise, which appears as random voltage fluctuations.

Given that an ideal LC oscillator is a charged capacitor dispensing it's energy into an inductor, and then the inductor giving it back in a continuous cycle, random fluctuations in voltage and current caused by the introduction of a resistor's random thermal noise effectively causes the cycle to 'fast-forward' or 'rewind' randomly, if the circuit is in a position due to ISF. This leads to a situation where the frequency does not produce a pure sinusoidal signal with a single frequency, but instead a spread of frequency, as shown below in Figure 3.10.

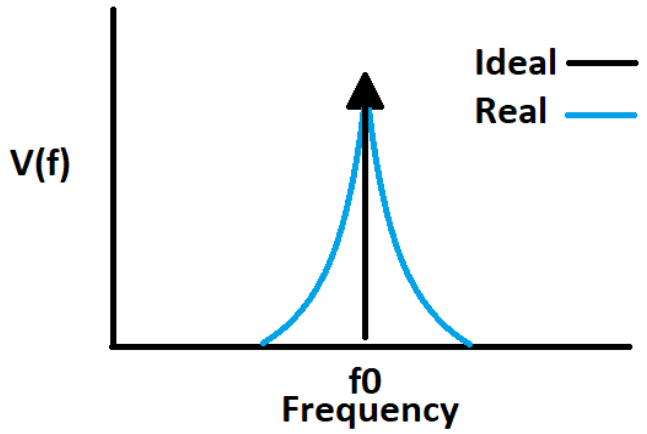

Figure 3.10: Ideal vs Real Oscillation, where in a real oscillator the frequency is instead a spectrum around resonant frequency f_0.

What this implies is that even if the LCR oscillator's sinusoidal output did not decay, the output signal we expect would be influenced by the noise produced by the resistor thus making our output frequency signal statistically centered around the frequency center-point, but not necessarily that frequency at any given point in time. Essentially, just as capacitive-to-digital converters based in the voltage domain suffer from noise, so to do time-domain circuits, which is not a surprising conclusion.

Despite the addition of active negative resistance to our oscillator, the phase noise issue has not been resolved. This is due to the transistors themselves, where the NMOS transistors will introduce flicker

and thermal noise of their own, similar to the resistor. And, given that the active negative resistance and the resistance of the LC tank are uncorrelated, we have introduced new noise to the system. This noise can be represented by I_{RN} and I_{AN} in parallel with the noise, where I_{RN} represents the resistor noise and I_{AN} represents the active noise, shown below in Figure 3.11.

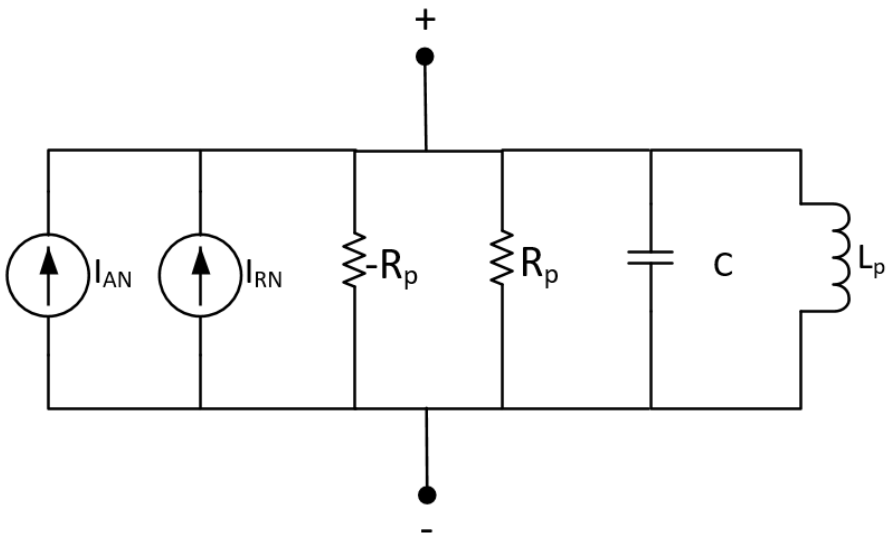

Figure 3.11: An LCR oscillator with negative resistance added through a cross-coupled NMOS pair. Both the resistor and active device add noise to the system, represented by current sources I_{RN} and I_{AN}.

This can be more formally described using Leeson's equation, a commonly used semi-empirical model used to describe RLC oscillators since 1966 [*3*], which is given by:

$$10\log\left[\frac{1}{2}\left(\left(\frac{f_0}{2Q_l f_m}\right)^2+2\right)*\left(\frac{f_c}{f_m}+1\right)*\left(\frac{FkT}{P_s}\right)\right] \quad (3.10)$$

Where:

f_0 is the output frequency,

Q_l is the loaded quality factor,

f_m is the offset from the output frequency (Hz),

f_c is the 1/f corner frequency,

F is the noise factor of the amplifier,

k is the Boltzmann's constant in joules/kelvin,

T is the absolute temperature in kelvins,

P_s is the available power at the sustaining amplifier input.

While there are many aspects to this equation, for the relevance of this thesis this tells us that the quality factor directly correlates with phase noise, and by improving it we should expect better phase noise performance. As well, it shows that the noise factor of the amplifier (in this case the negative resistance provided by the two cross-coupled NMOS transistors) linearly affects the phase noise performance, and since we cannot remove this noise completely from the transistors we cannot remove phase noise from the LCR oscillator we have described. Thus, a free-running 'open-loop' LCR oscillator with active resistance as we described will never be able to provide a pure sinusoidal frequency output, lowering the resolution of any circuit that is meant to convert this frequency signal into a digital output for the purposes of capacitance measurement.

3.4 Closed loop LC-VCO oscillator – the phase-locked-loop

Compared to open loop systems, closed loop or feedback systems are less susceptible to external noise. In VCO based capacitor sensors we have there is a unique advantage of the close loop VCO based sensors compared to open loop VCO based sensors. Given the relationship between capacitor and oscillation frequency, any sensor capacitance change translates to frequency change in a nonlinear manner. In an open loop system, we need to calibrate for the nonlinear transfer but in a close loop system, frequency change remains within a very small fraction where the curve is linear. This is because feedback loop changes the digital cap array to such that the frequency remains in its nominal value. Close loop systems are mostly built using PLL, below we will provide necessary background for that:

3.4.1 Phase-locked-loop fundamentals

Fortunately, as in most all systems that suffer from noise, the noise of the LCR oscillator that has been described can be reduced using a negative-feedback control loop. The reference this control loop is based off of is a more stable oscillating frequency source which is typically a crystal oscillator, a crystal oscillator being an oscillator system based on the mechanical vibrations of a quartz crystal when electricity is applied to it. While the quality factor of the LCR circuit we described is typically in the range of 5-30[*4*], crystal oscillators can have a Q value between 20,000-200,000, and even higher in specialty applications if required. Thus, while current technology cannot form a crystal oscillator whose frequency changes in response to the capacitance of a capacitive-sensor at this point in time with such a high Q factor (and thus low phase noise), one can use a crystal oscillator as a stable frequency reference to stabilize the phase noise of a more noisy LCR oscillator given additional circuitry.

One of the best and most ubiquitous techniques to correct a noisy oscillator (such as an LCR oscillator) with a stable oscillator (such as a crystal oscillator) so as to decrease phase noise in the noisy oscillator is a feedback loop known as the Phase-Locked Loop (PLL). A PLL is a circuit that outputs an oscillating signal whose phase is locked to an input signal. This inadvertently also produces an oscillating signal whose frequency is locked to an input frequency, as phase is the integration of frequency over time – a signal locked in phase is also locked in frequency. Phase locked loops have been used for decades to stabilize frequency signals, amongst other uses, and are an essential component in almost all circuit modern circuit design. This is shown in Figure 3.12:

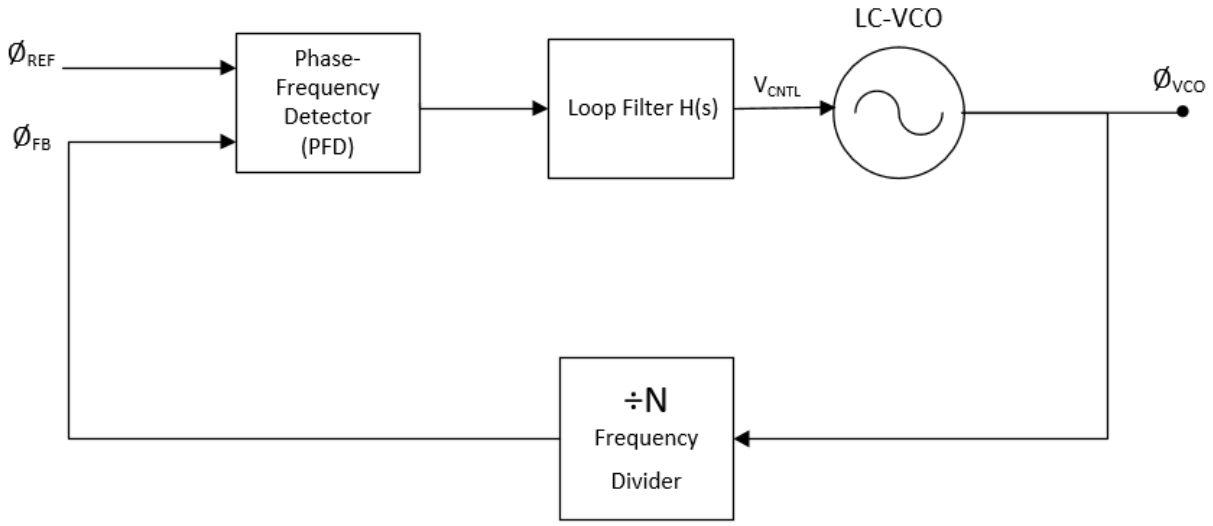

Figure 3.12: A typical Analog PLL. Note that the VCO does not have to be an LC type, but can be any variant that oscillates and can have its frequency changed by an input/inputs.

Almost all phase-locked loops operate on the basic negative feedback loop block diagram above. In brief, the VCO oscillator runs and outputs a sinusoidal signal with frequency F_{VCO} and phase $Ø_{VCO}$. This signal is divided by a frequency divider to a lower frequency, producing a phase signal $Ø_{FB}$, which is compared with the phase $Ø_{Reference}$. The resulting difference between them produces the signal $Ø_{Error}$ which indicates the deviation between the reference signal and the VCO, which is multiplied by a constant K_{PD}. This phase signal is then converted into a voltage V_{CNTL} through the use of a loop filter which is fed into the VCO, and changes it's frequency in a fashion so as to bring the VCO's frequency and phase back in line with that of the stable reference frequency, thus completing the control loop. The specifics of this will be expanded upon below.

Full 2nd order CP-PLL structure and S-domain equivalent

While the field of PLL design is large and complex, one of the more common and useful analog PLL designs is the Charge-Pump Phase-Locked Loop (CP-PLL). The CP-PLL is a second order analog variant of the phase-locked loop capable of stabilizing both phase and frequency for both frequency and phase

deviations, versus the type 1 PLL which can only correct for phase deviations, which is not discussed in this thesis. The CP-PLL is a popular design due to its theoretical offset zero static phase offset while also being simple and effective in operation [*5, 6*].

In the CPLL, the phase detector component consists of a Phase-Frequency-Detector (PFD) and a Charge-Pump (CP) combined together. The PFD quantifies the phase/frequency error between the reference $\emptyset_{REF}$ and the $\emptyset_{FB}$ output signal by producing a pair of digital pulses and comparing the positive or negative edges. The CP then converts the digital pulses into an analog current via a NMOS and PMOS switch. This current is then converted into a voltage via the loop filter, which in this case is a passive RC series low-pass filter, indicated by C_1 and R_1 above. For stability purposes, a second capacitor is added, C_2, to suppress voltage spikes. While the addition of the second capacitor C_2 produces a third order PLL which would imply stability issues, by making C_2 much less than that of C_1 ($1/10^{th}$) the value the system behaves fundamentally like a second order loop filter(reference). This control voltage, V_{CNTL}, is fed into the input of the VCO. Over time, this system will eliminate the phase error and frequency error present at the output of the VCO. Additionally, as is typical in all PLL designs, a frequency divider can be placed between the F_{VCO} signal and the PFD to instead compare the $\emptyset_{REF}$ signal with a divided signal F_{VCO}/N. This is for the purpose of generating a frequency that is faster than that of the Ref_{CLK}.

LC-VCO

If a control loop is to be designed to correct and minimize the phase noise of the LC oscillator that is meant to be used for the purposes of capacitance-to-frequency conversion, followed by frequency-to-digital conversion to form a capacitance-to-digital circuit, the LC oscillator must be modified so a control input can be applied to the oscillator to correct and return it to it's intended center frequency.

While there are many ways to do this, in the analog domain the input is designed to be a control voltage, V_{CNTL}, whose voltage is related to the output frequency linearly. If the voltage increases, the

frequency will increase, and if the voltage decreases, the frequency will decrease (the relation could be inverted, of course, but this is the typical implementation). This is typically done with a component known as a varactor, which is a capacitor whose capacitance is related to the input voltage. This is typically implemented using a diode, as the depletion region width between the P-N region is dependant on input voltage, and the depletion region is a crude form of a parallel plate capacitor. Thus, a LC Voltage-Control-Oscillator (VCO) is formed. Thus, a circuit is constructed that can convert an input voltage into a frequency output.

While LC-VCO's and VCO's in general are never truly linear over their whole range, in certain regions of their operation it can be a reasonable assumption to assume linearity. If it is assumed that the VCO being referenced is a single-input single-output VCO, we can relate the phase produced by it as an integration of the frequency:

$$\emptyset_{VCO} = \int_0^t (\omega_0 + K_{VCO} V_{cont}) dt \quad (3.11)$$

Where $\emptyset_{VCO}$ is the phase of the VCO output in radians,

ω_0 is the base frequency without any input.

K_{VCO} is the gain of the VCO and is a constant in radians/Volt,

V_{CONT} is the control voltage, in volts.

In the frequency domain, the integration presented above can be converted to:

$$\emptyset_{VCO} = \frac{K_{VCO}}{s} \quad (3.12)$$

Frequency divider

It is typical – but not necessary – to then divide the oscillating F_{VCO} signal produced by the VCO to a lower frequency using a circuit known as a frequency divider by an integer value N. As phase is the integration of frequency, this will also divide the phase $\emptyset_{VCO}$ by a similar amount as well. This is done as high Q crystal oscillators are in the range of 0.1-10MHz, while the frequencies produced by LC VCO's can

be in the range of 0.1-100GHz, potentially. Thus, to properly compare the high frequency VCO signal with the low frequency but low-noise crystal oscillator, the VCO frequency must be divided so that the divided frequency can be compared to the crystal oscillator.

Typically, dividers are implemented using chains of Flip-Flops, as shown below, where each D-Flip-Flop stage has half the frequency output as the last stage. For N stages, the frequency will be reduced 2^N times. This is shown in Figure 3.13 Using PWM techniques and switching between these divided frequencies, integer values of N can be produced that are not multiples of 2, but such techniques are not in the scope of this thesis.

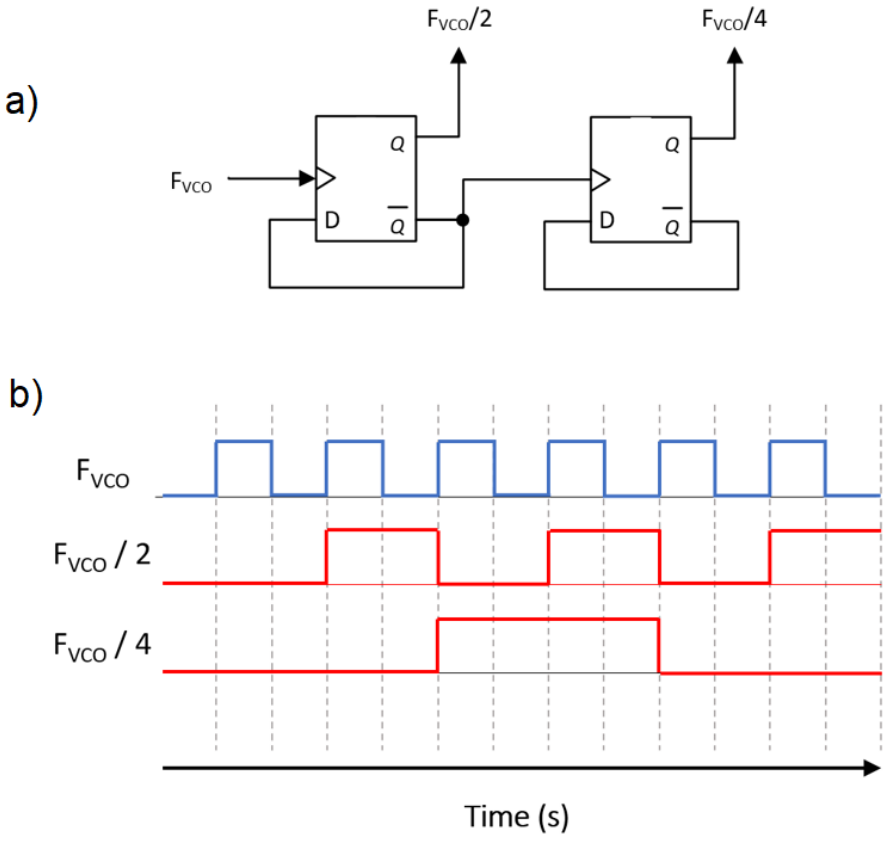

Figure 3.13: a) Two D Flip-Flop's connected in two stages to produce a divide by two and divide by four outputs, represented by $F_{VCO}/2$ and $F_{VCO}/4$ outputs respectively. b) example clock timing diagrams of input F_{VCO} vs output $F_{VCO}/2$ and output $F_{VCO}/4$, where each subsequent divide stage halves the frequency of the preceeding stage.

While each stage of the frequency divider will add its own noise due to jitter in rise and fall times, this can be solved by retiming the last stage with the original F_{VCO} signal, albeit at a significant power cost.

If a divider is used, the equation 3.12 simply becomes

$$\emptyset_{FB} = \frac{\emptyset_{VCO}}{N} = \frac{K_{VCO}}{sN} \quad (3.13)$$

Where N = the integer value the frequency is divided by.

Phase/frequency detector and charge pump

The divided sinusoidal signal F_{FB} with phase signal $\emptyset_{FB}$ must be compared to the reference phase signal $\emptyset_{REF}$ to determine the difference in phase between them and convert this into a linear signal. Just as a linear V_{CNTL} voltage signal is converted into a linear phase signal $\emptyset_{VCO}$, the linear phase error $\emptyset_{Error}$ must be converted back into a linear voltage. For the type 2 PLL being discussed, this is performed using a circuit known as a phase-frequency detector in conjunction with a charge-pump circuit. This is shown in Figure 3.14.

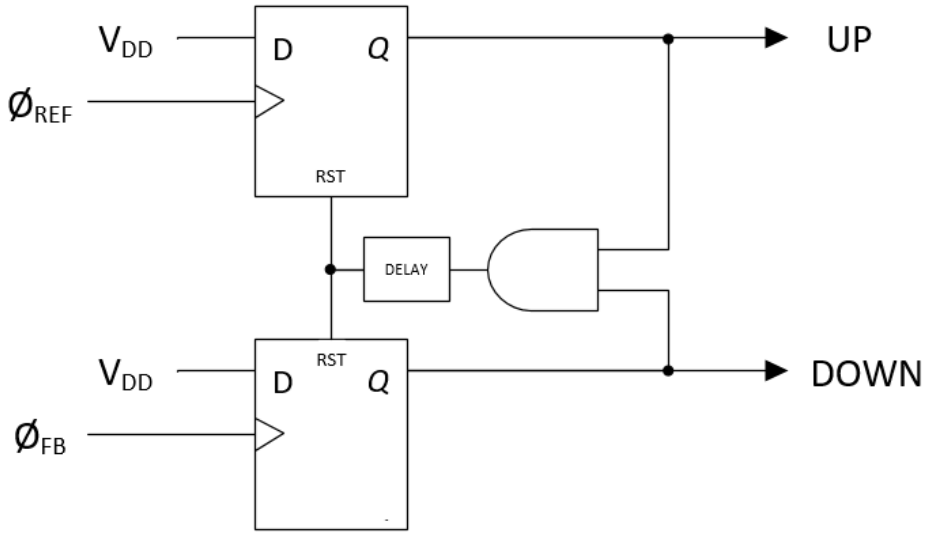

Figure 3.14: A Phase-Frequency-Detector formed from 2 D Flip-flops, 1 AND gate, and a delay component. When $Ø_{REF}$ leads $Ø_{FB}$ in phase, an UP signal is produced. When $Ø_{FB}$ leads $Ø_{REF}$, a DOWN signal is produced. Using these two signals, a charge-pump can be used to correct the VCO's phase and frequency.

There are many ways to form a phase-frequency detector, but the most common one in type 2 CP-PLL's is by using two d-flip flops, and an AND gate, and a delay function as shown below. Effectively, this circuit produces an 'UP' positive pulse when the reference signal is leading in phase as compared to the feedback signal, a 'DOWN' positive pulse when the reference signal is lagging in phase as compared to the feedback signal, and no output when they are both positive, provided by the AND gate clearing the D Flip-flop's outputs. The delay is necessary to avoid the production of harmonics, a concept known as 'deadbandwidth', and is not necessary to the fundamental operation of the device [*7*].

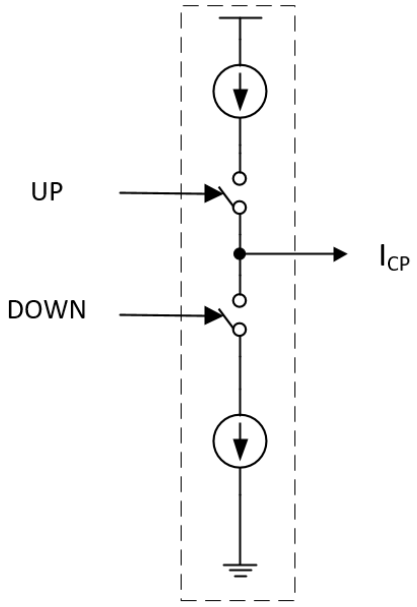

Figure 3.15: A Charge-Pump that uses the UP and DOWN signals from the PFD to produce the output I_{CP}. When the UP signal is high and the DOWN signal low, the output is charged with current from VDD. When the DOWN signal is high and the UP signal is low, the I_{CP} is drained of current to GND. With this, a voltage can be produced from a phase error if it is inputted into a low pass filter.

The 'UP' pulse and 'DOWN' pulse are then fed into a two-input, one-output device known as a charge-pump, consisting of a PMOS and NMOS current source that are switchable by the 'UP' pulse and 'DOWN' pulse respectively. When the 'UP' signal is high, the PMOS current source injects current into the output node, and when the 'DOWN' signal is high current is drained out of the output node. This allows a way to both add charge and subtract charge from the output respectively given the zero crossings of the reference and feedback signal. This is important, as it allows the circuit to correct for both frequency and phase, vs frequency alone.

Combining these two circuits, it can be interpreted as that the phase-frequency detector produces the phase error signal $\emptyset_{Error}$, which is then amplified by the charge pump into a useable signal by a factor K_{PD} , whose units are V/radian.

For the specific CPLL architecture, the K_{PD} is approximately:

$$K_{PD} = \frac{I_P}{2\pi} \quad (3.14)$$

By increasing the current used in the charge pump, the change in voltage produced by a change in phase error will increase. The output I_{CP} is shown in Figures 3.16 and 3.17 out of phase and in phase.

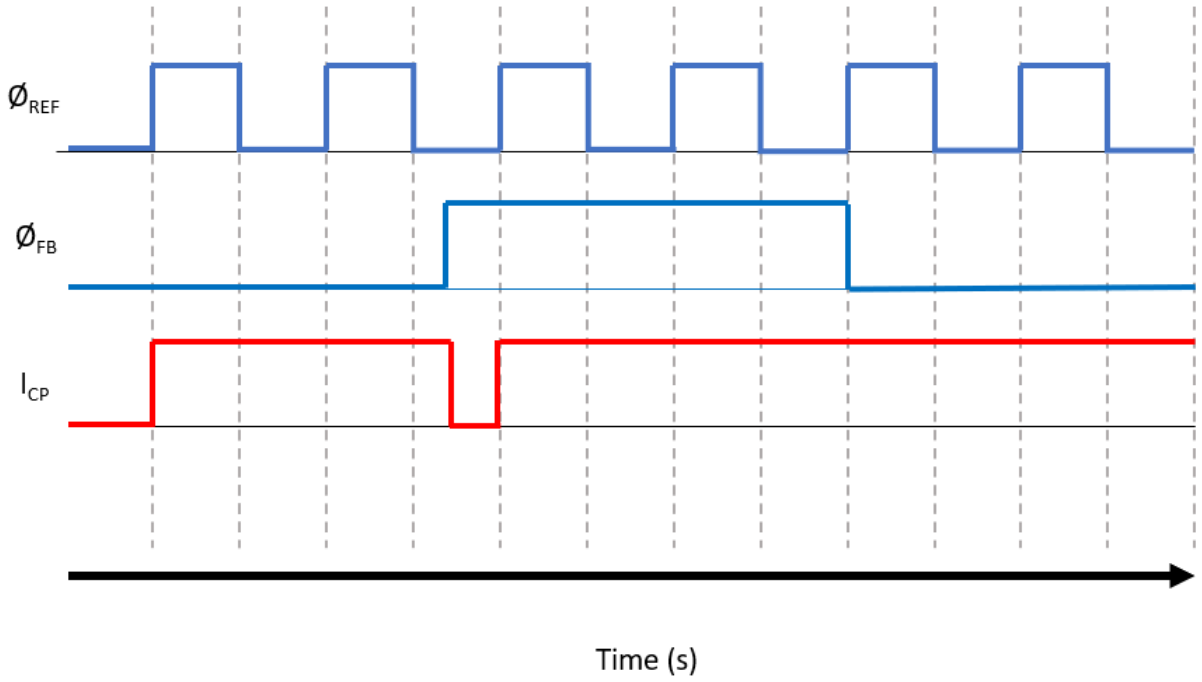

Figure 3.16: An example diagram of how if $Ø_{REF}$ and $Ø_{FB}$ are not aligned in phase due to a lower frequency present in $Ø_{FB}$, positive I_{CP} pulses will be produced, effectively 'speeding' up the frequency of $Ø_{FB}$ to match that of $Ø_{REF}$, as well as aligning phase. If the timing diagrams of $Ø_{REF}$ and $Ø_{FB}$ were switched, the same I_{CP} timing diagram would be produced, but with a negative $-I_{CP}$ magnitude value instead of a positive I_{CP} value.

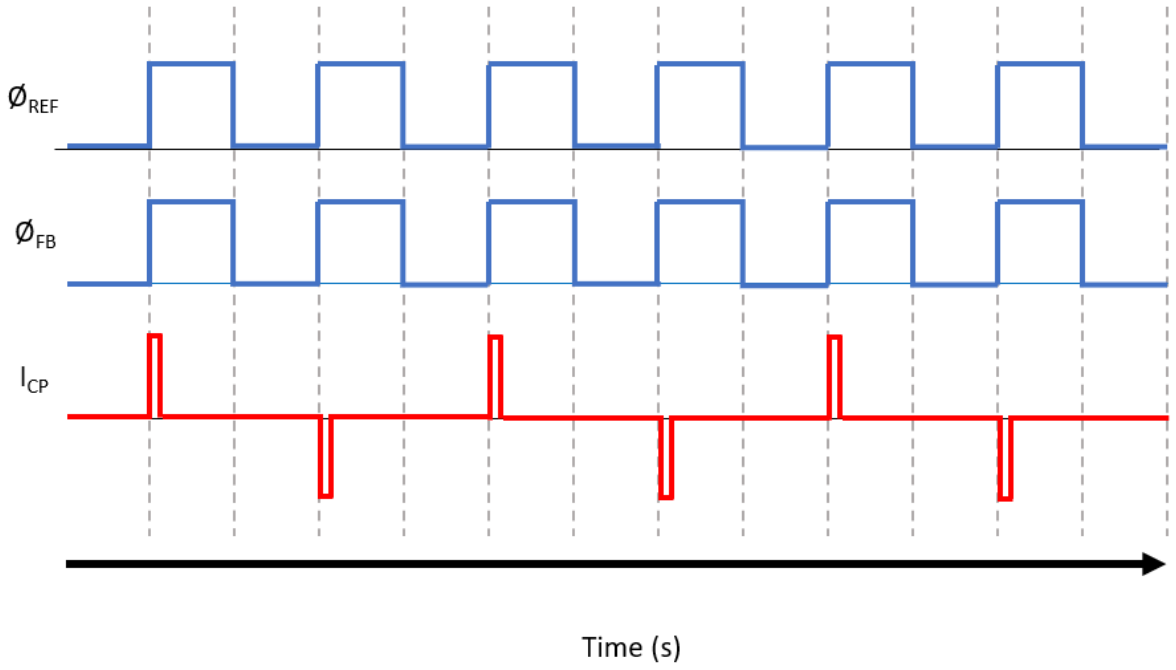

Figure 3.17: A timing diagram of the situation when Ø and are aligned and locked in phase and frequency. Due to the delay block, minute ICp positive and negative pulses are produced to avoid the 'deadzone' phenomena.

Loop filter

However, despite the relation between phase error being translated linearly into the injection and draining of current into the output node via the use of the charge pump, the output is a constantly changing high-frequency signal that is not the constant voltage V_{CNTL} signal needed to correct the VCO to it's proper phase and frequency. Thus, an analog loop filter is used to low-pass filter the charge pump signal into a useable V_{CNTL} signal.

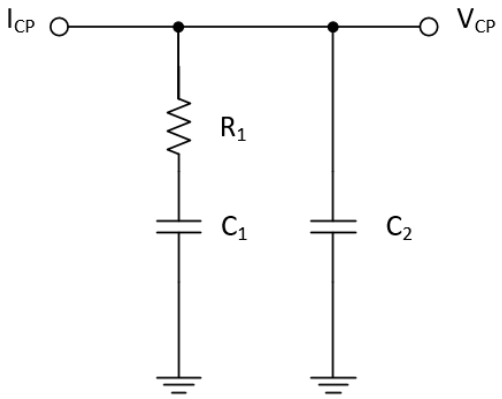

Figure 3.18: : A low-pass filter formed by R_1 and C_1 in series. For stability purposes, capacitor C_2 is added, usually being an order of magnitude lower than C_1 to avoid potential third order system difficulties[8].

A common and straightforward filter that is typically used is a series RC low-pass filter, as shown above in Figure 3.18, where a resistor R_1 and a capacitor C_1 are combined in series and connected to the charge-pump output node to produce the desired V_{CNTL} output voltage intended for the VCO. An additional C_2 capacitor is added for stability reasons discussed in later sections but is usually an order of magnitude smaller than C_1 and is not intended to greatly affect the low-pass filter properties[*8*].

The loop filter, which determines many properties of any PLL, is provided by a resistor R_1 and capacitor C_1 in series, to produce a low pass filter. This is necessary to low-pass filter the system and average out our control voltage by converting the injected I_P current into a voltage. The resistor R_1 is necessary due to the fact if it were not there and a lone capacitor was used to convert the current into voltage, the combination of the two integrators (the capacitor and the VCO) would lead to a 180° phase shift leading to an oscillating and unstable control loop. The resistor is necessary to decrease this phase shift below 180° at the gain crossover[*8*].

The loop filter in the phase domain can be represented as:

$$H(s) = R_1 + \frac{1}{C_1 s} \quad (3.15)$$

3.4.2 Capacitive sensing closed-loop CP-PLL

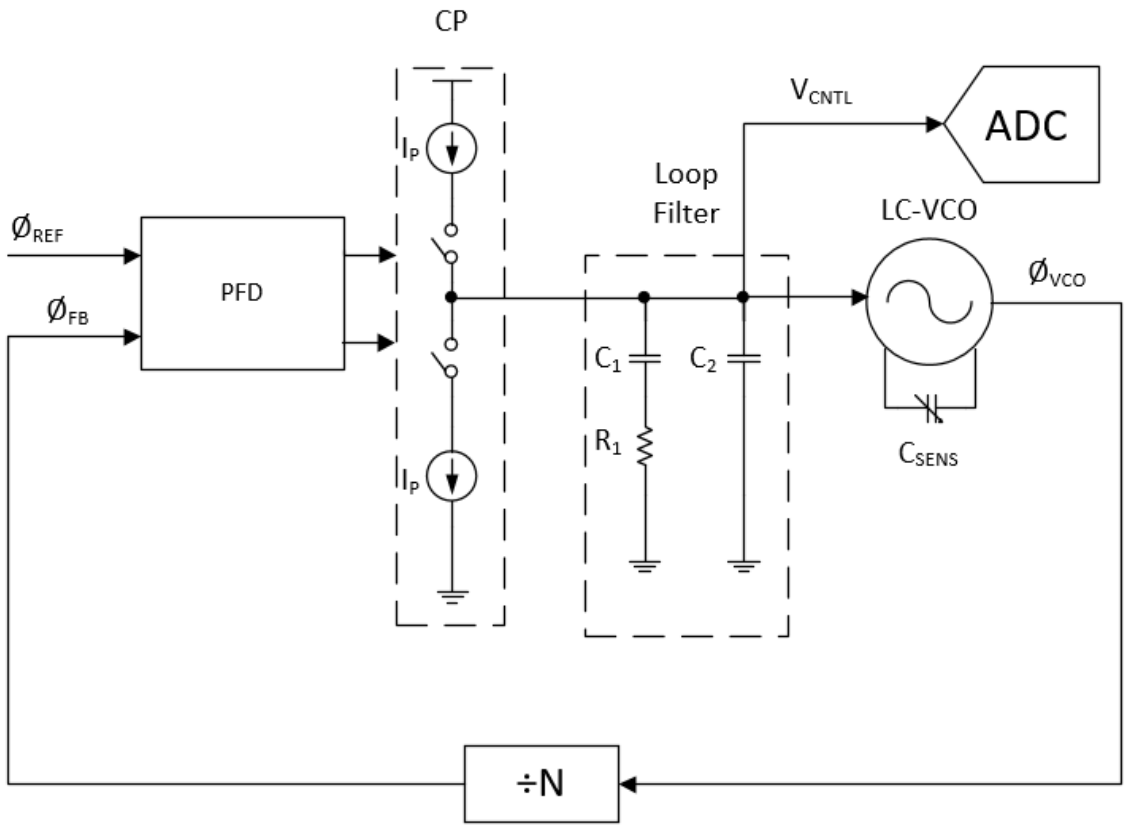

Figure 3.19: An analog 2nd Order Phase-Locked Loop (PLL) used in conjunction with an LC-VCO whose frequency can also be changed due ro the change in capacitance of a capacitive sensor hooked up to it, as well as a voltage ADC being used to measure the V_{CNTL} voltage for the purposes of capacitance-to-digital conversion, as proposed in [8]

If we modify our VCO to be a Capacitance-Voltage Controlled Oscillator (LC C-VCO) which has two input terminals that control the voltage instead of one – one input being a voltage control signal as before, while the new second input has a capacitor value as a signal input instead – we could take a variable capacitor sensor C_{Sens}, such as the one shown in Chapter 2, to make a PLL which responds to a change in sensor capacitance instead of voltage. If the capacitance of C_{Sens} changes value then the frequency of the VCO will change as well, which will be seen by the PLL as a phase-frequency error. The PLL will respond by changing the V_{CNTL} value to compensate and bring the VCO's F_{VCO} output back to its original frequency and

phase. If an ADC is placed on the V_{CNTL} pin, this change in voltage will be measured, and thus the capacitance change can be determined. Essentially, instead of measuring a change in frequency and converting this to a digital value directly in an open loop configuration, we instead measure the control signal required to counter the frequency changes caused by the capacitive sensor in a closed loop. This is the same method used in [*9*].

Disadvantages of analog PLL sensing and noise analysis

While the above circuitry is a legitimate way of forming a capacitance-to-digital sensor using time-domain techniques, there are several issues with it. From these two issues, it will be argued that a digital phase-locked-loop can avoid these issues and lead to better performance.

As discussed in Chapter 1, the first obvious disadvantage to using the analog PLL technique and measuring the V_{CNTL} pin to determine the capacitance value of our capacitive sensor is that capacitance has been converted into a frequency value in the time domain, but then is converted from a frequency signal into a voltage signal, thus effectively taking a longer route to yet again form a capacitance-to-digital circuit using voltage domain techniques. While there may be advantages such as not needing the pre-amplifier or other stability advantages, fundamentally this design has done nothing to address the pre-amplifier and comparator noise issues that are attached to voltage-based capacitance-to-digital conversion techniques.

The second issue is more theoretical and specific to phase noise suppression within the analog phase-locked loop system, which requires noise analysis in the s-domain and replacing the components with their s-domain equivalents, which is shown below.

3.4.3 S-Domain modelling of the CPLL and noise impact

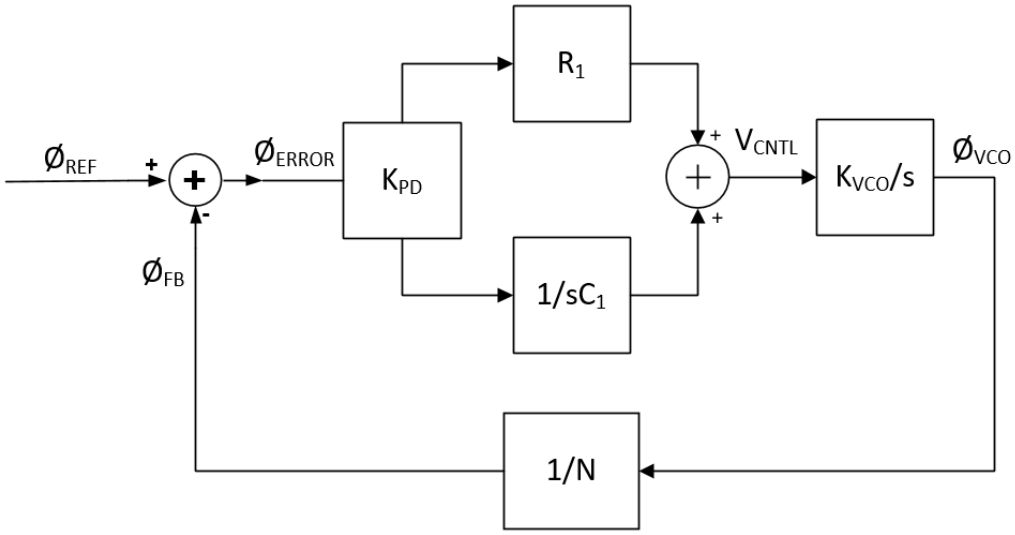

Figure 3.20: S-Domain Model of a 2nd Order CP-PLL control loop. Note that C2 is not included, due to the assumption C1 is much larger than C2.

While a second order CPLL is not a true linear system due to the pulse-edges produced by the PFD and the non-linear nature of many of the components, if the BW of the PFD is more than that of the PLL system it can be treated as such to produce a reasonable approximation [*8*]. The S-domain representation of the 2nd order CP-PLL is shown above in Figure 3.20.

The open loop transfer function from the $Ø_{Reference}$ to the output $Ø_{VCO}$ is:

$$\frac{Ø_{VCO}}{Ø_{REF}} = K_{PD} * H(s) * \frac{K_{VCO}}{s} = K_{PD} * \left(R_P + \frac{1}{C_1 s}\right) * \frac{K_{VCO}}{s} \quad (3.16)$$

If we define the forward path G as:

$$G(s) = K_{PD} * H(s) * \frac{K_{VCO}}{s} \quad (3.17)$$

And the feedback factor B as

$$B(s) = \frac{1}{N} \quad (3.18)$$

Then the closed loop transfer function should be equal to:

$$\frac{\emptyset_{VCO}}{\emptyset_{Feedback}} = \frac{G}{1+GB} = \frac{K_{PD} * G(s) * \frac{K_{VCO}}{s}}{1 + K_{PD} * B(s) * G(s) * \frac{K_{VCO}}{s}} = \frac{K_{PD} * \left(R_P + \frac{1}{C_1 s}\right) * \frac{K_{VCO}}{s}}{1 + K_{PD} * \left(R_P + \frac{1}{C_1 s}\right) * \frac{1}{N} * \left(\frac{K_{VCO}}{s}\right)} \quad (3.19)$$

As stated in sections 3.3, it is expected that the major source of noise in this control loop will appear at the oscillator, and it can be represented by a phase noise $\emptyset_N$ being added to the output phase $\emptyset_{VCO}$. As the purpose of this circuit for capacitance-to-digital conversion relies on measuring V_{CNTL}.

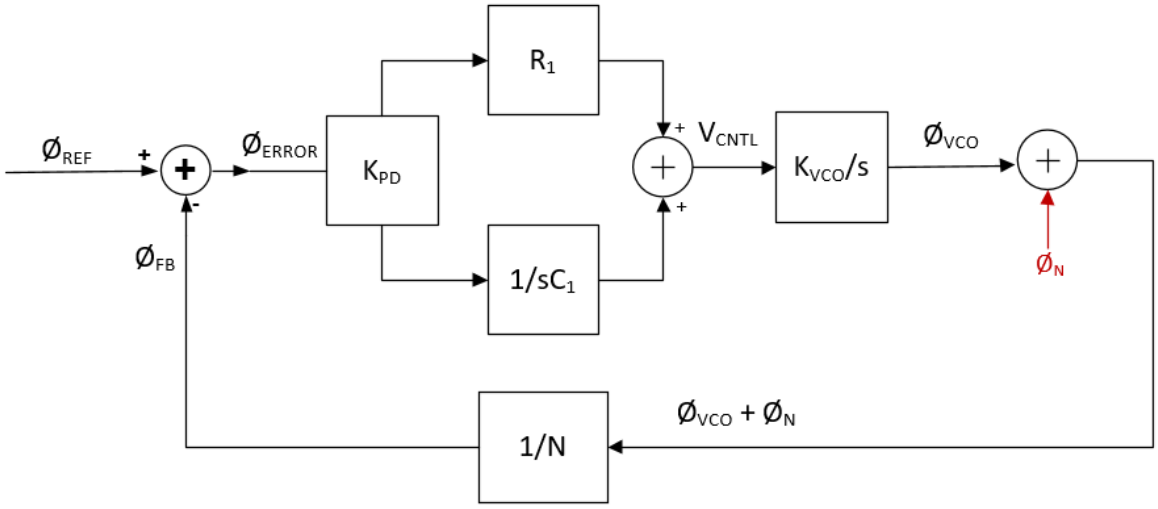

Figure 3.21: S-Domain model of 2nd order CP-PPL with noise source $\emptyset_N$.

$$\emptyset_{OUT} = \emptyset_e K_{PD} \left(R_1 + \frac{1}{sC_1}\right)\left(\frac{K_{VCO}}{s}\right) + \emptyset_N \quad (3.20)$$

$$\emptyset_{OUT} = \left(\frac{\emptyset_{OUT}}{N}\right) K_{PD} \left(R_1 + \frac{1}{sC_1}\right)\left(\frac{K_{VCO}}{s}\right) + \emptyset_N \quad (3.21)$$

$$\emptyset_{OUT} = \left(\frac{-\emptyset_{OUT}}{N}\right) K_{PD} \left(R_1 + \frac{1}{sC_1}\right)\left(\frac{K_{VCO}}{s}\right) + \emptyset_N \quad (3.22)$$

$$\emptyset_{OUT} * \left(1 + \left(\frac{1}{N}\right) K_{PD} \left(R_1 + \frac{1}{sC_1}\right)\left(\frac{K_{VCO}}{s}\right)\right) = \emptyset_N \quad (3.23)$$

$$\emptyset_{OUT} = \frac{\emptyset_N}{1 + \left(\frac{\emptyset_{OUT}}{N}\right) K_{PD} \left(R_1 + \frac{1}{sC_1}\right)\left(\frac{K_{VCO}}{s}\right)} \quad (3.24)$$

If we define the loop gain L(s) as:

$$L(s) = \left[\left(\frac{1}{N}\right) K_{PD} \left(R_1 + \frac{1}{sC_1}\right)\left(\frac{K_{VCO}}{s}\right)\right] \quad (3.25)$$

And

$$Kp = K_{PD} * R_1 \quad (3.26)$$

And

$$\frac{Ki}{s} = \frac{K_{PD}}{sC_1} \quad (3.27)$$

Then we can write equation (3.25) as:

$$L(s) = \left[\left(\frac{1}{N}\right)\left(Kp + \frac{Ki}{s}\right)\left(\frac{K_{VCO}}{s}\right)\right] \quad (3.28)$$

Or, more generally:

$$L(s) = \left[\left(\frac{1}{N}\right) * K_{PD} * H(s) * \left(\frac{K_{VCO}}{s}\right)\right] \quad (3.29)$$

Additionally, from Figure 3.21, we can also write $\emptyset_{OUT}$ as

$$\emptyset_{OUT} = \emptyset_N + \emptyset_{VCO} \quad (3.30)$$

Combining equations (3.24), (3.29), and (3.30), we can now write that

$$\frac{\emptyset_N}{1 + L(s)} = \emptyset_N + \emptyset_{VCO} \quad (3.31)$$

$$\frac{\emptyset_N}{1+L(s)} - \big(1+L(s)\big) * \frac{\emptyset_N}{1+L(s)} = \emptyset_{VCO} \quad (3.32)$$

$$\emptyset_N * \frac{(\,1-(1+\,L(s))}{1+L(s)} = \emptyset_{VCO} \quad (3.33)$$

$$\emptyset_N * \frac{\big(-L(s)\big)}{1+L(s)} = \emptyset_{VCO} \quad (3.34)$$

As we have defined $\emptyset_{VCO}$ as being:

$$\emptyset_{VCO} = \frac{K_{VCO}}{s} * V_{CNTL} \quad (3.35)$$

$$\emptyset_N * \frac{\big(-L(s)\big)}{1+L(s)} = \frac{K_{VCO}}{s} * V_{CNTL} \quad (3.36)$$

$$\frac{V_{CNTL}}{\emptyset_N} = \frac{s}{K_{VCO}} \frac{\left(-\left(\frac{1}{N}\right)\left(Kp+\frac{Ki}{s}\right)\left(\frac{K_{VCO}}{s}\right)\right)}{\left(1+\left(\frac{1}{N}\right)\left(Kp+\frac{Ki}{s}\right)\left(\frac{K_{VCO}}{s}\right)\right)} \quad (3.37)$$

Here, from the above equation we can see that for a given phase noise $\emptyset_N$ the response of the control voltage V_{CNTL} is negatively correlated, as it is essentially 'correcting' the phase noise. The greater the K_{VCO}, the less the V_{CNTL} response will be. This makes sense, as a VCO with a higher gain will require less voltage to cause a similar frequency change.

Using equation (3.37), we can substitute L(s) with it's expanded form, producing:

$$\frac{V_{CNTL}}{\emptyset_N} = \frac{-s}{K_{VCO}} * \frac{\left(\left(\frac{1}{N}\right)\left(Kp+\frac{Ki}{s}\right)\left(\frac{K_{VCO}}{s}\right)\right)}{\left(1+\left(\frac{1}{N}\right)\left(Kp+\frac{Ki}{s}\right)\left(\frac{K_{VCO}}{s}\right)\right)} \quad (3.38)$$

$$\frac{V_{CNTL}}{\emptyset_N} = \frac{-s}{K_{VCO}} * \frac{\left(\left(\frac{1}{N}\right)\left(Kp + \frac{Ki}{s}\right)\left(\frac{K_{VCO}}{s}\right)\right)}{\left(1 + \left(\frac{1}{N}\right)\left(Kp + \frac{Ki}{s}\right)\left(\frac{K_{VCO}}{s}\right)\right)} \quad (3.39)$$

$$\frac{V_{CNTL}}{\emptyset_N} = \frac{-\left(\left(\frac{1}{N}\right)\left(Kp + \frac{Ki}{s}\right)\right)}{\left(1 + \left(\frac{1}{N}\right)\left(Kp + \frac{Ki}{s}\right)\left(\frac{K_{VCO}}{s}\right)\right)} \quad (3.40)$$

Splitting our equation into two parts, to separate the Ki and Kp component, we arrive at:

$$\frac{V_{CNTL}}{\emptyset_N} = -\left[\frac{\left(\frac{1}{N}\right)Kp}{\left(1 + \left(\frac{1}{N}\right)\left(Kp + \frac{Ki}{s}\right)\left(\frac{K_{VCO}}{s}\right)\right)} + \frac{\left(\frac{1}{N}\right)\left(\frac{Ki}{s}\right)}{\left(1 + \left(\frac{1}{N}\right)\left(Kp + \frac{Ki}{s}\right)\left(\frac{K_{VCO}}{s}\right)\right)}\right] \quad (3.41)$$

At low frequencies, if we assume that

$$\left(\frac{1}{N}\right)\left(Kp + \frac{Ki}{s}\right)\left(\frac{K_{VCO}}{s}\right) \gg 1 \quad (3.42)$$

Then:

$$\frac{V_{CNTL}}{\emptyset_N} = \frac{-s}{K_{VCO}} \quad (3.43)$$

At higher frequencies, we get

$$\frac{V_{CNTL}}{\emptyset_N} = -\frac{\left(Kp + \frac{Ki}{s}\right)}{N} \quad (3.44)$$

If s is sufficiently high, then equation (3.44) becomes

$$-\frac{Kp}{N} \quad (3.45)$$

Which shows that phase noise from the VCO oscillator will appear at the V_{CNTL} node regardless if a digital or analog approach is used, and is not dependant on frequency.

However, if we were able to focus on the integral path only, we would be able to reduce noise due to the 1/s term present in the integral path:

$$\frac{V_{CNTL}}{\emptyset_N} = -\frac{Ki}{Ns} \quad (3.46)$$

From this, it can be seen that if one were able to isolate the -Ki/Ns term away from the Kp term the noise that appears in the V_{CNTL} node would be improved. As an example, let us assume a resistor value of 3000 Ω, K_{VCO} of 1E8 Hz/V, a capacitance value of 100nf, and an Icp of 30μA. Plugging these values into the equation over the span of 0 to 100KHz, the following plot in Figure 3.22 was generated, showing how the integral path has much less noise than the proportional path and integral path combined, leading to better noise performance if the integral path only is used.

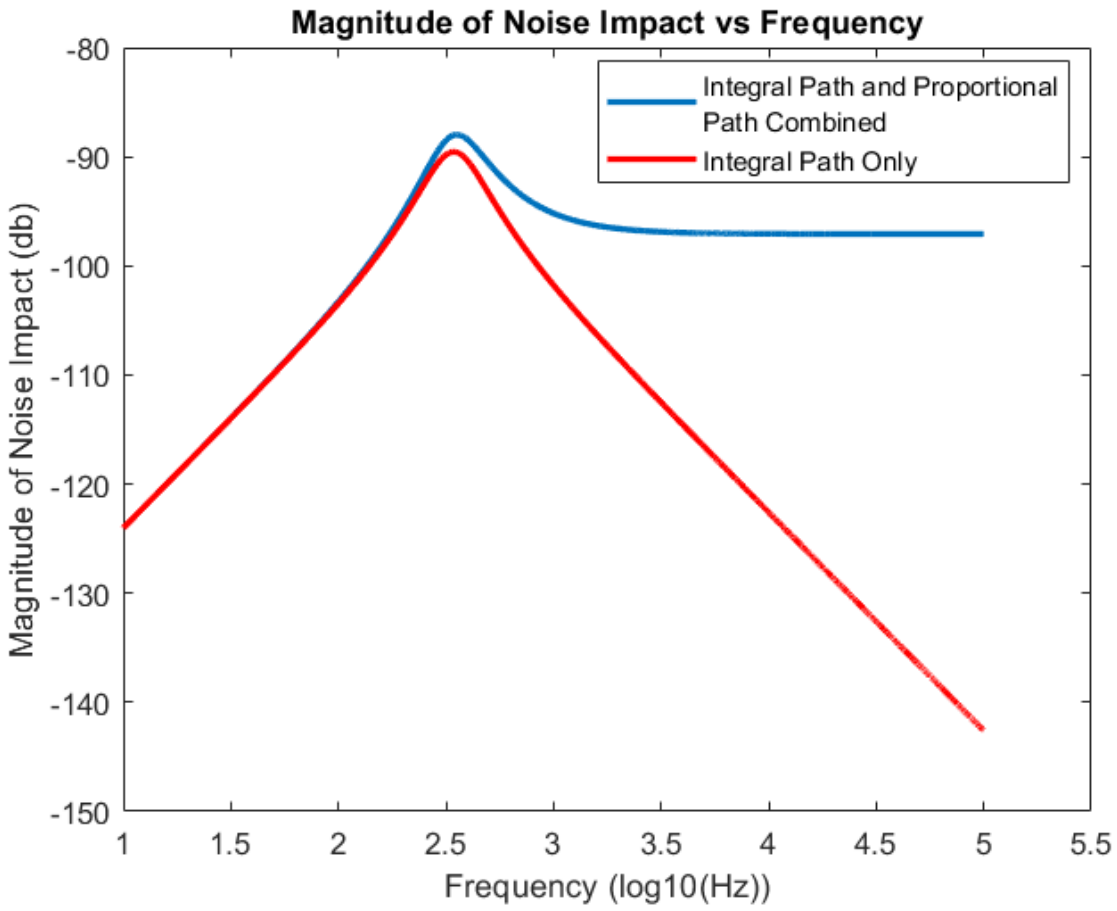

Figure 3.22: Magnitude of Noise Impact vs Frequency, with the Integral Path + Proportional Path combined plotted against the Integral Path only. It can be seen how the integral path has significantly less noise than the proportional path.

However, even if we figured out a way to isolate the integral term, for the noise impact on the integral path to reduce we require Ki to be small as possible, which requires a capacitor to be made big as possible. Not only does increasing capacitance lead to high area costs, the significant leakage current of a large capacitor in smaller technology nodes is significant and can impact PLL performance significantly[*10-12*]. The effect on increasing capacitance (and therefore reducing the noise impact on the integral path) can be seen in Figure 3.23

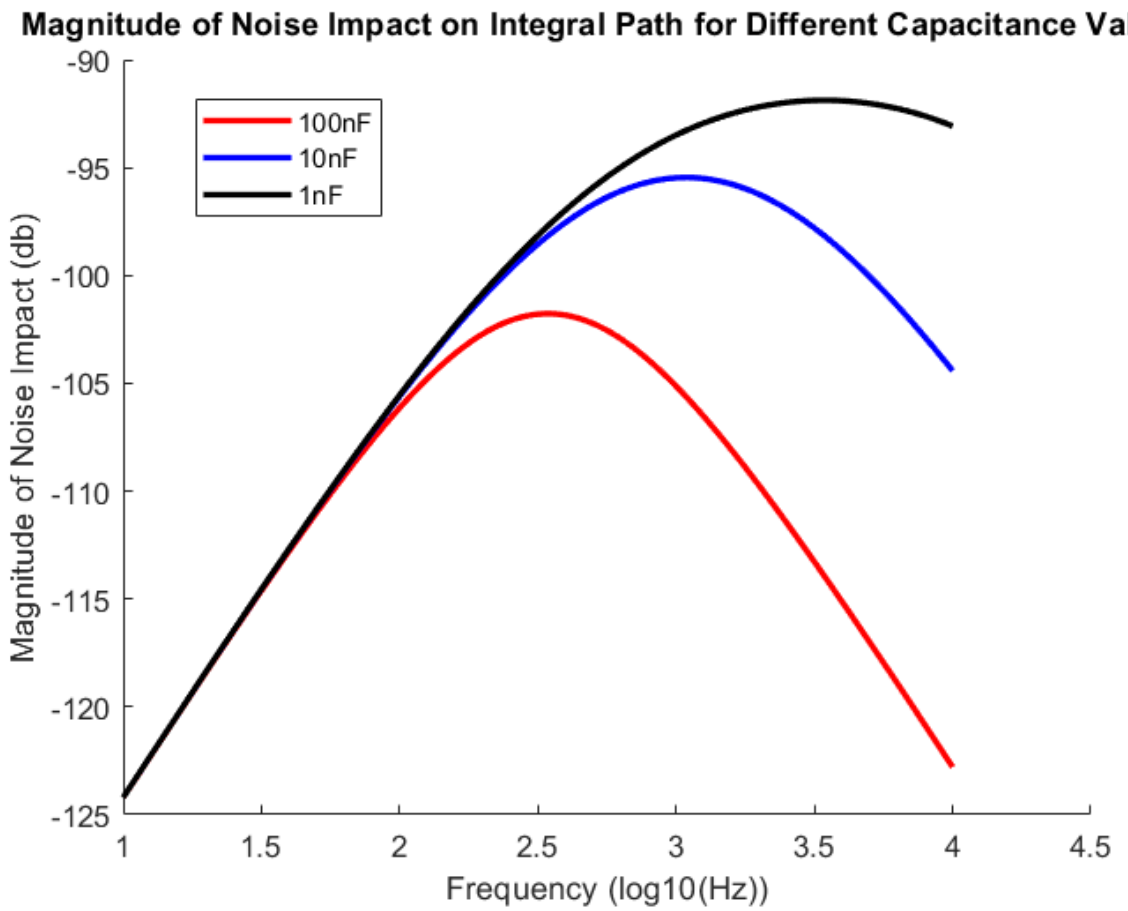

Figure 3.23: Noise Impact vs Frequency for the integral path output for 3 different capacitor C1 Values: 100nF, 10nF, 1nF, The larger the capacitor (or smaller the integral constant term Ki) the less impact noise has.

Thus, given that isolating the integral path leads to better noise performance, and the benefits of making the integral path smaller, going into the digital domain seems like a natural progression.

3.5 Digital PLL for capacitance sensing

The reason we have discussed at length the analog CPLL is because of how similar it is to the digital equivalent. While a true analysis of a digital PLL requires transformation into the Z domain, if certain parameters (discussed briefly below) are present than the analysis is a reasonable approximation [*13*]. The basic form of the digital PLL is shown below in Figure 3.24.

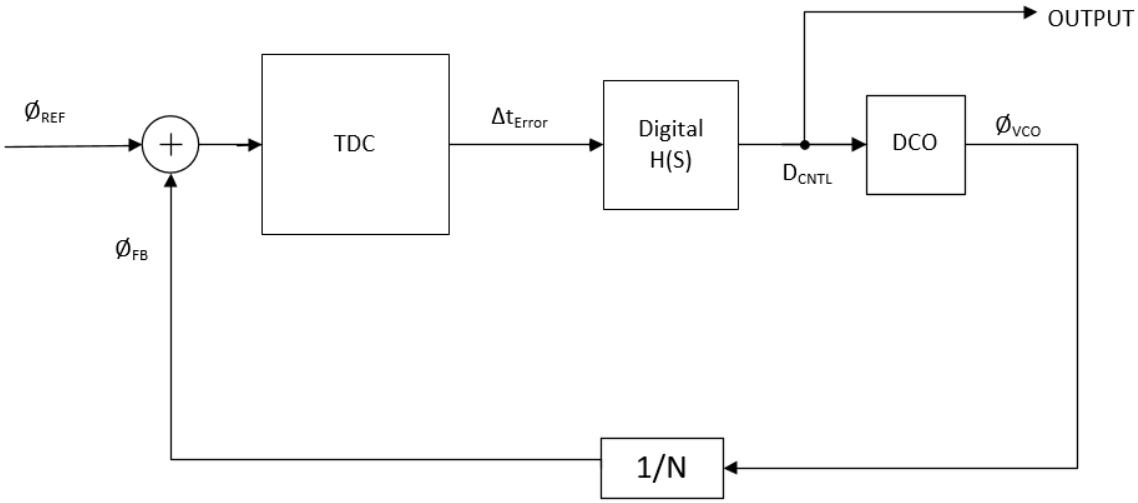

Figure 3.24: Standard Digital PLL Equivalent to the analog CP-PLL, discussed in section 3.4. Note that the output is not the full D_{CNTL} value but only the integral path portion of it.

Digital equivalents to analog components

While an analog PLL and a digital PLL are different, almost all the analog components have digital equivalents.

Time-to-digital-converter and PFD equivalent

For this project and most digital second order phase-locked loops, time is measured directly instead of phase, using a Time-to-Digital (TDC) conversion circuit.

Given a fixed reference frequency, the transfer function from the phase domain to the time domain is:

$$PFD(s) = \frac{T_{REF}}{2\pi * \Delta_{TDC}} \quad (3.47)$$

Where T_{REF} is the period of the reference frequency,

Δ_{TDC} is the resolution of the TDC circuit.

This makes sense, as the period T_{REF} is equivalent to 2π radians in the phase domain (relative to a fixed frequency F_{REF}), and the greater the resolution the more phase data will be available.

VCO – DCO equivalent

In the digital domain, instead of a VCO a Digitally-Controlled-Oscillator (DCO) is used instead, which is controlled by a digital binary input instead of an analog control voltage. Given that the digital binary input is equivalent to the analog control voltage up to it's bit resolution, the transfer function is like that of the analog domain:

$$\frac{K_{DCO}}{s} \quad (3.48)$$

Where K_{DCO} is the gain of the digital oscillator, expressed in V/Code

Digital filter

For the H(s) filter function, a digital filter is used instead of an analog one. The terms KP (represented by R_1) and K_i (represented by $1/sC_1$) are instead replaced by a digital KP_D and KI_D . For KP_D, it simply becomes a constant that is multiplied by the digital phase error, while KI_D performs the integrating function of the capacitor by using an accumulator, which repeatedly adds the current value to the summation of all previous values. To stop overflow, bi-polar phase error must be given that can represent both positive and negative phase error. The KI_D term and KP_D term are then added and outputted to the DCO to correct any phase error.

The Bi-linear transformation can be seen below in Figure 3.25.

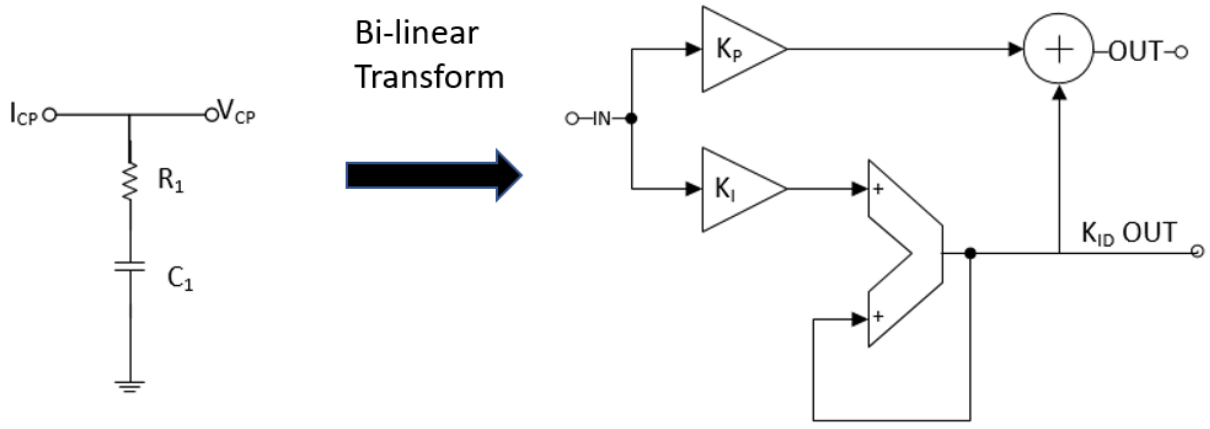

Figure 3.25: The Bi-Linear transform of the analog CP-PLL low-pass filter into a digital low-pass filter. Note that the integral path term KID is separable from the digital low-pass filter's output, unlike the analog variant.

From [*13*], we can reasonably approximate and relate KP_D and KI to their analog counterparts as:

$$KP_{Di} = R_1 - \frac{T_s}{2C_1} \quad (3.49)$$

$$KI_D = \frac{T_s}{C_1} \quad (3.50)$$

Where T_s is the sampling rate of the TDC.

What is important to note here in , as discussed before, is that while in the analog case the proportional path and integral path are lumped together and cannot be separated, in the digital filter this is not the case. We can combine the integral path and proportional path so as to make the phase-locked loop stay in lock and control, while also separating the integral path away from the proportional path for the sole purposes of reading the sensor information. This is not possible in the analog domain.

Additionally, the Ki term can be easier to represent digitally than the analog domain, as discussed before, and can be further digitally filtered if required to reduce noise even more, something that is not possible in the analog domain.

While a complete analysis of digital phase locked loops is required to fully encapsulate the digital PLL behavior, given the above approximations it is reasonable to build a DPLL by first building the equivalent analog PLL, and then converting it to the digital domain equivalent.

3.6 Physical implementation of digital PLL with discrete parts for sensor reading

To demonstrate our theory, we did two things. First, we simulated and fabricated a LC-DCO oscillator whose frequency could be controlled both by a digital input codeword and the change in capacitance of a variable capacitor modelled to be similar in electrical properties as the sensor constructed in Chapter 2. Second, we built a full digital PLL system using discrete parts based on the principles shown in section 3.5 that was able to detect a minute change in frequency and output a digital code-word in response detecting it.

3.6.1 LC-DCO and simulation

Sensor model

For the purposes of simulating the sensor block, we made a simple model where we assumed that the resistance and inductance of the sensor and bond-wire connections could be lumped together as an inductor and resistor in series, and the capacitive sensor between them. This is shown in Figure 3.26.

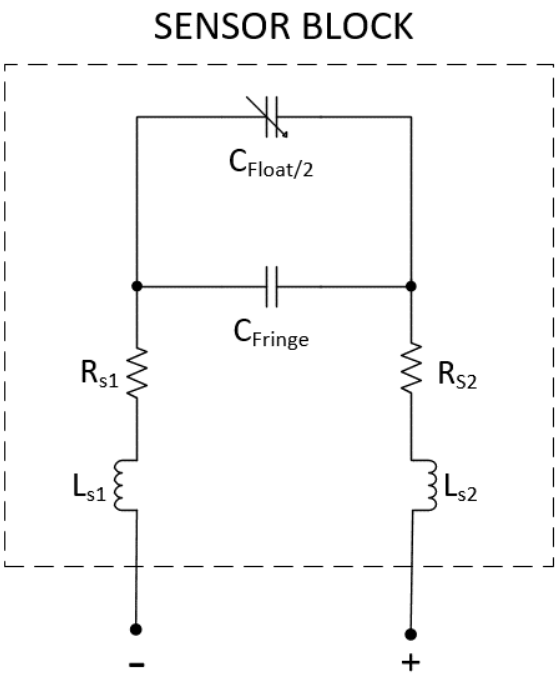

Figure 3.26: Simple LCR model of the capacitive sensor made in Chapter 2.

The typical values used in simulation for the above variables are shown in **Error! Reference source not found.** below:

Table 1: Typical 'Sensor Block' Values used to Characterize the Capacitive Pressure Sensor in Simulation.

Variable Name	**Value**
R_{S1} , R_{S2}	1 Ω
L_{S1}, L_{S2}	1 nH
C_{Fringe}	200 fF
$C_{Float/2}$	200 fF-1500 fF

Typical values may vary, but we concluded that the above values were a reasonable approximation. Given the figure above, we can write down the impedance in the s-domain between the two terminal sensor as:

$$Sensor_{Impedance} = (L_{s1} + L_{s2})s + \frac{1}{(C_{Fringe} + C_{Float2})s} + (R_{s1} + R_{s2}) \quad (3.51)$$

LC DCO

To make a LC-DCO that can have its output frequency both be changed by both the change of capacitance in a capacitive-pressure sensor and a separate digital control input, some modifications are required. The modifications made are described below, and were implemented in the 65nm technology node.

Capacitor-bank DAC

Unlike the analog LC-VCO that was discussed before that used an analog input voltage to control the frequency, in an LC-CCO a digital method must be implemented. This was done by using a capacitor bank DAC to form a variable capacitor that can be controlled by a digital input.

To form a variable capacitor of N bit resolution that can be controlled using N digital control signals, one can make a controllable capacitor bank. This consists of creating several switchable capacitors in parallel, with each subsequent capacitor being 2x larger than the last. For N capacitors, a capacitor bank can be formed with $C*2^{N-1}$ resolution, with C being the smallest capacitor, otherwise known as the least-significant-bit (LSB). This is shown in Figure 3.27 below:

.

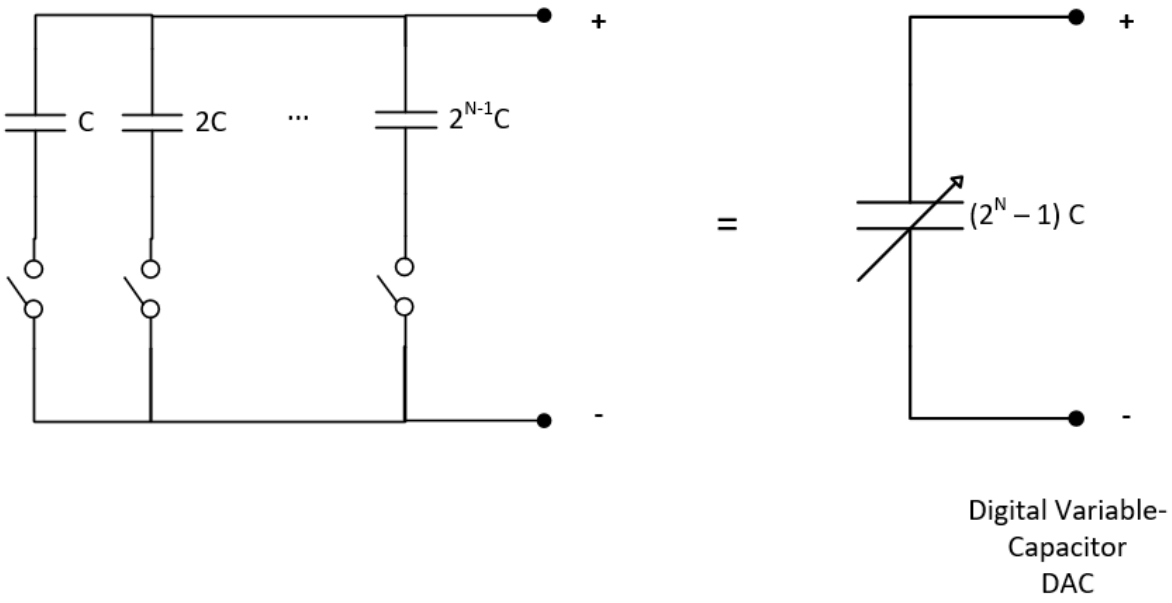

Figure 3.27: A digital DAC capacitor bank. Using N switchable capacitors in parralel, each one being 2x larger than the last one, a variable capacitor can be formed with N bit resolution for (2^N – 1) possible values with the LSB equalling C, the smallest capacitor.

For the 65nm chip that was taped, we chose an 8-bit capacitor DAC bank, with the LSB C equalling to approximately 2 fF, and constructed them on either side of the LC tank for symmetry, leading to an estimated range of 4 fF-1028 fF, with 4 fF resolution, which is around the capacitance values we expect for the pressure sensor constructed in Chapter 2.

Parasitic Inductance Negation via Cross-Coupled Transistors.

A method of attaching the sensor to LC-DCO oscillator is required.

While the simplest method of attaching the capacitive sensor is by bond-wiring it directly to the LC tank, the bond-wire connections will inherently add parasitic inductance between the sensor capacitor and the LC tank, as well as introducing non-symmetrical connections due to variations between the two connections. As we wished the connection to be symmetrical, this required the use a cross-coupled

impedance negator, which is commonly used to reduce the impact of parasitics on high-speed circuits. This is shown in Figure 3.28.

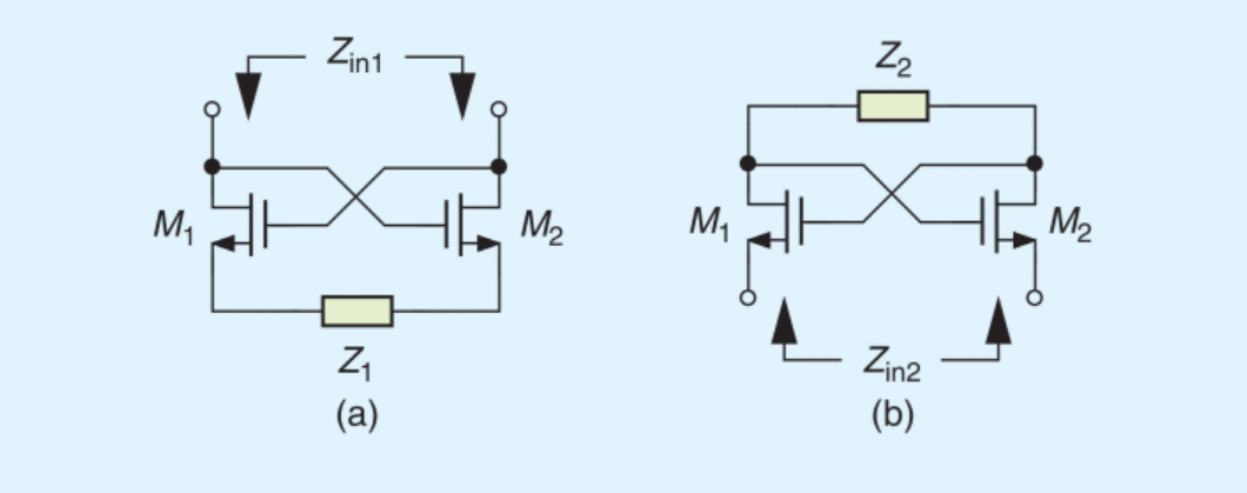

Figure 3.28: A Cross-coupled pair with a load Z1 can be used to negate the impedance of Z1. Reprinted from [14], Solid-State Circuits Magzine, with permission IEEE ©, 2014.

While it has been discussed previously how a cross coupled NMOS pair can form negative resistance, it can also be used to negate impedance in general, and is commonly used as a way to negate impedances other than resistance, such as inductance and capacitance. For a load Z_1, as shown in Figure 3.28 a), iit can be proven that the impedance Z_{in1} is equivalent to[*14*]:

$$Z_{in1} = -\frac{2}{gm} - Z_1 \quad (3.52)$$

Combining equations 3.52 and 3.53, we can infer that the approximate input impedance of the sensor will be:

$$Z_{in1} = -\frac{2}{gm} - \left[(L_{s1} + L_{s2})s + \frac{1}{(C_{Fringe} + C_{Float2})s} + (R_{s1} + R_{s2})\right] \quad (3.53)$$

Additionally, two current sources can be used with the cross-coupled impedance negator, as shown in Figure 3.29 below. This is required to bias the transistors, and also tune the gm of both transistors so they match, leading to a symmetrical circuit tuned to the LC tank.

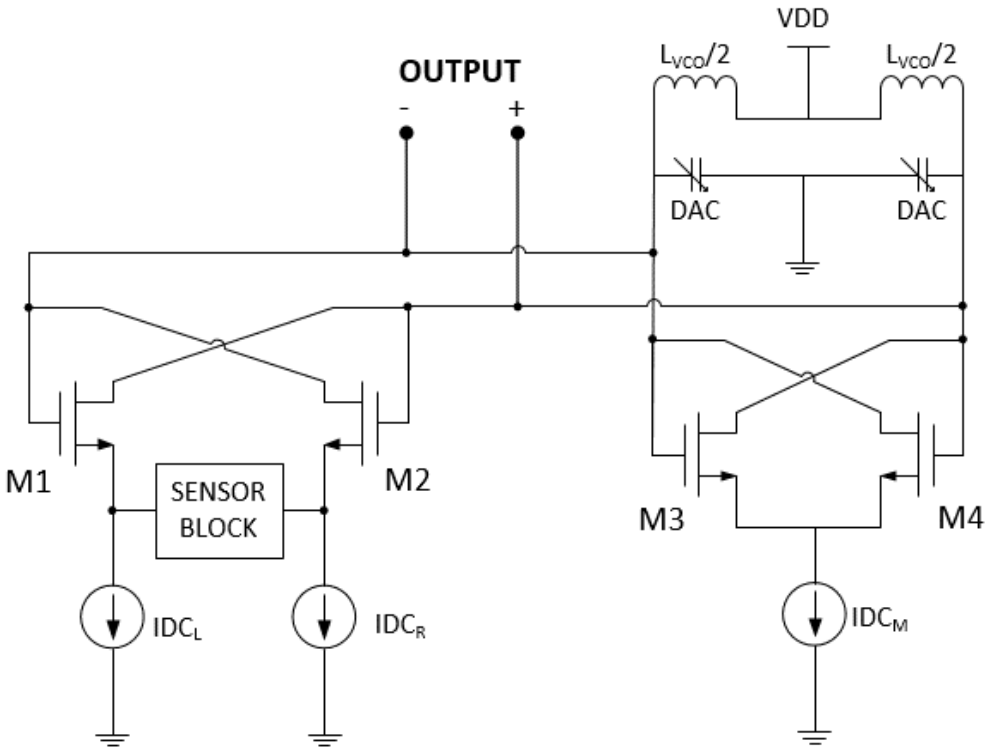

Figure 3.29: LC-DCO with the Capacitive Sensor (Sensor Block) connected to the LC tank using a biased Cross-Coupled Impedance Negator.

The L_{VCO} chosen above was simulated at a value of 2.25nH with a quality factor of 20, and each DAC capacitor bank had a range of 2-528fF, leading to a combined range of 4-1056fF in the LC-Tank with them combined.

By tuning the 3 static DC currents, IDC_M , IDC_L , and IDC_R, we are able to finely tune the circuit to the optimal oscillation response, and account for any non-idealities within the circuit or sensor. Thus, we can simplify the circuit diagram down into the one shown in Figure 3.1. By using the DAC capacitor banks,

we can create a feedback loop to counter any disturbances to the oscillator's frequency caused by the sensor capacitor.

Using the above simulation in Cadence Virtuoso environment, we simulated the change in the oscillator frequency as a function of changing sensor capacitance between 200 fF – 1500 fF, which is a similar range we showed in Chapter 2. The simulation results are found below in Figure 3.30.

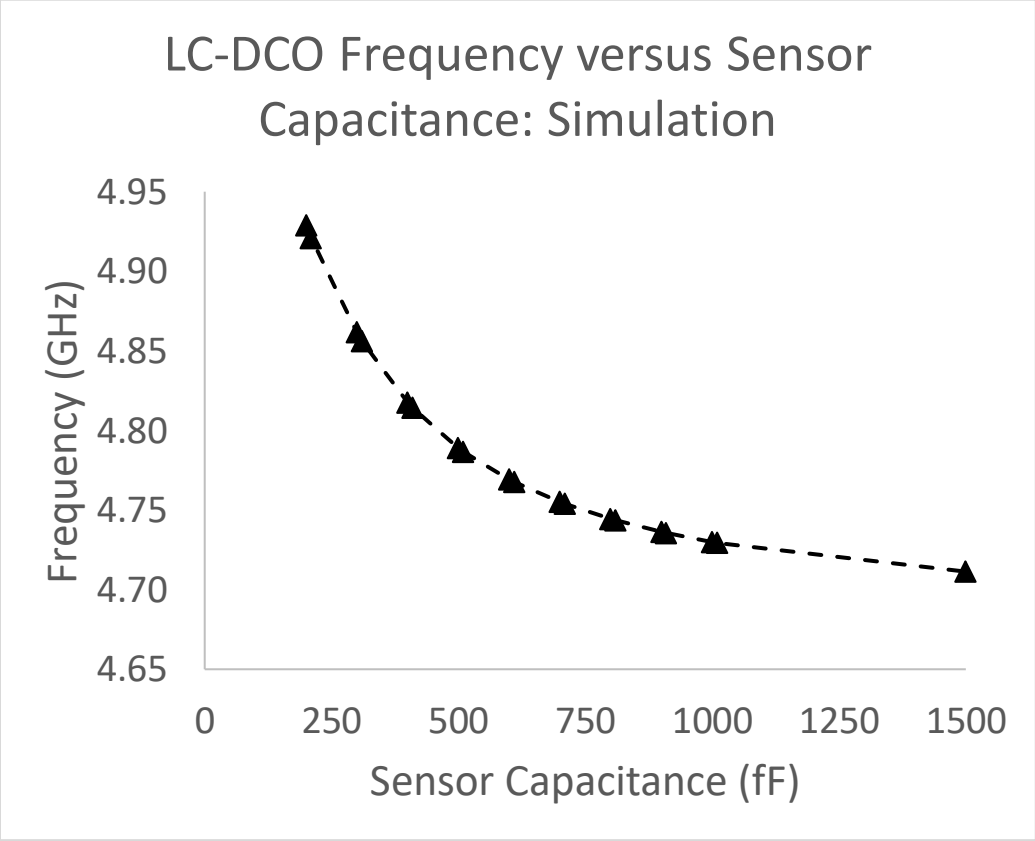

Figure 3.30: Frequency vs Sensor Capacitance, between the range of 200fF-1500fF..DAC capacitors were both set at the midrange value of 256fF

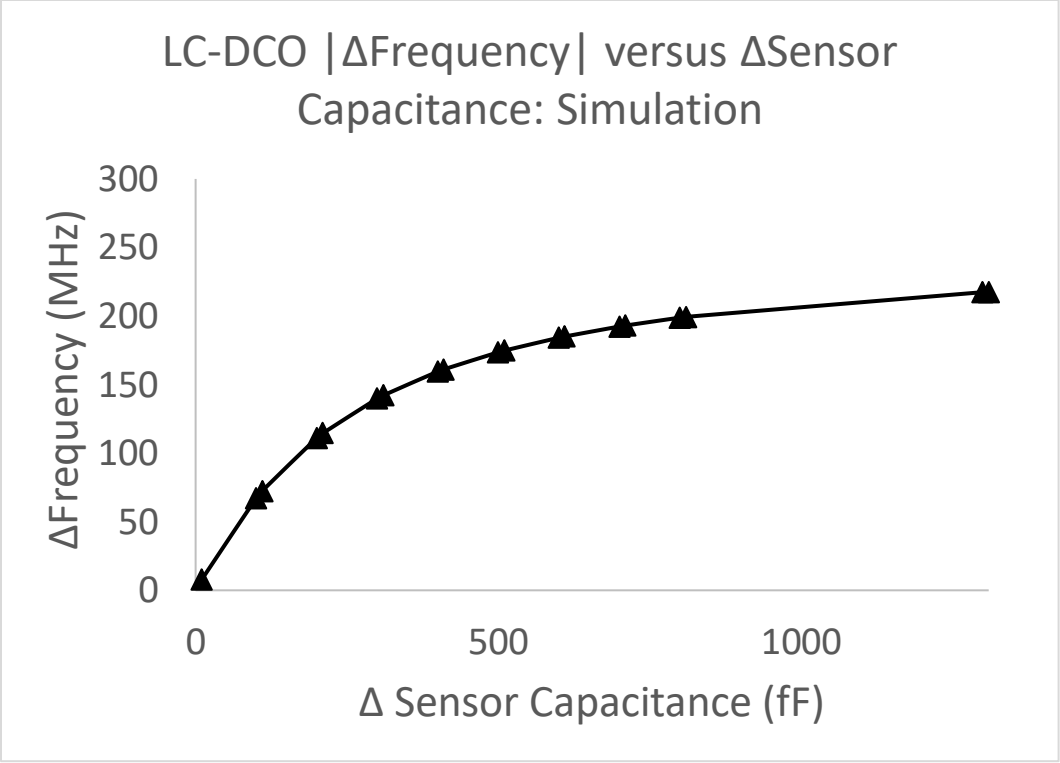

Figure 3.31: ΔFrequency (MHz) vs ΔSensor Capacitance (fF) from the data shown in Figure 3.30, showing the sensitivity of the oscillator frequency in response to a change in capacitance. Both DAC capacitor banks were set at the mid-range value of 256fF

For the simulation above in Figure 3.31, with the circuit simulated we found that it had an averaged sensitivity of 248kHz/fF frequency response to changing sensor values between 200fF and 1000fF, and between 1000fF and 1500fF it was found to have only a 18.5kHz/fF frequency response, implying the best range for the sensor for this circuit is in 200fF-1000fF range.

With better designing and more knowledge of the circuit parameters, this could be improved, but for the purposes of our discussion it is sufficient. Centered around the sensor capacitance value of 400fF as shown in 3.31, the normalized Δf/ΔC value (dividing the frequency change by the center frequency of the VCO) derived a value of 3.28E-05 Δf per fF of change.

Fabrication

As well, a layout for the circuit was made for the LC-DCO oscillator described above with a frequency divider included. This circuit was then fabricatated in the 65nm technology node from TSMC. Due to time constraints the circuit was not tested. A microscopic photo of the die is shown below with dimensions in Figure 3.32.

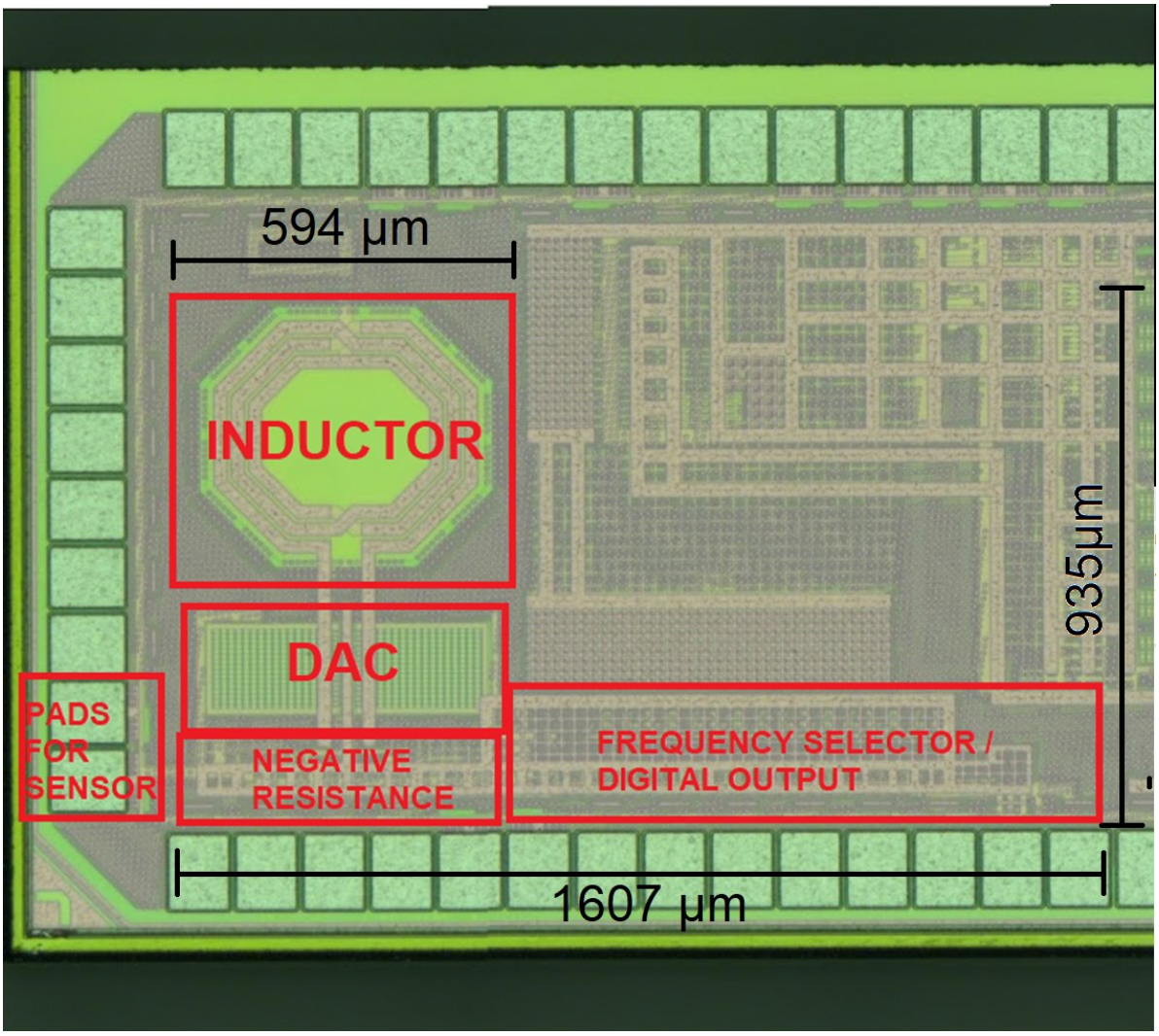

Figure 3.32: Microscopic photo of the 65nm DCO chip fabricated, with components and dimensions labelled.

3.6.2 Discrete part PLL

While it would be ideal to demonstrate the full digital PLL capacitance-to-digital sensor principle on a single IC chip with all components fabricated on one chip, due to time constraints this was not feasible. Instead, we chose to illustrate the concept using discrete parts available for purchase. Equivalents to the components shown in Figure 3.33 were purchased and connected into a digital PLL system, a photograph of which is provided in Figure 3.34. Each part of the section will be explained with the part that was selected.

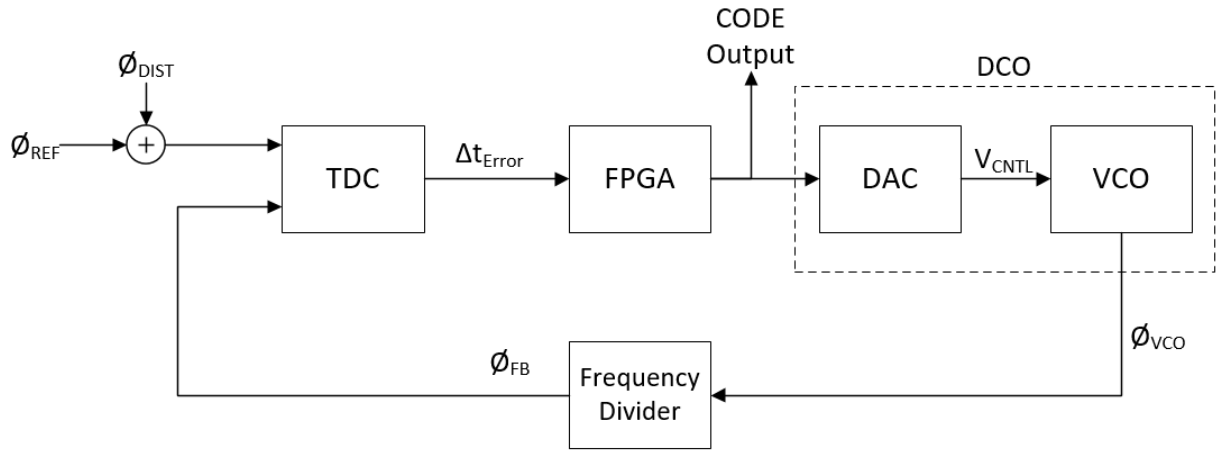

Figure 3.33: The discrete part digital PLL that was constructed. The FPGA is used as the digital filter, while the DAC and VCO combined form a DCO. For the purposes of empirical measurement, instead of having the $Ø_{VCO}$ signal change due to a disturbance we introduce to the VCO, we instead introduced the disturbance at the reference clock, which is equivalent.

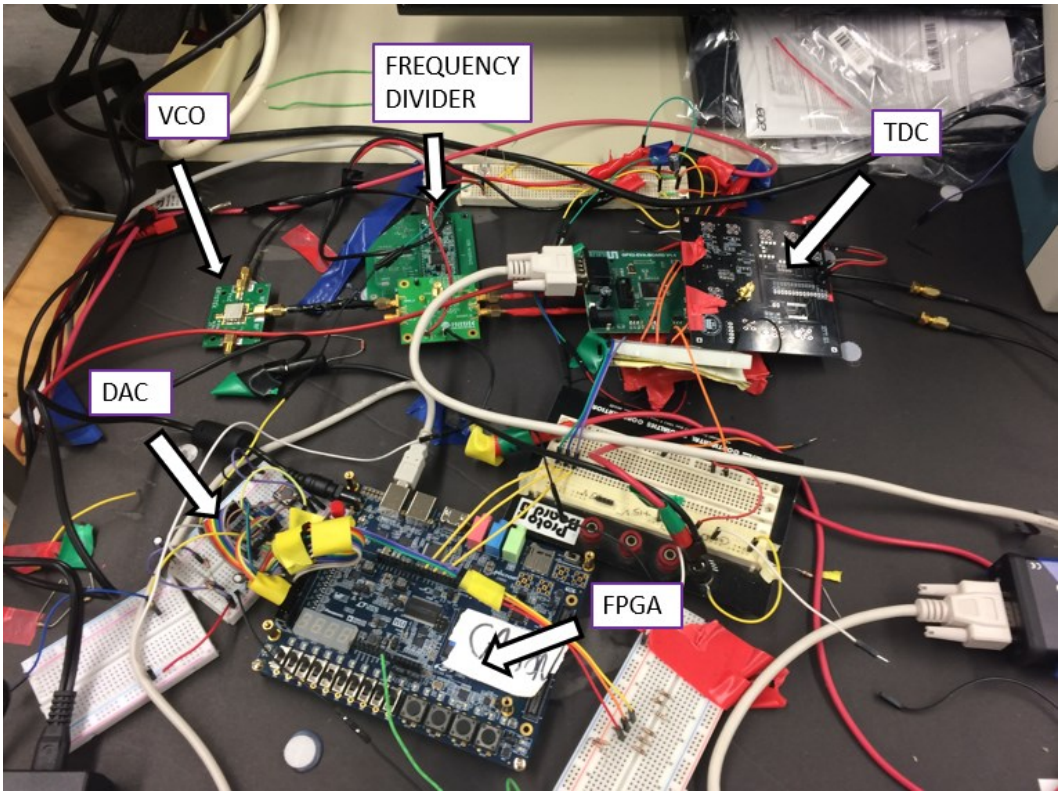

Figure 3.34: Implemented set-up using discrete parts, which follows the same structure as the block diagram shown in Figure 32. All components of the block diagram have their equivalent real-world part highlighted.

VCO

The first block of the hardware implementation is the VCO, which was implemented using a Crytek 42-46 MHz VCO [*15*]. The VCO is simple in design, with one input pin accepting a control voltage between 0.5-4.5V, and an output pin which produces a sinusoidal differential oscillating signal between the frequency of 40.416 MHz-48.256 MHz, which was confirmed experimentally. The output frequency voltage relation is:

$$Frequency(V) = 1.9146\ \text{MHz} * \text{V} + 39.412\ \text{MHz}. \quad (3.54)$$

With V being the input voltage.

DAC

Unfortunately, due to a limited selection of digitally controlled oscillators, the VCO selected was a traditional VCO whose input is an analog voltage. To form this into a digital-VCO representation, a DAC

was used in conjunction with the VCO. Instead of using a capacitor bank directly as shown in the previous section, instead we used the digitally controlled DAC to output an analog voltage to be fed into the VCO, forming a DCO effectively.

The DAC selected was the TLV5619 chip from Texas Instruments. It is a 12-bit voltage ouput DAC that can output between 0 and 5.1V, which covers the input range 0.5-4.5V of the VCO selected. Other than having 12-bits of accuracy and a voltage output range suited to our application, the input is parallel vs serial, similar to our proposed implementation of the full system using capacitor DAC banks that would be switched using multiple parallel digital inputs, and allowing for higher speed if used with an FPGA, versus a serial DAC. The DAC input relation vs Output Voltage is shown below.

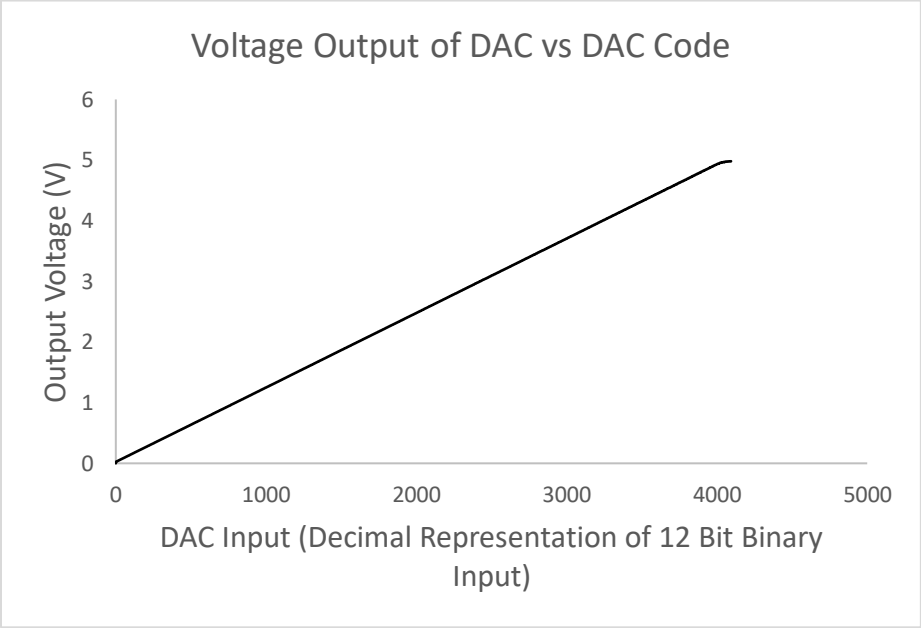

Figure 3.35: Voltage Output of the DAC vs 12 bit DAC Input code. Note that over the relevant range between 0.5-4.5V it has a linear voltage output.

Frequency divider

While it could be ideal to use the 40.416MHz-48.256MHz VCO signal directly, very few discrete TDC components can analyze time measurements accurately at this speed, not many traditional discrete part DAC's operate at this speed affordably. Additionally, as a divider is typical in PLL design, it made sense

to implement one, even if the purpose was not to make a high frequency signal from a low frequency stable reference signal,

The HMC988LPE Evaluation Board[*16*] was chosen for this project, as it can take frequencies up to 4Ghz and has selectable dividing factors between 2,4,8,16, or 32. It can accept differential or single ended inputs of low voltage swing (down to 20 mV), has programmable delay, and a low jitter noise ratio which is essential to the resolution of this project, between 10-35 femtoseconds (the range is due to frequency dependence jitter). The downside of the HMC988LPE is mainly the cost, and the non-CMOS outputs.

Taking the divided signal data, the 40.416-48.256 MHz signal is converted into a 1.263-1.508 MHz signal range. Thus, the equation 3.54 becomes:

$$Frequency(V) = 59.831\ \text{kHz} * \text{V} + 1.231\text{MHz}. \quad (3.55)$$

Measuring the VCO's output frequency over the range of the DAC output from 0.5-4.5V, we found that the relationship between our digital code and the divided frequency output of the VCO was sufficiently linear, as shown below in Figure 3.36.

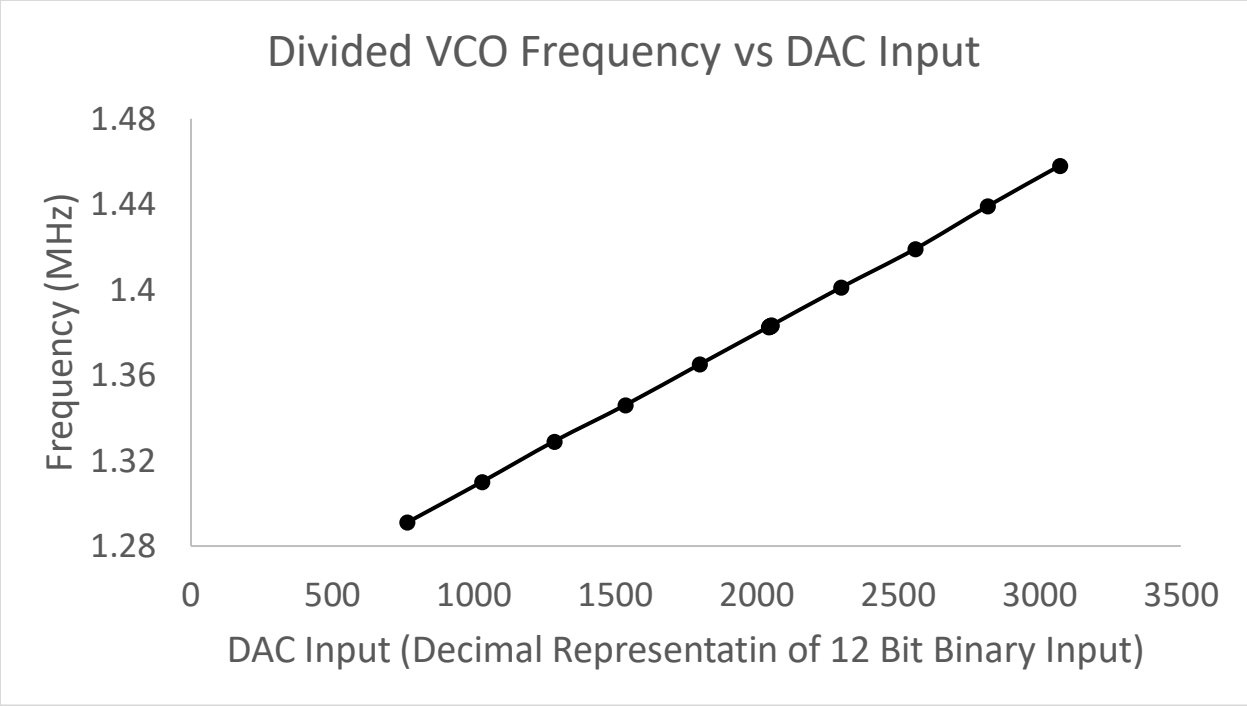

Figure 3.36: Divided VCO Frequency vs DAC Input, over the range of the DAC's 0.5-4.5V output. Note the linearity of the frequency response, which is important.

Cyclone V FPGA

The FPGA used was the Cyclone V FPGA Evaluation Board[*17*]. With multiple outputs, a 925 MHz clock, easy prototyping, an on-chip processor, and dedicated arithmetic modules, it is an excellent choice for this project, with sufficient capability to be used in any future iterations of this project that may have GHz signals vs MHz. Additionally, with it's Arduino capable headers, it serves as a functional basis to interact with other prototyping chips.

GPX2 TDC:

Instead of using a traditional phase detector which converts a phase difference into a voltage directly, a TDC was used instead to measure the Δt time difference between the two signals, and thus determine their phase. This is illustrated in Figure 3.37.

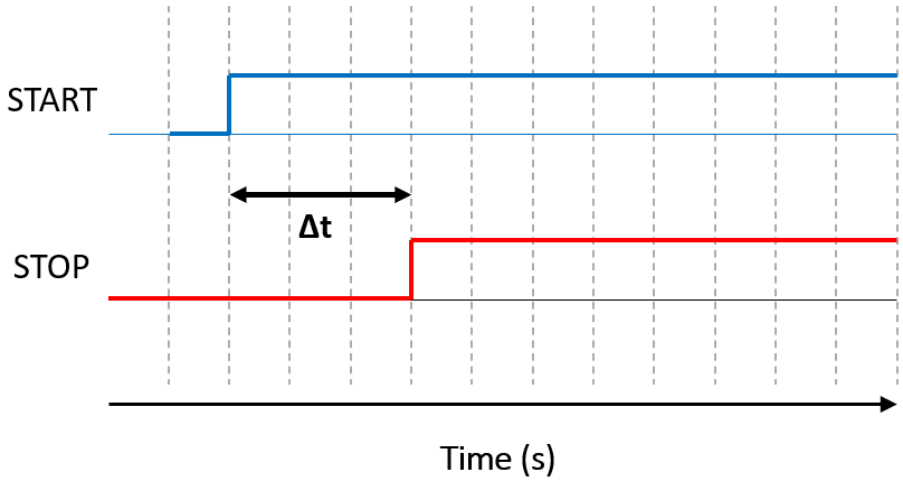

Figure 3.37: Timing diagram showing how the GPX2 measures the t between the START rising edge and the STOP rising edge.

While the details of operation of the GPX2 are quite complex, the main purpose is quite simple. Given two signals, one being a reference clock we can call the 'START' signal and the other being a signal input called our 'STOP' signal, the Δt between the START reference clock rising edge and the STOP signal's rising edge can be measured to an approximate accuracy of 20picoseconds using the GPX2, as shown in At maximum rate, it can measure time differences at a rate of 50Msps, but in the evaluation board we used the frequency was lowered to 750sps. Thus, a future project using the GPX2 TDC at it's maximum rate could see a significant improvement in performance, versus the very slow rate we were forced to use due to the evaluation board design.

For a fixed Reference 'START' frequency, we can convert the Δt into phase difference in degrees, effectively making it a phase detector instead. The transformation from Δt to degrees is given by:

$$Phase(degrees) = 360 * \frac{\Delta t}{TDC_{MAX}} \quad (3.56)$$

Where TDC MAX is the maximum Δt time period that can be measured, which is configurable on the board.For this project 19 bits was used for TDC_MAX. Thus, if a Δt code of 2^{19} was measured, that would equal 360°.

Unlike a traditional TDC, the GPX2 uses a useful feature to convert time into a binary format that is not based on a set bin width (ie one bit of information is equivalent to a fixed period of time), but is instead directly related to the period of the REFERENCE clock signal divided by the resolution settings of TDC_MAX, which is determined using on-board circuitry – thus, if a 1 MHz Reference signal is inputted into the GPX2 TDC with a resolution of 2^19, the circuitry will determine that the period of the signal is 1000 ns, and that each bit will be 1000 ns/(2^19) which equals 19 picoseconds. While excessive and not needed in a finished digital PLL design if it is designed for a specific reference signal, for our purposes this will be useful in the experimental section.

To verify and test the chip was functioning as phase detector without any linearity issues, a function generator was used to generate the REFERENCE clock 'START' signal and signal 'STOP' signal. The signals were generated to have the same frequency and a controllable phase between them. Applying several phase shifts in 60° increments, we set the TDC to output the Δt code in 19bit format vs these 60° phase shift between the 'START' and 'STOP' signals was tested at both the maximum frequency of the divided VCO (1.508 MHz) and the lowest frequency of the divided VCO signal (1.263 MHz). The TDC code vs phase-shift relation is shown below in Figure 3.38.

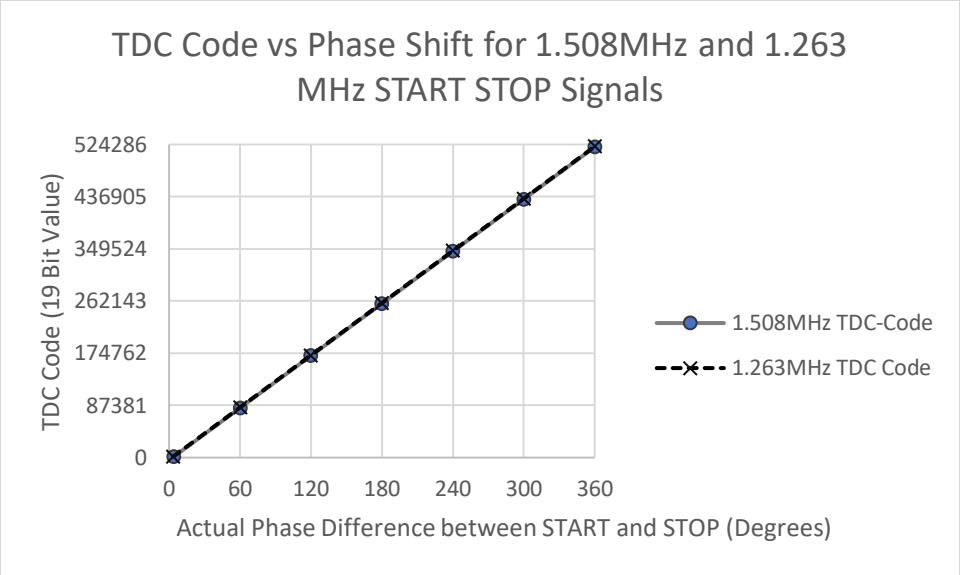

Figure 3.38: TDC Code vs Phase Shift for both 1.508MHz and 1.263MHz 'START' and 'STOP' signals. Note that the results are as expected, with a 360 degree phase shift equating to approximately 2^19 (524286).

As can be seen above, the 19 Bit TDC binary code increases linearly with phase-shift at both frequencies. If our assumption in equation (3.56) is correct, then we can use the equation to convert to degrees.

Using a trendline function in Microsoft Excel with the data, the relationship between the recorded phase angle and the actual phase angle for 1.508 MHz and 1.263 MHz are characterized by:

$$TDC - Phase(\Phi)_{1.508MHz} = \Phi - 2.9264° \quad (3.57)$$

$$TDC - Phase(\Phi)_{1.263MHz} = \Phi - 2.3284° \quad (3.58)$$

Two things can be gathered from these findings. First is that the relationship between the TDC phase and actual phase is linear for a fixed frequency – if the actual phase difference is increased by one degree at the 'STOP' signal, the TDC output code will increase by one degree. Second, there is an error offset at both frequencies of 2.9264° at a START and STOP signal frequency of 1.508 MHz and 2.3284° at a START-STOP frequency of 1.263 MHz – given an actual phase difference of 180° between the START and

STOP, the TDC will output a measurement of 177.07° and 177.67°. While this phase mismatch is undesired, signals it is still functional, as the PLL will lock onto an angle around 183° instead with a variance of approximately 0.598° between the high and low frequencies. Thus, updating equation (3.56), the actual TDC-Output Phase vs actual Phase relationship is expressed as:

$$TDC - Phase(\Phi) = \Phi - \ 2.3284° - \Delta\Phi_{\text{frequency\_variance}} \quad (3.59)$$

Where $\Delta\Phi_{\text{frequency\_variance}}$ is dependant on the frequency of the REFERENCE clock between 1.263 MHz and 1.508 MHz, with a value range of 0°-0.598° degrees.

3.6.3 Digital filter structure

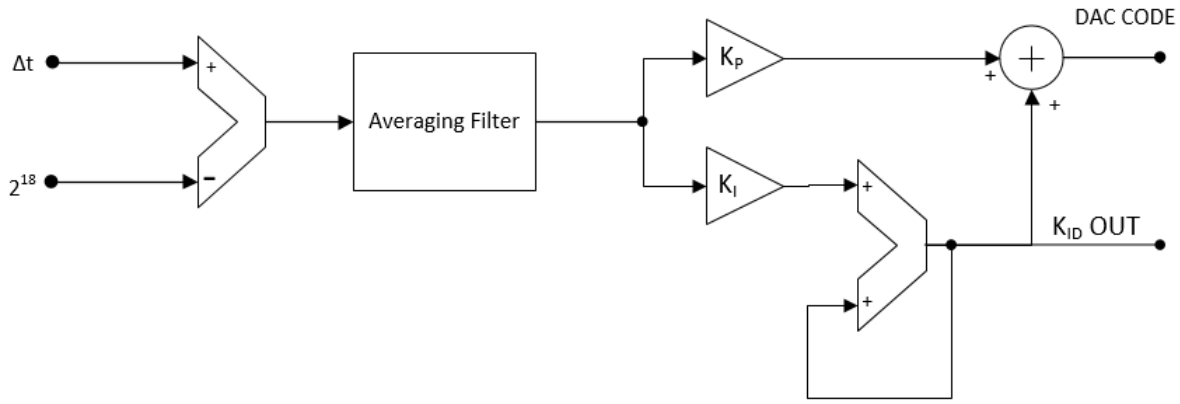

Figure 3.39: Digital filter architecture, where after being converted into a bi-polar value and averaged, it is fed into the digital equivalent of the CP-PLL low-pass filter. K_{ID} OUT contains the sensor information, while DAC CODE is used to keep the PLL locked.

As discussed in Section 3.5, a digital filter is needed to both derive the DAC CODE needed to control the DCO formed from the DAC and VCO, as well as outputting the integral path which will contain the sensor information. The digital filter is made up of 4 digital parts. Figure 3.39, above, shows the digital filter that was implemented on the FPGA board.

Bi-polar phase error

As was shown in the previous section, using the GPX2 TDC we can convert phase into a digital value between 0 and 524288 (2^{19}) Δt, 0 equalling 0 degrees phase difference while 524288 (2^{19}) is equivalent to a 360 phase difference. However, for our control system to work we need to have both positive and negative error, otherwise the accumulator that forms the integral path will overflow. This can be done on FPGA by subtracting the value 2^{18} from the phase code, converting the TDC code range to (-262,144, 262,144) which corresponds to phase values of (-180°,180°). If we now interpret this phase value as a 'phase-error' that we wish to make zero with our control system, the system will be 'locked' and in phase when the 'START' signal (the signal from our hypothetical sensor) is 180° separated from the 'STOP' signal, ie the phase-error is zero.

Of course, given the previous section the 'true' phase that will be locked onto will be around 177°, with the variation as well mentioned earlier. Given the small degree discrepancy, it was not seen as a significant issue.

Averaging filter

To decrease noise impact further, we experimented with low-pass filtering the signal before it reaches the integral and proportional path of the digital filter discussed in 3.5. This is done by merely storing the last N samples in memory, and calculating their medican value. More formally, this is represented by:

$$Average\ \Delta t = \frac{1}{N}\sum_{i=0}^{n-1} S_i \quad (3.60$$

S_i being the ith sample to be taken sequentially,

N being the number of samples averaged.

Due to the low sample rate of the evaluation board, it was found that for practical purposes a maximum of 8 values could be averaged, and more efficiently only a sample of 2 values could be used while also locking onto the phase locked loop. Due to significant delay from the time the sample was taken to the time the sample was read by the FPGA, making the average filter too large would increase this delay substantially to the point the loop was locking onto phase error values far in the past.

Integral path and proportional path

The integral path and proportional path, as discussed before, involves multiplying the averaged Δt by a factor Kp as well as adding it to an accumulator, an accumulator being a circuit that repeatedly takes the current value and adds it to a value that represents the sum of all previous values (definitely need to rephrase this), essentially acting like a digital integration.

The values for Ki and Kp were found experimentally to be Ki = 9.67277E-08, and Kp = 4.07E-05.

DAC conversion

A final conversion, not shown in Figure 3.39, is to take the DAC CODE value and convert it from it's 32 Bit format and convert it into an input that can relate the DAC CODE to a value that covers the 0.5-4.5V range of the DAC.

Unfortunately, due to the latency issues discussed, the LSB of the 12-bit DAC (approximately 98µV per step) was too much of a jump for the system, leading to over-correction. For more accuracy, we used a 4 bit PWM method, where instead we made the DAC code 16 bits, with the last 4 bits indicating the PWM ratio to switch between the first 12 bits and the value 1 bit higher.

3.6.4 Experimental method

Once constructing the discrete-part PLL, a method of testing the set-up was required. Ideally, we would have wished to have a way for our capacitive sensor to change the frequency of the VCO. However, there were not really any simple or precise ways to do this. As well, disturbing the VCO directly, such as changing the VDD of the VCO, did not have much effect on frequency.

Thus, an alternative method of testing was implemented. Instead of having the VCO signal be disturbed, we instead disturbed the Reference clock signal. A positive phase shift caused by an increase in frequency of the VCO is equivalent to the reference clock's frequency decreasing as far as the TDC is concerned. This allowed us to implement very accurate disturbances into the system for the PLL to measure.

The one issue with this technique is that as we defined the Reference frequency as 360°, by changing the reference frequency this would no longer hold as the Reference period changed. For example, if the reference frequency was defined at 1MHz, then 180° would be defined as half the period of the reference frequency, or 500 ns. If the reference frequency doubled to 2 MHz, then 500 ns should translate to 360°, but if the circuit still assumed the reference frequency was 1 MHz it would incorrectly interpret it as 180° still.

Luckily, due to the GPX2 being quite advanced the circuit calibrates it's resolution to equal to the width of the period, which it measures internally. Effectively, due to the advanced circuitry the above situation would not occur as it can recalibrate to the new Reference signal period. While ideally it would be quite expensive to have this circuitry added to a full Capacitance-to-Digital system we proposed, for the purposes of this experiment it is quite convenient.

Speed and latency

While the GPX2 is capable of 40-70 MSPS, this requires the LVDS option to be used which was not included in the EVA kit, while the SPI option allows around 1 MSPS. The sample rate of the GPX2 EVA kit used however was around 750 SPS, which is much slower than ideal. Additionally, the way the GPX2 works with multiple samples is through the use of a 16 stage FIFO buffer. This means that a measurement taken at t = 0 can only be outputted from the chip after the previous 15 measurements are outputted, leading to even more latency. This leads to an approximate 20 ms delay between a phase-error measurement taken at t = 0 and the feedback loop responding to this phase error.

If the GPX2 was able to be run at it's 40-70MSPS speed, not only would the latency decrease due to higher samples per second, but because the 16 stage FIFO buffer would not fill up (ie, every rising edge was measured and read before the next sample entered the FIFO buffer) the FIFO buffer delay would not be present. In a future work this could be improved upon greatly.

Thus, due to this, the disturbance we introduced had to be quite small for the loop to lock.

Procedure

Starting at the mid-value DAC output (2.5V), we set the Reference frequency to the VCO frequency found at this DAC value (1.38 MHz), and then had the loop lock-on to the Reference frequency.

The reference clock was disturbed in 10 Hz steps, and measurements of the KI_D were taken every 100Hz. The steps were done over a range of 2 kHz. This was done to simulate how a digital PLL would have it's output frequency disturbed by the capacitive pressure sensor we proposed in section 3.5 and 3.6.1. More steps over a wider range would have been ideal, but unfortunately due to the function generator having to be manually switched to a different frequency and the slow rate at which the frequency had to be changed, it became impractical to go beyond this point. If the latency issue were to be fixed, the whole range could be investigated. The results are shown below in Figure 3.40, with the Δf divided by the VCO

center frequency to normalize the results. The normalized change in code to a change in frequency was 3.97E7 code change per normalized change in frequency (relative to the center frequency of the VCO).

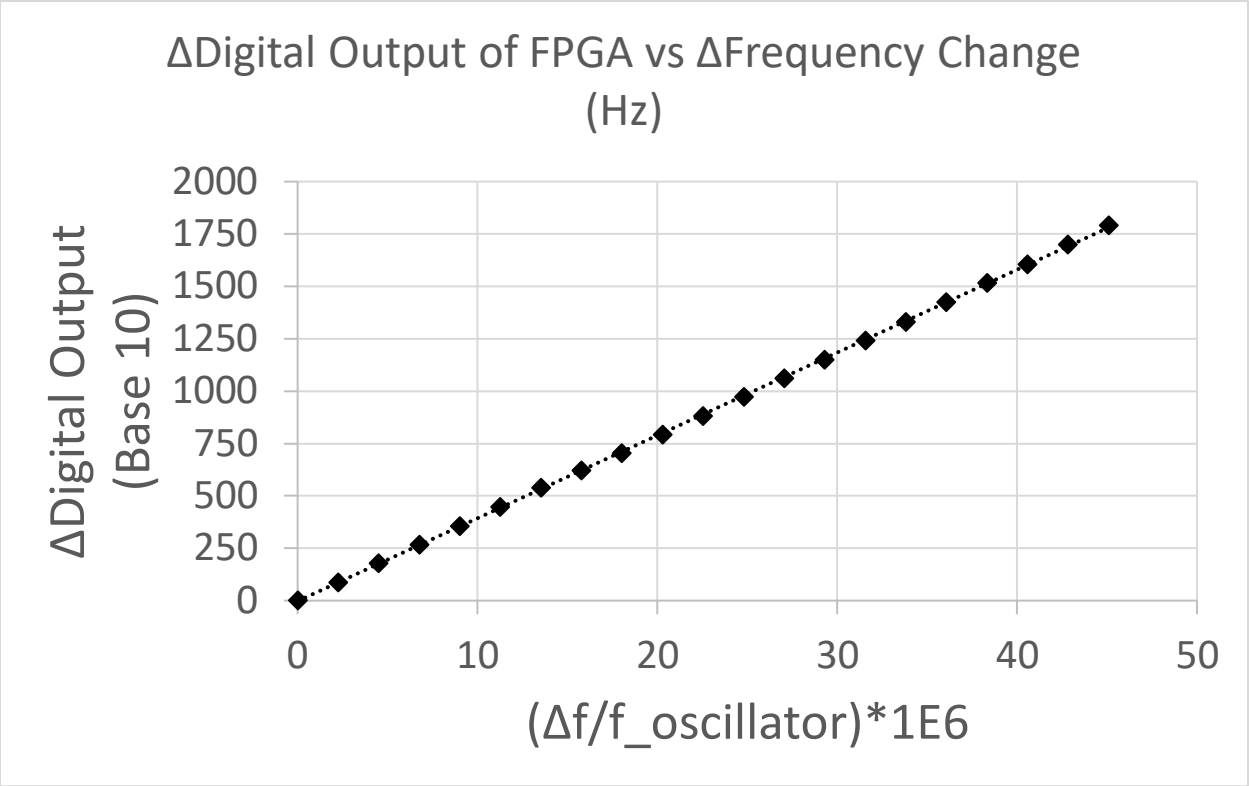

Figure 3.40: Digital Output code of FPGA vs Δf/f_oscillator, f_oscillator being the center frequency of the VCO (44.63MHz). Note the linearity.

Additionally, as this is a time varying system we also recorded the impulse response vs time of the system when we disturbed the Reference signal with a 10Hz step. It can be seen in Figure 3.41 how the phase is corrected by the loop in response to a frequency disturbance, and in Figure 3.42 it can be seen how the digital output code reacts to the disturbance, measuring at a new value.

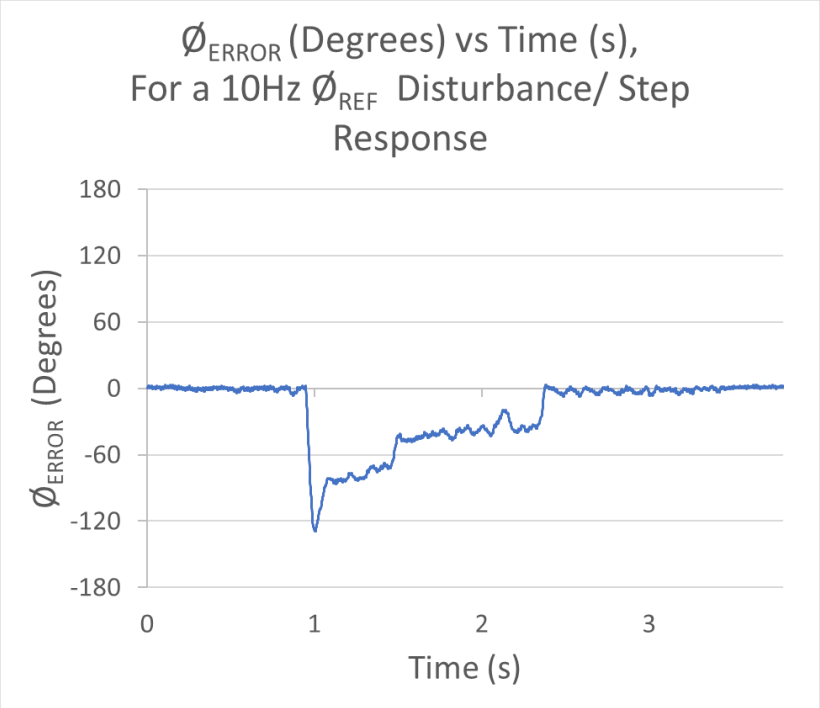

Figure 3.41: Phase error $Ø_{Error}$ vs time for a 10Hz impulse reseponse. It can be seen how the digital PLL corrects for the phase and brings it back to the zero.

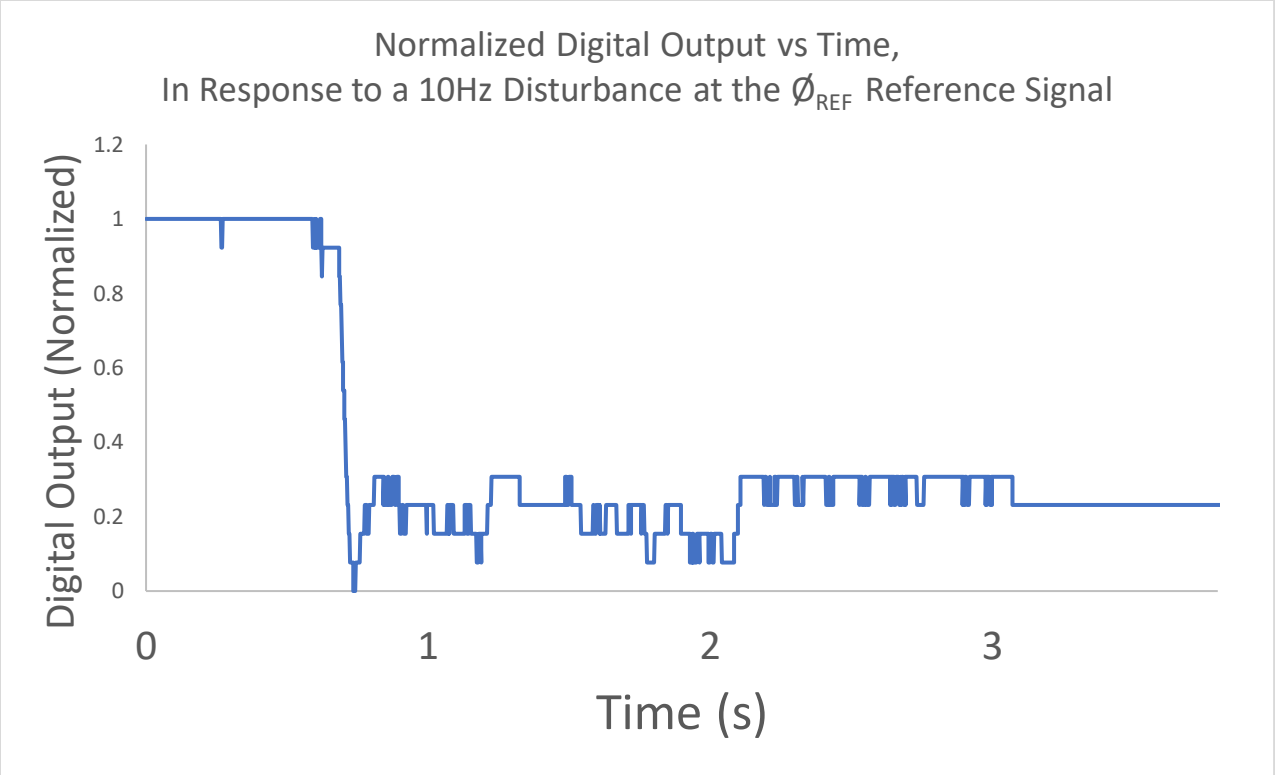

Figure 3.42: Normalized Digital Output vs Time, in response to a 10Hz Disturbance at the Reference Signal, for the same 10Hz response as shown in Figure 3.41.

We can see from above that the response acts like a second order differential equation with underdamping in response to the 10Hz impulse response. With better tuning of the variables Ki and Kp, this response could be tuned to an optimal value.

3.6.5 Discussion

With the above results, we found the digital code changed by 1791 decimal values, or 10.8 bits in response to a 2 khz frequency change. Given that the full range of the frequency disturbance range was 245 khz (1.508 MHz – 1.263 MHz), this can be extrapolated to 17.74 bits of possible detection resolution. Obviously, with the inclusion of noise, INL, and DNL, the actual resolution should be expected to be much less, requiring the whole range to be measured. This could be done over an extended period of time, but

a more practical solution would be decreasing the latency, so the cycle-slip problem did not occur if lock was lost.

Combining the change in capacitance to change in pressure relation of 4.6fF per kPa of pressure, the normalized change in frequency of 3.28e-05 frequency change per fF, and the code change of 3.97E6 per normalized frequency change, we estimate a sensitivity of 0.167 pA per bit of information if all systems were connected. The real resolution of course would have much less resolution due to INL, DNL, and other noise factors.

Given the results, it seems the discrete-part digital PLL we constructed demonstrated first-hand the potential of the digital-PLL concept as useful for capacitive-to-digital conversion, and with further work can be made very high performance.

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Chapter 4: Conclusion and future works

4.1 Summary

In this thesis, we proposed a new class of microstructure-based direct digital capacitive pressure sensor, including the microstructured pressure-to-capacitance transducer and its capacitance-to-frequency digital conversion circuitry. The microsturctured transducer design provides ease of fabrication and long-term durability. The novel sensor circuit using digital phase-locked-loop (PLL) enables highly sensitive detection of capacitance. Full implementation of the proposed sensor system, including taped out circuits and system-on-chip integration, requires years of tedious works and I am not able to finish within my master study. Thus, I carried out proof-of-concept demonstration. I first fabricated and characterized the microstructured transducer, and then constructed the digital PLL using discrete parts. The experimental results and analysis show the viability of implementing such sensor system in the future.

For the microstructured sensor (or called transducer), the fabrication was done using conventional semiconductor fabrication process. At first, a photolithography mask was made to achieve various sensor geometries. Then, sensors with different designs were fabricated. Finally, the capacitance values of those sensors were characterized using the Keithley 4200 Parameter Analyzer in the nanoFAB at the University of Alberta. Simulation works were also performed to model the sensors. The capacitances obtained in simulation agree with experimental results. Inductance and resistance values of the sensor was simulated using the model and those values are used for further analysis in the design of sensor circuitry.

For the sensor circuitry, we have presented capacitance to digital converter using digital PLL. While PLL has been used for capacitance to digital conversion in literature, they need additional ADC. The digital PLL eliminates the need for any additional ADC rather directly converts the capacitance change to

a digital code. While doing so, it also provides several advantages, both power and chip area are reduced and at the same time it is less affected by noise. In this chapter we have shown that unlike analog PLL where VCO phase noise directly impacts control node voltage, in digital version we can frequency shape the noise and further improve the noise performance by appropriately choosing the loop parameters. The implemented 65nm IC and experimental hardware implementation of the digital loop validates this proposed approach.

4.2 Future works

In this thesis work, I only carried out proof-of-concept demonstration of the proposed microstructure-based direct digital capacitive pressure sensor using discrete parts. To implement the full system onto a chip, the following works are required.

First, the capacitive pressure sensor (or transducer) would need to be physically integrated with the digital controlled oscillator IC of the sensor circuit. At first, the sensor size would have to be reduced to a smaller size than the full 4” wafer in a more professional form, which includes steps such as reducing the gap-height so the electrode pattern could be made smaller and the removal of the sensor from the 4” wafer by dicing. Then, the sensor would have to be wire-bonded to the IC due to the tight restrictions on the maximum parasitic inductance/capacitance specifications to allow the circuit to work, requiring both wire-bonding facilities and an IC designed for said wire-bonding. Finally, from a practical perspective, a new testing set-up would be required that could both measure the capacitance, inductance, resistance of the sensor and apply pressure to the capacitive sensor while it is attached to the entire system.

Second, the implementation of a full digital-PLL system utilizing a TDC circuit on a single IC chip is required, versus the discrete-part PLL demonstration done in this thesis. To achieve this goal, the first step would be to test the fabricated 65nm digital oscillator with a tunable capacitor. These experimental data could be compared with simulation results to find which parts of the simulation need to be changed to

account for parasitics and the deviations between the approximate circuit model and the real-world circuit. A second design could be produced to include an optimized digitally-controlled-oscillator (DCO) with improved performance and more tuned to the properties of our capacitive pressure sensor. As well, the rest of the digitally controlled circuit would need to be constructed along with the DCO which would include the TDC used to measure the frequency of the DCO, a precision frequency divider circuit, the programmable digital loop-filter, and the circuitry used for the sensor connection point.

Finally, all three connection types (direct-connection, tuned direct connection, and inductive coupling) of the closed-loop PLL circuit to the capacitance pressure sensor would need to be completed and evaluated. For the method of inductive coupling, a precision chip-bonding method would be required to position the micron sized inductors of the pressure sensor on top of the sensor-reading IC circuit so that their respective inductors can electromagnetically couple to the circuit.

In summary, the proposed microstructure-based direct digital capacitive pressure sensor can be achieved using the system-on-chip configuration in the future. This will enable a broad new applications of capacitive pressure sensors with superior speed, accuracy, and power savings.

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