Flexible Time-Stepping Dynamic Emulation of AC/DC Grid for Faster-Than-SCADA Applications

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***Abstract*—Dynamic simulation of the integrated AC/DC grids plays a crucial role in the energy control center. In this work, a faster than supervisory control and data acquisition (FT-SCADA) emulation based on flexible time-stepping (FTS) algorithm is proposed for the energy control center to predict and mitigate the impacts after serious disturbances using field-programmable gate arrays (FPGAs). To gain a high acceleration over SCADA/real-time, the FTS-based dynamic emulation is applied to the AC grid, which is the IEEE 118-bus system where a 9^{th}-order synchronous machine model is adopted. Meanwhile, the electromagnetic transient (EMT) emulation revealing the exact performance of the DC grid provides an insight into the impact on its AC counterpart. A power-voltage interface is inserted between the AC and DC grids since distinct emulation strategies are utilized, and the EMT-dynamic co-emulation is able to run concurrently on FPGA boards due to their massive parallelism. Three case studies are emulated to demonstrate the efficacy of the proposed algorithm, and a minimum of 101 times faster-than-SCADA/real-time can be achieved. Hence, following the occurrence of a disturbance, the FT-SCADA/RT emulator will generate an optimal solution in advance to maintain the stability of the hybrid AC/DC grid. The results of the FTS-based FT-SCADA/RT emulation are validated by the off-line transient stability simulation tool TSAT of the DSATools suite.**

***Index Terms*—AC/DC grid, dynamic simulation, electromagnetic transient, faster-than-SCADA, faster-than-real-time, field programmable gate arrays (FPGAs), flexible time-step, hardware emulation, parallel processing, predictive control, phasor measurement unit.**

I. Introduction

MODERN power systems are increasingly complex due to the interconnection between high voltage direct current (HVDC) and renewable energy, which makes the simulating, analyzing, and controlling the network difficult. Dynamic security assessment (DSA) is applied in power systems to ensure their stability and security. A complete DSA is composed of five stages [1]: measurements, modeling, computing, visualization, and control. The real-time measurements are captured by the supervisory control and data acquisition (SCADA) for basic state estimation, and then a detailed time-domain simulation is carried out for imminent contingencies. The obtained security indices are delivered to the system operators in the energy control center. The entire DSA cycle is conducted within 10-30 minutes to ensure that the operators have sufficient time to take remedial actions.

Due to the enormous computational burden in DSA systems and the expansion of power system scale, the hardware resources are stretched. For instance, to realize near real-time simulation of a power transmission system with more than 50,000 nodes and 3000 generators, the DSA is conducted on the supercomputer with more than 24,000 CPU cores for power system parallel simulation [2], which occupies a lot of hardware resources. On the other hand, the SCADA system collects data from the field every 2-5 s [3], this may be sufficient for steady-state tasks such as online power flow or state estimation, however, it falls short of predicting system stability and conducting online dynamic security assessment. The phasor measurement unit (PMU) technology provides a faster refresh rate (50/60 samples per second [3]) which is at least two orders of magnitude faster than SCADA, however, PMUs are expensive and cannot be installed on a wide-area to gather system dynamic situational awareness. Moreover, even if PMUs were widely deployed, communication delays to the energy control center would still exist.

In a real power system, the distributed and multi-input-multi-output (MIMO) wide-area damping controllers are also applied to mitigate the inter-area oscillations and reduce the computational burden. The MIMO controller of the power system can be estimated directly without the need for having a detailed model of the power system. Once the changing dynamics/operating points of the system are captured in the measured data, the MIMO model can be used for mode and control loop estimation. However, the MIMO identification of the power system, estimation of the control loops, and the design of the discrete linear quadratic regulator (DLQR) are done every 4s [4], and due to the slow rate of state estimation, MIMO identification is insufficient for real-time or faster-than-real-time estimation. The PMU based wide-area control of static synchronous compensator [5], on the other hand, has main restrictions such as the communication time-delay and the synchronization issues of wide-area controllers, which make them unsuitable for the FT-SCADA/RT emulation. Therefore, an integrated hardware platform based on FPGAs is established in this work for FT-SCADA/RT purpose so as to predict system dynamics faster and to take preventive control actions for mitigating the impacts of serious disturbances.

To provide fast, accurate, and time-synchronized data for the complex AC/DC grids, a high-fidelity simulation strategy is also needed. Traditional off-line dynamic simulation tools such as

Manuscript received June 19, 2020; revised September 24, 2020 and November 3, 2020; accepted November 15, 2020. Date of publication November 19, 2020; date of current version April 19, 2021. This work was supported by the Natural Science and Engineering Research Council of Canada (NSERC). Paper no. TPWRS-01013-2020. *(Corresponding author: Shiqi Cao.)*

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Color versions of one or more of the figures in this article are available online at https://doi.org/10.1109/TPWRS.2020.3038850.

Digital Object Identifier 10.1109/TPWRS.2020.3038850

PSS/E, and DSATools/TSAT apply fixed time-steps, and so do all commercial real-time simulators, which, as noticed, will require more hardware resources and prolong the simulation when the system scale becomes larger. A complex matrix solution is inevitable during the transient stability simulation and the admittance matrix will increase along with the system scale. Although the real-time simulation can be reached with the help of the high-performance processors [6]-[9] and the parallel algorithms [10]-[12], the execution time will increase along with the dimension of the admittance matrix. Some improved numerical methods are thereby put forward for accelerating the simulation, such as parallel-in-time [13]-[14], and parallel-in-space methods [15]-[17]. Although these methods help to accelerate the operation speed, the excessive iteration requirement of the parallel-in-time algorithm, as well as the difficulties in the programming of the parallel-in-space algorithm limit their widespread application. The variable time-steps (VTS) algorithms are also proposed for speeding up time-domain simulations, however, the varying time-steps of these methods are either doubled or halved during the dynamic simulation [18]-[21], which is inflexible once a serious fault occurs.

As various equipment have different dynamic responses to time-step, the local equipment based flexible time-stepping for FT-SCADA/RT emulation is proposed in this paper, which is able to decide a proper time-step for each circuit part. The proposed flexible time-stepping algorithm is applied on the integrated AC/DC network for FT-SCADA/RT emulation. The multi-terminal HVDC grids undergoing electromagnetic transient (EMT) simulation are utilized to enhance the stability of the traditional AC transmission system. Various contingencies, such as three-phase-to-ground fault, generator outage, and sudden load change are emulated to reveal the efficiency of the proposed local equipment based flexible time-stepping algorithm. The FT-SCADA/RT hardware emulation is suitable for a real power control center to predict the system's stability, as well as to select an optimal control strategy after a serious disturbance occurs.

The paper is organized as follows: Section II introduces the proposed flexible time-stepping method. The detailed modeling of the hybrid AC/DC grid including its interface is specified in Section III and Section IV focuses on the hardware design. The flexible time-stepping based FT-SCADA/RT emulation results and subsequent analysis are given in Section V. Section VI presents the conclusion and future work.

II. Flexible Time-Stepping Algorithm for Dynamic Emulation

A. Transient Stability Emulation Methodology

A practical power transmission system includes synchronous generators, buses, transmission lines, as well as various loads. The differential equation (1) describes the dynamic process of the synchronous machines and will be explained in detail in the following section. And the remaining components contribute to the algebraic equations which solve the network in conjunction with stator voltages of the generators.

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, \mathbf{u}, t), \tag{1}$$

$$\mathbf{g}(\mathbf{x}, \mathbf{u}, t) = 0, \tag{2}$$

where $\mathbf{x}$ refers to the vector of state variables, and $\mathbf{u}$ represents the bus voltages of a typical power system. The initial conditions can be written as:

$$\mathbf{x}_0 = \mathbf{x}(t_0). \tag{3}$$

Notice that the main challenge of emulating a power transmission system is basically solving a series of differential algebraic equations (DAEs). Due to the non-linear nature of the equations, the Newton-Raphson (NR) algorithm is required. The NR algorithm is essentially an iterative method, which is not ideally suited for parallel design in FPGAs due to the inherent sequence of iterations until convergence. The explicit methods such as Forward Euler, or 4^{th}-order Runge-Kutta (RK4) are applied in hardware emulation due to the low resource usage. In a trade-off between emulation efficiency and the accuracy, RK4 is adopted as the solution for calculating the non-linear DAEs, as given below:

$$RK_1 = dt \cdot f(t_n, x_n), \tag{4}$$

$$RK_2 = dt \cdot f\left(t_n + \frac{dt}{2}, x_n + \frac{RK_1}{2}\right), \tag{5}$$

$$RK_3 = dt \cdot f\left(t_n + \frac{dt}{2}, x_n + \frac{RK_2}{2}\right), \tag{6}$$

$$RK_4 = dt \cdot f(t_n + dt, x_n + RK_3), \tag{7}$$

$$x_{n+1} = x_n + \frac{1}{6}(RK_1 + 2RK_2 + 2RK_3 + RK_4), \tag{8}$$

where x_n refers to the state variables of the synchronous generator, dt is the emulation time-step.

B. Proposed Flexible Time-Stepping Algorithm

1) Flexible Time-Stepping: As mentioned above, all the DAEs should be discretized into numerical equations. The local truncation error is an estimate of the error introduced in a single time-step. Assuming that x_{n+1} is the calculated state variable, and $x(t_{n+1})$ refers to the corresponding exact value, the LTE can be expressed in the following equation:

$$LTE = x(t_{n+1}) - x_{n+1}. \tag{9}$$

Theoretically, LTE exists in both implicit and explicit numerical integration methods. However, it is difficult to find the exact value which is $x(t_{n+1})$ in a non-linear system. The approximate values can be solved by iterative methods or explicit integration methods using the results of the previous time-step, which means the exact state variables cannot be obtained directly in a non-linear system due to the time-varying state equations. Multistep integration approximations have higher precision than low-order integration methods. The results from the higher-order integration methods are treated as the exact values, the time-step can be resolved according to the true values. Taking the 5^{th}-order Adams-Bashforth (AB5) for example, the predicted value of the next time-step can be expressed as follows:

$$\dot{x} = F(t, x(t)), \tag{10}$$

$$\bar{x}_{n+1} = x_n + \frac{dt}{720} \cdot (1901F_n - 2774F_{n-1} + 2616F_{n-2} - 1274F_{n-3} + 251F_{n-4}), \tag{11}$$

where $\bar{x}_{n+1}$ is the predicted state variable of the next time-step, dt refers to the time-step. As the exact values are solved from AB5, the adaptive time-step ($\widetilde{dt}$) can be obtained as:

$$\widetilde{dt} = \frac{6(\bar{x}_{n+1} - x_{n+1}) \cdot dt}{(RK_1 + 2RK_2 + 2RK_3 + RK_4)}. \tag{12}$$

The principle of LTE-based variable time-stepping algorithm is as follows: if the LTE is larger than the predefined threshold ϵ, which is given in (13), the time-step is decreased to obtain higher accuracy and vice versa.

$$\epsilon = \left| \frac{\bar{x}_{n+1} - x_{n+1}}{\bar{x}_{n+1}} \right| \times 100\%. \tag{13}$$

According to (13), the calculated adaptive time-step could be extremely small after the occurrence of a disturbance. A restriction for the calculated time-steps should be properly designed. In order to maintain the emulation accuracy, the lower limit for the proposed flexible time-stepping algorithm is 1 ms. The upper limit is equally important because a large time-step could cause numerical divergence during the transient stability simulation. In this work, the upper limit of time-step is 10 ms, which can guarantee the emulation speed and prevent the system from diverging.

As can be seen, traditional LTE-based variable time-stepping algorithms are discrete. The time-step is doubled or halved until it reaches the upper or lower limit. With discrete time-steps, the calculated values may not be perfectly suitable for the specific step. The proposed flexible time-stepping strategy is able to yield a proper time-step instantly. In the traditional VTS algorithm, the time-step will be halved or doubled several times; in the meantime, the DAEs solved by the numerical integration method will also be calculated in each iteration until a suitable time-step is found. Therefore, the proposed flexible time-stepping algorithm can significantly reduce the computational burden and execution time.

2) Event-Based Flexible Time-Stepping: This algorithm is relative to the contingencies taking place in the system, such as three-phase-to-ground fault, generator outage, or sudden load change. In a dynamic transient emulation system, after a serious disturbance, the synchronous generators may lose synchronism, resulting in a rapid change of output voltages and generator rotor angles. Therefore, the rate of change voltage and rotor angle (dv/dt, $d\delta/dt$) can be treated as the main time-step control indices. When dv/dt or $d\delta/dt$ in a specific time-step change significantly, the time-step can be reduced or increased to ensure accuracy. This method has lower sensitivity than the flexible time-stepping algorithm, it is usually executed in a relatively large time-step, and therefore can significantly reduce the emulation time.

3) Local Equipment Based Flexible Time-Stepping: According to the sensitivity and stability of the various components in the power transmission system, different time-stepping control strategies are applied, which is beneficial to reduce the computational burden in low sensitivity parts. While the utilization of various time-stepping strategies may lead to an asynchronous time instant at the interface, which may lead to emulation unstable. Therefore, a hybrid time-step control algorithm should be generated. For instance, the output mechanical torque (T_m) of the governor system in the synchronous generator has a low sensitivity to time-step variation; in other words, a relatively large time-step will not influence the stability of the governor system. The event-based variable time-stepping method which provides time-steps ranging from 5-10 ms is employed in the generator control system as shown in Fig. 1(a). To ensure the accuracy of the mechanical and electrical parts, the flexible time-stepping strategy should be adopted, which is usually executed in small time-steps after a disturbance occurs.

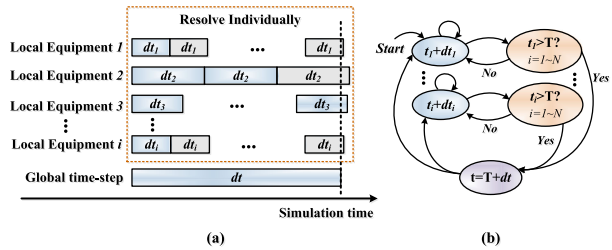

Fig. 1. Local equipment based flexible time-stepping for hybrid AC/DC grid emulation: (a) principle of the proposed algorithm, (b) time instant synchronization.

The local equipment based flexible time-stepping algorithm contributes a localized time-step dt_i produced in each component. Once a disparity emerges among local time-steps, the emulation goes forward only when the time instants of all variable time-stepping systems exceed the global time-step which is determined by the largest time-step of the subsystems. In the proposed emulation platform, the generator control systems are always computed with the largest time-step, which is therefore chosen as the global time-step. The synchronization mechanism works as follows: the control systems proceed at a much lower sample frequency, and they enter the next time-step only when the time instants of all local equipment reach beyond their current value; otherwise, all the components are computed individually while the global system waits for them to finish. The time instant synchronization of the local equipment based flexible time-stepping algorithm is given in Fig. 1(b).

III. AC/DC Grid Components Modeling

A. AC/DC Grid Interface

Fig. 2 shows a typical integrated AC/DC grid, where the IEEE 118-bus test systems [22], [23] are connected with four-terminal (4-T) HVDC systems at Bus 25 and Bus 54. *MMC*3 and *MMC*4 act as rectifier stations, while *MMC*1 and *MMC*2 are treated as inverter stations. The IEEE 118-bus systems undergoing the transient stability analysis have a flexible time-step ranging from 1 ms to 10 ms. On the other hand, to reveal the dynamic process of the 4-T HVDC, the electromagnetic transient (EMT) simulation is adopted for the DC grid, which has a fixed time-step of 200μs. The local equipment based flexible time-stepping is applied for establishing an integrated co-emulation time-step scheme. Due to the distinct emulation strategies of the AC and DC grid, a proper interface should be designed.

In this case, the converter stations are utilized for delivering power among IEEE 118-bus systems. The converters can be treated as time-varying P+jQ loads, which means both P and Q values are updated in every time-step to reveal the dynamic

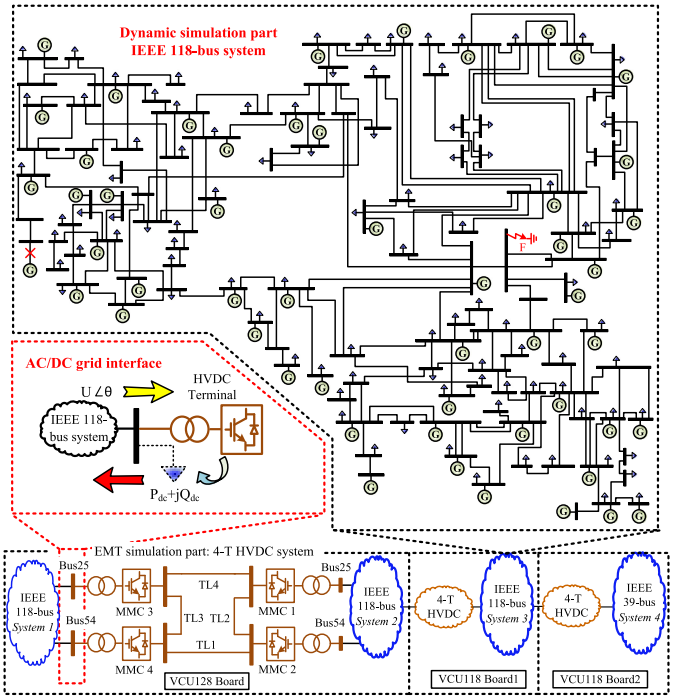

Fig. 2. Integrated AC/DC grid for dynamic-EMT co-emulation.

process of the converter stations. At the point of common coupling (PCC), the power injections of MMC stations can be calculated in (14) and introduced in the admittance matrix of the AC network:

$$Y_{Load} = \frac{(P_{Load} + j \cdot Q_{Load})}{V_{Bus}^2}. \tag{14}$$

The instantaneous voltages represented by a combination of amplitude U and phase angle θ at PCC are treated as the input of the EMT emulation. Hence, the mechanism of the interface strategy is as follows: the EMT emulation of MMC stations provide the time-varying P+jQ loads to the AC transmission system at the coupling bus, and the updated P+jQ loads act as the input of the AC grid for calculating the admittance matrix and subsequently solve the differential equations of synchronous generators and network equations in parallel. The resulting coupling bus phase voltages $U\angle\theta$ are in turn delivered to the DC grid. Meanwhile, step control should also be considered due to various time-steps in AC and DC grid, and the mechanism is similar to that of the flexible time-stepping algorithm. For instance, the DC and AC grids adopt a fixed time-step of 200μs and 1 ms during and after a disturbance, respectively. Therefore, each AC grid computation is accompanied by 5 independent DC grid calculations for synchronization of time instants in both grids.

In the proposed EMT and transient stability co-simulation of the hybrid AC/DC grid, the bus voltage angle can be directly obtained from the solution of the AC network equations, and therefore, the PLL is not used in the converter controller. Due to parallelism in the DC grid, the PLL has no impact on the emulation speed, albeit the hardware resource utilization increases slightly, as shown in Table II. To emulate the integrated AC/DC grid with high accuracy and low hardware resource burden, and also due to the fact that the PLL can trace the PCC phase angle instantly, it is reasonable to adopt the calculated phase angle.

TABLE I
LATENCY AND RESOURCE CONSUMPTION OF DETAILED MMC MODEL

Module	BRAM	DSP	FF	LUT	Latency
MMCDetailed	0	75	25418	40960	170 T_{clk}
MMCCNT	0	58	10013	19077	185 T_{clk}
MMCNetwork	0	20	2958	2868	185 T_{clk}

TABLE II
SPECIFICS OF MAJOR AC/DC GRID HARDWARE MODULES

Module	BRAM	DSP	FF	LUT	Latency
MMCCNT	0	54	5733	11085	85 T_{clk}
MMCAVM	16	208	8292	19277	90 T_{clk}
DCGrid	0	17	2209	2868	73 T_{clk}
PLL	0	8	892	1357	18 T_{clk}
YMatrix	12	1045	123388	126767	1470 T_{clk}
RK4	0	36	6970	7520	83 T_{clk}
AB5	0	98	12013	21077	135 T_{clk}
FTS	0	12	521	780	18 T_{clk}
Network	16	534	43928	57664	269 T_{clk}
Governor	0	17	3783	4598	29 T_{clk}
Update	0	38	4951	6875	33 T_{clk}
Total	44	4758	753450	848458	1873 T_{clk}
	1.02%	69.56%	31.87%	71.76%	–
XCVU9P	4320	6840	2364480	1182240	–

B. AC Grid Modeling

The main components in the AC grid are synchronous generators and networks. The synchronous generator model contains the mechanical part, electrical part, and excitation system. The transmission lines, compensators, as well as loads, contribute to the network.

1) Synchronous Machine Model: As mentioned in Section II, the differential equation (1) represents the dynamics of a synchronous generator which has nine state variables. Among the 9^{th}-order differential algebraic equations (DAEs), the mechanical equations which refer to the derivative of rotor angle and angular velocity are given below:

$$\dot{\delta}(t) = \omega_R \cdot \Delta\omega(t), \tag{15}$$

$$\Delta\dot{\omega}(t) = \frac{1}{2H}[T_e(t) + T_m(t) - D \cdot \Delta\omega(t)]. \tag{16}$$

The rotor electrical circuit equations adopt two windings on the d-axis and two damping windings on the q-axis, which can be expressed as:

$$\dot{\psi}_{fd}(t) = \omega_R \cdot [e_{fd}(t) - R_{fd} i_{fd}(t)], \tag{17}$$

$$\dot{\psi}_{1d}(t) = -\omega_R \cdot R_{1d} i_{1d}(t), \tag{18}$$

$$\dot{\psi}_{1q}(t) = -\omega_R \cdot R_{1q} i_{1q}(t), \tag{19}$$

$$\dot{\psi}_{2q}(t) = -\omega_R \cdot R_{2q} i_{2q}(t). \tag{20}$$

Meanwhile, the control system of the synchronous generator includes automatic voltage regulator (AVR) and power system

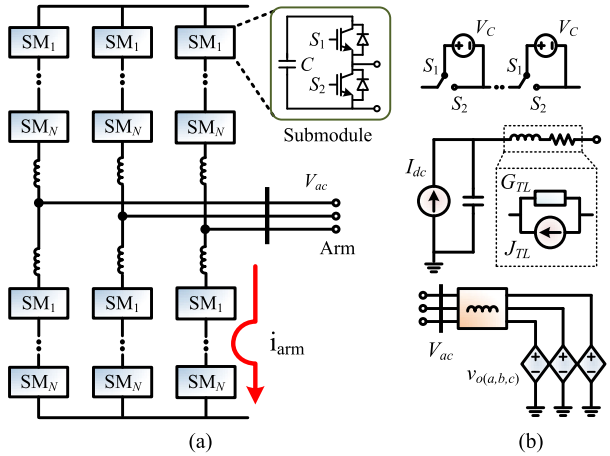

Fig. 3. Illustration of modular multilevel converter modeling: (a) three-phase topology, (b) average value model.

stabilizer (PSS), and the differential equations have the following expression:

$$\dot{v}_1(t) = \frac{1}{T_R} \cdot [v_t(t) - v_1(t)], \tag{21}$$

$$\dot{v}_2(t) = K_{stab} \cdot \Delta\dot{\omega}(t) - \frac{1}{T_\omega} v_2(t), \tag{22}$$

$$\dot{v}_3(t) = \frac{1}{T_2} \cdot [T_1 \dot{v}_2(t) + v_2(t) - v_3(t)]. \tag{23}$$

Therefore, $\mathbf{x}$ in (1) is a 9×1 vector for a single generator, which can be formulated as:

$$\mathbf{x} = [\delta, \Delta\omega, \psi_{fd}, \psi_{1d}, \psi_{1q}, \psi_{2q}, v_1, v_2, v_3], \tag{24}$$

where the meanings of the constant values in (15)-(23), such as ω_R, H, D, R_{fd}, R_{1d}, R_{1q}, R_{2q}, T_R, K_{stab}, T_ω, T_1, and T_2 can be found in [24].

2) AC Network Model: The main components in the AC network include transmission lines, compensators, and loads, where the fixed compensators and loads can be expressed as (14). The transmission lines are represented by a lumped π equivalent circuit. The DC system taken as loads at the AC/DC coupling points will be updated in every time-step. Therefore, all the components of the AC/DC network can be included in a single admittance matrix.

Sharing the same admittance matrix, the generators are solved together with the AC network in the following equation:

$$\begin{bmatrix} \mathbf{I_m} \\ \mathbf{I_r} \end{bmatrix} = \begin{bmatrix} \mathbf{Y_{mm}} & \mathbf{Y_{mr}} \\ \mathbf{Y_{rm}} & \mathbf{Y_{rr}} \end{bmatrix} \begin{bmatrix} \mathbf{V_m} \\ \mathbf{V_r} \end{bmatrix}, \tag{25}$$

where m and r represent the number of synchronous generator nodes and the number of remaining nodes, respectively. Since the current injections remain zero on the non-generator buses, i.e, $\mathbf{I_r} = [\mathbf{0}]$, the voltages of the remaining buses can be solved directly.

C. DC Grid Modeling

1) Modular Multilevel Converters: Fig. 3(a) provides the most common type of half-bridge MMC model, which is treated as the converter station in an HVDC grid. The operating principle is as follows: Once the upper IGBT is switched-on and the lower IGBT is switched-off the capacitor will charge or discharge depending on the direction of the arm current i_{arm}. In contrast, when the upper IGBT is switched off and the lower IGBT is switched-on the capacitor is bypassed. Therefore the submodule voltage V_{SM} can be express as the following equation:

$$V_{SM} = \int (\frac{i_{arm}}{C}) dt + i_{arm} \cdot r_{on}, (V_{g1} = 1) \tag{26}$$

where V_{g1} is a binary denoting the gate signal of the upper switch S_1, if $V_{g1} = 1$, the upper IGBT is switched-on, and r_{on} represents the on-state resistance of the switch.

2) MMC Average Value Model: A brief introduction of the MMC average value model (AVM) is presented here, further information can be found in [25]-[26]. In steady-state, assuming that the MMC is internally balanced [27], then each submodule can be treated as a voltage source as given in Fig. 3(b). The equivalent voltage source can be expressed as

$$\begin{cases} v_{sm(i)}(t) = \frac{V_{dc}}{N}, (V_{g(i)}(t) >= V_{th}) \\ v_{sm(i)}(t) = 0, (V_{g(i)}(t) < V_{th}) \end{cases} \tag{27}$$

where $V_{g(i)}(t)$ refers to a time-varying gate signal of the upper IGBT, V_{th} represents the threshold voltage, V_{dc} is the sum of all capacitor voltages of an arm. And the arm voltage equals to

$$v_{arm} = \sum_{i=1}^{N} v_{sm(i)} + L_{arm} \frac{di_{arm}}{dt}, \tag{28}$$

where L_{arm} represents the arm inductance.

Comparing with the detailed MMC model, AVM has the feature of lower latency under hardware implementation. Based on the proposed interface strategy, regardless the influences of the MMC model, there is no significant difference in power injection by using AVM and a detailed model. However, the detailed MMC model requires more hardware resources, as well as the detailed model being more sensitive to time-step. The latencies and hardware resources are given in Table I.With a maximum time-step of 50μs, the FT-SCADA/RT ratio of the detailed model can be calculated by $\frac{50\mu s}{185 \cdot 10ns}$, which is about 27 times faster-than-real-time. Therefore the AVM was chosen for hardware implementation.

IV. FT-SCADA/RT Emulation Platform on FPGAs

The hardware emulation of the hybrid AC/DC grids was conducted on Xilinx Virtex UltraScale+ FPGAs. The integrated hardware platform includes three FPGA boards: two VCU118 evaluation boards featuring the XCVU9P FPGAs and a VCU128 board with XCVU37P FPGA. Each XCVU9P FPGA includes 1182240 look-up tables (LUTs), 2364480 flip-flops (FFs), and 6840 DSP slices. The XCVU37P FPGA contains 9024 DSP slices, 1303680 LUTs, and 2607360 FFs. Two IEEE 118-bus systems connecting with one 4-T HVDC system are accommodated on the VCU128 board. The remaining parts are emulated on the two VCU118 boards, as shown in Fig. 2. The mechanism of the hardware design is as follows: the Xilinx Vivado package enables designing hardware modules by coding in C/C++ in its high-level synthesis (HLS) tool to shorten the design cycle; The components or functions which consist of the integrated

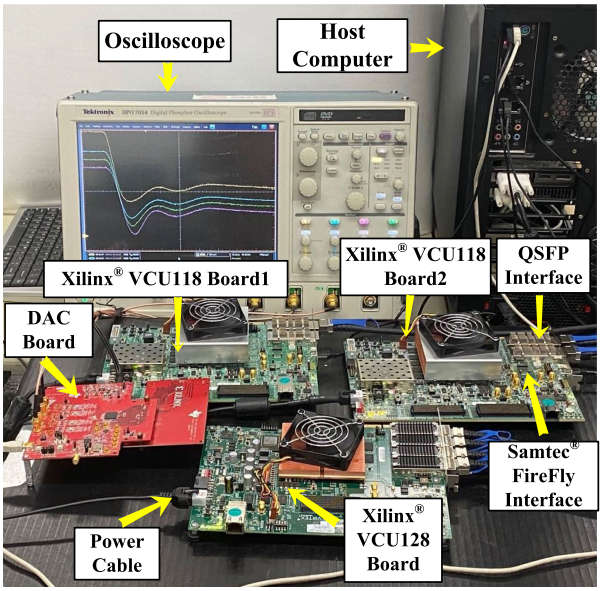

Fig. 4. Hardware setup for FT-SCADA/RT emulation.

AC/DC grid in Fig. 2 are transformed into a hardware module in HLS that can be imported into Vivado to form the top-level using the hardware description language VHDL. Fig. 4 shows the hardware configuration for the FT-SCADA/RT emulation.

In the integrated AC/DC grid, each subsystem and function can be designed as a reconfigurable hardware module, and the hardware-in-the-loop (HIL) emulation is achieved following proper connection of these modules and deployment onto the FPGA boards. For the FT-SCADA/RT emulation, the initial conditions and the functions are downloaded from the host computer via the joint test action group (JTAG) interface. The current operating conditions could be emulated on the FTRT platform based on the signals it receives. Each module reserves one or several input data channels for receiving real-time data. If a disturbance occurs, the received current operating conditions will be sent to the relative subsystems. The dynamic power injection data will be delivered to *Ymatrix* module and the output mechanical torque of the steam turbine will be calculated in the module, which represents the synchronous generator. With the required real-time data of the gird and the emulation model downloaded from the host computer, the FTRT predictive regulation control can be realized.

The main challenge of emulating such a complex hybrid AC/DC grid is data communication among the three boards. A communication strategy among the FPGA boards should be properly designed. The communication delay has always been a time-consuming part of DSA systems. The Xilinx Ultrascale+ series FPGA board provides more efficient communication ports, such as Quad Small Form-factor Pluggable (QSFP) and Samtec FireFly interfaces, for large data exchange with external devices or other FPGA boards. A maximum bidirectional data transmission speed of 4×28 Gbps provided by the dual QSFP cages accommodates delivering the current operating conditions from the real power transmission system or other FPGA boards. The Samtec FireFly connector provides up to 4×28 Gbps full-duplex bandwidth in four channels and realizes data communication from an FPGA to an industry-standard multi-mode fiber optic cable, which can be used for optical data communication as well as support cable lengths up to $100m$.

TABLE III
TIME-STEPS UNDER VARIOUS CONTINGENCIES

Contingencies	Time-steps in proposed algorithm	Time-steps in fixed time-step of $1ms$
Load Change	14664	30000
3-Phase Fault	14478	30000
Outage	15967	30000
Hardware execution time of proposed algorithm	Emulation time span	FT-SCADA/RT ratio
$274.56ms$	$30s$	109.23
$271.17ms$	$30s$	110.63
$296.18ms$	$30s$	101.29

The proposed interface strategy with less data transfer and the utilization of the QSFP interface will significantly shorten the communication delay. The VCU118 Board1 sends time-varying P and Q values calculated from the 4-terminal HVDC system to the VCU128 Board, and the instantaneous phase voltages are in turn delivered to VCU118 Board1 via the bidirectional QSFP interface, as given in Fig. 4. From each board's point of view, the P and Q values and the phase voltages are real-time measurements. In addition, the constantly updated P and Q values act as the inputs of the AC grid for calculating the admittance matrix, which can be treated as changing the network topology or dynamic conditions in every time-step.

Table II gives the hardware resources and the latencies of major modules on the VCU118 Board1, where the *MMCCNT* refers to the control system of MMC stations, *MMCAVM* represents the functions of MMC average value model, and *DCGrid* denotes the network equations of the DC grid. The modules in the 4-T HVDC system can be calculated in parallel. The latency of the DC grid is 90 T_{clk}, meaning with an EMT emulation time-step of 200μs, the FT-SCADA/RT ratio is over 222 with an FPGA clock cycle of 10 ns. Meanwhile, the *YMatrix*, *RK4*, *Network*, *Governor*, and *Update* denote the components in IEEE 118-bus system, where *YMatrix* refers to the functions for calculating the admittance matrix, *RK4* is the non-linear differential equation solver, *Network* represents the AC network equations given in (25), and *Governor* is the governor control system of synchronous generators. The proposed local equipment based flexible time-stepping algorithm is applied to the AC grids. The performances of the proposed flexible time-stepping are relative to the contingencies. For instance, a severe fault may lead to a long-term oscillation until the system reverts to steady-state, and the proposed algorithm will operate in a small time-step for a long period. Therefore, the total time-steps are different under various disturbances.

Table III gives the FT-SCADA/RT ratio, and the total time-steps in the AC system under various conditions. Although a relatively small time-step is adopted during or after the fault, and a minimum FT-SCADA/RT ratio of 101 can be achieved by utilizing the proposed flexible time-stepping method. If the EMT emulation time-step is reduced to 50μs, the FT-SCADA/RT emulation can still be realized. However, the FT-SCADA/RT

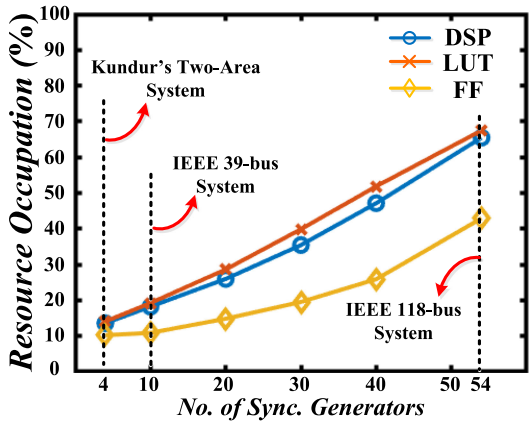

Fig. 5. Relationship between hardware resources and synchronous generators.

ratio could be highly dependent on the DC circuits, only 27 times faster than SCADA/real-time can be reached. Similarly, if the method of solving the DAEs switches to AB5 under a time-step of 1 ms during or after the disturbance, the accuracy can be guaranteed. However, the latencies of AB5 increase to 135 clock cycles as given in Table II, which are larger than RK4. To solve the DAEs during or after the occurrence of a fault, the RK4 is still chosen as the main method.

It is noticed that the hardware resources such as *DSP* and *LUT* are nearly full. The relationship between hardware resources and the number of synchronous generators is given in Fig. 5, where the synchronous machines are modeled in a set of 9^{th} order DAEs, and each generator has a governor system. The governor is mainly responsible for providing mechanical power P_m (the same as T_m in per unit) to the synchronous generator. Meanwhile, the control of mechanical power is regulated by the steam turbine, which is a relatively slow process. The input of T_m in *RK4* is provided by the results of *Governor* from the previous time-step, and thereby *RK4* and *Governor* modules can be calculated in parallel. Taking the IEEE 118-bus system as an example, the DSP utilization can be calculated as $(36+17)\times 54+1045+534+38=4479$, where the 54 refers to the number of generators. The DSP utilization of *RK4* and *Governor* modules are proportional to the synchronous machines. The remaining modules are solved in series in a specific time-step, such as *YMatrix* and *Network*. The hardware resources of those modules are directly related to the bus numbers and increase along with grid nodes. Therefore, the hardware resources are nearly proportional to the synchronous machines, and a single VCU118 FPGA board is able to accommodate about 70 synchronous generators in parallel.

V. FT-SCADA/RT Emulation Results and Validation

Various contingencies of the integrated AC/DC grid in Fig. 2 are emulated in the FT-SCADA/RT platform, and the results are validated by the off-line transient stability simulation tool TSAT in the DSATools suite.

A. Three-Phase-to-Ground Fault

At the time of 5 s, a three-phase-to-ground fault occurs at Bus 68 in *System 1*, as shown in Fig. 2. The impacts after

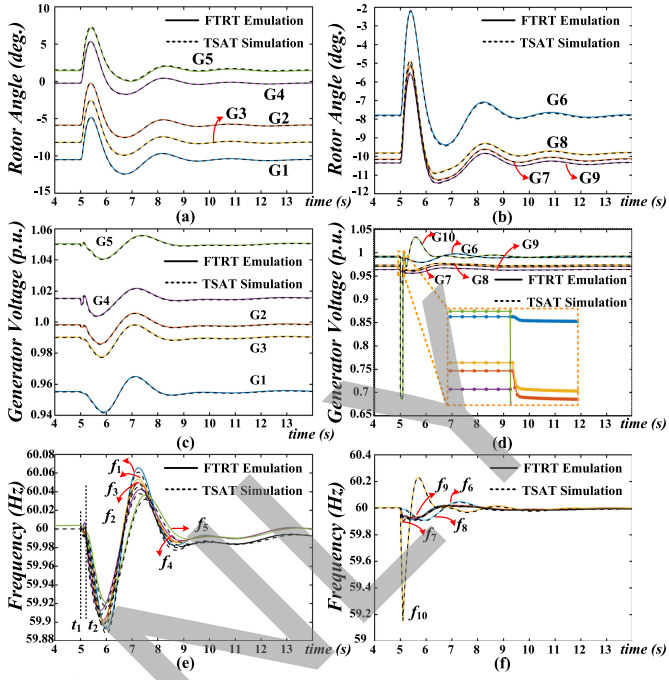

Fig. 6. FT-SCADA/RT emulation using FTS algorithm for preview of generator behaviours under AC system ground fault: (a) generator relative rotor angles (G1-G5), (b) generator relative rotor angles (G6-G9), (c) generator output voltages (G1-G5), (d) generator output voltages (G6-G10), (e) frequencies (G1-G5), and (f) frequencies (G6-G10).

the disturbance are severe to the AC system, including the generators' rotor angles, bus voltages, and the frequencies, as shown in Fig. 6. The synchronous generators lose synchronism after the ground fault as the relative rotor angles rise significantly as shown in Fig. 6(a) and (b). Meanwhile, in Fig. 6(c) and (d) the bus voltage of G5 decreases to $0.67p.u.$ in less than 0.1 s. The frequency of G10 plummets to $59.2Hz$ which is beyond the threshold of $\pm 1\%$ as shown in Fig. 6(e) and (f). At t_2=5.1 s, the three-phase-to-ground fault is cleared, and the system returns to the steady-state in about 5 s as given in Fig. 6.

In a real power transmission system, a more than 100 ms ground fault may lead to a stability issue. The long-term ground fault may lead to generator damage or subsynchronous resonance in a series compensated transmission system. Therefore, the flexible time-stepping based FT-SCADA/RT emulation is applied to the control center to predict or mitigate the oscillations after a severe disturbance. The zoomed-in plots in Fig. 6(d) and Fig. 9(a) show that the time-steps shrink right after the bus voltages drop. At steady-state, the time-step is 10 ms. Once the fault occurs, the time-step reduces to the lower limit to maintain accuracy.

B. Generator Outage and Sudden Load Change

At 5 s, the generator outage occurs at the generator G5. Fig. 7 shows the results of the rotor angles, generator voltages, and the frequencies before and after the contingency. The rotor angles of the generators decrease significantly after t_1, especially in G5, which is shown in Fig. 7(a) and (b). Meanwhile, the generator voltages decrease to $0.83p.u.$ in less than 0.2 s as shown in Fig. 7(c) and (d). Due to the robustness in a large

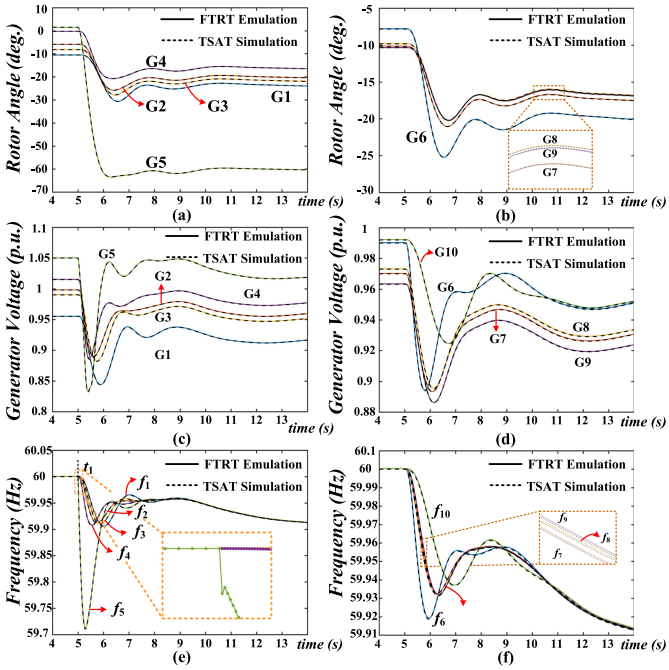

Fig. 7. FT-SCADA/RT emulation using FTS algorithm for preview of AC/DC grid behaviours under generator outage: (a) generator relative rotor angles (G1-G5), (b) generator relative rotor angles (G6-G9), (c) generator output voltages (G1-G5), (d) generator output voltages (G6-G10), (e) frequencies (G1-G5), and (f) frequencies (G6-G10).

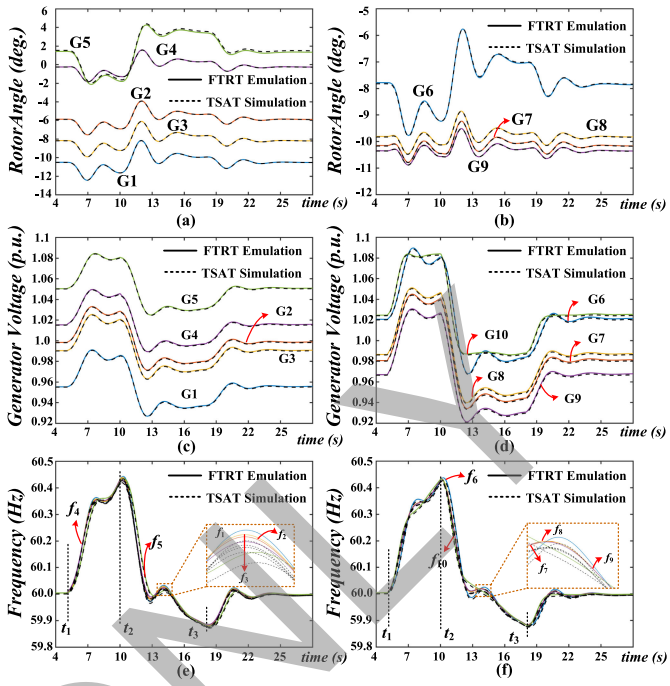

Fig. 8. FT-SCADA/RT based predictive control for power system stability analysis: (a) generator relative rotor angles (G1-G5), (b) generator relative rotor angles (G6-G9), (c) generator output voltages (G1-G5), (d) generator output voltages (G6-G10), (e) frequencies (G1-G5), and (f) frequencies (G6-G10).

power transmission system, the generator voltages and rotor angles may transfer to a new steady-state. The main impact of the generator outage contingency is the divisions on the frequencies. Fig. 7(e) and (f) present the frequencies drop to $59.7Hz$, which may cause the whole system to operate in a long-term unstable state. The zoomed-in plots in Fig. 7 (e) and Fig. 9(b) illustrate the proposed flexible time-stepping algorithm can significantly change time-steps after the occurrence of a disturbance to ensure the emulation accuracy. Meanwhile, a relatively large time-step is applied to accelerate the emulation.

The sudden load change disturbance happens at the load Buses 25 and 54 in IEEE 118-bus *System 1*. At $t_1 = 5.0$ s, a load of $200MW$ and $100MW$ are removed from Buses 25 and 54 respectively, causing the disturbance of the AC system which can not be restored even the loads are recovered at t_2=10 s to its original capacity of $277MW$ and $184MW$. The load change factor is relatively small in the large power transmission system, resulting in the slight changes in rotor angles and generator output voltages, as shown in Fig. 8 (a)-(d). However, the main impacts of the load change contingency are the frequencies, which reach the maximum allowed threshold of 1%. The power control center should select a proper strategy to mitigate the impacts after the load change. At t_2=10.0 s, *MMC*3 and *MMC*4 deliver extra $100MW$ and $50MW$ active power to Buses 25 and 54 respectively from IEEE 118-bus *System 1* to *System 2*. At t_3=18.0 s, the extra power injection is removed, and the whole system is therefore restored stable gradually in about 7 s. Introducing the HVDC system improves the stability of the integrated AC/DC grid by injecting active power into the AC grid or absorbing power from the AC system. The zoomed-in plots in Fig. 9(c) demonstrate that the proposed flexible time-stepping

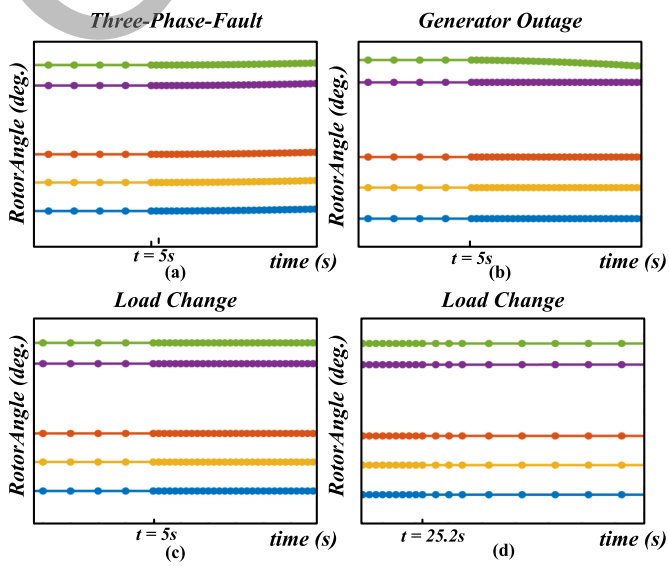

Fig. 9. Zoomed-in plots of rotor angles for three contingencies: (a) three-phase-to-ground fault (G1-G5), (b) generator outage (G1-G5), (c), and (d) sudden load change (G1-G5).

reduced the time-step to the lower limit for higher accuracy, and the time-step increases gradually when the system restores to a steady-state after the power injection, as shown in Fig. 9(d).

C. AC/DC Interface Results and Error Analysis

As mentioned before, the HVDC stations denoted by *MMC1* to *MMC4*, regardless of the type, i.e., rectifier or inverter, can be modeled as time-varying $P+jQ$ loads. The active power of

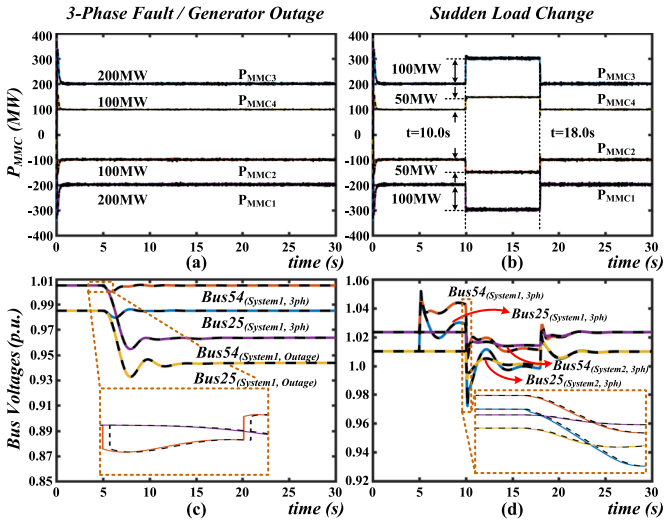

Fig. 10. AC/DC interface results.

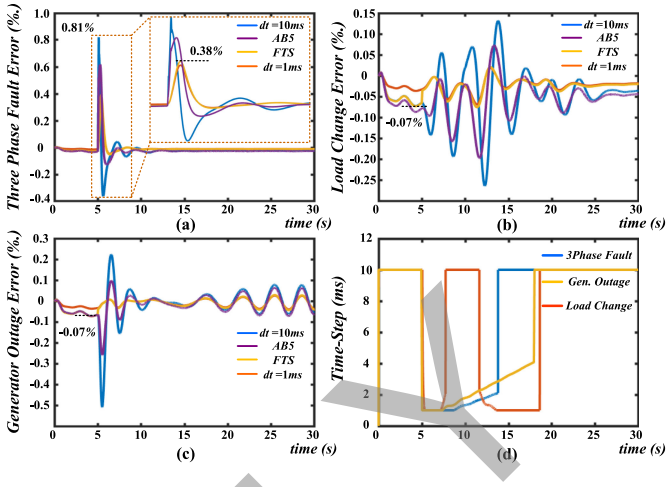

Fig. 11. (a)-(c) Relative errors compared with TSAT under various contingencies, (d) time-steps under various contingencies.

each converter station in the 4-T HVDC between IEEE 118-bus *System 1* and *System 2* is given in Fig. 10. Under the steady-state, IEEE 118-bus *System 1* delivers $200MW$ and $100MW$ to *System 2* from Bus 25 and Bus 54, respectively. The dashed lines in Fig. 10(a) and (b) refer to the received active power in the AC grid, in the meantime, dashed lines in Fig. 10(c) and (d) represent the input bus voltages of the DC system. The solid lines in Fig. 10(a)–(b) and (c)–(d) are the calculated active power and bus voltages in DC and AC grids, respectively. In the hardware emulation program, the DC part is calculated with the voltages and phase angles solved from the previous time-step in the AC system. The zoomed-in plots in Fig. 10(c) and (d) indicate that the receiving bus voltages of the DC system are always lagging the calculated voltages in the AC grid by one time-step.

During the three-phase to ground fault and generator outage, the output power of IEEE 118-bus *System 1* remains stable, as given in Fig. 10(a). The calculated interface bus voltages under the above two contingencies in *System 1* are provided in Fig. 10(c). After the sudden load change occurs, with the 109 times faster than real-time ratio, the power control center has sufficient time to come up with an optimum solution that helps maintain the synchronism of the generators and select the proper power that should be delivered by the HVDC system as given in Fig. 10(b). Meanwhile, Fig. 10(d) provides the interface bus voltages calculated in the AC grid in both *System 1* and *System 2*. Since in Fig. 10(a) and (b) the MMC stations undergo a dynamic process, the admittance matrix should be updated in every time-step to obtain practical emulation results.

In order to validate the accuracy and performance of the proposed method, Fig. 11(a)–(c) provide the relative errors of the rotor angle in Generator 1 under various contingencies, where the relative errors are calculated by the following equation:

$$\epsilon = \frac{V_{Calculated} - V_{TSAT}}{V_{TSAT}} \times 100\%. \tag{29}$$

Fig. 11(a)–(c) indicate that the maximum error appears when a serious contingency occurs. The maximum error among these three contingencies is merely 0.81%, which thoroughly demonstrates the accuracy of the proposed method. Fig. 11 (d) provides the adaptive time-steps of the synchronous machine model during the emulation. It shows that the time-step will shrink after the occurrence of a serious disturbance. Furthermore, the updated time-step avoids being halved or doubled several times according to (12), which means the proposed flexible time-stepping method is able to find a proper time-step instantly compared with the traditional variable time-stepping strategy.

VI. Conclusion

This paper proposed a flexible time-stepping based faster-than-SCADA/real-time transient stability analysis of the AC/DC grid. The local equipment based flexible time-stepping algorithm has the ability to modify the time-steps ranging from 1 ms-10 ms, which facilitates the FT-SCADA/RT emulation of a complex power transmission system on the FPGAs. Compared with the traditional variable time-stepping methods, the proposed algorithm can significantly reduce the computational burden by utilizing large time-steps under steady-state and small time-steps during or after a disturbance. Traditional variable time-step algorithms need several stages to find the appropriate time-step; in contrast, the proposed FTS scheme can achieve this instantly, and thus helps to further reduce the computational burden. On the other hand, the parallel architecture of the hardware platform makes transient stability emulation more efficient than traditional CPU based simulators. With the minimum FT-SCADA/RT ratio of 101, the energy control center has sufficient time to assess the dynamic security, predict power system responses, and select an optimal solution to maintain the system's stability. The results of flexible time-stepping based FT-SCADA/RT dynamic emulation are highly matched with the off-line dynamic simulation tool TSAT. Therefore, the FT-SCADA/RT emulation can help to rapidly mitigate the adverse impacts after a serious disturbance, which ensures the stability of the complex power transmission system. When more system contingencies need to be considered, the FT-SCADA/RT platform can be applied to accelerate contingencies screening and ranking in dynamic security assessment systems.

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