An Accurate and Fast Method for Conducted EMI Modeling and Simulation of MMC-Based HVdc Converter Station

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***Abstract*—The analysis of electromagnetic interference (EMI) noise of power electronic circuits involves both the transient characteristics of power semiconductor devices and the wideband stray parameters of passive equipment. Modular multilevel converters (MMCs) used in high-voltage direct current (HVdc) transmission systems contain thousands of submodules (SMs), which makes it considerably challenging to perform device-level simulation on the traditional commercial software. This article presents an accurate and fast method for wideband modeling and simulation of MMC-HVdc system for the assessment of conducted EMI during the design stage. Physical characteristics of the semiconductor devices, parasitic parameters of the insulated-gate bipolar transistor (IGBT) packages, and stray capacitances of the SMs are all taken into consideration, and massively parallel transient simulation of the wideband MMC model is carried out on the graphics processor (GPU). The accuracy and efficiency of the GPU-based parallel algorithm are validated by the comparison with the experimental measurement of an 11-level full-bridge MMC prototype. Furthermore, the stray capacitance network of the valve tower in HVdc project is extracted, and a matrix partition method based on the shielding plate configuration is utilized to conduct the computation in a fully parallelized manner. The developed GPU program is used to run the large-scale case of a 201-level two-terminal MMC-HVdc system, and the primarily affected frequency range by various factors is analyzed. Execution time test is conducted for different level topology, and it is demonstrated that the GPU can achieve a remarkable speedup over multicore CPUs, especially when the system scale is more substantial.**

***Index Terms*—Electromagnetic interference (EMI), graphics processor (GPU), high-voltage direct current (HVdc), insulated-gate bipolar transistor (IGBT), massively parallel processing, modular multilevel converter (MMC), wideband modeling.**

I. Introduction

MODULAR multilevel converter (MMC) technology, with its inherent advantages, such as more convenient troubleshooting, higher efficiency, and lower harmonics, is prevalent in different applications, such as voltage source converter high-voltage direct current (VSC-HVdc) schemes and flexible alternating current transmission systems[1]–[4]. Unfortunately, power electronic converters are natural sources of electromagnetic interference (EMI) due to the high-level dv/dt and di/dt generated by the commutation of semiconductor devices [5], [6]. In the MMC valve, the voltages across all insulated-gate bipolar transistor (IGBT) modules and the currents through them fall or rise rapidly and repeatedly during the switching transient, each of them exciting its propagation paths through the parasitic circuitry and producing perturbations that could be superimposed and propagated to the dc and ac yard [7]. Conducted EMI noise may interfere with adjacent communication, monitoring, and control systems by stray couplings path, hence, its proper management is an imperative issue in HVdc converter station design.

There are numerous publications on conducted EMI emission characterization and wideband modeling of the power electronic system, which can be grouped into two basic categories [8]: time-domain physics-based modeling approach and frequency-domain behavioral modeling approach. Regardless of which simulation method is adopted, the key to a successful EMI performance prediction is accurate noise source modeling and stray path extraction. The time-domain method mainly performs wideband modeling on all power devices and passive equipment in the system. The switches are always represented by a nonlinear physics-based model, and the high-frequency propagation path parameters are obtained through finite element analysis[9] or partial element equivalent circuit method [10].

In principle, the physics-based model can be very accurate with sufficient theoretical and parameter details. However, the convergence problem is often encountered, which makes it impractical. Besides, even the simplest physical model requires

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some intimate knowledge of the device, such as material properties, structure, and operating mechanism [11]. It is already pretty cumbersome to be applied to a system of simple construction with only a few switches, e.g., 2-level pulsewidth modulation (PWM)-based H-bridge converter, since it would be difficult and prohibitively time-consuming to model all the devices' physical details in the system to achieve sufficient accuracy, let alone the MMCs, which could involve up to thousands of semiconductor devices.

A frequency-domain approach requires knowledge on noise source and propagation path but significantly reduces computational effort and, thus, is recommended as the preferred approach in [12] and [13]. The basic idea is to model the noise source as a simplified function, such as trapezoidal [12] or piecewise linearization waveform [14], which has a known frequency-domain characteristic and acts as the excitation of the parasitic network with frequency-domain analysis. However, the use of the approximation is undoubtedly a compromise between accuracy and computational efficiency, especially in the high-frequency range. Moreover, due to the fluctuation of the bridge arm currents and the submodule (SM) capacitor voltages of the MMC, the transient switching waveforms of each switch are not the same at each moment, and cannot be represented identically. This problem can be eluded through a standard test and characterization procedure of the equivalent source with impedance under the specified operating conditions for a given prototype [15]–[17]. Nevertheless, the most noticeable deficiency is their dependency on measurement, which is unachievable for EMI verification before the equipment is manufactured. Actually, it is very desirable to make proper modeling of EMI noise generation and propagation in MMC-HVdc project an integral part of the design process.

In the traditional thyristor-based dc transmission and PWM-based 2-level VSC-HVdc converters, each switch of a specific bridge arm is uniformly controlled to execute the same switching command, which enables the stack of semiconductor devices to be modeled as few or even a single valve. The MMC topology and corresponding modulation strategy, however, does not trigger the IGBTs identically. Therefore, similar simplification cannot be analogically applied to MMC's configuration [18].

All the aforementioned facts account for the absence of an accurate and practical EMI modeling and prediction method suitable as a design tool for MMC-HVdc project due to the complexity of EMI noise generation and propagation mechanism. To analyze the impact of control strategy and parameters on the EMI characteristics, it is necessary to simultaneously take the control system of the converter, high-frequency parameters, and semiconductor devices' physical attributes into consideration. Thus, the computational burden will be so heavy that the currently available device-level simulators cannot handle such a large-scale system with a small time step, thousands of semiconductor devices, and a large number of nodes. Based on the powerful parallel computing capabilities, graphics processor (GPU) is well suited for large-scale power electronic system simulation, which has been employed previously [19]–[21].

In this article, GPU's massive parallelism is utilized to expedite the simulation of MMC-HVdc system EMI characteristics. By analyzing and simplifying the stray capacitance layout of the converter valve tower, the whole bridge arm is partitioned into cascaded two-port networks with the ground as the common terminal. Fine-grained network from the original system structure is obtained by separating all two-port networks and MMC SMs, whose similarity enables writing them in single instruction, multiple data format by the programming language CUDA C and parallel execution by multiple computational blocks and threads.

This article is organized as follows. Section II shows the nonlinear advanced dynamic IGBT/diode electrothermal model and the method of the parasitic parameters extraction. Section III presents the wideband model of the MMC, detailed partitioning methodologies of the GPU accelerated simulation framework, and the experimental verification of a 2 terminal 3 phases 11-level MMC prototype. Section IV shows the stray parameter extraction and the modeling method of the high-voltage valve tower structure in the actual projects, an overall impact analysis of different factors was carried out in Section V. Finally, Section VI concludes this article.

II. Nonlinear Dynamic IGBT/Diode Electrothermal Model and Parasitic Parameter Extraction

A. IGBT and Diode Pair Physics-Based Model

In order to analyze and estimate a range of devices and circuit behaviors, accurate IGBT and its antiparallel diode model are essential. The work of semiconductor devices involves the drift and diffusion of carriers, which is often described by the ambipolar diffusion equation (ADE). The most critical process of existing physical models is the solution of ADE, solved by the method of linear distribution simplification [22], Fourier series decomposition [23], finite element [24], and finite difference method [25]. Part of the parameters for all the models aforementioned need to be extracted from device transient waveforms and inevitably requires dedicated characteristic test equipment, which makes it impractical at the design stage.

Advanced dynamic electrothermal model of IGBT and dynamic diode model [26] are employed in this article, the main advantage of which is that all model parameters can be extracted through the manufacture's datasheet. As shown in Fig. 1(a), the equivalent circuit of IGBT contains seven nodes, whereas the diode has three nodes. Since the latter shares its anode and cathode with the emitter and collector of the former, the overall model has finally eight nodes.

1) IGBT Model: The model mainly reflects the static characteristics of the IGBT through the Darlington connection of MOSFET and bipolar junction transistor (BJT), whereas the junction and diffusion capacitances indicate the dynamic components of the switch.

The MOSFET part utilizes a Schichman–Hodges model [27] with its output characteristics of the linear and saturation region described by

$$I_{\rm mos}=\begin{cases} I_{\rm sat}\cdot(1+K_{\rm LM}\cdot\ V_{\rm ds})\cdot \\ \left(2-\frac{V_{\rm ds}}{V_{\rm sat}}\right)\cdot\frac{V_{\rm ds}}{V_{\rm sat}}, & V_{\rm ds}<V_{\rm sat} \\ I_{\rm sat}\cdot(1+K_{\rm LM}\cdot\ V_{\rm ds}), & V_{\rm ds}\geq V_{\rm sat} \end{cases} \quad (1)$$

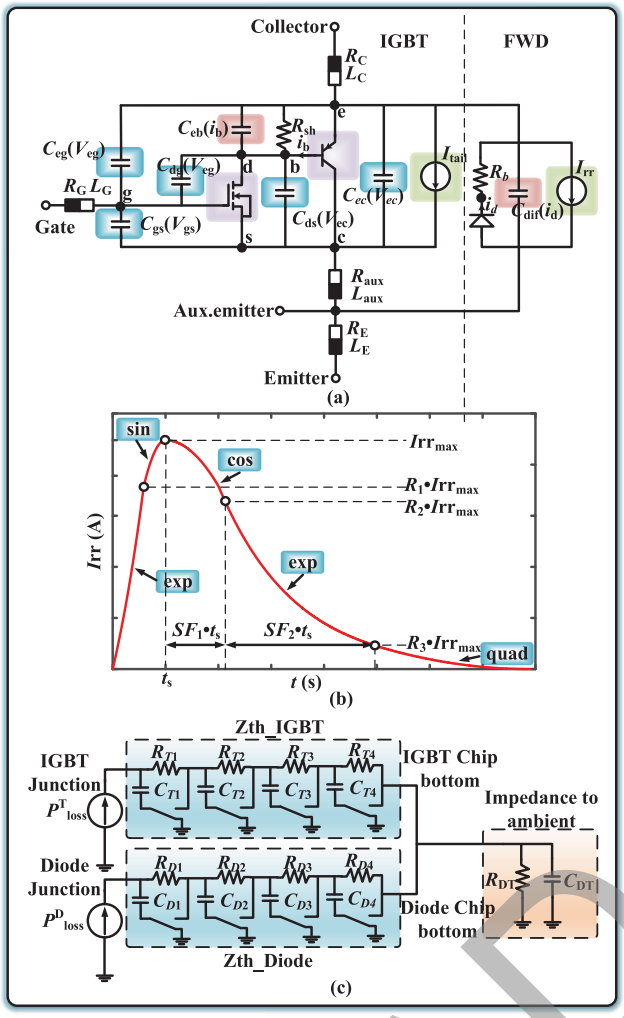

Fig. 1. Model details of IGBT and FWD. (a) Schematic of electrothermal dynamic IGBT model. (b) Diode reverse recovery waveform. (c) Thermal network of the IGBT/diode model.

where $V_{\rm ds}$ is the drain-source voltage, $I_{\rm mos}$ is drain current, which is equal to source current I_s, $K_{\rm LM}$ is model coefficient to be extracted, and $V_{\rm sat}$ and $I_{\rm sat}$ are saturation voltage and current, respectively, expressed as

$$V_{\rm sat} = A_{\rm FET}(V_{\rm gs} - V_P)^{M_{\rm FET}} \tag{2}$$

$$I_{\rm sat} = \frac{K}{2}(V_{\rm gs} - V_P)^{N_{\rm FET}} \tag{3}$$

where $V_{\rm gs}$ is the gate-source voltage, $A_{\rm FET}$, $M_{\rm FET}$, $N_{\rm FET}$, and K are all model coefficient together with the channel threshold voltage V_P.

Since there is no reverse blocking state of the IGBT under the operating mode of current converter design, only the forward conduction characteristics of the BJT is considered, which is formulated as [27]

$$I_c = b_n \cdot\ I_b, I_b = I_{\rm sat_{BJT}} \cdot \left[e^{\frac{V_{eb}}{(M_{\rm BJT} \cdot\ V_T)}} - 1\right] \tag{4}$$

where V_{eb}, I_b, and I_c are the base-emitter voltage, base and collector current respectively, $V_T = \frac{kT}{q}$ is the temperature voltage, and $I_{\rm sat_{BJT}}$, $M_{\rm BJT}$, and b_n are the parameters of BJT part.

The transient switching characteristics of IGBTs are mainly affected by junction capacitances; therefore, each of them should be modeled elaborately. All capacitances of the same type are represented in the same manner. When the p-n junction is positively biased, it is in an enhanced state; and depleted state when turned over. The corresponding capacitances are given as

$$C(V^*_{\rm JVCT}) = \begin{cases} C_0 \cdot \left(1 + (\beta - 1)\left(1 - \exp\left(-\frac{\alpha(1-\delta)V^*_{\rm JVCT}}{(\beta-1)V_{\rm diff}}\right)\right)\right), & V^*_{\rm JVCT} > 0 \\ C_0 \cdot \left(\delta + \frac{1-\delta}{(1-\frac{V^*_{\rm JVCT}}{V_{\rm diff}})^{\alpha}}\right), & V^*_{\rm JVCT} \le 0 \end{cases} \tag{5}$$

where C_0, α, β, δ, and $V_{\rm diff}$ are all coefficients which have their corresponding value for each junction capacitance, and $V^*_{\rm JVCT}$ is expressed as

$$V^*_{\rm JVCT} = K_{\rm shift} \cdot\ V_{\rm diff} - V_{\rm JNCT} \tag{6}$$

where $K_{\rm shift}$ is the parameter, and $V_{\rm JNCT}$ is the voltage between the p-n junction, which is V_{eg} for C_{eg} and C_{dg}, V_{ec} for C_{ec} and $C_{\rm ds}$, and $V_{\rm gs}$ for $C_{\rm gs}$. It is important to note that the parameters of the Miller capacitance are different between turn-ON and turn-OFF transient process. Besides, the gate capacitance is always formed by two parallel capacitances in the enhanced and depleted state, respectively, representing the capacitance of shorted P+ and N+ base regions to the gate metal terminal.

The diffusion capacitances at the base-emitter path of the BJT and within the freewheeling diode (FWD) are modeled using the same approach defined as

$$C_{\rm diff} = \tau \frac{i(t) + I_{\rm sat}}{M \cdot V_T} \tag{7}$$

with τ and M the coefficients, $i(t)$ should be substituted by i_b for C_{eb}, and i_d for $C_{\rm dif}$.

Parameters $\tau_{\rm tail}$ and $\delta_{\rm tail}$ influence the off switch current edge, as $\delta_{\rm tail}$ shapes the falling edge and $\tau_{\rm tail}$ sets the duration. The injected current $I_{\rm tail}$ at load current $I_{\rm load}$ is expressed as [28]

$$I_{\rm tail} = \delta_{\rm tail} \cdot\ I_{\rm load} \cdot \exp\left(-\frac{t}{\tau_{\rm tail}}\right). \tag{8}$$

All the dynamic parameters described earlier have working point dependency on current I, voltage V, and junction temperature T as

$$C_x = C_{x0} \cdot x_I(I) \cdot x_V(V) \cdot x_T(T) \tag{9}$$

$$x_I(I) = C_{C0} + (1 - C_{C0})\left(\frac{I}{I_{\rm NOM}}\right)^{CC} \tag{10}$$

$$x_V(V) = V_{C0} + (1 - V_{C0})\left(\frac{V}{V_{\rm NOM}}\right)^{VC} \tag{11}$$

$$x_T(T) = \left(\frac{T_J}{T_{\rm NOM}}\right)^{TC}. \tag{12}$$

2) Diode Model: The FWD is modeled as a simple diode in series with a current-dependent resistance as described by

$$I_{\mathrm{fwd}} = I_{\mathrm{sat_{fwd}}} \cdot \left[e^{\frac{V_{\mathrm{fwd}}}{(M_{\mathrm{fwd}} \cdot V_T)}} - 1 \right] \tag{13}$$

$$R_b = \frac{Rb_{\mathrm{fwd}}}{\sqrt{1 + \frac{I_{\mathrm{fwd}}}{I_{\mathrm{NOM}}}}} \tag{14}$$

with $I_{\mathrm{sat_{fwd}}}$, M_{fwd}, and Rb_{fwd} the parameters, and I_{NOM} the rated current of the IGBT module.

The waveform of reverse recovery current is defined as the form of a piecewise function with five sections, as shown in Fig. 1(b). All sections are connected so that the curve remains differentiable at the transition from one region to the other. The maximum current $I_{rr\,\max}$ is obtained by

$$I_{rr\,\max} = k \left(\tau_{\mathrm{fwd}} - \frac{1}{\tau_{\mathrm{fwd}}} - \frac{1}{T_n} \right) \left(1 - \exp\left(\frac{t_s}{\tau_{\mathrm{fwd}}} \right) \right). \tag{15}$$

where parameter k represents the turn-OFF slope, τ is the carrier life time, T_n is the electron transit time, and t_s when $I_{rr\,\max}$ is reached, are calculated from the reverse recovery charge Q_{rr} and the form factors.

As shown in Fig. 1(c), the thermal network configuration can be selected from Cauer-type (switches connect the thermal capacitances directly to the ambient node) and Foster-type model (the thermal capacitances are connected in parallel to the corresponding thermal resistances). The ground symbol represents the ambient space, and the electrical power losses P^T_{loss} and P^D_{loss} of both the IGBT and diode are injected into their thermal network, respectively.

B. Model Discretization and Linearization

The IGBT and FWD physical models contain a certain amount of nonlinear components, which brings about the main computational burden. In this article, the backward Euler method is used to linearize and discretize the model.

1) Linear Components: For the linear capacitance and inductance, the equivalent admittance and current source of their discrete Norton equivalent circuit with a time step Δt are given as

$$g_{C_{\mathrm{eq}}} = \frac{C}{\Delta t}, I_{C_{\mathrm{eq}}} = -\frac{C}{\Delta t} v_C(t - \Delta t) \tag{16}$$

$$g_{L_{\mathrm{eq}}} = \frac{\Delta t}{L}, I_{L_{\mathrm{eq}}} = i_L(t - \Delta t). \tag{17}$$

2) Controlled Sources: The static part of the MOSFET and BJT can be deemed as voltage-controlled current sources. The current of MOSFET is determined by both V_{gs} and V_{ds}, as a consequence, discretization of the component yields conductance $g_{\mathrm{mos}V_{\mathrm{ds}}}$ and transconductance $g_{\mathrm{mos}V_{\mathrm{gs}}}$ derived by taking partial derivatives with respect to V_{ds} and V_{gs}, which is shown as

$$g_{\mathrm{mos}V_{\mathrm{ds}}} = \frac{\partial I_{\mathrm{mos}}}{\partial V_{\mathrm{ds}}}, g_{\mathrm{mos}V_{\mathrm{gs}}} = \frac{\partial I_{\mathrm{mos}}}{\partial V_{\mathrm{gs}}} \tag{18}$$

and the conductance for BJT part is

$$g_{\mathrm{BJT}} = \frac{\partial I_b}{\partial V_{eb}}. \tag{19}$$

The Norton equivalent current for MOSFET and BJT can be expressed by the following combination:

$$I_{\mathrm{mos_{eq}}} = I_{\mathrm{mos}} - g_{\mathrm{mos}V_{\mathrm{ds}}} \cdot V_{\mathrm{ds}} - g_{\mathrm{mos}V_{\mathrm{gs}}} \cdot V_{\mathrm{gs}} \tag{20}$$

$$I_{b_{\mathrm{eq}}} = I_b - g_{\mathrm{BJT}} \cdot V_{eb}. \tag{21}$$

3) Nonlinear Capacitances: According to the relationship between the capacitance and junction voltage, the formula for charge and the voltage can be derived via the integration by voltage

$$Q_{jc} = \begin{cases} C_0 \cdot \left(V + (\beta - 1) \cdot \left(V - \frac{\exp(V \cdot A)}{A} \right) \right) + \frac{C_0 \cdot (\beta - 1)}{A}, & V^*_{\mathrm{JVCT}} > 0 \\ C_0 \cdot (\delta \cdot V + B \cdot \left(1 + \frac{V}{V_{\mathrm{diff}}} \right)^{1-\alpha} - C_0 \cdot B, & V^*_{\mathrm{JVCT}} \le 0 \end{cases} \tag{22}$$

where A and B are expressed as

$$A = \frac{\alpha \cdot (1 - \delta) \cdot V_{\mathrm{diff}}}{\beta - 1}, B = \frac{(1 - \delta) \cdot V_{\mathrm{diff}}}{1 - \alpha}. \tag{23}$$

The same approach is also applicable to the calculation of diffusion capacitance

$$Q_{\mathrm{diff}} = \tau \cdot I_{\mathrm{sat}} \cdot \left(\exp\left(\frac{V \cdot V_T}{M} \right) - 1 \right). \tag{24}$$

Since the current is the flow rate of charge, capacitance current can be discretized as

$$I_{jc} = \frac{Q_{jc} - Q_{\mathrm{old}}}{\Delta t}, I_{\mathrm{diff}} = \frac{Q_{\mathrm{diff}} - Q_{\mathrm{old}}}{\Delta t}. \tag{25}$$

The equivalent admittances and accompanying current sources are given as

$$g_{jc} = \frac{C}{\Delta t}, I\mathrm{eq}_{jc} = I - g_{jc} \cdot V \tag{26}$$

$$g_{\mathrm{diff}} = \frac{C}{\Delta t}, I_{\mathrm{diff_{eq}}} = I - g_{\mathrm{diff}} \cdot V. \tag{27}$$

According to KCL, the nodal equation for all the eight nodes in the advanced dynamic electrothermal model can be expressed

$$\mathbf{G} \cdot \mathbf{U}^{\mathrm{Node}} = \mathbf{I} \tag{28}$$

where $\mathbf{G}$ and $\mathbf{I}$ are given in (29) shown at the bottom of the next page, and (30), g_{sC}, g_{sE}, and $g_{s\mathrm{aux}}$ are the equivalent admittances of the package stray parameters, I_{sC}, I_{sE}, and $I_{s\mathrm{aux}}$ are the

corresponding current sources

$$\mathbf{I} = \begin{bmatrix} I_{sC} \\ -(bn+1)\cdot I_{b_{\mathrm{eq}}} - I_{ec_{\mathrm{eq}}} - I_{eg_{\mathrm{eq}}} - I_{Ceb_{\mathrm{eq}}} + I_{\mathrm{dif}_{\mathrm{eq}}} - I_{sE} \\ -I_{\mathrm{mos}_{\mathrm{eq}}} + I_{b_{\mathrm{eq}}} + I_{Ceb_{\mathrm{eq}}} \\ \frac{Vs}{Rg} - I_{\mathrm{gs}_{\mathrm{eq}}} + I_{eg_{\mathrm{eq}}} \\ I_{\mathrm{mos}_{\mathrm{eq}}} + bn\cdot I_{b_{\mathrm{eq}}} + I_{\mathrm{gs}_{\mathrm{eq}}} + I_{ec_{\mathrm{eq}}} + I_{\mathrm{saux}} \\ -I_{\mathrm{fwd}_{\mathrm{eq}}} - \frac{Vs}{Rg} - I_{\mathrm{dif}_{\mathrm{eq}}} - I_{\mathrm{saux}} + I_{sE} \\ I_{\mathrm{fwd}_{\mathrm{eq}}} \\ -I_{sE} \end{bmatrix}. \tag{30}$$

C. Stray Parameter Extraction of IGBT Module and MMC Prototype

An 11-level 3-phase MMC prototype is shown in Fig. 2(a) and (b) with the converter transformers are at the base, arm reactors in the middle, and at the top are the SM sections, whose details are shown in Fig. 2(c) and (d). The converter adopts a full-bridge SM (FBSM) structure with 12 SMs per phase, two of which are redundant. Bridge arm of each phase is composed of two sections, which consists of six SMs soldered on a printed circuit board (PCB).

The selected IGBT module is FUJI 6MBP30VAA060-50 intelligent power module (IPM), which contains six pairs of IGBTs and diodes, four of which are used to form the FBSM structure. The parameters of the dynamic electrothermal model are extracted by device characterization tool in ANSYS Simplorer. The main coefficients are shown in Table II in the Appendix, the parameters not listed are all 0. The prototype uses the direct current control strategy to decouple the active and reactive power management and nearest level modulation

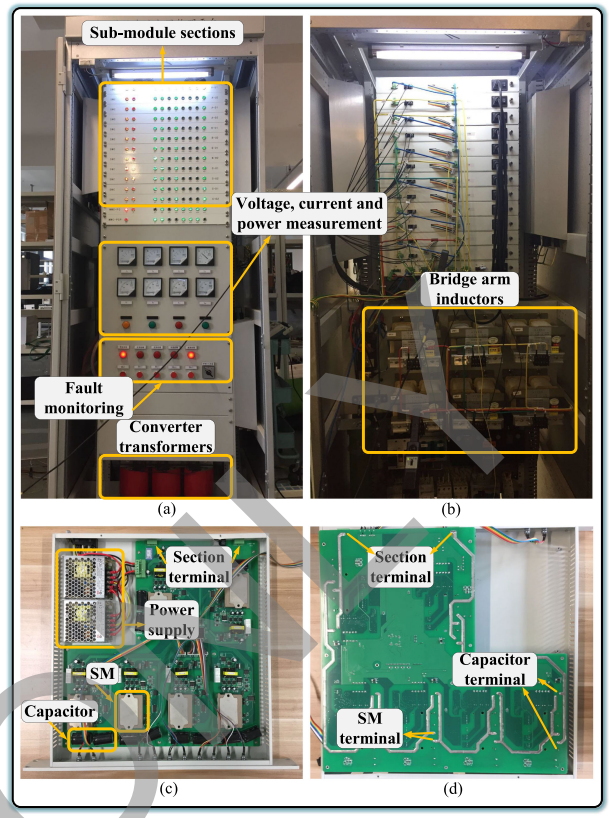

Fig. 2. Prototype of an 11-level MMC. (a) Front view. (b) Opposite view, bridge arm section of the MMC prototype. (c) Front view. (d) Opposite view.

$$\mathbf{G} = \begin{bmatrix} g_{sC} & -g_{sC} & 0 & 0 & 0 & 0 & 0 & 0 \\ -g_{sC} & \begin{matrix}(bn+1)\cdot g_{\mathrm{BJT}}+\\ \frac{1}{R_P}+g_b+g_{sC}+\\ g_{ec}+g_{eg}+\\ g_{Ceb}+g_{\mathrm{dif}}\end{matrix} & \begin{matrix}-(bn+1)\cdot g_{\mathrm{BJT}}-\\ \frac{1}{R_P}-g_{Ceb}\end{matrix} & -g_{eg} & -g_{ec} & -g_{\mathrm{dif}} & -g_b & 0 \\ 0 & -g_{\mathrm{bjt}}-\frac{1}{R_P}-g_{Ceb} & \begin{matrix}g_{\mathrm{mos}Vds}+g_{\mathrm{BJT}}+\\ \frac{1}{R_P}+g_{Ceb}\end{matrix} & g_{\mathrm{mos}Vgs} & \begin{matrix}-g_{\mathrm{mos}Vds}-\\ g_{\mathrm{mos}Vgs}\end{matrix} & 0 & 0 & 0 \\ 0 & -g_{eg} & 0 & \begin{matrix}\frac{1}{R_g}+g_{\mathrm{gs}}+\\ g_{eg}\end{matrix} & -\frac{1}{R_g}-g_{\mathrm{gs}} & 0 & 0 & 0 \\ 0 & -bn\cdot g_{\mathrm{BJT}}-g_{ec} & \begin{matrix}-g_{\mathrm{mos}Vds}+\\ bn\cdot g_{\mathrm{bjt}}\end{matrix} & \begin{matrix}-g_{\mathrm{mos}Vgs}-\\ g_{\mathrm{gs}}\end{matrix} & \begin{matrix}g_{\mathrm{mos}Vds}+\\ g_{\mathrm{mos}Vgs}+\\ g_{\mathrm{gs}}+g_{\mathrm{saux}}+\\ g_{ec}\end{matrix} & g_{\mathrm{saux}} & 0 & 0 \\ 0 & -g_{\mathrm{dif}} & 0 & \frac{1}{R_g} & -g_{\mathrm{saux}} & \begin{matrix}g_{\mathrm{fwd}}+\frac{1}{R_g}+\\ g_{\mathrm{saux}}+g_{sE}+\\ g_{\mathrm{dif}}\end{matrix} & -g_{\mathrm{fwd}} & -g_{sE} \\ 0 & -g_b & 0 & 0 & 0 & -g_{\mathrm{fwd}} & g_b+g_{\mathrm{fwd}} & 0 \\ 0 & 0 & 0 & 0 & 0 & -g_{sE} & 0 & g_{sE} \end{bmatrix} \tag{29}$$

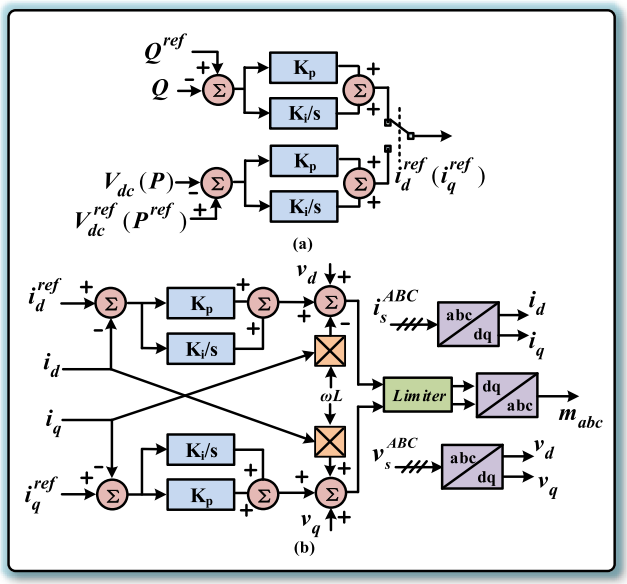

Fig. 3. Control strategy of 11-level MMC prototype. (a) Outer loop power control. (b) Inner loop current control.

(NLM) for the modulation scheme. The control block diagram is shown in Fig. 3, the corresponding control parameters are given in Table III. A traditional sorting method is used for SM voltage balancing.

The IGBT module integrates multiple chips into a package to improve the service life and reliability. Every power module contains parasitic resistances and parasitic inductances caused by the direct bonded copper, terminal buses, solder layer, and bond wires, as well as parasitic capacities provoked by parallel conductors separated by dielectric layers [29]. The three-dimensional (3-D) model of IPM and the bridge arm section are constructed in ANSYS Q3D extractor, and the stray parameters are extracted and shown in Table IV in the Appendix.

III. Parallel Implementation of Wideband MMC Model on GPU

A. Passive Device Wide-Band Model

The passive electrical element contains parasitics that usually manifest themselves at high frequency. The effect of stray parameters (lead inductance $L_{\rm lead}$ and parasitic resistance $R_{\rm par}$) in a capacitor should not be ignored during the fast switching operation. The parasitic inductance and resistance parameters vary with the dielectric material properties. For the inductors installed in bridge arm and ac yard, there are stray capacitances between turns and winding layers that can be represented by a parasitic capacitance $C_{\rm par}$, and the power loss is considered via $R_{\rm par}$. The simplified models of capacitor and inductor are shown in Fig. 4(a) and (b), respectively.

The converter transformer is a crucial component in the HVdc system used for connecting the valve and the ac side. The wideband effect of transformer model directly affects the validity of the prediction of the EMI noise. Fig. 4(c) shows the

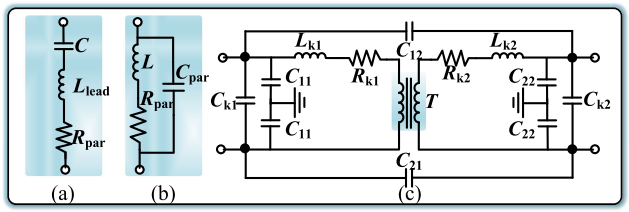

Fig. 4. Wideband model of (a) capacitor, (b) inductor, and (c) converter transformer.

wideband equivalent circuit of the transformer with a single-phase double-winding structure applied in the prototype. The high-frequency characteristics mainly involve the influence of parasitic capacitance, including the primary side winding-to-ground parasitic capacitance C_{11}, secondary winding-to-ground parasitic capacitance C_{22}, and the interterminal capacitances C_{k1}, C_{k2}, C_{12}, and C_{21}. T is a classical transformer model, which mainly considers the electromagnetic characteristics at the low-frequency range.

B. Circuit Partitioning for Simulation Acceleration

According to the internal structure of IPM, the stray inductance, resistance, and capacitance parameters of the copper layer, main terminals and bond wires shown in the Fig. 5(a) can be merged into the IGBT-diode pair model in Section II. The main terminals P, N, U, and V are soldered to the upper copper layer, thereby forming stray capacitances to the base plate, and another stray capacitance exists between the substrate and the grounded case, which causes the copper substrate to become a floating potential during operation. Applying Rosen's theorem [30], the node indicating the copper substrate can be eliminated, and replaced by interterminal (C_{UP}, C_{UN}, C_{VP}, C_{VN}, and C_{UV}) and grounded equivalent capacitances (C_{Ug}, C_{Vg}, C_{Pg}, and C_{Ng}), as shown in the Fig. 5(b) and the corresponding values are presented in Table IV in the Appendix.

The branch of the broadband capacitor and the corresponding stray parameters can be merged as a composite admittance paralleled with a current source. Thus, the FBSM model initially contains 28 nodes. However, considering the fourth IGBT is constantly under off state during normal operation, it can be omitted, and the new FBSM has 23 nodes. The node admittance matrix and injection current vector for the wideband FBSM model can be formed [21]. The nodal voltages are subsequently obtained by

$$\mathbf{U}_{\rm SM} = \mathbf{G}_{\rm SM}^{-1} \cdot \mathbf{J}_{\rm SM}. \tag{31}$$

According to the hierarchical and zonal computation circuit lemma, which indicates the relationship of branch voltages and currents [31], in the case where the SM capacitance is large enough and the simulation time-step is quite small, circuit partitioning can be conducted to split all individual components from their main circuit topology for alleviating the computational burden and improving numerical stability. In this article, a 10 ns time step (much smaller than in the system-level simulation) is selected to implement the EMI analysis within 150 kHz–30 MHz.

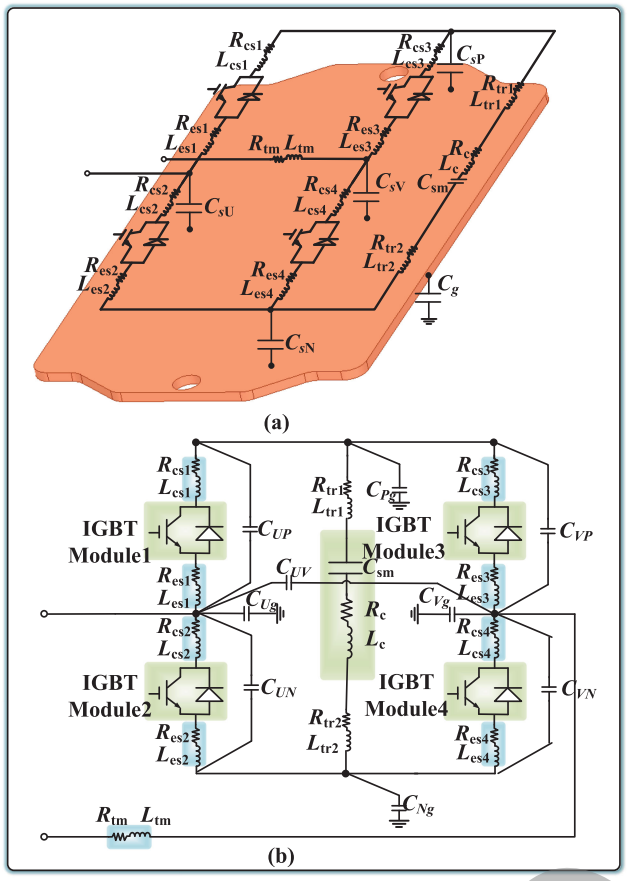

Fig. 5. Wideband model of FBSM. (a) Stray parameters configuration. (b) Detailed circuit of FBSM after star-mesh transformation.

Thus, the currents between two neighboring time-steps can be deemed as constant, and the SM components' characteristics can be split from the circuit topology, the processing of individual SMs is also decoupled from each other, which makes it extremely suitable for parallel computation.

C. Detailed Massively Parallel Implementation and Experiment Verification

GPU's many core architecture catering to numerous SMs is exploited where various kernels, defined on the GPU as a global function coded in CUDA C language, are executed in a single-instruction-multiple-threading mode to proceed the parallel simulation [32]. The GPU used in this article is the NVIDIA Tesla V100 (Volta architecture) with 5120 CUDA cores and 16 GB HBM2 memory run on a 64-b Windows 10 operating system with 2.20 GHz 20-core Intel Xeon E5-2698 v4 CPU and 192 GB RAM.

An illustration of the parallel program implementation is given in Fig. 6. At the beginning of every step, the trigger signals for all IGBT devices are derived from the PQ control kernel_1 and NLM kernel_2. The SMs are the primary part of massive parallelism in the GPU-based simulation since they outnumber other electrical equipment. The SM kernel_3 invokes a corresponding number of threads simultaneously, in which the IGBT physics-based model is programmed as a device function. When all the SM voltages converge, the output and capacitor voltages of each SM are obtained. The next step in kernel_5 is to calculate all the voltages and currents of the converter. Then, the input of kernel_1 in the next PQ control step and all the corresponding history values are updated. When the number of preset steps has been reached, the entire simulation is completed. kernel_4, kernel_6, and kernel_7 shown in dashed line are necessary for two-terminal MMC-HVdc valve tower, which will be elaborated in the next section.

To acquire the high-frequency current signals, Tektronix MSO/DPO2000B oscilloscope with the current probe are used in the experimental measurement at room temperature (25 °C). The voltage and power reference values are given in Table I in the Appendix. The amplitude-frequency characteristic of the CM and DM current in the range of 150 kHz to 30 MHz is shown in Fig. 7, compared with the calculation result, express as [33]

$$I_{\text{CM}} = i_A + i_B + i_C \tag{32}$$

$$I_{\text{DM},A} = i_A - \frac{I_{\text{CM}}}{3}. \tag{33}$$

Within the scope of less than 1 MHz, the predicted noise of the CM and DM current is slightly higher than that from measurement, but the envelope is almost the same. While when the frequency is higher than 4 MHz, the EMI simulation characteristics are lower than the test results, but the envelope difference is less than 5 dBμA in most of the scope, thus, the accuracy of the method is verified.

IV. Wideband Modeling and Massively Parallel Implementation of High-Voltage MMC Valve Tower

A. Parasitic Parameters Within Converter Valve Tower

In the actual HVdc project, the output terminal of SMs are usually connected by copper bars orderly and assembled as a valve tower, as shown in Fig. 8. Most IGBT modules applied in MMC-HVdc are with standardized package size and structure among each manufacturer. Thus, ABB Hi-Pack 5SNA1200E330-100 module is taken as an example, with the FEM model of the package and widely used half-bridge SM (HBSM) architecture built in ANSYS Q3D extractor, as shown in Fig. 9(a) and (b), respectively.

As shown in Fig. 8, the valve tower effectively forms a hollow coil structure according to its spiral connection mode in space, whose inductance can be obtained by

$$L = \frac{M^2 \mu_0 ab}{h} \tag{34}$$

where a and b are the length and width of a single layer, μ_0 is the air permeability, M is the total number of layers, and h is the height of the entire valve tower. L should be decomposed and merged into each SM, represented by $L_{\text{sm}} = \frac{L}{N}$, to take the intrinsic distributed nature into consideration.

Generally, the stray capacitances of a valve tower can be classified into three categories, i.e., capacitances for intershielding (including C_{SS} and C_{SV} for within and interlayer respectively), shielding to ground C_{SG}, and shielding to busbars C_{CS}, as

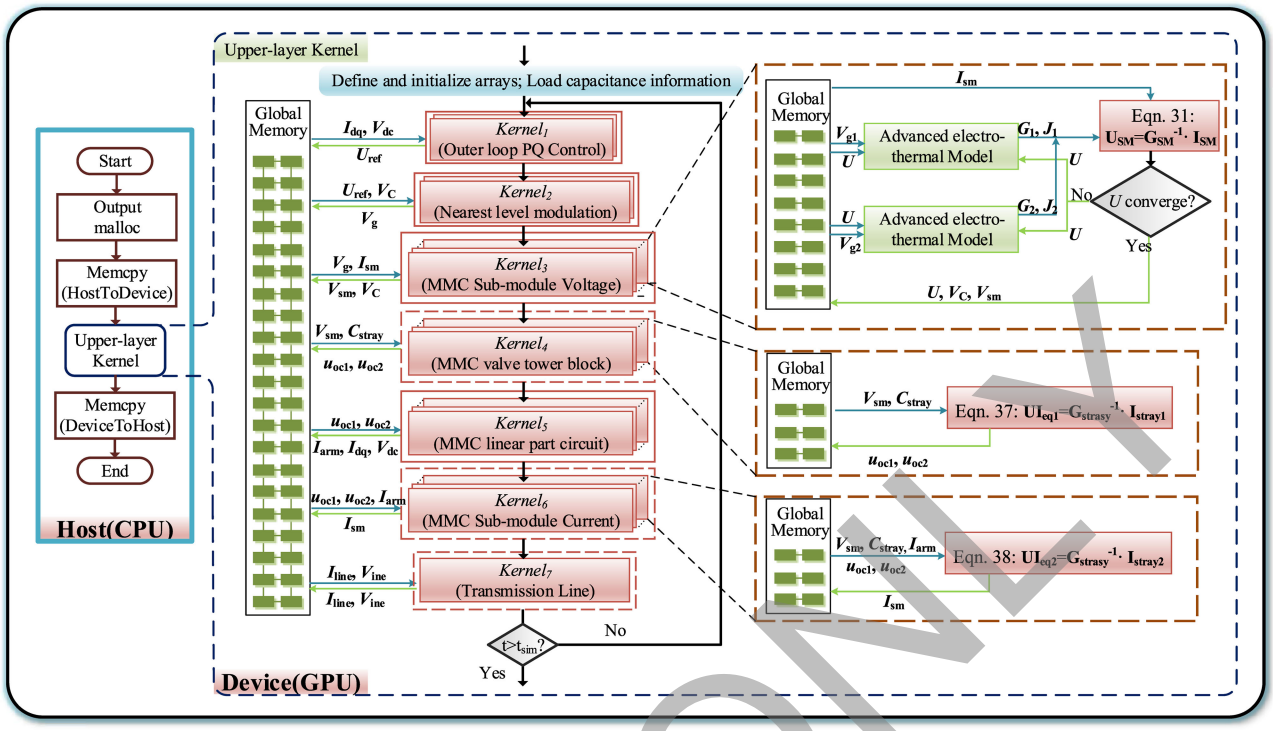

Fig. 6. Massively parallel architecture for simulation.

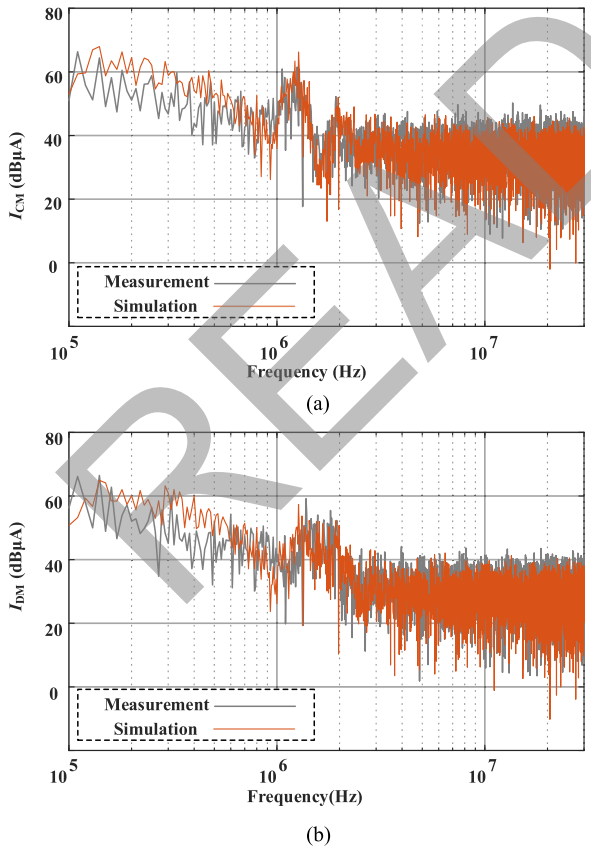

Fig. 7. 3-phase 11-level MMC prototype measurement and GPU massively parallel simulation comparison. (a) CM noise. (b) DM noise.

shown in Fig. 8. For an actual valve tower with five layers (20 SMs and six shielding plates per layer) and two shielding rings at both top and bottom end, a 135-order symmetric capacitance matrix, with 101 copper bars nodes, and 34 shielding nodes, can be formed, as shown in Fig. 10(a). Through FEM modeling of the valve tower in ANSYS Q3D, the capacitances between adjacent conductors are large (several or tens of picofarad levels), whereas the rest are so small that can be neglected. Moreover, capacitances between neighboring copper bars can be incorporated into the SMs, block A is consequently 0. D stands for intershielding capacitances, and B and C for bus-shielding capacitances.

The potential of the shielding system could either be floating or fixed in actual projects. However, based on Rosen's theorem, the capacitance matrix can be unified into the same schematic with dense and block diagonally dominant features by a series of the star-mesh transformation. According to KCL, the high-frequency current path is primarily determined by the large capacitances, whereas those relatively small ones do not bring substantial impact so that can be neglected. Therefore, the partitioned matrix with a total of 21 diagonal blocks is obtained, as shown in Fig. 10(b), with the following rules in summary.

1) The block size and form are related to the configuration of the shields.
2) The copper bars under the shelter of the same shield are coupled tightly to form a subblock.
3) The two blocks related to the corner shield plates are combined into one for the coupling of the corresponding long copper bars at the edge.

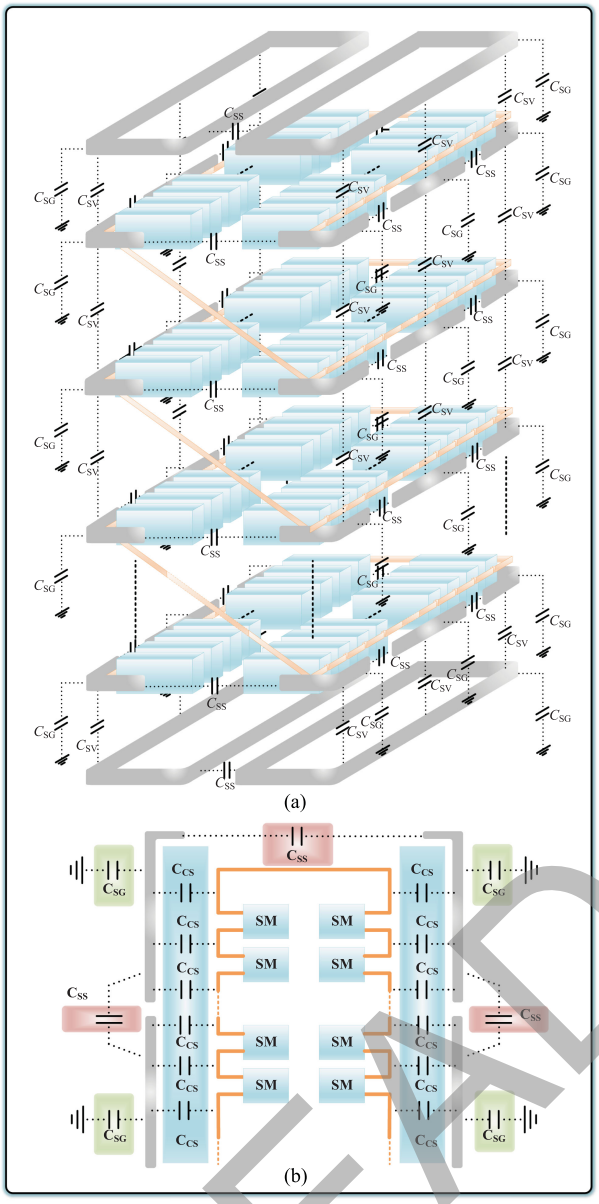

Fig. 8. MMC valve tower structure and stray capacitance layout. (a) 3D stray capacitances layout. (b) Stray capacitances layout within the valve layer.

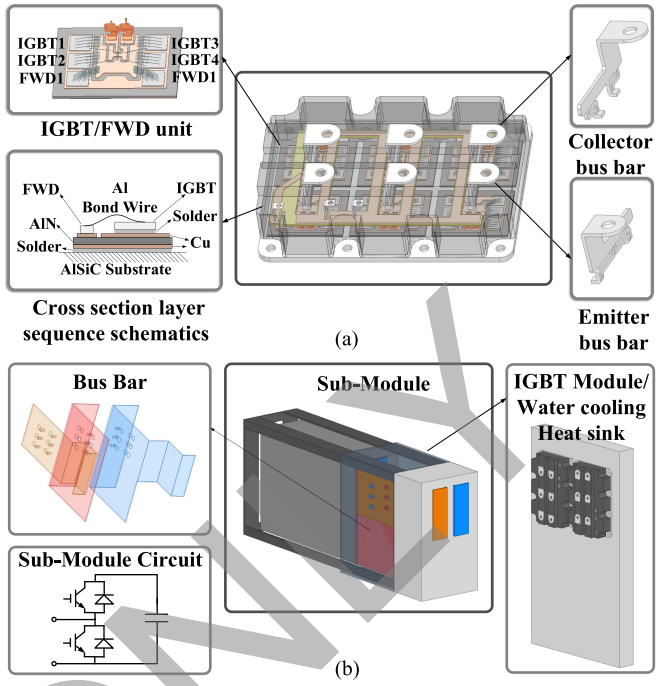

Fig. 9. 3-D FEM model of power IGBT module and HBSM. (a) Package structure for ABB 3300 V Hipak module 5SNA1200E330-100. (b) Simplified MMC SM structure.

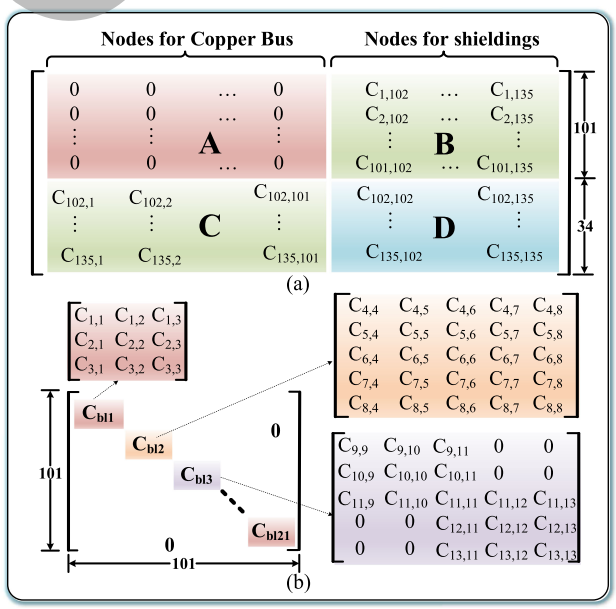

Fig. 10. Stray capacitances layout of MMC tower. (a) 3-D stray capacitances layout. (b) Stray capacitances layout in one layer.

B. Further Circuit Partitioning Methodology

For the wideband valve tower model, the output voltage of each SM can be deemed as an independent voltage source, whereas the stray capacitances are discretized into pairs of equivalent admittances and accompanying current sources. The valve tower is essentially a complex two-port network containing independent sources with the common ground terminal, as shown in Fig. 11(a) and (b). The final equivalent two-port network is given in Fig. 11(c) [34] and mathematically described as

$$u_1 = R_C \cdot i_1 + R_C \cdot i_2 + u_{1\text{oc}} \tag{35}$$

$$u_2 = R_C \cdot i_1 + R_C \cdot i_2 + u_{2\text{oc}}. \tag{36}$$

where R_C is the equivalent resistance with all the node-ground admittances paralleled, $u_{1\text{oc}}$ and $u_{2\text{oc}}$ are the open-circuit voltages of the terminal to ground, which can be obtained through the nodal analysis as

$$\mathbf{UI}_{\text{eq1}} = \mathbf{G}_{\text{stray}}^{-1} \cdot \mathbf{I}_{\text{stray1}} \tag{37}$$

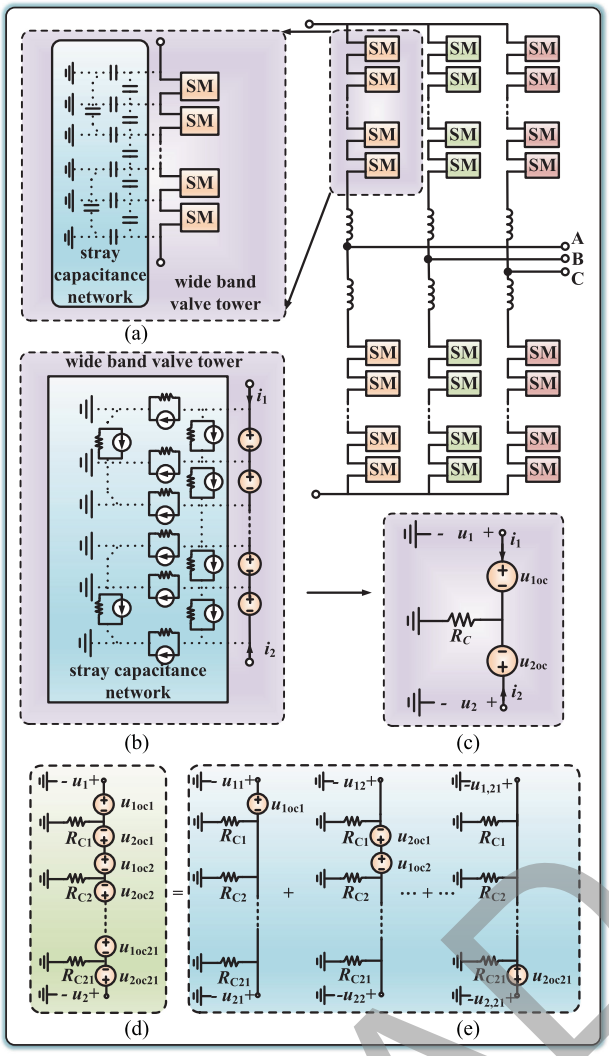

Fig. 11. Principle of the equivalent two-port network with independent sources for bridge arm. (a) MMC topology with wideband valve tower model. (b) Discretized wideband valve tower model. (c) Equivalent two-port network. (d) and (e) Partitioned parasitic capacitance blocks parallel algorithm.

where $\mathbf{UI}_{\text{eq1}}$ includes nodes' voltages and currents of the SM branch. Then, all the currents in the converter can be derived via the circuit solution of the MMC system. The input current of each SM can be calculated in $\mathbf{UI}_{\text{eq2}}$ by another nodal analysis with bridge arm currents added to corresponding nodes in $\mathbf{I}_{\text{stray1}}$ to form the new current injection vector $\mathbf{I}_{\text{stray2}}$

$$\mathbf{UI}_{\text{eq2}} = \mathbf{G}_{\text{stray}}^{-1} \cdot \mathbf{I}_{\text{stray2}}. \tag{38}$$

Due to matrix partitioning, the large stray capacitance matrix can be decoupled into multiple subsystems, which enable a fine-grained parallel algorithm. As shown in Fig. 11(d), the bridge arm can be viewed as a series of cascaded multiple two-port networks with the equivalent voltage sources $u_{1\text{oc}}$ and $u_{2\text{oc}}$ calculated in parallel based on the superposition theorem, as sketched in Fig. 11(e).

As shown in Fig. 6, for each time-step, when all the SM voltages converge, the output and capacitor voltages of each SM are

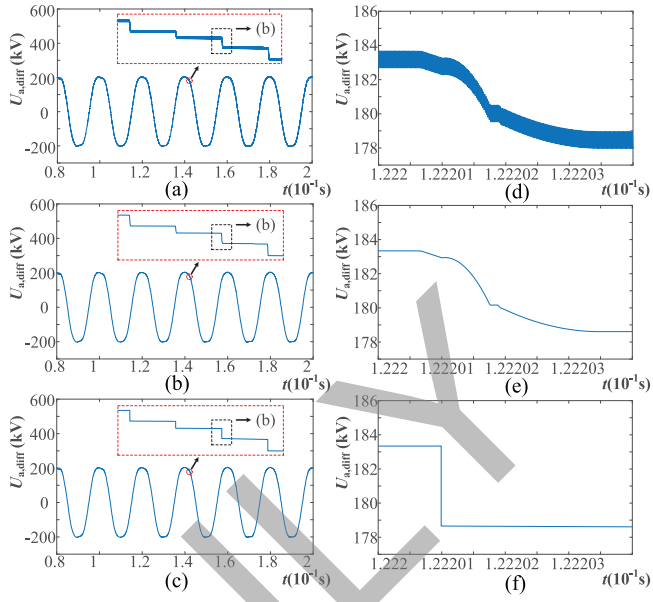

Fig. 12. 3-phase 201-level MMC-HVdc time-domain simulation result. (a) Differential mode voltage with wideband model. (b) Differential mode voltage with only physics-based IGBT model. (c) Differential mode voltage with ideal IGBT model. (d)–(f) Zoomed-in details of (a)–(c).

obtained. kernel_4 should be inserted between kernel_3 and kernel_5 for each subblock of the valve tower, the corresponding amount of threads is 41 for a bridge arm with two series-connected towers, and totally 41×6 for a 201-level MMC-HVdc converter station. Then, the injected current of each SM is obtained according to the bridge arm current as shown in kernel_6, which has the same amount of threads as kernel_4.

Moreover, the transmission line provides a natural circuit partition due to the time delay induced by traveling waves with its parameters highly frequency-dependent. Therefore, the frequency-dependent time-domain model is employed in this article, which is elaborated in [35]. Then, the voltages and currents of the dc transmission line are calculated in kernel_7.

V. Simulation Results and Discussion

A. Test Case for Wideband MMC-HVdc EMI Simulation and Time-Domain Results

The study case is a two-terminal dc transmission system. The level of the converters are all 201, and the length of the dc line is 100 km. See Table VI in the Appendix for the system and control parameters.

Fig. 12 shows the time domain simulation result of the differential mode voltage of phase A in the inverter station, which is defined as

$$U_{\text{diff}} = \frac{V_{dn} - V_{up}}{2}. \tag{39}$$

As shown in Fig. 12(a) and (d), stray parameters can cause significant high-frequency oscillations in the output waveform of the converter. If they are ignored, the estimation of the EMI noise will inevitably deviate from the actuality. The transient process

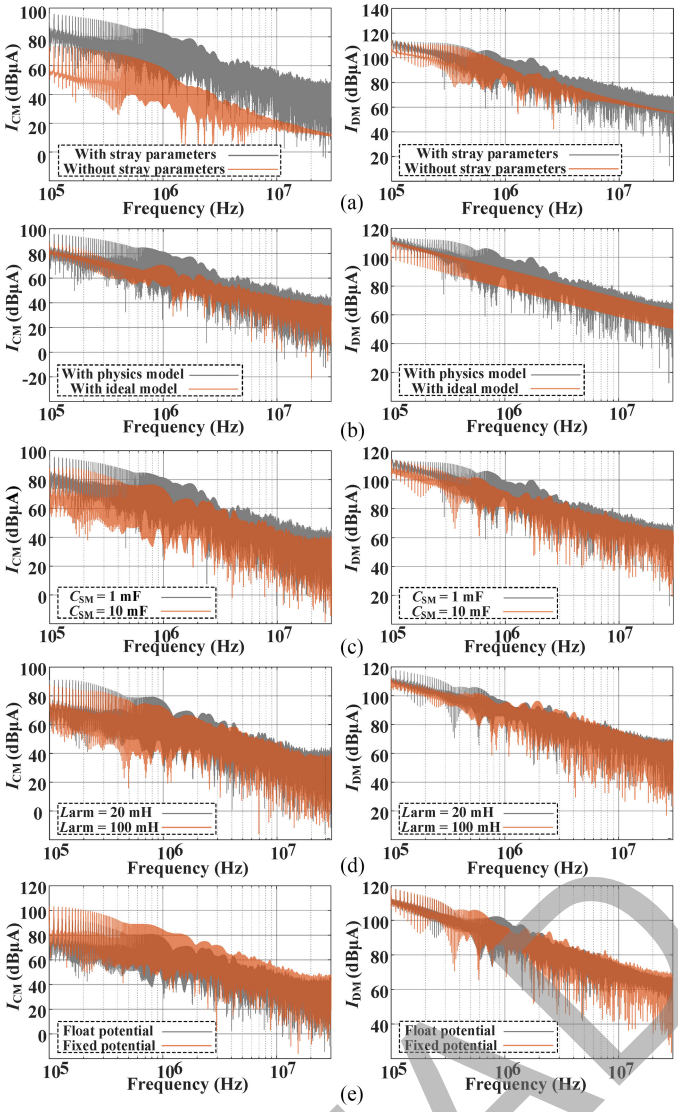

Fig. 13. Effect of main circuit parameters on EMI characteristics. (a) With and without stray capacitance network. (b) Ideal switch and physics-based model of IGBT. (c) 1 and 10 mF SM capacitance. (d) 20 and 100 mH bridge arm inductor. (e) With shielding float and fixed potential.

of the devices allows the level switching of the waveform to have a smooth process in Fig. 12(b) and (e) rather than the stepped wave exhibited by the ideal device in Fig. 12(c) and (f).

B. Frequency-Domain Results and Comparison

The stray capacitances provide a path for the high-frequency components in the IGBT switching waveform, and complex oscillations are formed between the capacitances and inductances. Moreover, as shown in Fig. 13(a), neglecting the stray parameters will result in an unreasonable underestimation of the CM and DM noise. Using an ideal device model will lead to an undervalued EMI all along the spectrum from 150 kHz to 30 MHz, as shown in Fig. 13(b).

The determination of various converter device parameters inevitably has a different effect on EMI characteristics. The

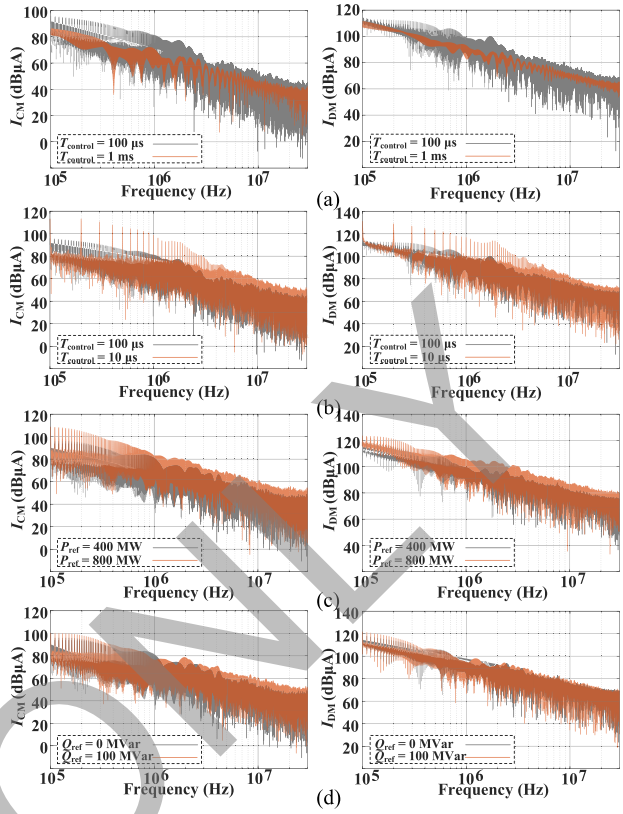

Fig. 14. Effect of control system on EMI characteristics. (a) With control period of 1 ms and 100 μs. (b) With control period of 1 ms and 100 μs. (c) With active power of 800 and 400 MW. (d) With reactive power of 100 and 0 MVar.

SM capacitor supports the dc-side voltage and can suppress the fluctuation of the dc voltage. The charging and discharging process of the SM capacitor inevitably has a particular influence on the high-frequency characteristics of the voltage and current. As shown in Fig. 13(c), increasing the SM capacitance can achieve suppression of the EMI level. The bridge arm inductor acts as the ac/dc power exchange medium of the converter, the current filtering and faults current limiting link, which directly affects the amplitude of the bridge arm high-frequency current. On the other hand, the inductance also determines the voltage drop of the bridge arm. As shown in Fig. 13(d), the inductance can also reduce the CM and DM noise to some extent.

The shield plate of the valve tower is often connected to the adjacent charged body through a fitting, thereby eliminating the floating potential. For example, the shield ring at the top is usually attached to the copper bus of the end SM, and then the cable is connected to the shield ring. EMI noise in both cases are compared in Fig. 13(e). Since the existence of the floating potential is equivalent to connecting another capacitance in series to the grounding path of each copper bus, the equivalent admittance to the ground is reduced, which is beneficial to the suppression of high-frequency current flowed into the ground. Therefore, on an occasion where only the EMI performance is considered, the structure of the floating shield plate is more preferred.

For an MMC, the level of the output waveform is not only affected by the number of SMs N but is also closely related to the control period. The length of the control cycle interval directly determines the switching frequency of SM. Due to the difference in voltage of each SM, even if the number of SMs in on-state does not change at a specific control operation, the sorted order of the SM capacitor voltages will lead to the selected SMs triggered into on-state differ from the last step. As shown in Fig. 14(a) and (b), the EMI characteristic exhibits distinct peaks of the frequency corresponding to the control period, which is 10 kHz for 100 μs, and 1 kHz for 1 ms. Obviously, a larger control period will contribute to the reduction of the CM and DM EMI noise. The reference of the active and reactive power directly determines the output current of the converter, which affects the current flowing through the IGBT module and the diode reverse recovery process. The increase of active power and reactive power will aggravate the EMI noise in most of the frequency range, as shown in Fig. 14(c) and (d).

Table I lists the time for CPUs and the NVIDIA Tesla V100 GPU to simulate the 2-terminal MMC-HVdc system for 2 cycles duration (0.04 s) with a time-step of 10 ns. It can be seen that the multiple cores CPUs require a barely acceptable long period, whereas the GPU gains a remarkable speedup over the CPU.

VI. Conclusion

An accurate and efficient simulation method for EMI noise prediction during the design stage of the converter station in MMC-HVdc transmission system based on massively parallel implementation on GPU is presented in this article. The physics-based electrothermal dynamic semiconductor device model is adopted to the IGBT and FWD for its higher accuracy and easier acquisition of parameters. The circuit model is discretized and linearized by the backward Euler algorithm for time-domain simulation. According to the actual structure of the IGBT module package and SMs assembly, FEM analysis is conducted and the stray parameters of the converter are extracted in ANSYS Q3D extractor. The computational burden caused by the numerous nonlinear components is alleviated by fine-grained circuit partitioning of the SMs, which also improves numerical stability. The stray capacitance network is simplified based on Rosen's theorem, and a two-port equivalent wideband model of valve tower is established to handle the growing dimension of the capacitance matrix with the increase in converter levels. Instead of solving the entire MMC system circularly, the partitioned schemes are designed into hierarchical GPU kernels due to their identical attributes and structures, which are proceeded with a corresponding number of computational blocks and threads to attain a significant speedup. The measurement result indicates that the model has the capability to conduct small time-step EMI simulation for MMC using detailed nonlinear device-level and wideband models, which is scarcely feasible on commercial software. Simulation results manifest that EMI characteristics can be predicted integrally and comprehensively with different parameters and under various operating conditions.

Appendix

TABLE I
Execution Time of Two-Terminal MMC-HVdc Grid by CPUs and GPU for Two Cycles (0.04 s)

MMC Level	Execution Time (s)		Speedup
	20 CPU cores	V100 GPU	
21-L	4.423×10^4	3.36×10^3	13.16
61-L	1.48×10^5	3.71×10^3	39.89
101-L	2.64×10^5	4.56×10^3	57.89
201-L	5.46×10^5	6.38×10^3	85.58

TABLE II
Model Parameters of FUJI 6MBP30VAA060-50

V_P = 3.75, K = 0.4, KLM = 0.001, A_{FET} = 0.2, M_{FET} = 1.28, N_{FET} = 1.5, bn = 15, M_{bjt} = 1.64, $I_{sat_{bjt}}$ = 5.4e-9, R_{sh} = 5000 M_{fwd} = 1.46, $I_{sat_{fwd}}$ = 1e-6, R_b = 0.032, $C0_{gs}$ = 7.5e-8, Kgs_{shift} = 3.75, α_{ge} = 0.8, δ_{ge} = 0.5, $C0_{eg}$ = 3.8e-10, $Veg_{diff,off}$ = 2, $Veg_{diff,on}$ = 2, $\alpha_{eg_{off}}$ = 0.5, $\alpha_{eg_{on}}$ = 0.5, $\beta_{eg_{off}}$ = 6.23, $\beta_{eg_{on}}$ = 1.1, $\delta_{eg_{off}}$ = 0.21, $\delta_{eg_{on}}$ = 0.08, $C0_{ec}$ = 5.04e-10, Vec_{diff} = 0.7, α_{ec} = 0.5, β_{ec} = 1.01, δ_{ec} = 0.1, $\tau_{eb} = 5.5 \times 10^{-8}$, $\tau_s = 8 \times 10^{-8}$, $\tau_{fwd} = 1.5 \times 10^{-9}$, $\tau_{tail} = 3.9 \times 10^{-8}$, $\delta_{tail} = 5.74$, $R1_{fwd} = 0.75$, $R2_{fwd} = 0.7$, $R3_{fwd} = 0.2$, $SF1_{fwd} = 1.5$, $SF2_{fwd} = 3$, $L_C = 5 \times 10^{-10}$, $L_E = 5 \times 10^{-10}$, $R_G = 0.475$, $L_{AUX} = 5 \times 10^{-10}$, $T_n = 3.75 \times 10^{-14}$

TABLE III
Simulation Parameters of Prototype

$C_{SM} = 6\ mF$, $L_{arm} = 20\ mH$, $S_{transformer} = 0.0015\ MVA$, $K_{transformer} = 0.38\ /\ 0.145$, $U_K\ \% = 15\ \%$, $Udc_{ref} = 90\ V$, $Q_{ref} = 0\ Var$, $Kp_{dc} = 0.08$, $Ki_{dc} = 0.8$, $Kp_Q = 0.01$, $Ki_Q = 0.1$, $Kp_d = 0.5$, $Ki_d = 0.5$, $Kp_q = 0.05$, $Ki_q = 0.5$,

TABLE IV
Stray Parameters of FBSM

$R_{cs} = 0.00156\ Ohm$, $R_{cs} = 17\ nH$, $R_{es} = 0.00158\ Ohm$, $R_{es} = 17.735\ nH$, $R_{tm} = 0.0029\ Ohm$, $R_{tm} = 25.118\ nH$, $C_{sU} = 103.44\ pF$, $C_{sV} = 121.66\ pF$, $C_{sP} = 102.22\ pF$, $C_{sN} = 99.13\ pF$, $R_C = 0.0018\ Ohm$, $L_C = 17.73\ mH$, $C_g = 1213.56\ pF$, $C_{UV} = 7.67\ pF$, $C_{UP} = 6.45\ pF$, $C_{UN} = 6.25\ pF$, $C_{VP} = 7.58\ pF$, $C_{VN} = 7.35\ pF$, $C_{PN} = 6.17\ pF$, $C_{Ug} = 76.54\ pF$, $C_{Vg} = 90.02\ pF$, $C_{Pg} = 75.64\ pF$, $C_{Ng} = 73.35\ pF$.

TABLE V
Model Parameters of ABB 5SNA1200E330100

V_P = 7.33, K = 22.44, KLM = 0.001, A_{FET} = 0.94, M_{FET} = 1.25, N_{FET} = 1.55, $bn = 15$, M_{bjt} = 2.348, $I_{sat_{bjt}} = 5.45^{-9}$, $R_{sh} = 10^6$, M_{fwd} = 1.35, $I_{sat_{fwd}}$ = 1e-6, R_b = 0.016, $C0_{gs} = 10^{-7}$, Kgs_{shift} = 3, α_{ge} = 0.5, δ_{ge} = 1, $C0_{eg} = 5 \times 10^{-8}$, $Veg_{diff,off}$ = 0.7, $Veg_{diff,on}$ = 0.7, $\alpha_{eg_{off}}$ = 0.5, $\alpha_{eg_{on}}$ = 0.5, $\beta_{eg_{off}}$ = 2, $\beta_{eg_{on}}$ = 2, $\delta_{eg_{off}}$ = 0.0001, $\delta_{eg_{on}}$ = 0.0001, $C0_{ec} = 2^{-8}$, Vec_{diff} = 0.2, α_{ec} = 0.5, β_{ec} = 2, δ_{ec} = 0.0001, $\tau_{eb} = 5.5 \times 10^{-8}$, $\tau_s = 1 \times 10^{-9}$, $\tau_{fwd} = 2 \times 10^{-7}$, $\tau_{tail} = 1 \times 10^{-7}$, $\delta_{tail} = 0.2$, $R1_{fwd} = 0.8$, $R2_{fwd} = 0.4$, $R3_{fwd} = 0.1$, $SF1_{fwd} = 0.8$, $SF2_{fwd} = 4$, $L_C = 35.9 \times 10^{-9}$, $R_C = 5.3 \times 10^{-6}$, $L_E = 23.2 \times 10^{-9}$, $R_E = 5.3 \times 10^{-6}$, $L_G = 26.1 \times 10^{-9}$, $R_G = 0.2$, $R_{g,ext} = 10$, $T_n = 3.75 \times 10^{-14}$.

TABLE VI
SIMULATION PARAMETERS OF STUDY CASE

$C_{SM} = 10\ mF$, $L_{arm} = 20\ mH$, $S_{transformer} = 1050\ MVA$,
$K_{transformer} = 380\ kV\ /\ 220\ kV$, $U_K\ \% = 15\ \%$, $Udc_{ref} = 200\ kV$,
$Q_{ref} = 0\ Var$, $Kp_{dc} = 0.2$, $Ki_{dc} = 1$,$Kp_Q = 0.2$, $Ki_Q = 1$,
$Kp_d = 0.6$, $Ki_d = 6$, $Kp_q = 0.6$, $Ki_q = 6$,

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