IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received November 1, 2018, accepted November 20, 2018, date of publication December 3, 2018,
date of current version January 7, 2019.

Digital Object Identifier 10.1109/ACCESS.2018.2884506

Real-Time Simulation of Hybrid Modular Multilevel Converters Using Shifted Phasor Models

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This work supported in part by the National Key Research and Development Program of China under Grant 2017YFB0902000, in part by the National Natural Science Foundation of China under Grant 51737007, in part by the Science and Technology Project of State Grid under Grant SGXJ0000KXJS1700841, in part by the Power Electronics Science and Education Development Program of Delta Group, and in part by the Technology Projects of State Grid Corporation of China under Grant 522000180001.

ABSTRACT The real-time simulation of modular multilevel converter (MMC) is essential to the evaluation and validation of its control and protection systems. Moreover, the dynamics at both sub-module level and system level are expected from the real-time simulations of MMCs. To achieve this objective, this paper proposes the shifted phasor modeling (SPM) of the MMC by representing each sub-module with a Thevenin equivalent circuit that is derived using shifted phasors with improved accuracy. The efficiency of the SPM is guaranteed by modeling each arm as a switch-dependent Thevenin equivalent circuit. The computational burden remains almost unchanged even when the number of sub-modules increases considerably. The proposed model is materialized using field programmable gate array. And, thus the real-time simulation of MMC-based DC grids can be realized to capture the dynamics at the system level as well as the sub-module level. The effectiveness of this paper has been validated in terms of both accuracy and efficiency on a two-terminal MMC-based low-voltage direct current system.

INDEX TERMS DC systems, electromagnetic transient (EMT), field-programmable gate array (FPGA), hardware design, modular multilevel converter (MMC).

I. INTRODUCTION

MMC offers a better prospect for cost-effective power transmissions [1], [2]. In practical MMC projects, the real-time simulation on FPGA plays an essential role in the implementation of the control and protection systems [3], [4]. Since the voltage and current stresses in the circuits and components of MMC are critical for the design of its control and protection strategies, the real-time simulations need to provide the very details of dynamic responses of the system, including dynamics not only at the system level but also at the sub-module level.

Recently, different MMC accelerated models have been proposed, which can be categorized into two types: (i) *Analytical models*, such as the continuous-variable dynamic model [5], [6], and the steady state model [7], [8], etc. They are accurate and efficient to represent the MMC under steady-state conditions or small disturbances. However, these models cannot simulate DC faults because the nonlinear characteristics of the freewheeling diodes are not represented. (ii) *Averaged value models or AVM*, for instance, i.e., the converter-averaged model (CAM) [9], [10] and the arm-averaged model (AAM) [11]. The CAM separates the whole MMC into ac- and dc- side circuits, or controlled sources. The AAM uses six arms as the basic elements and thus improves the simulation accuracy, especially under dc faults or blockings. The above two types of models focus more on system level dynamics and are mainly adopted in off-line analyses.

For the real-time simulation based on field programmable gate arrays (FPGAs), both sub-module level and system level dynamics are required for detailed studies of a MMC-based system. However, the sub-module level modeling of MMC has always been a challenging task due to the large number of sub-modules in a single arm [3], [4]. On the one hand, the massive switching components greatly increase the number of nodes and the size of the admittance matrix of the system. As a result, it is very hard to model the MMC with high accuracy and real-time efficiency simultaneously. On the other hand, the real-time simulation of a practical AC/DC system would consume huge hardware resources of FPGAs. Usually some special emulation strategies, for instance, system decomposition and parallelization, should be delicately designed to make full use of the limited FPGAs. This also makes it a challenge to model the MMC properly for the real-time simulation.

Previously, several MMC models have been proposed for real-time simulations, such as the CAM in [10], the AAM in [12]–[15] and the detailed equivalent model (DEM) in [16]–[18]. However, they mostly focus on the system-level dynamics, without a simultaneous consideration of the dynamics at the sub-module level. Generally, the responses following DC faults have not been thoroughly investigated [13]. Moreover, when the sub-module of the DEM transits from the on-state to the off-state during the blocking period, numerical problems, i.e., the oscillations of the arm current, would appear [16]. Even worse, the accuracy of the DEM is sensitive to the off-state resistances of switches. In [17], different voltage balanced methods are compared on FPGA in order to reduce the resource utilization and the calculation burden. It should be noted that all these existing models cannot give phasor values and instantaneous values of AC quantities at the same time. Therefore, there is an urgent need for a MMC model that can provide dynamics at both sub-module and system levels.

Another issue is that most of existing MMCs adopt the topology with half-bridge or full-bridge sub-modules. But a recent requirement of MMC (as least here in China) is that it should have dc-fault blocking and dc-fault ride-through capabilities. As a result, hybrid MMC configurations with those capabilities are undergoing fast development. Thus there is a need for the modeling of such hybrid MMC to investigate its detailed dynamics through real-time simulations.

In this paper, the real-time shifted phasor modeling (SPM) method is proposed to address the above issues. Special emphases are put on its embedment in the FPGA-based real-time simulation of a hybrid MMC configuration with the mixed use of double half-bridge sub-module (DBSM) and cross-connected double half-bridge sub-module (CC-DBSM). The developed SPM has the following salient features:

1) As derived using the nodal analysis approach, the real-time SPM is much more accurate than the traditional averaged model.

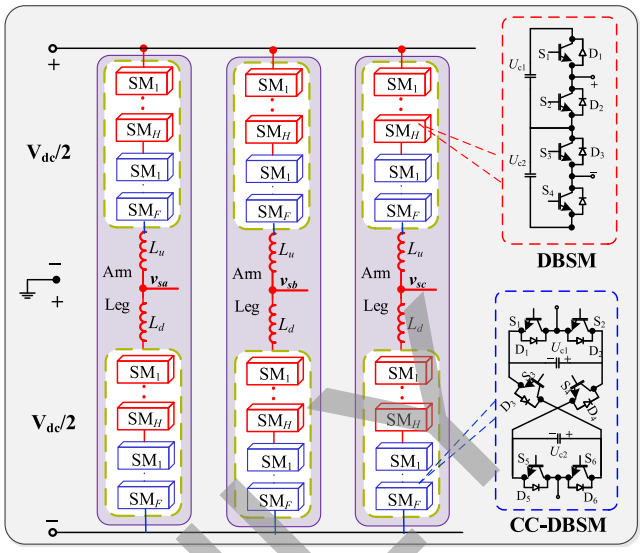

FIGURE 1. Circuit configuration of the hybrid MMC and its sub-modules.

2) It preserves the additional benefit of producing wide frequency band phasor and instantaneous values of AC quantities simultaneously and thus is suitable for the simulation of system dynamics at both sub-module and system levels..

3) With each arm of the SPM represented with a switch-dependent Thevenin equivalent circuit and the capacitor voltage of each sub-module updated in a parallel way, the computational burden remains almost unchanged as the number of sub-modules increases. In this way, the efficiency is guaranteed.

4) The SPM has been successfully implemented in the FPGA-based real-time simulation platform, on which the detailed dynamics of hybrid MMCs are emulated accurately and efficiently.

The rest of the paper is organized as follows: Section 2 presents the configuration of the target hybrid MMC. Section 3 details the SPM. In Section 4, the effectiveness of the SPM is validated with a practical hybrid-MMC based DC grid. Brief conclusions are drawn in Section 5.

II. HYBRID MODULAR MULTI-LEVEL CONVERTER

Fig. 1 shows the circuit configuration of the three-phase hybrid MMC, where each sub-module in a single arm can be either double half-bridge sub-module (DBSM) or cross-connected double half-bridge sub-module (CC-DBSM) [1]. The operation states of their switching devices are listed in Tables 1 and 2, respectively. As can be seen, both the DBSM and the CC-DBSM have broader output voltages than the half-bridge and full-bridge sub-modules. During normal states, DBSM and CC-DBSM can be regarded as double series-connected half-bridge sub-modules. Their output voltages are the sums of the capacitor voltages of the two inserted sub-modules. Another striking advantage of the hybrid MMC is that the additional CC-DBSMs in each arm enable the hybrid MMC to own the capability of blocking DC-side

TABLE 1. Operating State of DBSM.

State	S_1	S_2	S_3	S_4	Output
1	1	0	1	0	U_{c1}
2	0	1	0	1	U_{c2}
3	1	0	0	1	$U_{c1}+U_{c2}$
4	0	1	1	0	0
blocking	0	0	0	0	$U_{c1}+U_{c2}, i_{arm}>0$
					$0, i_{arm}<0$

TABLE 2. Operating State of CC-DBSM.

State	S_1	S_2	S_3	S_4	S_5	S_6	Output
1	0	1	1	0	0	1	U_{c1}
2	1	0	1	0	1	0	U_{c2}
3	0	1	1	0	1	0	$U_{c1}+U_{c2}$
4	1	0	1	0	0	1	0
5	1	0	0	1	0	1	$U_{c1}+U_{c2}$
blocking	0	0	0	0	0	0	$U_{c1}+U_{c2}, i_{arm}>0$
							$-U_{c1}-U_{c2}, i_{arm}<0$

TABLE 3. Switch number of different combinations(HBSM:half-bridge SM; FBSM:full bridge SM; CDSM: Clamp-Double SM).

Type	Submodule number	Switch number	Switch number of conduction	DC fault capability
HBSM+FBSM	$2N$	$5.732N$	$2.866N$	
DBSM+CDSM	N	$3.295N$	$1.431N$	
DBSM+CC-DBSM	N	$2.428N$	$1.214N$	yes

faults. That is to say, CC-DBSMs in blocking states can help to limit the fault current by providing the negative voltage in the circuit loop.

Suppose in each arm, there are n DBSMs and m CC-DBSMs in all. When the DC fault occurs and all the sub-modules are blocked, the maximum negative voltage provided by all the CC-DBSMs is:

$$v_{Fmax} = \frac{V_{dc}}{2(m+n)} \times 2m \tag{1}$$

In order to enable the dc-fault blocking capability, the maximum sum voltages of all the CC-DBSMs in the upper and lower arms should be larger than peak value of AC voltage (suppose the modulation ratio equals one):

$$\frac{V_{dc}}{2(m+n)} \times 4m > \frac{\sqrt{3}V_{dc}}{2} \tag{2}$$

In other words, the ratio between the number of CC-DBSMs and DBSMs should satisfy:

$$\frac{n}{m} \leq \frac{4}{\sqrt{3}} - 1 \tag{3}$$

As shown in Table 3, the combination of DBSMs and CC-DBSMs will have the least switch number and the least switch number of conduction, where the hybrid MMCs all have the dc fault blocking capability.

III. REAL-TIME SPM OF THE HYBRID MMCS BASED ON NODAL ANALYSIS APPROACH

A. BRIEF INTRODUCTION OF SHIFTED PHASOR MODELLING (SPM)

In a power system, electrical variables generally have a band-pass characteristic with their frequency band centered around the fundamental frequency ω_s, which can be represented by its shifted phasor form [19]–[21]:

$$\begin{cases} S(t) = \hat{S}(t)e^{j\omega_s t} \\ \hat{S}(t) = s_I(t) + js_Q(t) \end{cases} \tag{4}$$

where $\hat{S}(t)$ is also called complex envelope of the time-domain signal $S(t)$, which keeps the low-frequency dynamics of $S(t)$; $s_I(t)$ and $s_Q(t)$ are the real and imaginary parts of $\hat{S}(t)$. The envelope or the phasor of the time-varying signal $s_I(t)$ can be calculated by:

$$\left\|\hat{S}(t)\right\| = \sqrt{[s_I(t)]^2 + [s_Q(t)]^2} \tag{5}$$

Moreover, (1) can be also expressed as follows [19]–[21]:

$$S(t) = s(t) + jH[s(t)] \tag{6}$$

where

$$H[s(t)] = \frac{1}{\pi}\int_{-\infty}^{\infty} \frac{s(\tau)}{t-\tau} d\tau \tag{7}$$

denotes the Hilbert transformation.

Theoretically, SPM models have the following advantages:

i) They can use a much larger time step than traditional EMT models so that simulation efficiency will be dramatically improved without the loss of accuracy.

ii) The dynamics at both system level and sub-module level are preserved.

iii) They produce instantaneous and phasor waveforms simultaneously.

iv) SPM models capture wide-band frequency dynamics. Actually, the frequency band of SPM models is just limited by the time step.

Thanks to above distinct features, the SPM concept is adopted hereafter to develop the models of hybrid MMC.

B. SPM BASED EQUIVALENT MODEL OF THE CAPACITOR

Based on the concept of SPM, the dynamics of the capacitor in each sub-module can be expressed by [19]–[21]:

$$\frac{d\hat{v}_c(t)}{dt} = \frac{1}{C}[\hat{i}_c(t) - j\omega_s C\hat{v}_c(t)] \tag{8}$$

where $\hat{v}_c(t)$, $\hat{i}_c(t)$ are the shifted phasors of the capacitor voltage and current.

With shifted phasors converted back into the time-domain form, the capacitor current can be obtained and discretised based on the Trapezoidal algorithm, or

$$i_c(t) = [\frac{2C}{\Delta t} + j\omega_s C]v_c(t) + [-\frac{2C}{\Delta t} + j\omega_s C]v_c(t-\Delta t)e^{j\omega_s \Delta t} - i_c(t-\Delta t)e^{j\omega_s \Delta t} \tag{9}$$

where Δt is the simulation step. After some manipulations, the Norton equivalents, or the conductance and the equivalent current of the capacitor, can be expressed by

$$\begin{cases} i_c(t) = Gv_c(t) + J_c(t-\Delta t) \\ J_c(t-\Delta t) = Ai_c(t-\Delta t) + Bv_c(t-\Delta t) \end{cases} \tag{10}$$

where

$$\begin{cases} A = -e^{j\omega_s \Delta t} \\ B = [-\frac{2C}{\Delta t} + j\omega_s C]e^{j\omega_s \Delta t} \\ G = 1 \Big/ [\frac{2C}{\Delta t} + j\omega_s C] \end{cases} \tag{11}$$

Based on the rotation transformation matrix (9) [22], the capacitor current (7) is further expressed with the separate real and imaginary parts as shown in (10), where the parameters are derived by the rotation transformation.

$$T(t) = \begin{bmatrix} \cos\omega_s t & \sin\omega_s t \\ -\sin\omega_s t & \cos\omega_s t \end{bmatrix} \tag{12}$$

$$\begin{cases} \begin{bmatrix} i_c^x(t) \\ i_c^y(t) \end{bmatrix} = G_{cxy} \begin{bmatrix} v_c^x(t) \\ v_c^y(t) \end{bmatrix} + \begin{bmatrix} J_c^x(t-\Delta t) \\ J_c^y(t-\Delta t) \end{bmatrix} \\ \begin{bmatrix} J_c^x(t-\Delta t) \\ J_c^y(t-\Delta t) \end{bmatrix} = K_v \begin{bmatrix} v_c^x(t-\Delta t) \\ v_c^y(t-\Delta t) \end{bmatrix} + K_i \begin{bmatrix} i_c^x(t-\Delta t) \\ i_c^y(t-\Delta t) \end{bmatrix} \end{cases} \tag{13}$$

with

$$\begin{cases} G_{cxy} = \dfrac{2C}{\Delta t} I_{2\times 2} - T(-\dfrac{\pi}{2\omega_s})\omega_s C \\ K_v = -\dfrac{2C}{\Delta t} I_{2\times 2} - T(-\dfrac{\pi}{2\omega_s})\omega_s C \\ K_i = -T(-\dfrac{\pi}{2\omega_s}) \end{cases} \tag{14}$$

where G_{cxy}, $\left[J_c^x(t-\Delta t)\ J_c^y(t-\Delta t) \right]^T$ denotes the conductance matrix and the equivalent current vector in the xy coordinate.

Finally, the Thevenin resistance R_{ceq} and the Thevenin equivalent voltages $[v_{ceq}^x(t-\Delta t), v_{ceq}^y(t-\Delta t)]^T$ in the xy coordinate of the capacitor are obtained as:

$$\begin{cases} R_{ceq} = \left[G_{cxy}\right]^{-1} \\ \begin{bmatrix} v_{ceq}^x(t-\Delta t) \\ v_{ceq}^y(t-\Delta t) \end{bmatrix} = -\left[G_{cxy}\right]^{-1} K_v \begin{bmatrix} v_c^x(t-\Delta t) \\ v_c^y(t-\Delta t) \end{bmatrix} \\ -\left[G_{cxy}\right]^{-1} K_i \begin{bmatrix} i_c^x(t-\Delta t) \\ i_c^y(t-\Delta t) \end{bmatrix} \end{cases} \tag{15}$$

Eq. (9) instead of the Trapezoidal method in [3] is used for discretization because the former can achieve higher accuracy than the latter [19]. Moreover, the proposed method can produce phasor and instantaneous values simultaneously, showing dynamics at the sub-module level and the system level. Specifically, instantaneous values can be used for control and protection strategies of the MMC, and phasor values can be used for studying interactions between the MMC and the AC grids.

C. SPM BASED EQUIVALENT MODEL OF THE SUB-MODULE

As indicated above, either DBSM or CC-DBSM can be regarded as double series-connected half-bridge sub-modules in the normal state. So the equivalent models of DBSM and CC-DBSM can be obtained using those of the upper and lower half-bridge sub-modules.

Taking the capacitors and switches into account, the upper sub-module of the DBSM in Fig. 1 can be replaced with an equivalent Thevenin circuit, which is governed by

$$\begin{bmatrix} v_{sm}^x(t) \\ v_{sm}^y(t) \end{bmatrix} = \begin{bmatrix} R_{sm} & \\ & R_{sm} \end{bmatrix} \begin{bmatrix} i_{arm}^x(t) \\ i_{arm}^y(t) \end{bmatrix} + \begin{bmatrix} v_{sm,h}^x(t-\Delta t) \\ v_{sm,h}^y(t-\Delta t) \end{bmatrix} \tag{16}$$

In (16), the resistance R_{sm} and the sub-module voltage $v_{sm,h}(t-\Delta t)$ in the xy coordinate are calculated by

$$R_{sm} = \frac{R_2(R_1 + R_{ceq})}{R_1 + R_2 + R_{ceq}} \tag{17}$$

$$\begin{bmatrix} v_{sm,h}^x(t-\Delta t) \\ v_{sm,h}^y(t-\Delta t) \end{bmatrix} = \begin{bmatrix} v_2^x \\ v_2^y \end{bmatrix} + \frac{R_2}{R_1 + R_2 + R_{ceq}} \times \begin{bmatrix} v_1^x + v_2^x - v_{ceq}^x(t-\Delta t) \\ v_1^y + v_2^y - v_{ceq}^y(t-\Delta t) \end{bmatrix} \tag{18}$$

where $i_{arm}^x(t)$, $i_{arm}^y(t)$ are the arm current in the xy coordinate; R_1, R_2 are the on/off-state resistances of switches S_1 and S_2; v_i^x, v_i^y, $i = 1, 2$ are the corresponding on/off-state threshold voltages in the xy coordinate.

For each sub-module, the capacitor voltage is updated with (13). Particularly, the capacitor current for each sub-module is calculated by:

$$\begin{cases} i_c^x(t) = \dfrac{R_2 i_{arm}^x(t) + v_1^x + v_2^x - v_{sm,h}^x(t-\Delta t)}{R_1 + R_2 + R_{ceq}} \\ i_c^y(t) = \dfrac{R_2 i_{arm}^y(t) + v_1^y + v_2^y - v_{sm,h}^y(t-\Delta t)}{R_1 + R_2 + R_{ceq}} \end{cases} \tag{19}$$

Finally, by connecting the Thevenin equivalents of the upper and lower sub-modules in series connection, the overall switch- dependent Thevenin equivalent model of the DBSM, which are determined by the switch function S_1 and S_4, is given by

$$\begin{aligned} \begin{bmatrix} v_{Dsm}^x(t) \\ v_{Dsm}^y(t) \end{bmatrix} &= R_{Deq} \begin{bmatrix} i_{arm}^x(t) \\ i_{arm}^y(t) \end{bmatrix} + v_{Deq}^{xy}(t-\Delta t) \\ &= S_1 \left\{ \begin{bmatrix} R_{sm}^u & \\ & R_{sm}^u \end{bmatrix} \begin{bmatrix} i_{arm}^x(t) \\ i_{arm}^y(t) \end{bmatrix} + \begin{bmatrix} v_{sm,h}^{u,x}(t-\Delta t) \\ v_{sm,h}^{u,y}(t-\Delta t) \end{bmatrix} \right\} \\ &\quad + S_4 \left\{ \begin{bmatrix} R_{sm}^l & \\ & R_{sm}^l \end{bmatrix} \begin{bmatrix} i_{arm}^x(t) \\ i_{arm}^y(t) \end{bmatrix} + \begin{bmatrix} v_{sm,h}^{l,x}(t-\Delta t) \\ v_{sm,h}^{l,y}(t-\Delta t) \end{bmatrix} \right\} \end{aligned} \tag{20}$$

where R_{sm}^u, $\left[v_{sm,h}^{u,x}(t-\Delta t)\ v_{sm,h}^{u,y}(t-\Delta t) \right]^T$ are the equivalent resistances and voltages of the upper sub-module

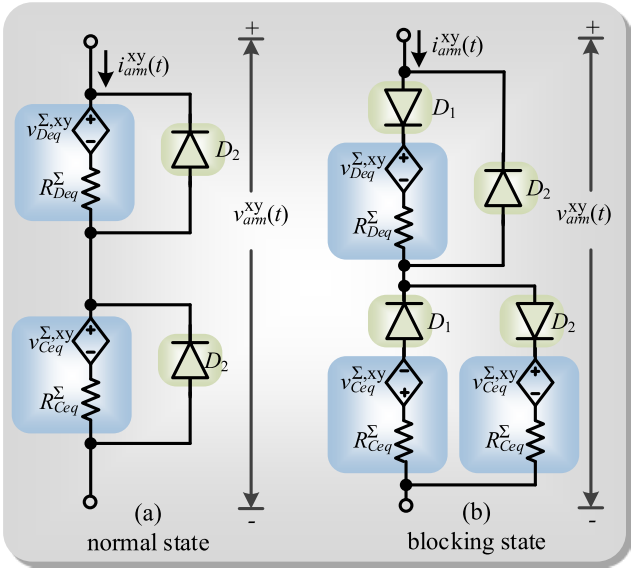

FIGURE 2. Equivalent arm model for the hybrid MMC considering the DC-fault blocking capability.

of DBSM; R^{l}_{sm}, $\left[v^{l,x}_{sm,h}(t-\Delta t)\ v^{l,y}_{sm,h}(t-\Delta t)\right]^{T}$ are the equivalent resistances and voltages of the lower sub-module of DBSM.

Similarly, the switch dependent Thevenin equivalent model of CC-DBSM, i.e., R_{Ceq}, $v^{xy}_{ceq}(t-\Delta t)$ can be derived.

D. SPM BASED EQUIVALENT MODEL OF THE ARM

As shown in Fig. 2, there are multiple DBSMs and CC-DBSMs connected in series for each arm. The final SPM-based equivalent model of the arm can be obtained by combining the equivalent models of all the sub-modules. Specifically, the equivalent resistance $R^{\sum}_{Deq}$ and the Thevenin equivalent voltage $v^{\sum,xy}_{Deq}(t-\Delta t)$ of all the DBSMs are calculated by

$$\begin{cases} R^{\sum}_{Deq} = \sum_{k=1}^{D} R^{k}_{Deq} \\ v^{\sum,xy}_{Deq}(t-\Delta t) = \sum_{k=1}^{D} v^{k,xy}_{Deq}(t-\Delta t) \end{cases} \tag{21}$$

where D is the number of DBSMs in the arm.

In (18), $R^{\sum}_{Deq}$, $v^{\sum,xy}_{Deq}(t-\Delta t)$ represent all the DBSMs. They are also the interface circuits for the system-level calculations. The Thevenin equivalents of all the CC-DBSMs, denoted as $R^{\sum}_{Ceq}$, $v^{\sum,xy}_{Ceq}(t-\Delta t)$, can be derived in the same way.

For practical implementation (see Fig. 2), the diodes are treated as a Ron/Roff resistance model in the network solution [4]. Specifically (see Fig. 2), when the voltage of the diode D_2,i.e., $v_{D2}(t)$ is larger than 0, the diode D2 is represented as a resistance of R_{on}, otherwise, it will be represented as a resistance of R_{off}. The overall Thevenin equivalents of DBSMs are derived by

$$R_D = \begin{cases} \dfrac{R_{on}R^{\sum}_{Deq}}{R_{on}+R^{\sum}_{Deq}},\ v_{D2}(t) \geq 0 \\ \dfrac{R_{off}R^{\sum}_{Deq}}{R_{off}+R^{\sum}_{Deq}},\ v_{D2}(t) < 0 \end{cases} \tag{22}$$

$$V_D = \begin{cases} \dfrac{V^{\sum,xy}_{Deq}R^{\sum}_{Deq}}{R_{on}+R^{\sum}_{Deq}}R^{\sum}_{Deq} + V^{\sum,xy}_{Deq},\ v_{D2}(t) \geq 0 \\ \dfrac{V^{\sum,xy}_{Deq}R^{\sum}_{Deq}}{R_{off}+R^{\sum}_{Deq}}R^{\sum}_{Deq} + V^{\sum,xy}_{Deq},\ v_{D2}(t) < 0 \end{cases} \tag{23}$$

where R_D, V_D are the Thevenin resistance and voltage of DBSMs, respectively; $v_{D2}(t)$ is the voltage of diode D_2. Thevenin equivalents of CC-DBSMs can be similarly derived.

Thus the equivalent arm model for the hybrid MMC is obtained as in Fig. 2, which consists two common states. As can be seen, only one node is added in the nodal voltage equation for each phase of the system. Otherwise the dimension of the nodal voltage equation will be expanded when the number of sub-modules rises [23], [24]. This is why the proposed Norton equivalent circuit guarantees the simulation efficiency by reducing the number of nodes in each arm. Specifically, in the normal state (namely State N), both DBSM and CC-DBSM are operated as double series-connected half-bridge sub-modules. The output voltage of each sub-module is either positive or zero and then the diode D_2 is always off. However, in the blocking state (namely State B), the diode D_1 is not bypassed and the capacitor of DBSM can only be charged, just like the characteristics of the half-bridge sub-modules. Unlike the DBSM, the capacitor of the CC-DBSM can either be charged or discharged according to the direction of $i_{arm}(t)$. When $i_{arm}(t) < 0$, the CC-DBSMs provide negative voltages to the circuit loop to limit the fault current. If the sum of the capacitor voltages is larger than the AC line voltage, the DC fault would be blocked. Otherwise when $i_{arm}(t) > 0$, the arm current flows into the capacitor. However, as the AC line voltage is smaller than the sum of the capacitor voltages, the capacitor voltage of the CC-DBSM would not be charged. It should be noted that the SPM can also applied to other typologies, and DBSM/CC-DBSM sub-modules are adopted as typical examples.

IV. REAL-TIME SIMULATIONS PLATFORM OF THE HYBRID MMCs ON FPGAs

Fig. 3 shows the hardware implementation of the real-time simulation platform of the hybrid MMCs. The core calculations are carried out in the Virtex 7 FPGA xc7x485tffg 1761-2, which has 303600 look-up tables (LUTs), 607200 flip-flops (FFs) and 2800 digital signal processing (DSP) slices. The simulation results obtained in the FPGA are transferred through a DAC board (DAC34H84 EVM) to the oscilloscope, which displays the results as waveforms.

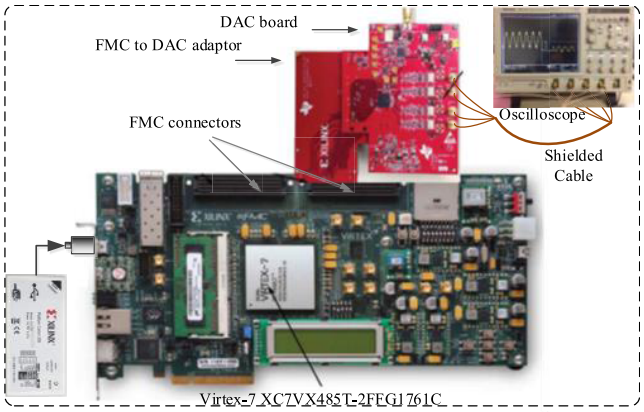

FIGURE 3. Experimental setup with FPGA-based hardware emulator.

TABLE 4. Latencies and hardware resource utilization (in percentage) of key hardware modules.

Module	Latency	LUT	FF(FIFO)	DSP
Phase shift control	33 T_{clk}	3837 (1.26%)	2320 (0.38%)	9 (0.32%)
Sub-module unit	109 T_{clk}	11811 (3.89%)	7963 (1.31%)	45 (1.61%)
Updates of capacitors	67 T_{clk}	22944 (7.56%)	15772 (3.11%)	94 (3.36%)
Network solution	110-120 T_{clk}	24834 (8.18%)	8925 (1.47%)	66 (0.63%)
Calculates of power	7 T_{clk}	1719 (0.57%)	1874 (0.31%)	27 (1.31%)

In order to achieve high-level parallelism as well as pipelined structure, the whole system is divided into several juxtaposed modules and each module is implemented as an IP-Core using the Vivado HLS® synthesis. The key modules are listed in Table 4. They are: i) the MMC controller, to implement the various control functions, including the current tracking control and the phase-shifted carrier control; ii) the sub-module solvers, to calculate the SPM-based equivalent model of each sub-module; iii) the capacitor updater, to update the capacitor voltage of each sub-module; iv) the network solvers, to calculate the nodal voltage equation of the AC system; and v) the power calculator, to calculate the instantaneous powers of the MMC. Moreover, every variable is represented in the form of single floating point format. IP cores in Xilinx Vivado HLS® synthesis are next used for matrix computation.

The latency and the hardware resource utilization (HRU) are two crucial factors that affect the real-time performance. Their values for each key module are obtained from Vivado HLS® synthesis and listed in Table 3. It can be seen that the longest latency is attributed to the module of network solver. It takes up to 110-120 T_{clk}, where $T_{clk} = 10\ ns$, referring to the clock cycle of the FPGA (Note: The frequency of FPGA is 100 MHz). To achieve real-time simulation, the sum of all latencies should be less than a single simulation step. In our design, the total latency is in the range of 326-336 T_{clk}, which means that a simulation with a time

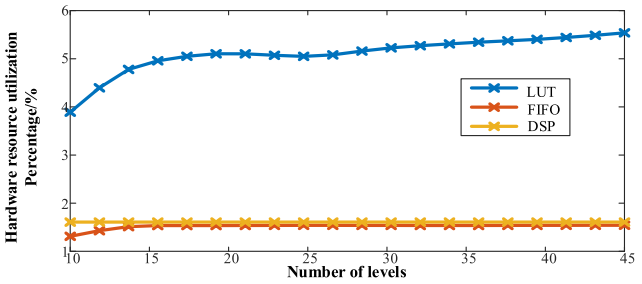

FIGURE 4. Relationship between the HRU and the level of MMC.

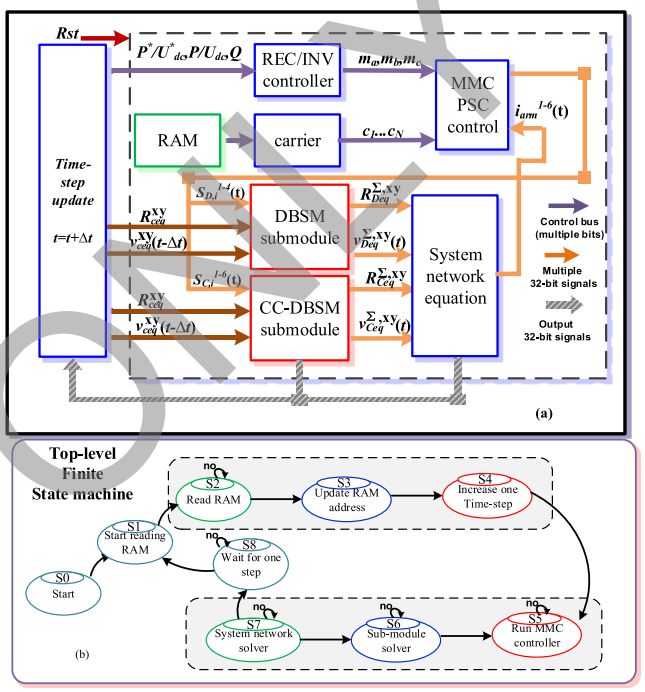

FIGURE 5. The functional configuration of the FPGA-based simulation platform (a) the pipe-lined hardware structure; (b) the top-level state machines.

step more than 10 μs can be efficiently implemented in real time with our developed platform.

Fig. 4 shows the exact relationship between the HRU in percentage and the level of MMC. As the level of MMC increases, the utilized LUTs and FFs of each module grow as well. Noticeably, the increase of HRU is very slow when the level of MMC reaches 30 or more. Specifically, a 45-level MMC just consumes less than 2 times of LUTs and FFs than the 10-level MMC. Therefore, the hardware resources of the target FPGA board are sufficient to simulate hybrid MMCs with even high levels.

Fig. 5(a) illustrates the pipelined hardware structure and the data flow routes of the FPGA-based simulation platform. Each module is packaged into a functional block that is executed in a parallel mode. Controlled by the finite-state machine, all the modules are simulated in a coordinated way, as shown in Fig. 5(b). When the FPGA is reset, the real-time simulation platform will be activated, leaving the standstill

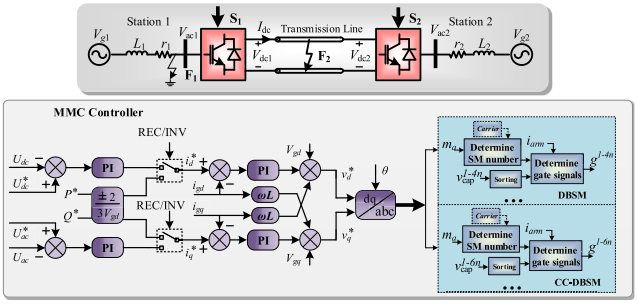

FIGURE 6. Two-terminal DC transmission system with an 11-level hybrid MMC and the control system.

state (S_0) for the initialization state (S_1). Then in the states of S_2 and S_3, the simulation reads the RAMs to load the previously stored data, such as the carrier waveforms for the MMC control. In the following state of S_4, the simulation time is increased by one iteration step. The control of MMC is fulfilled in state S_5. Specifically, the rectifier/inverter (REC/INV) stations receive the commands of reactive/active power or DC voltage and calculate the three-phase reference waveforms, i.e., m_a, m_b, m_c, based on the current-tracking strategies of the MMC. Correspondingly, the driving pulses for each sub-module are generated according to the phase-shifted carrier (PSC) control law. In the state of S_6, the SPM-based model of each sub-module is calculated and then summarized to constitute the overall SPM-based equivalent model of the arm, which is represented by the combination of the Thevenin equivalent of the DBSM, i.e., $R_{Deq}^{\sum}$, $v_{Deq}^{\sum,xy}(t-\Delta t)$ and the Thevenin equivalent of the CC-DBSM, i.e., $R_{Ceq}^{\sum}$, $v_{Ceq}^{\sum,xy}(t-\Delta t)$. The system network solver is executed in the state of S_7 to solve the nodal voltage equations of the entire circuit. Meanwhile, the arm currents or $i_{arm}^{1-6}(t)$ are sent back to the module of MMC control to derive the control variables for the next iteration. After that, the state is transferred from S_8 to S_2, starting a new round of simulation. The simulation would come to an end if the pre-set time is reached or it is manually terminated.

V. NUMERICAL SIMULATION RESULTS

Case studies are carried out on a two-terminal low voltage direct current (LVDC) system with an 11-level hybrid MMC, where the dc voltage is rated as ±20kV (see Fig. 6). Each arm of the MMC consists of 4 DBSMs and 1 CC-DBSM. The number of levels is selected according to a distributed network in Suzhou, Jiangsu Province in China and the level number of arm voltages can be identified from the waveforms of the oscilloscope clearly. Among the stations of S_1 and S_2, one is operated as the rectifier and the other as the inverter. The control structure of both stations, as also shown in Fig. 6, are the same except that different references are used for the different control mode. The inner loop is the current-tracking control in the d-q reference frame. In the outer loops, station S_2 adopts the DC voltage control to maintain the voltage of DC links; while station S_1 uses the reactive power control to produce the required var. The over-current protection (OCP) and the voltage-derivative protection (VDP) are also implemented in the simulation as the DC line protection (LPR) of the MMC. The PI section model is used for the transmission line. The reference curves are obtained using the detailed switching model with EMT simulations in PSCAD/EMTDC.

For the real-time simulations of our cases, both the main circuit and the controller are implemented in FPGA boards. Specifically, the main circuit in Fig. 6 is implemented as several modules in the FPGA, such as the sub-module solver module, capacitor updater network solver module, etc. The controller in Fig. 6 is also implemented as several modules in the FPGA, such as the MMC controller module, power calculator module, etc. As both the main circuit and the controller are programmed in the FPGAs, the new modelling of the main circuit and new control strategies can be tested in the FPGA freely.

A. STEADY-STATE SIMULATION

Fig. 7 shows the steady-state waveforms of the MMC, including the converter output voltage, the arm voltage and the currents of the upper & lower arms. In each sub-plot, the results obtained with the real-time simulation platform (in the upper part) are compared side by side with those obtained with the commercial software of PSCAD/EMTDC, where the time step of 10 μs is used. Obviously, they are very consistent. Moreover, the real-time simulation can capture the switching dynamics of the arm voltage.

The waveforms of capacitor voltages of the upper and lower arms in Fig. 8 also show that SPM produces almost the same dynamic responses of each sub-module as the PSCAD/EMTDC. Therefore, the effectiveness of the SPM in simulating the dynamics at the sub-module level is confirmed.

B. SIMULATION OF A SYMMETRICAL AC FAULT

A three-phase resistive short-circuit is applied at F1 in Fig. 6. The fault starts at $t = 0.35\ s$ and lasts for 50 ms. The comparisons of dynamic responses are displayed in Fig. 9. It can be seen that the real-time simulation results are in good agreement with those of PSCAD/EMTDC. Immediately after the fault, an evident drop of the arm voltage and the capacitor voltages can be observed in Figs. 9 (a) and (c). As a result, the magnitude of the arm voltage during the fault is much smaller than its steady-state value. Nevertheless, the sub-module of each arm will not be blocked during the AC fault. Such a simulation case has demonstrated that the SPM can precisely reflect the detailed responses of the capacitor at each sub-module when a fault happens on the AC side of the MMC. Moreover, Figs. 10-11 shows the AC voltages and currents, including instantaneous values in xy coordinate and their corresponding phasor curves. Clearly, the latter matches the envelopes of the former exactly. Of particular note is that the phasor curves of the SPM can perfectly reflect wide-band frequency interactions, especially around the clearance of the fault. Therefore, our SPM is more suitable for studies of both sub-module level and system level dynamics.

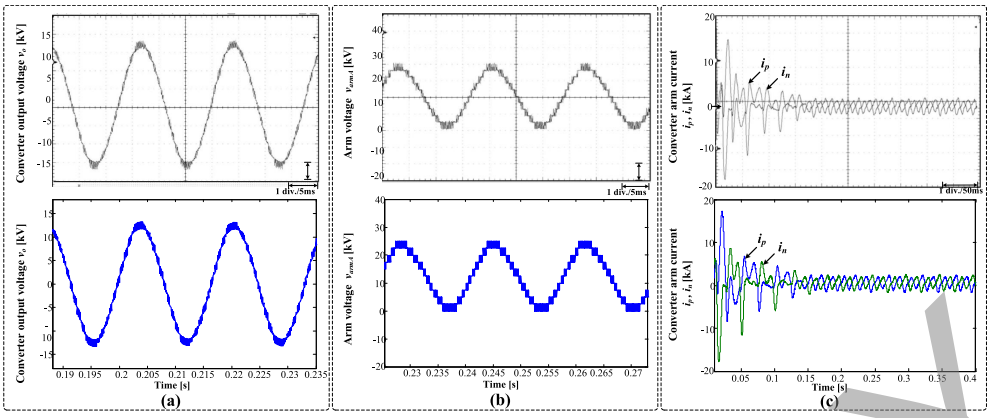

FIGURE 7. Steady-state results: (a) converter output voltage of phase A; (b) arm voltage of phase A; (c) upper and lower arm currents of phase A.

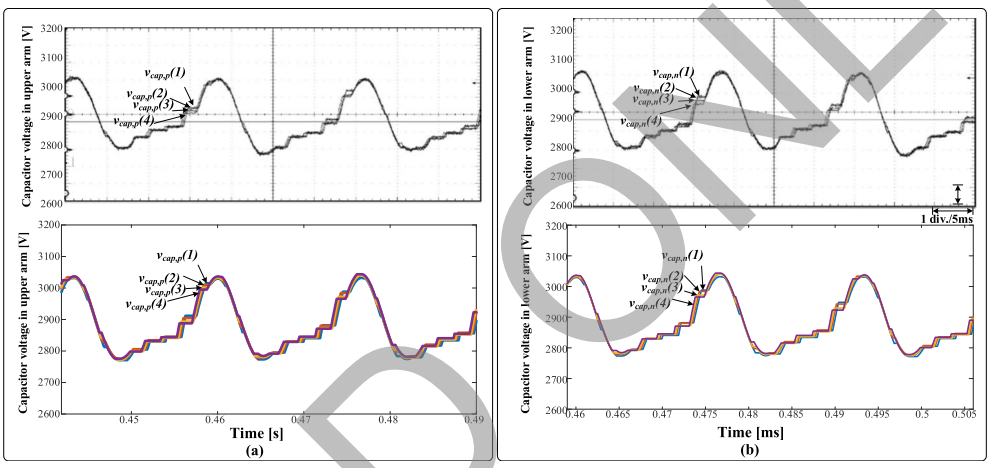

FIGURE 8. Capacitor voltages of upper and lower arms in phase A.

C. SIMULATION OF A DC FAULT WITH DC-FAULT BLOCKING

A DC pole-to-pole fault is trigged at 0.3 s. Soon the DC current reaches its threshold and the OCP acts to block all IGBTs. As a result, the MMC operates in the rectifier mode until t=0.32s, when the AC-side circuit breaker (CB) opens to isolate the MMC. This simulation case is used to validate the SPM of the hybrid MMC under a DC-fault blocking condition.

Fig. 12 shows the DC currents, the arm voltage of phase A and the capacitor voltages of both the DBSM and the CC-DBSM. It is demonstrated in Fig.12(a) that the fault current of the hybrid MMC is limited to less than 3.5 times of the steady state DC currents. The dynamics of capacitor voltages are displayed in Fig.12(c). Once the DBSM is blocked, its capacitor cannot be charged because the DC voltage of all inserted sub-modules is higher than the AC voltage. So the capacitor voltage is kept fixed. However, the blocking status of CC-DBSM does not prevent its capacitor from being charged by the arm current. As analyzed in Section III(B), when $i_{arm}(t) < 0$, the output voltage of CC-DBSM is negative. And the current from the AC side to the fault location at the DC side flows through the capacitor of each CC-DBSM. In such case, all the CC-DBSMs in the arm provide negative capacitor voltages and the DC fault current is limited. Meanwhile, the absolute values of capacitor voltages of CC-DBSMs will be increased due to the charging current. Otherwise, if $i_{arm}(t) > 0$, both the DBSM and the CC-DBSM provide positive voltages in the circuit loop. And the capacitor voltage of the CC-DBSM is still charged by the arm current. As shown in Fig. 12(c), only when the AC-side CB is switched off, will the DC current gradually drop to zero. Then the capacitor voltages of the CC-DBSM remain unchanged. As also displayed in Fig. 12(b), when $i_{arm}(t) > 0$, the arm current flows into each sub-module. The voltage of each sub-module as well as the whole arm is zero. However, when $i_{arm}(t) < 0$, the arm voltage is the sum of the voltages of all CC-DBSMs in that arm.

D. COMPARISONS OF SIMULATION PERFORMANCE

To compare the simulation accuracy, the proposed SPM and the DEM given in [10] are adopted in the same simulation platforms. The reference results are obtained by simulating

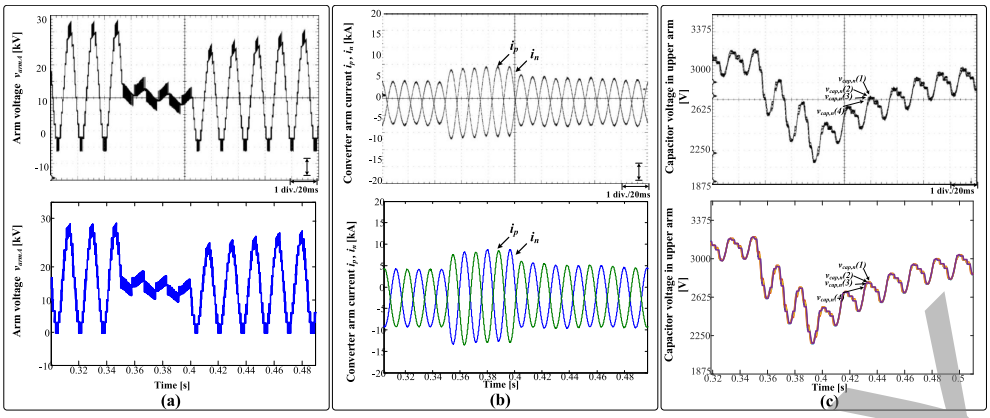

FIGURE 9. Responses with a 50 ms asymmetrical fault applied at $t = 0.35s$: (a) arm voltage of phase A; (b) upper and lower arm currents of phase A; (c) Capacitor voltages of the upper arm in phase A.

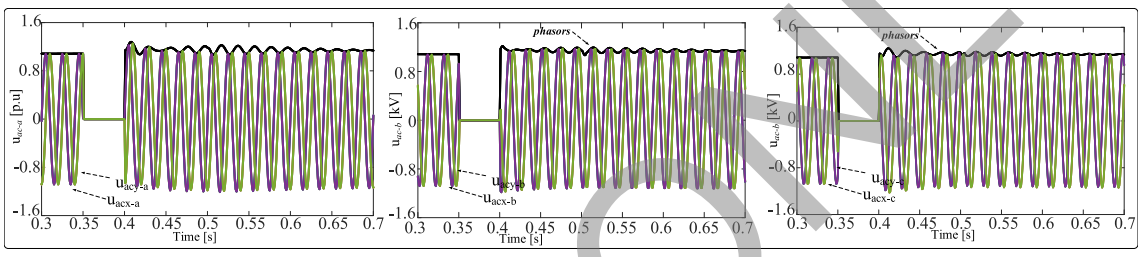

FIGURE 10. Phasors and instantaneous values of AC voltages.

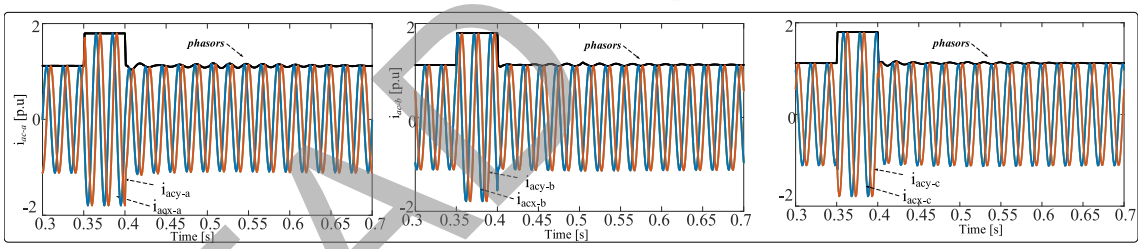

FIGURE 11. Phasors and instantaneous values of AC currents.

the system using the detailed model under an unanimous time step of 1 μs. Fig. 13 shows the relative accuracy improvement of the SPM over the DEM, which is defined as

$$R_\varepsilon = \left\| (\varepsilon_{avg}^{DEM} - \varepsilon_{avg}^{SPM})/\varepsilon_{avg}^{DEM} \right\| \tag{24}$$

where ε_{avg}^{DEM}, ε_{avg}^{SPM} are the per-unitized average simulation errors of DEM and SPM, respectively. The definition of the average simulation errors can be referred to [23].

Errors of different methods under different time steps are given in Table 5. As can be seen, errors of both DPM and DEM become larger when the time step is increased. However, results of the proposed DPM is more accurate than those the DEM at each time step. Fig. 13 shows the improvement in accuracy as the time step grows. Evidently, the accuracy of the DC current and voltage, achieves a more-than 50% improvement as compared to the DEM when the time step is 200 μs or above. As the time step become larger, the accuracy improvement of DPM over the DEM is even more significant. Taking such improvement in simulation accuracy and the real-time performances into account, the proposed model is

TABLE 5. Errors (ϵ_{avg}) (Unit: p.u.) of different methods under different time steps table

Methods	V_{ac1}	u_{dc}	i_{dc}	u_{armA}	i_{armA}	U_{cap1}	U_{cap2}
DEM-20s	0.041	0.01	0.004	0.064	0.016	0.015	0.018
DEM-50s	0.052	0.019	0.007	0.159	0.033	0.046	0.039
DEM-100s	0.082	0.028	0.012	0.191	0.078	0.071	0.082
DPM-20s	0.025	0.007	0.003	0.056	0.012	0.014	0.012
DPM-50s	0.048	0.012	0.005	0.101	0.025	0.032	0.024
DPM-100s	0.059	0.015	0.007	0.112	0.052	0.042	0.052

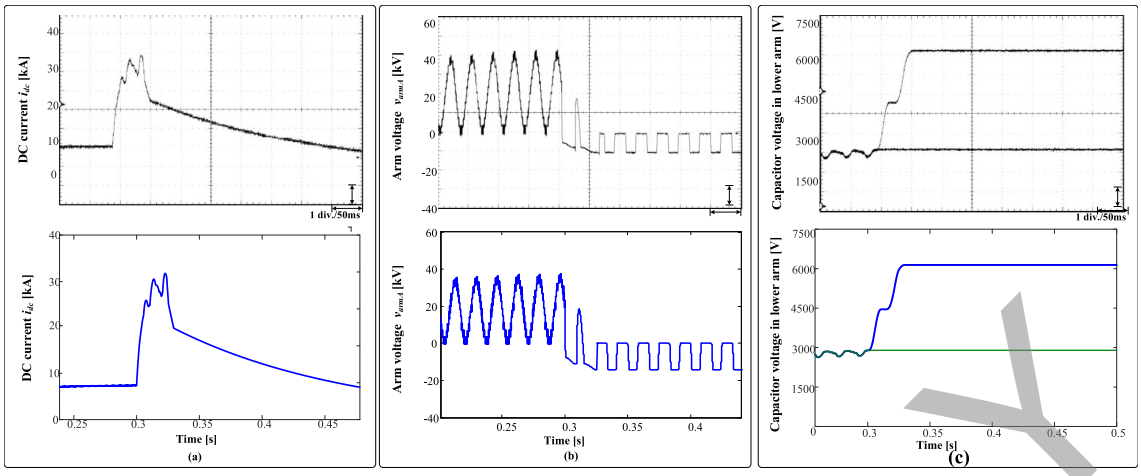

FIGURE 12. Responses with a DC pole-to-pole fault applied at t = 0.3s: (a) DC currents; (b) upper arm voltages of phase A; (c) Capacitor voltages of the DBSM and the CC-DBSM sub-modules.

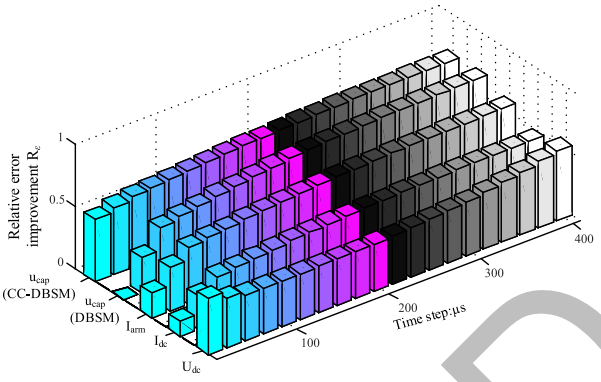

FIGURE 13. Relative Error improvement of SPM over DEM.

expected to be more suitable for the real-time simulation of large-scale AC/DC systems with even more complicated MMC topologies.

VI. CONCLUSION

In this paper, the real-time dynamic phasor modeling method, which is based on the nodal analysis approach, is proposed to capture the dynamics of MMC at both system and sub-module levels accurately and efficiently. Special emphasis has been put on the embedment of the DPM in the FPGA-based real-time simulation of a hybrid MMC configuration. Each sub-module of the hybrid MMC is equivalently represented by the dynamic phasor model (DPM), of which each arm is replaced by a switch-dependent Thevenin equivalent circuit and the sub-module capacitor voltage is updated in a parallel way.

The proposed SPM is realized in a real-time simulation platform based on FPGAs. As demonstrated in a two-terminal MMC-based LVDC system, the developed SPM can give phasor values and instantaneous values of AC quantities simultaneously, which is suitable for both sub-module level and system level dynamics. Moreover, it has achieved an improved accuracy over the traditional averaged model. Therefore, the real-time shifted phasor modeling method offers great potential for the accurate and real-time simulations MMC-based systems.

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