A Highly-Integrated Low-Intensity Ultrasound System for Wearable Medical Therapeutic Applications

by

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Abstract

Ultrasound therapy has a long history of novel applications in medicine. Compared to high-intensity ultrasound used for tissue heating, low-intensity ultrasound (LIUS) has drawn increasing attention recently due to its ability to induce therapeutic changes without significant biological temperature increase. To enable feasible therapeutic applications, small and light devices are needed. However, current commercially available LIUS devices are bulky and expensive. In this thesis, a battery-powered highly-integrated system is proposed to generate low-intensity therapeutic ultrasound for wearable applications.

As interfacing with ultrasound transducers generally requires a higher voltage than the battery supply voltage, one challenge of designing the battery-powered highly-integrated LIUS system is to design a DC-DC boost converter with a high output voltage while delivering sufficient output power, and meeting the small size constraint at the same time. Another important block of the LIUS system is the transducer driver. A half-bridge driver is utilized for the proposed LIUS system to drive the ultrasound transducer due to its compact design and the capability of high-speed switching. However, a high-voltage (HV) level shifter is needed for the high-side operation of the half-bridge transducer driver. The performance of the HV level shifter affects the speed, power consumption, and robustness of the half-bridge circuit. Therefore, the design of the high-performance HV level shifter presents another challenge.

The challenges have been effectively solved in this thesis. Charge pumps (also known as switched-capacitor DC-DC boost converters) with high current

drive capability and high power conversion efficiency are proposed to overcome the design challenge of the DC-DC boost converter. Undesired charge transfer, which has a direction opposite to that of the intended current flow, presents a significant source of power loss in charge pumps. The proposed charge pumps utilize charge transfer switches with a complementary branch scheme to significantly reduce undesired charge transfer, thereby improving power conversion efficiency and increasing current drive capability effectively. Additionally, an HV level shifter with short propagation delay and low power consumption is proposed in this thesis to enable the high-performance operation of the half-bridge transducer driver. The proposed HV level shifter achieves high-speed switching and low energy dissipation with the approach of pulse triggering. Additionally, fully symmetrical switching avoids signal skew. Compared with other HV level shifters implemented in the same process, the proposed circuit shows both shorter propagation delay and lower power consumption.

Based on the proposed charge pumps and half-bridge transducer driver, a proof-of-concept miniaturized LIUS device is designed and developed to generate low-intensity therapeutic ultrasound for wearable applications. The miniaturized LIUS device consists of a battery supply, a custom Application-Specific Integrated Circuit (ASIC), an off-chip digital control block, and a piezoelectric transducer. The ASIC, which integrates the proposed charge pump and transducer driver, is implemented in TSMC's 0.18-μm Bipolar-CMOS-DMOS Gen2 process. The digital control block is used to generate the control signals for the ASIC. The piezoelectric transducer is a customized transducer with a resonance frequency of 1.5 MHz. At this frequency, the proof-of-concept miniaturized LIUS device can generate continuous-wave ultrasound with a therapeutic power intensity of 32 mW/cm^2. Pulsed ultrasound can also be obtained at a lower power intensity. To further improve the miniaturized LIUS device, three improvements have been proposed in this thesis and a monolithic-chip solution

is obtained. An improved ASIC has been designed in AMS's 0.35-µm HVC-MOS process, and simulation results have verified its improved performance.

Compared to current commercially available LIUS devices, the proposed highly-integrated LIUS system is low-cost, compact, and light-weight, which enables affordable and wearable applications.

Preface

Parts of the work in Chapter 1 of this thesis have been published in X. Jiang, O. Savchenko, Y. Li, S. Qi, T. Yang, W. Zhang, and J. Chen, "A review of low-intensity pulsed ultrasound for therapeutic applications," IEEE Transactions on Biomedical Engineering, vol. 66, no. 10, pp. 2704–2718, 2019 (feature article for October 2019 issue). I was responsible for conducting the general research and investigation on low-intensity pulsed ultrasound (LIPUS) for therapeutic applications, its therapeutic mechanisms, and current commercially available LIPUS devices. I was also responsible for devising the outline, managing the project, composing parts of the manuscript, reviewing and editing the complete manuscript. O. Savchenko contributed to the detailed investigation of the therapeutic applications of LIPUS. O. Savchenko also contributed to composing the part of the manuscript of the LIPUS applications on bone healing enhancement and tissue engineering. Y. Li contributed to the detailed investigation of the therapeutic mechanisms of LIPUS and composed this part of the manuscript. Y. Li also contributed to the figure drawing of the manuscript. S. Qi contributed to the detailed investigation of the therapeutic applications of LIPUS for soft-tissue regeneration and inhibition of inflammation, and composed this part of the manuscript. T. Yang contributed to the detailed investigation on the therapeutic applications of LIPUS for non-invasive neuromodulation, and composed this part of the manuscript. W. Zhang contributed to the detailed investigation on LIPUS devices and composed this part of the manuscript. J. Chen devised the project, supervised the work, provided valuable insights, and contributed to reviewing and editing the manuscript.

Parts of the works in Chapter 2 of this thesis have been published as X.

Jiang, X. Yu, and J. Chen, "A low-voltage charge pump with improved pumping efficiency," in Proceedings of IEEE International Symposium on Circuits and Systems, 2017, pp. 1278–1281, and X. Jiang, X. Yu, K. Moez, D. G. Elliott, and J. Chen, "High-efficiency charge pumps for low-power on-chip applications," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 3, pp. 1143–1153, 2018. I was responsible for the circuit design, simulation, optimization, hardware prototyping, and manuscript composing. X. Yu provided guidance in the circuit design and hardware prototyping. K. Moez provided insights in the circuit design, contributed to reviewing and editing the manuscript. D. G. Elliott provided insights in the device reliability of the circuit, and provided advice in the figure presentation and the academic writing of the manuscript. J. Chen supervised the work, provided valuable guidance of the project, and contributed to reviewing and editing the manuscript.

Parts of the works in Chapter 1, 2, 3, and 4 of this thesis have been accepted by the IEEE Transactions on Biomedical Circuits and Systems as: X. Jiang, W. T. Ng, and J. Chen, "A miniaturized low-intensity ultrasound device for wearable medical therapeutic applications". I was responsible for the system and circuit design, simulation, optimization, hardware prototyping, testing, and manuscript composing. W. T. Ng provided insights in the system and circuit design, offered support in hardware prototyping, provided advice in IC packaging, PCB design, testing, and contributed to reviewing and editing the manuscript. J. Chen supervised the work, provided valuable guidance of the project, offered insights on the biomedical applications of the prototype, and contributed to reviewing and editing the manuscript.

Act in such a way that you treat humanity, whether in your own person or in the person of any other, never merely as a means to an end, but always at the same time as an end.

– Immanuel Kant

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I would like to express my appreciation to my supervisor Dr. Jie Chen for providing me the valuable opportunity to pursue the Doctor of Philosophy degree at the University of Alberta, and perform this project in his research group. Without his support, this thesis would not have been possible.

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I would like to thank my fellow research-mates at the Binary Lab, University of Alberta: Xiaojian Yu for his guidance in charge pump design and layout; Oleksandra Savchenko, Yufeng Li, Shiang Qi, Tianlin Yang, and Wei Zhang for their contributions and collaborations to a review paper; Xuanjie Ye for his help in the tapeout in AMS's 0.35 µm HVCMOS process. I am also very grateful to Yahui Leng, Weijia Zhang, and Jingshu Yu at the Smart Power Integration & Semiconductor Devices Research Group, University of Toronto, for their help in hardware prototyping and testing.

Finally, I would like to thank my parents and friends for their unfailing support and continuous encouragement throughout my years of study, and my life in general.

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List of Acronyms

ASIC Application-Specific Integrated Circuit

BCD Bipolar-CMOS-DMOS

BVD Butterworth-Van Dyke

CMUT Capacitive Micromachined Ultrasonic Transducer

CTS Charge Transfer Switch

EPT Energy Consumption per Transition

FDA Food and Drug Administration

FPGA Field-Programmable Gate Array

HS High-Side

HV High-Voltage

LIPUS Low-Intensity Pulsed Ultrasound

LIUS Low-Intensity Ultrasound

LS Low-Side

LV Low-Voltage

MIM Metal-Insulator-Metal

NICE National Institute for Health and Care Excellence

PCB Printed Circuit Board

PD Propagation Delay

PZT Lead Zirconate Titanate

SATA Spatial Average Temporal Average

SPTA Spatial Peak Temporal Average

VCO Voltage-Controlled Oscillator

Chapter 1

Introduction

1.1 Low-intensity ultrasound (LIUS) and its therapeutic effects

Ultrasound is a form of acoustic energy at frequencies above the limit of human audibility (greater than 20 kHz) [1], [2]. The use of ultrasound for medical applications, including diagnostics, surgery, and therapy, has been investigated for decades [3]. As early as the late 1920s, ultrasound therapy began to be explored by Wood and Loomis [4]. Early therapeutic applications focused on the thermal effects of high-intensity ultrasound to selectively raise the temperature of particular tissues [5], [6]. Recently, low-intensity ultrasound (LIUS) has drawn increasing attention due to its non-thermal effects [7]. The non-thermal effects of LIUS are attributed primarily to a combination of cavitation, acoustic streaming, and mechanical stimulation, which are able to induce therapeutic changes without significant biological temperature increase [8].

The LIUS waveform pattern is in accordance with the generalized ultrasound waveform pattern shown in Figure 1.1. Important parameters of LIUS include its frequency, pulse duration, pulse repetition period, and duty ratio (defined as the pulse duration divided by the pulse repetition period). Ultrasound power intensity, which is defined as the acoustic power divided by the transducer radiating surface area, is another important parameter.

Many researchers have explored the therapeutic effects of LIUS with different parameters. For example, continuous-wave (a duty ratio of 100%) LIUS at a frequency of 1 MHz and intensities of 30 mW/cm^2, 70 mW/cm^2, and 100

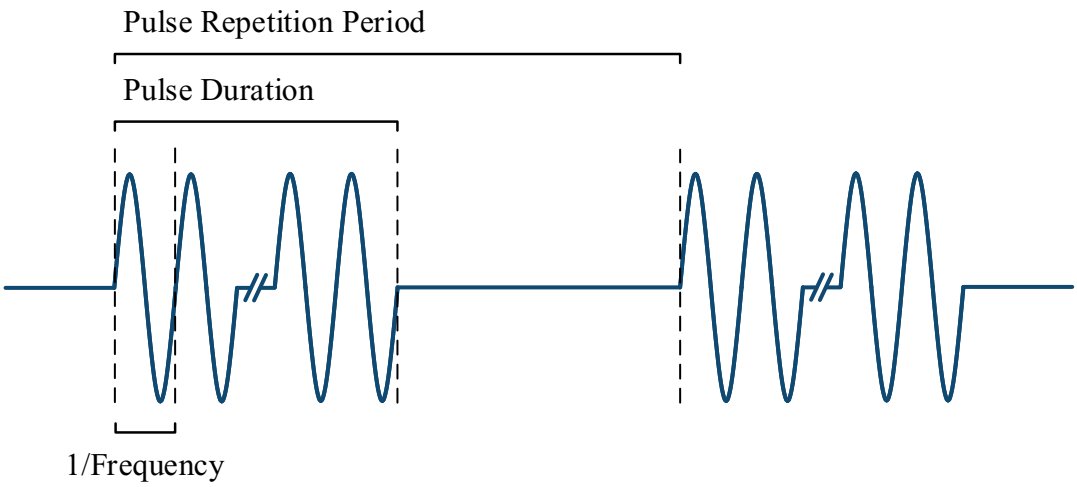
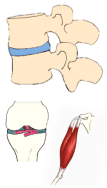


Figure 1.1: Generalized ultrasound waveform pattern (modified from [9]).

mW/cm^2 have been investigated to show an inhibitory effect on gramicidin D-induced red blood cell edema [10]. At a frequency of 45 kHz, a significant increase in nitric oxide was achieved at three intensities, 5 mW/cm^2, 30 mW/cm^2, and 50 mW/cm^2, when applying continuous-wave LIUS to human mandibular osteoblasts [11]. Continuous-wave LIUS at the same frequency has also been shown to have efficacy in healing osteoradionecrosis [12] and bone regeneration enhancement [13].

Pulsed LIUS, i.e., low-intensity pulsed ultrasound (LIPUS) has also been demonstrated to provide a non-invasive therapeutic modality with its therapeutic applications studied both *in vitro* and *in vivo*. Results have shown positive effects of LIPUS and its potential for broad applications including the areas of bone healing promotion, acceleration of soft-tissue regeneration, inhibition of inflammatory responses, and neuromodulation, etc. Table 1.1 summarizes the current status of LIPUS for different therapeutic applications. The acronym FDA in Table 1.1 denotes Food and Drug Administration. NICE represents National Institute for Health and Care Excellence. SATA denotes spatial average temporal average, and SPTA represents spatial peak temporal average.

Table 1.1: Current status of LIPUS for different therapeutic applications.

Application	**Target**	**LIPUS Parameters**	**Results**	**Current Status**
Bone healing 	Fresh Fracture [14]–[16]	Typically at 1.5 MHz; 30 mW/cm^2 SATA; 20 % duty cycle at 1 kHz	Reducing fracture healing time and providing clinical benefits, particularly in the circumstances of delayed healing and nonunion	U.S. FDA approved in 1994 and U.K. NICE supported in 2010
	Delayed union [17]			U.K. NICE supported in 2010
	Nonunion [18]			U.S. FDA approved in 2000 and U.K. NICE supported in 2010
Soft-tissue regeneration 	Tendon [19]	<3 MHz; <1 W/cm^2 no defined application protocol is universally accepted or used, and appropriate dosing of LIPUS treatments needs to be established and validated for achieving optimal results	Promoting tendon healing, ligament healing, intervertebral discs resorption, and cartilage recovery	Pre-clinical studies both *in vitro* and *in vivo* (animal models for all applications while human models have been conducted for cartilage)
	Ligaments [20]			
	Intervertebral discs [21]			
	Cartilage [22]			

Inflammation inhibition [23]–[25] 	Beneficial effects were shown with the same parameters used in the clinical treatment of bone fracture. LIPUS with other parameters were also investigated	Preventing periprosthetic inflammatory loosening, inhibiting lipopolysaccharide –induced inflammatory responses of osteoblasts and decreasing pro-inflammatory cytokines etc.	Pre-clinical studies both *in vitro* and *in vivo* (animal model)
Neuromodulation [26], [27] 	Effectiveness was shown with the parameters of 1 MHz; 528 mW/cm^2 SPTA; 5% duty cycle at 1 Hz. LIPUS with other parameters were also investigated	Treating traumatic brain injury, vascular dementia and Alzheimer's disease etc.	Pre-clinical studies both *in vitro* and *in vivo* (animal model)
Dental treatment [28]–[31] 	Beneficial effects were shown with the same parameters used in the clinical treatment of bone fracture	Promoting periodontal ligaments regeneration, restoring damaged dental roots and decreasing root resorption etc.	Aveo System, a LIPUS device for accelerating orthodontic treatment, was approved by Health Canada in 2016

LIPUS stimulation at a frequency of 1.5 MHz, a pulse duration of 200 µs, a duty ratio of 20%, and an intensity of 30 mW/cm^2 SATA is an established, widely used, and FDA approved intervention for accelerating bone healing in fresh fractures and nonunion [32]. However, more currently, researchers in [33] showed that various intensities (2 mW/cm^2, 15 mW/cm^2, and 30 mW/cm^2) of LIPUS were able to initiate osteogenic differentiation, while the highest increase of mineralization was with 2 mW/cm^2. The study in [34] showed that LIPUS with an intensity of 10 mW/cm^2, which is also below the current clinical standard, was able to improve mineralization in bone cell cultures. Similarly, the results in [21] demonstrated positive effects on DNA synthesis and content using LIPUS with intensities of 7.5 mW/cm^2 and 15 mW/cm^2. Other researchers have also shown positive effects of LIPUS with intensities lower than the current clinical standard [35], [36], suggesting that investigation on redefining the most effective LIPUS intensity for clinical use is needed.

Applications of ultrasound for medical therapeutic purposes have been an accepted and beneficial use of ultrasonic biological effects for years [37]. Though requiring further exploration with its doses, LIUS, both in continuous-wave and pulsed-wave form, provide a promising therapeutic tool for various medical applications [7]. To bring the benefits of LIUS to various therapeutic applications, and to facilitate research *in vitro* and *in vivo*, clinical trials, and home-based rehabilitation interventions, developing medical devices to generate LIUS is in high demand.

1.2 Proposed highly-integrated LIUS system for wearable therapeutic applications and its design challenges

To enable feasible therapeutic applications of LIUS, small and light-weight devices are needed. However, current commercially available therapeutic LIUS devices are bulky and expensive, such as the device described in [38]. These devices are generally built with discrete components mounted on printed circuit boards (PCBs). With advances in CMOS technology (including both

the standard low-voltage (LV) CMOS technology and the high-voltage (HV) CMOS technology), it is desirable to reduce manufacturing costs and include flexibility in operation with a highly-integrated solution to enable affordable and wearable applications.

1.2.1 Proposed highly-integrated LIUS system

To implement wearable therapeutic applications, a battery-powered highly-integrated system is proposed in this thesis to generate LIUS at therapeutic intensities. Figure 1.2 shows the block diagram of the proposed system. As shown, the system consists of five blocks: a battery supply, a digital control block, a DC-DC boost converter, a transducer driver, and an ultrasound transducer. The digital control block is used to generate control signals for the system. The DC-DC boost converter is used to generate the high voltage required by the system from a battery supply voltage. The transducer driver is used to generate high-energy HV pulses with the control signals of the digital control block and the power supply of the DC-DC boost converter. Finally, the ultrasound transducer converts the electrical pulses to ultrasound waves.

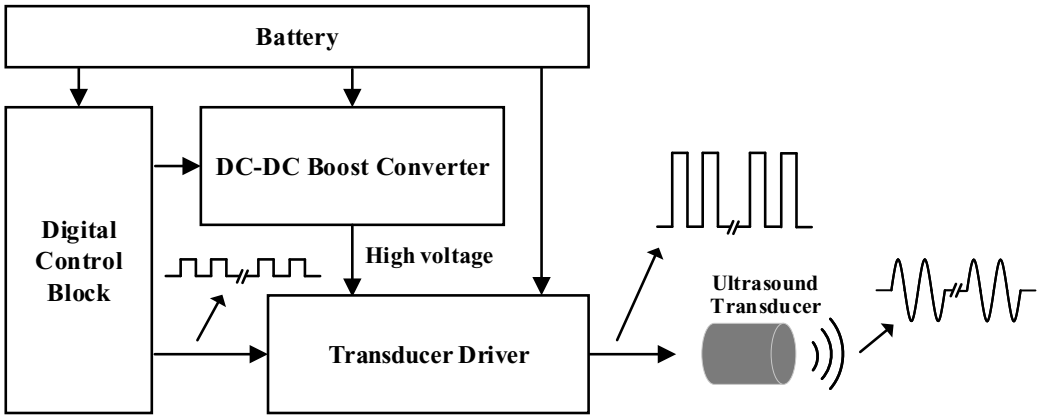


Figure 1.2: System block diagram of the proposed highly-integrated LIUS system.

1.2.2 Design challenges

To miniaturize the system for wearable applications, several challenges exist in developing the battery-powered highly-integrated LIUS system in Figure 1.2:

DC-DC boost converter

As interfacing with ultrasound transducers generally requires a higher voltage than the battery supply voltage [39], a DC-DC boost converter is needed to generate a sufficiently high voltage for the battery-powered system shown in Figure 1.2. However, it is challenging to develop a DC-DC boost converter with a high output voltage while delivering sufficient output power, and meeting the small size constraint at the same time. To achieve the ultrasound power intensity of the therapeutic LIUS (mostly between 10 mW/cm^2 and 100 mW/cm^2), the power delivered by the DC-DC boost converter needs to be up to 100 mW, depending on the transducer radiating surface area and the transducer transfer efficiency (from the electrical power to the acoustic power). For this power requirement, traditional inductor-based boost converters have been widely used [40]. However, the inductor-based solution requires a bulky off-chip inductor which makes it difficult to meet the size constraint of miniaturized LIUS devices.

Charge pumps, also known as switched-capacitor DC-DC boost converters, provide an alternative solution to generate high voltages. Compared to inductor-based boost converters, charge pumps require only capacitors as passives, which offer significantly higher energy densities [40]. Another advantage of the charge pump is that it occupies considerably smaller board area than inductor-based solutions, either fully-integrated with on-chip capacitors or highly-integrated with a limited number of off-chip capacitors. However, the use of charge pumps has traditionally been limited to applications requiring an average power of less than 10 mW [41], the power level of which is not sufficient for therapeutic LIUS applications.

Transducer driver

The transducer driver is used to generate high-energy HV pulses for ultrasound transducer excitation, with the control signals of the digital control block and the power supply of the DC-DC boost converter. To drive the ultrasound transducer with low power dissipation, the transformer push-pull topology

(Figure 1.3) has been widely used [42]. However, there are two drawbacks regarding this topology. First, transformers generally have limited bandwidth [43]. As discussed in Section 1.1, different therapeutic LIUS applications require different ultrasound frequencies ranging from tens of kHz to several MHz, the bandwidth of which is not easily achieved by transformers. Second, transformers are generally bulky components that will increase the board area and the weight of the LIUS device, which are not feasible for wearable applications.

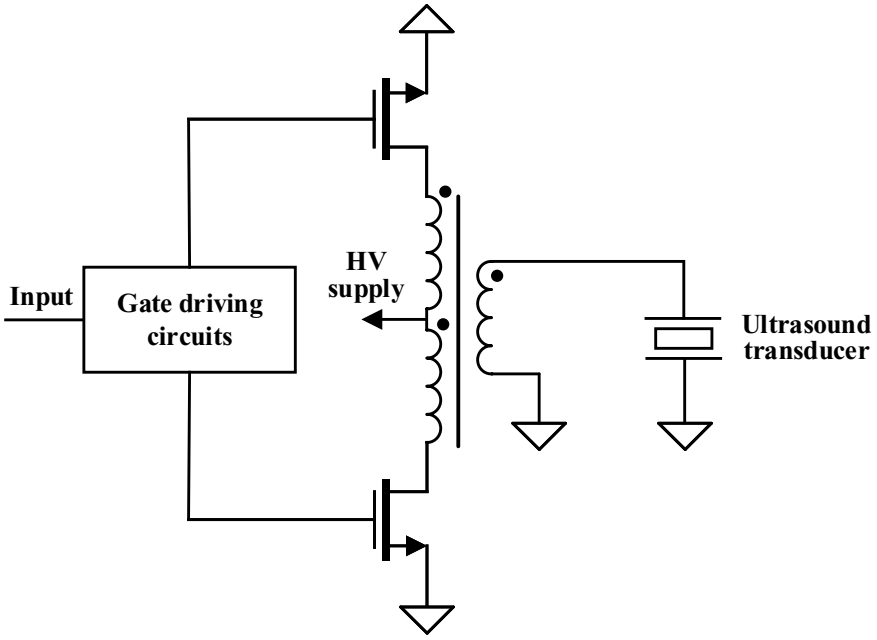


Figure 1.3: Transformer push-pull transducer driver (modified from [42]).

An alternative solution for transducer driving is the half-bridge architecture. Figure 1.4 shows the half-bridge transducer driver with one positive power supply and two n-type switches at the output stage: Q1 is the high-side (HS) switch, and Q2 is the low-side (LS) switch. The advantage of the half-bridge driver is that it has wide bandwidth, capable of both low-frequency operation and high-speed switching [44]. This makes it suitable for various therapeutic applications with different ultrasound frequency requirements. Moreover, the half-bridge circuit can be easily integrated on chip, making it desirable for wearable devices. However, the design of the gate driving circuits for the output switches in Figure 1.4 is of great complexity [44], [45]. This is because a floating gate driving circuit is needed for the HS switch, which

operates in a floating domain with respect to the switching node [45]. In the floating HS gate driving circuit, an HV level shifter is required to elevate the control signals from the LV domain to the floating HV domain, the design of which affects the speed, power consumption, and robustness of the half-bridge circuit [46]. This makes the design of the half-bridge transducer driver complex and challenging.

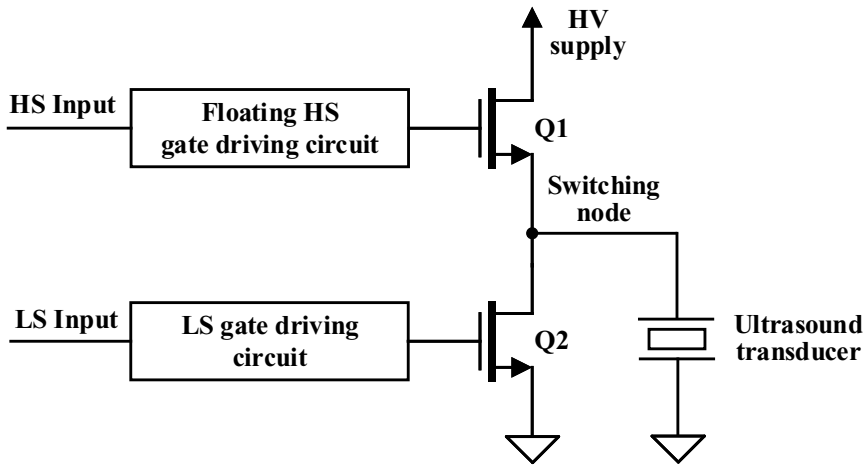


Figure 1.4: Half-bridge transducer driver with one positive power supply and two n-type switches at the output stage (modified from [44]).

The challenges described above have been effectively solved in this thesis:

- Charge pumps with high current drive capability and high power conversion efficiency are proposed to meet the power requirement as well as the size constraint of the wearable LIUS system. The charge pump could be either fully-integrated with on-chip capacitors or highly-integrated with a limited number of off-chip capacitors.

- A half-bridge circuit is used as the transducer driver for the proposed LIUS system due to its capability for wide-bandwidth operation and its feasibility to be integrated on chip. To achieve high-performance operation of the half-bridge transducer driver, an HV level shifter with short propagation delay and low power consumption is proposed in this thesis.

The rest of the thesis is organized as follows: Chapters 2 and 3 describe the proposed charge pumps and the transducer driver in detail, including a comprehensive investigation on current research status, detailed descriptions of the proposed designs (including operation principles, design considerations, simulation and measurement results), and the comparison of the proposed designs with previously reported works. Based on the proposed charge pumps and the transducer driver, a proof-of-concept miniaturized LIUS device is developed and tested in Chapter 4. Several improvements are also made based on the miniaturized LIUS device. Finally, conclusions and insights on further works are drawn in Chapter 5.

Chapter 2

Charge Pumps with High Current Drive Capability

2.1 Introduction

Charge pumps, also known as switched-capacitor DC-DC boost converters, have been extensively used in applications requiring output voltages higher than the supply voltage, such as writing or erasing the floating-gate devices of nonvolatile memories [47], [48], actuating radio-frequency micro-electro-mechanical systems [49], driving LCDs [50], and more recently radio frequency energy harvesters [51], [52], among many others [53]. For these applications, charge pumps can produce different DC output voltages by transferring electric charge in capacitor networks using switches controlled by clock phases [54]. Compared with traditional inductor-based or transformer-based converters, charge pumps benefit from the significantly higher energy density of capacitors [40], [55].

Conventional fully-integrated charge pumps have limited current drive capability (generally < 400 µA) [48], [56], [57]. However, for the application of the proposed LIUS system, high current drive capability is required to generate ultrasound at therapeutic intensities. In order to improve the current drive capability of the charge pump, the power conversion efficiency needs to be maximized.

In general, the power conversion efficiency (η) of a charge pump can be expressed as [58]

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \times 100\% \tag{2.1}$$

where P_{out} is the output load power and P_{loss} represents the power loss of the charge pump. To maximize the power conversion efficiency, P_{loss} needs to be minimized.

Typically, the power losses of a charge pump can be classified as redistribution loss, conduction loss, switching loss, and reversion loss [58]. The redistribution loss is caused by the inherent energy loss when a capacitor is charged or discharged by a voltage source or another capacitor [59] (the energy is lost in the resistive elements of the circuit, for instance, the equivalent series resistance of the capacitors). The conduction loss, which is caused by the non-zero on-resistance of switches, also plays an important role in power dissipation [58]. Figure 2.1 demonstrates the conduction loss of a MOSFET. The switching loss, which occurs due to the non-instantaneous transitions of the drain-source voltage and current, is present at each turn-on/off of the switch [60] (Figure 2.1).

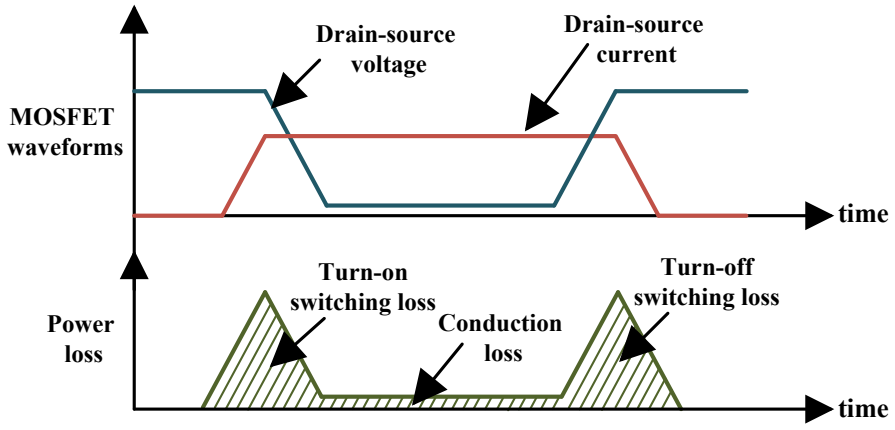


Figure 2.1: Power loss of a MOSFET (modified from [60]).

Another significant source of power loss in a charge pump is undesired charge transfer [61] (also known as reversion loss [58]). It is usually caused by the reverse charge transmitted in the direction opposite to that of the original current flow [61]. Among these power losses, the power loss caused by undesired charge transfer depends heavily on the topology of the charge

pump. Designing new charge pumps with reduced undesired charge transfer can effectively decrease the power loss and leads to higher power conversion efficiency, voltage pumping gain, and current drive capability.

This chapter proposes new charge pumps with improved power conversion efficiency as well as voltage pumping gain and current drive capability by reducing undesired charge transfer. Charge transfer switches controlled by auxiliary transistors are utilized in a complementary branch configuration. Undesired charge transfer caused by the simultaneous conduction of auxiliary transistors and delayed turning off of charge transfer switches are both eliminated or reduced, leading to higher power conversion efficiency, enhanced current drive capability, and improved voltage pumping gain. The proposed charge pumps are suited for highly-integrated applications such as battery-powered systems, where power conversion efficiency is of essential importance and where current drive capability of several to tens of milli-amperes is required.

2.2 Current research status

One of the most well-known charge pumps is the Dickson charge pump [62]. The n-stage NMOS-based Dickson charge pump circuit is shown in Figure 2.2. The NMOS transistors in this circuit function as diodes, so that charge can only be pushed in the source-to-load direction [63].

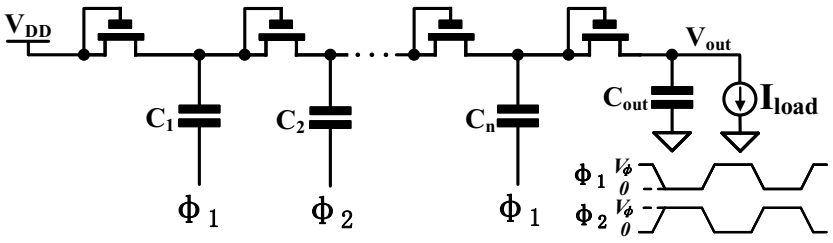


Figure 2.2: N-stage NMOS-based Dickson charge pump circuit [62].

The Dickson charge pump employs a simple two-phase clocking scheme comprising of two clock phases Φ_1 and Φ_2, which are out-of-phase and have a voltage of V_ϕ (generally equal in swing to the supply voltage, i.e., V_{DD}). The voltage gained at the ith stage can be expressed by [58]

$$V_i - V_{i-1} = \frac{CV_\phi}{C + C_s} - V_{TN}[V_{SB}(i)] \tag{2.2}$$

where i is an integer larger than 1 and smaller than $n+1$. C is the capacitance of the pumping capacitors ($\mathrm{C_1} \sim \mathrm{C_n}$) and C_s is the parasitic capacitance present at each pumping node. $V_{TN}[V_{SB}(i)]$ is the threshold voltage of the NMOS transistors at the ith stage, which depends on the ith stage source-to-body voltage $V_{SB}(i)$. We can see from equation (2.2) that the Dickson charge pump suffers from the threshold voltage drop across the drain-source terminal at each stage. Moreover, as the source-to-body voltage increases, due to the body effect, the threshold voltage increases accordingly resulting in higher voltage drops at later pumping stages.

In order to eliminate the effects of threshold voltage drop, charge pumps with complicated clocking schemes have been developed, for instance, charge pumps with bootstrap gate control strategies [56], [64]–[66]. Similarly, complex clocking schemes have been used to improve the power conversion efficiency, for example, a nonoverlapped rotational time-interleaving scheme was applied in [67], while [68] utilized a four-phase non-overlapping clock, and [69] applied phase-shifted clocks. However, complex clocking schemes require additional clock generators, which consume power and increase the circuit complexity.

One effective technique with a simple two-phase clocking scheme is to utilize the charge transfer switches (CTSs), which can be turned on or off completely, without incurring a threshold voltage drop [63], [70]–[73]. Researchers in [63] first devised the CTS charge pump topology. The study in [71] modified it with PMOS transistors as CTSs in order to eliminate the body effect. The work in [72] discussed the gate control strategies for the first and last stages. Figure 2.3 shows the n-stage CTS charge pump topology presented in [71]. PMOS transistors M1∼Mout, referred to as CTSs in this topology, are used to direct charge flow to the output. Floating well structures are used to eliminate the body effect of the PMOS CTSs. Each of the CTSs is controlled by a CMOS inverter (for example, MN3 and MP3 controlling the gate of M3). The idea is to use the lower voltages from the previous stages to effectively turn on PMOS

CTSs, enabling the pumping voltage at each stage to be free of the threshold voltage drop.

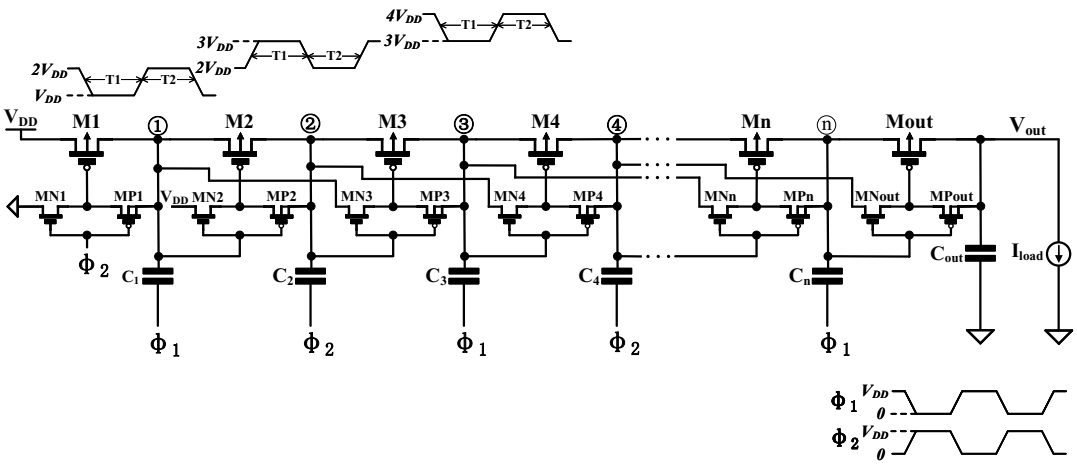


Figure 2.3: N-stage CTS charge pump circuit proposed in [71].

However, a shortcoming with this topology is that it suffers from undesired charge transfer during clock transitions, which has a direction opposite to that of the original current flow. An example of the switching waveforms at the third stage is demonstrated in Figure 2.4. As depicted in Figure 2.4(a), during the transition when clock Φ_1 decreases from V_{DD} to 0 and Φ_2 increases from 0 to V_{DD}, the voltage change at node 1 (V_1) is from $2V_{DD}$ to V_{DD}, V_2 is from $2V_{DD}$ to $3V_{DD}$ and V_3 is from $4V_{DD}$ to $3V_{DD}$. During this transition, transistor MP3 won't be turned off until V_2 reaches $V_3 - |V_{TP}|$, whereas MN3 already starts to be turned on as soon as V_2 reaches $V_1 + V_{TN}$. This causes MN3 and MP3 to be turned on simultaneously during the short time period T, as indicated in Figure 2.4. As voltage V_3 is larger than V_1 during this period, reverse charge occurs from node 3 back to node 1 through MN3 and MP3.

The energy loss caused by the undesired reverse charge transfer is referred to as reversion energy loss. The reversion energy loss E_{rev} during this clock transition can be expressed by the energy loss caused by simultaneous conduction E_{sc} as

$$E_{rev} = E_{sc}, \Phi_1 : V_{DD} \Rightarrow 0 \ \Phi_2 : 0 \Rightarrow V_{DD} \tag{2.3}$$

Similarly, during the other transition when clock Φ_1 rises from 0 to V_{DD} and

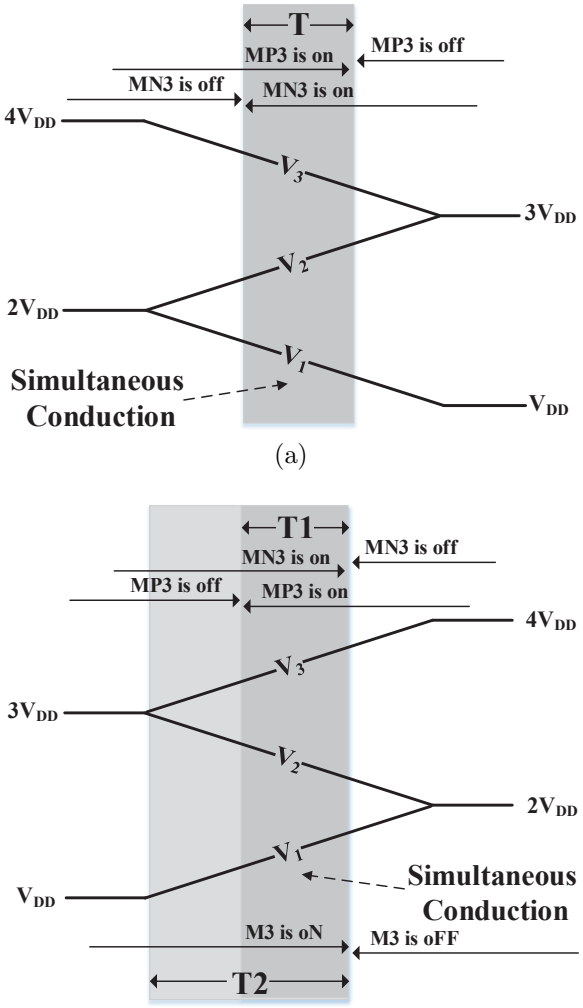


Figure 2.4: Switching waveforms of the CTS charge pump circuit shown in Figure 2.3 during (a) Φ_1: $V_{DD} \Rightarrow 0$ Φ_2: $0 \Rightarrow V_{DD}$, and (b) Φ_1: $0 \Rightarrow V_{DD}$ Φ_2: $V_{DD} \Rightarrow 0$.

Φ_2 drops from V_{DD} to 0, lossy discharge caused by the simultaneous conduction of MN3 and MP3 can also be found, as indicated by the short time period T1 in Figure 2.4(b). Another problem manifesting during the second transition is that, since the gate-drive signal of the CTS M3 is controlled by MN3 and MP3, M3 won't be turned off until MN3 is turned off disconnecting the gate terminal of M3 from node 1. Since voltage V_3 is larger than V_2 during this transition, the delayed turning off of M3 also causes reverse current flow, which transfers from node 3 back to node 2 through M3, as indicated by the time period T2 in Figure 2.4(b). As a result, there are two reverse charge paths

during the second clock transition and this reversion energy loss E_{rev} can be expressed by

$$E_{rev} = E_{sc} + E_{dt}, \Phi_1 : 0 \Rightarrow V_{DD}\ \Phi_2 : V_{DD} \Rightarrow 0 \tag{2.4}$$

where E_{sc} is the energy loss caused by the simultaneous conduction of the auxiliary transistors and E_{dt} is caused by the delayed turning-off of the CTS. Combining equations (2.3) and (2.4) together and assuming that the clock frequency is f_{ck}, the reversion power loss P_{rev} of the circuit depicted in Figure 2.3 can be described as

$$P_{rev} = f_{ck}(2E_{sc} + E_{dt}) \tag{2.5}$$

We can see from equation (2.5) that with the same clock frequency, the reversion power loss depends on the energy loss caused by both the simultaneous conduction of the auxiliary transistors and the delayed turning-off of the CTSs. To improve the power conversion efficiency, these two energy losses need to be eliminated or reduced.

Another charge pump utilizing a simple two-phase clocking scheme based on a cross-coupled configuration has been proposed by Pelliconi in [74] and described in [75]. A new control strategy was proposed in [76] to turn transistors in [75] on more effectively by driving NMOS transistors with $3V_{DD}$ using backward control and body biasing PMOS transistors. Figure 2.5 shows the n-stage Pelliconi cross-coupled charge pump circuit. As shown, this circuit consists of two cross-coupled branches where the gate-drive signals of these two branches are intertwined. As an example of the operating mechanism, in the phase that Φ_1 is low and Φ_2 is high, transistors MPA2 and MNA3 are turned on with their gates tied to V_{B2} and V_{B3} respectively. This pushes charge transferring from node A2 to node A3 through MPA2 and MNA3 without suffering from threshold voltage drop across either transistor. Similarly, in the opposite phase when Φ_1 is high and Φ_2 is low, MPA2 and MNA3 are turned off, preventing reverse charge transmitted from node A3 back to node A2.

However, since this technique applies a CMOS pair as pumping switches at

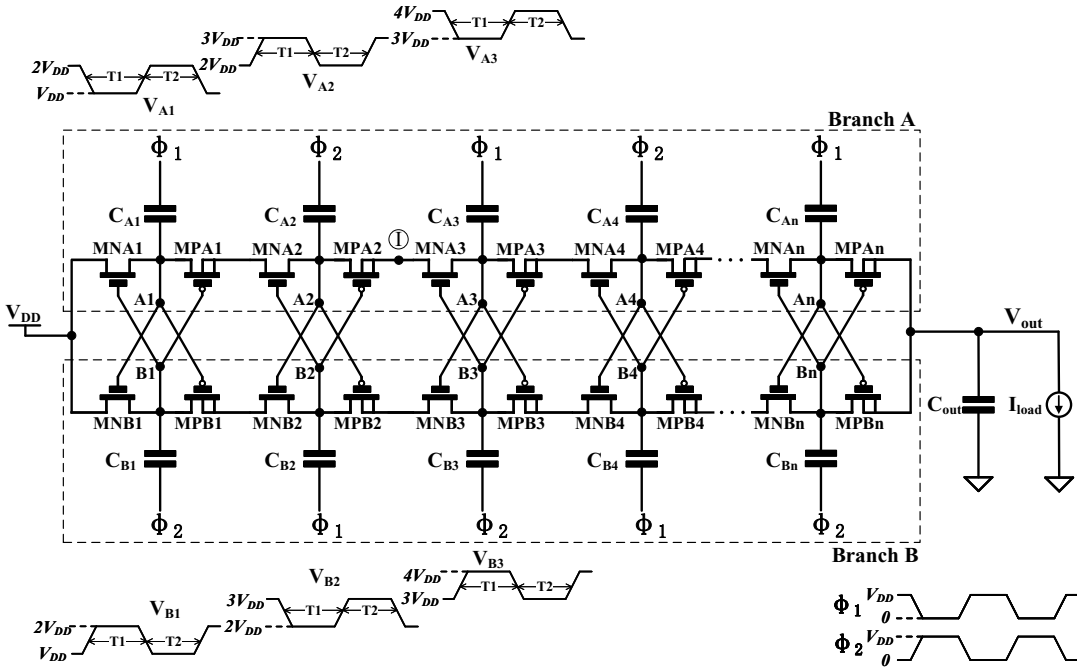


Figure 2.5: N-stage Pelliconi cross-coupled charge pump circuit proposed in [74] and described in [75].

each stage per branch, compared to charge pumps utilizing one pumping switch per stage per branch, the conduction loss caused by the switch on-resistance of the cross-coupled charge pump is much higher. As the transistors are operated in the linear region when turned on, the on-state switch resistance R_{on} can be given by [77]

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \tag{2.6}$$

where μ is the mobility of the electrons or holes, C_{ox} is the gate-oxide capacitance per unit area, and W and L are the width and length of the transistor, respectively. V_{GS} is the gate-to-source voltage and V_{TH} is the threshold voltage. We can see from equation (2.6) that, since μ, C_{ox} and V_{TH} are technology and device constants, with the same switch size parameters, R_{on} increases as V_{GS} decreases. This implies that when driving a high load current, V_{GS} decreases causing the increasing of the switch on-resistance, which leads to higher conduction loss.

Besides, undesired charge transfer also exists in this circuit during clock

transitions. Figure 2.6 shows the switching waveforms associated with the third stage operation of the cross-coupled charge pump circuit.

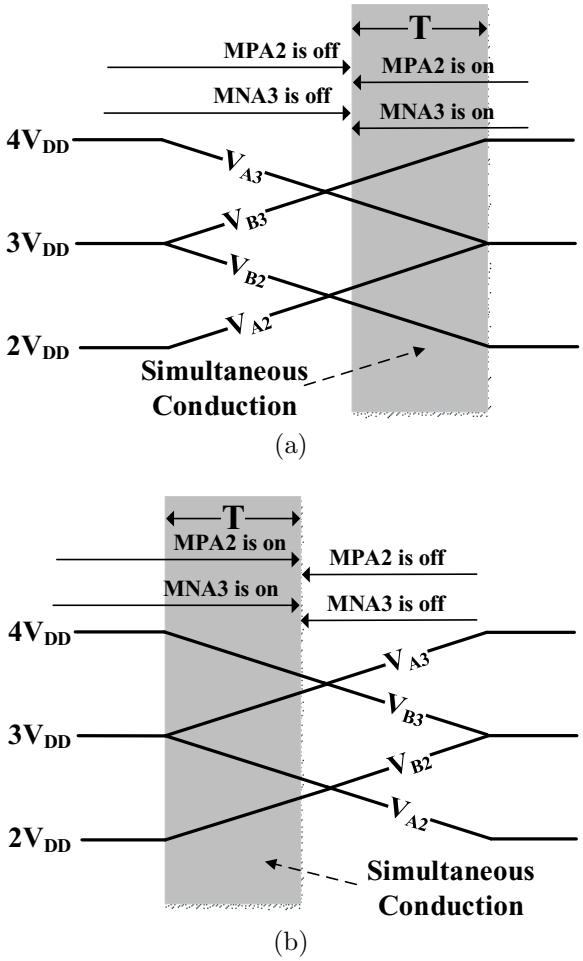


Figure 2.6: Switching waveforms of the cross-coupled charge pump circuit shown in Figure 2.5 during (a) Φ_1: $V_{DD} \Rightarrow 0$ Φ_2: $0 \Rightarrow V_{DD}$, and (b) Φ_1: $0 \Rightarrow V_{DD}$ Φ_2: $V_{DD} \Rightarrow 0$.

As illustrated in Figure 2.6(a), during the transition when clock Φ_1 goes down from V_{DD} to 0 and Φ_2 goes up from 0 to V_{DD}, the voltage at node B2 (V_{B2}) decreases from $3V_{DD}$ to $2V_{DD}$ and the voltage at node B3 (V_{B3}) increases from $3V_{DD}$ to $4V_{DD}$. Referring to the intermediate node between MPA2 and MNA3 as node I, as indicated in Figure 2.5, the voltage at node I (V_I) remains approximately $3V_{DD}$ during the operation. Therefore, MPA2 starts to be turned on after V_{B2} falls lower than $V_I - |V_{TP}|$. At this moment, MNA3 starts to be turned on as V_{B3} reaches $V_I + V_{TN}$ (assuming $V_{TN} = |V_{TP}|$).

Consequently, during the short period time T when V_{A3} is still larger than V_{A2}, undesired charge is generated, transferring from node A3 back to node A2 through MPA2 and MNA3. Similarly, during the other clock transition when clock Φ_1 increases from 0 to V_{DD} and Φ_2 decreases from V_{DD} to 0, the circuit also suffers from undesired charge transfer due to the simultaneous conduction of MPA2 and MNA3, as depicted in Figure 2.6(b).

We can see from the analysis above that, except for conduction power loss, undesired charge transfer exhibits another significant power loss in previously reported charge pumps. The undesired charge transfer phenomenon inherent in the charge pump circuits, shown in Figure 2.3 and Figure 2.5, manifests as a significant source of power consumption, which results in the degradation of power conversion efficiency as well as voltage pumping gain. It is thus desirable to develop effective techniques capable of reducing undesired charge transfer, while also keeping the conduction power loss at a low level.

2.3 Proposed charge pump circuits

We propose a new charge pump that improves the power conversion efficiency, voltage pumping gain, and current drive capability by reducing undesired charge transfer. A complementary branch scheme is applied based on the CTS charge pump topology. Undesired charge transfer caused by the simultaneous conduction of auxiliary transistors is eliminated with their gate control signals generated in both complementary branches. The n-stage proposed charge pump circuit is shown in Figure 2.7.

As we can see from Figure 2.7, this charge pump circuit consists of two complementary branches. These two branches are identical circuits with complementary clocks and are connected in parallel between the supply voltage and the output. PMOS transistors are used as CTSs except for the first stage. The use of PMOS transistors has the advantage that the body effect can be easily eliminated by connecting the body terminal of a PMOS transistor to its most positive voltage. Since only one transistor is used as the pumping switch at each stage per branch, compared to the pumping switch pair in the

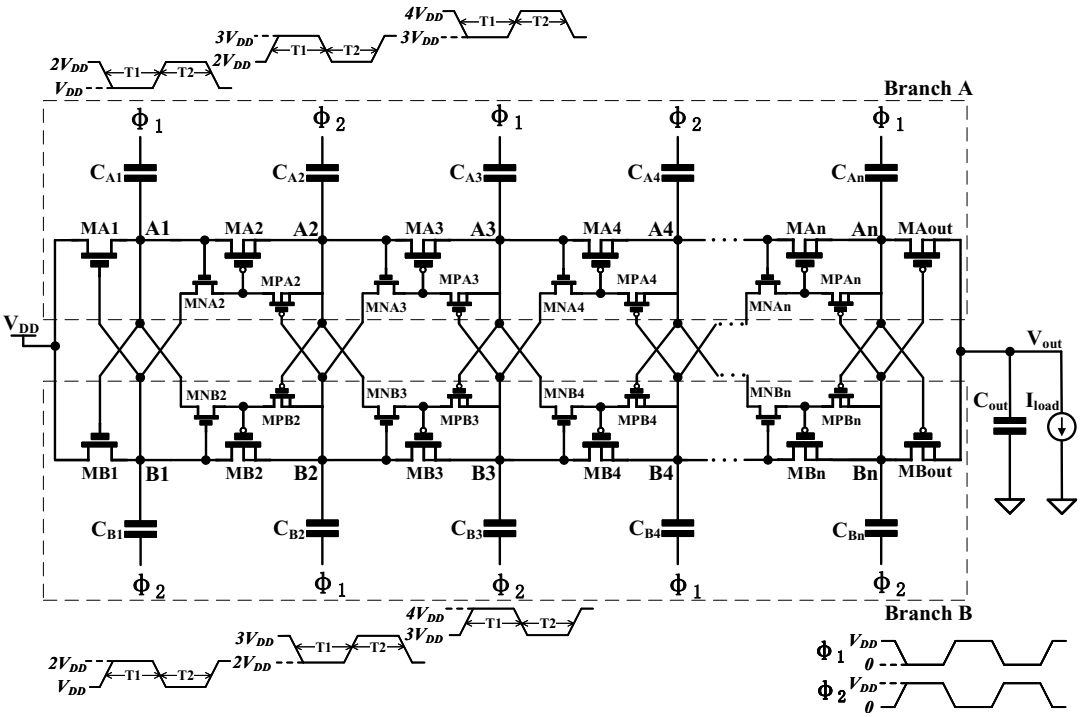


Figure 2.7: N-stage proposed complementary charge pump circuit (CP-1) based on CTSs.

cross-coupled charge pump (Figure 2.5), the proposed charge pump is able to keep the conduction loss at a low level, leading to increased power conversion efficiency and enhanced current drive capability. A simple two-phase clocking scheme is applied, i.e., the clock signals Φ_1 and Φ_2 are out-of-phase and both have a voltage swing identical to V_{DD}. The gate drive signal for each transistor is internally generated by both Branch A and Branch B. The detailed operation of the proposed charge pump circuit shown in Figure 2.7, which we refer to as CP-1, is explained below.

2.3.1 Operation principle

First stage

The first stage in CP-1 can be simplified from the CTS topology in Figure 2.3. As shown in Figure 2.7, only one NMOS transistor is used for each branch. For the transistor MA1, during the time interval T1 when Φ_1 is low and Φ_2 is high, the voltage at node A1 (V_{A1}) is close to but less than V_{DD}, while V_{B1}, which is generated in Branch B, is about $2V_{DD}$. As a result, MA1 is

turned on effectively by a gate-source voltage of V_{DD} enabling charge to be pushed from the supply voltage to the capacitor C_{A1}. Instead of the threshold voltage drop of the NMOS-based Dickson charge pump shown in Figure 2.2, the voltage drop across MA1 is V_{DS}, which is much less than the threshold voltage. During the time interval T2, V_{A1} goes up to $2V_{DD}$ while V_{B1} drops to V_{DD}, turning off MA1 to cut off the path from node A1 back to the power supply.

On the other hand, transistor MB1 operates in an opposite and complementary way such that it is turned off during the time interval T1 to cut off the path from node B1 back to the power supply, and turned on during the time interval T2 enabling charge to be pushed from the supply voltage to the capacitor C_{B1}.

Middle stages

In contrast to an inverter used to control the CTS in Figure 2.3, the two auxiliary transistors at each stage in CP-1 have different control signals, which are generated internally by the complementary branches. Since the middle stages follow the same operating mechanism, we consider the third stage as an example. During the time interval T1, both V_{A2} and V_{A3} are about $3V_{DD}$ with V_{A2} slightly higher than V_{A3}. V_{B2} and V_{B3}, which are generated in Branch B, are approximately $2V_{DD}$ and $4V_{DD}$, respectively. As a result, the auxiliary transistor MNA3 is turned on with a gate-source voltage of V_{DD} and MPA3 is turned off by the source-to-gate voltage of $-V_{DD}$. The ON state of MNA3 leads to the gate terminal of the CTS MA3 connected to node B2 (V_{B2} is about $2V_{DD}$), which turns on MA3 with a gate drive voltage of V_{DD}, allowing charge to be pushed from the capacitor C_{A2} to the capacitor C_{A3}. During the time interval T2, the auxiliary transistor MPA3 is turned on while MNA3 is turned off. The CTS MA3 is turned off since its gate and source terminals are connected together through MPA3, cutting off the path from node A3 back to node A2.

On the other hand, Branch B operates in a complementary manner. Specifically, MB3 is turned off during the time interval T1, cutting off the path from

node B3 back to node B2, and is turned on during the time interval T2, allowing charge transfer from node B2 to node B3.

Output stage

The output stage of CP-1 features a similar operating principle to the first stage. Instead of NMOS transistors, one PMOS transistor is used for each branch. The CTS MAout is turned on and MBout is turned off in one phase, and MAout is turned off and MBout is turned on in the other phase. The ON state of MAout enables charge transfer from the capacitor C_{An} to the output capacitor C_{out}. Similarly, charge can be delivered from C_{Bn} to C_{out} when MBout is on.

2.3.2 Analysis of undesired charge transfer

We can observe from the operation described above that both the body effect and the threshold voltage drop problem are eliminated in CP-1. Most importantly, compared to the charge pump circuit shown in Figure 2.3, undesired charge transfer is reduced in this topology due to the separate gate signals for the auxiliary transistors. To illustrate this, Figure 2.8(a) depicts the changing of waveforms when Φ_1 drops from V_{DD} to 0 and Φ_2 rises from 0 to V_{DD}. As V_{A2} increases from $2V_{DD}$ to $3V_{DD}$ and V_{B2} decreases from $3V_{DD}$ to $2V_{DD}$, transistor MNA3 starts to be turned on after V_{A2} reaches $V_{B2} + V_{TN}$. Similarly, with V_{A3} dropping from $4V_{DD}$ to $3V_{DD}$ and V_{B3} rising from $3V_{DD}$ to $4V_{DD}$, transistor MPA3 starts to be turned off after V_{B3} reaches $V_{A3} - |V_{TP}|$. Since MNA3 and MPA3 won't be turned on simultaneously during this clock transition, no reverse current path exists through MNA3 and MPA3 and charge won't be transferred from node A3 back to node B2. Therefore, the reversion energy loss caused by the simultaneous conduction of the auxiliary transistors, i.e., E_{sc} in equation (2.3), is eliminated in CP-1.

A problem with CP-1 is that, even though the undesired charge transfer is eliminated during the clock transition depicted in Figure 2.8(a), lossy discharge still occurs during the second clock transition. As illustrated in Figure 2.8(b), during the transition when Φ_1 goes up from 0 to V_{DD} and Φ_2 goes down from

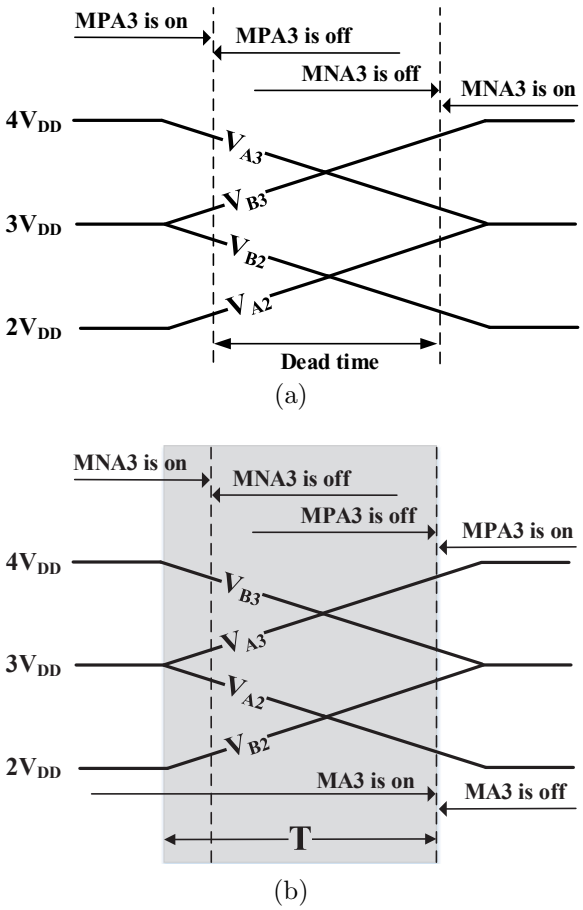


Figure 2.8: Switching waveforms of the proposed CP-1 circuit shown in Figure 2.7 during (a) Φ_1: $V_{DD} \Rightarrow 0$ Φ_2: $0 \Rightarrow V_{DD}$, and (b) Φ_1: $0 \Rightarrow V_{DD}$ Φ_2: $V_{DD} \Rightarrow 0$.

V_{DD} to 0, no reverse charge transfer occurs through the auxiliary transistors MNA3 and MPA3 since there is no simultaneous conduction of MNA3 and MPA3. However, reverse charge transfer still occurs with the CTS MA3. With its gate tied to MNA3 and MPA3, regardless of the OFF state of MNA3, MA3 won't be turned off until MPA3 is turned on to increase the gate voltage of MA3. As voltage V_{A3} is larger than V_{A2} during this transition, the delayed turning off of MA3 causes undesired charge transfer from node A3 back to node A2 through MA3, as indicated by the time period T in Figure 2.8(b). Consequently, the reversion energy loss during the second clock transition can be simplified from equation (2.4) such that only E_{dt} exists with E_{sc} eliminated:

$$E_{rev} = E_{dt}, \Phi_1 : 0 \Rightarrow V_{DD}\ \Phi_2 : V_{DD} \Rightarrow 0 \tag{2.7}$$

With the assumption of f_{ck} as the clock frequency. The reversion power loss P_{rev} of CP-1 can be described as

$$P_{rev} = f_{ck} E_{dt} \tag{2.8}$$

Comparing equations (2.5) and (2.8), we can conclude that the power loss caused by undesired charge transfer is significantly reduced in the proposed CP-1 circuit. However, it is desirable to reduce the delayed turning-off time of CTSs to reduce E_{dt} during each clock cycle in order to further improve the power conversion efficiency.

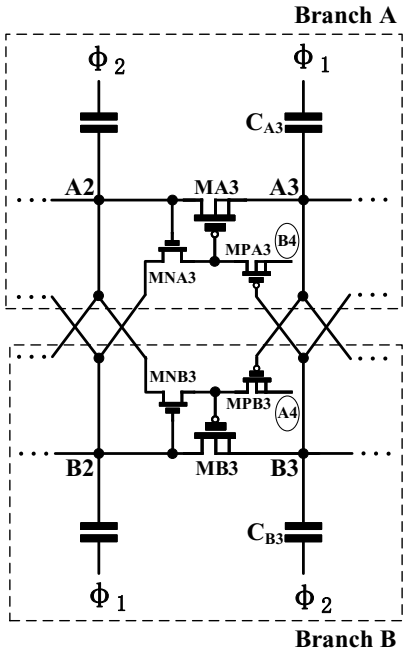


Figure 2.9: Optimized gate control scheme of the third stage for the proposed CP-2 circuit.

This delayed turning-off time of CTSs can be easily reduced with a simple modification of the gate control scheme. Taking the third stage in Branch A as an example (as shown in Figure 2.9), the source terminal of MPA3 is redirected to node B4 (as indicated by the ellipse in Figure 2.9) instead of being connected to node A3. The rationale is leveraging an already established high voltage at

node B4 to effectively turn on the auxiliary transistor MPA3 and then turn off the CTS MA3 in the second transition, shortening the lossy discharge time caused by the delayed turning off of MA3.

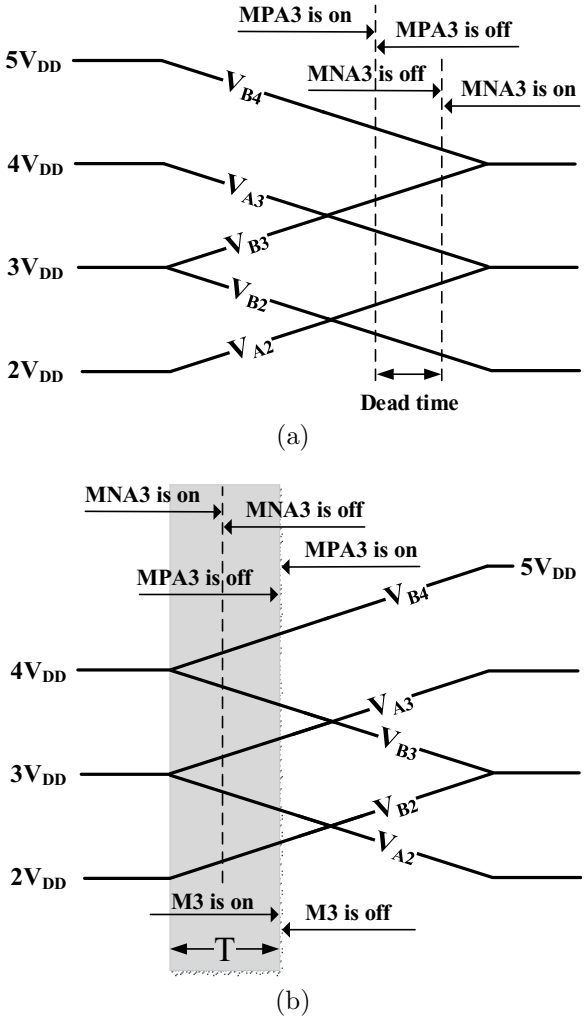


Figure 2.10: Switching waveforms of the proposed CP-2 circuit shown in Figure 2.7 during (a) Φ_1: $V_{DD} \Rightarrow 0$ Φ_2: $0 \Rightarrow V_{DD}$, and (b) Φ_1: $0 \Rightarrow V_{DD}$ Φ_2: $V_{DD} \Rightarrow 0$.

The merit of the optimized gate control strategy can be seen in Figure 2.10(b). When Φ_1 increases from 0 to V_{DD} and Φ_2 decreases from V_{DD} to 0, the voltage change at node B4 is from $4V_{DD}$ to $5V_{DD}$. The high voltage at node B4 brings the switching time of MPA3 closer to that of MNA3, turning off MA3 in time to reduce reverse charge flow. The reduced lossy discharge time is indicated by the time period T in Figure 2.10(b). It can be concluded

by comparing Figures 2.8(b) and 2.10(b) that the undesired charge transfer is substantially reduced due to the new gate control strategy. The optimized gate control strategy can still maintain the dead time between the auxiliary transistors MNA3 and MPA3, as demonstrated in Figure 2.10.

CP-2 is designated as the charge pump based on CP-1 but with the optimized gate control strategy. Since the architectures of both CP-1 and CP-2 are completely symmetrical, they can also be used for negative voltage generation.

2.3.3 Design considerations

To ensure the device reliability of the transistors in the CP-1 and the CP-2 circuits, the voltage applied across any two terminals of the transistors can not be allowed to exceed its maximum allowable value. Table 2.1 lists the maximum voltages across the gate, drain, and source terminals of the transistors in the CP-1 and the CP-2 circuits. As shown, the maximum $|V_{gd}|$ or $|V_{ds}|$ in the CP-1 and CP-2 circuits are $2V_{DD}$ and $3V_{DD}$, respectively. To ensure device reliability, the supply voltage needs to be lowered. For instance, if the maximum allowable voltage between $|V_{gd}|$ or $|V_{ds}|$ is $\mathrm{V_{max}}$, the maximum allowable supply voltages of CP-1 and CP-2 are $\mathrm{V_{max}}/2$ and $\mathrm{V_{max}}/3$, respectively. Alternatively, thick gate-oxide transistors, which have a higher voltage tolerance between terminals, can be used for the charge pumps to operate at a higher supply voltage.

Table 2.1: Maximum voltages across the gate, drain, and source terminals of the transistors in the CP-1 and the CP-2 circuits.

Devices	Maximum $\lvert V_{gs}\rvert$	Maximum $\lvert V_{gd}\rvert$	Maximum $\lvert V_{ds}\rvert$
Transistors in CP-1	V_{DD}	$2V_{DD}$	$2V_{DD}$
Transistors in CP-2	$2V_{DD}$	$3V_{DD}$	$3V_{DD}$

Considering the body terminals of the transistors, the body terminal of a PMOS transistor needs to be connected to its source, i.e., the terminal with the most positive value. For the NMOS transistors, triple-well structures are preferred to eliminate the body effect of the NMOS transistors.

There are several parameters involved in designing the proposed charge pumps, including the number of pumping stages, the operation frequency, the capacitance of the pumping capacitors and the output capacitor, the width/length ratio of the CTS transistors and the auxiliary transistors. Normally, the supply voltage V_{DD} is fixed in a design. The number of pumping stages is then designed to meet the output voltage specification. Increasing the pumping capacitance can effectively increase the current drive capability of the charge pump. For the output capacitor, increasing the capacitance of the output capacitor is able to reduce the voltage ripple with the drawback of a longer start-up transient response time.

At the same capacitance, higher operation frequency leads to higher output voltage, higher current drive capability, and reduced voltage ripple. However, higher operation frequency also leads to higher redistribution power loss and switching power loss. For the transistor parameters, the design of the width/length ratio of the CTS transistors and the auxiliary transistors is a trade-off between the switching power loss and the conduction power loss.

2.3.4 Simulation results

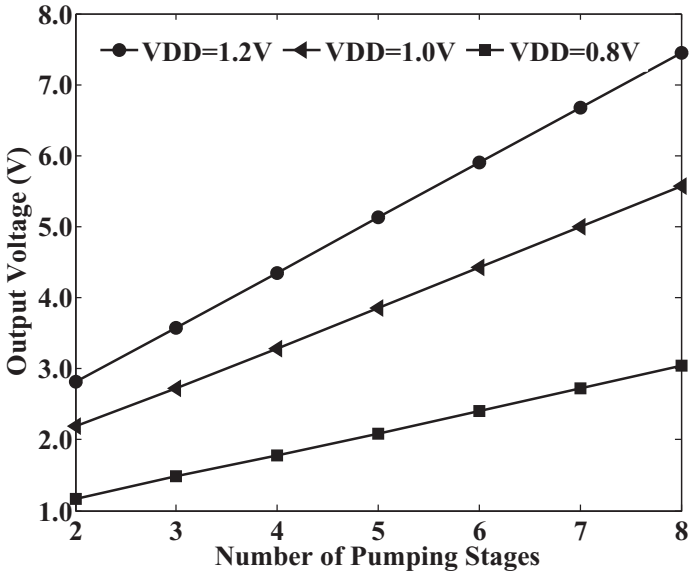
To compare the performance of the proposed charge pumps with the Dickson charge pump, the CTS charge pump (Ref [71]), and the Pelliconi charge pump (Ref [75]), simulations of 8-stage charge pump circuits were performed in the GlobalFoundries' 0.13-µm standard CMOS technology with the Cadence Spectre Circuit Simulator. Since the proposed charge pump circuits and the Pelliconi charge pump circuit are composed of two branches, for fair comparison, all circuits were simulated under the same branch condition, i.e., two identical branches with complementary clocks are connected in parallel for Ref [71] and the Dickson charge pump circuit due to their single branch scheme. Metal-insulator-metal (MIM) capacitors with a capacitance of 100 pF were used for the pumping capacitors and the output capacitor for all circuits.

As NMOS transistors are utilized in all circuits, a triple-well structure is used to eliminate the body effect of the NMOS transistors for all circuits. All transistors have the same dimensions except that a smaller size is chosen

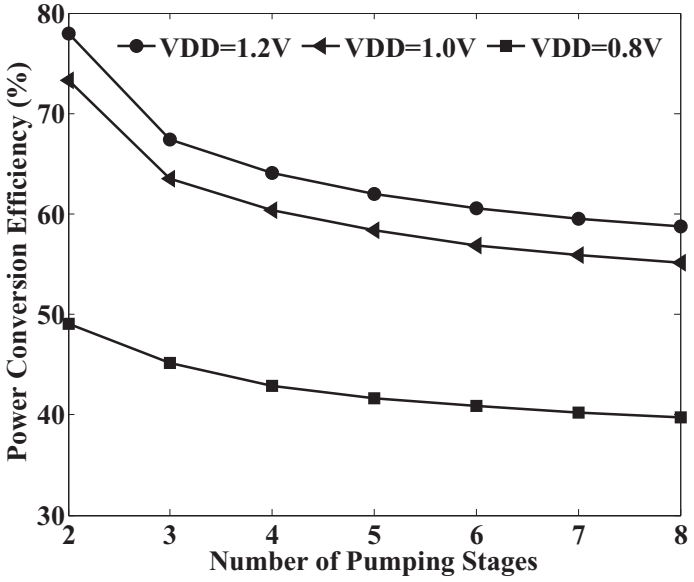
for the auxiliary transistors in the proposed charge pump circuits and [71]. All CTSs are designed with small on-resistance to reduce conduction power loss at high load current conditions. A high clock frequency of 100 MHz is used to enable the charge pumps with current drive capability of $\geq$ 5 mA. As the maximum gate-oxide voltages of the proposed charge pump circuits and Ref [71] exceed V_{DD}, thick-oxide MOSFETs are used in the proposed circuits and Ref [71] for gate-oxide reliability. As listed in Table 2.1, the maximum gate-oxide voltages of the proposed CP-1 and CP-2 circuits are $2V_{DD}$ and $3V_{DD}$ respectively, limiting the maximum allowable supply voltage to 1.2 V for the proposed CP-2 circuit in this technology. The additional area introduced by auxiliary transistors and the triple-well NMOS structure can be ignored as the chip area is dominated by the on-chip MIM capacitors. The maximum attainable output voltage of charge pumps is limited by the maximum allowable voltage of the MIM capacitors. Clock signals for charge pumps are provided by two pulse generator models in the analogLib library for simulation. A set of simulations has been performed by applying a variable current sink to the output. The simulations are done under typical conditions for both the NMOS and PMOS transistors.

Figures 2.11(a) and 2.11(b) show the simulated output voltages and power conversion efficiency of the proposed CP-2 circuit as the number of pumping stages increases. The supply voltage varies from 1.2 V to 0.8 V while the load current is fixed at 5 mA. As can be seen from Figure 2.11(a), the output voltage shows a linear growth with the increase in the number of pumping stages. This linearity remains but with reduced voltage gain as the supply voltage decreases. Power conversion efficiency drops as the number of pumping stages rises according to Figure 2.11(b). Similarly, the power conversion efficiency performance also diminishes as the supply voltage is lowered.

The simulated output voltages and power conversion efficiency of the proposed CP-2 circuit with 8 stages for various load currents are described in Figure 2.12(a) and Figure 2.12(b), respectively. Only the results at the load current ranging from 5 mA to 10 mA are shown to examine the circuit performance of high current drive capability. Supply voltages of 1.2 V, 1.0 V, 0.8

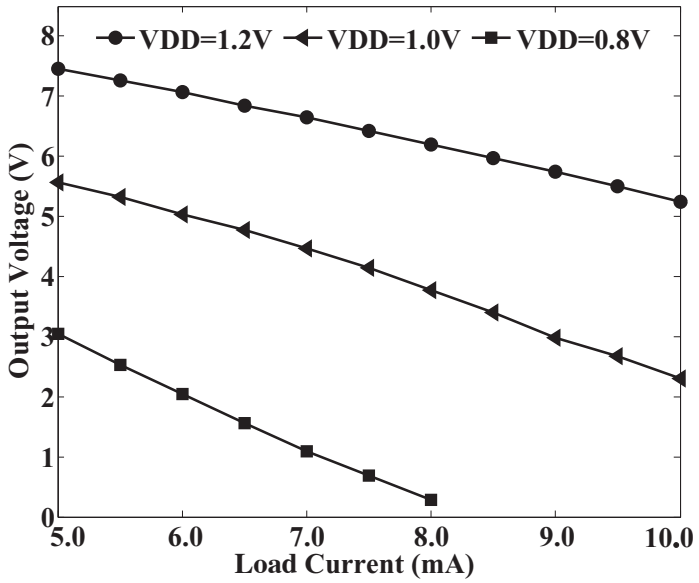


(a)

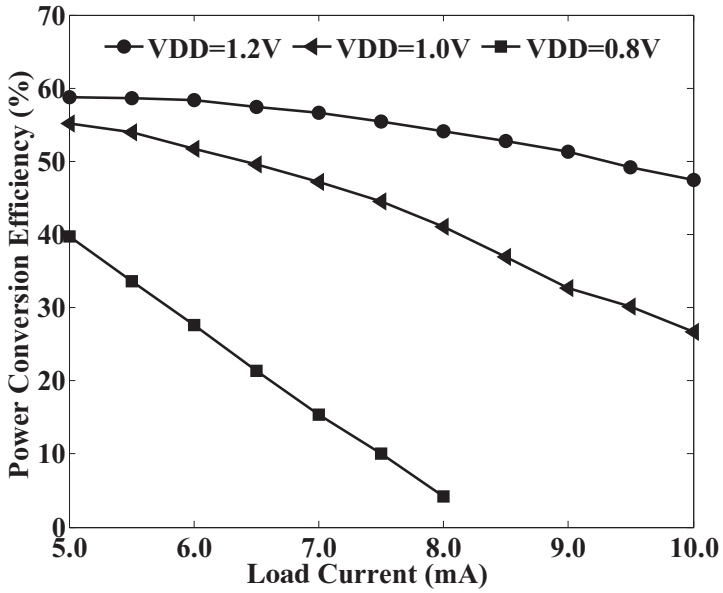


(b)

Figure 2.11: Simulated (a) output voltages and (b) power conversion efficiency of the proposed CP-2 circuit as the number of pumping stages increases. The supply voltage varies from 1.2 V to 0.8 V while the load current is fixed at 5 mA.



(a)



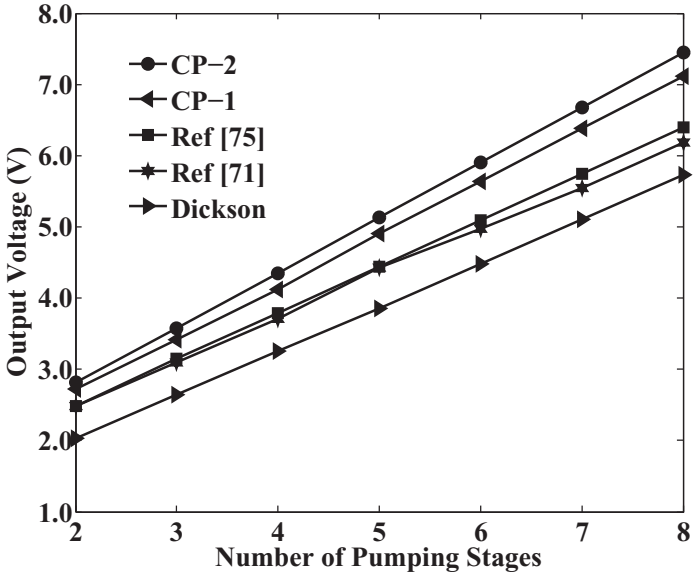
(b)

Figure 2.12: Simulated (a) output voltages and (b) power conversion efficiency of the proposed CP-2 circuit with 8 stages for various load currents under different supply voltages.

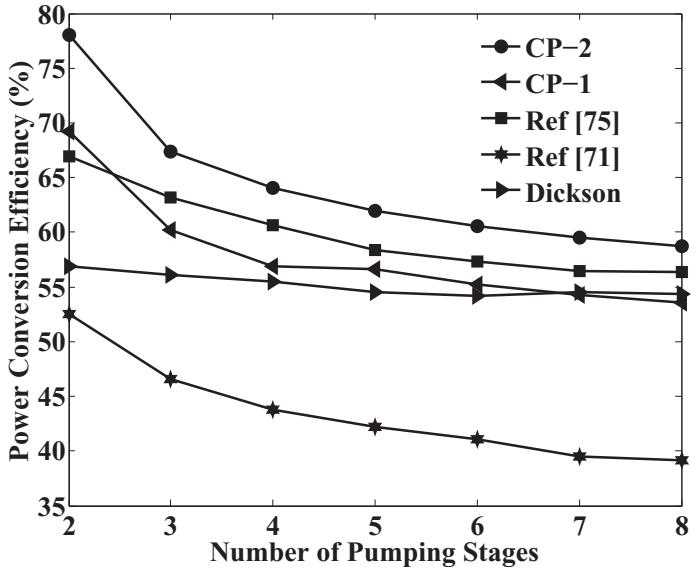
V are simulated. According to Figure 2.12(a), the output voltage reaches 7.45 V at a 5-mA load current and a 1.2-V supply voltage. With the increase of the load current, the output voltage is reduced. It is shown in Figure 2.12(a) that the output voltage of the proposed 8-stage CP-2 circuit still remains over 5 V (5.24 V) at the load current of 10 mA, which leads to an output power of as high as 52.40 mW. Furthermore, as depicted in Figure 2.12(b), the power conversion efficiency of the proposed CP-2 circuit with 8 stages reaches 58.72% at the load current I_{load} = 5 mA and the supply voltage V_{DD} = 1.2 V, and decreases while still maintaining about 50% for the load current ranging from 5 mA to 10 mA. Both the output voltage and the power conversion efficiency performance degrade as the supply voltage drops, implying that a sufficient supply voltage is needed to meet the requirement of high current drive capability.

Figures 2.13(a) and 2.13(b) compare the simulated output voltages and power conversion efficiency of Dickson, Ref [71], Ref [75], the proposed CP-1 and the proposed CP-2 circuit as the number of pumping stages increases. The supply voltage is 1.2 V and the output load current is 5 mA. As demonstrated in Figure 2.13(a), nearly all circuits show good linearity in output voltage as the number of pumping stages increases. By comparison, the proposed CP-2 circuit provides the highest output voltage compared to other circuits for any number of pumping stages, followed by the proposed CP-1 circuit. Likewise, the power conversion efficiency of the proposed CP-2 circuit is higher than other circuits at any number of stages as illustrated in 2.13(b). We can also see from 2.13(b) that the power conversion efficiency of Ref [75] exceeds the proposed CP-1 circuit at 3 or more stages, while the Dickson charge pump circuit maintains a stable power conversion efficiency for different pumping stages and Ref [71] shows a steady decline as the stage number increases.

Simulated output voltages and the power conversion efficiency of Dickson, Ref [71], Ref [75], the proposed CP-1 and the proposed CP-2 circuit with 8 stages for various load currents at a 1.2-V supply voltage are compared in Figure 2.14(a) and Figure 2.14(b), respectively. As shown in Figure 2.14(a), for the same output load current, the proposed CP-2 circuit generates higher



(a)



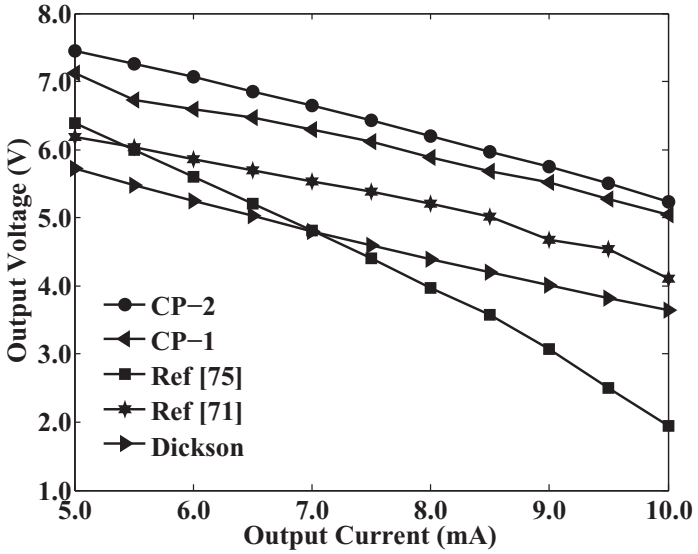
(b)

Figure 2.13: Comparison of simulated (a) output voltages and (b) power conversion efficiency of Dickson, Ref [71], Ref [75], the proposed CP-1 and the proposed CP-2 circuit as the number of pumping stages increases. The power supply voltage and output load current are 1.2 V and 5 mA, respectively.

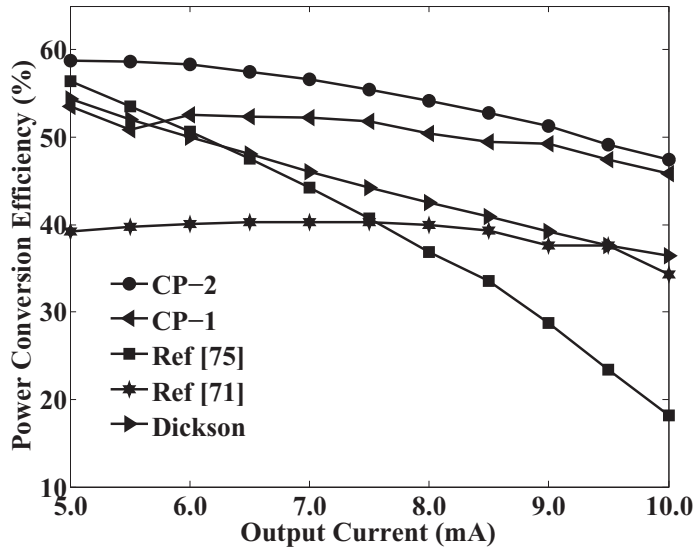
output voltages compared with other circuits, followed by the proposed CP-1 circuit, when the output load current varies from 5 mA to 10 mA. The output voltage of the charge pump in Ref [75] decreases very fast as the output load current increases, indicating a low current drive capability. Both Ref [71] the Dickson charge pump circuit show steady voltage decline similar to that of the proposed CP-1 and CP-2 circuits.

The improvement in power conversion efficiency of the proposed charge pump circuits is illustrated in Figure 2.14(b). The power conversion efficiency of the Dickson charge pump circuit steadily degrades due to the conduction loss caused by the threshold voltage drop across the drain-source terminals of transistors. Ref [71] has a relatively low conduction loss with threshold voltage drop problem eliminated, but suffers from large power loss caused by undesired charge transfer, leading to a stable power conversion efficiency of around 40% as the load current varies. With a relatively minor undesired charge transfer, the cross-coupled charge pump circuit in Ref [75] suffers from large conduction loss at high current loads due to the higher switch on-resistance of the pumping switch pair used at each stage per branch. The proposed charge pumps are designed to minimize the power loss caused by undesired charge transfer, while still be able to keep the conduction loss at a low level with only one pumping switch used at each stage per branch. As demonstrated in Figure 2.14(b), the proposed charge pump circuits are able to maintain a high efficiency even at high values of load current. We can conclude from Figure 2.14(a) and Figure 2.14(b) that compared to other circuits, the proposed charge pump circuits have higher power conversion efficiency, larger output voltage as well as higher current drive capability.

The effectiveness of the proposed charge pump circuits in reducing the output voltage ripple is demonstrated in Figure 2.15(a) under the conditions of 1.2-V supply voltage, 5-mA output current loading, and 8 pumping stages. We can see from Figure 2.15(a) that the proposed charge pump circuits present a smaller output voltage ripple compared to those of other circuits. Detailed waveform performance can be found in Table 2.2. Except for the enhancement in voltage gain, the output voltage ripple is reduced to less than 1% for both

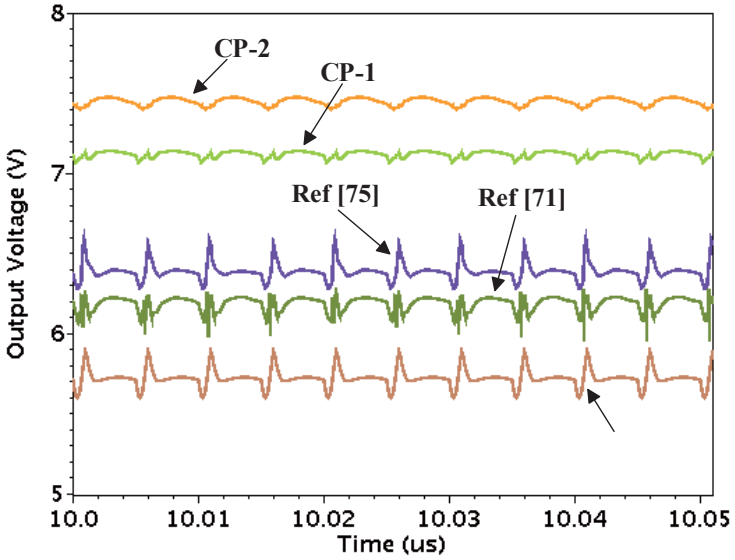


(a)

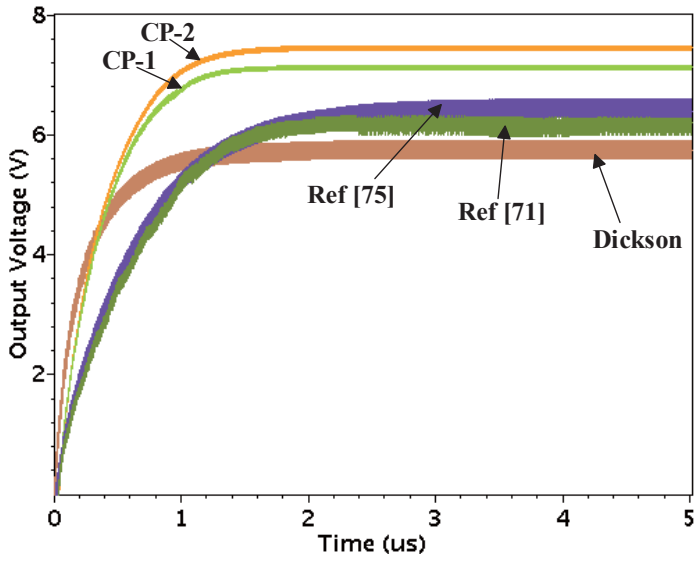


(b)

Figure 2.14: Comparison of simulated (a) output voltages and (b) power conversion efficiency of Dickson, Ref [71], Ref [75], the proposed CP-1 and the proposed CP-2 circuit with 8 stages for various load currents at a 1.2-V supply voltage.



(a)



(b)

Figure 2.15: Comparison of simulated (a) output voltage waveforms and (b) start-up responses of Dickson, Ref [71], Ref [75], the proposed CP-1 circuit and the proposed CP-2 circuit with 8 stages when driving a 5-mA current load with a 1.2-V supply voltage.

proposed CP-1 and CP-2 circuits according to Table 2.2.

In addition, comparison of start-up responses of all circuits is shown in Figure 2.15(b) with start-up response time demonstrated in Table 2.2. High average voltage slew rates at start-up can also be expected with proposed CP-1 and CP-2 circuits. We can see from Figure 2.15(b) and Table 2.2 that the proposed circuits can obtain a start-up response time of around 0.7 µs, which is preceded only by that of the Dickson charge pump circuit.

Table 2.2: Simulated output voltage performance of five different charge pump circuits.

Characteristics	Dickson	Ref [71]	Pelliconi (Ref [75])	CP-1	CP-2
Load current (mA)	5				
Number of stages	8				
Supply voltage (V)	1.2				
Output voltage (V)	5.73	6.19	6.39	7.12	7.45
Voltage gain	4.78	5.16	5.33	5.93	6.20
Output voltage ripple ΔV (mV)	292	334	310	65	73
Output voltage ripple percentage $\Delta V/V$ (%)	5.10	5.40	4.85	0.91	0.98
Start-up response time (µs)	0.55	1.11	1.20	0.75	0.77

2.4 Characterization of a 7-stage CP-2 circuit in a standard CMOS process

For a proof of concept, a 7-stage CP-2 circuit was physically implemented and tested in GlobalFoundries' 0.13-µm standard CMOS process. A complete circuit structure is shown in Figure 2.16. The parameters of all components are shown in Table 2.3. Thick-oxide transistors are used for all transistors for gate-oxide reliability. A triple-well structure is applied to all NMOS transistors

to eliminate the body effect. The sizes of the transistors were chosen to obtain small on-resistance so as to reduce conduction power loss at high current load, as well as keeping the switching power loss low when operating at a clock frequency of tens of megahertz. MIM capacitors with a capacitance of 100 pF were used for all pumping capacitors and the output capacitor.

Table 2.3: Component parameters of the 7-stage CP-2 circuit implemented in GlobalFoundries' 0.13-µm standard CMOS technology.

Function	Component	Type	Size or Value
NMOS CTS	MA1, MB1	Thick-oxide triple-well NMOS transistor	W=200 µm L=0.4 µm
PMOS CTS	MA2∼ MA7, MB2∼ MB7, MAout, MBout	Thick-oxide PMOS transistor	W=400 µm L=0.4 µm
Auxiliary NMOS	MNA2∼ MNA7, MNB2∼ MNB7	Thick-oxide triple-well NMOS transistor	W=20 µm L=0.4 µm
Auxiliary PMOS	MPA2∼ MPA7, MPB2∼ MPB7	Thick-oxide PMOS transistor	W=150 µm L=0.4 µm
Pumping capacitor	$C_{A1} \sim C_{A7}$, $C_{B1} \sim C_{B7}$	MIM capacitor	100 pF
Output capacitor	C_{out}	MIM capacitor	100 pF

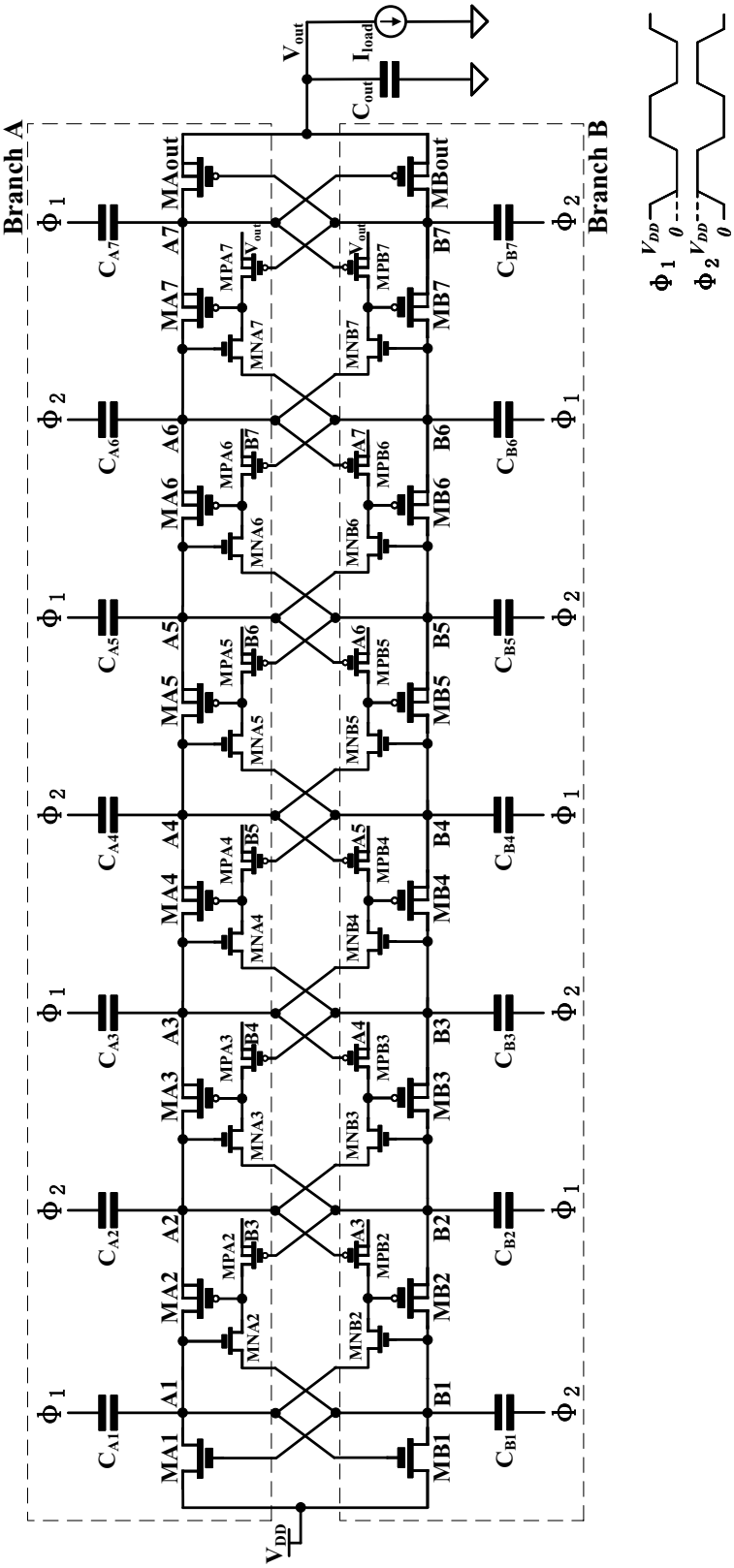


Figure 2.16: Structure of the 7-stage CP-2 circuit.

Figure 2.17 shows the micrograph of the die. The total die area is 2.0 mm^2. Both branches and the MIM capacitors are indicated. As shown in Figure 2.17, the silicon area is dominated by the on-chip MIM capacitors. A set of measurements have been performed by connecting the output to a variable current sink generated by an electronic load. The supply voltage is fixed at 1.2 V, which is the maximum allowable value to ensure gate-oxide reliability. No additional off-chip capacitors are used for the charge pump. For the clock signals, external clock driving circuits are used to amplify the power of the clock signals so as to provide sufficient input power to the charge pump.

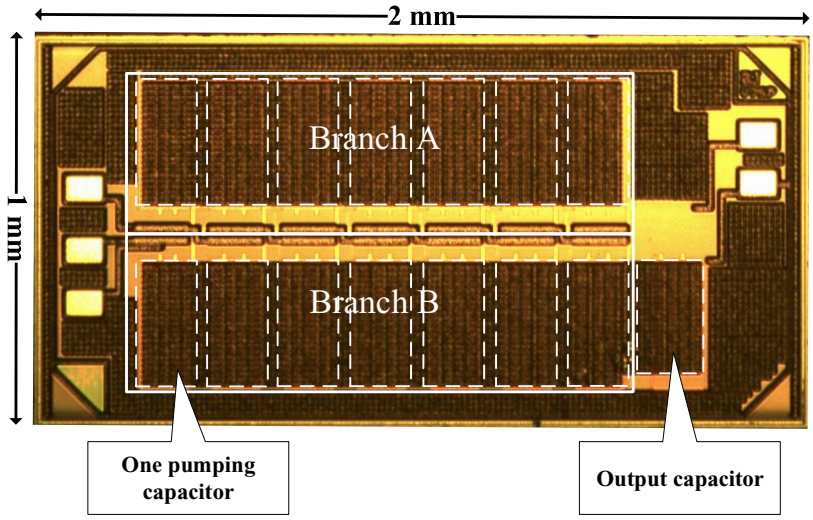


Figure 2.17: Die micrograph of the 7-stage CP-2 circuit implemented in GlobalFoundries' 0.13-µm standard CMOS technology (area: 2.0 mm^2).

Figure 2.18 shows the measured output voltage with increasing clock frequencies at no-load condition. As shown, the output voltage increases with increments in the clock frequency. The output voltage value is 5.5 V for 2 MHz and 7.2 V for 20 MHz. Since the clock signals are generated externally, due to I/O speed limitations, only operation up to 20 MHz could be measured. However, higher output voltages can be expected at higher operating frequencies.

Figure 2.19 plots the measured output voltage with the increase in load current at a clock frequency of 20 MHz. As can be seen in Figure 2.19, the

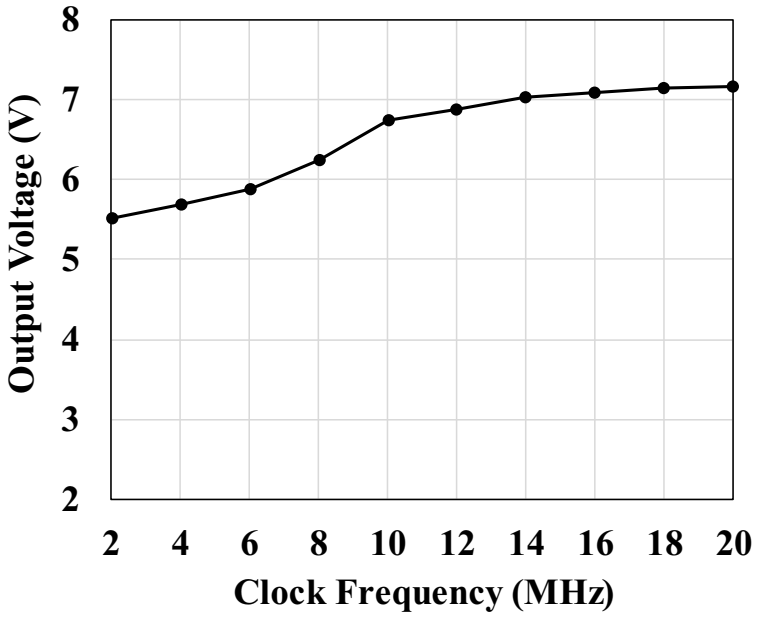


Figure 2.18: Measured output voltage as a function of the clock frequency of the 7-stage CP-2 circuit. No load current is applied to the output.

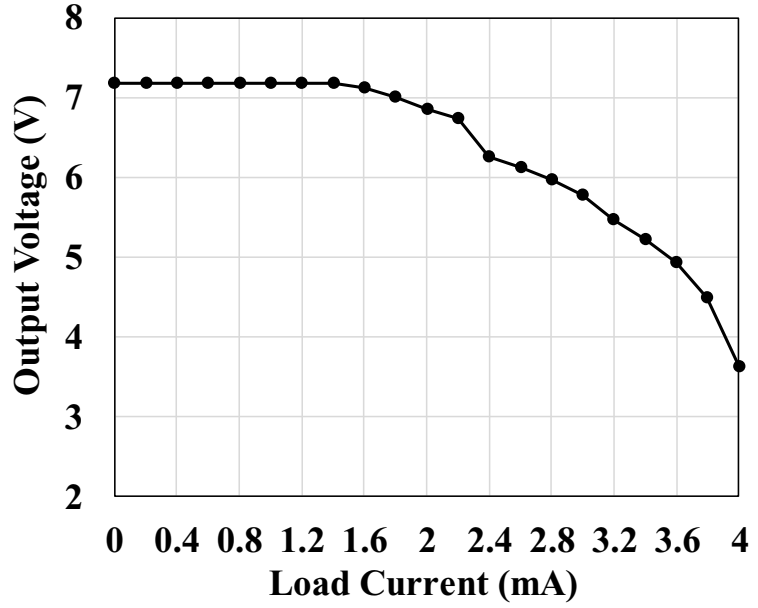


Figure 2.19: Measured output voltages as a function of the load current of the 7-stage CP-2 circuit. The clock frequency is 20 MHz.

charge pump is able to maintain an output voltage of 7.2 V as the load current increases to 1.4 mA. The output voltage then drops with further increases in load current. The power delivered to the output (P_{out}) has a maximum value of 18 mW, which occurs at a load current of 3.6 mA. As the clock signals are generated by external clock drivers, the input power can not be accurately measured, thus the power conversion efficiency with the increase of load current is not shown.

The measured output voltage waveform at the clock frequency of 20 MHz under no-load condition is shown in Figure 2.20. Observing the waveform in Figure 2.20, we can see that the voltage ripple has a period of around 25 ns, even though the operation period of the charge pump is 50 ns (the operation frequency is 20 MHz). This is because the proposed charge pump is composed of two branches, and power is delivered alternately to the load by the two branches. The value of the output voltage ripple is 1 V. The voltage ripple can be effectively reduced by increasing the capacitance of the output capacitor.

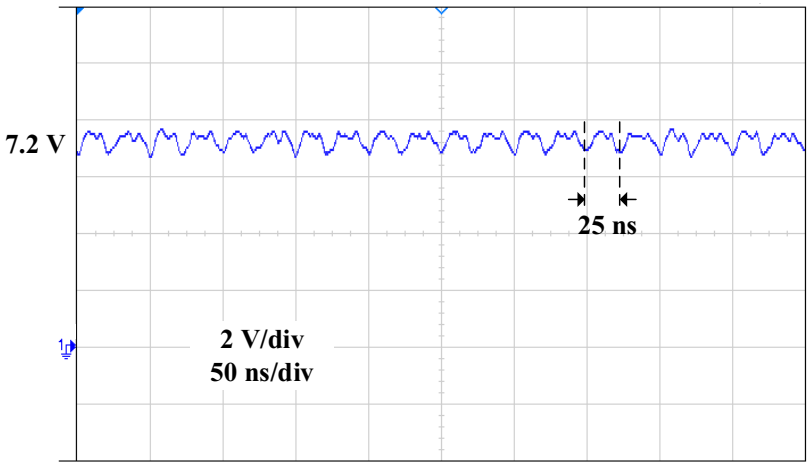


Figure 2.20: Measured Output voltage waveform of the 7-stage CP-2 circuit under no-load condition. The clock frequency is 20 MHz.

Table 2.4 compares the measured performance of the test chip with the other charge pumps implemented in standard CMOS processes with milli-ampere current drive capability. As shown, the proposed 7-stage CP-2 circuit has the highest voltage conversion ratio. Even though the peak power con-

Table 2.4: Performance comparison with other charge pumps implemented in standard CMOS processes with milli-ampere current drive capability.

	SCPC4 in [78]	[79]	This work
Technology	0.18-µm standard CMOS	0.13-µm standard CMOS	0.13-µm standard CMOS
Pumping capacitor	on-chip 260 pF per stage	on-chip 400 pF per stage	on-chip 200 pF per stage
Supply voltage	1.8 V	1 V	1.2 V
Maximum output voltage	5.4 V @ 10 MHz	1.8 V @ 20 MHz	7.2 V @ 20 MHz
Voltage gain	3	1.8	6
Peak power efficiency $\eta_{\max}$	83% @ 10 MHz	82% @ 20 MHz	around 60% @ 20 MHz
Maximum P_{out}	around 3.4 mW	around 2.7 mW	18 mW
Chip area	-	2.25 mm^2	2 mm^2

version efficiency of this work is lower than other charge pumps, the power delivered to the output is much higher compared to other charge pumps.

One note is that the clock signals for the 7-stage CP-2 circuit are generated by external clock drivers. This causes the ringing of the clock signals, which was introduced by the parasitic inductance and capacitance from the packages and the PCB. This ringing can cause the peak voltage of the clock signals to be over 1.2 V, which degrades the reliability of the circuit. Therefore, integrating the clock drivers on the same die with the charge pump is highly recommended.

2.5 Characterization of a 4-stage CP-1 circuit in an HVCMOS process

As listed in Table 2.1, the CP-1 circuit and the CP-2 circuit suffer from a maximum $|V_{ds}|$ of $2V_{DD}$ and $3V_{DD}$, respectively. This significantly limits the maximum allowable supply voltage. Improving the supply voltage of a charge pump is able to increase the output power effectively. This is desirable as

it includes more flexibility for the proposed LIUS system to be applied for different therapeutic applications with different ultrasound power intensity requirements.

To improve the supply voltage, HV devices provided by HVCMOS processes can be used. Many modern HVCMOS processes provide HV devices with high breakdown voltages across drain and source terminals, while the gate-source voltage $|V_{gs}|$ is limited. The high breakdown voltage across the drain-source terminal enables the charge pump to operate at a higher supply voltage, thus effectively improving the output power.

In this Section, a 4-stage CP-1 circuit is designed, implemented, and tested in TSMC's 0.18-µm Bipolar-CMOS-DMOS (BCD) Gen2 process. The CP-1 circuit structure is utilized instead of the CP-2 circuit structure. This is because the CP-2 circuit suffers from a maximum $|V_{gs}|$ of $2V_{DD}$, which limits the maximum allowable supply voltage, while the CP-1 circuit has a maximum $|V_{gs}|$ of V_{DD}, enabling the supply voltage to operate up to the maximum allowable $|V_{gs}|$. Therefore, when implemented in HVCMOS processes, the CP-1 circuit structure is preferred than the CP-2 circuit structure in terms of improving the supply voltage.

Figure 2.21 shows the structure of the proposed 4-stage CP-1 circuit implemented in an HVCMOS technology. Unlike the devices of the charge pump circuit in Figure 2.16, which only utilizes LV transistors from a standard CMOS process, all transistors in Figure 2.21 are HV transistors, which offer high breakdown voltages across drain and source terminals, while the gate-source voltage is limited. For a better illustration, HV devices are indicated with two bars at the drain terminals.

Similar to the circuits implemented in standard CMOS processes, the circuit in Figure 2.21 consists of two complementary branches. Each branch consists of transistors for charge transfer (for instance, MA1, MA2, MA3, MA4, and MAout in Branch A) and auxiliary transistors for gate control (for example, MNA2 and MPA2 controlling the gate of MA2). The body diodes of auxiliary transistors are not shown in Figure 2.21. Same as the circuits implemented in standard CMOS processes, a simple two-phase clocking scheme

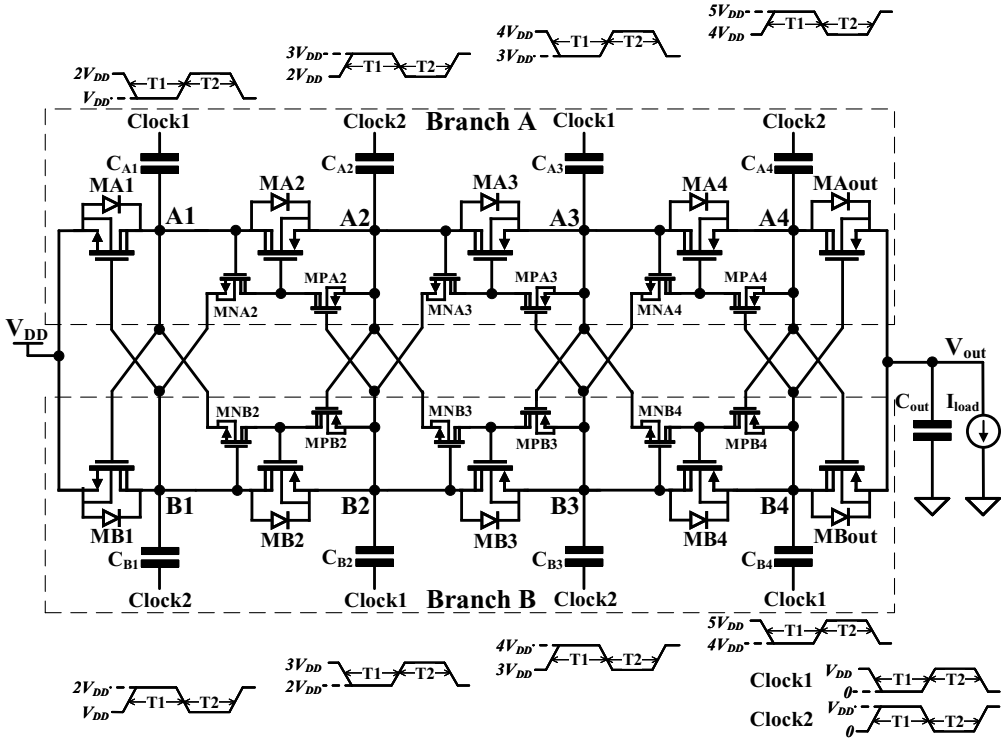


Figure 2.21: Structure of the 4-stage CP-1 circuit. All devices in this figure are HV devices.

is used for the circuit in Figure 2.21, i.e., Clock1 and Clock2 are out-of-phase and both have voltage levels between V_{DD} and the ground.

Different from the charge pumps implemented in standard CMOS processes, which only utilize LV devices, charge pumps implemented in HVCMOS processes need to be taken with extra design considerations. This is because the drain and source terminals of the HV transistors are not exchangeable. Besides, compared to the LV transistors, HV transistors suffer from parasitic body diodes. For the charge pump implemented using HV devices, we have taken advantage of the body diodes of the HV transistors. To explain this, the detailed operation of the circuit in Figure 2.21 is described below.

Operation principle

For the first stage, during the time interval T1 when Clock1 is low and Clock2 is high, the voltages at the nodes A1 and B1 are close to but smaller than V_{DD} and $2V_{DD}$, respectively. HVNMOS MB1 in Branch B is turned off with

its gate connected to node A1, cutting off the path from the high voltage node B1 back to the power supply. While in Branch A, desirable charge is pushed from the power supply to the capacitor C_{A1} through both the body diode and the channel of MA1. It is crucial to connect the source terminals of HVNMOS MA1 and MB1 to the power supply, so that they are able to cut off the reverse charge from high voltage nodes back to the power supply when they are turned off. The first-stage operation is intuitively depicted in Figure 2.22. Devices that are turned off are indicated in grey and the arrows in Figure 2.22 indicate the flow of charge.

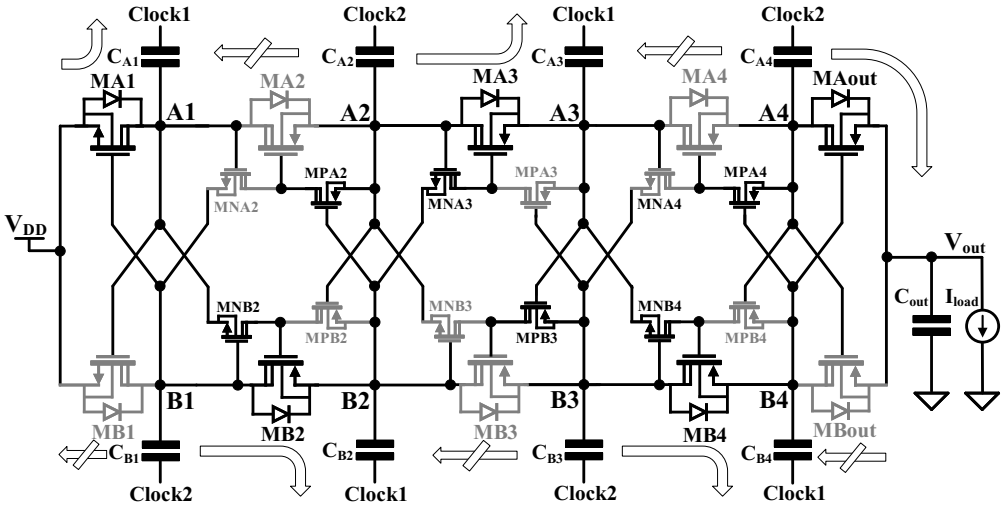


Figure 2.22: Circuit operation of the 4-stage CP-1 circuit during the time interval T1 when Clock1 is low and Clock2 is high (devices that are turned off are indicated in grey and the arrows indicate the flow of charge).

To describe the operation of the middle stages, taking the second stage as an example. During the time interval T1, the voltages at the nodes A2 and B2 are about $3V_{DD}$ and $2V_{DD}$, respectively. This turns the auxiliary transistor MPA2 on with a source-gate voltage of V_{DD}. The on-state of MPA2 connects the gate terminal of HVPMOS MA2 to its source terminal, turning off MA2 and thus preventing the reverse charge from the high voltage node A2 back to the low voltage node A1. On the other hand, HVPMOS MB2 in Branch B is turned on with its gate terminal connected to node A1 through MNB2, charging the capacitor C_{B2} with a high voltage at node B1 through both the body diode and the channel of MB2. The circuit operation at the second stage

during the time interval T1 can also be intuitively seen from Figure 2.22. Similar to HVNMOS MA1 and MB1, the connection method of HVPMOS MA2 and MB2 is able to cut off the reverse charge from the high voltage nodes back to the low voltage nodes while maintaining the desirable charge flow by taking advantage of their body diodes.

For the output stage, only one HVPMOS device is used, i.e., MAout for Branch A and MBout for Branch B. During the time interval T1, MAout is turned on, enabling the high voltage at node A4 to charge the output capacitor C_{out}, while MBout is turned off to cut off the reverse charge transfer. Intuitive demonstration of the circuit operation at the output stage during the time interval T1 is also shown in Figure 2.22.

The operation of the proposed charge pump during the time interval T2 works in a complementary fashion compared to that of the time interval T1. Capacitors C_{A2}, C_{A4}, C_{B1}, C_{B3} are charged, while capacitors C_{A1}, C_{A3}, C_{B2}, C_{B4} are discharged, and the charge is delivered to the output from node B4. Figure 2.23 intuitively shows the circuit operation during the time interval T2.

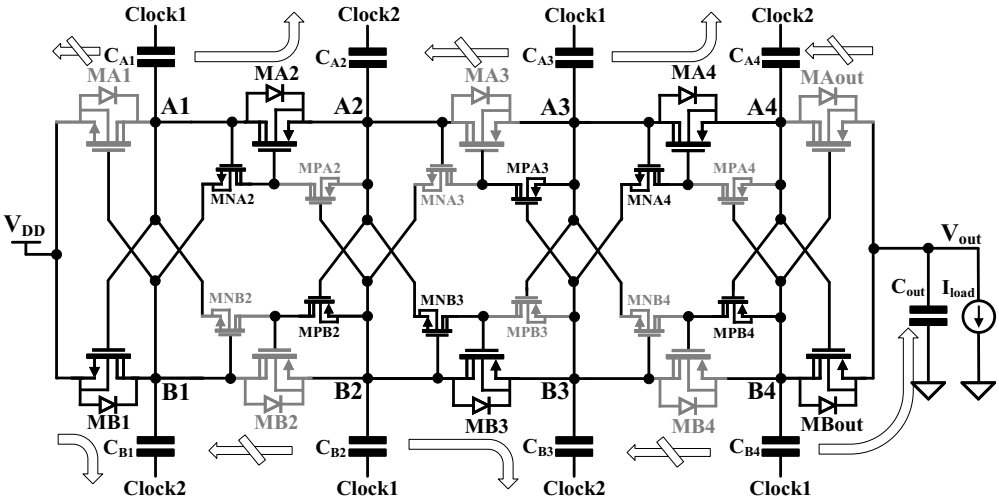


Figure 2.23: Circuit operation of the 4-stage CP-1 circuit during the time interval T2 when Clock1 is high and Clock2 is low (devices that are turned off are indicated in grey and the arrows indicate the flow of charge).

The maximum voltages of $|V_{gs}|$, $|V_{gd}|$, and $|V_{ds}|$ for all transistors in Figure 2.21 are V_{DD}, $2V_{DD}$, and $2V_{DD}$, respectively. Though with limited gate-source voltage, the HV transistors offer high breakdown voltage across drain-source

terminals (hence high breakdown voltage for gate-drain terminals). This enables the circuit to operate at a supply voltage up to the maximum allowable $|V_{gs}|$.

Clock drivers

Most of the input power of the charge pump is supplied by Clock1 and Clock2. In order to provide sufficient input power to the charge pump, two clock drivers are designed and integrated on the same die with the charge pump. The circuit structures of the clock drivers are shown in Figure 2.24.

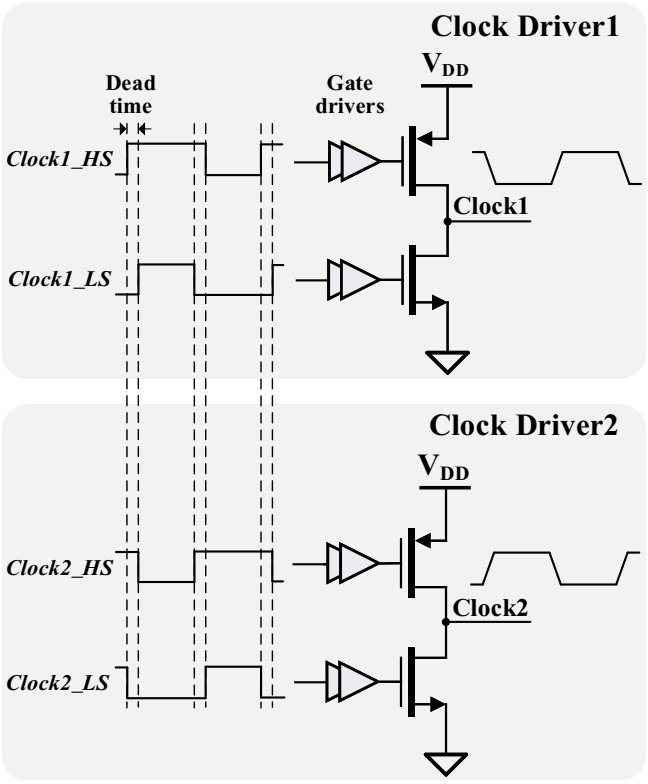


Figure 2.24: Structure of the two clock drivers.

As shown in Figure 2.24, the clock drivers for Clock1 and Clock2 have the same structure but use different control signals. The clock drivers apply a half-bridge topology. Each half-bridge driver utilizes a PMOS device as the high-side switch and an NMOS device as the low-side switch at the output stage. For its parameter design, each output switch needs to be designed with wide transistors with low on-resistance to reduce conduction power loss.

However, wide transistors tend to have high switching power loss. To optimize the power performance, the trade-off between the switching power loss and the conduction power loss needs to be considered.

As demonstrated in Figure 2.24, two clock control signals are used for each clock driver, i.e., *Clock1_HS* and *Clock1_LS* for Clock Driver1, and *Clock2_HS* and *Clock2_LS* for Clock Driver2. For each clock driver, dead time is generated between the high-side and low-side control signals to prevent shoot-through current from V_{DD} to the ground. Clock control signals between the two clock drivers are also correlated in terms of dead time, as shown in Figure 2.24, in order to generate out-of-phase *Clock1* and *Clock2*.

The gate drivers for the output switches apply a inverter-chain structure, also known as tapered buffer structure. Figure 2.25 shows the tapered buffer structure used for the gate drivers of the output switches in Figure 2.24. The tapering factor of the tapered buffer in Figure 2.25 is 4, meaning that the transistors channel width has a scale of 1 to 4 in any two consecutive inverters. It is also generally known as the driving strength being 4 times higher for each added inverter, as demonstrated in Figure 2.25.

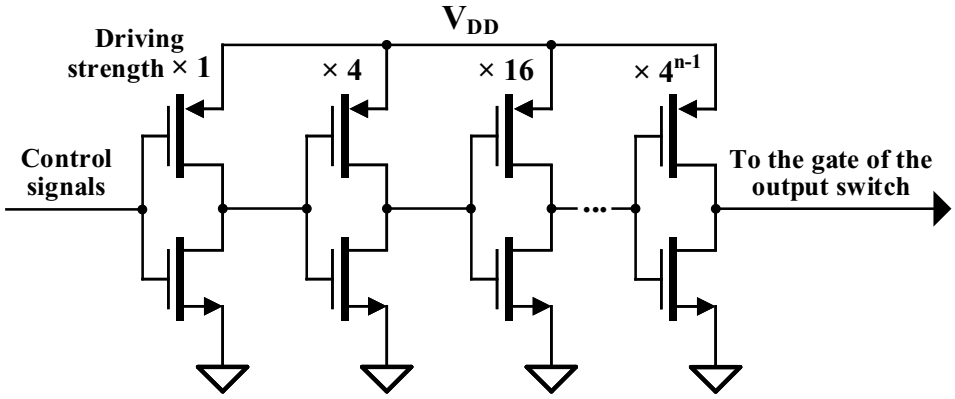


Figure 2.25: Tapered buffer structure used for the gate drivers of the output switches.

As all transistors operate at a low supply voltage of V_{DD}, standard LV transistors are used for all devices in Figures 2.24 and 2.25.

Measurement results

The 4-stage CP-1 circuit shown in Figure 2.21 has been implemented with the HVCMOS technology provided by TSMC's 0.18-µm BCD Gen2 process. The design parameters are shown in Table 2.5. Additionally, the parameters for the output switches of the clock drivers are designed with width/length ratios of 10 mm/0.6 µm for the NMOS transistors and 20 mm/0.5 µm for the PMOS transistors, which have an on-resistance of around 200 mΩ. The parameters are designed by optimizing the power conversion efficiency when operating at a clock frequency of 20 MHz while delivering an output power of up to 100 mW (output voltage of around 10 V and output current of around 10 mA).

Table 2.5: Component parameters of the 4-stage CP-1 circuit implemented in TSMC's 0.18-µm BCD Gen2 process.

Function	Component	Type	Size or Value
NMOS CTS	MA1, MB1	HVNMOS transistor	W=10 mm L=1.3 µm
PMOS CTS	MA2∼ MA4, MB2∼ MB4, MAout, MBout	HVPMOS transistor	W=20 mm L=0.4 µm
Auxiliary NMOS	MNA2∼ MNA4, MNB2∼ MNB4	HVNMOS transistor	W=40 µm L=1.3 µm
Auxiliary PMOS	MPA2∼ MPA4, MPB2∼ MPB4	HVPMOS transistor	W=300 µm L=0.4 µm
Pumping capacitor	$C_{A1} \sim C_{A4}$, $C_{B1} \sim C_{B4}$	MIM capacitor	132 pF
Output capacitor	C_{out}	MIM capacitor	264 pF

Figure 2.26 shows the micrograph of the chip. As shown in Figure 2.26, the chip size is dominated by the on-chip MIM capacitors. Since the unit capacitance of the MIM capacitors in an HV technology is generally several times less than that in a LV technology [49], the silicon area is quite large (5.0

mm^2 excluding bonding pads).

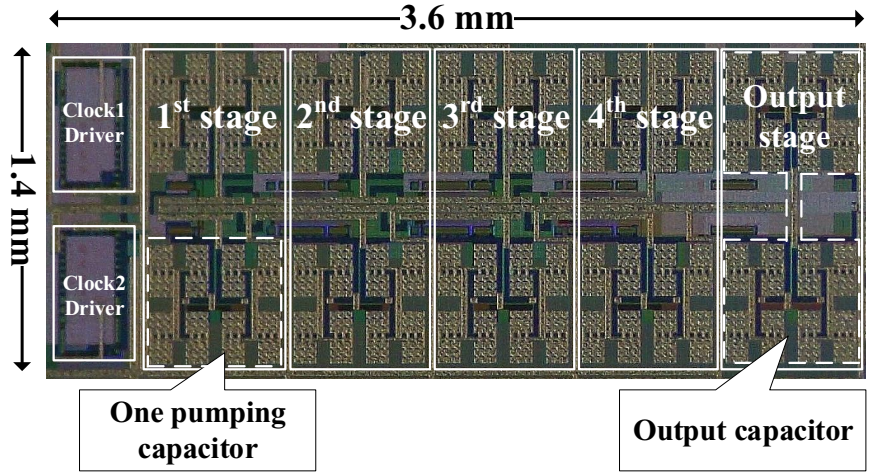


Figure 2.26: Micrograph of the test chip, including both the charge pump and the clock drivers (total area: 5 mm^2).

A set of measurements was performed applying a variable current sink (generated by an electronic load) to the output. A supply voltage of 3.7 V was used. However, the proposed circuit could operate with a supply voltage of up to 5 V, which is the maximum allowable voltage for $|V_{gs}|$ of the HV transistors. A higher output voltage can be expected with a higher supply voltage.

The control signals *Clock1_HS*, *Clock1_LS*, *Clock2_HS*, and *Clock2_LS* for the clock drivers are generated externally by a Field-Programmable Gate Array (FPGA), which have a frequency of 20 MHz and a dead time of 5 ns. Figure 2.27 shows the measured control signals. The voltage ringing in Figure 2.27 is caused by the parasitic inductance and capacitance from the package leads and the PCB. A slight waveform distortion can be observed from Figure 2.27. This is mostly caused by the differences of the oscilloscope probes, which get more apparent at high frequencies.

The measured output voltage and power conversion efficiency with the increase in load current are shown in Figure 2.28 and Figure 2.29, respectively. As shown in Figure 2.28, the output voltage drops with increases in the load current. The proposed 4-stage charge pump is able to maintain an output voltage of over 10 V as the load current increases to 10 mA. From Figure 2.29, it can be seen that the power conversion efficiency increases with the load

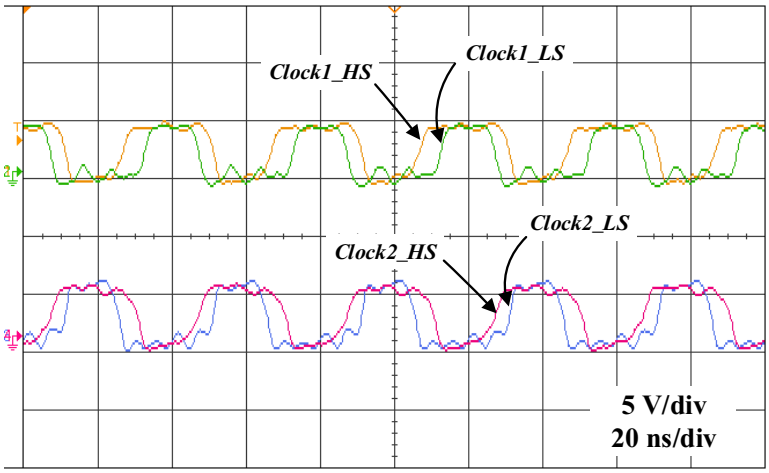


Figure 2.27: Measured control signals *Clock1_HS*, *Clock1_LS*, *Clock2_HS*, and *Clock2_LS* generated by an FPGA.

current until it reaches its maximum. The peak power conversion efficiency is 29% at a load current of 11 mA, considering both the power loss of the clock drivers and the charge pump. output power at the peak efficiency is 105 mW.

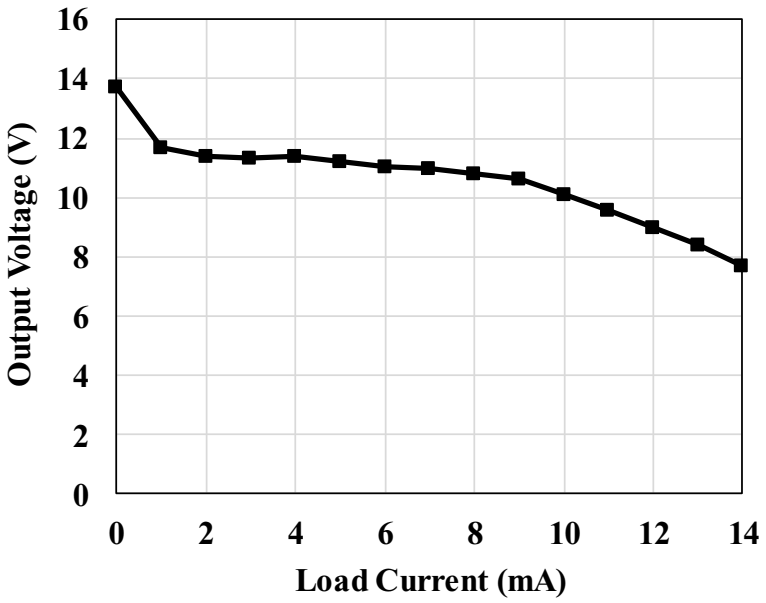


Figure 2.28: Measured output voltage of the 4-stage CP-1 circuit with the increase in load current at the clock frequency of 20 MHz.

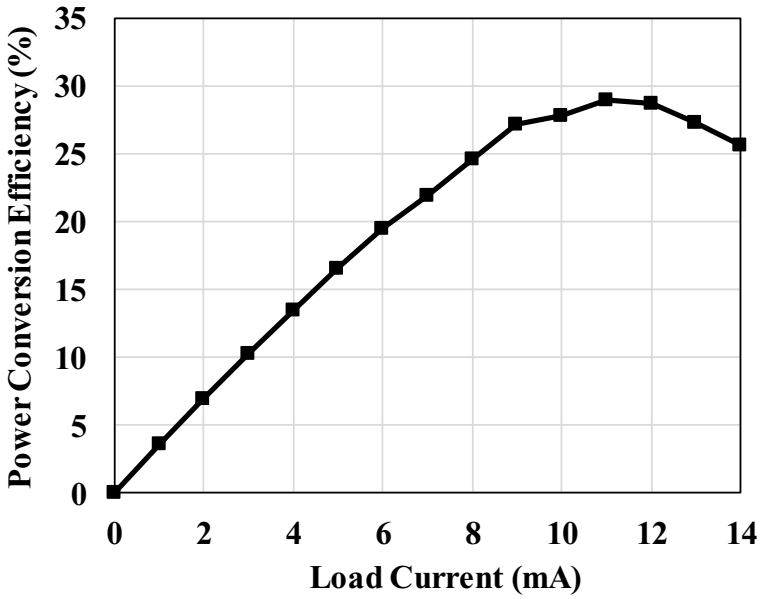


Figure 2.29: Measured power conversion efficiency of the 4-stage CP-1 circuit with the increase in load current at the clock frequency of 20 MHz (power losses of both the clock drivers and the charge pump are considered).

The power losses mainly consist of the conduction power loss and the switching power loss contributed by both the clock drivers and the charge pump. Since all transistors of the charge pump are HV transistors and the on-resistance of HV transistors is generally larger than that of LV transistors, the proposed charge pump has a higher conduction power loss compared to the loss in charge pumps that are implemented in standard technologies. Moreover, since MIM capacitors are used for all the pumping capacitors as floating capacitors, and MIM capacitors in HV technologies have a higher degree of non-ideality (the parasitic parameter can be up to 0.4 [49]), this leads to higher power consumption of the proposed 4-stage CP-1 circuit. The large on-resistance of the HV transistors and the non-idealities of the HV capacitors also limit the value of the output voltage. The power conversion efficiency and the output voltage can be effectively improved by using off-chip capacitors with the drawback of increased board size.

Figure 2.30 shows the output voltage waveform of the charge pump under no-load condition. Similar to the output voltage waveform shown in Figure 2.20, it can also be observed from Figure 2.30 that the voltage ripple has

a period of around 25 ns, due to the complementary branch scheme of the proposed charge pump. The value of the output voltage ripple is 2.2 V. The voltage ripple can be reduced by enlarging the output capacitor of the charge pump. On another note, the load current in the results shown in Figure 2.28 and Figure 2.29 is continuous current. When driving a pulsed current load, which is the case of the proposed LIUS system, the proposed charge pump is able to deliver a higher peak current, but the average output power delivered by the charge pump is similar, i.e., up to 100 mW.

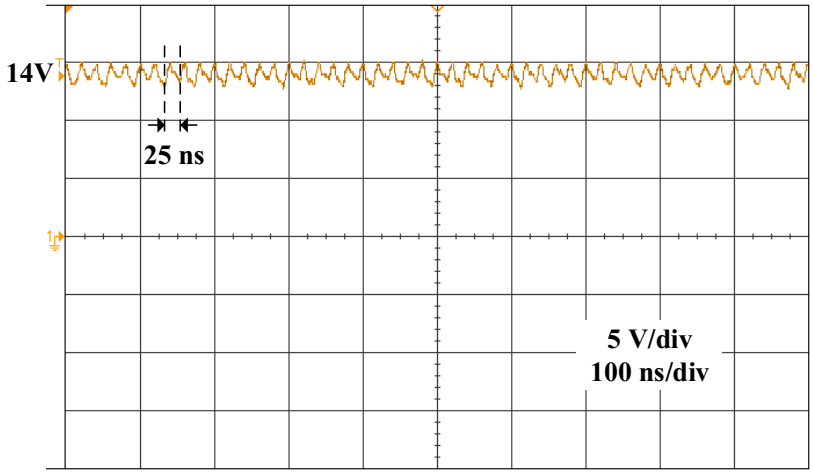


Figure 2.30: Measured output voltage waveform of the 4-stage CP-1 circuit at a clock frequency of 20 MHz under no-load condition.

To compare the performance of the proposed charge pump circuit with other recent charge pump circuits implemented in HVCMOS technologies, Table 2.6 summarizes the results of the proposed circuit and the data reported in [80] and [81]. The supply voltages of all circuits are low voltages. The number of stages used for [80], [81], and the proposed circuit is 7, 36, and 4, leading to a maximum output voltage of 32 V, 120 V, and 14 V, respectively. The charge pump capacitors for all circuits are on-chip capacitors. Compared with [80], the proposed circuit has slightly lower power conversion efficiency. However, the output power delivered by the proposed circuit is significantly higher than that of [80]. Compared with [81], both the power conversion efficiency and the output power of the proposed circuit are much higher than those of [81].

Table 2.6: Comparison with other charge pumps implemented in HVCMOS technologies.

Parameters	[80]	[81]	This work
Technology	0.18-µm HVCMOS	0.35-µm HVCMOS	0.18-µm HVCMOS
Supply voltage	5 V	3.7 V	3.7 V
Number of stages	7	36	4
Maximum output voltage	32 V	120 V	14 V
Frequency	60 kHz	10 MHz	20 MHz
Pumping capacitor	On-chip 100 pF per stage	On-chip (no exact value given)	On-chip 264 pF per stage
Maximum power efficiency $\eta_{\max}$	35%	12.6% (excluding clock drivers)	29%
Output power @ $\eta_{\max}$	160 µW	13.7 mW	105 mW
Chip area	1 mm^2	21.84 mm^2	5 mm^2

2.6 Conclusion

This chapter presents two new charge pump circuits with high current drive capability for the application of the proposed LIUS system. These two circuits employ a complementary branch scheme based on the CTS topology to minimize the reverse charge transfer in previously reported charge pump circuits. A two-phase clocking scheme with internally generated control signals is utilized to reduce circuit complexity. In the first proposed charge pump (CP-1), undesired charge transfer caused by simultaneous conduction of the auxiliary transistors is eliminated using gate control signals that are generated in both complementary branches. To further improve the design, the second proposed charge pump circuit (CP-2) optimizes the gate control strategy to reduce the reverse charge transfer caused by delayed turning off of CTSs. Simulations of an 8-stage case of the proposed CP-2 circuit implemented in a 0.13-µm standard CMOS technology show an output voltage of 7.45 V with a 5-mA current

load from a 1.2-V supply voltage at a 100-MHz clock frequency while achieving a power efficiency of 58.72%, where both the voltage pumping gain and the power conversion efficiency are higher than those of previously reported charge pumps simulated under the same condition.

A 7-stage CP-2 circuit was physically implemented and tested in a 0.13-µm standard CMOS process. Measurement results show that at a clock frequency of 20 MHz, the proof-of-concept test chip has high voltage conversion ratio (1.2 V to 7.2 V when driving a load current of up to 1.4 mA) and high current drive capability (up to 4 mA).

Device reliability is analyzed for the proposed CP-1 and CP-2 circuits, showing that the maximum $|V_{gs}|/|V_{gd}|/|V_{ds}|$ is $V_{DD}/2V_{DD}/2V_{DD}$ for CP-1 and $2V_{DD}/3V_{DD}/3V_{DD}$ for CP-2. This limits the maximum allowable supply voltage of the charge pump when implemented in standard CMOS processes.

This problem can be solved by implementing charge pumps in HVCMOS processes. A 4-stage CP-1 circuit was designed, implemented, and tested in a 0.18-µm HVCMOS process that supports a higher supply voltage so as to improve the output power level. The HV transistors in the HVCMOS process provide high break-down voltages across drain-source/gate-drain terminals, while the gate-source voltage is limited. The CP-1 circuit structure is utilized instead of CP-2 as the first design can operate at a supply voltage up to the maximum allowable $|V_{gs}|$. Measurement results of the 4-stage CP-1 circuit show that a maximum output voltage of 14 V is achieved with a supply voltage of 3.7 V. The peak power conversion efficiency is 29 % (considering both the power losses of the charge pump and the clock drivers) and the output power at this point is 105 mW. The high output power of the charge pump offers more flexibility for the the proposed LIUS system to be applied for different therapeutic applications with different ultrasound power intensity requirements.

Chapter 3

Half-Bridge Transducer Driver with a High-Speed Low-Power-Consumption HV Level Shifter

3.1 Ultrasound transducer models

As the load of the transducer driver, the model of the ultrasound transducer is first examined. For therapeutic applications, most systems utilize piezoelectric transducers, mostly lead zirconate titanate (PZT) transducers. Recently, capacitive micromachined ultrasonic transducers (CMUTs) have been studied and shown to provide an alternative solution for therapeutic applications [82]. However, since the efficacy of using CMUTs for therapeutic applications still needs further investigation, we applied a PZT transducer as the load for the proposed LIUS system.

The PZT ultrasound transducer is a type of electroacoustic transducer that is able to convert electrical energy into acoustic energy [83]. One popular model of the PZT transducer is the Butterworth-Van Dyke (BVD) circuit [84], [85], as depicted in Figure 3.1(a). This circuit consists of an R-L-C circuit corresponding to the motional arm, shunted by a static capacitance C_o, which is the parallel plate capacitor [86]. The resistance R_1 in the R-L-C circuit represents the mechanical consumption (both the dissipation and the acoustic emission into medium), while the inductance L_1 is the oscillatory mass and the

capacitance C_1 is its compliance [87]. The impedance of the PZT transducer model in Figure 3.1(a) can be derived as

$$Z = \frac{\omega^2 C_1 L_1 - 1 - j\omega R_1 C_1}{\omega^2 R_1 C_o C_1 + j(\omega^3 C_o C_1 L_1 - \omega C_o - \omega C_1)} \tag{3.1}$$

where ω is the angular frequency and j is the unit imaginary number. At the mechanical resonance frequency of a piezoelectric transducer, the series inductance and capacitance cancel each other out and a simplified equivalent circuit can be obtained, as demonstrated in Figure 3.1(b) [88]. The PZT transducer impedance is thus simplified as

$$Z = \frac{R_{eq}}{1 + j\omega C_{eq} R_{eq}} \tag{3.2}$$

where $C_{eq} = C_o$ and $R_{eq} = R_1$. For the proposed LIUS system, the PZT transducer operates at its resonance frequency. Therefore, the PZT transducer model in Figure 3.1(b) is used to simplify the system design.

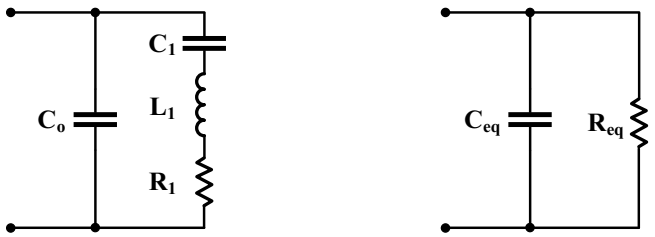


Figure 3.1: PZT transducer models: (a) the BVD model (modified from [84], [85]) and (b) the simplified model at the resonance frequency (modified from [88]).

3.2 Half-bridge transducer driver

To drive a PZT transducer with the models shown in Figure 3.1, a half-bridge driver is used for our proposed LIUS system. This is because half-bridge drivers have the capability for wide-bandwidth operation, which is desirable for the proposed system to generate LIUS with different ultrasound frequencies for different therapeutic applications, as discussed in the Chapter 1. Half-bridge

drivers can also be easily integrated on chip, reducing the board area of the proposed LIUS system.

Figure 3.2 shows the block diagram of the transducer driver. It has the same circuit structure as in Figure 1.4 but is presented here with more detail. The high voltage V_{PP} in Figure 3.2 is connected to the output of the charge pump proposed in Chapter 2. The transducer load is connected between the switching node of the half-bridge circuit and the ground. Two n-type switches Q1 and Q2 are utilized at the output stage. Similar to the HVNMOS devices used in the charge pump in Figure 2.21, these two n-type switches are HVNMOS devices with a high breakdown voltage across drain-source terminals while the gate-source voltage V_{gs} is limited (the body diodes of the HVNMOS devices are not shown). One advantage of utilizing an n-type switch at the high side is that the half-bridge circuit can tolerate the voltage ripple of V_{PP} when the high-side (HS) switch is on. This is because a stable voltage is applied across the gate-source terminals of the HS switch using a bootstrap circuit to turn it on completely, regardless of the voltage ripple of V_{PP}. However, a more complicated gate control scheme is needed for the HS switch.

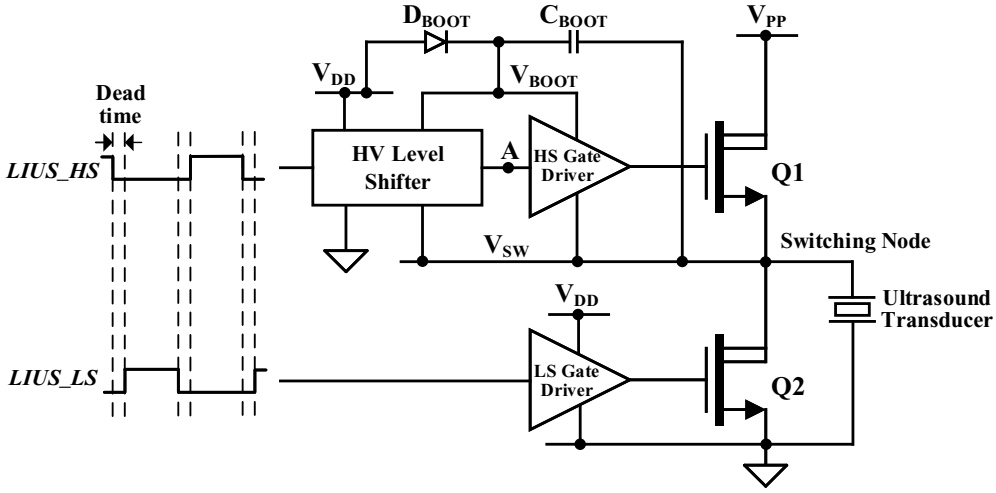


Figure 3.2: Block diagram of the half-bridge transducer driver.

The control signals *LIUS_HS* and *LIUS_LS* in Figure 3.2 are generated by the digital control block in the LV domain ($0 \sim V_{DD}$). The low-side (LS) control signal *LIUS_LS* is fed to the gate of the LS switch Q2 through the LS

gate driver. The HV level shifter elevates the HS control signal *LIUS_HS* from the LV domain to the floating HV domain ($V_{SW} \sim V_{BOOT}$) and drives the gate of the HS switch Q1 through the HS gate driver. V_{SW} is the voltage at the switching node, while V_{BOOT} is generated by a bootstrap circuit consisting of a diode $\mathrm{D_{BOOT}}$ and a capacitor $\mathrm{C_{BOOT}}$, generating $V_{BOOT} = V_{SW} + V_{DD}$. Both V_{SW} and V_{BOOT} are at floating levels, i.e., their voltage levels change during the operation rather than a fixed level like a power supply rail.

During the operation when the LS control signal *LIUS_LS* is high (i.e., equal to V_{DD}) and the HS control signal *LIUS_HS* is low (i.e., equal to 0), the LS switch Q2 is turned on with a gate-source voltage of V_{DD} and connects the switching node to the ground.

The HS control scheme is more complicated because the gate and source terminals of the HS switch Q1 are at floating levels. When the HS control signal *LIUS_HS* goes high and the LS control signal *LIUS_LS* is low, the HS switch Q1 is turned on, pulling up the switching node voltage V_{SW} toward V_{PP} ($V_{SW} = 0$ at the beginning of changing). The bootstrap voltage V_{BOOT} increases accordingly such that V_{BOOT} is kept at $V_{SW} + V_{DD}$ during the operation to maintain a positive voltage for $\mathrm{V_{gs}}$ of Q1. In the end, V_{SW} has a maximum swing of $0 \sim V_{PP}$, while V_{BOOT} has a maximum swing of $V_{DD} \sim V_{PP} + V_{DD}$.

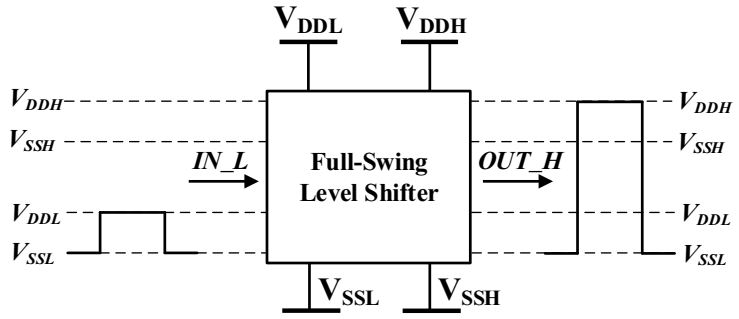
To reduce the conduction power loss caused by the on-resistance of the output switches, switches Q1 and Q2 need to be designed with a large width-to-length ratio. However, this increases the switching power loss. Therefore, the trade-off between the conduction power loss and the switching power loss needs to be considered to minimize the power dissipation of the half-bridge transducer driver. Furthermore, to prevent the shoot-through current from $\mathrm{V_{PP}}$ to the ground caused by the simultaneous conduction of Q1 and Q2, dead time between *LIUS_LS* and *LIUS_HS* is needed, as shown in Figure 3.2.

3.3 HV level shifter

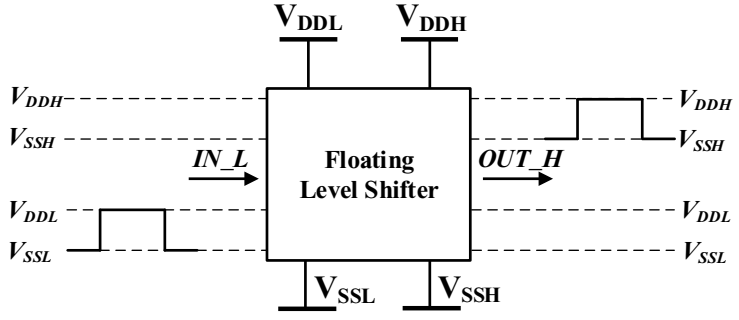
From the operation described above, we can see that the HV level shifter is an essential block of the half-bridge transducer driver shown in Figure 3.2. As

the communication bridge between different voltage domains, the performance of the HV level shifter affects the speed, power consumption, and robustness of the half-bridge circuit [46]. An HV level shifter with short propagation delay and low power consumption is proposed in this chapter for the high-performance operation of the half-bridge transducer driver shown in Figure 3.2.

Level shifters are categorized into two types: the full-swing level shifter and the floating level shifter. Figure 3.3 shows the level shifting behaviours of these two types of level shifters. The difference between these two level shifters is that the full-swing level shifter shown in Figure 3.3(a) is able to shift an input signal from $V_{SSL} \sim V_{DDL}$ to $V_{SSL} \sim V_{DDH}$, while the floating level shifter shown in Figure 3.3(b) elevates the input signal from $V_{SSL} \sim V_{DDL}$ to $V_{SSH} \sim V_{DDH}$. The HV level shifter in our works refers to the floating level shifter depicted in Figure 3.3(b).



(a)



(b)

Figure 3.3: The level shifting behaviour of (a) a full-swing level shifter, and (b) a floating level shifter (refered to as HV level shifter in our works). This figure is modified from [89].

3.3.1 Current research status

To sustain the high voltages in the circuit, most HV level shifters are implemented in HVCMOS processes with HV transistors, while researchers in [90], [91] presented a stacked-transistor structure, which is able to be implemented in LV standard CMOS processes. This has the advantage of decreasing the die area and process cost caused by HV devices. The stacked-transistor structure proposed in [90] is depicted in Figure 3.4. The operating principle is to use multiple layers of inverter stacks to sustain the high voltage V_{DDH}, so that the voltage across each device is lower than its breakdown voltage.

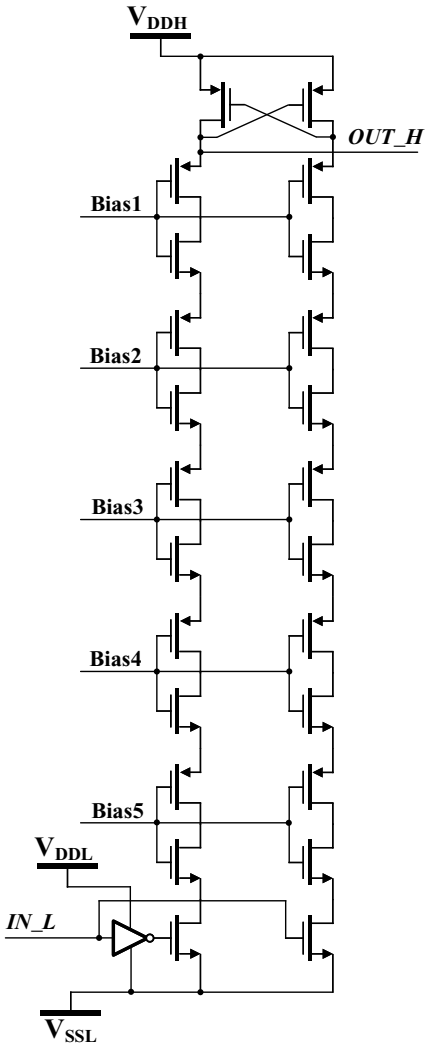


Figure 3.4: The stacked-transistor HV level shifter implemented in LV standard technologies (modified from [90]).

A disadvantage of the stacked-transistor HV level shifter is that it requires an extra bias voltage for each stack layer, for instance, Bias1∼Bias5 shown in Figure 3.4. This increases the circuit complexity and power consumption as additional circuits are needed to generate the bias voltages. Another drawback of the stacked-transistor HV level shifter is that the switching speed is limited due to the large propagation delay of the transistor stack. According to [90], the circuit in Figure 3.4 needs to operate at a frequency lower than 1 MHz. Moreover, more stack layers are needed to ensure the device reliability at higher V_{DDH}. This further increases circuit complexity, die area, and power consumption, and decreases the circuit switching speed. Therefore, for applications with a high V_{DDH} and requiring a high switching speed, such as our proposed LIUS system, the stacked-transistor structure in LV standard technologies is not desired, and HV level shifters implemented in HV processes are preferred.

For HV level shifters implemented in HVCMOS processes, most topologies are based on the structure proposed in [92], as depicted in Figure 3.5. Transistors M1 and M2 in Figure 3.5 are HVNMOS transistors, while transistors M3∼M6 are standard LV PMOS transistors. Note that HV transistors are indicated with different symbols than those used for LV transistors, i.e., as noted in Chapter 2, HV transistors are shown with two bars at the drain terminals.

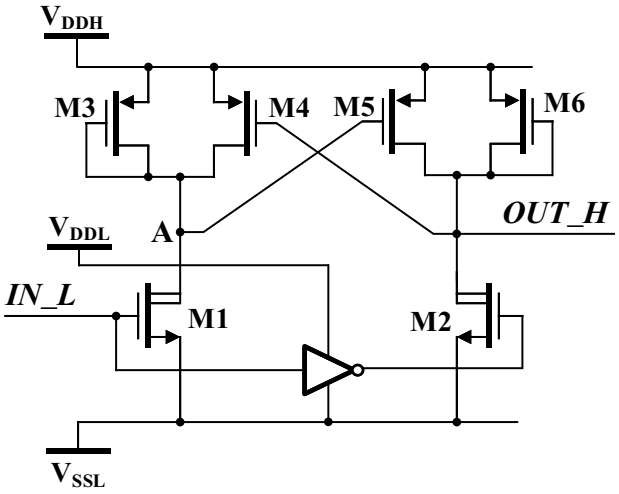


Figure 3.5: Conventional HV level shifter (modified from [92]).

For this circuit, when the input signal IN_L is high (has a voltage of V_{DDL}), HVNMOS M1 is turned on, while HVNMOS M2 is turned off due to the existence of the inverter. The on-state of M1 pulls down the voltage at node A. The diode-connected PMOS M3 is utilized to clamp the voltage at node A to be no lower than V_{SSH} ($V_{SSH} = V_{DDH} - V_{DDL}$) to prevent the source-drain breakdown of PMOS M3 and M4. The voltage at node A turns on PMOS M5 with a source-gate voltage of V_{DDL}. The on-state of M5 pulls up the output signal OUT_H to V_{DDH} (logic 1 in the HV domain), which is the same logic state as the input signal. Similarly, when the input signal is low, HVNMOS M2 is turned on, pulling down the output signal to V_{SSH} (logic 0 in the HV domain) with the clamp of the diode-connected PMOS transistor M6.

One major drawback of the HV level shifter shown in Figure 3.5 is that constant static current floating from V_{DDH} to V_{SSL} exists during the operation, either through M3 and M1 (when IN_L is high) or through M6 and M2 (when IN_L is low). This results in significant power consumption. To reduce this power consumption, different current limit strategies have been presented in [93]–[95]. For instance, the current limit enforced by a current mirror proposed in [95] is shown in Figure 3.6. As shown, a current mirror composed of M1 $\sim$ M4 is added. The diode-connected transistor M4 functions as the load transistor of the current mirror. Transistors M3 and M4 can be sized to limit their on-current to the micro-ampere or even nano-ampere level so as to limit the current going through M1 and M2. However, even though the power consumption is reduced with the current limit shown in Figure 3.6, static power consumption still exists due to the constant current (at a much lower level compared to that of Figure 3.5) floating from V_{DDL} to V_{SSL}, as well as from V_{DDH} to V_{SSL}.

To eliminate the static power consumption, a modified structure is shown in Figure 3.7. As shown, this circuit also uses a cross-coupled latch (consisting of M7 and M8), but without the diode-connected load. For its operation, when the input signal IN_L is high, NMOS transistor M1 is turned on pulling down voltage V_{D1} to V_{SSL}. This turns on M3 with a gate-source voltage of V_{DDL} and in turn pulls down the voltage V_{D3} to V_{SSL}. This then pulls down V_{S1}

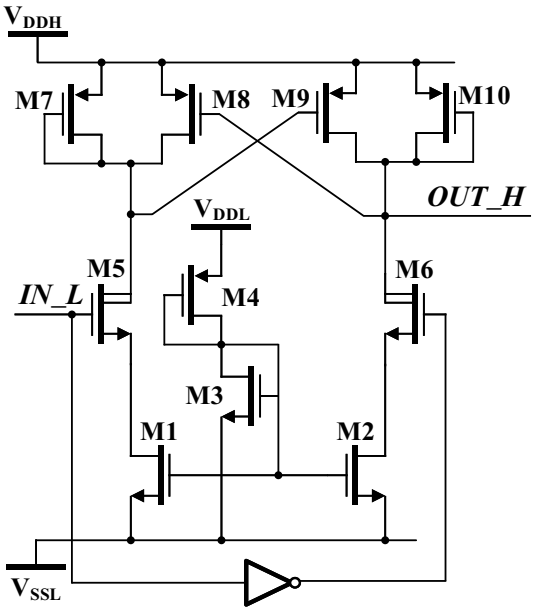


Figure 3.6: Conventional HV level shifter with current limit (modified from [95]).

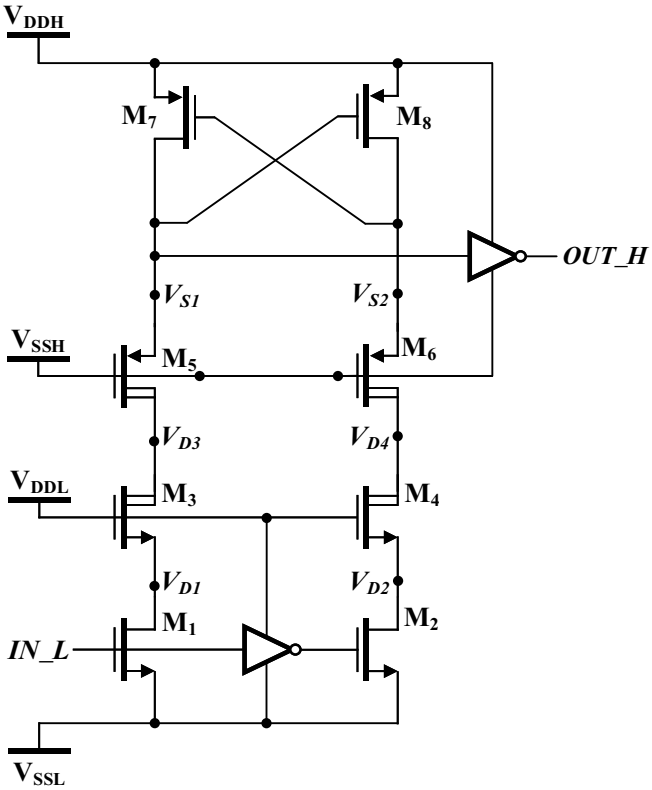


Figure 3.7: Conventional HV level shifter with no static power consumption (modified from [96]).

close to V_{SSH}, i.e., the floating ground of the HV domain. PMOS transistor M8 is turned on with its gate terminal connected to V_{SSH} and source terminal connected to V_{DDH}. The on-state of M8 pulls up voltage V_{S2} to V_{DDH}. The high voltage V_{S2} turns M7 off completely, avoiding static current flowing from V_{DDH} to V_{SSL} through M7, M5, M3 and M1. The circuit operation at the other phase when the input signal IN_L is low can also eliminate static power consumption, such that transistor M8 is turned off completely, cutting off the current path from V_{DDH} to V_{SSL} through M8, M6, M4, and M2.

We can conclude, from the operation described above, that the circuit shown in Figure 3.7 is free of static power consumption compared to the circuits in Figure 3.5, and Figure 3.6. However, there still exist several drawbacks. For instance, even though the gates of HVPMOS M5 and M6 are biased by V_{SSH} to prevent the voltages V_{S1} and V_{S2} from dropping below V_{SSH}, the leakages of M5 and M6 can still pull V_{S1} and V_{S2} down by several volts, weakening or destroying the gate oxides.

To further improve the performance of the HV level shifter shown in Figure 3.7, researchers in [96] proposed several improvement techniques. Figure 3.8 shows the "active clamping" HV level shifter proposed in [96]. In Figure 3.8, the HVNMOS transistors M1 and M2 are used directly as pull-downs rather than as cascodes in Figure 3.7 to save some die area. Additional transistors M7 and M8 are connected to actively pull down the voltages V_{S1} and V_{S2} to V_{SSH}. This speeds up the circuit dynamic operation. Transistors M7 and M8 also have the function of preventing voltages V_{S1} and V_{S2} from dropping below V_{SSH} caused by the leakage of M3 and M4.

One common disadvantage of the circuits in Figure 3.4 $\sim$ Figure 3.8 is that their switching is asymmetrical, which results in undesired signal skews. To explain this, we take the dynamic operation of the circuit in Figure 3.8 as an example. At the transition when the input signal IN_L goes high, the left branch triggers, and the voltage V_{S1} is pulled down to V_{SSH}. The voltage V_{S1} is fed into the input of an inverter and a clean logic high of the HV domain (V_{DDH}) is obtained for the output signal OUT_H. We can see that the change of the output signal during this transition depends mainly on the left branch

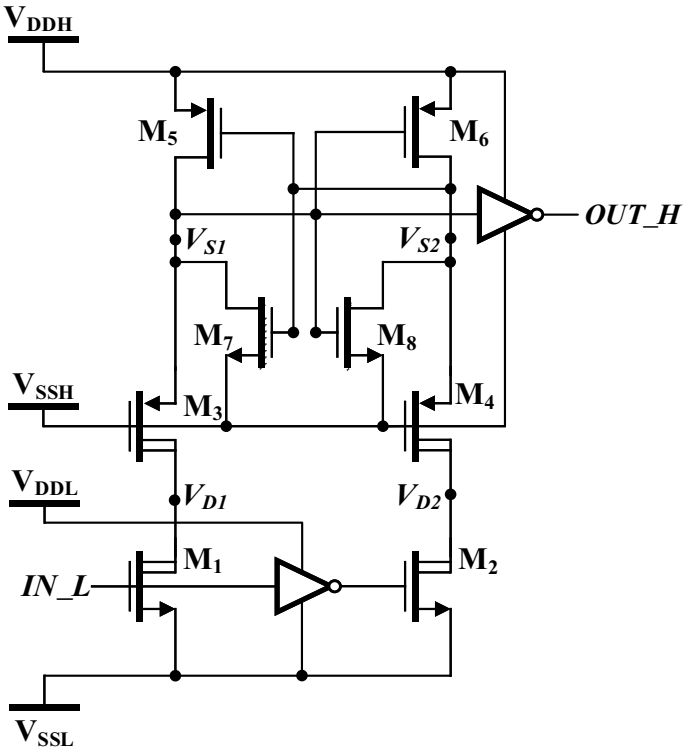


Figure 3.8: The "active clamping" HV level shifter proposed in [96].

of the circuit. At the other transition when the input signal IN_L goes low, the right branch triggers and pulls down the voltage V_{S2} to V_{SSH}. However, the voltage V_{S2} can not directly change the state of the output signal and extra steps are needed. Extra steps include turning on M5 and pulling up the voltage V_{S1} to V_{DDH}. Then the output signal OUT_H flips its state through the inverter operating at the HV domain. The change of the output signal at the second transition involves the actions of the right branch of the circuit as well as the left branch. We can see from the circuit dynamic operation that the switching of the output signal costs different time at the rising and falling edges of the input signal due to the extra steps introduced at the falling edge of the input signal. We refer to this phenomenon as asymmetrical switching. The asymmetrical switching problem introduces undesired signal skews to the input signal.

To illustrate the signal skew problem in detail, Figure 3.9 shows the input and output signals of an HV level shifter with or without signal skews.

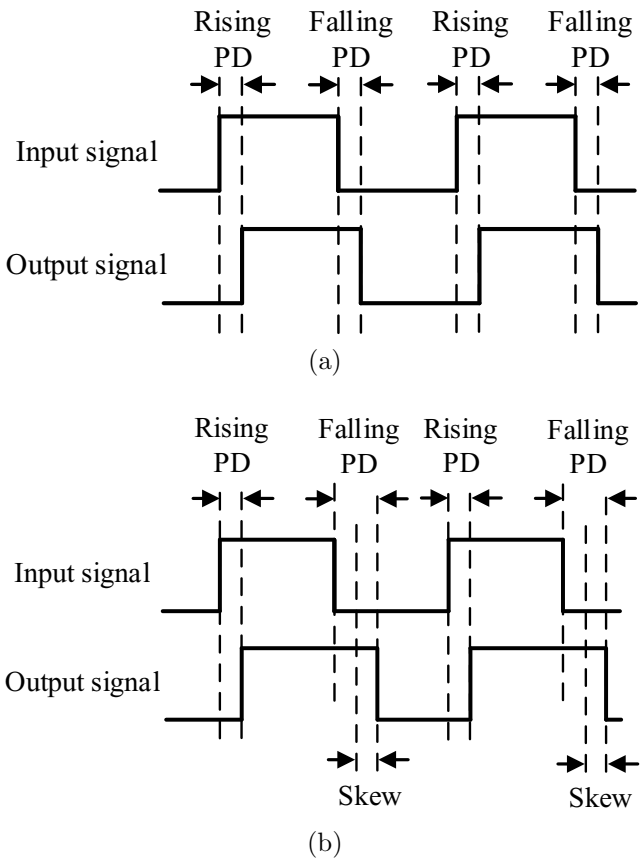


Figure 3.9: The input and output signals of an HV level shifter (a) with signal skews and (b) without signal skews.

For an HV level shifter without signal skews (Figure 3.9(a)), the propagation delays (PDs) between the input signal and the output signal are similar at the rising and falling edges of the input signal, and the signal integrity is maintained. For an HV level shifter with asymmetrical switching, signal skews are introduced. Its input and output signal waveforms are shown in Figure 3.9(b). As shown, the signal skew enlarges the propagation delay at the falling edge of the signal. What's worse, the pulse width of the output signal is increased compared to the input signal due to the existence of the signal skew. When applied to a half-bridge circuit, for example, the circuit shown in Figure 3.2, the increased pulse width could dissolve the dead time between the gate signals of Q1 and Q2, and result in large shoot-through current from V_{PP} to the ground. This problem gets more severe at high operation frequencies. Therefore, symmetrical switching of HV level shifters is needed to keep the

signal integrity of the input signal and ensure the high performance of the half-bridge driver.

To achieve symmetrical switching, a simple improvement was made in [96] based on the circuit in Figure 3.8. Figure 3.10 demonstrates the improved HV level shifter with symmetrical switching (referred to as the "fast" mode HV level shifter in [96]). The disadvantage of asymmetrical switching in Figure 3.8 is overcome by the addition of custom inverters and a NAND gate latch in the HV domain in Figure 3.10. The first-stage inverters are sized to be sensitive to the initial dip in the source voltages of M3 and M4 to speed up the circuit dynamic operation. The two-stage inverters also function as buffers to increase the pulling strength (using low-impedance path) of the source voltages of M3 and M4. The NAND gate latch delays switching until both branches of the level shifter have changed state. The addition of the extra gates in the HV domain achieves symmetrical switching and ensures the signal integrity of the input signal.

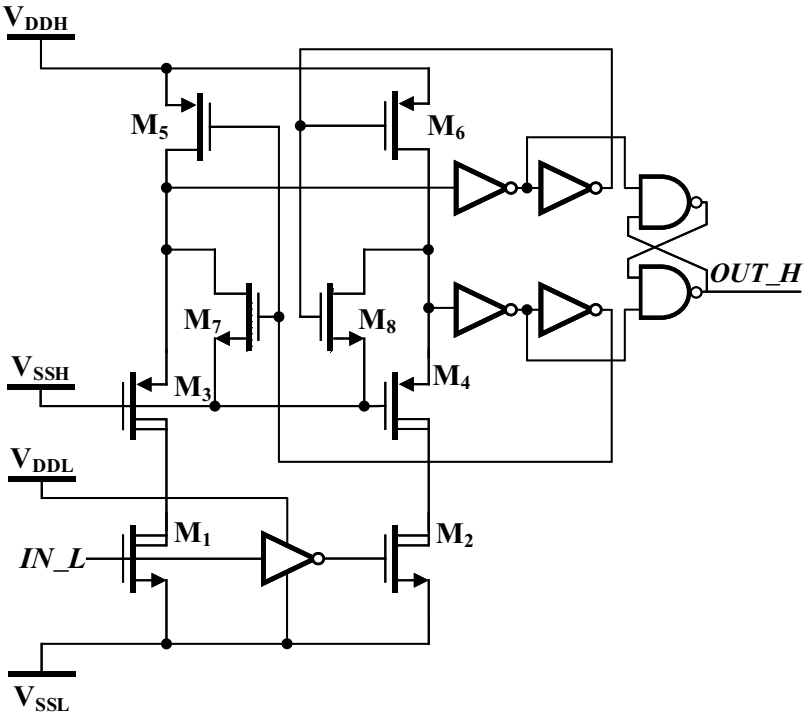


Figure 3.10: The "fast" mode HV level shifter proposed in [96].

The HV level shifter in Figure 3.10 is a level-triggered design, meaning that the gate signals of M1 and M2 in Figure 3.10 need to be kept low or high in order to maintain the state of the output signal. The HV level shifters in Figure 3.4 $\sim$ Figure 3.8 are also level-triggered designs. Compared to the pulse-triggered designs (circuits in Figure 3.11 and Figure 3.12), the circuit speed and power performance of level-triggered designs are less efficient [97]. The reason is that for the pulse-triggered designs, for instance in Figure 3.11, only pulses at the rising and falling edges of the input signal are needed to charge the gates of HNM1 and HNM2 to flip and maintain the state of the output signal. This is more efficient as power is mainly consumed during the short triggering pulses so that a low average power dissipation can be easily achieved.

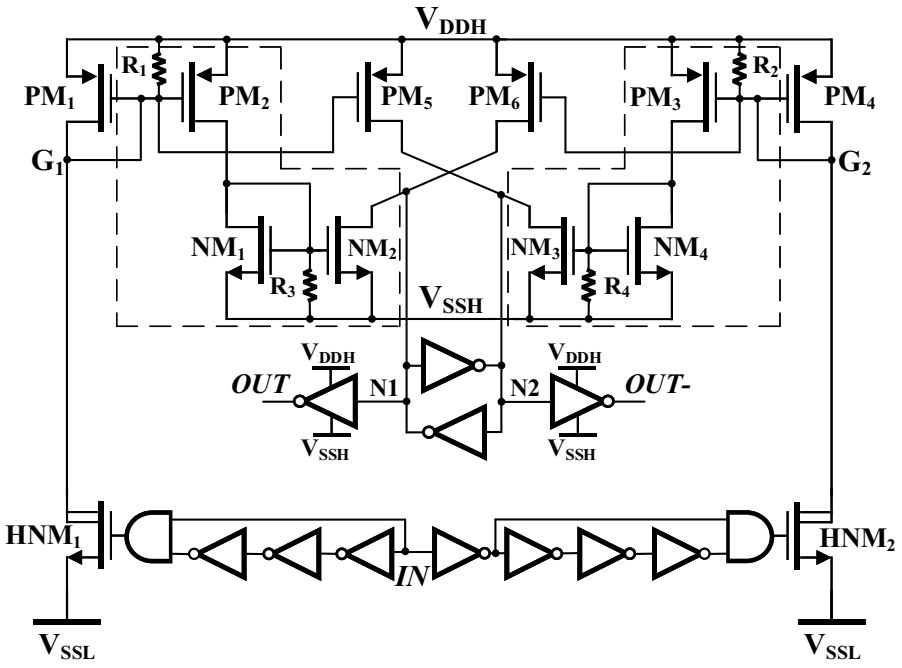


Figure 3.11: The "optimized" HV level shifter in [97].

For the operation of the circuit shown in Figure 3.11, a pulse generator is used to generate the pulses at the rising and falling edges of the input signal. At the rising edge, the left branch triggers with HVNMOS HNM1 turned on. Transistor PM5 mirrors the current through PM1 and pulls up the voltage at node N2. A latch composed of two inverters latches the voltages at the nodes

N1 and N2 to be V_{SSH} and V_{DDH}, respectively. These two voltage levels were held by the inverter latch after HNM1 is turned off. The output signal OUT switches its state from low to high during this transition and is held high after the transition. The circuit operation at the falling edge of the input signal features a similar principle, such that the right branch triggers and the output signal OUT flips from high to low.

One disadvantage of the pulse-triggered design in Figure 3.11 is that it has relatively high circuit complexity with the use of two additional circuit blocks (as indicated by the dashed boxes) to avoid asymmetrical switching and current mirror mismatch. Another drawback is the use of relatively bulky on-chip resistors. Their values cannot be accurately controlled and they could increase the die area depending on their values and the fabrication process.

Figure 3.12 shows another pulse-triggered HV level shifter. It also exhibits high circuit complexity where diode stacks connecting V_{DDH} to V_{Da3} and V_{Da4} are needed to provide extra current paths for transistors Ma7 and Ma8. Furthermore, an additional bias voltage higher than V_{SSH} is required for the gates of Ma3 and Ma4, in order to protect the LV transistors in the HV domain.

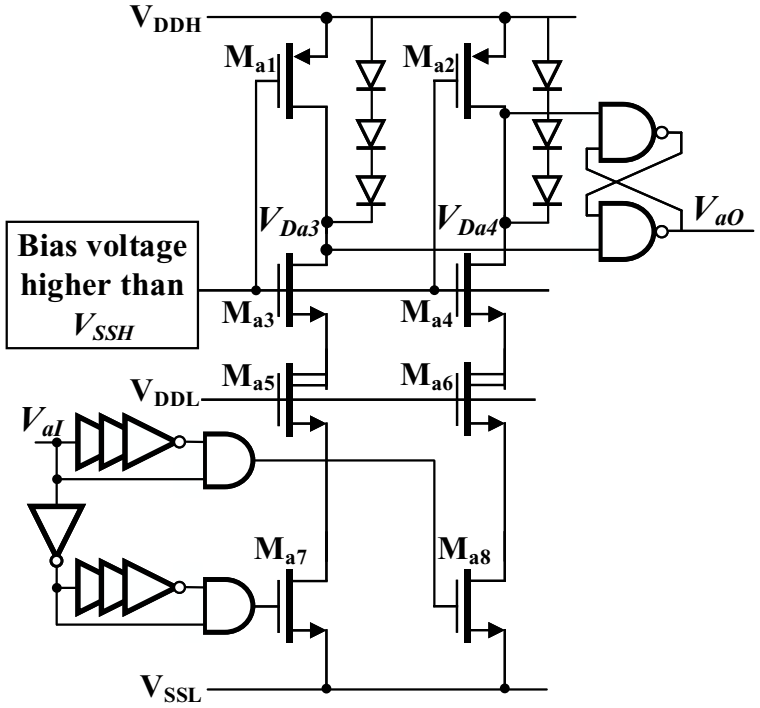


Figure 3.12: The fast low-power HV level shifter in [98].

In this chapter, we propose a simple HV level shifter based on Figure 3.10 [96] but with a pulse-triggering approach. The pulse-triggering approach effectively reduces the power dissipation and propagation delay of the original design in Figure 3.10. Furthermore, the proposed HV level shifter has less circuit complexity and occupies less die area compared to the pulse-triggered designs shown in Figure 3.11 and Figure 3.12, without the use of on-chip resistors and diode stacks.

3.3.2 Proposed HV level shifter

Figure 3.13 shows the proposed pulse-triggered HV level shifter. Referring to the transducer driver shown in Figure 3.2, the input signal *IN_L* of the HV level shifter is the same signal as *LIUS_HS* shown in Figure 3.2, while the output signal *OUT_H* of the HV level shifter is the signal at node A in Figure 3.2. The voltage levels V_{SSL}, V_{DDL}, V_{SSH}, and V_{DDH} of the HV level shifter are equal to the voltage levels 0, V_{DD}, V_{SW}, and V_{BOOT} of the transducer driver shown in Figure 3.2, respectively. Same as V_{SW} and V_{BOOT}, voltages V_{SSH} and V_{DDH} are at floating levels.

As shown in Figure 3.13, the proposed HV level shifter circuit is composed of three main blocks: signal edge detection, level shifting, and latching. The edge detection block is used to generate pulses at the rising and falling edges of the input signal. It operates in the LV domain with a range of $V_{SSL} \sim V_{DDL}$. The level-shifting block elevates the signals from the LV domain to the floating HV domain ($V_{SSH} \sim V_{DDH}$). As shown, the level shifting block has two identical branches, one consisting of transistors M1, M3, and M5, and the other involving transistors M2, M4, and M6. On each transition, only one branch triggers. The latching block in Figure 3.13 stores and flips the state of the output signal *OUT_H*. This block works in the HV domain floating between V_{SSH} and V_{DDH}.

Transistors M1 (or M2) and M3 (or M4) in Figure 3.13 are HVNMOS and HVPMOS transistors, respectively. They offer high breakdown voltage across the drain and source terminals with low breakdown voltage across the gate and source terminals. All other transistors in Figure 3.13 are LV standard

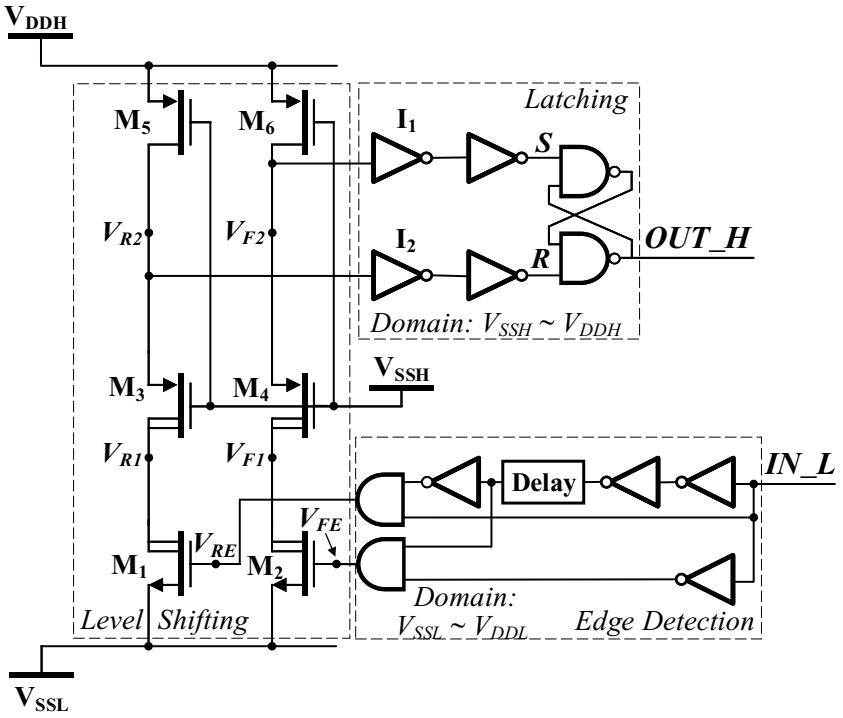


Figure 3.13: Circuit topology of the proposed HV level shifter.

transistors. Many modern HV processes provide N+ buried layers and N+ isolation rings, etc. as junction isolation for HV and LV transistors. Transistors operating in different voltage domains need to be placed in different isolation N-wells. For the proposed level shifter, HVNMOS devices M1 and M2 each have their own isolation N-well, while HVPMOS devices M3 and M4 may have their own isolation wells or may share one well depending on the process. LV transistors M5 and M6 and the transistors in the latching block share one isolation well because they all operate in the HV domain. The transistors in the edge detection block, which operate in the LV domain, share another isolation well.

DC Operation

In steady state, the input signal *IN_L* is at stable low or high, no pulses are produced at V_{RE} and V_{FE} in the edge detection block (RE stands for rising edge and FE stands for falling edge). Therefore both M1 and M2 are off. As M5 and M6 in the level-shifting block are permanently turned on by having their gates

connected to V_{SSH}, the voltages V_{R2} and V_{F2} (voltages at the drain terminals of M5 and M6, respectively) are both pulled up to V_{DDH} (neglecting the on-state voltage drop across the source-drain terminals). These two signals flow into the latching block, representing a high state for the set and reset signals of the NAND gate latch. As a result, the output signal OUT_H remains in its latched state. This is the same state as the input signal, as will be explained later in the circuit dynamic operation.

The HVPMOS transistors M3 and M4 are both on during DC operation with a source-to-gate voltage of $V_{DDH} - V_{SSH}$. Consequently, voltages V_{R1} and V_{F1} (voltages at the drain terminals of M3 and M4, respectively) follow V_{R2} and V_{F2} and are pulled up to V_{DDH}. Transistors M1 and M2 need to tolerate a V_{DDH} voltage drop across their drain-source terminals. For this reason, HVNMOS transistors are used for M1 and M2.

Dynamic Operation

To explain the circuit dynamic operation, the operation waveforms of the proposed level shifter are depicted in Figure 3.14. When IN_L changes from low to high, a rising edge is detected and a pulse is produced at V_{RE} (the delay caused by the edge detection block is indicated by t_1 in Figure 3.14). The short pulse at V_{RE} charges up the gate of M1 and turns it on. If the pull-down strength of M1 is stronger than the pull-up strength of M3 and M5, the voltage V_{R1} will be pulled down close to V_{SSL}. The delay of this transition is t_2 as indicated in Figure 3.14. The low voltage V_{R1} in turn quickly pulls down V_{R2} close to V_{SSH} through M3 with a delay of t_3. As V_{F2} remains at V_{DDH} during this transition, the two-stage inverters at the latching block transfers this information as $S = 1$ and $R = 0$ to the NAND gate latch. This flips the state of the output signal OUT_H from low to high, which is the same transition as the input signal. The delay caused by the latching block is indicated by t_4 in Figure 3.14. After V_{RE} goes back to low and turns M1 off, no pull-down strength exists such that M5 and M3 pull up V_{R2} and V_{R1} back to V_{DDH}. The output signal OUT_H is held high by the NAND gate latch.

The transition at the falling edge of IN_L operates in a similar way such

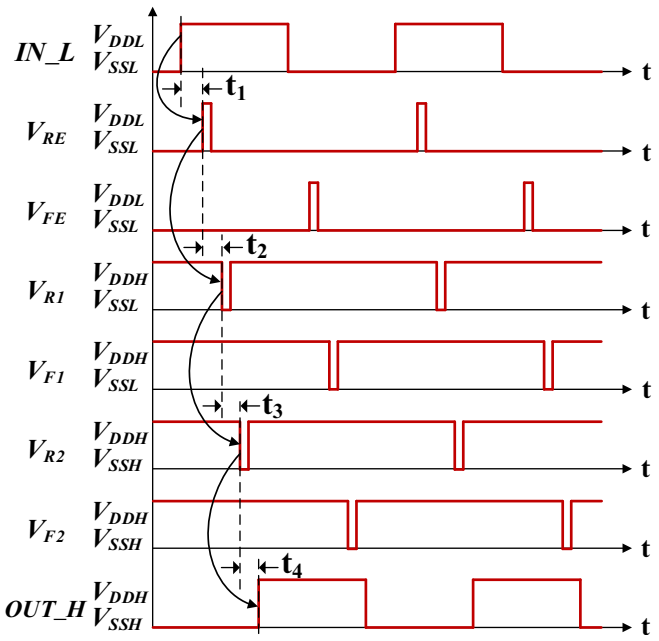


Figure 3.14: Operation waveforms of the proposed HV level shifter.

that M2 is turned on with a short pulse of V_{FE}. V_{F1} is pulled down close to V_{SSL}. V_{F2} follows V_{F1} while remaining above V_{SSH} with the protection of M4. Signals $S = 0$ and $R = 1$ are transferred to the NAND gate latch and changes the state of the output signal OUT_H from high to low, which is in the same manner as the input signal IN_L. The output signal OUT_H is then latched low after V_{FE} goes back to V_{SSL}. The delay between the change of IN_L and OUT_H at the falling edge is also similar to that at the rising edge.

The operation described above shows that with the use of the NAND gate latch, the output signal switches in the same manner when it is triggered by the rising and the falling edges of the input signal, making the switching fully symmetrical. HVPMOS transistors M3 and M4 prevent voltages V_{R2} and V_{F2} from decreasing beyond V_{SSH} during the operation. This is crucial for protecting the transistors sitting between the V_{SSH} and V_{DDH} rails as well as ensuring the reliability of the MOS gate for M3 and M4. The leakage of HVPMOS transistors M3 and M4 can be neglected for the proposed circuit as each branch is only triggered for a short period time. As the voltage swing at V_{R1} and V_{F1} is from V_{SSL} to V_{DDH}, M3 and M4 must be HVPMOS transistors to avoid source-drain breakdown.

Design Considerations

Adequate pulse width in the edge detection block is needed for V_{RE} and V_{FE} to trigger the branches in the level-shifting block and flip the state of the latching block over all process corners. The edge detection block also needs to be carefully designed to guarantee similar time delays from the input signal *IN_L* to V_{RE} and V_{FE}. The sizes of transistors M1∼M6 in the level-shifting block must be chosen carefully to ensure proper dynamic operation. Voltages V_{R2} and V_{F2} must be pulled down close to V_{SSH} to exhibit a clear low-state signal for the first-stage inverters in the latching block. The first-stage inverters I1 and I2 in the latching block are designed with strong PMOS and weak NMOS transistors to make it sensitive to the initial dip of V_{R2} and V_{F2}. The second-stage inverters in the latching block then present accurate and clean signal transitions to the inputs of the NAND gate latch.

Consider the branch composed of M1, M3, and M5 as an example. In order to pull V_{R2} down close to V_{SSH}, the pull-down strength provided by M1 and M3 needs to be stronger than the pull-up strength of M5 when the branch is triggered. As transistors M1 and M3 are HVMOS devices which generally have low on-resistance, the minimum sizes allowed by the fabrication technology are sufficient to provide enough pull-down strength. Weakening the pull-up strength of M5 allows a faster drop at V_{R2}, leading to shorter propagation delay. However, it requires longer recovery time for V_{R2} to be pulled back to V_{DDH} and consequently limits the maximum operating frequency of the level shifter. On the other hand, it is not necessary to pull V_{R1} all the way down to V_{SSL} in order to pull V_{R2} close to V_{SSH}. Lowering the voltage swing at V_{R1} by enhancing the pull-up strength of M5 has the advantage of reduced power consumption. In other words, the sizing of M5 is a trade-off between the propagation delay, the power consumption, and the maximum operating frequency.

Compared to the level-triggered HV level shifter shown in Figure 3.10, the pulse-triggering approach of the proposed circuit leads to shorter propagation delay. This is because the switching of the output signal of the circuit in Figure

3.10 relies on the toggling of both branches due to its cross-coupled topology, while the proposed circuit only requires the toggling of one branch to flip the state of the output signal. Besides, the proposed circuit has reduced power dissipation due to the fast dynamic operation compared to that in Figure 3.10. Compared to the pulse-triggered designs in Figure 3.11 and Figure 3.12, the proposed HV level shifter has much less circuit complexity and occupies smaller die area without the use of on-chip resistors and diode stacks.

3.3.3 Simulation and measurement results

The proposed HV level shifter is implemented in TSMC's 0.18-µm BCD Gen2 process. The LV devices are 5-V standard transistors and the HV devices are 20-V HVMOS transistors. The 20-V HVNMOS devices can tolerate a 20-V drain-source (or source-drain for HVPMOS) voltage and a 5-V gate-source (or source-gate for HVPMOS) voltage. Table 3.1 shows the transistor sizes of the proposed HV level shifter. HV devices M1∼M4 are at their minimum sizes. The sizes of M5 and M6 are chosen based on minimizing the propagation delay × the power consumption product. The first-stage inverters I1 and I2 of the latching block in Figure 3.13 are designed with strong PMOS and weak NMOS transistors to make it sensitive to the initial dip of V_{R2} and V_{F2}.

Table 3.1: Transistor sizes of the proposed HV level shifter.

Transistor	Type	W / L (µm / µm)
M1, M2	20 V HVNMOS	10 / 1.6
M3, M4	20 V HVPMOS	10 / 0.4
M5, M6	5 V PMOS	1 / 0.5
PMOS in inverters I1 and I2	5 V PMOS	5 / 0.5
NMOS in inverters I1 and I2	5 V NMOS	0.22 / 0.6

Figure 3.15 shows the micrograph of the fabricated IC with each block of the proposed HV level shifter indicated. Since the output signal of the HV level shifter doesn't have enough drive strength to drive the I/O pad directly, an output buffer with ×64 drive strength is added to the output of the HV level shifter to provide sufficient drive capability for testing purposes. The

output buffer operates in the HV domain and shares the same isolation N-well with the latching block of the HV level shifter. The total silicon area of the test chip is 0.018 mm^2 (the area occupied by the HV level shifter itself is 0.012 mm^2).

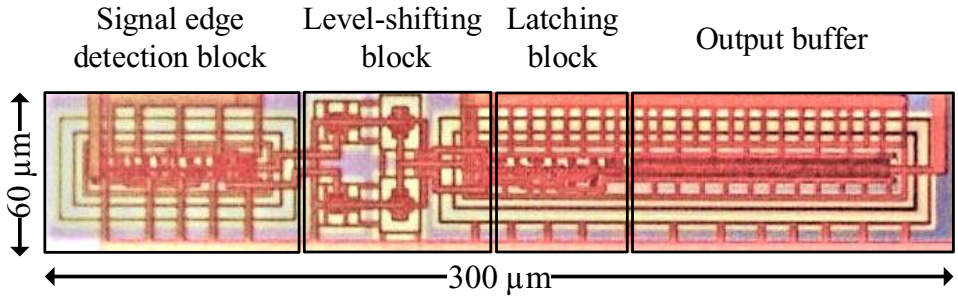


Figure 3.15: Micrograph of the test chip (consisting of the HV level shifter circuit and the output buffer with total area: 0.018 mm^2).

Figure 3.16 shows the measurement setup for the test chip. The input signal is generated externally with a signal generator passing through a Schmitt trigger. The probes of the oscilloscope are connected to the input and the output of the test chip. Input signals with a frequency of 10 MHz are tested.

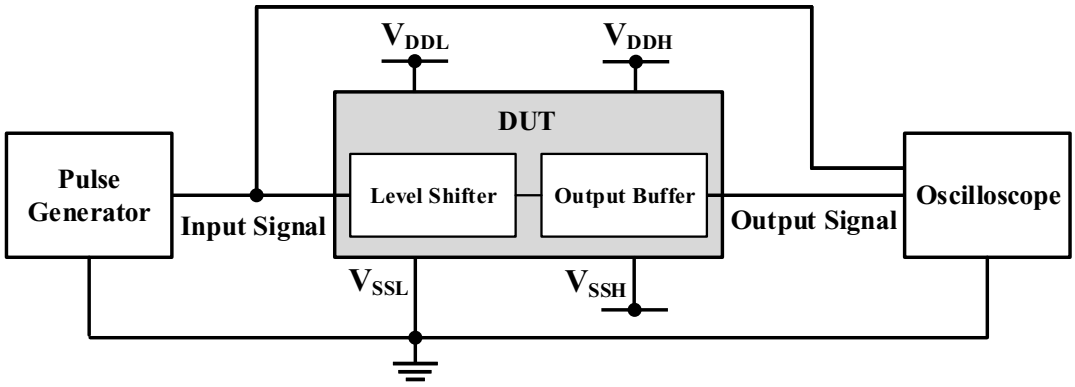


Figure 3.16: Measurement setup.

Figure 3.17 demonstrates the measured input and output waveforms of the test chip at $V_{DDH} = 20$ V, $V_{SSH} = 15$ V, and $V_{DDL} = 5$ V. The voltage ringing at the input and output signals in Figure 3.17 are caused by the parasitic inductance and capacitance from the packages and the PCB. The propagation delay t_p between the input signal and the output signal of the test chip (including the delay from both the HV level shifter circuit and the output buffer)

is 3.51 ns. Subtracting the post-layout simulated delay caused by the output buffer (2.75 ns), it can be deduced that the propagation delay of the proposed HV level shifter is 0.76 ns.

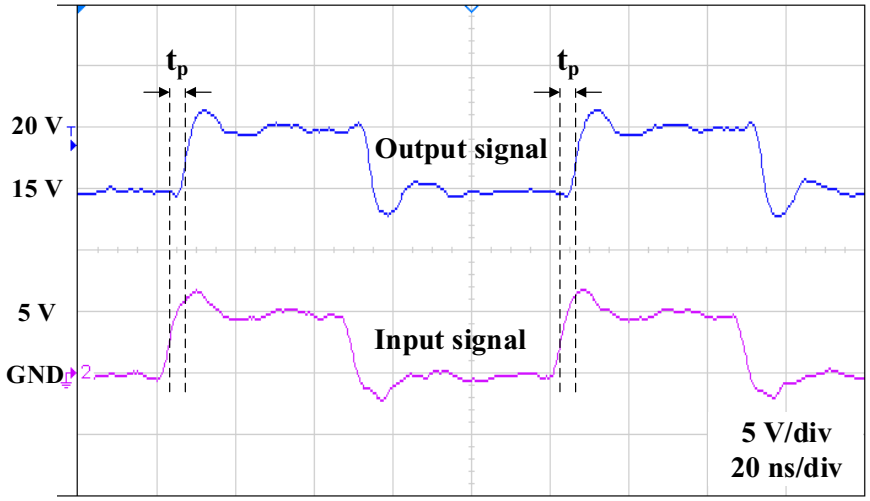


Figure 3.17: Measured input and output waveforms of the test chip at V_{DDH} = 20 V, V_{SSH} = 15 V, and V_{DDL} = 5 V.

Post-layout simulated and measured propagation delay of the proposed HV level shifter at V_{DDL} = 5 V are shown in Figure 3.18. V_{DDL} is fixed at 5 V. V_{DDH} was swept from 5 V to 20 V while keeping $V_{DDH} - V_{SSH}$ = 5 V fixed (the voltage swing of V_{SSH} is $0 \sim 15$ V). The measurement results were obtained by using the measured propagation delay of the test chip (consisting of both the HV level shifter circuit and the output buffer) subtracting the post-layout simulated propagation delay of the output buffer. Both the post-layout simulated and the measured results were evaluated at the rising edge of the input signal. It can be seen from Figure 3.18 that the measured results are in close agreement with the post-layout simulated results. They both show a tendency that the propagation delay slowly decreases as V_{DDH} increases. This is because the node voltages V_{R2} and V_{F2} in the level-shifting block discharge faster at higher V_{DDH}, which leads to a faster response of the circuit. At V_{DDH} = 20 V (V_{SSH} = 15 V accordingly), the measured results show a propagation delay of 0.76 ns. When V_{DDH} is swept from 5 V to 20 V, V_{SSH} is swept from 0 to 15 V, accordingly. The proposed HV level shifter is able to keep the propagation delay in sub-nanosecond range for all V_{DDH} conditions.

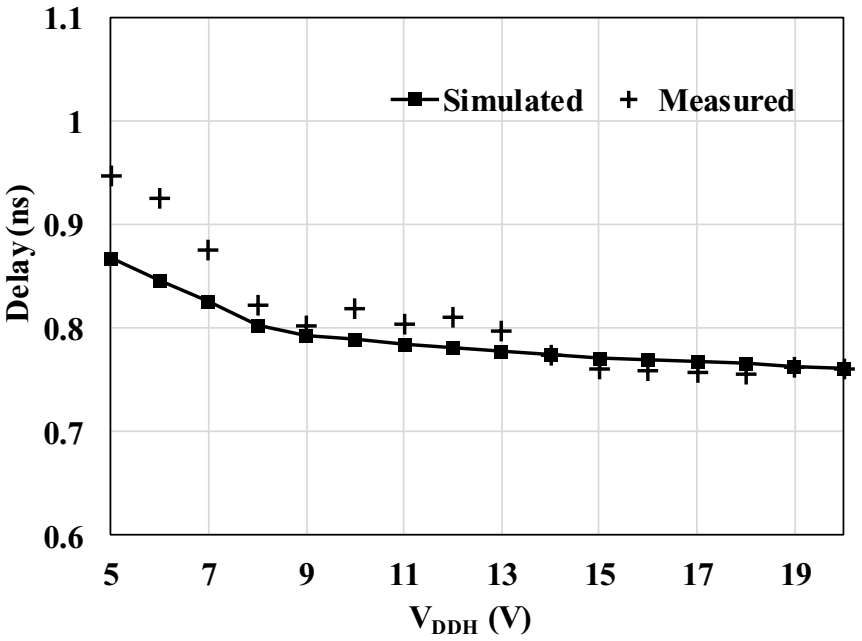


Figure 3.18: Post-layout simulated and measured propagation delay of the proposed HV level shifter at V_{DDL} = 5 V. V_{DDH} is swept from 5 V to 20 V while keeping $V_{DDH} - V_{SSH}$ = 5 V fixed.

The propagation delay of the proposed HV level shifter is also evaluated with 3.3 V input signals. Figure 3.19 depicts the post-layout simulated and measured propagation delay at V_{DDL} = 3.3 V. As shown, the measured propagation delay correlates closely with the post-layout simulated results, both showing a slow decline as V_{DDH} increases. Compared to the results at V_{DDL} = 5 V shown in Figure 3.18, the propagation delay at V_{DDL} = 3.3 V is larger at the same V_{DDH}. The reason is that a higher input voltage provides faster charging for gate capacitors of M1 and M2, leading to a faster transition of the level-shifting block.

As power consumption is highly frequency-dependent, the energy consumption per transition (EPT) is examined to evaluate the power consumption of the proposed HV level shifter. Figure 3.20 shows the post-layout simulated EPT of the proposed HV level shifter for both V_{DDL} = 5 V and V_{DDL} = 3.3 V. The EPT of the fabricated HV level shifter cannot be measured because the power consumed at the output buffer and the I/O pads of the test chip is much higher than that of the HV level shifter circuit. As shown in Figure 3.20,

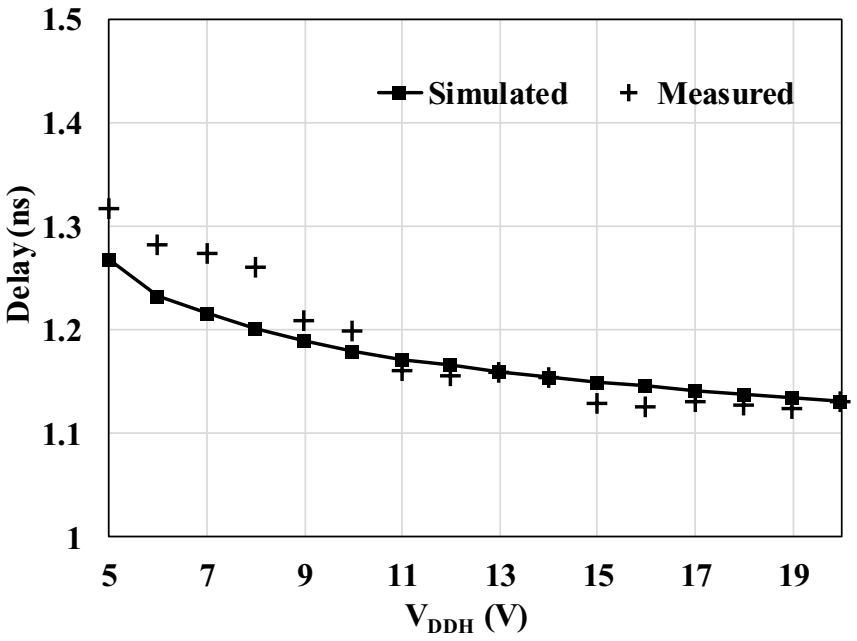


Figure 3.19: Post-layout simulated and measured propagation delay of the proposed HV level shifter at $V_{DDL} = 3.3$ V. V_{DDH} is swept from 5 V to 20 V while keeping $V_{DDH} - V_{SSH} = 3.3$ V fixed.

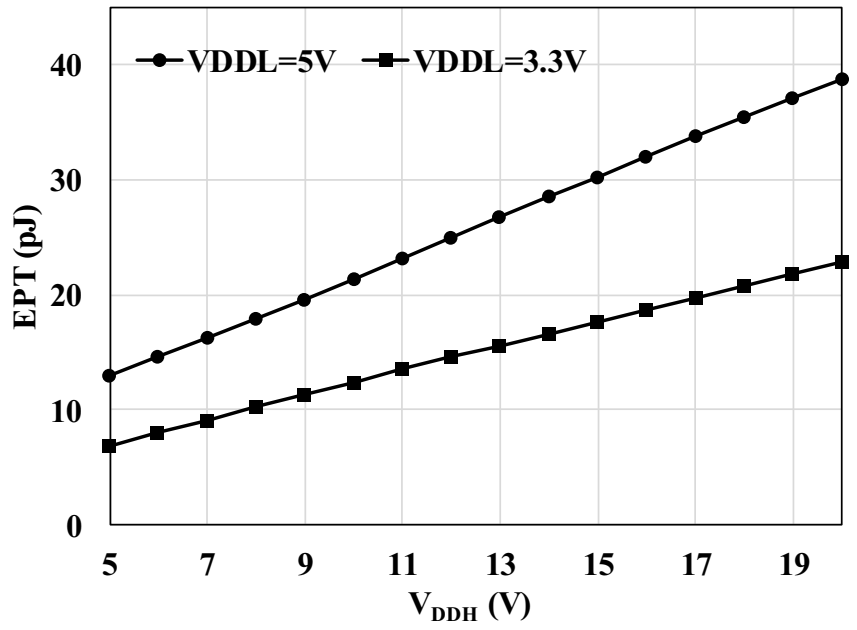


Figure 3.20: Post-layout simulated EPT of the proposed HV level shifter at both $V_{DDL} = 5$ V and $V_{DDL} = 3.3$ V. V_{DDH} is swept from 5 V to 20 V while keeping $V_{DDH} - V_{SSH} = V_{DDL}$ fixed.

the EPT at both V_{DDL} = 5 V and V_{DDL} = 3.3 V grows linearly with V_{DDH}. This is mainly contributed by the linear increase in the power dissipation of the level-shifting block. Figure 3.20 also shows that the EPT at V_{DDL} = 5 V is higher than that at V_{DDL} = 3.3 V for all V_{DDH} conditions. This indicates that lowering the input voltage can effectively decrease the circuit power dissipation.

To compare the proposed HV level shifter with other circuits that consume no static power consumption and has symmetrical switching, i.e., the circuits shown in Figure 3.10 $\sim$ Figure 3.12, we implemented and simulated these circuits using the same process as the proposed circuit with the same LV and HV devices. The circuits in Figure 3.10 $\sim$ Figure 3.12 are all designed and optimized to achieve the minimum Propagation Delay $\times$ EPT product at V_{DDL}=5 V and V_{DDH} = 20V. Layouts of the circuits were also completed as well as the post-layout simulation. Table 3.2 compares the propagation delay, the EPT, and the silicon area of the proposed circuit and the circuits in Figure 3.10 $\sim$ Figure 3.12.

Table 3.2: Comparison with the HV level shifters shown in Figures 3.10 $\sim$ 3.12 (all circuits are implemented in the same process with the same LV and HV devices).

Parameters	Circuit in Figure 3.10	Circuit in Figure 3.11	Circuit in Figure 3.12	Proposed design
V_{DDL} (V)	5			
V_{DDH} (V)	20			
Propagation Delay (ns)	4.1	0.79	0.91	0.76
EPT (pJ)	85	54	49	39
Area (mm^2)	0.0068	0.028	0.024	0.012

As shown in Table 3.2, the proposed circuit has both the shortest propagation delay and the lowest EPT compared with other circuits. The speed of the circuit in Figure 3.11 is similar to that of the proposed circuit. However, it's power consumption is higher. The main power consumption of the proposed

circuit and the circuit in Figure 3.11 both come from their triggering branches. For example, HNM1 and PM1 for the circuit in Figure 3.11, and M1, M3 and M5 for the proposed circuit. The circuit in Figure 3.11 has a smaller equivalent resistance in its branch when triggered because only one HVMOS device (low on-resistance) is used in each branch. Consequently, the power dissipation of the circuit in Figure 3.11 is higher than that of the proposed circuit at the same V_{DDH}.

According to Table 3.2, the silicon area occupied by the circuit in Figure 3.11 is the largest. This is due to the use of on-chip resistors. The circuit in Figure 3.12 also suffers from area penalty with the use of diode stacks. The proposed circuit is area-efficient compared to the circuits in Figure 3.11 and Figure 3.12 because it only utilizes LV and HV devices. The circuit in Figure 3.10 has the smallest silicon area as it is a level-triggered design and no pulse-generation block is needed at the rising and falling edges of the input signal, which saves more die area compared to the proposed circuit.

3.4 Conclusion

In this chapter, models of PZT transducers are discussed, including the BVD model and the simplified model at the resonance frequency. An on-chip half-bridge transducer driver is presented to drive the PZT transducer. The half-bridge driver structure is used due to its capability of wide-bandwidth switching with a compact design. To enable the high-performance operation of the half-bridge transducer driver, an HV level shifter with short propagation delay and low power consumption is proposed.

The proposed HV level shifter is designed, simulated, fabricated and tested using TSMC's 0.18-µm BCD Gen2 process. Measurement results show that it is able to elevate a 0-5 V signal (V_{SSL} = 0, V_{DDL} = 5 V) to 15-20 V (V_{SSH} = 15 V, V_{DDH} = 20 V) with a propagation delay of 0.76 ns. When V_{DDH} is swept from 5 V to 20 V (V_{SSH} is swept from 0 to 15 V, accordingly), the proposed level shifter is able to keep the propagation delay in sub-nanosecond range for all V_{DDH} conditions. The proposed HV level shifter is area-efficient

without the use of on-chip capacitors and resistors. Additional advantages are its low power consumption and fully symmetrical switching. Compared with other HV level shifters implemented in the same process, the proposed circuit has the shortest propagation delay and the lowest power consumption. The proposed HV level shifter enables the high-performance operation of the half-bridge transducer driver.

Chapter 4

Highly-Integrated LIUS Systems

4.1 A proof-of-concept miniaturized LIUS device

Based on the charge pumps proposed in Chapter 2 and the half-bridge transducer driver presented in Chapter 3, a proof-of-concept miniaturized LIUS device is developed. Figure 4.1 shows the system architecture of the miniaturized LIUS device. The system architecture is in accordance with the system block diagram shown in Figure 1.2 but with more detail. As shown in Figure 4.1, the miniaturized LIUS device consists of a battery, a custom Application-Specific Integrated Circuit (ASIC), an off-chip digital control block, and a PZT transducer. The battery is used as the power supply of the system. It is a lithium-ion battery with a nominal voltage of 3.7 V. The PZT transducer is used as the load. It is a customized PZT transducer manufactured by APC International, Ltd.

In the ASIC design, a half-bridge transducer driver is used to drive the PZT transducer to generate ultrasound. The output of the half-bridge transducer driver is V_{SW}, which is equals the voltage that is applied across the PZT transducer. An internal bootstrap circuit, consisting of a diode D_{BOOT} and a capacitor C_{BOOT}, is used to generate the bootstrap voltage V_{BOOT} for the high-side operation of the half-bridge transducer driver. The other block in the custom ASIC is a DC-DC boost converter, which consists of a charge pump

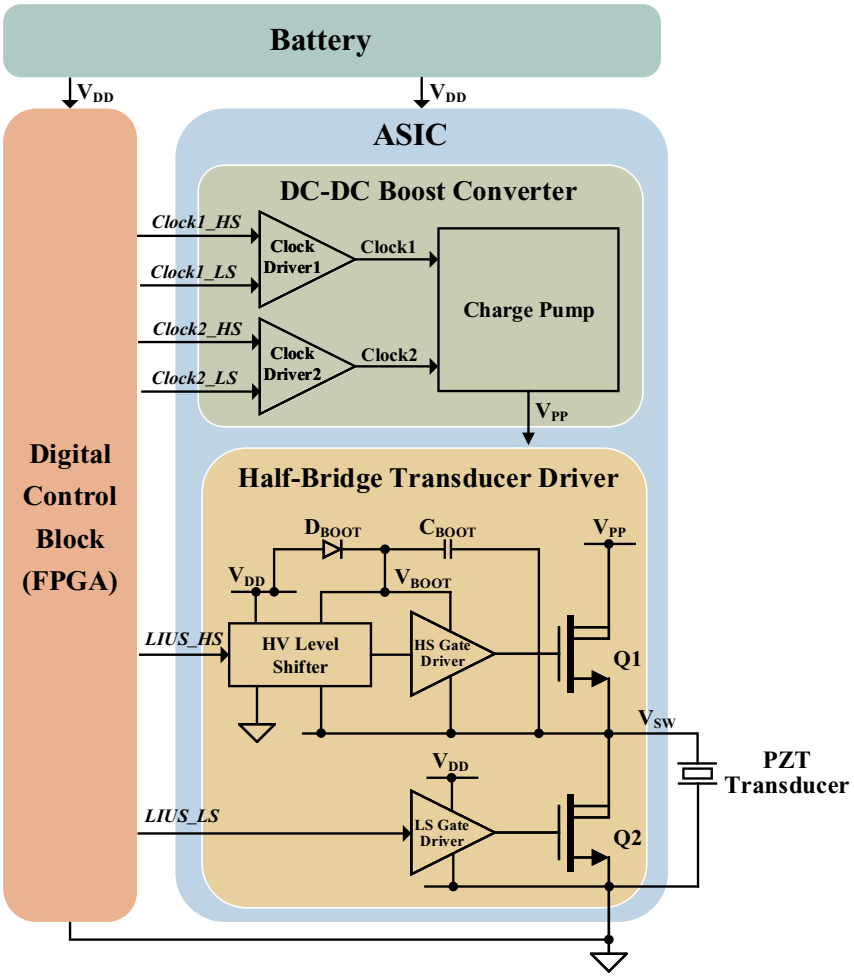


Figure 4.1: System architecture of the miniaturized LIUS device.

and two clock drivers. The DC-DC boost converter is used to generate the high voltage V_{PP} needed by the transducer driver to interface with the PZT transducer. The custom ASIC is implemented in TSMC's 0.18-µm BCD Gen2 process.

In this prototype, digital control signals for the ASIC are generated by the digital control block with an FPGA. The control signals generated by the digital control block include *Clock1_HS*, *Clock1_LS*, *Clock2_HS*, and *Clock2_LS* for the clock drivers in the DC-DC boost converter, and the control signals *LIUS_HS* and *LIUS_LS* for the half-bridge transducer driver. The waveforms of the control signals are shown in Figure 4.2.

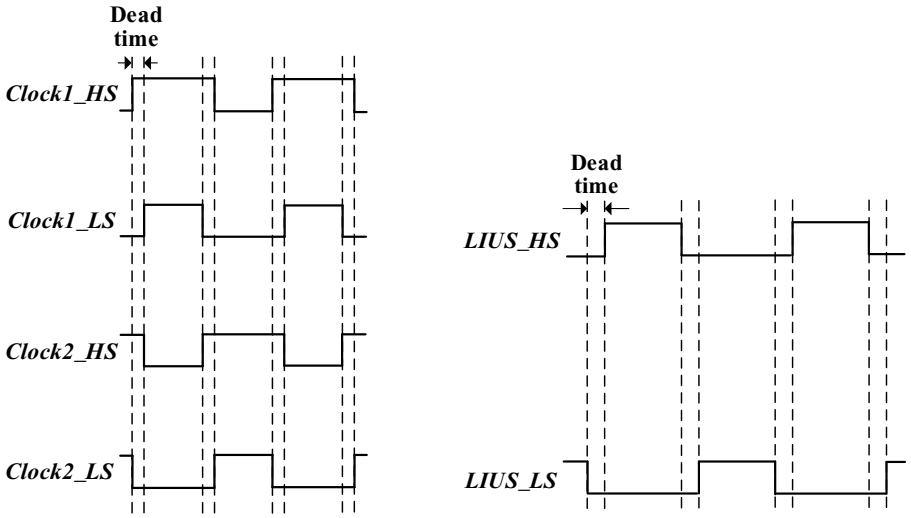


Figure 4.2: Control signals generated by the digital control block for the custom ASIC: (a) control signals for the clock drivers in the DC-DC boost converter (same as in Figure 2.24) and (b) control signals for the half-bridge transducer driver (same as in Figure 3.2).

4.1.1 System specifications design

As mentioned, a customized PZT transducer is used as the load of the miniaturized LIUS device. This PZT transducer has a resonance frequency of 1.5 MHZ and a radiating surface area of 0.63 mm^2. The impedance of the customized PZT transducer is measured with an impedance meter (model: Biologic SP-200). The impedance magnitude at the resonance frequency is 348 Ω while the phase is -30°.

To drive the customized PZT transducer at its resonance frequency, the output wave of the half-bridge transducer needs to be designed with a frequency of 1.5 MHz. Figure 4.3 shows the output wave of the half-bridge transducer. As shown, it is a periodic wave with a duty cycle of 50%. Ideally, It is a square wave with a magnitude of V_{PP}. To design the value of V_{PP}, let's review the concept of Fourier series.

A Fourier series is defined as an expansion of a function or representation of a function in a series of sines and cosines [99]. For the wave generated by the half-bridge transducer driver (shown in Figure 4.3), its function $f(t)$ can be defined as

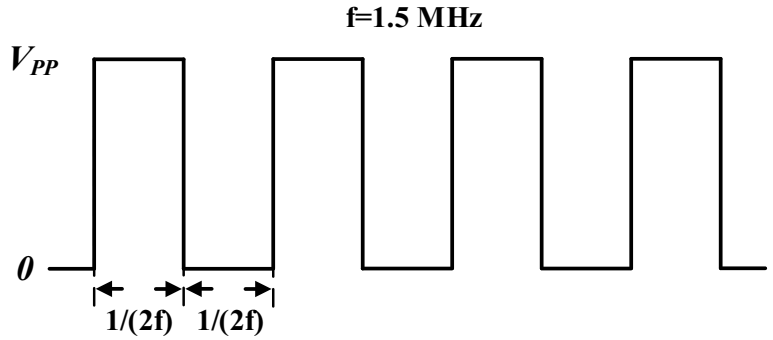


Figure 4.3: Wave generated by the half-bridge transducer driver for driving the PZT transducer.

$$\begin{aligned} f(t) &= 0, \quad -\frac{1}{2f} < t < 0 \\ f(t) &= V_{PP}, \quad 0 < t < \frac{1}{2f} \end{aligned} \tag{4.1}$$

where t represents time, f is the wave frequency (designed to be the same as the resonance frequency of the PZT transducer, i.e., 1.5 MHz for the cutomized PZT transducer), and V_{PP} is the wave amplitude.

The resulting Fourier series is

$$f(t) = \frac{V_{PP}}{2} + \frac{2V_{PP}}{\pi}\{\sin(2\pi ft) + \frac{1}{3}\sin(3 \times 2\pi ft) + +\frac{1}{5}\sin(5 \times 2\pi ft) + \dots\} \tag{4.2}$$

As discussed in Section 3.1, the BVD model of a PZT transducer is an R-L-C circuit in parallel with a capacitor (Figure 3.1(a)). At the resonance frequency, the series inductance and capacitance cancel each other out and the PZT transducer can be modeled as a resistor in parallel with a capacitor (Figure 3.1(b)). Therefore, the effective component of the series in equation (4.2) is the sine wave at the resonance frequency of the PZT transducer. We refer it as $v(t)$. The function is expressed as

$$v(t) = \frac{2V_{PP}}{\pi}\sin(2\pi ft) \tag{4.3}$$

For a load transducer with an impedance of $z = |z|\underline{/\phi}\ \Omega$. The current $i(t)$ going through the load at $v(t)$ can be calculated as

$$i(t) = \frac{2V_{PP}}{|z|\pi} \sin(2\pi ft - \phi) \tag{4.4}$$

The active power delivered to the load transducer can be obtained as

$$P_{active} = \frac{2{V_{PP}}^2}{|z|\pi^2} \cos(\phi) \tag{4.5}$$

We can see from equation (4.5) that due to the existence of the parallel capacitor, which leads to a phase of ϕ, the active power delivered to the load transducer is decreased by $\cos(\phi)$.

According to equation (4.5), the value of V_{PP} can be chosen by considering the design specifications of the output power requirement and the impedance of the load transducer. After considering the voltage drop across the drain-source terminals of the high-side switch of the transducer driver, V_{PP} needs to be designed slightly higher than that calculated by equation (4.5). On another note, the output voltage wave is not the ideal square wave shown in Figure 4.3 during the operation when the load transducer is connected.

For the specifications design of the DC-DC boost converter in the proof-of-concept miniaturized LIUS device (Figure 4.1), the 4-stage CP-1 circuit and the clock drivers described in Section 2.5 were designed with a power conversion efficiency that was maximized when driving the customized PZT transducer. For the half-bridge transducer driver, two HVNMOS devices are used as output switches. As discussed in Section 3.2, one advantage of utilizing an n-type switch at the high-side is that the half-bridge circuit is robust to the voltage ripple of V_{PP}. This is because a stable voltage is applied to the gate-source terminals of the high-side switch using a bootstrap circuit to turn it on completely, regardless of the voltage ripple of V_{PP}. As shown in the output voltage waveform of the 4-stage CP-1 circuit (Figure 2.30), the voltage ripple is quite large. However, the half-bridge transducer driver can tolerate this voltage ripple.

Two identical inverter chains, both with the tapered buffer structure (Figure 2.25), are used as the gate drivers for the output switches of the half-bridge transducer driver. Considering the trade-off between the switching power loss

and the conduction power loss, each output switch is designed with an on-resistance of 7 Ω.

The HV level shifter with short propagation delay and low power consumption proposed in Section 3.3 is used as the HV level shifter for the high-performance operation of the half-bridge transducer driver. The parameters of the HV level shifter are the same as in Table 3.1. A MIM capacitor with a capacitance of 100 pF and a diode made with an NPN bipolar transistor (base and collector tied together) are used for the on-chip bootstrap circuit of the half-bridge transducer driver.

Figure 4.4 shows the assembled miniaturized LIUS device. Each block of the system and the die micrograph of the ASIC are indicated. In the board level, the digital control block utilizes an FPGA board (model: Digilent Cmod A7-35T) to generate control signals at 3.3 V, and an LV level shifting circuit to elevate the controls signals from 0 ∼ 3.3 V to 0 ∼ 3.7 V, i.e., to the battery supply voltage level.

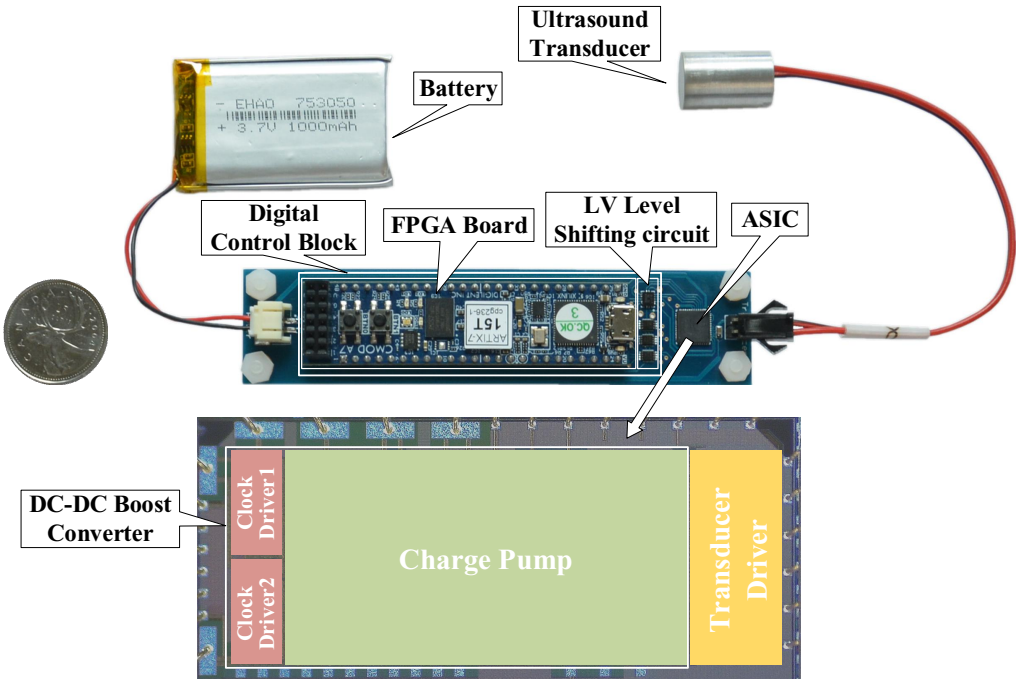


Figure 4.4: The proposed miniaturized LIUS Device comparing with a 25 cent Canadian coin. Each block of the system and the die micrograph of the ASIC are indicated.

Even though a supply voltage of 3.7 V is used, the proposed LIUS system is able to operate with a supply voltage of up to 5 V, which is the maximum allowable voltage for $|V_{gs}|$ of the HV devices as well as the maximum allowable voltage between any two terminals of the LV devices.

4.1.2 Measurement results

The system measurement setup is shown in Figure 4.5. An ultrasound power meter (model: OHMIC Instruments UPM-DT-1PA) is used to measure the ultrasound power generated by the transducer. As shown, the transducer is submerged and positioned directly over the cone target. The measurement principle of the power meter is the radiant force method [100]. More specifically, the ultrasonic energy passing through the distilled water is reflected off the cone target. It is then absorbed by the lining of the tank. The radiant ultrasound power is directly proportional to the total downward force on the cone target. The meter senses this force and converts the reading into an ultrasound pressure in watts. For the electrical characteristics, an oscilloscope is used to measure the voltage at the output voltage of the charge pump (V_{PP}), the switching node of the half-bridge transducer driver (V_{SW}), and the bootstrap voltage of the half-bridge transducer driver (V_{BOOT}). A current probe is used to measure the current flowing through the load transducer (I_{out}).

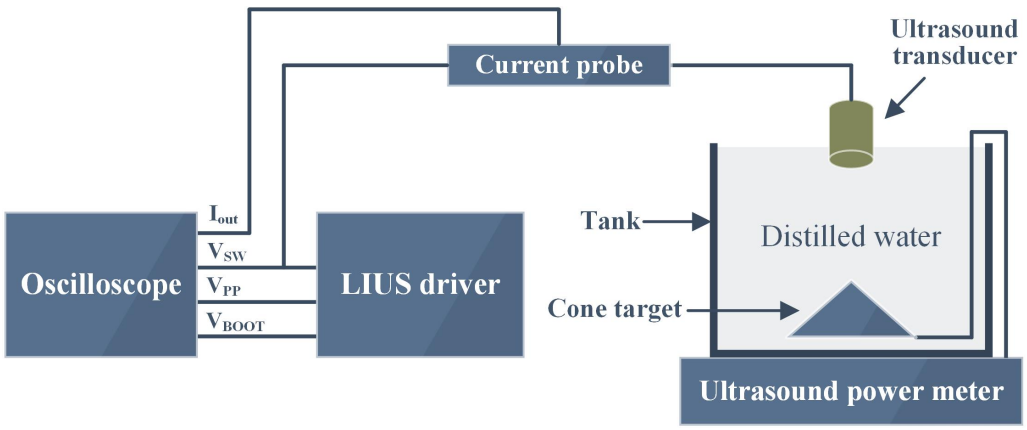


Figure 4.5: System measurement setup.

The charge pump and its clock drivers operate at the same conditions as described in Section 2.5, i.e., the control signals *Clock1_HS*, *Clock1_LS*,

Clock2_HS, and *Clock2_LS* have a frequency of 20 MHz and a dead time of 5 ns. The control signals *LIUS_HS* and *LIUS_LS* for the half-bridge transducer driver have a frequency of 1.5 MHz, which is the resonance frequency of the load transducer. The dead time for *LIUS_HS* and *LIUS_LS* is 10 ns. The control signals *LIUS_HS* and *LIUS_LS* are operated in continuous mode, leading to continuous waves of generated ultrasound. The VHDL codes for the FPGA to generate the continuous-mode control signals are described in Appendix A.

The measured voltage at the switching node V_{SW} is demonstrated in Figure 4.6. As shown, V_{SW} is able to maintain around 10 V when driving the transducer load. The frequency of V_{SW} is 1.5 MHz, which is the resonance frequency of the PZT transducer.

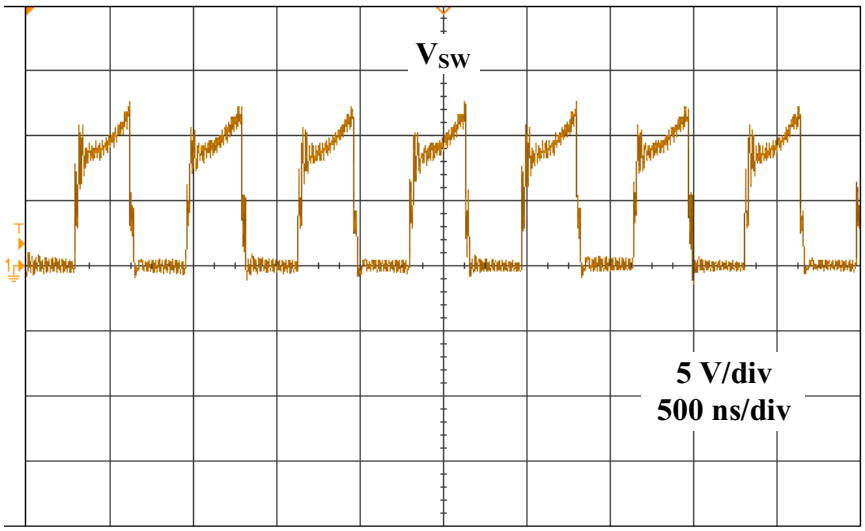


Figure 4.6: Measured waveform of the voltage at the switching node V_{SW}.

Figure 4.7 shows the measured bootstrap voltage V_{BOOT} compared with the voltage waveform at the switching node V_{SW}. It can be seen that the bootstrap circuit is able to keep a voltage difference between V_{SW} and V_{BOOT} during all times. This ensures the appropriate operation of the half-bridge transducer driver.

Figure 4.8 shows the voltage at the switching node V_{SW} and the output voltage of the charge pump V_{PP}. During the phase when the high-side switch Q1 of the transducer driver is on, the charge pump delivers power to the transducer (V_{SW} is close to V_{PP} during this phase). When the low-side switch Q2

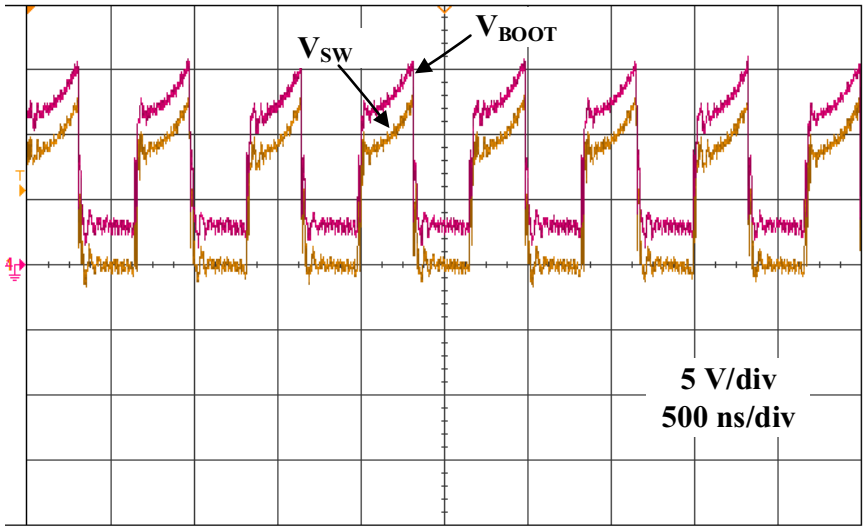


Figure 4.7: Measured waveforms of the bootstrap voltage V_{BOOT} compared with the voltage waveform at the switching node V_{SW}.

of the transducer driver is on, the charge pump operates at no-load condition, and restores its output voltage level. As shown, the changing waveform of V_{PP} deviates V_{SW} from an ideal square wave. This is caused by the limited current drive capability of the charge pump. However, the ultrasound transducer is relatively insensitive to this distortion as it is mainly responsive to the first harmonic of V_{SW} (equation (4.3)), which is a sinusoidal wave.

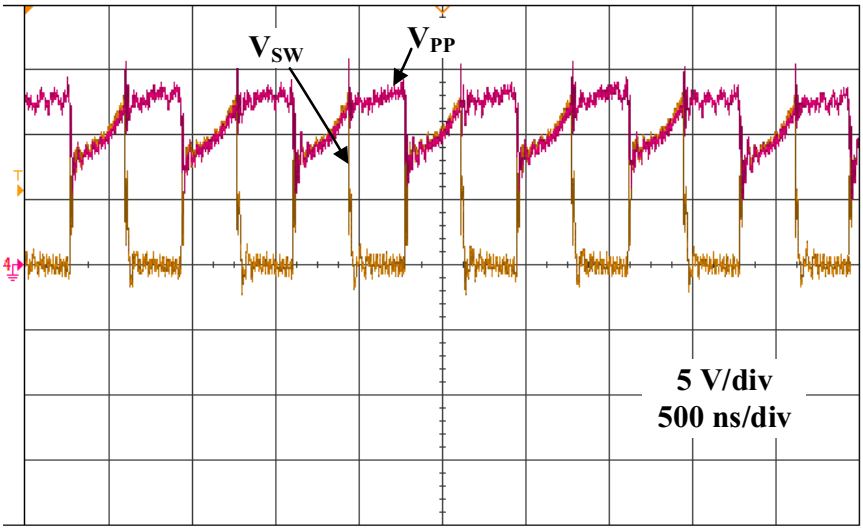


Figure 4.8: Measured waveforms of the voltage at the switching node V_{SW} and the charge pump output voltage V_{PP}.

Figure 4.9 shows the voltage at the switching node V_{SW}, which is equal to the voltage across the load transducer, and the current flowing through the load transducer I_{out}. As mentioned, the effective component causing the resonance of the PZT transducer is the first harmonic of V_{SW} (equation (4.3)), which presents a sinusoidal function. Similarly, the current flowing through the transducer is also nearly sinusoidal, as shown in Figure 4.9. The average power delivered to the transducer, which is calculated using V_{SW} and I_{out}, is 72 mW.

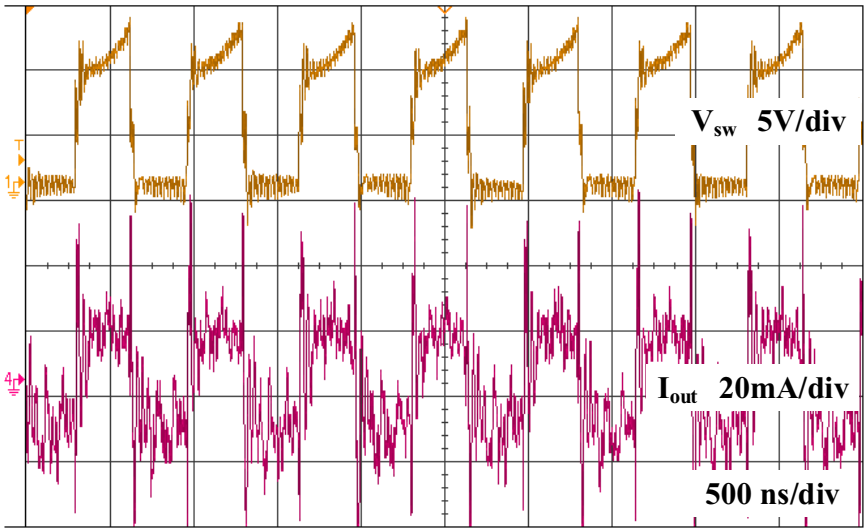


Figure 4.9: Measured waveforms of the voltage at the switching node V_{SW} and the current flowing through the load transducer I_{out}.

The system performance of the miniaturized LIUS device generating ultrasound with continuous waves is summarized in Table 4.1. The power efficiency of the ASIC is limited by the power conversion efficiency of the on-chip DC-DC boost converter. The generated ultrasound power measured by the ultrasound power meter is 20 mW, which leads to an ultrasound power intensity of 32 mW/cm^2.

Pulsed ultrasound can also be achieved with the proposed miniaturized LIUS device by simply changing the control signals *LIUS_HS* and *LIUS_LS* to pulsed mode. More specifically, instead of the continuous-mode control signals shown in Figure 4.2(b), *LIUS_HS* and *LIUS_LS* can be designed with on- and off-time for the miniaturized LIUS device to generate pulsed ultrasound.

Table 4.1: Summary of the system performance of the proposed miniaturized LIUS device generating continuous-wave ultrasound.

Power supply voltage	3.7 V
Chip area of the ASIC	10 mm^2
Measured output power delivered to the load transducer by the ASIC (P_{out})	72 mW
Measured input power of the ASIC (P_{in})	421 mW
Calculated power efficiency of the ASIC (P_{out} / P_{in})	17%
Measured ultrasound power ($P_{acoustic}$)	20 mW
Calculated transfer efficiency of the load transducer ($P_{acoustic}$ / P_{out})	28%
Radiating surface area of the load transducer (A)	0.63 cm^2
Calculated ultrasound power intensity ($P_{acoustic}$ / A)	32 mW/cm^2

Figure 4.10 shows the pulsed-mode control signals *LIUS_HS* and *LIUS_LS*. To generate the pulsed ultrasound shown in Figure 1.1, the frequency, pulse duration, and pulse repetition period of the control signals in Figure 4.10 need to be designed the same as in Figure 1.1.

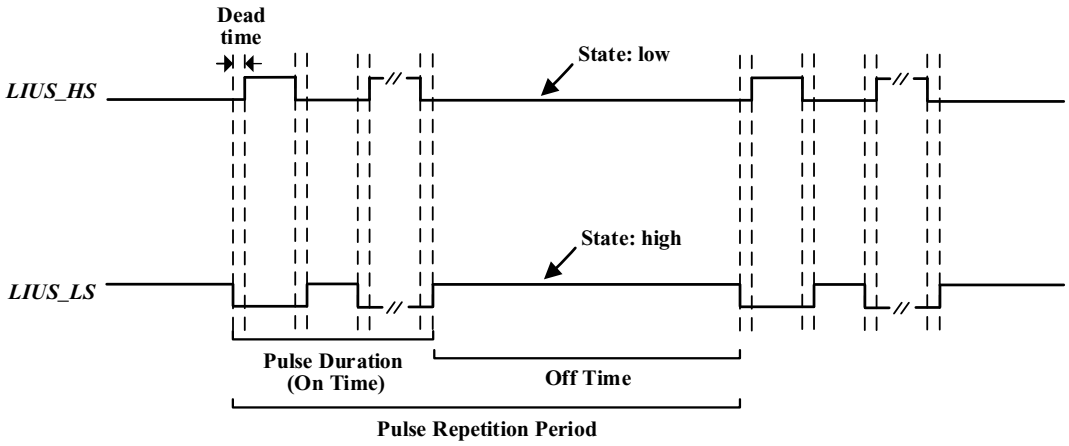


Figure 4.10: Pulsed-mode control signals *LIUS_HS* and *LIUS_LS*.

During the on-time, *LIUS_HS* and *LIUS_LS* are the same as in continuous-mode shown in Figure 4.2(b). During the off-time when there is no pulse output, the control signal *LIUS_HS* needs to be kept low to turn off the high-side switch Q1 of the half-bridge transducer driver (Figure 4.1), and the control

signal *LIUS_LS* needs to remain high to turn on the low-side switch Q2. In this way, both terminals of the PZT transducer are connected to the ground and no ultrasound is generated during the off-time.

To generate pulsed ultrasound with a pulse duration of 200 µs, and a pulse repetition period of 1 ms, we chose the control signals *LIUS_HS* and *LIUS_LS* to have the same parameters, leading to the voltage waveforms of the switching node V_{SW} in Figure 4.11. During the 200 µs pulse duration, V_{SW} in Figure 4.11 has the same waveform as in Figure 4.6.

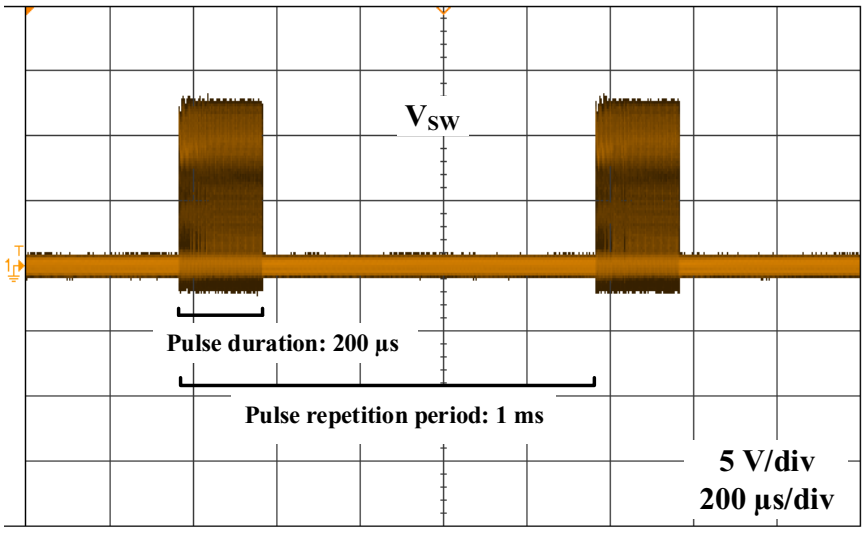


Figure 4.11: Measured waveform of the voltage at the switching node V_{SW} for generating pulsed ultrasound.

Figure 4.12 demonstrates the pulsed-mode waveforms of the voltage at the switching node V_{SW} and the bootstrap voltage V_{BOOT}. As shown, the bootstrap circuit is able to maintain V_{BOOT} higher than V_{SW} for about V_{DD} (3.7 V) during the off-time. The waveforms of V_{SW} and V_{BOOT} during the pulse duration in Figure 4.12 are the same as those in Figure 4.7.

Due to the large off-time of V_{SW} (800 µs) compared to the on-time (200 µs), the average power delivered to the load transducer is low (14 mW). Because of the low transfer efficiency of the PZT transducer, only 4 mW average ultrasound power is generated, as measured by the ultrasound power meter. This leads to an average ultrasound power intensity of 6.3 mW/cm^2.

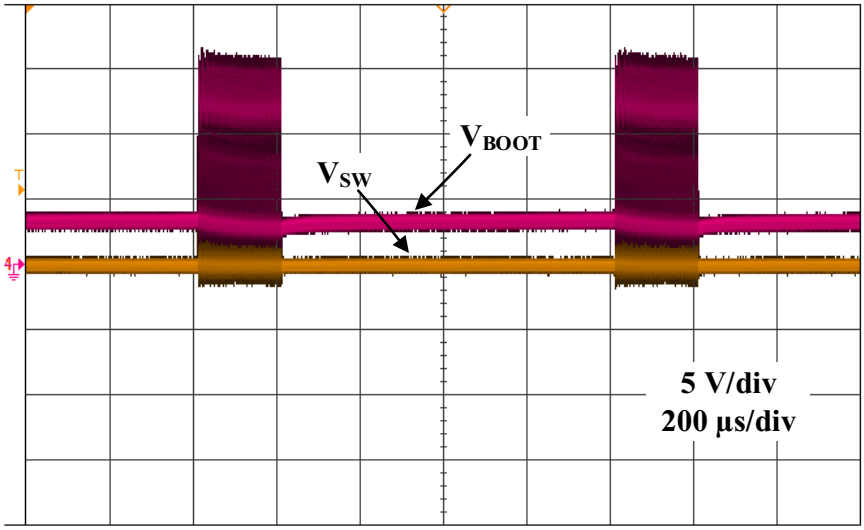


Figure 4.12: Measured waveforms of the voltage at the switching node V_{SW} and the bootstrap voltage V_{BOOT} for generating pulsed ultrasound.

4.1.3 Discussion

The proposed miniaturized LIUS device is suitable for therapeutic applications requiring an ultrasound power intensity of ≤ 32 mW/cm^2 in continuous mode. For instance, the research in [10] has shown 30 mW/cm^2 continuous-wave LIUS is able to inhibit gramicidin D-induced red blood cell edema.

Pulsed ultrasound can also be produced by the proposed miniaturized LIUS device at a lower power intensity, making it suitable for applications requiring low-intensity pulsed ultrasound. For instance, an ultrasound power intensity of 6.3 mW/cm^2 is achieved with the proposed miniaturized LIUS device at a frequency of 1.5 MHz, a pulse duration of 200 µs, and a pulse repetition period of 1 ms. Researchers have shown therapeutic effects using pulsed ultrasound with the same parameters while requiring an ultrasound power intensity of $\leq$ 6.3 mW/cm^2. For example, the study in [33] showed the efficacy of the pulsed ultrasound with an intensity of 2 mW/cm^2 in enhancing osteogenic differentiation of rat bone marrow stromal cells.

The load transducer can be replaced by other PZT transducers with low resonance frequencies, enabling applications requiring low-frequency LIUS, such as the study on the healing of fractures and osteoradionecrosis [11], [12], and the research on bone regeneration enhancement [13], etc.

4.2 Design improvements and a monolithic-chip solution

While the proof-of-concept miniaturized LIUS device is able to generate ultrasound with low intensities in both continuous mode and pulsed mode, there are still several aspects that can be improved, including:

- Improvement 1: Integrating the digital control block on the ASIC. As shown in the miniaturized LIUS device (Figure 4.4), the digital control block occupies a large area of the circuit board. Integrating the digital control block on the ASIC would further reduce the board area and the power dissipation of the system.

- Improvement 2: Adding an impedance matching circuit for the PZT transducer. As discussed, the PZT transducer model can be represented by a resistor in parallel with a capacitor when operating at its resonance frequency. The capacitance leads to a negative phase of the load impedance (for instance, the impedance of the customized PZT transducer is $348\underline{/-30^\circ}\Omega$), which results in the degradation of the active output power by $\cos(-30^\circ)$ (equation (4.5)). To increase the active output power, an impedance matching circuit could be added to cancel out the capacitance and match the PZT transducer into a resistive load at the resonance frequency.

- Improvement 3: Increasing the output power of the DC-DC boost converter. As described in Chapter 1, current LIUS therapy has a wide variety of applications, which requires different ultrasound power intensities. Increasing the output power of the DC-DC boost converter would allow the proposed LIUS system to generate ultrasound at higher intensities, which would include more flexibility for the proposed system to be applied for various applications.

4.2.1 Improvement 1

To integrate the digital control block on chip, an improved ASIC is designed. The functional block diagram of the improved ASIC is shown in Figure 4.13. As shown, three supply voltage pairs are used, i.e., DV_{DD} and DGND, AV_{DD} and AGND, PV_{DD} and PGND. Pins DGND, AGND, and PGND are all connected to the ground, and pins DV_{DD}, AV_{DD}, and PV_{DD} have the same voltage potential (3.7 V), which is the nominal voltage of the lithium-ion battery. Same as in Figure 4.1, the charge pump and its two clock drivers in Figure 4.13 constitutes the DC-DC boost converter. The half-bridge transducer driver also has the same structure as in Figure 4.1. The bootstrap circuit in Figure 4.13 is implemented with an external diode and an external capacitor. For the digital control block, two clock sources are used:

1. Clock Source1: provided by an external crystal oscillator.

2. Clock Source2: provided by an internal voltage-controlled oscillator (VCO).

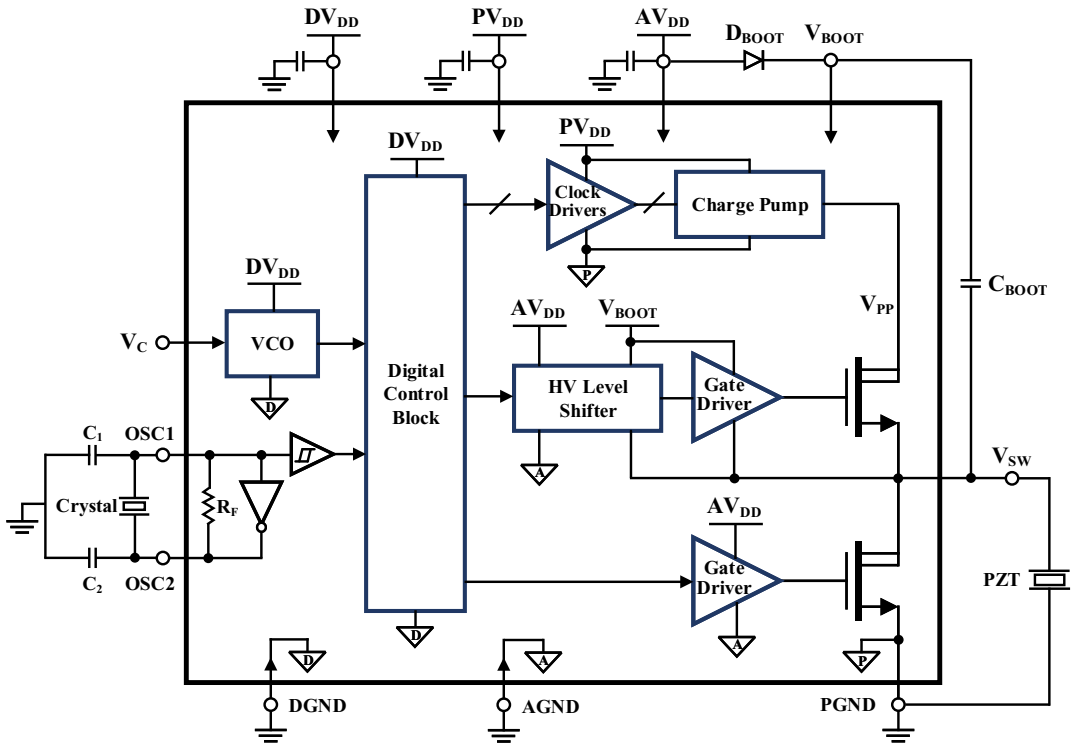


Figure 4.13: Functional block diagram of the improved ASIC.

For Clock Source1, the external oscillator is implemented with a quartz crystal, two capacitors, an inverter, a feedback resistor, and a Schmitt trigger. The advantage of the external crystal oscillator is that it offers high accuracy. It is used to generate an accurate 12 MHz clock signal, which is passed to the digital control block to generate control signals *LIUS_HS* and *LIUS_LS*. High accuracy is required for *LIUS_HS* and *LIUS_LS* to control the half-bridge transducer driver to interface with the PZT transducer at its resonance frequency. This is because the impedance of the PZT transducer varies significantly when operating off its resonance frequency.

For Clock Source2, an on-chip VCO is utilized. The clock signal provided by the VCO is used by the digital control block to generate control signals *Clock1_HS*, *Clock1_LS*, *Clock2_HS*, and *Clock2_LS*. The VCO block is used for this purpose for two reasons: (1), the DC-DC boost converter has no requirement for high-accurate-frequency control signals. That is to say, a few kHz off the optimum operating frequency has minor effects on the performance of the DC-DC boost converter as long as the dead time of the control signals are appropriately correlated, and (2), the frequency of the clock signal provided by the VCO can be tuned by the external control voltage V_C (shown in Figure 4.13). The tunable frequency is desirable as it can change the frequency of the control signals *Clock1_HS*, *Clock1_LS*, *Clock2_HS*, and *Clock2_LS*, and in turn adjust the output power of the DC-DC boost converter. The tunable output power of the DC-DC boost converter can include more flexibility for the proposed LIUS system to generate ultrasound with different power requirements, even though this may deviate the power conversion efficiency of the DC-DC boost converter from its optimized value.

As mentioned, the function of the digital control block in Figure 4.13 is to generate the control signals *Clock1_HS*, *Clock1_LS*, *Clock2_HS*, and *Clock2_LS* for the clock drivers of the DC-DC boost converter, and the control signals *LIUS_HS* and *LIUS_LS* for the half-bridge transducer driver. A simple non-overlapping clock generator structure can be used to generate continuous-mode *Clock1_HS_CM*, *Clock1_LS_CM*, *Clock2_HS_CM*, and *Clock2_LS_CM* (CM denotes continuous-mode). We use suffix CM to indicate continuous-mode and

PM for pulsed-mode from this point. Figure 4.14 shows the non-overlapping clock generator structure. The input signal *Clock1_in_VCO* in Figure 4.14 is the clock signal provided by the VCO. Two non-overlapping clock generators with a similar structure are used to generate four output signals. For each clock generator, a NAND gate latch and two delay blocks work together to produce the dead time between the output signals. Inverters are used at the output to adjust the output signals to their desired phases.

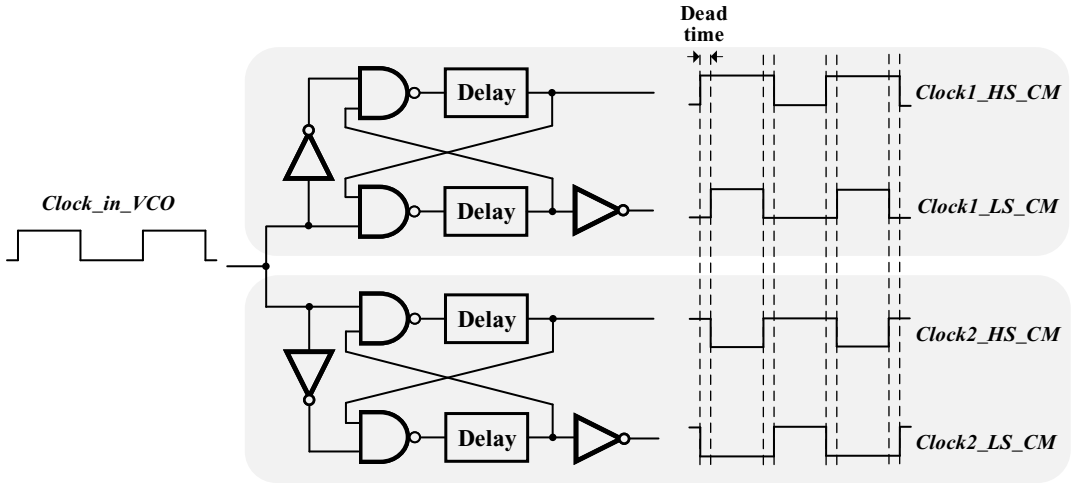


Figure 4.14: Non-overlapping clock generators for generating continuous-mode control signals *Clock1_HS_CM*, *Clock1_LS_CM*, *Clock2_HS_CM*, and *Clock2_LS_CM*.

To generate continuous-mode control signals *LIUS_HS_CM* and *LIUS_LS_CM*, a non-overlapping clock generator with a simple modification based on Figure 4.14 can be used. Figure 4.15 shows the non-overlapping clock generator.

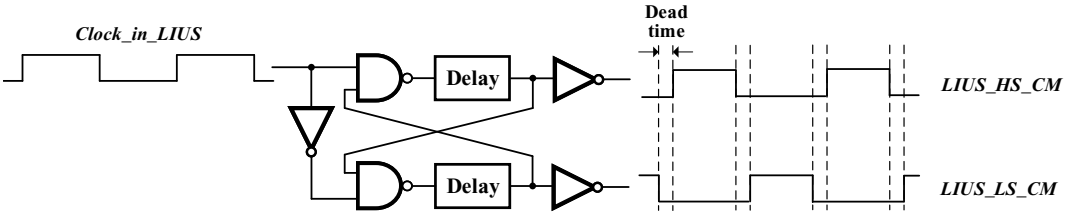


Figure 4.15: Non-overlapping clock generator for generating continuous-mode control signals *LIUS_HS_CM* and *LIUS_LS_CM*.

For the LIUS system to generate pulsed ultrasound, pulsed-mode control signals *LIUS_HS_PM* and *LIUS_LS_PM* (PM denotes pulsed-mode) are

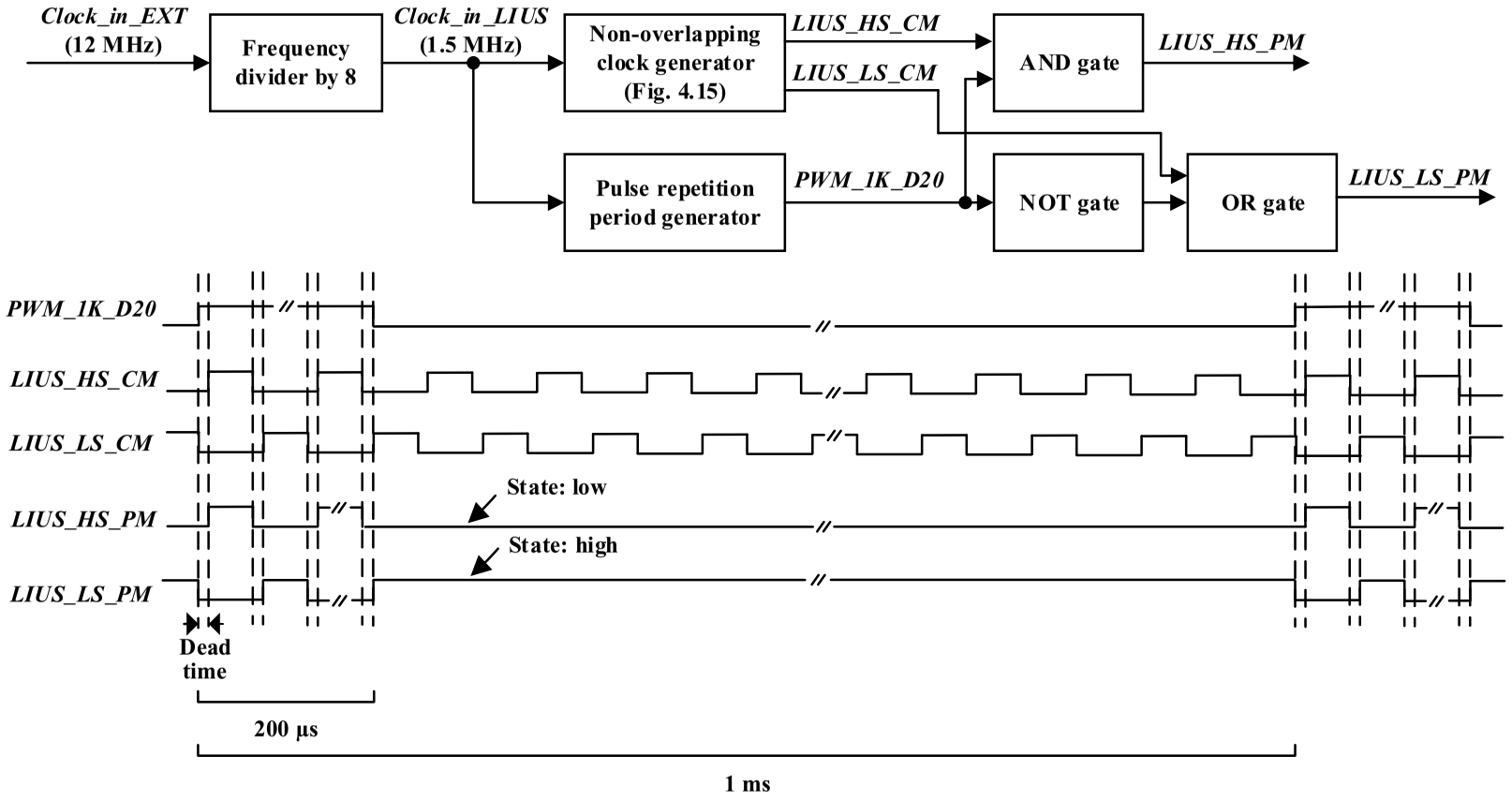


Figure 4.16: Block diagram for generating pulsed-mode control signals *LIUS_HS_PM* and *LIUS_LS_PM*.

needed. For example, to generate pulsed ultrasound with a pulse duration of 200 µs and a pulse repetition period of 1 ms, *LIUS_HS_PM* and *LIUS_LS_PM* need to be designed with the same parameters. Figure 4.16 shows the detailed block diagram for generating *LIUS_HS_PM* and *LIUS_LS_PM* with a pulse duration of 200 µs and a pulse repetition period of 1 ms. The 12 MHz input clock signal *Clock1_in_EXT* in Figure 4.16 is provided by the external crystal oscillator. A frequency divider composed of three D flip-flops is used to divide the 12 MHz clock signal to 1.5 MHz, which is the resonance frequency of the PZT transducer. The non-overlapping clock generator in Figure 4.16 is the same as in Figure 4.15. The pulse repetition period generator in Figure 4.16 is used to generate the signal *PWM_1K_D20*, which has a period of 1 ms, and a pulse width of 200 µs. The pulse repetition period generator can be implemented with a frequency divider and a counter. The waveforms of *PWM_1K_D20*, *LIUS_HS_CM*, and *LIUS_LS_CM* are depicted in Figure 4.16. After some simple logic processing of *PWM_1K_D20*, *LIUS_HS_CM*, and *LIUS_LS_CM*, the control signals *LIUS_HS_PM* and *LIUS_LS_PM* can be obtained with the desired pulse duration and pulse repetition period, as shown in Figure 4.16.

When operating in pulsed mode, the operation of the charge pump can be paused during the off-time to reduce the power dissipation of the LIUS system. This can be done by simply putting control signals *Clock1_HS_PM*, *Clock1_LS_PM*, *Clock2_HS_PM*, and *Clock2_LS_PM* (PM represents pulsed-mode) to a high state. More specifically, these four control signals have a waveform same as Figure 4.14 during the on-time, and have a voltage of V_{DD} during the off-time. In this way, the outputs of the clock drivers, i.e., Clock1 and Clock2 are both connected to the ground during the off-time, pausing the operation of the charge pump.

4.2.2 Improvement 2

To maximize the active power delivered to the PZT transducer, an impedance matching circuit can be used to match the PZT transducer into a resistive load. A low-cost matching method was presented in [101] employing a simple

L-C matching network. Figure 4.17 shows the L-C impedance matching circuit presented in [101]. The transducer composed of C_{eq} and R_{eq} is the simplified transducer model same as in Figure 3.1(b) with one terminal connected to the ground. L_m and C_m constitute the matching network. R_g is the target resistive load that we are matching the impedance into. Denoting ω as the angular frequency, the value of L_m and C_m are deducted in [101] as

$$\begin{aligned} L_m &= \frac{R_g}{\omega}\sqrt{\frac{R_{eq}}{R_g} - 1} \\ C_m &= \frac{1}{\omega R_{eq}}\sqrt{\frac{R_{eq}}{R_g} - 1} - C_{eq} \end{aligned} \tag{4.6}$$

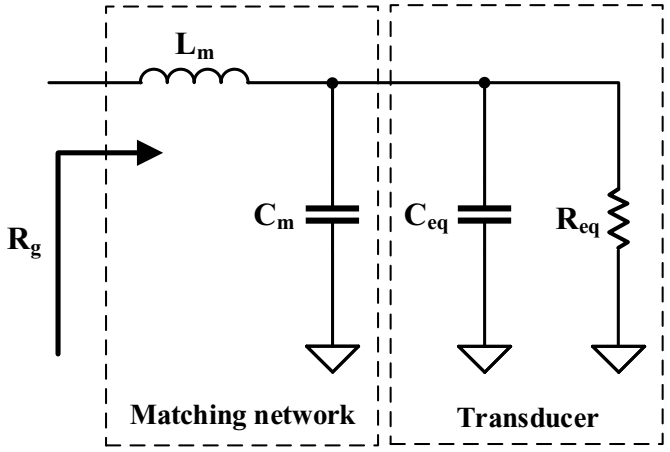


Figure 4.17: L-C impedance matching circuit (modified from [101]).

For the improved LIUS system, we devise the desirable resistive load to be 100 Ω. The values of the parallel capacitor and resistor of the customized PZT transducer (the impedance is 348 $\angle -30°$) can be calculated as $C_{eq} = 153$ pF, and $R_{eq} = 401$ Ω based on equation (3.2). According to equation (4.6), the matching network parameters can be obtained as

$$\begin{aligned} L_m &= 18.4 \text{ µH} \\ C_m &= 1.68 \text{ nF} \end{aligned} \tag{4.7}$$

The additional inductor and capacitor introduced by the matching network add a minor area penalty for the circuit board. However, this is greatly outweighed by increasing the active output power.

4.2.3 Improvement 3

Improvement 3 is about increasing the output power of the DC-DC boost converter so as to enable the LIUS system for a wider variety of therapeutic applications. As discussed in the design considerations of the proposed charge pumps (Section 2.3.3), increasing the capacitance of the pumping capacitors can effectively increase the current drive capability, thus the output power level. However, as on-chip capacitors occupy large die areas and would not be cost-effective when designed with large capacitance, it's not feasible to increase the capacitance of the on-chip capacitors to improve the output power of the charge pump. For this reason, off-chip capacitors were used as the pumping capacitors and the output capacitor of the improved charge pump to achieve high output power.

An improved DC-DC boost converter was designed in AMS's 0.35-µm HVCMOS process with off-chip capacitors to achieve high output power. To enable the proposed LIUS system for therapeutic applications with high ultrasound power intensity requirements, we devised the output power of the system to be 400 mW when operating in continuous mode (the system supply voltage is 3.7 V). As described in Improve 2, the impedance of the load PZT was matched to a resistive load of 100 Ω. To deliver an output power of 400 mW to the 100 Ω load, the RMS voltage across the load is 6.32 V (calculated by $\sqrt{0.4 \times 100}$). According to equation (4.3), the output voltage of the charge pump (V_{PP}) needs to be 14.1 V (calculated by $6.32 \times \sqrt{2} \times \pi \div 2$) when driving the load. Taking consideration of the voltage drop across the drain-source terminals of the high-side switch in the half-bridge transducer driver, V_{PP} needs to be higher than 14.1 V. Therefore, to achieve the system output power requirement of 400 mW, considering the power consumption of the transducer driver, the improved DC-DC boost converter needs to be designed with the capability of delivering an output power of over 400 mW with an output voltage higher than 14.1 V at a supply voltage of 3.7 V.

The improved charge pump was also designed in 4 stages using the CP-1 structure (the same as in Figure 2.21). The parameters of the charge pump

are listed in Table 4.2. For the clock drivers of the charge pump, the same structures as in Figure 2.24 were used. The output PMOS and NMOS switches were designed with an on-resistance of 100 mΩ. The parameters of the charge pump and its clock drivers were designed by maximizing the power efficiency while delivering over 400 mW output power for the system when operating at a clock frequency of 20 MHz.

Table 4.2: Component parameters of the 4-stage CP-1 circuit implemented in AMS's 0.35-µm HVCMOS process.

Function	Component	Type	Size or Value
NMOS CTS	MA1, MB1	20 V HVNMOS	W=2.2 mm L=0.5 µm
PMOS CTS	MA2∼ MA4, MB2∼ MB4, MAout, MBout	20 V HVPMOS	W=2.7 mm L=1 µm
Auxiliary NMOS	MNA2∼ MNA4, MNB2∼ MNB4	20 V HVNMOS	W=300 µm L=0.5 µm
Auxiliary PMOS	MPA2∼ MPA4, MPB2∼ MPB4	20 V HVPMOS	W=1.8 mm L=1 µm
Pumping capacitor	$C_{A1} \sim C_{A4}$, $C_{B1} \sim C_{B4}$	Off-chip capacitor	4.7 nF
Out capacitor	C_{out}	Off-chip capacitor	4.7 nF

4.2.4 Simulation results

Except for the charge pump and its clock drivers discussed above, a half-bridge transducer driver has also been designed in AMS's 0.35-µm HVCMOS process. Its component parameters are listed in Table 4.3. The output switches of the half-bridge transducer driver were designed to have an on-resistance of 2.8 Ω. This was chosen by minimizing the power loss of the half-bridge transducer driver by considering the trade-off between the conduction power loss and the

switching power loss. The parameters of the HV level shifter were designed according to the design considerations discussed in Section 3.3.2.

Table 4.3: Component parameters of the half-bridge transducer driver implemented in AMS's 0.35-µm HVCMOS process.

Transistor	Type	W / L (µm / µm)
For the half-bridge transducer driver shown in Figure 3.2		
Output switches Q1 and Q2	50 V HVNMOS	10000 / 0.5
For the proposed HV Level shifter shown in Figure 3.13		
M1, M2	50 V HVNMOS	10 / 0.5
M3, M4	50 V HVPMOS	10 / 1
M5, M6	5 V PMOS	0.5 / 0.5
PMOS in inverters I1 and I2	5 V PMOS	5 / 0.5
NMOS in inverters I1 and I2	5 V NMOS	0.4 / 0.5

The layout of the improved ASIC has been carried out. Figure 4.18 shows the layout with each circuit block indicated. The total die area of the improved ASIC is 4.0 mm^2. Compared to the die area of the ASIC in the proof-of-concept miniaturized device, which is 10 mm^2, the die area of the improved ASIC is substantially reduced. This is because the capacitors of the charge pumps are implemented off chip in the improved ASIC. Furthermore, with the digital control block integrated on chip, the FPGA board of the proof-of-concept miniaturized device (Figure 4.4) can be removed. This leads to a monolithic-chip solution with smaller board area, as well as reduced weight, cost, and power consumption for the system.

Figure 4.19 shows the simulated voltage waveform of V_{SW} of the improved system in continuous mode. Compared to the V_{SW} waveform of the proof-of-concept miniaturized LIUS device shown in Figure 4.6, the improved system can deliver a higher voltage to the load, as demonstrated in Figure 4.19.

Simulated voltage waveforms of V_{SW} and V_{BOOT} of the improved system in

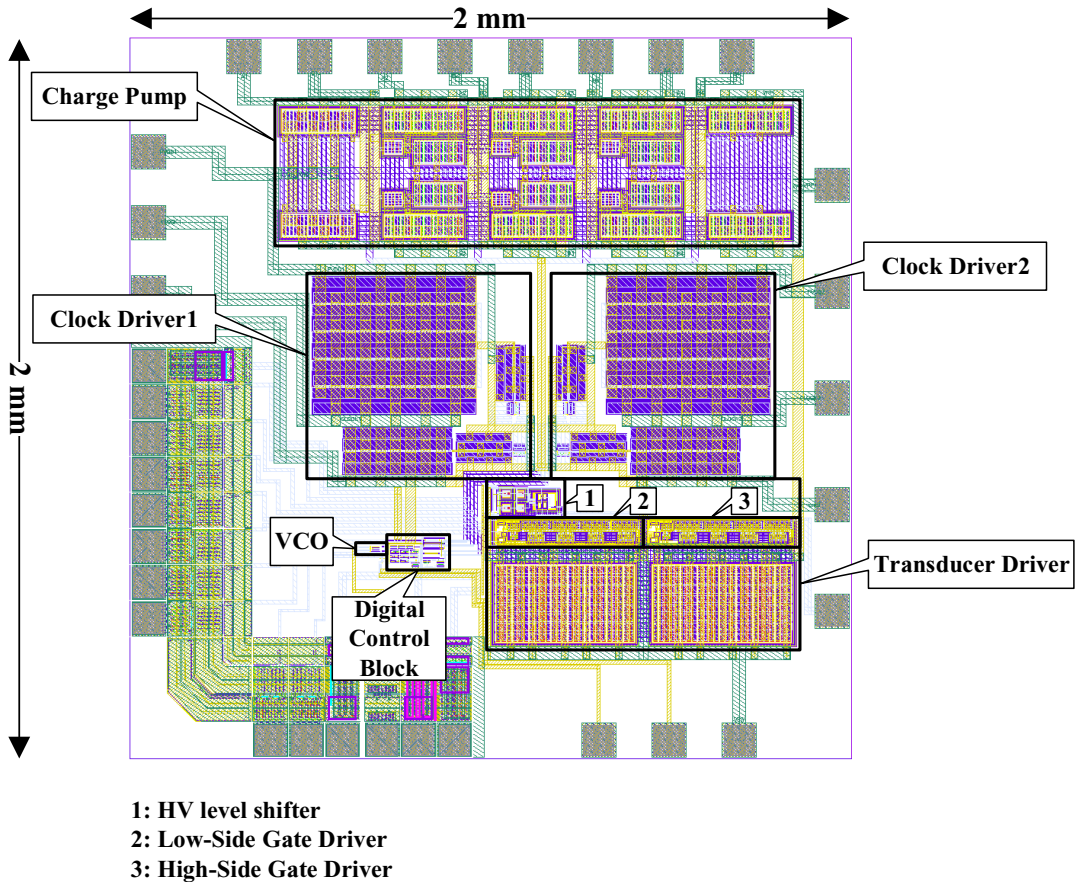


Figure 4.18: Layout of the improved ASIC (total area: 4 mm^2).

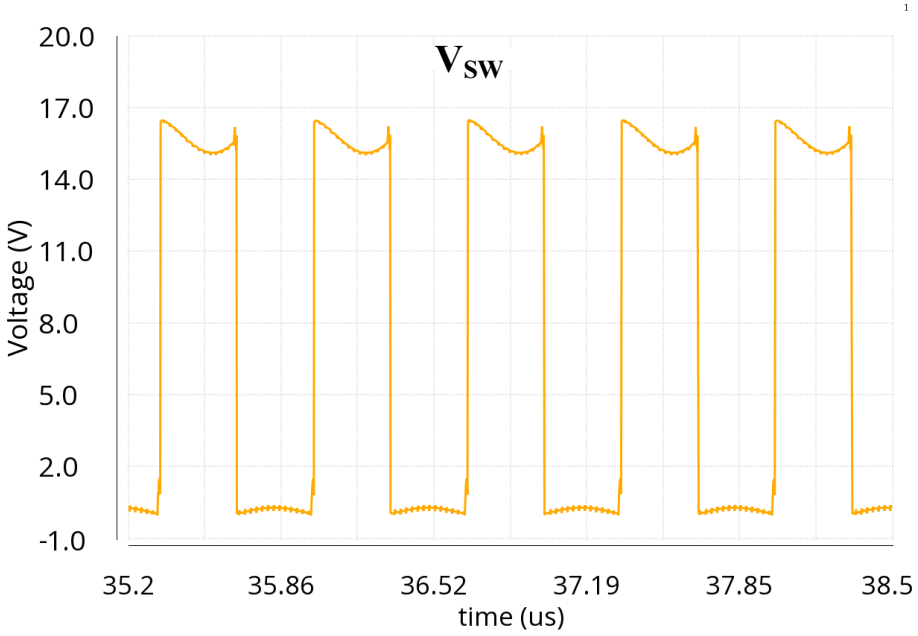


Figure 4.19: Simulated waveform of the voltage at the switching node V_{SW} of the improved system in continuous mode.

continuous mode are shown in Figure 4.20. Similar to the waveforms depicted in Figure 4.7, the bootstrap circuit is able to keep V_{BOOT} higher than V_{SW} at all times, ensuring the proper operation of the half-bridge transducer driver.

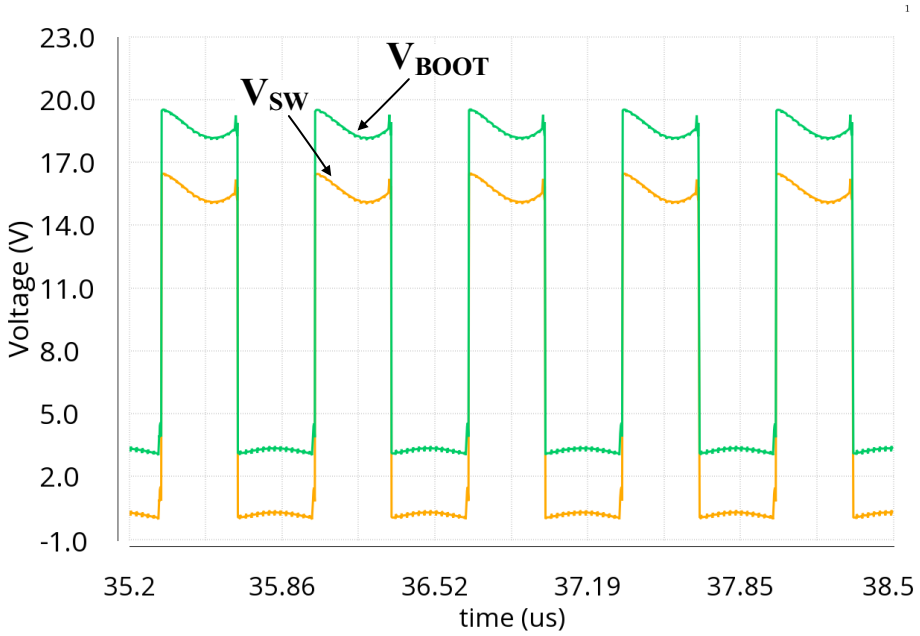


Figure 4.20: Simulated waveforms of the voltage at the switching node V_{SW} and the bootstrap voltage V_{BOOT} of the improved system in continuous mode.

Figure 4.21 demonstrates the voltage waveform of V_{SW} of the improved system compared to that of V_{PP}. Similar to that of Figure 4.8, during the phase when the high-side switch Q1 of the transducer driver is on, the charge pump delivers power to the load (V_{SW} is close to V_{PP} during this phase). When the low-side switch Q2 of the transducer driver is on, the charge pump operates at no-load condition, and restores its output voltage level.

Figure 4.22 shows the simulated waveforms of V_{SW} and I_{out} of the improved system in continuous mode. As shown, an ideal sinusoidal wave can be obtained for the current going through the load. Besides, the output current is much higher compared to that of Figure 4.9, contributed by the increased current drive capability of the improved DC-DC boost converter. The output power calculated by V_{SW} and I_{out} is 418 mW, meeting the design specification of the improved system.

The improved system performance when operating in continuous mode is

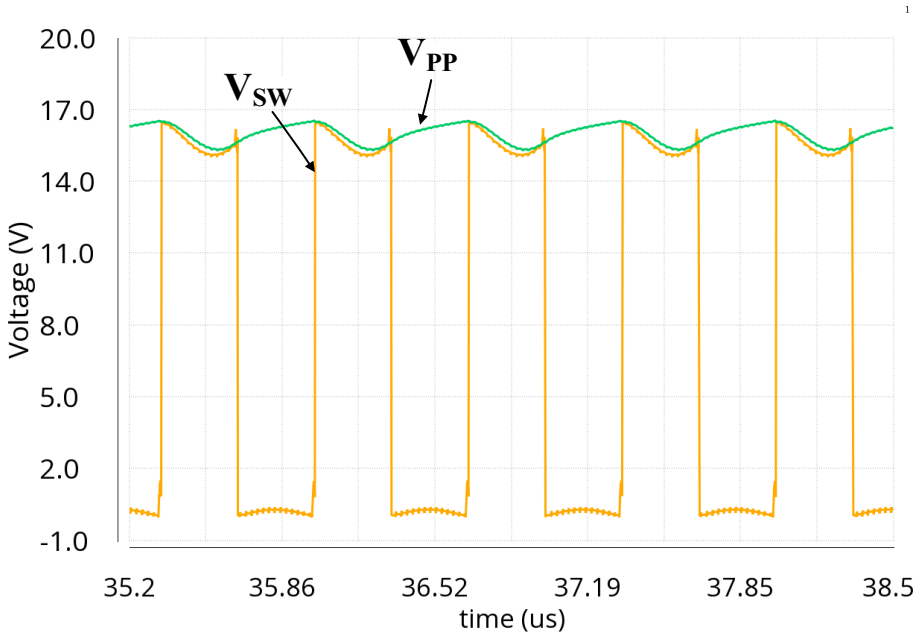


Figure 4.21: Simulated waveforms of the voltage at the switching node V_{SW} and the output voltage of the charge pump V_{PP} of the improved system in continuous mode.

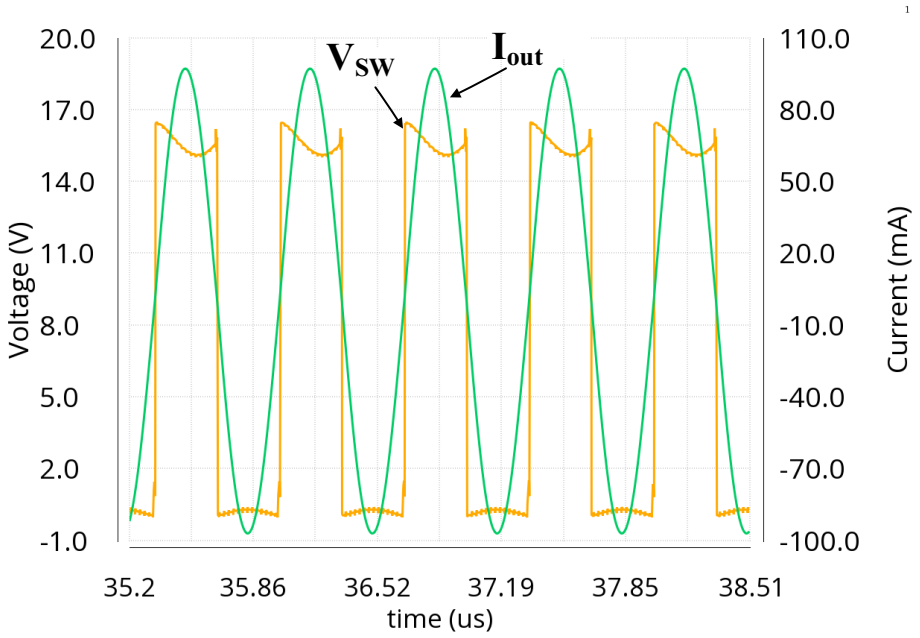


Figure 4.22: Simulated waveforms of the voltage at the switching node V_{SW} and the current going through the load I_{out} of the improved system in continuous mode.

summarized in Table 4.4. The performance of the system in pulsed mode (has a pulse duration of 200 µs and a pulse repetition period of 1 ms) has also been investigated and summarized in Table 4.4.

Table 4.4: Performance summary of the improved system.

Power supply voltage		3.7 V
Chip area of the ASIC		4 mm^2
Performance for generating continuous-wave ultrasound		
Half-bridge transducer driver	Simulated input power	460 mW
	Simulated output power	418 mW
	Calculated power efficiency	90.9 %
DC-DC boost converter	Simulated input power	974 mW
	Simulated output power	441 mW
	Calculated power efficiency	45.3 %
The ASIC	Simulated input power	996 mW
	Simulated output power	418 mW
	Calculated power efficiency	42.0 %
Performance for generating pulsed-wave ultrasound		
Half-bridge transducer driver	Simulated input power	92.3 mW
	Simulated output power	83.4 mW
	Calculated power efficiency	90.4 %
DC-DC boost converter	Simulated input power	200 mW
	Simulated output power	88.3 mW
	Calculated power efficiency	44.2 %
The ASIC	Simulated input power	205 mW
	Simulated output power	83.4 mW
	Calculated power efficiency	40.7 %

As demonstrated, the power conversion efficiency of both continuous-mode and pulsed-mode operations is dominated by the DC-DC boost converter. The power conversion efficiency of the DC-DC boost converter in the improved system is higher than that in Table 4.1 mainly due to the use of off-chip capacitors. Benefiting from the operation pause of the DC-DC boost converter during the off-time, the power conversion efficiency of the improved system in

pulsed mode can remain similar to that of the continuous-mode operation. Compared to the results of the proof-of-concept miniaturized LIUS device listed in Table 4.1, both the output power level and the power efficiency of the ASIC has improved.

4.3 Conclusion

In this chapter, a proof-of-concept miniaturized LIUS device is designed and developed to generate low-intensity therapeutic ultrasound based on the system structure proposed in Chapter 1. The miniaturized LIUS device consists of a battery supply, a custom ASIC, an off-chip digital control block, and a piezoelectric transducer. The ASIC integrating a DC-DC boost converter (consisting of a charge pump and two clock drivers proposed in Chapter 2), and a transducer driver (proposed in Chapter 3) is implemented in TSMC's 0.18-µm BCD Gen2 process. A digital control block with an FPGA in this prototype is used to generate the control signals for the AISC. A customized PZT transducer with a resonance frequency of 1.5 MHz is used as the load.

Measurement results show that the proof-of-concept miniaturized LIUS device is able to generate continuous-wave ultrasound with a power intensity of 32 mW/cm^2 at the resonance frequency of the load transducer. Pulsed ultrasound can also be produced by the proof-of-concept miniaturized LIUS device at a lower power intensity. Compared to current commercially available LIUS devices, the miniaturized LIUS device is low-cost, small, and light-weight, thus enabling affordable and wearable applications.

To further improve the miniaturized LIUS device, three improvements have also been proposed in this chapter. The improvements include 1) integrating the digital control block on chip, 2) matching the impedance of the PZT transducer to increase the active output power, and 3) increasing the power deliver capability of the DC-DC boost converter. By integrating the digital control block on chip, the FPGA board in the proof-of-concept miniaturized LIUS device is removed and a monolithic-chip solution is obtained. By matching the impedance of the PZT transducer and increasing the power deliver capa-

bility of the DC-DC boost converter, the improved LIUS system is able to generate ultrasound at higher intensities, which includes more flexibility for the proposed system to be applied for various therapeutic applications. The improved ASIC has been designed in AMS's 0.35-µm HVCMOS process, and simulation results have verified the improved performance.

Chapter 5

Conclusion

In this thesis, a miniaturized LIUS device for wearable medical therapeutic applications was designed and developed from concept to prototype. The design flow can be summarized as 1) system design, 2) circuit design and optimization, 3) physical design and verification, and 4) test and characterization.

The miniaturized LIUS device is based on the highly-integrated LIUS system structure proposed in Chapter 1. The design challenges of the highly-integrated LIUS system are also discussed in Chapter 1. One challenge is designing a DC-DC boost converter with a high output voltage while delivering sufficient output power, and meeting the small size constraint at the same time. The other challenge is designing a half-bridge transducer driver with a high-performance HV level shifter.

Chapter 2 solves the challenge of the DC-DC boost converter by proposing charge pumps (also known as switched-capacitor DC-DC boost converters) with high current drive capability. Power losses in previously reported charge pumps were investigated and improved charge pumps were proposed to reduce the power loss caused by undesired charge transfer. The detailed operation principles of the proposed charge pumps were described as well as the design considerations. Simulation results show better performance of the proposed circuits compared to other circuits with respect to the voltage pumping gain, current drive capability, and power conversion efficiency. Two charge pump ICs were implemented and tested in a standard CMOS process and an HVCMOS process, respectively, verifying that the increased current drive capability can

be obtained by the proposed charge pumps.

Chapter 3 solves the challenge of the half-bridge transducer driver. An HV level shifter with short propagation delay and low power consumption is proposed for the high-performance operation of the half-bridge transducer driver. The current research status of HV level shifter typologies is presented in detail and an improved HV level shifter is proposed. The detailed operation principle of the proposed HV level shifter is described as well as the design considerations. Simulation results show shorter propagation delay and lower energy consumption of the proposed HV level shifter compared to previously reported works implemented in the same process. A test IC implemented in an HVCMOS process was implemented and tested to verify the performance of the proposed HV level shifter.

Based on the charge pumps proposed in Chapter 2, and the half-bridge transducer driver presented in Chapter 3, a proof-of-concept miniaturized LIUS device is designed and developed in Chapter 4 to generate low-intensity therapeutic ultrasound. The miniaturized LIUS device consists of a battery supply, a custom ASIC (composed of the proposed charge pump and its clock drivers, as well as the proposed half-bridge transducer driver), an off-chip digital control block (utilizing an FPGA), and a piezoelectric transducer. Measurement results show that the miniaturized LIUS device is able to generate continuous-wave ultrasound with a power intensity of 32 mW/cm^2 at the resonance frequency of the load transducer. Pulsed ultrasound can also be produced by the proposed LIUS device at a lower power intensity. Compared to current commercially available LIUS devices, the miniaturized LIUS device is low-cost, small, and light-weight, enabling affordable and wearable applications.

To further improve the miniaturized LIUS device, three improvements have been proposed in Chapter 4 and a monolithic-chip solution is obtained. The improvements include 1) integrating the digital control block on chip, 2) matching the impedance of the load PZT to increase the active output power, and 3) increasing the output power of the DC-DC boost converter to enable the LIUS system for a wider variety of therapeutic applications with different

ultrasound power intensity requirements. An improved ASIC was designed in AMS's 0.35-µm HVCMOS process based on the three improvements, and simulation results verified its improved performance.

For future work, an implementation of the improved ASIC could be submitted for fabrication to assemble a second-generation prototype. PZT transducers with higher transfer efficiency could be developed to increase the capability of the LIUS system with higher ultrasound power intensities. Furthermore, additional circuit blocks could be integrated in the system to ensure the performance and reliability of the system. For instance, an Undervoltage-Lockout block could be integrated to turn off the power of the transducer electronic interface when the battery supply voltage drops below the operational value.

References

[1] J. Blitz, *Fundamentals of ultrasonics*, Second. New York: Plenum Press, 1967.

[2] T. S. Awad, H. A. Moharram, O. E. Shaltout, D. Asker, and M. M. Youssef, "Applications of ultrasound in analysis, processing and quality control of food: A review," *Food Research International*, vol. 48, no. 2, pp. 410–427, 2012.

[3] D. Ensminger and L. J. Bond, *Ultrasonics : fundamentals, technologies, and applications*, Third. Boca Raton: CRC Press, 2011.

[4] R. W. Wood and A. L. Loomis, "The physical and biological effects of high-frequency sound-waves of great intensity," *Philosophical Magazine*, vol. 4, pp. 417–436, 1927.

[5] G. Ter Haar, "Therapeutic applications of ultrasound," *Progress in Biophysics and Molecular Biology*, vol. 93, no. 1-3, pp. 111–129, 2007.

[6] S. J. Warden, "A new direction for ultrasound therapy in sports medicine," *Sports Medicine*, vol. 33, no. 2, pp. 95–107, 2003.

[7] J.-M. Escoffre and A. Bouakaz, *Therapeutic ultrasound*. Springer International, 2016.

[8] T. Watson and S. R. Young, "Therapeutic ultrasound," *Watson T. Electrotherapy Evidence-Based Practice. Edinburgh, UK: Churchill Livingstone*, pp. 179–200, 2008.

[9] P. R. Hoskins, K. Martin, and A. Thrush, *Diagnostic ultrasound: physics and equipment*. Cambridge University Press, 2010.

[10] M. H. Lim, A. R. Seo, J. Kim, B.-H. Min, E. J. Baik, S. R. Park, and B. H. Choi, "Effects of low-intensity ultrasound on gramicidin D-induced erythrocyte edema," *Journal of Ultrasound in Medicine*, vol. 33, no. 6, pp. 949–957, 2014.

[11] P. Reher, M. Harris, M. Whiteman, H. Hai, and S. Meghji, "Ultrasound stimulates nitric oxide and prostaglandin e2 production by human osteoblasts," *Bone*, vol. 31, no. 1, pp. 236–241, 2002.

[12] N. Doan, P. Reher, S. Meghji, and M. Harris, "In vitro effects of therapeutic ultrasound on cell proliferation, protein synthesis, and cytokine production by human fibroblasts, osteoblasts, and monocytes," *Journal of Oral and Maxillofacial Surgery*, vol. 57, no. 4, pp. 409–419, 1999.

[13] A. Maddi, H. Hai, S.-T. Ong, L. Sharp, M. Harris, and S. Meghji, "Long wave ultrasound may enhance bone regeneration by altering OPG/RANKL ratio in human osteoblast-like cells," *Bone*, vol. 39, no. 2, pp. 283–288, 2006.

[14] S. J. Warden, K. L. Bennell, J. M. McMeeken, and J. D. Wark, "Can conventional therapeutic ultrasound units be used to accelerate fracture repair?" *Physical Therapy Reviews*, vol. 4, no. 2, pp. 117–126, 1999.

[15] R. Zura, S. Mehta, G. J. Della Rocca, J. Jones, and R. G. Steen, "A cohort study of 4,190 patients treated with low-intensity pulsed ultrasound (LIPUS): findings in the elderly versus all patients," *BMC Musculoskeletal Disorders*, vol. 16, no. 45, pp. 1–10, 2015.

[16] R. W. Poolman, T. Agoritsas, R. A. C. Siemieniuk, I. A. Harris, I. B. Schipper, B. Mollon, M. Smith, A. Albin, S. Nador, W. Sasges, S. Schandelmaier, L. Lytvyn, T. Kuijpers, L. W. A. H. van Beers, M. H. J. Verhofstad, and P. O. Vandvik, "Low intensity pulsed ultrasound (LIPUS) for bone healing: a clinical practice guideline," *BMJ*, vol. 356, no. j576, pp. 1–6, 2017.

[17] U. Farkash, O. Bain, A. Gam, M. Nyska, and P. Sagiv, "Low-intensity pulsed ultrasound for treating delayed union scaphoid fractures: case series," *Journal of Orthopaedic Surgery and Research*, vol. 10, no. 72, pp. 1–7, 2015.

[18] B. G. Dijkman, S. Sprague, and M. Bhandari, "Low-intensity pulsed ultrasound: Nonunions," *Indian Journal of Orthopaedics*, vol. 43, no. 2, pp. 141–148, 2009.

[19] S. L. J. Júnior, G. L. Camanho, A. C. F. Bassit, A. Forgas, S. J. M. Ingham, and R. J. Abdalla, "Low-intensity pulsed ultrasound accelerates healing in rat calcaneus tendon injuries," *Journal of Orthopaedic & Sports Physical Therapy*, vol. 41, no. 7, pp. 526–531, Jul. 2011.

[20] L. Ren, Z. Yang, J. Song, Z. Wang, F. Deng, and W. Li, "Involvement of p38 MAPK pathway in low intensity pulsed ultrasound induced osteogenic differentiation of human periodontal ligament cells," *Ultrasonics*, vol. 53, no. 3, pp. 686–690, 2013.

[21] T. Iwashina, J. Mochida, T. Miyazaki, T. Watanabe, S. Iwabuchi, K. Ando, T. Hotta, and D. Sakai, "Low-intensity pulsed ultrasound stimulates cell proliferation and proteoglycan production in rabbit intervertebral disc cells cultured in alginate," *Biomaterials*, vol. 27, no. 3, pp. 354–361, 2006.

[22] A. Loyola-Sánchez, J. Richardson, K. A. Beattie, C. Otero-Fuentes, J. D. Adachi, and N. J. MacIntyre, "Effect of low-intensity pulsed ultrasound on the cartilage repair in people with mild to moderate knee osteoarthritis: A double-blinded, randomized, placebo-controlled pilot study," *Archives of Physical Medicine and Rehabilitation*, vol. 93, no. 1, pp. 35–42, 2012.

[23] M. ElHag, K. Coghlan, P. Christmas, W. Harvey, and M. Harris, "The anti-inflammatory effects of dexamethasone and therapeutic ultrasound in oral surgery," *British Journal of Oral and Maxillofacial Surgery*, vol. 23, no. 1, pp. 17–23, 1985.

[24] I. Hashish, W. Harvey, and M. Harris, "Anti-inflammatory effects of ultrasound therapy: Evidence for a major placebo effect," *Rheumatology*, vol. 25, no. 1, pp. 77–81, 1986.

[25] X. Zhao, G. Zhao, Z. Shi, C. Zhou, Y. Chen, B. Hu, and S. Yan, "Low-intensity pulsed ultrasound (LIPUS) prevents periprosthetic inflammatory loosening through FBXL2-TRAF6 ubiquitination pathway," *Scientific Reports*, vol. 7, no. 45779, pp. 1–11, 2017.

[26] W.-S. Su, C.-H. Wu, S.-F. Chen, and F.-Y. Yang, "Low-intensity pulsed ultrasound improves behavioral and histological outcomes after experimental traumatic brain injury," *Scientific Reports*, vol. 7, no. 15524, pp. 1–10, 2017.

[27] L. Zhao, Y. Feng, A. Shi, L. Zhang, S. Guo, and M. Wan, "Neuroprotective effect of low-intensity pulsed ultrasound against MPP+-induced neurotoxicity in PC12 cells: Involvement of K2P channels and stretch-activated ion channels," *Ultrasound in Medicine & Biology*, vol. 43, no. 9, pp. 1986–1999, 2017.

[28] T. El-Bialy, I. El-Shamy, and T. M. Graber, "Repair of orthodontically induced root resorption by ultrasound in humans," *American Journal of Orthodontics and Dentofacial Orthopedics*, vol. 126, no. 2, pp. 186–193, 2004.

[29] E. B. Rego, T. Takata, K. Tanne, and E. Tanaka, "Current status of low intensity pulsed ultrasound for dental purposes," *The Open Dentistry Journal*, vol. 6, pp. 220–225, 2012.

[30] T. El-Bialy, A. Alhadlaq, B. Wong, and C. Kucharski, "Ultrasound effect on neural differentiation of gingival stem/progenitor cells," *Annals of Biomedical Engineering*, vol. 42, no. 7, pp. 1406–1412, 2014.

[31] K. S. Alhazmi, T. El-Bialy, A. R. Afify, L. A. Merdad, and A. H. Hassan, "Ultrasound enhances dentoalveolar remodeling in an ex vivo orthodontic, ovariectomy-induced osteoporotic model," *Ultrasound in Medicine & Biology*, vol. 43, no. 9, pp. 1963–1974, 2017.

[32] C. Rubin, M. Bolander, J. P. Ryaby, and M. Hadjiargyrou, "The use of low-intensity ultrasound to accelerate the healing of fractures," *The Journal of Bone & Joint Surgery*, vol. 83-A, no. 2, pp. 259–270, 2001.

[33] S. Angle, K. Sena, D. Sumner, and A. Virdi, "Osteogenic differentiation of rat bone marrow stromal cells by various intensities of low-intensity pulsed ultrasound," *Ultrasonics*, vol. 51, no. 3, pp. 281–288, 2011.

[34] J. Weidman, "Effects of low intensity pulsed ultrasound and low level heat on bone cells," Master's thesis, Ryerson University, 2010.

[35] N. Heybeli, A. Yeşildağ, O. Oyar, U. K. Gülsoy, M. A. Tekinsoy, and E. F. Mumcu, "Diagnostic ultrasound treatment increases the bone fracture–healing rate in an internally fixed rat femoral osteotomy model," *Journal of Ultrasound in Medicine*, vol. 21, no. 12, pp. 1357–1363, 2002.

[36] Z.-J. Zhang, J. Huckle, C. A. Francomano, and R. G. Spencer, "The effects of pulsed low-intensity ultrasound on chondrocyte viability, proliferation, gene expression and matrix production," *Ultrasound in Medicine & Biology*, vol. 29, no. 11, pp. 1645–1651, 2003.

[37] D. L. Miller, N. B. Smith, M. R. Bailey, G. J. Czarnota, K. Hynynen, I. R. S. Makin, and B. C. of the American Institute of Ultrasound in Medicine, "Overview of therapeutic ultrasound applications and safety considerations," *Journal of Ultrasound in Medicine*, vol. 31, no. 4, pp. 623–634, 2012.

[38] *Accusonic Li-Pus Low Intensity Ultrasound - Ultrasound - Metron*. [Online]. Available: `http://31.222.174.230/metron/ultrasound/accusonic-li-pus-low-intensity-ultrasound_accusonic-lipus.html` (visited on 06/14/2019).

[39] R. Chebli and M. Sawan, "Fully integrated high-voltage front-end interface for ultrasonic sensing applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 1, pp. 179–190, 2007.

[40] S. R. Sanders, E. Alon, H.-P. Le, M. D. Seeman, M. John, and V. W. Ng, "The road to fully integrated DC–DC conversion via the switched-capacitor approach," *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4146–4155, 2013.

[41] V. W.-S. Ng, "Switched capacitor DC-DC converter: Superior where the buck converter has dominated," PhD thesis, University of California at Berkeley, 2011.

[42] L. Svilainis, V. Dumbrava, and A. Chaziachmetovas, "Investigation of the half bridge and transformer push–pull pulser topologies for ultrasonic transducer excitation," *Journal of Circuits, Systems and Computers*, vol. 24, no. 5, pp. 1–13, 2015.

[43] A. Chaziachmetovas, T. E. G. Alvarez-Arenas, and L. Svilainis, "Comparison of direct and transformer drive high voltage ultrasonic pulser topologies," in *IEEE International Conference on Intelligent Data Acquisition and Advanced Computing Systems: Technology and Applications (IDAACS)*, 2017, pp. 1111–1116.

[44] H. Peng, J. Sabate, K. A. Wall, and J. S. Glaser, "GaN-based high-frequency high-energy delivery transformer push–pull inverter for ultrasound pulsing application," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6794–6806, 2018.

[45] L. Svilainis, A. Chaziachmetovas, and V. Dumbrava, "Half bridge topology 500 V pulser for ultrasonic transducer excitation," *Ultrasonics*, vol. 59, pp. 79–85, 2015.

[46] S. Finco, P. Tavares, P. Santos, A. Casimiro, F. Behrens, M. Lanca, and M. C. Simas, "A cost effective smart power approach with NMOS based blocks in standard CMOS technology," in *1998 IEEE International Conference on Electronics, Circuits and Systems. Surfing the Waves of Science and Technology (Cat. No. 98EX196)*, 1998, pp. 135–138.

[47] T. Tanzawa, "Circuit technologies for a single-1.8 V flash memory," in *IEEE Symposium on VLSI Circuits*, 1997, pp. 63–64.

[48] A. Richelli, L. Mensi, L. Colalongo, P. L. Rolandi, and Z. M. Kovacs-Vajna, "A 1.2-to-8V charge-pump with improved power efficiency for non-volatille memories," in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, 2007, pp. 522–619.

[49] Y. C. Wong, T. Arslan, A. T. Erdogan, and A. O. El-Rayis, "Efficient ultra-high-voltage controller-based complementary-metal-oxide-semiconductor switched-capacitor DC–DC converter for radio-frequency micro-electro-mechanical systems switch actuation," *IET Circuits, Devices & Systems*, vol. 7, no. 2, pp. 59–73, 2013.

[50] T. Ying, W.-H. Ki, and M. Chan, "Area-efficient CMOS charge pumps for LCD drivers," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 10, pp. 1721–1725, 2003.

[51] A. Mansano, S. Bagga, and W. Serdijn, "A high efficiency orthogonally switching passive charge pump rectifier for energy harvesters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 7, pp. 1959–1966, 2013.

[52] Z. Hameed and K. Moez, "A 3.2 V–15 dbm adaptive threshold-voltage compensated RF energy harvester in 130 nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 4, pp. 948–956, 2015.

[53] T. Van Breussegem and M. Steyaert, *CMOS integrated capacitive DC-DC converters*. Springer Science & Business Media, 2012.

[54] O.-Y. Wong, W.-S. Tam, C.-W. Kok, and H. Wong, "A novel gate boosting circuit for 2-phase high voltage CMOS charge pump," in *IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC)*, 2009, pp. 250–253.

[55] M. D. Seeman, "A design methodology for switched-capacitor DC-DC converters," PhD thesis, University of California at Berkeley, 2009.

[56] C. Lauterbach, W. Weber, and D. Romer, "Charge sharing concept and new clocking scheme for power efficiency and electromagnetic emission improvement of boosted charge pumps," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 5, pp. 719–723, 2000.

[57] I. Vaisband, M. Saadat, and B. Murmann, "A closed-loop reconfigurable switched-capacitor DC-DC converter for sub-mW energy harvesting applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 2, pp. 385–394, 2015.

[58] D. Ma and R. Bondade, *Reconfigurable switched-capacitor power converters*. Springer-Verlag New York, 2013.

[59] M. Evzelman and S. Ben-Yaakov, "The effect of switching transitions on switched capacitor converters losses," in *IEEE 27th Convention of Electrical and Electronics Engineers in Israel*, 2012, pp. 1–5.

[60] M. S. Haque, M. Mohammad, J. L. Pries, and S. Choi, "Comparison of 22 kHz and 85 kHz 50 kW wireless charging system using Si and SiC switches for electric vehicle," in *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pp. 192–198.

[61] C. Falconi, G. Savone, and A. D'Amico, "High light-load efficiency charge pumps," in *IEEE International Symposium on Circuits and Systems*, 2005, pp. 1887–1990.

[62] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, 1976.

[63] J.-T. Wu and K.-L. Chang, "MOS charge pumps for low-voltage operation," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 4, pp. 592–597, 1998.

[64] T. Nakayama, Y. Miyawaki, K. Kobayashi, Y. Terada, H. Arima, T. Matsukawa, and T. Yoshihara, "A 5 V only one-transistor 256 K EEPROM with page-mode erase," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 4, pp. 911–915, 1989.

[65] K. Sawada, Y. Sugawara, and S. Masui, "An on-chip high-voltage generator circuit for EEPROMs with a power supply voltage below 2 V," in *IEEE Symposium on VLSI Circuits, Digest of Technical Papers*, 1995, pp. 75–76.

[66] J. Liu, A. Bazzini, and S. Gregori, "Fully-integrated PMOS-based charge pumps in standard CMOS process without high-voltage switches," in *IEEE Canadian Conference on Electrical & Computer Engineering*, 2012, pp. 1–4.

[67] T. Das, S. Prasad, S. Dam, and P. Mandal, "A pseudo cross-coupled switch-capacitor based DC-DC boost converter for high efficiency and high power density," *IEEE Transactions on Power Electronics*, vol. 11, pp. 5961–5974, 2014.

[68] B. Rumberg, D. W. Graham, and M. M. Navidi, "A regulated charge pump for tunneling floating-gate transistors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 3, pp. 516–527, 2017.

[69] Z. Luo, M.-D. Ker, W.-H. Cheng, and T.-Y. Yen, "Regulated charge pump with new clocking scheme for smoothing the charging current in low voltage CMOS process," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 3, pp. 528–536, 2017.

[70] Y. Moisiadis, I. Bouras, and A. Arapoyanni, "A CMOS charge pump for low voltage operation," in *IEEE International Symposium on Circuits and Systems*, 2000, pp. 28–31.

[71] K.-H. Cheng, C.-Y. Chang, and C.-H. Wei, "A CMOS charge pump for sub-2.0 V operation," in *IEEE International Symposium on Circuits and Systems*, 2003, pp. V-89-V-92.

[72] F. Su, W.-H. Ki, and C.-Y. Tsui, "Gate control strategies for high efficiency charge pumps," in *IEEE International Symposium on Circuits and Systems*, 2005, pp. 1907–1910.

[73] D.-H. Lee, D. Kim, H.-J. Sing, and K.-S. Min, "A modified Dickson charge pump circuit with high efficiency and high output voltage," *IEICE Transactions on Electronics*, vol. E91-C, no. 2, pp. 228–231, 2008.

[74] R. Pelliconi, D. Iezzi, A. Baroni, M. Pasotti, and P. L. Rolandi, "Power efficient charge pump in deep submicron standard CMOS technology," in *Proceedings of the 27th European Solid-State Circuits Conference*, 2001, pp. 73–76.

[75] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Design of charge pump circuit with consideration of gate-oxide reliability in low-voltage CMOS processes," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 5, pp. 1100–1107, 2006.

[76] H. Peng, N. Tang, Y. Yang, and D. Heo, "CMOS startup charge pump with body bias and backward control for energy harvesting step-up converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 6, pp. 1618–1628, 2014.

[77] B. Razavi, *Design of analog CMOS integrated circuits*. McGraw-Hill Education, 2000.

[78] Y. Allasasmeh and S. Gregori, "High-performance switched-capacitor boost–buck integrated power converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 11, pp. 3970–3983, 2018.

[79] T. Van Breussegem and M. Steyaert, "A 82% efficiency 0.5% ripple 16-phase fully integrated capacitive voltage doubler," in *IEEE Symposium on VLSI Circuits*, 2009, pp. 198–199.

[80] H.-Y. Tang, D. Seo, U. Singhal, X. Li, M. M. Maharbiz, E. Alon, and B. E. Boser, "Miniaturizing ultrasonic system for portable health care and fitness," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 9, no. 6, pp. 767–776, 2015.

[81] K. Hofmann, L. Shen, E. González-Rodrıguez, H. Maune, I. A. Shah, D. Dahlhaus, and R. Jakoby, "Fully integrated high voltage charge pump for energy-efficient reconfigurable multi-band RF-transceivers," in *Intelec*, 2012, pp. 1–4.

[82] B. T. Khuri-Yakub and Ö. Oralkan, "Capacitive micromachined ultrasonic transducers for medical imaging and therapy," *Journal of Micromechanics and Microengineering*, vol. 21, no. 5, pp. 54 004–54 014, 2011.

[83] J. Gallego-Juarez, "Piezoelectric ceramics and ultrasonic transducers," *Journal of Physics E: Scientific Instruments*, vol. 22, no. 10, pp. 804–816, 1989.

[84] D. W. Dye, "The piezo-electric quartz resonator and its equivalent electrical circuit," *Proceedings of the Physical Society of London*, vol. 38, no. 1, pp. 399–458, 1925.

[85] K. S. Van Dyke, "The piezo-electric resonator and its equivalent network," *Proceedings of the Institute of Radio Engineers*, vol. 16, no. 6, pp. 742–764, 1928.

[86] A. Arnau Vives, *Piezoelectric transducers and applications*. Springer, 2004.

[87] A. Alassi, M. Benammar, and D. Brett, "Quartz crystal microbalance electronic interfacing systems: A review," *Sensors*, vol. 17, no. 12, p. 2799, 2017.

[88] V. Khmelev, I. Savin, R. Barsukov, and S. Tsyganok, "Problems of electrical matching of electronic ultrasound frequency generators and electroacoustical transducers for ultrasound technological installations," in *Proceedings 5th International Siberian Workshop and Tutorial*, 2004, pp. 211–215.

[89] F. Yang, C. Wang, H.-M. Lam, Q. Zhao, J. Fan, and S. Zhang, "A floating high-voltage level shifter used in a pre-charge circuit for large-size AMOLED displays," in *IEEE International Conference on Electron Devices and Solid-State Circuits*, 2016, pp. 267–270.

[90] D. Pan, H. W. Li, and B. M. Wilamowski, "A low voltage to high voltage level shifter circuit for MEMS application," in *Proceedings of the 15th Biennial University/Government/Industry Microelectronics Symposium (Cat. No. 03CH37488)*, 2003, pp. 128–131.

[91] J. Rocha, M. Santos, J. D. Costa, and F. Lima, "High voltage tolerant level shifters and DCVSL in standard low voltage CMOS technologies," in *IEEE International Symposium on Industrial Electronics*, 2007, pp. 775–780.

[92] M. Declerq, M. Schubert, and F. Clement, "5 V-to-75 V CMOS output interface circuits," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 1993, pp. 162–163.

[93] J. Doutreloigne, H. De Smet, J. Van den Steen, and G. Van Doorselaer, "Low-power high-voltage CMOS level-shifters for liquid crystal display drivers," in *ICM'99. Proceedings. Eleventh International Conference on Microelectronics (IEEE Cat. No. 99EX388)*, 1999, pp. 213–216.

[94] W.-K. Park, C.-U. Cha, and S.-C. Lee, "A novel level-shifter circuit design for display panel driver," in *IEEE International Midwest Symposium on Circuits and Systems*, 2006, pp. 391–394.

[95] M. Khorasani, L. van den Berg, P. Marshall, M. Zargham, V. Gaudet, D. Elliott, and S. Martel, "Low-power static and dynamic high-voltage CMOS level-shifter circuits," in *IEEE International Symposium on Circuits and Systems*, 2008, pp. 1946–1949.

[96] Y. Moghe, T. Lehmann, and T. Piessens, "Nanosecond delay floating high voltage level shifters in a 0.35μm HV-CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 2, pp. 485–497, 2010.

[97] D. Liu, S. J. Hollis, H. C. Dymond, N. McNeill, and B. H. Stark, "Design of 370-ps delay floating-voltage level shifters with 30-V/ns power supply slew tolerance," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 7, pp. 688–692, 2016.

[98] T. Lehmann, "Design of fast low-power floating high-voltage level-shifters," *Electronics Letters*, vol. 50, no. 3, pp. 202–204, 2014.

[99] G. B. Arfken and H. J. Weber, *Mathematical methods for physicists*. Elsevier, 2005.

[100] Ohmic Instruments, *Digital ultrasound wattmeter UPM-DT-1PA, UPM-DT-10PA, and UPM-DT-1000PA user manual*, 2015. [Online]. Available: `http://www.bcgroupstore.com/Assets/PDF/Manuals/Ohmic_UPM-DT-xPA_Series_User_Manual.pdf`.

[101] M. Garcia-Rodriguez, J. Garcia-Alvarez, Y. Yañez, M. Garcia-Hernandez, J. Salazar, A. Turo, and J. Chavez, "Low cost matching network for ultrasonic transducers," *Physics Procedia*, vol. 3, no. 1, pp. 1025–1031, 2010.

Appendix A

VHDL codes for the FPGA to generate continuous-mode control signals in the proof-of-concept miniaturized LIUS device

digital_control_block.vhd (Top-level file)

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

--clk_in_sys is the system clock, which has a frequency of 12
   MHz

entity digital_control_block is
Port ( clk_in_sys : in STD_LOGIC;
       LIUS_HS : out STD_LOGIC;
       LIUS_LS : out STD_LOGIC;
       Clock1_HS : out STD_LOGIC;
       Clock1_LS : out STD_LOGIC;
       Clock2_HS : out STD_LOGIC;
       Clock2_LS : out STD_LOGIC);
end digital_control_block;

architecture Behavioral of digital_control_block is

component clk_200M_generator is
port (clk_out: out STD_LOGIC; clk_in: in STD_LOGIC);
end component clk_200M_generator;

component LIUS_control_generator is
```

```
Port ( clk_200M : in STD_LOGIC; LIUS_HS : out STD_LOGIC; LIUS_LS
    : out STD_LOGIC);
end component LIUS_control_generator;

component clock_driver_control_generator is
Port ( clk_200M : in STD_LOGIC; clk1HS : out STD_LOGIC; clk1LS :
    out STD_LOGIC; clk2HS : out STD_LOGIC; clk2LS : out
   STD_LOGIC);
end component clock_driver_control_generator;

signal clk_200M: std_logic;

begin

g1: clk_200M_generator port map(clk_200M, clk_in_sys);

g2: LIUS_control_generator port map (clk_200M, LIUS_HS, LIUS_LS)
   ;

g3: clock_driver_control_generator port map( clk_200M, Clock1_HS
   , Clock1_LS, Clock2_HS, Clock2_LS);

end Behavioral;
```

LIUS_control_generator.vhd

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity LIUS_control_generator is
    Port ( clk_200M : in STD_LOGIC;
           LIUS_HS : out STD_LOGIC;
           LIUS_LS : out STD_LOGIC);
end LIUS_control_generator;

architecture Behavioral of LIUS_control_generator is

signal LIUS_HS_signal: STD_LOGIC := '1';
signal LIUS_LS_signal: STD_LOGIC := '0';

begin

LIUS_HS<=LIUS_HS_signal;
LIUS_LS<=LIUS_LS_signal;
```

```
process (clk_200M) is

variable count : integer :=0;

begin

if rising_edge (clk_200M) then
count:=count+1;

if count=65 then

LIUS_LS_signal<='1';
elsif count=67 then
LIUS_HS_signal<='0';
elsif count=132 then
LIUS_HS_signal<='1';
elsif count=134 then
LIUS_LS_signal<='0';
count:=0;

end if;

end if;

end process;

end Behavioral;
```

clock_driver_control_generator.vhd

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity clock_driver_control_generator is
    Port ( clk_200M : in STD_LOGIC;
           clk1HS : out STD_LOGIC;
           clk1LS : out STD_LOGIC;
           clk2HS : out STD_LOGIC;
           clk2LS : out STD_LOGIC);
end clock_driver_control_generator;

architecture Behavioral of clock_driver_control_generator is
```

```
signal clk1HS_signal: STD_LOGIC := '1';
signal clk1LS_signal: STD_LOGIC := '0';
signal clk2HS_signal: STD_LOGIC := '1';
signal clk2LS_signal: STD_LOGIC := '0';

begin

clk1HS<=clk1HS_signal;
clk1LS<=clk1LS_signal;
clk2HS<=clk2HS_signal;
clk2LS<=clk2LS_signal;

process (clk_200M) is

variable count : integer :=0;

begin

if rising_edge (clk_200M) then
count:=count+1;

if count=1 then

clk1LS_signal<='1';
clk2HS_signal<='0';
elsif count=5 then
clk1LS_signal<='0';
clk2HS_signal<='1';
elsif count=6 then
clk1HS_signal<='0';
clk2LS_signal<='1';
elsif count=10 then
clk1HS_signal<='1';
clk2LS_signal<='0';
count:=0;

end if;

end if;

end process;

end Behavioral;
```