University of Alberta

A LOW-VOLTAGE, LOW-POWER INTRAOCULAR PRESSURE MEASUREMENT INSTRUMENT

by

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Abstract

Wireless sensing of abnormal intraocular pressure (IOP) levels associated with Glaucoma, a leading cause of blindness, was first proposed in the late 1960's. While much research has been applied in the intervening time, a suitable commercially available wireless IOP monitoring instrument remains unavailable.

The primary difficulty in developing a wireless IOP instrument is reduction of instrument size and power requirements. For implantation, the instrument is desired to be on the order of a few square millimeters. With such a small instrument, achieving biocompatible operation during electromagnetic field exposure necessary for inductively transferred wireless-power requires very low-power, low-voltage operation. This research presents a 325 mV, sub-μW capacitive-to-digital converter with power levels suitable for near-field wireless power operation with using an integrated circuit coil. This low-voltage, low-power operation creates the opportunity for a monolithic, millimeter-scale IOP monitoring instrument using integrated circuit technologies.

The designed capacitive sensing circuitry uses $\Sigma\Delta$ modulation to perform capacitance-to-digital conversion. The modulator is implemented with fully-differential switched-capacitor circuits. Operational transconductance amplifiers required for the modulation are implemented with subthreshold inverters. Experimental testing shows the prototype instrument, comprised of the designed modulator and commercial capacitive pressure sensors, is capable of resolving 2.1 mmHg while operating at 325 mV using only 30 nW. In comparison with other systems in the field of IOP monitoring, this work represents the lowest operating voltage and power consumption reported to date.

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LIST OF SYMBOLS

A_o amplifier open loop gain.

C_1 reference MEMS sensing capacitor.

C_2 variable MEMS sensing capacitor.

C_3 direct capacitor to second integrator.

C_4 sample-and-hold capacitor to second integrator.

C_L integrator total load capacitance.

C_{coil1} primary-coil capacitance.

C_{coil2} secondary-coil capacitance.

C_h holding capacitor.

C_{int1} integrating capacitance at first integrator.

C_{int1} integrating capacitance at second integrator.

C_{int} integrating capacitance.

C_{load} integrator output load capacitance.

C_m on-chip matched capacitor.

C_{pi} integrator parasitic input capacitance.

C_{po} integrator parasitic output capacitance.

C_{rect} rectifier input capacitance.

C_s sampling capacitance.

$E(Q_{cs}^2)$ mean square charge noise on sampling capacitor.

$E(V_{cs}^2)$ mean square voltage noise on sampling capacitor.

E_1 additive error of internal ADC.

E_2 additive error of internal DAC.

I_{DS} transistor drain-source current.

K_1 gain of first integrator to C_s.

K_3 gain of second integrator to C_3.

K_4 gain of second integrator to C_4.

$Q_{in_{rms}}$ input signal charge power.

R_{2s} secondary coil series resistance.

R_{on} switch on-resistance.

R_{rect} rectifier input resistance.

SNR_q signal-to-noise ratio due to quantization noise.

$S_{ito}(f)$ transistor drain-current noise power spectral density.

$S_{vtR_{on}}(f)$ switch on-resistance noise power spectral density.

V_2 secondary coil terminal voltage.

V_{CM} common mode voltage.

V_{DDCOMP} comparator voltage supply.

V_{DDIO} level-shift voltage supply.

V_{DD} integrator, switches and logic power supply.

V_{DS} transistor drain-source voltage.

V_{GS} transistor gate-source voltage.

V_T transistor threshold voltage.

V_{in_p} peak input voltage.

V_{in} input voltage.

V_{offset} offset voltage.

V_o output voltage.

V_{refC1} reference voltage for reference MEMS capacitor.

V_{refC2} reference voltage for sensing MEMS capacitor.

V_{ref} reference voltage.

W/L transistor width to length ratio.

ΔC_{cal} calibration dummy capacitive difference.

ΔC differential sensing capacitance.

α inverse of amplifier open loop gain.

β_{fb} integrator closed-loop feedback factor.

μc_{ox} transistor transconductance.

μ transistor carrier mobility.

ϕ_1 phase one of four-phase non-overlapping clock.

ϕ_2 phase two of four-phase non-overlapping clock.

ϕ_3 phase three of four-phase non-overlapping clock.

ϕ_4 phase four of four-phase non-overlapping clock.

ϕ_A input sampling clock A.

ϕ_B input sampling clock B.

ϕ_C input sampling clock C.

ϕ_D input sampling clock D.

$\tau_{R_{on}}$ transistor switch and capacitor time constant.

τ_{int} integrator closed-loop time constant.

a_1 gain of feedforward path of first integrator.

a_2 gain of feedforward path of second integrator.

b_2 gain for feedback to second integrator.

c_{ox} transistor gate capacitance.

$f_{3dB_{sw}}$ transistor switch 3 dB frequency.

f_s clock frequency used to generate four phase clocks.

f_u amplifier unity-gain frequency.

gm_N transconductance of NMOS transistor.

gm_P transconductance of PMOS transistor.

kT product of Boltzmann constant and temperature.

k_1 gain of internal ADC.

k_2 gain of internal DAC.

r_{oN} output resistance of NMOS transistor.

r_{oP} output resistance of PMOS transistor.

t_d delay time.

v_{o1} output of the first integrator.

ADC analog to digital converter.

AS1-MEMS die-level prototype instrument.

AS1TB1 test board for AS1.

BMP085 BOSCH high performance pressure and temperature sensor.

BW bandwidth.

C/D capacitance to digital.

C/F capacitance to frequency.

C/I capacitance to current.

C/V capacitance to voltage.

CDS correlated double sampling.

CLT central limit theorem.

CMOS complementary metal oxide semiconductor.

CR charge rebalance.

DAC digital to analog converter.

DIP dual in-line package.

DUT device under test.

ENOB effective number of bits.

FCC federal communications commission.

FOM figure of merit.

FS full scale.

IC integrated circuit.

IEEE institute of electrical and electronics engineers.

IOP intra-ocular pressure.

lpnfet low-power n-type field-effect transistor in the IBM 0.13 μm technology.

lppfet low-power p-type field-effect transistor.

MEMS micro electro-mechanical system.

MIM metal-insulator-metal.

N number of bits used in the mean-estimate.

nfet regular n-type field-effect transistor.

NMOS n-type metal oxide semiconductor.

NTF noise transfer function.

OSR oversampling ratio.

pfet regular p-type field-effect transistor.

PFM pulse to frequency modulation.

PMOS p-type metal oxide semiconductor.

PSD power spectral density.

PWM pulse width modulation.

RFID radio frequency identification.

SAR successive approximation register.

SC switched capacitor.

SNDR signal to noise and distortion ratio.

STF signal transfer function.

TNinv n-type transistor in the inverter amplifier.

TPinv p-type transistor at the inverter amplifier.

VNCAP vertical natural capacitor.

Y modulator transfer function output.

z z-domain discrete-time variable.

CHAPTER 1

INTRODUCTION

Wireless monitoring of physiological parameters is an important application of electronics in health care and disease research. The field of wireless monitoring in medical applications began over 35 years ago with the wireless observation of the fetal heart rate [1]. Since then, the number of applications has increased to include blood pressure, core body temperature, respiration rate, blood oxygen saturation and much more [2, 3]. In addition to in-hospital use, wireless monitoring is applicable for use in home-care and remote-care monitoring where acquired health data can be transmitted using telecommunications technologies [4, 5]. The convergence of advanced technologies applied to medical monitoring has great potential to decrease health care cost, improve patient care, and improve our understanding of disease processes. Toward the advancement of wireless health monitoring, however, a first and necessary step is always the development of appropriate instrumentation.

Instrumentation for the biomedical application of wireless intraocular pressure (IOP) measurement has received considerable research attention [6–15]. IOP measurement is used to monitor abnormal pressure that occurs with glaucoma disease. The term "glaucoma disease" is used to generally describe a collection of specific disease mechanisms that result in poorly controlled intraocular pressure. In a healthy eye, pressure is physiologically regulated at approximately 10–20 mmHg above ambient atmospheric levels; in a diseased eye, pressure can reach up to 50 mmHg above ambient [16,17]. Indicators for disease development include both diurnal pressure variations and elevated average pressures over several days [18]. Worldwide, glaucoma is the second leading cause of blindness and, due to an aging population, it is the leading cause of blindness in developed countries [19]. While research into wireless IOP measurement has produced several promising instrumentation efforts, none have successfully met all of the challenges.

1.1 IOP Measurement

Clinical measurement of IOP is currently done with applanation tonometry. Applanation tonometry works by measuring both the deflection and the applied force used to flatten the corneal tissue (either through direct contact or air-puff pressure application). The indirectness of this measurement technique introduces considerable patient-to-patient variability, primarily due to individual differences in corneal tissue [20–22]. Tonometry methods can have up to 4 mmHg variation between patients and variation of several mmHg between different tonometry techniques [20]; absolute accuracy of any particular tonometry technique is usually verified on mouse studies. The main shortcoming of tonometry techniques, however, is not inaccuracy

but an inability to obtain sufficient samples over time to monitor diurnal pressure variation and average-pressure variation over several days, both of which are risk factors for disease.

Implanted directly in the eye, a wireless pressure sensing microsystem could provide accurate pressure measurement. As it can occur outside of a clinical setting, an implanted monitoring device could also take frequent measurements. An idealised IOP measurement system is shown in Fig. 1.1. The system consists of external (reader) electronics that both transmits power and receives data, and internal implant electronics at the IOP measurement instrument (tag)[1]. The implant electronics performs the pressure measurement operation and communicates the result back.

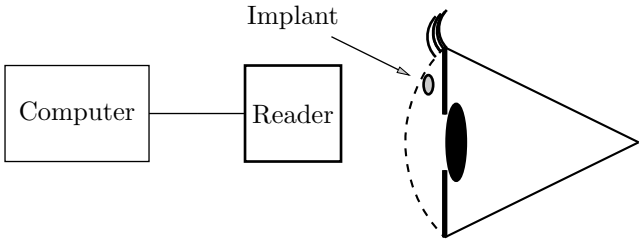

Figure 1.1: Diagram of eye with preferred instrument location shown. The reader both powers the implant and receives data. The data is transmitted to a computer where it can be viewed and stored.

An implanted device for IOP measurement was first suggested by Collins [23] in 1967. In the intervening 45 years, engineering research has pursued both passive electronic [8,10,11], and active electronic solutions [6,13–15,24,25], as well as strain based [26] and optical [27] methods. At the time of writing, commercial development has proceeded only in an external, contact-lens based, indirect measurement system; a commercially available implanted wireless IOP monitoring instrument remains

[1]The terminology of reader/tag are associated with radio-frequency identification (RFID).

unavailable.

The key challenge of developing an implanted IOP measurement instrument is the reduction of the instrument size and power requirements. To preserve eye tissue for later surgeries required during disease management, a very small implant is desired. Ideally, the IOP measurement instrument size would be on the order of a cubic millimeter.

1.2 Fully Integrated IOP Measurement

Conceptually, an ultra-small IOP measurement instrument could be constructed using integrated circuit (IC) technologies. A monolithic IC instrument would offer a small form factor and integral packaging for coating with a suitable biocompatable sealant.

Figure 1.2 shows a functional block diagram of an external reader and IOP measurement implant device. The implant is comprised of pressure-sensing circuitry, power rectification and regulation and an integrated antenna for wireless-power reception. As it provides a communication linke, wireless power transfer is the preferred method for powering biomedical implants [28]; the implant is shown with coupled-inductor coils allowing the transfer of power and as well as communication. Communication between coupled coils occurs by load modulation which is achieved by varying the implant coil impedance. The impedance variation is reflected through the coupled coils and recorded at the reader electronics. In Fig. 1.2, the load modulation implementation is shown with a switch in parallel with the coil. The parallel switch changes the inductor coil load as required to transmit digitized data.

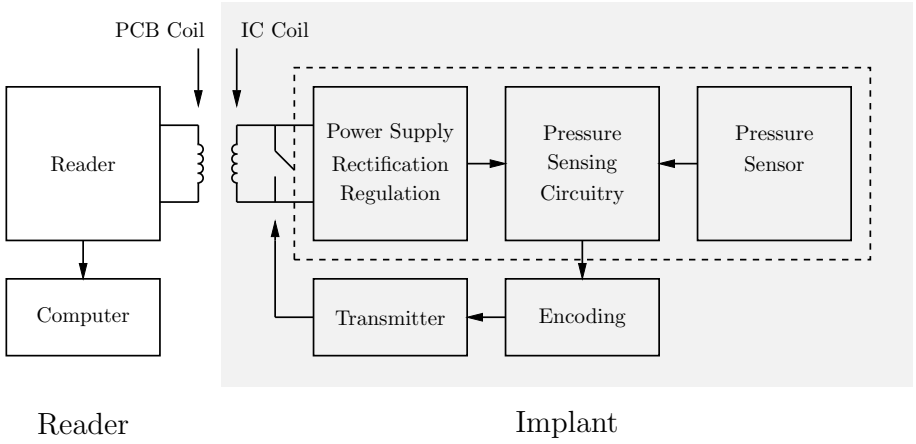

Figure 1.2: Functional block diagram of an ideal IOP measurement instrument consisting of an implant and a reader. Communication is accomplished with load modulation shown with the transmitter and coil switch.

1.2.1 Size Constraints

Because integrated circuit technologies are extremely compact, a fully integrated instrument could be within the millimeter-scale required for medical implantation. With chemical-mechanical polishing, the implant could additionally be made as thin as 60 μm [29]. Such a compact instrument would be ideally suited for a non-invasive implant for IOP measurement.

1.2.2 Power Constraints

While integrated circuit technologies suit the size constraints of IOP measurement, the millimeter-scale size constraint makes obtaining sufficient power difficult.

Wireless power-transfer for powering biomedical implants can occur with near-field inductive transfer or with far-field radiative transfer. Near-field inductive power transfer offers more energy [30] than far-field power transfer, but this energy may

also heat tissue or interferre with surrounding electonics and must be limited. For inductive near-field power transfer, the power-transfer link is typically operated at 13.56 MHz within the industrial, scientific and medical (ISM) band worldwide and exposure levels are regulated through the Federal Communications Commission (FCC) in the United States (see Appendix C). The relatively low frequency of 13.56 MHz avoided tissue loss believed to occur strongly at frequencies much higher than 10 MHz, but generally resulted in large implant antenna. The trade-off between tissue loss and power reception has recently been given more attention with the result that operation in the GHz range may be optimal [31, 32], allowing for reduction in the implant antenna size and operation at higher frequencies.

To the best of the authors knowledge, at the time of writing, there have been no reported cases of fully integrated biomedical implants. A fully integrated implant is one which operates with all circuitry, including the power reception system and antenna coil implemented in integrated circuit technologies. Investigations into wireless power transfer to millimeter-scale coils have resulted in overall power tranfer efficiencies on the order of 0.06–0.8% [33, 34] through roughly 10–15 millimeter of tissue. The power supply system comprised of the antenna, rectifier and load are highly coupled and reported system optimisation is usually based on a preset criteria, such as obtaining a 1.2 V power supply common in RFID systems.

Because many power scavaging systems, including weakly coupled inductive links, intrinsically supply power at low voltage, there is increasing recognition that sensor-interface circuits must target low-voltage operation over performance [28]. For this purpose, ultra low-voltage and low-power circuit techniques are actively being researched [35–39]. While analog circuitry commonly benefits from

operation at higher voltages, there is increasing success in operation in the low voltage region [40] [41]. Data conversion at low-voltage, low-power and low-frequency (in particular) is an area that has little research [36] compared to other forms of data conversion, such as high–accuracy or high–speed conversion, and is a technique highly applicable to low frequency biomedical applications such as IOP measurement.

While fully integrated power-supply systems are being explored for size and power limits, rapid advances are being made in ultra-low voltage analog circuit operation. The answers to such questions as how much power is required to measure elevated IOP, and how much power may be obtained with a millimeter-scale implant, are both areas of active research. A review of power transfer to integrated circuit coils, and biocompatability of operation, is provided in Appendix C.

The following section discusses the range of instrumentation, including the power supply voltage and operating power, currently applied to implantable IOP measurement.

1.3 Prior Work

Due to the fact that there are many ways to achieve the same instrumentation objective and different methods to implement power reception, wirelessly-powered pressure-sensing microsystem reports in general are highly disparate. An overview of instrumentation efforts for IOP measurement can be found in Appendix A. The following paragraphs review the most compact IOP measurement instruments reported using integrated circuit technologies:

Stengel et al, 2001 [24] was an important advancement for IOP measurement. A single integrated circuit (IC) was used for pressure measurement, data storage and calibration operations. The integrated circuit housed the capacitive sensor and measurement electronics and was fabricated in a 1.2 μm CMOS technology. The CMOS die (2.6 mm x 2.6 mm) was flip-chip bonded with a 10.5 mm diameter coil antenna and powered wirelessly in the inductive near-field with a frequency of 13.56 MHz. A resolution of 0.73 mmHg was obtained over a pressure range[2] from 600–975 mmHg. The CMOS pressure sensing circuitry required 210 μW from a 3 V supply. Details of the link performance were not published. Due to the large inductor coil, surgical implantation required replacement of the natural lens.

Irazoqui et al., 2010 [13, 25] created an IOP measurement system using external micro-electro-mechanical-system (MEMS) capacitive sensors. The system used far-field radiation with communication at 2.4 GHz and power at 3.65 GHz. The far-field link was facilitated with an approximately 30 mm long whip antenna, intended to be wrapped around the pupil along the iris resulting in a 16 mm diameter loop. The system required 200 μW at 1.5 V, with the oscillator circuits requiring 160 μW and the reference and regulators requiring 40 μW. A further 1.5 mW was required for intermittent data transmission. A resolution of 0.5 mmHg was obtained.

Wise et al., 2011 [14] reported a highly-integrated IOP measurement instrument combining several technologies, including an external MEMS sensor, CMOS integrated circuits, a miniature solar cell and a thin-film lithium rechargeable battery. The analog circuitry utilised a $\Sigma\Delta$ capacitance-to-digital converter requiring 7 μW

[2]Typical atmospheric pressure is 760 mmHg.

at 3.6 V. Stored data was transmitted on demand with a carrier generating oscillator and amplifier consuming 46 mW. This system obtained 0.5 mmHg resolution, and was energy autonomous (the solar cell satisfied all power needs) at an unspecified lower resolution. The output was calculated from 500k single-bit output data samples from the $\Sigma\Delta$ modulator; the single-bit output data rate was 50 kHz. Without stating the instrument's exact dimensions, the report describes the volume as "cubic millimeter".

Otis et al., 2011 [15] reported the use of a novel low-power reference voltage and a MEMS capacitive pressure sensor to implement a relaxation oscillator technique to measure IOP. For the oscillator, an operating power of 1.74 μW was required at 1.5 V. The band-gap reference and regulators required a balance of 0.56 μW. The instrument was powered in the far-field at 2 GHz, with a 10 mm diameter printed circuit board (PCB) coil antenna. Backscatter communication was used. The instrument measured temperature and capacitance, and was capable of a pressure resolution of 0.9 mmHg.

1.3.1 Summary

Size and power requirements represent the key challenge in developing an implantable IOP measurement instrument. Where wireless power transfer is used, such power must not expose the patient to additional health concerns.

While the earliest work [24] transferred power inductively at 13.56 MHz to a 10.5 mm diameter antenna coil, it did not report radio-frequency (RF) energy exposure levels. The far-field power link reported in [13, 25] met the Federal

Communications Commission (FCC) occupational RF energy exposure levels at 3.65 GHz, but ignored eye-specific health research showing well verified development of hot spots in eye tissue above 600 MHz [42–44]. Tissue radiation exposure was calculated at 2.6 mW/cm^2 in [15], lower than than the permissible level of 6.6 mW/cm^2 at 2 GHz, but this report also ignored the development of hot spots above 600 MHz. In [14], active power transfer was eliminated completely resulting in a compact solar powered instrument. This technique, however, necessitated a communication link that required 46 mW power consumption at the implant; the health impact of thermal transfer from this communication, and the need for eventual battery replacement were not addressed.

Reports reviewed above are summarised below in Table 1.1. While voltage and power levels have decreased since 2001, levels remain relatively high compared to advances in analog circuit design at low-voltage and low-power.

Work	Supply (V)	Power (μW)	Time (s)	Energy	Resolution (mmHg)	Instrument Size
[24]	3.00	210	n/a	n/a	0.7	$\varnothing$10.5 mm
[13, 25]	1.50	160	0.001	0.16 μJ	0.5	$\varnothing$16 mm
[14]	3.60	7	10	70 μJ	0.5	$\approx$ 1 mm^3
[15]	1.50	1.74	n/a	n/a μJ	0.9	$\varnothing$10 mm

Table 1.1: Tabulated summary of reported IOP measurement systems sensing circuitry. Power reported in [24] is for full system rather than sensing circuitry alone.

1.4 Overview of Thesis

This research envisions the possibility of a monolithic, fully-integrated IOP measurement instrument suitable for use with RFID-style wireless-power transfer to a millimeter-scale IC coil, as shown in Fig. 1.3. For the purposes of this project, it is estimated that biocompatable wireless-power transfer at roughly 450 MHz to a millimeter-scale coil inductor will provide only a few μW to the IOP measurement implant circuitry. This dissertation addresses the development of ultra low-voltage, low-power pressure sensing circuitry for the application.

The document proceeds as follows. Chapter 2 reviews pressure-sensing and low-power data-conversion. Chapter 3 describes the system-level design of a capacitance-to-digital converter using $\Sigma\Delta$ modulation. The low-voltage, low-power circuit-level design of the modulator is presented in Chapter 4. Experimental results are given in Chapter 5. Conclusions and future work are described in Chapter 6.

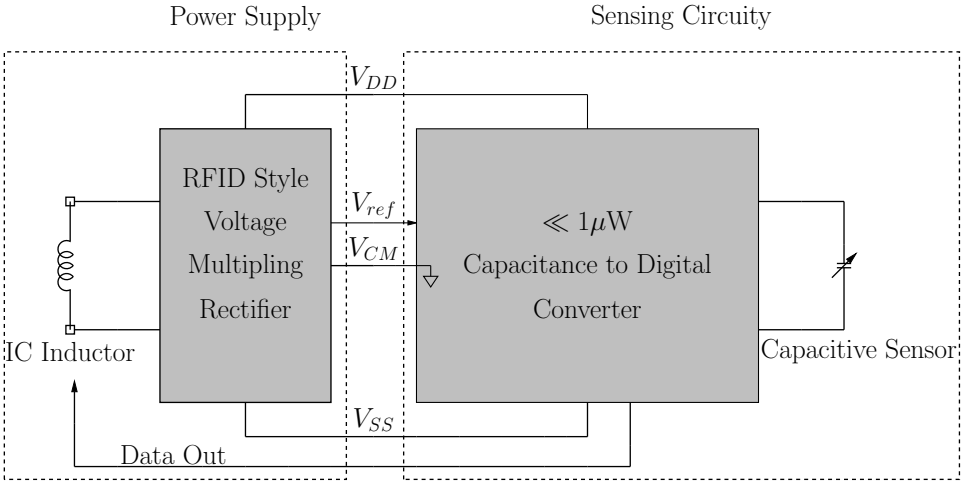

Figure 1.3: Block diagram of a minimalistic IOP measurement instrument including an integrated circuit coil, a voltage multiplying rectifier and low-voltage, low-power pressure sensing circuitry.

CHAPTER 2

LITERATURE SURVEY

In the last chapter, IOP measurement for monitoring abnormal pressures associated with glaucoma disease was described. This Chapter presents a literature review for circuit techniques for pressure sensing and low-voltage, low-power data conversion.

2.1 Instrument Sensing Needs

In a healthy eye, pressure is physiologically regulated at approximately 10–20 mmHg above ambient atmospheric levels; in a diseased eye, pressure can reach up to 50 mmHg above ambient [16, 17]. Risk factors and indicators for disease development include diurnal pressure variation and average pressures obtained over several days [18], neither of which are obtained by infrequent measurement in a clinical setting. Resolution of the pressure to at least 2 mmHg is desired; pressure variations

of 2 mmHg is sufficient for disease research and drug compliance monitoring [45]. The industry-standard IOP measurement technique, Goldmann applanation tonometry, is subject to error from corneal thickness and elasticity variation and other effects [46] and has been shown to have errors as large as 4 mmHg [20]. Detection of approximately 2 mmHg over a 50 mmHg range corresponds to approximately 5 bits of resolution. With sampling desired at an hourly or sub-hourly rate, the pressure variation measurement is essentially a DC signal.

2.1.1 Sensor Selection

While the required pressure resolution of 2 mmHg over a range of 50 mmHg is relatively low, the actual resolution of the circuitry depends on the sensitivity of the sensor[1] used. There are two forms of pressure sensing elements commonly implemented in semiconductor, resistive variation sensors (with piezoresistive response) and capacitive variation sensors.

Piezoresistive sensors work by strain mechanisms which vary the likelihood of electrons to be raised into the conduction band and varies conductive carrier mobility. Capacitive sensors vary the capacitance by controlling the distance of two conductors, typically through deflection of a conductive membrane. Because the response is proportional to deflection, rather than variation of carrier number and mobility due to deflection-induced stress, capacitive pressure transducers are roughly an order of magnitude more sensitive than similarly constructed piezoresistive devices [47–51]. In addition, peak sensitivity of piezoresistive sensors results in relatively

[1] As the output variation is already an electrical quantity, a capacitor transducer is also a capacitive sensor. In the literature, both terms may be used. In this document the term sensor will apply to the transducer.

low (10's kΩ) impedance which necessitates a large quiescent operating currents. Since the capacitive transducer requires no quiescent current, capacitive pressure-sensing circuits can require less power compared to piezoresistive pressure-sensing circuits. In addition, capacitive sensors have the advantage of better temperature stability, less drift and lower sensitivity to packaging stress [52]. The primary disadvantage of capacitive sensors is the increased complexity in the sensor readout electronics.

2.2 Capacitance Measurement

The first thing a capacitive sensor readout circuit must do is to convert the naturally high output-impedance of a capacitor to a measurand with a low output-impedance. Traditionally this is accomplished with a capacitance to voltage C/V converter circuit.

Figure 2.1 shows methods to convert capacitance to voltage. A capacitance-to-voltage conversion (C/V) can be obtained using switched-capacitor (SC) circuits [53–56]. Alternatively, C/V conversion can be accomplished more simply by obtaining a buffered version of a capacitively divided voltage using the a floating gate method [57], or by tracking the voltage of a charging or discharging capacitor. In the former case, two distinct input voltages can determine the capacitive ratio. In the latter case, a variable capacitance can be determined in many ways: controlled timing and end-of-cycle voltage measurement, or differential voltage measurement between a fixed and variable capacitor [24, 58].

In a C/V conversion stage, the accuracy of the conversion is limited by the analog circuitry. With a SC implementation of a C/V conversion stage, analog

circuit error-correction techniques such as correlated double sampling (CDS) can be applied. Correlated double sampling is a technique commonly used in SC circuits to reduce amplifier offset and low-frequency noise. The technique operates by sampling amplifier offset during a clock phase when the amplifier is not in use, and then subtracting this value at a later time. Because offset and low-frequency noise have longer time constants than typical system sampling frequencies, there is a high correlation between the previously sampled offset and the offset at the time of removal [59]. In addition, SC C/V conversion stages can be implemented with stray-insensitive circuit structures. Stray insensitive SC circuit structures are robust to voltage-dependent stray capacitance at the front-end [53].

As a alternative to C/V conversion, a capacitance-to-current (C/I) circuit can be used. This can be constructed easily by placing a variable capacitor at the output of a voltage buffer tracking a charge/discharge voltage from a reference capacitor [60]; the current of the variable capacitor is then proportional to the capacitor ratio. For data storage or transmission, the output of the C/V (or C/I) circuit must be processed to either a digital or a quasi-digital output, such as PWM or pulse-frequency-modulation (PFM).

Direct conversion from capacitance-to-frequency (C/F) is also possible [58, 61–64]. As it is usually implemented with a relaxation oscillator, this technique has the advantage of simplicity but is well known to be sensitive to analog circuit parameters [65]. Depending on the implementation, relaxation oscillators can also be sensitive to stray capacitance, power supply and temperature. To reduce sensitivity to power supply, temperature and other influences, a differential approach is often used

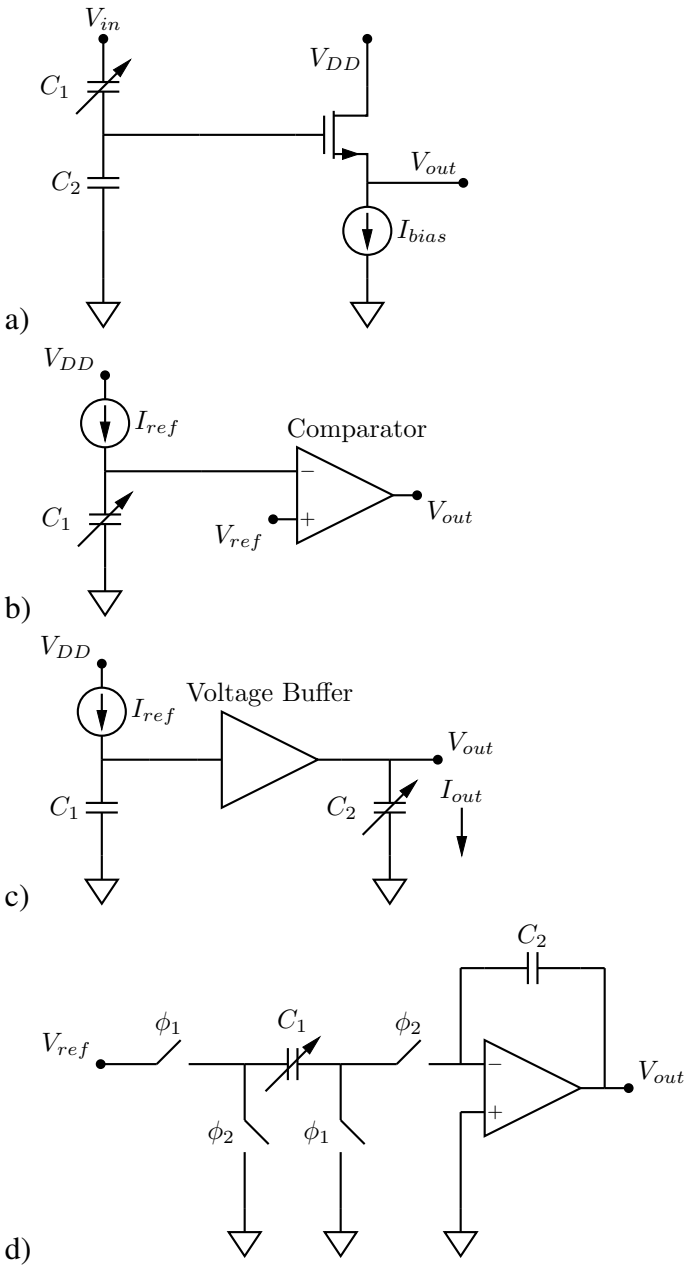

Figure 2.1: Various forms of converting a capacitance to a low output-impedance measurand, including: a) a capacitive divider with voltage buffer (a voltage follower is shown); b) a variable capacitor charged with a fixed reference current where the output of the comparator provides a pulse width modulated PWM signal (reset of the capacitor is required); c) an implementation of a C/I converter where the charging current I_{out} is dependent on the variable capacitor; c) a SC C/V converter where the output $V_{out} = V_{ref}C_1/C_2$ is available at the end of the clock phase ϕ_2.

where the analog circuit parameter, such as current, is used to charge both a sensor and reference capacitance allowing the variation to cancel as the difference signal is observed. Stray insensitive SC based oscillators have been used to improve the performance of C/F conversion [66, 67]. A relaxation oscillator C/F readout circuit has been implemented with a SC C/V conversion stage, followed by a voltage-input relaxation oscillator, allowing for both robustness to stray capacitance and front-end error correction possible with SC circuits [68].

Limitations Circuit error at the C/V (or C/I) conversion stage is often the limiting factor in obtaining high-accuracy capacitance measurement. Even the simplest implementation of a voltage buffer, a single MOS transistor configured as a voltage follower, may contribute to error due to variation in threshold voltage and channel length modulation [57, 60, 69]. In SC circuitry, switch thermal-noise, clock-feedthrough and charge-injection as well as amplifier thermal noise can all adversely impact performance. With off-chip capacitive sensors, readout circuitry is subject to error due to stray capacitance. Readout circuits that use counting methods with a higher frequency clock face additional resolution limits due to limited clock frequency and accuracy.

Observation of accuracy limitations due to analog circuit error lead to the use of a SC $\Sigma\Delta$ modulator for the measurement of capacitive ratio [70, 71], and also for capacitive-sensor readout circuitry [72]. The $\Sigma\Delta$ technique is well known to be robust to analog circuit impairment and is commonly used for high accuracy analog-to-digital conversion (ADC). Using a stray-insensitive switched-capacitor implementation, the modulator front-end is easily suited for use with a capacitive sensor. The $\Sigma\Delta$ technique is now commonly used in capacitive readout circuits

[54, 71–78] as a capacitance-to-digital (C/D) converter.

In addition to the $\Sigma\Delta$ converter, the successive-approximation-register (SAR) data converter has been used as a C/D converter by incorporating the capacitive sensor into a charge re-balancing (CR) front-end using a SC feedback digital-to-analog converter (DAC) [79, 80].

2.3 Low Power Data Conversion & Sensing

Both the SAR and the $\Sigma\Delta$ technique, as well as the lesser used cyclic converter technique, are well known for low-power operation and have been applied in biomedical sensing applications. In some cases, system-level constraints of an application can be used to determine the particular converter type; applications with a large number of multiplexed inputs, for instance, may choose the SAR topology to avoid $\Sigma\Delta$ decimation filter delay.

While there is general understanding of the overlap in application-space of various forms of A/D conversion (i.e. both SAR and $\Sigma\Delta$ are suitable to low-power, low-frequency applications), there is little research on the differences between the conversion techniques within the overlap space. One report from a prominent researcher in the field of SC circuits studied the power effectiveness between the SAR, Cyclic and $\Sigma\Delta$ converters implemented in SC circuitry and specifically applied to low-power capacitive-sensor readout circuits; it was found that, despite the need for oversampling, the $\Sigma\Delta$ technique has the highest power efficiency overall[2] [81]. No related reports were found.

[2]The analysis was completed on the analog circuitry along, without consideration of the digital filter power requirements.

The work reported in [81] was follow-up research after a SAR ADC had been converted for use as CDC. The capacitive sensor was incorporated into the SAR ADC as the MSB capacitor. Reported difficulties included the high parasitic capacitance of the MEMS sensor and overall reduction of capacitor matching in the SAR structure. Due to these difficulties, the resolution of the CDC system (comprised of the ADC plus MEMS capacitive sensor) was two bits lower than the resolution of the SAR ADC alone [82].

2.3.1 Low-power Reports

A survey into reported work shows there are several recent reports of low-power ADC's and capacitive readout circuits:

Low-power ADC's in the biomedical range of a few Hz to a few kHz, frequently use either the SAR or the $\Sigma\Delta$ conversion technique.

For an inductively-coupled wirelessly-powered human-body sensor system, a 10 bit SAR suitable for operation on a 50 kHz bandwidth was reported to consume 2.2μW from a 1.7 V supply [83]. For neural sensing, an adaptive resolution SAR using a 50 kHz bandwidth was reported to consume between 0.23 μW to 0.90 μW from 1.2 V for 3-8 bit resolution [84]. Using MOS transistors working in weak-inversion, a second-order SC $\Sigma\Delta$ data converter applied to the biomedical signal range of 25 Hz, obtained 66 dB (11 bits) resolution consuming 0.14 μW from a 1.2 V supply [85]. For a pacemaker application with a bandwidth of 120 Hz, a third-order SC $\Sigma\Delta$ modulator using subthreshold inverters for operational transconductance amplifiers was reported with a resolution of 72 dB (12 bits) consuming 0.73 μW

from a 1.5 V supply [86]. Also using subthreshold inverter amplifiers in a SC $\Sigma\Delta$ modulator, 56 dB (9.2 bits) resolution for 100 kHz bandwidth was reported using 0.8μW from a 1 V supply [87].

Low-power capacitive readout circuits for the purpose of biomedical sensing applications, are often reported as part of wirelessly-powered system designs. Power consumption and system design are driven by the needs of the application.

Using an SC C/V stage followed by an 11-bit cyclic ADC, a capacitive readout circuit designed for wireless monitoring of mouse blood pressure was recently reported with a resolution of 0.1 mmHg and a power consumption of 18 μW from a 2 V supply [88, 89]. The ADC data rate was 2 kS/s and the sensor capacitance had a nominal value of 2 pF with a sensitivity of 0.7 fF/mmHg. This sensitivity required the circuit resolution to better than 70 aF for 0.1 mmHg resolution. The C/V converter used CDS to reduce front-end circuit error and noise. With 18 μW operation and 2 kS/s, the measurement cycle is 0.5 ms with 9 nJ per conversion.

Several of the lowest power capacitive readout circuits are reported for application in IOP measurement. The capacitive readout circuitry for the IOP measurement system reported in 2011 [14], used a single-order $\Sigma\Delta$ modulator based on SC current-steering. Single bit output was available at a rate of 50 kS/s and the power consumption was 7 μW from a 3.6 V supply. The measurement was ratiometric, comparing the variable capacitor to a fixed capacitance, which offered reduced sensitivity to clock and power supply variation. The IOP measurement reported in 2010 [13], uses a PWM technique. Two matched nano-amp current sources are used to charge a MEMS sensor capacitor and a reference capacitance. The voltage at each charged capacitor is used to trip a schmitt trigger; the time between the two trigger

events is used to form a variable pulse width which is then measured by counting with a higher frequency clock. The nominal value of the capacitive sensor is 5.3 pF and the circuitry power consumption was 160 μW operating power. While this was a high operating power, the measurement cycle was reportedly 1-millisecond resulting in an energy consumption of only 160 nJ for the measurement operation.

RFID-suitable sensor tags for environmental monitoring has produced several low-power wireless systems reports[3]. The systems have traditionally been used for monitoring temperature [90–95], but recent reports have included more sophisticated circuitry such as a low-noise chopper-stabilized amplifier together with an 8-bit SAR ADC intended for biosignal amplification [96]. For capacitive sensing, an RFID ready sensor tag has been reported with a second-order SC $\Sigma\Delta$ readout circuit [97]. The modulator achieved 81.9 dB (13.65 bits) consuming 11.8 μW at 1.2 V. A lower resolution of 11.2 bits was obtained at 0.8 V, power consumption at this voltage was not reported. The capacitive sensor had a nominal value of 3 pF with $\pm$1.5 pF variation. Also for RFID systems, a 12 bit SAR operating with with 6.25 kS/s was reported using 0.85 μW from a 1.2 V supply [98].

2.3.2 Application and Comparison

This section discusses low-power, low-frequency capacitive sensing, describes the commonly used ADC figure of merit (FOM) and provides a tabulation of low-power, low-frequency ADC reports.

[3]RFID suitable sensor tags are communication ready using off-the-shelf commercial RFID readers and often have unique identification numbers to be implemented in clusters.

Application Particular to biomedical sensing is the low-frequency range of the signal. The frequency range of common physiological signals is below 10 kHz and many applications exist within the frequency range of 0 - 100 Hz [99].

Low-power capacitive sensing circuitry is diverse and the implementation often depends on system-level constraints. Performance and power requirements depend strongly on the application and the signal characteristics, including the signal bandwidth, often making direct comparisons difficult. Further, when the rate of conversion is very low, a significant portion of the power consumption can arise from static, or leakage, current. At 10 kHz switching, for instance, leakage current on a near minimum sized inverter with a fan out of four can exceed 50% of the total power consumption [100].

As previously discussed, the two structures most commonly used for low-frequency data conversion are the SAR and the $\Sigma\Delta$. These techniques both require several operational cycles more than the Nyquist rate of operations, hence their suitability and frequent use in conversion of low-frequency signals. Power and voltage within low-power SC $\Sigma\Delta$ modulation has been reduced by the use of low-power subthreshold inverter amplifiers. The subthreshold inverter used as a dynamically-biased amplifier was researched during the early development of switched-capacitor circuits in the 1980's [101–103]. At the time of writing, this technique had not yet been applied to capacitive sensing.

ADC Figure of Merit A commonly used figure of merit (FOM) for analog to digital conversion is a function of the power, bandwidth (BW) and effective number

of bits (ENOB) as follows,

$$FOM = \frac{Power}{2 \times BW \times 2^{ENOB}}. \tag{2.1}$$

This FOM has been widely applied in the comparison of ADC performance. However, obtaining an additional bit requires an incremental amount of power that depends on the architecture which means the FOM should be applied with caution. The FOM can be used reliably to compare similar architectures, or similar resolutions only.

As previously stated, when the rate of conversion is very low, a significant portion of the power consumption can arise from static, or leakage, current making the FOM less applicable to applications with widely ranging frequency of operations. Low-power, low-frequency ADC represents a diversion from the more well-researched consumer-use data converter applications, such as audio converters. Within low-frequency ADC are instrumentation applications, but these are often are very high (16 - 24 bit) resolution which differ from biomedical sensing needs. Table 2.3.2 shows comparative data on reports of analog to digital converters designed for low-frequency applications.

Report	[104]	[82]	[85]	[99]	[86]	[100]
Year	2003	2006	2008	2009	2009	2012
Technology [μm]	0.18	0.8	0.5	0.35	0.35	0.13
Voltage [V]	0.5	2.5	1.2	1	1.5	1 & 0.4
Power [μW]	0.85	3	0.140	0.23	0.73	0.053
Architecture	SAR	SAR	$\Sigma\Delta$	SAR	$\Sigma\Delta$	SAR
Data Rate kS/s	4.1	0.8	0.05	1	0.24	1
Signal BW [Hz]	2000	400	25	500	120	500
SNDR [dB]	43.3	56	61	63	65	56
FOM [pJ/step]	1.8	7.2	2.7	0.2	2.1	0.095

Table 2.1: Low-power, low-frequency analog-to-digital converters. The data rate shows rate of full resolution output for SAR and $\Sigma\Delta$. The reported $\Sigma\Delta$ modulators did not include power requirements for digital filtering.

2.4 Summary

The challenge of low-power capacitive readout circuitry is similar to the challenge of low-power ADC design. For low-power ADC, as well as for capacitive readout circuitry, SC circuits have gained popularity. Implementation with SC circuitry enables front-end analog circuit error-correction for increased accuracy. Research into the power differences between the SAR, Cyclic and $\Sigma\Delta$ converters implemented in SC circuitry for the specific purpose of low-power capacitive sensor readout circuits, has shown the $\Sigma\Delta$ technique has the highest power efficiency overall[4], despite the need for oversampling [81].

From the literature, there are several circuit methods that can be applied toward development of a low power capacitive readout circuit. With both low-power and low-voltage operation possible, use of subthreshold inverters is of interest. Use of

[4]The analysis was completed on the analog circuitry along, without consideration of the digital filter power requirements.

a subthreshold inverter amplifier has recently come back into research interest for low-power data conversion.

For a wirelessly-powered IOP measurement instrument, low-power consumption *and* low-voltage operation are both important. Also relevant is the total energy per conversion. The energy per conversion in recent IOP measurement reports varied from 160 nJ to 70 μJ; the time taken for these measurements was 1 ms and 10 s at power levels of 160 μW and 7 μW respectively. To achieve an operating power suitable to a millimeter-scale IC coil antenna, a measurement time of several seconds and a higher energy per conversion may be an acceptable trade-off.

CHAPTER 3

CAPACITANCE TO DIGITAL CONVERTER DESIGN

This Chapter describes the system-level design of the capacitance-to-digital converter. First, the options for sensing circuit architecture are discussed in Sec. 3.1. Next, the commercial capacitive sensor purchased for system integration is described in Sec. 3.2. The second-order $\Sigma\Delta$ modulator design used in the capacitance-to-digital converter is described in Sec. 3.3. The charge-sensing input stage of the modulator is described in more detail in Sec. 3.4 and the expected circuit performance is discussed in Sec. 3.5.

3.1 Sensing Circuit Architecture

As discussed in the previous chapter, capacitive sensing can encompass several different circuit techniques and implementations including direct conversion at the front-end of a switched-capacitor analog-to-digital converter. Analog-to-digital converters suitable to low-power, low-frequency operation are the SAR and $\Sigma\Delta$ modulator. These converter forms require several internal cycles for each conversion, and have been shown to be implemented with very low-power. The $\Sigma\Delta$ modulator is well known to be robust to operation with with low-gain amplifiers [105]. Low-gain amplifiers are anticipated with the low-voltage operation desired for this project. In addition, the single-bit $\Sigma\Delta$ modulator is suitable for the purpose of implantation with single-bit data transferred out of the wireless implant; the single-bit data stream of the $\Sigma\Delta$ modulator alleviates need for data package management, reducing the overall ancillary circuit support. In the case of capacitive sensing using switched-capacitor circuits, research has indicated that, despite the need for oversampling, the $\Sigma\Delta$ modulator is more power efficient than the SAR [81]. For these reasons, the $\Sigma\Delta$ modulator was chosen for the project. At the time of this decision and design of the modulator, the $\Sigma\Delta$ modulation technique had not yet been applied to IOP measurement. To reduce the likelihood of so called ”dead zones” where the modulator is unresponsive to changes in DC inputs, second-order modulation was selected; first order modulators with DC (inactive) inputs are most highly prone to dead zones [106, 107]. The likelihood of dead-zones is increased with leaky integrators which can result from the use of low-gain amplifiers as is anticipated in this project.

3.2 Commercial MEMS Capacitive Sensor

Fully-integrated CMOS capacitive pressure sensors have been demonstrated in other reports [24], but because of technology constraints they are unavailable for this project. A commercial capacitive MEMS pressure sensor (E1.3N, microFAB Bremen) has been purchased for the system development. The sensor physical dimensions are (1.2 mm x 0.6 mm) in length and width respectively, including bond-pad area for wire bonding. The sensor has a height of 0.5 mm. At atmospheric pressure, the nominal static capacitance is approximately 6 pF. The sensitivity in the pressure range of interest is 0.6 fF/mmHg. To observe pressure changes of 2 mmHg, it is required to resolve 1.2 fF. The full-scale sensor output response for approximately 50 mmHg applied pressure difference is 30 fF.

3.3 Capacitive Sensing $\Sigma\Delta$ Modulation

This section describes the capacitive-to-digital converter $\Sigma\Delta$ modulator. The general operation of a second-order $\Sigma\Delta$ modulator is described in Appendix D. A single-bit $\Sigma\Delta$ modulator loop attenuates the in-band contribution of large quantization errors at the comparator. Closed-loop feedback of a $\Sigma\Delta$ modulator is constructed with integrators and the loop is well known to be very robust to low-gain amplifiers. For second-order modulation, increased in-band quantization noise power is less than 1 dB if the amplifier DC gain is comparable to the oversampling ratio [105].

The purpose of the $\Sigma\Delta$ modulator is to encode the DC pressure signal and minimize the impact of the quantizer noise at the receiver. While the quantizer noise is minimized by the loop noise-shaping transfer function, the modulator front-end

circuit noise is transferred unattenuated to the output. The front-end circuit noise will be addressed in Chapter 4.

To modify a $\Sigma\Delta$ modulator to be a capacitive-sensor the front-end capacitors, normally switched to a varying voltage, may be replaced with sensor capacitances switched to a fixed voltage [72]. While the modulator loop itself generally does not require modification, some structures have modified the loop for the purpose. A $\Sigma\Delta$ modulation for high accuracy on-chip capacitive ratio testing was reported in [70] where a bilinear stage [108] was used at the second integrator.

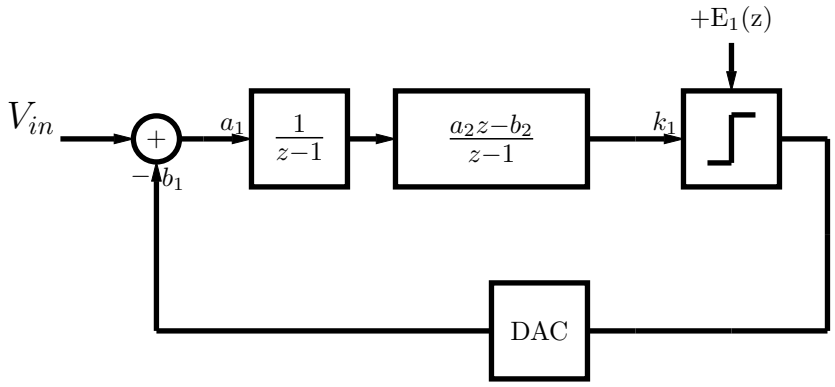

Figure 3.1: Second-order $\Sigma\Delta$ modulator modified with a bilinear transform at the second integrator.

The use of the bilinear stage in [70] avoids insertion of the feedback voltage into the second integrator. In this project, the reference-feedback voltage is expected to be the power-supply voltage. Front-end sampling only of the feedback-voltage allows the loop to avoid sampling variations if the power-supply voltage is varying; the sampled input-charge is taken at similar time-points, other variations due to power-supply variation are introduced solely through second-order effects.

3.3.1 Improvements for Power Reduction

While the capacitive sensing modulator in [70] is capable of determining a capacitive-ratio to high-accuracy, the front-end design is such that charge from the full input-capacitance is sampled and introduced to the modulator. As shown in Fig. 3.2, the input capacitors C_1 and C_2 are compared with each other, but each introduced full sampled charge to the integrator. To maintain the properties of the loop, the integration capacitance is required to be $1/a_1$ times the larger of C_1, or C_2 or $1/a_1(C_1+C_2)$ if the input capacitors are similar in size. With large sensor capacitors, this would produce a large power consumption at the first integrator.

To reduce power consumption, the loop was modified so that only a difference charge is introduced to the modulator. Capacitors C_1 and C_2 are sampled to the reference voltage, V_{ref}, but only the differential charge is introduced into the summing junction as shown in Fig. 3.3. This charge is balanced with the introduction of a third capacitor for sampling, C_s. The sampling capacitor C_s supports the feedback signal path and is designed to exceed the expected span of the difference capacitance Δ C = $(C_1 - C_2)$ where C_1 is the sensor capacitor and $C_2 \approx C_1$ is a reference capacitor. In general, the sensitivity of capacitive sensors is low and the static capacitance far exceeds the dynamic capacitance, $\Delta C \ll C_{1,2}$. Using the differential approach, the modulator circuitry may be designed to be responsive to the scale of the dynamic capacitance rather than the scale of the static capacitance. The first stage integrator capacitance is required to be $\frac{1}{a_1}C_s$ where $C_s > \Delta C$ to ensure that the modulator input range is not exceeded.

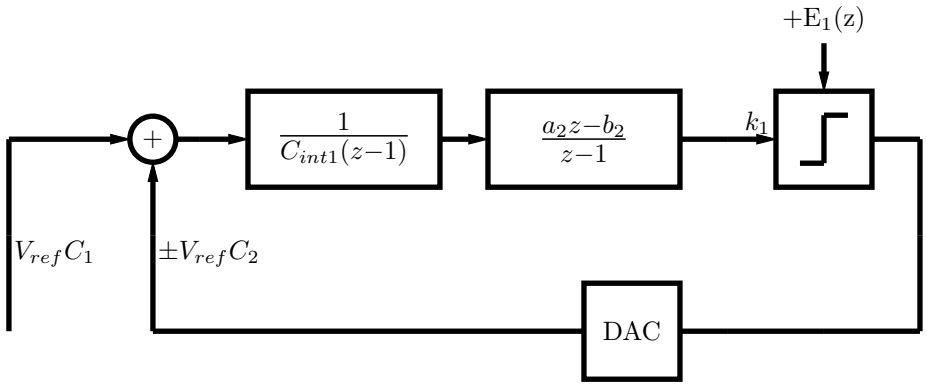

Figure 3.2: $\Sigma\Delta$ modulator used for capacitive-ratio measurement. Capacitors C_1 and C_2 are compared to each other with the difference between the two capacitors represented in the output bit-stream average value.

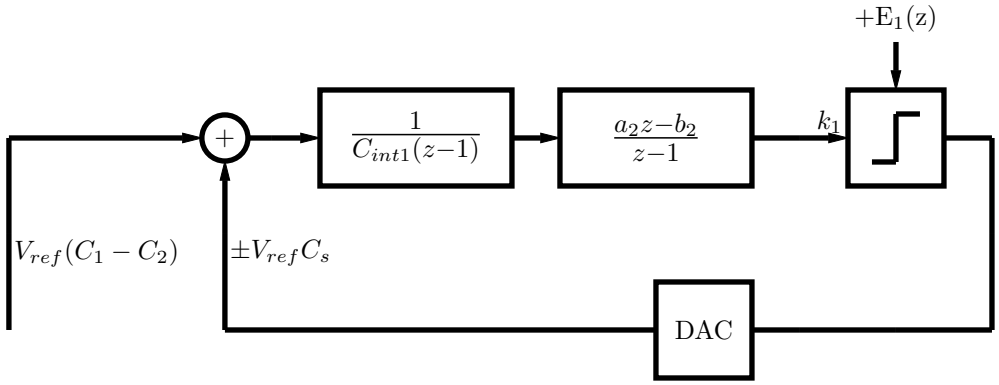

Figure 3.3: Modified low-power $\Sigma\Delta$ modulator used for capacitive sensing. The difference capacitance $\Delta C = C_1 - C_2$ is compared to C_s and result is represented in output bit-stream average value. The capacitor C_s is required to span the range of the expected difference capacitance and C_{int1} is scaled to C_s. The capacitor C_s can be made much smaller than either C_1 or C_2 which represent the static capacitance of the sensor.

3.3.2 Integrator Gain Scaling

The modulator loop fully implemented with capacitive-ratio gain scaling is shown Figure 3.4. This section will determine the capacitive ratio relations which control the loop equations and the integrator gain scaling.

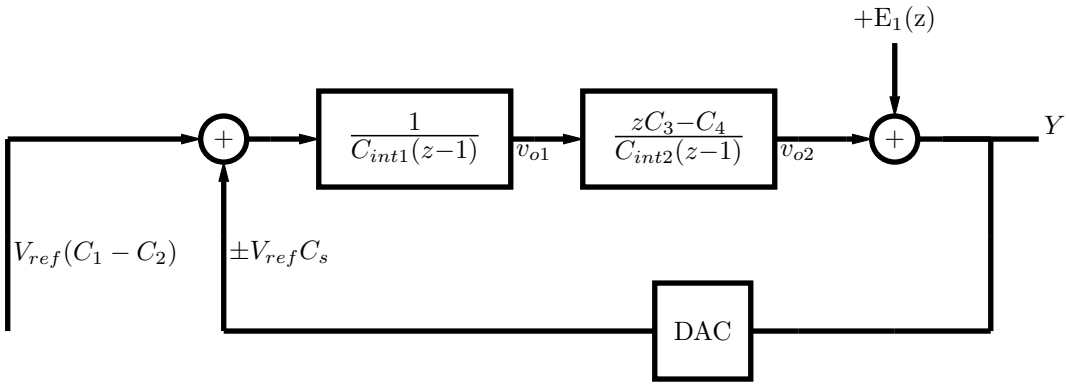

Figure 3.4: Modified modulator shown with capacitor scaling elements.

The first integrator takes charge from the input capacitor, C_s, and the difference capacitance between the reference and varying capacitors, $\Delta C = (C_1 - C_2)$ as follows,

$$v_{o1}(n+1) - v_{o1}(n) = y(n)V_{ref}\frac{C_s}{C_{int1}} + V_{ref}\frac{\Delta C(n)}{C_{int1}}, \tag{3.1}$$

where v_{o1}(n) is the output sample of the first integrator and $y(n)$ is the output sample of the modulator taken at the n^{th} clock cycle. The value $y = 0$ reverses the charge sampling polarity compared with the value $y = 1$. The term $y(n)V_{ref}$ is used for the analysis. Without loss of generality, let $V_{ref} = 1$ for the analysis.

The second integrator takes charge from both the previously integrated value of

v_{o1}, with the use of a sample and hold, and the current value,

$$v_{o2}(n+1) - v_{o2}(n) = \frac{C4}{C_{int2}} v_{o1}(n) - \frac{C3}{C_{int2}} v_{o1}(n+1) \tag{3.2}$$

This enables the second integrator to obtain content from both the input signal and output y, as is required for stable modulation. Substituting Eq. 3.1 into Eq. 3.2 and simplifying,

$$v_{o2}(n+1) - v_{o2}(n) = \left[\frac{C_4}{C_{int2}} - \frac{C_3}{C_{int2}}\right] v_{o1}(n) - \frac{C_3}{C_{int2}} \left[y(n)\frac{C_s}{C_{int1}} + \frac{\Delta C(n)}{C_{int1}}\right]. \tag{3.3}$$

The z-transform of the second integrator output is,

$$V_{o2}(z) = \frac{1}{z-1}\left[\left(\frac{C_4}{C_{int2}} - \frac{C_3}{C_{int2}}\right) V_{o1}(z) - \frac{C_3 C_s}{C_{int2} C_{int1}} Y(z) - \frac{C_3}{C_{int2}} \frac{\Delta C(z)}{C_{int1}}\right]. \tag{3.4}$$

And the z-transform of the first integrator is,

$$[v_{o1}(n+1) - v_{o1}(n)] \rightarrow V_{o1}(z) = \frac{1}{z-1}\left[Y(z)\frac{C_s}{C_{int1}} + \frac{\Delta C(z)}{C_{int1}}\right]. \tag{3.5}$$

Rewriting Eq. 3.4 produces,

$$\begin{aligned} V_{o2}(z) = &\left[\frac{C_4 - C_3}{C_{int2}} \frac{1}{(z-1)^2} - \frac{C_3}{C_{int2}} \frac{1}{(z-1)}\right] \frac{\Delta C}{C_{int1}} \\ &+ \left[\frac{(C_4 - C_3)}{C_{int2}} \frac{C_s}{C_{int1}} \frac{1}{(z-1)^2} - \frac{C_3 C_s}{C_{int2} C_{int1}} \frac{1}{(z-1)}\right] Y(z) \end{aligned} \tag{3.6}$$

The modulated output $Y(z)$ can be expressed as the output of the second integrator

plus the comparator quantization noise,

$$Y(z) = V_{o2}(z) + E(z) \tag{3.7}$$

where $E(z)$ is the transformed quantization error. Thus,

$$\begin{aligned} Y(z) = &\left[\frac{C_4 - C_3}{C_{int2}(z-1)^2} - \frac{C_3}{C_{int2}}\frac{1}{(z-1)}\right]\frac{\Delta C}{C_{int1}} \\ &+ \left[\frac{(C_4 - C_3)C_s}{C_{int2}C_{int1}(z-1)^2} - \frac{C_3 C_s}{C_{int2}C_{int1}}\frac{1}{(z-1)}\right]Y(z) \\ &+ E(z). \end{aligned} \tag{3.8}$$

This can be further simplified to:

$$\begin{aligned} \text{LHS} &= Y\left((z-1)^2 - \left(\frac{C_4 - C_3}{C_{int2}}\right)\frac{C_s}{C_{int1}} + \frac{C_3 C_s}{C_{int2}C_{int1}}(z-1)\right) \\ \text{RHS} &= \left[\frac{C_4 - C_3}{C_{int2}} - \frac{C_3}{C_{int2}}(z-1)\right]\frac{\Delta C}{C_{int1}} + E(z)(z-1)^2. \end{aligned} \tag{3.9}$$

Differentiation of the quantization noise is obtained by setting the LHS equal to only a delay as follows,

$$\left(z^2 + z\left(\frac{C_3 C_s}{C_{int2}C_{int1}} - 2\right) + (1 - \frac{C_s}{C_{int1}}\frac{C_4}{C_{int2}})\right) = z^2. \tag{3.10}$$

The capacitive ratio C_s/C_{int1} is the gain of the first integrator to the input sampling capacitor, C_s. The ratio C_s/C_{int1} is now expressed as k_1. Ratios C_3/C_{int2} and C_4/C_{int2}, the gains of the second integrator to capacitors C_3 and C_4 respectively, are expressed as k_3 and k_4. Eq.3.10 represents an under specified system of two

equations with three unknowns,

$$k_3 k_1 = 2 \tag{3.11}$$

$$k_1 k_4 = 1. \tag{3.12}$$

In this system, one unknown may be freely chosen. The first integrator gain is set to $k_1 = 1/2$ which provides a reasonable integration range. This sets the following values for all integrator gains:

$$k_1 = 1/2 \tag{3.13}$$

$$k_3 = 4 \tag{3.14}$$

$$k_4 = 2. \tag{3.15}$$

Note that while the ratio of k_3 to k_4 is important, the actual gain at the second integrator is unimportant as it is followed by a single bit comparator. Because the single bit comparator is a highly non-linear element with dynamic gain, the integrator proceeding it can have arbitrary gain. For low power and reduced integrator output swings, the gain values at the second integrator have been reduced: k_3 and k_4 are set to 1/2 and 1/4 respectively which represent 1/8th of the gain values determined above.

With the selected gain values, the modulated output can be expressed as,

$$Y(z) = \left(\frac{2-4z}{z^2}\right)\frac{\Delta C}{C_{int1}} + \left(\frac{z-1}{z}\right)^2 E(z) \tag{3.16}$$

The noise transfer function (NTF) is second order differentiation and the signal

transfer function (STF) is expressed by,

$$STF(z) = 2z^{-2} - 4z^{-1}. \tag{3.17}$$

Using the complex number representation of z,

$$\begin{aligned} STF(z) =& 2\left[\cos(2 \times 2\pi f/f_s) - j\sin(2 \times 2\pi f/f_s)\right] \\ & - 4\left[\cos(2\pi f/f_s) - \sin(2\pi f/f_s)\right]. \end{aligned} \tag{3.18}$$

For frequencies f much lower than the sampling frequency,

$$\begin{aligned} STF(z) &= 2z^{-2} - 4z^{-1} \\ &= 2\left[1 - j4\pi f/f_s\right] - 4\left[1 - j2\pi f/f_s\right] \\ &= (2-4) - j\left(8\pi f/f_s - 8\pi f/f_s\right) \\ &= -2, \end{aligned} \tag{3.19}$$

and the modulator output reduces to,

$$Y(z) = -2\frac{\Delta C}{C_{int1}} + \left(\frac{z-1}{z}\right)^2 E(z). \tag{3.20}$$

Because of the relation $C_s = C_{int1}/2$, the modulator output can also be stated as

$$Y(z) = -\frac{\Delta C}{C_s} + \left(\frac{z-1}{z}\right)^2 E(z). \tag{3.21}$$

With the appropriate filtering the differentiated quantization noise can be removed

and a measure of the variable capacitor C_2 can be obtained as follows,

$$C_2 = C_1 + C_s \times E(Y) + e \tag{3.22}$$

where e represents any remaining error.

The mean value of the modulated output represents the input capacitance change. By using the sensor specifications, varying values of C_2 can be related back to changes in intraocular pressure change.

3.3.3 Simulation Results

The modulator is simulated with a full-scale AC input voltage at 4 Hz as shown in Fig. 3.5. The simulated power spectral density of modulator is shown in Figure 3.6. The PSD demonstrates 40 dB per decade noise shaping as expected from the second order modulator.

The integrator output range scales with the input signal magnitude. Histogram plots of the integrator outputs for a full scale (FS) AC input signal are shown in Figure 3.7. In the case of a full scale input signal, the first integrator output exceeds the full scale range necessitating a power supply larger than the feedback reference. Alternatively, the output range can be reduced by further decreasing the integrator gains which has the disadvantage of increasing the relative effect of integrator output noise on the overall noise performance.

During capacitive sensing the differential capacitance $\Delta C = (C_1 - C_2)$ is expected to be small compared to the sampling feedback capacitor C_s which ensures

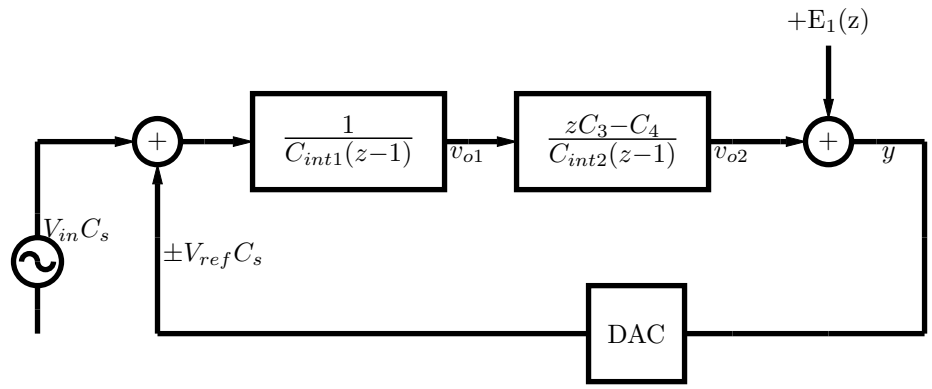

Figure 3.5: Modulator shown in AC input test mode. The input signal is sampled on a capacitor equal in value to C_s. Integrator gain scaling capacitors are shown.

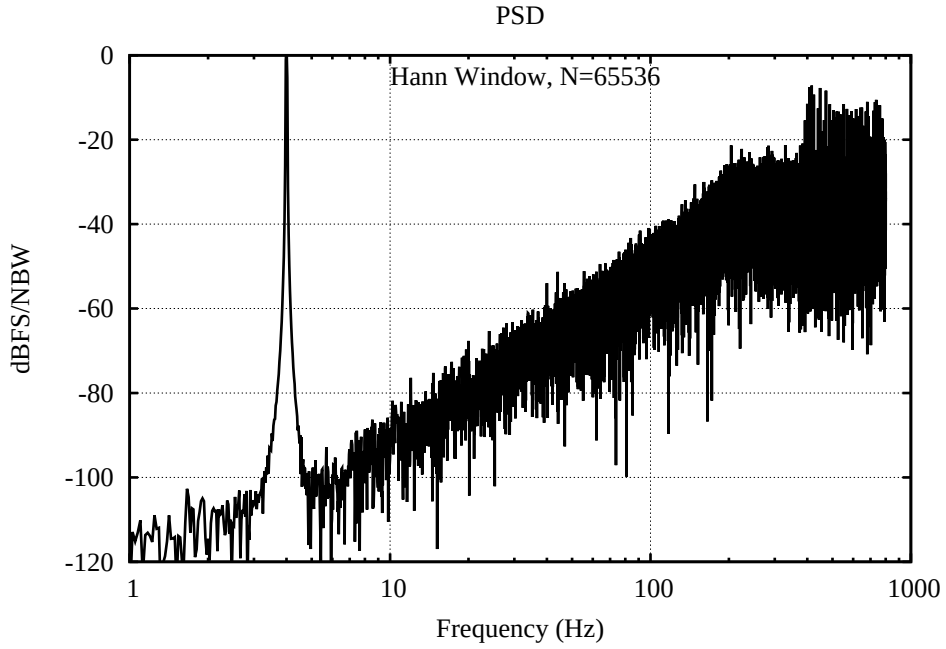

Figure 3.6: Simulated power spectral density for scaled modulator. The result is shown for a 4 Hz input signal at full-scale magnitude.

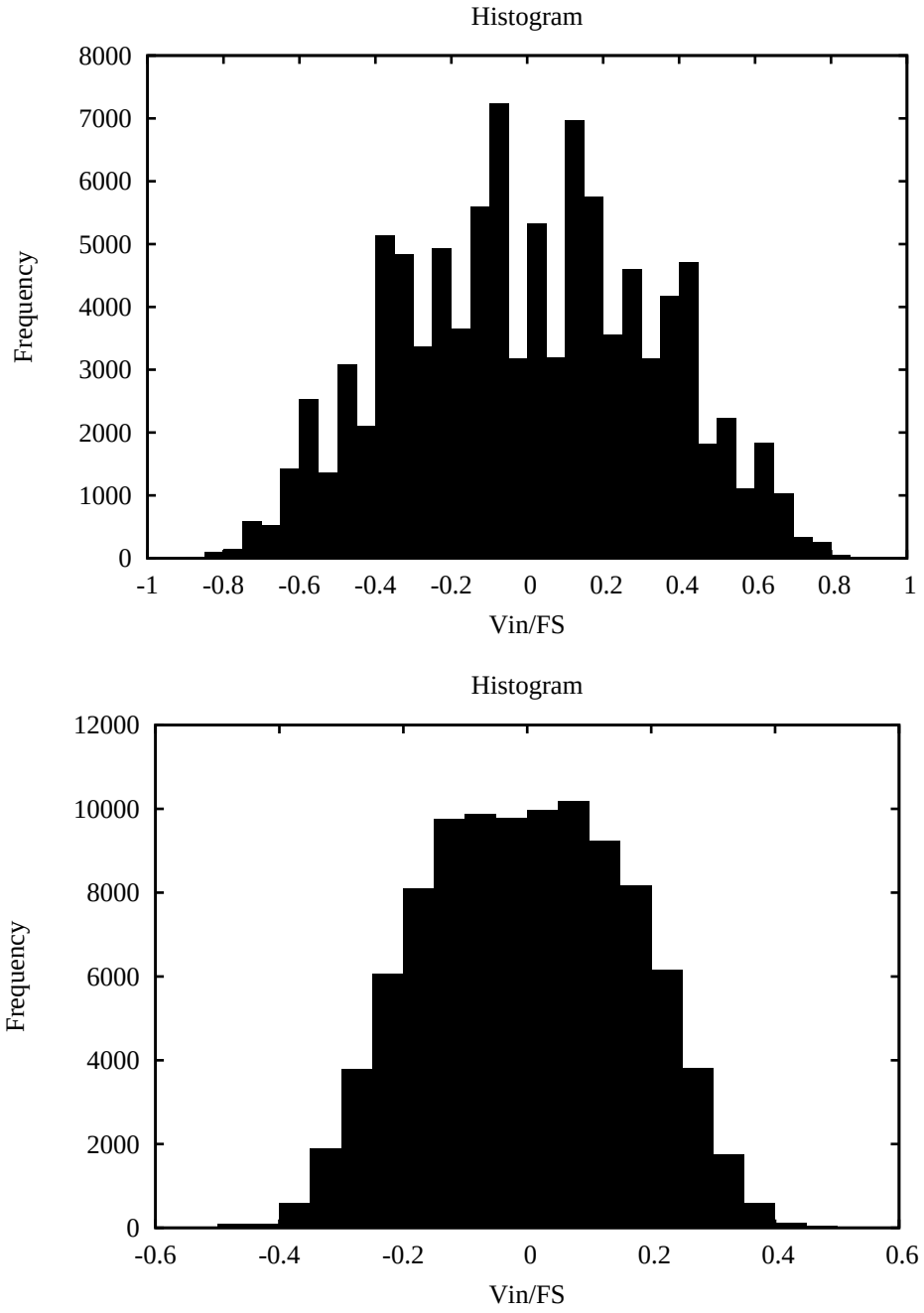

Figure 3.7: Histogram plots for integrator outputs v_{o1} (top) and v_{o2} (bottom) with FS AC input signal. The range is scaled to FS.

the modulator should experience minimal integrator output swing. Without substantial input from ΔC, the modulator is expected to oscillate between logical high and logical low. In this circumstance the integrator output range will lie between $\frac{1}{4}V_{DD}$–$\frac{3}{4}V_{DD}$ which leaves $\frac{1}{4}V_{DD}$ for the inverter amplifier V_{DS}. The decision was made to leave the integrator gains unchanged. As discussed in Section 3.4.1 below, the modulator feedback voltages were independently controlled, allowing for the reduction of the integrator output swing relative to the power-supply voltage.

3.4 Fully-differential Circuit Implementation

To reduce circuit level impairment, the modulator is implemented in fully-differential circuits. The fully-differential modulator is shown in Fig. 3.8. With four phase clocking, a capacitive MEMS sensor and reference MEMS capacitor pair is able to service the fully differential front end. The circuit level implementation is discussed in more detail in Chapter 4.

The MEMS capacitor and reference are used to service fully-differential circuitry with a four phase clock; the front-end sampling occurs twice during each full integration cycle so that each side may process charge from the MEMS capacitor.

3.4.1 Input Stage

This section discusses the capacitive-sensing input stage in more detail.

The capacitive-sensing input stage uses a MEMS sensor (C_2) and reference MEMS capacitor (C_1) to implement a difference-charge sampling proportional to $\Delta C = C_1 - C_2$. A simplified single-ended, first-order modulator is shown in Fig. 3.9.

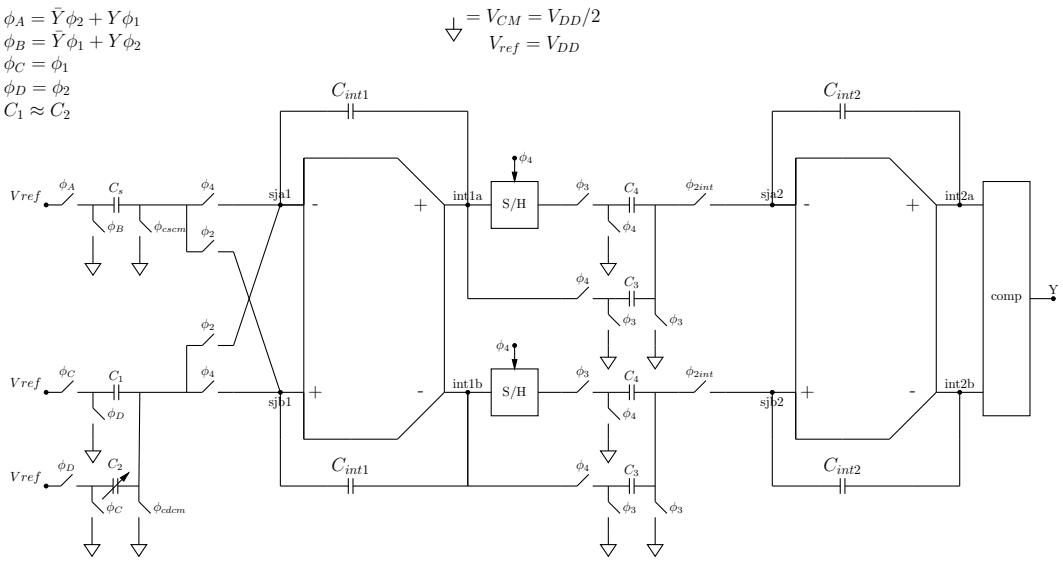

Figure 3.8: Modulator shown with fully-differential circuit implementation. A MEMS sensor and fixed MEMS reference capacitance is used to service the fully-differential implementation with a four phase clock. Reference voltages are sampled only at the front-end.

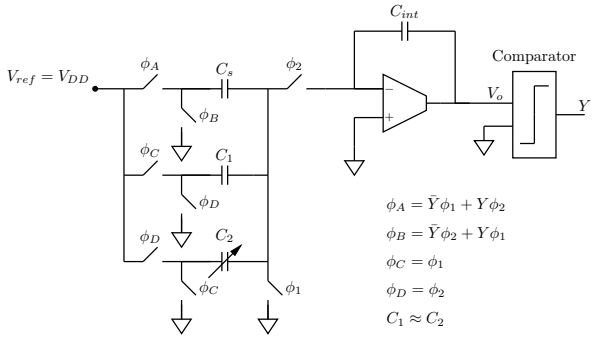

Figure 3.9: Simplified single-ended, first-order, capacitive-sensing modulator with differential capacitive sampling.

The modulator equivalent input voltage, input range and polarity, offset voltage control and circuit calibration are discussed below.

Equivalent Input Voltage The discrete time integrator is non-inverting to C_1 and inverting to C_2. If $Y = 1$, the integrator is inverting to C_s; if $Y = 0$, the integrator is non-inverting to C_s. The integrator output is described by,

$$V_{o1} = \frac{(C_1 - C_2)}{C_{int}} V_{ref} \pm \frac{C_s}{C_{int}} V_{ref}, \tag{3.23}$$

where the polarity of the last term depends on the value of Y. Charge into the summing junction is described by,

$$q(Y = 1) = (C_1 - C_2)V_{ref} + C_s V_{ref} \tag{3.24}$$

$$q(Y = 0) = (C_1 - C_2)V_{ref} - C_s V_{ref}. \tag{3.25}$$

This charge input is identical to a standard voltage input structure with feedback voltage $\pm V_{ref}$ sampled onto capacitor C_s. The equivalent input voltage is,

$$V_{in} = \frac{(C_1 - C_2)}{C_s} V_{ref}. \tag{3.26}$$

From this, the output of the capacitive sensing modulator is indistinguishable from that of a voltage input modulator with an input voltage described by Eq. 3.26. As it uses the same front end sampling scheme and has the same conditional charge input, the second-order modulator has the same equivalent input voltage. For fixed values

of V_{ref} and C_s, the dynamic range of the input signal is determined by the variation of $\Delta C = (C_1 - C_2)$.

Range and Polarity The modulator can process either positive or negative capacitive difference signals. The magnitude of an equivalent voltage input signal for 2 fF capacitive difference with $V_{ref} = 250$ mV and $C_s = 250$ fF is given by,

$$V_{in} = \left(\frac{2\text{fF}}{250\text{fF}}\right) 250\text{mV} = 2\text{mV}. \tag{3.27}$$

Independent Input Voltages The reference voltages V_{refC1} and V_{refC2} are brought off-chip separately from the input sampling capacitor voltage reference V_{ref}. This allows for a voltage input test-mode and for DC offset correction in the case of sensor capacitance mismatch as discussed below.

A voltage input option replaces C_1 and C_2 with two on-chip matched capacitors, C_m with values equal to $C_{1,2}$ shown in Fig. 3.10. The equivalent input voltage then is,

$$V_{in} = \frac{(V_{refC1} - V_{refC2})\, C_m}{C_s} = (V_{refC1} - V_{refC2})\,. \tag{3.28}$$

Gross mismatch in the sensor and reference capacitor, C_1 and C_2, can be additionally be offset by an applied differential DC input voltage.

Calibration The calibration mode introduced in [70] has been implemented in the design of the capacitive sensing modulator. Calibration eliminates charge sampling from the difference capacitance $\Delta C = (C_1 - C_2)$. During calibration, charge is

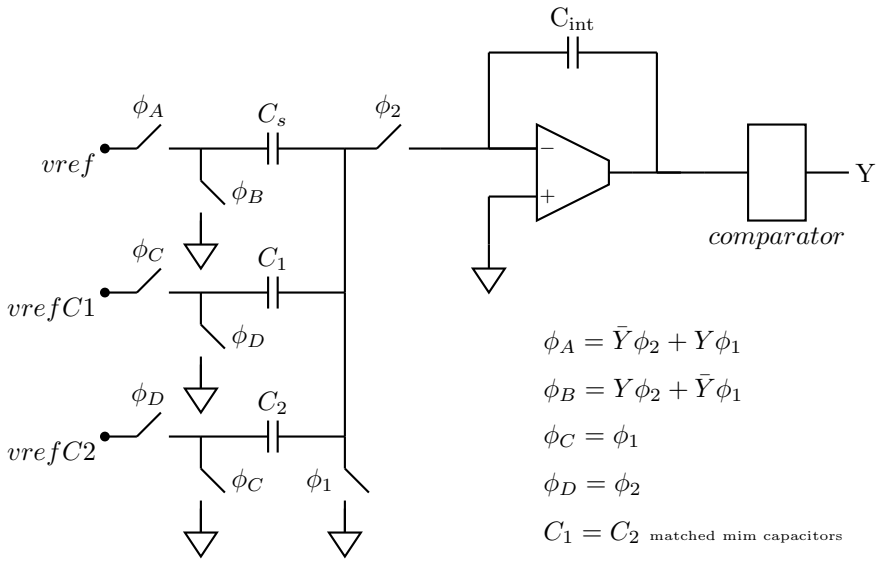

Figure 3.10: Simplified first-order single-stage modulator shown with independent input voltages.

sampled on C_s only and the digital output should ideally oscillate between a logical one and zero. Accumulation of integrated charge due to non-ideal effects will cause the output to vary from the ideal value. The difference between the ideal result and the actual result during calibration can be used to remove the DC accumulation of non-ideal effects during normal operation.

3.5 Signal to Quantization Noise Ratio

Quantization noise enters the signal path at the comparator. Input referred, the noise is shaped by second-order differentiation. For second-order modulation, the in-band mean square noise power is [106]

$$E(V_{qrms}^2) \approx \left(\frac{\pi^4}{5 \times \mathrm{OSR}^5}\right) e_{rms}^2 \tag{3.29}$$

where e_{rms}^2 is the mean square noise power of the comparator acting as a single-bit quantizer and OSR is the modulator oversampling ratio. Assuming an AC input signal with magnitude is described by Eq. 3.26, the signal-to-noise ratio due to quantization noise, SNR_q, is,

$$SNR_q = \frac{\left(\frac{\Delta C}{C_s} V_{ref}\right)^2 \times 5 \times \mathrm{OSR}^5}{2 \times \pi^4 \times e_{rms}^2}. \tag{3.30}$$

Assuming a white-noise model with uniform distribution for the single-bit quantizer, $e_{rms}^2 = \Delta^2/12$ and $\Delta = V_{DD}$. With the reference scaled to the comparator power supply $V_{ref} = V_{DD}/2$ the SNR_q is independent of V_{DD}. A plot of the

signal to quantization noise ratio versus oversampling ratio for a capacitive input signal,ΔC = 2 fF and a sampling capacitor, C_s = 250 fF is given in Fig. 3.11. For an oversampling ratio of 64, an SNR_q of 40 dB is possible.

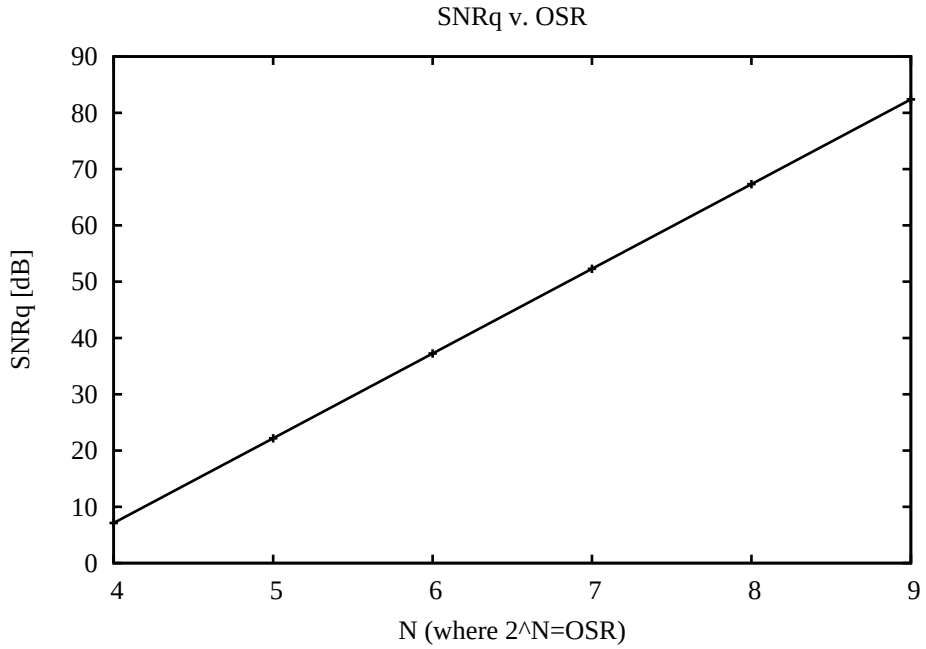

Figure 3.11: Signal to quantization noise ratio, SNR$_q$, for ΔC = 2 fF and C_s = 250 fF.

3.5.1 Comment on Signal to Noise Ratio

The quantization signal-to-noise ratio is typically not designed as the limiting factor in $\Sigma\Delta$ modulation. Input-referred front-end circuit noise, which transfers directly to the modulated output along with the signal, is usually the performance limiting noise source. Front-end circuit noise forms a white-noise floor which is generally higher than the shaped-quantization noise in the bandwidth of interest.

3.6 Summary

This chapter described the system-level design of the capacitance-to-digital converter. The converter was based on a $\Sigma\Delta$ modulator using a bilinear second-stage. The bilinear stage enabled front-end charge sampling only, avoiding the insertion of the feedback voltage into the modulation. The modulator loop was modified to support a differential-capacitor ($\Delta C = C_1 - C_2$) front-end structure for low-power operation. The mean-value of the modulator output is proportional to the differential capacitance, ΔC, and can be used to estimate varying capacitive change induced by pressure change. Fully-differential circuitry is used to implement the modulator, reducing circuit error. A simplified first-order, single-ended modulator was used to demonstrate the equivalent input voltage and the signal range and polarity. The signal to quantization-noise ratio was determined. Front-end circuit noise, expected to be the performance limiting factor, is discussed in the next chapter.

CHAPTER 4

LOW-VOLTAGE LOW-POWER CIRCUIT DESIGN

This Chapter describes the circuit level design of the modulator. First, the selected CMOS technology process is discussed in Sec. 4.1. Next, the inverter amplifier chosen for low-voltage, low-power circuit operation is described in Sec. 4.2. An overview of the switched-capacitor modulator implemented with the inverter amplifiers is given in Sec. 4.3. A detailed design of the modulator subcircuits is presented in Sec. 4.4. A design summary is given in Sec. 4.5 and system-level simulation results are given in Sec. 4.6. The layout-level details of the integrated circuit fabrication are provided in Sec. 4.7. The wire-bond of the integrated circuit die with the MEMS sensors is described in Sec. 4.8. Finally, a summary is given in Sec. 4.9.

4.1 CMOS Process Selection

The long-term goal of the project included wider-group work for a full monolithic implementation of a pressure sensing microsystem together with an IC inductor coil for wireless-power reception. For this reason, the modulator was implemented in the IBM 0.13 μm CMOS technology. The IBM 0.13 μ technology provides a range of transistors for circuit design purposes as well as high-quality RF metal layers for later implementation of an IC coil inductor.

The IBM 0.13 μm technology has three thin-oxide core-transistor N/PMOS pairs and two thick-oxide I/O-transistor N/PMOS pairs. The core-transistors are available in standard, low-power and low-threshold options. The low-power nfet (lpnfet) has approximately twice the threshold-voltage of the regular threshold transistor (nfet) and approximately 1/100 the leakage current. Leakage current is drain-source current flow which occurs by subthreshold conduction, discussed in the following sections.

The IBM 0.13 μm technology also has well-matched metal-insulator-metal (MIM) capacitors and vertical-natural capacitors (VNCAP) which are capable of implementing very small capacitance values. Both the MIM capacitors and the VNCAP capacitors are useful in low-power SC circuits; the VNCAP can be used where capacitor values less than the minimum value of the MIM capacitor is required and where matching is a lesser concern.

4.2 Inverter Amplifier

The inverter amplifier has been used for low-voltage, low-power circuit design [86, 87]. The inverter amplifier acts as a dynamically biased amplifier and has previously been researched within the early development of SC circuits [101–103]. Due to the potential of low-voltage and extremely low-power operation, the inverter amplifier was selected for this project.

4.2.1 Subthreshold Operation

An inverter with it's input gates biased to the midpoint of the power supply has the properties of an amplifier as shown in Fig. 4.1. Assuming the transistor transcon-

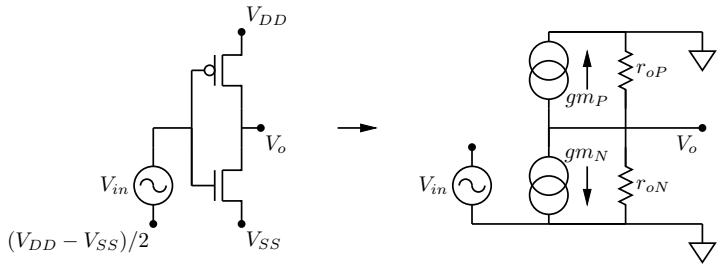

Figure 4.1: Inverter showing small signal amplifier characteristics.

ductance $gm_N = gm_P = g_m$ and transistor output resistances $ro_P = ro_N = r_o$ the inverter amplifier low-frequency gain is described by

$$A_o = -g_m \times r_o. \tag{4.1}$$

And the inverter amplifier gain-bandwidth is described by,

$$GBW = \frac{g_m}{\pi C_L} \tag{4.2}$$

where C_L is the total load capacitance at the amplifier output.

Depending on the transistor region of operation, the amplifier transconductance and output resistance vary. For the strong inversion, or saturation, region the MOS transistor transconductance and output resistance follow

$$g_{m_{si}} \propto \sqrt{I_{DSQ_{si}}}$$
$$r_o \propto \frac{1}{I_{DS_{si}}}$$

In the weak inversion region, the MOS transistor transistor transconductance and output resistance follow

$$g_{m_{wi}} \propto I_{DSQ_{wi}}$$
$$r_o \propto \frac{1}{I_{DQ_{wi}}}$$

where $I_{DQ_{si}}$ and $I_{DQ_{wi}}$ are the quiescent drain-source current in strong and weak inversion respectfully. The weak inversion region is also referred to as the subthreshold region. Strong and weak inversion will be explained later.

The general trend of the MOS transistor over the regions of strong and weak inversion are shown in Fig. 4.2. As the output-resistance is the same in either region, and the weak-inversion region provides the highest transconductance per unit current, the weak-inversion region also achieves the highest gain for the least

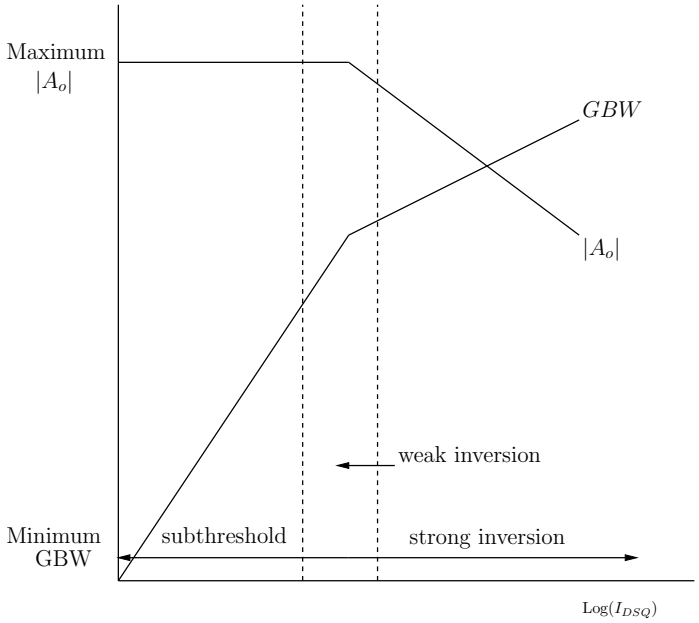

Figure 4.2: Amplifier operating region open-loop gain and gain-bandwidth shown versus bias current.

amount of current. While the overall transconductance is low in weak inversion (due to low current) causing a decreased GBW for a fixed capacitive load C_L, the gain per unit current is highest in weak inversion. As the operation shifts further toward lowest current operation, or deep subthreshold, the GBW is decreased but the gain remains constant.

The operation of an amplifier in a SC circuit requires high-gain (to accurately transfer charge) and sufficiently high gain-bandwidth to satisfy the closed-loop integrator time-constant for settling the charge transfer. In an amplifier which has a preset bias-current, these needs are in contradiction with each other. In the inverter amplifier, however, there is no preset amplifier bias-current. The inverter-amplifier can be used as a dynamic amplifier responding in different operating regions depending on the bias conditions applied during that phase of operation.

Within SC circuits at a clock phase when the integrator is not actively integrating, the inverter-amplifier can have a controlled gate-voltage applied. For consistency with the input sampling switches, the gate-voltage setting is typically analog ground, $V_{CM} = V_{DD}/2$ which is the reference for input charge sampling. During the clock phase when the gate-voltage is applied, the gate-voltage setting of $V_{DD}/2$ offers control of the amplifier subthreshold-current ($I_{DS_{wi}}$) and small-signal properties such as GBW and A_o. During the clock phase when the inverter amplifier responds in integration, however, the gate-voltage is floating and is influenced by the integrator capacitive feedback loop. As discussed in Sec. 4.2.3 below, the gate-voltage is boosted at the start of integration and larger drain-source current results providing the inverter-amplifier with a temporarily higher GBW. As the integration completes, the inverter amplifier gate-voltage stabilises and returns to V_{CM}. In this manner, the inverter amplifier starts the integration phase with increased GBW and ends with nominal GBW and A_o set from the gate-voltage V_{CM}. Provided the final settling is sufficient, non-linearity in settling, incurred due to a departure from amplifier linear-settling behavior, is not a concern in SC circuits.

4.2.2 Drain Current and Current Noise

The gate-voltage setting of $V_{DD}/2$ controls the amplifier current for the majority of time and largely determines the inverter-amplifier power consumption. In the weak-inversion, or subthreshold, region the drain-source current of the MOS transistor is generally described by [109]

$$I_{DS_{wi}} = (W/L) I_{Do} \exp \frac{v_{GS}}{nkT/q} \tag{4.3}$$

where W/L is the transistor width-length ration, v_{GS} is the gate-source voltage and kT/q is the thermal voltage. The factor n is given by,

$$n = \frac{C_{BC}}{C_{GC}} + 1 \tag{4.4}$$

where C_{BC} is the bulk-channel capacitance and C_{GC} is the gate-channel capacitance. These controlling capacitances have a large impact in subthreshold operation; because there is no effective channel, electron transport is strongly influenced by capacitances C_{BC} and C_{GC} which act on either side. These capacitances control the rate of change of current with respect to changes in gate-source voltage. Subthreshold transconductance is described by

$$g_{m_{wi}} = \frac{\partial I_{DS_{wi}}}{\partial v_{GS}} = \frac{I_{DS_{wi}}}{nkT/q}. \tag{4.5}$$

For the remainder of this document, the subscript for weak-inversion will be omitted in favor of the general term g_m for transconductance and the inverter-amplifier is understood to be operating in the subthreshold region.

The subthreshold region has different conduction modes which give rise to linear-behavior or saturation-behavior within the subthreshold region [110]. Saturation behavior, for instance, results in a subthreshold current with little to no dependence on the drain-source voltage; linear-behavior results in current with a linear relationship to the drain-source voltage. The current described in Eq. 4.3 assumes the transistor is operating in subthreshold-saturation [109, 110] with V_{DS} approximately equal to or greater than a few kT/q. The voltage kT/g is referred to as the thermal voltage and is equal to approximately 26 mV, thus a drain-source

voltage of roughly 100 mV is required for the transistor to have saturation behavior in subthreshold.

Subthreshold current in a MOS transistor is caused by minority-carrier diffusion in the depleted channel region under the gate. Subthreshold charge transport in an NMOS transistor is comprised of thermally-energetic electrons which originate in the source-region and make their way across the energy barrier from source to channel, then, by virtue of a locally high electron concentration, diffuse into the drain region *as well as* current generated by electrons in the drain-region crossing the drain-channel barrier and diffusing into the source-region. The energy barrier is lowest at the source, giving rise to a dominant electron transport from the source to drain; provided V_{DS} is at least equal to few kT/q, the diffusion current from the drain is negligible and the current is described well by Eq. 4.3.

White-noise associated with the current I_{DS} derive from the same processes that generate I_{DS}; thermally excited generation and the diffusive transport which have inherent uncertainties. The white-noise of the subthreshold current can either be thought of as thermal-noise or shot-noise as these noise mechanisms are the same [111]. The noise is described by

$$\overline{I_{DS}^2} = 2qI_{DS}\Delta f \tag{4.6}$$

where q is the charge of an electron, and Δf is the bandwidth. To use the noise term in circuit design, it is convenient to express it in terms of the design parameter g_m as follows,

$$\overline{I_{DS}^2} = 2nkTg_m\Delta f \tag{4.7}$$

In a SC integrator, the inverter-amplifier thermal noise is sampled when the integrator switch opens at the completion of integration. At this time the transistor should be at the nominal bias conditions set by the gate-voltage of V_{DD}/2; for noise purposes, this current value should be set as low as possible. Noise sampling in the SC modulator circuit is discussed in more detail in Sec. 4.4.1.

4.2.3 Dynamic Settling Behavior

The settling behavior of the subthreshold inverter amplifiers used in the modulator is not the same as with an amplifier using a fixed-slew quiescent current. In response to a SC integrator gate-voltage glitch, the inverter amplifier provides increased charge/discharge current as shown in Fig. 4.3 which *improves* settling response. This is contrary to a standard transconductance amplifier where bias transistors can be pushed into triode and must recover in order to operate properly.

In the sample phase, ϕ_1, of Fig. 4.3 the input capacitor, C_s, is shown sampling a zero-voltage input; in the integration phase, ϕ_2, the inverter amplifier responds in an inverting manner to the sampling of $(V_{DD} - V_{DD}/2) = V_{DD}/2$ at C_s. Also shown in Fig. 4.3 is the inverter amplifier in a unity-gain configuration sampling onto C_h; this will be discussed in the following section. From ϕ_2 of Fig. 4.3 at the start of integration the voltages $V_{C_s} = 0$ and $V_{C_h} = 0$ and the amplifier has not yet responded. At this time, the sampled voltage V_{DD} is transferred directly to the gates of the inverter amplifier. In response, the PMOS transistor enters cut-off and the NMOS transistor is strongly driven to balance the integration. As the integration completes, the charge is balanced and the summing junction returns to virtual ground.

The current boost that occurs during the start of integration is a non-linear response to a large transient gate voltage. Charge balancing that occurs during integration returns the gate-voltage to the virtual ground value and the amplifier to linear operation where it can complete linear settling toward the final settled value. Transient settling in SC circuits does not affect accuracy provided that settling is allowed to complete to the final required settled value.

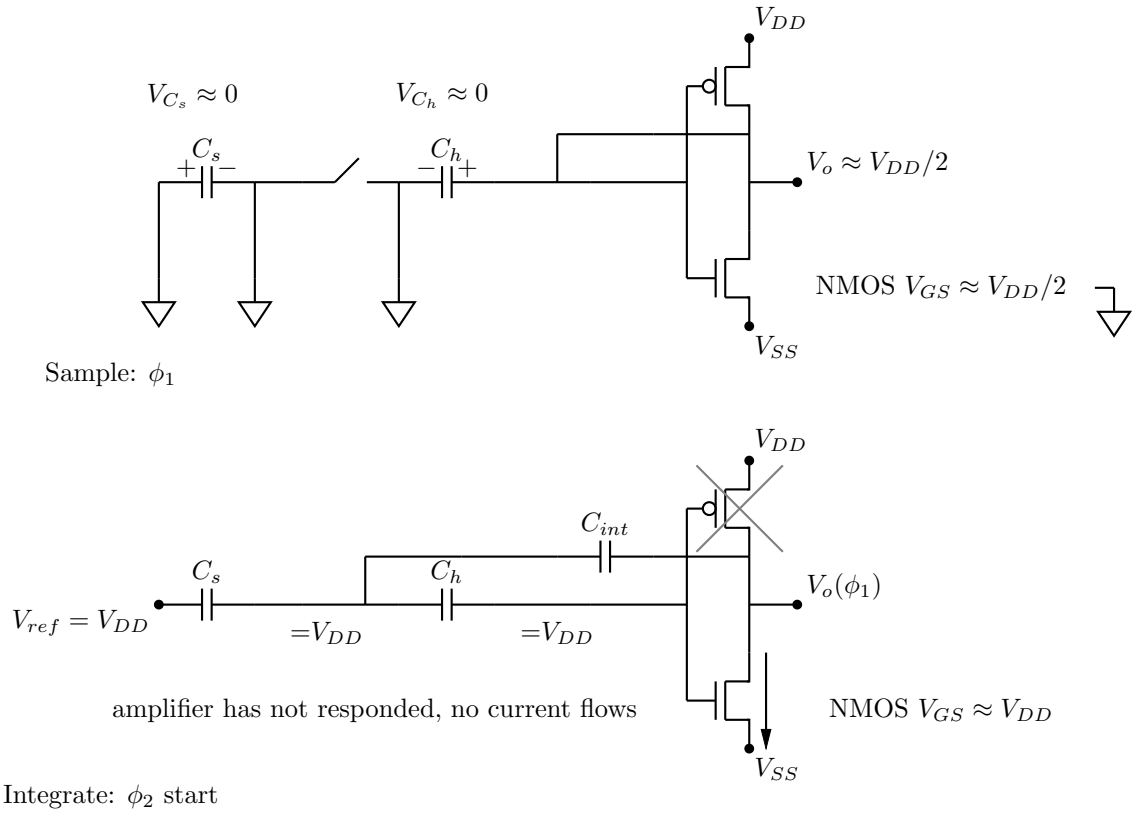

Figure 4.3: Inverter amplifier dynamic settling. At the start of the integration phase, ϕ_2 the amplifier has not yet responded to the sampled charge and the full voltage V_{DD} is transfered to the gates of the inverter, boosting current response in a transient manner.

4.2.4 Design Objectives

Other work [41, 86, 87] suggests operation of the inverter amplifier at the point where the gain has achieved a maximum value and where the gain-bandwidth is not substantially reduced, which is at an operating point in between the weak and strong inversion regions. This project, however, has the objectives of very low-voltage, low-power operation and very low-frequency operation is acceptable.

Figure 4.4 shows a plot of the current response vs. gate-voltage for low-power and regular NMOS transistors with the same W/L ratio. As seen on the plot, the low-power transistor enters subthreshold operation at a much higher gate-voltage than the regular transistor. In the plot shown, a nominal gate voltage of 250 mV (V_{DD}/2) produces a drain-source current, I_{DS}, of roughly 5 nA; during a transient settling event, where the gate voltage would be boosted to V_{DD}, the drain-source current is dramatically increased to just over 1 μA, an increase of over two orders of magnitude. At the start of integration, the inverter amplifier acts with a boosted current and gain-bandwidth that can be 100$\times$ larger than that obtained with the nominal gate-voltage at mid-supply. In general, in the subthreshold region of the low-power transistor, a gate-voltage increase of 100 mV is sufficient to increase the drain-source current by a 10$\times$ factor.

To benefit from the substantially reduced leakage current, inverter amplifiers for this project were implemented with low-power transistors available in the technology. Due to operation with MEMS capacitors, the inverter amplifier is subject to widely varying capacitive loads. Capacitive loading and the selection of the transistor gain-bandwidth are discussed in more detail in Sec. 4.4.7.

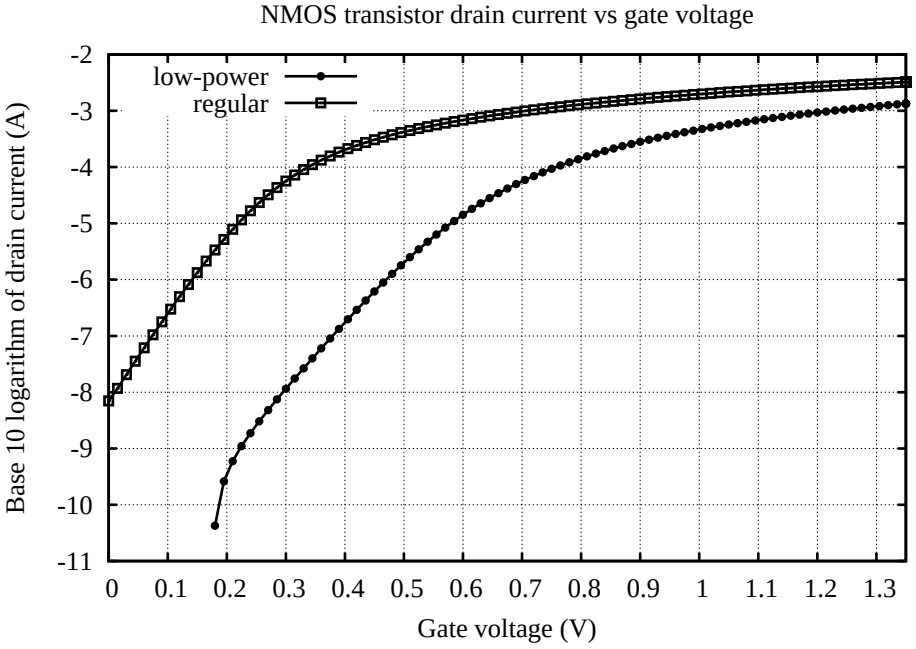

Figure 4.4: Simulated NMOS drain-source current vs. gate voltage. Results are shown for low-power and regular NMOS transistors of the same W/L ratio (top curve shows regular threshold transistor response). Current reduces sharply as the transistor enters the subthreshold region. For the low-power transistor operating in subthreshold, a gate-voltage increase of approximately 100 mV is sufficient to increase the drain-source current by an order of magnitude.

4.2.5 Virtual Ground

The inverter is a single-input amplifier which does not provide a virtual ground node. A poorly controlled, or absent, virtual ground node can cause significant errors in switched-capacitor circuits. Referring to the top diagram of Fig 4.5, the charge transferred to the integrating capacitor during ϕ_2 is proportional to $(V_{in} - V_A)$ where V_A is the voltage at the input node of the amplifier. The voltage V_A satisfies the following relationship,

$$\begin{aligned} V_A + V_{Cint} &= -A_o(V_A - V_{offset}) \\ V_A &= A_o V_{offset}/(1 + A_o) - V_{Cint}/(1 + A_o) \\ V_A &\approx V_{offset} \end{aligned} \tag{4.8}$$

where A_o is the open-loop gain of the inverter amplifier and V_{offset} is the inverter offset voltage. Because the offset voltage varies with several factors including gate noise, the charge transfer is impaired. Cancellation of this offset voltage and establishment of a virtual ground is required.

When the inverter is in a closed-loop configuration with its input gate connected to the output voltage (phase ϕ_1 at the bottom diagram of Fig. 4.5),

$$\begin{aligned} V_o = -A_o(V_A - V_{offset}) &= V_A \\ V_A(1 + A_o) &= A_o V_{offset} \\ V_A &\approx V_{offset}. \end{aligned} \tag{4.9}$$

Sampling the offset voltage in this configuration forms the basis of constructing

a virtual ground. During ϕ_1, the holding capacitor C_h samples and holds V_{offset} relative to analog ground ($V_{CM} = VDD/2$). During clock phase ϕ_2 the inverter loop closes around the integrating capacitor C_{int}. As discussed above, the gate voltage would be forced to the offset voltage V_{offset}. Since the offset voltage is already held on C_h, the voltage at the summing junction of the offset-corrected integrator is forced to analog ground, V_{CM}, thereby providing an error-corrected virtual ground for charge integration.

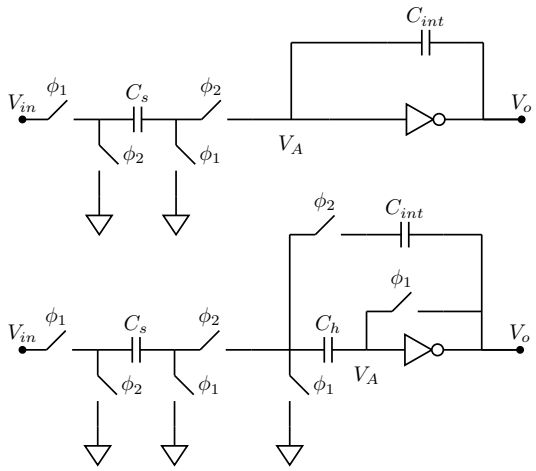

Figure 4.5: Inverter amplifier in integrator configuration with no input offset correction (top) and with input offset correction (bottom).

4.2.5.1 Correlated Double Sampling

The establishment of a virtual ground in the inverter amplifier implements correlated-double-sampling. As was discussed in Chapter 2, correlated-double-sampling is a technique used in SC circuits to reduce amplifier offset and low-frequency noise. The technique operates by sampling amplifier offset at a phase when the amplifier is

not in use, and then subtracting this value at a later time. Because offset and low-frequency noise have longer time constants than typical system sampling frequencies, there is a high correlation between the offset sample taken and the offset at the time of removal. This technique and others are described in more detail in [59].

In this project, with low-voltage operation and without the ability to stack transistors for additional gain, an important benefit of correlated-double-sampling is an effective increase in the amplifier gain. With correlated-double-sampling, the effective value of the offset becomes V_{os}/A_o where A_o is the nominal amplifier gain, and the effective amplifier gain becomes A_o^2 [70, 112]. The gain enhancement can be understood by considering that the charge transfer is made close-to-ideal through the action of improvements to the virtual ground, as would occur were a higher gain amplifier used. This is an advantage to using switched-capacitor circuits in the low-voltage environment.

4.2.6 Output Common-mode Control

In the case of the inverter amplifier, there is no means to control the output common-mode directly at the output. The operation of the two transistors of the inverter amplifier are both fully controlled by the power-supply and gate voltages. Inverter amplifier output common-mode control is accomplished through integration of charge in the normal course of integrator operation; the integrated charge represents the control signal between the common-mode set voltage and the common-mode output voltage. First, the common-mode set voltage is sampled on two capacitors, then each integrator output is sampled against this charge. If the sum of the integrator output voltages is less (greater) than twice the set voltage, the integrator responds in

an inverting manner by raising (lowering) the output voltage. By directing common-mode feedback charge into the integrator inputs, the common-mode control can operate over the entire output range of the integrator output.

4.3 Modulator Circuit Level Overview

This section provides an overview of the modulator using inverter amplifiers; later sections discuss the detailed design of the sub-circuitry.

The fully-differential modulator previously shown in Fig. 3.8 is now shown implemented with inverter amplifiers in Fig. 4.6. This section proceeds as follows. First, the inverter amplifier supporting circuitry and the pseudo-differential nature of the signal path are discussed. Next, integrator and comparator operation during different clock phases is described. Finally, the timing diagram is given for the modulator.

4.3.1 Pseudo-differential Implementation

The signal path for the modulator is not fully-differential, but rather is pseudo-differential with individual integrators supporting each side of the fully-differential signal path. Four phase clocking is used throughout in the modulator operation. The differential signal is supported with a single capacitive MEMS sensor and matched MEMS dummy capacitor at the front-end (C_1 and C_2). Front-end sampling operations are completed with clock signals, ϕ_A, ϕ_B, ϕ_C, ϕ_D as defined in Fig. 4.6. All capacitors are switched between the reference voltage and analog ground for a stray-insensitive structure.

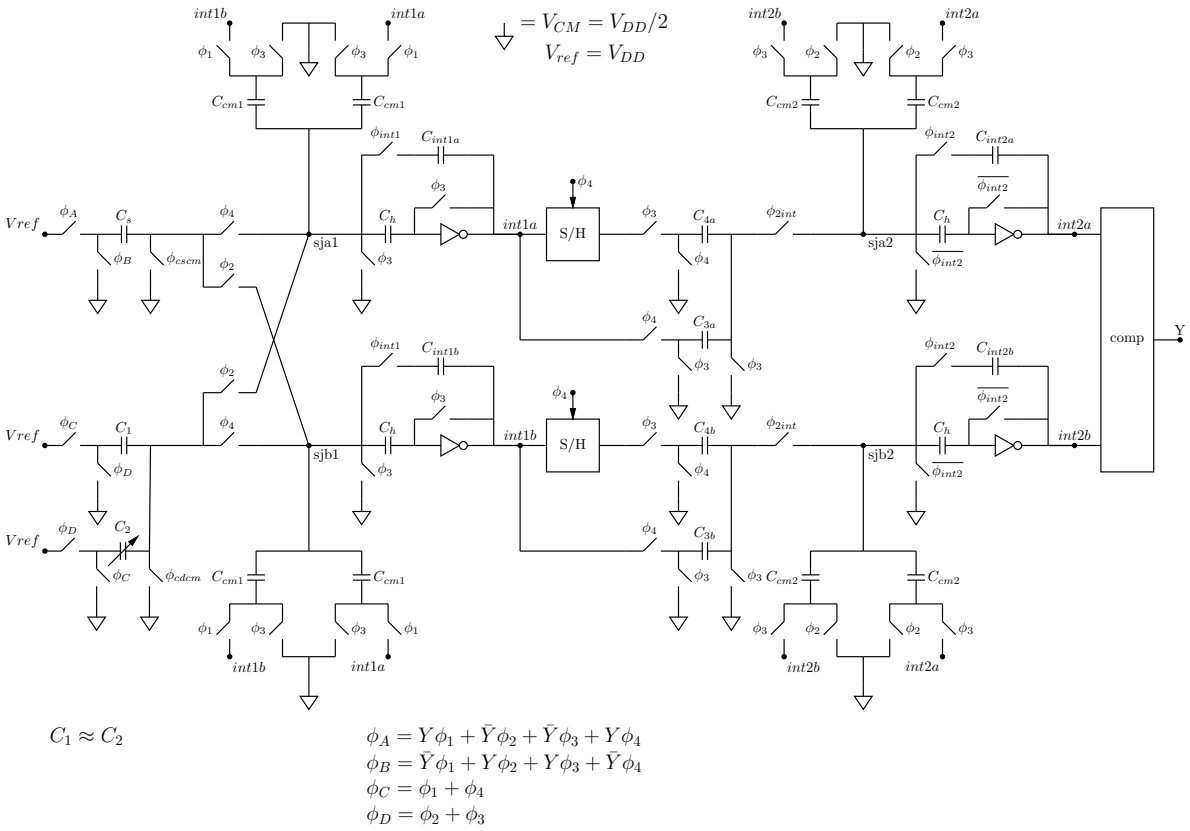

Figure 4.6: Switched capacitor $\Sigma\Delta$ modulator designed for low-power capacitive sensing with operational transconductance amplifiers implemented with subthreshold inverters. All capacitors are switched between the reference voltage and analog ground for a stray insensitive structure. By using a four-phase clock, the fully-differential signal path is supported with a single capacitive sensor and matched dummy capacitor.

Each inverter amplifier in the modulator is supported with common-mode feedback circuitry using charge injection at the summing junction of the integrator through capacitors C_{cm}. Using common-mode control through charge injection at the summing junction removes control circuitry from the amplifier output, simplifying the circuitry and expanding the output operating range. Each inverter amplifier is also supported with offset cancellation using correlated double sampling with capacitor C_h. The inverter amplifiers are implemented with low power transistors available in the technology. The switches are implemented with regular technology transistors.

In this circuit with a pseudo-differential signal path, correlated-double-sampling also assists by ensuring that each side of the pseudo-differential path has a reliable and consistent virtual ground. The controlled setting of the virtual ground removes a source of error normally present in pseudo-differential circuits where there may be differences between the positive and negative signal paths.

4.3.2 Four Phase Clock & System Timing

This section describes the operation of the integrators and comparator during the four clock cycles. The switch-level circuit and timing diagram are shown at the end of the section.

First Integrator For the first integrator, the four-phases of the system clock are allocated for the following operations. During ϕ_1 the common-mode correction charge is integrated. During ϕ_2, the crossed input path is integrated so that $int1a$ responds to charge sampled on ΔC, and $int1b$ responds to charge sampled on C_s.

During ϕ_3 the integration is switched off, the inverter closed-loop output voltage is sampled on C_h and the common-mode set voltage (V_{CM} = V_{DD}/2) is sampled onto the common-mode correction capacitors C_{m1}. Finally, during ϕ_4 the direct input path is integrated so that $int1a$ responds to charge sampled on C_s, and $int1b$ responds to charge sampled on ΔC.

Between sampling events, appropriate changes are made to the polarity of the switches at the input sampling capacitors so that the charge injection is differential in nature to the pseudo-differential signal path.

By the end of ϕ_4 the integrator has completed integration of both the input and feedback signal in a fully-differential manner as well as completed necessary support functions such as common-mode control and sampling of the closed-loop offset.

Note that because the signal integration occurs in two different phases, ϕ_2 and ϕ_4, the pseudo-differential common-mode output is unbalanced during ϕ_3. During this phase, the common-mode circuit samples the common-mode set point, but does not sample the integrator outputs. The common-mode output balances to the correct value only at the end of ϕ_4 after both integrators have received charge from C_s and ΔC. After the ϕ_4 clock cycle, the circuit is able to sample the amplifier output voltages to then integrate charge to make the necessary adjustment during ϕ_1.

Second Integrator For the second integrator, the four phases of the system clock are allocated as follows. During ϕ_1 and ϕ_2 the integration is switched off. The inverter closed-loop voltage is sampled during both ϕ_1 and ϕ_2. During ϕ_2 the common-mode set voltage is sampled onto the common-mode correction capacitors C_{m2}. During ϕ_3 the common-mode correction charge is integrated. During ϕ_4 the sampled charge on both C_3 and C_4 is integrated.

As discussed in the context of the modulator transfer function in Chapter. 3.3, the second integrator relies on having both the present and previous value of the first integrator output. For this, the output of the first integrator is sampled and held during it's valid output time ϕ_4. During the next cycle of ϕ_3, the previously held value is sampled onto C_4. During the integration phase of the second integrator, ϕ_4, charge from the previous value of the first integrator is obtained from C_4; charge from the current voltage of the first integrator is obtained from C_3.

Comparator The comparator is preceeded by a sample-and-hold stage for the output of the second integrator. To avoid clock glitch, the sampling action completes slightly in advance of the completion of the integration clock cycle ϕ_4. The comparison is then activated on the falling edge of ϕ_4.

4.3.3 Input Signal Swing

Front-end sampling at V_{refC1}, V_{refC2} and V_{ref} occurs twice during the four-phase integration cycle.

Each side of the pseudo-differential signal-path processes sampled-charge with adjusted polarity. The adjusted polarity is achieved by switching the inverting and non-inverting integration between C_1 and C_2. For the positive signal path, the integration is non-inverting to C_1 and inverting to C_2 such that charge injected is proportional to $(C_1 - C_2)$; for the negative signal path, the integration is inverting to C_1 and non-inverting to C_2 such that the charge injected is proportional to $(C_2 - C_1)$. In this manner, the pseudo-differential circuitry processes charge proportionate to $2 \times (C_1 - C_2)$. This use of inversion to support the signal path allowed the use

of two MEMS capacitive sensors (one rendered pressure-insensitive as a reference capacitor) to service the differential signal path.

In the case of pressure input, the reference voltages V_{refC1} and V_{refC2} are fixed at V_{DD} producing a differential charge injection of $(V_{DD} - V_{CM}) \times 2 \times (C_1 - C_2)$. In voltage mode, however, an AC voltage input is applied between V_{refC1} and V_{refC2} with peak values of V_{DD} and V_{SS} allowing for additional input signal swing.

In voltage mode, the charge is sampled on matched on-chip capacitors C_m. For the positive signal path, the integration is non-inverting to V_{refC1} and inverting to V_{refC2} such that charge injected is $C_m \times ((V_{refC1} - V_{CM}) - (V_{refC2} - V_{CM}))$; for the negative signal path, the integration is inverting to V_{refC1} and non-inverting to V_{refC2} such that the charge injected is $C_m \times ((V_{refC2} - V_{CM}) - (V_{refC1} - V_{CM}))$. The total differential charge is

$$q = C_m \times 2 \times ((V_{refC1} - V_{CM}) - (V_{refC2} - V_{CM})) \tag{4.10}$$

With $V_{refC1} = V_{DD}$ and $V_{refC2} = V_{SS} = 0$, the differential charge is given by

$$\begin{aligned} q &= C_m \times 2 \times ((V_{DD} - V_{DD}/2) - (0 - V_{DD}/2)) && (4.11) \\ &= C_m \times 2 \times V_{DD} && (4.12) \end{aligned}$$

In the opposite case, where $V_{refC1} = V_{SS} = 0$ and $V_{refC2} = V_{DD}$, the injected charge is $q = -C_m \times 2 \times V_{DD}$. Thus the input voltage signal swing is between $\pm 2 \times V_{DD}$ for a peak value of $2 \times V_{DD}$. Each side of the pseudo-differential signal path processes a $2 \times V_{DD}$ signal swing, leading to signal truncation at the integrators.

Although C_s is slightly larger than C_m, the increased voltage signal swing will introduce increased distortion in the modulator output.

The voltage input mode of the modulator was designed for test operation only, the modulator was optimally designed to process charge proportionate to a small differential capacitance. The small signal expected from the variable charge path $\Delta C = (C_1 - C_2)$ provides the least amount of integrator accumulation. In addition, switching the variable capacitance between only two voltages provides inherent linearity. In general, however, differences between the static properties of the MEMS capacitors C_1 and C_2 will also introduce difference charge into the integration. With constant operating conditions, however, any difference charge should only result in a constant differential input offset charge. If static charge injection is large, this may interfere with proper modulator operation.

4.3.4 Modulator Timing Diagram

The modulator circuit diagram together with a timing diagram are shown in Fig. 4.7. The system clock is a positive edge detector used to control the pulsewidth and frequency of a four-phase clock generator circuit. Due to observed failures over process variation, a four-phase clock generator was implemented off-chip. Data is available after each cycle of ϕ_4, which occurs at a rate of f_{sys}/4. The modulator sampling frequency is thus $f_s = f_{sys}$/4.

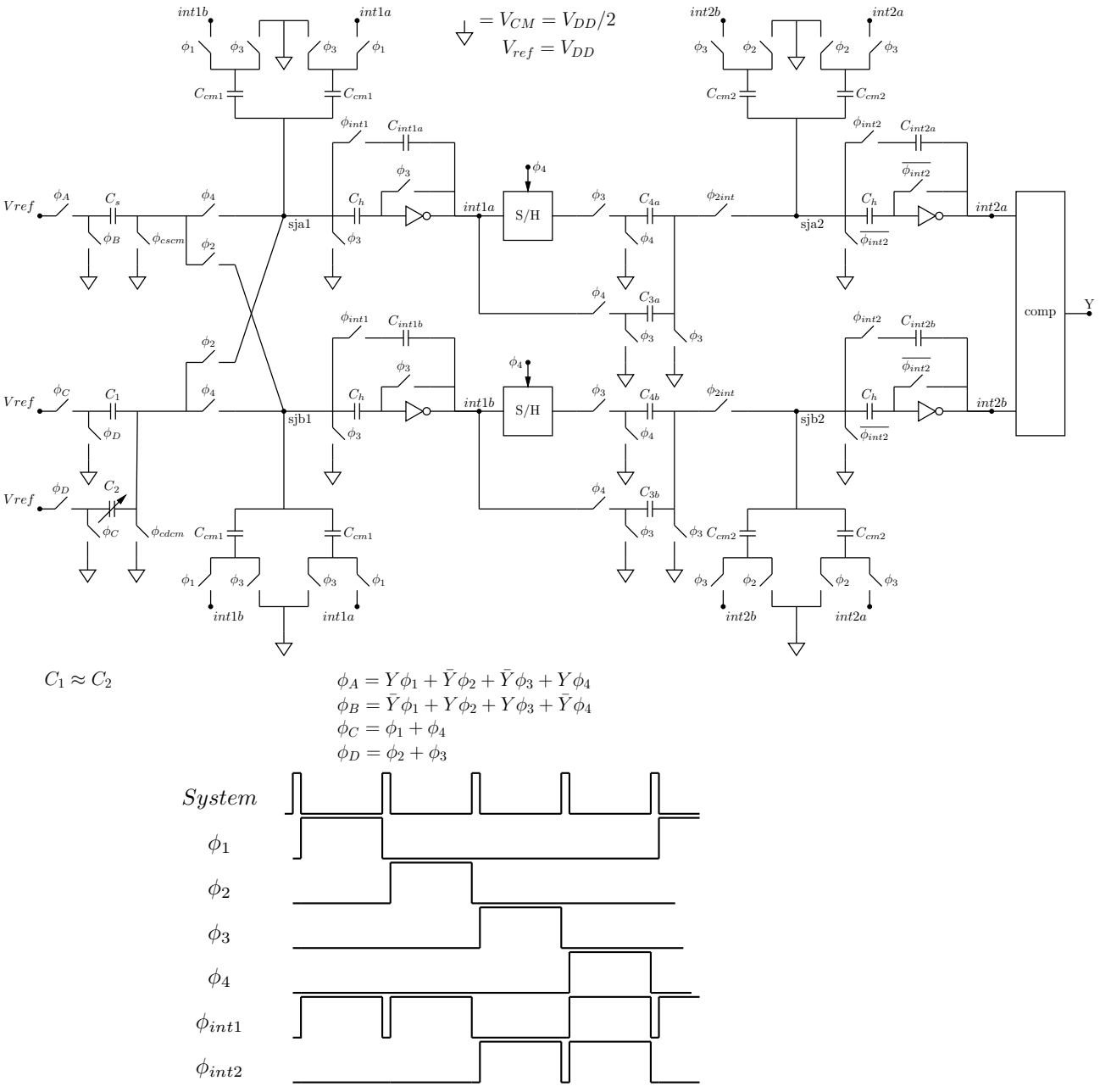

Figure 4.7: Modulator clocking scheme showing system clock, four-phase clocks and integrator clocks.

4.4 Modulator Subcircuit Design

This section describes the design constraints of the modulator including thermal noise considerations with a least-power design constraint, input switch settling, common-mode feedback control, capacitor charge-loss and voltage-droop, integrator settling and amplifier gain-bandwidth.

The modulator was designed with a nominal clock rate of f_s = 1600–6400 Hz and nominal power supply voltage of V_{DD} = 500–600mV. A clock rate of f_s = 1600 Hz allows approximately 160 μs pulsewidth for each of the four sampling clock phases, ϕ_1, ϕ_2, ϕ_3 and ϕ_4; a clock rate of f_s = 6400 Hz allows approximately 40 μs for each of the sampling phases.

4.4.1 Thermal Noise

First, the thermal noise from the sampling switches and the inverter amplifier will be considered. Then, noise in the two phases of the integrator will then be determined. Finally, to determine a thermal noise signal-to-noise ratio (SNR), total noise power will be compared to signal power at the sampling capacitor. Where required, the input signal voltage equivalent defined in page 40 will be used.

Input Switch Input sampling occurs as shown in Fig. 4.9 shown on page 82. The input switch operates in triode with a noise-power spectral density (PSD) given by,

$$S_{vtR_{on}}(f) = 4kTR_{on} \tag{4.13}$$

in units of V^2/Hz. When attached to a sampling capacitor, C, this transistor switch on-resistance white-noise source is low pass filtered and ceases to be white noise. The mean square value of the low-pass filtered noise is given by,

$$E(V_{tR_{on}}^2) = \frac{4kTR_{on}}{4\tau} \tag{4.14}$$

where $\tau = R_{on}C$ is the filter time-constant ($f_{3dB_{sw}} = 1/2\pi\tau$).

As described in Sec. 4.4.3, the switch should settle to a specified accuracy within the sampling clock phase. For sufficient input settling to occur $f_{3dB_{sw}}$ is typically larger than the sampling frequency f_s. Sampling at a frequency lower than the noise bandwidth causes aliasing. Aliasing folds down higher frequency noise into the bandwidth of sampling. Folding of high-frequency noise causes the total wide-band mean square noise given by Eq. 4.14 to be represented in within the bandwidth of sampling. Due to folding down of high-frequency noise, samples taken at f_s are highly uncorrelated and the noise can be considered very nearly white. A single sided PSD can be formed by,

$$S_{vto} = \frac{E(V_{tR_{on}}^2)}{f_s/2} = \frac{S_{vtR_{on}}/4\tau}{f_s/2} = \frac{S_{vtR_{on}}}{2\tau f_s}. \tag{4.15}$$

Observe that the PSD has been increased by $1/2\tau f_s$ above that from the white-noise of the switch prior to sampling. While the PSD has been increased, low-pass filtering after modulation removes much of the noise.

Inverter Amplifier The inverter amplifier has two transistors biased in subthreshold. The drain current-noise PSD of a transistor operated in subthreshold is propor-

tional to the current and is given by [113],

$$S_{ito}(f) = 2\mathrm{kT}g_m \tag{4.16}$$

in units of A^2/Hz. For simplification, the MOS parameter n is set to 1 and the current is assumed to the same in each transistor[1]. The generalization is made that g_m describes the overall amplifier transconductance. Total input referred voltage noise due to channel current noise processes in the inverter amplifier is given by,

$$S_{vta} = 4\mathrm{kT}/g_m = 8\mathrm{kT}/g_m \tag{4.17}$$

in units of $\mathrm{V}^2_{\mathrm{rms}}/\mathrm{Hz}$.

Sampled Noise in Integrator Configuration For convenience, the first part of the following analysis assumes a single input capacitor integrator with a two phase clock. This section uses the noise analysis technique set out in [114].

The sampling capacitor is denoted by C_s. Input sampling occurs during ϕ_1 and integration occurs during ϕ_2. At the end of the sampling phase, the mean square value of the sampled switch noise is

$$E(V^2_{cs})_{\phi 1_{sw}} = \frac{2 \times 4\mathrm{kTR_{on}}}{4\tau} = \mathrm{kT/C_s} \tag{4.18}$$

where $\tau = 2R_{on}C_s$ due to two transistor switches. At the end of the sampling phase, charge is held on the sampling capacitor and the integration phase begins.

At the end of the integration phase, noise results from both the sampling switch

[1]This assumption is accurate when the amplifier is in not in slew.

and the amplifier and is given by [114],

$$V_{cs}(s) = \frac{V_{tnRon}(s) - V_{vta}(s)}{1 + s\tau} \tag{4.19}$$

where V_{tnRon} represents noise due to switch on-resistance and V_{vta} represents amplifier noise. With three transistor switches on during integration, the time-constant for the transfer function of the noise onto the sampling capacitor is given by,

$$\tau = (3R_{on} + 1/gm)C_s. \tag{4.20}$$

The mean square noise due to the on-resistance of the switches during the integration phase ϕ_2 is given by

$$E(V_{cs}^2)_{\phi_2 sw} = \frac{3 \times 4\mathrm{kTR_{on}}}{4\tau} = \frac{kT}{C_s}\left(\frac{1}{1 + 1/x}\right) \tag{4.21}$$

where $x = 3R_{on}gm$. Note that noise due to the input sampling switch during the sampling phase and the integration phase differ due to the number of switches and a difference in the low pass filter pole. The mean square noise from the amplifier at the end of ϕ_2 is,

$$E(V_{cs}^2)_{\phi_2 amp} = \frac{4\mathrm{kT}/g_{m_{N,P}}}{4\tau}. \tag{4.22}$$

Assuming that $gm = 2 \times g_{m_{N,P}}$ as discussed in Sec. 4.2, then

$$E(V_{cs}^2)_{\phi_2 amp} = \frac{2\mathrm{kT}}{C_s}\frac{1}{(1 + x)}. \tag{4.23}$$

By the end of the integration phase, total noise power at the sampling capacitor from

both the sampling phase and the integration phase is given by,

$$E(V_{cs}^2)_{\phi_2+\phi_1} = \frac{\mathrm{kT}}{C_s}\left(1 + \frac{1}{1+1/x} + \frac{2}{1+x}\right) = \frac{\mathrm{kT}}{C_s}\left(2 + \frac{1}{1+x}\right). \qquad (4.24)$$

Least Power Design For this project least power is desired. For the least power solution, the assumption is made that $x \ll 1$ (or $gm \ll 1/R_{on}$) meaning that the amplifier transconductance is minimal. The mean square voltage noise power then becomes,

$$E(V_{cs}^2) = \frac{3\mathrm{kT}}{C_s}. \qquad (4.25)$$

Note that a *least noise* design is obtained from the design choice of $x \gg 1$ or, equivalently, $gm \gg 1/R_{on}$, corresponding to a large amplifier bandwidth and switch dominated noise. The design trade-off for decreased power is increased noise.

Additional Input Switches Each input switched capacitor contributes noise. This is most easily analysed with charge noise. The mean square voltage noise in Eq. 4.25 can be converted to a mean square charge noise by,

$$E(Q_{cs}^2) = 3\mathrm{kT}C_s. \qquad (4.26)$$

Ignoring the reduction in noise due to two switches instead of three during integration of the common-mode feedback control charge, the total charge noise into each integrator over a four-phase clock cycle is given by,

$$E(Q_{total}^2) = 3\mathrm{kT}\left(C_1 + C_2 + C_s + 2 \times C_{cm1}\right). \qquad (4.27)$$

From this, it is possible to work out the signal to noise ratio of the modulator. The single-ended peak input equivalent voltage that would be sampled on C_s was given in Eq. 3.26 and is restated here for convenience:

$$V_{in_p} = \frac{\Delta C}{C_s}(V_{DD}/2).$$

Assuming a sinusoidal input with peak value of V_{in_p}, the signal power is given by,

$$V_{in_{rms}}^2 = \frac{\left(\frac{\Delta C}{C_s}(V_{DD}/2)\right)^2}{2}.$$

The signal charge power is obtained by using the relation $Q = CV$,

$$Q_{in_{rms}}^2 = \frac{(\Delta C(V_{DD}/2))^2}{2}$$

The single sided noise spectrum is spread out in frequency from 0 Hz to f_s/2 and the in-band, mean-square noise is reduced by the oversampling ratio. The resulting thermal signal-to-noise ratio, SNR_t, is given by,

$$SNR_t = \frac{Q_{in_{rms}}^2 \times \mathrm{OSR}}{3\mathrm{kT}\,(C_1 + C_2 + C_s + 2 \times C_{cm1})} \tag{4.28}$$

where $Q_{in_{rms}}^2$ is the input signal power expressed in terms of charge. Capacitors C_1 and C_2 dominate the total capacitance. Figure 4.8 shows SNR_t versus the oversampling ratio for ΔC = 2 fF, $C_1 = C_2$ = 6 pF, C_s = 250 fF and C_{cm1} = 100 fF. These results indicate that a resolution of 2 fF is possible with an OSR as low as 16.

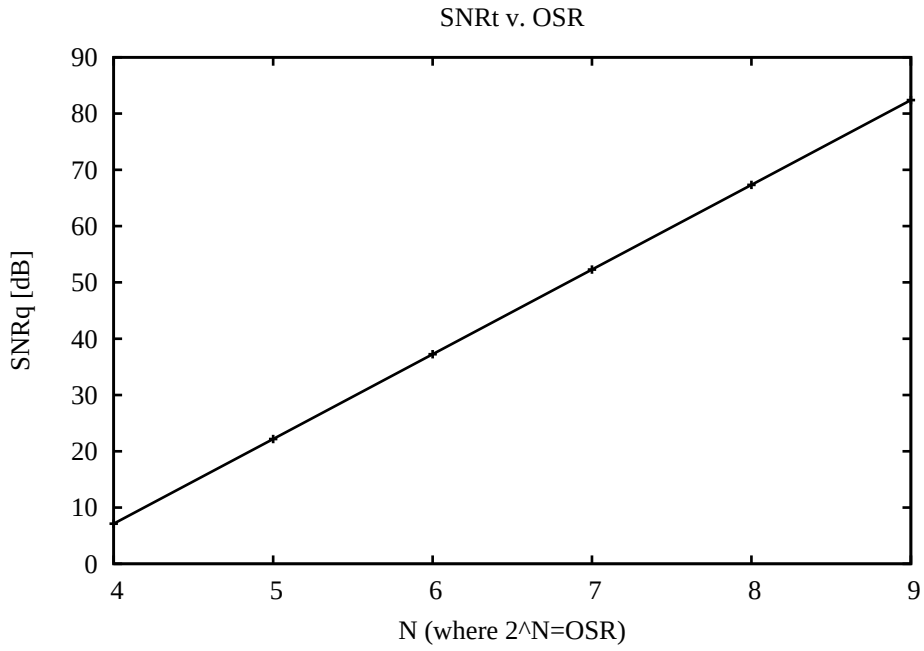

Figure 4.8: Simulated SNR_t from thermal sources versus the oversampling ratio. Results are shown as determined by the single-ended analysis of Eq. 4.28.

4.4.2 Noise Simulation

Because the noise sources are bias dependent and the noise transfer function is periodically time-varying, periodic steady-state and periodic-noise simulation is necessary to simulate the input referred noise. At the time of tape-out, however, attempts to simulation the periodic-steady-state (PSS) operation and to calculate periodic-noise at the first integrator did not converge. Since the tape-out, the first integrator has been successfully simulated for periodic-noise and the input referred noise is higher than than indicated by the prior thermal noise analysis.

4.4.2.1 Periodic Noise Simulation

The first integrator of the modulator was simulated for periodic-steady-state operation with SpectreRF using voltage-mode input with on-chip matched capacitors.

Results are shown for a 100-fold periodic-noise simulation with two different operating conditions:
V_{DD} = 500 mV, f_s = 3200 Hz

```
Device              Param    Noise Contribution   % Of Total
/Iint1/I8/TNinv       id       1.58344e-05          21.98
/Iint1/I115/TNinv     id       1.54326e-05          20.88
/Iint1/I8/TPinv       id       1.51927e-05          20.23
/Iint1/I115/TPinv     id       1.48071e-05          19.22
/Iint1/I1/T1          id       9.33431e-06          7.64
/Iint1/I17/T1         id       9.16128e-06          7.36
Spot Noise Summary (in V/sqrt(Hz)) at 10 Hz
Sorted By Noise Contributors
```

```
Total Input Referred Noise = 0.015581
```

V_{DD} = 600 mV, f_s = 6400 Hz

Device	Param	Noise Contribution	% Of Total
/Iint1/I8/TNinv	id	6.21411e-06	22.05
/Iint1/I115/TNinv	id	5.98369e-06	20.45
/Iint1/I8/TPinv	id	5.91226e-06	19.96
/Iint1/I115/TPinv	id	5.69393e-06	18.52
/Iint1/I1/T1	id	3.40699e-06	6.63
/Iint1/I17/T1	id	3.34049e-06	6.37

```
Spot Noise Summary (in V/sqrt(Hz)) at 10 Hz
Sorted By Noise Contributors
Total Input Referred Noise = 0.000773083
```

As expected, the thermal noise is dominated by the n-type and p-type transistors at the inverter amplifier, TNinv and TPinv. With a fully-differential full-scale input signal this results in a maximum SNR range of:

$$SNR_{t_{max}} = 20 \times \log_{10}\left(\frac{(1200 - 1000\text{mV})/\sqrt{2}}{\sqrt{25\text{Hz}} \times (0.7 - 15.6)\text{mV}/\sqrt{\text{Hz}}}\right) = 47 - 19\text{dB} \quad (4.29)$$

Circuit noise is expected to be the dominant performance limitation, especially at low voltage and sampling rates. Transistors in the inverter amplifiers at the first integrator comprise the largest noise sources in the modulator. The sampled noise is highly variable with operating voltage V_{DD} and sampling frequency f_s; over the operating range of V_{DD} = 500–600 mV and f_s = 3200- 6400 Hz, noise limited performance varied between 47–19 dB.

In Context of IOP Measurement Instrument In the application of an IOP measurement instrument, the modulated output is expected to be highly oversampled, providing an opportunity to reduce the impact of white-noise sources. Resolution of the IOP is desired to be at least 2 mmHg, corresponding to approximately 5 bits over a full-scale pressure range of 0–50 mmHg. In the presence of noise-limited performance of the modulator circuitry, total noise may be reduced by taking a longer sample.

4.4.3 Analog Switches

To mitigate the impact of charge injection, fully-differential circuitry is used throughout the modulator and summing junction switches are opened in advance of sampling switches. To avoid excessive leakage current that can occur with low-threshold transistors, regular-threshold transistors were selected for use in all switches. To avoid increased threshold voltage that can occur from short channel effects, the transistor length was chosen to be four times the process minimum length. For reliability reasons, a minimum width that supported two contacts to the drain/source diffusion was selected. These constraints resulted in a transistor size of at least,

$$W/L_{sw} = \frac{0.8\mu\text{m}}{0.48\mu\text{m}}. \tag{4.30}$$

Other factors to consider in the design of the analog switches include the on-resistance and settling error.

In the capacitive sensing mode of the modulator, there are two input voltages in the modulator design. In this circumstance, the on-resistance linearity of the switches

is not a concern provided there is full settling. The input capacitors are switched between analog signal ground at V_{DD}/2 and the reference at V_{DD}. While this input signal range is best processed with the PMOS transistor, full transmission gate switches are used to reduce clock feedthrough charge injection. To best minimize clock feedthrough, the PMOS and NMOS transistors are the same size.

On Resistance When a transistor is used as a switch to charge a capacitor as shown in Fig 4.9, the conductance varies over the charging period. Current in the MOS transistor channel is described generally by

$$I_{DS}(t) = \mu c_{ox}(W/L)\left[(V_{GS}(t) - V_T(t)) - V_{DS}(t)/2\right]V_{DS}(t). \tag{4.31}$$

Assuming a constant threshold voltage, taking the partial derivative of I_{DS} with respect to V_{DS}

$$\partial I_{DS}(t)/\partial V_{DS}(t) = g_{ON}(t) = \mu c_{ox}(W/L)\left[(V_{GS}(t) - V_T) - V_{DS}(t)\right] \tag{4.32}$$

is the conductance of the MOS transistor switch as a function of the varying voltages applied to it's terminals, as well as it's physical properties. The on-resistance is the inverse of the conductance

$$R_{on} = 1/g_{on}(t) = \frac{1}{\mu c_{ox}(W/L)\left[(V_{GS}(t) - V_T) - V_{DS}(t)\right]}. \tag{4.33}$$

It is necessary to consider two different cases, one when the capacitor is charging and another when the capacitor is discharging.

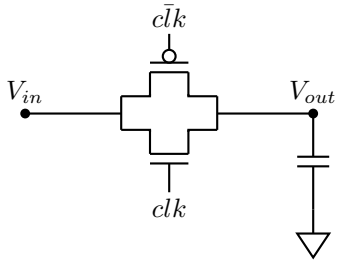

Figure 4.9: CMOS transmission gate circuit used to charge and discharge a capacitor.

Charging From Fig. 4.9, when the input voltage $V_{in} = V_{DD}$ is larger than the voltage on the capacitor $V_{out} = V_{DD}/2$ the capacitor is charged. With a supply voltage V_{DD} = 500 mV and a nominal threshold voltage of $\approx$ 225 mV for both transistors, the NMOS transistor is not capable of processing this voltage range. The PMOS transistor has a gate voltage of $V_{SS} = 0$ and source voltage of $V_{DD} = 500\mathrm{mV}$, available at V_{in}. At the start of charging, $V_{DS} = V_{in} - V_{out} \approx V_{DD}/2$ which reduces the conductance according to Eq. 4.32. At the end of the charging period, the PMOS source voltage is still $V_{DD} = 500\mathrm{mV}$, but now $V_{DS} = 0$ which giving a higher conductance. Thus, when the capacitor is charging, the on-resistance of the transmission gate switch decreases.

Discharging From Fig. 4.9, when the input voltage $V_{in} = V_{DD}/2$ is less than the voltage on the capacitor $V_{out} = V_{DD}$, the capacitor is discharged. Again, with a supply voltage V_{DD} = 600 mV and a nominal threshold voltage of 225 mV for both transistors, the NMOS transistor is not capable of processing this voltage range. The PMOS transistor has a gate voltage of $V_{SS} = 0$. The PMOS has a source voltage of $V_{DD} = 600\mathrm{mV}$, available at V_{out}. At the start of charging $V_{DS} = V_{in} - V_{out} \approx V_{DD}/2$ which reduces the conductance

according to Eq. 4.32. As the discharge occurs, the source voltage steadily decreases. At the end of the charging period, $V_{DS} = 0$ again which increases the conductance, but the source voltage is now $V_{DD}/2$ which reduces the conductance. Thus the on-resistance of the transmission gate switch does not necessarily decrease over the charging period as it did during charging.

Figures. 4.10 and 4.11 show the on-resistance of a regular threshold transmission gate switch W/L=0.8μm/0.48μm when charging and discharging a capacitor. The on-resistance is shown versus the charge or discharge progress. Results are shown for both $V_{DD} = 500$ mV and $V_{DD} = 600$mV over the process corners, including the extreme (functional) corners. The maximum on-resistance is 550 kΩ for $V_{DD} = 500$ mV and 180 kΩ for $V_{DD} = 600$ mV.

Settling Error at Input Switches For single time-constant settling,

$$V_{out} = V_{in}\left(1 - \exp^{\frac{-\Delta t}{\tau_{R_{on}}}}\right), \tag{4.34}$$

where Δt is the time available in the sampling phase and $\tau_{R_{on}}$ is the time-constant formed by the sampling capacitor and the input switch on-resistance.

For 12-bit settling performance, the capacitive sensor and dummy capacitor should settle to 12 bits. Setting V_{in} equal to the full-scale input step, and allowing V_{out} to be within 1 LSB of the full-scale step results in,

$$V_{DD}/2\left(1 - \frac{1}{2^{12} - 1}\right) \leq V_{DD}/2\left(1 - \exp^{\frac{-\Delta t}{\tau_{R_{on}}}}\right), \tag{4.35}$$

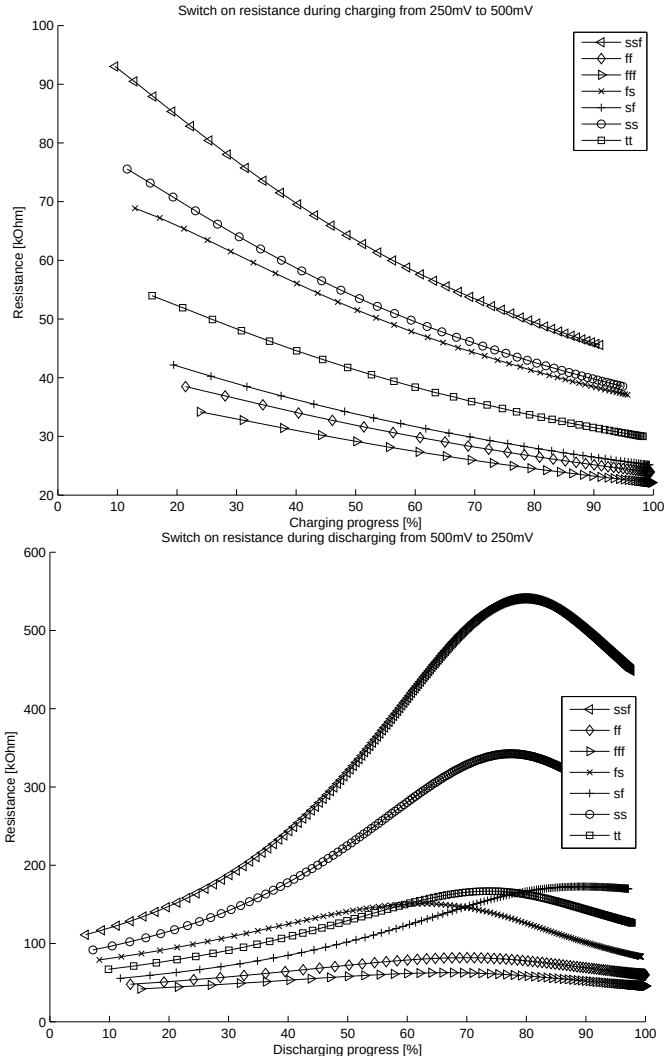

Figure 4.10: Schematic-level circuit simulation of transmission gate on-resistance for charging from $V_{DD}/2 = 250\text{mV}$ to $V_{DD} = 500\text{mV}$ (top) and discharging from $V_{DD} = 500\text{mV}$ to $V_{DD}/2 = 250\text{mV}$ (bottom).

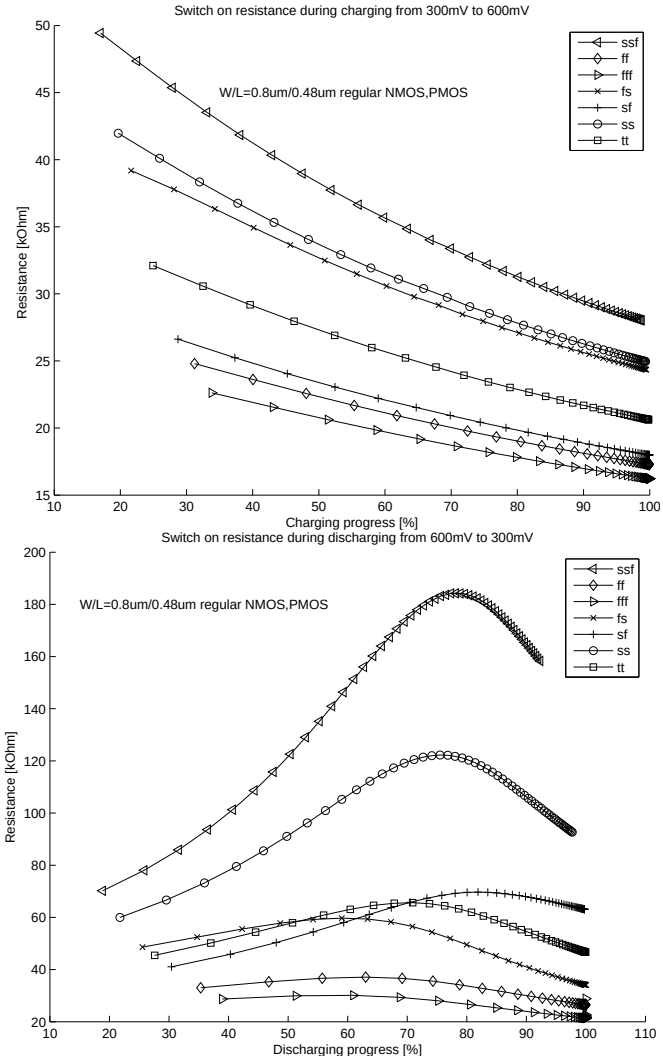

Figure 4.11: Schematic-level circuit simulation of transmission gate on-resistance for charging from $V_{DD}/2 = 300$mV to $V_{DD} = 600$mV (top) and discharging from $V_{DD} = 600$mV to $V_{DD}/2 = 300$mV (bottom).

which reduces to,

$$\frac{\Delta t}{\tau_{R_{on}}} \geq \ln(2^{12} - 1) \approx 8.3. \tag{4.36}$$

With two switches in the charge/discharge path of the capacitors,

$$\tau = 2R_{on}C. \tag{4.37}$$

The worst case corner settling performance is shown below for the nominal value of C = 6 pF at the capacitive sensor and dummy capacitor.

Power Supply	Maximum R_{on}	$\Delta t/\tau_{R_{on}}$ (40μs)	$\Delta t/\tau_{R_{on}}$ (160μs)
500 mV	550 kΩ	6	24
600 mV	185 kΩ	18	72

The sampling frequency target is f_{sys} = 6400 Hz (f_s = 1600) which allows roughly 160 μs settling per clock phase. At V_{DD} = 500 mV the input switch settling at the worst case process corner is slightly less than the that required for 12-bit settling performance; in the case of V_{DD} = 600 mV there is ample switch settling.

4.4.4 Output Common-mode Control

The output common-mode output of the inverters forming the pseudo-differential signal path is controlled by directing charge into the integrator inputs as follows. First, the common-mode set voltage is sampled on capacitors C_{cm} as shown in Fig. 4.6. Next, each inverter integrator output is sampled against this charge. If the sum of the integrator output voltages is less (greater) than twice the set voltage, the integrator responds in an inverting manner by raising (lowering) the output

voltage. By directing common-mode feedback charge into the integrator inputs, the common-mode control can operate over the entire output range of the integrators.

The common-mode capacitors sample between the set voltage and the integrator output. In one phase, the inverters source or sink the required amount of charge to make up the difference voltage; in the next phase, the common-mode voltage sources or sinks the appropriate charge. To reduce the overall power, the common-mode capacitors are sized quite small, 100 fF for the first integrator and 50 fF for the second integrator.

The trade off for small common-mode capacitors is a low common-mode feedback gain and slower common-mode transient recovery. The gain of the output common-mode control is equal to the ratio of the common-mode capacitor to the integrating capacitor. The first integrator has a common-mode gain of approximately 1/5, while the second integrator has a gain of 1/4. Figure 4.12 shows the first integrator common-mode transient response from V_{DD}.

4.4.4.1 Impact of Capacitor Mismatch

Mismatch errors associated with the capacitor technology impact the common-mode control gain (when mismatch occurs with the integrating capacitor) and the accuracy of the common-mode sensing (when mismatch occurs between the common-mode sampling capacitors). For the first integrator, the common-mode capacitor is implemented in VNCAP and will be poorly matched to the integrating capacitor which is implemented in the MIM technology.

For the sizes chosen, three-sigma mismatch between the common-mode sampling capacitors at the first integrator is expected to be less than $\approx 1\%$. At the

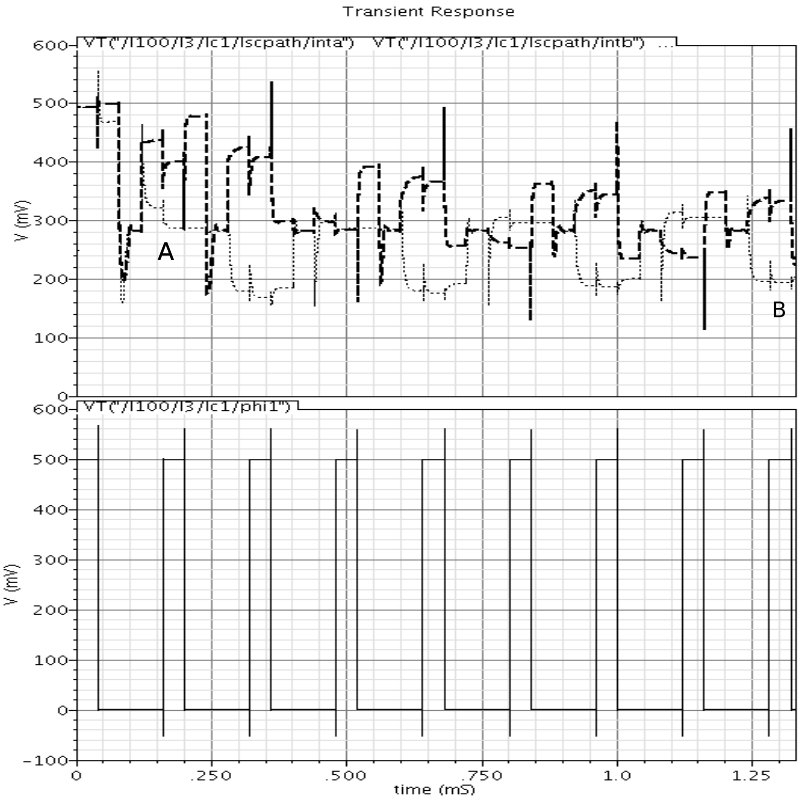

Figure 4.12: Schematic-level circuit simulation of the common-mode feedback transient at the first integrator. The integrator outputs (top) and the integrating clock for the common-mode correction (bottom) are shown. Both integrator outputs start at V_{DD} = 500mV. At point A, the correction is substantial whereas at point B the correction is minor as the common-mode is brought close to $V_{DD}/2$ within eight clock cycles of common-mode integration.

first-stage integrator, no reliable estimate may be made on the matching quality between the common-mode sampling capacitors and the integration capacitance. At the second integrator, both the common-mode and integrating capacitors are implemented in VNCAP and an assessment may be made on the relative quality of the matching between the common-mode sampling capacitors and with the integration capacitance. Mismatch between the common-mode capacitors and between the common-mode and integrating capacitors at the second-stage integrator is expected to be less than $\approx 2\%$.

Overall, common-mode transients are settled within several clock cycles as shown in Fig. 4.12 and are not expected to be a large source of error for this project where a large number of output samples will be averaged.

4.4.5 Charge Loss & Voltage Droop

A voltage held on a capacitor will discharge to substrate ground through any available resistive path according to the following relation,

$$V_c(t) = V_c(0)(e^{-t/RC}) \tag{4.38}$$

where $V_c(t)$ is the capacitor voltage over time, $V_c(0)$ is the initial value of the capacitor voltage and RC is the time-constant of discharge.

In the modulator design, capacitors as small as 50 fF at the common-mode feedback circuitry must hold their sampled voltage for tens of microseconds. A 50 fF capacitor, discharging through a 1 GΩ resistor undergoes a full time-constant

of signal loss ($\approx 30\%$) in 50 μs. To mitigate the impact of voltage droop, pseudo-differential circuitry is used. Impairment due to charge loss and voltage droop is expected in the modulator at low clock rates.

4.4.6 Integrator Settling

With the inverter transistors operating in deep subthreshold, the inverter amplifier bandwidth is expected to be low. Low amplifier bandwidth can adversely impact system performance by incomplete settling. The impact of incomplete settling can be understood by modeling the integration phase as a step input.

Assuming a single-pole amplifier response and a standard voltage input integrator, the output voltage is given by

$$V_o = \frac{C_s}{C_{int}} \left(V_{in} - V_{ref}\right) \left(1 - \exp^{\frac{-\Delta t}{\tau_{int}}}\right) \tag{4.39}$$

where $(V_{in} - V_{ref})$ is the step input voltage, C_s and C_{int} are the input sampling and integrating capacitors, τ_{int} is the 3 dB time-constant of the integrator and Δt is the available settling time in the integration phase. The integrator closed-loop response time-constant is given by,

$$\tau_{int} = \frac{1}{\beta_{fb}\left(2\pi \times f_u\right)} \tag{4.40}$$

where $\beta_{fb} = C_{int}/\left(C_{int} + C_s\right)$ is the closed-loop feedback factor and f_u is the unity-gain frequency of the amplifier. To settle to $(1 - \exp^{-N})$ of the final value, the amplifier gain-bandwidth must satisfy

$$f_u \geq \frac{N}{\beta_{fb}\left(2\pi \times \Delta t\right)}. \tag{4.41}$$

Historically, switched-capacitor circuits solved the problem of inadequate resistor matching in integrated filters. For accurate pole and zero placement for integrated filters, 0.1% settling was a common design goal. This level of settling required the integration clock phase to be roughly seven times the closed-loop time-constant which became a switched-capacitor design rule-of-thumb.

For the capacitive sensing $\Sigma\Delta$ modulator described in this report, however, the integrator linear settling requirements are not well constrained. Firstly, the inverter amplifier settling behavior is dynamic and the amplifier does not have constant unity-gain frequency over it's response. Secondly, low-performance $\Sigma\Delta$ modulation is extremely robust to gain errors[2] and linear settling error can be lumped into integrator gain error. Impact of distortion due to incomplete and non-linear integrator settling is typically addressed at the 16-bit performance level which is higher than the project design objectives.

4.4.7 Amplifier Gain-bandwidth & Open-loop Gain

The gain-bandwidth of the inverter amplifier is a function of the capacitive load, the inverter power supply voltage (V_{DD}), the transistor threshold voltage and the transistor size. The amplifier open-loop gain is determined by the small signal properties of the inverter transistors, namely the transconductance and the output impedance. This section calculates the expected capacitive load in the various integrator configurations and determines requirements for the amplifier gain-bandwidth.

The inverter integrator with parasitics and load capacitance is shown in Fig. 4.13

[2]The poles of a single bit modulator are dynamic. For stable modulator designs, excessive gain errors on the order of $\geq$ 20% can eventually cause the modulation to become unstable but small gain errors do not otherwise interfere with modulator loop performance.

in both the sampling phase (top) and integrating phase (bottom). The integrator total

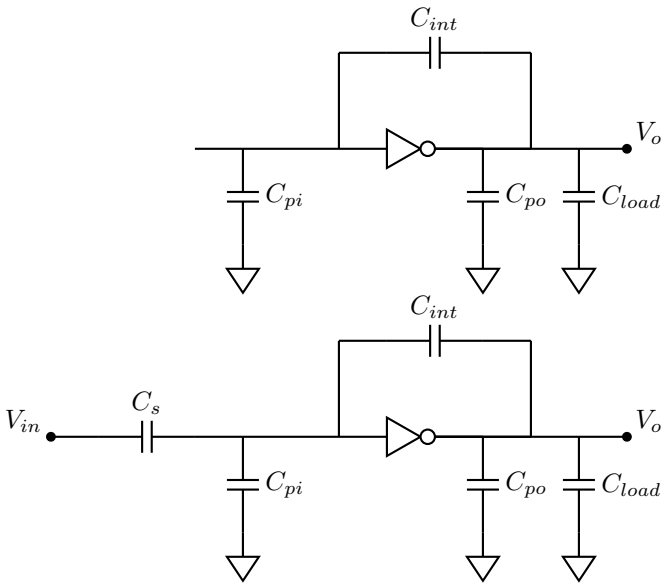

Figure 4.13: Simplified single-ended integrator shown with input and output parasitic capacitances in both integrating (top) and sampling (bottom) phases.

load capacitance, C_L, is given by,

$$C_L = \frac{C_{pi}C_{int}}{C_{pi} + C_{int}} + C_{load} + C_{po} \tag{4.42}$$

in the sampling phase, and

$$C_L = \frac{(C_{pi} + C_s)C_{int}}{(C_{pi} + C_s) + C_{int}} + C_{load} + C_{po} \tag{4.43}$$

in the integration phase. In the sampling phase, the input parasitic capacitance (C_{pi}) is composed of common-mode (C_{cm}) and holding capacitor (C_h) bottom plate parasitic capacitance to substrate as well as switch parasitic capacitances. In the integrating phase, there is additional parasitic capacitance from the input sampling

capacitance. The output parasitic capacitance (C_{po}) is composed of the integrator MOS transistor parasitic capacitance as well as integrating capacitor (C_{int}) bottom plate parasitic capacitance and switch parasitic capacitance to substrate. The output load capacitance (C_{load}) varies depending on the timing of the following stage and the common-mode feedback capacitors.

For calculation of total load capacitance and capacitive feedback factors, individual parasitic capacitances were modeled with Cadence CAPTAB analysis at the typical process corner. Parasitic capacitance due to routing was ignored. Tables 4.2 and 4.1 show the estimated total load capacitance and integrator feedback factor respectively for each inverter during each clock phase. The largest capacitive load is on $int1b$ during clock cycle ϕ4 and has a value of 850 fF. The worst case feedback factor of β_{fb}=0.04 is when the MEMS capacitors, C_1 and C_2, are switched into integrator $int1b$ during the clock cycle ϕ_4, and on $int1a$ during the clock cycle ϕ_2.

	$C_L(\phi_1)$	$C_L(\phi_2)$	$C_L(\phi_3)$	$C_L(\phi 4)$
$int1a$	450f	540f	n/a	550f
$int1b$	450f	240f	n/a	850f
$int2a$	n/a	n/a	260f	290f
$int2b$	n/a	n/a	260f	290f

Table 4.1: Estimated integrator capacitive loads during various clock cycles.

The amplifier gain-bandwidth was designed to be 5$\times$ larger than the switching rate at the nominal system clock and worst-case loading. The nominal system clock is $f_s = 3200$ Hz and the integrator switching rate is $4\times f_s$. To avoid short channel impact on the threshold voltage, the inverter amplifier transistor length was chosen as four times the minimum size. Fig. 4.4.7 shows the inverter amplifier gain-

	$\beta_{fb}(\phi_1)$	$\beta_{fb}(\phi_2)$
$int1a$	$\frac{C_{int1}}{2\times C_{cm1}+C_{int1}} = 0.7$	$\frac{C_{int1}}{C_1+C_2+C_{int1}} = 0.04$
$int1b$	$\frac{C_{int1}}{2\times C_{cm1}+C_{int1}} = 0.7$	$\frac{C_{int1}}{C_s+C_{int1}} = 0.67$
$int2a$	n/a	n/a
$int2b$	n/a	n/a

	$\beta_{fb}(\phi_3)$	$\beta_{fb}(\phi 4)$
$int1a$	n/a	$\frac{C_{int1}}{C_s+C_{int1}} = 0.67$
$int1b$	n/a	$\frac{C_{int1}}{C_1+C_2+C_{int1}} = 0.04$
$int2a$	$\frac{C_{int2}}{2\times C_{cm2}+C_{int2}} = 0.67$	$\frac{C_{int2}}{C_3+C_4+C_{int2}} = 0.57$
$int2b$	$\frac{C_{int2}}{2\times C_{cm2}+C_{int2}} = 0.67$	$\frac{C_{int2}}{C_3+C_4+C_{int2}} = 0.57$

Table 4.2: Estimated integrator feedback factors during various clock cycles.

bandwidth over process with a low-power transistor sizing of W/L = 10μm/0.48μm in the CMOS 0.13μm technology. The amplifier gain-bandwidth is exponentially responsive to the inverter power supply voltage V_{DD}. At $V_{DD} = 500$ mV, the amplifier gain-bandwidth is sufficient for $5\times4\times f_s \approx 63$ kHz at the typical process corner. This value was decided to be sufficient due to the variability of process and the lack of strict constraints on integrator settling.

Fig. 4.15 shows the inverter amplifier open-loop gain versus power supply voltage over process. As a single-stage amplifier, the open-loop gain was approximately 36 dB. The amplifier open-loop gain was unresponsive to inverter power supply voltage V_{DD} over the range of interest for the project.

4.4.8 Digital Supporting Circuits

This section describes the modulator digital supporting circuitry which includes the comparator, modulator control logic and the output level shifting buffer.

4.4.8.1 Comparator

Without the requirement for high-speed operation, the comparator did not have large design constraints. The comparator uses a latched cross-coupled pair input and an SR-latch output. The comparator was simulated to V_{DD} = 250 mV where it showed a worst-case delay over process variation of only t_d = 0.5 μs, which is insignificant compared to a total settling time of approximately 80 μs with a modulation clock of f_s = 3200 Hz. For flexibility during test, the comparator power supply was brought out individually to a package pin.

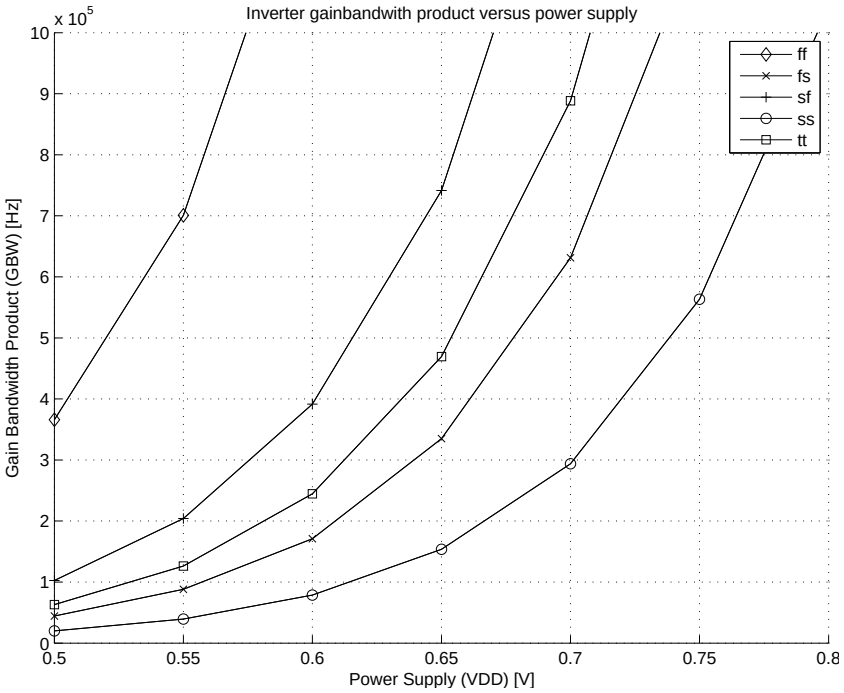

Figure 4.14: Schematic-level circuit simulation of inverter gain bandwidth versus power supply for C_L=0.9pF and W/L=10μm/0.48μm using the CMOS 0.13μm technology low-power transistor. The inverter was biased in the middle of the supply.

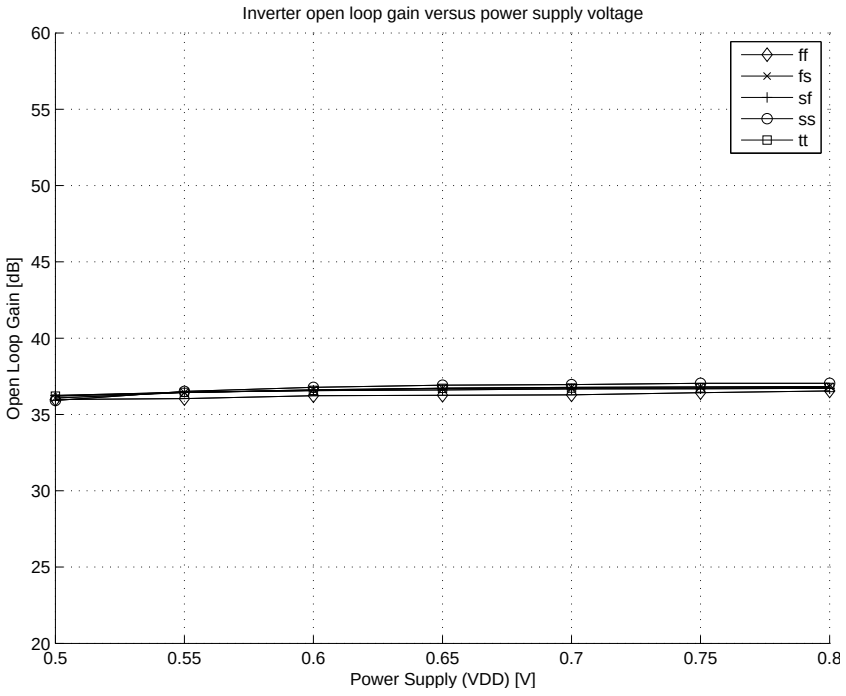

Figure 4.15: Schematic-level circuit simulation of the inverter amplifier open-loop gain versus power supply voltage for W/L=10μm/0.48μm using the CMOS 0.13μm technology low-power transistor.

4.4.8.2 Digital Control Logic

Control logic for the modulator includes clock signals the front-end sampling signals, ϕ_A, ϕ_B, ϕ_C, ϕ_D, ϕ_{cscm} and ϕ_{cdcm}, as well as integrator control signals, ϕ_{int1}, ϕ_{int2}. A buffer stage was used to increase the signal fan out in advance of the switches at the modulator, and to provide logical compliments for fully differential switching.

Note that the four-phase clock signals, ϕ_1, ϕ_2, ϕ_3 and ϕ_4 were not implemented on chip. These signals were brought in from off-chip, supplied to minimal sized gates at the logic control block, and buffered for use within the digital logic block. The four-phase clock used within the digital logic block was fed through to the buffer block and then provided on to the SC signal path.

The digital logic control block and buffer block were simulated together for worst-case delay over process and voltage. At voltages as low as 250 mV, the worst-case delay on the slowest corner was approximately 450 ns.

4.4.8.3 Output Level-shifting Buffer

The level shifter uses a cross-coupled pair to bring the output voltage up to the level of V_{DDIO}. The level shifted output voltage is buffered to be capable of driving 50 pF off-chip loads using power from V_{DDIO}.

The level-shifting buffer was simulated over process with voltages V_{DD} as low as 300 mV and V_{DDIO} at 1.2 V. Under these conditions, the level shifter was operational over process with an input pulse width of 160μs (f_s = 1600) but failed on the slowest corner at a pulsewidth of 80 μs (f_s=3200). With the output voltage of the level shifter reduced to V_{DDIO} = 500 mV, the circuit was functional with pulsewidths as

low as 10 μs.

The level shifter was also simulated to voltages as low as V_{DD} = 250 mV. In this circumstance, both the input and the output power-supply voltages were set to 250 mV. At 250 mV, the level-shifting buffer failed on only the slowest corner at a pulsewidth of 160 μs.

4.5 Design Summary

Previous sections described details of the modulator design. This section discusses the modulator operation in low-voltage and how the output bit-stream is used for pressure measurement. For the discussion, the switch-level circuit diagram of the modulator first shown on page 64 is repeated here in Fig. 4.16 for convenience.

There are several summary points to be made regarding the design. First, the SC signal path shown in Fig. 4.16 has no obvious limit to low-voltage operation. Decreasing the power-supply voltage impacts the operating performance of the MOS transistor circuit elements, but the operating region of each transistor is unchanged. The SC signal path consists of switches operating in the triode region, and inverter amplifiers operating in the subthreshold region. Decreasing the power-supply voltage impacts the switch on-resistance, and thereby impacts the settling accuracy of the switches, and also impacts the gain-bandwidth of the inverter amplifiers, which impacts the integrator settling.

Settling errors, however, have minimal impact on the operation of the circuitry. The input switches are switched between only two voltages preserving inherent

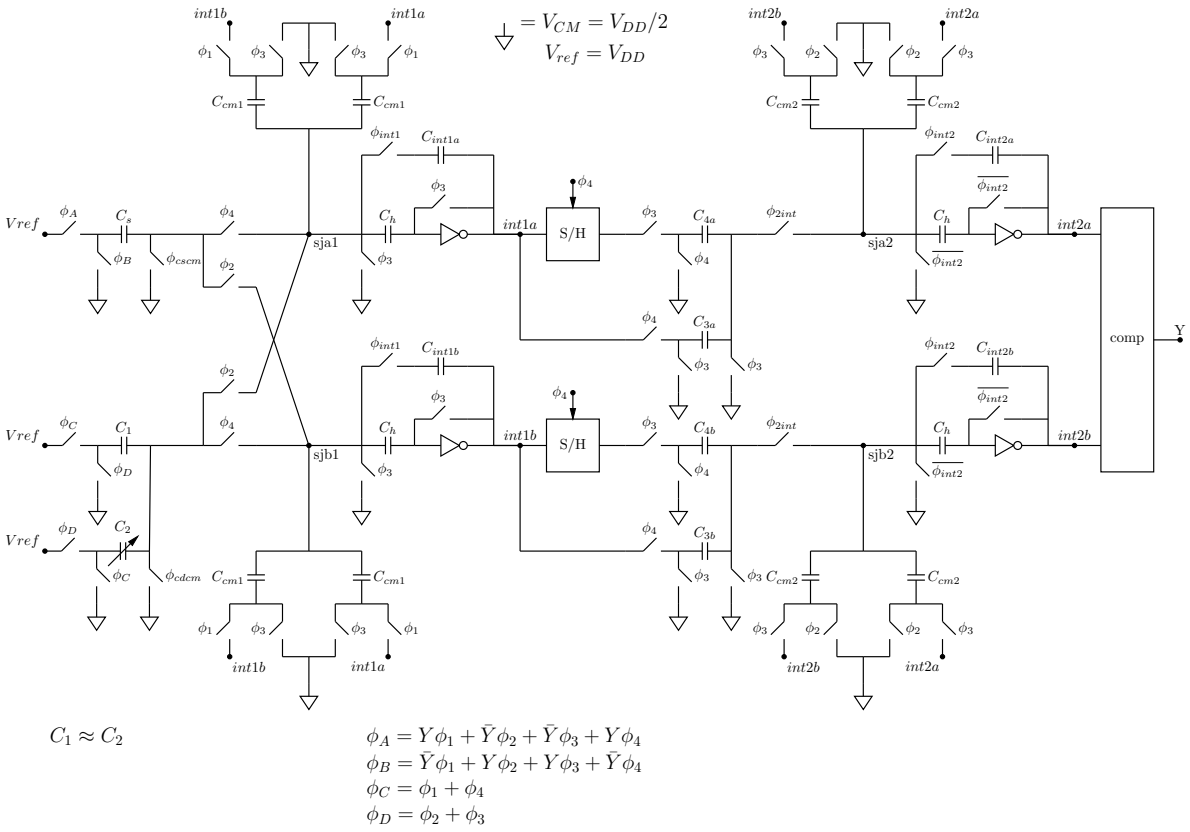

Figure 4.16: Switch-level diagram of the $\Sigma\Delta$ modulator for design summary discussion. Shown is the SC signal path; not shown are the digital logic block and buffers.

linearity; incomplete switch settling translates to an input gain error. Likewise, incomplete integrator settling presents as a gain-error in the integration, which may impair the closed-loop noise-shaping $\Sigma\Delta$ loop. Impairment in noise-shaping can cause "leakage" of quantization noise into the low-frequency region. This becomes problematic if the noise-floor is sufficiently low that leaked quantization-noise exceeds other noise sources to become the dominant noise source.

Settling errors can be mitigated with an increased settling time. At a particular power-supply voltage, however, the impact of settling errors may reside below the performance requirement. In this circumstance, increasing the settling time will have adverse effect on the total-energy required to sample; for a fixed number of single-bit samples, increasing the settling time increases the sample time and energy. Increased sample time also increases the likelyhood that voltage-droop may interfere with normal circuit operation.

Beyond the SC signal path are the comparator, the digital logic control and the buffers. Operating as subthreshold digital circuitry, these are impacted primarily by increased delay. The comparator is comprised of a regenerative-latch input stage followed by an SR-latch, both of which are robust to low-voltage operation given sufficient time. The comparator was simulated to V_{DD} = 250 mV where it showed a worst-case delay over process variation of only t_d = 0.5 μs, which is insignificant compared to a total settling time of approximately 160 μs with a modulation clock of f_s = 1600 Hz. Likewise, the digital control and output buffers combined showed a worst-case delay of 450 ns on the slowest corner at 250 mV. The level-shifting buffer circuitry was robust to low-voltage operation provided the input and output power-supply voltages were both brought down.

Modulator as Pressure Sensing Instrument The purpose of modulation is to encode DC pressure signals for telemetry to bring the data out of the ocular environment. The $\Sigma\Delta$ noise-shaping minimizes the impact of single-bit quantizer noise; the quantization noise is shaped through differentiation and thereby pushed into the high-frequency region. Front-end circuit noise is, on the other hand, transferred directly to output. To estimate DC pressure changes, the modulated bit-stream is received with a mean-value filter. The averaging process obtained by the mean filter can be considered in either the time-domain or the frequency-domain, as follows:

Time Domain in the time-domain, the mean-estimate is formed from an N-bit sample of the single-bit output,

$$\text{mean} = \frac{\sum_1^N x_i}{N} \tag{4.44}$$

where x_i are the logical values of the single-bit data output. The variance of the mean-estimate is the sum of the variances of each individual term in the summation, divided by the sample length squared

$$\sigma^2_{mean} = \frac{\left(\sum_i^N \sigma^2\right)}{N^2} = \frac{\sigma^2}{N}, \tag{4.45}$$

where σ is the variance of the population of the single-bit data.

Provided variance of each single-bit x_i is random and finite and the sample size N is sufficiently large, the central limit theorem provides that the mean-estimate follows a Gaussian-normal distribution. Under these conditions, the variance of the

samples of the mean-estimate is also a random variable with well defined statistics[3]. The standard deviation of the mean-estimate is $\sigma/\sqrt{N}$ and becomes smaller as the mean-estimate sample-size increases.

Frequency Domain in the frequency domain, the thermal-noise power or the amplitude spectral density can be used together with the effective-noise-bandwidth of the mean-estimate filter to determine the uncertainty in the mean-estimate. From page 78, the pseudo-differential input-referred spot-noise at 10 Hz was found to be $S_{V_t}(10Hz) = 0.015V/\sqrt{Hz}$ for the operating conditions of V_{DD} = 500 mV and f_s = 3200 Hz. The low-frequency noise consists primarily of aliased white-noise and is assumed to be very nearly white.

By using the relationship $\mathrm{q} = \mathrm{CV}$, the noise-amplitude spectral density can be converted to a charge-amplitude spectral density or a capacitance-amplitude spectral density. Using the nominal values of sampling capacitance $C_s = 250$ fF and sampling voltage V_{DD}/2 = 0.250 V, the capacitive-amplitude spectral density is,

$$S_C(10Hz) = 250 \times \frac{0.015}{0.250} = 15\frac{\mathrm{fF}}{\sqrt{Hz}}. \tag{4.46}$$

Taken over a predetermined bandwidth, the capacitive-amplitude spectral density produces a capacitive uncertainty which can be related back to a pressure uncertainty. Taking an average of N=10,000 samples, say, creates low-pass filter with an effective noise bandwidth of f_o = 1/NT. At f_s = 3200 Hz, T = 312 μs and an

[3]The variance of the mean-estimate samples follow the χ^2-distribution scaled by the multiplying factor of $\sigma^2/(n-1)$ with $n-1$ degrees of freedom, where σ^2 is the variance of the population of mean-estimates and n is the number of samples taken of the mean-estimate. Samples of the variance associated with the mean-estimate will themselves have a mean value which estimates the variance of the mean-estimate population; the variation of the sample variance is described by χ^2 statistics.

N=10,000 sample mean-estimate filter creates a noise bandwidth of 0.32 Hz causing a capacitive-error of approximately 8.5 fF. The sensitivity of the E1.3N capacitive sensor is expected to be 0.6 fF/mmHg. Charge from the MEMS sensor is injected into the modulation in a differential manner, so that the differential signal for a 1 mmHg pressure variation is 2×0.6 fF, or 1.2 fF differentially. This results in an uncertainty of 8.5 fF/(1.2 fF/mmHg) = 7 mmHg; taking N=100,000 the uncertainty may be reduced to $1/\sqrt{10}$ of this value, or 2.2 mmHg.

Summary As the power-supply voltage is decreased, the modulator will experience settling errors. These errors may become substantial, or may be swamped by circuit noise. Circuit noise in the modulator was designed to be power limited, with the dominant sampled noise being the inverter amplifiers; for low voltage operation, the inverter amplifier is expected to have restricted bandwidth and will contribute the dominant noise to the sampled input.

In pressure sensing, the design is ratiometric, meaning that the output bit-stream is related to the capacitive input ratio between C_s and $\Delta C = (C_1 - C_2)$. Thus the *signal* is not dependent on signal-swing range within the power-supply voltage and V_{DD} may be decreased to suit low-power operation needs. The actual operating value of V_{DD} depends on settling needs and is strongly dependent on process parameters.

4.6 System-Level Simulation

The previous sections described the design of sub-circuits required for the modulator. This section describes system-level simulations on the full modulator. The full modulator was simulated for ability to measure capacitance and for power consumption.

Due to prohibitively long simulation times, as explained below, the modulator was not simulated extensively for circuit-level impact on system performance.

4.6.1 Power Consumption

With the modulator operating at V_{DD} = 500 mV and f_s = 3200 Hz, the total modulator power consumption (excluding the level shifting output buffer) varied over process from 41 nW to 298 nW, with a typical process value of 95 nW.

In the design of the modulator, the inverter amplifiers operate with a nominal gate-voltage of $V_{GS} = V_{DD}/2$. For this reason, the design implemented the inverter amplifiers with low-power transistors (lpnfet and lppfet). The selection of low-power transistors at the inverter amplifier substantially reduced the power consumption; a modulator power consumption of approximately 8μW was required with the use of regular threshold transistors. The trade-off for using low-power transistors is a reduced inverter amplifier speed which was accounted for in the design.

The simulated power consumption versus power-supply voltage is shown in Fig. 4.17. The modulator was tested for power consumption over the voltage range of V_{DD} = 300–800mV; for the regular threshold transistor NMOS/PMOS pair, the sum of the threshold voltages was approximately 950 mV. Over the voltages tested, the power consumption increases exponentially with increasing power-supply voltage.

Simulated power consumption for the modulator at V_{DD} = 500 mV, f_s = 3200 and typical-process corner, is shown in Table. 4.3 broken down by functional circuit blocks[4]. The functional blocks within the design are: a) the digital logic control

[4]The generation of the four-phase clock was not completed on-chip. Rather, the four-phase clock

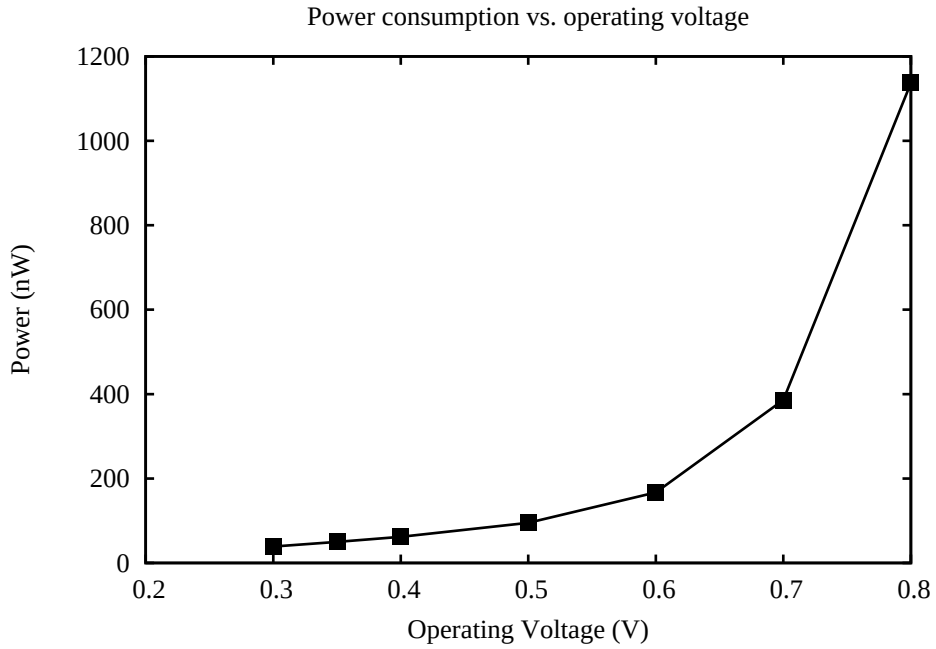

Figure 4.17: Schematic-level simulation of modulator power consumption versus operating voltage. Results are shown for V_{DD} = 300 mV–800 mV and f_s = 3200 Hz.

block; b) buffers for the control signals to the switches; c) the switched-capacitor signal path; and d) the comparator. The comparator is used to compare the output of the final integrator stage. The buffers provides increased fan-out and an inverted-logic signals for complementary switch control. The digital logic control block determines the SC signal path switch control signals from the four-phase clock inputs and the modulated output. From the functional block break-down of power consumption, the digital logic control block consumes the largest amount of power.

In addition to establishing all necessary switch controls for the SC signal path, the digital logic control block also inserted consistent gate-delays for various signals to preserve relative timing. The digital logic control block contained the highest

inputs were brought to near minimum-sized gates at the package level and then buffered internally.

Functional Block	**Power (nW)**
Logic control	37.3
Buffer	25.5
Total SC path	12.4
-stage 1 integrators	5.9
-stage 2 integrators	5.9
Comparator	20.9

Table 4.3: Schematic-level simulation of modulator power consumption for V_{DD} = 500 mV and typical-process corner. The total power in the SC signal path was dominated by the power at the integrators. Each integrator consumed approximately 1/2 of 5.9 nW, or 2.95 nW. The largest power consumption was at the digital logic block.

transistor count of all the functional blocks in the modulator; the logic block used 80 NAND-gates, 11 minimum-sized buffers and 4 increased ($4\times$) fan-out buffers. In order to test the SC signal path and modulator core circuits with predictable timing as the power-supply voltage was decreased, the digital logic block was implemented in with regular-threshold transistors (nfet and pfet). At the expense of additional leakage current and power, regular threshold transistors at the digital logic control block ensured that gate-delay was less sensitive to process variation and was predictably short.

To reduce the power consumption of the digital logic control block, low-power transistors may be used. The IBM 0.13 μm technology advises that a $100\times$ reduction in leakage current may be expected between the regular and low-power transistors. For a 0.13 μm technology inverter delay can ranged between 0.16 ns–0.45 ns [115] for regular transistors and low-power transistors. With the highest clock rates of f_s = 6400 Hz, the time between individual clock phases is approximately 40 μs. With clock pulse widths on the order of 40 μs, the modulator could be tolerate to increased control logic throughput delay, provided that relative timing of the switch control signals is preserved.

Controlled relative timing is critically important in SC circuits in order to avoid imbalancing sampled or integrated charge. Delay in digital circuits when operating in subthreshold varies exponentially with variations in threshold voltage; timing in digital logic operated in deep subthreshold is increasingly sensitive to process variation and variations in threshold-voltage due to a decreased V_{GS}. Ultra low-voltage digital circuit design is an area of active research [115–122], including increased robustness to process variation [117, 123].

For ultra low-power digital logic, increased delay and substantially decreased power is possible. One technique is to stack additional transistors in order to achieve a local body-effect, increasing the transistor threshold-voltage and decreasing sub-threshold channel leakage, as is described in [115]. Such modifications to digital logic circuits can substantially increase throughput delays, from 0.45 ns to 4 μs on an inverter, but also substantially decrease power consumption, from 10 nW to 5 pW at 10 kHz operation.

4.6.2 Capacitive Detection

Fig. 4.18 shows the results of simulation of the modulator to estimate capacitance C_2 as determined according to Eq. 3.22 on page 37. The modulator was simulated at the schematic level with UltraSim and operating conditions of V_{DD} = 500mV and f_s = 3200. The results show that even with only 1000 points taken for the mean estimate, the modulated output was able to be related back to the input capacitance.

The same simulation for larger capacitance at C_1 and C_2 ($\approx$ 6 pF) produced no meaningful results for fF capacitance variation with sample sizes of only 1000 single-bit data points.

4.6.3 Simulation Time

The switched-capacitor circuitry in this research used low sampling rates. The time between individual clock phases is 40 μs at a modulator clock rate of f_s = 6400 Hz. Because of the nature of circuit simulators, which must converge the differential equations to the specified accuracy at the internal time step, simulation for accurate

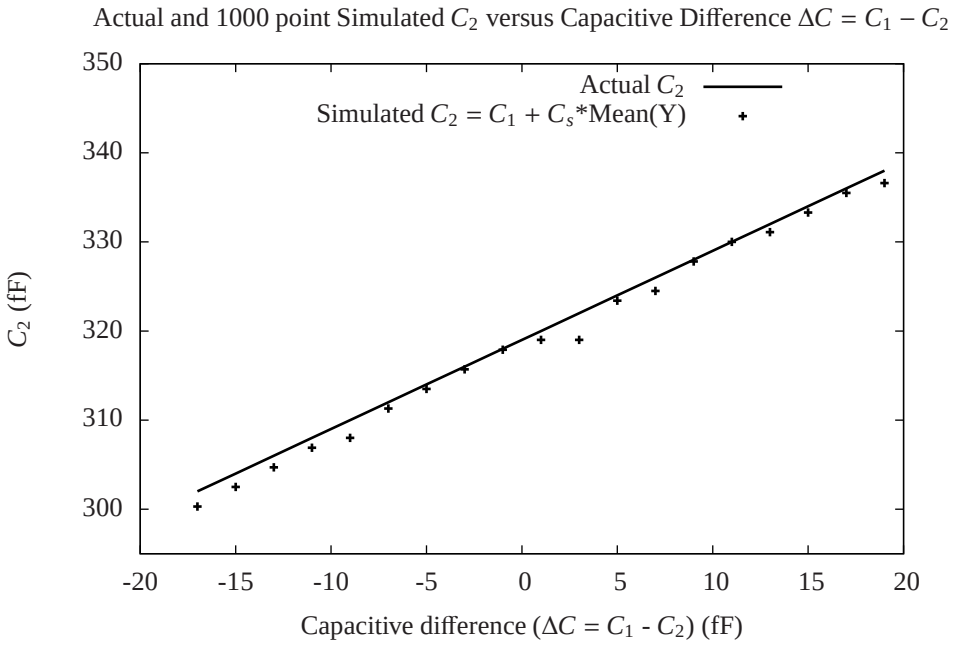

Figure 4.18: Schematic-level circuit simulation showing C_2 versus capacitive difference $\Delta C = C_1 - C_2$. Actual values of C_2 used in the simulation sweep are shown by the solid line. Simulated results are obtained with 1000 samples of the single-bit output. Results show the mean value of the modulated output can be related back to the varying capacitance.

performance of the overall system was problematic.

Simulation to obtain long samples of single-bit data was completed using the chip-level FASTSpice simulator, UltraSim. At f_s = 6400 Hz, 160 milliseconds of simulation was required to obtain 1000 single-bit data samples. Simulations with Ultrasim using an analog simulation mode and a high accuracy setting (comparable to Spectre "conservative"), took just over 25 minutes to complete; capacitive sweeps with 20 points took 8.5 hours to complete. To complete the same sweep with 100k single-bit data samples would take 35 days.

It is important to note that the Ultrasim simulator is not as accurate as Spectre. The UltraSim FASTSpice simulator is intended for chip-level operational verification and digital block performance checks, but not necessarily for accurate performance of individual analog circuit blocks contained within the larger chip. In this project in particular, the analog circuitry has integrators which can accumulate error and make the overall result much less reliable.

The approach taken with simulation prior to tape-out was to verify analog subcircuit performance over process and expected supply voltage variation, and to verify the system level operation through FASTSpice simulations.

4.7 Integrated Circuit Fabrication

This section describes the integrated circuit layout and capacitive element sizes. A list of layout pad names and their description is provided in Appendix E.

4.7.1 Top Level Layout

The core area of the modulator is 775 μm x 445 μm. The layout is shown together with the bonding concept for attachment to the two MEMS sensors in Fig. 4.19. The die (AS1) was taped-out using a tile of 2000 μ x 1000 μm. Due to additional bond-pads required for voltage and pressure-bonding options, the layout was pad limited. Care was taken in the top-level layout to handle the analog signals and references (on the leftmost side) away from digital power supplies and clock signals (on the rightmost side). The digital output buffer and level shifter, V_{DDIO}, was expected to be the largest signal aggressor and was placed at the lower right side of the die near the digital control logic generation and clock input pads. To minimize the loop area of the inductive path for output driving currents, the current return path (V_{SS}) was placed directly beside V_{DDIO}.

The digital control logic was laid out by hand with repeated cells that provided ease-of-placement rather than compactness. The voltage references, V_{ref}, V_{refC1}, and V_{refC2} were routed in thick metal traces seen directly under the integrators; where free space was available nearby, the reference voltage metal traces were bypassed. The modulator digital control distributed to the SC signal path crossed the reference voltage lines in perpendicular fashion at a single location after the first integrator. Care was taken to distribute the integrator clocking such that delays were matched. Layout and timing of critical delays, such as sampling at the final

integrator and activation of the comparator, were carefully inspected and verified with chip-level extracted simulation.

4.7.2 Capacitor Values

This section describes the values of the capacitors selected for the SC signal pathway. Inherent in the design, the modulator had a variable power supply voltage and variable amplifier performance. This generated few constraints to determine capacitive element sizing. Where no constraint was available, values were chosen as small as reasonable to limit power consumption. Values were decided to be reasonably small if they were implementable without compromising reliability and the values sufficiently exceeded nearby parasitic element values.

At the first integrator, C_s and C_{int1} are implemented with matched metal-insulator-metal (MIM) capacitors. Capacitors past the first integrator were primarily implemented in the vertical natural capacitor, VNCAP, realised by inter-metal direct and fringing capacitance. Capacitor sizes of less than C = 100 fF were only supported by VNCAP in the technology.

C_s	250 fF
$C_{int1a,b}$	500 fF
C_{cm1}	110 fF
C_{cm2}	50 fF
C_h	100 fF
$C_{S/H}$	200 fF
$C_{3a,b}$	100 fF
$C_{4a,b}$	50 fF
$C_{int2a,b}$	200 fF

Table 4.4: Implemented capacitor values in SC signal path.

A sample-and-hold capacitor implementing a delay to C_4 is implemented in VNCAP at approximately 200 fF. Voltage mode input is implemented with a bond-option with pad $c1a$ connected to $cm1a$, $c2a$ connected to $cm2a$ and cdb connected to $cmdb$. Matched on-chip MIM capacitors of C_m = 210 fF are used to implement the voltage input mode.

4.7.3 Bypass Capacitors & Layout Dummy Elements

Power supplies V_{DD} and V_{DDCOMP} are bypassed at the integrated circuit core with 16 pF and 10 pF MIM capacitors capacitors respectively. At the integrators, further bypassing is done with VNCAP where space allows. At each integrator, V_{DD} and V_{CM} are bypassed with approximately 0.35 pF.

Dummy elements where provided in the layout to improve matching. Wherever sensitive capacitor and transistor matching were required, dummy elements were used to extend the layout environment uniformity and improve element matching.

In addition, there were several bypass-capacitors distributed over the layout area. Both the common-mode voltage, V_{CM}, and the integrator power supply voltage, V_{DD}, were bypassed at several locations around the circuit layout. Insufficient bypassing can introduce distortion to the signal path. Common-mode capacitors, for instance, draw charge proportionate to the integrator output swings. This is signal dependent charge draw and can introduce harmonic distortion if the common-mode voltage is not insufficiently bypassed.

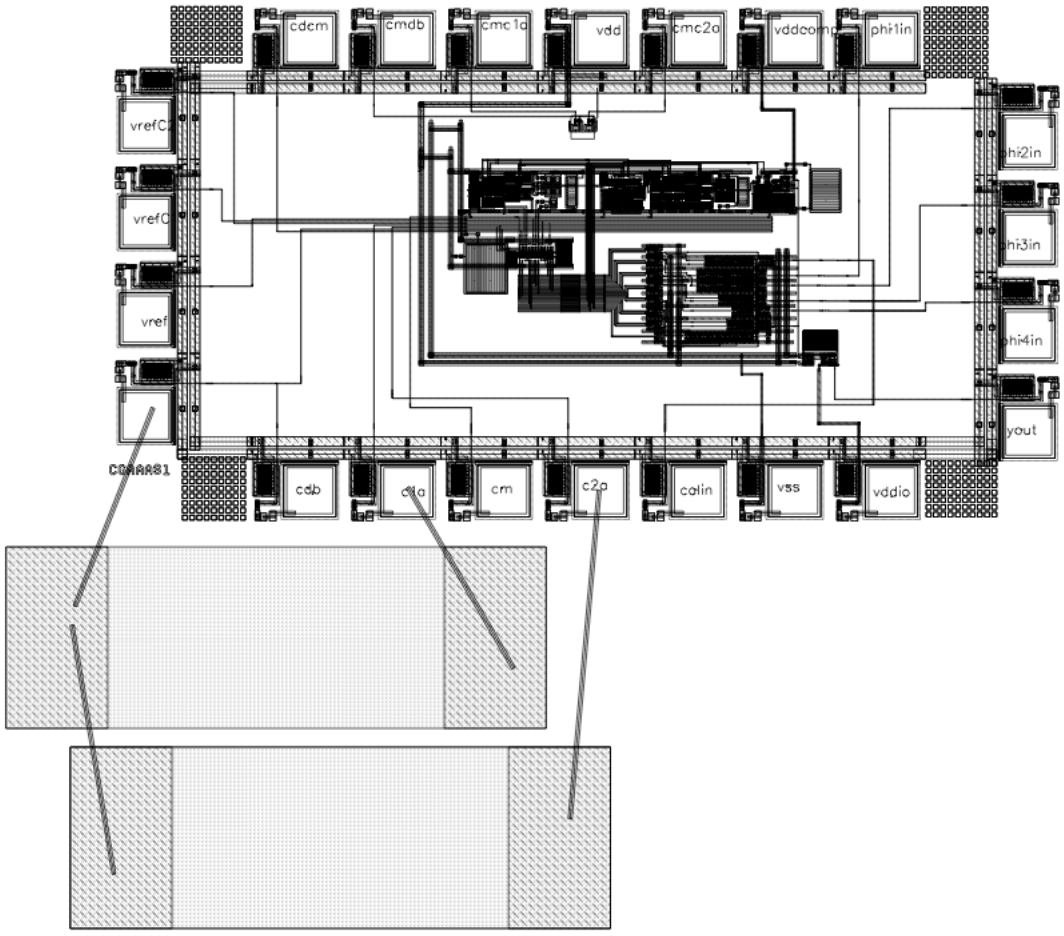

Figure 4.19: Diagram of die level prototype, AS1-MEMS, consisting of the integrated circuit die AS1 wire-bonded with two MEMS capacitive sensors. One capacitive sensor will be rendered insensitive to pressure by application of a sealant.

4.8 MEMS Capacitive Sensor Wire-bond

To test the modulator with pressure input, the integrated circuit die AS1 is designed to be wire-bonded with two E1.3N MEMS sensors. After wire-bonding, one MEMS is rendered insensitive to pressure with the application of epoxy. Figure 4.19 shows a diagram of the AS1 die is shown bonded with to-scale mock sensors. The wire-bond implements the die level prototype, AS1-MEMS. The wire-bond is implemented inside the cavity of 40-pin ceramic dual in-line IC package (DIP).

4.9 Summary

This chapter described the low-voltage, low-power circuit-level design of the $\Sigma\Delta$ modulator capacitance-to-digital converter.

To achieve low-voltage, low-power operation the modulator was implemented with inverter amplifiers operating in deep subthreshold. Within this chapter, the operation of the modulator was described during each cycle of the four-phase clock. A pseudo-differential signal path was used with a four-phase clock. The inverter amplifiers required output common-mode control through input charge injection. Correlated-double-sampling was used to establish a virtual-ground node. Because the virtual-ground is controlled at both branches of the signal path, the use of correlated-double-sampling also improves the operation of the pseudo-differential signal path.

Subcircuit design was completed with consideration of a varying power-supply voltage and sample-clock frequency; the design of the modulator subcircuits was done in such a way as to be tolerant to varying test conditions. Circuit noise analysis was completed with periodic-noise simulations on the first integrator. At an operating voltage of V_{DD} = 500 mV and sampling frequency of $f_s s$ = 3200 Hz, the circuit thermal noise levels anticipated a peak performance of SNR_t = 19 dB in voltage mode and roughly 7 mmHg pressure uncertainty in N=10,000 sample mean-estimate.

The design choices made in this project favored low-power operation over low-noise operation. Whereas other work has used the inverter amplifiers in weak inversion to preserve speed of operation [86], this work operated the inverter amplifiers in deep subthreshold. The majority of the modulator input noise is derived

from the transistors of the inverter amplifiers. It is anticipated that long samples of the single-bit output will decrease the impact of thermal noise and allow improved resolution pressure resolution.

CHAPTER 5

EXPERIMENTAL RESULTS

This chapter describes the results of experimental testing on the modulator.

5.1 AS1 Die Bond Options

For voltage testing, the integrated circuit die, AS1, was bonded into a voltage input option, with on-chip capacitors. The voltage input bonding is shown in Fig. 5.1. For pressure testing, the AS1 die was hybrid bonded with two MicroFAB E1.3N MEMS pressure sensitive capacitive sensors, as shown in Fig. 5.2. The prototype hybrid-bond instrument is named AS1-MEMS.

Die Identification For this work, several different die were tested. The tested die are distinguished in this report by DX, where X represents the unit number.

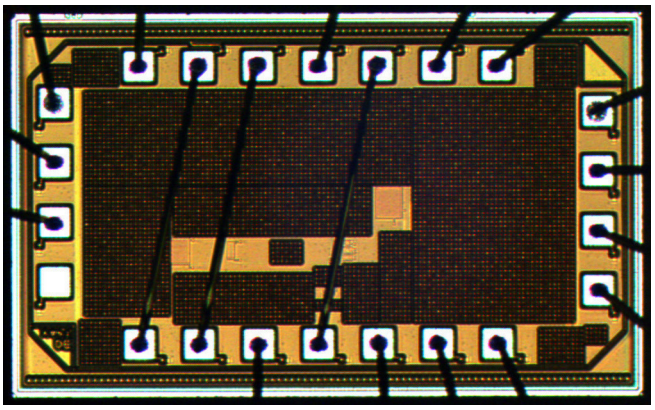

Figure 5.1: AS1 die shown bonded for voltage input testing. Bond lines are shown crossing AS1 connecting the input sampling switches to onboard matched capacitors.

5.2 Test Setup

Testing of the AS1 die, and the AS1 bonded to MEMS capacitors, was completed using the printed circuit board AS1TB1. The AS1TB1 board is described in more detail in Appendix. G.

For pressure testing, an air-tight chamber was built using a Pelican case enclosure. Reference pressure and temperature were measured using a Bosch Sensortec BMP085 high-precision pressure and temperature sensor. Pictures of the pressure test set-up, including the pressure chamber and test board AS1TB1 can be seen in Sec. 5.3.3 on page 139.

Test board AS1TB1 provides the required input signals for the modulator. The modulator requires four non-overlapping clock phases scaled to the power supply of the device under test, the power supplies V_{DD}, V_{DDCOMP} and V_{DDIO}, a mid-supply voltage $V_{CM} = V_{DD}/2$ used for analog ground, and a fully-differential input voltage signal. The fully-differential input voltage signal was provided using an ADC-driver at the test board AS1TB1. The power supply V_{DDCOMP} supplies the comparator

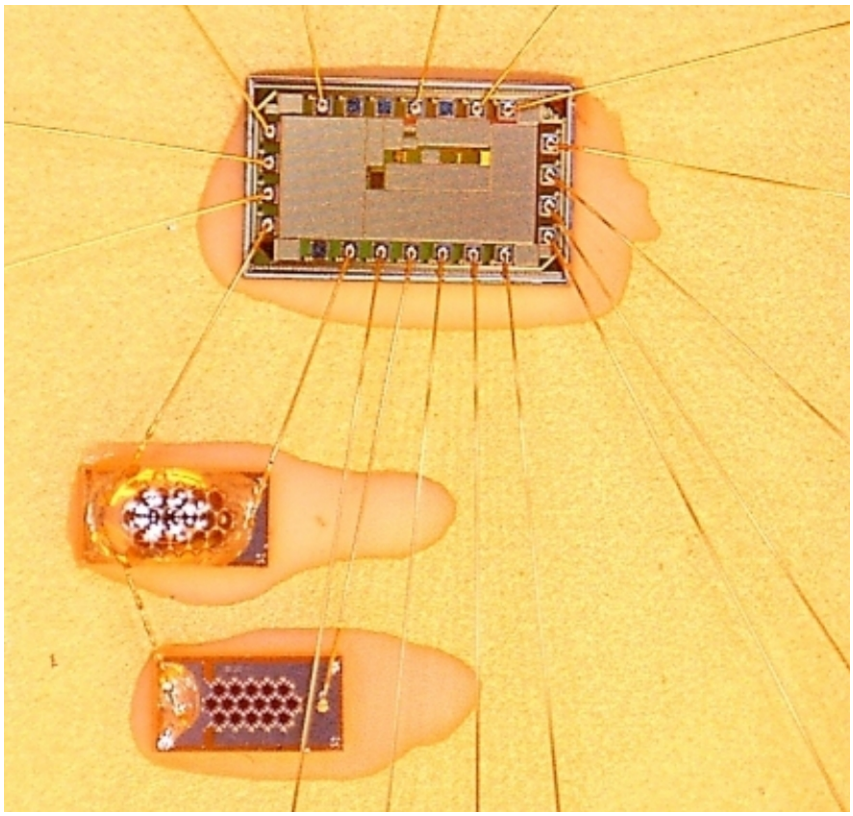

Figure 5.2: AS1 die bonded for pressure input testing with two MEMS capacitive sensors. One MEMS sensor is rendered insensitive to pressure with the application of application of epoxy.

only; the power supply V_{DD} supplies all other circuitry required for modulation (digital logic and buffers, as well as the full SC signal path). The power supply V_{DDIO} supplies the level-shifting output buffer only. The output buffer brings the modulated output off chip. The buffered modulated output was collected using an Adruino Uno microcontroller and stored on a computer for analysis.

Power consumption is calculated from measured voltage and current. Current is measured using jumpers at V_{DD} and V_{DDCOMP} on the AS1TB1 board. To measure current, a Keithley 6487 Picoammeter is placed in series using one of the jumpers.

Each current measurement was obtained using an average of 100 individual readings. The collection and averaging analysis of 100 individual samples was facilitated by Keithley 6487 built-in functions.

5.3 Measurement Results

Whereas pressure-input testing evaluates the prototype pressure sensing instrument for IOP measurement, voltage input testing provides performance measures of the modulator.

5.3.1 Voltage Mode Operation

In voltage mode, the modulator was tested with both AC and DC input signals. Important performance measures are the effective number of bits (ENOB) and the power consumption.

5.3.1.1 AC Input

The AC testing of the modulator was conducted with a voltage input signal frequency of 4 Hz. The modulator sampling frequency, f_s, and the power-supply voltage were varied. For spectral analysis of the wide-band $\Sigma\Delta$ output, a Hann window [124, 125] was used on the data as described in Appendix H. The SNR and SNDR were calculated from the power spectra of the single-bit output using a "brick wall" filter approach[1] at a bandwidth of 25 Hz.

[1] A brick wall filter has full transmission in the passband and complete attenuation in the stop band.

Table 5.1 shows a summary of the modulator peak performance for AC testing. The selected test power supply voltages (275 mV, 300 mV, 500 mV and 600 mV) were chosen to bracket the design value of 500 mV and to capture the lowest surviving operating voltage. If it was observed to improve performance at severely reduced power supply voltages, the reference voltage was lowered to below the power supply voltage. At 600 mV the modulator achieves a peak SNDR of 25.5 dB (3.9 ENOB) with a power consumption of 125 nW. At 300 mV, the modulator achieves a peak SNDR of 18.7 dB (2.8 ENOB) with a power consumption of only 23 nW. Decreasing the voltage to 275 mV, the modulator SNDR decreased to 15.2 dB (2.2 ENOB) with a power consumption of 21 nW.

The ADC FOM, which is traditionally applied to the comparison of analog to digital converters, was used with the modulator as a method of comparing performance with varying operating conditions of voltage supply and clock frequency. Of the values tested, the best FOM was obtained at 300 mV where the modulator obtained a peak SNDR of 18.7 dB (2.8 ENOB) with a power consumption of 23 nW. Between 300 mV and 275 mV, distortion increased and worsened the SNDR without a commensurate reduction in power, resulting in a worsening of the FOM. Also as the power-supply voltage increased to 600 mV, the FOM worsened. At increased voltages, the amount of leakage power consumed in the digital control block exceeds the performance improvement available from increased input signal swing and the FOM is thus decreased.

Performance This section discusses issues related to the modulator performance, including process variation, reduced integrator swing, lowest operating voltage and

AC Test Results					
Device	D7	D4	D4	D4	D4
Supply voltage	250 mV	275 mV	300 mV	500 mV	600 mV
Power	17.9 nW	21 nW	23 nW	52 nW	125 nW
Vref	250 mV	200 mV	200 mV	500 mV	600 mV
BW	25 Hz	25 Hz	25 Hz	25 Hz	25 Hz
f_{sys}	3200 Hz	6400 Hz	6400 Hz	12800 Hz	25600 Hz
f_s	800 Hz	1600 Hz	1600 Hz	3200 Hz	6400 Hz
OSR	16	32	32	64	128
Peak SNR	9.3 dB	16.0 dB	20.2 dB	23.5 dB	29.5 dB
Peak SNDR	8.1 dB	15.2 dB	18.7 dB	23.5 dB	25.5 dB
ENOB	1.0	2.2	2.8	3.6	3.9
FOM	178 pJ/step	91 pJ/step	66 pJ/step	85 pJ/step	167 pJ/step

Table 5.1: Modulator AC voltage performance summary. The FOM was defined in Equation 2.1 on page 23 and is used here to compare performance at differing operating conditions. The frequency of the sampling clock was varied with the power supply.

performance versus input frequency.

Process Variation The modulator performance is subject to process variation between tested units. Figure 5.3 shows the peak SNR and SNDR versus input voltage for three units D5, D6, D7. Due to harmonic distortion, the peak SNDR is generally lower than the SNR. The SNR is related to the average value of the noise floor which, although affected by process, is fairly consistent between the units. The SNDR, on the other hand, is related to available integrator range which is impacted by system offset voltages and which can have a high variability between units.

Reduced Integrator Swing By lowering the reference feedback voltage, V_{ref}, the integrator output swing requirements are reduced and the harmonic distortion is

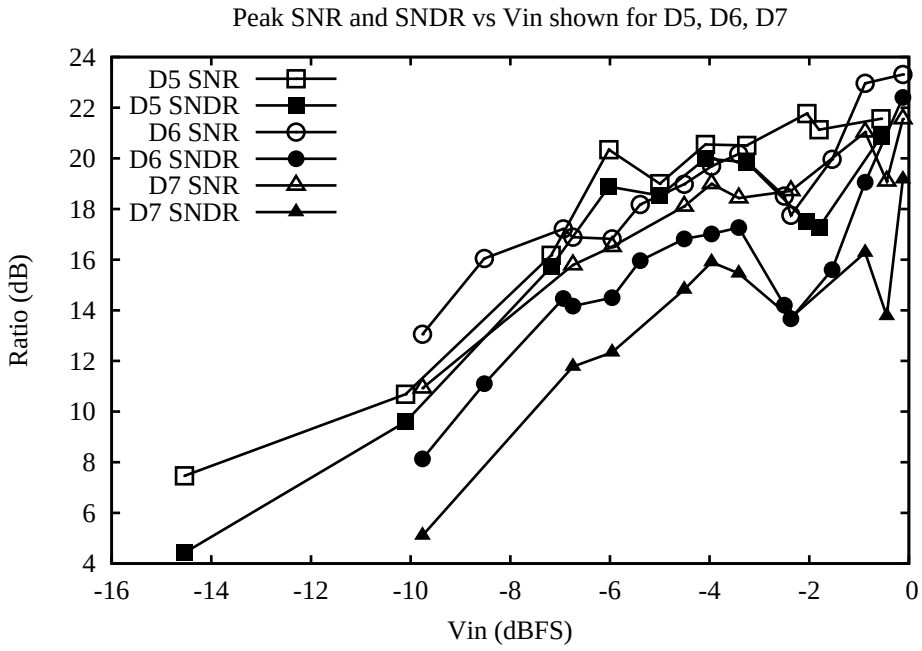

Figure 5.3: Experimental test results for SNR and SNDR versus input voltage for D5, D6 and D7 operating at $V_{DD} = V_{DDCOMP}$ = 400 mV with f_s = 1600 Hz. The power consumption was 35.5 nW, 42.5 nW and 38.0 nW for D5, D6 and D7 respectively.

decreased. The SNR and SNDR versus input signal is shown in Fig. 5.4 for D8 with V_{DD} = 275 mV and f_s = 1600 Hz. While the SNR remains similar throughout the input range, the SNDR was slightly improved when V_{ref} = 200 mV compared with V_{ref} = 275 mV plotted on the same graph. The PSD for V_{in} = -13 dBFS is shown in Fig. 5.5 for both V_{ref} = 275 mV and V_{ref} = 200 mV. Here, noticeable impairment to the NTF and STF is observed with V_{ref} = 275 mV, as well as mildly increased harmonic distortion.

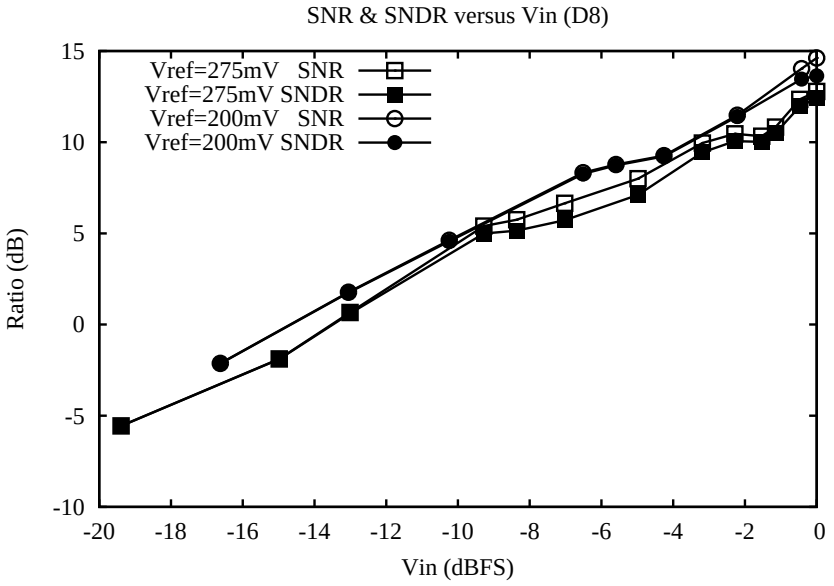

Figure 5.4: Experimental test results for SNR and SNDR shown for D8 with V_{DD} = 275 mV and f_s = 1600 Hz. Results are shown for two different values of the reference feedback voltage, V_{ref} = 275 mV and V_{ref} = 200 mV. Power consumption was 23 nW in both cases. The SNDR improves slightly when V_{ref} is reduced.

The presence of second-order distortion in the PSD indicates poor operation of the pseudo-differential signal path. In all cases, even at V_{DD} = 275 mV, the

correlated double sampling circuit is believed to be working; power spectral density formed with energy scaling shows no indication of 1/f noise. At V_{DD} = 275 mV, the modulation NTF is seen to be impaired at high frequencies.

Lowest Operating Voltage The modulator was operational at V_{DD} = 250 mV with a reduced performance, and failure typically occurred around V_{DD} = 230 mV. At $V_{DD} = V_{ref}$, the SNR was 9.3 dB, the SNDR was 8.1 dB and the ENOB = 1.0 with a power consumption of 17.5 nW (D7). Results were similar for D6 (ENOB 0.9, 18.7 nW) and D8 (ENOB = 0.3, 19 nW).

Performance at Various Frequencies Figure 5.6 shows the SNR and SNDR versus input frequency for D8 operating at V_{DD} = V_{ref} = 275 mV and f_s = 1600 Hz. For this test, harmonic distortion terms continue to be collected beyond 25 Hz. The SNR and SNDR are identical indicating that the performance measures are noise dominated. The SNR and SNDR remain relatively stable over the input signal bandwidth; the standard deviation for both SNR and SNDR is just over 1 dB which does not exceed expected variation in the calculation technique.

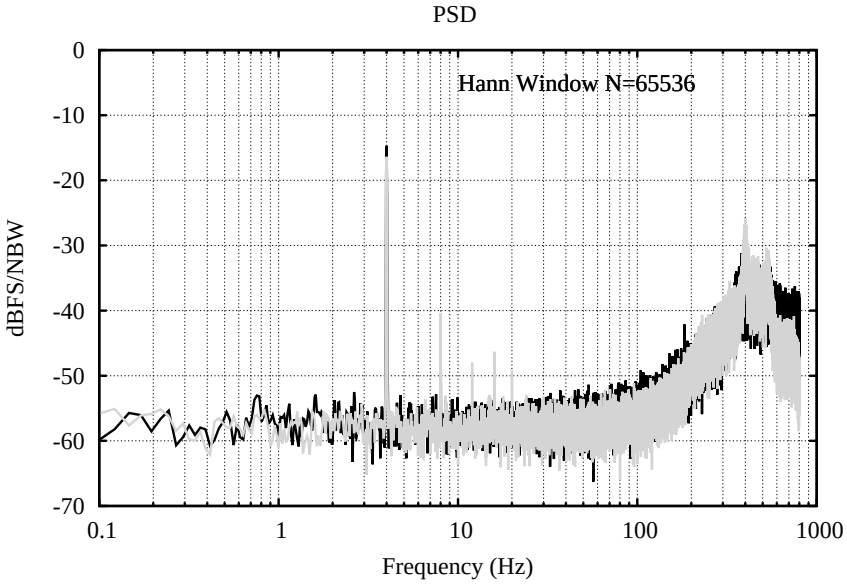

Figure 5.5: Experimental test results for power spectral density for D8 with V_{DD} = 275 mV and f_s = 1600 Hz. The PSD is shown for V_{in} = -13 dBFS with the two different conditions V_{ref} = 275 mV (grey) and V_{ref} = 200 mV (black). The higher value of V_{ref} led to slightly increased distortion and impairment in the modulation noise shaping, as seen at the highest frequencies.

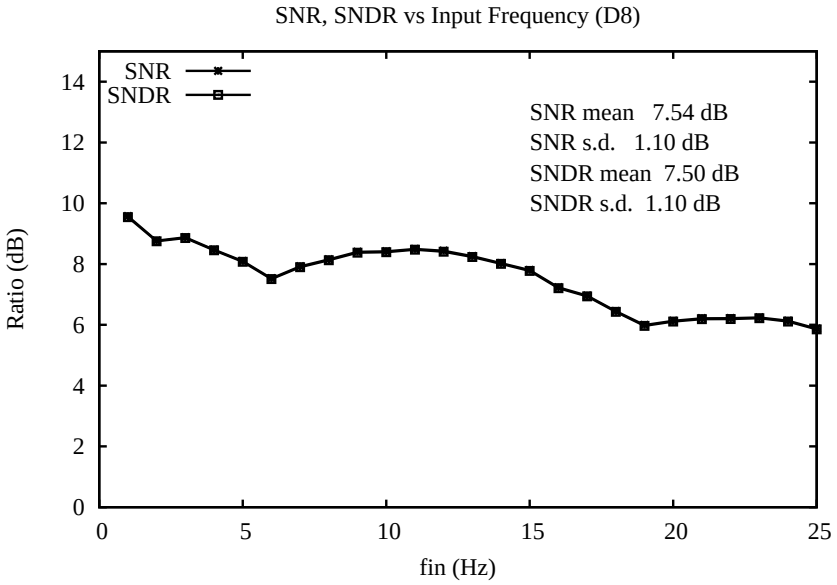

Figure 5.6: Experimental test results for SNR and SNDR versus input frequency for D8 with $V_{DD} = V_{ref}$ = 275 mV, f_s = 1600 Hz and the fully-differential input signal near full-scale at V_{in} = 422 mV. Mean and standard deviation of the measures are indicated on the plot. The SNR and SNDR remain relatively stable over the bandwidth from 1–25 Hz.

Power Consumption This section assesses the relative contributions of static and dynamic power consumption in the modulator operation at various frequencies. An objective of this project is to explore the lowest operating power and voltage. It is of interest to understand limitations to the perceived benefit of decreased speeds within the designed circuitry.

Static and Dynamic Power The modulator power consumption is due to both static and dynamic current. For the purposes of this document, static current is defined as current consumed other than current required to integrate or sample onto capacitors. In the modulator, static current is caused by transistor subthreshold leakage at switches and logic, and subthreshold leakage current associated with the inverter amplifiers.

By design, the inverter amplifiers operate with a nominal gate-voltage set near V_{DD}/2. Transistors in the inverter amplifier are implemented with low-power transistors available in the technology; all other transistors in the circuit are regular threshold MOS. In simulation, the dominant power consumption occurred at the digital logic control block and overall power consumption followed a characteristic exponential response with increasing voltage.

By disconnecting capacitors C_1 and C_2 from the input signal path, the modulator is placed in a calibration mode. In calibration mode, the output oscillates between logical high and logical low (10101010); power is concentrated at f_s/2 and dynamic power is at it's maximum. At this time, the circuit includes sampling capacitor C_s but not C_1 and C_2 (which have been disconnected). Modifying the clock rate can

affect the relative proportions of static and dynamic current requirements. At lower voltages, below roughly V_{DD} = 400 mV, the calibration-mode ceased to function and although the output was very active the oscillation was no longer exactly "0101010".

Figures 5.7 and 5.8 show power consumption for V_{DD} and V_{DDCOMP} versus the modulator sampling frequency, f_s. The impact of dynamic power on V_{DD} is most observable past approximately f_s = 1600 Hz. The current at V_{DDCOMP} is for the comparator alone and is relatively insensitive to frequency over the range. Both currents scale with power supply, but V_{DD} is a stronger function of supply.

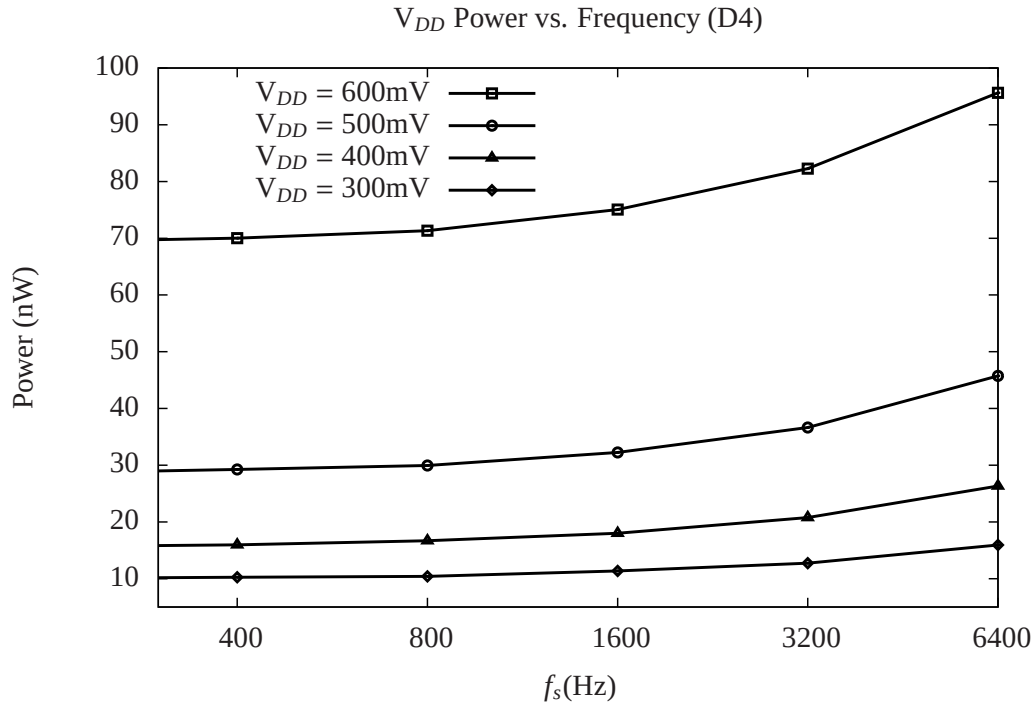

Figure 5.7: Experimental test results showing power consumption at V_{DD} versus modulator operating frequency f_s for unit D4.

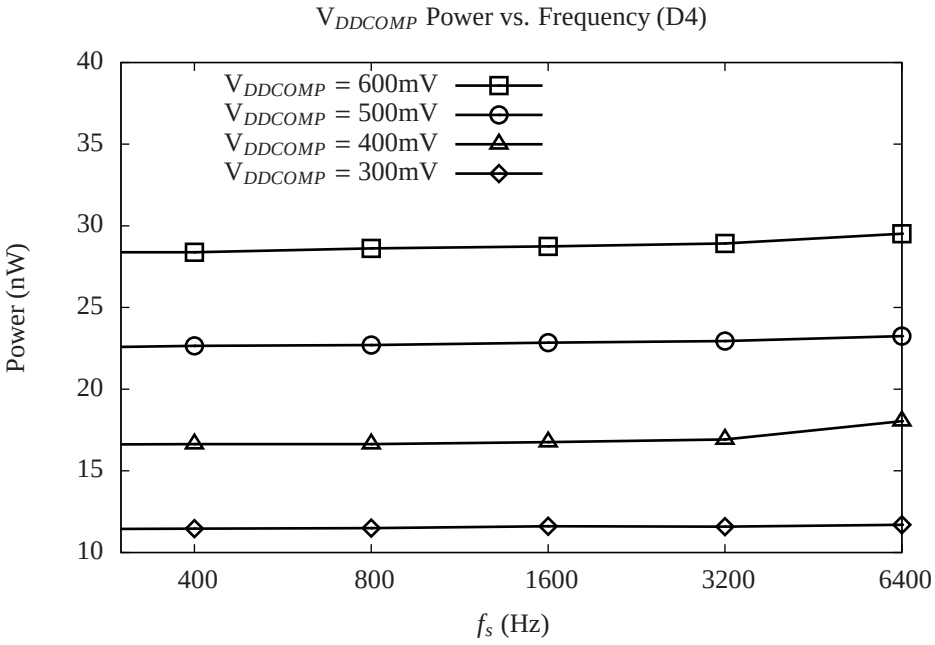

Figure 5.8: Experimental test results showing power consumption at V_{DDCOMP} versus operating frequency f_s for unit D4.

Power versus frequency for several values of V_{DD} is also shown in Figure 5.9. Extrapolating the curve to $f_s = 0$ Hz provides an estimate of the leakage power. At $V_{DD} = 400$ mV and $f_s = 3200$ Hz, the leakage power estimate represents approximately 80% of the total operating power. A plot of the estimated power at $f_s = 0$ Hz versus the power-supply voltage, V_{DD}, is shown in Fig. 5.10. The power consumption versus power-supply shows an exponential character consistent with the expected voltage dependent response of subthreshold leakage power.

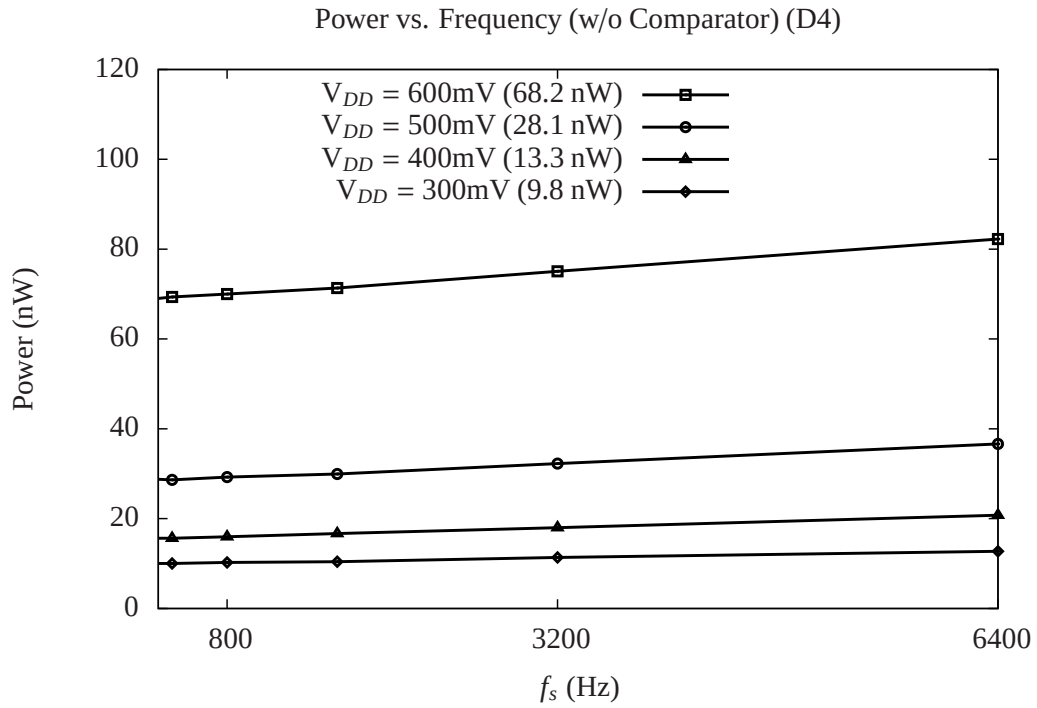

Figure 5.9: Experimental test results showing power consumption at V_{DD} versus frequency f_s for D4, and showing zero-frequency intercept at each supply voltage. The zero-frequency intercept power provides an estimate of leakage power consumption.

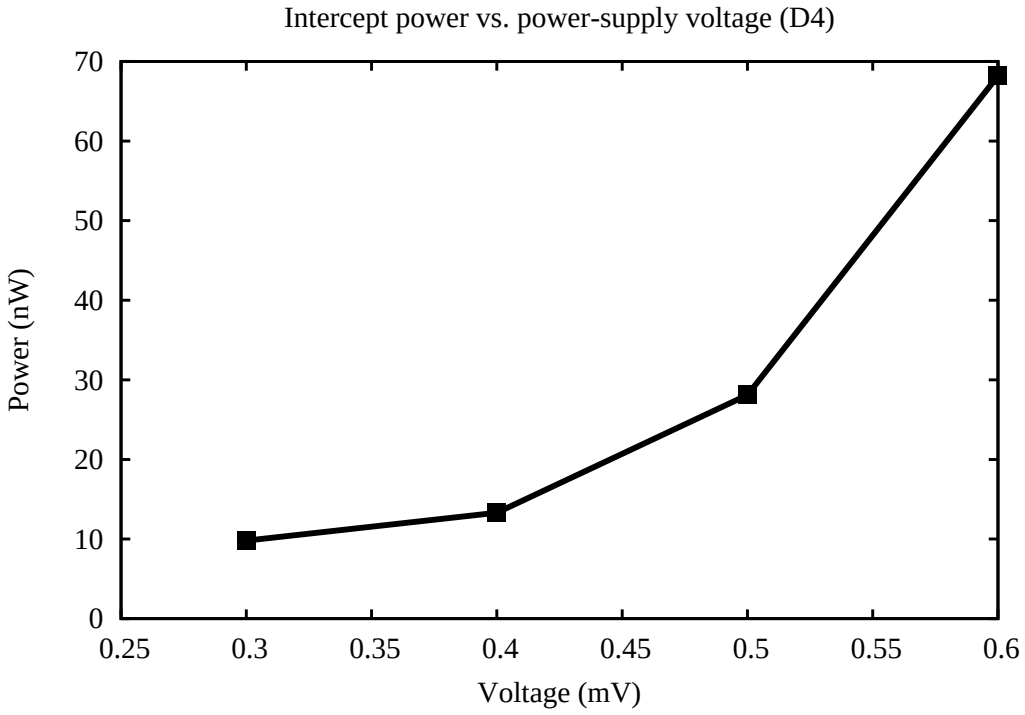

Figure 5.10: Experimental test results showing the zero-frequency intercept power versus the power-supply voltage, V_{DD}, for unit D4. The power consumption has characteristic exponential increase with increasing V_{DD}.

The results shown are not exhaustive; the integrated circuits were tested by hand and the data collection was not automated. The key observation is that trade offs need to be considered for the circuit within in the application. While a lower clock speed will result in a minimal operating power, lower clock rates have a diminishing return because a the majority of power consumption is static power. For fixed sample lengths, low clock speeds result in longer sample times and fast clock rates result in shorter sample times. Design limitations, however, impact performance at both ends of the frequency spectrum. At slow speeds, voltage droop may impact circuitry, such as the common-mode feedback in the pseudo-differential signal path, and impact comparator operation through poorly controlled common-mode content at the second integrator. At high speeds, performance can be adversely impacted by incomplete switch settling.

The dominant power consumption in modulator was subthreshold leakage power at the digital logic control block. To ensure consistent relative-timing over process variation, this block was implemented in regular threshold transistors. The power-supply voltage has the a strongest impact on the modulator total operating power; decreased instrument operating frequency had a lesser impact. To reduce the power consumption of the digital blocks it is of interest to explore alternative power-reducing logic structures with reduced sensitivity to process variation [117, 123].

5.3.1.2 DC Input

The modulator was tested for response to DC input at various supply voltages. For testing, a DC differential input voltage was applied to the input V_{refC1} - V_{refC2}. The DC input voltage was measured with a handheld multimeter at an earlier point in the circuitry. The modulator single-bit output was collected and a mean-estimate was obtained. The mean-estimate was used as the instrument output response to DC input voltage.

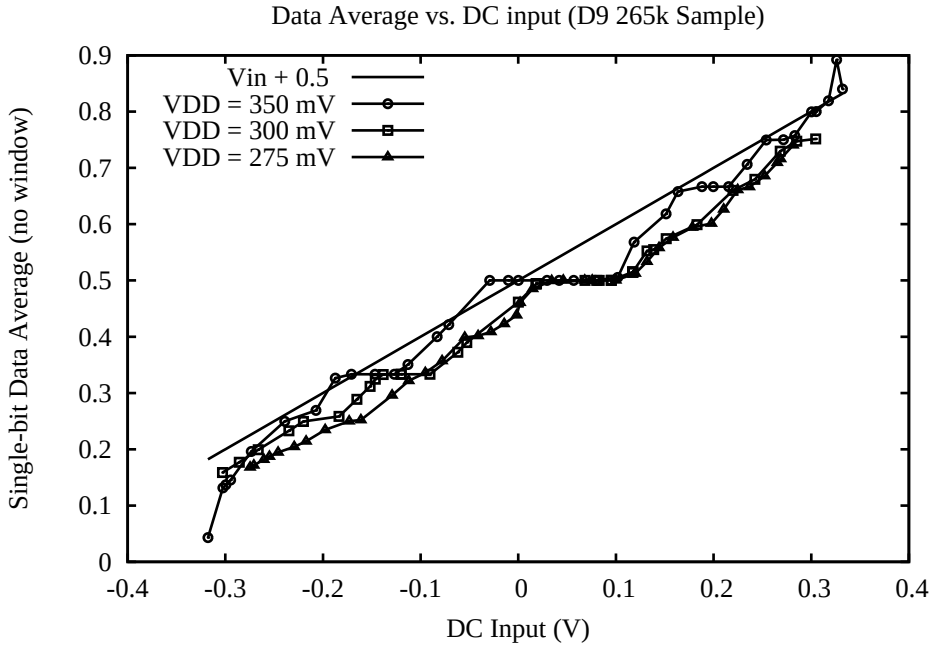

Figure 5.11: Experimental test results showing single-bit mean-estimate versus DC input voltage for D9. The data average is obtained from the mean-estimate of 265,000 single-bit samples. The expected result, which would produce an average of 0.5 for a 0 V input, is shown with a solid line. Data was obtained with V_{ref} = V_{DD}.

The mean-estimate was fitted to a straight line for each of the power-supply

voltages tested. The results are shown in Table 5.2. While the results shown are for mean-estimates obtained with 265,000 single-bit data points, these results were substantially unchanged from mean-estimates obtained from single-bit data samples as short as 5,000.

Modulation dead-zones are most noticeable near zero input and were most significant at V_{DD} = 350 mV. The best linearity was obtained at V_{DD} = 275 mV but this also coincided with the largest offset from the expected transfer function.

N=265k	V_{DD}	Slope	Offset	RMS Residual
	350 mV	1.062	0.472	0.034
	300 mV	0.926	0.442	0.023
	275 mV	0.982	0.433	0.018

Table 5.2: Parameters for straight line fit of response to DC input. The best fit resulted with V_{DD} = 275 mV, but this also coincided with the largest offset. The largest dead zone occurred with V_{DD} = 350 mV.

Overall, the modulator response to DC input was very rough and the showed several dead-zones, where the modulator was unresponsive to input changes. The large fitting residuals, an indicator of poor response due to dead zones, is on the order of tens of millivolts. As discussed on page 42, a lack of response to stimulus on the order of millivolts would correspond to a capacitive insensitivity of an similar amount of fF. Specifically for V_{DD} = 350 mV, the DC test results indicate a potential capacitive insensitivity as high as 48 fF using the observed residual value of 23 mV. The modulator had relatively minor variation in slope and offset in the DC input response with variation in supply voltage V_{DD}.

5.3.2 Summary

Voltage testing of the modulator provided a general performance overview. The AC performance indicators of the modulator, SNR and SNDR, were dominated by the circuit noise floor and the modulator ENOB ranged from 3.9–1 over a power-supply voltage variation from V_{DD} = 600 mV–275 mV. The modulator was operational at voltages as low as V_{DD} = 250 mV with power consumption on the order of 20 nW. The following section presents the results of pressure mode testing.

5.3.3 Pressure Mode Operation

The prototype IOP measurement instrument, AS1-MEMS, was created by wire-bonding the AS1 die with two MicroFAB E1.3N MEMS pressure sensitive capacitive sensors. The wire-bond was done inside the 40-pin DIP package cavity. One MEMS capacitor was rendered insensitive to pressure with the application of epoxy[2]. The AS1TB1 board and the the AS1-MEMS instrument were placed inside a pressure test-chamber. The pressure chamber was constructed from a Pelican brand water-sport utility case. The Pelican case was fitted with Swagelock valves for the controlled insertion (removal) of air for pressure increment (decrement) with a 60 mL plastic syringe. A hermetically-sealed circular connector is used to bring electrical signals into and out of the chamber as shown in Fig. 5.12. The Pelican case pressure-release valve (black valve on the case front in the top image) was sealed internally with epoxy to allow positive pressure within the case. The test environment is discussed in more detail in Appendix G.

The pressure sensitivity of MicroFAB E1.3N MEMS capacitive pressure sensors in the pressure range of interest is 0.6 fF/mmHg. The E1.3N also has temperature sensitivity of 0.6 fF/^{o}C [15]. The pressure chamber is instrumented with a BOSCH BMP085 high-precision pressure and temperature sensor with data obtained over an I^{2}C interface controlled by an Arduino Uno microcontroller. Pressure and temperature data from the BMP085 is collected and place into the file footer of each sample taken from the AS1-MEMS. The resolution capability of the BMP085 is 0.0075 mmHg. Over a range of 525 – 825 mmHg, the BMP085 has an accuracy of $\pm$0.15 mmHg and $\pm$0.5^{o}C when operating at a nominal temperature of 25^{o}C.

[2]LePage Speed Set Epoxy was used

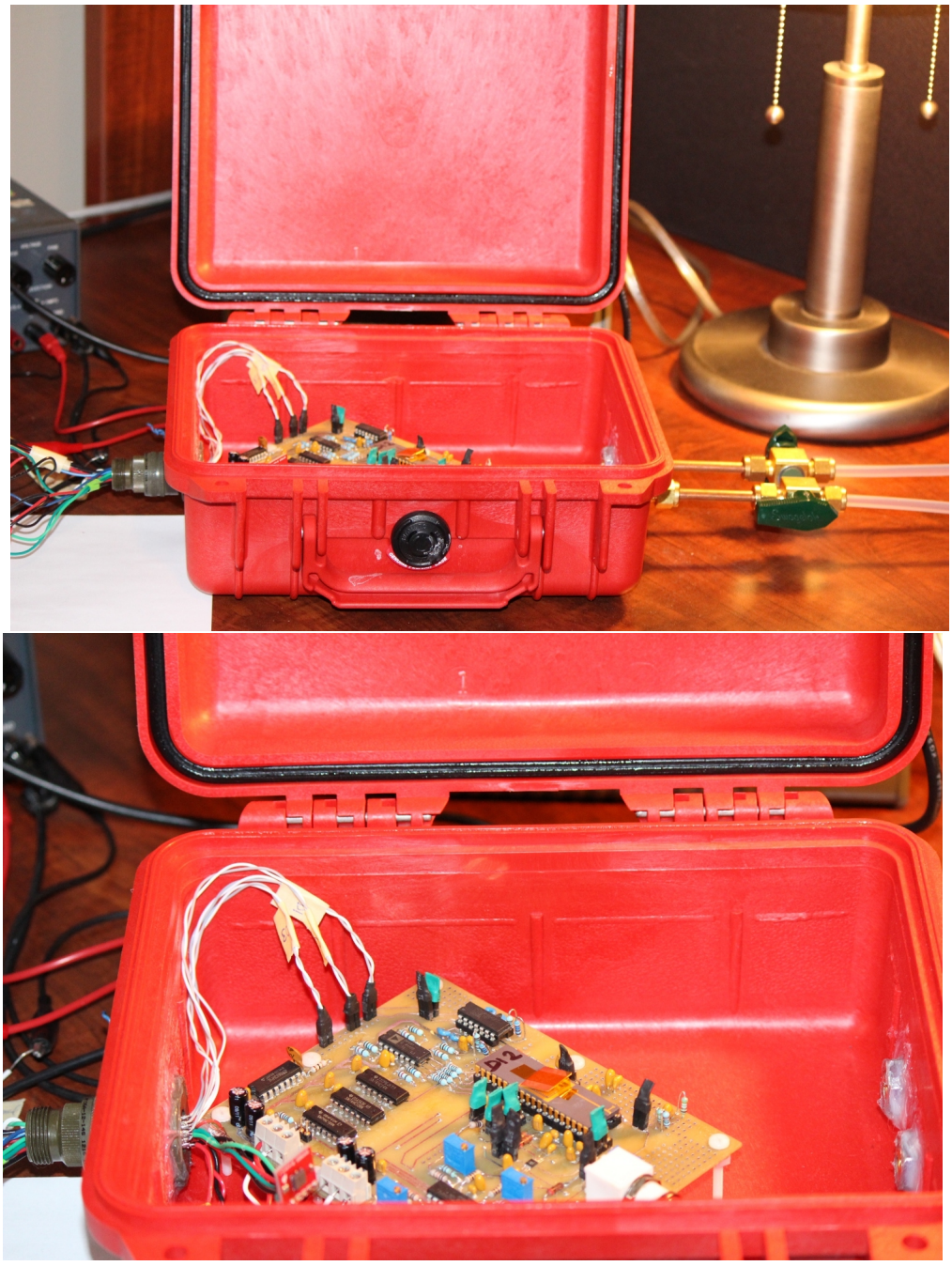

Figure 5.12: Experimental test setup, showing Pelican brand case made into a pressure test chamber. Inside the chamber, AS1-MEMS is shown on the test board AS1TB1. A hermetically sealed circular-connector is used for electrical inputs and outputs seen on the left hand side of the top image. Air is admitted or released with a 60 mL HSW syringe using the nylon tubes seen on the right hand side of the top image. Swagelock valves are used to maintain pressure conditions, or allow air transport. The bottom image shows D12 with the lid held ajar with Kapton tape.

Chamber temperatures observed during testing of AS1-MEMS ranged from 25 – 27 ^{o}C with high consistency over any given testing period; temperature variation over any specific test was much less than 0.1 ^{o}C. The BMP085 was located approximately 1.5 inches away from the AS1-MEMS inside the chamber.

Data Handling A mean-estimate is formed from an N-bit sample of the single-bit output,

$$\text{mean} = \frac{\sum_1^N x_i}{N} \tag{5.1}$$

where x_i are the logical values of the single-bit data output. The variance of the mean-estimate is the sum of the variances of each individual term in the summation, divided by the sample length squared,

$$\sigma^2_{mean} = \frac{\left(\sum_i^N \sigma^2\right)}{N^2} = \frac{\sigma^2}{N} \tag{5.2}$$

where σ is the variance of population of single-bit data.

Provided that the sample size N is sufficiently large and the variance of each single-bit x_i is finite and random, the central limit theorem provides that the mean-estimate follows a Gaussian-normal distribution. Under these conditions, the variance of the samples of the mean-estimate is also a random variable with well defined statistics. The standard deviation of the mean-estimate is $\sigma/\sqrt{N}$ and becomes smaller as the mean-estimate sample-size increases. Thus the mean-estimate is an unbiased estimator of the population mean.

The experimental test results were used to plot the error in the mean-estimate

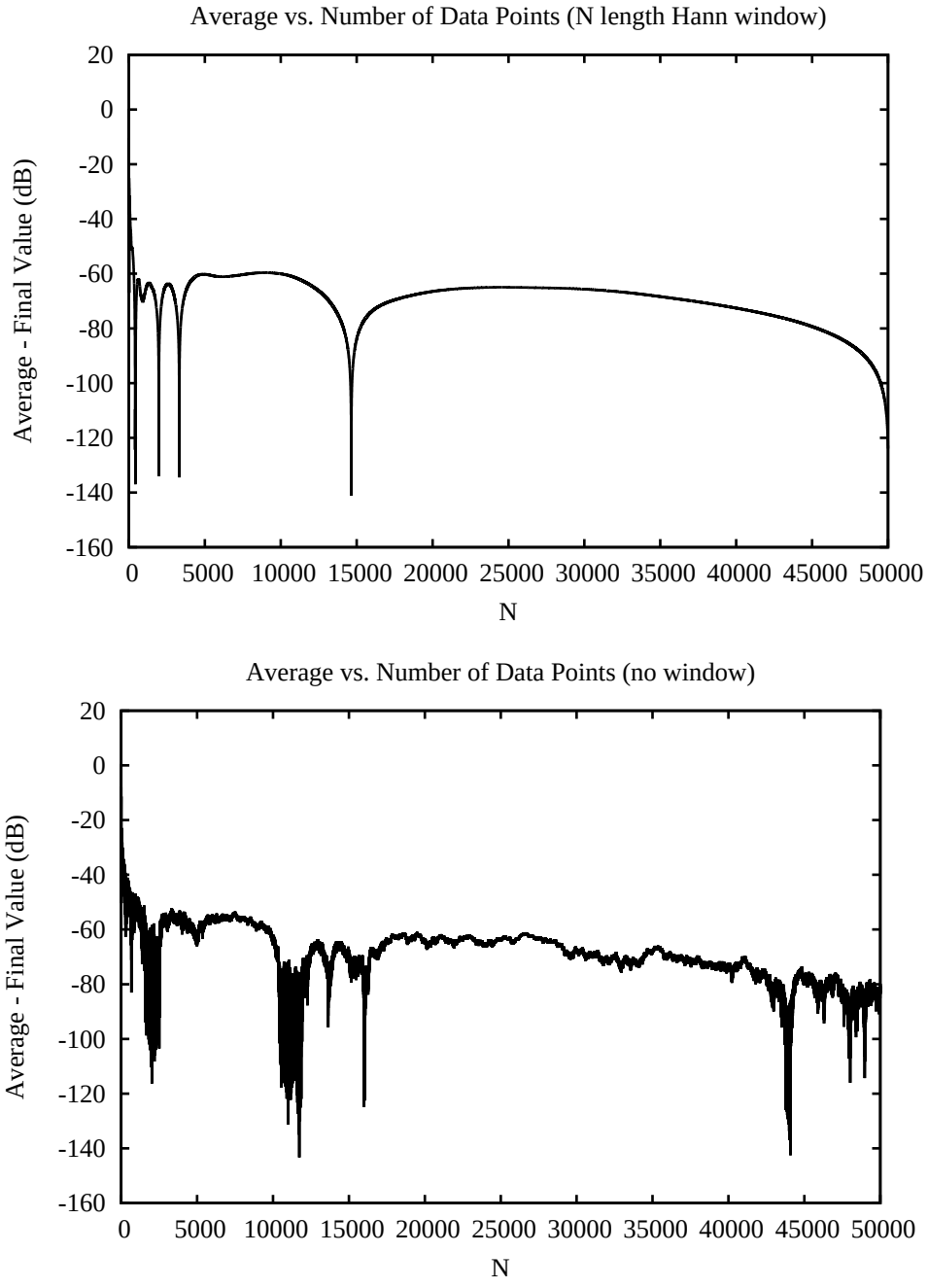

Figure 5.13: Experimental test results showing error in the mean-estimate versus the number of data points taken, compared with the final mean-estimate value. Results are shown with Hann Window filtering (top) and without (bottom). The mean-estimate value used for the comparison was obtained with N=50k windowed data points. Points of extremely low error result of the estimate occasionally converging to the final estimate value. Overall, the curves indicate that the error settles rapidly and there is diminishing return past approximately N = 5–10k data points.

versus the number of data points used in the mean-estimate in Fig. 5.13. The results are similar with and without windowing of the data but, due to reduced sensitivity on the most recent bits obtained, windowing produced a smoother variation in response. Both results showed a diminishing return for averages much longer than approximately N = 5–10k in length.

The sample length determines the length of time required for sampling and thereby the energy consumed. The performance and energy trade off is of research interest. To preserve equal weighting on each data point, an unwindowed mean-estimate was selected to represent the instrument output. It is important to note that while an unwindowed mean-estimate applies an equal weighting to each data point, it may also result in increased sample-to-sample variation particularly in the presence of modulation tones.

Instrument Performance The AS1-MEMS was tested over the pressure range from 700 mmHg to 770 mmHg.

Figures 5.14 through 5.17 show the AS1-MEMS mean-estimates from single-bit data samples varying in length from 10k to 1M. Results are shown for unit D12 operated with V_{DD} = 325 mV, f_s = 1600 Hz and a power consumption of 30 nW. The mean-estimate increased monotonically with increasing pressure and the response was linear. The instrument error was calculated as the integral non-linearity, or maximum deviation from a straight line fit, over the tested pressure range. The results were not substantially changed with the use of windowed data.

The AS1-MEMS error, sample-time and energy are summarised in Table 5.3 below. The sample time is determined by the number of data points obtained divided by the single-bit data rate. The error is defined as the worst-case deviation from the

linear fit over the pressure range. The desired pressure resolution for this project, approximately 2 mmHg, was achieved with a sample-length of 100k obtained over approximately one minute for a total energy usage of 1.88 μJ.

Data Points	Time (seconds)	Energy (μJ)	Error
10k	6.25	0.18	$\leq$ 7.6 mmHg
50k	31.25	0.93	$\leq$ 3.2 mmHg
100k	62.50	1.88	$\leq$ 2.1 mmHg
1M	625.00	18.80	$\leq$ 3.0 mmHg

Table 5.3: Tabulation of experimental test results for AS1-MEMS instrument showing the number of single-bit data points taken, the total sample time, energy and pressure-resolution error.

Test Chamber Leakage At high test pressures, the test-chamber demonstrated observable pressure loss over the longest sample time. Figure 5.18 shows the mean-estimate as it varies over time during sampling for N = 1M samples at 770 mmHg. The middle plot shows consecutive mean-estimates formed with 10,000 single-bit data samples; the bottom plot shows the same data with a 9-point moving average filter applied. Readings from the reference pressure sensor were recorded at the start of sampling (stored in the file header), and again at the end of sampling (stored in the file footer). At the start of sampling, the chamber pressure was 770.5 mmHg; at the end of sampling, the pressure was 767.4 mmHg for a measured pressure loss of 3.1 mmHg over the approximate 10 minutes of sampling. Using the linear fit parameters shown in the bottom plot, and taking the initial recorded pressure of

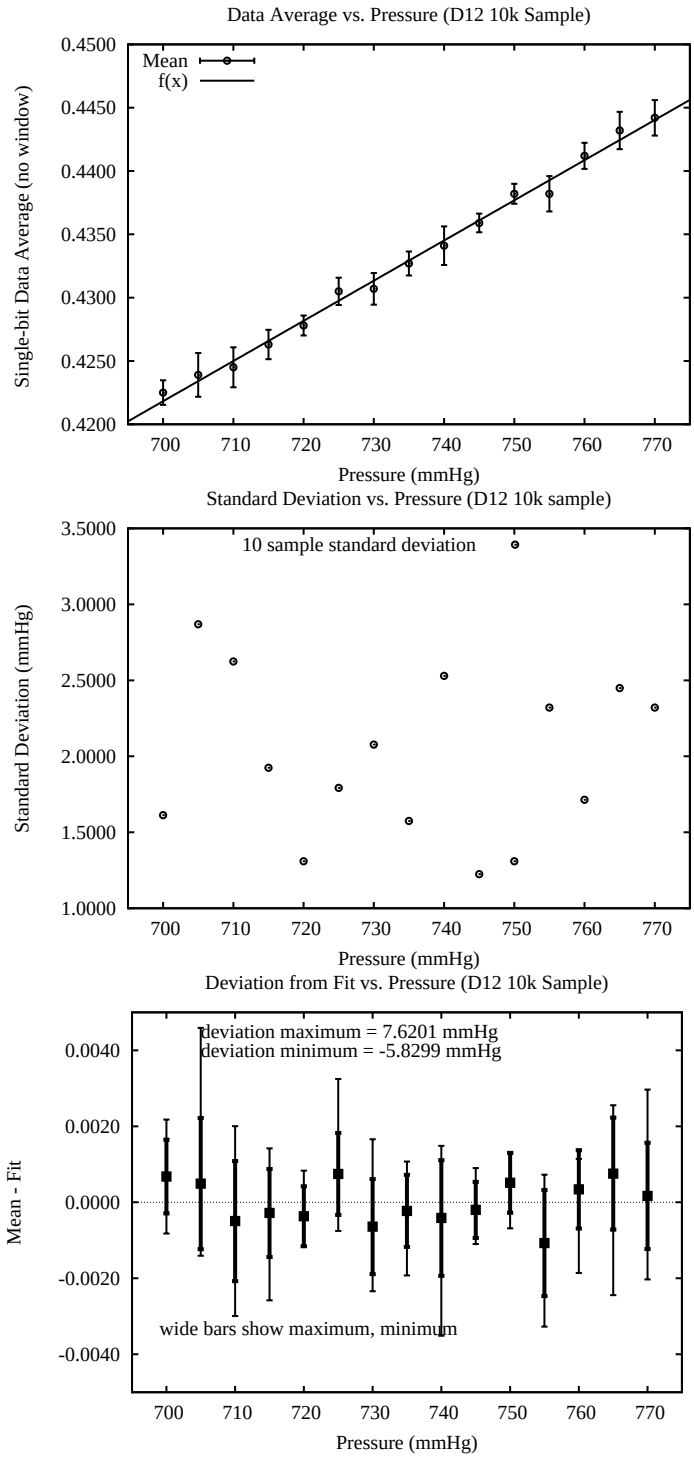

Figure 5.14: Experimental test results showing AS1-MEMS instrument response for a 10,000 single-bit samples. The plotted mean and standard deviation were formed from 10 samples. Each sample was comprised of a mean-value estimate of N=1,000 single-bit data. The standard deviation was fairly consistent over the range of pressure. The maximum deviation from the fit line was approximately 7.6 mmHg.

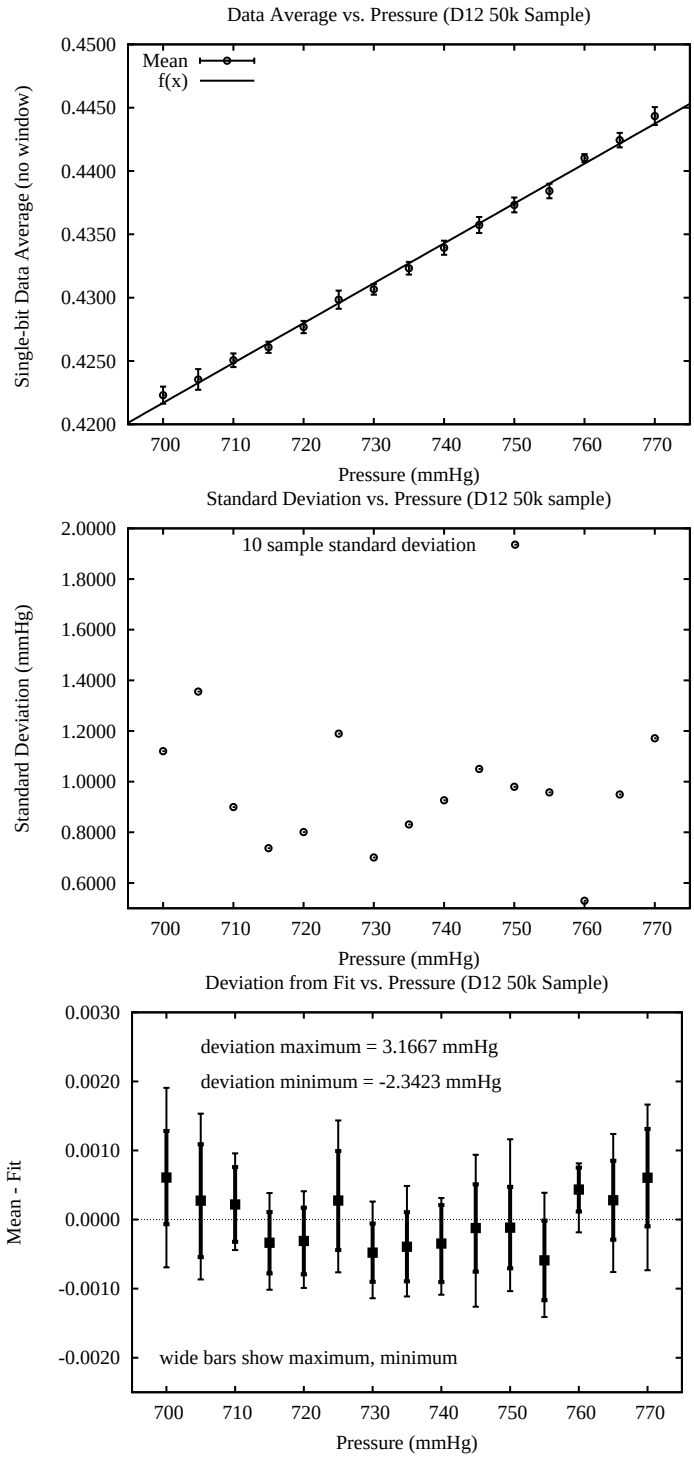

Figure 5.15: Experimental test results showing AS1-MEMS instrument response for 50,000 single-bit data points. The plotted mean and standard deviation were formed from 10 samples. Each sample was comprised of a mean-value estimate of N=5,000 single-bit data. The standard deviation was fairly consistent over the range of pressure. The maximum deviation from the fit line was approximately 3.2 mmHg.

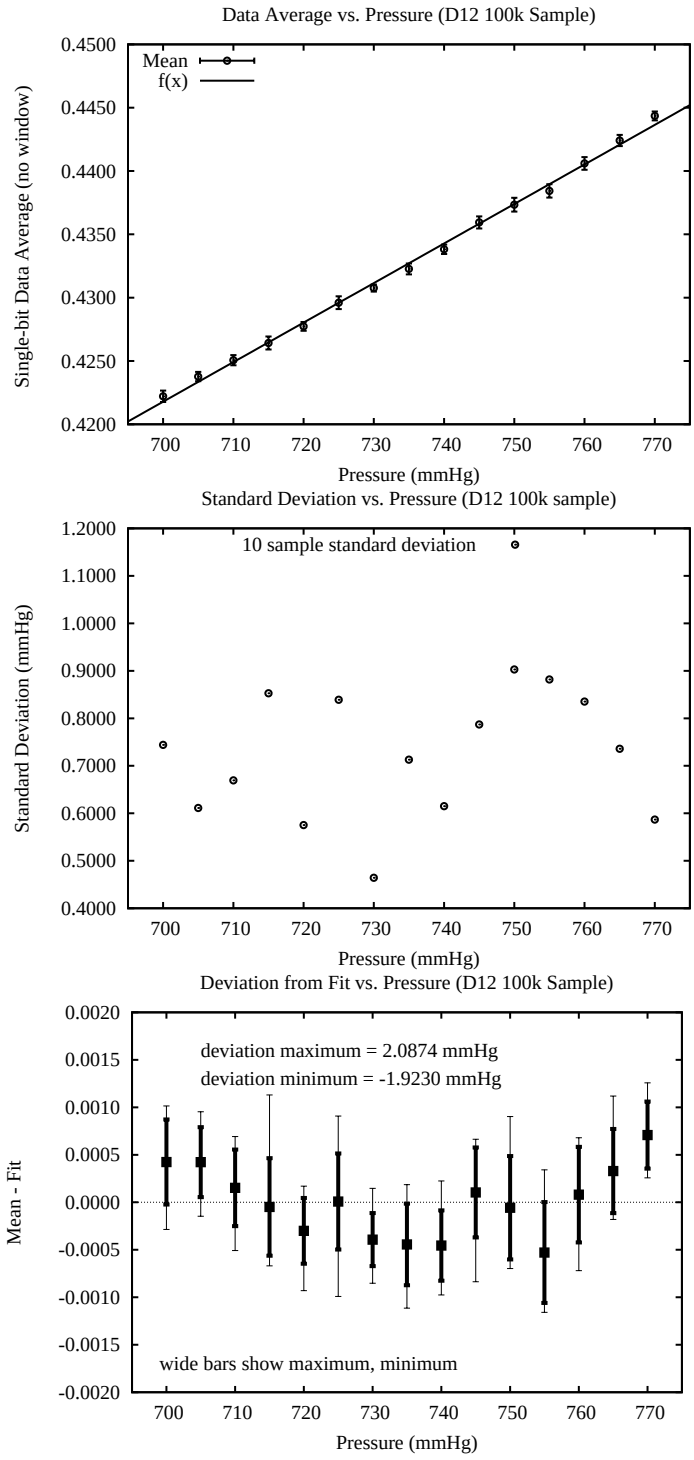

Figure 5.16: Experimental test results showing AS1-MEMS instrument response for 100,000 single-bit data points. The plotted mean and standard deviation were formed from 10 samples. Each sample was comprised of a mean-value estimate of N=10,000 single-bit data. The maximum deviation from the fit line was less than 2.1 mmHg.

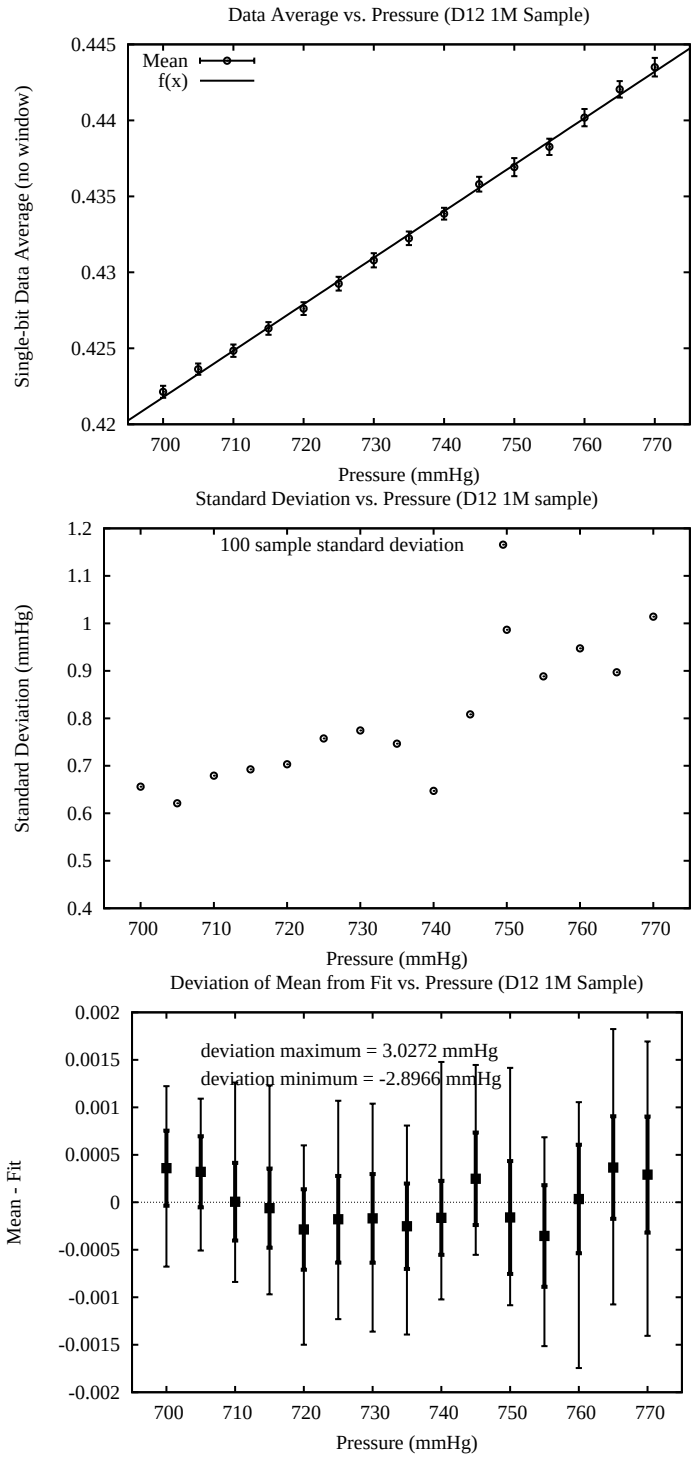

Figure 5.17: Experimental test results showing AS1-MEMS instrument response for 1,000,000 single-bit samples. The plotted mean and standard deviation were formed from 100 samples. Each sample was comprised of a mean-value estimate of N=10,000 single-bit data. At higher pressures, the standard deviation increased at high pressure due to tank leakage. The maximum deviation from the fit line was approximately 3.0 mmHg.

770.5 mmHg as the y-intercept (b=0.444284), the linear fit model $y = a * x + b$ predicts a final chamber pressure of 768. 1 mmHg, estimating a pressure loss of 2.4 mmHg.

The application of a 9-point moving average filter applied in the bottom plot of Fig. 5.18 revealed an unexpected low-frequency oscillation on the order of 6 mHz in the N = 1M data sample. Oscillations on this scale are present in all samples taken over the pressure test range pressures. Figure 5.19 shows results for the AS1-MEMS instrument response during chamber leakage at various pressures. The cause of the mHz oscillations is unknown. It may be caused by electronic noise or interference, from voltage or pressure-change induced oscillations on the MEMS membrane or from pressure variation due to room pressure fluctuations. The Pelican-case pressure chamber was not entirely rigid and may have been able to transmit external pressure changes into the chamber. During testing, the pressure chamber was located on a desk which was above a regular heating vent and was also adjacent to an external window, offering the possibility of convective drafts.

For the oscillations occurring at 770 mmHg, the peak-to-trough variation of the oscillation is on the order of 1.5 mmHg. While it was anticipated that variance in the mean-estimate could be decreased with increased sample lengths, oscillations of this scale present throughout the data prevent resolution improvement by averaging. The variance of a mean-estimate of a random variable regularly follows a χ^2 distribution, but the oscillation present in the data is deterministic and cannot be further reduced. The middle plot on Fig. 5.17 from 700–730 mmHg demonstrates the decreased variance in the standard deviation of the mean-estimate for 1 M sample length; at pressures below roughly 730 mmHg, the standard deviation is fairly consistently at

0.6 mmHg which is approximately 1/2 of the peak-trough variation of the observed oscillation.

The energy-scaled PSD of the modulator output at 770 mmHg is shown in Fig. 5.20. The data was zero-padded to increase the resolution to approximately 0.00012 Hz. A Blackman Harris window was used on the data prior to spectral analysis, to better distinguish adjacent tones in the spectrum. At the lower frequencies it is not possible to resolve any particularly strong tones within the noise of the FFT. The noise floor of the PSD is easily seen at -40 dB/$\sqrt{Hz}$. With a power supply voltage of V_{DD} = 325 mV, this relates to a capacitive input uncertainty of 15 fF/$\sqrt{Hz}$. With N = 1 M samples, the uncertainty due to the noise floor is 0.7 mmHg.

From observation of the trend in the mean-estimate as it tracks the test-chamber pressure leakage at 770 mmHg, it is expected that the instrument would be able to resolve pressure variation of less than 1 mmHg were the oscillation absent. Further research is required to resolve the cause of the oscillations.

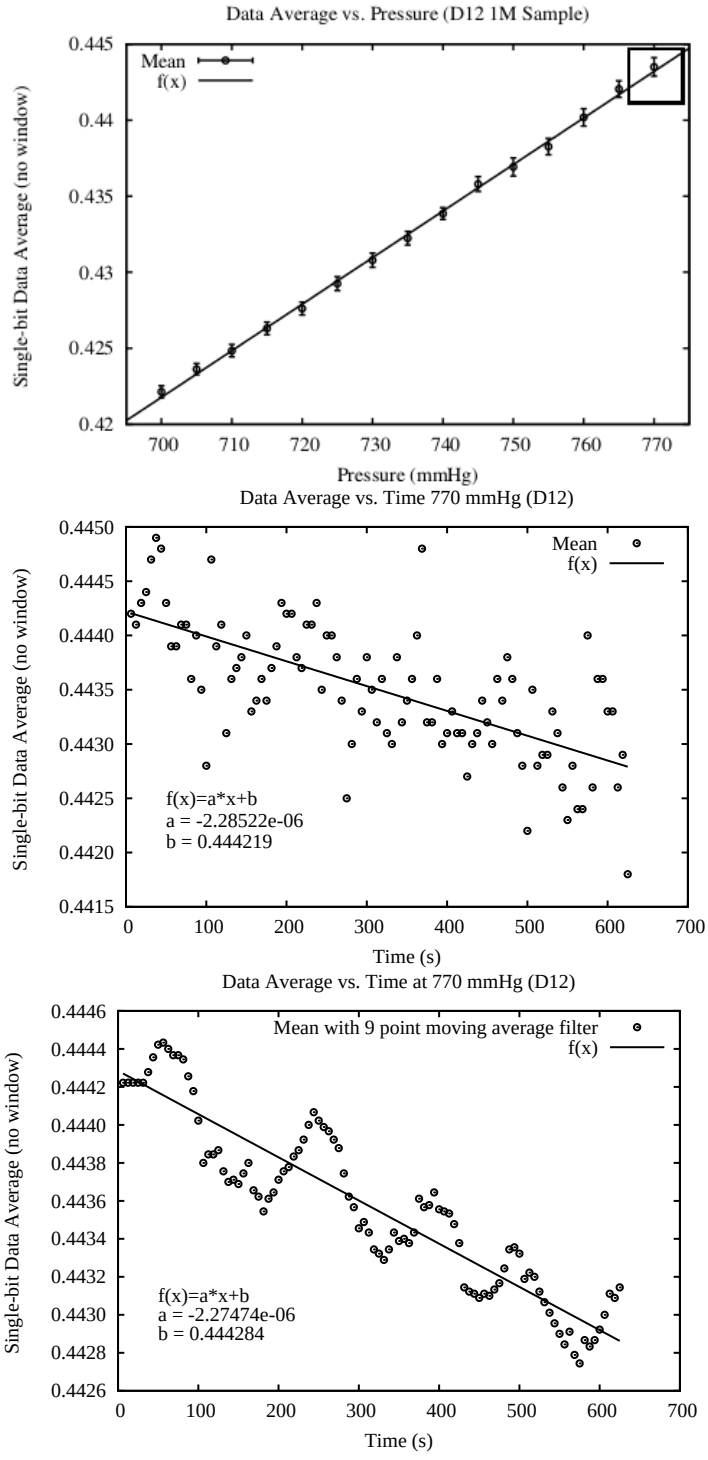

Figure 5.18: Experimental test results showing AS1-MEMS instrument response during chamber leakage at 770 mmHg. A total of 1,000,000 single-bit data points were obtained over the 10 minute sampling time interval. The middle plot shows mean-estimates formed with consecutive N=10,000 single-bit data points; in the lower plot, the same data is shown with a 9-point moving average filter.

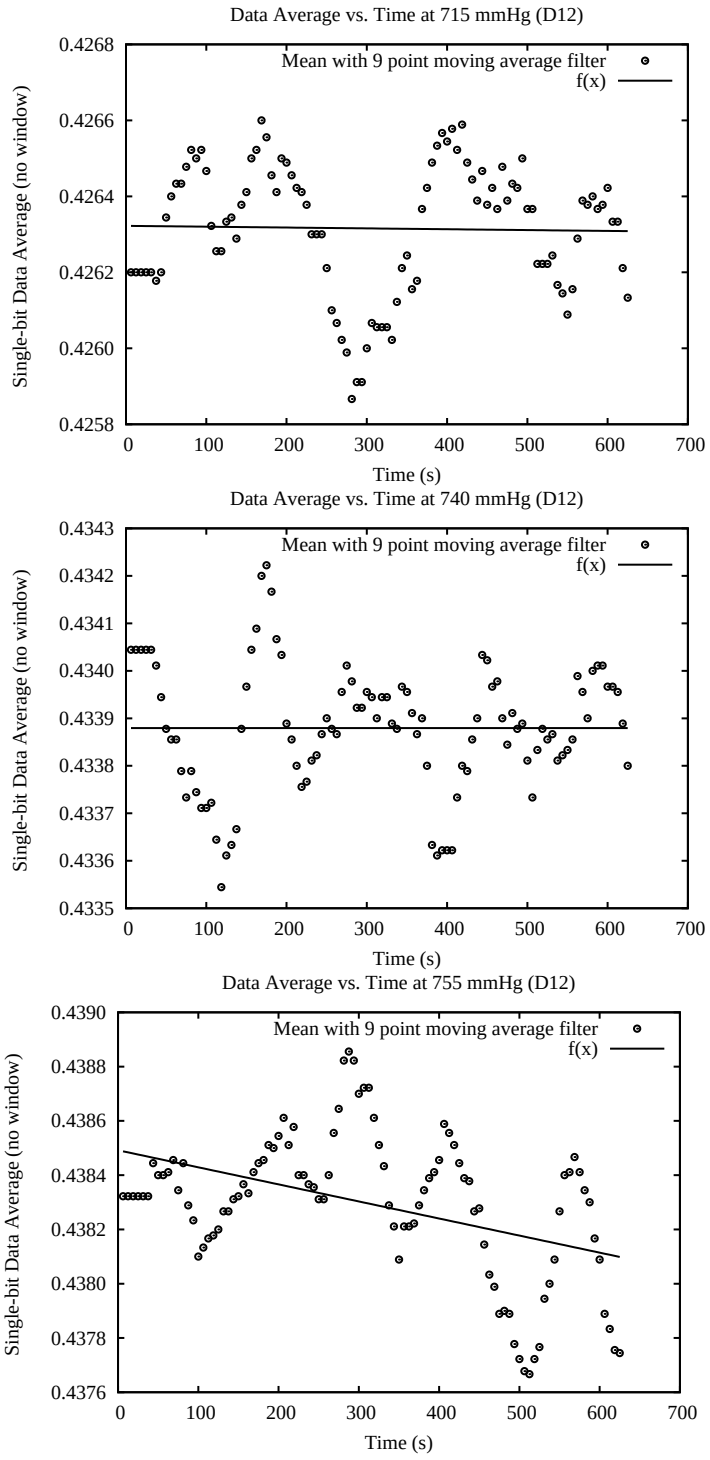

Figure 5.19: Experimental test results showing AS1-MEMS instrument response during chamber leakage at various pressures. Data is shown for mean-estimates formed with consecutive N=10,000 single-bit data point samples. A 9-point moving average filter was applied to all data. Oscillations on the scale of mHz were present in all data samples.

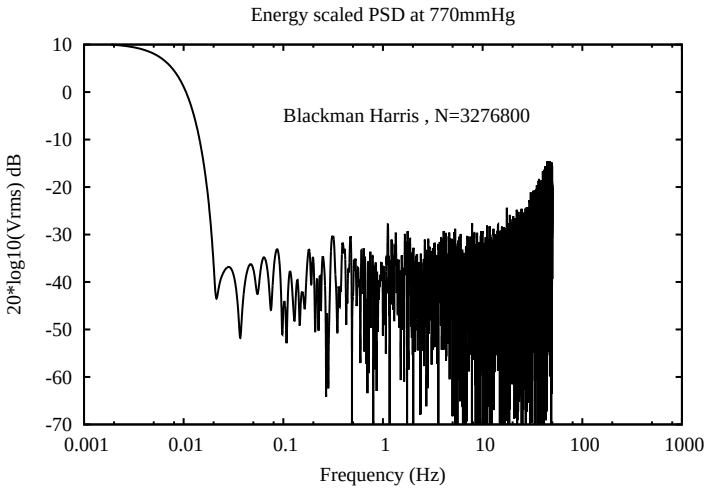

Figure 5.20: PSD of modulated output at 770 mmHg. The data had a Blackman Harris filter applied and was zero-padded to increase the spectral resolution to 0.00012 Hz.

5.3.3.1 Supply Voltage Variation

The AS1-MEMS was designed with a ratiometric comparison of pressure induced capacitance change, thus the circuitry was expected to tolerate changes in the power supply voltage. This section describes the testing of AS1-MEMS for rejection of power supply voltage variation.

Adjustment for V_{DD} was located on the board AS1TB1. To avoid disturbances due to mechanical jostling (see Section 5.3.3.2) that would have been caused by repeatedly opening the case to adjust V_{DD}, sensitivities to power-supply variation was tested with voltage input, rather than pressure input. The voltage input test was arranged as follows: $q_s = C_s(V_{ref} - V_{CM})$, the charge injected at the sampling capacitor, and $q_{C12} \approx (C_1 - C_2)(V_{refC1,2} - V_{CM})$, the charge injected at the differential capacitors, were contrived to remain constant while the supply voltage, V_{DD}, and common-mode voltage, $V_{CM} = V_{DD}/2$, were varied. To increase sensitivity during the test, the reference voltage V_{ref} was fixed at only 10 mV above V_{CM}. The voltage applied to the differential input $V_{refC1,C2}$ was varied from 10–50 mV above V_{CM}. By design, $q_{C1,C2} \ll q_s$, which ensured modulator stability throughout this testing. By holding the reference voltage V_{ref} at C_s low, the relative sensitivity to C_1 and C_2 is increased. The power supply V_{DD} was varied and $V_{CM} = V_{DD}/2$ at all times during the test.

The test circuit is shown in Fig. 5.21 together with expected MEMS parasitic resistances. The modulator input charge is differential. For the positive input path the modulator is non-inverting to C_1 and inverting to C_2. In the negative input path

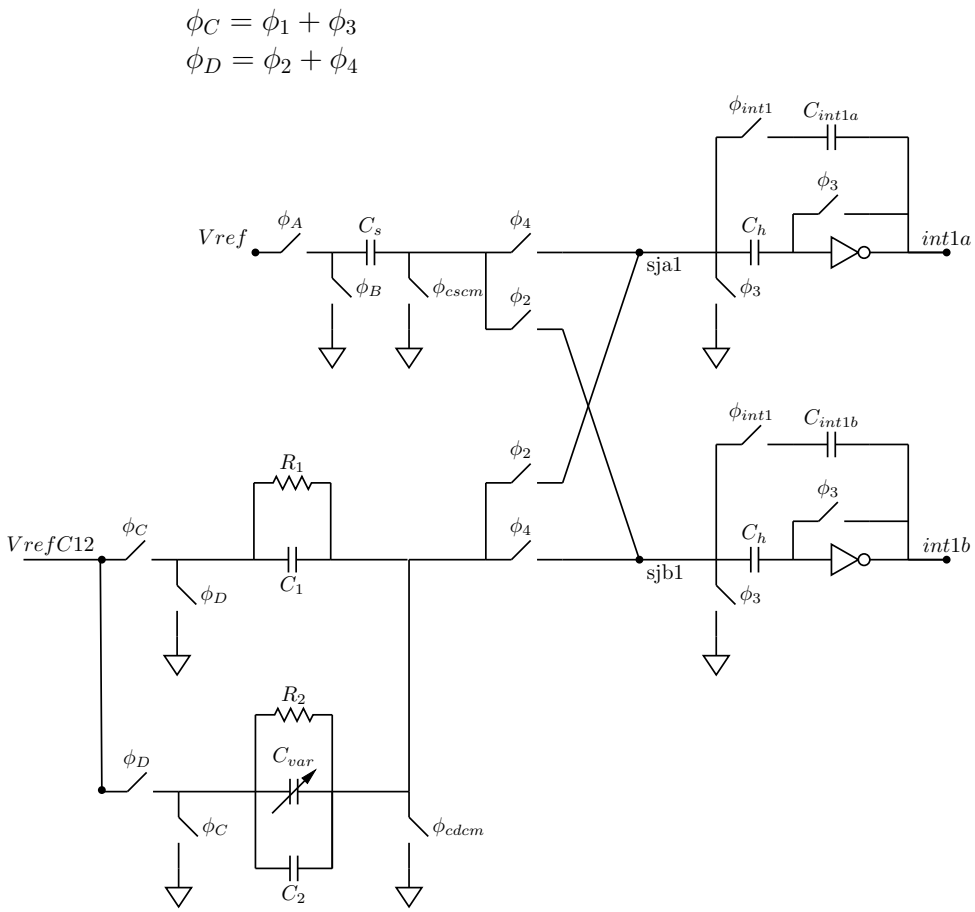

Figure 5.21: Diagram showing test setup for varying power-supply voltage, V_{DD}.

the modulator is inverting to C_1 and non-inverting to C_2. During the integration switch closure, the modulator also receives leakage charge from the input resistance of the MEMS parasitic resistance as follows,

$$\begin{aligned}\Delta Q_{pos} =&(V_{refC12} - V_{CM})C_1 + ((V_{refC1,2} - V_{CM})/R_1)\Delta t \\ &- ((V_{refC1,2} - V_{CM})(C_2 + C_{2var})) \\ \Delta Q_{neg} =&(V_{refC1,2} - V_{CM})(C_2 + C_{2var}) + ((V_{refC12} - V_{CM})/R_2)\Delta t \\ &- (V_{refC12} - V_{CM})C_1.\end{aligned}$$

Taking the differential signal, Q_{pos} - Q_{neg}, and allowing $(V_{refC12} - V_{CM}) = \Delta V_{test}$,

$$\Delta Q = \Delta V_{test}((2 \times C_1 - 2 \times C_2 - 2 \times C_{2var}) + \Delta V_{test}(1/R_1 - 1/R_2)\Delta t.$$

From this, if $C_1 \approx C_2$ and $R_1 \approx R_2$ the input charge should be entirely related to the variable capacitance C_{2var} and this differential charge contribution determines the varying modulator output response. Any response to poor matching, in the event that $R_1 \neq R_2$, for instance, contributes to the injected charge but appears at the output only as a scale-factor on the response slope to varying V_{refC12} provided it is independent of V_{DD}. If, for instance, C_1 and C_2 are voltage dependent, the injected capacitive sampled charge may vary in the positive and negative signal path depending on the voltage dependent capacitive mismatch. Likewise, subthreshold leakage current from the switches in the off-configuration at C_1 and C_2 may vary with responsiveness to varying V_{DD}.

Provided there are no circuit response proportionate to V_{DD}, the circuit is ratio-

metric to the capacitances and the varying voltage at inputs V_{ref} and V_{refC12}; the circuit should be relatively unresponsive to changes in power-supply voltage V_{DD}.

Figure 5.22 shows test results for the AS1-MEMS instrument to varying power-supply voltage V_{DD}. The single-bit data was used to form a mean-estimate. A linear response over the variation of voltage at V_{refC12} was as expected. Variation due to operation at differing power supply voltages V_{DD}, however, was unexpected. The modulator had a substantial response to changes in V_{DD}. The sensitivity to V_{DD}, over the tested range from 275 mV to 375 mV, varied the mean-estimate value by roughly 65%. Results of this testing contradict the relatively consistent performance for DC input versus power-supply voltage (shown previously in voltage input testing) and are not fully understood.

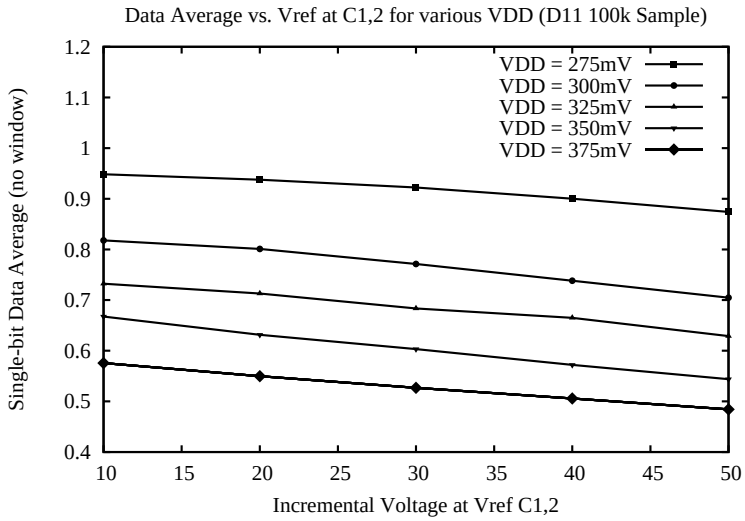

Figure 5.22: Experimental test results showing AS1-MEMS instrument response with varying V_{DD}. The mean-estimate versus varying reference voltage at $V_{refC1,2}$ is shown for various values of V_{DD}. Despite a ratiometric circuit design, the response shows responsiveness to varying V_{DD}. Varying V_{DD} from 275 mV to 375 mV produces an output variation of over 50%.

Using the data at $V_{DD} = 375$–350 mV and $V_{refC12} = 30$ mV, the estimated sensitivity in the output is calculated at 300 ppm/mV. It is possible that voltage-dependant parasitics at the MEMS sensors are influencing the circuit at varying V_{DD}, or that switch voltage dependent subthreshold leakage current is varying with V_{DD} which is used to drive the switches.

5.3.3.2 Other Results

The AS1-MEMS instrument was observed to be sensitive to mechanical jostling, exhibited a large day-to-day response variation and also demonstrated time varying response believed to be due to relaxation processes. These sensitivities may be related to the MEMS sensors, and in particular may be related to the effect of the epoxy covering on one MEMS sensor; it was not possible to separate the performance of the sensor and sealant from the performance of the circuitry.

Unit Variation there were a total of 4 units wire-bonded into AS1-MEMS prototype instruments. Units D10 and D12 provided the best response; other units had an output mean-estimate value closer to the extreme of 1 or 0 (eg. 0.7) and were less responsive to pressure changes. Unit D10 exhibited what appeared to be a relaxation process, possibly associated with the epoxy coating on the MEMS (discussed below). Unit D12 had an increased amount of epoxy applied, gave no indication of relaxation effects and provided the most consistent results during experimentation without relaxation tendencies impacting the data sampling.

Mechanical Jostling by, for instance, snapping closed the sealed Pelican case lid, produced an abrupt step change in the instrument average output. As shown in

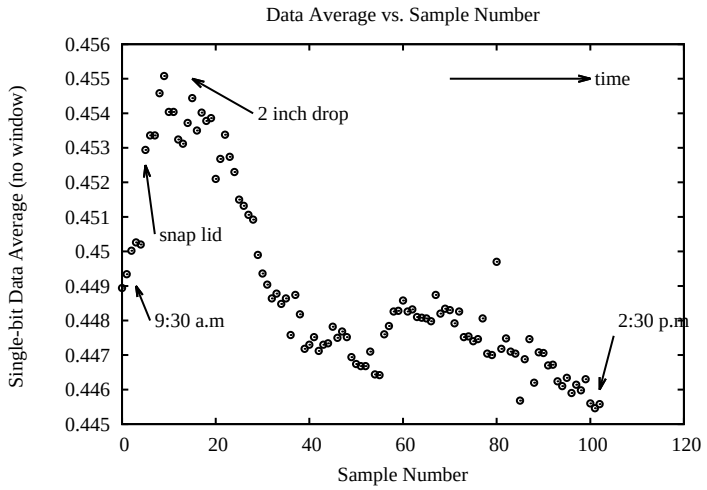

Figure 5.23: Experimental test results showing AS1-MEMS response to mechanical jostling (D10). The result shown includes both chamber snap-lid closure and chamber drop from a height of two inches. The chamber was vented to atmosphere continuously during the test. The time interval between sampling was roughly the same.The trend downward at the end of data sampling indicates that inadvertent jostling may have occurred prior to initial data sampling.

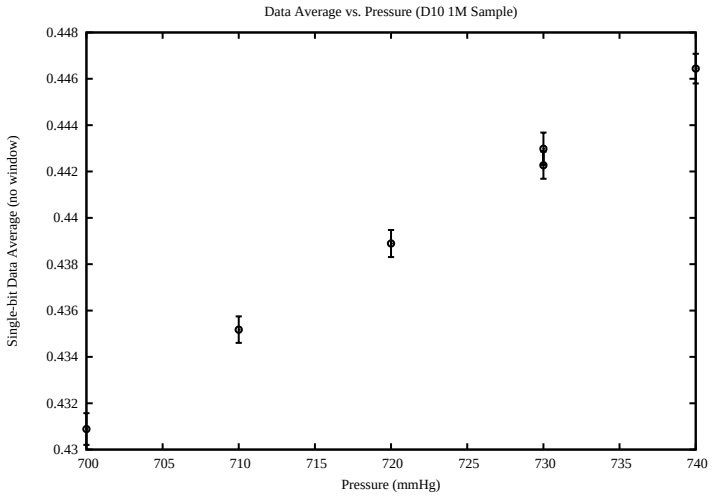

Figure 5.24: Experimental test results showing AS1-MEMS response to light jostling. The chamber was rapidly moved approximately three inches along a flat surface prior to a second reading at 730 mmHg. The chamber was not moved up or down. The higher output was obtained after jostling. The mean and standard deviation are shown for 100 samples of N=10,000 data point mean-estimate.

Fig. 5.23 for D10, the effect from closing the Pelican case lid required several hours to settle. In addition, the measurement was also sensitivity to very slight mechanical jostling as shown in Fig. 5.24. During testing, this sensitivity was taken in account and the chamber was closed well in advance of sampling and significant care was taken not to disturb the chamber during the duration of each test over the range of pressures.

Day to Day Variation was observed on all units. Figure 5.25 response of D12 on two different days. The chamber temperature and operating conditions were consistent between the two days. Temperature variations were not considerable, temperature varied from 25 – 27 ^{o}C over the entire testing period. Temperature variation over a single sample was negligible; temperature variation over a sweep from 700 mmHg to 770 mmHg varied by only approximately 0.2 ^{o}C. Humidity variation was not recorded.

Relaxation Processes were observed on the AS1-MEMS instrument. The AS1 circuitry relies on differential capacitance to produce a response. If the applied pressure is impacting both sensors in an identical fashion, no variation in the differential signal results. The MEMS sensor with epoxy applied was suspected of slowly responding to applied pressure, diminishing the differential signal over time. Figure 5.26 shows the response of D10 versus pressure over time. At higher applied pressures, the differential signal is diminished over time. Relaxation was most

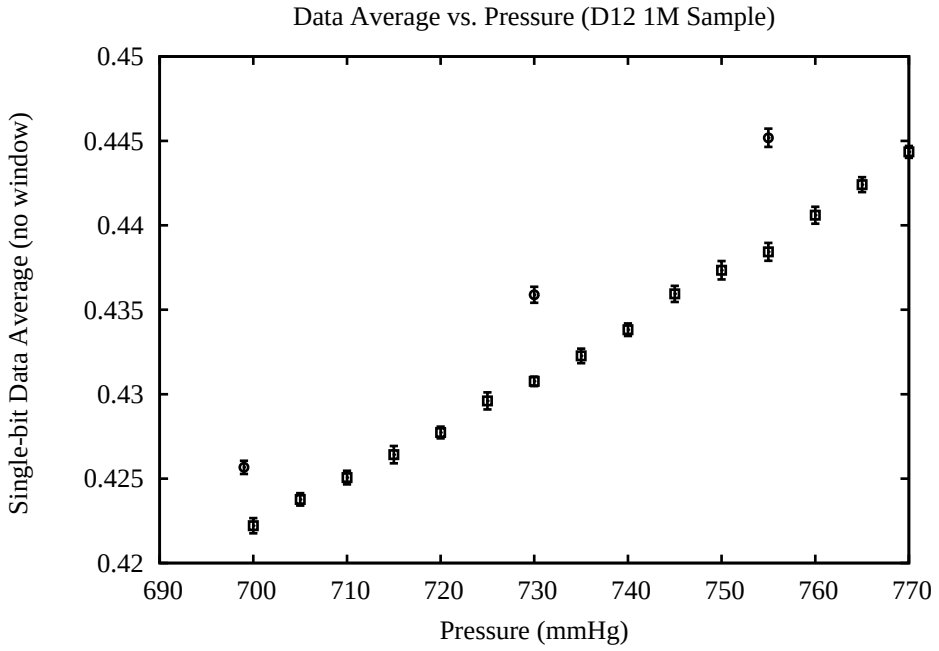

Figure 5.25: Experimental test results showing the mean-estimate versus pressure taken on two different days (D12). The chamber temperature and AS1 operating voltage conditions were consistent between the days. Mean and standard deviation is shown for 100 samples of a N=100,000 data point mean-estimate. The upper data points correspond to sampling a day later than the lower values.

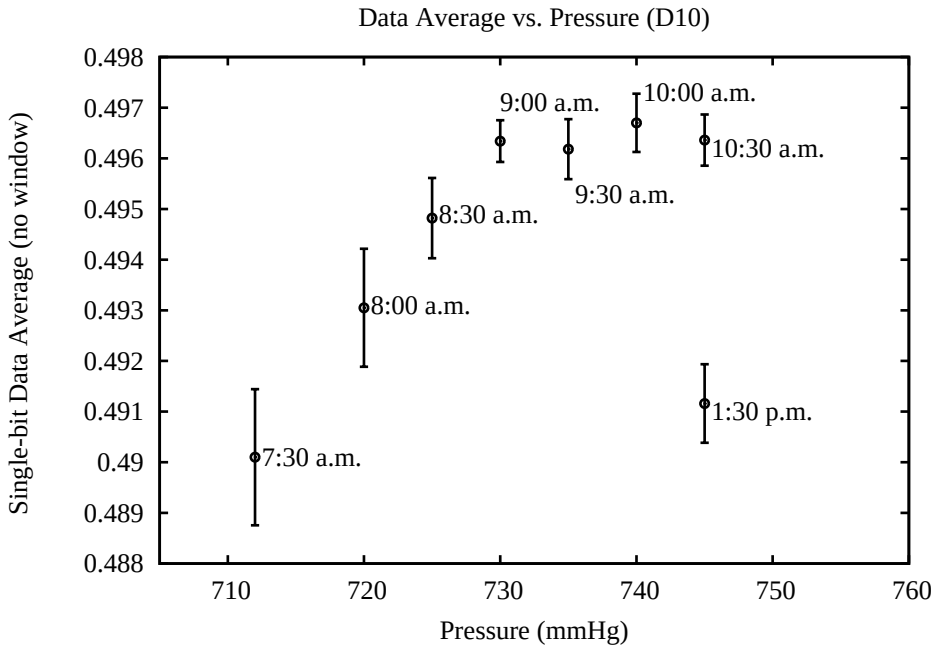

Figure 5.26: Experimental test results showing data average versus applied pressure over time for D10. Results indicate a diminishing differential signal over time. Mean and standard deviation is shown for 10 samples of a N=5,000 data mean-estimate.

strongly observed on D10 and was not observed on D12. Later builds of AS1-MEMS used larger amounts of the epoxy on the MEMS sensor. A larger amount of epoxy was expected to offer increased resistance to deformation under pressure. Device D12 exhibited no observable pressure relaxation.

5.3.4 Summary

The AS1-MEMS prototype instrument was formed by wire-bonding the AS1 die with two E1.3N MEMS capacitive sensors. The AS1-MEMS instrument was tested over a pressure range from 700–770 mmHg. The AS1-MEMS was also tested for response to varying power-supply voltage.

Calculation of a mean-estimate versus input pressure showed that the instrument was capable of resolving mmHg-scale pressure changes while operating at 325 mV with 30 nW (D12). Tests for D12 with various single-bit data lengths varying from 10k to 100k resulted in pressure resolutions of 7.6–2.1 mmHg over the pressure range 700–770 mmHg; the associated energy of sampling varied from 0.18 μJ to 18.8 μJ. In general, instrument resolution improved with increasing sample lengths. At sample lengths requiring approximately 10 minutes, however, there was increased variation in the mean-estimate due to pressure leakage in the test-chamber over the tested pressure range.

On closer inspection of the time-series data over the leakage at 770 mmHg, very low frequency oscillations became apparent. The cause of the oscillations is not understood, but the magnitude of the oscillation is determined to be the limiting factor in resolution improvement over longer samples. From the trend estimation during pressure leakage at 770 mmHg, it is expected that the instrument would be able to resolve pressure variation of less than 1 mmHg were the oscillation absent.

The AS1-MEMS instrument was observed to have a strong response to mechanical jostling and to have what appear to be relaxation processes, in addition to day-to-day variations. These issues are believed to be associated with the MEMS and epoxy sealant.

5.4 Discussion

The modulator was tested in both voltage-mode and pressure-mode. This section compares the test results with other work and with simulation.

Comparison With Other ADC Table 5.4 shows this work compared to other low-power, low-frequency data converters (tabulated reports shown on page 24 are reproduced here here with the inclusion of this work for comparison).

Report	[104]	[82]	[85]	[99]	[86]	[100]	**This work**
Year	2003	2006	2008	2009	2009	2012	
Technology [μm]	0.18	0.8	0.5	0.35	0.35	0.13	0.13
Voltage [V]	0.5	2.5	1.2	1	1.5	1 & 0.4	**0.25**–0.6
Power [μW]	0.85	3	0.140	0.23	0.73	0.053	**0.017**–0.052
Architecture	SAR	SAR	$\Sigma\Delta$	SAR	$\Sigma\Delta$	SAR	$\Sigma\Delta$
Data Rate kS/s	4.1	0.8	0.05	1	0.24	1	
Signal BW [Hz]	2000	400	25	500	120	500	25
SNDR [dB]	43.3	56	61	63	65	56	8.1-25
FOM [pJ/step]	1.8	7.2	2.7	0.2	2.1	0.095	66-178

Table 5.4: This work shown with other low-power, low-frequency analog to digital converters for comparison. This work shows substantially reduced operating voltage and power, but also much lower levels of performance.

While this work shows substantial reductions in low-voltage operation, the FOM is not comparable to other work low-voltage, low-power analog to digital conversion. The modulator for this work was designed with an inverter amplifier operating in deep subthreshold. While other work [86] suggests operation of the inverter amplifier at the onset of weak-inversion, where the gain has achieved a maximum value and the GBW is minimally decreased, this work had the opportunity

to have very low-frequency operation and had the requirement for very low-voltage, low-power operation. The dominant power loss within the modulator was with the digital logic control block, which, other than ensuring the correct signal timing, has little performance impact on the signal path. A substantial amount of power in the modulator design is for supporting circuitry rather than in the signal path; the SC signal path only comprised roughly 13% of the total power. Decisions such as the implementation of the digital logic control block in regular threshold CMOS adversely impacted the power consumption and the FOM performance, but are relatively simple to improve upon afterward and allowed testing of SC signal path core with reduced risk of impediment from digital logic relative timing failures.

Capacitance Sensing Operating with 30 nW at 325 mV, the modulator resolved pressure to roughly 2.1 mmHg over the tested range from 700–770 mmHg. The MicroFab particular E1.3N sensor used has a sensitivity of 0.6 fF/mmHg in this pressure range[3]. Thus the modulator performance using 100k single-bit samples corresponds to a capacitive sensitivity of 1.25 fF.

Power Consumption During voltage input testing, the power consumption for the operating conditions V_{DD} = V_{DDCOMP} = 500 mV and f_s = 3200 Hz, was found to be 53 nW (D4), 56 nW (D5) and 105 nW (D7). Power consumption was strongly dependent on the technology process corners and for the same operating conditions simulated power consumption varied from 41–298 nW. Fig. 5.27 shows the measured power consumption of D4 (both V_{DD} and V_{DDCOMP}) versus simulation results over

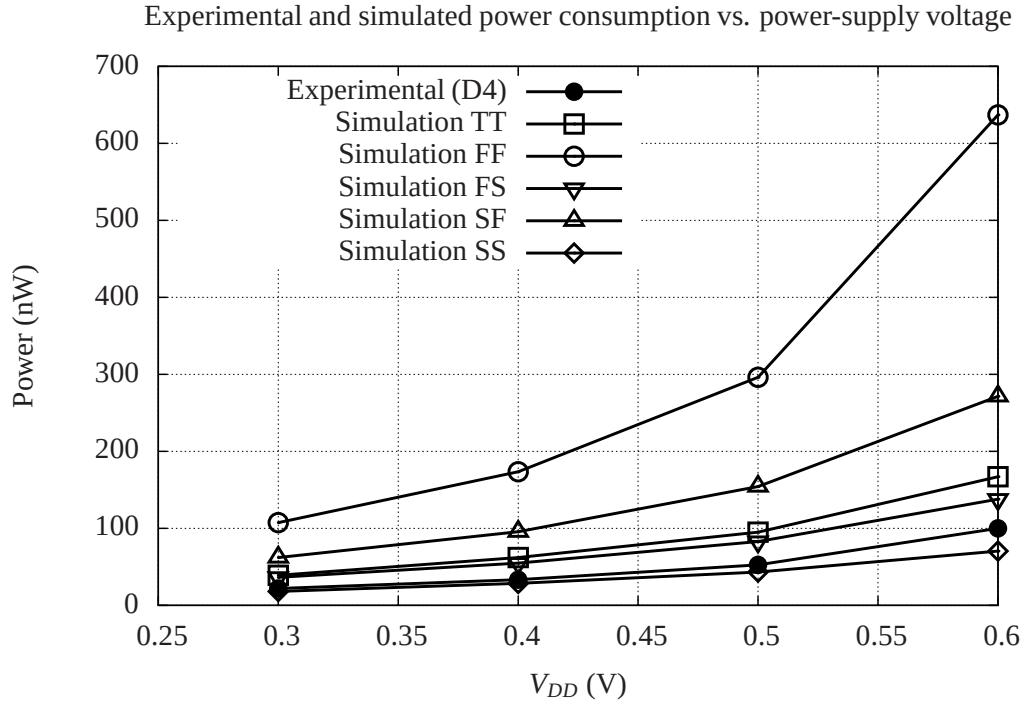

Figure 5.27: Experimental results of power consumption measurement (D4) versus simulation over V_{DD} and process.

process for varying values of V_{DD}.

Comparison with Other IOP Work The performance of AS1-MEMS is compared with other published works for IOP measurement in Table 5.5 below (tabulated data from page 10 is reproduced and the results of this work using sample sizes of 10k and 100k is added for comparison). The 1-2 mm ⌀ size estimate of this work includes AS1 core-circuitry and an estimated area for an integrated coil antenna.

[3]MicroFAB, Bremen has recently produced higher sensitivity MEMS capacitive sensor dies, with sensitivities up to 1.6 fF/mmHg.

Work	Supply (V)	Power (μW)	Time (s)	Energy	Resolution (mmHg)	Instrument Size
[24]	3.00	210	n/a	n/a	0.7	$\varnothing$10.5 mm
[13, 25]	1.50	160	0.001	0.16 μJ	0.5	$\varnothing$16 mm
[14]	3.60	7	10	70 μJ	0.5	$\approx$ 1 mm^3
[15]	1.50	1.74	n/a	n/a μJ	0.9	$\varnothing$ 10 mm
this work:						
100k sample	0.325	0.03	62.5	1.88 μJ	2.1	$\varnothing$ 1–2 mm
10k sample	0.325	0.03	6.2	0.18 μJ	$\leq$ 7.6	$\varnothing$ 1–2 mm

Table 5.5: Tabulated summary of reported IOP measurement systems sensing circuitry. Power reported in [24] is for full system rather than sensing circuitry alone. The 1-2 mm $\varnothing$ size estimate of this work considered the core circuitry and an integrated coil antenna.

The power numbers shown in Table 5.5 are as close as possible to an "apples to apples" comparison; except for [24] which did not report individual block power, the power consumption numbers listed are based on sensing circuitry alone and do not include power required in ancillary circuits, such as voltage regulation. In [13, 25], for instance, power regulation required 40 μW and the capacitive sensing circuitry required 160 μW. In [15], the sensing circuitry consisted of an oscillator requiring 1.74 μW; the total on-chip power was 2.3 μW including a low-power bandgap-reference and regulator circuit. In this work, power consumption is for comparable sensing circuitry alone. Power consumption in this work includes the complete modulator core (including the logic control, buffers, SC signal path and comparator). Not included in this work is the power required to establish the four-phase non-overlapping clocks, and the output level-shifting buffer required for board level testing.

The CDC reported in this work demonstrates a high sensitivity with record

low-voltage and power operation. Compared to other work in IOP measurement instrumentation where $\Delta\Sigma$ modulation was applied to capacitive sensor with a resolution of 26 fF/mmHg [14, 126], this work obtains a 20$\times$ improvement in capacitive-sensitivity at substantially reduced operating voltage and power. In [14, 126] a resolution of 0.5 mmHg is obtained by averaging 50 sets of mean-estimate data where each mean-estimate is a count of the number of cycles where the single-bit value is high over 10k clock cycles. With the CDC clock operating at 50 kHz, 10 seconds is required to collect 500k single-bit data samples. With the power consumption of the CDC at 7 μW, the energy-per-measurement is 70 μJ when resolving 0.5 mmHg and the associated capacitive resolution of 13 fF. Using the observed $1/\sqrt{N}$ character of the CDC reported in this work, the expected resolution at 500k data sample length is 7.6 mmHg/$\sqrt{50}$=1.1 mmHg and 0.66 fF. Operating at $f_s = 1600$ Hz, a 500k data sample requires 312 seconds and the energy-per-measurement is 9.4 μJ. Conversely, the use of a 26 fF/mmHg with the circuitry reported in this work would permit the reduction of the sample length and time to 1.25k data samples and 0.78 seconds, providing an energy-per-measurement of only 0.024 μJ at a pressure resolution of 0.5 mmHg.

Of the reported IOP measurement instrumentation to date, this work achieves the lowest operating voltage and power. Within work supportive of a millimeter-scale implant, this work offers a potential for a tenfold improvement in the energy required per sample.

CHAPTER 6

CONCLUSIONS

This chapter concludes the thesis, summarising the major contributions of the work and presenting suggestions for future work.

6.1 Contributions

The key challenge in obtaining a suitably small IOP measurement instrument is the operating voltage and power; using wireless power transfer, the operating voltage and power requirements directly determine the implant size and wireless-power biocompatability. This work demonstrates a significant improvement in the state of the art for capacitive pressure sensing in the biomedical range. Compared to prior IOP instrument reports, the designed prototype instrument obtained a $4.5\times$ reduction in operating voltage and a $75\times$ reduction in operating power.

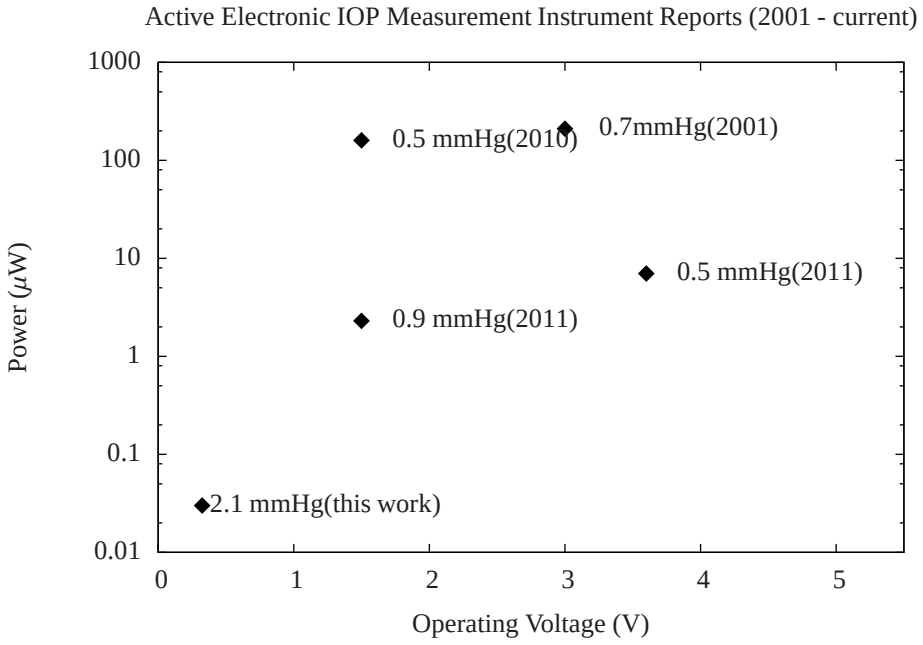

Figure 6.1: Active electronic IOP measurement instrument reports showing operating voltage and power from 2001 to present. Pressure resolution and year of publication is shown with each data point.

Figure 6.1 shows the operating voltage, power and pressure-resolution of active electronic IOP measurement instrument reports, including this work. The instrument was tested over the pressure range of 700–770 mmHg with an integral non-linearity of 2.1 mmHg. Increased sample lengths were anticipated to allow increased resolution, but at samples lengths of N = 1 M, low-frequency oscillations became apparent; without the oscillation, it is expected that the instrument reported in this work would provide a resolution better than 1 mmHg. The ultra-low 0.325 V, 30 nW operating voltage and power obtained in this work creates an opportunity for a monolithic IOP measurement instrument in integrated-circuit technologies and suitable for use with RFID-style wireless-power transfer to a millimeter-scale IC coil.

Work	Supply (V)	Power (μW)	Time (s)	Energy	Resolution (mmHg)	Instrument Size
(2001) [24]	3.00	210	n/a	n/a		$\varnothing$10.5 mm
(2010) [13, 25]	1.50	160	0.001	0.16 μJ	0.5	$\varnothing$16 mm
(2011) [14]	3.60	7	10	70 μJ	0.5	$\approx$ 1 mm^3
(2011) [15]	1.50	1.74	n/a	n/a μJ	0.9	$\varnothing$10 mm
this work						
100k	0.325	0.03	62.5	1.88 μJ	2.1	$\varnothing$1–2 mm
10k	0.325	0.03	6.2	0.18 μJ	$\leq$ 7.6	$\varnothing$1–2 mm

IOP measurement instrument reports shown in Fig. 6.1 are tabulated above showing the total energy per sample. Among reports capable of millimeter-scale implementation, this work achieves the lowest energy per sample. Not shown in the tabulation is the implementation technique used for power transfer and other details of the implementation. In reports [13, 15, 25] wireless-power transfer at frequencies above 600 MHz was used, despite well verified eye-health research which indicates the development of hot-spots in the eye above this frequency [42–44]. In [14] wireless-power transfer was avoided, but solar-charging circuitry and a battery was used, necessitating eventual battery replacement and risking leakage of battery constituents into the eye. Regarding pressure resolution, prior reported instruments have achieved quite high resolution whereas key features to monitor for eye health primarily include diurnal pressure variation and average-pressure variation over several days, both of which are risk factors for disease [16–18]. A resolution of

2 mmHg is deemed to be acceptable for IOP monitoring; resolutions higher than this are not necessarily required for disease research or monitoring for drug effectiveness or compliance [45].

Converter Performance While the modulator developed in this work showed poor performance when considered to other data converter reports using the ADC figure of merit[1], to the best of the authors knowledge it also obtained the lowest power of any reported modulator or ADC.

Techniques employed in the modulator design present a fruitful approach to further work in biomedical instrumentation. Design decisions in this work favored low-power operation over low-noise operation. The inverter amplifiers at the first integrator accounted for only roughly 12% of the total modulator power, but were responsible for a full 80% of the sampled noise[2]. Significant oversampling in this work allows much of the circuit noise to be filtered out of the mean-estimate.

With a need to keep circuitry simple for low-voltage operation and with strong variability under process and power supply voltage, this work was subject to wide performance variation. Due to a lack of clear bias current control on the inverter amplifiers, there was limited design flexibility to mitigate this variability. In this work, the operation of the inverter amplifier was directed by the power supply, process and the gate-voltage nominal-value at mid-rail. Recent work on near-V_T inverter amplifier biasing and feed-forward modulation architectures[3] reported a 250

[1]The ADC FOM = $\mathrm{Power}/(2 \times \mathrm{BW} \times 2^{ENOB})$

[2]Circuit noise is discussed on page 78 and operating power on page 104. The 12% portion of power represents 12 nW out of 95 nW total.

[3]Feed-forward $\Sigma\Delta$ architectures feed signal content forward, combating the accumulation at integrator outputs. These are effective in reducing integrator output swing for low-voltage modulator implementation and also reduce associated distortion.

mV, 7.5 μW, 61 dB SNDR modulator [41], a significant milestone in the field of data conversion. The near-V_{th} bias allows for more consistent operation over process and the feed-forward technique offers a reduction in circuit distortion with low-voltage operation. These techniques should be investigated for their applicability to the the ultra low-power region of deep subthreshold operation and for possible improvements in the capacitive-sensing loop architecture.

While the field of analog-to-digital conversion is mature, the vast majority of research has been concentrated on techniques for either high-speed conversion (for telecommunications applications), or high-accuracy conversion (for instrumentation applications). Significantly less research has been completed on low-speed, low-to-moderate accuracy ultra-low-power data conversion [81, 100]–an area with broad applicability to biomedical instrumentation. Low-speed, low-accuracy conversion represents the bottom of the data conversion range; this work sought to explore the bottom for low-voltage, low-power operation and application to IOP measurement instrumentation.

6.2 Future Work

This section describes future work relating to both the pressure sensing instrument, AS1-MEMS, and in the context of the large system, where the instrument may operate with RFID-style wireless-power transfer.

6.2.1 Pressure Sensing Instrument

The pressure sensing prototype instrument AS1-MEMS achieved record low-voltage, low-power operation for capacitive sensing and application to IOP measurement. Future work includes addressing the observed sensitivity to V_{DD}, on-chip clock generation, further power reduction and addressing general instrument concerns such as absolute accuracy, drift and temperature sensitivity.

Voltage Sensitivity Although the AS1-MEMS was designed for ratiometric comparison of pressure-induced capacitance change and the circuitry was expected to tolerate changes in the power supply voltage, experimental testing showed that the instrument output was sensitive to the power supply voltage and demonstrated a 300 ppm/mV response.

This result contradicts the relatively consistent performance for DC input versus power-supply voltage obtained in voltage input testing and is not fully understood. It is possible that voltage-dependant parasitics at the MEMS sensors are influencing the circuit at varying V_{DD}, or that drive-dependent subthreshold leakage current at the switches may be varying with changing V_{DD}. The switch driving voltage (gate, source and drain voltages) are variable with V_{DD}. This will need to be investigated in more detail for various causes and supply regulation may be required in future designs.

On-chip Clock Generation Options for the design of a system clock include either a voltage controlled oscillator, or division of the AC coil input voltage. Obtaining the clock using a voltage controlled oscillator offers the possibility to apply voltage-regulation feedback through the wireless-power communication link.

Future Power Reduction In this work, the modulator SC input path was designed to consume ultra low-power by operating the inverter amplifiers in deep subthreshold and the majority of the modulator power was consumed at the digital blocks. The digital blocks were designed with regular threshold transistors. Regular threshold transistors, compared to low-power transistors, provided predictable low-voltage relative timing performance over process variation. Consistent and controlled relative timing is important in the $\Sigma\Delta$ modulator to avoid imbalancing sampled or integrated charge in the SC signal path.

As the supply-voltage is decreased, digital circuits operating in subthreshold are increasingly sensitive to process variation. Robust ultra-low voltage digital circuit design is an area of active research [115–122], including increased robustness to process variation [117, 123]. In general, the adverse impact of power reduction strategies for subthreshold logic CMOS increase the delay. The low-frequency operation of the $\Sigma\Delta$ modulator-based IOP instrument make it suitable to these strategies, provided that critical relative delay timing is preserved.

General Instrument Concerns General concerns for any instrumentation include temperature sensitivity, drift and absolute accuracy.

Temperature sensitivity Recent work in IOP measurement instrumentation has estimated that at an ocular implant depth of 4 mm a temperature range of 30.6–37.3^{o}C can be expected from an ambient exposure from 0–35^{o}C [15]. The capacitive pressure sensor E1.3N used in this work has a temperature sensitivity of 0.6 fF/^{o}C. It is expected that temperature variation in the CMOS circuits designed in this work would produce common-mode response in the circuit which would be reduced to

a second-order effect in the pseudo-differential circuitry. Future work should have full temperature sensitivity assessment, including any MEMS used.

Drift Drift of the instrument response over time is of high concern in any implanted instrument. In this work, the correlated double sampling reduce the sensitivity to CMOS transistor parameter drift, such as slow variation of transistor offset over time, but other aspects of the instrument, particularly the MEMS capacitive sensors and biocompatable sealant may be prone to drift over time.

The best solution for operating precision is automatic in-place calibration through an auxiliary dummy capacitor-pair. Similar to the calibration scheme proposed in [70], but using additional capacitors rather than ommitting capacitors, the calibration cycle could use a dummy capacitor-pair forming a difference capacitor ΔC_{cal}. Calibration will occur at start up with ΔC_{cal} switched in for a fixed number of clock cycles. The variation in mean-estimate data with ΔC_{cal} in place represents changes in the SC signal path with variations in operating conditions; if the dummy-capacitors are constructed in the same technology as the operational capacitors, then voltage dependent parastic changes may also be removed by calibration. In-place calibration in this manner represents a digitally-assisted design technique that preserves the advantage of minimalist ultra-low voltage operation.

Absolute Accuracy Absolute accuracy must be established for the instrument through a calibration with a standard IOP measurement instrument in a known pressure environment. Future work should consider appropriate means to establish absolute accuracy in a fluid environment with the instrument encased in a biocompatable coating.

6.2.2 In Context of the Large System

The pressure sensing $\Sigma\Delta$ modulator developed in this work was intended as a contributing piece of a larger-group research project. The pressure sensing circuitry was envisioned for use with a CMOS integrated circuit inductor coil using RFID-style wireless-power transfer. In RFID-style wireless power transfer, voltage multiplying rectifiers are commonly used to boost coil voltages to levels suitable for circuitry.

Figure 6.2 shows the modulator together with an inductive coil and a two-stage voltage multiplying rectifier. The rectifier provides the modulator power supply voltage V_{DD}, as well as the analog ground mid-rail voltage, V_{CM}, to the modulator. The single-bit output bit-stream, Y, is shown directed toward the inductor for the purpose of load modulation and communication back to the reader. An expanded view of the designed modulator circuitry is shown. Within the context of the larger system, $\Sigma\Delta$ modulation offers an advantage in that it generates an output data bit-stream that requires no header information. By bringing the bit-stream out directly, the digital filtering is implemented at the external receiver, effectively shifting power requirements away from the implant.

Voltage multiplying rectifiers for RFID wireless-power transfer have been reported with as little as 200 mV induced coil voltage using low-threshold CMOS transistors [15, 127, 128]. As discussed in Appendix F, multiplying rectifiers implemented with low-threshold transistors are subject to relatively large reverse-biased diode currents and are most efficiently operated with a minimal voltage increment per stage. The optimal voltage increment, ensuring the most efficient operation of the rectifier, depends on the power consumption of the load circuitry [129]. The

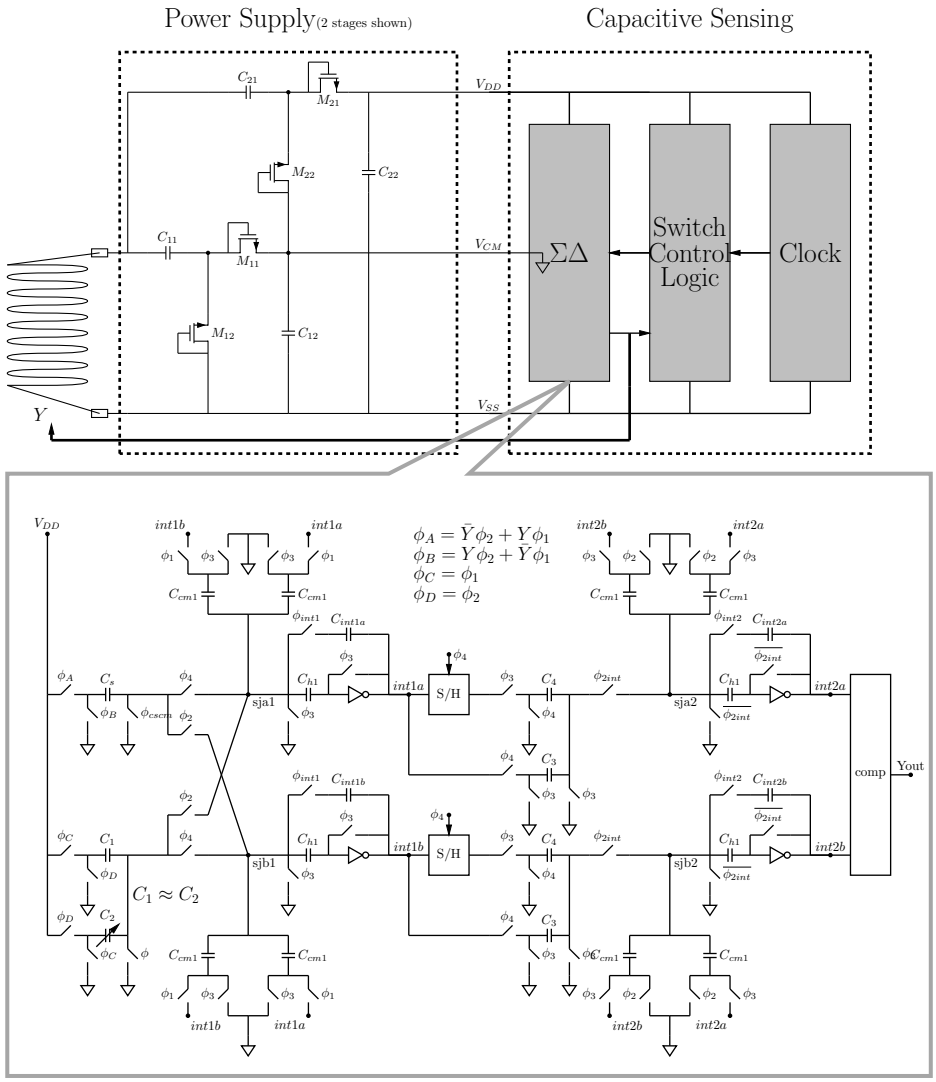

Figure 6.2: Envisioned full IOP measurement system with RFID-style power transfer. The figure shows the voltage multiplying rectifier, ΣΔ modulator and capacitive sensor (within the modulator circuitry). This work investigated the low-voltage, low-power operation capabilities of the modulator together with capacitive sensors.

design of the voltage multiplying rectifier with several stages allows for several intermediate output voltages which may be used creatively within the modulator circuitry.

Research work remaining for the large system include investigation of further power-reduction strategies using the range of voltage outputs from a multistage rectifier, by using lower voltages at digital logic block, for instance; post-processing of MEMS capacitive sensors; development of suitable biocompatable coating that facilitates the transmission of pressure to the sensors; development of the communication circuitry from the implant to the reader; and development of a closed-loop control system to regulate the implant voltage through the communication link.

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APPENDIX A

GLAUCOMA & INTRAOCULAR PRESSURE MEASUREMENT

The purpose of this appendix is to provide a brief description of gluacoma disease and to review the prior gluacoma instrumentation research.

A.1 Introduction

Glaucoma describes a collection of diseases that cause damage to the optic nerve, leading to blindness if left untreated. The primary indicator of glaucoma is elevated intraocular pressure; normal intraocular pressure is approximately 20 mmHg, whereas elevated pressure associated with glaucoma can be as high as 50 mmHg [45].

An implanted intraocular pressure sensor was first suggested by Collins [23] in

1967. In the intervening 30 years, research into miniaturiased implantable sensors specifically for the purpose has pursued both passive [8, 10, 11], and active [6, 24] electronic techniques as well as alternative methods.

An implanted system needs to be reliable, accurate and small. The small size is required for a non-invasive placement to preserve healthy eye tissue for later surgeries. Surgeries is typically required during the course of disease treatment to install drainage systems to release fluid pressure.

A.2 Prior Instrumentation

There has been research into mechanical, passive electronics and active electronic instrumentation for pressure measurement.

A.2.1 Mechanical

The mechanical approach has been researched for external application, in a contact lens implementation, and for implantation.

Tai, et al., 2006 For IOP sensing, an unpowered mechanical micromachined paralene MEMS sensor for use with optical readout circuit was reported in 2004 [27]. For operation, the sensor translates pressure to rotation of a spiral tube and radial displacement is optically observed. The device radius is 1 mm. A response of 0.13 degrees / mmHg was reported for operation in a saline solution.

Renaud, et al., 2004 Also for IOP sensing, contact lens were developed with an embedded strain gauge [26]. The contact lens was noted to be sensitive to fitting

errors, mechanical slippage, and response variation from true intraocular pressure due to indirect measurement through the corneal tissue. Despite the challenges, a contact lens solution is currently being developed commercially [130]. At the time of writing, the performance of the contact lens system was not readily available.

A.2.2 Passive Electronic

Passive electronic techniques have been applied to pressure monitoring. The passive technique uses a pressure sensitive element within a parallel LC resonant tank. The tank resonant frequency is described by,

$$\omega = \sqrt{1/LC} \tag{A.1}$$

where L and C are the tank inductance and capacitance. During operation, the resonant tank is stimulated over a varying frequency range using a nearby antenna. With one of the L, C elements pressure sensitive, a shift in resonant frequency can be related to the pressure changes. Most commonly, the capacitive element is made pressure sensitive.

There are different assembly techniques for construction of a pressure sensitive capacitance. Electrostatic or anodic bonding of silicon to glass can produce highly sensitive capacitive structures suitable for passive sensing; full scale sensitivities of 250% have been reported [53]. Capacitive sensors built directly into the integrated circuit process typically produces much lower sensitivities on the order of approximately 10%.

The following case studies demonstrates some passive systems solutions.

Najafi, et al., 2001 An inductor and pressure sensitive capacitor constructed for the pressure range of 0 – 50 mmHg was reported in [131]. The pressure sensitive capacitor was formed by bonding a doped silicon diaphragm bonded to a glass substrate. Capacitance varied from 2 – 2.35 pF over the pressure range of 0 to 50 mmHg. A 1.2 uH inductor was built by depositing 24 turns of electroplated gold in recesses of the glass structure. A low quality factor in the electroplated inductor coil was stated to be the limiting factor in the maximum operating distance of 2 mm. The device had an area of 2.6 mm x 1.6 mm. Device thickness was not stated. The frequency response was 120 kHz/mmHg with a nominal (zero-pressure) operating frequency of 76 MHz.

Puers, et al., 2004 For IOP pressure sensing, a similar passive approach was used in [8]. Copper coils were deposited onto a silicon substrate, giving an inductance of 400 nH. The technology of the capacitive sensor was not described, but a full scale sensitivity of 250% was stated which presumes an silicon-glass sensor. The size of the implant was approximately 3 mm x 3 mm. An operational distance of 7.5 mm was obtained between the implant electronics and the stimulating electronics. No publications were made on the testing of the instrument in an ocular environment. The sensitivity of the system to mmHg was not stated.

A.2.3 Active Electronic

An active electronic system uses active circuits to measure pressure from a transducer. Data is transmitted from the implant to nearby receiver electronics. Instruments reviewed here were previously outlined in the introduction section of this thesis.

Mokwa et al., 2001 Designed specifically for IOP measurement, this microsystem used novel integrated CMOS capacitive sensors and an external planar coil inductor with an outer diameter of 10.5 mm for communication and power transfer [24]. The external coil was flip chip bonded to the 1.2 μm CMOS integrated circuit. The circuit, coil and capacitive sensor are shown in Fig. A.1. The receiver required 3 V operation and used 210 μW. Operating distance was not stated. Instrument implantation required replacement of the natural lens.

Capacitance measurement was performed using a charge/discharge circuit. Both a reference capcitor (C_{ref}) and sensing capacitor (C_{var} = C_{ref} + C_{fixed}) are charged with matched weak inversion current sources. The voltage difference is sensed by a hysteresis comparator. When the comparator input reaches the hysteresis trip point, the capacitors are flushed of charge and the cycle can begin again. The sensing capacitor C_{var} increases with pressure, making the charge/discharge cycle occur faster. The number of charge/discharge cycles are during a controlled clock period.

Second order circuit effects were considered. Through the use of a hysteresis comparator, voltage dependent capacitive parastics at the comparator input are consistent with each comparison. A calibration cycle is included to account for the temperature sensitive weak inversion current sources. A resolution of 0.73 mmHg was obtained.

The work reported in [24] was developed from earlier work reported in [9, 132]. The earlier work reported a size of 15 mm diameter and 4.5 mm thickness and used micro-wire fabrication that was less robust than flip-chip methods. While the final outcome of the research represents a successful active design, it did not receive medical acceptance due to the highly invasive lens replacement surgery required for

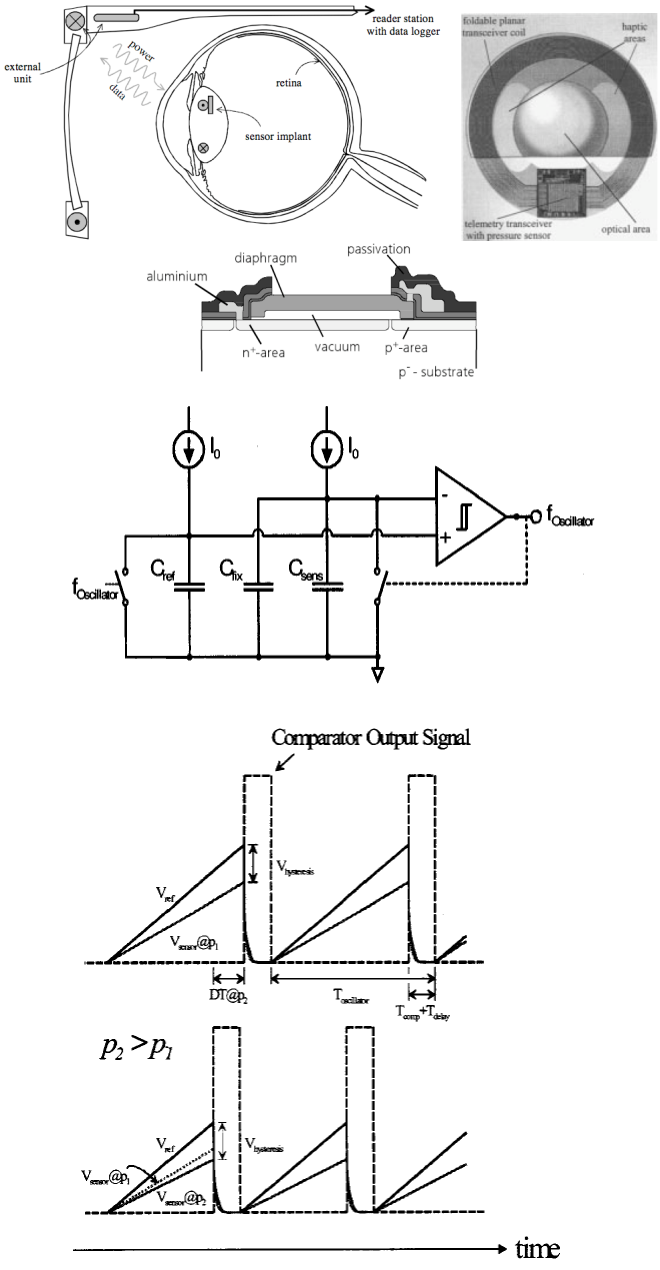

Figure A.1: Microsystem designed for IOP measurement as reported by Mokwa et al. in 2001 [24, 58]© IEEE. The integrated circuit and power receiving coil are embedded into a replacement lens. The pressure sensors (top far right hand side) were manufactured directly in the CMOS process. The capacitive sensing circuit (bottom) uses the charge/discharge technique.

implantation.

Irazoqui et al., 2010 An IOP measurement microsystem using external capacitive sensors was reported in 2010 by Irazoqui et al [13, 25]. Rather than inductive power transfer and communication, the system used radiated data transmission at 2.4 GHz and power reception at 3.65 GHz. Both functions were facilitated with an approximately 3 cm long whip antenna. The integrated circuits required a 1.5 V regulated supply and a 1.3 V reference. Without the data transmitter, the integrated circuits required 200 μW (approximately 160 μW for the sensing circuitry and 40μW voltage regulation and reference). The data transmitter required 1.15 mW. Operating distance for the system during power and data transfer was 10 cm. Far field operation of the power transfer allowed the calculation of a SAR at 3.89 W/kg, just below the controlled exposure limit.

For capacitive measurement, a charge/discharge circuit similar to that reported in [24] was used. From Fig. A.2, two matched nA current sources were used to charge a sensor capacitor (MEMS cap) and a reference capacitor (base cap). The reference capacitor is smaller than the sensor capacitor and trips the schmitt trigger first. The pressure on the sensor capacitance is detected in the additional time taken for the MEMS cap to sufficiently charge and trip it's schmitt trigger. The two schmitt trigger outputs are used to form a pulse which is then measured by a counter. The counter clock is based off a current starved ring oscillator. A resolution of 0.5 mmHg was obtained.

A 24 μF capacitor array is used to hold 48 μC of charge, sufficient charge for pressure sampling at 5 minute intervals; power transfer and data collection was

completed every 24 hours. A picowatt timer was used to control charge delivery from the capacitor array to the voltage regulator. The sensor measurement completes in 1 ms. With 160 μW for the analog sensing circuitry, this corresponds to 0.16 μJ per conversion.

Wise et al., 2011 A capacitive sensing microsystem using a solar cell was reported for intraocular pressure sensing in 2011 [14]. The system is highly integrated with several technologies present, including a MEMS sensor, CMOS integrated circuits (with a microprocessor, memory and analog sensing circuitry), a thin film lithium rechargable battery and a miniature solar cell. The battery provides 3.6 V to the microsystem. For low power subthreshold operation of the digital circuits, the battery voltage is stepped down with 75% effcient switched capacitor network. The system and sensing circuitry is shown in Fig. A.3.

The capacitive sensing circuitry operates as follows. Using the switched capacitor technique, a current proportional to the sum of C_1 and C_2 is generated. This current is then mirrored to a branch supplying the capacitive sensor (designed to be less than C_1 + C_2). The capacitive sensor is similarly switched and therefore draws a portion of the mirrored current. The excess current is used to charge up capacitor C_{int}. Voltage V_{int} is compared to a reference with a clocked comparator; when V_{int} exceeds the reference, the mirrored current is switched off and the capacitive sensor draws currrent off C_{int} until such time as V_{int} falls below the reference and the comparator output switches low. When the comparator output goes low, the mirrored current branch is switched back on and the process begins again. Notice that if C_{int} were instead flushed of charge and the time taken to charge up past the reference was

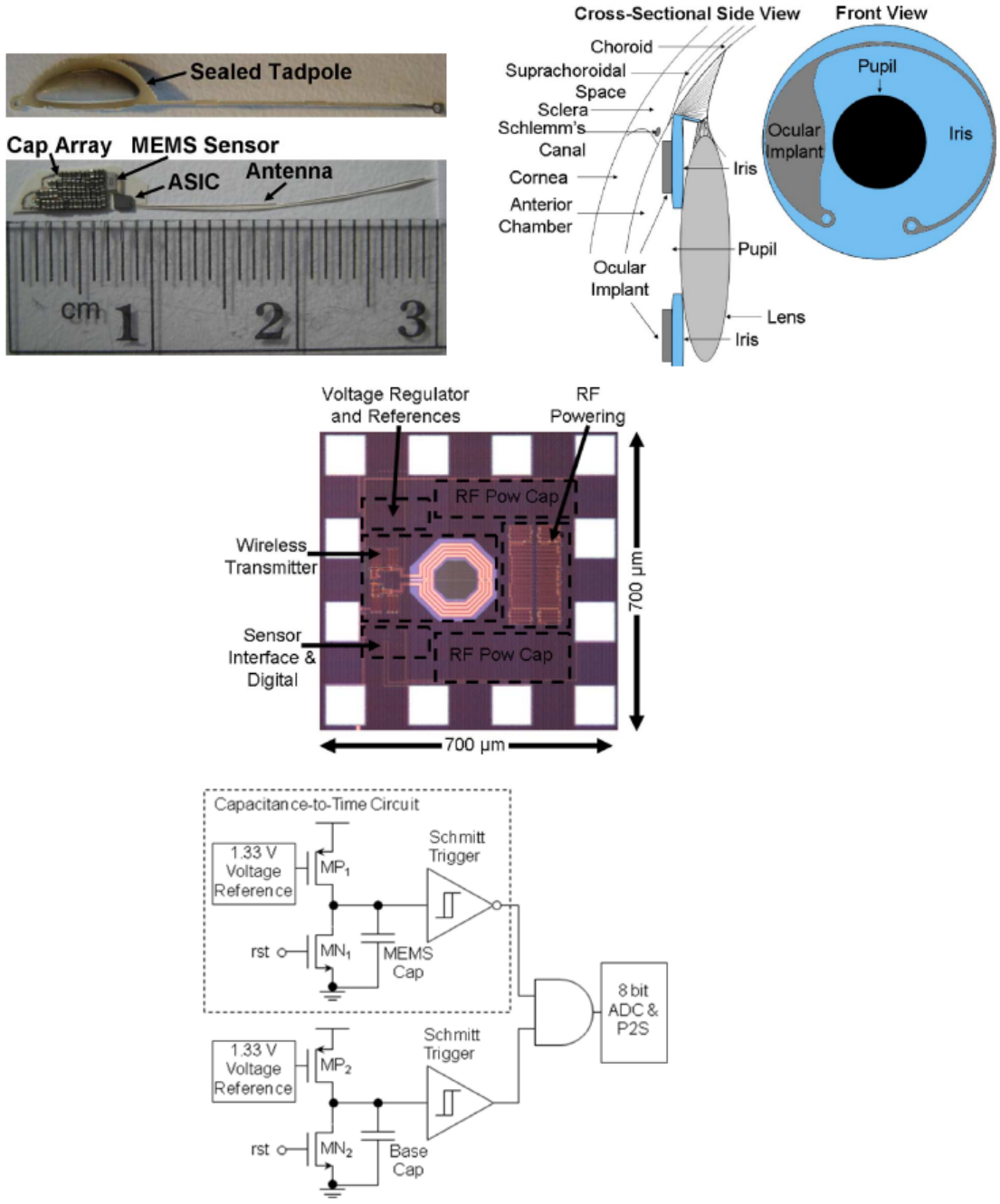

Figure A.2: Microsystem designed for IOP measurement as reported by Irazoqui in 2010 [13]© IEEE. The assembled microsystem, including 52 individual 0.24 μF capacitors, is shown on the top left hand side. Intraocular placement is shown on the top right hand side; the whip antenna is curved around the pupil along the iris. The integrated circuit, showing the data transmitter inductor coil, is shown on the bottom left hand side. The sensing circuitry is shown on the bottom left hand side.

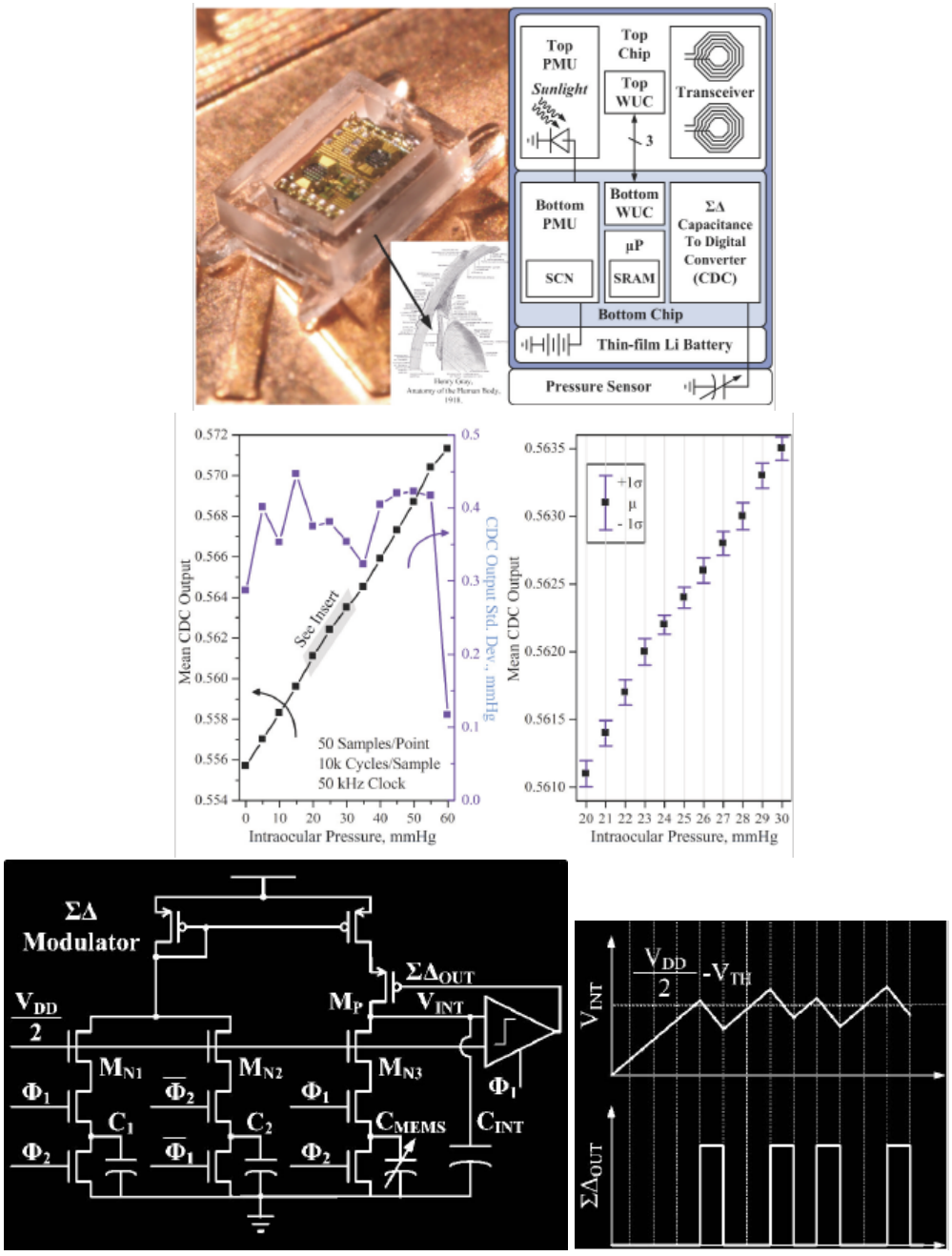

Figure A.3: Microsystem designed for IOP measurement as reported by Wise et al. in 2011 [14] © IEEE.

recorded instead, this circuit would be similar to the previous conversion methods. The introduction of memory (integrated charge) and feedback converts the system into a single bit $\Sigma\Delta$ measurement. The measurement is ratiometric, comparing the variable capacitor to a fixed capacitance, allowing the circuitry to be relatively insensitive to timing and power supply variation. Power for the capacitance to digital conversion circuits alone was 7 μW.

To obtain 0.5 mmHg resolution it was required to average 50 samples. Each sample is obtained by an average of 10,000 single bit data points from the modulator. At 50 kHz, this process takes 500,000 single bit samples and requires 10 seconds. To obtain 0.5 mmHg resolution at 15 minute intervals, a total of 6720 μJ are required daily which translates to 78 nW operation. The reported power specification of 143 μJ per day and 5.3 nW operation was based on obtaing only 10,000 single bit samples. The microsystem is not energy autonomous at a resolution of 0.5 mmHg and the resolution at 10,000 samples is not stated.

In order to be insensitive to non-linearities in capacitor charging, switched capacitor circuits typically only pass on accurately settled capacitor voltage forward in the signal path. In this report, capacitor C_{int} collects current during the PMOS start up, or switching event if the current is shunted aside to avoid a start up transient. The design does not appear to be robust to non-linearities in capacitor charging. The report [14] is a conference paper, so many design details are not yet discussed.

A.3 Conclusion

Instrumentation research has applied mechanical, passive electronic and active electronic solutions to the IOP measurement. The passive electronics technique has the advantage of eliminating the need for implant powering but require a highly sensitive capacitive transducer; the active technique can use low sensitivity capacitive sensors compatible with CMOS processes but wireless power and signal transfer is required. To date, active electronics circuits have provides the highest level of performance in terms of resolution and implant operating distance. Size reduction is hindered in both passive and active electronic solutions. Passive circuitry requires a highly sensitivity capacitive sensor, typically produced by very large structures. Active circuitry typically requires a large inductor for power transfer.

APPENDIX B

CMOS IC COILS FOR POWER TRANSFER

The purpose of this appendix is to give an overview of the technical challenge of inductive wireless power transfer to integrated circuit coils for biomedical purposes, and overview work to date on power transfer to integrated circuit coils.

B.1 Wireless Inductive Power Transfer

This section briefly describes the technical challenges and limitations of inductive wireless power transfer.

Wireless inductive power transfer is achieved with two coupled inductors forming a transformer circuit. To obtain maximum drive current, the power transmitting cir-

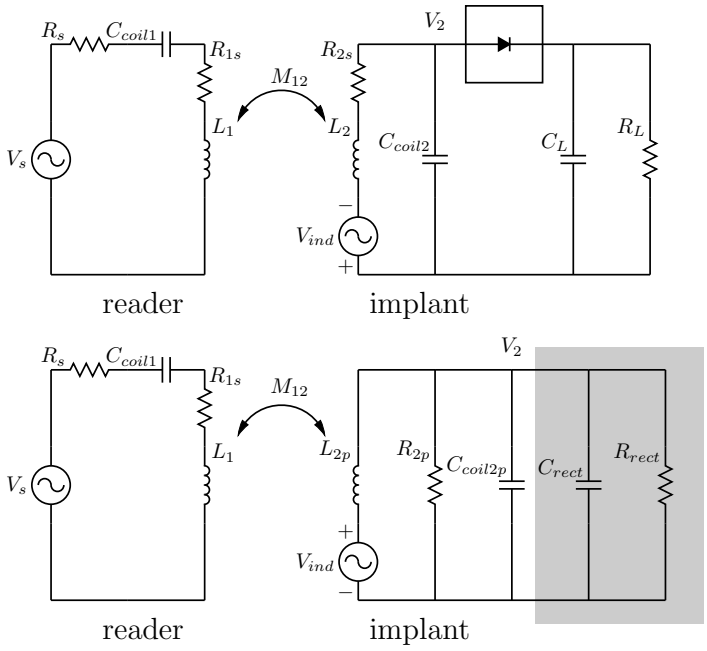

Figure B.1: Coupled inductors for wireless power transfer. The reader electronics uses a series resonant circuit for maximum current drive. The implant uses a parallel resonant circuit for maximum input impedance. The implant is shown with a series (top) and parallel equivalent (bottom) circuit model for the coil. For simplicity, the rectifier/diode is assumed to be ideal. Reader electronic elements are referred to with the subscript "1", and the implant electronics are referred to with the subscript "2". The average input resistance and capacitance of the rectifier when the implant is powered, is denoted as R_{rect} and C_{rect} respectively, are shown in the shaded box in the parallel equivalent circuit.

cuitry (reader electronics) use a series-tuned circuit; for maximum input impedance, the implant circuitry uses a parallel-tuned circuit. A representative coupled inductor circuit is shown in Fig. B.1. For increased efficiency, the two inductors are typically tuned to a common resonance frequency. The power transfer link is fully described by fourth-order bandpass transfer function equations. The reader is referred to [133] for more information on the operation of such a link for biomedical applications.

The design of inductive power transfer links was well covered in the literature from the early 1980's [134–136]. The major challenges of power efficiency and sensitivity to coil displacement were addressed. In a typical inductively coupled wirelessly-powered biomedical system, the inductors are assumed to be strongly coupled with the inter coil distance on the same order or smaller than the diameter of the implanted coil. Such closely located and strongly coupled, links with fixed orientation can be optimised with a critical coupling that ensures least sensitivity of the implant voltage on the physical arrangement of the coils [133–135]. When the size of the implant inductor coil is severely limited, and the coupled inductors may not be strongly coupled, the operation of the wireless power transfer link is said to be weakly coupled.

Due to a presumed weakly couple link, standard design procedures for biomedical links do not apply when considering millimeter scale integrated circuit coils at the implant. Because the power transfer capability of an inductive link scale directly with the area of the implant coil, typical biomedical applications start the design process with the largest medically accepted implant coil then determine the inter coil distance required to achieve critical coupling. The procedure of determining

and using the critical coupling inter coil distance is done to obtain least sensitivity in the voltage transfer. When the diameter of the coil is required to be smaller than the implant depth, as would be the case in a millimeter-scale IOP instrument, the critical coupling cannot be achieved and the link voltage transfer function necessarily has a strong sensitivity to inter coil distance.

In the case of an implant diameter smaller than the critical coupling inter coil distance (the presumed case for this project) the voltage at the implant increases rapidly with decreasing distance between the two coils. Because the reader coil is typically less restricted in size and materials, the link voltage and power transfer capability primarily depends on the quality and system parasitics associated with the implanted coil. From this, the most crucial and important aspect of the system design is exposed.

Simply put, the most critical design aspect of the larger system design is the power and voltage requirement at the implant electronics. A large power consumption at the implant decreases the efficiency of the power transfer link and makes generating sufficient terminal voltage difficult. Conversely, extremely low-power and low-voltage pressure measurement circuitry greatly ease the challenge of power transfer by decreasing the effective loading on the IC coil.

To see this in circuit terms, consider the simple circuit model of the inductive power transfer link shown in Fig. B.1. Prior to forward bias operation of the rectifier diode, the implant coil is subject to a parasitic resistance and capacitance shown by R_{2s} and C_{coil2p} as well as parasitic input capacitance of the diode, C_{rect}. When a sufficient level of dynamic magnetic flux is received at the inductor coil, the magnitude of the terminal voltage V_2 increases and the rectifier becomes forward

biased to power the implant electronics. During operation of the implant sensing circuitry, when the rectifier provides sufficient DC voltage for the circuitry to function, the coil is loaded by the average input resistance and capacitance of the rectifier which is then operating to provide the required DC load power. In order that the terminal voltage V_2 be sustained, additional loading must not substantially affect the coil; alternatively, using the parallel circuit model of the coil, $R_{rect} \gg R_{2p}$. If loading due to the implant circuitry is excessive, the coil terminal voltage will decrease substantially, the rectifier will fail to function, and power will no longer be transferred to the load.

B.1.1 Summary

In the case of implantation distances larger than the implant diameter, the standard design procedures of coupled inductor wireless power transfer links does not apply. The link is subject to strong variations in implant voltage with variations in the inter coil distances. High power consumption at the implant circuitry increases the load on the implant coil, decreasing the efficiency of the power transfer link making the generation of a terminal voltage much more difficult. For a given coil diameter and implantation distance, the terminal voltage depends on the implant coil parameters and the strength of the field exposure. As discussed, RF field exposure should be minimized in biomedical applications making low-power, low-voltage implant circuitry desirable. Circuit architectures that are capable of low-voltage operation and robust to variations in power supply voltage are additionally desirable due to expected variation in supply and additional power loss in on-chip regulation.

B.2 History

This section outlines the developments in integrated CMOS inductor coils used for wireless power transfer.

The first report of a wirelessly powered CMOS integrated coil was given in [137, 138]. The inductor was implemented in a standard 3 μm p-well CMOS. The metals in the technology were highly resistive and there were no special provisions for implementation of integrated inductors. The reported inductors had quality factors less than unity [138]. The inductor was designed as a 30 turn coil using a 5 μm trace width. The outer dimensions of the inductor were 4.4 mm x 7.5 mm. A bridge rectifier and filtering capacitor formed the rest of the integrated power supply circuitry. With a 0.02 T field stimulation at 800 kHz, 3 V was obtained on a 10 kΩ load (corresponding to 0.9 mW).

In [139] an inductor coil was obtained by a placing metal trace around the perimeter of a CMOS die. The core area was fully utilized with CMOS circuitry. The inductor coil used 6 turns and was implemented in the upper 5 metal layers of a 0.25 μm CMOS technology. The outer dimensions of the inductor were 4 x 4 mm^2. With a 1.1 mT field the generated voltage was greater than or equal to 0.8 V. Power consumption of the circuitry was not stated.

At UHF frequencies, a fully integrated RFID transponder tag with inductor coil and rectifier was reported in [128]. The inductor was 550 μm x 550 μm. The inductor was implemented in a standard 0.18 μm CMOS with no special provisions for high quality inductor metals. The inductor was operated with frequency of 900 MHz. The reader antenna was a square 4 turn printed circuit board coil with an outer dimension of 5 mm x 5 mm. At a distance of 4 mm, the mutual inductance of

the coupled system was estimated at 4 nH. Estimation of the magnetic field using a simple circular model for the transmit antenna with a stated reader current of 318 mA peak gives approximately 48 μT. Under these conditions, a 0.3 V was induced on the integrated circuit inductor coil. The inductor voltage was applied to a voltage multiplying rectifier to obtain a 1 V supply providing 2.7 μW.

For 2.45 GHz RFID applications, an ultra-small 300 μm x 300 μm fully integrated transponder was constructed [29]. The coil antenna is made with a post-processing step of depositing gold plating on top of a standard CMOS 0.18 μm integrated circuit. Parasitic capacitance was used to form the high frequency LC tank. With an intended application of paper document anti-counterfit measures, the integrated circuit was thinned to be only 0.06 mm thick. A voltage of 0.5 V was obtained from the coil and integrated circuit rectifier. At 0.5 V operation, the circuitry had a current consumption of 3 μA for a power consumption of 1.5 μW. An 80 pF capacitor formed by gate oxide was used to bypass and buffer the power supply. The operating distance was reported as 1.2 mm. No statements were made on the stimulating field or transmitting antenna.

B.3 Summary

The following points summarises the success and timeline progression of integrated circuit inductor coil power transfer reports that have been outlined in this section.

- In 2001 complementary metal oxide semiconductor (CMOS) metal coil was used to receive power for a smart card application operating at 13.56 MHz [139]. The coil was 1.5 mm^2 and operated with a 1.1 mT magnetic field.

Power consumption during field stimulated operation was not reported.

- In 2004 the smallest reported IC coil for power reception was reported as a post processed gold coil antenna of 0.4 mm x 0.4 mm operated at 2.45 GHz [29]. The operating power of the digital circuitry at minimum was 1.5 μW from 0.5 V. The field exposure required for operation was not given, but a maximum distance of 1.2 mm from the reader antenna was reported.

- In 2008 a 1 mm x 0.5 mm copper coil was to be placed above the CMOS circuitry with a post processing step of adding undoped silicon glass [140]. The RFID circuitry had power consumption of 10 μW at memory read and 56 μW at memory write. Memory write operations required a dc-dc step-up converter to produce the required voltage of 8 V. The stimulating magnetic field was not reported, but read/write operations were achieved only at a distance of less than 0.5 mm from the reader antenna.

- In 2008, a thick metal, RF CMOS process was used to implement a 0.5 mm x 0.5 mm antenna using five metal layers [141]. At 900 MHz operation, the coil and associated voltage rectifier [142] were capable of providing 10μA at 1V operated 4 mm from the reader antenna.

APPENDIX C

WIRELESS POWER TRANSFER BIOCOMPATIBILITY

This section will review the available research and regulation with the aim of finding a definitive upper limit for power transmission for the IOP measurement instrument operating in an ocular environment.

C.1 Introduction

Wirelessly powered electronics have two primary heating sources. Tissue absorption of incident electromagnetic energy, and tissue absorption of power dissipation within the electronics. With extremely low power electronics, absorption of electromagnetic energy is expected to be the most significant heating contribution. Damage to eye

tissue can occur with a temperature rise of $3^{\circ}\mathrm{C}$, and temperatures at or above $41^{\circ}\mathrm{C}$ are known to greatly increase the risk of lens cataract [42].

C.1.1 FCC Guidelines

The Federal Communications Commission (FCC) [143] which regulates RF energy from telecommunications, provides biological exposure guidelines. Researchers in the field of wirelessly powered implanted instruments have used the FCC guidelines, shown in Table C.1, to determine preliminary biocompatability of systems with large power receiving coils [144, 145].

Frequency (MHz)	Electric Field (V/m)	Magnetic Field (A/m)	Power Density (mW/cm^2)	Averaging Time (min)
0.3–3.0	614	1.63	100	6
3–30	1842/f	489/f	$900/f^2$	6
30–300	61.4	0.163	1	6
300–1500	n/a	n/a	f/300	6
1500–100,000	n/a	n/a	5	6

Table C.1: Tabulated values of maximum permissible occupational RF energy exposure levels given by the FCC.

Calculations for biocompatibilty of a wireless power recieving antenna is done as follows. Using the occupational exposure levels, an implant with an area of one

square millimeter could ideally capture the following powers at various frequencies:

$$\begin{aligned}
P_{max_{13.56\mathrm{MHz}}} &= \tfrac{900}{13.56^2}\left(\tfrac{\mathrm{mW}}{\mathrm{cm}^2}\right)1\mathrm{mm}^2\left(\tfrac{1\mathrm{cm}}{10\mathrm{mm}}\right)^2 = 0.049\mathrm{mW} \\
P_{max_{200\mathrm{MHz}}} &= 1\left(\tfrac{\mathrm{mW}}{\mathrm{cm}^2}\right)1\mathrm{mm}^2\left(\tfrac{1\mathrm{cm}}{10\mathrm{mm}}\right)^2 = 0.010\mathrm{mW} \\
P_{max_{433\mathrm{MHz}}} &= 433/300\left(\tfrac{\mathrm{mW}}{\mathrm{cm}^2}\right)1\mathrm{mm}^2\left(\tfrac{1\mathrm{cm}}{10\mathrm{mm}}\right)^2 = 0.014\mathrm{mW} \\
P_{max_{1500\mathrm{MHz}}} &= 1500/300\left(\tfrac{\mathrm{mW}}{\mathrm{cm}^2}\right)1\mathrm{mm}^2\left(\tfrac{1\mathrm{cm}}{10\mathrm{mm}}\right)^2 = 0.050\mathrm{mW}.
\end{aligned}$$

While the available power is larger at 13.56 MHz than it is at 433 MHz, voltage development at lower frequencies on an inductor coil at lower frequencies is impaired. In the range of 300-1500 MHz, the allowable power density increases with frequency such that the power available at 1500 MHz is equivalent to that at 13.56 MHz.

C.2 IEEE Recommendations

The FCC refer to the IEEE Standard C95.1-2005 [146] for health and biological impact of RF energy. The IEEE guidelines are expressed in units of specific rate of absorption, or SAR. Calculation of the SAR considers both the incident electric field strength, polarization and the frequency dependent tissue conductivity. In general, the SAR increases with frequency [147]. For this reason, most biomedical applications typically stay within a few 10's of MHz where the SAR is well below the peak value as shown in Fig C.1.

The IEEE recommends a general SAR limit of 1.6 W/kg for the human body. Regarding the human eye, the IEEE standard states that a peak spatial-average SAR

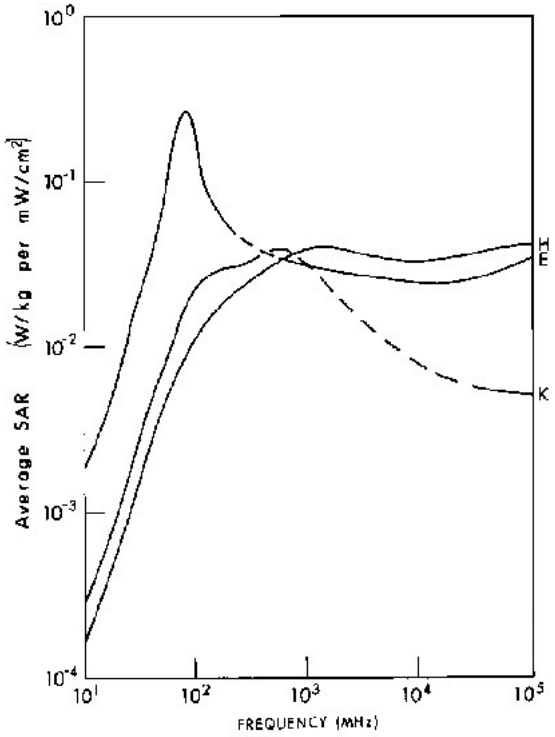

Figure C.1: Whole body averaged SAR for a model of an average man [147]. Incident power of 1 mW/cm^2 shown for three different electric field polarizations.

of 10 W/kg averaged over 10 g is deemed to be low enough to avoid adverse effects such as cataracts [146]. Research reviewed for the standard showed that SAR values of $\geq$ 150 W/kg for $\geq$ 30 minutes are required to bring the temperature near a rabbit eye lens to 41°C . The value of 150 W/kg is significantly higher than the general exposure levels of 1.6 W/kg used for the occupational guidelines given in Table C.1. The research indicates that the FCC guidelines provided are very conservative.

C.3 Eye Health Research

C.3.1 Telecommunications Research

Research has been conducted to determine the thermal impact of radiation exposure at common telecommunications frequencies. To determine a temperature rise from a power density exposure or a SAR value, modeling is done with heat transfer coefficients from the eye to it's surroundings. This section presents a brief survey of research in this area.

- (1975) Power incident at 100 mW/cm^2 generated an internal hot spot of 40.4°C using simple heat sink models to represent eye vascularisation while simulating 1.5 GHz plane wave exposure [148]. No such hot spot was present at the same incident power levels for 750 MHz. The development of internal hot spots in the eye occurring at specific frequencies above approximately 600 MHz is a well verified and accepted phenomena [42, 44].

- (2000) Power incident at 0.5 W/cm^2 at frequencies between 600 MHz and 6 GHz produced the SAR and temperature changes shown in Fig. C.2 [42]; peak temperature rise of 0.3°C resulted at 6 GHz. The same research also indicates that the impact of eye size variation is slight; a modeled eye diameter between 2.4 and 2.8 cm caused only an approximately 10% variation in SAR and temperature rise.

- (2007) Results of [42] used heat transfer coefficients derived in 1982 which have recently (2006) been determined to be underestimated [149]. More

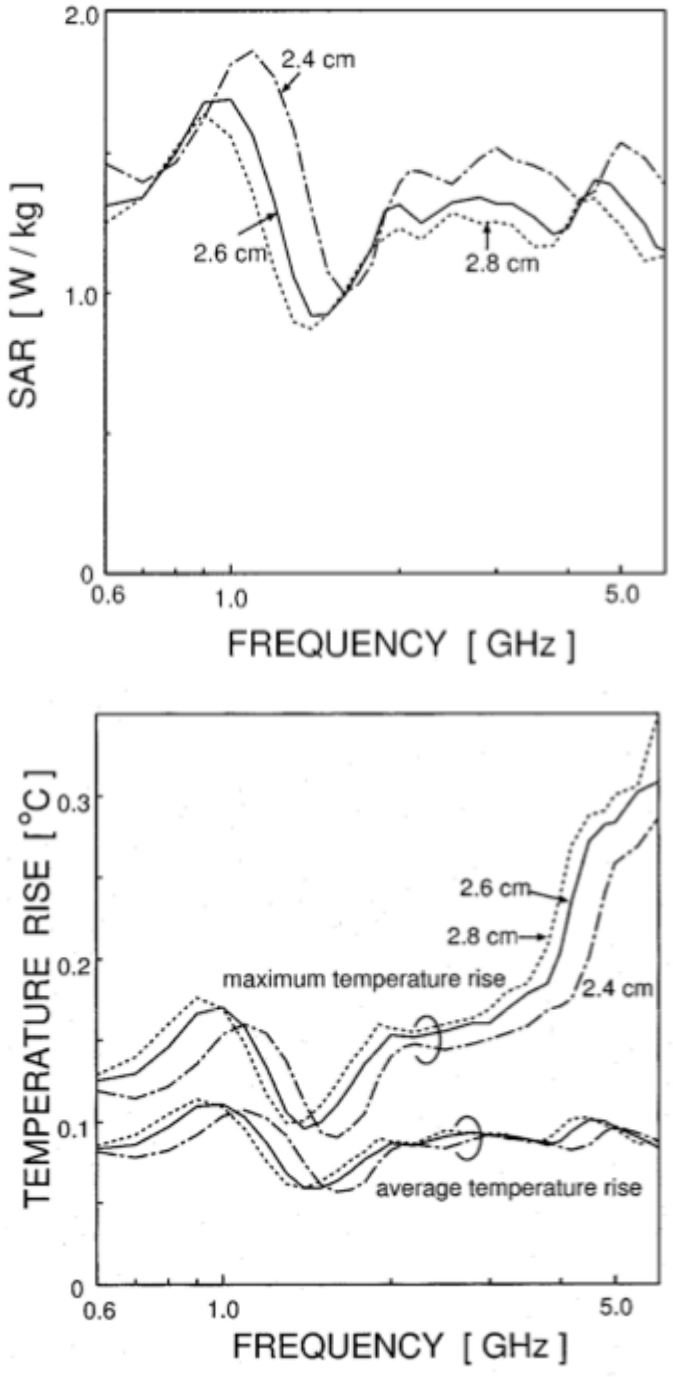

Figure C.2: Whole eye SAR in W/kg for incident power of 0.5 W/cm^2 at various frequencies (upper) and associated temperature rise (lower) given by eye-tissue heat transfer modeling as reported in [42].

detailed simulations with newer heat transfer coefficients have shown temperature increases to be lower with similar exposure levels. Results for three different thermal eye models are shown below. Note that the SAR values all exceed the IEEE suggested exposure limit of 1.6 W/kg, yet the anticipated temperature rise is less than $0.3^{o}\mathrm{C}$ in all model cases.

	900 (MHz)	1500 (MHz)	1800 (MHz)
SAR (humor) (W/kg)	4.5	7.7	8.4
SAR (avg. eye)	1.7	2.5	2.2
Temperature Rise			
Model: Discrete Vascularisation (DIVA)	$0.22^{o}\mathrm{C}$	$0.27^{o}\mathrm{C}$	$0.25^{o}\mathrm{C}$
Model: Pennes Bioheat	$0.19^{o}\mathrm{C}$	$0.24^{o}\mathrm{C}$	$0.22^{o}\mathrm{C}$
Model: Spherical	$0.15^{o}\mathrm{C}$	$0.22\ ^{o}\mathrm{C}$	$0.20^{o}\mathrm{C}$

C.3.2 MRI Research

Ocular heating due to magnetic field exposure during magnetic resonance imaging (MRI) has also been researched. Because the energy absorbed depends on the strength of the static field, not just the RF field [150], the data is not directly relevant for the project. However, imaging for eye pathology has obtained data for the direct measurement of corneal temperature after exposure with a calculated SAR values. In this research it was found that a SAR as high as 8.4 W/kg produced a maximum temperature rise of $1.8^{o}\mathrm{C}$ [151].

C.4 Reported Powered Integrated Circuit Coils

This section reviews reported power levels obtained with from millimeter-scale integrated circuit (IC) coils. Transmitted power must not expose the patient to additional health concerns through excessive exposure to radio-frequency energy. Within the power review of transmitted power to IC coils below, attention is paid to exposure levels.

While radio frequency identification (RFID) systems have reported inductive power transfer to on-chip IC coils, to the author's knowledge there have been no reports of biomedical applications using IC coils.

In many reports of wirelessly powered IC coil circuits for RFID, the incident power and IC operating power are not reported together (see Appendix B), making simultaneous power and biocompatability estimates difficult. Frequently the tag electronics are stated to be operated in subthreshold conditions, with communication back to the reader verifying operation but without the tag operating power reported concurrently. Operated in the extreme near field of the reader coil antenna, the magnitude of the magnetic field terms are not easily determined.

A recent report of a standard CMOS IC coil antenna RFID tag [141, 142] and a low-voltage rectifier [128] operating at 900 MHz provides both output power and rectifier operating efficiency from which a biocompatability estimate can be made. From an output power of 10 μW and a rectifier efficiency of approximately 30% [129, 142, 152, 153], the total power input to the rectifier was roughly 30 μW. Assuming no loss at the coil, this corresponds to an incident power density of approximately 12 μW/mm^2. The IEEE Standard C95.1-2005 [146] recommends a general radio-frequency specific absorption rate limit of 1.6 W/kg for the human

body. The FCC incorporates the IEEE exposure limits in their guidelines for radio-frequency energy exposure. At a frequency of 900 MHz, the FCC controlled occupational exposure is 30 μW/mm^2; the general population uncontrolled exposure limit is set at 6 μW/mm^2.

While the CMOS IC coil antenna RFID report at 900 MHz [141] indicates an operating power level of 10 μW would be biocompatible, the target operating frequency for eye health should be below 600 MHz above which hot spots have been demonstrated to occur [42,44]. In Canada, a suitable frequency is within the amature radio allocation from 420–450 MHz [154]. At 450 MHz, the FCC allowable power densities are reduced to 15 μW/mm^2 and 3 μW/mm^2 for occupational and general exposure, respectively.

The FCC tabulated occupational exposure amounts are time averaged over 6 minutes. With intermittent operation requiring seconds, allowable incident power for the instrument could be higher. However unknown impact of tissue loss and the expectation of loss with the IC coil, as well as additional losses due to link communication using load modulation, make this an unbounded problem until an entire system is constructed or modeled in detail.

C.5 Conclusion

To obtain an upper limit for power transmission, this section reviewed the available regulation and research. A definitive guideline for the upper limit for power transmission was not found. While both the IEEE Standard C95.1-2005 and the FCC provide general guidelines, both specifically state that their recommendations are not meant to govern biomedical applications. Eye health research indicates that the

eye can support exposure levels higher than indicated in the FCC guidelines. For this project, the following observations are made:

- Due to the formation of internal eye hot spots, operating with frequencies below below 600 MHz is recommended.

- Eye health research shows that vascularisation models have a significant impact on temperature rise. In recent research exposing the eye to high frequency energy, thermal response was less than expected, and well below concerning levels. However, it is unknown if a diseased eye has the same functional vascularisation as a healthy eye.

- The near field of the inductor coil is comprised mostly of an alternating magnetic field; the electric field is intended to be contained in the implant coil. Outside of the near field region of a coil antenna, there will be both magnetic and electric fields which must be considered. However, with a poorly radiating antenna these are not expected to be substantial. Under these conditions, the primary contributer to heating will be dissipative eddy current losses in the tissue. This has not been well studied.

APPENDIX D

SECOND-ORDER $\Sigma\Delta$ MODULATION

The purpose of this appendix is to describe the operation of second-order $\Sigma\Delta$ modulation.

D.1 Second Order $\Sigma\Delta$ Modulation

Second-order $\Sigma\Delta$ modulation was first reported by Candy in 1985 [155]. For loop stability, the second integrator receives signal content from both the first stage and the modulated output.

With unity-gain on both integrator input feedforward paths, $a_1 = a_2 = 1$ and unity-gain on both the ADC and feedback DAC, $k_1 = k_2 = 1$, a second-stage

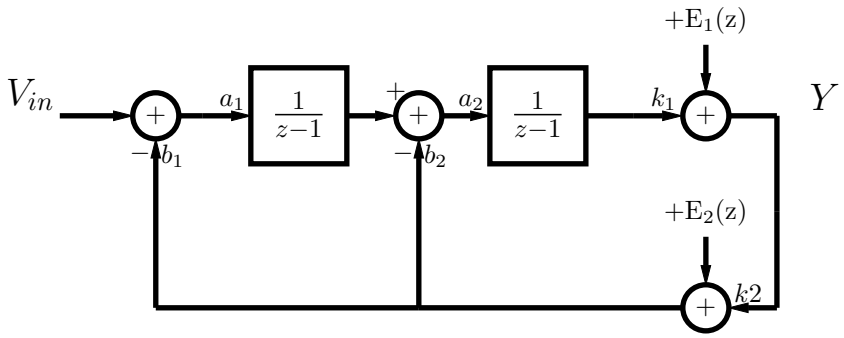

Figure D.1: Second-order ΣΔ modulator with both the embedded ADC and DAC modeled as a linear gain elements, k_1 and k_2, with additive noise E_1 and E_2.

feedback coefficient of $b_2 = 2$ is required to place the z-domain pole at the origin for maximum stability. The resulting transfer function is

$$\begin{aligned} Y(z) = V_{in}(z) &\left(\frac{1}{z^2}\right) \\ &+ E_1(z)\left(\frac{(z-1)^2}{z^2}\right) \\ &- E_2(z)\left(\frac{1+2(z-1)}{z^2}\right), \end{aligned} \tag{D.1}$$

where E_1 and E_2 are the additive errors of the internal ADC and DAC.

The use of multi-bit data converters in ΣΔ modulation placed high demands on the linearity of these components; level placement errors of the converters embedded in the loop translated to distortion error in the ΣΔ modulated output. Single-bit data conversion solved the problem of distortion easily as the two points of a single DAC or ADC perfectly define a straight line. Using single-bit modulation, additive error from the DAC was eliminated and level placement became gain error only. An embedded single-bit ADC converter is easily implemented with a comparator.

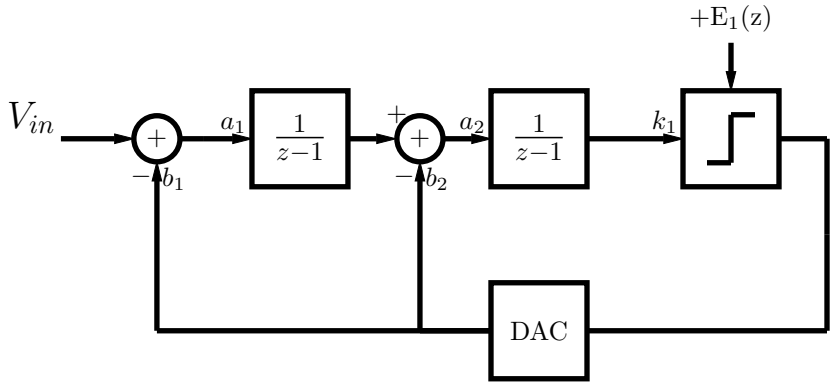

Figure D.2: Second-order ΣΔ modulator with single-bit quantization shown with a comparator implementing the ADC and an ideal feedback DAC.

The single-bit second-order ΣΔ modulator transfer function is,

$$Y(z) = V_{in}(z)\left(\frac{1}{z^2}\right) + E_1(z)\left(\frac{(z-1)^2}{z^2}\right). \tag{D.2}$$

With single-bit modulation, the gain term of the embedded ADC is not fixed and varies depending on the magnitude of the sampled output at the second integrator; thus the system poles become dynamic. The poles stay within the unit circle, and modulator is unconditionally stable, if and only if the first integrator gain, $a1$, is less than or equal to 0.8 times the feedback factor to the second integrator $b2$ [156].

To facilitate the difference in gain between the feedforward signal of the first integrator and the feedback signal of the modulated output to the second integrator, two different input-signal pathways are required at the second integrator. To eliminate the need for different input-signal pathways, a scaled integrator structure, where the feedback factor of 2 was brought through the summing junction for a gain

of 1/2 at each integrator, became popular [105, 157, 158]. Because the second integrator was immediately followed by a single-bit comparator with variable gain, the second-integrator could be further scaled to reduce signal swing without impacting the loop stability. Further gain scaling at the second integrator is often applied to reduce the integration range and ease the circuit implementation.

There are several circuit level effects in the modulator that are relevant for this project:

Integration Range $\Sigma\Delta$ modulators of order greater than one must use simulation to determine the integrator output range [106]. When the integrator output range exceeds the linear range of the amplifiers used to implement the integrator, the modulated output suffers from increased distortion. The range of integrator output is a function of the input signal range; small input signals produce small integrator output ranges.

Pole Error Because the gain element inside the closed loop transfer function is an integrator, a $\Sigma\Delta$ modulator is particularly robust to low gain amplifiers.

The impact of low gain amplifiers on the integrator is a pole error in the integrator transfer function. An ideal integrator transfer function is as follows,

$$\frac{V_o}{V_{in}} = \frac{C_s}{C_{int}} \left(\frac{1}{z} \right), \tag{D.3}$$

where V_o is the output voltage, V_{in} is the input voltage, C_s is the integrator sampling capacitance, C_{int} is the integrating capacitance. Pole error results in an integrator

transfer function of,

$$\frac{V_o}{V_{in}} = \frac{C_s}{C_{int}} \left(\frac{1}{z - (1 - \alpha)} \right), \tag{D.4}$$

where α is approximately equal to $1/A_o$ where A_o is the amplifier open loop gain.

When there an integrator pole error occurs, the closed loop transfer function is impaired, quantization noise shaping is less effective and in-band quantization noise increases. For second-order modulation, increased in-band quantization noise power is less than 1 dB if the amplifier DC gain is comparable to the oversampling ratio [105]. This predicts that the modulation will continue to be functional with low-gain of amplifiers resulting from low-voltage, low-power operation.

Comparator While $\Sigma\Delta$ modulators are generally robust to comparator offset, comparator offset has consequences on the operation of the circuitry implementing the loop. Due to the high feedback around the loop, comparator offset is stored at the output of the integrator proceeding the comparator [156]. This can introduce operating point changes in the comparator and other circuitry that receives the output of the second integrator. Stored offset also affects the integrator output range, introducing increased distortion for large comparator offsets.

Noise Floor A fundamental limit to the maximum resolution of a $\Sigma\Delta$ modulator is imposed by the noise sources at the modulator input; noise at the input of the modulator is transferred directly to the output unattenuated whereas noise introduced at later stages is attenuated by the noise shaping properties of the loop.

APPENDIX E

AS1 PAD NAMES & DESCRIPTION

V_{DDCOMP}	comparator power supply voltage
V_{DD}	logic, switches and integrator power supply
V_{DDIO}	power supply voltage for the level shift output
V_{CM}	mid-supply common-mode voltage, V_{CM} = $V_{DD}/2$
V_{ss}	substrate, analog and digital ground.
V_{ref}	reference voltage input for sampling capacitor C_1
V_{refC2}, V_{refC1}	reference voltages for C_2 and C_1
V_{cdb}	input for bottom plate of the differential capacitors, C_1 and C_2.
$cmc1a$	top plate of mimcap capacitor for voltage input mode.
$cmc2a$	top plate of mimcap capacitor for voltage input mode.
$cmdb$	bottom plate of mimcap capacitor for voltage input mode.
$cdcm$	cm input for differential capacitors C_1 and C_2.

$c1a$, $c2a$	accepts top plate of sensing capacitor C_1, C_2.
$calin$	calibration control, active high (vdd).
$phi1in$, $phi2in$, $phi3in$, $phi4in$	phase 1, 2, 3 &4 of the 4 phase clock input.
Y	buffered modulator output Y.

APPENDIX F

POWER SUPPLY

This section discusses the design of a voltage multiplying rectifier using low-threshold voltage transistors.

F.1 Voltage Multiplying Rectifier

The purpose of a rectifier is to convert AC voltage to DC voltage. Design goals of a rectifier include power efficiency, large input-resistance, and a high voltage-sensitivity. Voltage-sensitivity is a measure of the DC output voltage response for a given AC voltage input.

In the case of wirelessly powered systems, the AC voltage source is the induced voltage at the terminals of the inductor coil. To overcome low inductor coil voltages in RFID applications, voltage multiplying rectifiers have been applied [128, 129, 159,

160]. Voltage multiplying rectifiers offer high voltage sensitivity because they act to multiply the voltage. Voltage multiplying rectifiers do not provide any additional power; thus as voltage is increased, the available drive current is reduced.

F.1.1 Basic Operation

A voltage doubler is a single-stage voltage-multiplying rectifier shown in Fig. F.1. Voltage rectification is accomplished with two independent circuit operations of a charge pump and a peak detector. The charge pump operation occurs when the AC input signal is negative relative to ground. At this time, the charge pump capacitor C_1 stores the voltage through the diode-connected transistor M_2. Peak detection occurs when the AC input signal is positive relative to ground. At this time the peak value of the DC shifted voltage is processed through the diode-connected transistor M_1. The DC shift is equal to V_p - V_D where V_p is the peak voltage of the ac input, and V_D is the forward voltage drop of M_2 in the diode configuration. Finally, the voltage stored on C_2 is equal to $2\times V_p$ - $2\times V_D$. With ideal diodes, $V_D = 0$, and the voltage stored on C_2 would be *double* the peak voltage.

Several stages of a multiplying rectifier can be stacked for an increased DC voltage.

F.1.2 Design Issues

In CMOS, a rectifier is built from diode-connected MOS transistors. The forward voltage drop of a diode-connected transistor is equal to the gate-source voltage as described by,

$$|V_{GS}| = |V_{DS}| = |V_{TH}| + \sqrt{\frac{2I_D}{\mu C_{ox}(W/L)}} \tag{F.1}$$

where V_{TH} is the threshold voltage, I_D is the drain current, W/L is the width to length ratio and μC_{ox} is the product of the carrier mobility and oxide capacitance. To calculate the maximum forward voltage drop, the drain current is the peak current experienced through the transistor.

F.1.2.1 Design Approach

In a single cycle of the input signal, transistors in the rectifier go through several operating regions. Due to large signal diode operation, the rectifier is strongly non-linear. For this reason, estimation and simulation is used for design. The rectifier input resistance is estimated by,

$$R_{in} = V_{in_{rms}}^2 / P_{in} \tag{F.2}$$

where P_{in} is the input power of the voltage source V_{in}. The power, P_{in}, is obtained by simulation using discrete samples of the instantaineous voltage and current input

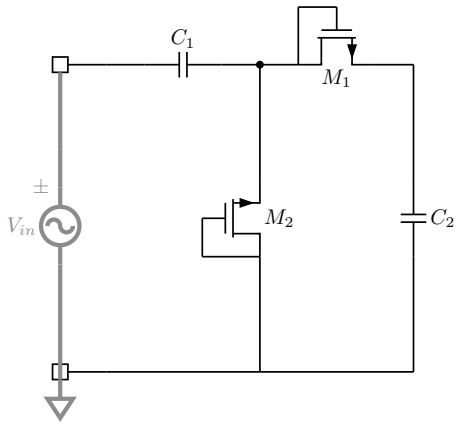

Figure F.1: Single stage voltage multiplying rectifier, commonly called a voltage doubler.

as follows,

$$P_{in} = \frac{1}{N}\sum_{1}^{N} V_{in}(n) \times I_{in}(n). \tag{F.3}$$

The rectifier efficiency, η, is given by the ratio of the power consumed at the load to the power consumed in the rectifying transistors and the load,

$$\eta = P_{load}/(P_{load} + P_{M_1} + P_{M_2}). \tag{F.4}$$

The power in the rectifying transistors, $P_{M_{1,2}}$, is obtained by using simulated voltage and current waveforms.

F.1.2.2 Capacitive Loading

The rectifier capacitive input is determined by parasitic capacitance at the active nodes. The active nodes are the input (node 1) and the node connected to both M_1 and M_2 (node 2). Capacitors C_1 and C_2 do not require charge/discharge cycling after the initial startup transient; both capacitors are AC short circuits and thus do not represent capacitive loads. The rectifier input capacitance can be calculated by,

$$C_{in} = C_{p1}|| \left(\frac{C_{p2} + C_1}{C_1 C_{p2}}\right)^{-1} \tag{F.5}$$

where

$$\left(\frac{C_{p2} + C_1}{C_1 C_{p2}}\right)^{-1} \rightarrow C_{p2}, \tag{F.6}$$

and,

$$C_{in} \approx C_{p1}||C_{p2}. \tag{F.7}$$

From this, the rectifier input capacitance is formed by both top and bottom plate parasitic capacitance as well as transistor parasitics at node 2.

There are several trade offs in the capacitor sizing. Capacitor C_1 acts as a charge pump capacitor and a large ratio of C_1/C_2 decreases the start up transient. To minimize the output voltage ripple, a large C_2 is desired. The size of C_1 is determined in the lower limit by the allowable transient time for startup and in the upper limit by the size of the parasitic capacitance which ultimately loads the inductor. The rectifier input capacitance thus loads the inductor coil and limits the frequency of operation. The rectifier capacitance at node 2 also impacts the total output voltage of the rectifier and the power delivered to the load. The total real power utilized by the load depends on the load voltage, which is impacted by the capacitive divider as follows,

$$V_2 = V_{in}\frac{C_1}{C_1 + C_{p2}}. \tag{F.8}$$

F.1.2.3 Design with Low V_{th} Transistors

While low threshold transistors can operate with a low voltage, they suffer from relatively large leakage current during the operation phase when the transistor is configured as a reverse-biased diode. Transistor size impacts leakage current during the reverse biased phase and impacts transistor on-resistance during the forward-biased phase. Larger transistors offer decreased on-resistance and reduced forward-bias voltage drop, but suffer from an increased reversed-biased leakage current.

Efficient rectifier design with low threshold voltage transistors limits leakage

current and improves rectifier efficiency with a small transistor [129]. As a consequence, the the forward voltage drop is increased and the voltage sensitivity is decreased. The optimal energy efficiency operation of a voltage multiplying rectifier is one with a large forward voltage drop per stage, and with an increased number of stages to provide the required output voltage.

A single-stage voltage-doubler rectifier in the IBM 0.13μm technology has been simulated. Figure F.2 shows the input resistance, efficiency and output voltage versus the transistor W/L ratio at a supply current of 0.5 μA and an input voltage of 200 mV. Due to the high reverse-bias leakage current, rectifier efficiency peaks at a low W/L ratio where the rectifier operates with less than full output voltage as show in Fig. F.2. The input resistance is also a decreasing function of the W/L ratio as shown in Fig. F.3. In addition to transistor sizing, the efficiency is also affected by the input voltage and the output load current. Higher order multipliers can be created by increasing the number of stages. As each stage appears in parallel, the input resistance of higher order multiplier structures is reduced accordingly.

F.2 Holding Capactance

The highest capacitive density found in CMOS technology is the gate oxide. However, a gate capacitor functions well only if the underlying channel is under strong accumulation; if the channel is depleted this lesser series capacitance will combine to reduce the total capacitance. For this reason it is advantageous to use low-threshold transistors to achieve strong accumulation for the MOS capacitors with a low (100's of mV) internal supply voltage.

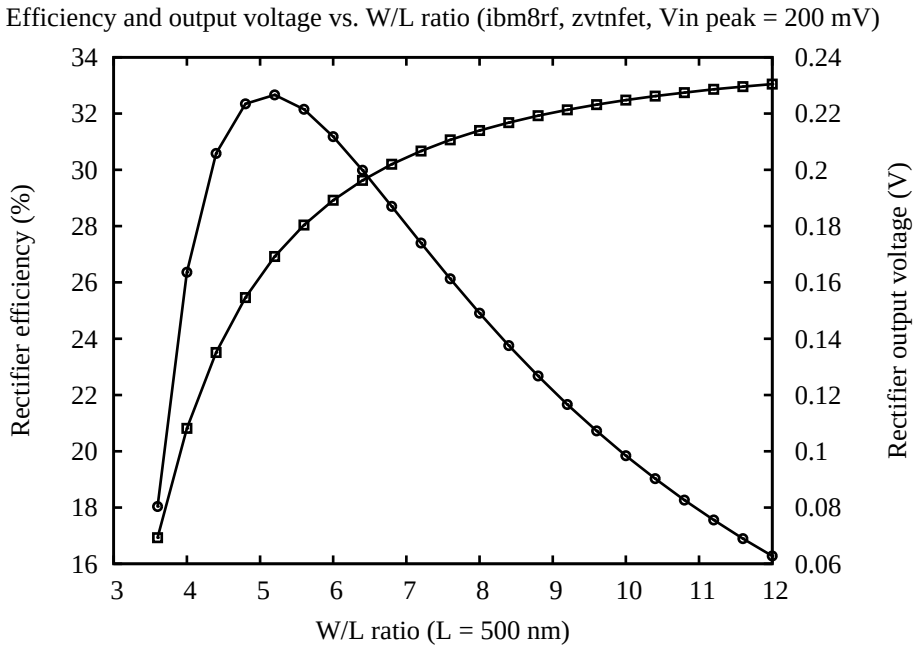

Figure F.2: Efficiency and output voltage versus transistor size for a single-stage voltage-multiplier rectifier.

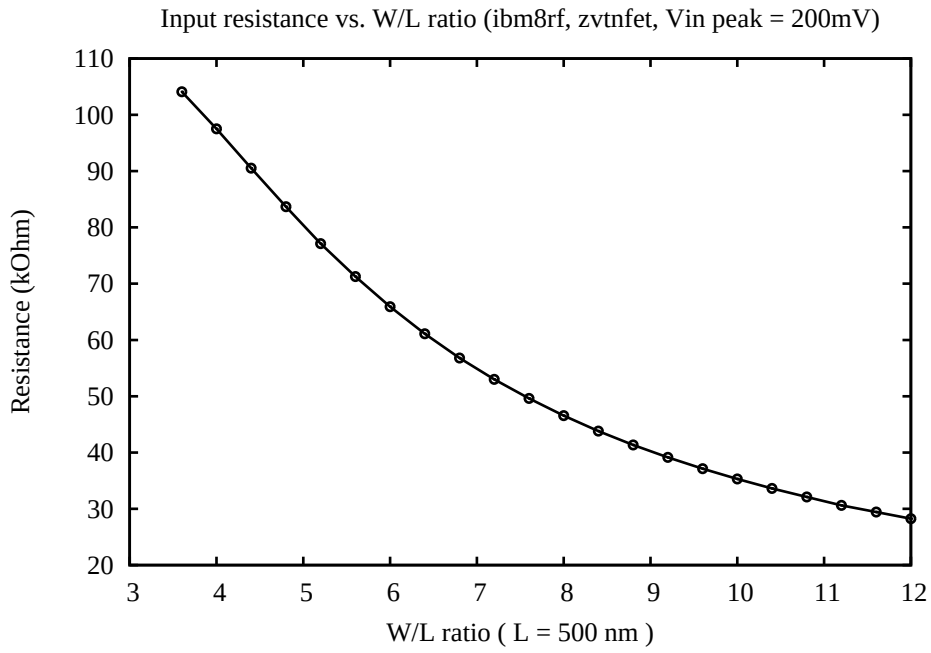

Figure F.3: Input resistance versus transistor size for a single-stage voltage-multiplier rectifier.

A large bypass capacitor was built using the gate oxide of the MOS transistor in TSMC 0.18μm mixed-signal RF technology. To obtain a fully inverted channel at low voltage, native transistors were used. Because MOS gate capacitors are slow, due to delay in charge arriving to the bottom plate, a faster capacitive structure will additionally be used in parallel.

A unit-cell consisting of two transistor transistors sized with W/L = 50/20 was built. To form the large capacitor, a total of 210 unit cells were placed in parallel. Due to the changing channel accumulation, the capacitance varied with gate bias. Unit cell capacitance simulated at nominal process varied from 9.9 – 13.8 pF for a gate voltage ranging from 50 – 200 mV. Thus, with at least a 50 mV gate voltage for accumulation, total gate capacitance of 210 cells was expected to be greater than 2.0 nF.

For bench measurement, a capacitance formed by 210 unit cell capacitors was placed in series with a nominal 560 kΩ resistor to form a single pole low pass filter driven with a function generator. The function generator provided a 300 mV dc offset voltage to accumulate the channel and a 50 mV ac signal to determine the frequency response of the construction. The 3-dB attenuation occurred at 420 Hz from which the total capacitance was determined to be 670 pF. The discrepancy between the measured value of 670 pF and the estimated value of $\geq$ 2.0 nF was not resolved.

APPENDIX G

TEST SETUP

This section describes the test board AS1TB1 and the test setup for voltage mode testing of AS1 and pressure mode testing of AS1-MEMS. The toplevel design of AS1TB1 is shown in Figure G.2.

The analog and digital functions of the AS1TB1 board, together with the respective ground planes, are split across the board. The digital circuitry generates an attenuated four phase non-overlapping clock and provides DUT output signal gain and buffering. The analog circuitry provides power supply and input signals to AS1 and AS1-MEMS. Both the AS1 and the AS1-MEMS are tested in 40-pin DIP package placed at the DUT location on the board AS1TB1. Input signals to the DUT include the modulation reference voltage, V_{ref} (optionally jumpered to V_{DD}) the common-mode voltage, V_{CM}, and the reference voltages to capacitors C_1 and C_2, V_{refC1} and V_{refC2} respectively.

The DUT has switched capacitor inputs that require anti-alias filtering. AS1TB1 implements anti-alias filters on V_{ref}, V_{refC1}, V_{refC2}, V_{CM} and V_{DD} when optionally switched in at the reference location. The anti-alias filter is the same at all inputs and is comprised of a single-pole low-pass filter using R_f = 200 Ω and C_f = 3.4 μF comprised of a 3.3 μF tantalum and 0.1μF ceramic bypass capacitors located at the DUT input pins. The filter provides f_{3dB} = 234 Hz and roughly 20 dB attenuation at 2300 Hz.

Power is measured at the AS1TB1 board. To obtain current into the DUT, a Keithley 6487 Picoammeter is placed in series with power supply voltages V_{DD} and V_{DDCOMP} using jumpers on the AS1TB1 board. Each current measurement used an average of 100 readings from the 6487 Picoammeter.

The single-bit digital output from AS1TB1 is brought out to an Arduino Uno microcontroller board and then transferred to a computer. Code for the Arduino sketch is in Section G.1. The Arduino standard code was not capable of handling the required data exchange rate. The Arduino code was written to implement a port read and Python Pyserial was used to serial port support transfer from the Uno to the computer. The Pyserial interface code is in Section G.2.

In order to minimize the time between clock phases, the four phase clock circuitry used an input signal with runt pulses to independently control clock phase duration and time between clock cycles. The runt pulses were obtained from a positive edge detector. The runt pulse width kept at approximately 1–2 μs throughout testing. The clock phases are shown in Fig. G.1.

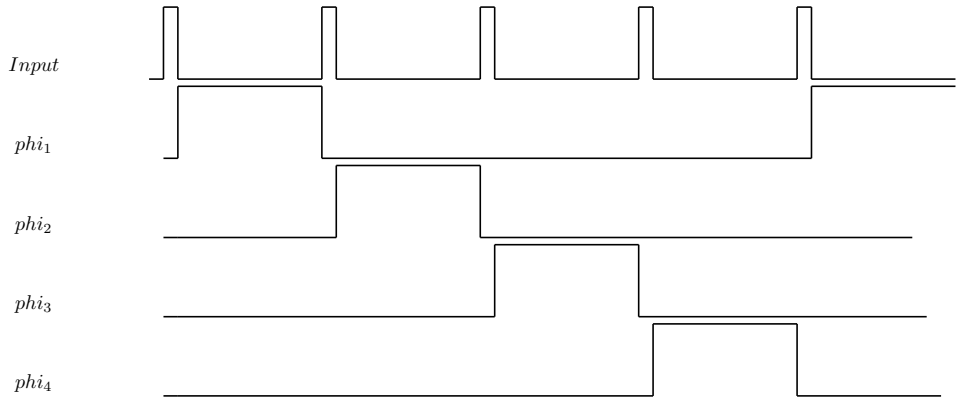

Figure G.1: Clock signals on test board AS1TB1 are generated from the output of a positive edge detector.

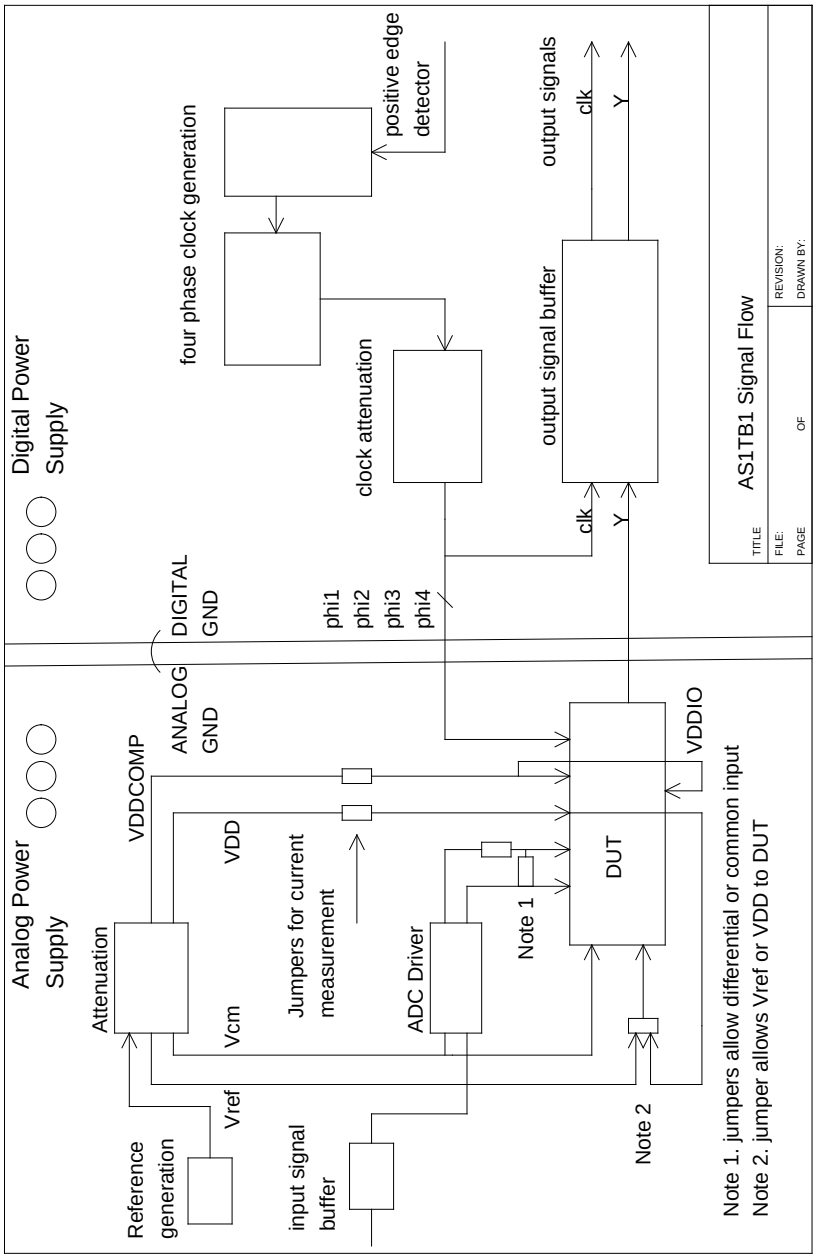

Figure G.2: Test board AS1TB1 toplevel functional schematic showing both analog and digital circuitry blocks.

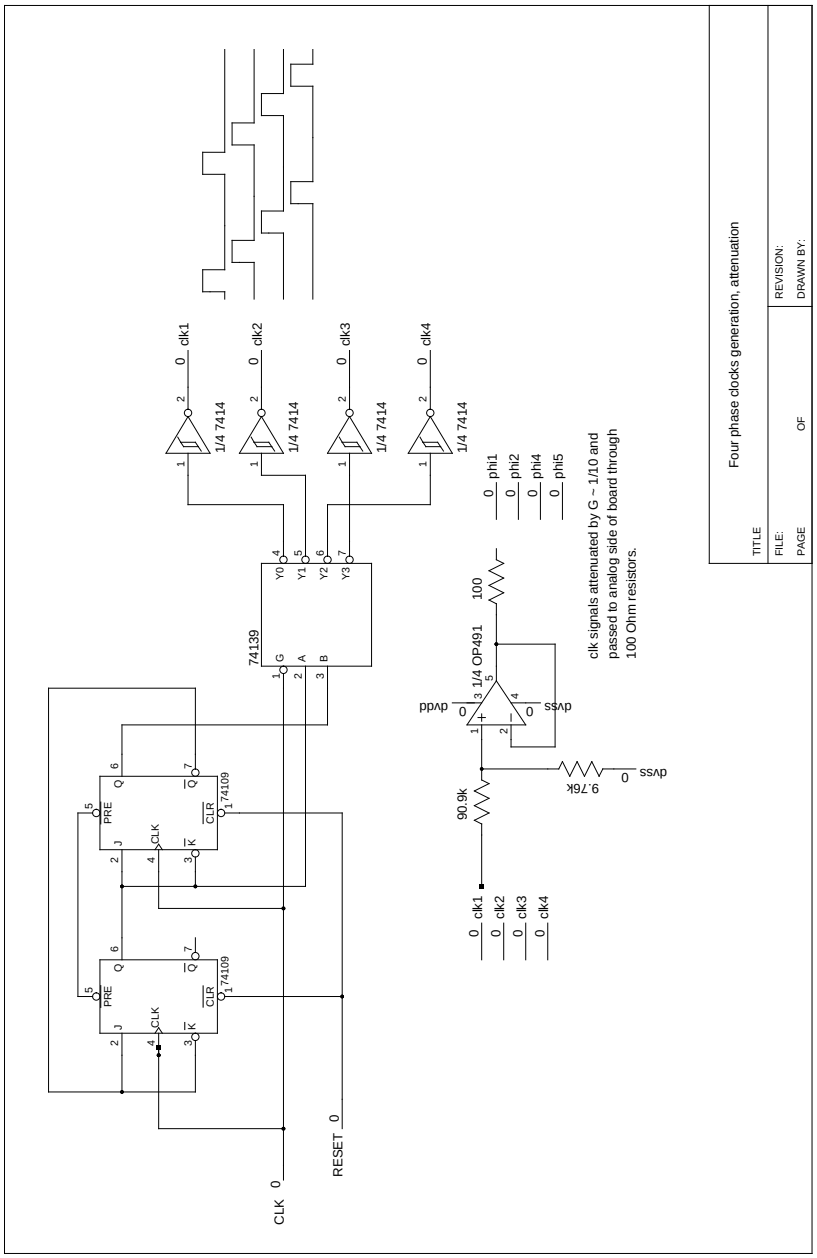

Figure G.3: Test board AS1TB1 four phase clock generation. To avoid long delays between the phases, an edge detect signal was provided to the circuitry rather than a clock waveform. The edge detect allowed rough control (μs) of the delay between phases, and accurate control of the clock phase width.

G.1 Arduio Sketch

```
/*

This code both gets Temperature and Pressure readings, writes to
the serial port then obtains the data and sample clk at the rate to the
the modulator clk. The program has an interrupt on pin 2 (interrupt 0),
reads the input at pins 4, 6 and then writes to the serial port (USB)

*/
#include <Wire.h>
#define BMP085_ADDRESS 0x77  // I2C address of BMP085
#include <PinChangeInt.h>
// end of file definition
#define CTRL(x) ('x' & 0x1F)

// Variables for Data Collection

  volatile boolean dataready = false;
  volatile boolean overwrerror = false;
  boolean errorswritten=false;
  volatile int my_data;
  long datacount=0;
  int errorcnt=0;
```

```
  int datacomp=0;
  long samplelength=1000000;
  int bitmask=B00010000;
  int bitmaskshift=4;

unsigned long time;
// Variables for Pressure and Data Collection
const unsigned char OSS = 3;  // oversampling setting
// Calibration values
  int ac1;
  int ac2;
  int ac3;
  unsigned int ac4;
  unsigned int ac5;
  unsigned int ac6;
  int b1;
  int b2;
  int mb;
  int mc;
  int md;

// variables for reading dc input voltage level
// b5 is calculated in bmp085GetTemperature(...),
// this variable is also used in bmp085GetPressure(...)
// so ...Temperature(...) must be called
// before ...Pressure(...).
```

```
  long b5;
  short temperature;
  float temp;
  long pressure;
  float p;
  int HEADER=1;
  int dcendfile=1;

// configure pin 2 (interrupt) as an input
// and enable the internal pull-up resistor

void setup(){
  Serial.begin(230400);
  Wire.begin();
  bmp085Calibration();
  pinMode(2, INPUT_PULLUP);
  attachInterrupt(0, CollectBits, FALLING);
}

// The main loop sequence:
// a) get dc input
// b) get the PT while disabling the interrupt, then
// c) get the PORTD byte through the ISR
// d) write the port data to serial
// e) write the error count to file
// f) write PT again while disabling the interrupt
```

```
void loop()
{
// go into PT program if first time through loop
  if (HEADER)
  {
    detachInterrupt(0);
    HEADER=0;
    startbmp085ReadUT();
    Serial.print("%Time at HEADER: ");
    time = millis();
    Serial.println(time);
//  reconnect interrupt, clean all errors and flags
    attachInterrupt(0, CollectBits, FALLING);
    dataready=false;
    overwrerror=false;
    errorcnt=0;
  }
// if data is ready, write to serial port
  if ( (dataready) && (datacount < samplelength))
  {
    dataready = false;
    datacount++;
    Serial.println(my_data & bitmask);
  }
  if ((overwrerror) && (datacount < samplelength))
```

```
  {
    overwrerror=false;
    errorcnt++;
  }
  if ((datacount == samplelength) && (!errorswritten))
// detach interrupt
// print time
// print errors
// get finished Temp Read
  {
    detachInterrupt(0);
    Serial.print("%Time at end of data collection: ");
    time = millis();
    Serial.println(time);
    Serial.print("%errors");
    Serial.println(errorcnt);
    errorswritten=true;
    temperature = bmp085GetTemperature(finishbmp085ReadUT());
    temp = (float) temperature/10;
    Serial.print("%Temperature,");
    Serial.print(temp, 1);
    Serial.println(",*0.1 deg C");
    for (int m=0; m < 11; m++)
    {
      pressure = bmp085GetPressure(bmp085ReadUP());
      Serial.print("%END Pressure,");
```

```
      p=pressure*(0.00750);
      Serial.print(p, 2);
      Serial.println(",mmHg");
    }
    Serial.print("%ENDEND");
  }
}

// Interrupt service routine (ISR)
// read the data and clk and set flags

void CollectBits()
{
  if (dataready){overwrerror=true;};
  dataready=true;
  my_data=PIND;
}

// Code for Pressure Sensor
/* BMP085 Extended Example Code
  by: Jim Lindblom
  SparkFun Electronics
  date: 1/18/11
  license: CC BY-SA v3.0 - http://creativecommons.org/
  licenses/by-sa/3.0/
```

```
  Get pressure and temp. from the BMP085 and calculate
  altitude. Serial.print at 9600 baud to serial monitor.

  Update (7/19/11): I've heard folks may be encountering
  issues with this code, who're running an Arduino at 8MHz.
  On Arduino Pro 3.3V/8MHz, or the like, you may need to
  increase some of the delays in the bmp085ReadUP and
  bmp085ReadUT functions.
*/

// Stores bmp085's calibration values into global var
// Cal values required to calculate temp and pressure
// Should be called at the beginning of the program

void bmp085Calibration()
{
  ac1 = bmp085ReadInt(0xAA);
  ac2 = bmp085ReadInt(0xAC);
  ac3 = bmp085ReadInt(0xAE);
  ac4 = bmp085ReadInt(0xB0);
  ac5 = bmp085ReadInt(0xB2);
  ac6 = bmp085ReadInt(0xB4);
  b1 = bmp085ReadInt(0xB6);
  b2 = bmp085ReadInt(0xB8);
  mb = bmp085ReadInt(0xBA);
  mc = bmp085ReadInt(0xBC);
```

```
  md = bmp085ReadInt(0xBE);
}

// Calculate temperature given ut.
// Value returned will be in units of 0.1 deg C

short bmp085GetTemperature(unsigned int ut)
{
  long x1, x2;
  x1 = (((long)ut - (long)ac6)*(long)ac5) >> 15;
  x2 = ((long)mc << 11)/(x1 + md);
  b5 = x1 + x2;
  return ((b5 + 8)>>4);
}

// Calculate pressure given up
// calibration values must be known
// b5 is also required so bmp085GetTemperature(...)
// must be called first.
// Value returned will be pressure in units of Pa.
long bmp085GetPressure(unsigned long up)
{
  long x1, x2, x3, b3, b6, p;
  unsigned long b4, b7;
  b6 = b5 - 4000;
  // Calculate B3
```

```
  x1 = (b2 * (b6 * b6)>>12)>>11;
  x2 = (ac2 * b6)>>11;
  x3 = x1 + x2;
  b3 = (((((long)ac1)*4 + x3)<<OSS) + 2)>>2;
  // Calculate B4
  x1 = (ac3 * b6)>>13;
  x2 = (b1 * ((b6 * b6)>>12))>>16;
  x3 = ((x1 + x2) + 2)>>2;
  b4 = (ac4 * (unsigned long)(x3 + 32768))>>15;
  b7 = ((unsigned long)(up - b3) * (50000>>OSS));
  if (b7 < 0x80000000)
    p = (b7<<1)/b4;
  else
    p = (b7/b4)<<1;
  x1 = (p>>8) * (p>>8);
  x1 = (x1 * 3038)>>16;
  x2 = (-7357 * p)>>16;
  p += (x1 + x2 + 3791)>>4;
  return p;
}

// Read 1 byte from the BMP085 at 'address'
char bmp085Read(unsigned char address)
{
  unsigned char data;
  Wire.beginTransmission(BMP085_ADDRESS);
```

```
  Wire.write(address);
  Wire.endTransmission();
  Wire.requestFrom(BMP085_ADDRESS, 1);
  while(!Wire.available())
    ;
  return Wire.read();
}

// Read 2 bytes from the BMP085
// First byte will be from 'address'
// Second byte will be from 'address'+1
int bmp085ReadInt(unsigned char address)
{
  unsigned char msb, lsb;

  Wire.beginTransmission(BMP085_ADDRESS);
  Wire.write(address);
  Wire.endTransmission();
  Wire.requestFrom(BMP085_ADDRESS, 2);
  while(Wire.available()<2)
    ;
  msb = Wire.read();
  lsb = Wire.read();

  return (int) msb<<8 | lsb;
}
```

```
// Read the uncompensated temperature value
unsigned int bmp085ReadUT()
{
  unsigned int ut;

  // Write 0x2E into Register 0xF4
  // This requests a temperature reading
  Wire.beginTransmission(BMP085_ADDRESS);
  Wire.write(0xF4);
  Wire.write(0x2E);
  Wire.endTransmission();

  delay(5000);

  // Read two bytes from registers 0xF6 and 0xF7
  ut = bmp085ReadInt(0xF6);
  return ut;
}

unsigned int startbmp085ReadUT()
{

  // Write 0x2E into Register 0xF4
  // This requests a temperature reading
  Wire.beginTransmission(BMP085_ADDRESS);
```

```
  Wire.write(0xF4);
  Wire.write(0x2E);
  Wire.endTransmission();

  // Wait at least 4.5ms
  // delay occurs while data is collected
}

unsigned int finishbmp085ReadUT()
{
  unsigned int ut;
  // delay has occurred
  // Read two bytes from registers 0xF6 and 0xF7
  ut = bmp085ReadInt(0xF6);
  return ut;
}

// Read the uncompensated pressure value
unsigned long bmp085ReadUP()
{
  unsigned char msb, lsb, xlsb;
  unsigned long up = 0;

  // Write 0x34+(OSS<<6) into register 0xF4
  // Request a pressure reading w/ oversampling setting
  Wire.beginTransmission(BMP085_ADDRESS);
```

```
  Wire.write(0xF4);
  Wire.write(0x34 + (OSS<<6));
  Wire.endTransmission();

  // Wait for conversion, delay time dependent on OSS
  delay(2 + (3<<OSS));

  // Read register 0xF6 (MSB), 0xF7 (LSB), and 0xF8 (XLSB)
  Wire.beginTransmission(BMP085_ADDRESS);
  Wire.write(0xF6);
  Wire.endTransmission();
  Wire.requestFrom(BMP085_ADDRESS, 3);
  while(Wire.available() < 3)
    ;
  msb = Wire.read();
  lsb = Wire.read();
  xlsb = Wire.read();
up = (((unsigned long) msb << 16)|((unsigned long) lsb << 8)|
(unsigned long) xlsb) >> (8-OSS);
return up;
}
```

G.2 Pyserial Code

```
 #! /usr/bin/env python
```

```
import serial
import datetime

now=datetime.datetime.now()

f=open('./f1', 'w')
f.write('%')
f.write(str(now.ctime()))
f.write('\n')

print "Starting serial read..."
print now.ctime()

ser = serial.Serial('/dev/ttyACM0', 230400, timeout=1)

finished = 0;
while ( finished == 0):
        line = ser.readline()
        f.write(line)
        if ( '%ENDEND' in line ):
                finished = 1

print "Finished collecting and writing ..."
now=datetime.datetime.now()
print now.ctime()
```

```
ser.close()

f.close()
```

APPENDIX H

SPECTRAL ANALYSIS

The purpose of this appendix is to describe the spectral analysis procedures used to analyse the wide-band $\Delta\Sigma$ single-bit output for SNR performance and eperimental noise floor. While the test conditions were varied was varied during experimentation, this section describes typical operating conditions.

H.1 SNR Calculations

The typical system clock rate was f_{sys} = 6400 Hz giving a modulator clock rate of f_{sys}/4 = f_s = 1600 Hz. The $\Sigma\Delta$ single-bit output was collected at the rate f_s and stored in a computer for analysis. The length of a typical collected data set was 150k single-bit data samples. A typical FFT analysis length of N=131072 was used, sampling approximately 82 input cycles of the 4 Hz input signal. Prior to

spectral analysis, the $\Sigma\Delta$ data stream was converted from logical values (01010) to a modulated voltage stream ($\pm V_{DD}$) and offset was removed (-V_{DD}/2). Because the signal was incoherently sampled, a Hann window was used on the data prior to calculating the FFT and the power spectral density.

In favor of obtaining as much frequency resolution as possible from the FFT sample length, periodogram averaging was not typically used. The typical frequency resolution of the FFT was f_s/N = 0.01 Hz per FFT bin. Within the 0-25 Hz bandwidth, the FFT length of N=131072 provides a total of 2048 bins. A high number of bins reduces the variance on the SNR measurement[1]; application of at least N = 64$\times$OSR provides a standard deviation of less than 1 dB using a standard SNR estimate calculations [125]. The typical OSR of 32 obtained for f_s = 1600 Hz in this work led to N = 2048 for the desired FFT frequency resolution. However, as the following paragraph explains, the SNR calculation method for this work did not use all the in-band bins to calculate the noise.

In this work the input signal was close to DC (4 Hz) and incoherently sampled. Under these conditions, the PSD may be influenced by offset and by spectral smearing of the input signal. By using the FFT content away from the input signal and away from DC, the SNR calculation in this work made an *estimate* of the average noise floor and then used the estimate to calculate in-band noise.

The SNR was calculated as follows. The FFT was calculated using sine-wave scaling and the square magnitude was calculated to provide the PSD. The sine-wave-scaled PSD is used to calculated the spectral content floor between the 2nd and 6th order harmonics of the input (from 8 Hz to 24 Hz) while avoiding content at

[1]Recall that the FFT of a random variable is itself a random variable, and any SNR calculation made from the FFT is subject to variation.

the harmonics themselves. The mean value of the spectral floor is then converted to energy scaling by multiplication with the equivelent factor between sine-wave scaling and energy scaling,

$$M = \frac{FS^2}{16 \times NBW} \tag{H.1}$$

where FS is the full scale input and NBW is the noise bandwidth of the window (details on windows and the two scale factors can be found in [125]). Because the FFT input was scaled to voltage, the use of energy scaling to the FFT output provides voltage spot noise, V_{rms}^2/Hz. An estimate of the total in-band noise power is then obtained by multiplying by the signal bandwidth. The input signal power is obtained direct the sine-wave-scaled PSD by observation of the peak value at the input frequency. The SNR is formed the the ratio of the signal power to noise power. The SNDR is formed by adding the distortion power to the noise prior to forming the ratio; the distortion power is determined from direct reading of sine-wave-scaled PSD peak value at specified harmonic frequencies.

H.2 Noise Floor

While the sine-wave-scaled PSD allows a direct reading of the input signal power at the input frequency, the energy-scaled PSD allows a direct reading of the circuit noise floor. Figure H.1 shows an energy-scaled PSD of the modulated output. In the bandwidth from 0–25 Hz for the single-sided PSD shown, there are 2048/2 FFT bins; 465 bins are used to calculate the single-sided noise floor power estimate between 8–24 Hz. The estimated PSD floor is -40.1 dB or 97 μV^2/Hz (or 0.0098

$V_{rms}^2/\sqrt{Hz}$). Overall, experimental results for the modulator operating with V_{DD} = 500 mV and f_s = 1600 Hz produced average noise floor with values between 110 μV_{rms}^2/Hz (D5)–70 μV_{rms}^2/Hz (D4).

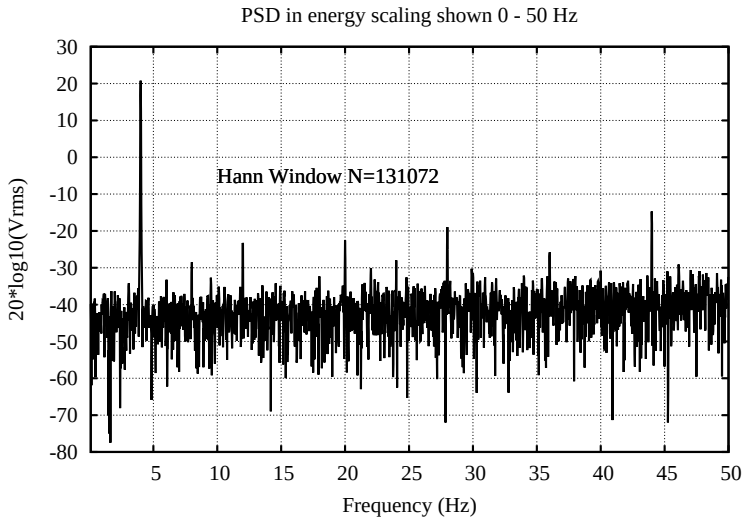

Figure H.1: Energy scaled PSD of the modulated output operating with V_{DD} = 500 mV, f_s = 1600 Hz and a fully-differential input signal of 420 mV. The estimated noise floor, obtained between frequencies 8 to 24 Hz, is -40.1 dB or 97 μV_{rms}^2/Hz.

The noise floor of 70 μV_{rms}^2/Hz for D4 provides a hand calculation of the peak SNR as,

$$SNR_{max} = 20 \times \log_{10}\left(\frac{1000\text{mV}/\sqrt{2}}{\sqrt{25\text{Hz}} \times 8.3\text{mV}/\sqrt{\text{Hz}}}\right) = 24.6\text{dB} \qquad \text{(H.2)}$$

which is consistent with the peak experimental SNR of 23.5 dB.