NOTICE

The quality of this microform is heavily dependent upon the quality of the original thesis submitted for microfilming. Every effort has been made to ensure the highest quality of reproduction possible.

If pages are missing, contact the university which granted the degree.

Some pages may have indistinct print especially if the original pages were typed with a poor typewriter ribbon or if the university sent us an inferior photocopy.

Reproduction in full or in part of this microform is governed by the Canadian Copyright Act, R.S.C. 1970, c. C-30, and subsequent amendments.

AVIS

La qualité de cette microforme dépend grandement de la qualité de la thèse soumise au microfilmage. Nous avons tout fait pour assurer une qualité supérieure de reproduction.

S'il manque des pages, veuillez communiquer avec l'université qui a conféré le grade.

La qualité d'impression de certaines pages peut laisser à désirer, surtout si les pages originales ont été dactylographiées à l'aide d'un ruban usé ou si l'université nous a fait parvenir une photocopie de qualité inférieure.

La reproduction, même partielle, de cette microforme est soumise à la Loi canadienne sur le droit d'auteur, SRC 1970, c. C-30, et ses amendements subséquents.

UNIVERSITY OF ALBERTA

INVESTIGATION OF LATERAL TRANSISTOR STRUCTURES DESIGNED AS MAGNETIC FIELD SENSORS

BY

MY THE DOAN

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND RESEARCH

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF SCIENCE

DEPARTMENT OF ELECTRICAL ENGINEERING

EDMONTON, ALBERTA

SPRING 1990

NOTICE

The quality of this microform is heavily dependent upon the quality of the original thesis submitted for microfilming. Every effort has been made to ensure the highest quality of reproduction possible.

If pages are missing, contact the university which granted the degree.

Some pages may have indistinct print especially if the original pages were typed with a poor typewriter ribbon or if the university sent us an inferior photocopy.

AVIS

La qualité de cette microforme dépend grandement de la qualité de la thèse soumise au microfilmage. Nous avons tout fait pour assurer une qualité supérieure de reproduction.

S'il manque des pages, veuillez communiquer avec l'université qui a conféré le grade.

La qualité d'impression de certaines pages peut laisser à désirer, surtout si les pages originales ont été dactylographiées à l'aide d'un ruban usé ou si l'université nous a fait parvenir une photocopie de qualité inférieure.

ISBN 0-315-60307-0

Canada

UNIVERSITY OF ALBERTA

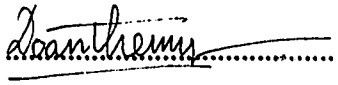
RELEASE FORM

NAME OF AUTHOR: My The Doan

TITLE OF THESIS: Investigation of lateral transistor structures designed as magnetic field sensors.

DEGREE: Master of Science

YEAR THIS DEGREE GRANTED: 1990



10244 - 89 Street

Edmonton, Alberta,

Canada (T5H - 1R1)

Date: March 12, 1990

THE UNIVERSITY OF ALBERTA

FACULTY OF GRADUATE STUDIES AND RESEARCH

The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research for acceptance, a thesis entitled *Investigation of lateral transistor structures designed as magnetic field sensors*, submitted by My The Doan, in partial fulfillment of the requirements for the degree of *Master of Science.*

.....
Supervisor

.....

.....

.....

Date: February 28, 1990

Người Việt vốn là Con Rồng Cháu Tiên

Bài luận án này là để đền đáp một chút ít
công ơn sâu rộng của Cậu Mợ dành cho con.

Cựu Học Sinh Lê Qúi Đôn

ABSTRACT

The experimental analysis of two types of magnetic-field-sensitive lateral magnetotransistor is presented. One device is sensitive to magnetic field applied parallel or perpendicular to the chip surface and is fabricated in CMOS technology. The other device is sensitive to magnetic field applied parallel to the chip surface and is fabricated in bipolar technology. For each device, the influence of operating conditions on sensitivity is investigated and analyzed. Measurement results for both devices indicate: 1) carrier deflection appears to be the dominant mechanism of magnetic operation, 2) the sensitivity increases with the substrate voltage, and 3) the sensitivity decreases when high injection level has been reached. For the CMOS device, three additional experiments are carried out in order to investigate 1) the role of the surface effects on sensitivity, 2) the device's signal to noise ratio (or resolution), and 3) the noise correlation between the collector voltages of differential structures. The surface effects are controlled by applying potential on the gate contact. For $V_G < 0$, the sensitivity improves by 10 %; for $V_G > 0$, the sensitivity decreases drastically. The resolution of the CMOS device is in the range of 10 μT at f = 1 kHz. No correlation between the two collector noise voltages is observed. For the bipolar device, the role of the n^+-buried layer on the electrical and magnetic characteristics of the device is also studied. With the presence of the n^+-buried layer, the influence of the substrate voltage on sensitivity becomes insignificant.

ACKNOWLEDGEMENT

I would like to extend my gratitude to Dr. Ljubisa Ristic' , my supervisor, for setting the direction of my research work and for providing continuous guidance and motivation throughout the last two years.

I would also like to thank my friend Dr. T. Smy, who in countless discussions have helped me to clarify my ideas about magnetic field sensors. Sincere appreciation is due to the other two members of the examining committee, Dr. I. Filanovsky and Dr. W. Allegretto, for their invaluable time spent on this thesis and their suggestions. I would like to thank Ash, Dave, Glen, Graham, Ken, Kris, and Tien for their technical support as well as their encouragement. The support that I have received from my familly is always appreciated.

Finally, I also sincerely thank the Alberta Microelectronic Centre for its financial assistance.

TABLE OF CONTENTS

List of Tables

List of Figures

List of Symbols

Symbol	Name	Unit
$\mathbf{B}$	Magnetic induction vector	tesla
C	capacitance	farad
D_n	Electron diffusion coefficient	m^2/s
D_p	Hole diffusion coefficient	m^2/s
$\mathbf{E}$	Electric field vector	volts/meter
E_x	Electric field vector in x direction	volts/meter
E_y	Electric field vector in y direction	volts/meter
E_{ay}	Accelerating electric field in y direction	volts/meter
f	Frequency	Hz
Δf	Frequency bandwith	Hz
$\mathbf{F}$	Lorentz force	newton
g_m	Transconductance	amp/volt
h_{fe}	AC current gain	-
H_{FE}	DC current gain	-
$i_n(t)$	Current noise	amp
I_C, I_B, I_E, I_S	Collector, base, emitter, and substrate current	amp
I_{C0}	Collector current at zero magnetic field	amp
I_{Csat}	Collector current at saturation	amp
ΔI_C	Collector current change due to a magnetic field	amp
I_D	Drain current	amp
I_r	Current through p^+ stripes	amp
I_{Bc}	Critical base current	amp
$\vec{J}_n$	Electron current density vector	amp/m^2
J_{nx}	Electron current density in x direction	amp/m^2

J_{ny}	Electron current density in y direction	amp/m^2
J_{n0}	Electron current density at zero magnetic field	amp/m^2
k	Boltzmann's constant	J/K
K	Noise constant for a particular device	-
m	Ideality factor	-
N_A, N_D	Acceptor and donor doping concentration	m^{-3}
NF	Noise figure	dB
n	Electron carrier concentration	m^{-3}
p	Hole carrier concentration	m^{-3}
P(t)	Noise average power	watt
q	Elementary electronic charge	coulomb
r_H	Hall scattering coefficient	-
r_{bb}	Base spreading resistance	ohm
r_{be}	Base emitter resistance	ohm
R_H	Hall coefficient	$m^{-3}coulombs^{-1}$
S_a	Absolute sensitivity	amp/tesla
$S_i(w)$	Power spectral density of current noise	amp^2/Hz
S_r	Relative sensitivity	% / tesla
S_{rf}	Relative sensitivity when gate is floating	% / tesla
S_{rg}	Relative sensitivity when gate is connected	% / tesla
$S_i(w)$	Power spectral density of voltage noise	V^2/Hz
S/N	Signal to noise ratio	-
T	Temperature	Kevin
v	Velocity vector	meter/sec
V_{bi}	Built in voltage	volts
V_C, V_S, V_B	Collector, substrate, base voltage	volts
V_G	Gate voltage	volts

V_H	Hall voltage	volts
$v_n(t)$	Voltage noise	volts
$V_n(w)$	Fourier transform of $v_n(t)$	volt-sec
$V_n^*(w)$	Complex conjugate of $V_n(w)$	volt-sec
V_r	p^+ stripe voltage	volts
V_{rc}	Critical p^+ stripe voltage	volts
V_{Sc}	Critical substrate voltage	volts
V_T	Thermal voltage	volts
V_{TH}	Threshold voltage	volts
w	Angular frequency	Hz
W_B	base width	meter
W_{eff}	Effective width of lateral electron flow	meter
ε	Permittivity	$C^2/N\text{-}m^2$
τ	Relaxation time	second
μ_n	Electron drift mobility	$meter^2/volt\text{-}sec$
μ_p	Hole drift mobility	$meter^2/volt\text{-}sec$
μ_n^*	Electron Hall mobility	$meter^2/volt\text{-}sec$
μ_p^*	Hole drift mobility	$meter^2/volt\text{-}sec$
μ_0	Magnetic permeability of free space	amp/meter-tesla
μ_r	Relative magnetic permeability	amp/meter-tesla
σ_n	Electrical conductivity in n region	$(\Omega - m)^{-1}$
σ_p	Electrical conductivity in p region	$(\Omega - m)^{-1}$
θ_H	Hall angle	radians
ρ	Resistivity	volt-meter/amp

1. INTRODUCTION

All silicon magnetic field sensors (MFSs) that can be batch fabricated in standard IC technologies such as bipolar or CMOS technology can be classified into four categories: Hall cell devices (HCDs), MOSFET magnetic field sensors (MAGFETs), Magnetodiodes (MDs), and Magnetotransistors (MTs) [1,2]. All these devices, however, are based on the action of the Lorentz force, $\mathbf{F} = q\mathbf{v} \times \mathbf{B}$, acting on the moving charge carriers in the semiconductive slab. Here q represents the elementary charge, v is the velocity with which the charge is moving, and **B** is the magnetic induction.

The HCDs are the simplest, oldest, and best understood MFSs. They, however, generally have low sensitivity and high offset. A HCD is usually just a rectangular slab of Si or GaAs material with four ohmic contacts; two contacts are for driving current and two are for sensing the Hall voltage.

MAGFETs refers to MFSs based on the MOSFET operation. The inversion layer of the MOSFET serves as a Hall plate. Among MAGFETs, the triple drain device is the most sensitive one. Both HCDs and MAGFETs have their output voltages varying linearly with respect to the applied magnetic field.

Magnetodiodes have high relative magnetic sensitivity but, unfortunately, their output voltage or current varies nonlinearly with respect to B. This makes them more expensive for practical applications because of the need of more conditioning circuits to process their output signals. The crucial requirements for MD operation are two different recombination rates at the top surface and at the bottom surface of a slab, the slab geometry, and high injection current.

The most recent and most promising MFSs are the magnetotransistors. The MT is based on bipolar transistor action. The MT is used in common base or common emitter configurations, and the change in collector currents due to the

action of the Lorentz force is used to measure the strength of the applied B. For practical purposes, most MTs are designed as differential structures, i.e. they have at least 2 collectors. There are also structures with more than 2 collectors which are capable of detecting two and three components of the magnetic field vector simultaneously [3,4]. Moreover, MTs have the highest sensitivity among all silicon based MFSs. For example, the suppressed sidewall injection magnetotransistor (SSIMT) has a relative sensitivity of up to 3000 %/T [5].

At the present, MTs are realized in both standard bipolar and CMOS technologies. MTs can also be integrated with circuitry on the same chip, for example, in an angular displacement transducer [6], or in a Magneto-Operational Amplifier (MOP) [7]. These inherent advantages coupled with our access to 5μ and 3μ CMOS processes offered by Northern Telecom through CMC are the reasons we focus our research on MTs which are fabricated in standard CMOS technology.

1.1 BASIC PARAMETERS OF A SENSOR

A sensor in general is an input stage of a process control system. Its output signal is then processed by the next stage which is called the signal processing stage. This stage may include an amplifier, some compensation circuits to minimize the influence of temperature and offset, and an A/D converter. For successful functioning of the system it is crucial that the sensor is characterized in terms of the following parameters: sensitivity, signal to noise ratio (magnetic field resolution), frequency response, linearity, and offset. So we will briefly discuss in the following some of the basic parameters relevant to sensors.

For sensors, the first figure of merit to be considered is the sensitivity. The sensitivity figure can be defined either in absolute or in relative terms. The

absolute sensitivity is defined as

$$S_a = \left.\frac{\partial S}{\partial M}\right|_{Q_i=\text{const}} \tag{1.1}$$

where S represents the output signal, M is the measurand, and Q_i is a set of different parameters having a constant value.

Whereas, the relative sensitivity is defined as

$$S_r = \frac{1}{S_o}\left.\frac{\partial S}{\partial M}\right|_{Q_i=\text{const}} \tag{1.2}$$

where S_o is the value of the output signal different than zero when M=0.

An analysis of the device noise is meaningful because noise figure provides more information regarding the application range of the device as opposed to just the figure of sensitivity on its own. A commonly used parameter for noise characterization is the equivalent input noise spectral density

$$S_{n,in} = \frac{S_{n,out}(f)}{S_a^2} \tag{1.3}$$

where $S_{n,out}$ (f) is the noise spectral density at the sensor output, and S_a is the absolute sensitivity.

Nonlinearity is defined as

$$NL = \frac{S - S_l}{S_l} \times 100\ (\%) \tag{1.4}$$

where S is the output signal, and S_l is the best linear fit of the output signal. The parameter NL is applicable only if the output signal should have linear dependence on the measurand.

Offset is the signal at the output of the sensor in the absence of the measurand. Offset is usually the result of mask misalignment, and of mechanical stress introduced while bonding. Offset characterization is important because the signal generated from offset is indistinguishable from the useful signal in static and low frequency measurements. In other words, offset limits the resolution of the measurand. The offset is characterized as

$$M_e = \frac{S_{off}}{S_a} \qquad 1.5$$

where M_e is the equivalent value of the measurand, and S_{off} denotes the output offset signal.

1.2 SCOPE OF THE WORK

In this work, we focus our investigation on lateral magnetotransistors, and in particular the device that can detect B which is either perpendicular or parallel to the chip surface. It is important to understand the operation of this device since it can serve as a basis for understanding multidimensional structures. The device can be used either in single ended mode or in differential mode. In addition to the usual device characterization, an extensive investigation of the influence of different biasing conditions on the magnetic sensitivity of the device has been carried out.

Besides the sensitivity characterization, we investigate the noise of LMT structures. There are basically 3 reasons for this. First of all, these LMT structures are unconventional, i.e. they have low current gain, $\beta < 1$, therefore their noise may not be properly modelled using models derived for conventional high

gain transistors. Second, since the ultimate goal is to integrate the sensor with signal processing electronics, it is necessary to determine the device operating conditions for optimum signal to noise (S/N) ratio. Third, there is an open question about the collector noise correlation in differential structures. We hope that our investigation will provide some answers.

It is well known that surface effects are important in the operation of semiconductor devices, but so far there have been no studies on the influence of surface effects on LMT characteristics. Hence, we will also analyze this problem.

The final goal of this work is to investigate LMT structures fabricated in bipolar technology. So far, bipolar technology has been used mainly to make VMTs, and there is no reported work on LMTs fabricated in standard bipolar process.

In Chapter 2, the history of MTs' development is recapitulated, from the early Ge bipolar transistor to the more sophisticated SSIMT. The unique features in design and the important theories related to the operation of different versions of MT are highlighted. Here, we also discuss why MTs are classified into vertical magnetotransistors (VMTs) and lateral magnetotransistors (LMTs).

In Chapter 3, the basic structure and operation of a LMT structure sensitive to the magnetic field applied either parallel or perpendicular to the chip surface are described. For example, we will discuss how an additional P^+ stripe surrounding the emitter on the 3 sides of the emitter will shape the flow path of the injected electrons. The influence of different operating conditions on the device characteristics such as the base current I_B, the substrate voltage V_S, and the voltage applied on the P^+ stripe V_r are also studied. In section 3, the measured d.c and a.c electrical characteristics of the device are presented for different operating conditions. Finally, the last section of the chapter deals with the magnetic characteristics of the device.

Since it is known that surface effects play an important role in the operation of semiconductor devices, in Chapter 4 we will see how surface effects influence the LMT characteristics. The surface effects are controlled by the applied gate potential.

Chapter 5 is dedicated to noise studies. The first section of this chapter outlines the problems associated with noise. This is followed by the definitions and formulas of different noise sources. Then the description of the experimental set up and the noise measurement procedures are presented. The remainder of Chapter 5 deals with the experimental results on the collector noise of single ended and differential LMTs.

In Chapter 6 the results related to LMTs fabricated in bipolar technology are presented. Special attention is paid to the role of the n^+-buried layer on the electrical and magnetic characteristics of the device.

In the conclusion, we summarize the performance of our LMTs and then propose future investigation into MT.

2. REVIEW OF MAGNETOTRANSISTOR STRUCTURES

The purpose of this chapter is to highlight important achievements in the development of MTs . We will look at various structures fabricated using different processes and discuss in detail important concepts in designing and analyzing MTs.

Investigation into the effect of magnetic field on certain parameter of a bipolar transistor has begun since 1950 by Brown [9]. He discovered that the cut-off frequency, f_c, and the current gain, α', of a point contact transistor decrease when a negative transverse magnetic field is applied and increase with a positive field. In 1959, Trivadi and Srivastava [10] extended this investigation to the germanium junction transistor. Unlike Brown, they found that the effect of magnetic field on f_c was negligible. They also found that the current gain α' drops when either positive or negative transverse magnetic field is applied. The explanation was that the transverse magnetic field modulated the effective diffusion length of the minority carriers in the base region. Trivadi and Srivastava were the first to suggest that the transistor be used as a device to measure the strength of magnetic field by measuring the change in α'. Lack of interest and lack of potential commercial applications with solid state magnetic field sensors prevented further study in the field of magnetic transducers using regular bipolar transistors. It was not until the end of the 60's and in the early 70's that some interest was revived. Although there were only a few research papers reported, the whole approach to make a transistor which can serve as a MFS took a turning point. For the first time, specific transistors were designed to be magnetic field sensors. Here, the change in collector currents or voltages was used to measure the strength of **B**. Hudson [11] received the first patent on the transistor used as a semiconductive magnetic transducer in 1968. Two years later, Flynn [12] reported a two collector vertical

magnetotransistor used as a magnetometer. In the same year, Davies and Wells [13] presented the first drift aided lateral magnetotransistor. The device was actually a lateral double collector transistor embedded into a Hall plate.

Since these devices were the first generation of MTs, they were not optimized and so their relative sensitivity was rather low, in a range of 0.02 T^{-1}. Therefore they provided no alternatives to the already mature Hall cell devices. Thus there was another long, stagnant period in the investigation of MT. In the early 80's when industries and consumers demanded a much higher sensitivity, higher reliability, and less expensive MFSs, the Hall cell devices could not meet all the requirements. This brought a surge of interest in the field. Many novel structures were designed, and at the same time many models and theories were developed. In all, three distinct structures were considered: VMTs, LMTs, and SSIMTs. In addition, three different mechanisms – injection modulation, carrier deflection, and magnetoconcentration – were introduced to account for the galvanomagnetic effects in MTs. These three mechanisms are manifested from the action of the Lorentz force on the charge carriers. Carrier deflection refers to the action of the Lorentz force acting on the minority carriers in the base region or in the depletion region of the collector. It is characterized by the linear response of the output signal with respect to the applied field. Emitter injection modulation, on the other hand, is related to the Hall electric field generated by the Lorentz force acting on the majority carriers in the base region. This Hall field then modulates the potential along the emitter-base junction and therefore the injection of the minority carriers, and thus brings about an unsymmetrical injection along the emitter perimeter. Magnetoconcentration refers to the modulation of the conductivity in the base region at high injection levels. The last two mechanisms are characterized by the nonlinear response of the device with respect to the applied magnetic field. Depending on a particular design and at a certain biasing condition, one of these

three mechanisms could prevail. Most of the structures designed during this period were one dimensional MTs. They could only detect one component of the **B** vector. Multidimensional MTs have been pursued actively only in the last 3 years [3,4,14,15]. These devices still need to be optimized to achieve high relative sensitivity in all three directions and to have no cross sensitivity.

The classification of MTs is based on the main current flow of the MT that is used to sense B with respect to the chip surface. The VMT is a transistor that has its main current flow perpendicular to the chip surface and deflect sideways due to the Lorentz force when B is applied perpendicular to the current flows. On the other hand, lateral current flow parallel to the chip surface of a LMT is essential for magnetic field detection.

2.1 VERTICAL MAGNETOTRANSISTOR (VMT)

An example of a VMT is depicted in Fig.2.1. It is proposed by Zieren and Duynham [14] and is fabricated in bipolar IC technology with n^+-buried layer. The device is a npn differential transistor with 2 collectors. The collectors are formed by splitting the n^+-buried layer into two halves. A gap between two collectors is necessary to avoid short circuiting the collector contacts. When B is zero, the main current which flows down towards the two n^+-buried layers will be collected equally by the two collectors. If B is applied parallel to the chip surface, the current beam will be deflected sideways by a Hall angle θ_H. The Hall angle is defined as the angle between the electric field and the current density vector. It is defined by the condition

$$\tan \theta_H = \mu_H B \qquad 2.1$$

where μ_H is the Hall mobility, and B the magnetic induction. The deflection of the current beam leads to an imbalance in collector currents which can then be measured. An average relative sensitivity of 0.05 T^{-1} is obtained. Sensitivity increases with a longer effective deflection length L and with a narrower emitter beam. At higher injection, the emitter injects electrons from its edges, thereby broaden the effective emitter beam. Consequently, the relative sensitivity is drastically decreased. The output signal of the device is linearly proportional to the magnetic field B. This linearity is attributed to the fact that the dominant mechanism for magnetic effect is minority carrier deflection in the n-epilayer.

Another possible VMT is proposed by Maenaka et al. [15] (see Fig.2.2). Unlike Zieren's VMT, this device is fabricated in bipolar process with no n^+ buried layer. However, the principle of operation is essentially the same. The only drawback is a lower relative sensitivity, around 0.02 T^{-1}. They also investigated the effect of emitter length and magnitude of I_C on the sensitivity. The conclusion was that at low and moderate injection levels, the sensitivity increases with higher I_C and decreases with longer emitter length.

At the same time, both Zieren's group and Maenaka's group have introduced their two dimensional VMTs capable of detecting both components of the in-plane magnetic field simultaneously. Actually, Zieren's device is the first multidimensional MT. The structure consists of a circular emitter, a base region, and four buried n^+ collector contacts (see Fig.2.3). In Maenaka's 2-D VMT shown in Fig.2.4, there are two 1-D VMT placed 90 ° apart. Its operating principle is the same as the structure shown in Fig.2.2. More recently, Kordic introduced a 3-D magnetic field sensor [4]. The sensor is a 2-D VMT with additional collector contacts. The 2-D VMT senses the in plane components of the magnetic field while the additional inner collector contacts are used to detect the perpendicular component of B vector. The simplest structure has two 'x' and two 'y' collectors

and one 'z' collector pair. The main problem of this structure is that the output signal of the z component is extremely low and comparable to the cross-output signal between x- and y-channels. A more advanced device incorporates 4 'z' collector pairs (see Fig.2.5). The output signal from the z collector pairs is much higher in this case because the contacts z_i' are connected together as well as those of z_i. However, this structure still has some inherent cross-sensitivities. The uniqueness of this 3-D MFS, the author claims, is its small spatial resolution.

2.2 LATERAL MAGNETOTRANSISTOR

A lateral pnp magnetotransistor proposed by Davies and Wells [13] is shown in Fig.2.6. The n type base region acts as a Hall plate. There are 2 base contacts. In the presence of a potential difference between the base contacts, an electric field will be established in the base region, and this in turn will give rise to a drift component of the minority carrier current density. When B is applied perpendicular to the surface, the action of the Lorentz force rotates the total electric field in the base region by a Hall angle θ_H for the majority carriers (electrons), e.g. the charges accumulated on two sides of the base region. This rotation in E results in an additional rotation for the minority carriers (holes). Hence the total deflection angle of the total current density vector is given by the angle,

$$\theta_p = \arctan(\mu_p B) + \arctan(\mu_n B) \qquad 2.2$$

where μ_n and μ_p are the Hall mobilities for electrons and holes respectively.

Modulation of emitter injection is claimed to be the dominant effect in Vinal and Masnari's device [16,17]. They explain that an applied perpendicular magnetic field causes a voltage variation along the emitter-base junction due to the

established Hall field along the emitter-base junction. This results in nonuniform carrier injection into the base, and subsequently unequal currents in the two collectors. More specifically, when V_{B1} is used to bias emitter-base junction, a Hall field is established from right to left (see Fig.2.7). This induced Hall field increases the emitter-base voltage by an amount on the right side of the front surface of the emitter, and decreases the emitter-base voltage the same amount on the left side. The right side of the emitter, therefore, injects more electrons, and so the right collector current increases. On the other hand the left side of the emitter injects less electrons, and the left collector current decreases. The difference between the collector currents I_{CR} and I_{CL} is used to measure the strength of the magnetic field. When V_{B2} is used to bias the emitter base junction, a Hall field is established from left to right and all the previously mentioned effects reverse. Now the left collector current increases while the right collector current decreases. Vinal and Masnari also present another injection modulation based on lateral npn transistor that is sensitive to the magnetic field applied parallel to the chip surface. The approach in that structure is to use a recessed oxide surrounding the emitter so that no injection will take place from the perimeter of the emitter.

It is easy to show that when the emitter injection modulation is involved, the Hall voltage created in the base region of the MT can be expressed as

$$V_H = KR_H I_B B \qquad 2.3$$

where K is the geometrical constant, R_H is the Hall coefficient, I_B is the base current, and B is the magnetic induction. This voltage is superimposed to the emitter-base junction voltage and produces

$$I_C(B) = I_{C\,sat}\exp[q(V_{BE} + V_H)/mkT] \qquad 2.4$$

Therefore, the net collector current is an exponential function of V_H, and the change in collector currents varies nonlinearly with B.

The MTs' structures described so far are fabricated in bipolar technology. There are also LMTs fabricated in CMOS technology. The first device is proposed by Popovic [18,19] (see Fig.2.8). It is a device sensitive to B applied parallel to the chip surface and features a relative sensitivity of 1.5 T^{-1}. The device has two base contacts to create an accelerating E field in the base region for aiding the drift current component. The emitter, the collector, and the base contacts are situated inside a P-well which serves as a base region. The substrate in this case is acting as a second collector and is considered a parasitic collector. The device is sensitive to B applied parallel to the chip surface. At moderate injection, even though both mechanisms--carrier deflection and injection modulation--have their roles in magnetic transduction, the former one is more dominant. The result is a linear response with B. At high injection, magnetoconcentration effect becomes important. The magnetic sensitivity decreases with increasing emitter current beyond 1.0 mA. More information about its principle of operation will be given in Chapter 3 when we discuss the principle of operation of our structure.

2.3 SUPPRESSED SIDEWALL INJECTION MAGNETOTRANSISTOR (SSIMT)

The most sensitive magnetotransistor so far is the one designed at the University of Alberta. It is called the Suppressed Sidewall Injection Magnetotransistor (SSIMT). Its sensitivity ranges from 0.5 T^{-1} to 30 T^{-1} depending on the

operating condition. The collector currents at maximum sensitivity are of the order of 400 μA [5, 20].

The SSIMT is a special form of LMT. Its unique feature is the placement of two P^+ stripes along the edges of the emitter and parallel to the collectors (see Fig.2.9). For simplicity, let us consider only the right half of the differential structure. When a potential V_r , less than or equal to the emitter potential, is applied to the P^+ stripes, a lateral current which is supposed to be injected from the emitter will be suppressed due to the reverse bias of the vertical portion of the emitter. This means that carriers injected from the emitter into the neutral base are confined to the bottom of the emitter-base junction. At the same time a lateral accelerating electric field is created in the neutral base because $V_b > V_r$. This E field helps to sweep part of the injected current to the collectors. The two P^+ stripes play another important role. By applying a slightly different negative potential to each P^+ stripe, the offset can be reduced.

When the emitter-base junction is forward biased and the P^+ stripes are grounded or biased with negative potential V_r, the current injected from the emitter will flow downward and then split into three distinct current flows. The major part of the injected current flows downward and is collected by the substrate. The small portion of the injected current that is due to the lateral accelerating electric field flows laterally, and is collected by the 2 collectors C1 and C2.

When B is directed into the figure plane, the Lorentz force deflects the left lateral current towards the device surface and the right towards the base-substrate interface; therefore, the left collector current increases while the right one decreases. The deflection of the vertical current flow to the left brings about a further increase in the left collector current and a further decrease in the right collector current. Thus the difference between the two collectors becomes greater

and the sensitivity increases. Under the bias of V_{CE} = 5.0 V, V_S = 5.0 V, I_B = 7 mA, and V_r = -0.2 V, a sensitivity of 30 T^{-1} was obtained [20].

In [5], an elaborate theory about the operation of the SSIMT is given. After many derivations, the overall expression for the relative sensitivity is given as

$$S_r = \mu_H \frac{L_1 + L_2}{W_{eff}} \qquad 2.6$$

where L_1 describes how deep the injected carriers travel in the vertical direction before being swept laterally by the E field, L_2 represents the lateral length the injected carriers have to travel before reaching the collector, W_{eff} is the effective width for the carriers flowing in the lateral direction, and μ_H is the Hall mobility. The term (L_1 + L_2) is the total length for an electron to travel from the emitter to the collector. To increase S_r, we have to make W_{eff} as small as possible. Three parameters that can influence the magnitude of W_{eff} are V_r, V_S, and I_B.

By applying negative potential V_r to the P^+ stripes, we do two things. First we push the injected carriers further down before they can be swept laterally. Second, the difference between V_B and V_r creates the lateral E field. As already mentioned, the E field helps to collect electrons more effectively. It is shown in [5] that as V_r is biased more negatively, W_{eff} becomes smaller and S_r increases. At some critical value V_{rc}, W_{eff} can be reduced to zero and so collector currents become zero. V_r also affects the term (L_1 + L_2). Increasing V_r increases (L_1 + L_2). In fact, V_r has the most important influence on the W_{eff} and consequently on S_r.

The second parameter that affects W_{eff} is V_S. When the device is biased with V_S, a depletion region between the P-well/N-substrate junction is established. As V_S increases, the depletion region gets wider and so the W_{eff} becomes smaller.

The end result is an increase in S_r. It has been experimentally shown that the sum $L_1 + L_2$ is relatively insensitive to changes in V_S.

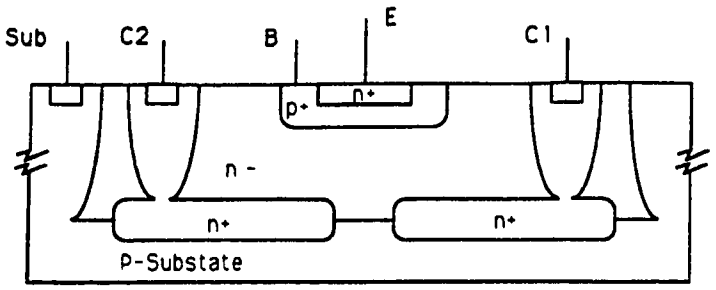
Finally, W_{eff} is also affected by I_B. Decreasing I_B brings about a reduction in W_{eff}. I_B must be biased higher than the critical base current I_{BC} in order to establish the collector currents. The dominant mechanism that describes the SSIMT magnetic transduction is carrier deflection. The evidence is a linear response with respect to changes in B. To conclude this chapter, we provide Table 2.1 for comparison among MTs.

	Sensitivity	Directional sensitivity	Dimensions	Type
Nield [1973]	0.37%/T	B_z	-	lateral pnp / drift aided
Halbo [1980]	1.77%/T	B_z	-	lateral pnp / drift aided
Popovic [1986]	120%/T	B_x	-	lateral npn / carrier deflection
Ristic et al [1987]	3000%/T	B_x	-	SSIMT
Vinal [1984]	6.7%/T	B_x	-	†lateral pnp / injection modulation
Vikulin [1981]	2.6%/T	B_z	-	lateral pnp / carrier deflection
Zieren [1983]	5.0%/T	B_x	8x20x140	vertical pnp / carrier deflection
Ristic et al. [1988]	Sx=160%/T Sz=20%/T	B_x B_z	6x36x36	lateral npn / carrier deflection
Ristic et al. [1989]	Sx=40%/T Sy=38%/T	B_x B_y		lateral npn / carrier deflection
Zieren [1983]	Sx=5%/T Sy=5%/T	B_x B_y	8x20x20	vertical pnp / carrier deflection
Kordic [1988]	Sx=1.4%/T Sy=2.2%/T Sz=0.3%/T	B_x B_y B_z	8x10x20	vertical pnp / carrier deflection
Ristic et al. [1989]	Sx=40%/T Sy=38%/T Sz=10%/T	B_x B_y B_z	6x36x36	lateral npn / carrier deflection

Table 2.1 COMPARISON AMONG DIFFERENT MAGNETOTRANSISTORS

† nonlinear devices.

a)



b)

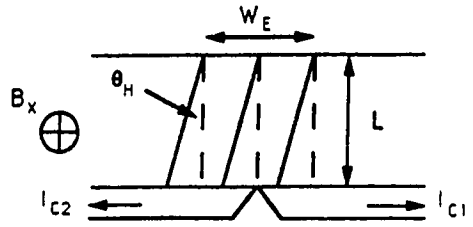
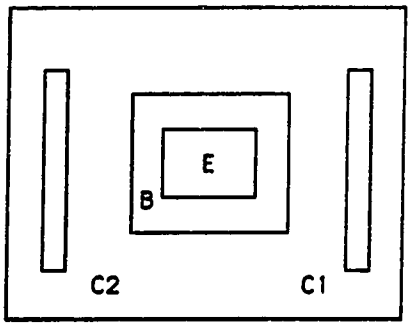


Fig.2.1 a) Cross section of a npn differential VMT designed by Zieren, b) magnetic induction B causes assymetry in collector currents.

a)



b)

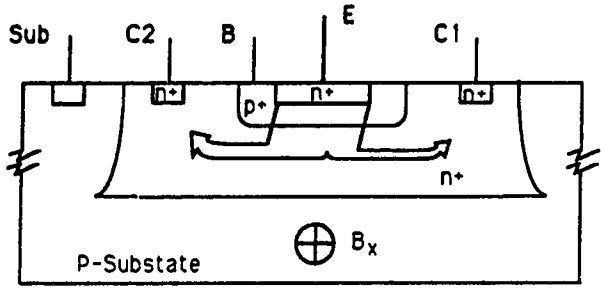


Fig.2.2 Maenaka's VMT, top view a), and cross section b).

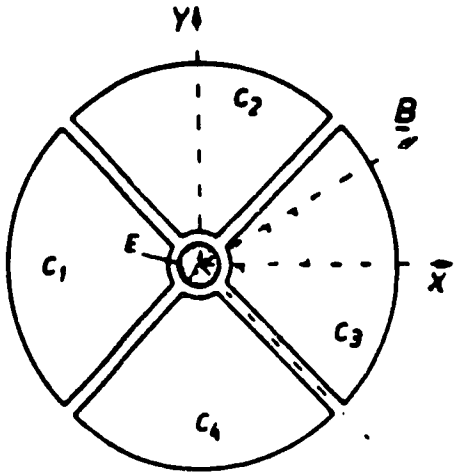


Fig.2.3 Top view of Zieren's 2-D VMT.

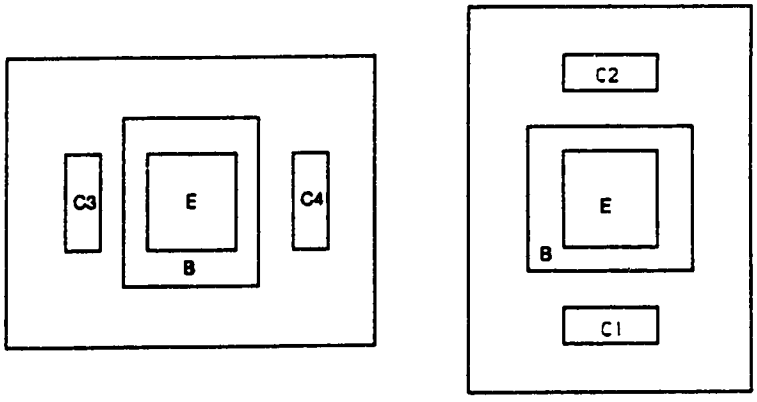


Fig.2.4 Top view of Maenaka's 2-D VMT.

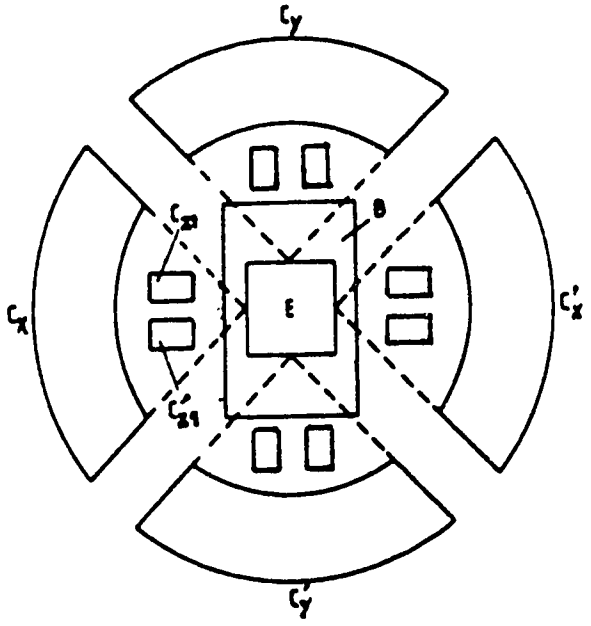


Fig.2.5 Top view of Kordic's 3-D MT. The 4 outer collector contacts are used to detect the in plane B vector, B_X and B_Y. The 8 inner collector contacts are used to sense B_Z.

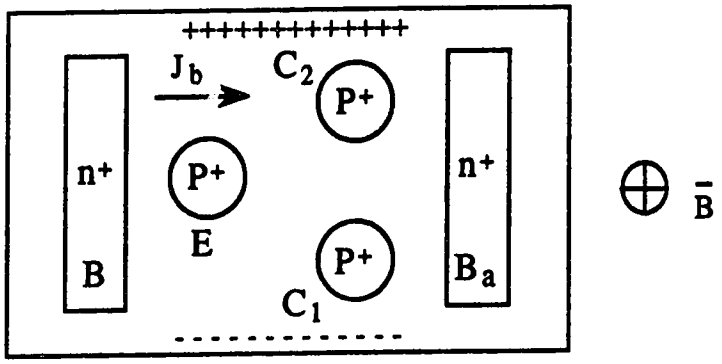


Fig.2.6 A drift-aided LMT proposed by Davies and Wells. When B_Z is applied, charges redistribute in the x-dir, thus creating a Hall field, E_{Hx}.

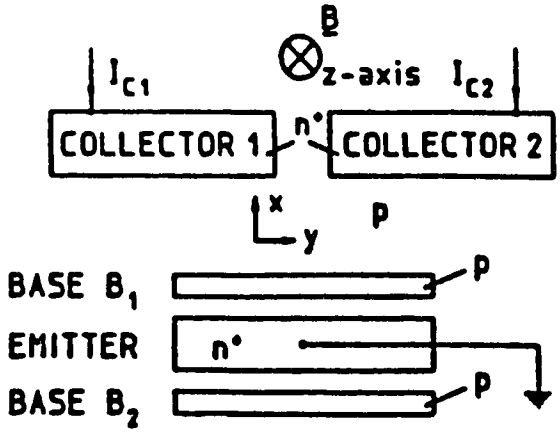


Fig.2.7 Vinal and Masnari's differential LMT. The device operation is dominated by the emitter injection modulation.

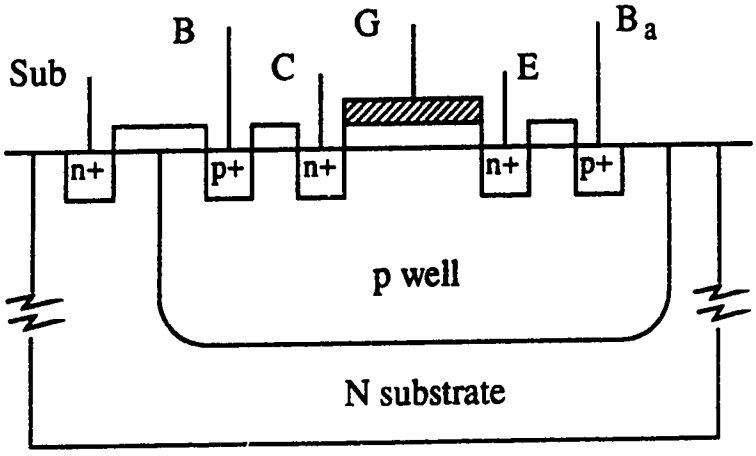
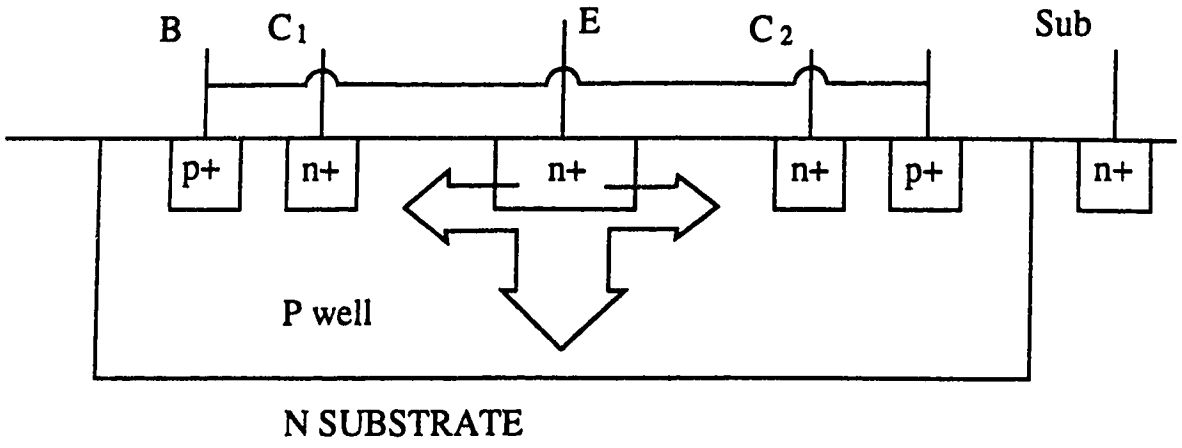
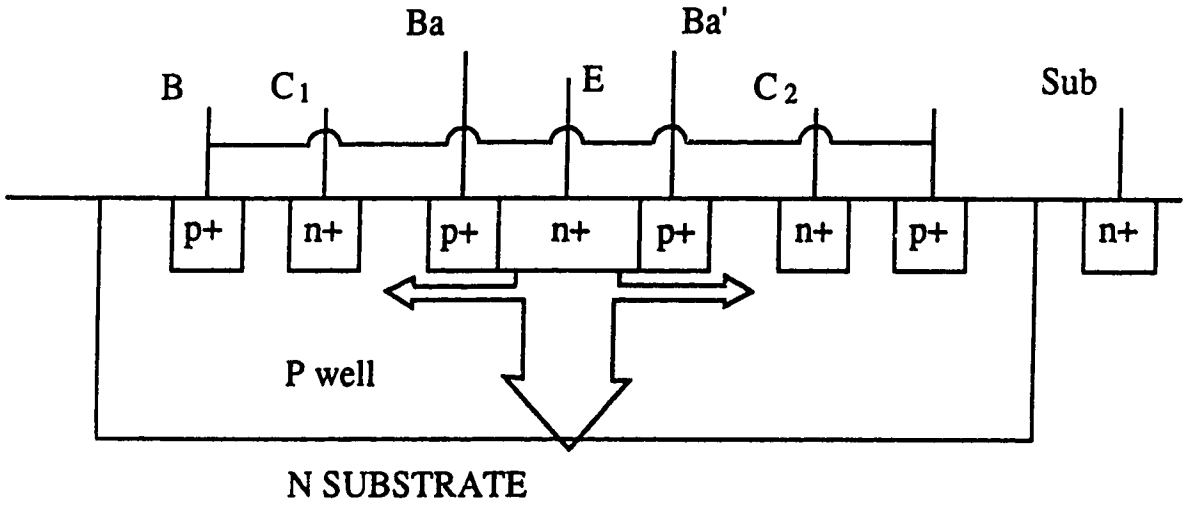


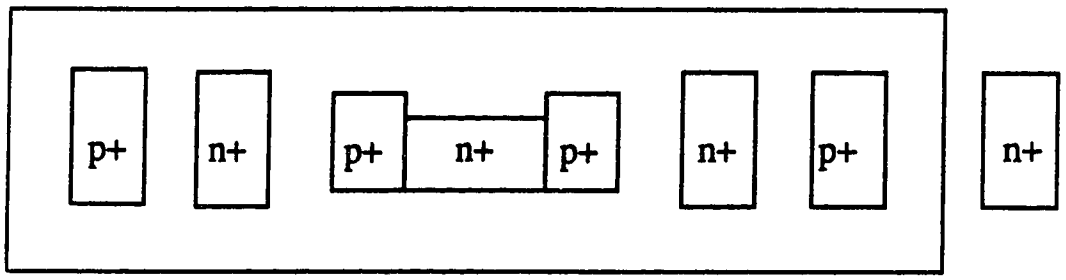
Fig.2.8 Popovic's LMT fabricated in CMOS technology.



a)



b)



c)

Fig.2.9 a) cross section of a regular LMT, b) cross section of a SSIMT, and c) top view of a SSIMT. The additional p^+ stripes adjoining the vertical edges of the emitter reduce the W_{eff} of the collector current beams.

3. LMT STRUCTURE SENSITIVE TO MAGNETIC FIELD EITHER PARALLEL OR PERPENDICULAR TO THE CHIP SURFACE

Optimizing VMTs and LMTs has been the main effort of many researchers. Maximum sensitivity of various MTs can be obtained with optimum geometry and operating principles. We investigate here a new lateral magnetotransistor that is fabricated in CMOS technology. The device is sensitive to B applied either parallel or perpendicular to the chip surface.

3.1 DESCRIPTION OF DEVICE STRUCTURE

The structure of the new device is shown in Fig.3.1. It consists of 2 LMTs that are mirror images of each other. Each LMT is similar to Popovic's device shown previously in Fig. 2.8. Each LMT is comprised of a single emitter, a base region, and a collector purposely placed asymmetrically between the emitter and the base contact in order to sense B applied either parallel or perpendicular to the chip surface. The emitter is surrounded by a p^+ region on 3 sides of its perimeter. Both LMTs share the same substrate. The device was fabricated in standard CMOS technology using the Northern Telecom 5μm process. The base region is formed by a p-impurities implantation and diffusion. The n^+ and p^+ were realized using the standard doping process of the source and drain of n-channel and p-channel MOS transistors. The junction depth for the n^+ and p^+ diffusions are 1.2 μm and that of the p-well is 10 μm. The p-well doping is 10^{16} atoms/cm^3, the substrate 10^{15} atoms/cm^3, and the n^+ and p^+ 10^{20} atoms/cm^3.

The p^+-region surrounding the 3 sides of the emitter is intended to create a better defined current flow of carriers towards the collector. This can be readily understood as a consequence of the variation in the built-in voltage along the

emitter-base junction. At the vertical edge of the emitter on the 3 sides, there is a n^+/p^+-junction, while on the side facing the collector a n^+/p-junction exists. Since the built in voltage, V_{bi}, depends on the doping concentration

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right) \qquad 3.1$$

where N_A is the doping concentration of the base region, N_D is the doping concentration of the n^+ emitter, and n_i is the intrinsic concentration, it follows that V_{bi} at the 3 sides of the emitter is higher than the V_{bi} on the side toward the collector. Thus, the injected lateral carriers from the emitter on the 3 sides can be neglected when compared to that from the side facing the collector.

3.2 PRINCIPLE OF OPERATION

In this section we will describe the device's operation starting from the simplest biasing condition towards the most complicated one. The biasing circuit of the differential LMT is shown in Fig.3.2. The values I_S, V_B, V_C, V_r, and V_G determine the operating point of the device. The effect of V_G on the device's characteristics will be examined in Chapter 4. For now we leave V_G floating.

3.2.1 Floating V_S and V_r.

The simplest configuration to analyze our device in terms of electrical characteristics, noise, and temperature would be the lateral npn transistor with the substrate, the p^+ stripes, and the gate disconnected. For simplicity, let us consider only the right LMT of the differential structure for the time being. In the forward active regime, (the base emitter junction is forward biased and the base

collector junction is reverse biase) electrons are injected from the bottom and from the right vertical edge of the emitter into the base region. While in the base region, some electrons will diffuse and drift to the base collector depletion region and get collected by the collector. Some will recombine with majority carriers, holes. Most of the collector current is contributed by the electrons injected from the right vertical edge of the emitter. For the differential structure, when B is zero, the two collector currents I_{C1} and I_{C2} will be equal because of the symmetry of the structure. When B is applied parallel to the chip surface in the negative x-direction, the Lorentz force deflects I_{C1} and I_{C2} in opposite z-directions. Thus I_{C1} increases while I_{C2} decreases. If we reverse the B field in the positive x direction, then I_{C2} increases while I_{C1} decreases. Next, let us consider the situation when B is applied perpendicular to the chip surface. The Lorentz force will deflect I_{C1} and I_{C2} in the opposite of the x-direction. There is no Hall field established in the base region in this case; therefore, we can rule out the emitter injection modulation effect. At moderate injection, carrier deflection is the only important galvanomagnetic effect. Thus, following the derivations presented in [14,19], the relative sensitivity S_r in this mode of operation can be expressed as,

$$S_r = -\mu_n \frac{W_B}{W_{eff}} \qquad 3.2$$

where W_B is the effective length for electrons to travel from emitter to collector, μ_n is the electron mobility of silicon, and W_{eff} is the width of the lateral current flow. When the device is used to sense B_X, W_{eff1} = Y, the depth of the P-well. On the other hand, when the device is used to sense B_Z, W_{eff2} = L, the overlapping distance between the emitter and the collector. This equation suggests that in order to increase the sensitivity, W_{eff} should be as small as possible and W_B

should be long. For the time being, we assume that W_{eff} is constant. It remains to analyze the influence of W_B.

We can increase W_B in 2 ways: 1) physically make a longer device, and 2) increase the collector voltage. Popovic's experiments with several groups of devices similar to ours with different W_B, ranging from 10 to 60 μm, have given a good indication that $S_r \alpha W_B$. Hence, we do not need to confirm it again. Our base width is designed to be 70 μm. Next, let us see how much V_C can influence W_B. We start with the expression of I_C,

$$I_C = \frac{qA\bar{D}_n n_i^2}{Q_B} \exp\left(\frac{V_{BE}}{V_T}\right) \qquad 3.3$$

where q is the elementary charge, A is the cross sectional area of the lateral flow, D_n is the average diffusion constant for electrons, and Q_B is the number of doping atoms in the base per unit area. The only parameter that is affected by V_C is Q_B. Differentiating of (3.5) with respect to V_{CE} yields

$$\frac{\partial I_C}{\partial V_{CE}} = \frac{-I_C}{Q_B} \frac{\partial Q_B}{\partial V_{CE}} \qquad 3.4$$

If we assume the doping concentration in the base region is uniform, then $Q_B = W_B N_A$. So,

$$\frac{\partial I_C}{\partial V_{CE}} = \frac{-I_C}{W_B} \frac{\partial W_B}{\partial V_{CE}} \qquad 3.5$$

where N_A is treated as a constant.

For a reverse biased junction, $\frac{\partial W_B}{\partial V_{CE}}$ is usually given as,

$$\frac{\partial W_B}{\partial V_{CE}} = \left(\frac{\varepsilon}{2qN_A\left(1 + \frac{N_A}{N_D}\right)(V_{bi} + V_{CE})} \right)^{1/2} \qquad 3.6$$

where ε is the dielectric permittivity for silicon. Quick calculation will reveal that this is very small, and hence W_B can be assumed to be constant. In conclusion, we do not expect varying the V_C will change the magnetic sensitivity.

3.2.2 Substrate bias

When the substrate is connected to positive voltage, there will be another reverse biased junction, the P-well/N-substrate junction. The portion of the electrons that contribute to the collector current will again originate from the right edge of the emitter plus a small portion of the electrons from the bottom of the emitter adjacent to the right edge. The rest of the electrons will diffuse and drift towards the substrate. In effect, there are two MTs, a LMT and a VMT superimposed on each other.

When B is applied parallel to the chip surface in the positive x-direction, not only the collector current is deflected by the Lorentz force but the substrate current also is deflected in the positive y-direction; I_S decreases (see Fig.3.1d). The deflection of I_S brings about a further increase in I_{C2}, because more electrons contribute to the collector current. Because of this "double deflection" ΔI_{C2} is larger than when the substrate is disconnected, and the relative sensitivity is higher. When B is applied perpendicular to the chip surface, there is no deflection of I_S because B is in the direction of flowing I_S.

The carrier deflection is the underlying mechanism that describes the magnetic transduction at low and moderate injection levels. We can use the same equation (3.2) to calculate the theoretical S_r. However, we need to redefine W_{eff}. For easier interpretation of the flow of the minority carriers in the base region, let us

introduce an imaginary plane in the z-direction that divides the base region into two regions. The region above this plane will contain electrons that will reach the collector, whereas the electrons that flow below this plane will be collected by the substrate. When B is applied parallel to the chip surface, W_{eff1} will now be the distance between the chip surface and the z-plane. When B is applied perpendicular to the chip surface, W_{eff2} remains the same as before.

The substrate voltage can affect W_{eff1}. By increasing V_S, we make the depletion region of the P-well/N-substrate junction wider and therefore the z-plane will move up closer to the chip surface. In other words, W_{eff1} becomes smaller. Electrically, I_C will drop considerably as we increase V_S because the effective area of the lateral flow becomes less. The next logical question to ask is "How much influence can V_S have on W_{eff1}, and hence S_r ?" To answer the question, we can use those derivations for $\partial W_B / \partial V_{CE}$ as a first order approach. We need to make some changes though, because now we have to account for the vertical graded doping of the base region. If we consider the P-well/N-substrate junction as a linear graded junction for which depletion region is proportional to $(V_{bi} + V_S)^{1/3}$ [21], then W_{eff1} is proportional to [5],

$$W_{eff1} \approx \left(\frac{12\varepsilon}{qa}\right)^{1/3}(V_{bi} + V_S - V_{BN})^{1/3} \qquad 3.7$$

where a is the impurity gradient at the junction, and $(V_{bi} - V_{BN})$ is the base voltage. Therefore, the first derivative of W_{eff1} is

$$\frac{\partial W_{eff1}}{\partial V_S} \approx \frac{1}{3}\left(\frac{12\varepsilon}{qa}\right)^{1/3}\frac{1}{(V_{bi} + V_S - V_{BN})^{2/3}} \qquad 3.8$$

To compare this with (3.6) is difficult, because we do not know exactly the doping profile in the base region. It remains for experimental characterization of the device to determine how much V_S can influence the device's operation. We should also watch for the critical value of V_S, i.e. when W_{eff1} becomes zero.

The exact relationship between I_B and W_{eff1} is difficult to derive, because now I_B affects the operation of both the VMT and the LMT. Once again we have to rely on experimental characterization.

3.2.3 Combination of substrate and p^+ stripe bias.

When p^+ stripe is grounded or negatively biased, 2 important things occur. First, because the p^+/n^+ junction exists, its depletion region will reduce the area of the bottom of the emitter. This means that the effective bottom area for the injection of electrons becomes smaller as V_r becomes more negative. Second, the biased p^+-stripe provides an additional path for the holes to travel from the base. This means also that the lateral accelerating electric field E_{ay} will be increased. This E_{ay} will help the electrons to drift towards the collector more effectively. To operate the device, a much higher biasing I_B is needed to overcome the partial flow of holes through the p^+ stripe.

Following the model derived by Popovic in [19] for a similar structure, we can obtain the expressions for the relative sensitivity due to both carrier deflection and emitter injection modulation.

Let us first look at the cross section of the right LMT of the differential structure (see Fig.3.1). If $-B_X$ is applied, then a Hall field is created in the z-direction. We then begin with the expressions for the minority carrier density in the base region [19],

$$J_{ny} = J_{noy} + \mu_n^* B_X J_{noz} \tag{3.9.a}$$

$$J_{nz} = J_{noz} - \mu_n^* B_X J_{noy} \tag{3.9.b}$$

where

$$J_{noy} = \mu_n q n E_{ay} + q D_n \frac{\partial n}{\partial y} \tag{3.10.a}$$

$$J_{noz} = \mu_n q n \left(E_{bz} + E_{pz}^H\right) + q D_n \frac{\partial n}{\partial z} \tag{3.10.b}$$

where E_{pz}^H is the Hall field due to majority carriers and equals $\mu_n^* B_x E_{ay}$. The "*" is used to differentiate between hole or electron mobility and Hall mobility which has taken into account the scattering factor r_H [22]

$$\mu^* = \mu r_H \tag{3.11}$$

After introducing the imaginary z-plane and assuming B has no influence on the electron concentration, the S_r for B_X due to the carrier deflection mechanism becomes,

$$S_{rx}^D = \left(\frac{W_B}{W_{eff1}}\right) \frac{\mu_p^* \mu_n q n E_{ay} - \mu_n^* \left(q \mu_n n E_{ay} + q D_n \frac{\partial n}{\partial y}\right)}{q \mu_n n E_{ay} + q D_n \frac{\partial n}{\partial y}} \tag{3.12}$$

If the diffusion component is dominant, $q\mu_n n E_{ay} << q D_n \frac{\partial n}{\partial y}$, then (3.12) becomes

$$S_{rx}^D = - \mu_n^* \left(\frac{W_B}{W_{eff1}}\right) \tag{3.14}$$

In the opposite case, when the drift component is more important, (3.12) becomes

$$S_{rx}^{D} = (\mu_p^* - \mu_n^*)\left(\frac{W_B}{W_{eff1}}\right) \qquad 3.14$$

To get S_r due to emitter injection modulation, we have to find the Hall voltage along the emitter-base junction

$$V_H = \int E_p^H dl \cong K R_H I_B B \qquad 3.15$$

and therefore

$$I_C(B) = I_{Csat} \exp[(V_{BE} + V_H)/mV_T] \qquad 3.16$$

which gives us

$$S_{rx}^{I} = \frac{q}{nkT}\frac{\partial V_H}{\partial B} \leq \frac{q}{nkT}\mu_p^* E_{ay} Z \qquad 3.17$$

where Z is the diffusion depth of P-well.

Following the same steps and procedures, we can obtain S_r when B_Z is applied. The Hall field is now in the x-direction. Equations (3.13), (3.14), and (3.15) become,

$$S_{rz}^{D} = -\mu_n^*\left(\frac{W_B}{W_{eff2}}\right) \qquad 3.18$$

$$S_{rz}^{D} = \left(\mu_p^* - \mu_n^*\right)\left(\frac{W_B}{W_{eff2}}\right) \qquad 3.19$$

$$S_{rz}^{I} = \frac{q}{nkT}\frac{\partial V_H}{\partial B} \le \frac{q}{nkT}\mu_p^* E_{ay} X \qquad 3.20$$

where X is defined in Fig.3.1.

The influences of V_S, I_B, and V_C on the relative sensitivity will remain the same as in the previous cases.

3.3 ELECTRICAL CHARACTERISTICS

3.3.1 Large signal analysis

All measurements related to the d.c., a.c., and magnetic sensitivity of the device were done in the common emitter configuration. The d.c and magnetic sensitivity measurements were done with a HP-4145A semiconductor parameter analyzer, a Varian V-4005 four inch electromagnet driven by a V-2900 regulated magnet power supply, a LDJ gaussmeter, and some external power supplies. The specifications for the HP-4145A are given in [23]. A magnetic induction of up to 1 T can be created by the electromagnet if the 2 poles are placed 2.5 cm apart. The maximum current rating on the magnet power supply is 80A. The gaussmeter and its InSb Hall probe have an accuracy of 1% each.

There are two sets of I-V characteristics, one set for the input terminals (I_B versus V_{BE}) and the other set for the output terminals (I_C versus V_{CE}). Other sets of graphs are related to the relationship between the input and output signals, and the effect of the substrate when it is biased and acts as a second collector. When the substrate is left floating, the device is just a lateral npn transistor.

Therefore, all large signal curves should look like those of conventional transistors. However, we should expect some differences in terms of magnitude because all geometries of the devices were optimized to achieve high relative sensitivity. For example, the device has a long base width.

Fig.3.3 shows a Gummel plot of the device. From the plot, after accounting for the ratio of natural to common logarithm, the ideality factor of p-n junctions 'm' can be calculated. For the base-emitter junction, m is found to be 2.9; for the collector-base junction, m equals 1.2. The large value of m for the emitter-base junction is probably due to the long base width of the lateral device which involves an additional voltage drop across the base resistance. At high current levels, m for the collector-base junction approaches 2. The decrease in I_C is partly due to the high level injection and partly due to the onset of the Kirk effect [24]. It is important to note that the I_B curve is higher than the I_C curve. This means that the gain of the npn LMT even in the common emitter configuration is less than 1. Again, the reason for this is the long base width - most of the electrons injected from the emitter recombine with the majority hole in the base region. Only a fraction of the injected carriers from the emitter is collected by the collector. Another parameter that can be extracted from Fig.3.3 is the saturation current I_{Csat}, which is the y-intercept of the extrapolated line drawn through the I_C measurements with the current axis at $V_{BE} = 0$ V. It equals 8.8×10^{-15} A.

Fig.3.4 illustrates the d.c current gain versus logI_C. It has the usual shape of a conventional transistor except that the current gain is less than 1.

Fig.3.5 displays the I-V output signal characteristic of the device. When the slope of the curve is extrapolated back to the x-axis, the early voltage V_A is found to be between -50 $\rightarrow$ -60 V. The breakdown voltage was also measured, BV_{CEO} = 24 V.

When the substrate is biased at 5 V, things get complicated. The p-well/n-substrate junction is reverse biased and acts as a second collector. We then have a lateral npn transistor and a vertical npn transistor superimposed on each other. Because the base width of the vertical transistor is approximately 1/10 of the lateral transistor, I_S should be at least 10 times I_C. When the VMT turns on, its action will dominate, i.e. most of the injected carriers will be collected by the substrate. Fig.3.6 and Fig.3.7 show the device characteristics of the vertical transistor. The substrate current levels off (saturates) and becomes insensitive to the increment of I_B when $I_B > 400\ \mu A$. In addition, it should be noted that H_{FE} of the VMT is much higher than H_{FE} of the LMT.

Fig.3.8 shows the base voltage as a function of I_B for different biasing conditions. It is interesting to note that the curves show negative resistance when the vertical transistor is turned on.

Finally the I_C - V_{CE} output characteristic of the LMT is shown in Fig.3.9. It clearly shows that the current gain is less than 1.

The effect of the bias P^+ stripe on the collector current can be seen from Fig.3.10. When $V_r = 0$, there are no available electrons for the collector at all until $I_B = 3.0$ mA . For $I_B > 3.0$ mA, the lateral flow is established; but the magnitude of the I_C is still much smaller than in the case when V_r is disconnected. As V_r becomes more negative, the critical I_{BC} increases and I_C decreases. It is also interesting to note from the plot that for $V_r < 0$, there is a region where the collector actually injects electrons and so behaves just like an emitter. The cause of this strange phenomenon can be found by looking at the corresponding V_B versus I_B graph, Fig.3.11. The region where the collector behaves as an emitter corresponds to the condition where $V_B > 5.0$ V. Therefore, the base collector junction is no longer reverse biased but rather is forward biased. Since both the base-emitter junction and base collector junction are forward biased, the transistor

is in the saturation region. Further increasing of I_B will lower V_B. This strange behavior is due to the fact that the high injection level has been reached. This condition modulates the conductivity in the base region, and R decreases. After $I_B > I_{BC}$, the base-collector junction will be once again reverse biased. Hence, once again the transistor operates in the normal active region.

The same explanation can be used to describe Fig.3.12, where I_S is plotted against I_B. To avoid forward biasing the base-collector junction, we can increase the V_C. Increasing V_C to 10 V, we obtain Fig.3.13. As can be seen, I_C never goes to negative. However, the collector current is larger due to the Early effect.

3.3.2 Small signal analysis

The small signal analysis is important because it gives us an insight into the frequency performance of the LMT. The characterization was done using a small sinusoidal signal input current i_b superimposed on the quiescent base current I_B. This caused a small variation in collector current, i_c .

The summary of the h-parameters of the device is given in Table 3.1. Again the results are separated into two groups; one is when V_S is disconnected and one is when V_S equals 5.0V. The semi log plot of the amplitude frequency response characteristic of the device is shown in Fig.3.14 and Fig.3.15. The cut-off frequency, f_c, is determined from the graph where A_i is down by 3 dB. For the case when V_S floats, f_c = 170 kHz; and for the case when V_S = 5V, f_c = 110 kHz .

Table 3.1. Small signal parameters of a LMT at f = 1 kHz

Parameters	Vs is floating	Vs = 5 V
hfe	0.59	0.74
hie	210.85	61.44
hoe	6.22×10^{-6}	8.71×10^{-6}
rbe	99.10	55.53
rbb	111.80	5.92

3.4 MAGNETIC RESPONSE OF LMT

In this section, we will first try to confirm that the carrier deflection mechanism describes the magnetic transduction of the LMT. We will then investigate the effects of each of the parameters V_C, I_B, V_S, and V_r on the relative sensitivity of the device.

The easiest way to confirm that the carrier deflection is the sole mechanism accounting for the galvanomagnetic effects of our device is to observe the change in collector currents with respect to the applied B. We know that for emitter injection modulation, a change in collector currents, ΔI_C, varies exponentially with B. On the other hand, for carrier deflection, ΔI_C varies linearly with B. In Figs.3.16 and 3.17, the responses of $\Delta I_C = I_{C2} - I_{C1}$ to a magnetic field applied in the z and x direction, are shown. For both biasing schemes, a linear relationship between ΔI_C and B was obtained. We conclude, therefore, that the carrier deflection mechanism is responsible for the magnetic transduction. From the plot we also see that when B field is reversed, ΔI_C switches sign. Furthermore ΔI_C when B_Z is applied is smaller than ΔI_C when B_X is applied. The reasons for this are 1) there is no double deflection when the device is subjected to B_Z, and 2) $W_{eff2} > W_{eff1}$.

The characterization of the device is also done for the case when P^+ stripes are biased (Fig.3.18). ΔI_{CX} again varies linearly with B. We conclude that the carrier deflection mechanism is the dominant mechanism that describes the magnetic transduction of our device.

For all calculations related to S_r, we use the formula

$$S_R = \frac{|I_{C1} - I_{C2}|}{I_{C10} + I_{C20}} \times \frac{1}{B} \quad [T^{-1}] \qquad 3.22$$

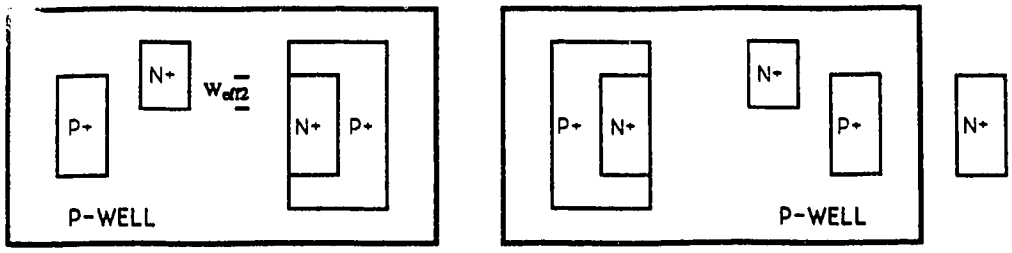
where I_{C1O} and I_{C2O} denote collector currents when B = 0, I_{C1} and I_{C2} represent collector currents when $B \neq 0$, and B is the magnetic induction.

Fig.3.19 illustrates the influence of V_C on S_r. The relative sensitivity seems to drop as V_C increases from 1 V to 5 V. But this reduction in S_r is very small and so V_C has an insignificant influence on S_r. This confirms our conclusion in section 3.2.

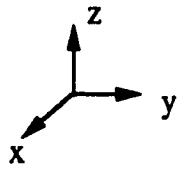
S_r as a function of I_B is considered next. From Fig.3.20, for low injection condition $I_B < 400$ μA, the sensitivity increases with the base current. This seems to contradict the statements we made earlier in 3.2.1. We have stated that as I_B increases, W_{eff} also increases and S_r becomes smaller. This is only observed for $I_B > 400$ μA. In this case, a possible explanation is that the device just turns on and so the lateral E field is weak. Therefore, the minority carriers are not confined but rather dispersed, and so W_{eff} is actually large. The peak S_r is at $I_B = 400$ μA. The same kind of shape is obtained for the case when $V_S = 5$ V and $V_r = 0$ V (Fig.3.21). The peak of S_r for this case is at $I_B = 3.1$ mA. It is also interesting to note that the sensitivity is higher when V_r is used. This can be attributed to the focusing effect of V_r.

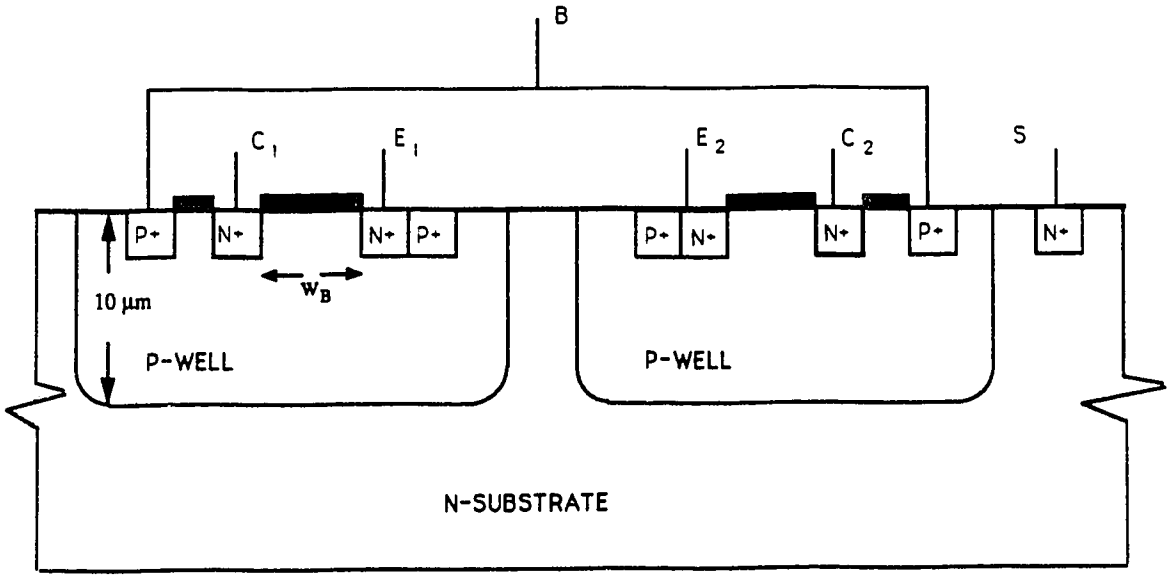
In section 3.2 the analysis shows that V_S plays an important role in the sensitivity. This is because as V_S increases, the imaginary plane z is pushed up

toward the chip surface; thus, W_{eff} becomes narrower. This in turn increases the relative sensitivity. The results shown in Figs.3.22 and 3.23 confirm our expectation. The influence of V_S is most significant with the P^+ stripes biased. A relative sensitivity of almost 400 %/T was obtained. The peak of sensitivity corresponds to the condition when the collector current is driven down by the V_S, I_C = 89.9 μA (see Fig.3.24).


N+
P+
W_{eff2}
N+
P+
P-WELL
P+
N+
N+
P+
N+
P-WELL
N-SUBSTRATE

a)


z
y
x


B
C_1
E_1
E_2
C_2
S
P+
N+
N+
P+
P+
N+
N+
P+
N+
10 µm
W_B
P-WELL
P-WELL
N-SUBSTRATE

b)

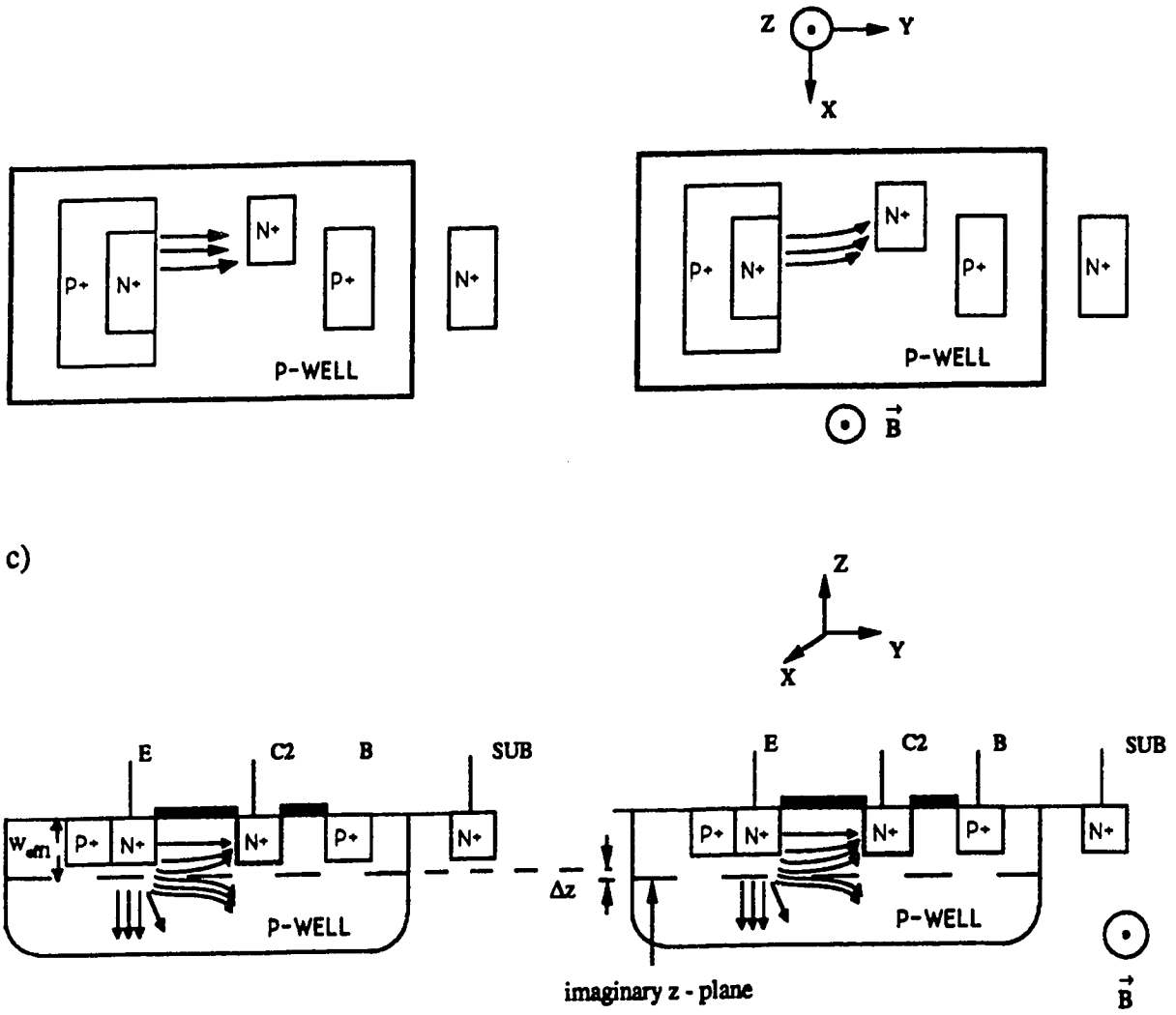


Fig.3.1 Our differential pair 2-D LMT, a) top view, and b) cross-section. $W_B = 70\mu m$, $W_{eff1} = 1.5\ \mu m$, and $W_{eff2} = 12\ \mu m$. c) I_{C2} increases when B_Z is applied, and d) I_{C2} increases when B_X is applied. Note in particular how B_X influences the imaginary z-plane. Minority carriers that are below the z-plane go to the substrate. Otherwise they go to the collector.

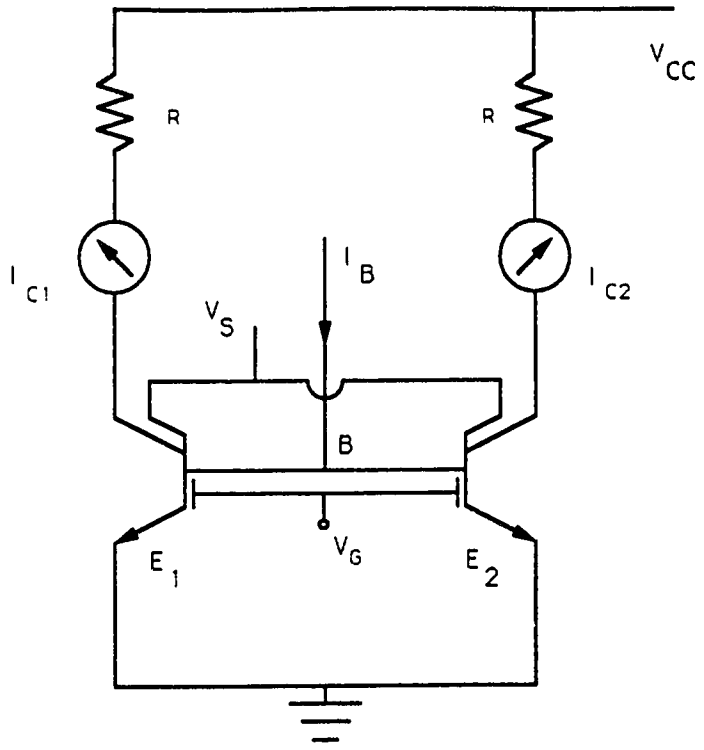


Fig.3.2 Biasing circuit.

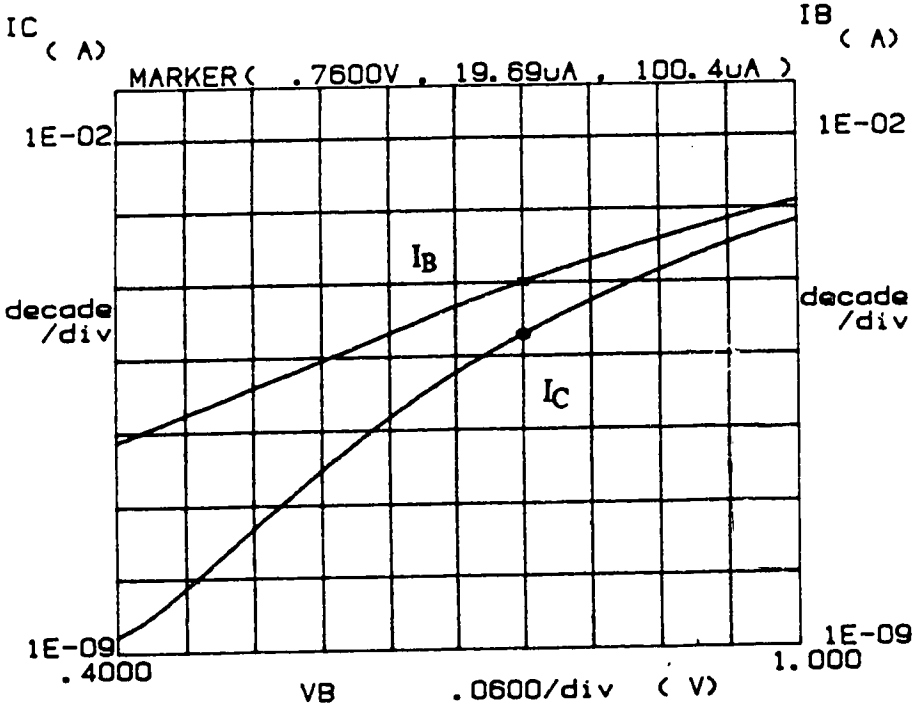


Fig.3.3 Gummel plot of the LMT biasing at V_{BC} = 0V, and V_S is disconnected.

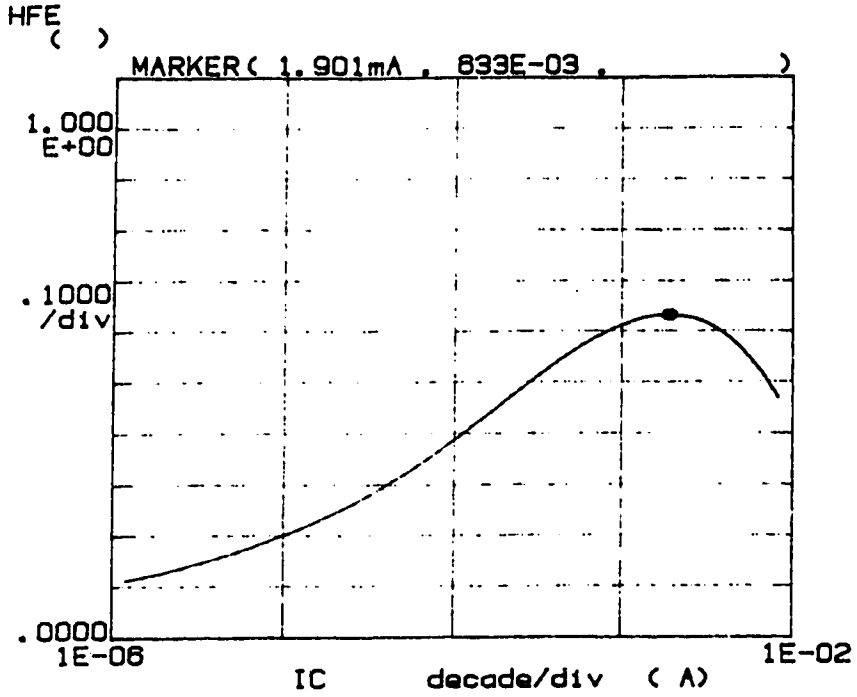


Fig.3.4 Current gain versus log I_C. V_C = 5V, and V_S is floating.

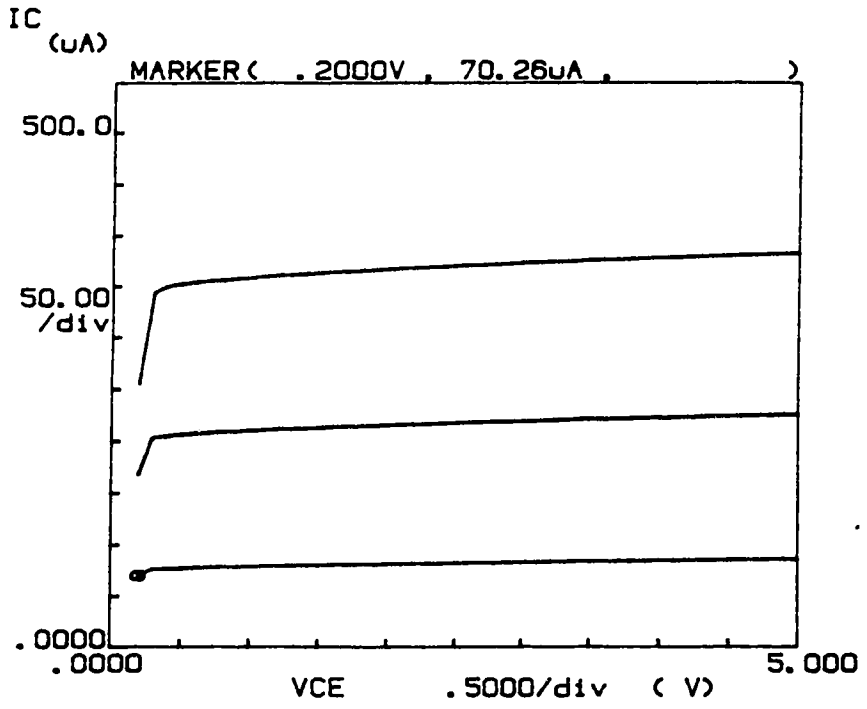


Fig.3.5 Output characteristic with I_B = 250 μA → 750 μA in steps of 250 μA, and V_S is disconnected.

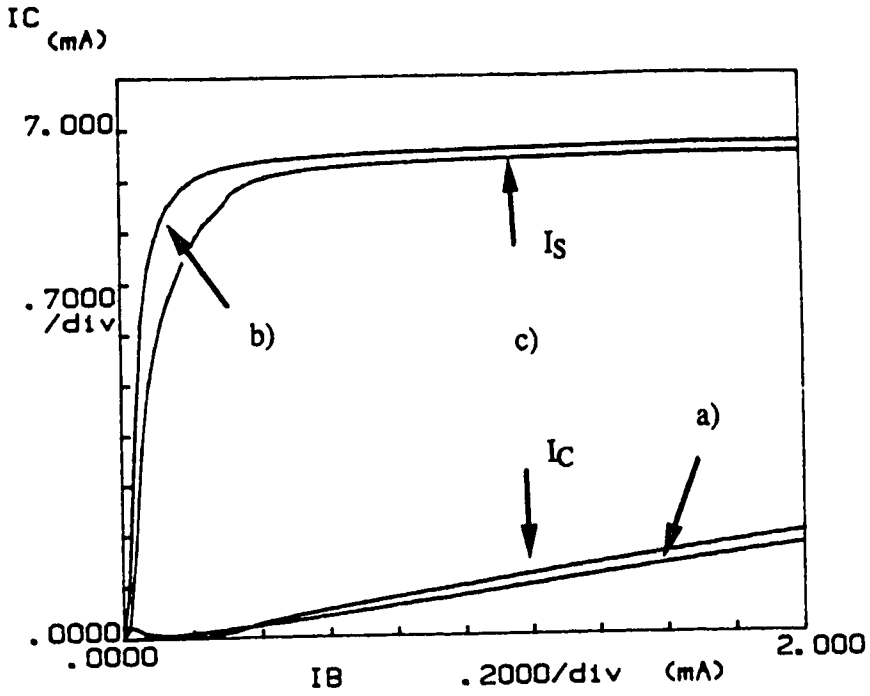


Fig.3.6 I_C and I_S versus I_B graph. a) $I_C(I_B)$ with V_S floating,i.e. only LMT is on, b) $I_S(I_B)$ with V_C floating, i.e. only the VMT is on, and c) $I_C(I_B)$ and $I_S(I_B)$ with both V_S & V_C are used, i.e. both the LMT and the VMT are on. $I_S > I_C$ and I_S reaches saturation at I_B = 0.4mA.

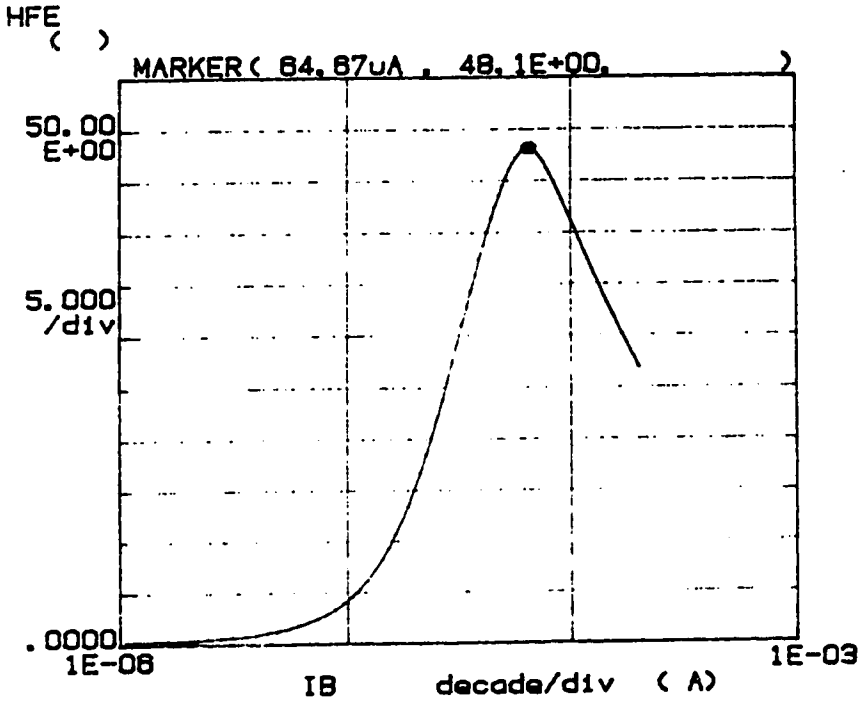


Fig.3.7 H_{FE} versus I_B graph of the VMT by itself, i.e.V_C is disconnected.

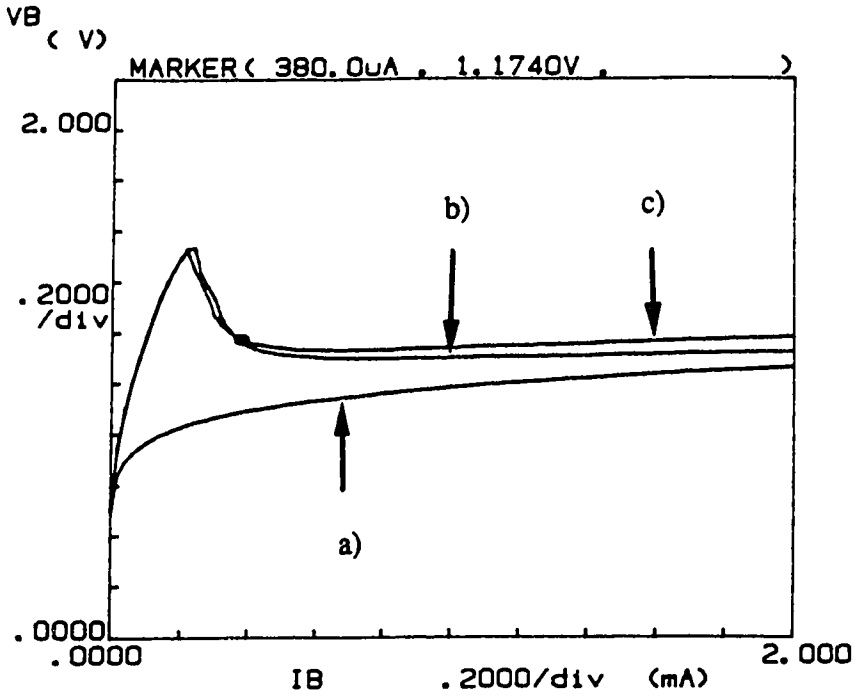


Fig.3.8 V_B versus I_B graph. a) V_S is disconnected, b) V_C is disconnected, and c) V_S & V_C are both connected. Note the drop in V_B when $I_B >$ 0.25 mA for the cases b) and c).

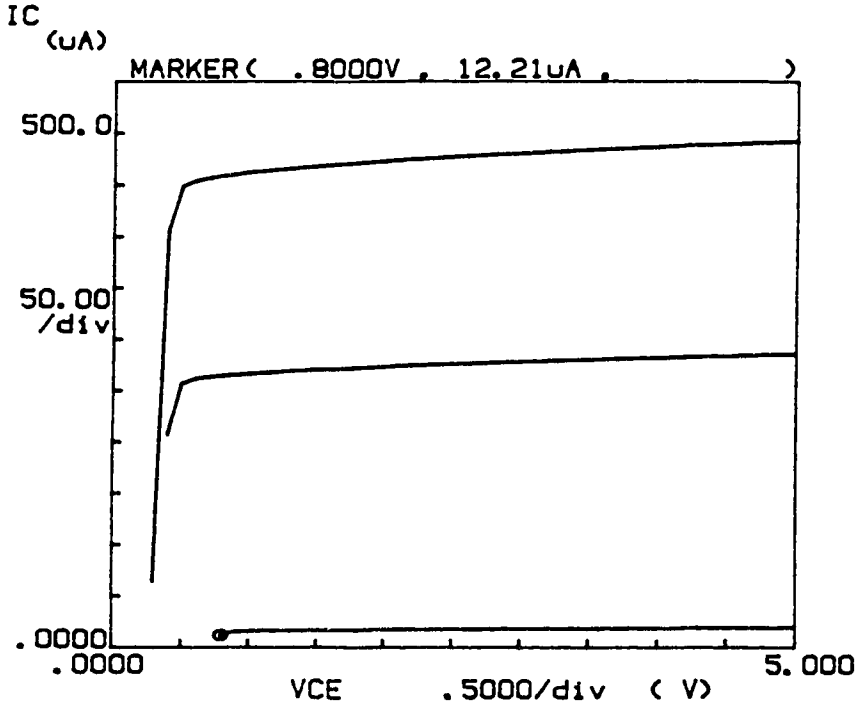


Fig.3.9 I_C versus V_{CE} graph when $V_S = 5.0V$. $I_B = 250\ \mu A \rightarrow 750\ \mu A$ in steps of 250 μA

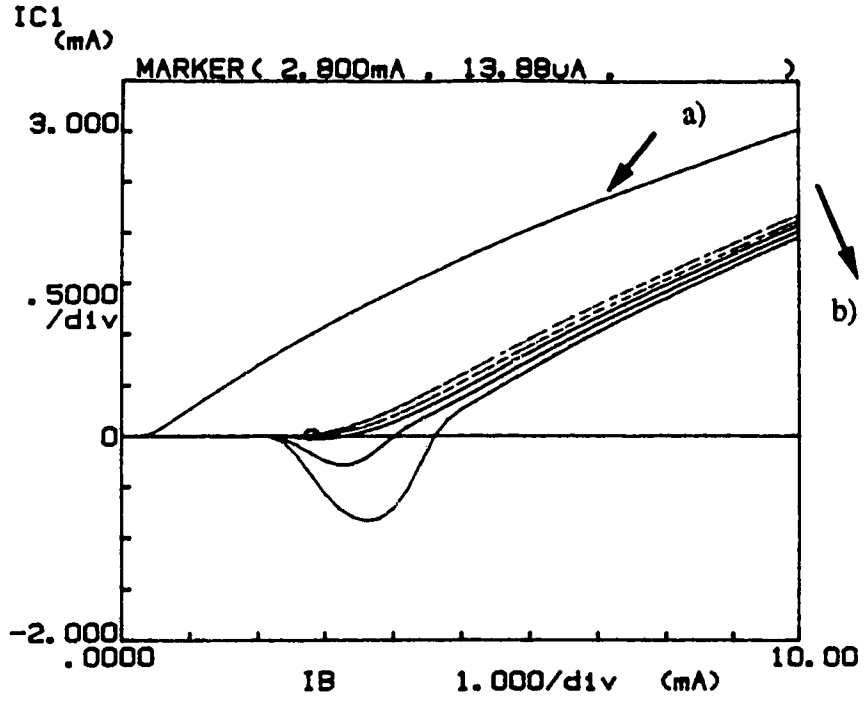


Fig.3.10 Comparison of $I_C(I_B)$ between a) V_r is floating, and b) for V_r = .1V to -.1 V in steps of 0.05V. I_C decreases as V_r becomes more negative. For example the lowest curve is when V_r = -.1 V. $V_S = V_C$ = 5.0V.

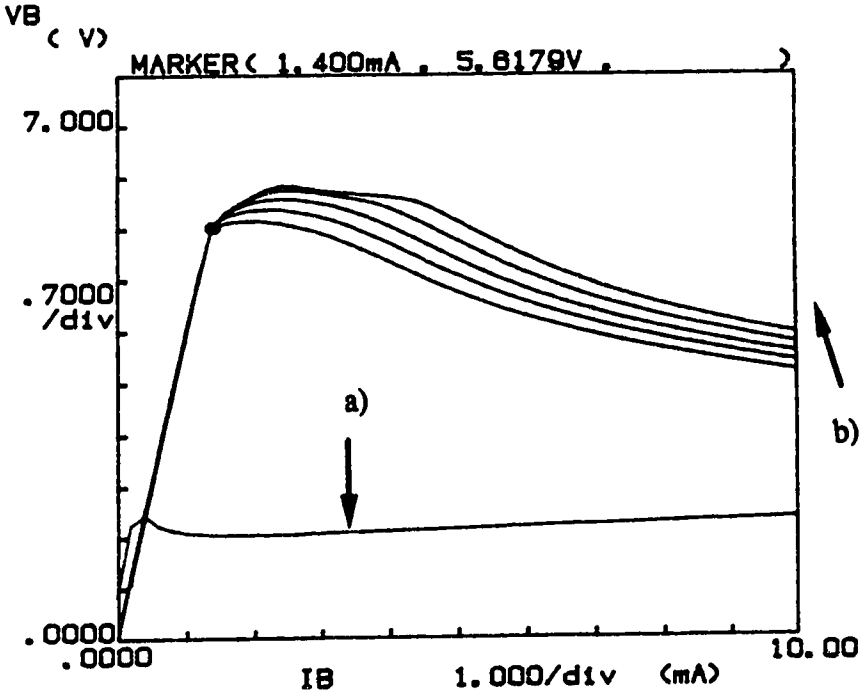


Fig.3.11 Comparison of $V_B(I_B)$ between a) V_r is floating, and b) for V_r = .1V to -.1V in steps of 0.05V. V_B increases as V_r becomes more negative. For example the highest curve is when V_r = -.1 V. $V_S = V_C$ = 5.0V.

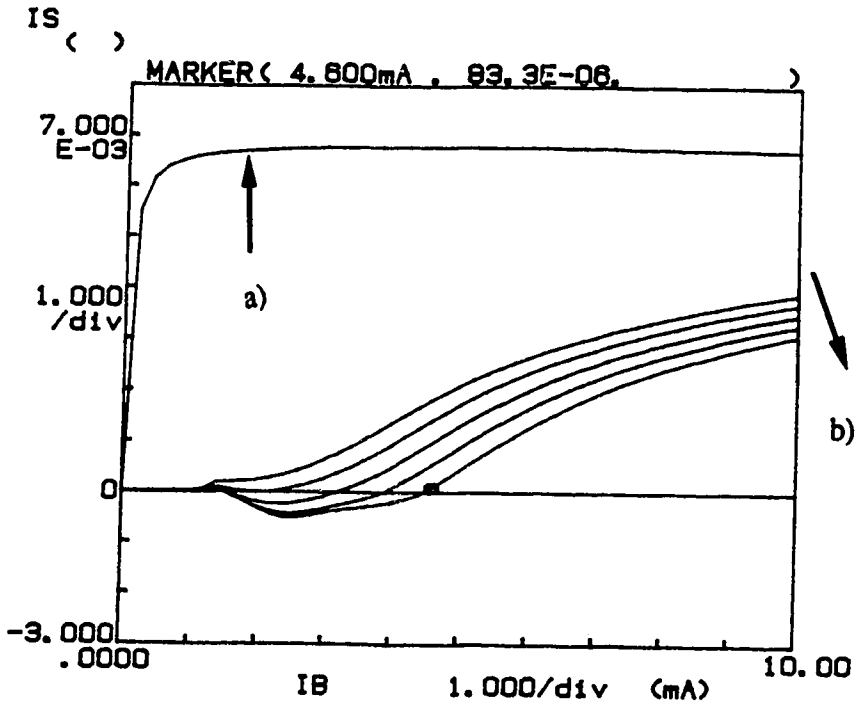


Fig.3.12 Comparison of $I_S(I_B)$ between a) V_r is floating, and b) for V_r = .1V to -.1 V in steps of 0.05V. I_S decreases as V_r becomes more negative. For example the lowest curve is when V_r = -.1 V. $V_S = V_C = 5.0V$.

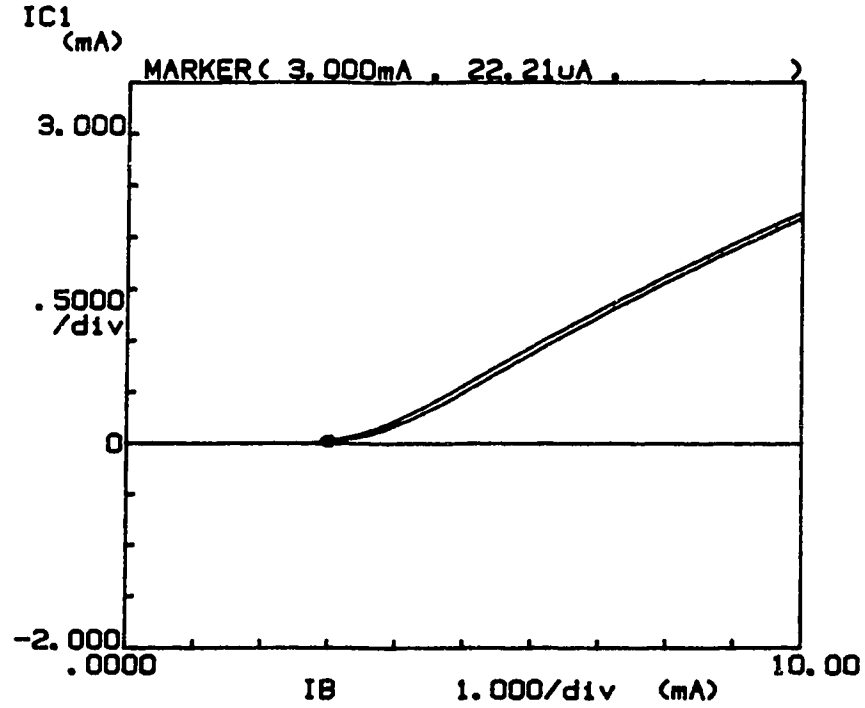


Fig.3.13 I_C versus I_B when V_C = 10.0V, V_S = 5.0V, and V_r = 0V and -0.1V.

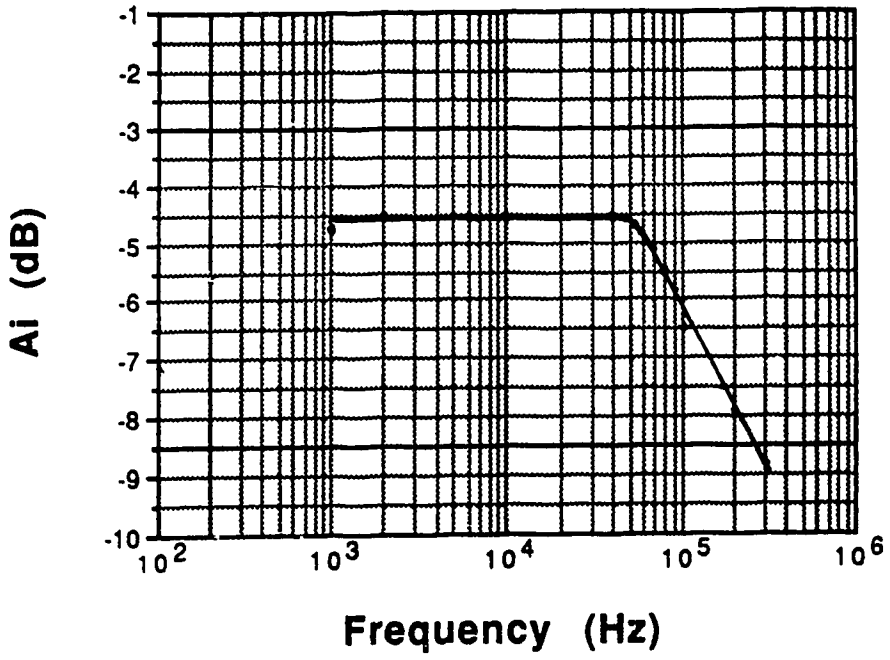


Fig.3.14 Current gain frequency response of LMT with V_S =fl, V_C = 5.0V, and I_B = 619μA.

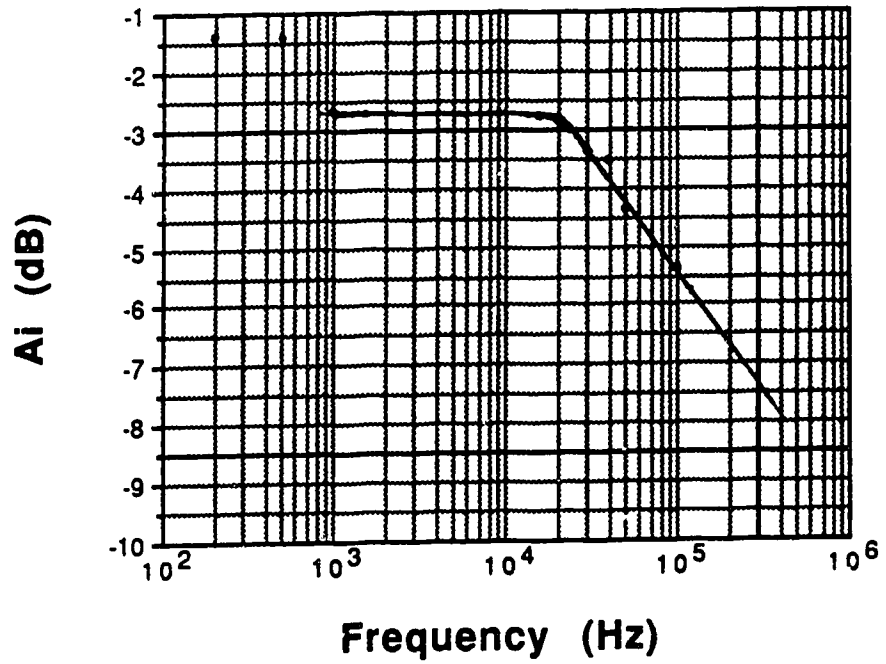


Fig.3.15 Current gain frequency response of LMT with V_S = V_C = 5.0V, and V_B = 1.226V.

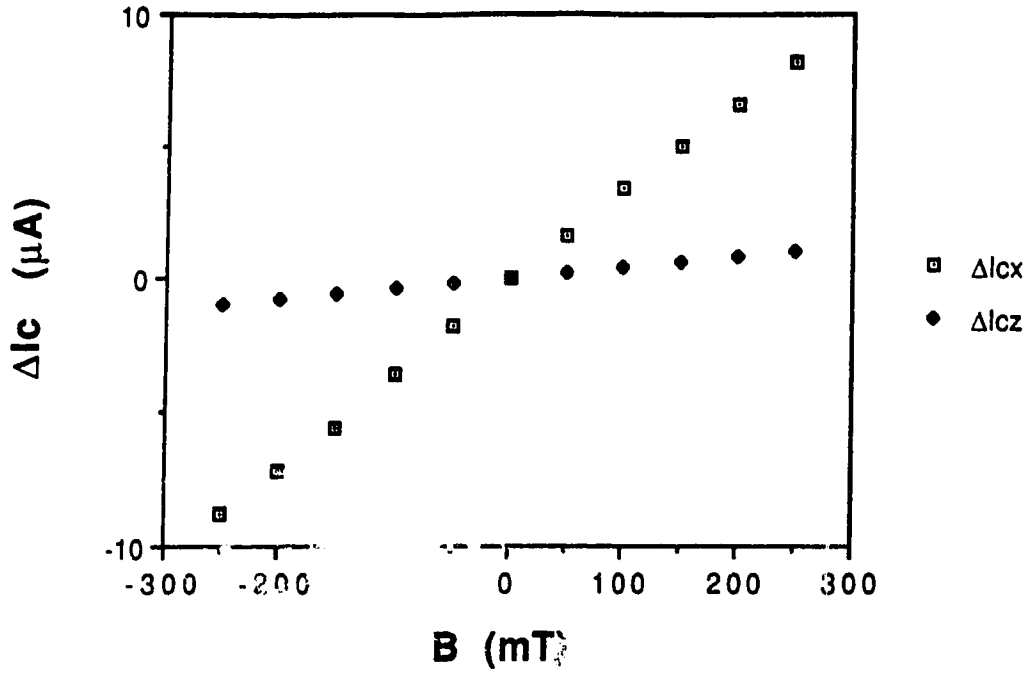


Fig.3.16 Relative change in collector current, ΔI_C, versus B. $V_C = 5.0V$, V_S is floating, and $I_B = 0.5mA$.

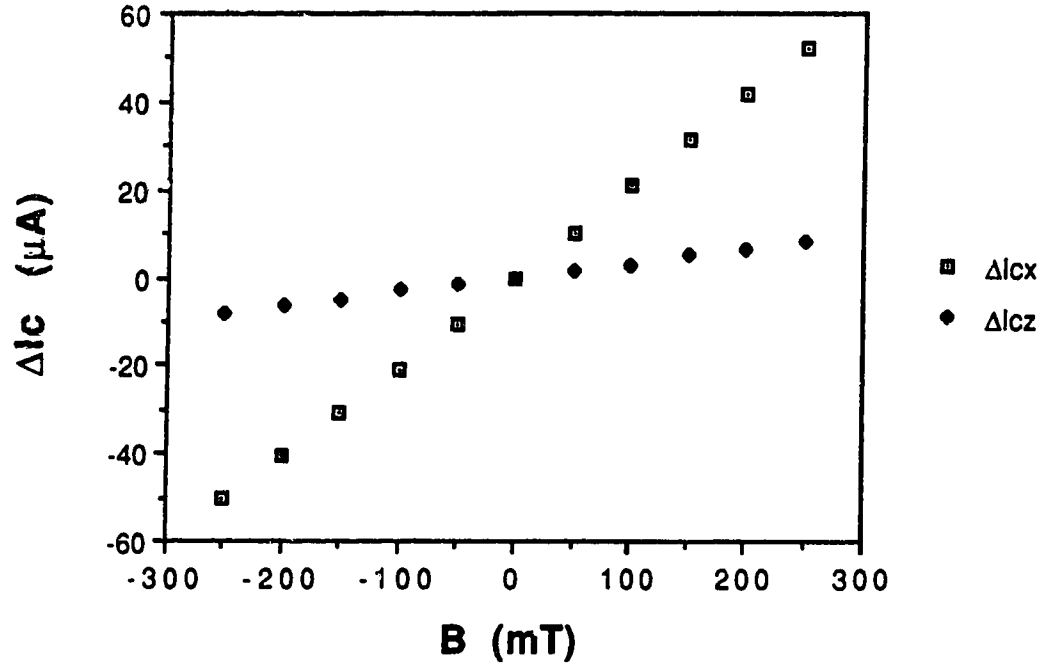


Fig.3.17 Relative change in collector current, ΔI_C, versus B. $V_C = V_S = 5.0V$, and $I_B = 0.5mA$.

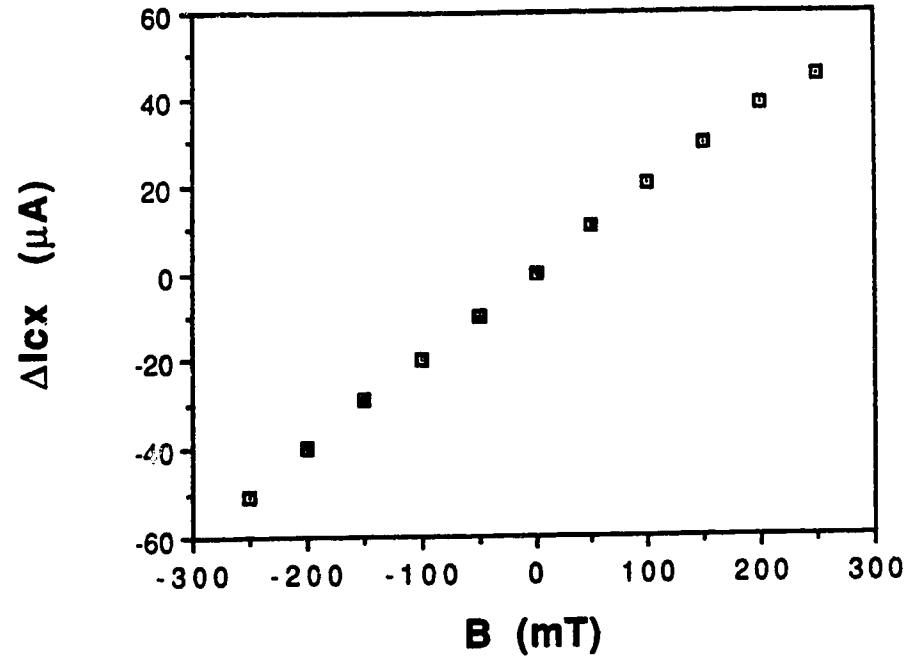


Fig.3.18 Relative change in collector current, ΔI_{CX}, versus B. $V_C = V_S = 5.0V$, $I_B = 3.5mA$, and $V_r = 0V$.

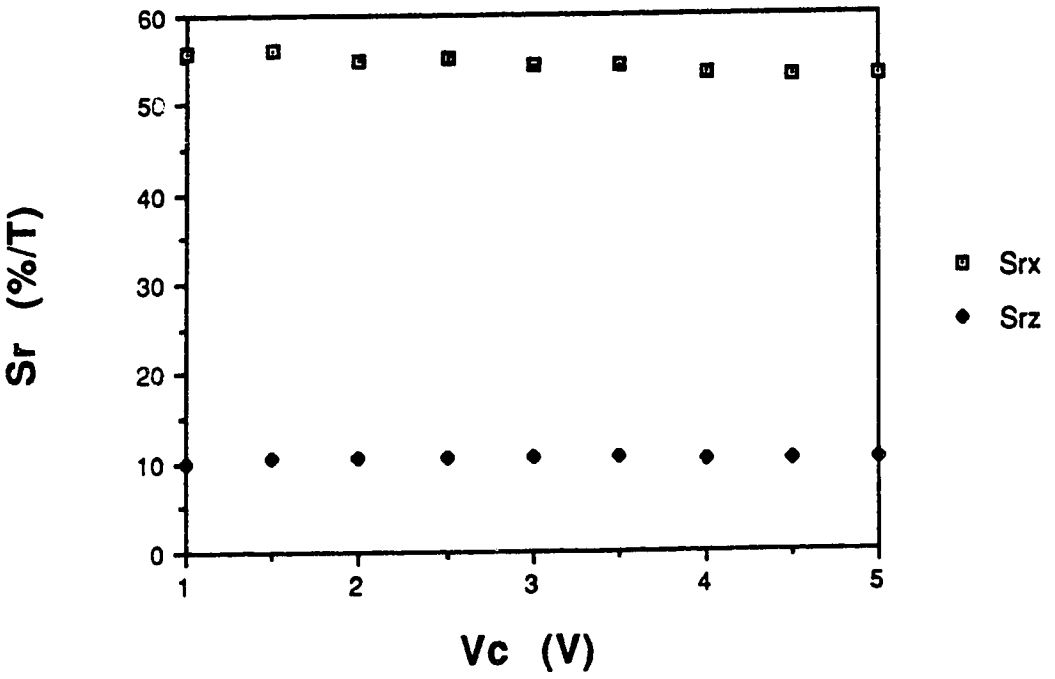


Fig.3.19 Relative sensitivity as a function of V_C. $V_S = 5.0V$, and $I_B = 0.5mA$.

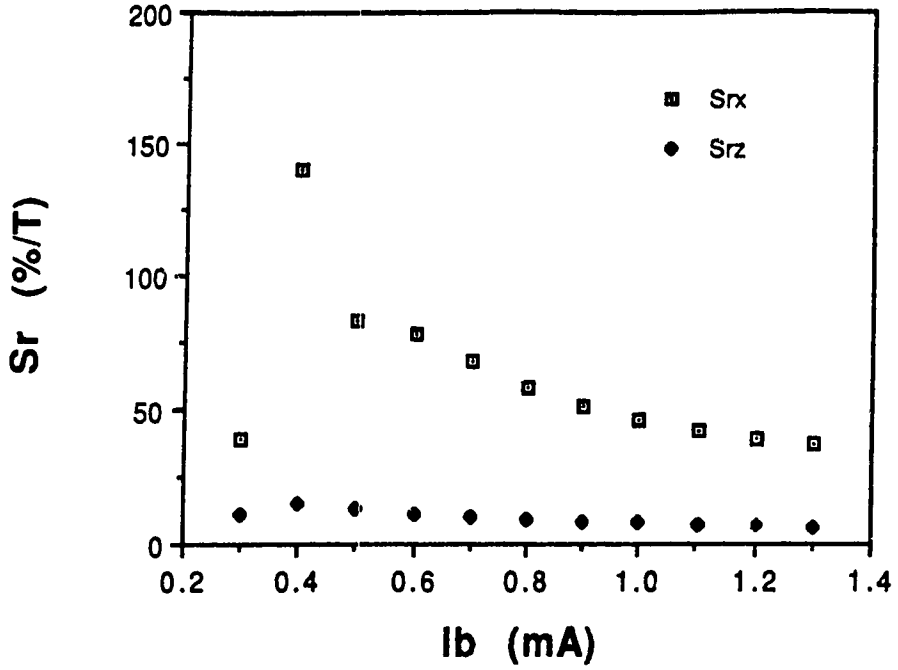


Fig.3.20 Relative sensitivity as a function of I_B. $V_C = V_S = 5.0V$, and B = 0.2mT.

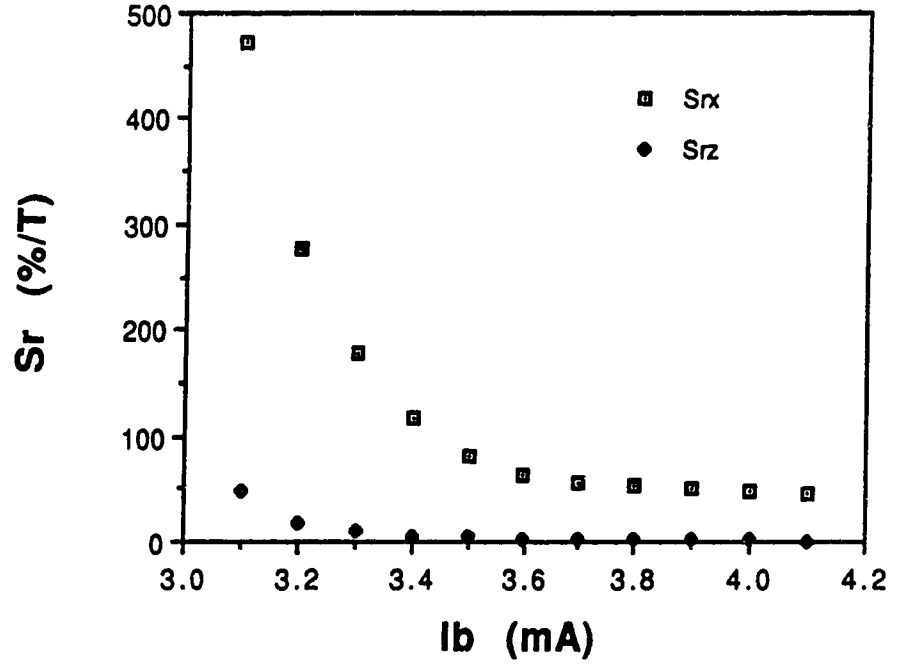


Fig.3.21 Relative sensitivity as a function of I_B. $V_C = V_S = 5.0V$, $I_B = 3.5mA$, and $V_r = 0V$.

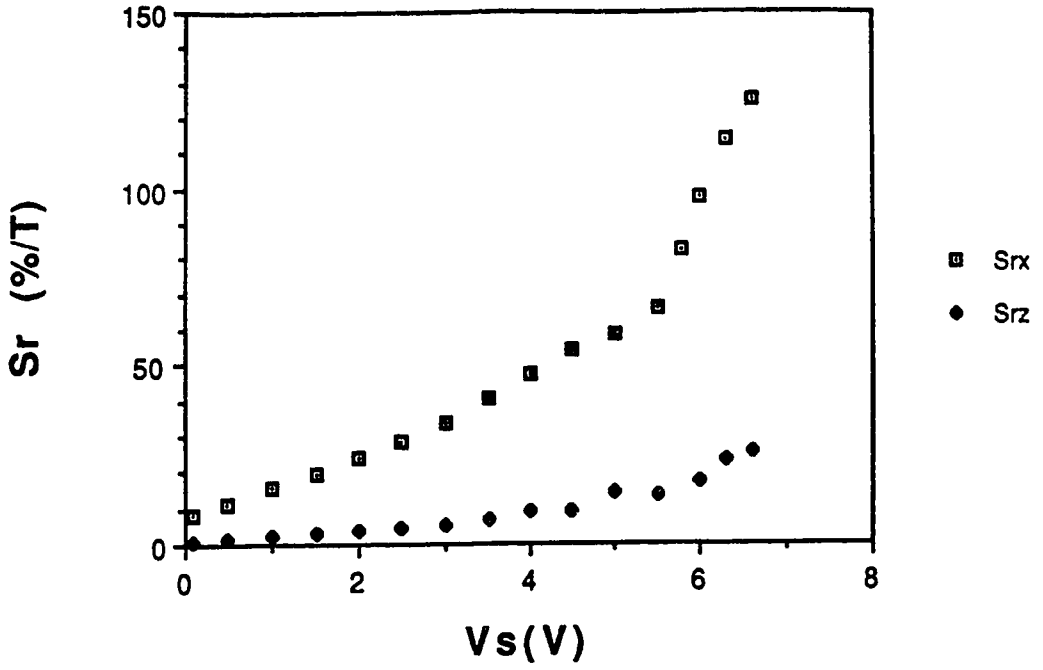


Fig.3.22 Relative sensitivity as a function of V_S. V_C = 5.0V, and I_B = 0.75mA.

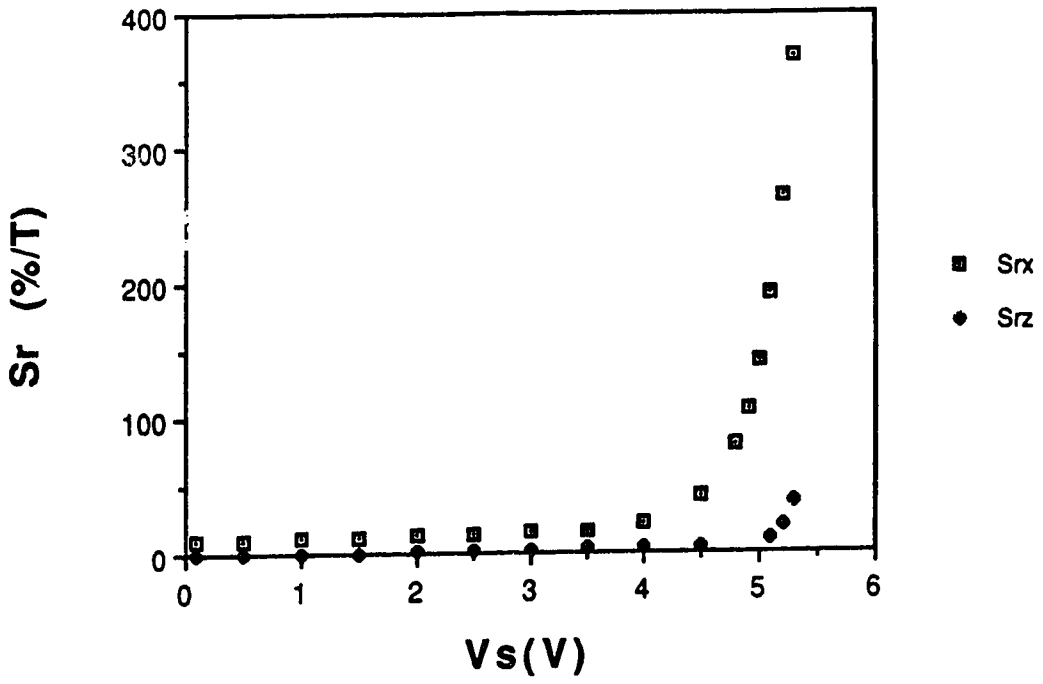


Fig.3.23 Relative sensitivity as a function of V_S. V_C = 5.0V, V_r = 0V, and I_B = 3.5mA.

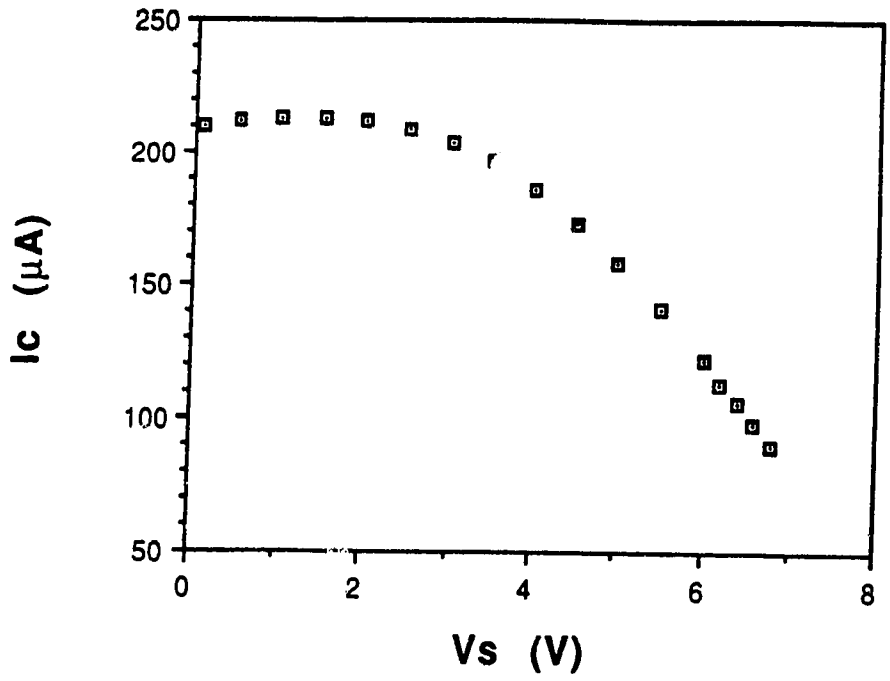


Fig.3.24 Collector current as a function of V_S. V_C = 5.0V, I_B = 0.75mA, and V_r = 0V

4. SURFACE EFFECTS

4.1 INTRODUCTION

As was mentioned earlier, the LMT uses the carriers' flow parallel to the chip surface to sense B. This flow of carriers is in the vicinity of the Si/SiO_2 interface. Any instability phenomena at the surface, therefore, will have a direct influence on the electrical characteristics and hence the magnetic sensitivity of the device. Surface effects are usually related to the presence of extra currents which originate or transit in the vicinity of the Si/SiO_2 interface. The surface currents can be introduced in a controllable manner by applying the voltage potential to the gate contact.

In section 4.2, we describe briefly how the surface effects can alter the electrical characteristics of a bipolar transistor. Experimental results and discussion of the influence of surface effects on the sensitivity of the LMT are then given in section 4.3.

4.2 THEORY OF SURFACE EFFECTS ON A TRANSISTOR

4.2.1 Surface effects and the electrical characteristics of a bipolar transistor

Most conventional bipolar transistors do not possess a gate. However, since our lateral bipolar transistor is fabricated in CMOS technology and to make the device fully compatible with the standard CMOS process, its base region is covered by a thin oxide layer and then on top of it a polysilicon gate. It becomes a so-called "gate controlled bipolar transistor." This gate can be used to investigate the surface effects.

It is known that in many devices there is a portion of the currents that is associated with the presence of generation/recombination centers at the Si/SiO_2 interface. In normal operation of a bipolar transistor, e.g. $I_C > 100\mu A$, the current associated with the surface effects is negligible as compared to the diffusion current. It only becomes important when the device is low biased, e.g. $I_C < 10\mu A$. Since it is so small and is masked by other types of currents, it is very difficult to measure its magnitude accurately. But with the gate, we can modulate the surface potential and the volume of the bulk region (i.e. there will be a field-induced space charge layer underneath the gate) and hence the magnitude of the surface current.

Let us first look at the effect of the gate potential on the base-emitter junction when it is forward biased. Fig.4.1 illustrates the cross section of a B-E junction under different gate biasing conditions. For $V_G < 0$, the base region is in accumulation of holes and electrons are pushed away from the Si/SiO_2 interface. The end results is a reduction in the dimension of the field-induced space charge layer near the interface [25]. As V_G varies from negative to positive, the base region goes from accumulation to depletion, and electrons are now attracted to the interface. The dimensions of the field-induced space charge layer thus merges with the main space charge layer (Fig.4.1.c). If we continue to increase the gate voltage, $V_G >> 0$, an inversion layer will be created (Fig. 4.1.d). For the reverse biased collector-base junction, the carriers are not injected into the depletion region but rather extracted from it. The concentration of carriers is reduced well below their equilibrium concentrations. According to Grove [25] the generation current under reverse bias is affected by the gate potential in the same percentage manner as the recombination current under forward bias. However, because the concentration of carriers in the reverse biasing condition is so small as compared to the concentration in the forward biasing condition, it follows that $I_{SF} >> I_{SR}$,

where I_{SF} is the surface recombination current for forward bias junction and I_{SR} is the surface recombination current for reverse bias junction.

Now let us analyze the influence of the surface effects on the lateral npn bipolar transistor. The first thing to be noticed is that unlike conventional gate controlled bipolar transistors, the lateral bipolar transistor with the gate structure between the emitter and collector can operate either as a MOSFET or as a BJT or both [26,27]. It becomes clearer if we look at Fig.4.2. If V_G is positive and greater than V_{TH} (threshold voltage), then there will be an n-channel formed from the emitter to the collector (Fig.4.2d). Thus the bipolar transistor action will be violated.

For V_G positive but less than V_{TH} (Fig.4.2c), the depletion case, I_C should increase but not as dramatically as in the inversion case.

For V_G negative, the influence of the gate potential on I_C should be small because 1) any change in I_C due to G/R current in the depletion region is insignificant, and 2) a decrease of the concentration of electrons in the bulk region is small (electrons are minority carriers).

4.2.2 Surface effect and S_r

Because of the way the LMT operates, any change in I_C should affect S_r. We expect a change in S_r when V_G is negative because the electrons will be pushed away from the interface. On the other hand, when $V_G > V_{TH}$, the relative sensitivity should decline drastically because the n-channel is formed between the emitter and the collector.

4.3 EXPERIMENTAL RESULTS

The results related to the characterization of the LMT with respect to surface effects are divided in two sections: electrical characteristics and magnetic characteristics.

4.3.1. Influence of surface effects on electrical characteristics of the LMT

The typical I_C (V_{CE}) transfer characteristics measured with a) a floating gate, and b) a ground gate are depicted in Fig.4.3 and Fig.4.4. With the substrate floating, I_C decreases by a small amount, 1.4 μA. With V_S = 5.0 V, the effect is more pronounced: I_C decreases by 11 μA, which is 11/45 the original I_C. The change in V_{CE} does not appear to affect this reduction as ΔI_C stays constant for $V_{CE} > V_{CE}(sat)$. What is the reason for this reduction in I_C ? To find the answer, let us look at the equation (3.3).

The two possible parameters that could modulate I_C are W_B and V_{BE}. W_B is associated with V_{CE} and we know from the plot I_C-V_{CE} that ΔI_C is insensitive to V_{CE}. Therefore let us look at V_{BE} for the 2 cases V_G = floating and V_G = 0. Fig.4.5 shows the plot V_B versus V_{CE} and we see that V_{BE} is indeed modulated by the gate. Fig.4.6 illustrates the influence of various biasing V_G on the collector current I_C. For $V_G < 0$ V, change in I_C is very small. However for $0 < V_G < 0.5$ V, I_C increases. This is because the n channel underneath the gate from emitter (source) to collector (drain) begins to form. When V_G reaches 0.5 V and beyond, I_C now consists of the current in the channel I_D, and the regular collector current I_{CO}. So I_C increases rapidly. If the base is grounded and everything else is the same, then the bipolar action will be violated and will be replaced completely by the MOS action. Fig.4.7 illustrates this biasing scheme with V_{GS} increases from 0

to 5 V in steps of 1 V. The collector current I_{C1} is essentially the drain current I_D, and V_C represents V_{DS}.

4.3.2. Influence of surface effects on sensitivity of LMT

The relative sensitivity as a function of V_G, S_{rg}, at I_B = 300 μA is calculated and then compared to the relative sensitivity of LMT for the case when the gate is disconnected, S_{rf} (Fig.4.8). As can be seen from the plot, the relative sensitivity for negative values of V_G is increased by 10% compared to the floating gate case. Going from negative to positive gate potential, the sensitivity drops significantly in value. As we have stated earlier, the reason for this is that the bipolar transistor action is violated when the n-channel is formed between the emitter and the collector.

The combination of the surface effects with different biasing conditions, such as I_B and V_S, has been investigated. For example, Fig. 4.9 depicts S_{rx} versus I_B with V_G = 0 V and V_S increases from 4 to 6.5 V. The trend that has been previously observed in section 3.4 is present again. As I_B increases, S_r decreases; and as V_S increases, S_r increases. The combination of V_G with I_B and V_S improves the relative sensitivity unexpectedly. At V_S = 6.5 V and I_B = 0.3 mA, a peak in S_{rx} of about 500 %/T is obtained. Therefore, in real application, we could expect that the application of V_G can increase the sensitivity.

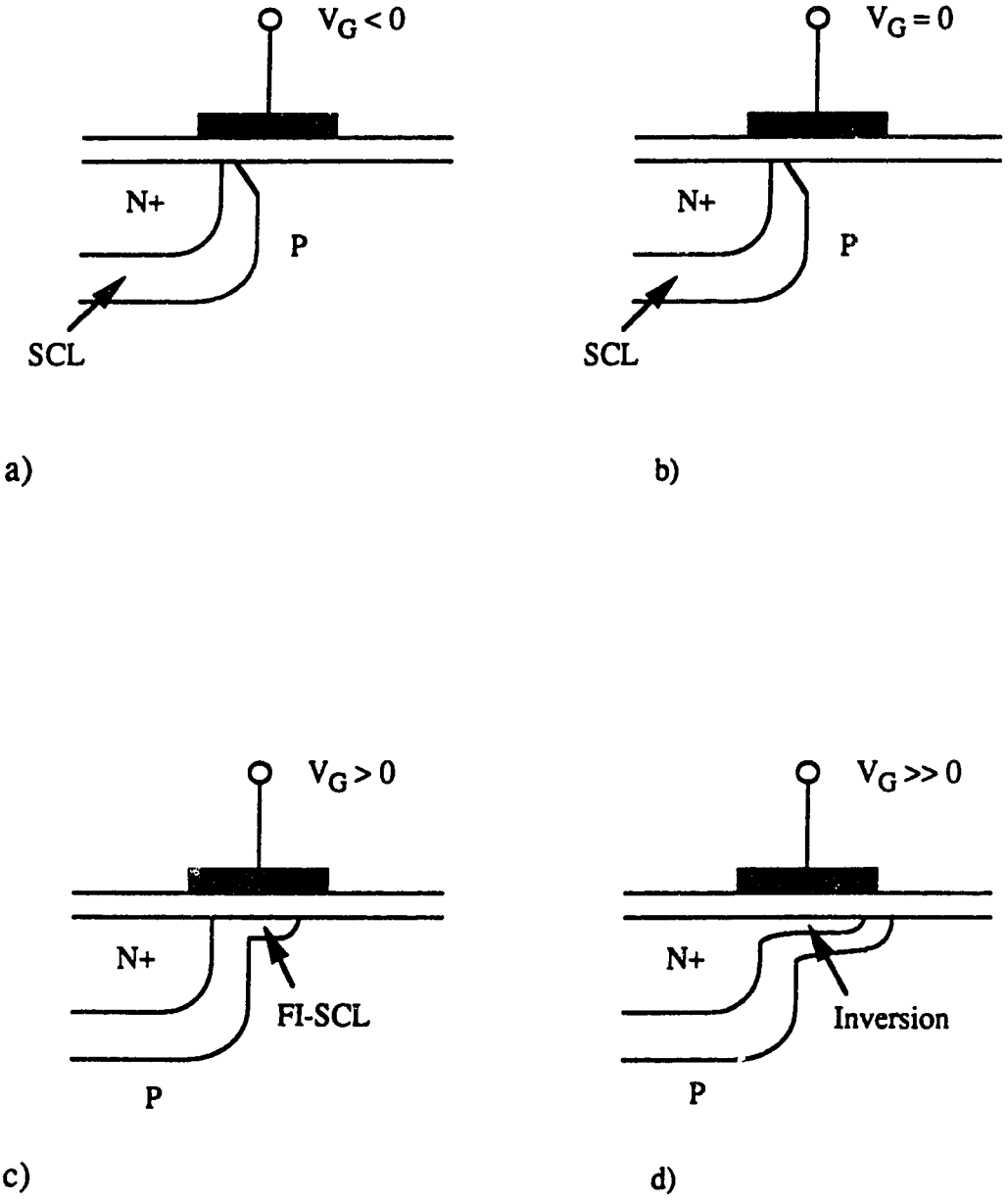


Fig.4.1 Gate controlled diode. a) accumulation case, $V_G < 0$, b) $V_G = 0$, c) depletion case, $V_G > 0$, and d) inversion case, $V_G >> 0$. SCL - space charge layer, FI-SCL - field induced space charge layer.

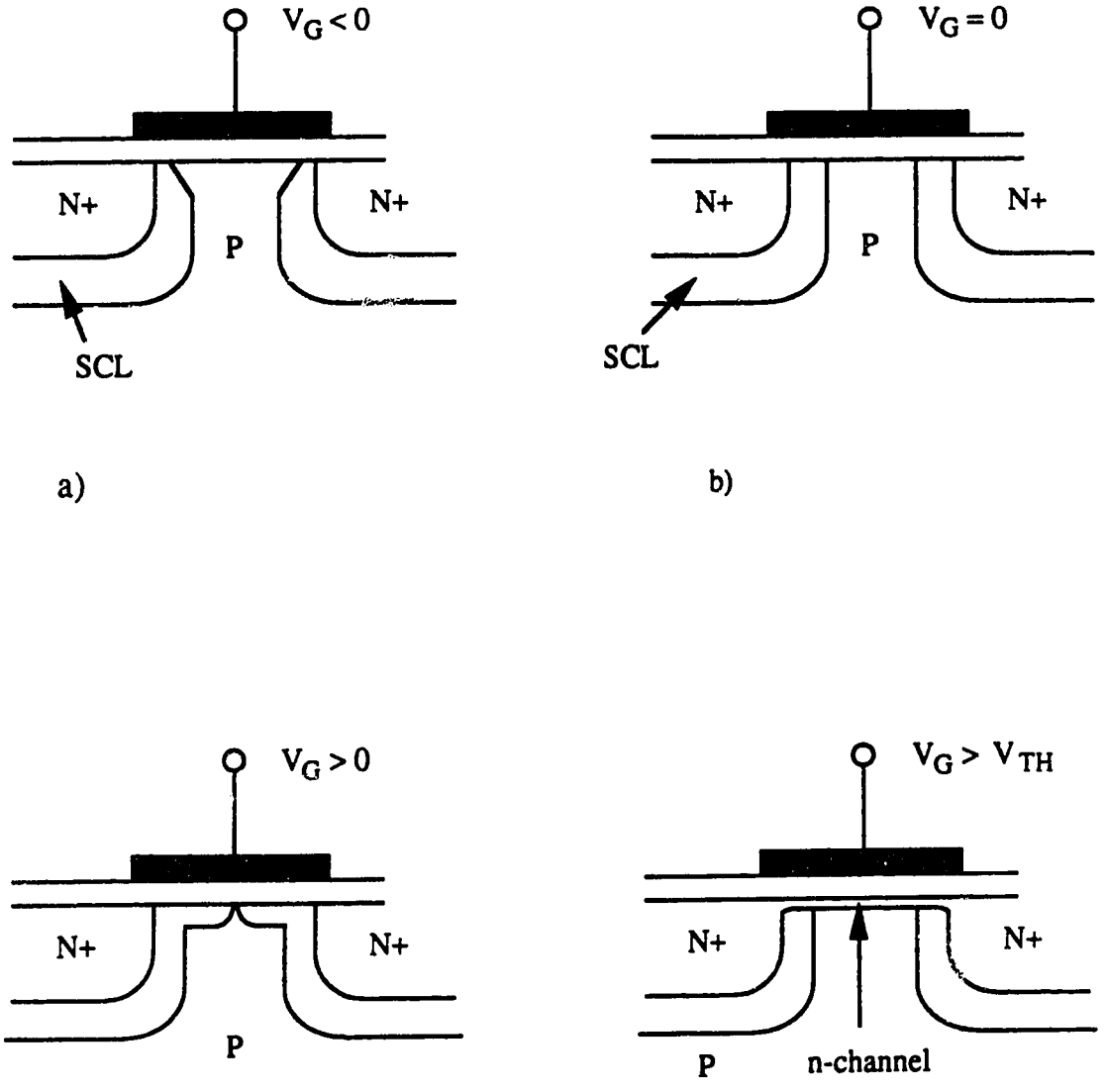


Fig.4.2 Gate controlled LMT in CMOS technology. a) accumulation case, $V_G < 0$, b) $V_G = 0$, c) depletion case, $V_G > 0$, and d) inversion case, $V_G > V_{TH}$. V_{TH} is the threshold voltage.

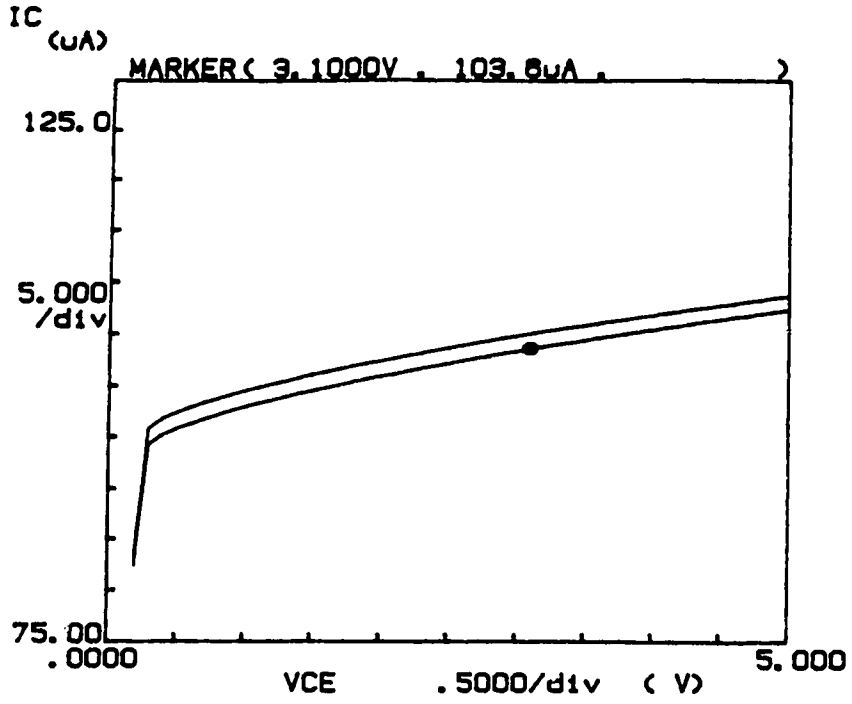


Fig.4.3 The influence of surface effects on the output characteristic. The upper curve is when the gate is floating. The lower curve is when the gate is grounded. V_C = 5.0 V, I_B = 0.5mA, and V_S is floating.

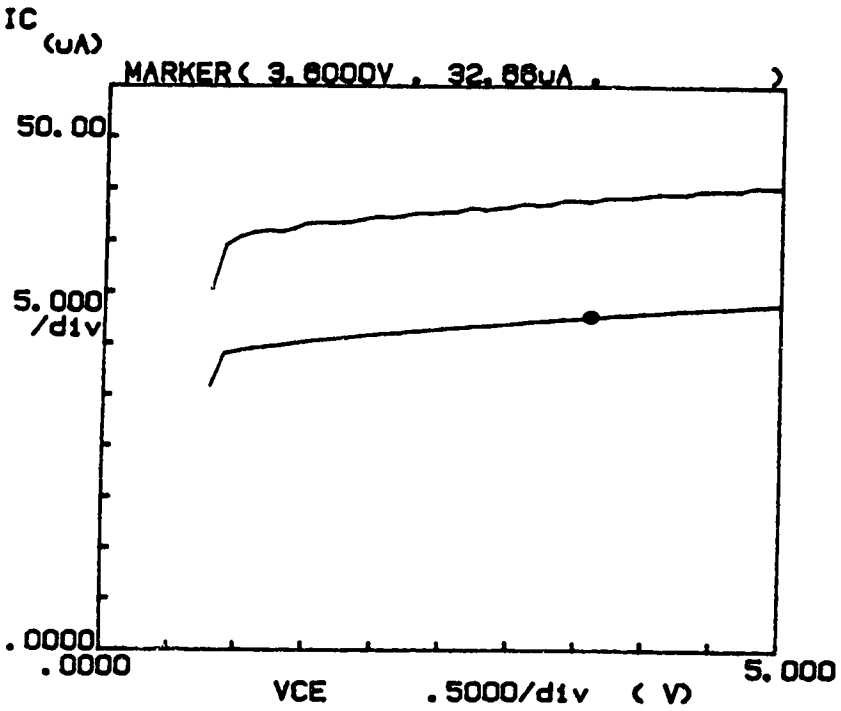


Fig.4.4 The influence of surface effects on the output characteristic. The upper curve is when gate is floating. The lower curve is when the gate is grounded. V_C = V_S = 5.0V, I_B = 0.5mA.

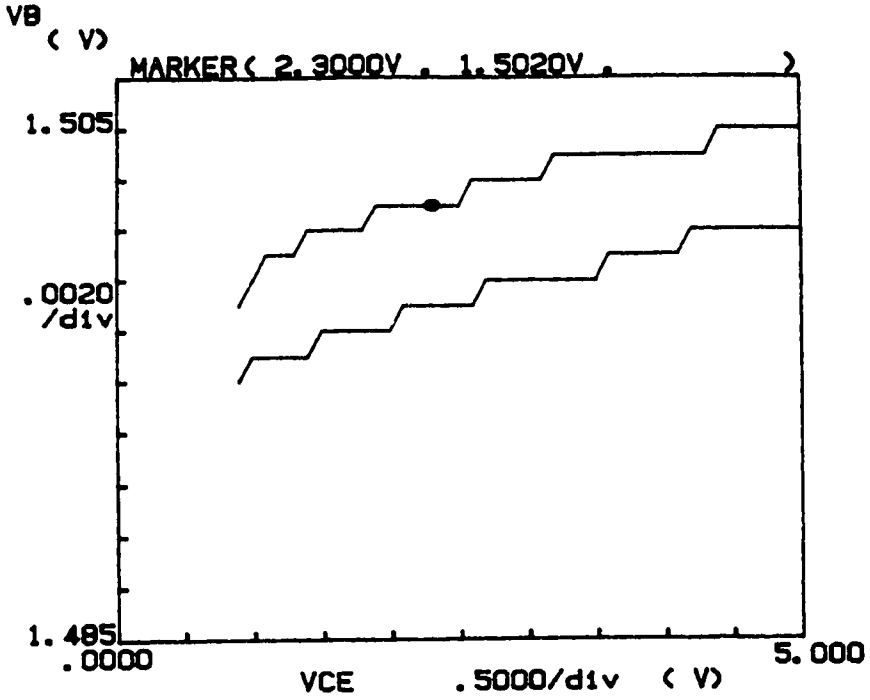


Fig.4.5 V_B versus V_{CE}. The upper curve is when the gate is floating. The lower curve is when the gate is grounded. $V_C = V_S = 5.0V$, $I_B = 0.5mA$.

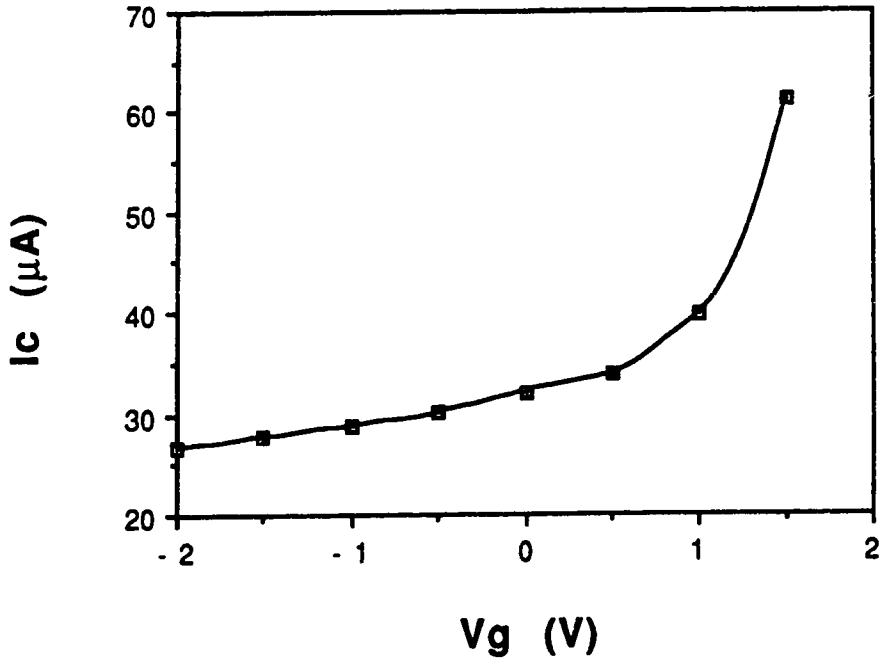


Fig.4.6 I_C versus V_G. I_C increases as V_G going from negative to positive potential. $V_C = V_S = 5.0V$, $I_B = 0.5mA$.

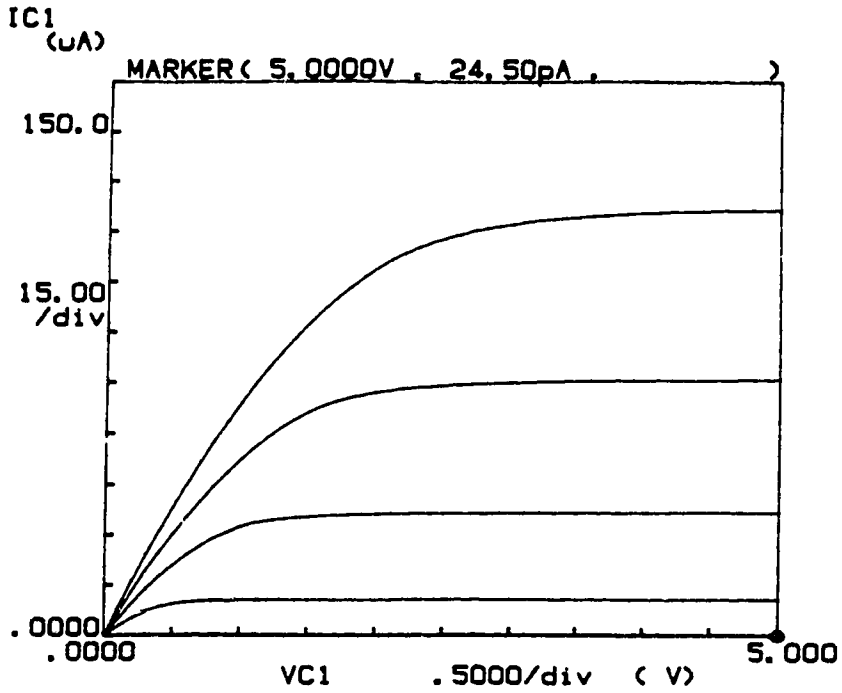


Fig.4.7 LMT operates like a MOSFET when the base is grounded. V_{GS} increases from 0 to 4V in steps of 1V.

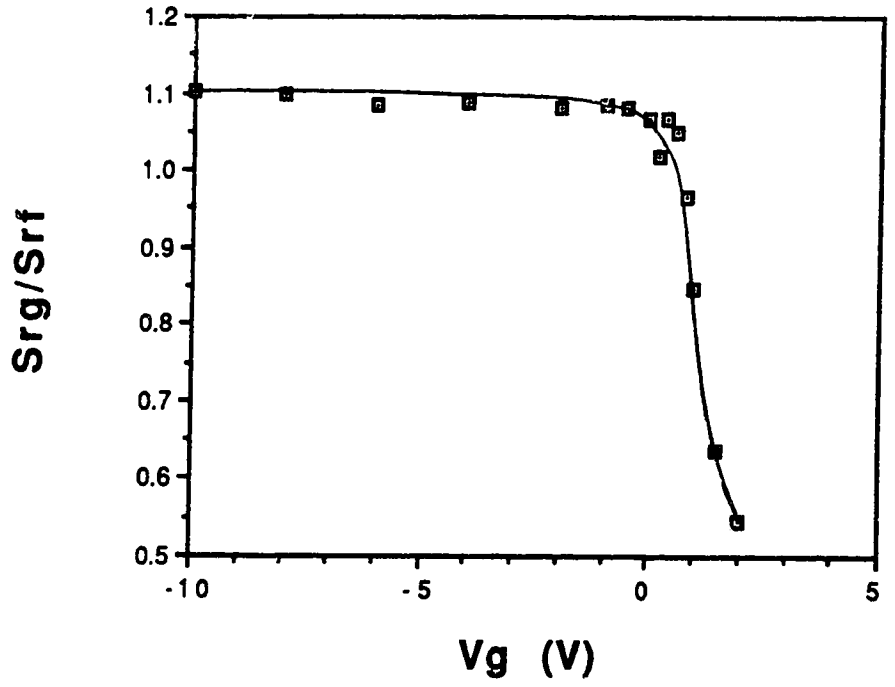


Fig.4.8 The influence of surface potential on the relative sensitivity. S_{rg} is S_r with applied potential on the gate, and S_{rf} is S_r with gate floating.

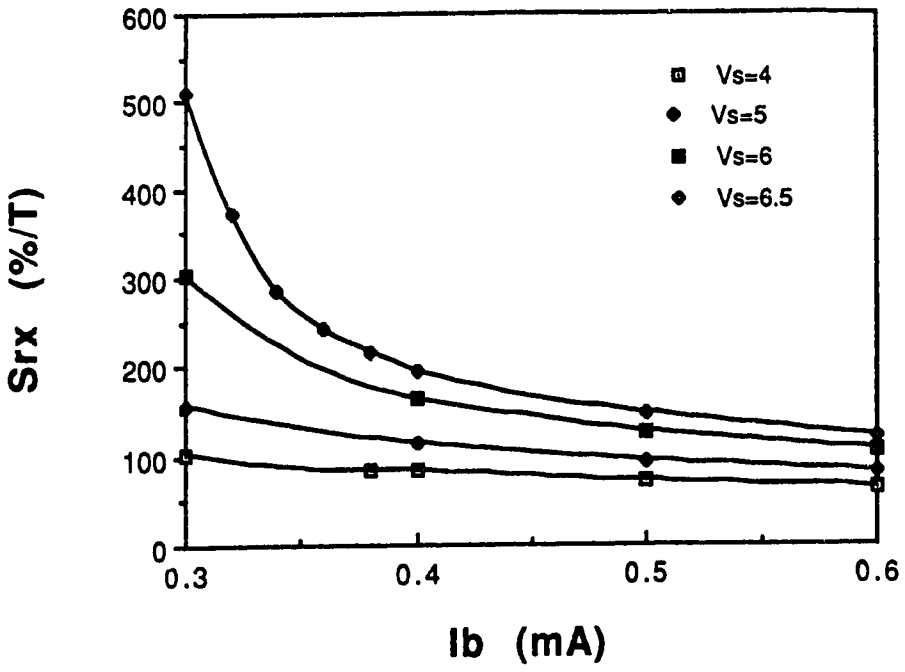


Fig.4.9 S_{rx} under various combinations of surface effects, I_B, and V_S. V_C = 5 V, and V_r = 0 V.

5. NOISE MEASUREMENTS

5.1 INTRODUCTION

In general, noise is a manifestation of the physical properties and statistical behavior of matter. Most of the time noise is regarded as detrimental to the system, and our goal is to reduce it as much as possible. In electronic devices and systems, noise exists because of the spontaneous fluctuations in the current and voltage that are generated within the system itself and also because of improper contacts which pick up external interference. Unwanted external interference can be suppressed by a careful design of the measurement system. To fully eliminate the intrinsic noise generated within the system, however, is an impossible task. We can reduce it to an acceptable level by investigating the noise sources and their corresponding magnitude. Once they are determined, perhaps we can minimize them by altering the parameters of the devices or of the systems. In doing so we may have to compromise on the device performance, such as the sensitivity of the device to the magnetic field.

In this chapter, the various electronic noise sources are considered, and the noise measurement procedure is described. Then the experimental results of the noise of single ended LMT at different biasing conditions are presented. The influence of B field on the device noise and the estimated noise correlation coefficient of differential structures are also analyzed.

5.2 NOISE SOURCES

5.2.1 Thermal noise

Perhaps the two most commonly encountered types of noise are thermal noise and shot noise. Thermal noise is associated with the random thermal motion of the charge carriers in any resistive material. As a result of this random motion, a fluctuating electromotive force V(t) is developed across the terminals of the conductor. Thermal noise was predicted by Einstein in 1906, first observed by Johnson in 1928, and subsequently formulated by Nyquist. Therefore, sometimes thermal noise can be referred to as Johnson noise or Nyquist noise.

As the name suggested, thermal noise is directly proportional to the temperature T, and theoretically as T approaches 0 K, thermal noise goes to zero. There are two ways of presenting the thermal noise in a resistor. One way is to have a noise voltage generator $\overline{v^2}$ in series with the resistor R. The other way is to have a noise current generator $\overline{i^2}$ connected in parallel with R. Thermal noise can be expressed as

$$\overline{v^2} = 4kTR\Delta f \quad (V^2) \tag{5.1}$$

$$\overline{i^2} = 4kT\frac{1}{R}\Delta f \quad (A^2) \tag{5.2}$$

$$\overline{i^2} = \frac{\overline{v^2}}{R^2} \quad (A^2) \tag{5.3}$$

where k is the Boltzman constant, T the temperature in Kelvin, R the resistance, and Δf the frequency band of consideration. At room temperature $4kT = 1.6457 \times 10^{-20}$ J

(or V.C). Dividing (5.1) and (5.2) by Δf, we obtain the spectral density that is independent of frequency. Noise with such spectra is called white noise.

5.2.2 Shot noise

Shot noise is another form of white noise. Shot noise occurs when carriers cross potential barriers independently and at random. In electronic devices, the potential barriers are the depletion layers of p-n junctions. Shot noise is also known as Schottky noise, named after Schottky who developed the theory in 1918. Its spectral density is given by,

$$S_i = \frac{\overline{i^2}}{\Delta f} = 2qI \qquad 5.4$$

where q is the electronic charge, and I the mean current. As can be seen, the spectral density is frequency independent.

Since both thermal noise and shot noise have flat frequency spectra and follow Gaussian amplitude distribution, they are indistinguishable once they are introduced into a circuit.

5.2.3 Generation-recombination noise

The other noise sources that exist are generation-recombination noise, 1/f noise, and burst noise. Generation-recombination noise occurs when free carriers are randomly generated or recombined in a semiconductor. Its location can be in the bulk region where the creation or annihilation of hole electron pairs causes a perturbation in minority carrier distribution, or at the surface, or in the depletion

layer where random trapping and detrapping of carriers by Shockley-Hall-Read-recombination centers in the forbidden energy band gap of the semiconductor produces a current fluctuation at the output terminals. For a single time constant G-R process, the expression of G-R noise can be written in the form

$$S_i(f) = 4\Delta N^2 \frac{\tau}{1 + w^2\tau^2} \qquad 5.5$$

where ΔN^2 is the variance of N numbers of carriers, τ the time constant of the process, and w the angular frequency. Details of the derivation of (5.5) are provided in reference [28].

5.2.4 1/f noise

The noise sources mentioned above are all fairly well understood, since their theoretical models are overwhelmingly supported by experimental evidence. Unfortunately, the same can not be said for 1/f or flicker noise. Though many results have been found and various theoretical models [29-34] have been developed, its origin in general is still a mystery. The problem is that no model can adequately account for or give an entirely satisfactory explanation for many of the observed 1/f noise waveforms. There are 2 schools of thought. One claims that 1/f noise originates from the fluctuation of carriers trapping and detrapping in the space charge region, or at the oxide surface, or at dislocations [35]. The other believes that 1/f noise is the result of current fluctuations within the bulk region of the semiconductor [36]. The only common understanding is that 1/f noise is the most dominant at low frequency. Its power spectral density follows a $f^{-\alpha}$ law over a wide range of frequency. Exponent α usually varies from 0.8 to 1.4.

The question that is often posed is whether a spectrum is exactly 1/f in the range $0 < f < \infty$. Theoretically, the answer is "no" because the integral which represents the spectrum of 1/f noise diverges at both the upper and lower limits. The next question is at what frequency does the spectrum drift away from 1/f ? To find it, researchers encountered many problems simply because a) at lower limits, the time required for even one cycle of measurement is too long, i.e. 5×10^{-7} Hz requires approximately 7 weeks for one reading, and b) at higher limits say > 100 kHz, 1/f noise is often masked by white noise. Kleinpenning [37] reported that $S_V(f)$ of a noisy carbon sheet resistor is still almost 1/f at $f = 3.3 \times 10^{-6}$ Hz. The frequency at which 1/f noise is masked by white noise is called the flicker noise corner frequency.

Spectral density of 1/f noise is of the form,

$$S_i = \frac{\overline{i^2}}{\Delta f} = K\frac{I^a}{f^\alpha} \tag{5.6}$$

where K is a constant for a particular device, I the direct current, "a" a constant ranging from 0.5 to 2, and α a constant close to unity.

It is important to know that the constant K is related to the contamination and crystal defects in the semiconductor. Therefore, K varies from device to device even if they are on the same silicon wafer. However, if a number of devices from a given process were measured, an average value of K could be used to predict the 1/f noise performance of different devices fabricated from that process.

5.3 NOISE MEASUREMENT

5.3.1 Noise measurement procedure

Fig.5.1 illustrates the general block diagram of the noise measurement system that we used The device under test, the batteries, the high pass filter, and the low noise pre-amplifier (LNA) are all placed inside a shielded steel container 0.375 inch thick. This is to eliminate the EM interference. A preferred environment would be a shielded, temperature-controlled room. Batteries are used instead of an a.c. power supply to minimize the 60 x n Hz noise. The batteries are of the rechargeable, sealed lead acid type. The high pass filter has a corner frequency of 0.03 Hz. The LNA is a Brookdeal 5006 differential amplifier which can operate both as a single ended or differential amplifier. It has a fixed gain of 60 dB±0.3 dB (or 1000±1), and a bandwidth from 0.1 Hz to 1 MHz. Its input impedance is 100 MΩ in parallel with 30 pF. The input noise is typically 4nV rms/$\sqrt{Hz}$. The output of the LNA is connected to the dynamic signal analyzer HP-3561A which evaluates the noise spectra using the Fast Fourier Transform (FFT) Technique. The spectrum analyzer takes the analog signal waveform, samples it during a time interval T, repeats the process many times, and takes the average. The analyzer is very useful in a sense that we can obtain both the time and frequency measurement, and we can obtain the plot of the spectrum in question. The details of how the FFT analyzes a signal are presented in [38] . All resistors and capacitors are of low noise type. Resistors are the metal film type with a tolerance of 1%; capacitors are the metallized polyester film type. All considerations to minimize the external noise were taken, i.e. using short lead wire, soldering the joints, using coaxial cable for the output from the LNA, making proper grounding, etc.. It is assumed that in the measurements, the temperature

variations inside the container are small and have no effect on the device noise spectrum. To ensure relatively narrow band measurements, the entire span was constructed from measurements on a smaller frequency span, i.e. 1 → 100 Hz, 100 → 1 kHz, 1 kHz → 10 kHz, 10 kHz → 100 kHz. The corresponding number of average readings for each frequency span are 500, 2000, 5000, 5000. The details of error analysis are presented in [23].

The device noise was measured with the device in common emitter configuration. The collector voltage was kept constant at 5.0 V. The input noise source was the biasing base resistor R_B. All measurements were done at room temperature, T = 295 K. There were four sets of noise measurements. The first set was to investigate the noise of the single collector LMT with the substrate floating. The second set was with the Vs biased at 5.0 V. The third set was to find the noise and noise correlation of differential structures. The fourth set was to find the correlation of a split collector contact LMT. For the first two sets, the effect of B on the noise of the device was also studied.

5.3.2 Current noise spectrum

Before doing any noise measurements of the device, noise characteristics of the LNA had to be carried out first. This enabled us to determine the appropriate biasing condition of the device so that the device noise was not drowned by the amplifier noise. The device noise should be at least one order of magnitude higher than the amplifier noise. In other words, we want the amplifier noise to be negligible in all noise measurements. The amplifier noise for both single ended and differential mode with R_S = 3.3 kΩ connected between its inputs and ground is given in Fig.5.2. Therefore, we had to choose biasing conditions such that the white noise level of the device is at least 145 dB. Fig.5.3 shows a typical noise

spectrum S_{ic} (f) of the device. The biasing conditions are I_B = 0.5 mA, V_{BE} = 0.915 V, V_C = 5.0 V, and I_C = 0.227 mA. Three types of noise were observed:

a) flicker noise or $1/f^{a}$ noise for f = 1 Hz to 5 kHz

b) generation-recombination noise bumps for f = 5 kHz

c) white noise for f > 50 kHz

The white noise above 50 kHz is not just shot noise, for $2qI_C = 7.264 \times 10^{-23}$ A^2/Hz. What is the additional noise source? If we look at the small signal equivalent circuit with noise sources [39] and neglecting the 1/f noise at high frequency, we have for the current noise spectrum

$$S_{ic}(f) = \frac{\overline{v_o^2}}{\Delta f}\frac{1}{R_L^2} = g_m^2 \times \frac{r_{be}^2}{(r_{be}+R_S+r_{bb})^2} \times \frac{1}{1+\left(\frac{f}{f_c}\right)^2}\left(4kT(R_S+r_{bb}) + 2qI_B(R_S+r_{bb})^2\right) + 4kT\frac{1}{R_L} + 2qI_C \tag{5.7}$$

If we use r_{bb}, r_{be}, and f_c from the small signal analysis, we obtain S_{ic} (50 kHz) = 1.3×10^{-22} A^2/Hz. This value is very close to the measured white noise level, around 10% deviation. Apparently from equation (5.7), we can find the base spreading resistance r_{bb} from the noise measurements if R_S is small and the noise corner frequency is within the bandwidth of the LNA and of the analyzer. In [40], Unwin and Knott suggest that low frequency noise measurement techniques are perhaps the best techniques to determine r_{bb} of all type of transistors over a wide range of bias.

We also investigated the bias dependance of the device 1/f output noise. The plot of S_{ic} versus logI_C at f = 1 kHz is given in Fig. 5.4. Using equation (5.6) and taking the log on both sides of the equation, we arrive at

$$\log_{10}\left(\frac{\overline{i_c^2}}{\Delta f}\right) = \log_{10}\left(\frac{K}{f^{\alpha}}\right) + a\log_{10}(I_C) \qquad (5.8)$$

which is of the y = mx + b type of equation. So the slope of the plot is "a" and the y-intercept is K. After some numerical calculations we find that for I_C = 1 μA, a = 1.22 and K = 1.24 x 10^{-21} A^2. In theory, if a = 1, then the diffusion process is the dominant noise mechanism; if a = 2, then the generation-recombination process is mainly responsible for the device noise. Here, the formulas do not include the drift current component. However, our device is a drift-aided device and so we would expect some deviations from the values 1 and 2. The conclusion we draw from this plot is that the diffusion noise is the more dominant noise.

What happens to the device noise when V_S is used ? We would certainly . the device noise to increase because there are now a lot more carriers . cted from the emitter, i.e. I_E increases. S_{ic} (1KHz)$|_{V_S=fl}$ = 1.04 x 10^{-21} A^2/Hz, whereas S_{ic} (1KHz)$|_{V_S=5}$ = 1.54 x 10^{-20} A^2/Hz when I_B = 0.5 mA in both cases. Hence, the results confirm our expectation. A noise spectrum S_{ic} (f) of the device with V_S is shown in Fig.5.5. Again, 1/f noise is predominant at low frequency and white noise, which consists of thermal noise and shot noise, prevails at high frequency. The corner frequency is around 35 kHz.

5.3.3. Noise figure

Another figure of merit that is commonly found in device specifications is the noise figure, NF. The noise figure is useful in relating how much additional noise a particular transistor or amplifier has injected into a signal in going from its input to its output. As is often the case, the input noise is taken as the noise in the source

impedance and the output noise is the total noise including the noise of the source impedance. The formula for NF is usually expressed as,

$$NF\ (dB) = 10\log_{10}\left(\frac{S_{out}(f)}{4kTR_S}\right) \tag{5.9}$$

From (5.9) we see that NF varies with frequency and source impedance. Figs.5.6 and 5.7 show that the NF of the LMT varies with frequency for 2 different cases, V_S floating and V_S = 5V.

5.3.4 Noise and magnetic field

In [23], Briglio found that the spectra of a square MAGFET, when subjected to a magnetic field of 0.27 T, was indistinguishable from the zero field case. Our experimental results for the LMT give the same conclusion (Fig.5.3 and Fig.5.5).

5.3.5. Signal to noise ratio

Perhaps the most useful figure of merit for a sensor is the signal to noise ratio,S/N, which is a relative measure of the desired signal power, P_S, to the noise signal power, S_N. It is usually expressed mathematically as

$$S/N = \frac{P_S}{S_N} \tag{5.10}$$

and in decibel form as,

$$S/N = 10\log_{10}\left(\frac{P_S}{S_N}\right) \tag{5.11}$$

In our case we will use,

$$S/N = 20\log_{10}\left(\frac{\Delta I_C}{\overline{i_C}}\right)\Bigg|_{\substack{f=1KHz \\ B=1.0T}} \qquad (5.12)$$

From Chapter 3 we know that the output signal of our device varies linearly with respect to B. Therefore, ΔI_C obtained experimentally with B = 0.06 T will be extrapolated to B = 1 T by multiplying with a factor of 1/0.06. This is done because when we measure the device noise, the static magnet only generates 0.06T. When the S/N ratio equals 1, we can determine the minimum detectable field, B_{min}, of our MFS. The various S/N ratios and B_{min} of the LMT with V_S = fl and V_S = 5.0 V at different biasing I_B are given in Tables 5.1 and 5.2. We can see that the S/N ratio increases with the input current I_B. However, we must keep in mind that heat dissipation or power consumption also increases accordingly. It should be noted that the definition of the S/N ratio is the inverse of the equivalent input noise density signal, equation (1.3).

Table 5.1. S/N ratio and Bmin of LMT at f = 1 KHz and Vs = fl

Biasing Cond. I_B	200μA	500μA	900μA	1700μA
Signal: ΔIcx (μA/T)	3.16	16.40	36.80	84.00
Signal: ΔIcz (μA/T)	0.32	2.40	5.60	12.00
RMS noise (pA)	14.94	32.20	49.46	82.50
S/N for Bx (dB)	106.49	113.93	117.43	120.15
S/N for Bz (dB)	86.60	97.23	101.08	103.25
Bmin for Bx (μT)	4.74	2.01	1.34	0.98
Bmin for Bz (μT)	46.8	13.75	8.80	6.90

Table 5.2. S/N ratio and Bmin of 2 LMT at f = 1 KHz and Vs = 5V

Biasing Cond. I_B	300μA	500μA	700μA	1100μA	1500μA
Signal: ΔIcx (μA/T)	38.84	109.80	132.80	155.00	182.00
Signal: ΔIcz (μA/T)	6.38	14.40	16.80	33.00	40.00
RMS noise (pA)	201.00	124.00	97.74	103.00	112.00
S/N for Bx (dB)	105.72	118.94	122.66	123.55	124.22
S/N for Bz (dB)	90.03	101.30	104.70	110.11	111.11
Bmin for Bx (μT)	5.46	1.13	1.34	0.74	0.62
Bmin for Bz (μT)	31.50	8.61	5.82	3.12	2.80

5.4 NOISE CORRELATION IN DIFFERENTIAL LMT STRUCTURES

Differential structures are widely employed in designing analog integrated circuits because we can readily obtain the information of two different inputs. In MTs, differential structures have an advantage over single ended structures since single ended structures need some reference input to be compared with. The reference input usually is a collector current at B = 0 and has to be stored in some memory circuits. These memory circuits make the transducer more expensive. In addition, for single ended structures we must calibrate or refresh the memory cells regularly because the output signal does not stay constant over time or under different biasing conditions. On the other hand, with differential structures we do not have to worry about those above-mentioned factors because we monitor only the relative change between 2 collectors. The total output signal, I_C, of a differential structure is twice that of a single ended structure, but the relative sensitivity is the same for both structures. This is because the change in collector currents, ΔI_C, due to the applied B field is also twice as much in a differential structure as in a single ended structure. When we use a differential structure, we want to know the noise level. We also want to know if the noise between the 2 collectors is statistically dependent or independent. If the noise between the two collectors is statistically independent or uncorrelated, then the differential noise power will be double that of the single ended noise power. Therefore the S/N ratio will remain the same. For the correlated case, there are 2 situations. One is a positive correlated case where the differential noise is much smaller than the noise from a single collector, and so S/N ratio will improve greatly. The other is a negative correlated case where differential noise is much greater than single ended noise, and S/N ratio will reduce drastically.

5.4.1 Cross correlation function

The cross correlation between the 2 collectors can be expressed in either the time domain or the frequency domain. The relationship connecting the time average and power spectrum density can be derived using the Wiener-Khinchin theorem. The development of this theorem is based on the Fourier analysis technique. For example, if $v_{ni}(t)$ is the noise from an i^{th} collector, and

$$v_{niT}(t) = \begin{cases} v_{ni}(t) & -T < t < T \\ 0 & \text{elsewhere} \end{cases}$$

then its Fourier transform is

$$V_{niT}(w) = \int v_{niT}(t)e^{-jwt}dt = \int_{-T}^{T} v_{ni}(t)e^{-jwt}dt \qquad 5.13$$

If T is finite then

$$\int_{-T}^{T} |v_{ni}(t)|dt < \infty$$

which in reality is true, for energy of a system is finite. Next, using Parseval's energy theorem,

$$\int_{-T}^{T} v_{ni}^2(t)dt = \frac{1}{2\pi}\int_{-\infty}^{\infty} |V_{ni}(w)|^2 dw \qquad 5.14$$

where

$$|V_{ni}(w)|^2 = V_{ni}(w)V_{ni}^*(w)$$

and $V_{ni}^*(w)$ is the conjugate of $V_{ni}(w)$.

Dividing (5.14) by 2T, the average power P(t) in $v_{ni}(t)$ over the interval (-T,T) is obtained as

$$P(t) = \frac{1}{2T}\int_{-T}^{T} v_{ni}^2(t)dt = \frac{1}{2\pi}\int_{-\infty}^{\infty} \frac{|V_{ni}(w)|^2}{2T}dw \qquad 5.15$$

P(t) here just represents the power in one sample function and not the whole process. Therefore we have to take the expected value of P(t) to form an average power, P_{ii}, and have to form the limit as T approaches infinity.

$$P_{ii} = \lim_{T\to\infty} \frac{1}{2T}\int_{-T}^{T} E[v_{ni}^2(t)]dt = \frac{1}{2\pi}\int_{-\infty}^{\infty} \lim_{T\to\infty} \frac{E[|V_{ni}(w)|^2]}{2T}dw \qquad 5.16$$

For a wide sense stationary process $v_{niT}(t)$, $E[v_{ni}^2(t)] = \overline{v_{ni}^2}$, which is constant so $P_{ii} = \overline{v_{ni}^2}$. In frequency domain, the power density spectrum for the random process is given by

$$S_{ni}(w) = \lim_{T\to\infty} \frac{E[|V_{ni}(w)|^2]}{2T} = \lim_{T\to\infty} \frac{\overline{|V_{ni}(w)|^2}}{2T} \qquad 5.17$$

The inverse Fourier transform of this power density spectrum is the time average of the auto-correlation function of the process, Wiener-Khinchin's theorem.

$$R_{ni}(\tau) = \frac{1}{2\pi}\int_{-\infty}^{\infty} S_{ni}(w)e^{jw\tau}dw \qquad 5.18$$

Following the same procedure, we can find the cross spectral density. Now if

$$v_{n1T}(t) \leftrightarrow V_{n1T}(w)$$

$$v_{n2T}(t) \leftrightarrow V_{n2T}(w)$$

where $v_{n1T}(t)$ is the noise from collector #1, and $v_{n2T}(t)$ the noise from collector #2, then

$$P_{12} = \frac{1}{2\pi}\int_{-\infty}^{\infty} \lim_{T \to \infty} \frac{E[V^*_{n1T}(w)V_{n2T}(w)]}{2T} \qquad 5.18$$

and the cross spectral density is

$$S_{n12}(w) = \lim_{T \to \infty} \frac{\overline{V^*_{n1}(w)V_{n2}(w)}}{2T} \qquad 5.19$$

After we have established the expression for the noise power spectrum density for each collector and the cross spectral density between the two collectors, we can then proceed to find the cross correlation function in the frequency domain. The power spectral density of a differential noise $[v_{n1}(t) - v_{n2}(t)]$ is

$$[v_{n1}(w) - v_{n2}(w)][v_{n1}(w) - v_{n2}(w)]^* = v_{n1}(w)v_{n1}^*(w) + v_{n2}(w)v_{n2}^*(w) - 2\mathrm{Re}(v_{n1}(w)v_{n2}^*(w)) \qquad 5.20$$

The average power spectral density, $S_D(w)$, becomes

$$S_D(w) = \overline{[V_{n1}(w)-V_{n2}(w)][V_{n1}(w)-V_{n2}(w)]^*} = S_{n1}(w) + S_{n2}(w) - 2\mathrm{Re}[S_{n12}(w)] \qquad 5.21$$

where $\mathrm{Re}[S_{n12}(w)]$ represents the real part of $S_{n12}(w)$. If the two noise signals are uncorrelated, then $2\mathrm{Re}[S_{n12}(w)] = 0$. For partial correlation between two noise signals, we divide (5.21) by $(S_{n1}(w) + S_{n2}(w))$ and then rearrange the equation to get a cross correlation function in frequency domain, $\Gamma(w)$

$$\Gamma(w) = \frac{2\mathrm{Re}[S_{n12}(w)]}{[S_{n1}(w) + S_{n2}(w)]} = 1 - \frac{S_D(w)}{[S_{n1}(w) + S_{n2}(w)]} \qquad 5.22$$

Γ ranges from -1 to 1.

The time average cross correlation function, γ, can not be obtained from inverse Fourier transform of (5.22) using Wiener-Khinchin's theorem because the imaginary part of $S_{12}(w)$ is lost. Instead, it can be found by measuring the rms noise voltage in the time domain. By assuming that 1/f noise, shot noise, and thermal noise follow Gaussian probability distribution [41], we have

$$\overline{(v_{n1}(t) - v_{n2}(t))^2} = \overline{v_{n1}^2(t)} + \overline{v_{n2}^2(t)} - 2\overline{v_{n1}(t)v_{n2}(t)} \qquad 5.23$$

and

$$\gamma = \frac{2\overline{v_{n1}(t)v_{n2}(t)}}{\overline{v_{n1}^2(t)} + \overline{v_{n2}^2(t)}} = 1 - \frac{\overline{(v_{n1}(t) - v_{n2}(t))^2}}{\overline{v_{n1}^2(t)} + \overline{v_{n2}^2(t)}} \qquad 5.24$$

γ also ranges from -1 to 1.

5.4.2 Differential noise in LMT

Using the same experimental set up as in 5.3, we tested a differential pair LMT shown in Fig.5.8, and a differential LMT shown in Fig.5.9. The testing was done for both structures in single collector mode and differential mode. The results are shown in Figs.5.10 and 5.11. For both structures, the P.S.D. differential noise is on average 3 dB higher than the single ended P.S.D. noise. Although the results are not presented in the Figs.5.10 and 5.11, we have found that the P.S.D. voltage noise from one collector is the same as from the other collector. This is to be expected because of the symmetry of the devices' geometries and because of the same operating conditions. This result transform the simplified equations (5.22) and (5.24) into

$$\Gamma(w) = 1 - \frac{S_D(w)}{2S_{n1}(w)} \qquad 5.25$$

$$\gamma = 1 - \frac{\overline{(v_{n1}(t) - v_{n2}(t))^2}}{2\overline{v_{n1}^2(t)}} \qquad 5.26$$

Converting dB values back to V^2/Hz and applying (5.25) we find $\Gamma = 0$ for both structures. This means that there is no correlation between the two collector noise voltages in differential LMT structures. To double check this statement, we measured the noise in the time domain. The plots of the time averaging noise versus time for both structures, in single ended and differential mode, are given in Fig.5.12 and Fig.5.13. By inspection of the graphs, we can see that the differential noise is on average twice as much as the noise from a single collector. A rough estimation was taken by considering only the thickness of the waveforms. For example, in Fig.5.12 there is about 15 mV above and below the 0.0 V line for the single LMT, and about 30 mV above and below the 0.0 V line for the differential pair. Applying (5.26), γ is found to be close to 0 for both structures. The results obtained here are opposite to the results presented in [42].

At this point, it is worth mentioning that there is no definite answer regarding the collector 1/f noise in silicon bipolar transistors. The few attempts to prove or disprove its existence have failed [43, 44]. There are also results that suggest that the collector noise is just the amplified base noise source [33, 34]. The results published in [42] identify the emitter-base junction as a source of 1/f noise. At the same time, the results presented in [42] show that the differential noise voltage is 40 to 50 dB less than the noise of the single ended counterpart, and the correlation coefficient is close to 1.

What could be the explanation for the discrepancy between the results obtained here and the results published in [42]?

If the logic implied in [42] were followed here, then for the structure shown in Fig.5.9 the differential noise should be lower than the single ended noise, because it also has only one emitter-base junction. But that is not the case. The higher differential noise for the lateral structures can be attributed to the base region and to the collector-base junctions. In both structures, Figs.5.8 and 5.9, there are two collector-base junctions as compared to the one collector-base junction of the vertical transistors presented in [42], Fig.5.14. In both of our cases, the differential noise is higher.

We believe that this explanation is equally applicable to the results presented in [42]. The analyzed structures in [42] are not "real" differential structures, because there is only one collector-base junction in each of the differential structures, and the collector current is split between the two collector contacts. The strong correlation found there represents the correlation of the collector signal with itself; therefore the "differential" noise voltage is smaller.

In order to prove our assumptions, we have designed a single lateral magnetotransistor with split collector contact (C' and C"), Fig.5.15. This LMT was tested in single ended mode (using either C' or C"), and in differential mode (measuring the noise signal between C' and C"). The results are shown in Fig.5.16. The results for C' and C" are identical and denoted as $S_{11}(w)$ and $S_{22}(w)$, respectively. As can be seen, the "differential" noise, $S_D(w)$, in this case is much lower than the single ended noise. We also found that the correlation coefficient in this case was close to 1. These results are similar to the results obtained in [42].

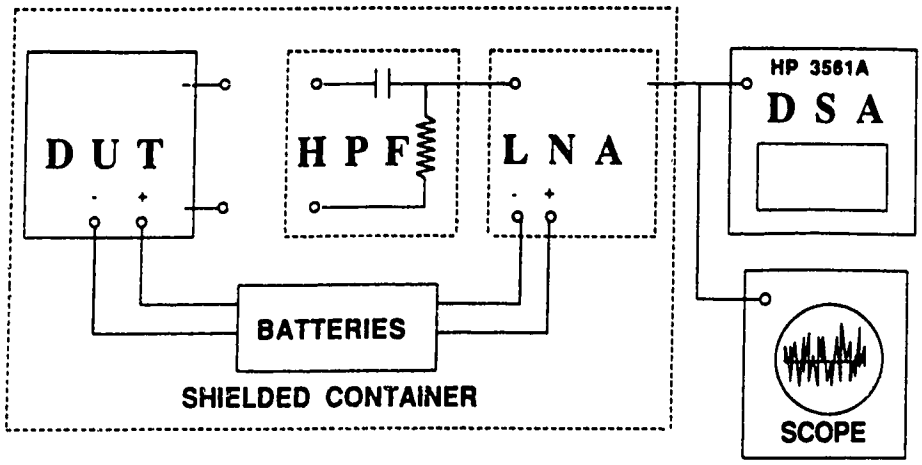


Fig.5.1 Schematic of the noise measurement system. High pass filter (HPF) has a corner frequency of 0.03 Hz.

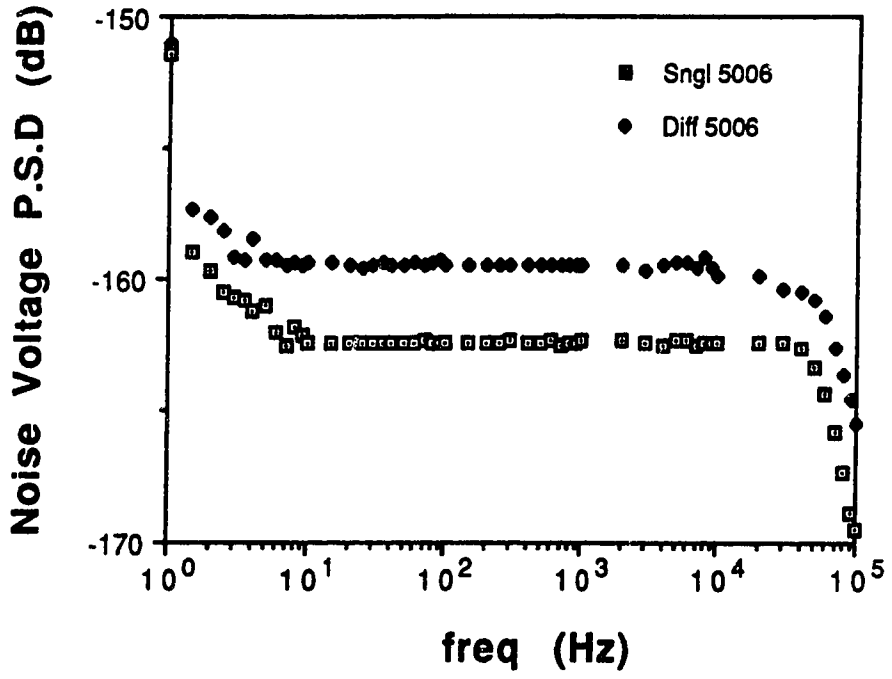


Fig.5.2 Voltage noise of a Brookdeal linear differential amplifier 5006. The differential noise is on average 3dB higher than the single ended noise. Input resistance R_S is 3.3 KΩ.

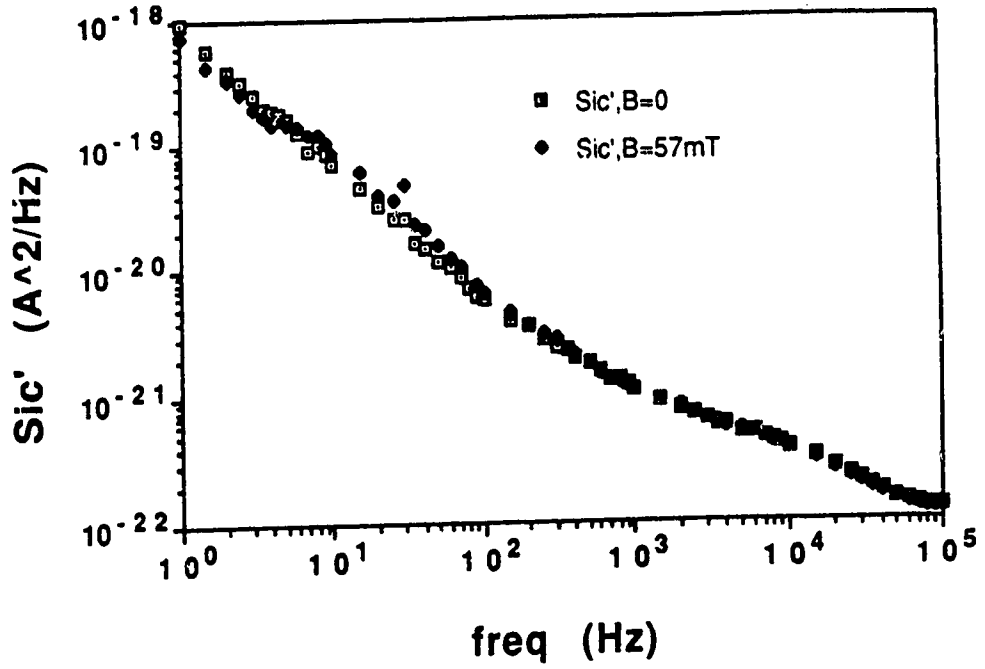


Fig.5.3 Output current noise $S_{ic'}$ spectrum. I_B = 0.5mA, V_B = 0.915V, I_C = 0.227mA, and V_C = 5.0V.

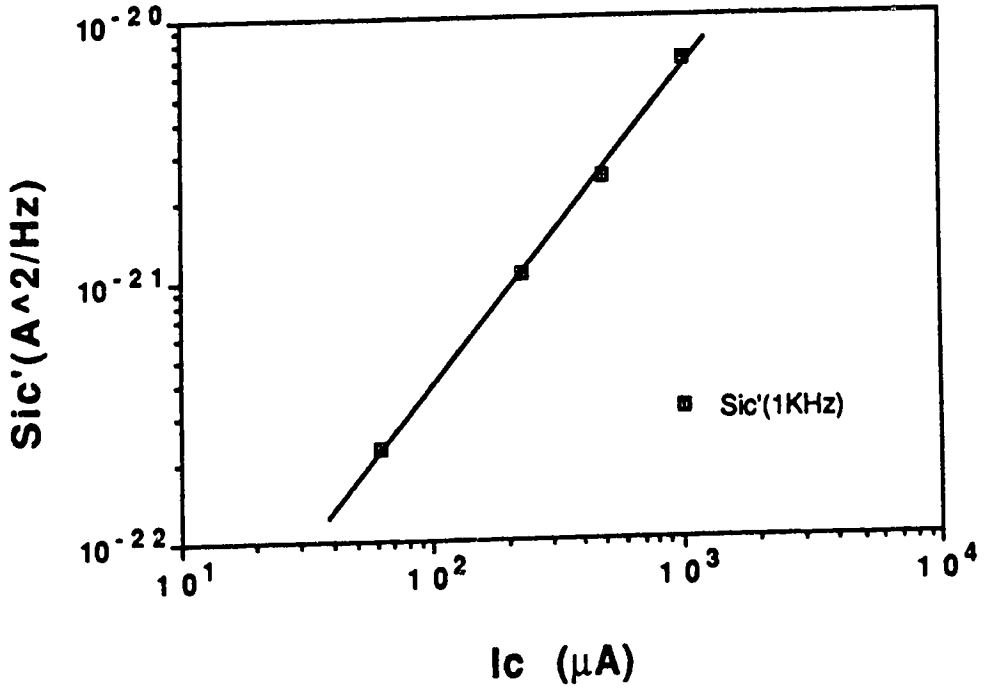


Fig.5.4 $S_{ic'}$ versus logI_C. I_B = 0.2mA, 0.5mA, 0.9mA, and 1.7mA. V_S = floating, and f = 1kHz.

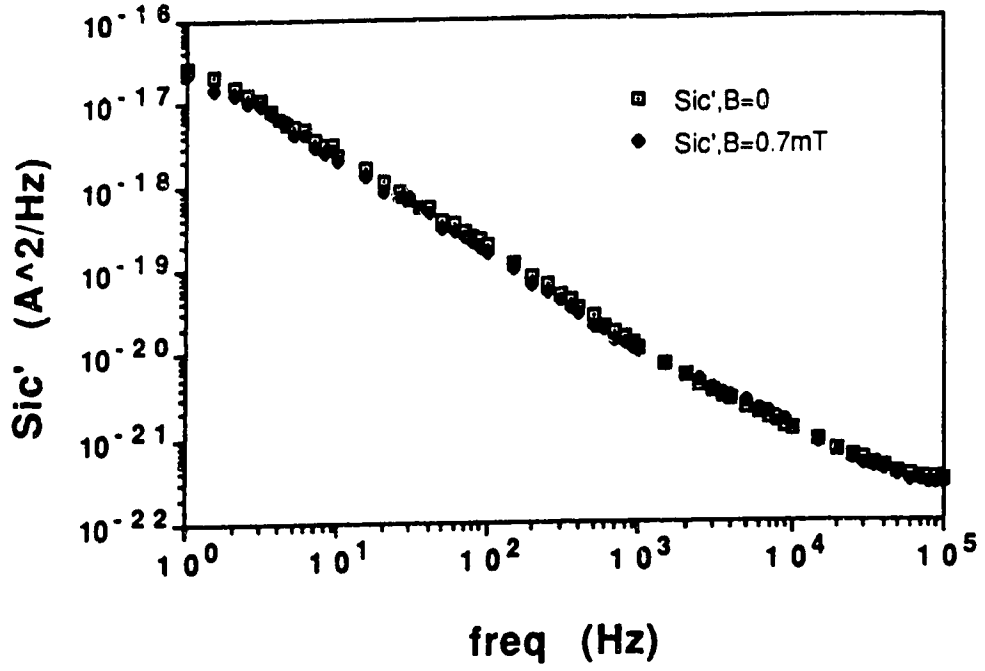


Fig.5.5 Output current noise $S_{ic'}$ spectrum with $V_S = V_C = 5.0V$, $I_B = 0.7mA$, $V_B = 1.138V$.

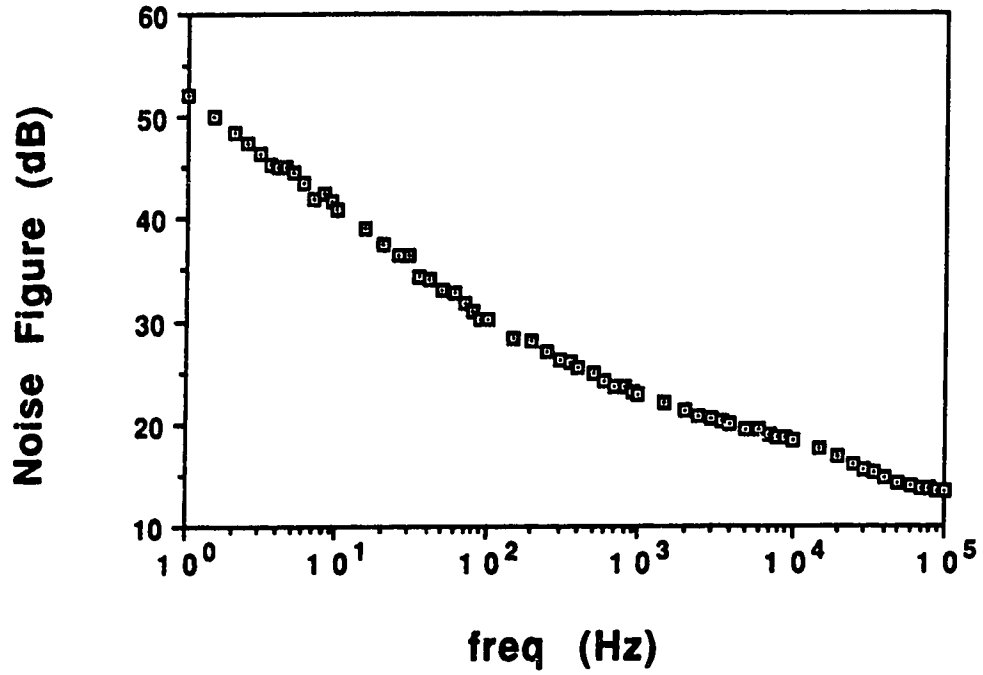


Fig.5.6 Noise figure spectrum for the case when V_S is disconnected.

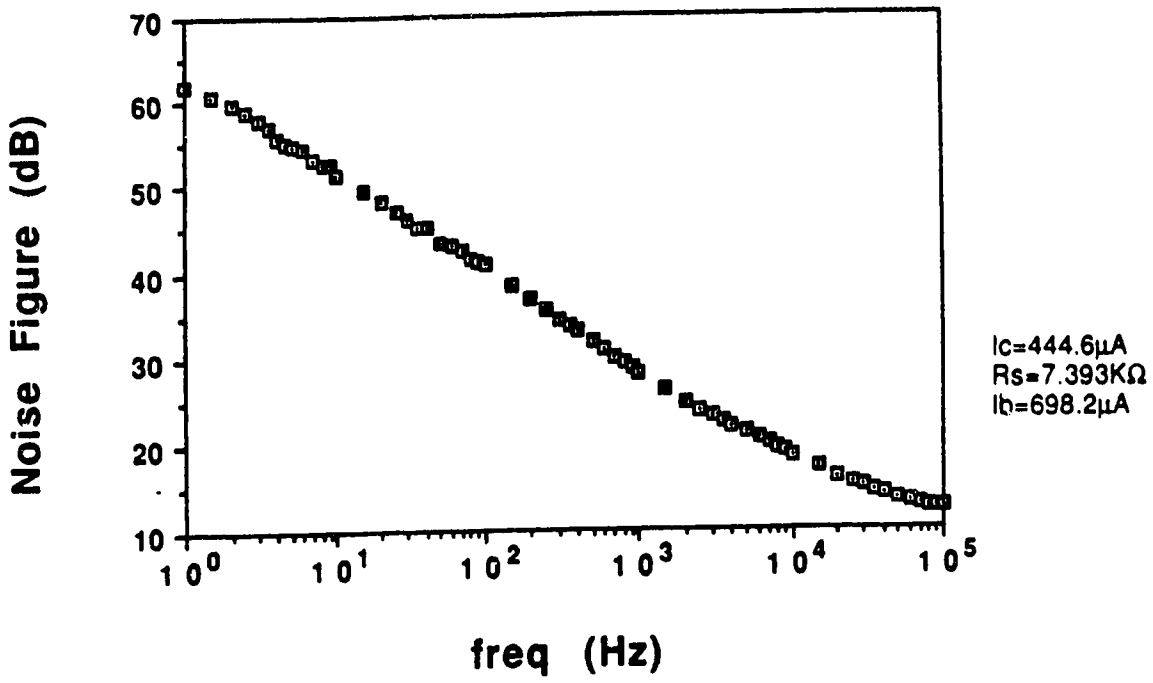


Fig.5.7 Noise figure spectrum for the case when V_S = 5.0V.

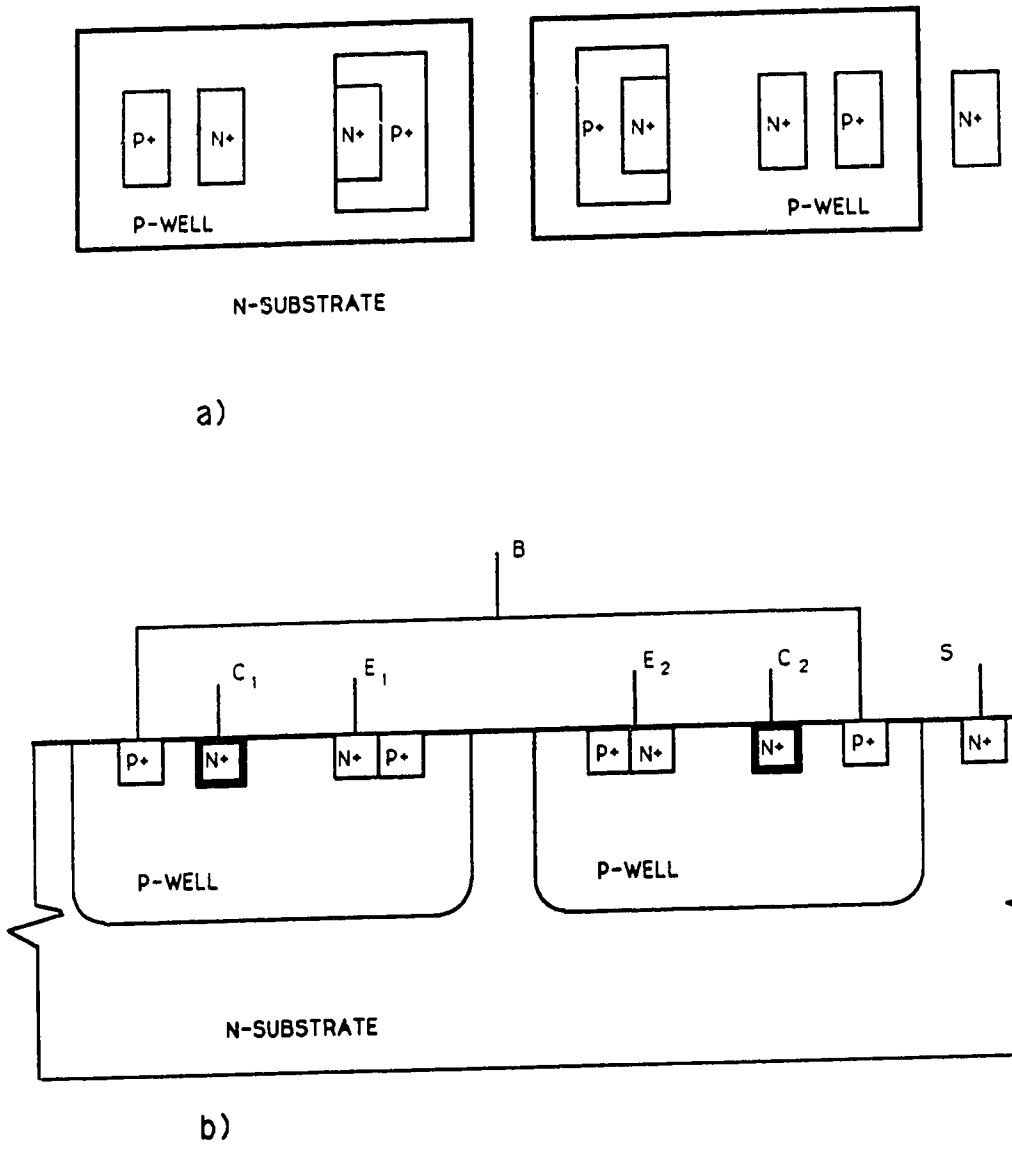


Fig.5.8 A differential pair, a) top view and b) cross section. Note: there are two base collector junctions.

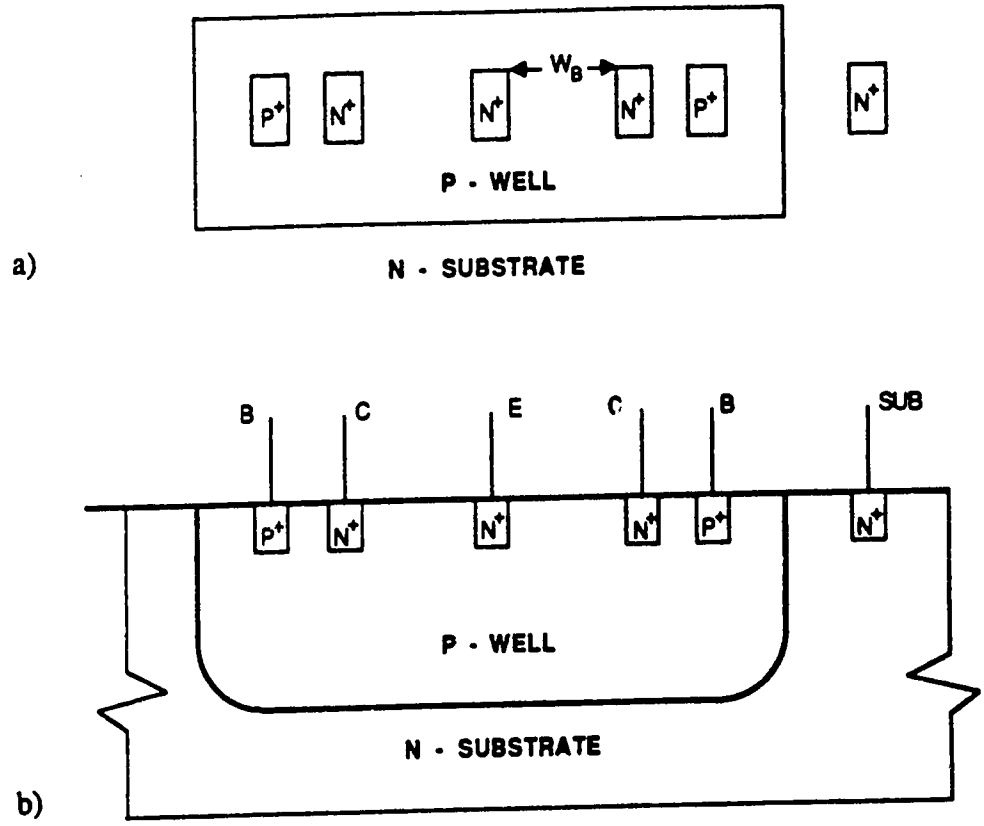


Fig.5.9 A differential LMT, a) top view and b) cross section. Note: there are two base collector junctions.

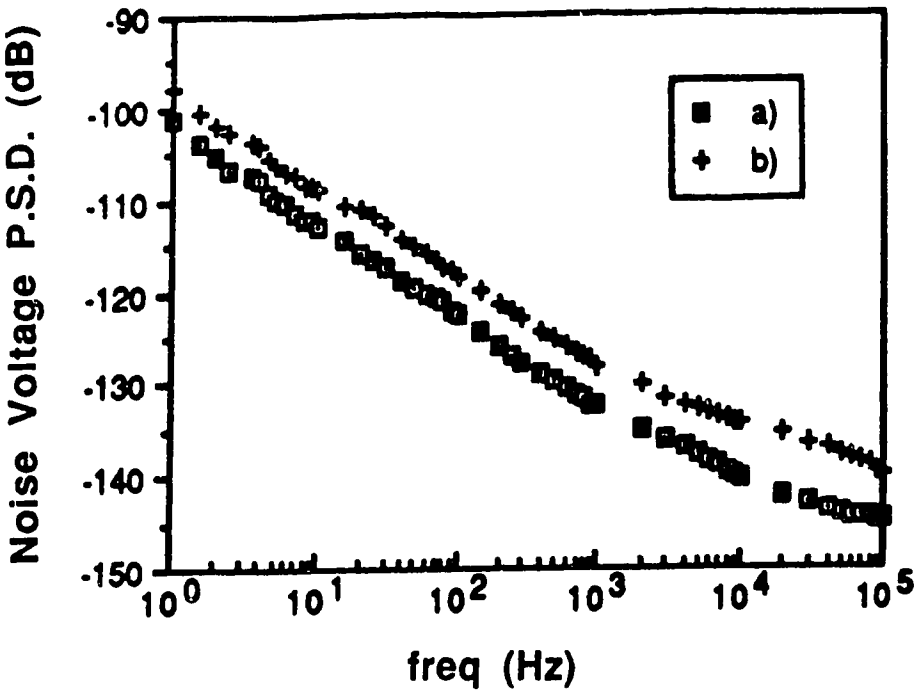


Fig.5.10 Voltage noise P.S.D. of a differential pair, a) single ended and b) differential noise.

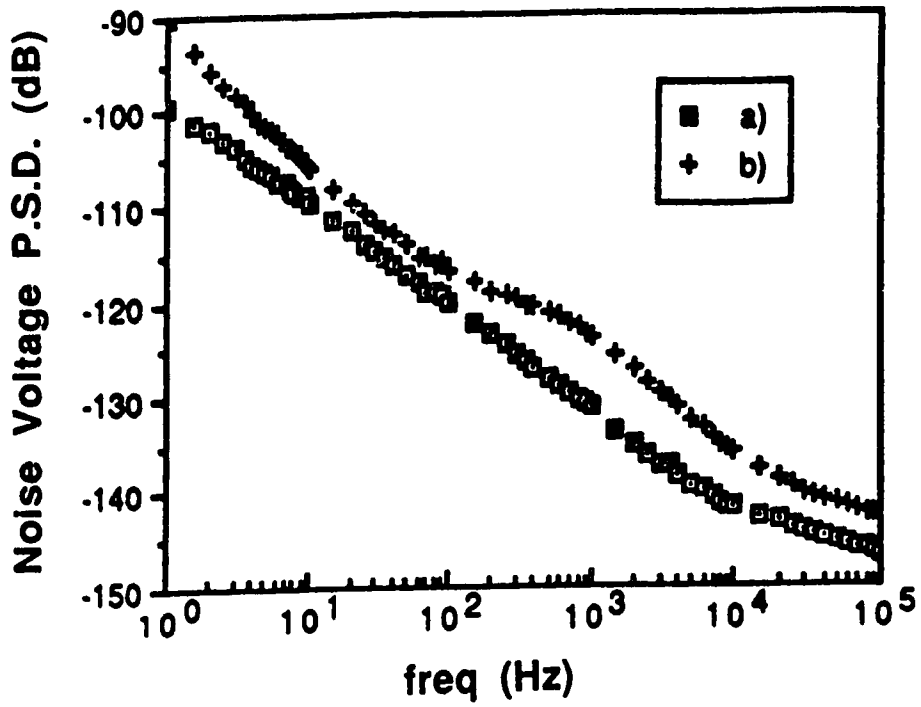
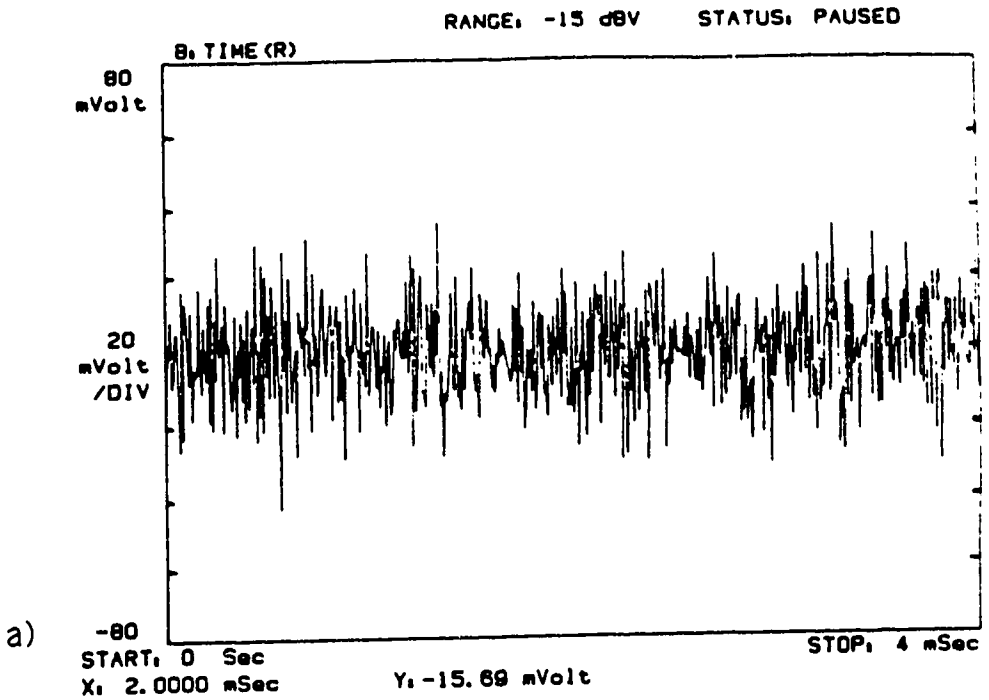
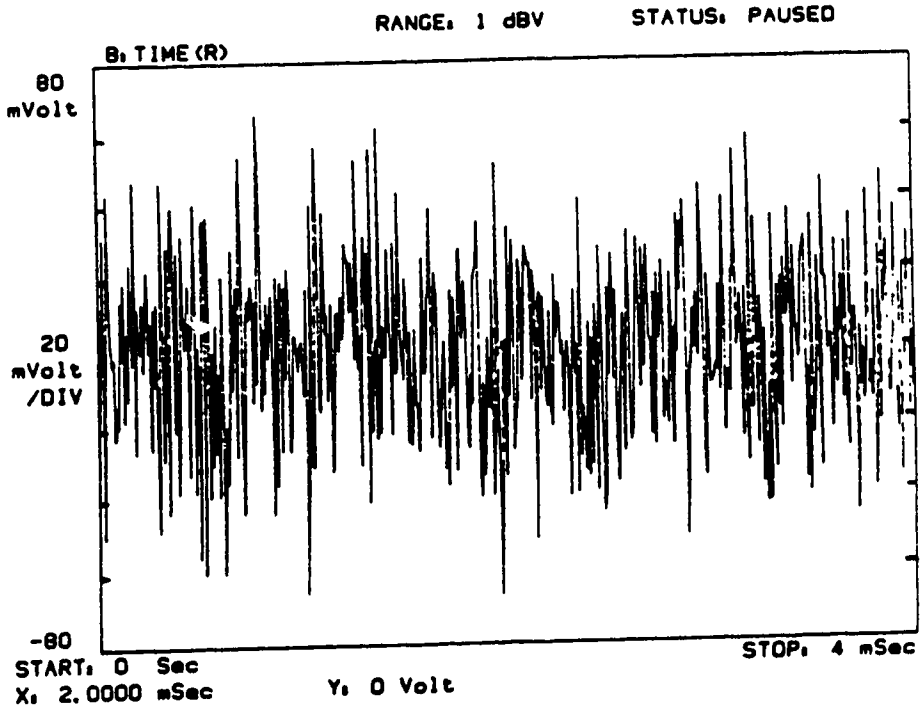


Fig.5.11 Voltage noise P.S.D. of a differential LMT, a) single ended and b) differential noise.

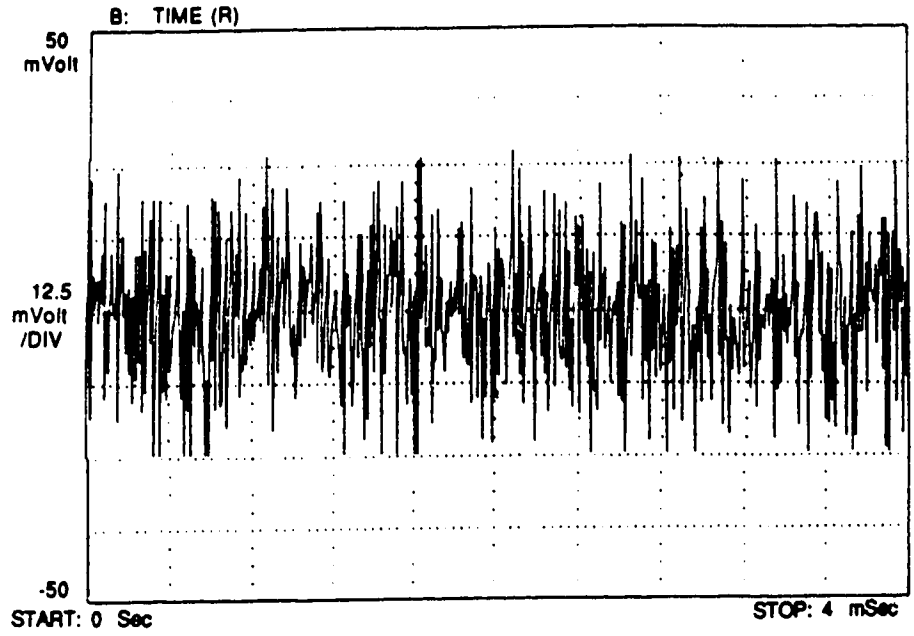


a)

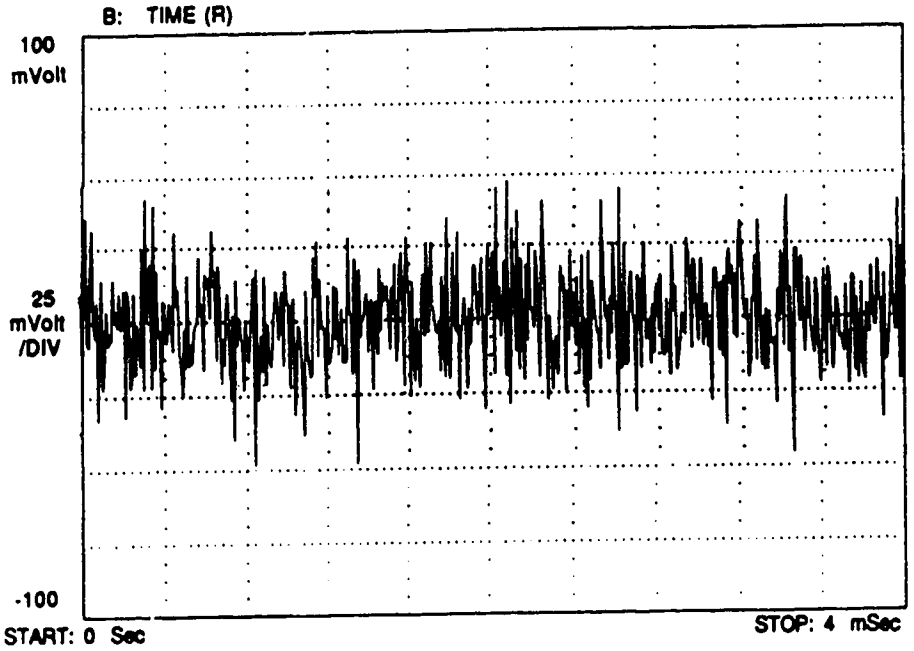


b)

Fig.5.12 Time averaging voltage noise of a differential pair, a) single ended and b) differential noise.



a)



b)

Fig.5.13 Time averaging voltage noise of a differential LMT, a) single ended and b) differential noise.

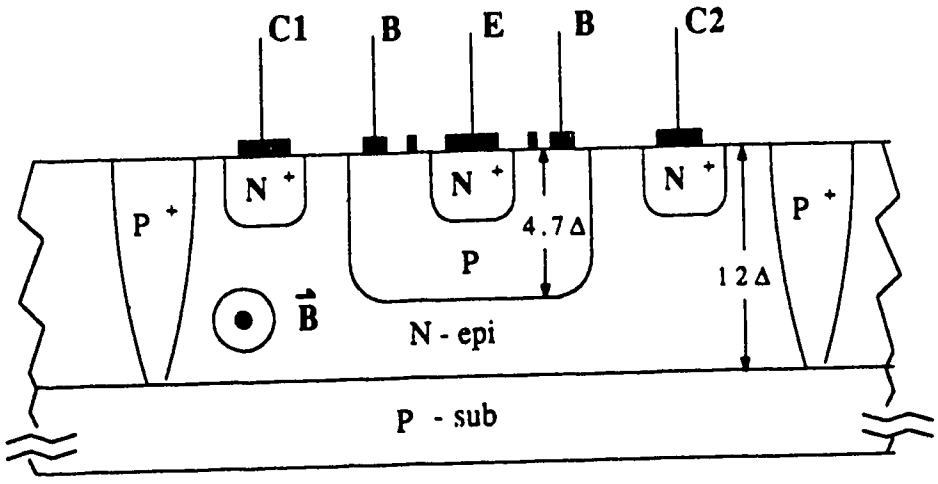


Fig.5.14 Cross section of a differential VMT, [43]. Note: there is only one base collector junction.

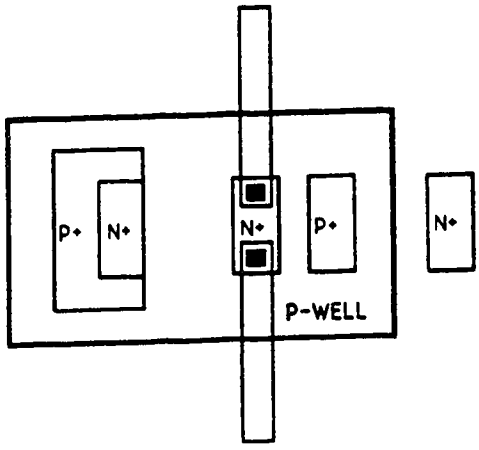


Fig.5.15 Top view of a split collector contact LMT. Note: there is only one base collector junction.

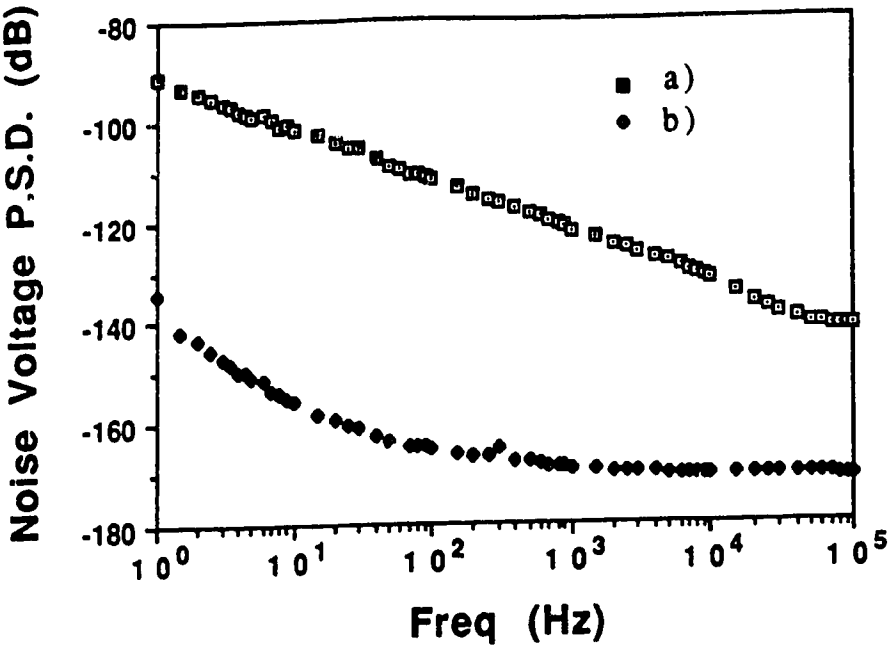


Fig.5.16 P.S.D. voltage noise of a split collector contact LMT, a) single ended noise and b) differential noise.

6. LMT IN BIPOLAR TECHNOLOGY

6.1 INTRODUCTION

Up to now, VMTs have been usually fabricated in bipolar technology and LMTs in CMOS technology. In this chapter, we present results related to a pnp MT designed as a lateral MT and fabricated in bipolar technology. The main focus of our investigation is on the role of the n^+-buried layer in the LMT. We will look at the influence of the n^+-buried layer on the electrical and magnetic characteristics of the device.

6.2 DEVICE STRUCTURE AND PRINCIPLE OF OPERATION

The pnp MT designed as a LMT is shown in Fig.6.1. As can be seen, the structure of the device is similar to the suppressed sidewall injection magnetotransistor fabricated in CMOS technology [5,20]. We have chosen that type of structure because of its high sensitivity. The difference, though, is that the structure in Fig.6.1 is fabricated in bipolar technology, and we deal here with a pnp LMT. The n-epi layer serves as the base region, and the p-diffusion (which normally serves as the base region of a standard vertical npn transistor) is used to make the emitter (E), and the collectors (C1 and C2). An n^+-diffusion is used to make the base contacts (B1), and the n^+-stripes (B2). The role of the n^+-stripes is to suppress the lateral injection from the emitter into the base in the region that is in the vicinity of the chip surface. In effect, the presence of n^+-stripes shapes the flow of injected carriers from the emitter, and therefore enhances the device sensitivity [5,20]. The emitter area is 25 x 30 μm^2, and the distance between the emitter edges and each collector is 28 μm (on the mask).

The device operation is as follows. In forward active regime, the holes are injected from the emitter into the base, and then split into two lateral components collected by C1 and C2 , and one vertical component collected by the substrate. In the absence of a magnetic field, the collector currents I_{C1O} and I_{C2O} are equal because of the structure's symmetry. When a magnetic field is applied parallel to the chip surface (in -x direction), an imbalance arises in the collector currents due to the action of the Lorentz force on the holes [5,20]. Therefore, I_{C2} increases and I_{C1} decreases. The net effect of the Lorentz force on the vertical component is zero and hence has no influence on the device sensitivity.

As already mentioned, we paid special attention to the n^+-buried layer. To investigate the role of the n^+-buried layer, we have designed another LMT, Fig.6.2, with identical dimensions but without the n^+-buried layer. To simplify the description of the electrical and magnetic results, let us denote the LMT which has the n^+-buried layer as device A and the LMT which does not have the n^+-buried layer as device B.

6.3 ELECTRICAL CHARACTERISTICS

The effect of the n^+-buried layer on the collector current can be seen from Fig.6.3. At the same biasing condition, the collector current of device A is higher than that of device B. The explanation for this phenomenon is well known. The addition of the n^+-buried layer reduces the base resistance and suppresses the collection of holes at the junction between the epitaxial layer and the substrate, i.e. reducing the substrate current (Fig.6.4). Also we note that there is an inflection point on the I_C versus I_B of device B. This inflection point occurs at I_B = 3.0 mA. The explanation for this is that when I_B < 3.0 mA, the domination of the VMT action inhibits the minority carriers to flow laterally towards the collectors. It is

only when $I_B > 3.0$ mA that the lateral flow is established. There is no inflection point on the curve of device A because the n^+-buried layer reduces the influence of the VMT action. From Fig.6.3, we can also estimate the d.c. gain of the devices. The gain of device A is much higher than the gain of device B. However, both gains are less than 1. Again, this is because the majority of the injected electrons either go to the substrate or recombine in the base region. Only a small fraction of the total injected carriers from the emitter are collected by the collectors.

Next, we investigate I_C as a function of V_S. For device A, beyond 0.5V, V_S has no influence on the collector current (Fig.6.5) and no influence on the substrate current (Fig.6.6). The reason for this is that the added donors in the n^+-buried layer inhibit the extension of the space charge region between the n-epi layer and the p-substrate. On the other hand, V_S affects the collector current and the substrate current of device B greatly. In this case, increasing V_S increases the n-epi/p-substrate depletion region. Hence, it decreases the collector current while increases the substrate current.

6.4 MAGNETIC RESULTS OF A PNP LMT FABRICATED IN BIPOLAR TECHNOLOGY

The structure of these pnp LMTs is similar to that of the SSIMT fabricated in CMOS technology [5,20]; therefore, we would expect to obtain the same type of results except that the magnitude of the sensitivity would be lower, e.g. $\mu_p < \mu_n$.

From the experimental results obtained in the previous section, we know that the presence of the n^+-buried layer reduces the effect of the VMT action; since we know from the results obtained in Chapter 3 that V_S plays an important role in the device's sensitivity, we expect that V_S will have no effect on the S_r of device A but will influence the S_r of device B.

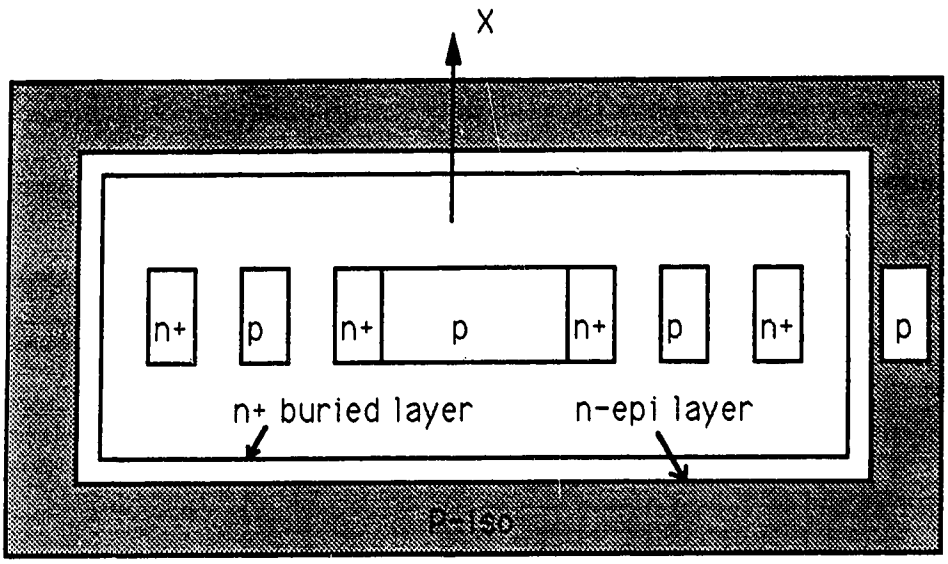
Fig.6.7 shows the response of ΔI_C to a magnetic field applied in the x direction. The biasing conditions are $V_C = V_S = 5.0V$ and $I_B = -4$ mA. As can be seen, even though both devices show a linear relationship between ΔI_C and B, the response of device B is much higher than that of device A. The presence of the n^+-buried layer is responsible for the low ΔI_C of device A. The linear relationship between ΔI_C and B obtained here is in agreement with the results obtained in [5,20] and confirms once again that the carrier deflection mechanism is responsible for the magnetic transduction.

The role of the n^+-buried layer on the sensitivity of a LMT can be studied more effectively if V_S is varied. By doing so we can obtain the relationship between the potential applied on the substrate and the shaping of the flow of carriers in the neutral base region, and consequently the device sensitivity. Fig.6.8 illustrates the relative sensitivity as a function of V_S for both devices. The biasing conditions are: $V_C = -5V$ and $I_B = -4mA$. The relative sensitivity is unchanged as V_S varies from 0V to -5V for device A. This means that with the n^+-buried layer there is negligible change of the depletion region on the side of the n^+-buried layer; thus W_{eff}, and consequently S_r, are unchanged. On the contrary, the sensitivity of device B increases as V_S goes from 0V to -5V. Like the original structure in CMOS technology [20], the space charge region of the junction between the substrate and the base region increases as the magnitude of V_S increases. This leads to the increment of the sensitivity.

We also studied the effect of I_B on the sensitivity of the pnp LMT fabricated in bipolar technology. The sensitivity as a function of I_B is presented in Fig.6.9. The results obtained for device B are similar to the results obtained for the npn SSIMT fabricated in CMOS technology. The sensitivity increases as I_B goes from -0.5 mA to -3.5 mA, then drops off as $I_B > -3.5$ mA. The increment in the sensitivity as I_B goes from -0.5 mA to -3.5 mA is because in the beginning the lateral electric field

is weak, and so W_{eff} is actually large. As I_B approaches -3.5 mA, the lateral field is stronger, and the flow of the holes is more confined. This leads to a reduction in W_{eff} and an increment in S_r. For $I_B > -3.5$ mA, W_{eff} increases, and S_r decreases. It is also interesting to note that because this is a pnp LMT, its sensitivity is less than the sensitivity of the npn SSIMT fabricated in CMOS technology [5,20]. For device A, S_r is insensitive to the change in I_B. The explanation for this can be seen from Fig.6.6, which shows that I_C is insensitive to the change in I_B.

In conclusion, even though the presence of the n^+-buried layer improves the current gain and the frequency response of the LMT, it makes the S_r of the LMT insensitive to the change of V_S and I_B, and contributes to the low values of S_r.



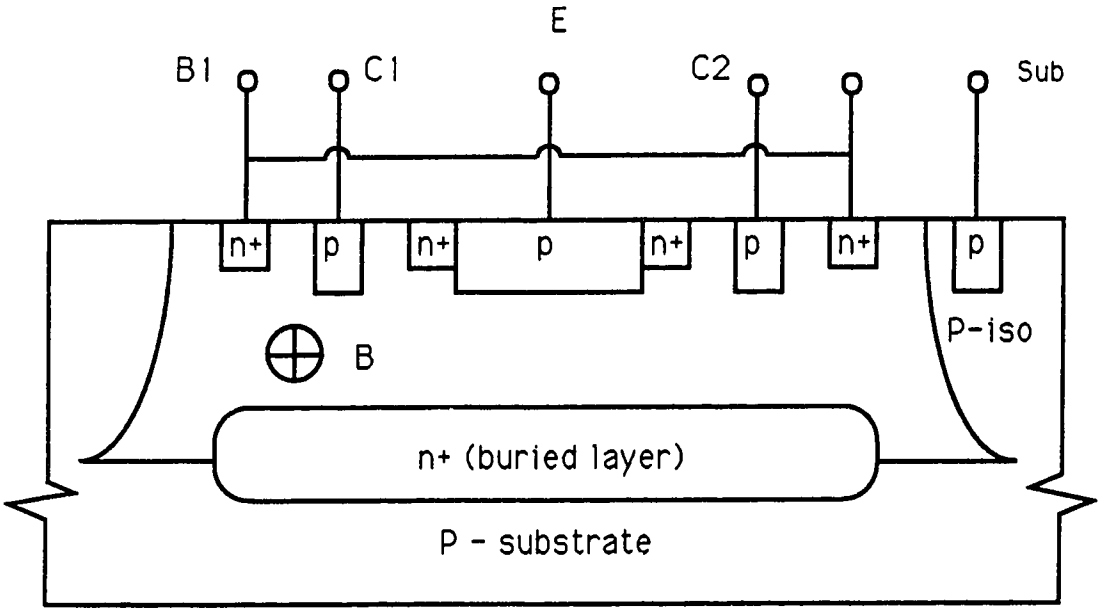
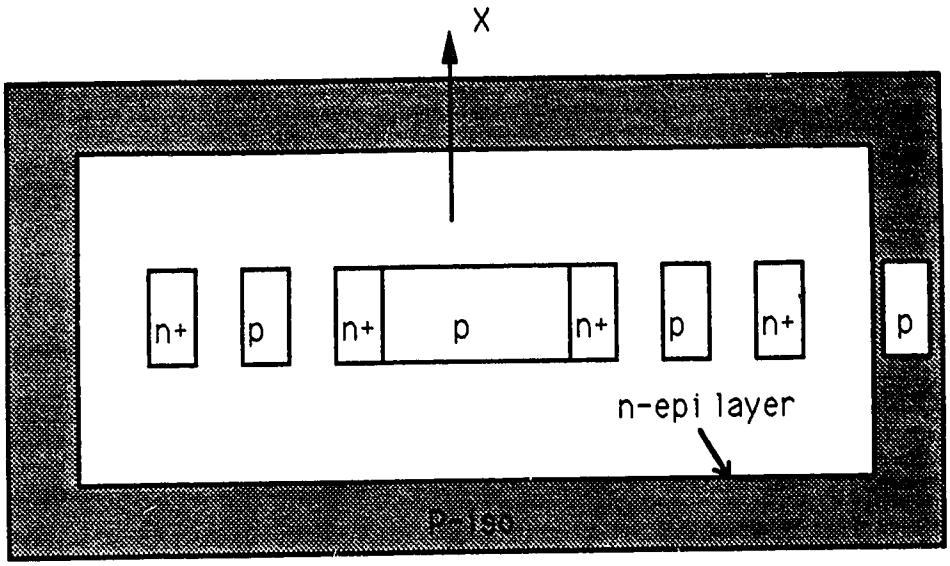


Fig.6.1 **Lateral pnp magnetotransistor with n⁺-buried layer. E - emitter, B_1 - base, and C_1 & C_2 - collectors.**



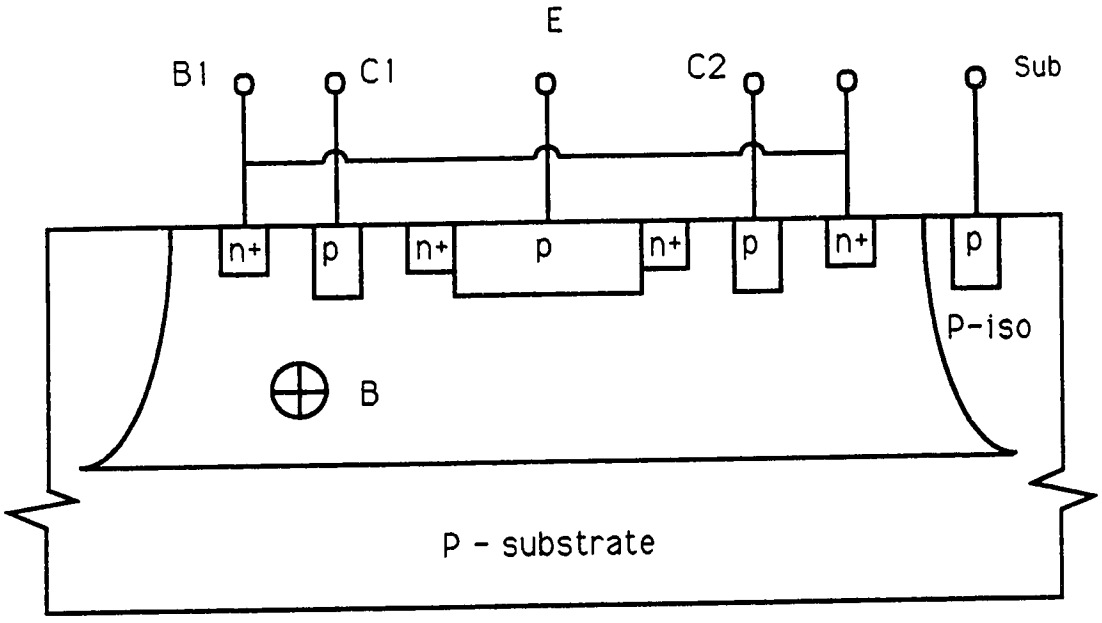


Fig.6.2 Lateral pnp magnetotransistor without n^+-buried layer. E - emitter, B_1 - base, and C_1 & C_2 - collectors.

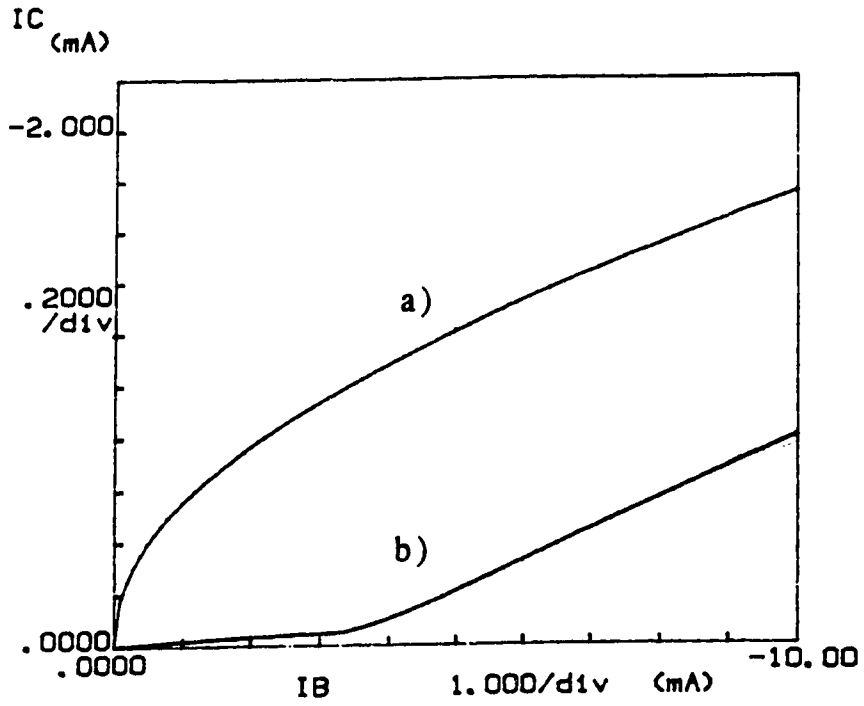


Fig.6.3 Comparison of $I_C(I_B)$ between a) device with n^+-buried layer, and b) device without n^+-buried layer. $V_C = V_S = -5$ V.

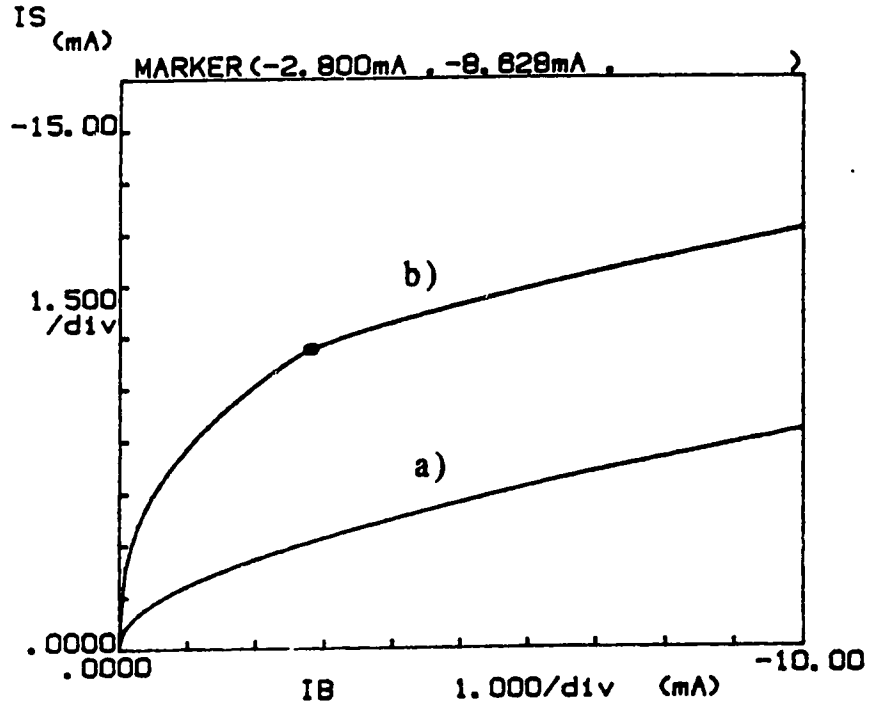


Fig.6.4 Comparison of $I_S(I_B)$ between a) device with n^+-buried layer, and b) device without n^+-buried layer. $V_C = V_S = -5$ V.

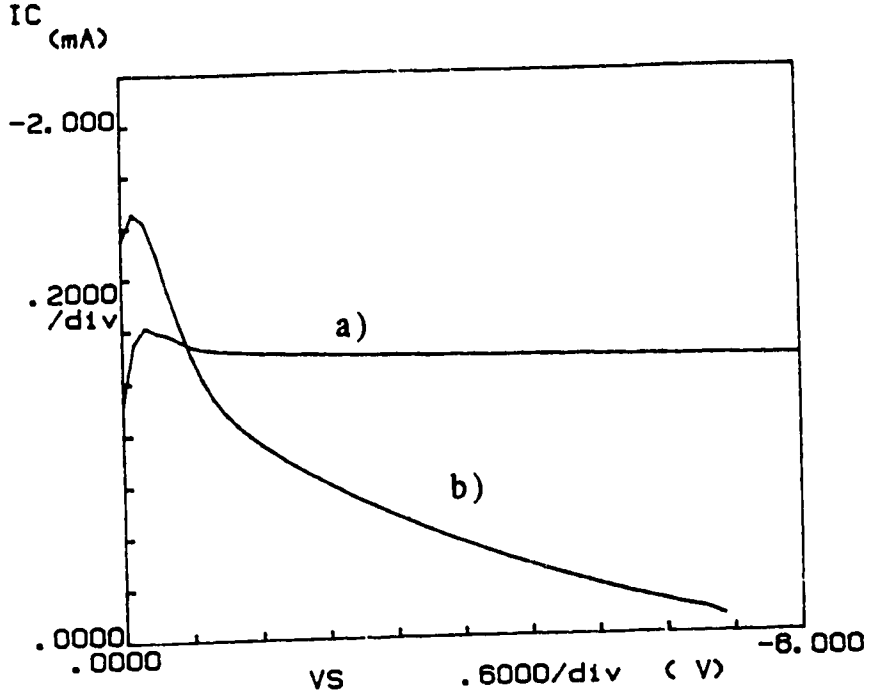


Fig.6.5 Comparison of $I_C(V_S)$ between a) device with n^+-buried layer, and b) device without n^+-buried layer. V_C = -5 V, and I_B = -4mA.

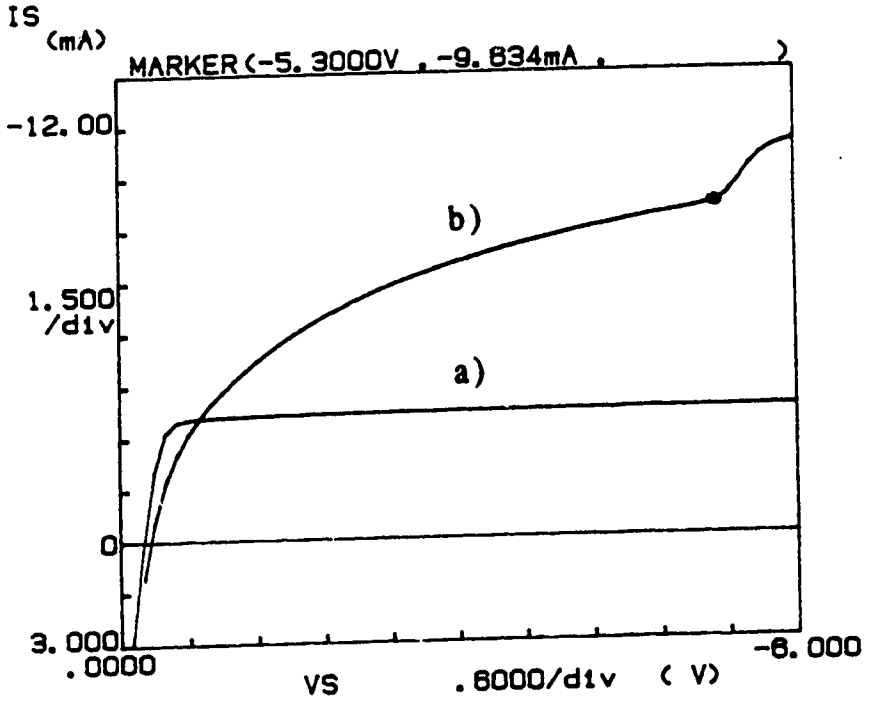


Fig.6.6 Comparison of $I_S(V_S)$ between a) device with n^+-buried layer, and b) device without n^+-buried layer. V_C = -5 V, and I_B = -4mA.

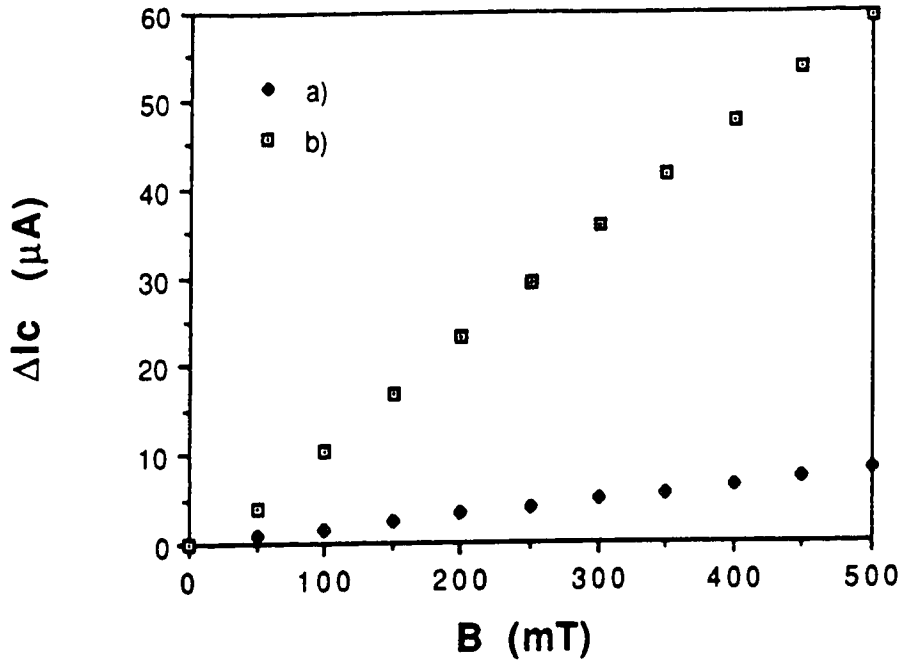


Fig.6.7 Comparison of $\Delta I_C(B)$ between a) device with n^+-buried layer, and b) device without n^+-buried layer. $V_C = V_S = -5$ V, and $I_B = -4$mA.

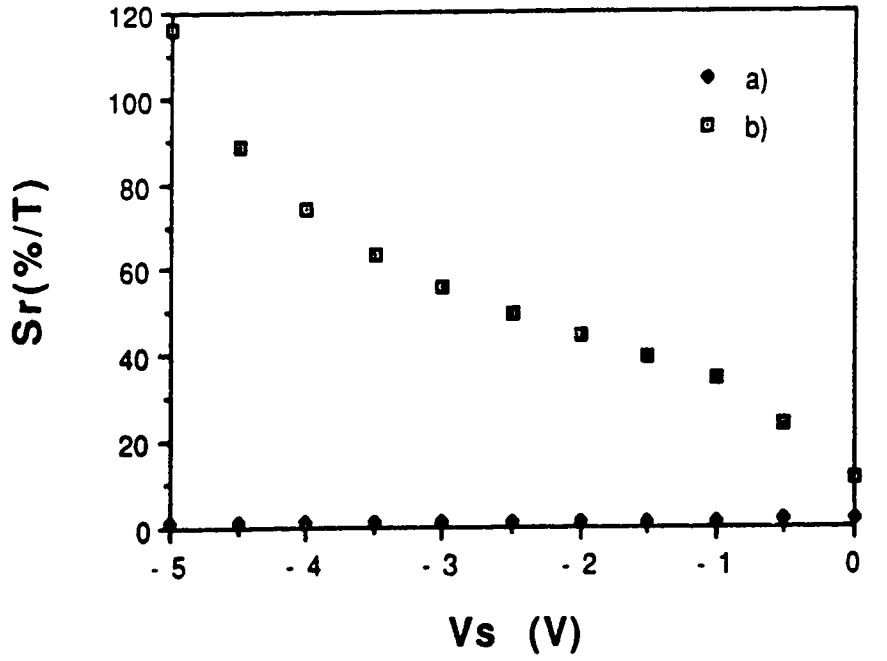


Fig.6.8 Comparison of S_r (V_S) between a) device with n^+-buried layer, and b) device without n^+-buried layer. $V_C = -5$ V, and $I_B = -4$mA.

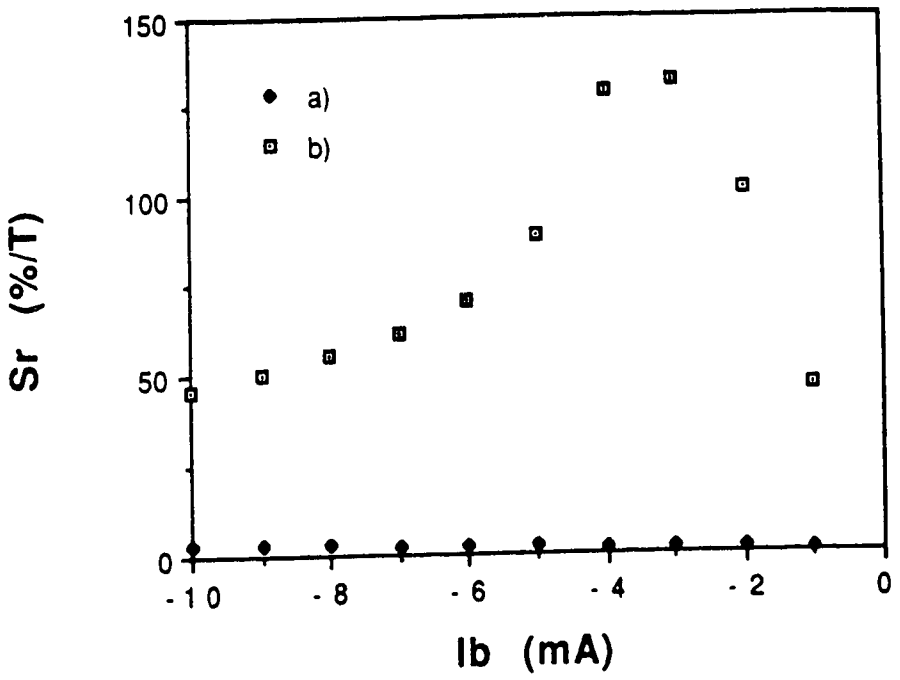


Fig.6.9 Comparison of $S_r(I_B)$ between a) device with n^+-buried layer, and b) device without n^+-buried layer. $V_C = V_S = -5$ V.

7. CONCLUSION

The aim of this work was to investigate different LMT structures, particularly the LMT that can detect a magnetic field applied either parallel or perpendicular to the chip surface. We wanted to find out sufficient information regarding to device's performance to build a multidimensional magnetic transducer. Many tests were performed on the LMT which was fabricated in a standard 5μm CMOS technology. The results are briefly summarized below.

When the device is operated in single ended mode, it is the simplest LMT that can detect 2 components of vector B. Because of the long base width to maximize the relative sensitivity, its gain is less than 1 and its ideality factor "m" deviates from the conventional values of 1 and 2. With respect to the magnetic response, we conclude that the dominant gavalnomagnetic effect is carrier deflection of minority carriers in the base. Depending on the biasing condition, the relative sensitivity varies. Generally when I_B increases, S_r decreases. S_r also increases with increasing V_S. The role of the p^+ stripe even when disconnected, is to suppress local injection from the vertical edges of the emitter where the p^+ stripes are adjoined. In other words, it shapes the flow of the electrons.

The frequency response of the device is moderate when compared to that of a conventional bipolar transistor. The cut-off frequency is around 100 kHz.

The influence of surface effects on sensitivity was studied by the means of gate potential. When the gate was biased negatively, S_r improved by 10%. When the gate was biased positively, S_r decreased drastically because a n-channel is formed between the emitter and the collector (the bipolar transistor action is violated).

In addition, special attention was paid to the noise of a LMT sensitive to B parallel or perpendicular to the chip surface. The 1/f noise region at different biasing condition extends to 50 kHz. This is unfavorable for low frequency

application, because the noise level is high and fluctuates with Δf. We also found that the collector current noise varied linearly with $\log I_C$. Very interesting results were obtained for the S/N ratio. Even though the S_r of the device when V_S was connected to 5.0V was an order of magnitude higher than the S_r of the device when V_S was disconnected, the S/N ratios for both cases were in the same order of magnitude. Subsequently, the minimum field detection for both cases was of the same order of magnitude. When parallel B is applied, the B_{min} is in the range of 1 μT; when perpendicular B is applied, the B_{min} is in the range of 10 μT. Further, both frequency and time average correlation coefficients of the differential pair and the differential LMT are found to be 0, which suggests that the voltage noise of the 2 collectors is not correlated. It was also found that the differential noise was higher than the noise in the single collector LMT.

A new pnp LMT has been designed and manufactured in bipolar technology. The results show that the n^+-buried layers plays a crucial role in the design of this type of structure. In term of relative sensitivity, the device without the n^+-buried layer has one order of magnitude higher than the device with n^+-buried layer. A sensitivity of 135 %/T is measured- the highest ever reported for a pnp MT.

The work presented here has generated new questions, and to find the answers a further investigation is needed. In terms of the magnetic sensitivity, certainly we would like to improve S_{rz} so that it is at least in the same order of magnitude as S_{rx}. This could be the toughest challenge because V_S does not influence S_{rz} to the same degree that it does on S_{rx}. Second, now that we have good results in sensing magnetic field in two different directions, we believe that 2-D and 3-D devices based on LMTs are realizable. Further investigation of these devices will require much work because their operation will be more complicated.

In terms of noise, further work in needed in finding the location of the 1/f noise sources in a simple LMT. The questions that need to be answered are 1) which p-

n junction is the most dominant noise source, and 2) will the noise decrease when the gate is used? The second question is raised because if the 1/f noise is dominated by the surface noise, then perhaps with the negative voltage applied to the gate we can push action (i.e. trapping and detrapping at G/R centers) away from the surface.

The past ten years have been a time of remarkable growth in the area of magnetotransistors. Principles of operation of various structures have been studied. Sensitivity, noise, offset, linearity, etc. have been evaluated. With all of this knowledge, and with the information which will be obtained within the next couple of years, the MT will reach maturity and will be incorporated in an integrated transducers for different applications.

8. REFERENCES

[1] H.P. Baltes and R.S. Popovic, "Integrated Semiconductor Magnetic Field Sensors," Proc. IEEE, vol. 74, pp. 1107-1132, 1986.

[2] S. Kordic, "Integrated Circuit Magnetic Field Sensor," Sensors and Actuators, vol. 10, pp.347-378, 1986.

[3] Lj. Ristic, M. Doan, and M. Paranjape, "3-D Magnetic Field Sensor as a Lateral Magnetotransistor in CMOS Technology," Sensors and Actuators, in print.

[4] S. Kordic and P. J. A. Munter, "Three-Dimensional Magnetic Field Sensors", IEEE Electron Dev., vol.35, pp.771-779, 1988.

[5] Lj. Ristic, T. Smy and H.P. Baltes, "A Lateral Magnetotransistor Structure with a Linear Response to the Magnetic Field", IEEE Trans. Electron Devices, vol. ED-36, p. 1076-1086, 1989.

[6] L. Halbo and J. Haraldsen, "The Magnetic Field Sensitive Transistor: A New Sensor for Crankshaft Angle Position," Trans. ASE, vol. 89, p. 701, 1981.

[7] K. Maenaka, H. Okada, and T. Nakamura, "Universal Magneto-Operational Amplifier (MOP)," Transducer 89',

[8] Lj. Ristic, T. Q. Truong, M. T. Doan, D. Mladenovic,H. P. Baltes, " Influence of Surface Effects on the Sensitivity of Magnetic Field Sensors," Canadian Journal of Physics, vol. 67, p. 207,1989.

[9] C. B. Brown, "High Frequency Operation of Transistors," Electronics, vol 23, pp. 81-83, 1950.

[10] P. C. Trivedi, and G. P. Srivastava, "Transistors in Magnetic Field," Electronic & Radio Engineer, pp. 368-371, 1959.

[11] E. C. Hudson Jr., "Semiconductive Magnetic Transducer," U. S. Patent 3 389 230, 1968.

[12] J. B. Flynn, "Silicon Depletion Layer Magnetometer," J. Appl. Phys., vol. 41, pp. 2750-2751, 1970.

[13] L. W. Davies and M. S. Wells, "Magneto Transistor Incorporated in an Integrated circuit," in Proc. IREE, Australia, pp. 235, June 1971.

[14] V. Zieren and B. P. M. Duyndam, "Magnetic-Field-Sensitive Multicollector N-P-N Transistors," IEEE Trans. Electron Devices, vol. ED-29, pp. 83-90, 1982.

[15] K. Maenaka, T. Ohsakama, M. Ishida, and T. Nakamura, "Characteristics of the Vertical Magnetic Field Sensitive Transistor (VMT)," Proc. 6th Sensor Symp., pp. 47, 1986.

[16] A. W. Vinal and N. A. Masnari, "Response to "Comment on 'Magnetic transistor behavior explained by modulation of emitter injection, not carrier deflection'," IEEE Electron Device Lett., vol. EDL-3, pp. 396-397, 1982.

[17] A. W. Vinal and N. A. Masnari, "Operating Principles of Bipolar Transistor Magnetic Sensors," IEEE Trans. Electron Devices, vol. ED-31, pp. 1486-1494, 1984.

[18] R.S. Popovic and R. Widmer, "Sensitivity and noise of a lateral magnetotransistor in CMOS technology", IEDM 1984, Tech. Dig., IEEE, pp. 568-571, 1984.

[19] R. S. Popovic and R. Widmer, "Magneto-Transistor in CMOS Technology," IEEE Trans. Electron Devices, vol. ED-33, pp. 1334-1340, 1986.

[20] Lj. Ristic, T. Smy, H.P. Baltes and I. Filanovsky, "Suppressed Sidewall Injection Magnetotransistor with Focused Emitter Injection and Double Carrier Deflection", IEEE Elec. Dev. Lett., vol. EDL-8, pp. 395, 1987.

[21] S. M. Sze, Physics of Semiconductor Devices, 2nd ed. New York, NY: Wiley, 1981.

[22] R. S. Popovic, and H.P. Baltes, "An Investigation of the Sensitivity of Lateral Transistors", IEEE Electron Dev. Lett, vol. EDL-4, pp. 51-53, 1983.

[23] D.R. Briglio, Characterisation of CMOS Magnetic Field Sensors, M.Sc.Thesis, University of Alberta, Canada, 1988.

[24] R. S. Muller, and T. I. Kamins, Device Electronics for Integrated Circuits, 2nd Ed. New York, NY: Wiley, 1986.

[25] A. S. Grove, Physics and Technology of Semiconductor Devices, New York: Wiley & Sons, 1967.

[26] E. A. Vittoz, "MOS Transistors Operated in the Lateral Bipolar Mode and Their Application in CMOS Technology, " IEEE Jour. Sol.-St. Circuits, vol. SC-18, pp. 273-279, 1983.

[27] B. L. Hart and R. W. J. Barker, "First Order Theory of MOSFET Hybrid-mode Operation," Int. J. Electron., vol. 38, no. 5, pp. 625-630, 1975.

[28] A. Van der Ziel, Noise in Solid State Devices and Circuits, New York: Wiley & Sons, 1986.

[29] J. L. Plumb, and E. R. Chenette, "Flicker Noise in Transistors," IEEE Trans. Electron Devices, vol. 10, pp. 304-308, 1963.

[30] M. Conti, "Surface and Bulk Effects in Low Frequency Noise in NPN Planar Transistors," Solid State Electron., vol. 13 , pp. 1461-1469, 1970.

[31] Y. Netzer, "The design of Low Noise Amplifiers," Proc. IEEE, vol. 69, 1981.

[32] G. Blasquez and D. Sauvage, "Flicker Noise Due to Minority Carrier Trapping in the Bulk of Bipolar Transistors," in Noise in Physical Systems and 1/f Noise, D. Amico and Mazzetti, Eds. Amsterdam: Elsevier, 1985.

[33] A. Van der Ziel, Xiaonan Zhang, and A. H. Pawlikiewicz, "Location of 1/f Noise Sources in BJT's and HBJT's - I. Theory," IEEE Trans. Electron Devices, vol. 33, pp. 1371-1376, 1986.

[34] A. H. Pawlikiewicz, and A. Van der Ziel, "Location of 1/f Noise Sources in BJT's and HBJT's - II. Experiment," IEEE Trans. Electron Devices, vol. 34, pp. 2009-2012, 1987.

[35] A. L. McWhorter, Semiconductor Surface Physics, R. H. Kingston, Philadelphia: University of Pennsylvania Press, pp207-228.

[36] F. N. Hooge, T. G. M. Kleinpenning, and L. K. J. Vandamme, "Experimental Studies on 1/f Noise," Rep. Prog. Phys., vol. 44, pp. 479-532, 1981.

[37] T. G. M. Kleinpenning, "1/f Noise in the Micro Hertz Range," in Noise in Physical Systems and 1/f Noise, D. Amico and Mazzetti, Eds. Amsterdam: Elsevier, 1985.

[38] E. Oran Brigham, The FFT and its Applications, Prentice Hall, Englewood, New Jersey, 1988.

[39] P. R. Gray, and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 2nd Ed., New York, NY: Wiley, 1984.

[40] R. T. Unwin, and K. F. Knott, "Comparison of Methods used for Determining Base Spreading Resistance," IEE Proc. vol. 127, Pt. - I, No. 2, pp. 53-61, 1980.

[41] M. E. Gruchalla, "Measurement Wide Band White Noise Using a Standard Oscilloscope," EDN, pp. 157-160, June 5, 1980.

[42] A. Nathan, H. P. Baltes, D. Briglio, and M. T. Doan,. " Noise Correlation of Lateral Magnetotransistors," IEEE Trans. Electron Devices, vol. 36, pp. 1073-1075,1989.

[43] X. N. Zhang, A. Van Der Ziel, and H. Morkoc, "Location of 1/f Noise Sources in Bipolar Transistors," in Noise in Physical Systems and 1/f Noise, D. Amico and Mazzetti, Eds. Amsterdam: Elsevier, 1985.

[44] X. C. Zhu and A. Van der Ziel, "The Hooge parameters of n^+-p-n and p^+-n-p Silicon Bipolar Transistors", IEEE Trans. Electron Dev., vol. ED-32, p. 658, 1985.