# Nonlinear Magnetic Equivalent Circuit-Based Real-Time Sen Transformer Electromagnetic Transient Model on FPGA for HIL Emulation

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Abstract—Strategic power-flow control using a Sen transformer (ST) can be a robust and cost-effective solution to relieve grid congestion due to increased installation of renewables. The ST consists of a multiwinding transformer and tap changer that can regulate the power flow through a transmission line by injecting a series-connected controllable voltage. This paper develops a realtime high-fidelity magnetic equivalent circuit-based electromagnetic transient model for the ST on the field-programmable gate array (FPGA) for hardware-in-the-loop applications. This geometry-based model was developed to depict the major flux paths in the transformer core, and complex nonlinear phenomena, such as saturation, hysteresis, and eddy currents. The entire real-time ST model and other power system components are emulated by hardware description language, employing the 32-b floating point precision on the FPGA chip. A fully paralleled and pipelined hardware architecture is developed to achieve accurate real-time emulation as well as the lowest latency and smallest hardware resource consumption. The real-time results are validated against 3-D finite-element simulation using JMAG software.

*Index Terms*—Electromagnetic transient (EMT) analysis, field-programmable gate arrays (FPGAs), finite-element methods, hardware-in-the-loop (HIL) emulation, hysteresis, magnetic equivalent circuits, parallel algorithms, parallel processing, power-flow control, pipelining, real-time systems, Sen transformer (ST).

## I. INTRODUCTION

**G** ROWING demand by a plethora of sensitive loads, stringent reliability constraints, and heightened environmental concerns that favour greater integration of renewables, have created perfect conditions for a highly stressed and dyspeptic transmission grid [1], [2]. Congestion of lines under these conditions has become commonplace with increased probability of major outages leading to blackouts. While long-term transmission planning and expansion still remains the prudent solution, a near term economical alternative might be the strategic placement of power-flow controllers to relieve transmission bottlenecks [3]–[6]. The unified power-flow controller

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(UPFC) [7], [8] is one such solution which consists of a series and a shunt converter that can generate a compensation voltage to insert in series with the transmission line. The compensation voltage is fully controllable both in magnitude and phase angle with respect to the line voltage, for independent regulation of the active and reactive power flowing through the line in both directions. However, high installation and operation costs have hitherto prevented the UPFC's widespread implementation. The Sen transformer (ST) proposed in [9], can address the same objectives but with a lower cost, higher reliability, and efficiency [10]; however, no ST has been commissioned yet in a power system. The ST consists of a single-core three-limb three-phase transformer and tap changers. The multi-winding transformer has three primary windings and nine secondary windings. By setting the tap changers into different combinations, the ST can inject a compensation voltage with controllable magnitude and phase angle much the same way like the UPFC, thereby providing an independent active power and reactive power-flow control. The concept of the smart power-flow controller (SPFC) was introduced in [11] which offered the ST with the option of either a low-cost electromechanical design with mechanical tap changers or a power electronics-based design using thyristor-based tap changers.

A detailed electromagnetic transient model of the ST in realtime is necessary to study its impact on the host power system. It would also allow rapid testing and prototyping of new control algorithms under hardware-in-the-loop (HIL) conditions [12]. A real-time transient ST model was developed on the CPU in [13], and an advanced tap-changing algorithm was proposed in [14]; however, this real-time ST model was developed based on a lumped electrical circuit model, which ignored the detailed transformer core geometry and flux paths in the core. Furthermore, in this model nonlinear core saturation was included using a piece-wise linear approximation, which is prone to numerical oscillations; complex behavior such as hysteresis and eddy current transients were entirely omitted. The increased computational complexity of detailed electromagnetic transient ST model makes the CPU an unlikely implementation platform for real-time HIL emulation.

This paper proposes a real-time high-fidelity nonlinear magnetic equivalent circuit (MEC)-based ST electromagnetic transient (EMT) model on the field-programmable gate array (FPGA) for HIL emulation. The MEC approach [15], [16] which is geometry-based is employed to model the multi-winding transformer consisting of magnetomotive

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Fig. 1. Schematic of the ST and its interconnection to the transmission network.

force (mmf) sources and permeance elements. The nonlinear permeance elements necessitate a time-varying transformer nodal admittance matrix which in turn require the entire power system matrix to be updated in every emulation time-step. The hysteresis and eddy current behavior are modeled based on Preisach theory [17], [18] and frequency-dependent equivalent network [19], [21], respectively. All of these details increase the computational burden of the high-fidelity electromagnetic transient model and put upward pressure on the emulation time-step. The FPGA has previously proven to be an efficacious platform for transient simulation of power systems [22]–[25] mainly due to its capability of exploiting hardware parallelism and pipelining. The real-time hardware emulation results are validated using 3-D finite-element (FE) simulation in JMAG®.

The remainder of this paper is organized as follows. Section II presents the ST operation background and nonlinear MEC-based ST model. Section III gives the implementation details of the hardware emulation. Section IV provides the case studies and real-time results to validate the emulated MEC-based ST on the FPGA. Finally, Section V presents the conclusion.

## II. GEOMETRICAL SEN TRANSFORMER (ST) EMT MODEL

## A. ST Operating Principle

The three-phase, three-limb ST circuit schematic and its interconnection to the transmission line is shown in Fig. 1. At the sending-end the three-phase transmission line supplies voltages,  $V_{ST,pa}, V_{ST,pb}$  and  $V_{ST,pc}$  to the ST primary windings, which are connected in Y and in shunt with the transmission line. The nine secondary windings:  $a_1, a_2$ , and  $a_3$  are placed in the first limb;  $b_1, b_2$ , and  $b_3$  are placed in the second limb; and  $c_1, c_2$  and  $c_3$  are placed in the third limb. The three secondary windings which are placed in different limbs are connected in series with the transmission line and inject a compensation voltage, e.g., windings  $a_1, b_1$  and  $c_1$  for the compensation voltage  $V_{ST,ca}$  in phase-a; windings  $a_2, b_2$  and  $c_2$  for the compensation voltage  $V_{ST,cb}$  in phase-b, windings  $a_3, b_3$  and  $c_3$  for the compensation voltage  $V_{ST,cc}$  in phase-c. By using the on-load tap changers, the active number of turns of the nine secondary windings can be configured so that the induced compensation voltage can be controlled both in magnitude and phase angle independently. If the 120° phase-shift compensation voltage is series connected with the transmission line, as shown in Fig. 1, the previous sending-end voltage (the ST primary side voltage),  $v_{ST,p}$ , is modified to a new effective sending-end voltage (the ST secondary side voltage),  $v_{ST,s}$ , as can be seen from the top lefthand corner of Fig. 1. The number of turns of the secondary windings can be classified into three groups:  $a_1, b_2$  and  $c_3$  ( $GP_1$ );  $b_1, c_2$ and  $a_3$  (*GP*<sub>2</sub>); and  $c_1, a_2$  and  $b_3$  (*GP*<sub>3</sub>). The windings in one group have the same tap setting, however, one group may have a different tap setting from others. The major flux paths consisting of core and leakage fluxes in the yoke and limb are also depicted in Fig. 1.

## B. Tap-Selection Algorithm

The Control Unit takes the measurements of the sending end voltage,  $V_{ST,p}$ , and the receiving end voltage,  $v_r$ , from the transmission network as well as the required power level,  $P_{ref}$  and  $Q_{ref}$  as inputs. The calculated compensation voltage magnitude  $v_{ST,c}$  and the phase angle  $\alpha$  are further forwarded to the Tap-setting Unit to generate the combinations of the tap settings for each secondary winding. Further information regarding the tap-setting algorithm and its implementation can be found in [14].

## C. High-Fidelity Nonlinear Magnetic Equivalent Circuit (MEC)-Based ST Model

The three-phase, three-limb MEC-based ST representation, is shown in Fig. 2. Each limb consist of four types of components: 1) MMF sources,  $N_{A}i_{ST,a}$ ,  $N_{B}i_{ST,b}$  and  $N_{C}i_{ST,c}$ , generated by the current flow through the primary windings in phases *a*, *b* and *c*, respectively;  $N_{a1}i_{ST,sa}$ ,  $N_{a2}i_{ST,sb}$ ,  $N_{a3}i_{ST,sc}$ ,  $N_{b1}i_{ST,sa}$ ,  $N_{b2}i_{ST,sb}$ ,  $N_{b3}i_{ST,sc}$ ,  $N_{c1}i_{ST,sa}$ ,  $N_{c2}i_{ST,sb}$  and  $N_{c3}i_{ST,sc}$  are generated by the current flow through the secondary windings in phases a, b, and c, respectively; 2) nonlinear permeances,  $P_A$ ,  $P_B$  and  $P_C$  represent nonlinear iron core permeances for ST primary windings in phases a, b and c, respectively;  $P_{a1}, P_{a2}, P_{a3}, P_{b1}, P_{b2}, P_{b3}, P_{c1}, P_{c2}$  and  $P_{c3}$ represent nonlinear iron core permeances for the ST secondary windings in phases a, b and c, respectively; 3) linear permeances,  $P_{la1}$  to  $P_{la4}$ ,  $P_{lb1}$  to  $P_{lb4}$  and  $P_{lc1}$  to  $P_{lc4}$  represent the ST leakage air permeances in phases a, b and c, respectively; 4) linear permeances  $P_{a0}$ ,  $P_{b0}$ ,  $P_{c0}$  represent ST zero-sequence permeances in phases a, b and c, respectively. In addition, there are also two nonlinear iron permeances  $P_{ab}$  and  $P_{bc}$  that represent ST yoke between phase-a and phase-b, and phase-b and phase-c, respectively.

The branch fluxes and the mmf's in the ST core can be related to each other by the following equation,

$$\boldsymbol{\phi} = \mathbf{P}(\mathbf{N}\boldsymbol{i} - \boldsymbol{\xi}') \tag{1}$$

where  $\phi$ , *i* and  $\xi'$  are  $n \times 1$  vectors of branch fluxes, winding currents, and branch mmf's, respectively. And **P** and **N** are  $n \times n$ diagonal matrices of branch permeances and number of winding turns, respectively.

According to Gauss' law for magnetism [26], the summation of fluxes entering or leaving a node in the magnetic equivalent circuit must be zero, given as,

$$\boldsymbol{C}_{nb}^{T}\boldsymbol{\phi}=\boldsymbol{0}, \qquad (2)$$

where  $C_{nb}^{T}$  is the node-branch connection matrix, its entries can be 1, -1, and 0 which stands for branch flux entering, leaving, and no connection to the node, respectively.

The branch MMF vector can be obtained by applying matrix  $C_{nb}^{T}$  to node MMF vector  $\boldsymbol{\xi}_{node}$  given as,

$$\boldsymbol{C}_{nb}\boldsymbol{\xi}_{node} = \boldsymbol{\xi}'. \tag{3}$$

By combining the above three equations the relationship between the branch fluxes and the winding currents can be established:

$$\boldsymbol{\phi} = \mathbb{P}\mathbf{P}\mathbf{N}\boldsymbol{i},\tag{4}$$

where

$$\mathbf{D} = \mathbf{I} - \mathbf{P} \mathbf{C}_{nb} (\mathbf{C}_{nb}^T \mathbf{P} \mathbf{C}_{nb})^{-1} \mathbf{C}_{nb}^T.$$
(5)

**I** is the  $n \times n$  identity matrix.

By partitioning the permeance network into two branch sets,  $\phi^M$ , for the branches with MMF sources and permeance elements, and  $\phi^P$ , for branches with only permeance elements, (4) can be rewritten as:

$$\boldsymbol{\phi}^M = \mathbb{P}^{MM} \mathbf{P}^M \mathbf{N}^M \boldsymbol{i}^M, \tag{6}$$

where  $\mathbb{P}^{MM}$  is a 12 × 12 sub-matrix of  $\mathbb{P}$ .  $\phi^M$  and  $i^M$  are 12  $\times$  1 vectors, and  $\mathbf{P}^{M}$  and  $\mathbf{N}^{M}$  are diagonal 12  $\times$  12 matrices, given as:

$$oldsymbol{\phi}^{M} = egin{bmatrix} \phi_{A}(t) \ \phi_{B}(t) \ \phi_{C}(t) \ \phi_{a1}(t) \ \phi_{b1}(t) \ \phi_{c1}(t) \ \phi_{a2}(t) \ \phi_{b2}(t) \ \phi_{c2}(t) \ \phi_{a3}(t) \ \phi_{b3}(t) \ \phi_{c3}(t) ig]^{T} \,,$$



Fig. 2. High-fidelity magnetic equivalent circuit representation for the ST iron core

$$\begin{split} \mathbf{i}^{M} &= [i_{ST,a}(t) \ i_{ST,b}(t) \ i_{ST,c}(t)) \ i_{ST,sa}(t) \ i_{ST,sa}(t) \ i_{ST,sa}(t) \ i_{ST,sa}(t) \\ &\quad i_{ST,sb}(t) \ i_{ST,sb}(t) \ i_{ST,sc}(t) \ i_{ST,sc}(t) \ i_{ST,sc}(t) \ i_{ST,sc}(t)]^{T} , \\ \mathbf{P}^{M} &= diag \left\{ P_{A}(t) \ P_{B}(t) \ P_{C}(t) \ P_{a1}(t) \ P_{b1}(t) \ P_{c1}(t) \\ &\quad P_{a2}(t) \ P_{b2}(t) \ P_{c2}(t) \ P_{a3}(t) \ P_{b3}(t) \ P_{c3}(t) \right\} , \\ \mathbf{N}^{M} &= diag \left\{ N_{A}(t) \ N_{B}(t) \ N_{C}(t) \ N_{a1}(t) \ N_{b1}(t) \ N_{c1}(t) \\ &\quad N_{a2}(t) \ N_{b2}(t) \ N_{c2}(t) \ N_{a3}(t) \ N_{b3}(t) \ N_{c3}(t) \right\} . \end{split}$$

From Faraday's law the winding terminal voltages can be written in matrix format as,

$$\boldsymbol{v}_{ST} = \mathbf{N}_Z \frac{d}{dt} \boldsymbol{\phi}^M(t), \tag{7}$$

where  $N_Z$  is a 6 × 12 winding turns matrix.  $v_{ST}$  is a 6 × 1 ST terminal voltage vector, given as:

$$\mathbf{v}_{ST} = \begin{bmatrix} v_{ST,pa}(t) \ v_{ST,pb}(t) \ v_{ST,sc}(t) \end{bmatrix}^{T}, \\ v_{ST,sa}(t) \ v_{ST,sb}(t) \ v_{ST,sc}(t) \end{bmatrix}^{T}, \\ \mathbf{N}_{Z} = \begin{bmatrix} N_{A} & 0 & 0 & N_{A} & 0 & 0 \\ 0 & N_{B} & 0 & 0 & N_{B} & 0 \\ 0 & 0 & N_{C} & 0 & 0 & N_{C} \\ \vdots & \vdots & 0 & N_{a1} & 0 & 0 \\ \vdots & \vdots & N_{b1} & 0 & 0 \\ \vdots & \vdots & N_{b1} & 0 & 0 \\ \vdots & \vdots & N_{c1} & 0 & 0 \\ \vdots & \vdots & \ddots & N_{b2} & 0 \\ \vdots & \vdots & \vdots & N_{b2} & 0 \\ \vdots & \vdots & \vdots & N_{b2} & 0 \\ \vdots & \vdots & \vdots & N_{b3} \\ 0 & 0 & 0 & 0 & 0 & N_{c3} \end{bmatrix}$$

2485

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The discrete-time difference equations of (7) can be obtained by applying Trapezoidal rule,

$$\mathbf{N}_{Z}\boldsymbol{\phi}^{M}(t) = \frac{\Delta t}{2}\boldsymbol{v}_{ST}(t) + \boldsymbol{\phi}_{hist}^{M}(t), \qquad (8)$$

where  $\Delta t$  is the simulation time-step, with  $\phi_{hist}^{M}(t)$  being the 6  $\times$  1 history vector term expressed as:

$$\boldsymbol{\phi}_{hist}^{M}(t) = \frac{\Delta t}{2} \boldsymbol{v}_{ST}(t - \Delta t) + \mathbf{N}_{Z} \boldsymbol{\phi}^{M}(t - \Delta t).$$
(9)

Substituting (6), the left hand side of (8) can be rewritten as,

$$\mathbf{N}_Z \boldsymbol{\phi}^M(t) = \mathbf{Z} \, \boldsymbol{i}^M, \tag{10}$$

where **Z** is a  $6 \times 12$  matrix given as:

$$\mathbf{Z} = \mathbf{N}_Z \mathbb{P}^{MM} \mathbf{P}^M \mathbf{N}^M.$$
(11)

Further (10) can be rewritten as:

$$\mathbf{N}_Z \boldsymbol{\phi}^M(t) = \mathbf{Z} \boldsymbol{i}^M = \mathbf{Z}' \boldsymbol{i}^{M'}, \qquad (12)$$

with  $\mathbf{Z}'$  being the 6 × 6 impedance matrix and  $\mathbf{i}^{M'}(t)$  being the 6 × 1 current vector, given as shown in the equation at the bottom of the page. By noting that the ST current vector  $\mathbf{i}_{ST}$  is expressed, shown in the equation at the bottom of the page.

Equation (8) can be further rewritten as

$$\mathbf{Z}_{ST}\boldsymbol{i}_{T}(t) = \frac{\Delta t}{2}\boldsymbol{v}_{ST}(t) + \boldsymbol{\phi}_{hist}^{M}(t), \qquad (13)$$



Fig. 3. Hysteresis major and minor loops corresponding to the reversal point stack (*RPS*) within the Preisach hysteretic unit (PHU).



Fig. 4. High fidelity MEC-based ST model interfaced with cascaded equivalent circuit.

where  $\mathbf{Z}_{ST}$  is the 6 × 6 matrix given as shown in the equation at the bottom of the page.

$$i_{ST} = [i_{ST,pa}(t) \ i_{ST,pb}(t) \ i_{ST,pc}(t) \ i_{ST,sa}(t) \ i_{ST,sb}(t) \ i_{ST,sc}(t)]^T,$$
  
and  
$$i_{ST,pa}(t) = i_{ST,a}(t) - i_{ST,sa}(t),$$
  
$$i_{ST,pb}(t) = i_{ST,b}(t) - i_{ST,sb}(t),$$
  
$$i_{ST,pc}(t) = i_{ST,c}(t) - i_{ST,sc}(t).$$

Then, the Norton equivalent formula for MEC-based ST is given,

$$\mathbf{i}_{ST}(t) = \mathbf{Y}_{ST}(t)\mathbf{v}_{ST}(t) + \mathbf{I}_{hist,ST}(t), \qquad (14)$$

where

$$\boldsymbol{I}_{hist,ST}(t) = \mathbf{Z}_{ST}^{-1} \boldsymbol{\phi}_{hist}^{M}(t), \qquad (15)$$

$$\mathbf{Y}_{ST}(t) = \frac{\Delta t}{2} \mathbf{Z}_{ST}^{-1}.$$
 (16)

The time-varying matrix  $\mathbf{Y}_{ST}(t)$ , due to the nonlinear permeance matrices  $\mathbb{P}^{MM}$  and  $\mathbf{P}^{M}$  in (11), causes the overall power system admittance matrix  $\mathbf{Y}$  to be time-varying as well. Therefore, a LU decomposition needs to be performed to invert the matrix  $\mathbf{Y}$  in every emulation time-step and then to find the final network solution by using the nodal analysis method.

## D. Iron Core Hysteresis

The permeance matrix  $\mathbf{P}$  is divided into two sets  $\mathbf{P}^M$  and  $\mathbf{P}^P$  as described in Section II(C). The entries in the matrix  $\mathbf{P}^P$  representing the leakage permeance are constant, however, the entries in the matrix  $\mathbf{P}^M$  representing the nonlinear iron permeance change in every simulation time-step. In this work, the Preisach model [18] is used to represent the nonlinearity as well as hysteresis behaviour. The major loop function is represented as (17), once the major loop function is fixed, all the minor loop trajectories from a reversal point follow this uniform template,

$$\boldsymbol{B}_{p\_m}(\boldsymbol{H}_m) = \frac{1}{2} \sum_{u=1}^{3} a_u [\tanh(b_u \boldsymbol{H}_m) + c_u \sec h^2(b_u \boldsymbol{H}_m)],$$
(17)

where  $a_u, b_u, c_u$  are the parameters to define this hyperbolic template,  $\mathbf{H}_m = [H_{m1} \ H_{m2} \ \dots \ H_{mnl}]^T$  is the magnetization current vector flowing through the nonlinear elements and  $\mathbf{B}_{p\_m} = [B_{p\_m1} \ B_{p\_m2} \ \dots \ B_{p\_mnl}]^T$  are the flux corresponding to this current vector on the major loop. The subscript 'p\_m' stands for Preisach major loop and  $n_l$  stands for the number of nonlinear permeance.

Once the major loop function is defined, all the upward and downward minor loop trajectories from a reversal point  $(H_{rl}, B_{rl})$  follow this uniform template can be expressed as (18) and (19), respectively, with  $H_r = [H_{r1} \ H_{r2} \ \dots \ H_{rn_l}]^T$ and  $\mathbf{B}_r = [B_{r1} \ B_{r2} \ \dots \ B_{rn_l}]^T$ :

$$B_{p\_u}(H_m) = -B_{p\_m}(-H_m) - B_{p\_m}(H_r) + B_r \quad (18)$$
  
+ 2K(-H<sub>r</sub>)K(H<sub>m</sub>),  
$$B_{p\_d}(H_m) = B_{p\_m}(H_m) + B_{p\_m}(-H_r) + B_r \quad (19)$$
  
- 2K(H<sub>r</sub>)K(-H<sub>m</sub>),

where

$$\begin{aligned} \boldsymbol{K} &= [K_1 \ K_2 \ \dots \ K_{n_l}], \\ K_l(x) &= \begin{cases} \sqrt{\phi_{p\_m}(-x)}, & x < 0\\ \frac{\phi_{p\_m}(-x) + \phi_{p\_m}(x)}{2\sqrt{\phi_{p\_m}(x)}}, & x > 0, \end{cases} \\ l &= 1, 2, \dots, n_l. \end{aligned}$$

A Preisach Hysteretic Unit (PHU) shown in Fig. 5 is designed to implement this model. As shown in Fig. 3, a minor loop trajectory is enclosed in a major loop trajectory. In order to code the reversal point correctly, a reversal point stack RPS is necessary while traversing the hysteresis loop. In Fig. 3, the RPS initialized by saving the two points in the major loop, A and B at the bottom of the stack which can not be removed since all the minor loops are enclosed inside the major loop. Travelling on the major loop, a reversal point C is detected; then point C is pushed into the stack to define the upward minor trajectory C-D. When the trajectory reaches the next reversal point D, the downward minor trajectory D-C is defined by point D, which is also pushed into the stack. If this downward minor trajectory reaches point C and decrease further, the point B is used define the downward minor trajectory C-A, so that the last two reversal points C and D are removed from the stack.

Once the nonlinear B-H curve is obtained the nonlinear permeability  $\mu_{nl}$  can be calculated as,

$$u_{nl} = \frac{B_{nl}}{H_{nl}},\tag{20}$$

and the nonlinear permeance  $p_{nl}$  can be calculated as

$$p_{nl} = \frac{\mu_{nl}A}{0.5l},\tag{21}$$

where A is cross-sectional area and l is the length of the limb.

To calculate the linear air permeances, the value of leakage impedance  $X_{leakage}$  is necessary, which can obtained the shortcircuit test or provided by the transformer manufacturer. By assuming the leakage inductance are equally divided amongst the primary and secondary windings, the leakage permeance can be obtained as

$$P_{leakage} = \frac{0.5X_{leakage}}{2\pi f N^2},\tag{22}$$

where N is the number of winding turns.

### E. Core Eddy Currents

Eddy currents are frequency dependent current flows within the transformer core dissipated as active power loss. In the proposed nonlinear MEC-based ST model, the eddy current is represented by a four section cascaded R-L lumped circuit (continued fraction model). Compared to other lumped eddy current models such as Foster equivalent, uniformly and non-uniformly discretized lamination models, this model can achieve similar accuracy using fewer R-L sections which can simulate transients up to 200 kHz with an error less than 5% [19]–[21]. The discretizing Norton equivalent formula can be expressed as in (23), where  $i_E(t), v_E(t)$  and  $Y_E$  are the node current and voltage vectors, and lumped circuit admittance matrix, respectively,

$$\boldsymbol{i}_E(t) = \boldsymbol{Y}_E \boldsymbol{v}_E(t) + \boldsymbol{I}_{hist,E}(t), \qquad (23)$$

where  $I_{hist,E}(t)$  is the eddy current history term vector which is updated by:

$$\boldsymbol{I}_{hist,E}(t) = \mathbf{G}_E \boldsymbol{v}_E(t - \Delta t) + \boldsymbol{I}_{hist,E}(t - \Delta t).$$
(24)

2487

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Fig. 5. Pipelined and paralleled hardware design architecture during one time-step of emulation for the ST and the host power system.



Fig. 6. Finite state machine of the high-fidelity nonlinear MEC-based ST EMT model and power system.

In order to integrate the cascaded equivalent circuit into the MEC-based ST model, the required parameters of the lumped R-L circuit can be calculated by the following equations:

$$L_{0} = \frac{N^{2}A\mu}{l} \text{ and } L_{k} = \frac{L_{0}}{(4k-3)},$$
  

$$R_{0} = \frac{4N^{2}A}{ld^{2}\gamma} \text{ and } R_{k} = R_{0}(4k-1),$$
(25)

where  $\mu$  is the magnetic permeability of the steel lamination,  $\gamma$  is the electric conductivity of the steel lamination, A is the total cross-sectional area of all laminations, d is the thickness of the lamination, l is the length of core limb, and N is the number of coil turns.

Finally, the overall detailed frequency dependent nonlinear ST model is as shown in Fig. 4 where the cascade R-L circuit is externally interfaced to the MEC-based ST model.

## III. HARDWARE EMULATION OF HIGH-FIDELITY NONLINEAR MEC-BASED ST MODEL

## A. Network Transient Emulation With Embedded ST

The hardware emulation of the ST and other power system components, such as sources, passive elements, transmission



Fig. 7. FEM simulation: (a) coupled external electrical circuit, (b), (c) 3D FEM model.

lines and switch modules is depicted in Fig. 5, which fully exploits pipelining and parallelism to achieve real-time emulation. Each emulation time-step can be finished in 5 stages, and while the stages are executed sequentially, all the modules or units



Fig. 8. Single-line diagram of the power system with the ST model for the real-time HIL case study.



Fig. 9. Latencies for one emulation time-step for the high-fidelity MEC-based ST model.

within any stage are executed in parallel. All the calculations inside the hardware modules and units are fully pipelined and paralleled to achieve the lowest latency and resource consumption.

In Stage 1, the PHU is designed to evaluate the ST nonlinear iron core permeance matrix  $\mathbf{P}^{M}$  by reading the ST core fluxes  $\phi^M$ . Combining  $\mathbf{P}^M$  with the linear permeance matrix  $\mathbf{P}^{P}$  gives the overall permeance matrix  $\mathbf{P}$ , which is then involved in the computation of the matrix  $\mathbb{P}$  using (5). The eddy current module, as well as the transmission line and passive element modules in parallel update their history current terms by reading the node voltage vectors,  $v_E$  and  $v_O$ , respectively. The source module is designed to output the source voltage by reading a sinusoidal function look up table (LUT) implemented in it. The switch module sends the network admittance matrix  $\mathbf{Y}_N$  to the network solver module, combined with the ST admittance matrix  $\mathbf{Y}_{ST}$  to carry out the finally node voltage calculation. To efficiently perform the sparse and dense matrix-matrix and matrix-vector multiplications, such as in (5) and (15), a sparse-dense matrix multiplication unit (SMxDM) and matrix-vector multiplication unit (MxV) were designed respectively, in this work. In order to perform the matrix inversion operation in (5), (15) and (16), an LU-based Matrix Inverter Calculation (IMC) was implemented in the ST module, as described in Section III(B). The ST admittance matrix  $\mathbf{Y}_{ST}$  is combined with the network admittance matrix  $\mathbf{Y}_N$  to obtain the overall matrix **Y**. Similarly, the ST history current vector  $I_{hist,ST}$  is combined with the network history current terms  $I_{hist,N}$  and the source current injection vector  $I_s$  resulting in the  $I_{node}$  vector. Then the overall admittance matrix Y and the injection current vector  $I_{node}$  are forwarded to the Network Solver Module to finally find the network node voltages, consisting of  $v_{ST}$ ,  $v_E$ and  $v_{O}$ . The LU-based decomposition (**LUD**), forward substitution unit (**FWS**) and backward substitution unit (**BWS**) are implemented in the network solver module, and the vector  $I_{node}$ is pushed into the **FWS** unit input ports for the nodal solution.

Fig. 6 shows the detailed finite state machine (FSM) for the MEC-based ST and host power system hardware design. In the state  $S_1$ , the calculations in Stage 1 are executed including the transformer nonlinear iron core permeances, the eddy current module, as well as the passive element and transmission line modules update their history terms  $I_{hist,E}$  using (23) and  $I_{hist,O}$  in parallel. The Stage 2 is split into two states,  $S_2$  and

 $S_3$ . The state  $S_2$  performs two functions in parallel: 1) calculates matrix  $\mathbb{P}$  using (5), and 2) calculates network history terms  $I_{hist,N}$  by combining  $I_{hist,E}$  and  $I_{hist,O}$ . State  $S_3$  calculates the ST admittance matrix  $\mathbf{Z}_{ST}$  using (13). Stage 3 is also split into two states:  $S_4$  and  $S_5$ . In  $S_4$  the matrix  $\mathbf{Z}_{ST}$  goes through the IMC unit to compute the inverse matrix  $\mathbf{Z}_{ST}^{-1}$ . In state  $S_5$ the ST history term vector  $I_{hist,ST}$  and admittance matrix  $\mathbf{Y}_{ST}$ are computed in parallel using (15) and (16), respectively. The Stage 4 is fully implemented in  $S_6$ , to parallel compute the summation of the all the history currents  $I_{hist}$  and construct the entire power system network admittance matrix Y. The stage 5 is divided into two states,  $S_7$  and  $S_8$ . In state  $S_7$ , the current injection vector  $I_{node}$  is calculated and the network solver module is executed to compute the network node voltages v. Finally state  $S_8$  updates the transformer winding and yoke fluxes using (6).

## IV. REAL-TIME EMULATION CASE STUDIES

## A. Finite-Element Validation

To validate hardware emulation of the real-time MEC-based ST model, a 3-D three-phase, three-limb, twelve winding FE transformer model was developed in JMAG®. A half transformer core and coil model was built in JMAG Designer, which was then converted to a full transformer model by setting boundary symmetry. To build the half transformer model, 47730 elements and 8647 nodes were used with the element size of 0.15 m. To run a t = 0.5 s FE simulation with the time-step of  $\Delta t = 500 \ \mu s$  took more than 5 hours on a PC featured by Intel® i7 and 8 GB memory. The geometric parameters and the rating of the transformer can be found in the Appendix A. The symmetry boundary target is set in the middle of the model and its external coupled electrical circuit is shown in Fig. 7(a). In the coupled electrical circuit, each winding is assigned to a coil in the geometry model, and the current inflow face of each coil is as shown in Fig. 7(c). This 3D-FE ST model was connected with a voltage source on the primary side and an open-circuit on the secondary side.

#### B. Case Studies

The following case studies are analysed in this paper to show the accuracy and efficiency of the proposed the real-time hardware high-fidelity nonlinear MEC-based ST model. The power system shown in Fig. 8 consists of one ST model, two voltage sources,  $G_{s1}$  and  $G_{s2}$  and two transmission lines,  $L_1$  and  $L_2$ , modeled by the distributed parameter line model. In the case studies, the power system network including the ST is emulated on the Xilinx® Virtex-7 VC707 XC7VX485T FPGA, and the detailed latency for each FSM in one emulation time-step is summarised in Fig. 9. The maximum clock frequency of this design can reach to 90 MHz, with 3575 clocks latency for one time-step emulation giving the execution time of 40  $\mu$ s. The hardware resource utilization is summarised in Table I.

1) Energization Transient and Steady-State Emulation: To validate against the FE simulation results, the same power system is configured in Fig. 8 by the switching of  $SW_3$  to position 2 and leaving other breakers open. The parameters of the power system are given in Appendix C. The ST energization



Fig. 10. Real-time emulation and JMAG® simulation results for the energization transient.

TABLE I FPGA HARDWARE RESOURCE UTILIZATION

	MEC Based ST Model	Other Modules
Slice Registers	77631 (12.7%)	29267 (4.8%)
Slice LUTs	113746 (37.4%)	50562 (16.7%)
LUT-RAM	3180 (24%)	9636 (7.35%)
BRAM/FIFO	90 (2.9%)	59 (9.6%)
DSP48E1	746 (26.6%)	221 (7.6%)
BUFG	11 (34.4%)	4 (12.4%)

transient is initialized by closing the three-phase breaker  $SW_1$ at t = 0.05 s, and the inrush transient current flows through the breaker. The real-time inrush current emulation results and the corresponding 3D-FE simulation results are plotted in Fig. 10. The magnitude of the inrush current in different phases is determined by the instantaneous magnitude of the applied voltages in different phases when the breaker  $SW_1$  is closed. As can be seen in Fig. 10, the magnitude of transient current in phase-b and phase-c whose peak value can reach up to 80% of the ST rated current, is much larger than that in phase-a due to the above reason and all the currents in each phase decay to steady-state after t = 2 s, as shown in Fig. 11. The real-time emulation results show close agreement with the 3D-FE simulation results both in transient and steady state. However discrepancies exist in the magnitudes of the waveforms. The main reason for these differences is that even though the proposed real-time ST model was developed based on high-fidelity MEC approach, the mesh number and node are still much smaller than those in the FEM model. The Trapezoidal discretization can also introduce numerical differences between these two simulation results. Furthermore, in the FEM model, the nonlinear effect is modeled by a piece-wise nonlinear curve; however in the real-time MEC model the nonlinear effect in the ST core is represented by Preisach approach. In addition, even though the transformer core nonlinearity and frequency-dependent phenomena are included in the proposed model, this model cannot predict the high-frequency effects in the windings such as skin effect or proximity effect.

2) Hysteresis Transient Emulation: The hysteresis transient is emulated initializing the transformer core flux on the downward major loop trajectory (point A). Fig. 11 shows the real-time emulation results of the flux and the magnetizing current in the core and the hysteresis characteristic of the transformer. The ST is energized by a voltage source at a value of 0.8p.u. starting form t = 0 s and the corresponding hysteresis trajectory during the first cycle (A-B) is asymmetric due to the initial



Fig. 11. Real-time emulation and JMAG® simulation results for the ST steadystate current.

flux. After the first cycle, the flux travels on the set of asymmetric minor loops (C-D) due the asymmetric magnetizing current through the transformer core. From t = 0.087 s to t = 0.168 s, the breaker  $SW_1$  is opened and the flux is locked at 0.35 p.u. After t = 0.168 s the breaker  $SW_1$  is closed again and the value of voltage source increases to 1.2 p.u. The corresponding hysteresis trajectory (E-F) travels on the major loop since the voltage source is high enough to drive the transformer into the saturation region when the peak flux value reaches 1.2 p.u.

3) Power-Flow Control Emulation: To investigate of the ST transition response, during the step-by-step regulation active and reactive powers in transmission lines, the circuit shown in Fig. 8 was configured into a two transmission line system by opening breaker  $SW_4$  and switch  $SW_3$  to position 1 and leaving other breakers closed. The real-time emulation results of power regulation of the two lines is shown in Fig. 13.

At the beginning of the emulation, as shown in this figures, the ST works in the uncompensated mode; the line  $L_1$  active power  $P_{r1}$  and reactive power  $Q_{r1}$  is equal to 80 MW and -20 MVAr, respectively and the line  $L_2$  active power  $P_{r2}$  and reactive power  $Q_{r2}$  is equal to 38 MW and 20 MVAr, respectively, and the injected voltage is zero. At  $t_1 = 0.5$  s a compensation voltage of 0.25 p.u. at angle of 0° is requested by the controller which means that the tap-setting on the secondary winding of  $GP_1$  should start to increase to 0.25 p.u. with step size of 0.05 p.u., which require 0.5 s for each step transition. Thus from  $t_1 = 0.5$  s to  $t_2 = 3$  s the tap-setting increased to 0.25 p.u. with the step size of 0.05 p.u. in 2.5 s. As can be seen in Fig. 13 during this period, the powers  $P_{r1}$  and  $Q_{r1}$  increase while the powers  $P_{r2}$  and  $Q_{r2}$  decrease, which proves that the ST has the capability to regulate the power flow in both transmission lines.



Fig. 12. Real-time emulation results of (a) the magnetizing current (1 divx1 = 0.04 s; 1 divy1 = 0.04 p.u.); (b) flux in the core (1 divx2 = 0.04 s; 1 divy2 = 0.32 p.u.); (c) the hysteresis characteristic of ST (1 divx3 = 0.04 p.u.; 1 divy3 = 0.32 p.u.).

Finally, the  $P_{r1}$  and  $Q_{r1}$  increase to 134 MW and 98 MVAr, and  $P_{r2}$  and  $Q_{r2}$  decrease to 5 MW and -98 MVAr respectively. At  $t_3 = 3.5$  s, the controller sends a request to ST to inject a compensation voltage of 0.4 p.u. at an angle of 240°, thus the ST secondary winding tap-setting of  $GP_1$  needs to decrease to 0 p.u. again and  $GP_3$  needs to increase to 0.4 p.u. Starting from  $t_3 = 3.5$  s to  $t_5 = 6$  s, the  $GP_1$  windings' tap-setting decreases to 0 p.u. position, and GP<sub>3</sub> increases to 0.25 p.u. position, respectively. From  $t_5 = 6$  s, the  $GP_3$  winding increases further to 0.4 p.u. As can be seen during this period the reactive power in both  $L_1$  and  $L_2$  is kept constant since the angle of the injection voltage is equal to 240°. The ST secondary winding current transition behavior during the entire period (t = 0 s to 7.5 s) is shown in Fig. 14(a). The current magnitude decreases during the power reversal period, starting from  $t_3 = 3.5$  s until  $t_4 = 5.5$  s since the absolute value of active power is decreased, however at the time  $t_4 = 5.5$  s the current magnitude starts to increase due to the fact that the absolute active power value is increased at this time, as shown in Fig. 13. The transition of the corresponding injected compensation voltage is shown in Fig. 14(b); the initial value is zero since the ST works in uncompensated



Fig. 13. Real-time emulation of active power and reactive power regulation on the two transmission lines (a) Line  $L_1$  (1 divx1 = 0.8 s; 1 divy1 = 30MW/MVAr); (b) Line  $L_2$  (1 divx2 = 0.8 s; 1 divy2 = 43 MW/MVAr).



Fig. 14. Real-time emulation of step-by-step transition response of (a) secondary winding current (1 divx1 = 0.8 s; 1 divy1 = 0.18 p.u.); (b) injected compensation voltage of ST (1 divx2 = 0.8 s; 1 divy2 = 0.084 p.u.).

mode, and then the step-by-step changing of the voltage magnitude can be clearly seen at the request of the controller.

4) Fault Transient Emulation: A three-phase to ground fault was created at  $t_1 = 2.1$  s at the receiving end of the Line  $L_1$  and cleared at  $t_2 = 2.15$  s. Fig. 15 shows the real-time emulation results of the ST secondary side voltage and current, as well as the



Fig. 15. Real-time emulation results of ground fault transient (a) secondary side current (1 divx1 = 0.01 s; 1 divy1 = 0.95 p.u.); (b) secondary side voltage (1 divx2 = 0.01 s; 1 divy2 = 0.32 p.u.); (c) injected compensation voltage (1 divx3 = 0.01 s; 1 divy3 = 0.067 p.u.).

injected compensation voltage. The fault current peak magnitude reached up to 3.8 p.u. compared to the steady-state magnitude of 0.7 p.u. and decays to steady-state after 2.4 s. The magnitude of ST secondary side fault transient voltage decreased to 0.64 p.u. from 1.16 p.u. in the steady-state, and the recovery voltage reach to 1.40 p.u. then decays to steady-state in two cycles. The recovery injection compensation voltage is up to 0.3 pu compared to 0.2 p.u. under steady-state. At the inception and clearing of the fault the high frequency transient can be observed.

## V. CONCLUSION

A power-flow controller comprised of the Sen transformer has the potential of providing a low-cost alternative for power-flow regulation in stressed transmission networks. This paper presented a real-time electromagnetic transient model of the ST based on a high-fidelity magnetic equivalent circuit accounting for the major linear and nonlinear flux paths in the transformer core. Such a model can be used in a HIL scenarios to not only implement and test newer power-flow control algorithms, but can also be used for the electromagnetic transient analyses, transformer design optimization, energy efficiency analyses and for designing protection schemes, for transformers used in various applications. The exploitation of full parallelism and deep pipelining on the FPGA has resulted in an ST model that is not only highly accurate but also has a low computational latency and resource consumption to be included in HIL emulations. The proposed real-time model is able to accurately capture the nonlinear behavior due to core saturation, hysteresis and eddy currents. Comparison with finite-element simulations prove satisfactory performance of the real-time model. Future work in this area would include

inclusion of an electronic tap changer to increase the speed of operation of ST for power-flow control.

### APPENDIX

A. Geometry parameters of transformer: limb length: 7.18 m, limb cross-section area:  $0.454 \text{ m}^2$ , yoke length: 2.66 m, yoke cross-section area:  $0.454 \text{ m}^2$ .

B. Magnetic equivalent circuit parameters: material resistivity:  $5.2^{-7}$  ohm/m, lamination thickness: 0.0005 m,  $X_{leakage}$ : primary winding: 0.25 mH; winding numbers: primary side 64, secondary side 26; parameters of hysteresis trajectory:  $a_1 = 0.7900, a_2 = 486, a_3 = 312, b_1 = 0.00186, b_2 = 0.011236, b_3 = 0.01898, c_1 = 0.4271, c_2 = 0.3824, c_3 = 1.0406.$ 

C. Parameters of the case study, for energization transient:  $V_{base}$  :  $20/\sqrt{3}$  kV, voltage source 1.0 p.u.,  $R_s = 0.507 \Omega$ ; for hysteresis transient: voltage source  $V_{base}$  :  $16/\sqrt{3}$  kV; for power-flow control emulation and fault transient:  $G_1 = 28$  kV,  $G_2 = 28$  kV lagging  $20^{\circ}$ ; Transformer ST: 260 MVA; System base values:  $V_{base} = 28$  kV,  $S_{base} = 260$  MVA; Transmission line inductance: mode 0:  $5.819 \times 10^{-7}$  H/m, mode +:  $1.556 \times 10^{-7}$  H/m; Transmission line capacitance: mode 0:  $0.012 \times 10^{-8}$  F/m, mode +:  $0.0194 \times 10^{-8}$  F/m; Transmission lines  $L_1, L_2$ : 10 km, 12 km; Loads  $Load_1 : 10 \Omega$ ; Impedance:  $Z_1 : 0.5 \Omega$  and  $19.17 \times 10^{-6}$  H;  $Z_2 : 0.4 \Omega$  and  $10.17 \times 10^{-6}$  H

D. Tap changer: 8 tap positions, 0.05 p.u./step, 0.5 s/step.

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