# Implementation of an FPGA-Based Online Hardware-in-the-Loop Emulator Using High-Level Synthesis Tools for Resonant Power Converters Applied to Induction Heating Appliances

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***Abstract*—This paper proposes a field-programmable-gate-array-based emulator of the series-resonant half-bridge inverter for measuring the inverter efficiency and detecting hard-switching conditions. The proposed emulator is able to compute the converter operating conditions and efficiency each mains half-cycle, providing useful information for the control unit. In addition, it is designed taking advantage of recent advances in high-level synthesis tools, which provides an optimized and straightforward implementation. The proposed emulator has been applied to an induction heating (IH) appliance as an example of efficient and environmentally friendly appliances with a major economic and social impact. The obtained results are compared with classical offline simulation and experimental measurements, proving that the proposed emulator achieves the required accuracy for the IH application. As a consequence, the proposed system can be used for improving the system safety and optimizing the converter efficiency and reliability.**

***Index Terms*—Digital control, field-programmable gate arrays (FPGAs), hardware in the loop (HIL), high-level synthesis, induction heating (IH), resonant power conversion.**

## I. Introduction

INDUCTION heating (IH) cooktops are gaining popularity because of their advantages with respect their counterparts. Among these advantages are the safety, the cleanness, and the efficiency of the heating process. These appliances have to fulfill the user expectations and to ensure the system safety and to comply with the pertinent regulations. Moreover, IH developers make a special effort to improve the system efficiency due to its economic, environmental, and social advantages [1], [2].


Fig. 1. IH cooktop functional view.

Fig. 1 shows the main components of an IH appliance. From a functional point of view, these appliances consist of three main subsystems: *power electronics*, *control electronics*, and *inductor–vessel system*. The power electronics subsystem transfers the power from the mains to the vessel. The main component is the resonant inverter, which supplies a medium-frequency (30–80 kHz) current to the inductor coil. Commonly, IH appliances feature resonant or quasi-resonant inverter topologies such as the full-bridge [3], half-bridge (HB) [4], [5], single-switch [6], [7], and multiinverter topologies [8]. Among them, the series-resonant HB (SR-HB) inverter is the most used because of its good tradeoff between cost and performance. The inductor–vessel system is composed of the inductor coil and the vessel. The coupling between them is commonly modeled as the series connection of an equivalent resistance, i.e., $R_{\mathrm{eq}}$, and an equivalent inductance, i.e., $L_{\mathrm{eq}}$ [4], [9]. Due to the fact that the inductor–vessel system is part of the resonant tank, its impedance sets the inverter operating point and safe operating area (SOA). Finally, the control electronics subsystem manages the inverter operation and performs high-level tasks, e.g., user interface and vessel detection. The power supplied to the vessel is controlled by applying one or more inverter modulation strategies. The most used modulation

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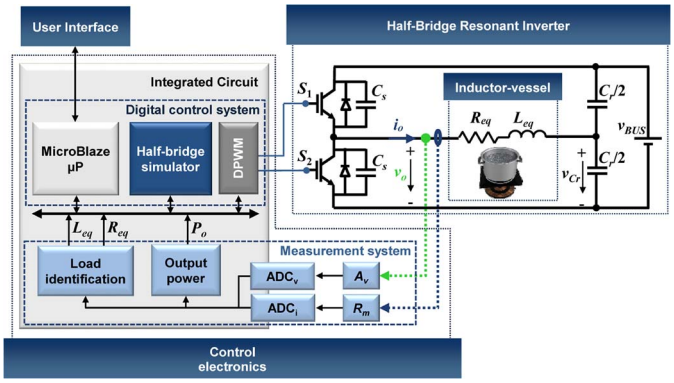



Fig. 2. IH system.

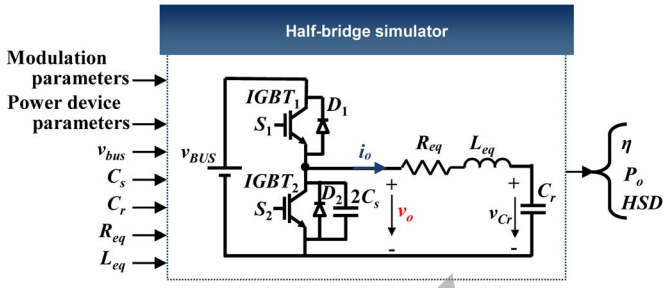



Fig. 3. SR-HB emulator.

strategies applied to the SR-HB inverter topology are square wave modulation [10], asymmetrical duty cycle control, pulse density modulation strategy [11], and discontinuous mode control. Due to the fact that the implementation of the aforementioned tasks requires complex and math-intensive control algorithms, digital control architectures [12] are usually selected to implement the IH control electronic system, including either microprocessors, FPGAs/application-specified integrated circuits (ASICs), or both of them [13].

IH appliances have to perform output power control for a wide range of operating conditions and loads. Although the power control algorithm is intended to supply the selected power to the vessel, the power stage safety has also to be ensured. Several causes may lead to an unsafe inverter operation. Among them are that the resonant power converter is not operating under soft-switching conditions, that the power device maximum ratings have been exceeded, or a low-efficiency inverter operation. Due to these facts, the inverter efficiency measurement and the hard-switching operation detection would be helpful to improve the power control algorithm performance when operating under real operating conditions. In this paper, an online hardware-in-the-loop (HIL) emulator [14]–[16] of the resonant converter is proposed, taking advantage of the online load identification system detailed in [17]. The proposed HIL emulator performs online efficiency measurement and hard-switching operation detection, allowing to improve the converter performance. The proposed emulator will be embedded within the complete FPGA-based control system, and its implementation will be performed taking advantage of the recently developed high-level synthesis tools [18]–[20].

The remainder of this paper is organized as follows. Section II details the design of the proposed SR-HB emulator. Section III details its FPGA implementation, and Section IV presents the main simulation and experimental results. Finally, the main conclusions of this paper are drawn in Section V.

## II. SR-HB Emulator Design

### A. SR-HB Inverter Emulator for Domestic IH

Fig. 2 shows the SR-HB inverter schematic circuit and the control electronics general block diagram for the *online SR-HB emulation* application. The impedance of the SR-HB inverter resonant tank is a series $RLC$ circuit made up of the inductor–vessel equivalent circuit parameters, i.e., $R_{\rm eq}$ and $L_{\rm eq}$, and the resonant capacitor, i.e., $C_r$. The resonant capacitor value is a design parameter, and therefore, it is considered known. The inverter is controlled applying the asymmetrical duty cycle modulation strategy, which controls the output power by modifying the switching frequency, i.e., $f_{\rm sw}$, and the duty cycle, i.e., $D$. To minimize the turn-off switching losses, two snubber capacitors, i.e., $C_s$, are included in parallel with the power devices. The control electronics system consists of the *measurement system* and the *digital control system*. The measurement system identifies the inductor–vessel model parameters and measures the power supplied to the vessel [21], [22]. The digital control system manages the IH system operation. This system performs the power control algorithm and implements several safety tasks to ensure the system integrity. Among them are the verification of the inverter soft-switching conditions and whether the power devices are operating inside their SOA.

The general block diagram of the SR-HB emulator is shown in Fig. 3. The HB circuit shown in Fig. 2 has been simplified to the equivalent SR-HB converter detailed in Fig. 3 to minimize the emulator hardware requirements. The emulator inputs configure the main emulation parameters: modulation parameters, power device [insulated-gate bipolar transistor (IGBT) and power diodes] model parameters, bus voltage, i.e., $v_{\rm BUS}$, snubber capacitor value $C_s$, and the resonant tank parameter values $R_{\rm eq}$, $L_{\rm eq}$, and $C_r$. The proposed emulator returns the inverter efficiency, i.e., $\eta$, the output power, i.e., $P_o$, and the hard-switching detection *(HSD)* signal that measures whether the zero voltage switching (ZVS) condition is satisfied, checking that the snubber capacitors have been completely charged or discharged before the IGBT commutation [23].

The online emulator application imposes several constraints to the HB emulator, which have to be fulfilled. The accuracy of the efficiency estimation and the output power have to be better than $0.1\%$ and $5\%$, respectively. Moreover, the emulation time is limited. Fig. 4 shows the time diagram of the closed-loop control algorithm. The control algorithm is executed at the zero-crossing of the mains voltage as part of the control interrupt service routine $\rm ISR_{Ctrl}$, when the signal *Sync.* is activated. The control algorithm sets the modulation parameters for the next mains half-cycle. Moreover, this routine starts the SR-HB emulation (*HB sim*) and evaluates the emulation results. Thus, in order to achieve online emulation, the SR-HB emulator has to complete the required emulation before the next zero-crossing of the mains voltage. Considering a mains frequency of 50 Hz, the available time is $T_B = 10$ ms.

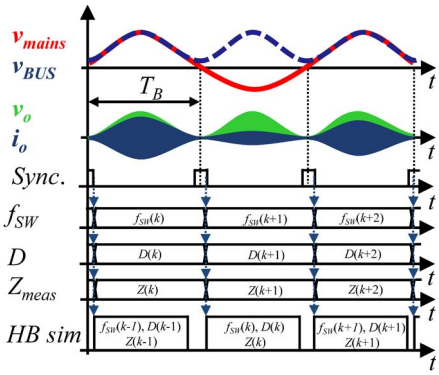
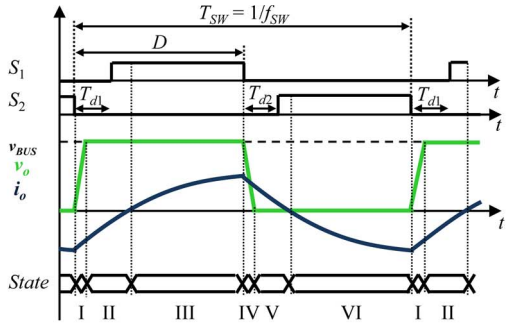
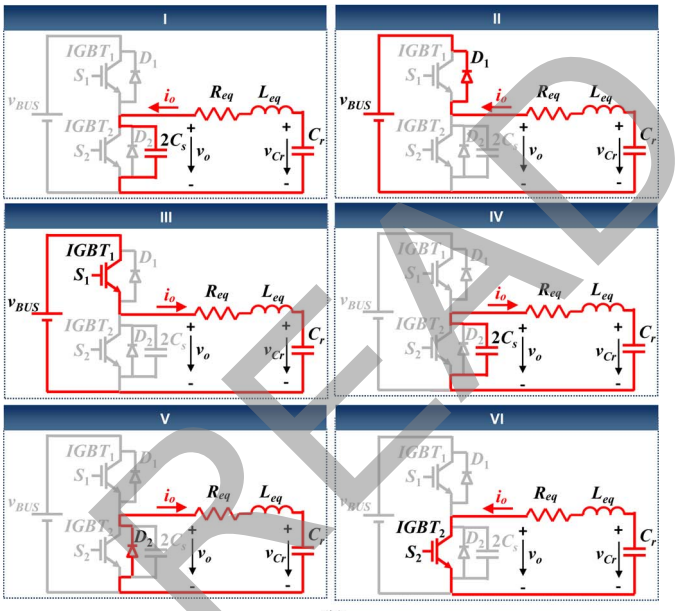



Fig. 4. SR-HB emulator time diagram.




(a)




(b)

Fig. 5. SR-HB inverter. (a) Main waveforms and modulation parameters while working under soft-switching conditions. (b) Circuit stages.

## B. Modeling of the Converter

The SR-HB emulator implements the schematic detailed in Fig. 3. The semiconductor power devices have been considered quasi-ideal, and the only parameter considered at this point is the voltage drop in the IGBT saturation state, i.e., $V_{\mathrm{ce,sat,IGBT}}$, and diode on state, i.e., $V_{d,\mathrm{on},D}$. The SR-HB main waveforms while operating under ZVS conditions are illustrated in Fig. 5(a). The HB inverter operation can be divided into six different states. Fig. 5(b) shows the circuit elements involved in each stage. The inverter states can be classified into two groups according to the output voltage $v_o$ characteristic. In states II, III, V, and VI, the output voltage is an independent voltage source fixed by the bus voltage and the power device voltage drop parameters $V_{\mathrm{ce,sat,IGBT}}$ and $V_{d,\mathrm{on},D}$. Moreover, these parameters are considered as constants during the emulation. On the other hand, during states I and IV, the output voltage is a state variable of the series $2C_s-R_{\mathrm{eq}}-L_{\mathrm{eq}}-C_r$ circuit.

TABLE I
OUTPUT VOLTAGE VALUE FOR EACH INVERTER STATE

| State | II | III | V | VI |
|---|---|---|---|---|
| $v_o$ | $v_{BUS}$-$V_{ce,sat,IGBT}$ | -$V_{d,on,D}$ | $V_{d,sat,IGBT}$ | $v_{BUS}$+$V_{ce,on,D}$ |

The SR-HB inverter has been modeled by using the state-space description. For each state, the state-space description is given by

$$\dot{\mathbf{x}}_i(t) = \mathbf{A}_i\mathbf{x}_i(t) + \mathbf{B}_i\mathbf{u}_i(t) \tag{1}$$

where subscript $i$ denotes the circuit configuration, i.e., SR-HB state, $\mathbf{x}_i(t)$ is the energy state vector, $\mathbf{u}_i(t)$ is the independent input sources vector, and the matrices $\mathbf{A}_i$ and $\mathbf{B}_i$ depend on the equivalent converter configuration.

For digital emulation, this continuous-time model has been discretized using the forward Euler method due to its simplicity. The discrete-time model is given by

$$\mathbf{x}_i(k+1) = \mathbf{F}_i\mathbf{x}_i(k) + \mathbf{G}_i\mathbf{u}_i(k). \tag{2}$$

In the case of independent output voltage, the equivalent circuit is a series $R_{\mathrm{eq}}-L_{\mathrm{eq}}-C_r$ circuit, which is in series with the output voltage $v_o$. Considering the inductor current, i.e., $i_o$, and the resonant capacitor voltage, $v_{\mathrm{Cr}}$, as the system state variables, this system can be modeled as

$$\begin{aligned}\begin{pmatrix} i_o(k+1) \\ v_{\mathrm{Cr}}(k+1)\end{pmatrix} &= \mathbf{F}_{\mathrm{independent}}\begin{pmatrix} i_o(k) \\ v_{\mathrm{Cr}}(k)\end{pmatrix} \\ &\quad + \mathbf{G}_{\mathrm{independent}}v_o(k) \\ \begin{pmatrix} i_o(k+1) \\ v_{\mathrm{Cr}}(k+1)\end{pmatrix} &= \begin{pmatrix} 1-\frac{T_{\mathrm{st}}R_{\mathrm{eq}}}{L_{\mathrm{eq}}} & \frac{-T_{\mathrm{st}}}{L_{\mathrm{eq}}} \\ \frac{T_{\mathrm{st}}}{C_r} & 1\end{pmatrix}\begin{pmatrix} i_o(k) \\ v_{\mathrm{Cr}}(k)\end{pmatrix} \\ &\quad + \begin{pmatrix} \frac{T_{\mathrm{st}}}{L_{\mathrm{eq}}} \\ 0\end{pmatrix} v_o(k)\end{aligned} \tag{3}$$

where $T_{\mathrm{st}}$ is the SR-HB emulator sampling time, that is, the interval of the SR-HB emulation samples.

Table I shows the output voltage value for each state.

During states I and IV, the equivalent circuit is a series $2C_s-R_{\mathrm{eq}}-L_{\mathrm{eq}}-C_r$ circuit without independent sources. Considering the inductor current and the capacitor voltage $i_o$ and $v_{\mathrm{Cr}}$ as the system state variables, this system can be modeled as

$$\begin{aligned}\mathbf{x}(k+1) &= \mathbf{F}_c\mathbf{x}(k) \\ \begin{pmatrix} i_o(k+1) \\ v_{\mathrm{Cr}}(k+1) \\ v_o(k+1)\end{pmatrix} &= \begin{pmatrix} 1-\frac{T_{\mathrm{st}}R_{\mathrm{eq}}}{L_{\mathrm{eq}}} & \frac{-T_{\mathrm{st}}}{L_{\mathrm{eq}}} & \frac{T_{\mathrm{st}}}{L_{\mathrm{eq}}} \\ \frac{T_{\mathrm{st}}}{C_r} & 1 & 0 \\ \frac{T_{\mathrm{st}}}{2C_s} & 0 & 1\end{pmatrix}\begin{pmatrix} i_o(k) \\ v_{\mathrm{Cr}}(k) \\ v_o(k)\end{pmatrix}.\end{aligned} \tag{4}$$

TABLE II
RANGE OF VALUES OF THE IH SYSTEM PARAMETERS

| Parameter | Minimum value | Maximum value |
|---|---|---|
| $L_{eq}$ | 10 µH | 30 µH |
| $R_{eq}$ | 2.5 Ω | 8 Ω |
| $C_s$ | 5 nF | 20 nF |

### C. HB Emulator Design

The emulation performance highly depends on the emulation parameters, the approximations considered, and the device models selected. Moreover, these parameters have to be designed to meet the specific application requirements. The next points detail the design of the SR-HB emulation parameters.

*Emulation Time Step Selection:* In this paper, the emulation step $T_{\rm st}$ has been selected to be fixed. Then, the emulation step selection is a tradeoff between accuracy and resource consumption. Small emulation steps entail good accuracy at the expense of increasing the required resources. Moreover, the emulation step has to be designed to be low enough to allow the emulation model to follow the system dynamic response. The fastest dynamic response of the HB inverter corresponds with HB states I and VI. Due to the fact that the snubber capacitor value is much lower than the resonant capacitor, i.e., $C_s \ll C_r$, the equivalent $2C_s{-}R_{\rm eq}{-}L_{\rm eq}{-}C_r$ circuit can be approximated by the equivalent $2C_s{-}R_{\rm eq}{-}L_{\rm eq}$ circuit. This circuit is a second-order circuit whose characteristic equation is

$$s^2 + 2\xi\omega_o s + \omega_o^2 = 0 \tag{5}$$

where $\xi$ is the damping factor, and $\omega_o$ is the resonant angular frequency. These parameters can be calculated as

$$\omega_o = \frac{1}{\sqrt{L_{\rm eq}2C_s}} \quad \xi = \frac{R_{\rm eq}}{2}\sqrt{\frac{2C_s}{L_{\rm eq}}}. \tag{6}$$

In this paper, the circuit parameters have been considered to be in the ranges shown in Table II. These values entail underdamped response, i.e., $0 < \xi < 1$.

The period of the natural oscillation is given by

$$T_n = \frac{2\pi}{\omega_o\sqrt{1-\xi^2}}. \tag{7}$$

To follow the natural dynamic response, the emulation step has been selected to be $T_{\rm st} < T_n/10$, which entails a maximum emulation time of $T_{\rm st} < 199$ ns.

In addition to this, the forward Euler discretization method may transform stable continuous-time systems into unstable discrete-time systems. In order to ensure the discrete-time system stability, the modulus of the matrix $\mathbf{F}_c$ eigenvalues (4) has to be less than unity. In the case of a series $RLC$ circuit and the forward Euler discretization method, this entails that $T_{\rm st} < 2\xi/\omega_o$.

Considering the parameters shown in Table II, the maximum emulation step to ensure the stability is $T_{\rm st} = 25$ ns.

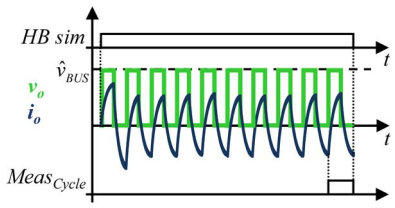



Fig. 6. SR-HB emulator time diagram.

Finally, the digital pulsewidth modulator (DPWM) clock frequency is 100 MHz (see Fig. 2). Thus, the IGBTs gating signals are generated with a resolution of 10 ns. In order to synchronize the emulation step with the gating signal changes, the emulation sampling frequency has been selected to be a multiple of the DPWM clock frequency.

The emulation time step has been selected to be the maximum emulation step, which complies with the aforementioned restrictions, leading to an emulation time step of $T_{\rm sim} = 10$ ns.

*Emulation Time Diagram:* Fig. 4 shows the control loop time diagram of the IH system. The HB emulator simulates the resonant inverter considering the operating conditions of the previous mains half-cycle by using the previous modulation parameters and the identified impedance, i.e., $Z_{\rm meas}$. Due to the high emulation sampling frequency and the number of required operations [see (3) and (4)], the real-time emulation of the whole half mains cycle, i.e., $T_B$, is unfeasible. Thus, in order to achieve online emulation, instead of emulating the whole half mains cycle, the proposed HB emulator has been designed to emulate the switching cycle placed at the peak of the bus voltage $\hat{v}_{\rm BUS}$.

The time diagram of the HB emulator is shown in Fig. 6. Due to fact that the switching frequency is much higher than mains frequency, the bus voltage has been considered constant during one switching cycle. Moreover, the proposed system simulates ten switching cycles in order to reach the steady-state operation. Thus, the required parameters are measured during the last switching cycle, i.e., $\rm Meas_{Cycle}$.

*Power Device Models:* The power device models have direct impact on the measurement accuracy and the emulation complexity. Since the proposed system is to be implemented in a mass-market cost-oriented application, the proposed architecture needs to be optimized. To maintain low emulation complexity while achieving good accuracy in the power dissipation measurements, two different device models have been considered: *emulation models* and *measurement models*. The emulation models, which are used for simulating the HB converter, are shown in Fig. 7(a) and (b). The IGBT and power diode models consist of the ideal power device in series with a forward voltage source, i.e., $V_{\rm ce,sat,IGBT}$ or $V_{d,{\rm on},D}$. The measurement models consider more complex power devices models [see Fig. 7(c) and (d)] to improve the power dissipation estimation. Both the IGBT and power diode models include a forward voltage source $V_{\rm ce,0,IGBT}$ or $V_{d,0,D}$ and a series equivalent resistance $R_{s,\rm IGBT}$ or $R_{s,D}$, respectively. Moreover, the IGBT switch-off current tail has been modeled to fall with two slopes, as shown in Fig. 7(c).

*Measurements:* The proposed emulator calculates the output power, the efficiency, and the hard-switching detection

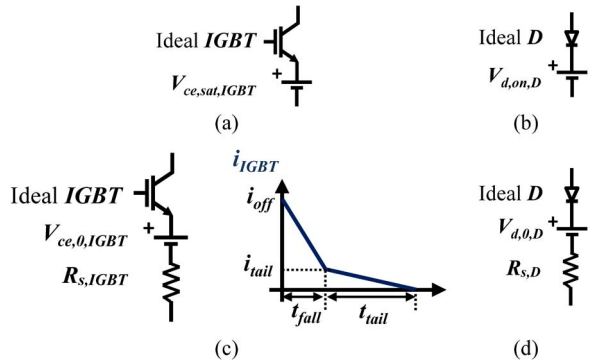



Fig. 7. Power device models. (a) Emulation IGBT model. (b) Emulation power diode model. (c) Measurement IGBT model. (d) Measurement power diode model.

parameters during the last simulated switching frequency cycle (see Fig. 6). First, several parameters of the power device currents and the output current are obtained using

$$|i_{\text{device}}|_{\text{mean}} = \frac{1}{N_{\text{SW}}} \sum_{k=1}^{N_{\text{SW}}} |i_{\text{device}}(k)| \tag{8}$$

$$i_{\text{device,rms}} = \sqrt{\frac{1}{N_{\text{SW}}} \sum_{k=1}^{N_{\text{SW}}} i^2_{\text{device}}(k)} \tag{9}$$

where $\hat{i}_o$ is the output current peak value, $i_{\text{device}}$ is the power device current, i.e., $i_{\text{IGBT}}$ or $i_D$ or the output current $i_o$, $|i_{\text{device}}|_{\text{mean}}$ is the mean of the absolute value of $i_{\text{device}}$, $N_{\text{SW}}$ is the number of samples in one switching cycle, and $i_{\text{device,rms}}$ is the root-mean-square (RMS) value of the device current.

The output power $P_o$ is calculated as

$$P_o = i^2_{o,\text{rms}} R_{\text{eq}}. \tag{10}$$

The power dissipated in the power diode is obtained using

$$P_D = |i_D|_{\text{mean}} V_{d,D} + i^2_{D,\text{rms}} R_{s,D}. \tag{11}$$

The power dissipated in the IGBTs is calculated as the sum of the conduction losses, i.e., $P_{\text{IGBT,on}}$, and the switching losses, i.e., $P_{\text{IGBT,sw}}$, i.e.,

$$P_{\text{IGBT}} = P_{\text{IGBT,on}} + P_{\text{IGBT,sw}} \tag{12}$$

where the conduction and switching losses are calculated integrating voltage and current as [24]

$$P_{\text{IGBT,on}} = |i_{\text{IGBT}}|_{\text{mean}} V_{\text{ce,IGBT}} + i^2_{\text{IGBT,rms}} R_{s,\text{IGBT}} \tag{13}$$

$$P_{\text{IGBT,sw}} = \left( \frac{2i_{\text{off}} i_{\text{tail}} + i^2_{\text{off}} - 3i^2_{\text{tail}}}{24 \cdot 2C_s} t^2_{\text{fall}} + \frac{4i_{\text{off}} i_{\text{tail}} - 3i^2_{\text{tail}}}{24 \cdot 2C_s} t^2_{\text{tail}} + \frac{i_{\text{off}} i_{\text{tail}} - i^2_{\text{tail}}}{2C_s} t_{\text{fall}} t_{\text{tail}} \right) f_{\text{SW}}. \tag{14}$$

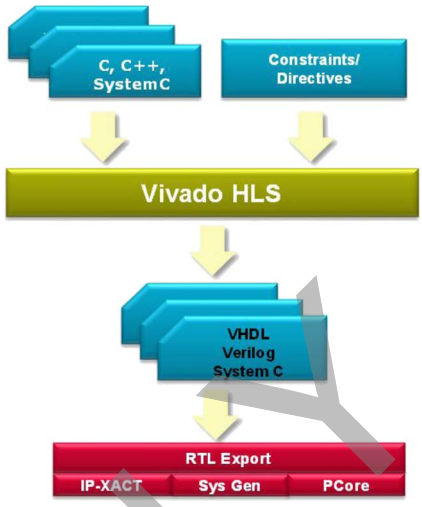



Fig. 8. High-level synthesis implementation workflow [25].

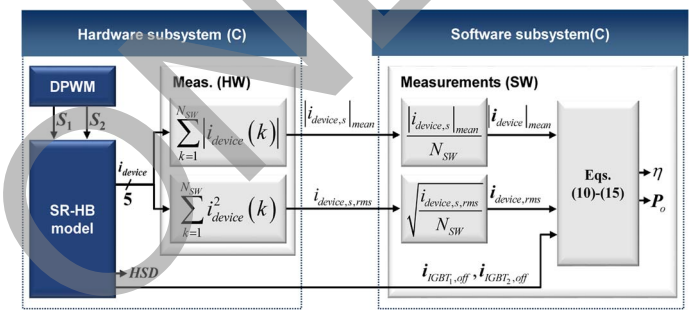



Fig. 9. Architecture of the proposed HB emulator.

The HB efficiency in percentage is computed as

$$\eta = 100 \frac{P_o}{P_o + P_{\text{IGBT}_1} + P_{\text{IGBT}_2} + P_{D_1} + P_{D_2}}. \tag{15}$$

Finally, the calculation of the hard-switching conditions detection (HSD) will be detailed in the FPGA implementation section.

## III. FPGA Implementation Using High-Level Synthesis Tool

The HB emulator has been implemented using the Vivado HLS tool. Fig. 8 shows the workflow proposed by Xilinx, where the source code, directly written in C, is translated by the tool into a hardware description language, such as VHDL, to get the register transfer level (RTL) description. It is important to highlight that this process is controlled by the user through directives, allowing optimizing the design according to prescribed constraints and an easy design-space exploration [26].

Fig. 9 shows the block diagram of the proposed HB emulator. It has been described in C language and takes advantage of the hardware–software codesign [27], which means that part of the algorithm will be implemented in hardware and part will be executed by the soft-core microprocessor. Since both parts are first described in C code, the whole system simulation is greatly simplified.

The hardware subsystem consists of three main blocks: *DPWM*, *HB model*, and *Measurements (HW)*. The DPWM

block implements the digital pulsewidth modulator that generates the gating signals, i.e., $S_1$ and $S_2$, of the power devices, i.e., $\text{IGBT}_1$ and $\text{IGBT}_2$. The HB model block implements the model of the HB inverter detailed in Section II. In case that improper switching is detected, the HB model block activates the hard-switching detection signal *HSD*. Finally, the Measurements (HW) block implements in digital hardware the high-demanding operations of the required measurements. These measurements operate the device currents at the rate of 100 MSPS.

The software subsystem implements the calculations that are computed only once per emulation. Therefore, the timing constraints to perform these calculations are not restrictive. First, the software subsystem calculates the required parameters of the power device currents by computing the operations of (8) and (9) that have not been implemented in hardware. From these parameters, the output power and efficiency parameters can be obtained as it has been previously detailed [see (10)–(15)].

In order to achieve the required accuracy, the SR-HB difference equations and the measurement equations have been implemented using single-precision floating-point format.

The main constraint of the proposed emulator is the maximum emulation time allowable to perform online emulation. The time diagram represented in Fig. 4 shows that the maximum emulation time is $T_{\text{emulation,max}} = 10$ ms. The emulation time, i.e., $T_{\text{emulation}}$, can be divided into the time required to simulate the hardware subsystem, i.e., $T_{\text{hardware}}$, and the time required to execute the software program, i.e., $T_{\text{software}}$. The $T_{\text{hardware}}$ time can be calculated as

$$T_{\text{hardware}} = N_{\text{sim}} T_{\text{CLK}} L_{\text{sim}} = 10 N_{\text{SW}} T_{\text{CLK}} L_{\text{sim}} = \frac{10 L_{\text{sim}}}{f_{\text{SW}}} \tag{16}$$

where $N_{\text{sim}}$ is the number of simulated samples, $T_{\text{CLK}}$ is the digital system clock frequency, $L_{\text{sim}}$ is the number of latency cycles required to calculate one emulation sample, $N_{\text{SW}}$ is the number of emulation samples in one switching cycle, and $f_{\text{SW}}$ is the switching frequency.

Considering $T_{\text{software}}$ much smaller than $T_{\text{hardware}}$, the emulation time $T_{\text{emulation}}$ can be approximated as $T_{\text{hardware}}$. Then, the maximum allowable emulation latency can be obtained as

$$L_{\text{sim}} < \frac{T_{\text{emulation,max}} f_{\text{SW}}}{10}. \tag{17}$$

Considering a minimum switching frequency of 30 kHz, the maximum allowable latency is $L_{\text{sim}} = 29$ cycles. This latency has been selected as a constraint in Vivado HLS. Consequently, Vivado HLS configures the system using the minimum number of paralleled arithmetic operators that complies with the selected latency, being the achieved value $L_{\text{sim}} = 17$ cycles. Then, the maximum emulation time consumed by the HB emulator, i.e., $T_{\text{emulation}}$, is approximately 6 ms, which complies with the system requirements. The logic resources used to implement the proposed HB emulator in a XILINX Spartan-6 XC6SLX45 FPGA are 3318 slice registers, 2911 slice lookup tables, and five DSP48A1s.

TABLE III
INDUCTION LOAD VALUES

| IH LOAD | $R_{eq}(\Omega)$ | $L_{eq}(\mu\text{H})$ |
|---|---|---|
| $L_1$ | 5 | 25 |
| $L_2$ | 4 | 15 |
| $L_3$ | 3.5 | 20 |
| $L_4$ | 2.92 | 19.4 |

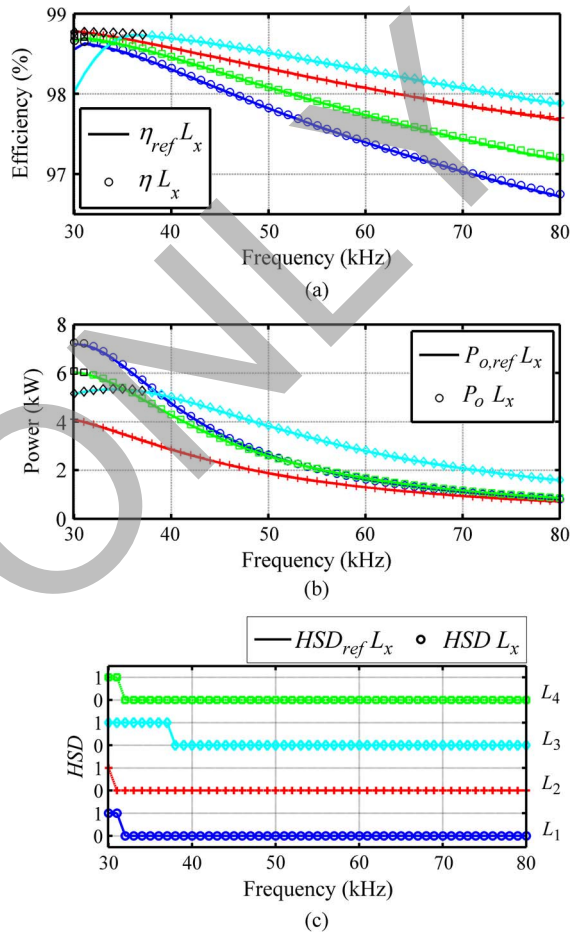



Fig. 10. Simulation results for different IH loads and 50% duty cycle. (a) Efficiency. (b) Output power. (c) Hard-switching detection.

## IV. SIMULATION AND EXPERIMENTAL RESULTS

### A. Emulator Accuracy

The implemented system has been simulated using the XILINX Vivado HLS tool. Moreover, the results obtained with the proposed SR-HB emulator have been verified with the ones obtained through circuital simulation. The reference test bench has been implemented using the mixed-signal simulation tool ADVance MS from Mentor graphics. The HB resonant inverter has been modeled in ELDO-Spice. In order to obtain accurate reference measurements, the SR-HB inverter has been implemented using the PSpice IGBT model (HGTG20N60) provided by the manufacturer. This model includes both IGBT and antiparallel diode models. Moreover, to compare these reference values with the simulator results, the bus voltage $v_{\text{BUS}}$ has been considered constant. The value of the resonant

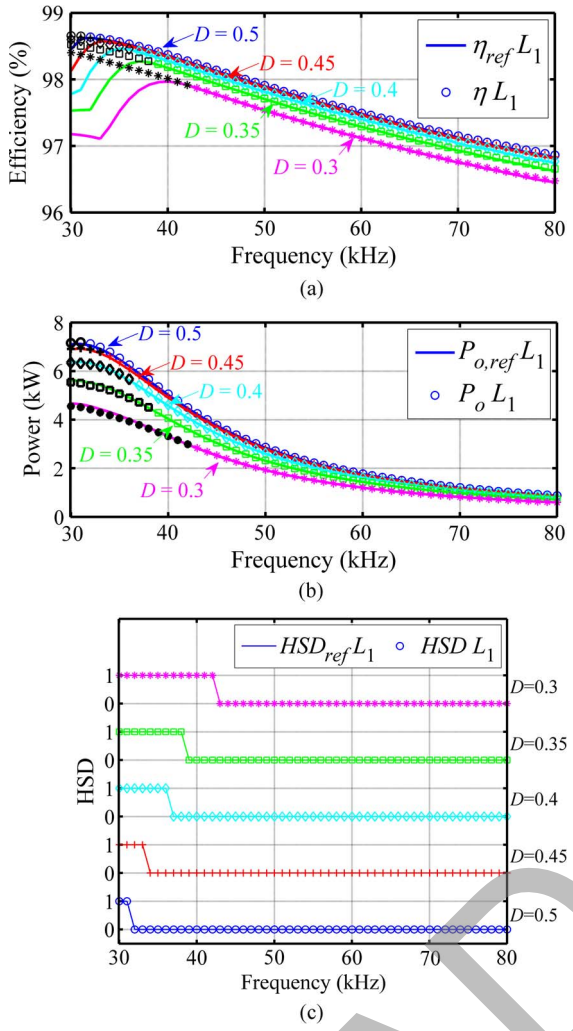



Fig. 11. Simulation results for different duty cycles. (a) Efficiency. (b) Output power. (c) Hard-switching detection.

capacitor has been selected to be $C_r = 1440$ nF, and the value of the snubber capacitors is $C_s = 15$ nF.

The simulation results for the four IH loads summarized in Table III, i.e., $L_1 - L_4$, and 50% duty cycle are shown in Fig. 10. These figures plot together the reference simulation values and the ones obtained with the proposed emulator for the following measurements: efficiency, output power, and hard-switching detection. The reference measurements, i.e., $\text{Param}_{\text{ref}}$, are displayed using lines, whereas the measurements performed with the proposed emulator, i.e., Param, are represented using markers. Moreover, black markers indicate that the SR-HB inverter is operating under hard-switching conditions. Fig. 11 shows the simulation results for the load $L_1$ and different duty cycles.

The simulation results show that the achieved accuracy is better than 0.04% for the efficiency measurement and approximately 1% for the output power measurement, which complies with application requirements. Moreover, the proposed HB emulator properly detects the hard-switching operating conditions.

## B. Experimental Results

The proposed online SR-HB emulator has been verified while operating under real operating conditions using an IH

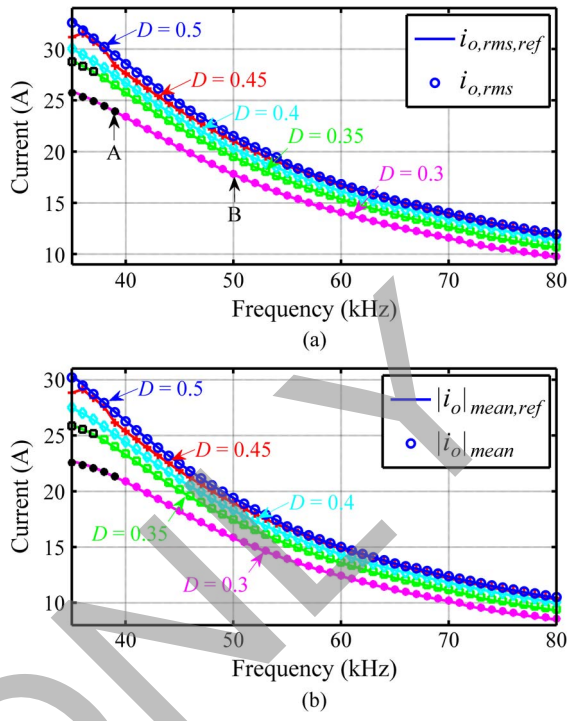



Fig. 12. Experimental results for different duty cycles. (a) Output current RMS value. (b) Output current mean of the absolute value.

prototype. The SR-HB inverter features HGTG20N60 IGBTs from Fairchild. The resonant capacitor value is $C_r = 1440$ nF, and the value of the snubber capacitors is $C_s = 15$ nF. Finally, the SR-HB inverter is fed by a dc voltage of $v_{\text{BUS}} = 230$ V.

The experimental test evaluates the emulator hard-switching detection capability and the accuracy of the output current RMS and mean of the absolute measurements. Fig. 12(a) and (b) shows the experimental results for the output current RMS value and the output current mean of the absolute value, respectively, for an IH load and different duty cycles. The measurement results obtained with the SR-HB emulator have been compared with the ones obtained with a DPO7354 oscilloscope from Tektronix and a Rogowski CWT current probe from PEM, which have been considered as the reference values. The reference measurements $\text{Param}_{\text{ref}}$ are displayed using lines, and the measurements performed with the proposed emulator Param are represented using markers. Finally, black markers indicate that the SR-HB emulator has detected hard-switching conditions.

Fig. 13(a) and (b) shows the main waveforms of the SR-HB inverter at experimental points A and B, respectively, which have been highlighted in Fig. 12(a). On the top are displayed the power devices gating signals $S_1$ and $S_2$. At the center are displayed the inverter output voltage and current signals. Fig. 13(a) shows the results for a 30% duty cycle and a switching frequency of 40 kHz. The inverter is operating under hard-switching conditions due to the fact that the snubber capacitors have not been completely charged before the $S_1$ activation. Fig. 13(b) shows the results for a 30% duty cycle and a switching frequency of 50 kHz. The inverter is operating under soft-switching conditions due to the fact that the output voltage has reached the bus voltage prior the $S_1$ activation.

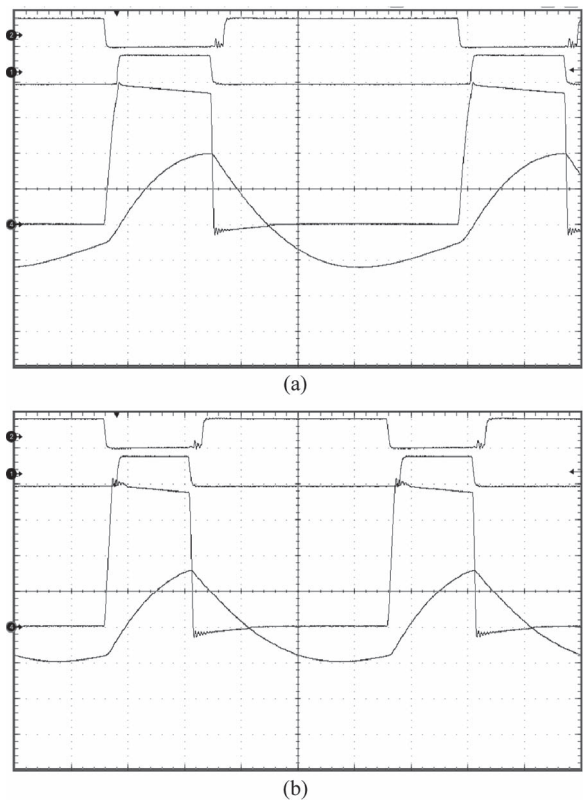



Fig. 13. Experimental waveforms for 30% duty cycle. (a) Hard-switching operating point A. (b) Soft-switching operating point B. (Top to bottom) $S_2$, $S_1$, $v_o$ (60 V/div), and $i_o$ (20 A/div).

The experimental results show that the proposed emulator provides accurate measurements along the whole operating range. Moreover, it properly detects when the power converter is operating under hard-switching conditions. Consequently, all the assumptions and simplified models proposed in the emulator design are proved to be valid, and the emulation tool feasibility for the IH application is confirmed.

## V. Conclusion

In this paper, an online SR-HB emulator applied to the domestic IH application has been proposed. The proposed emulator takes advantage of an online load identification system to estimate the power converter efficiency and to detect the hard-switching operation. The HB emulator has been implemented and verified using the high-level synthesis tool Vivado HLS using floating-point arithmetic, proving the benefits in terms of design-space exploration and optimization of such approach. Moreover, it has been designed as a hardware–software codesign.

In order to assess the accuracy of the proposed emulator, simulation and experimental analysis has been performed. The simulation results show that the proposed emulator achieves an accuracy better than 0.04% for the efficiency measurement and approximately 1% for the output power measurement. The experimental results validate the expected performance and prove the feasibility of the proposed online HB emulator. As a consequence, this system can be used for increasing the system safety and improving the power control behavior while operating under real operating conditions, with economic, environmental, and social advantages derived from the efficiency optimization. The proposed approach has a major potential impact, since it can be also extended to any other FPGA-controlled power converter.

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