Investigation of Eutectic and Solid State Wafer Bonding of Silicon with Gold

by

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ABSTRACT

Permanent wafer bonding technology is a very important process for different types of applications such as MEMS (microelectromechanical systems), LED (light-emitting diode) devices, advanced packaging, 3D stack and SOI (silicon on isolator) substrate applications. Depending on the type of application, several bonding technologies exist. The MEMS market road map suggests the market for MEMS will be close to $21B in 2017.

The driving force for development of different wafer bonding processes is the large applications that need to be addressed. The wafer bonding market generated almost 5 million 8-inch wafers bonded for BSI (back-illuminated sensor), CIS (CMOS image sensor) and MEMS device applications and it is expected to reach 16 million 8-inch bonded wafers in 2019. The growing demand is mainly driven by the miniaturization required for 3D Stack TSV (through- silicon via) applications.

Among different wafer bonding techniques, eutectic bonding is more appealing due to its good hermeticity, ability to create electrical connection, good mechanical strength and low temperature processing.

In this study, Au-Si eutectic bonding was applied due to its high bonding strength, excellent hermeticity and good tolerance to surface topology prior to bonding. Au/a-Si wafer bonding was introduced in order to reduce the risk of possible damage to active devices in Au/c-Si wafer bonding due to formation of large craters in c-Si. Solid state

bonding was introduced in order to reduce the process temperature, which is desirable in the manufacturing industry. Bonding parameters were optimized as much as possible. The microstructure of bonded pairs was imaged using SEM (scanning electron microscopy) and TEM (transmission electron microscopy) for both Au/a-Si and Au/c-Si samples and for both eutectic and solid state methods. In-situ TEM imaging of the Au/a-Si diffusion couple during annealing was performed in an attempt to understand and explain the reason for the layer exchange mechanism in Au/a-Si wafer bonding. The diffusion coefficient for Au in a-Si was also calculated using in-situ TEM results. The mechanical strength of bonded wafers was measured using shear testing on eutectic and solid state bonded Au/a-Si and Au/c-Si samples.

KEYWORDS: Au, a-Si, c-Si, wafer bonding, eutectic bonding, solid state bonding

PREFACE

This thesis is an original work by Maryam Abouie carried out at University of Alberta under the supervision of Professor D.G. Ivey and Professor Q. Liu.

Part of Chapter 4 of this thesis has been published as Maryam Abouie, Qi Liu, Douglas G. Ivey, “Eutectic and solid-state wafer bonding of silicon with gold”, Materials Science and Engineering: B, vol. 177, issue 20, December 2012, 1748-1758. I was responsible for the data collection and analysis as well as the paper composition. Douglas G. Ivey and Qi Liu assisted with paper composition and edits.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS

D_i	Interstitial diffusivity in hypothetical trap-free a-Si
H_i^M	Boltzmann constant
T	Temperature
σ	Residual stress
h_s	Substrate thickness
h_f	Thin film thickness
E_s	Young's modulus
ν_s	Poisson's ratio
α	Coefficients of thermal expansion
ρ	Density
Z	Acoustic impedance
P	Pressure
A	Area
F	Force
D	Diffusion coefficient
D_0	Frequency factor
Q	Activation energy
R	Ideal gas constant
ω	Peak position
I_{L_0}	Maximum peak amplitude
Γ	FWHM
μ	Mean of the total population
S	Standard deviation
n	Sample size
$\overline{X}$	mean of the sample population

Chapter 1

Introduction

Chapter 1 - Introduction

MEMS (microelectromechanical systems) have been applied for the fabrication of numerous devices, some of them have been widely used for several years and some of which are under development. There are various wafer bonding techniques. Apart from direct bonding, other processes based on using an intermediate layer are wildly being used. Selection between different intermediate layers is based on required process temperatures and other materials properties (i.e., thermal conductivity, electrical conductivity and outgassing).

Among different bonding methods, eutectic bonding has several advantages over other methods. Eutectic wafer bonding takes advantage of the special properties of eutectic metals. Similar to soldering alloys, they have low melting temperatures. This property is beneficial to achieve planar surfaces.

Various eutectic systems have been reported and studied, such as Au-Sn, Au-Si, Al-Ge, Au-Ge and Au-In. The main advantages of the Au-Si system are good mechanical stability and the absence of intermetallics which can cause fabrication issues. Au-Si is used in microfabrication because of its high bonding strength, excellent hermeticity which permits vacuum wafer-level packaging and good tolerance to surface topography as a result of the formation of a liquid phase. It is also a good heat sink for packaged devices such as high power transistors, lasers and LED devices. Au-Si eutectic bonding is not without its limitations; however, including high cost (due to the presence of Au), high modulus of elasticity, limited die size and the potential for chip damage.

The typically used Au-Si eutectic bonding temperature is 400°C, but there are two issues with this condition. First, this temperature may be too high and may damage devices on the wafer during the bonding process. Second, the formation of the liquid phase increases the risk of spill out of the Au-Si liquid, which can also damage the devices on the wafer. In this work a solid-state wafer bonding process, which relies on

solid-state diffusion, is proposed as an alternative to eutectic bonding. During solid-state diffusion bonding, temperatures lower than eutectic temperatures can be used (350°C in this study), so the risk of thermal damage to devices is lowered and spill out of molten solder is prevented.

In this project, an amorphous Si layer was applied in Au-Si wafer bonding. A common observation in the Au/crystalline Si (c-Si) system is formation of faceted craters or V-shaped grooves at the Au-c-Si interface. This is a result of anisotropic Au and Si reaction due to Si preferential dissolution. One solution to this problem and subsequent crater formation is to coat the c-Si wafer with an amorphous Si (a-Si) layer. This is also likely to shorten the bonding time. Amorphous Si does not have any preferential dissolution planes and has a lower density than c-Si, so that it should form a liquid Au-Si mixture more rapidly without crater formation.

Another objective of this work was to study and optimize the Au-Si wafer bonding process. In the bonding process there are different parameters of importance, e.g., bonding time, bonding temperature, bonding pressure and bonding atmosphere. In order to obtain bonds with high yield, mechanical strength and coverage, these parameters need to be optimized. In addition, the diffusion mechanisms for Au and Si need to be understood.

Characterization of the formed bonds and microstructures was performed in detail. In order to compare the bonds formed for a-Si and c-Si and during solid-state and eutectic bonding, cross sections of the bonds and, in some cases, bonded areas were evaluated by different characterization methods.

To perform wafer level bonding, full wafers should be bonded with a minimum number of defects and voids. The optimal parameters obtained from bonding of small samples was applied to full wafer bonding with some modifications in the processing parameters based on size differences between full wafers and small samples (e.g., pressure).

Comparison of bonds formed using either a-Si or c-Si and eutectic and solid-state bonding in terms of bond yield, bond shear strength, bond coverage and crater size was another objective of this work.

The most important part of the objectives was to understand the reaction and layer exchange mechanisms. In-situ TEM imaging was performed on Au/a-Si diffusion couples during annealing at different temperatures and the results were used to propose a model for the layer exchange mechanism.

In order to present this work clearly and systemically, this thesis is divided into 8 chapters. Chapter 2 provides a literature review on the available research works, including an introduction to MEMS and device packaging and an entire view of different bonding techniques and their requirements in terms of surface flatness, smoothness and bonding temperature. It also focuses on the basic principles of Au-Si eutectic bonding and previous research already available in this field. Different key parameters and their effect on bond uniformity, bond yield and strength are also discussed.

Experimental methods for the work performed in the thesis are presented in Chapter 3. Details of the preparation of silicon substrates, the bonding process, shear testing and different characterization methods are explained.

Chapter 4 presents annealing results for Au/a-Si and Au/c-Si diffusion couples and diffusion calculations.

In Chapter 5, bonding of small samples using eutectic and solid state method is discussed. Bond yield and shear test results are presented as well. The results obtained from scanning electron microscopy (SEM), energy dispersive X-ray spectroscopy (EDX), transmission electron microscopy (TEM), Auger electron spectroscopy (AES), X-ray diffraction (XRD) and scanning acoustic microscopy (SAM) of bonded areas are also presented and discussed in terms of bond quality.

Chapter 6 presents the application of small sample bonding parameters to full wafer bonding and the results of that work.

Chapter 7 presents the results of in-situ TEM experiments and a proposed model to explain the observed layer exchange mechanism in the Au/a-Si system.

In the final chapter (Chapter 8), the main conclusions, the significance of this work and some recommendations for future work are summarized.

Chapter 2

Literature Review

Chapter 2 - Literature Review

2.1. Introduction to Micro Electro Mechanical Systems

Micro electro mechanical systems (MEMS) utilize a process technology to create tiny integrated devices or systems that combine mechanical and electrical components. They are fabricated using integrated circuit (IC) batch processing techniques and can range in size from a few micrometers to millimetres. These devices or systems have the ability to sense, control and actuate on the micro scale and generate effects on the macro scale.

MEMS can be found in different systems such as automotive, medical, electronic, communication and defence applications. Current MEMS devices include accelerometers for airbag sensors, inkjet printer heads, computer disk drive read/write heads, projection display chips, blood pressure sensors, optical switches, microvalves, biosensors and many other products that are all manufactured and shipped in high commercial volumes. Some of the applications are listed in Table 2.1 [1].

2.2. MEMS packaging

Most MEMS devices such as accelerometers, pressure sensors and gyroscopes can be easily damaged from dirt, moisture, air, etc. [2][3][4], so the devices should be encapsulated under desired pressures and ambient conditions for these applications [5]. In traditional IC packaging, the overall packaging steps are: (1) wafer dicing, (2) pick-and-place, (3) electrical connections and (4) plastic moulding or housing for the sealing process. Unlike regular ICs, the diversity of MEMS products complicates sealing issues. MEMS packaging processes cannot directly follow the procedures set by the IC packaging industry, due to the possible free-standing physical structures or chemical substances which cannot survive the dicing or pick-and-place steps before the sealing process. It has been suggested that MEMS packaging processes, including the sealing

Table 2.1. Applications for MEMS [1].

Automotive	Electronics	Medical	Communications	Defence
Internal navigation sensors	Disk drive heads	Blood pressure sensor	Fibre-optic network components	Munitions guidance
Air conditioning compressor sensor	Inkjet printer heads	Muscle stimulators & drug delivery systems	RF Relays, switches and filters	Surveillance
Brake force sensors & suspension control accelerometers	Projection screen televisions	Implanted pressure sensors	Projection displays in portable communications devices and instrumentation	Arming systems
Fuel level and Vapour pressure sensors	Earthquake sensors	Prosthetics	Voltage controlled Oscillators (VCOs)	Embedded sensors
"Intelligent" tires	Mass data storage systems	Pacemakers	Tuneable lasers	Aircraft control
Airbag sensors	Avionics pressure sensors	Miniature analytical instruments	Splitters and couplers	Data storage

process, should be considered right from the beginning in the device development plan and packaging schemes should be designed and incorporated into the device fabrication process [6].

Packaging also provides electrical contact between the device and electrical system. In addition, it provides electrical isolation, mechanical and environmental protection and a path for heat removal and spreading [7]. There are different kinds of packages: Metal Packages, Ceramic Packages, Thin-Film Multilayer Packages and Plastic Packages [8].

The packaging cost can be more than 70% of the total expense. Fortunately, most packages use a die level process which reduces the total cost by packaging the device at the wafer level. Wafer bonding technology is necessary for effective wafer level encapsulation of the device wafer [9].

2.3. Wafer bonding

Wafer bonding is a promising technology for manufacturing three-dimensional complex MEMS and packaging. It has been an important process for integrating electronics, photonics and micromechanical devices.

Wafer bonding is divided into two main groups: 1) direct bonding and 2) intermediate layer bonding. These two techniques are further divided into different categories depending on the processing conditions and requirements (Figure 2.1). These techniques have been used in integrated circuits and MEMS for many years. In the following sections, a short description is given about different bonding methods and their requirements regarding wafer cleaning, flatness and bonding procedures [10][11].

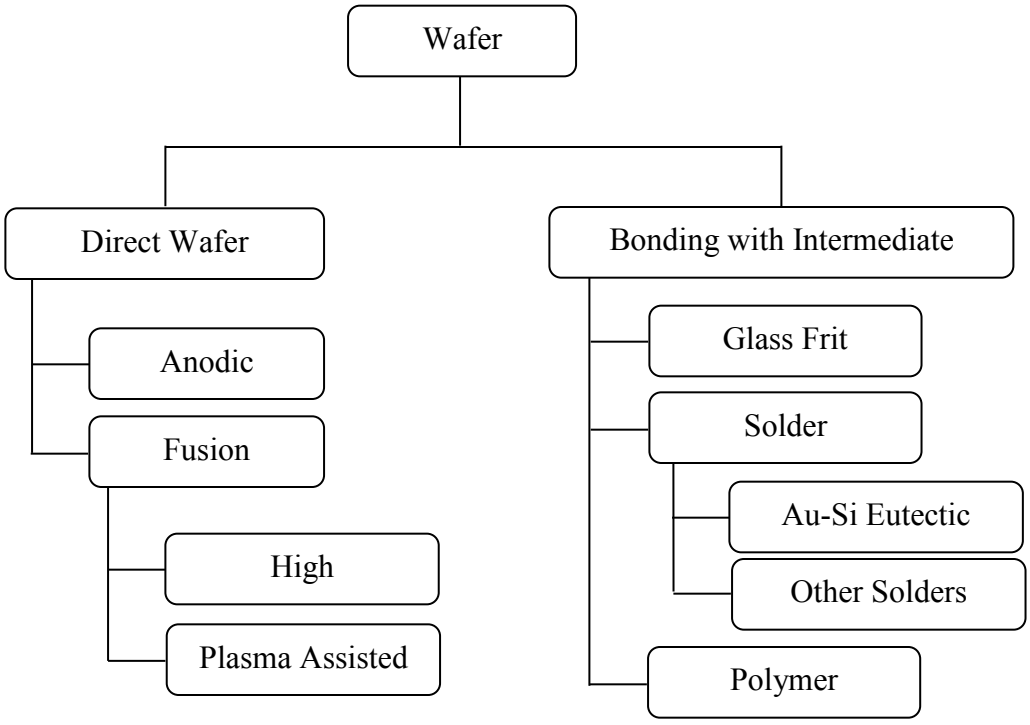


Figure 2.1. Classification of wafer bonding [10].

2.3.1. Bonding requirements and procedure

2.3.1.1. Si wafer cleaning

Cleaning is a very important step in any bonding process and it determines the strength and reliability of the bond. The cleaning process should be compatible with wafer bonding and it should not degrade the bonding surface [10]. Native oxide on the surface traps metallic and organic contamination. Standard Clean 1 (SC1), which is a mixture of ammonium hydroxide and hydrogen peroxide used for removing organic contamination followed by a basic oxide etch (BOE) which is a selective etch to remove SiO_2, is often used in the semiconductor industry. The purpose of SC1 is to remove organic contamination and particles from wafers. SC1 will rapidly attack most organic materials and some metals. SC1 should be used as a final polishing clean to remove the last residues or to clean new wafers before starting processing [12]. BOE removes oxides from areas of interest; it etches Si dioxide and other Si oxides and reduces surface metals [13].

2.3.1.2. The bonding procedure

It is important to bond the wafers immediately after cleaning to minimize the contamination of wafer surfaces. Bonding is usually carried out in a clean room to minimize the amount of particles and contamination involved in the procedure. However, high amounts of hydrocarbons, organic compounds and other contaminants may readily adsorb onto the surface from the atmosphere of the clean room.

Bonding can be done either manually or by making use of commercial bonders, but it is preferable to use a bonder, especially in cases where wafer alignment is necessary. Different atmospheres can be used for bonding such as oxygen, nitrogen, argon or vacuum [10].

After cleaning the two wafers, they are put together such that the mirror polished sides face each other. Removable spacers are used to separate the wafers from each other in the bonder. The upper wafer is dropped on the lower wafer by removing the spacers. A thin air cushion is usually developed if bonding is performed in air. By pressing the wafers gently together, in order to squeeze out the air, bonding will be started. The bonding area will spread over the entire surface spontaneously within a few seconds [14].

2.3.2. Direct bonding

Direct wafer bonding is a method of joining Si wafers without using any intermediate bonding medium [15]. Direct wafer bonding works according to two basic conditions. First, the two surfaces to be bonded should be flat enough to have sufficient contact. Second, appropriate processing temperatures are required for bonding [10].

Bonding usually takes place in two steps. First, the wafers are bonded through microscopically short range surface forces at room temperature. For this reason, the bonding process starts with wafer hydration (soaking in an H_2O_2-H_2SO_4 mixture, diluted H_2SO_4, boiling nitric acid or oxygen plasma) in order to form a hydrophilic top layer consisting of O-H groups. The second step is annealing at high temperatures (700-1100°C) to form bonds at the interface. A schematic image of this technique is shown in Figure 2.2.

The advantage of this method is high strength bond formation without using any intermediate bonding layer or pressure. This method has found application in advanced micro and optoelectronic devices and MEMS [15]. The major drawback of this method is that its application is limited by high temperature processing and void problems. Conventional direct wafer bonding is conducted at high temperatures in order to get sufficient bond strength, but many problems arise at these temperatures such as gas formation, alignment difficulty and damage of sensitive devices located on the wafer. These drawbacks decrease the applicability of this method for wafer

bonding and increase the need for development of other lower temperature techniques [16]. However, special techniques such as plasma surface treatment can be used in order to conduct bonding at room temperature [6].

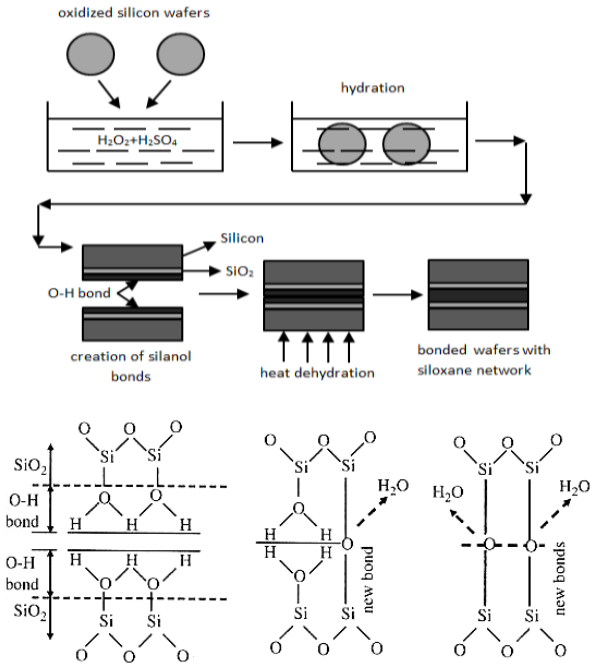


Figure 2.2. Si direct bonding by hydration [17].

Direct wafer bonding can be classified as either anodic bonding or fusion bonding. There are 3 methods of fusion bonding, i.e., 1) high temperature hydrophilic bonding, 2) plasma assisted bonding and 3) high temperature hydrophobic bonding.

2.3.2.1. Anodic bonding

While Si direct bonding needs high temperatures and chemical pre-treatment of the Si surface to get high strength bonds, strong bonds can be produced by anodic bonding using a thin glass layer at temperatures ranging from 300-400°C and by using a special low melting point glass even at room temperature [18]. Pyrex 7740 and Schott 8330, containing a high concentration of alkali ions, are the most common glasses used for anodic bonding. The coefficient of thermal expansion (CTE) of the processed glass

needs to be similar to the bonding partner to maintain low stress within the bonded pair [19].

In this method a high voltage (>1000V) is used to generate a high electrostatic force to pull the bonding surfaces together [20]. A negative voltage at the glass plate pulls the sodium ions to the cathode and creates a negatively charged region across the interface. Movement of positive ions leaves oxygen at the interface between the glass and Si. An electrochemical reaction occurs and oxygen bonds are formed to the Si at the interface by creating strong SiO_2 bonds [19]. The thickness of the glass layer is a few microns and can be deposited by sputtering, spin-on glass or vapor deposition methods onto Si wafers. Anodic bonding, by sputtered glass layers, has the disadvantage of very low deposition rates and different compositions compared with the glass target [20]. Figure 2.3 shows a schematic of the anodic bonding process.

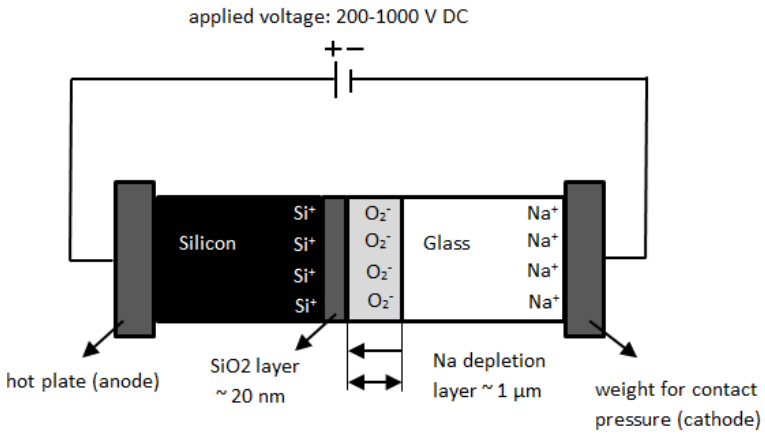


Figure 2.3. Schematic image of Si to glass bonding process [17].

If there are free-standing, conductive micromechanical structures on any of the wafers, care must be exercised as the high voltage can move the micromechanical structure and damage may occur. In order to solve this problem, a thin metal film patterned on the glass cap can be formed to provide shielding [6]. Glass-to-glass bonding has found useful applications in bio-MEMS, microfluidics and display devices [21].

2.3.2.2. Fusion bonding

Fusion bonding is a special kind of direct bonding in which a chemical bond forms between two materials at their hetero-interface without any intermediate layer. The two joining surfaces should be oxide-free and they are annealed to form a bond. The process requires temperatures between 700-1100°C.

Direct bonding requires high demands for surface flatness and cleanliness. The contamination which affects bond quality can be classified as 1) particles, 2) organic contamination such as hydrocarbons and 3) ionic contamination (usually metal ions from tweezers or glass containers). Particles usually act as spacers and pose the most obvious problem in wafer bonding. Organic contamination usually does not create an unbonded area as organics are present on the surface in the form of a film or as single molecules. This contamination can limit adhesion and may lead to the nucleation of interface bubbles during annealing. Metallic ions do not inhibit bonding, but they can affect the electronic properties of the semiconductor materials [14].

2.3.2.2.1. High temperature hydrophilic bonding

Si wafers can easily oxidize if exposed to the ambient atmosphere. Usually the thickness of the native oxide is 1-2 nm. This oxide layer terminates the Si wafer surface by Si-OH groups called silanol groups. Polarization of the hydroxyl group and the amount of silanol groups can define the hydrophilicity of the surface. For high temperature hydrophilic bonding, the wafers should have an oxide layer (the native oxide, thermally grown oxide or deposited oxide) [10].

The reaction starts as the contact is established between the two surfaces, where water molecules form a bridge between the two surfaces. During the following annealing process, water molecules will diffuse out from the interface and dissolve into the surroundings or react with the Si surface forming more silanol groups on the surface. Continued heating will result in bond formation between silanol groups by

completely removing water molecules. At the end, silanol groups react to form Si-O-Si bonds by removing water molecules [19].

$$Si\text{-}OH + Si\text{-}OH \rightarrow Si\text{-}O\text{-}Si + H_2O \quad (2.1)$$

Water molecules can diffuse into the Si and react with it forming oxide and releasing hydrogen.

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \quad (2.2)$$

The remaining hydrogen can lead to formation of voids and trapped gas. Having an oxide layer >50 nm thick can solve this problem. The oxide has a high solubility for hydrogen. The amount of oxide required depends on the amount of water present at the surface, so that all the hydrogen can be dissolved [19].

2.3.2.2.2. Plasma assisted bonding

Low temperature bonding processes are required for wafers which contain temperature sensitive materials or components, or for materials with different CTEs. A low temperature hydrophilic process is possible using plasma activation. In these methods a short plasma treatment is required to activate the surface prior to bonding. Many processes have been reported for plasma activation but the most common plasma gases are argon, nitrogen and oxygen. After the plasma treatment, strong bonding can be achieved at low temperatures (<400°C); even room temperature bonding processes have been reported [22][23][24][25].

2.3.2.2.3. High temperature hydrophobic bonding

The oxide layer is not required for some applications. The Si wafer is usually dipped in hydrofluoric acid or ammonium fluoride to remove the oxide layer. The solution will etch away the oxide layer from the surface and the bare Si will be terminated by hydrogen. Sometimes fluoride termination is also detected. A hydrophobic Si surface can be contaminated quickly by hydrocarbons as compared with a hydrophilic surface.

Therefore, after removing the oxide layer, wafers should be bonded quickly or they should be stored in vacuum. After intimate contact is established, HF molecules will form bridges between the two surfaces. Annealing from 150°C to 700°C rearranges the bonds and then hydrogen desorbs from the surfaces resulting in Si-Si bonding [19].

$$Si\text{-}H + Si\text{-}H \rightarrow Si\text{-}Si + H_2 \quad (2.3)$$

Void formation as a result of hydrogen presence at the bond interface, is the main problem in this type of bonding.

2.3.3. Intermediate layer bonding

Wafer bonding can be done using an intermediate layer between wafers. These processes find application where lower bonding temperatures or stronger bond interfaces are required, but cannot be obtained from direct bonding processes. In addition, during these processes the intermediate layer may reflow and fill the gaps between the two bonding surfaces. As such, the requirement of fine surface roughness in the direct bonding process is not as stringent for wafer bonding with intermediate layers [6]. Bonding with intermediate layers includes glass frit bonding, polymer bonding and eutectic bonding [10].

2.3.3.1. Glass frit bonding

Glass frit bonding employs low melting point glass as an intermediate layer. Of the various wafer bonding techniques, glass frit bonding offers advantages such as superior hermeticity, less stringency on the roughness required by the surfaces and thermal expansion matching of the materials being joined.

Glass frit bonding is carried out in three main steps: glass paste deposition by screen printing, conditioning of the paste and actual bonding [26].

In the first step, a sealing glass paste is screen printed into the desired shape [27]. The main advantage is the possibility of material deposition on the cap wafer with holes or high steps. No additional effort, like photolithography, is necessary for structuring. The low melting point glass has to be milled into a powder with a grain size of less than 15 µm. Mixing this powder with an organic binder forms the printable paste. By adding inorganic fillers, the properties of the melted glass paste can be adjusted (e.g., the CTE can be modified to that of Si). This layer is dried using an infrared oven and heated to an intermediate temperature, where the glass does not fully melt, in order to allow outgassing of the organic additives. This process is called “glazing”, which can be done either in a belt or box furnace under atmospheric conditions. Then the pre-glazed wafer is placed in a wafer bonder and bonded to a cap wafer in a temperature-time-pressure cycle under the desired vacuum in a process called “frit bonding” to produce a hermetically sealed assembly. Figure 2.4 shows the thermal conditioning during glass-frit bonding. The quality of the resultant seal depends on both the seal glass material used and the process variables employed in both glazing and frit bonding [26].

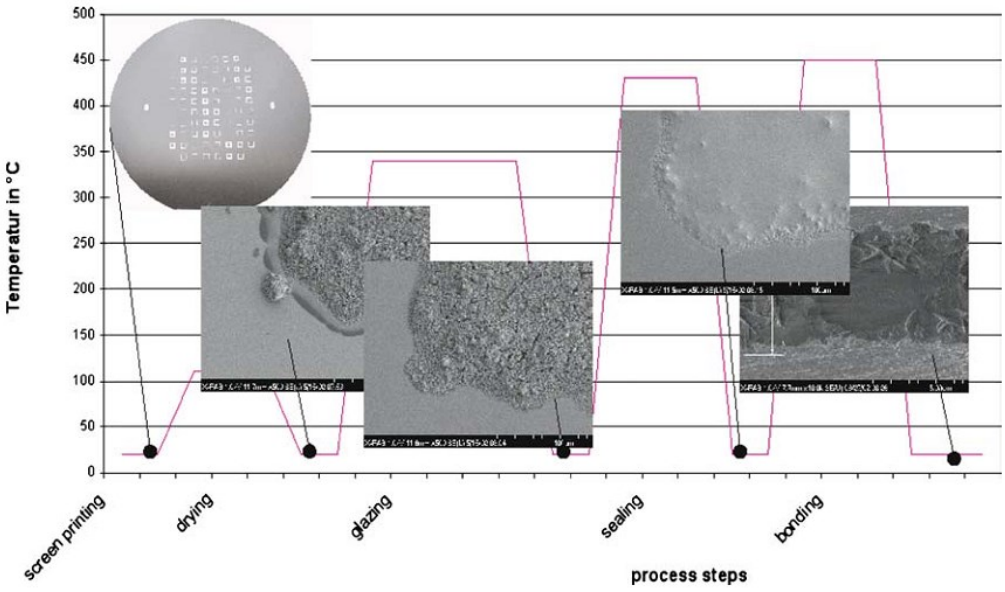


Figure 2.4. Thermal conditioning during glass-frit bonding [26].

2.3.3.2. Polymer bonding

In this technique, several different polymers are used as an intermediate material for bonding, such as polyamides, epoxies, thermoplastic adhesives and photoresists.

Some of the advantages of this technique are:

1. The bonding temperature can be lower than 100°C (suitable for complementary metal-oxide-semiconductor (CMOS) applications).
2. Different wafer materials can be joined [28].
3. Insensitivity to the topology of the wafer surfaces [29].
4. High bonding strengths are achievable.
5. Stress reduction as a result of the elastic properties of some polymers.
6. Low cost.
7. Compatibility of most polymers with clean room standard processing.

Adhesive bonding also has some disadvantages:

1. Incapability of achieving hermetic seal as a result of bonding with polymers.
2. Limited long-term stability of many polymer materials.

The process steps are as follows:

1. Wafers are cleaned using H_2O_2 and H_2SO_4 in the ratio of 1:2.5 and dried afterwards.
2. An adhesion promoter is supplied to both wafers.
3. The polymer is spun onto the wafers.
4. The polymer is pre-cured in order to evaporate the solvents.
5. Pressure is applied in a vacuum environment to join the wafers.
6. The polymer is cured with temperature ramping while applying pressure.

Polymer adhesive bonding is specialized for MEMS or electronic component production [30].

2.3.3.3. Eutectic bonding

Eutectic bonding is a wafer bonding technique with an intermediate metal layer. Typically for wafer bonding, alloys with low melting points are used, containing Sn, Ag, Al and Au [31]. Many different types of eutectic alloys exist with a wide variety of melting temperature ranges. The main eutectic systems are listed in Table 2.2 [32]. In eutectic bonding, the metal alloy works as a glue for bonding the two surfaces [31]. The solder system is selected based on optimization of properties such as wettability, mechanical properties, melting point, fatigue life, CTE and thermal and corrosion resistance [33].

In eutectic bonding there is less concern about substrate roughness and flatness as compared with direct bonding. However, in fusion bonding a high bonding temperature and low roughness of the bonded surfaces is required to assemble small structures. Anodic bonding has the potential to bond surfaces at low temperature but it requires high electric fields, which can be detrimental to electrostatic MEMS. Other advantages of eutectic bonding methods are better out-gassing and hermeticity compared to bonding with organic intermediate layers [34].

There are two different kinds of solders: soft solders and hard solders. Soft solders are usually used in SMT (surface-mount technology) and flip-chip technology to make terminal materials. They have low melting temperatures, e.g., Sn-In alloys, but they show low yield strengths which results in low creep resistance. The drawback of using soft solders is that the alignment of the devices cannot be maintained over time [35]. Their melting temperature is below 200°C. Usually the stress concentration is in the bonding layer as it is softer than the die or substrate. Solder yield strengths are low, usually less than 10 MPa [36].

Table 2.2. Main process characteristics for eutectic wafer bonding [32].

Parameter	**Eutectic wafer bonding**			
	Eutectic Elements	Process Temperature	Eutectic Temperature	Eutectic Composition
Process Parameters	Au-Sn	~300°C	~280°C	(70% at Au- 30% at Sn)
	Au-Si	~380°C	~363°C	(81% at Au-19% at Si)
	Au-Ge	~380°C	~361°C	(72% at Au- 28% at Ge)
	Al-Ge	~440°C	~424°C	(70% at Al- 30% at Ge)
	Au-In	~510°C	~495°C	(66% at Au- 34% at In)
Temperature Variation	+(10°C-20°C) from eutectic point			
Surface Quality	Low			
Contact Force	Low			
Atmosphere	Inert or reducing			
Liquid Phase	Yes			

On the other hand, hard solders such as Au-rich Au-Sn, Au-Si and Au-Ge alloys have higher melting temperatures and yield strengths [36][35][37]. Their melting temperature range is between 270 and 363°C [38]. Au-Sn, Au-Ge and Au-Si systems are commonly considered as hard solders. They have high thermal conductivity and long term reliability [36][35]. Due to their high strength, they are free of thermal fatigue which results in elastic rather than plastic deformation. Using hard solders produces high stress on the die because of the lack of plastic deformation, but if the bonding layer is free of voids, the high stress produced is lower than the die strength so they should not crack easily [39]. The other advantages of hard solders over soft ones are high corrosion resistance and the possibility for a fluxless process for optoelectronic packaging [40].

2.4. Au-Sn eutectic bonding

Flip chip bonding technology has used the Au-Sn eutectic system for many applications such as microwave devices and optoelectronic packaging, because it has good thermal conductivity, high yield strength and good wetting behavior [44,45,46]. Its high thermal conductivity (about 57 W/m°C) makes it useful for bonding high power devices which need good heat dissipation. The other advantages of using this kind of solder are the ability to solder without flux, good mechanical and electrical properties, formation of a hermetic seal and low rate of intermetallic growth when used over Ni, Pd or Pt. The disadvantage of this solder is that it needs extreme accuracy and precise control to maintain the desired eutectic composition and the formation of different intermetallics which is not desirable in terms of mechanical properties [37].

2.5. Au-Ge eutectic system

The advantages of the Au-28Ge (at%) eutectic alloy system are high thermal and electrical conductivity, good mechanical properties, and good corrosion resistance. In addition, the Au-Ge phase diagram is simple eutectic type without formation of any intermetallics. The applications can be listed as high-temperature lead free solder materials for highly loaded components such as high-power MEMS, space technology and corrosion-resistant solders for components exposed to aggressive media such as sensors in corrosive atmospheres and biomedical devices. The drawback of this system is that joint reliability highly depends on the phases forming at the interface between Au-Ge base alloys and different substrates; e.g. Si, Cu and Ni. As a result, the Au-Si system was chosen for study in this thesis for its simple eutectic system.

2.6. Au-Si eutectic bonding

This section presents a review of Au-Si eutectic bonding. In addition to the basic principles of Au-Si eutectic bonding and the specific characteristics which make

eutectic bonding worthy for microsystem technology, different constraints which have significant effects on bond strength and bond yield are discussed.

2.6.1. Principles of Au-Si eutectic bonding

Au-Si eutectic bonding has been widely used in microfabrication. The bonds have high bond strength, good stability at higher bonding temperature (363°C) against oxidation, which makes fluxless bonding possible, excellent hermeticity allowing for vacuum wafer-level packaging and good tolerance to surface topography as a result of the formation of a liquid phase [41][42].

The main drawback of the Au-Si system is the difficulty to obtain complete bonding over large areas and the presence of native oxide which can prevent bonding from taking place [43]. Bonding stress is also a problem for Au-Si eutectic bonding, because the Si CTE is not the same as for Au. When the bond cools, thermal stresses are generated [44].

The bonding temperature for the eutectic bonding procedure depends on the material used. Bonding is possible at a specific wt% and temperature. For the Au-Si eutectic, bonding is possible at 363˚C at 2.85 wt% Si based on the Au-Si phase diagram (Figure 2.5). The eutectic temperature of the Au-Si eutectic system is much less than the melting points of Au and Si, which are 1063˚C and 1412˚C, respectively [10].

During the bonding process, diffusion of Au and Si will happen as a result of atomic contact between Au and Si and elevated temperatures. Mechanical pressure is applied during bonding to keep the wafers in contact. A liquid phase will form when the eutectic composition and eutectic temperature are reached [34].

Decreasing the temperature or changes in the concentration ratio leads to solidification of the eutectic mixture. Solidification results in the formation of numerous protruding small Si islands from a continuous polycrystalline Au film [34][45].

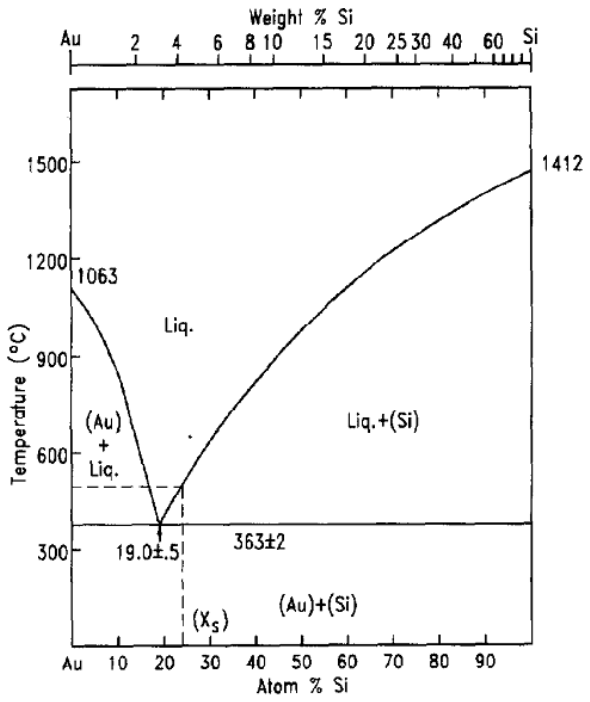


Figure 2.5. Au-Si phase diagram [46].

2.6.2. Amorphous Si (a-Si) versus crystalline Si (c-Si)

Crystalline Si has the same structure as diamond; thus it can be described by a face centered cubic lattice. In c-Si, each Si atom is covalently bonded to four other Si atoms with covalent bonds towards the four corners of a regular tetrahedron. This basic structure extends in all directions in 3D forming a giant covalent structure.

An amorphous solid is one in which there is no long-range order in the position of the atoms. Determination of the structure of a crystal is made easy because of its characteristic long range order, symmetry and periodicity. But lack of this long-range order and periodicity in amorphous materials makes it difficult, if not impossible, to determine the exact arrangement of the regular tetrahedral [47].

One of the problems with a c-Si/Au bonding system is the formation of large craters (Figure 2.6) at the bond interface, which is due to the anisotropic nature of c-Si. The reaction rate of c-Si highly depends on the crystalline orientation of the Si wafer. The

dissolution of Si into the Au layer is preferential along particular planes which have the highest surface energy. In c-Si, (111) planes have the lowest surface energy so they have the highest resistance to dissolution in Au. The V-shape grooves are formed as a result of this preferential dissolution.

Jing et al [48] observed (Figure 2.6) that the thickness of the bond interface of the non-crater regions is nearly the same as that of the deposited metal film, and the bond interface of these regions is filled with Si precipitates or Au. The Au/c-Si reaction is non-uniform, leading to an Au/Si bond interface consisting of crater and non-crater regions. In order to explain the non-uniformity of the Au/Si reaction, a sample from the bonded wafer pair was analyzed by transmission electron microscopy (TEM).

Figure 2.7 shows cross-sectional TEM image of the Au/c-Si bonded structure. A very thin native oxide layer (about 3 nm in thickness), can be seen at the bond interface of the non-crater regions. Even though the bare Si wafer used in the Au/Si bonding structure was dipped in HF to remove the native oxide prior to bonding, it was rinsed in de-ionised water and exposed to air for several minutes before bonding, and it is possible that oxidation occurred during this time. It has been reported by Hiraki et al [49] that the presence of an oxide layer between the Si surface and Au film tends to prevent significant Si diffusion into the Au layer.

The strong Si dissolution at the crater regions can be the result of localized disruption of the native oxide layer and subsequent direct contact between Si and Au. While the mechanism for local disruption of native oxide is currently unknown, from the above analysis, it can be concluded that the non-uniformity of the Au/Si reaction is due to the native oxide on the bare Si surface, which results in the poor quality of the Au/Si bond.

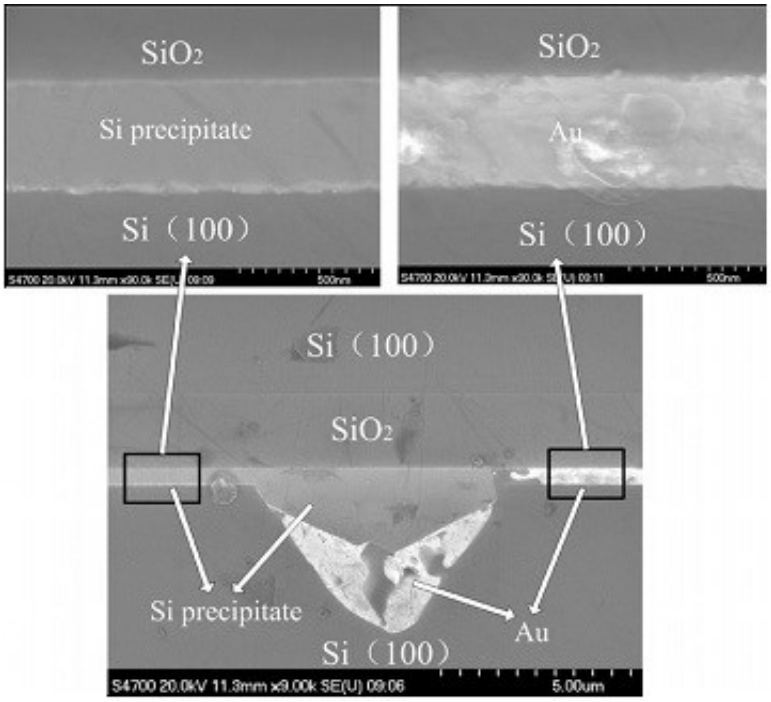


Figure 2.6. Cross-sectional SEM image of an Au/c-Si bond structure. The bond interface consists of crater and non-crater regions and these regions are filled with Si precipitates or Au [48].

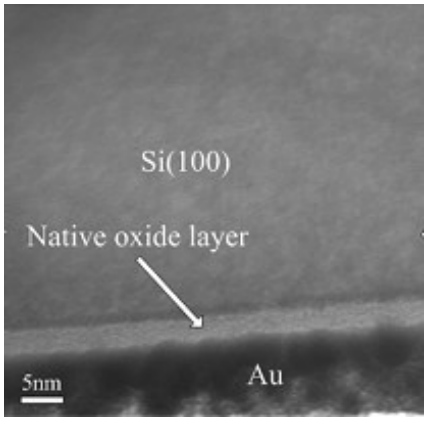


Figure 2.7. Cross-sectional TEM image of the Au/Si bonding structure. A thin native oxide is present at the bond interface of the non-crater regions [48].

Considering the above analyses, a model was proposed to describe the formation process of the interface morphology, as shown in Figure 2.8. During bonding, due to localized disruption of the native oxide layer, exposed underlying Si will become in

contact with Au, leading to its dissolution into Au and rapid diffusion along the grain boundaries of the Au film. As Si concentration in the Au layer exceeds the solubility limit, Si nuclei will form at preferential sites [49].

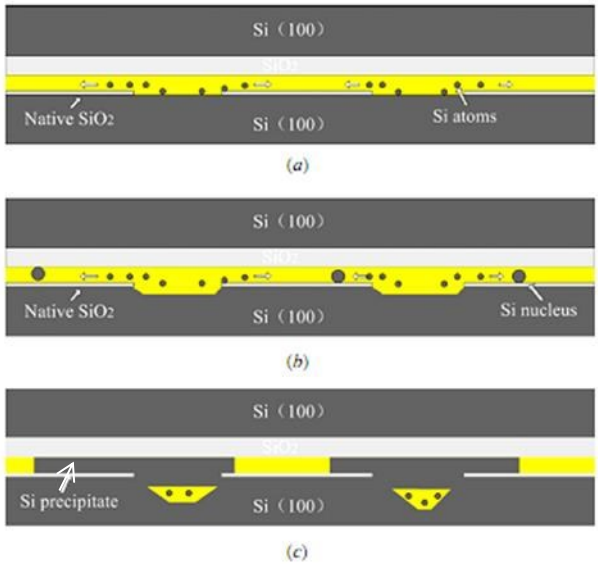


Figure 2.8. Schematic illustration showing the formation mechanism at the Au/Si bond interface. a) Si dissolution and diffusion; b) formation of Si nuclei; c) growth of Si precipitates and refilling of Au [48].

Continuous Si dissolution from the crater results in lateral growth of the Si nuclei and their joining together, leading to a continuous Si precipitate. Simultaneously, Au is repelled from the growing Si precipitate and moves through the disrupted spots in the native oxide layer to refill the crater at the Si substrate left behind by Si diffusion, ultimately segregating to the bottom of the crater. As a consequence of this process, the interface morphology shown in Figure 2.6 is formed [48].

One of the solutions to the crater problem is coating the Si (100) wafer with a layer of a-Si. Crater formation in a-Si/Au is very limited. The reason is due to the rapid formation of a uniform Au-Si liquid alloy, due to the low density of the a-Si structure. After rapid consumption of a-Si to form a liquid eutectic alloy, c-Si starts to react with the liquid alloy at a much slower reaction rate than in the c-Si/Au case, which prevents the formation of large craters and air voids [50].

When using an a-Si layer, during bonding, the Si diffuses into the Au and forms a mixture of Au and Si. Annealing at 400°C results in the decomposition of the mixture and the released Si will nucleate at preferential sites. As Si dissolution from the a-Si layer proceeds, the Si nuclei will grow radially and join together, leading to large Si grains across the bond interface. Accompanying the diffusion of the Si atoms into the original Au layer, the Au is repelled from the growing Si grains and moves to refill the locations left by Si out diffusion resulting in Au enrichment at the crystalline growth front. Au acts as a catalyst in the transformation of the a-Si to c-Si. The process continues and, in the end, large Si grains will form across the bond interface, whereas a mixed c-Si/Au layer will develop at the location of the original a-Si layer, which is consistent with the interfacial morphology shown in Figure 2.9 [51].

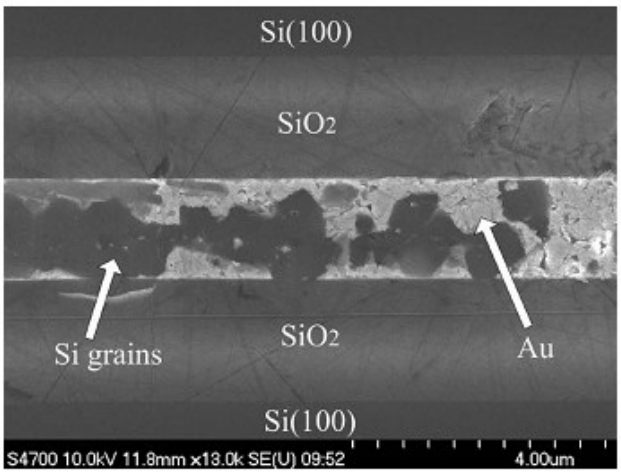


Figure 2.9. Cross-sectional SEM image of Au/a-Si bond [48].

2.6.3. Metastable phases

A large number of metastable intermediate phases have been produced in binary alloy systems through the application of the comparatively new liquisol-quenching or splat-cooling techniques (106 to 108°C/s) [52][53].

In the quenching technique, the Au-Si alloy melt, with a composition near the eutectic value, is quenched to liquid nitrogen temperatures to form an amorphous phase [54]. This phase crystallizes on warming to room temperature. In addition, two crystalline non-equilibrium intermediate phases have been produced in alloys containing 1 to 5 wt% Si and 5 to 12 wt% Si, respectively. These two phases, designated β and γ have been indexed on the basis of large face-centred cubic (FCC) unit cells containing a maximum of 32 and 500 atoms and with lattice parameters a_β = 0.7844 nm and a_γ = 1.9503 nm, respectively. The Au-rich phase with the smaller unit cell has been provisionally assigned the formula Au_7Si [55]. This conclusion has been questioned because of the reported formation of a metastable phase with possibly a γ-brass type structure with 52 atoms per unit cell and a= 0.960 nm after liquisol-quenching of Au-Si alloys containing 4 wt% Si [56] . The situation has been further complicated by the reported occurrence of a metastable phase with the formula Au_5Si by Dixmier and Guinier [57].

There have been further reports of metastable Au-Si phases, one by Anderson et al. [58] for a possible Au_3Si phase, with an orthorhombic structure with a = 0.782nm, b = 0.555 nm and c = 1.116 nm, after quenching alloy melts into iced water. The other is by Krutenat et al. [59] with the formation of a non-equilibrium phase, with a γ-brass-type structure and a = 0.960 nm, after sputter deposition of a Au-5 wt% Si alloy followed by annealing [53].

2.6.4. Metal induced crystallization

Recently, special attention has been given to low temperature polycrystalline Si (poly-Si), aiming at the use of this material in large area devices, such as thin film transistors and solar cells, where it is crucial to use low cost substrates such as glass [60][61]. Crystallized a-Si normally presents better electrical properties than as deposited poly-Si. So, lowering the crystallization temperature of a-Si is an important point concerning the application of this material in devices. One of the most implemented techniques to obtain poly-Si from a-Si is by solid phase crystallization [62]. However, in this process

the crystallization temperature is too high and the time required for full crystallization is too long. Another way of obtaining poly-Si is using excimer laser annealing [63], which produces good quality films on glass substrates. It has some important disadvantages; however, such as high cost and low uniformity over large area substrates. Some metals when deposited on a-Si can lower the crystallization temperature due to the reaction that occurs at the interlayer by diffusion in a process known as metal induced crystallization (MIC) [64]. This enhancement of crystallization occurs due to interaction of the free electrons from the metal with the Si covalent bonds near the growing front, leading to a metal silicide, a eutectic alloy, the migration of the metal silicide or some combination of these that reduces the crystallization temperature [65].

The metals used can be classified into two groups: silicide forming metals, such as Ni and Pd, and elemental metals that do not form silicides, such as Al and Au. Thin Au layers are known to react with Si at temperatures below 200°C, starting the crystallization process. There are reports that even at room temperature this reaction can take place, but needs a long time period [66].

In spite of the lower crystallization temperature, there is the potential for metal contamination in crystallized Si when using MIC. Most metals are deep dopants or act as recombination centers [67]. This fact is dependent on metal diffusion and solubility and is related to the metal thickness deposited on a-Si and the annealing temperature. So, it is important to find a compromise between the metal thickness and the electrical properties.

2.6.5. Influence of metal thickness

After annealing at 500°C for 30 h with 0.5 nm of Au, the Si layer still remains amorphous. At this temperature the metal thickness is not sufficient to induce the crystallization process. Longer annealing times (t_A) would likely lead to crystallization. For a metal thickness of 20 Å, ellipsometry data suggests the presence of a significant

crystalline phase. After annealing for 30 h, the sample generates a crystalline volume fraction (f) value of 0.57. A further increase in the metal thickness up to 50 Å leads to enhancement in f. Indeed, spectroscopic ellipsometry (SE) data shows that a fraction of 0.809 is obtained for a sample annealed for 30 h and a significant doping effect caused by Au incorporation was detected. This doping effect is even more pronounced when using 100 Å of Au. SE data shows that f rises to 0.895, confirming that an increase in metal thickness enhances the crystalline degree of annealed samples but with an increase in the doping effect induced by the metal. This strong metal thickness dependence suggests that the crystallization process occurs through the formation of an Au–Si intermixed layer responsible for c-Si nucleation. After that, c-Si grows by diffusion of Si atoms from the intermixed layer. Even if the intermixed phases are formed at relatively low temperature (around 180°C) [68], their formation depends strongly on the metal/Si ratio since in the Au–Si system the formed phase is Au-rich. So, in the formation of intermixed phases the Au is consumed and its thickness is the limiting factor. A thicker Au layer will form a thicker intermixed layer that enhances Si diffusion; however, doping effects are enhanced as well.

2.6.5.2. Influence of annealing time

The crystallization process is explained by the formation of an intermixed layer and diffusion of the Si from that nucleation site. An increase in the annealing time is also responsible for the enhancement of Si diffusion and an increase in the crystallinity degree achieved.

2.6.5.3. Influence of annealing temperature

The annealing temperature (T_A) also plays an important role when crystallizing a-Si. The Si diffusion responsible for crystallization is enhanced with increasing temperature as expected for a diffusion process and this explains the increase in the crystallinity with

increasing T_A. Crystallization occurs preferentially along the {111} planes since these are the ones that present the lowest formation energy [69].

The formation of a localized liquid phase occurred for samples with Au during annealing, since the MIC process was performed at 500°C. This liquid phase is formed where the Au is in contact with the Si and may be responsible for enhancement of the diffusion process, since it allows for better homogeneity of the Au-Si mixture [70]. The formed liquid reduces the activation barrier of the thermodynamically favourable a-Si to c-Si transition. The mechanism proposed for this behaviour is based on constitutional supercooling (CS), due to the lower melting point of a-Si when compared with c-Si, which leads to crystalline Si precipitation [71].

The model for crystallization also suggests that after the process is complete, the metal will be segregated to the grain boundaries or to the bottom/top of the crystallized film. Since Au diffuses in Si preferentially through interstitial sites [72], this may also lead to lower effective doping by metal atoms (Au in this case) as they will not occupy many substitutional electronically active sites.

Another phenomenon which has been observed in the eutectic systems of Si and Ge with metals such as Al, Au, and Ag is layer exchange [73][74][75]. This phenomenon has been extensively studied, although its mechanism remains unclear. Nast et al [76] investigated layer exchange for the a-Si/Al system, where layer exchange takes place during isothermal annealing at temperatures significantly below the eutectic temperature of 577°C and results in the growth of large grained poly-Si films [77][78]. It was shown in an earlier study that Si nuclei are formed at the a-Si/Al interface inside the metal layer; they grow into the Al layer while incorporating the Si atoms diffused from the a-Si film through the Al layer toward the growing Si grains. Once the size of the Si grains reaches the thickness of the Al layer, they start to grow laterally since they are constrained by the substrate and the a-Si/Al interface. During the process of poly-Si growth, the Al layer is gradually displaced. Due to the high diffusivity of Si within polycrystalline Al and the supply of Si atoms from the a-Si film, a continuous poly-Si

film is typically formed in less than 1 h at temperatures of about 450°C when adjacent grains impinge on one another [79]. The parameters, which seem to have a major influence on the overall process, are 1) the annealing time, 2) the layer thickness ratio, 3) the temperature, 4) the layer sequence, 5) the Al grain structure and 6) the Al/a-Si interface [80].

2.6.6. Au diffusion in Si

While the values for diffusion coefficients lie within a very narrow range for gases (10^{-1}-1 cm^2/s) and liquids (10^{-6}-10^{-4} cm^2/s), diffusivities in solids are characterized by a much wider range of values. For example, diffusion coefficients in c-Si lie in the range of 10^{-5}-10^{-20} cm^2/s. In fact, diffusion can occur through different mechanisms determined by the particular role that intrinsic defects play in them. Diffusion in c-Si and its technological relevance can be classified as follows:

1) Most transition metals (e.g., Fe, Co, Ni and Cu) behave as fast diffusers that diffuse by jumping from one interstitial site to another. Their diffusion coefficients are very high (~10^{-5}-$10^{-7}cm^2/s$ in the temperature range of 500-1400°C) [81] and are characterized by a low activation energy (< 1 eV).
2) Self-atoms and substitutional solutes diffuse by indirect mechanisms where self-interstitials and vacancies act as diffusion vehicles. As a result of low thermal equilibrium concentration (<$10^{16}/cm^3$) and high formation energies of intrinsic defects, the diffusion coefficients of these solutes are quite low (10^{-9}-10^{-14} cm^2/s in the temperature range of 500-1400°C)[81] and are characterized by very high activation energies (3-4 eV).
3) Some of the transition metals (Zn, Pt and Au) diffuse at rates intermediate between interstitial and substitutional solutes (activation energy of ~2 eV and diffusion coefficient of ~10^{-6}-10^{-12} cm^2/s for the temperature range of 500-1400 °C)[81][82].

The features for the diffusion of Au in Si have been established: Au atoms may occupy both substitutional (Au_s) and interstitial (Au_i) sites. The solubility of Au_s is larger compared to Au_i, whereas the diffusivity of Au_i is much higher than that for Au_s and exceeds the diffusivity of Group-III or Group-V elements in Si by several orders of magnitude. There are two different opinions about the interchange of Au atoms between substitutional and interstitial sites occurring during the diffusion of Au in Si. The first mechanism is the Frank-Turnbull mechanism [83].

$$V + Au_i \rightleftarrows Au_s \qquad \text{(V: vacancy)} \quad (2.4)$$

And the second is the "kick-out" mechanism,

$$Au_i \rightleftarrows Au_s + I \qquad \text{(I: Si self-interstitial)} \quad (2.5)$$

A key argument in favour of the kick-out model is that the Au_s concentration in the middle of Au-diffused Si wafers increases proportionally with the square root of the time for diffusion. The Frank-Turnbull model is unable to explain this observation; however, it has been accounted for in the kick-out model [84].

In a-Si, the understanding of diffusion is not very clear. Modelling the structure of a-Si [85] demonstrated a long-range order which is suppressed by bond bending, while local order is defined by directional covalent bonding. This indicates that the local order in a-Si and c-Si is very similar, but there are significant differences as a result of the high density of intrinsic defects inherent to the a-Si. This high defect density (e.g., up to 2 at% in a-Si prepared by ion-implantation of c-Si) can account for the extremely high equilibrium solubility of transition metals in a-Si, exceeding the corresponding solubility in c-Si by orders of magnitude. In as-deposited a-Si the defect concentration is not at the equilibrium value, but thermal annealing results in a lower equilibrium concentration of defects (still higher compared with c-Si). It is obvious that diffusion processes can be influenced by the high concentration of intrinsic defects in a-Si [86].

Experiments on transition-metal diffusion in a-Si, by means of Rutherford back scattering spectroscopy (RBS) [87] (Zn, Pt, Au, Ag, Pd, Cu) led to the following results: In

a-Si all transition metals investigated underwent direct interstitial diffusion that was retarded by temporary trapping at intrinsic defects. As a result, Pd and Cu diffused slower in a-Si than in c-Si where they were interstitial diffusers, while Zn, Pt and Au diffused faster in a-Si than in c-Si where they were hybrids diffusing by the kick-out mechanism. In this model, the value of the diffusion coefficient was expected to be strongly dependent on the ratio of the solute concentration to the defect concentration.

Ulfcrt et al [86] investigated the temperature dependence of Au diffusion in a-Si in the temperature range of 50°C to 430°C. The results are presented in the Arrhenius plot shown in Figure 2.10.

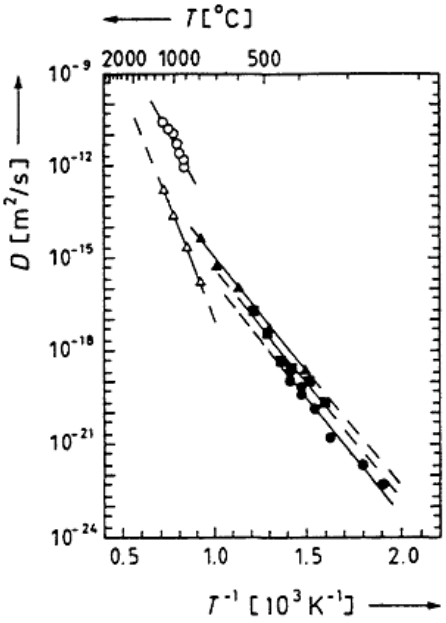


Figure 2.10. Comparison of the diffusion coefficients for Au in dislocation-free c-Si (Δ, [88]), dislocated c-Si (o, [88]) and a-Si produced by sputter deposition (•, [87]), by ion implantation (■ , [89]) and by CVD (▲,[72]).

Although the Au-diffusion coefficient at a given temperature depends on the Au concentration and the diffusion time, fitting to the Arrhenius plot is reasonable with a pre-exponential factor of 7×10^{-9} m^2/s and an activation enthalpy of (1.5 ± 0.1) eV. Therefore the diffusion coefficient of Au in Si at different temperatures can be calculated using the following equation:

$$D_i = D_{i,0}\exp(-\frac{H_i^M}{KT}) \quad (2.6)$$

D_i is the interstitial diffusivity in hypothetical trap-free a-Si which is assumed to be approximately equal to D_i in c-Si, with pre-exponential factor $D_{i,0}$ and the migration enthalpy H_i^M; k is the Boltzmann constant and T is the temperature in K [86].

2.6.7. Si diffusion in Au

When a Si wafer covered with Au was heated in air to about 150°C, the following facts were observed: (1) Si atoms migrated through the Au film and accumulated on its front surface. (2) The accumulated Si was chemically bound in the form of an oxide layer. (3) The major growth of the layer took place within the first 10 to 15 min of annealing. (4) The thickness of the layer increased with increasing temperature. During annealing a visible change in the color of the surface was observed. However, the final appearance depended on the heat treatment and the Au thickness. This migration of Si through Au took place well below the eutectic temperature, since the Au-Si eutectic temperature is at 363°C. Using RBS analysis it was shown that the Si accumulated as a uniform oxide layer over Au. Oxide layers as thick as 200 nm have been obtained at 250°C. The thickness of Si oxide which grows during annealing depends on the ambient atmosphere. Air enhances the Si oxide formation process when compared with a nitrogen atmosphere. At temperatures above 250°C but still below the eutectic, Au begins to penetrate into the Si [90].

2.6.8. Stress in Si layer

There are many factors that affect the crystallization temperature. Stress is one factor that can significantly influence crystallization temperature and grain size. Thin film deposition can introduce residual stresses and resultant bending of substrates. The degree of substrate bending depends on the deposition processes, material properties of the thin films and the substrates. Stoney's equation is used to calculate the residual stresses of thin films [75].

$$\sigma = \frac{E_s}{6(1-\nu_s)} \frac{h_s^2}{h_f} \left(\frac{1}{R_2} - \frac{1}{R_1}\right) \quad (2.7)$$

where σ, h_s, and h_f are the residual stress of a thin film, the thickness of the substrate and the thickness of the thin film, respectively. E_s and ν_s are the Young's modulus and Poisson's ratio of the Si substrate, respectively. The terms R_1 and R_2 are the substrate radius of curvature before and after the deposition of a thin film, respectively.

Tensile stress causes a wafer to bend concavely, while compressive stress causes a wafer to bend convexly. Sputtering a-Si induces a compressive stress, and the value of the stress varies significantly with the thickness of the deposited film, which is higher than for PECVD a-Si. In addition, a thicker a-Si film exhibits a smaller compressive stress.

The total stress in an amorphous thin film at a given temperature consists of intrinsic and thermal stresses [91]. Intrinsic stress is produced during thin film growth and thermal stress is generated by the difference in CTE between a thin film and a substrate. In order to reduce the intrinsic stress of a thin film, a post deposition anneal is required. The cooling rate also plays an important role because the more slowly the samples are cooled, the smaller is the stress that develops. Since the cooling rates are usually slow (about 1°C/min), the intrinsic stress measured at room temperature should be close to the intrinsic stress at the annealing temperature. As the total stress of the thin films also includes thermal stress, it is necessary to evaluate the thermal expansion of the materials. The CTEs are 2.5×10^{-6}/°C, 4.0×10^{-6}/°C, 3.0×10^{-6}/°C and 19.2×10^{-6}/°C for c-Si, PECVD a-Si:H, sputtered a-Si and Au, respectively [91]. At the annealing temperature, the differences in thermal expansion for a-Si:H, a-Si and the Si substrate are small, while the CTE of Au is significantly higher. Thermal stress induced by adjacent films can be estimated from the CTE from the following equation:

$$\sigma_1 = (\alpha_2 - \alpha_1)\Delta T E_1 \quad (2.8)[91]$$

where σ_1 is the thermal stress of film 1, ΔT is the change in temperature and E_1 is the Young's modulus of film 1. α_1 and α_2 are the coefficients of thermal expansion of two adjacent materials, 1 and 2.

Chapter 3

Experimental Methods

Chapter 3 - Experimental Methods

3.1. Diffusion couple experiments

In order to understand the diffusion mechanisms during solid-state Au/Si wafer bonding, annealing experiments were performed on Au/a-Si and Au/c-Si diffusion couples. The native oxide from (100) oriented Si wafers was removed by RF etching for 2 min at 250 V bias with a base pressure of 133 Pa. An a-Si layer (2 µm) was deposited immediately after cleaning by plasma enhanced chemical vapor deposition (PECVD) followed by sputtering of 800 nm of Au directly on a-Si. For the c-Si samples, after cleaning, a thin Ti adhesion layer (10 nm) was deposited followed by deposition of the Au layer (200 nm). The layer thicknesses and deposition parameters are summarized in Table 3.1.

The wafers were sectioned into 8 mm × 8 mm squares using a diamond saw. The samples were annealed at three different temperatures (250, 300 and 350°C) in a tube furnace for 10, 20 and 30 min in forming gas (5% H2–95% N_2) to minimize Si oxidation. After cooling, the samples were cleaved and cross sections of the fracture surfaces were examined by scanning electron microscopy (SEM) using a JEOL JAMP 9500F field emission Auger microprobe. The instrument was operated as an SEM using an accelerating voltage of 15 kV and a working distance of 22.4 mm; secondary electrons (SE) were used to form the images. Focused ion beam (FIB) methods were applied to prepare site specific transmission electron microscopy (TEM) samples for higher resolution examination. A Hitachi NB5000 dual beam FIB/SEM, operated at 30 kV, was used for this purpose with a 7 nm Ga+ beam as the ion source. The lift-out technique was used to prepare the FIB samples. In this method a parallel sided piece of sample was directly removed from the bulk sample via an internal nanomanipulator and transferred to a Cu TEM grid. Carbon was sputtered onto the surface to prevent any damage to the sample due to the ion beam. The sample was placed in the chamber and a suitable location was determined. A layer of 1 µm thick W was deposited on an area

of 2 µm x 12 µm to glue the manipulator probe to the sample and then to the grid. FIB milling was performed to obtain an electron transparent lamella. A machine setting of 40-1-300 (accelerating voltage, condenser lens on, aperture size) was used, which resulted in 20 nA of milling current for rough milling. The sample was lifted and placed onto a Mo lift out grid and attached with W. For the initial W deposition and milling, high beam currents and accelerating voltages were used to accelerate the process (machine settings of 40-1-80 giving a beam current of 10 nA). For the final thinning and polishing, lower current beams and accelerating voltages were used to reduce the beam damage and have better control (machine settings of 40-1-30 and 40-1-15 giving currents of 0.1 nA and <0.1 nA).

A JEOL 2010 TEM, operated at 200 kV and equipped with a Noran ultrathin window (UTW) X-ray detector, was used for imaging and high spatial resolution diffraction and composition analysis. Line scans were performed using the Tecnai F20 TEM/STEM, operated at 200 kV, at the University of Calgary.

Table 3.1. Deposition parameters for diffusion couple experiments

Sample	Layers	Thickness	Deposition parameters
Au/a-Si/c-Si	Au	800 nm	Sputtered 1 kW in 133 Pa Ar Deposition rate of 12 nm/min
	a-Si	2 µm	PECVD 133 Pa base pressure 30 sccm SiH_4 and 500 sccm He
Au/Ti/c-Si	Au	200 nm	Sputtered 1 kW in 133 Pa Ar Deposition rate of 12 nm/min
	Ti	10 nm	Sputtered 1 kW in 133 Pa Ar Deposition rate of 12 nm/min

3.2. Small samples bonding experiments

Silicon wafers, (100) oriented and 100 mm in diameter, were used for bonding. The processing details are summarized in Table 3.2 and are briefly described below. The

native oxide was removed by RF etching for 2 min at 250 V bias with a base pressure of 133 Pa. Immediately after removing the oxide, 200 nm of TiW was sputtered onto half of the wafers (the other half of the wafers was used to deposit a-Si) using a plasma enhanced sputtering system. The TiW acts as a diffusion barrier and an adhesion layer for subsequent Au deposition. Following this step, 800 nm of Au was sputtered under the same sputtering conditions as TiW. For a-Si wafer samples, after wafer cleaning, 800 nm of a-Si was deposited using plasma-enhanced chemical vapor deposition (PECVD).

According to the phase diagram and Equation (3.1) [92] in order to reach the eutectic composition, the ratio of Au to Si thickness should be 3.9. To achieve that thickness ratio, the wafer was diced into 8 mm × 9 mm samples and an additional Au layer (2.63 µm) was deposited by electrodeposition.

$$t_{Si} = \left(\frac{wt.\%Si}{wt.\%Au}\right)\frac{\rho_{Au}}{\rho_{Si}}t_{Au} \tag{3.1}$$

where t_{Si} is the Si layer thickness, t_{Au} is the Au layer thickness, ρ_{Si} is the Si density, ρ_{Au} is the Au density, wt.% Si is the weight percent of Si and wt.% Au is the weight percent of Au.

A Dynatronix DuPR 10-0.1-0.3 pulse plating power supply, with a maximum current rating of 100 mA average current and 300 mA peak current, was used for electrodeposition. Electroplating experiments were carried out under pulsed current (PC) conditions. In the pulsed current mode, a current density of 3 mA/cm^2, an on-time of 2 ms, an off-time of 8 ms and a plating time of 46 min were used based on previous work [93]. The deposition rate was about 0.06 µm/min. The a-Si wafer was diced into 8 mm × 8 mm samples. The size difference between the two mating pairs was beneficial for shear testing.

Table 3.2. Deposition parameters for a-Si wafer bonding experiments

Wafer pairs	Thickness	Deposition parameters
Au/TiW/c-Si	TiW: 200 nm Au: 800 nm	Sputtered 1 kW in 133 Pa Ar 12 nm/min (TiW); 50 nm/min (Au)
a-Si/c-Si	a-Si: 800 nm	PECVD 300°C and 133 Pa pressure SiH_4 gas flow rate of 30 sccm and He gas flow rate of 500 sccm for 6 h

According to previous work on Au-Si wafer bonding [94], four parameters were considered as the main bonding parameters: bonding temperature, bonding time, bonding pressure and bonding atmosphere. The range of the bonding temperatures reported in the literature was from 380-430°C [94][95][96]. Preliminary experiments were performed at different temperatures in this range and two temperatures (400 and 425°C) with the best results were chosen for subsequent experiments. A bonding time range of 10-60 min was also reported in the literature [92][94][95]. In this work, 20 and 40 min were chosen according to preliminary experiments. The bonding tool pressure used in industry is in the 0.133-0.4 MPa range. For these experiments two values, one lower than this range (ten times smaller) (0.0133 MPa) and another at 0.133 MPa were chosen. Also, two different bonding atmospheres, a vacuum at a pressure of 2×10^{-8} MPa and pure nitrogen at a pressure of 1×10^{-3} MPa, were used. Sixteen experiments were designed according to Table 3.3.

Table 3.3. Bonding parameters used for a-Si wafer bonding

Sample #	T (°C)	T (min)	P (MPa)	Atmosphere (MPa)
1	400	20	100	2×10^{-8} (Vacuum)
2	400	20	100	1×10^{-3} (Nitrogen)
3	400	20	1000	2×10^{-8} (Vacuum)
4	400	20	1000	1×10^{-3} (Nitrogen)
5	400	40	100	2×10^{-8} (Vacuum)
6	400	40	100	1×10^{-3} (Nitrogen)
7	400	40	1000	2×10^{-8} (Vacuum)
8	400	40	1000	1×10^{-3} (Nitrogen)
9	425	20	100	2×10^{-8} (Vacuum)
10	425	20	100	1×10^{-3} (Nitrogen)
11	425	20	1000	2×10^{-8} (Vacuum)
12	425	20	1000	1×10^{-3} (Nitrogen)
13	425	40	100	2×10^{-8} (Vacuum)
14	425	40	100	1×10^{-3} (Nitrogen)
15	425	40	1000	2×10^{-8} (Vacuum)
16	425	40	1000	1×10^{-3} (Nitrogen)

According to Dragoi et al. [97], to obtain uniform diffusion before reaching the eutectic temperature and to achieve a good quality bond, the temperature should be raised to a value lower than the eutectic temperature (e.g., 350°C) and kept at that temperature for a short period of time (20 min was chosen here based on preliminary tests). In addition, the samples should be heated from both the top and bottom at the same time. Then the temperature should be raised to above the eutectic temperature (e.g., 400°C) and held for the bonding duration. For this work, different bonding times, from 5 to 40 min, were initially tried and the heating rate was 0.3°C/s for both the pre-anneal and bonding.

Prior to bonding, the a-Si wafer pieces were cleaned with BOE (6:1 volume ratio of 40% NH_4F in water to 49% HF in water) for 5 min, rinsed with deionized water and then dried with nitrogen. The samples were bonded immediately after cleaning. Sample pairs were loaded in a SUSS SB6L bonder and the bonding atmosphere was established before and maintained during bonding.

The initial method used to estimate bond quality was scanning acoustic microscopy (SAM). SAM is a non-destructive method, which can detect cracks, fractures and delaminations as well as other hidden internal defects. A Sonoscan D9000 SAM was used in the present study; it employs a 230 MHz transducer collecting an image of 1024×1024 pixels over the full 8 mm × 8 mm bonded wafer piece. The SAM operates in reflection or echo mode, i.e., sound waves that are reflected from surfaces (including internal surfaces) are detected. As such, bond defects or additional interfaces will show up as brighter regions in SAM images. Ultrasonic waves are reflected at boundaries where there is a difference in the acoustic impedances (Z) of the materials on each side of the boundary. This difference in Z is commonly referred to as the impedance mismatch. The greater the impedance mismatch, the greater the percentage of energy that will be reflected at the interface or boundary between one medium and another. The fraction of the incident wave intensity that is reflected can be calculated from the impedances [98].

$$R = \frac{(Z_2 - Z_1)^2}{(Z_2 + Z_1)^2} \tag{3.2}$$

Z_1 is the acoustic impedance of medium 1, Z_2 is the acoustic impedance of medium 2 and R is the reflection coefficient. For Au and Si, the Z values are 63.8 and 19.7 Pa-s/m^3 (acoustic ohm (Ω)), respectively. Based on Equation (3.2), R is 0.279 so about 28% energy will be reflected in passing a sound wave from Au to Si and vice versa. The percentage of bonded or non-bonded area was measured using Image J software.

After cooling, the samples were cleaved and cross sections of the fracture and polished surfaces were examined by SEM. FIB methods were applied to prepare site specific TEM samples for higher resolution examination.

Mechanical properties of the bonds were measured in terms of shear strength using a Dage 5000 shear tester with a maximum load of 100 kg. During testing, the loading tool pushes the upper part of the die until the sample is broken and the force at failure is recorded (Figure 3.2.1).

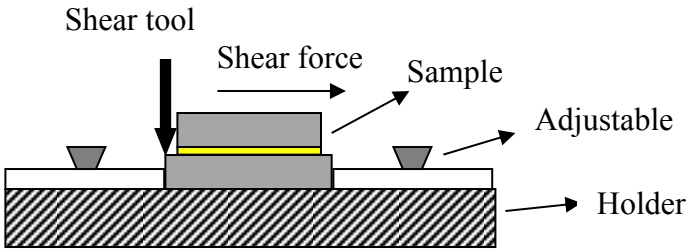


Figure 3.1. Schematic of the shear test tool set up (side view).

For the next step, to observe the effect of pressure, three samples were bonded at different pressures of 0.0133, 0.133 and 0.4 MPa. The reason for choosing these pressures was to try a range of low, medium and high pressures used in industry to observe the effect of pressure. The other parameters were fixed at T= 425°C, t= 40 min and P= 2×10^{-8} MPa. The maximum bonding time and temperature were chosen to allow the formation of sufficient liquid to form the bond. A vacuum environment was used to reduce Si oxidation. SAM images were taken from the bonded pairs.

In order to compare the bonds formed between a-Si and c-Si, c-Si samples were bonded with the same conditions as the a-Si samples. The deposition parameters for c-Si wafer bonding experiments are summarized in Table. 3.4.

Table 3.4. Deposition parameters for a-Si wafer bonding experiments

Wafer pairs	Thickness	Deposition parameters
Au/TiW/c-Si	TiW: 200 nm Au: 800 nm	Sputtered 1 kW in 133 Pa Ar 12 nm/min (TiW); 50 nm/min (Au)
c-Si	-------	----------

In order to compare the effect of bonding temperature for both a-Si and c-Si samples, two different temperatures, i.e., 400 and 425°C were chosen. The rest of the parameters were fixed at t= 30 min, P= 0.0133 MPa and a vacuum pressure of 2×10^{-8} MPa. SAM, SEM and AES (both point analysis and mapping) were performed on cross section and plan view orientations of these samples. Each bonding condition was duplicated to test reproducibility.

Due to delamination and cracking issues, the a-Si deposition method was changed from PECVD to low pressure chemical vapor deposition (LPCVD). The LPCVD conditions for a-Si deposition were 550°C, 40 Pa pressure and a SiH_4 gas flow rate of 30 sccm for 6 h. The surface roughness of the deposited a-Si layers by LPCVD and PECVD were compared using Asylum Research atomic force microscopy (AFM) model MFP-3D.

Stress is one of the important issues in semiconductors, which can result in formation of cracks and voids. Raman spectroscopy is a nondestructive method that can be used to measure stress with good spatial resolution. Mechanical stress results in a shift in Raman modes (phonons). The magnitude of this shift is proportional to the amount of strain. The Raman spectrometer was first calibrated with a standard sample and then the spectra for c-Si, LPCVD a-Si and PECVD a-Si were obtained. MATLAB software was used to fit the Lorentz equation to the curves obtained by Raman spectroscopy and to estimate peak locations.

To minimize dissolution of c-Si from the wafers, a thickness ratio of Au:Si of 2:1 was used for the rest of the samples. In order to improve pressure uniformity, instead of placing one sample in the middle of the chuck, four samples were placed on the chuck as shown in Figure 3.2.

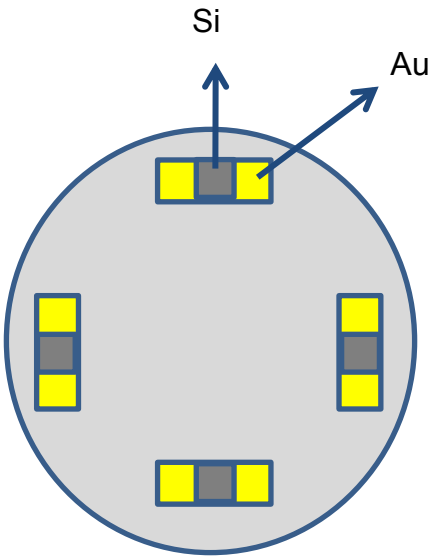


Figure 3.2. Four sample configuration used on the chuck in order to improve pressure uniformity.

During testing, it was found that the range of applied pressures (0.133-0.4 MPa) used in industry is for bonding full 100 mm diameter wafers that are patterned. In order to correct the applied pressures and calculate suitable pressures for small pieces, it was assumed that 30% of the wafer was patterned. Therefore the actual bonded area is given as:

0.30 × 7850 mm^2 (area of full 100 mm diameter wafer) = 2355 mm^2

There is a relationship between the virtual pressure shown by the bonder (P_{tool}) and actual pressure applied to the sample (P_W), which is shown by Equation 3.3:

$$P_w = \frac{A_{chuck}}{A_{wafer}} \times P_{tool} \qquad (3.3)$$

where A_{chuck} is the area of the chuck used in the bonder, which for the bonder used in this work (SUSS SB6L) is equal to 22,223 mm^2, and A_{wafer} is the area of the sample used.

In order to find the forces corresponding to P_{tool} shown on the bonder, the bonder was tested with a sample at different P_{tool} values; the forces (F) and the ratio of F/P are reported in Table 3.5. There is usually a slight difference between the programmed tool pressure and the tool pressure obtained, which is also reported in Table 3.5. According to data in Table 3.5, which was obtained from the bonder, the force needed for a P_{tool} of 0.133 MPa is 2973 N. Therefore the P_w for bonding a full wafer is:

$P_w = F/A = 2973\ N/2355\ mm^2 = 1.26\ MPa$

To achieve the same bonding pressure for small samples, with a total area (4 samples) of 4 × 8 mm × 8 mm = 256 mm^2:

$F = 1.26\ MPa \times 256\ mm^2 = 322\ N$

Table 3.5. Data obtained from the bonder

P_{tool} programmed (MPa)	P_{tool} obtained (MPa)	Force(N)	F/P
0.0133	0.0143	319	2.95
0.033	0.034	746	2.96
0.066	0.066	1472	2.96
0.133	0.134	2973	2.96
0.0266	0.236	5240	2.96
0.399	0.399	8874	2.96

If the data in Table 3.5 is plotted (Figure 3.3), a linear equation is obtained relating the actual pressure and force:

F (N) = 22241 P (MPa) – 3.5293

Therefore, the tool pressure needed in the bonder is:

322 = 22241 P - 3.5293 or P = 0.0146 MPa

Similarly, to achieve the maximum pressure used in industry for bonding of full 100 mm diameter wafers (0.4 MPa), P_{tool} should be set to 0.0435 MPa.

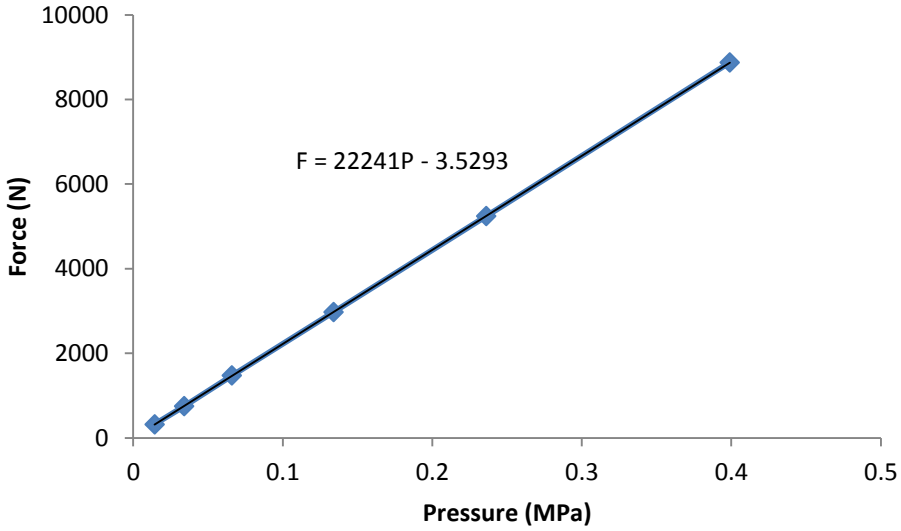


Figure 3.3. Force versus pressure plot for the bonder.

Therefore, the pressures chosen for preheating and bonding were 3.76 and 1.26 MPa, respectively. The pressure was reduced during the bonding stage to minimize solder spill out. Since the four sample configuration was not very effective for pressure uniformity, five samples were placed on the chuck as shown in Figure 3.4. Bonding pressures were calculated according to the new bonded area and the tool pressure used for the samples during preheating and bonding were 0.0542 and 0.0182 MPa, respectively. Cross section SEM images and SAM images were obtained from the samples.

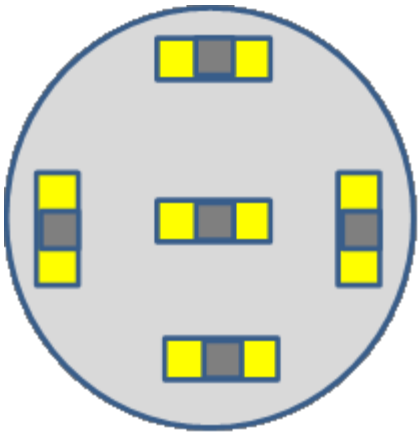


Figure 3.4. Five sample configuration used on the chuck in order to improve pressure uniformity.

Two graphite sheets were installed beneath the upper and lower chuck to improve the pressure distribution. Pressure paper tests were conducted to compare the pressure uniformity before and after installing the graphite sheets.

In order to reduce the process temperature, a-Si solid-sate bonding was performed at 350°C for 10 and 20 min at a pressure of 2×10^{-4} MPa. The five sample configuration (Figure 3.4) was used. The bonding pressure was increased to 6 MPa to improve contact between the wafers. Each condition was repeated three times to test repeatability. SAM images were taken from all samples. SEM SE images were taken from samples bonded for 20 min and a FIB sample was made from the same sample. TEM images and electron diffraction patterns were obtained from the samples bonded for 20 min.

Eutectic bonding tests were repeated after installing the graphite sheets for a-Si wafers. Samples were preheated to 350°C for 20 min and bonded at 400°C for 30 min. The five sample configuration was used. The tests were repeated three times. SAM imaging was performed on the samples.

Eutectic and solid-state bonding were performed on the c-Si samples with the same parameters as for the a-Si samples. The five sample configuration was used. SAM

imaging was performed on all the samples. SEM SE imaging was performed on cross sections of the bonded c-Si pairs for both solid-state and eutectic bonding. A FIB TEM sample was prepared from the c-Si sample bonded at 350°C for 20 min and TEM images and electron diffraction patterns were obtained.

Shear testing was performed on a-Si and c-Si samples, which were bonded under solid-state and eutectic conditions.

3.3. Full wafer bonding experiments

Full wafer solid-state and eutectic bonding were performed on both a-Si and c-Si samples. The thicknesses were chosen based on the eutectic composition. The patterned Au wafers provided had 823 nm thick Au layers. The goal then was to deposit 210 nm of a-Si. The actual thickness of a-Si was 193 nm. These layers were deposited by LPCVD with similar deposition parameters as for LPCVD a-Si used in small sample bonding. Gold was also sputtered with the same deposition parameters given in Table 3.1. The pattern dimensions were 5 mm × 5 mm.

The first set of samples was cleaned (prior to bonding) with buffered oxide etch (10 HF:1 H_2O) for 5 min, rinsed with deionized water and then dried with nitrogen. The resultant bond showed impurities in the bonded area. Another step was added to the cleaning process, i.e., SC1 cleaning which was done before HF cleaning. SC1 is used to remove organic contamination and particles from the wafers. The solution is a mixture of ammonium hydroxide (30% NH_4OH), hydrogen peroxide (30% H_2O_2) and deionized water at a ratio of 1:1:5. The solution was warmed to 75°C and the wafers soaked for 10 min. This was followed by thorough rinsing with deionized water and drying with nitrogen.

To increase the pressure uniformity of the bonder, two blank Si wafers and a graphite sheet were placed directly on top on wafer stacks. Based on the wafer pattern, 0.060 MPa and 0.023 MPa tool pressures were used for preheating and bonding,

respectively. For preheating and solid-state bonding, 350°C and 20 min were chosen. Bonding was done at 400°C for 15 min.

SAM imaging was performed on the full wafers after bonding. The wafers were then diced into 5 mm × 5 mm pieces for cross section SEM imaging, AES mapping and shear testing.

3.4. In-situ TEM experiments

In-situ TEM annealing experiments were carried out to investigate the mechanism for layer exchange which happens in the Au-Si system both in Au/a-Si diffusion couples and bonded samples, as discussed in Section 2.4.4 in Chapter 2. A diffusion couple of Au/a-Si with the same thicknesses (50 nm) of Au and a-Si was used. The Si wafer was cleaned with HF to remove the oxide layer. Then a-Si was deposited by PECVD using a 133 Pa base pressure, 30 sccm SiH_4 and 500 sccm He. The desired thickness was 50 nm, but the actual layer thickness was 60 nm. Gold was deposited on a-Si by sputtering at 1 kW in 133 Pa Ar with a deposition rate of 12nm/min after the oxide layer was removed from a-Si surface by etching the surface layer.

Three different temperatures (250, 300 and 350°C) were chosen to observe the temperature effect on the rate of Au and Si diffusion and layer exchange. Cross section TEM samples were prepared with a Hitachi NB 5000 SEM/FIB dual beam instrument, following a procedure similar to the sample preparation for diffusion couple experiments mentioned earlier in this chapter. TEM lamellae about 100 nm thick were plucked out and mounted onto TEM grids, using a 10 kV Ga beam in the final polishing step to minimize beam damage to the sample.

In-situ TEM analysis was carried out on a Hitachi H9500 Environmental TEM, operating at 300 kV. The heating time was 10 min from room temperature to the desired temperature. The pressure was kept at 2.3×10^{-6} Pa. Bright field (BF) TEM images were acquired automatically during the annealing process at 2 s intervals.

For the sample annealed at 250°C, the images were taken at 30,000x magnification. The diffusion was very slow at this temperature, so sample was annealed for 8 h until diffusion of Au in c-Si was observed. The reaction rate was higher for the sample annealed at 300°C; therefore, the annealing time needed for Au to start diffusing into c-Si was 3 h. The images were taken at 20,000x magnification for the 300°C anneal. The reaction rate was so fast for the 350°C anneal that the heating was done in steps to slow down the reaction. The magnification used was 40,000x. First the sample was heated 250°C in 10 min. After 20 min at 250°C, heating was continued to 300°C in 10 min and the sample was held at that temperature for 20 min. The final step was heating from 300 to 350°C in 10 min and keeping the sample at 350°C for 20 min. Using Movie Maker software, the image frames were combined to make a video of Au and Si interdiffusion and layer exchange at different temperatures.

Chapter 4

Diffusion Couple Results

Chapter 4 - Diffusion Couple Results

4.1. a-Si diffusion couple

To better understand the diffusion effects associated with Au and Si, annealing experiments were done with Au/a-Si and Au/Ti/c-Si couples prior to bonding. Figure 4.1 and Figure 4.2 show SEM SE images of as deposited Au/a-Si and Au/Ti/c-Si couples, respectively, after storage for 2 weeks at room temperature. There is evidence for interdiffusion between the Au and a-Si layers for the Au/a-Si couple (Figure 4.1). The diffusion zone is ~400 nm thick and consists of regions of bright and dark contrast. Auger analysis of the two regions indicated that they are Au (bright) and Si (dark). The Au/Ti/c-Si diffusion couple did not show any obvious sign of interdiffusion (Figure 4.2), i.e., the interface between Au and Si was sharp.

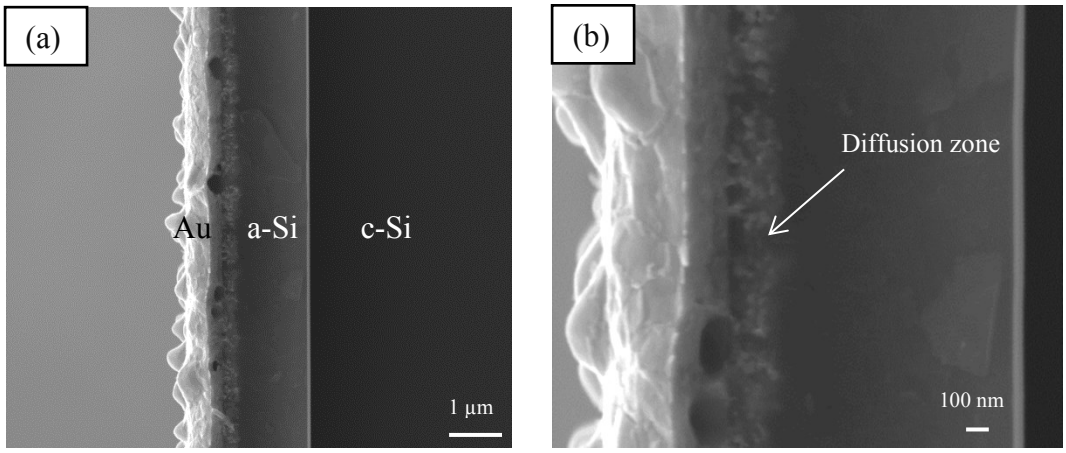


Figure 4.1. SEM SE images of a cleaved cross section for as-deposited Au/a-Si/c-Si diffusion couple: (a) low magnification image and (b) higher magnification image. The sample was stored for 2 weeks at room temperature prior to imaging.

For the Au/a-Si couples, annealing at 250, 300 and 350°C for 10, 20 and 30 min (Figure 4.3, 4.4 and 4.5, respectively) shows that the degree of interdiffusion increased with increasing annealing temperature and time. Note that the entire a-Si layer has been consumed for the 30 min anneal at 350°C.

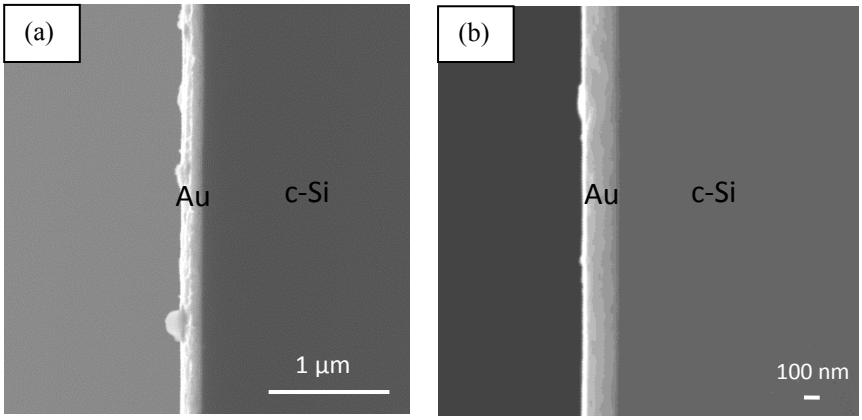


Figure 4.2. SEM SE images of cleaved cross sections for as-deposited Au/Ti/c-Si diffusion couple: (a) low magnification image and (b) higher magnification image. The sample was stored for 2 weeks at room temperature prior to imaging.

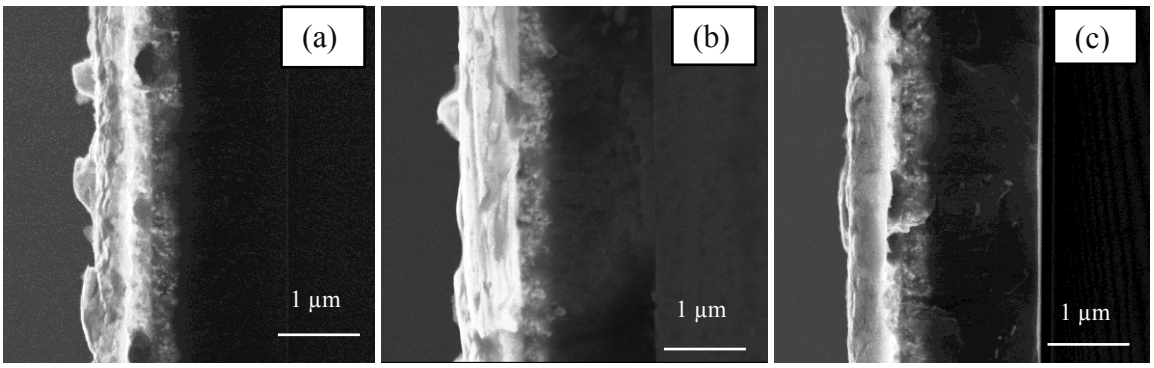


Figure 4.3. SEM SE images of cleaved cross sections for Au/a-Si diffusion couples annealed at 250°C for (a) 10 min, (b) 20 min and (c) 30 min.

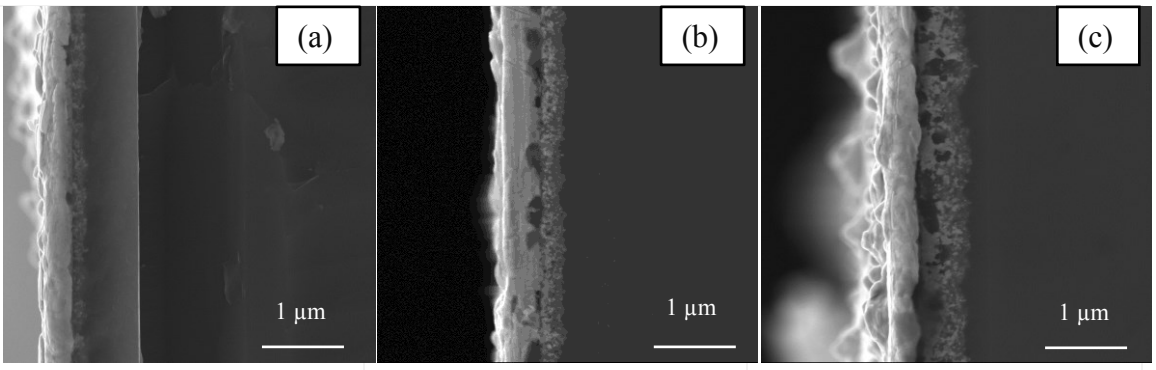


Figure 4.4. SEM SE images of cleaved cross sections for Au/a-Si diffusion couples annealed at

300°C for (a) 10 min, (b) 20 min and (c) 30 min.

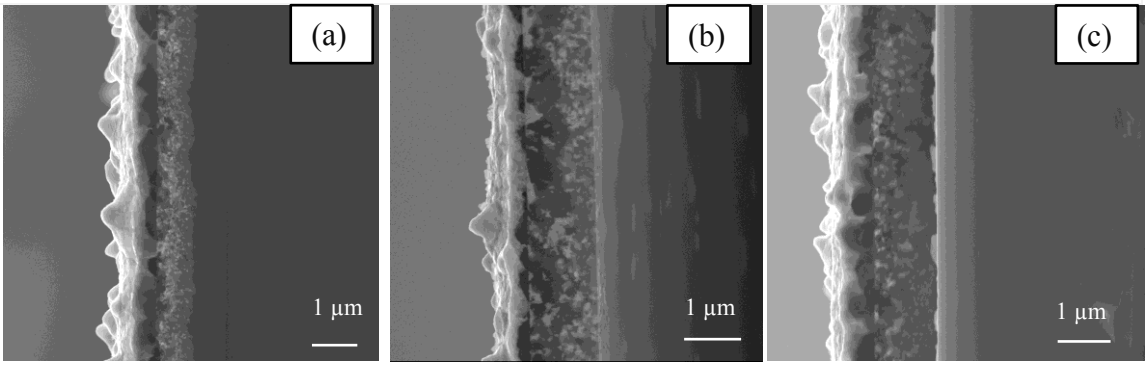


Figure 4.5. SEM SE images of cleaved cross sections for Au/a-Si diffusion couples annealed at 350°C for (a) 10 min, (b) 20 min and (c) 30 min.

To study the interdiffusion process in more detail, a FIB specimen was prepared from the sample annealed at 350°C for 20 min and examined in the TEM. A bright field (BF) image is shown in Figure 4.6(a). Two distinct regions are present in the diffusion zone. One region is a mixture of Au and Si, which was confirmed by energy dispersive X-ray (EDX) spectroscopy and selected area diffraction (SAD) (Figure 4.6(b)). The SAD pattern consists of 2 sets of concentric rings, which can be indexed to Au (FCC structure) and Si (diamond cubic structure). A SAD pattern from one of the bright grains indicated in Figure 4.6(a) is shown in Figure 4.6(c). The diffraction pattern is single crystalline and can be indexed to Si with a zone axis close to the $[1\ \overline{2}\ 1]$ orientation. The crystallization process for a-Si is due to so-called metal-induced crystallization (MIC) of Si, which is discussed in detail Chapter 3. It is clear that crystallization of a-Si starts when Au begins to intermix with the Si. It has been suggested previously by Tu [99] and Hiraki [100] that in the presence of Au, the Si bonds adjacent to the metal becomes unstable by screening the Coulomb interaction via its mobile free electrons. An alloyed interface region can form as a result of a reduction in activation energy for Si dissociation in which released Si atoms can migrate readily.

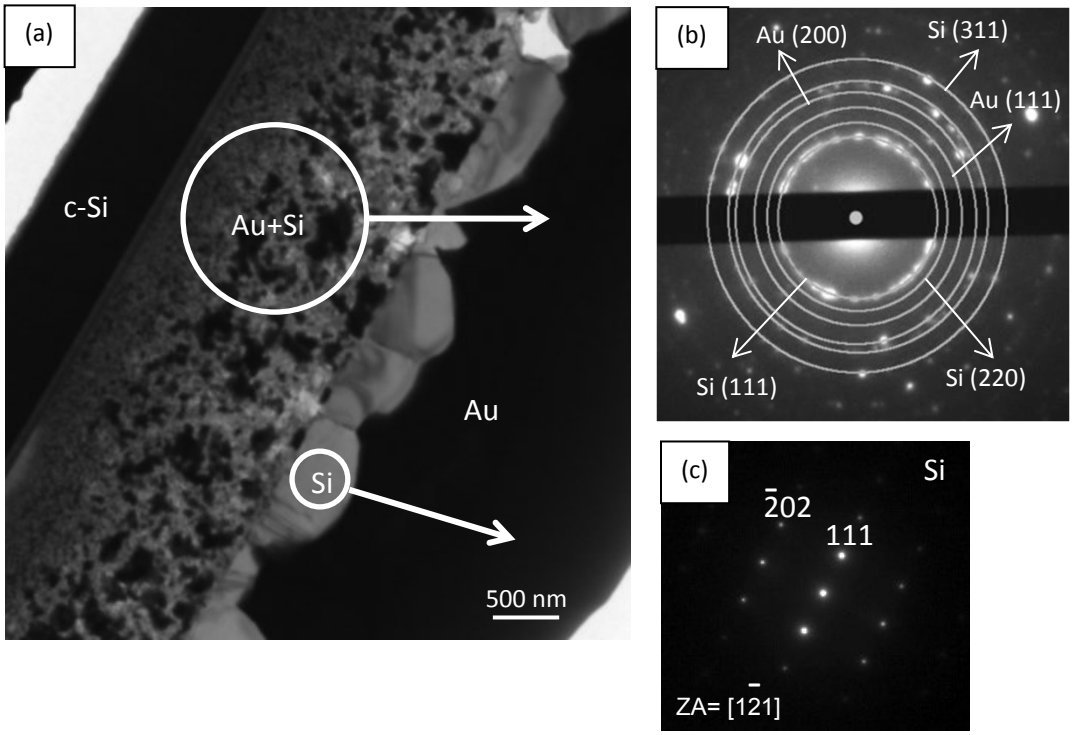


Figure 4.6. a) TEM BF image, b) SAD pattern of the Au-Si intermixed region and c) SAD pattern from the Si grain indicated in (a) for the Au/a-Si diffusion couple annealed at 350°C for 30 min.

Nast et al. [79] have suggested a model for layer exchange in the Al/a-Si system. According to their model the process of crystal growth can be divided into 3 steps (summarized in Figure 4.7) which are (1) the diffusion of Si atoms into the Al layer, (2) diffusion of Si atoms in the Al and (3) joining of dissolved Si atoms to the Si nuclei. The initial interaction of the Al and a-Si layers involves partial dissolution of the Al or Si oxide interfacial layer, depending on the layer sequence, to allow for interdiffusion of the materials. This process has been analyzed by Kim and Lee for Al/native SiO_2/a-Si structures [101]. They proposed that the Si oxide layer is transformed by the Al into a mixture of Al oxide and an Al_xSi phase. This newly formed Al_xSi phase provides a diffusion channel for the Si and Al atoms. However, this mechanism cannot be expanded to the Au-Si system as an Au oxide layer does not exist in this system. Although Au and Si have very limited solubility, a very small amount of dissolution

happens at temperatures below the eutectic temperature of 363°C. It is assumed that there should be a minimum Au concentration available to act as a catalyst for a-Si crystallization. This may be the reason that the first nuclei form and grow in locations with high Au concentration (within Au layer rather than inside the a-Si layer).

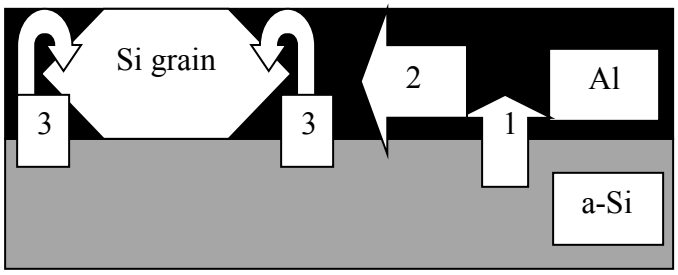


Figure 4.7. Schematic diagram of the diffusion and interface processes involved in the grain growth [79].

The mobility of dissolved Si atoms is high, which helps in the diffusion of Si atoms towards the growing Si grains within the film or along the interfaces [102]. The faster growth in the Au layer in comparison with the growth in the normal direction to the layer will result in the formation of continuous poly-Si film between the interfaces [79]. Nast et al. [79] have shown that decreasing the annealing temperature will result in the formation of larger grains in the polycrystalline material due to larger growth rate compared to nucleation rate. The grain size distribution depends on the ratio of the grain growth rate to the nucleation rate; therefore, this ratio increases with decreasing annealing temperature. It is suggested [79] that at lower annealing temperatures the effective diffusion distance is longer, which results in larger depletion areas around the growing grains, which prevents further nucleation. Therefore, the grains grow to a larger size before impingement occurs. It has been considered that both nucleation and growth are thermally activated processes. Therefore at lower annealing temperatures, complete crystallization takes longer [79].

The activation energy for Au and Si interdiffusion in the Au/a-Si couples was estimated by measuring the thickness of the diffusion zone and relating it to the diffusion time and temperature according to Equation 4.1 [103]:

$$x^2 \propto Dt = D_0 t \, exp[\frac{-Q}{RT}] \quad (4.1)$$

where x is the size of the diffusion zone, t is time, D is the diffusion coefficient, D_0 is the frequency factor, T is temperature, Q is the activation energy and R is the ideal gas constant (8.314 J/(K mol)). Only the 10 and 20 min samples were used for this purpose, as the 2 µm a-Si layer was completely consumed for the 30 min anneals at 300 and 350°C. The activation energy was determined from a plot of $\ln(x^2)$ vs. 1/T (Figure 4.8). Values of 60 and 69 kJ/mol were obtained for the 20 min and 10 min samples, respectively. These compare favorably with the value quoted in [104] (69 kJ/mol), which was determined from studies of Au implanted (200 keV) at room temperature in CVD a-Si that had been deposited at 450°C. The implanted structures were annealed at 400-800°C from 1 s to 40 min. Rutherford backscattering spectroscopy (RBS) was used to measure the Au concentration profile in[72].

4.2. c-Si diffusion couples

SEM SE images for Au/c-Si couples annealed at 250, 300 and 350°C for 10, 20 and 30 min are shown in Figure 4.9, 4.10 and 4.11, respectively. Annealing resulted in the formation of faceted craters, with facets protruding into the Si along the {111} type planes (Figure 4.13(b)). As for the a-Si samples, the degree of interdiffusion increased with increasing annealing temperature and time and the size of the craters increased as a result of the increase in Si dissolution.

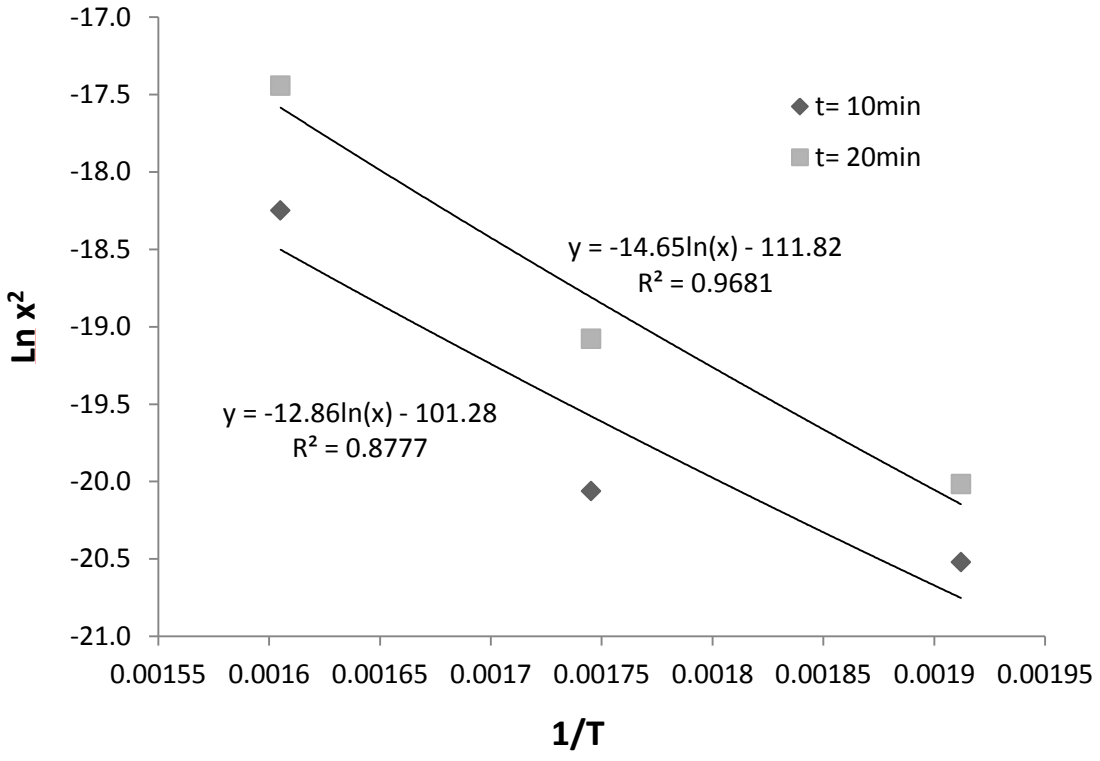


Figure 4.8. Plot of the natural logarithm of diffusion depth squared vs. inverse annealing temperature for a-Si diffusion couples annealed for 10 and 20 min.

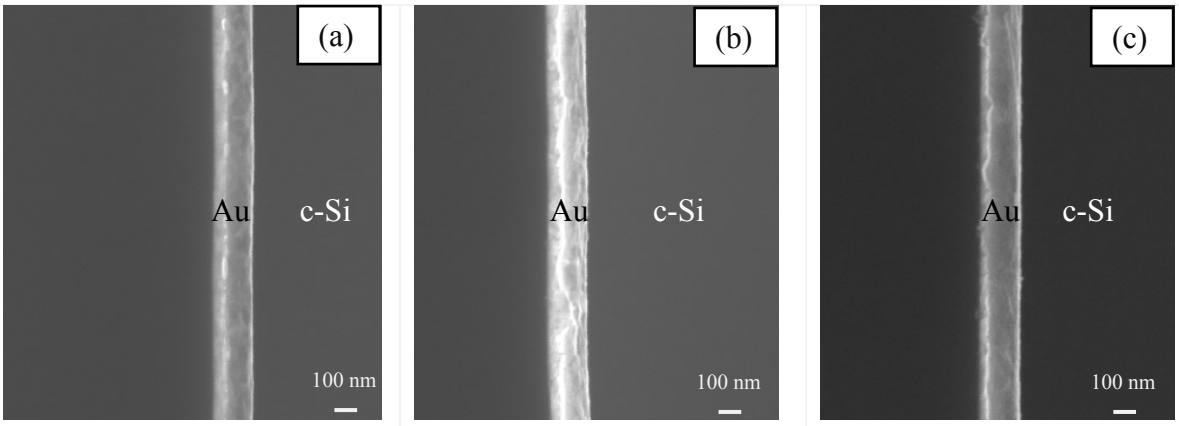


Figure 4.9. SEM SE images of cleaved cross sections for Au/c-Si diffusion couples annealed at 250°C for (a) 10 min, (b) 20 min and (c) 30 min.

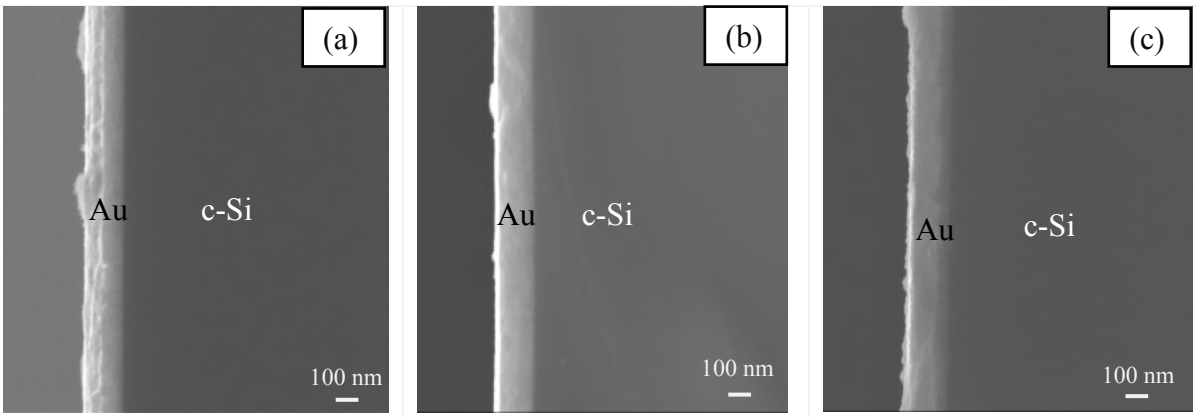


Figure 4.10. SEM SE images of cleaved cross sections for Au/c-Si diffusion couples annealed at 300°C for (a) 10 min, (b) 20 min and (c) 30 min.

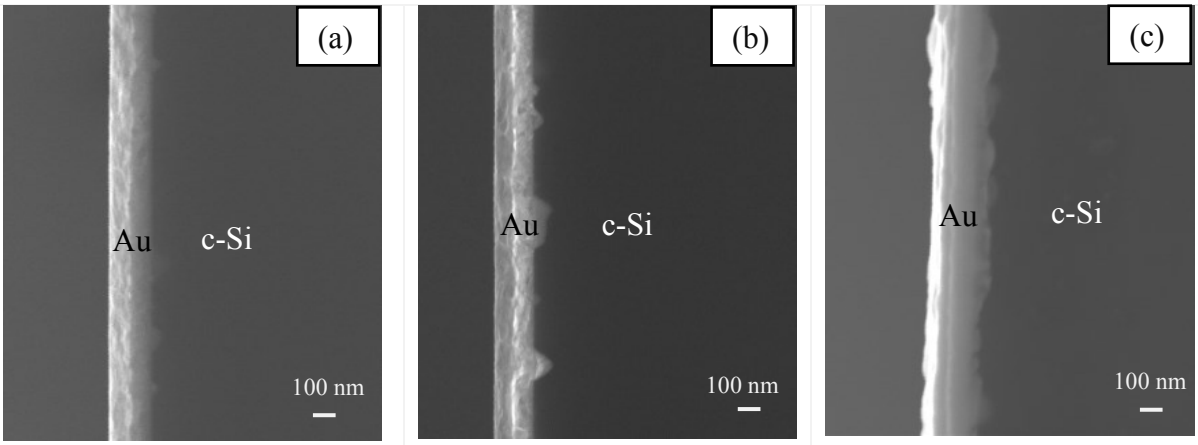


Figure 4.11. SEM SE images of cleaved cross sections for Au/c-Si diffusion couples annealed at 350°C for (a) 10 min, (b) 20 min and (c) 30 min.

Comparison of the a-Si/Au couples with the c-Si/Au couples shows that the rate of reaction is much faster for the a-Si/Au couples. The reason is the high dependence of the c-Si/Au reaction rate on the crystallography of the Si wafer. In other words, Si dissolution into the Au layer proceeds preferentially along particular planes, usually the planes with the highest surface energy. In crystalline Si, the (111) plane has the lowest surface energy, so is the most resistant to dissolving in Au. This means that, as Si reacts with and dissolves in Au, faceted craters, i.e., V-shape grooves or inverted pyramids form on the c-Si surface [105]. For a-Si samples, diffusion occurred even at room temperature while in c-Si samples no Au diffusion in c-Si was detected, by AES, at

room temperature or even in samples annealed at 250°C for 30 min. The presence of the large number of dangling bonds in a-Si causes a high defect density, which in this case results in faster Au diffusion in a-Si compared with c-Si.

Another interesting observation is the formation of holes on the Au surface during annealing as a result of the formation of craters, which act as sinks for Au. The holes increase in number and size as the annealing time and temperature are increased. This is apparent in Figure 4.12 for samples annealed at 250, 300 and 350°C for 30 min. There were no holes observed for samples annealed at 250°C for 10, 20 and 30 min. Figure 4.13 shows an SEM image of a tilted sample that had been annealed at 350°C for 30 min. A hole on the Au surface is visible above a crater at the Au/Si interface, although the two are slightly offset relative to one another.

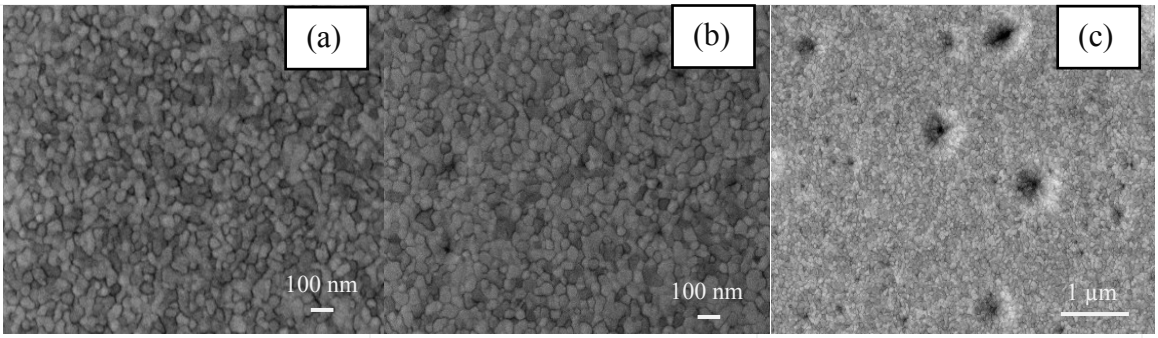


Figure 4.12. SE SEM images of hole formation on the Au surface at (a) 250°C, (b) 300°C and (c) 350°C for samples annealed for 30 min.

A FIB specimen from the Au/c-Si interface of the sample annealed at 350°C for 30 min was prepared for TEM analysis. Two overlapping faceted craters are shown in Figure 4.14(a). Diffraction analysis (e.g., Figure 4.14(b)) and EDX analysis (Figure 4.14(c)) confirmed that the craters were single crystalline and filled with Au. The small Si peak in the EDX spectrum is likely from the area surrounding the crater. The faceted craters tend to form where the grain boundaries of the columnar Au grains intersect with the c-Si surface (Figure 4.14(a)), which indicates that Au is supplied through diffusion along the grain boundaries.

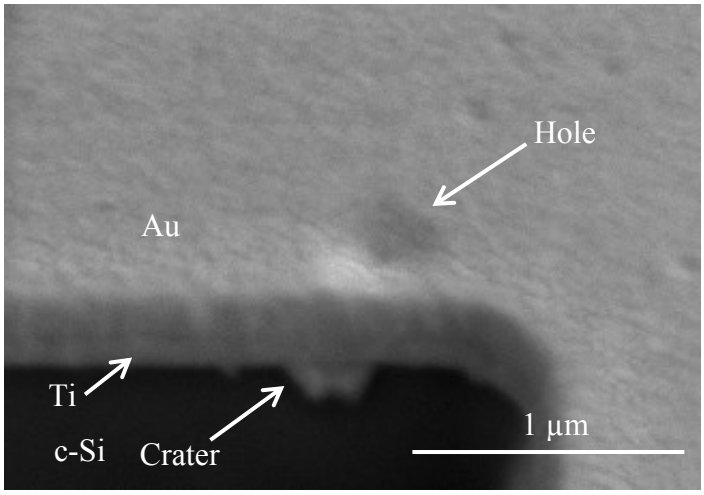


Figure 4.13. SEM SE image of crater/void formation during annealing of a Au/Ti/c-Si couple at 350°C for 30 min.

In order to investigate the distribution of different elements (i.e., Au, Si and Ti), X-ray line scans were done on cross section samples, as shown in Figure 4.15. Line scan results indicate that both Si and Ti have diffused to the Au surface after annealing at 350°C for 30 min. The diffusion of Si to the surface happens very fast, even at room temperature, as observed from the XPS spectrum of the as deposited Au/Ti/c-Si sample in Figure 4.16. Silicon peaks are present in the XPS spectrum along with an O peak, which shows the likelihood of Si oxide formation. The Si and O concentrations on the surface are 10.4 and 18.4 at%, respectively, which are close to the stoichiometric ratio for Si and O in SiO_2. However, the source of O may be contamination on the surface, along with N and C. From XPS results it appears that diffusion rate of Ti at room temperature is lower than Si, since no Ti was detected on the Au surface of the as deposited sample.

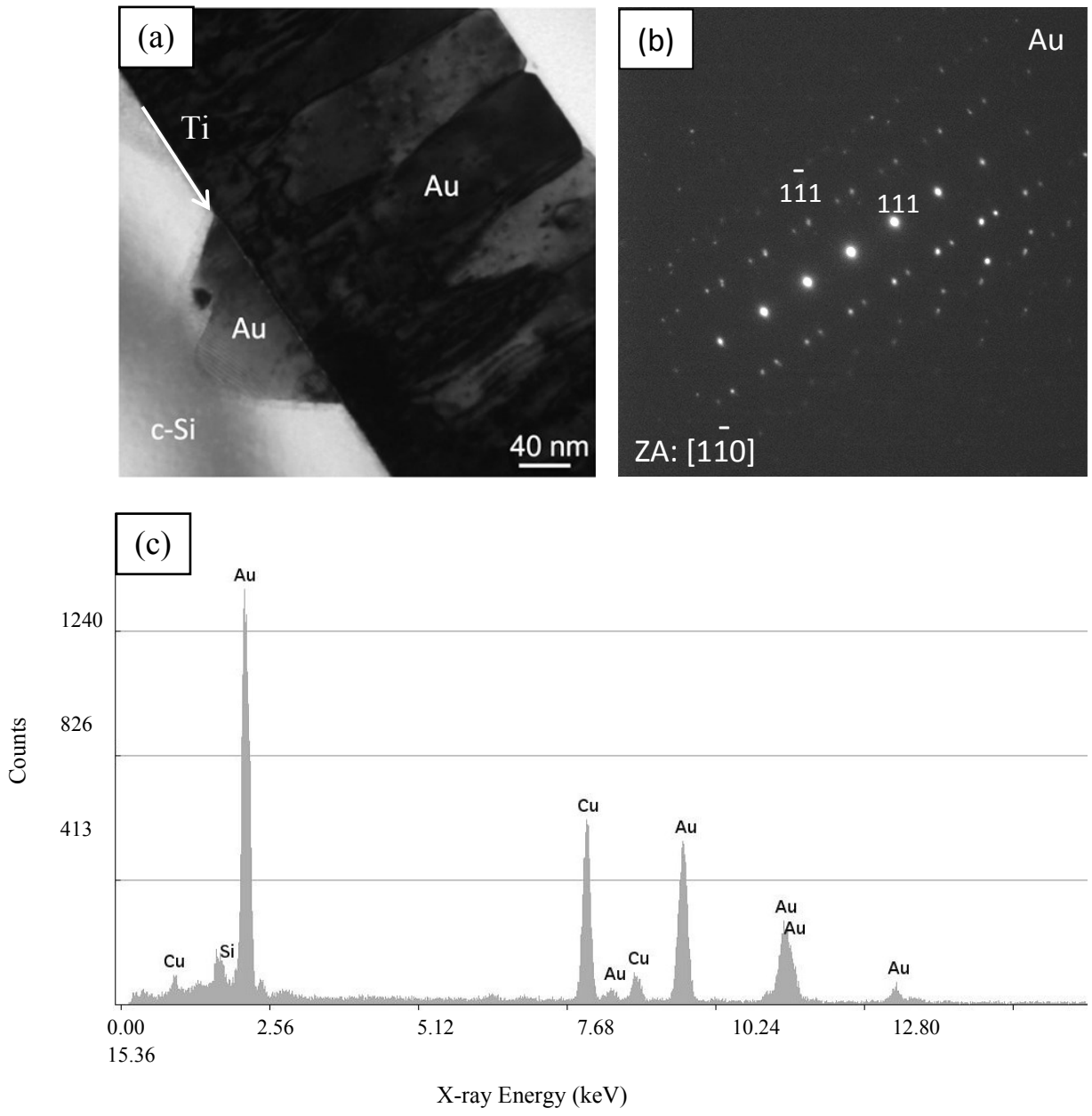


Figure 4.14. (a) TEM BF image, (b) SAD pattern and (c) EDX spectrum from the crater area of a Au/Ti/c-Si sample annealed at 350°C for 30 min.

The formation of Si oxide is in agreement with the observation of other researchers. Hiraki [106] has reported that when a Si substrate is covered with an evaporated Au layer and heated at temperatures well below the Au-Si eutectic point (363°C) in an oxidizing atmosphere, silicon atoms migrate through the gold film and accumulate on

its outside surface. These silicon atoms are oxidized and form a SiO_2 layer. The presence of this layer is also detected from the color change of the surface. The thickness of the oxide layer increases with increasing temperature or time of the heat treatment. This study point outs, that at low temperatures (150-250°C), both the dislodgement of Si atoms from the tightly bound covalent crystal and the formation of SiO_2 occur.

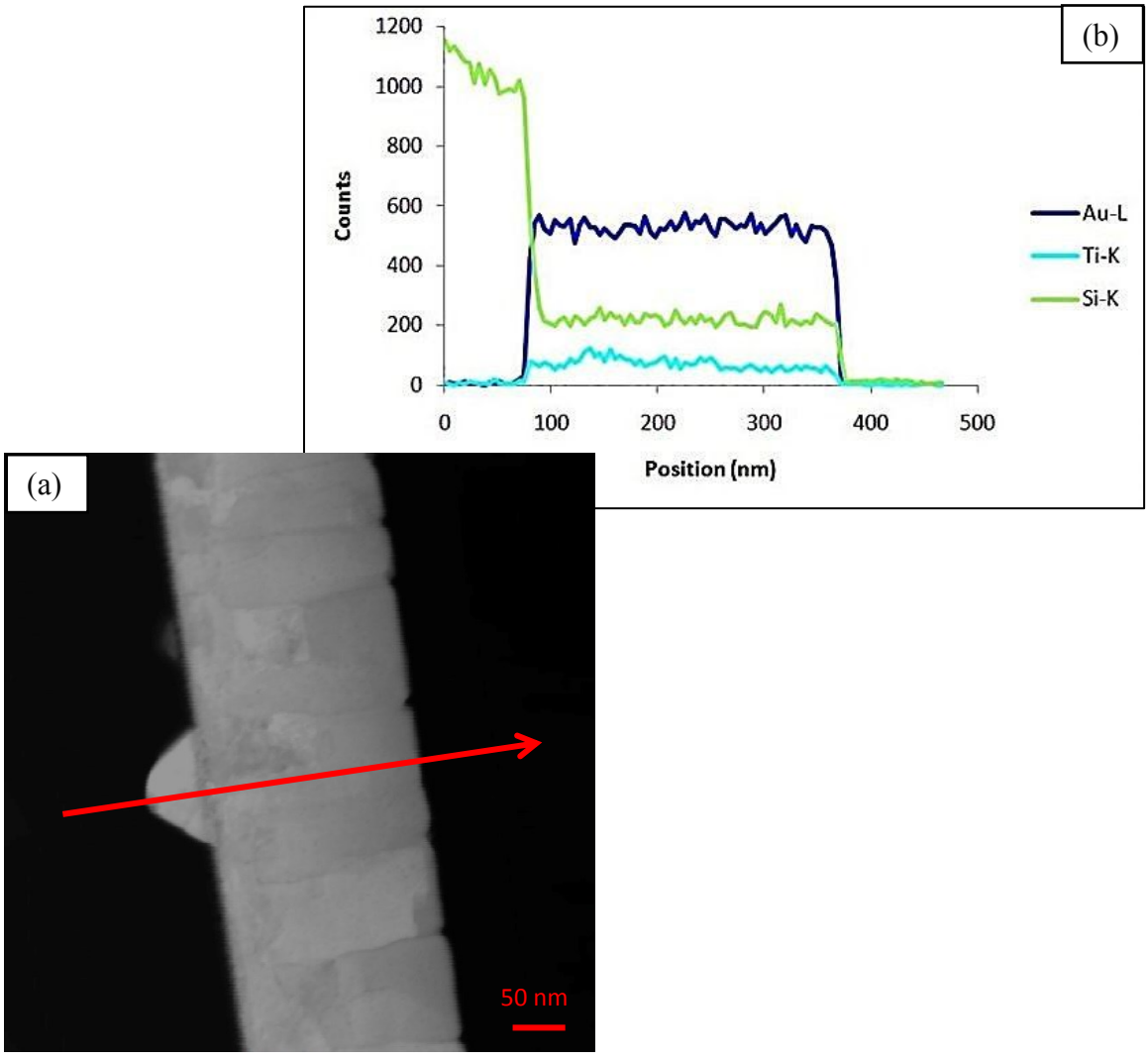


Figure 4.15. (a) STEM high angle annular dark-field (HAADF) image of a cross section specimen of the Au/Ti/c-Si sample annealed at 350°C for 30 min. (b) X-ray line scan across the interfacial region (indicated by the arrow in (a)).

In the process of oxide layer formation, Si atoms dissolve from the substrate and diffuse through the Au layer. If an oxide layer is present at the Au/c-Si interface, the dissolution of Si from the substrate can be prevented. The thickness of interface oxide layer is not always uniform which can lead to non-uniform oxide formation on the Au surface (Figure 4.17(a)) [106].

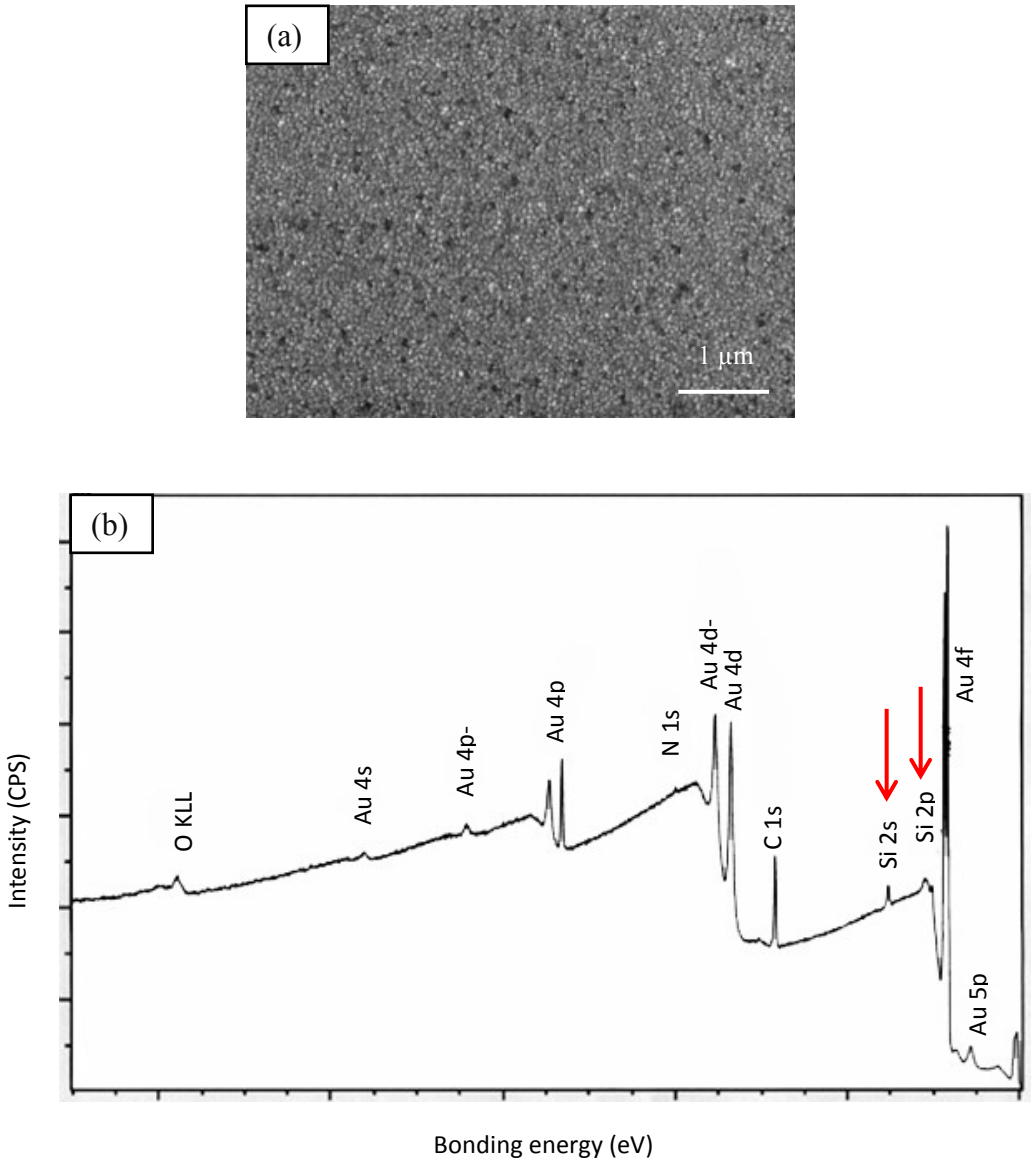


Figure 4.16. (a) SEM image from an as deposited Au surface for the Au/Ti/c-Si sample and (b) XPS spectrum from the Au surface showing the presence of Si on the Au surface. No Ti was detected on the surface.

In order to determine whether Si diffuses through the grain boundaries to the surface or through the Au grains, an X-ray line scan was done across a grain boundary as shown in Figure 4.18. The change in the Si signal was not significant, which may be due to either poor lateral resolution of the TEM or similar concentration of Si in the grain boundaries compared to within the Au grains.

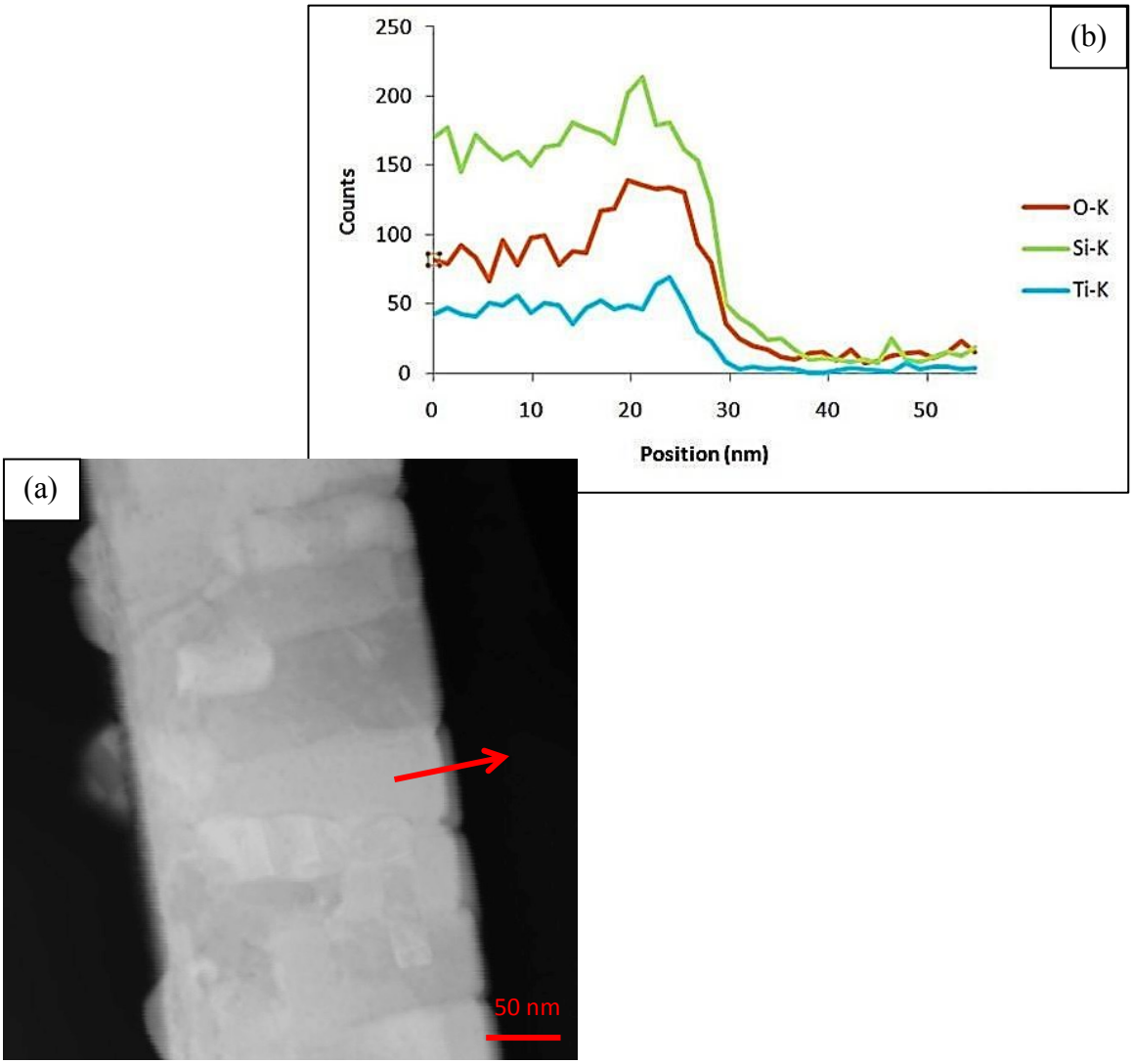


Figure 4.17. (a) STEM HAADF image from a cross section of the Au/Ti/c-Si sample annealed at 350°C for 30 min. (b) X-ray line scan across the oxide layer in (a) (indicated by the arrow).

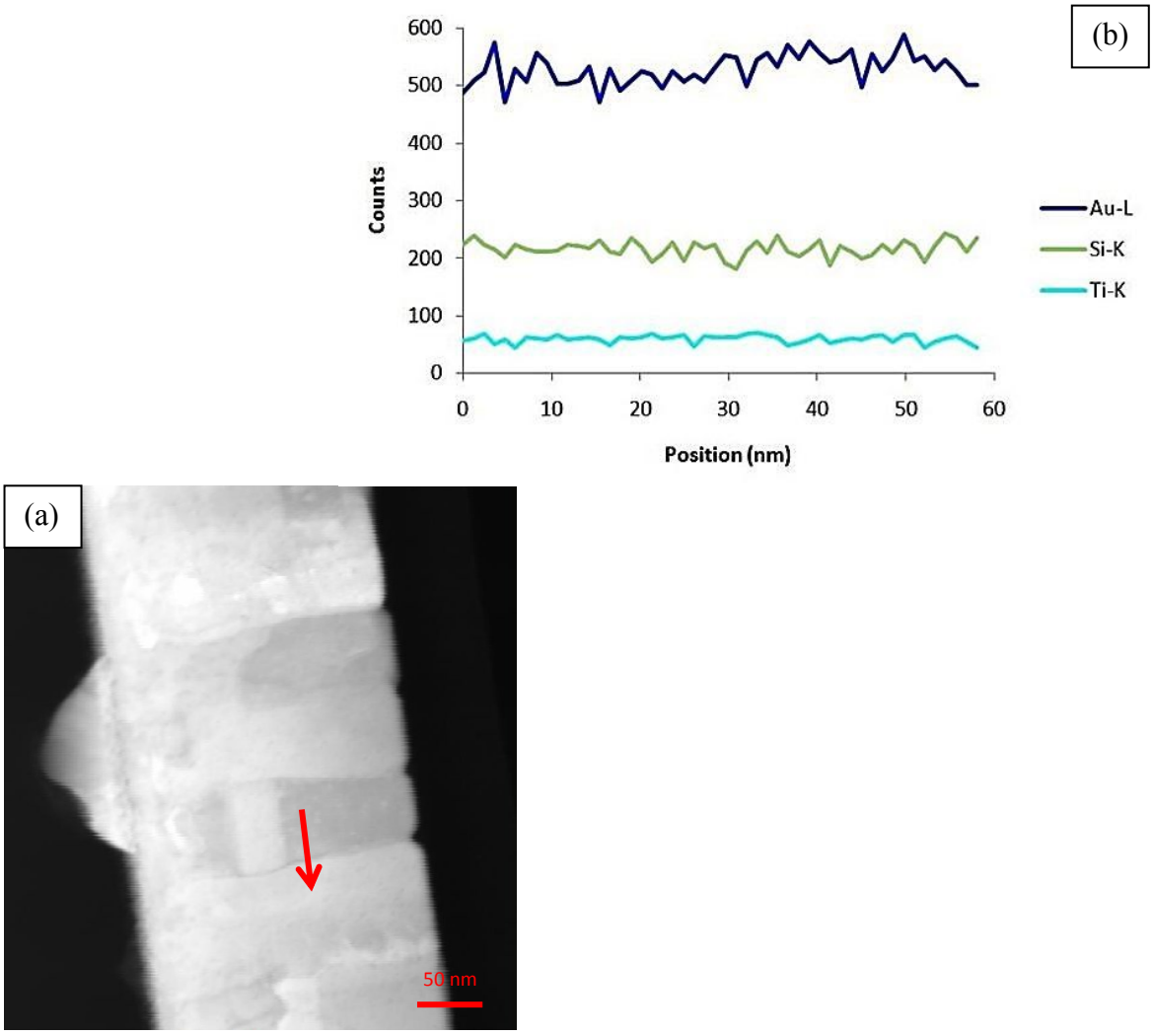


Figure 4.18. (a) STEM HAADF image of a cross section specimen from the Au/Ti/c-Si sample annealed at 350°C for 30 min. (b) X-ray line scan across a grain boundary (indicated by the arrow in (a)).

4.3. Summary

At room temperature, interdiffusion was observed in the Au and amorphous Si diffusion couples (Au/a-Si), but was not observed in the Au and crystalline Si diffusion couples (Au/Ti/c-Si). At an annealing temperature of 350°C, interdiffusion in the Au/a-Si diffusion couples was accelerated compared with Au/Ti/c-Si due to higher diffusion rates in a-Si. The activation energy for interdiffusion was estimated to be 60–69 kJ/mol.

For the Au/Ti/c-Si couples, annealing at 350°C resulted in the formation of faceted craters along the Si {111} planes in the substrate. Both Si and Ti were detected on the Au surface using XPS. Silicon is a fast diffuser and it can diffuse to the Au surface even at room temperature; however, Ti appears to have a lower diffusion rate.

Chapter 5

Small Sample Bonding Results

Chapter 5 - Small Sample Bonding Results

The objective of this chapter is to perform Au-Si wafer bonding on a small scale in order to be able to optimize bonding parameters and use different bonding configurations. These conditions can then be applied to full wafer bonding. Both eutectic and solid state bonding are performed and the results are compared in this chapter.

5.1. Au-Si eutectic bonding

5.1.1. a-Si

Reliable MEMS fabrication requires thin conductive films, good adhesion to the substrates and optimal thermal stability up to post-metallization processing temperatures. Diffusion to the active areas should be minimized. In order to meet these requirements, an intermediate layer is needed as a diffusion barrier [107] and to promote adhesion. In order to sputter Au on Si, the use of TiW as a barrier has shown to be successful [108]. Therefore, the initial wafer stack used for bonding, provided by Micralyne, was as follows:

Au (0.8 µm)/ TiW (0.2 µm)/ Si wafer

a-Si (0.8 µm)/ Si wafer

As mentioned in Chapter 3, an additional Au layer (2.63 µm) was deposited by electrodeposition. An SEM cross section image of the cleaved sample after Au electrodeposition is shown in Figure 5.1.

As explained in Section 3.2 in Chapter 3 (Table 3.3), 16 bonding experiments were performed to compare the effect of bonding temperature, bonding time, bonding pressure and bonding atmosphere. Table 5.1 shows the SAM results obtained for these samples. In the majority of the samples, cracks were observed and are one of the reasons for the low shear strengths obtained. There are several possible reasons for

the appearance of cracks, i.e., high bonding pressure, high film stress, etc. Turner et al. [109] reported that if there is sufficient residual stress following bonding the wafers may delaminate. In addition, the strain energy release rate increases with crack length suggesting that if a crack initiates it will propagate unstably and the wafers will delaminate completely. In most cases, additional samples bonded under the same bonding conditions indicated different bonding results and weak repeatability. Another issue with bonding was the formation of partial bonds in most of the samples which will be discussed.

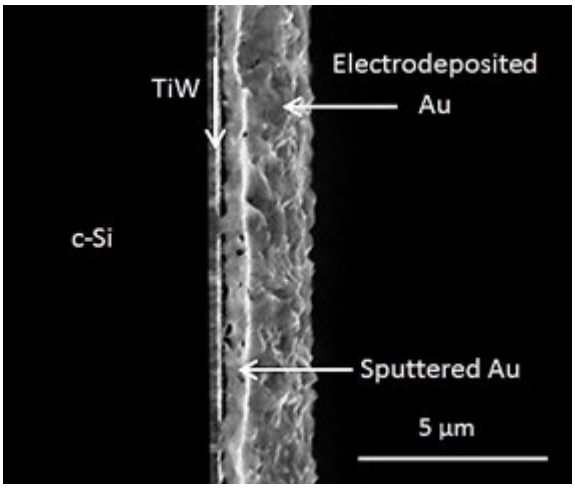
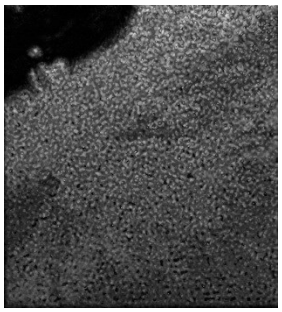
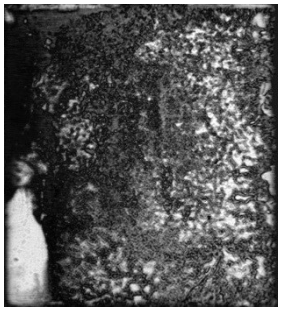
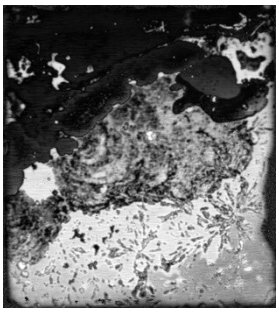
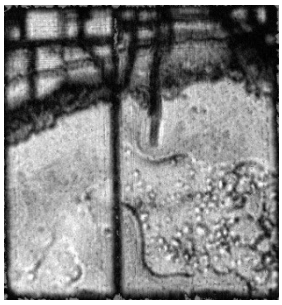
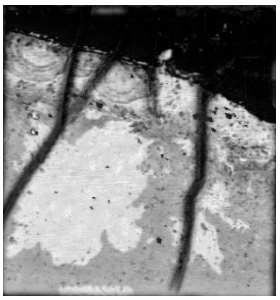
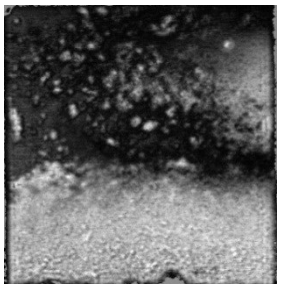
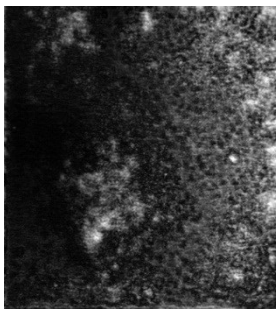


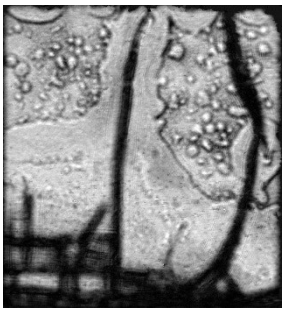
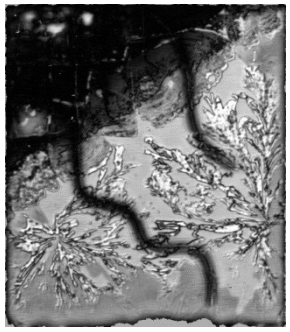
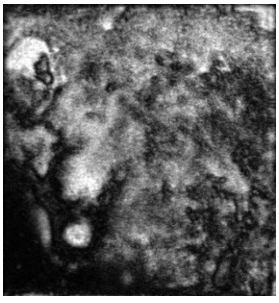
Figure 5.1. SEM BSE cleaved cross section image of Si/TiW/sputtered Au/electrodeposited Au layers.

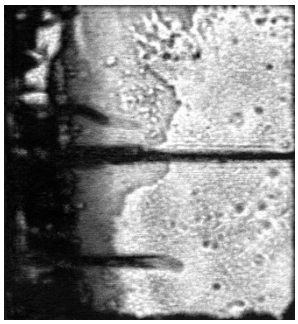
Table 5.1. SAM images of bonded samples at 16 different bonding conditions.

Sample	T (°C)	T (min)	P (MPa)	Atmosphere (MPa)	SAM Image
1	400	20	0.0133	2×10^{-8} Vacuum	
2	400	20	0.0133	1×10^{-3} Nitrogen	

Sample	T (°C)	T (min)	P (MPa)	Atmosphere (MPa)	SAM Image
3	400	20	0.133	2×10^{-8} Vacuum	
4	400	20	0.133	1×10^{-3} Nitrogen	
5	400	40	0.0133	2×10^{-8} Vacuum	
6	400	40	0.0133	1×10^{-3} Nitrogen	

Sample	T (°C)	T (min)	P (MPa)	Atmosphere (MPa)	SAM Image
7	400	40	0.133	2×10^{-8} Vacuum	
8	400	40	0.133	1×10^{-3} Nitrogen	
9	425	20	0.0133	2×10^{-8} Vacuum	
10	425	20	0.0133	1×10^{-3} Nitrogen	

Sample	T (°C)	T (min)	P (MPa)	Atmosphere (MPa)	SAM Image
11	425	20	0.133	2×10^{-8} Vacuum	
12	425	20	0.133	1×10^{-3} Nitrogen	
13	425	40	0.0133	2×10^{-8} Vacuum	
14	425	40	0.0133	1×10^{-3} Nitrogen	

Sample	T (°C)	T (min)	P (MPa)	Atmosphere (MPa)	SAM Image
15	425	40	0.133	2×10^{-8} Vacuum	
16	425	40	0.133	1×10^{-3} Nitrogen	

As mentioned in Chapter 3, the SAM works in reflection mode, therefore the bright regions in the SAM images are indicative of reflection from interfaces and thus would be expected to represent unbonded areas. The darker regions represent areas with little or no reflection of sound waves and would be expected to be well bonded.

5.1.1.1. Bonding pressure

Pressure was one of the parameters which could be related to the unbonded area and cracks. If the pressure was not high enough, there was insufficient contact between the wafers for interdiffusion; however, if the pressure was too high, crack formation could be induced in the wafers. To study the effect of pressure on the bonded area, three different samples were bonded at three different pressures of 0.0133, 0.133 and 0.4

MPa and the rest of the parameters were fixed at T= 425°C, t= 40 min and ambient pressure of 1×10^{-3} MPa. The highest temperature and time were chosen to ensure adequate interdiffusion. SAM results are shown in Table 5.2. Increasing the pressure not only resulted in less bonded area but also in the formation of more cracks within the samples. Increasing the bonding pressure also resulted in more spill out of the melt. The best results in terms of pressure were obtained using 0.0133 MPa. Preliminary experiments showed that pressures lower than 0.0133 MPa did not produce bonds with adequate robustness. As a result, the reason for partial bonding was not due to low bonding pressure. Spill out may be one of the reasons for the formation of partial bonds, since an adequate amount of melt would not be available for complete bond formation.

A possible reason for spill out is pressure non-uniformity on the small samples, which can result in spill out from some corners. There may be some surface contamination present on the samples prior to bonding as well.

Table 5.2. SAM results for samples bonded at three different bonding pressures (T= 425°C, t= 40 min and ambient pressure of 1×10^{-3} MPa N_2)

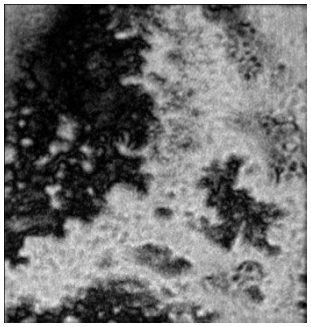
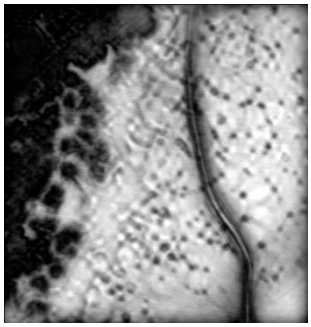
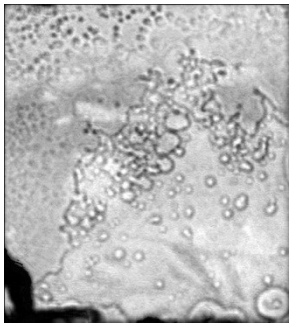
Pressure (MPa)	SAM	Bonded area (%)
0.0133		87%
0.133		5%
0.4		22%

5.1.1.2 Bonding temperature

Bonding temperature is one of the important parameters affecting bond reliability and uniformity. The principle of eutectic bonding is based on the diffusion of Au and Si. During the diffusion process, a eutectic alloy forms across the interface at appropriate temperatures. It has been found that increasing the bonding temperature will increase the amount of diffusion and the solubility of Au into the silicon substrate. Therefore, a higher processing temperature is preferable for eutectic bonding. In addition, at higher temperatures, more Au atoms are available to diffuse into the Si substrate. As a result, the layer of Au-Si alloy formed will be thicker and a strong eutectic bond is expected [72]. However, a too high bonding temperature can lead to significant diffusion of the Au into the Si. Therefore, the bond will be less reliable and it will degrade the Si device. A high temperature also increases the risk of the spill out of the melt. In order to observe the effect of temperature on the bond coverage and strength, bonding was performed at two different temperatures of 400°C and 425°C. The other bonding parameters were kept fixed as t= 30 min, P= 0.0133 MPa and a chamber pressure of 2×10^{-8} MPa. The reason for choosing these values was that a bonding time of more than 30 min is not desirable in industry, due to potential thermal damage to devices. Also, previous work (Table 5.2) showed that a bonding pressure of 0.0133 MPa resulted in the formation of bonds without cracks and desirable bond coverage. Each bonding test was duplicated to measure the bond yield. Table 5.3 shows the SAM results for bonded a-Si samples.

The results were not consistent. Cracking and partial bonding issues were decreased, but still existed. Samples were diced into 4 quarters. During dicing, the parts which appear bright in SAM images detached and the rest of the samples survived dicing. SEM imaging was performed on the plan view orientation of the detached parts, as well as polished cross sections of the pieces that remained attached. Shear testing was done on the attached pieces.

Table 5.3. SAM results for a-Si samples bonded at 400 and 425°C (t= 30 min, P= 0.0133 MPa and bonder pressure of 2×10^{-8} MPa)

T=400°C	 Sample 1 Bonded area: 42% Shear strength: 14 MPa	 Sample 2 Bonded area: 32% Shear strength: 10 MPa
T=425°C	 Sample 3 Bonded area: 56% Shear strength: 21 MPa	 Sample 4 Bonded area: 2% Shear strength: 0 MPa

Sample 1 (a-Si bonded at 400°C) mostly stayed attached after dicing, except for the bottom right corner. For sample 6 (the duplicate of sample 5), the right half of the sample was detached during dicing. Polished cross sections of samples 1 and 2 are shown in Figure 5.2 and Figure 5.3, respectively. The cross section images are taken from the regions shown by the arrows in Figure 5.2(a) ad 5.3(a). The cross section microstructures are similar between these two samples.

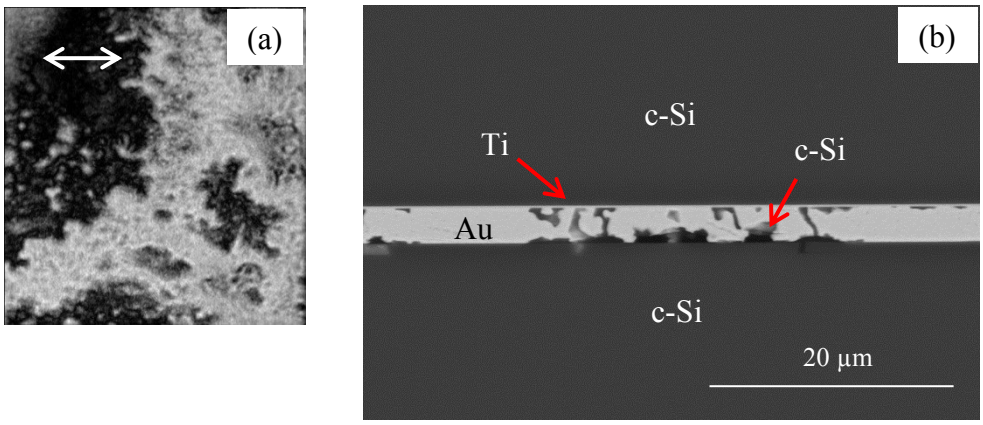


Figure 5.2. Cross section BSE image (b) of the region indicated by the arrow in SAM image (a) for an a-Si sample bonded at 400°C for 30 min (sample 1).

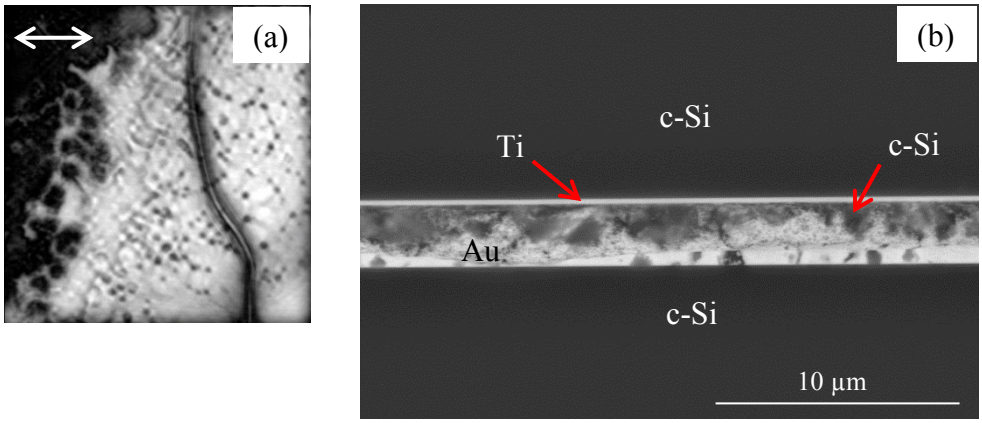


Figure 5.3. Cross section BSE image (b) of the region indicated by the arrow in SAM image (a) for an a-Si sample bonded at 400°C for 30 min (sample 2).

Figure 5.4(a) and Figure 5.4(b) are plan view SEM SE images from the Au side of the detached pieces of sample 2 and Figure 5.4(c) and 5.4(d) are SEM SE images from the Si side of the same sample. Pressure non-uniformity during bonding is apparent in Figure 5.4(a) as some parts were not in contact during bonding. EDX area analysis of the surface from the Au side (Figure 5.4(b)) shows that it is mostly Au with about 6 wt% Si. For the Si side, delamination and cracking of the a-Si layer occurred (Figure 5.4(c)). Some of the Au layer remained attached to the Si side after the pieces delaminated

during dicing; these are the bright regions shown by the square in Figure 5.4(c). A higher magnification image of one of these Au regions (Figure 5.4(d)) revealed mostly Au-rich regions and scattered areas of Si (dark contrast).

A SAM image and cross section SEM BSE images from sample 3 (a-Si bonded at 425°C) are shown in Figure 5.5. The cross section images (Figure 5.5(b) and (c)) are taken from the region shown by the arrow in the SAM image (Figure 5.5(a)). These show a coarser microstructure than the microstructure obtained from the lower temperature anneals (Figure 5.2(b) and 5.3(b)). The reason is that, as mentioned in Chapter 4, increasing temperature will enhance interdiffusion, crystallization and growth of a-Si. The region shown by the black rectangle in Figure 5.5(a) was detached during dicing. Plan view images of the Au side are shown in Figure 5.5(c) and 5.5(d). Delamination of the Au layer from the Si wafer is apparent in Figure 5.5(c) as shown by the black square. EDX analysis of the entire surface area in Figure 5.5(d) showed a composition of 65 wt% Au and 35 wt% Si. The bright areas are Au and the dark spots are Si. Some of the detected Si comes from the substrate Si.

Sample 4 (duplicate of sample 3) did not form any bonds and the pieces detached instantly after the samples were removed from the bonder. There was no observable reaction at the surface.

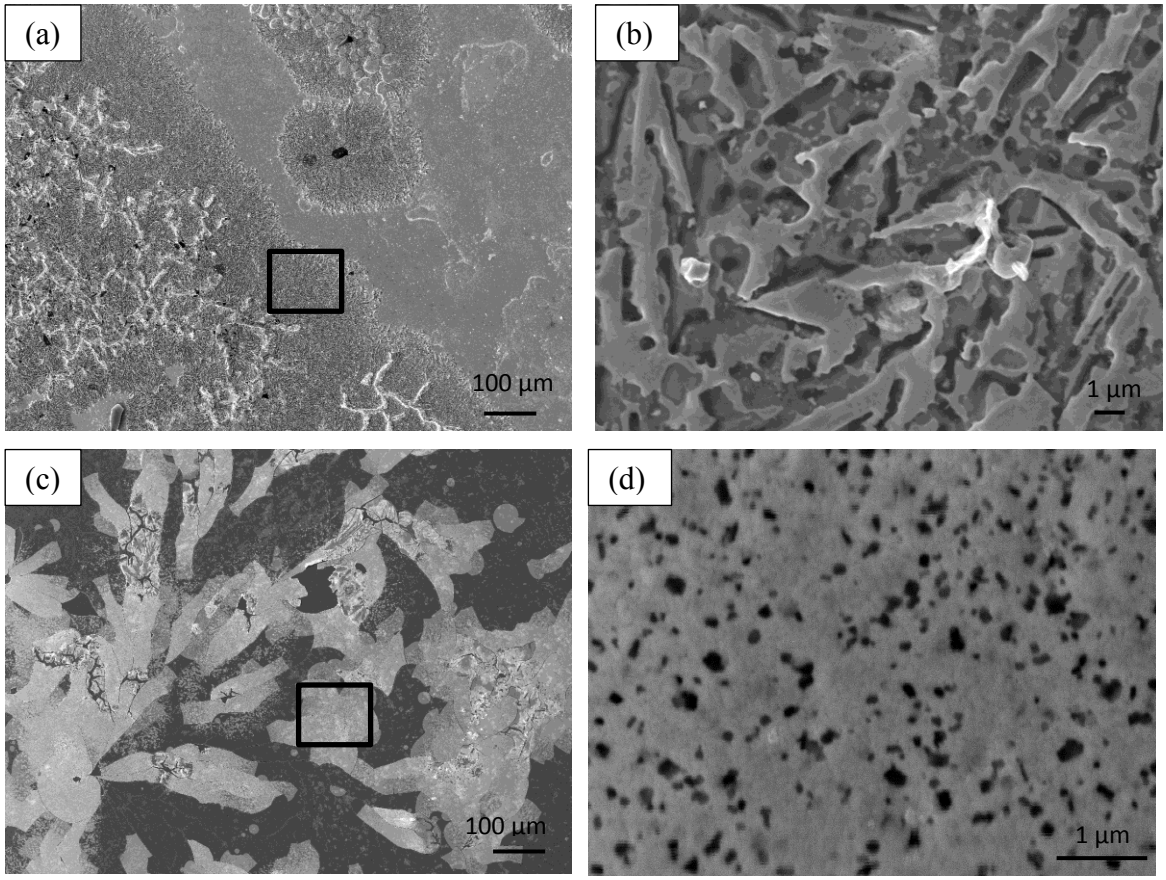


Figure 5.4. SEM SE plan view images of sample 2 (a-Si bonded at 400°C) pieces after dicing. The Au side: (a) low magnification image and (b) high magnification of the area indicated in (a). The Si side: (c) low magnification image and (d) high magnification of the area indicated in (c).

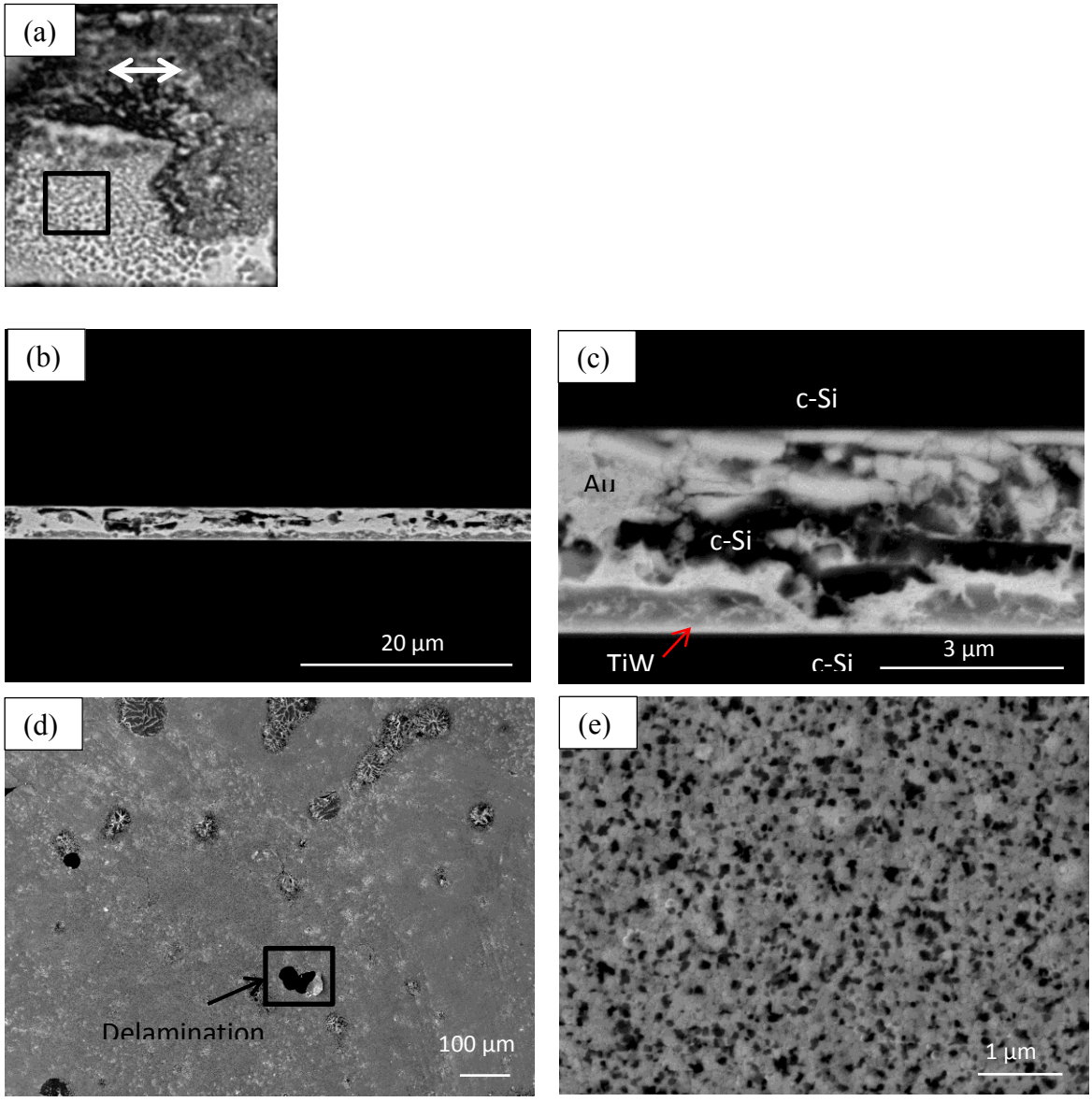


Figure 5.5. Images taken from the Au side of sample 3 (a-Si bonded at 425°C). (a) SAM image, (b) low magnification and (c) high magnification SEM BSE cross section images from the region indicated by the arrow in (a). (d) Low magnification and (e) high magnification SE plan view images of the detached pieces from the black square shown in (a).

Plasma enhanced chemical vapor deposition (PECVD) is known to introduce high residual stresses in a-Si layers, which is likely the reason for a-Si delamination and cracking in this work. Low pressure chemical vapor deposition (LPCVD) was used instead to improve the adhesion of a-Si to c-Si and to reduce the stress of the

deposited layer. Atomic force microscopy (AFM) imaging and roughness measurements were performed on a-Si layers deposited by PECVD and LPCVD to compare the roughness of layers. The results are shown in Figure 5.6. AFM plan view images show that PECVD a-Si (Figure 5.6(a)) has a coarser microstructure than LPCVD a-Si (Figure 5.6(b)). The roughness is also compared in Figure 5.7(a) (PECVD) and 5.7(b) (LPCVD) and the root mean square (RMS) values were measured as 3.78 nm and 0.266 nm, respectively. As a result, a-Si deposited by LPCVD method is more favorable in terms of roughness for wafer bonding. The next step is to evaluate layer stress.

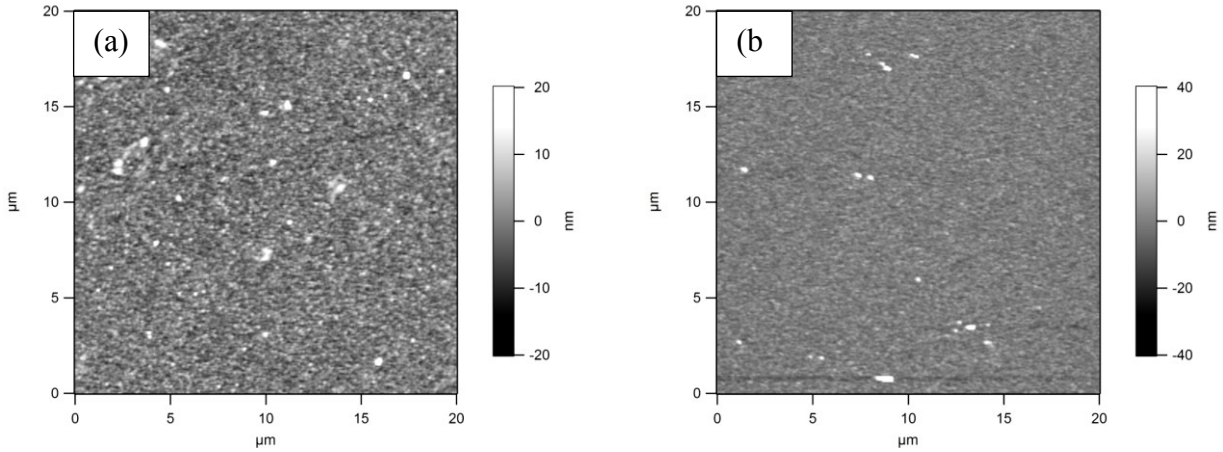


Figure 5.6. AFM plan view images of a-Si layer deposited by (a) PECVD and (b) LPCVD methods.

One of the non-destructive methods to measure a-Si stress is Raman spectroscopy. The basics of this method have been explained in Chapter 3. In the absence of stress, the Raman shift for c-Si will be ω_0 = 521 cm^{-1} [110]. The Raman spectrum of a-Si has two distinct bands, at about 150 cm^{-1} and 480 cm^{-1}.

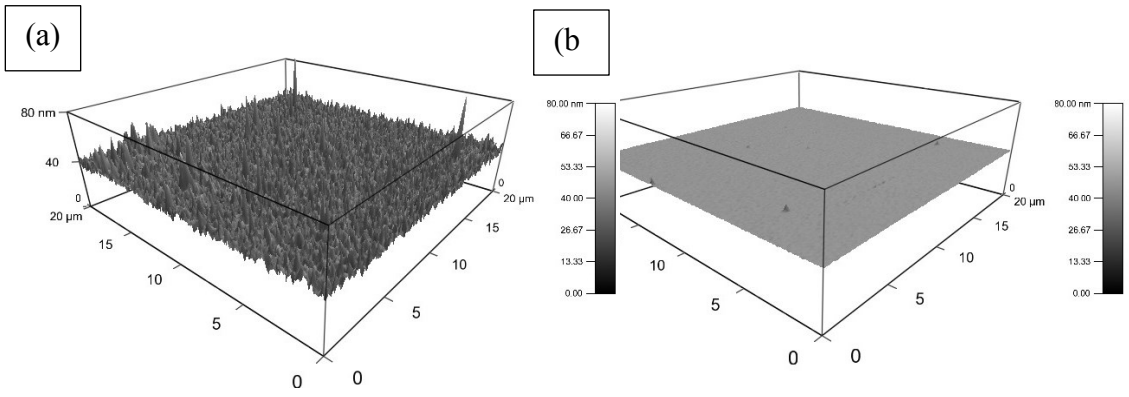


Figure 5.7. AFM surface roughness measurement of a-Si deposited by (a) PECVD and (b) LPCVD methods.

For the case where the stress is assumed to be biaxial (plain stress due to the existence of a thin film), the film stress can be calculated according to Equation (5.1):

$$\sigma\ (MPa) = -250\ \times \Delta\omega_z(cm^{-1}) \qquad (5.1)[111]$$

$\Delta\omega_z$ is the shift in the peak due to stress and σ is the stress value. Therefore, the larger the peak shift from the standard peak position, the higher is the stress level of the film. Tensile stress shifts the silicon Raman peak to lower frequencies, while compressive stress shifts the Raman peak to higher frequencies. Raman spectra were obtained from both PECVD and LPCVD deposited films and the c-Si sample as a reference (Figure 5.8). The average spectrum for ten different points tested on each sample has been plotted.

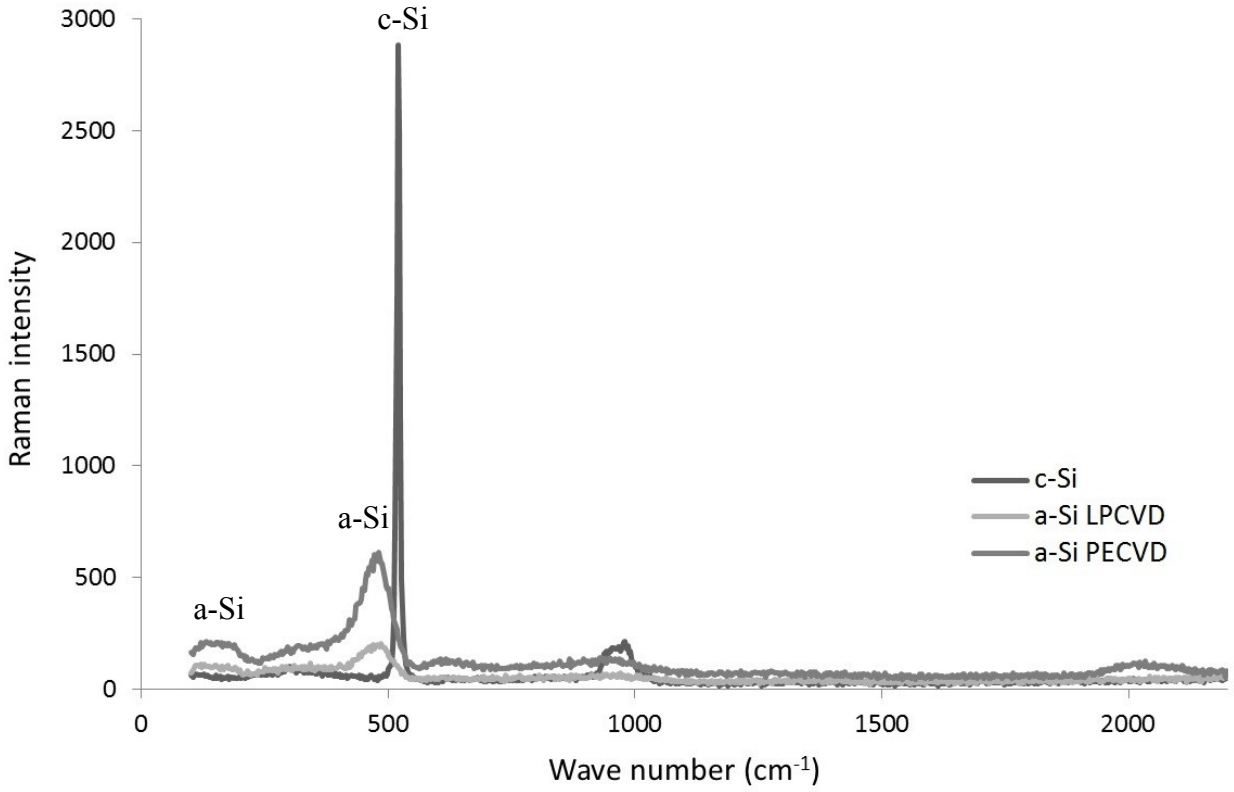


Figure 5.8. Raman spectra obtained from c-Si, a-Si deposited by LPCVD and a-Si deposited by PECVD. Laser power: 4.32 mW; exposure time: 10 s, laser wavelength: 514 nm.

The Lorentz equation (Eq. 5.2) was fitted using MATLAB software to the spectra to determine the peak values of each spectrum as accurately as possible [110].

$$I_L(\omega) = I_{L_0}/1 + \left(\omega - \frac{\omega_0}{\Gamma}\right)^2 \quad (5.2)$$

where

ω_0 is the peak position, Γ is the FWHM (full width at half maximum) and I_{L_0} is the maximum peak amplitude..

The peak values were calculated and are given as follows:

c-Si: 520.8 cm^{-1} a-Si LPCVD: 470.7 cm^{-1} a-Si PECVD: 467.8 cm^{-1}

Raman spectra of a-Si show two distinct peaks, at about 150 cm^{-1} and 480 cm^{-1}, associated with the transverse acoustic (TA) and the transverse optic (TO) vibrational modes, respectively.

Some of the features in Raman spectrum are highly sensitive to a-Si structural properties. As an example, the width of TO peak is related to the root-mean-square bond-angle variation Δθ in the amorphous network. As Δθ decreases, the TA/TO intensity ratio decreases and the TO peak frequency increases. Δθ is calculated as 12° and 13° for LPCVD and PECVD a-Si, respectively.

Using Eq. 5.1, the values for the a-Si layer stress can be estimated using the 480 cm^{-1} a-Si peak [112] as the reference peak. However, the peak locations obtained in this work for a-Si deposited by both LPCVD and PECVD are shifted to lower frequencies which resulted in higher calculated stresses than expected (bulking and delamination could happen at these levels of stress). This abnormal shift can be related to several parameters such as surface contamination and existence of Si oxide on the surface.

σ_{LPCVD}= -250 × (480 - 470.7) = -2325 MPa

σ_{PECVD}= -250× (480 - 467.8) = -3050 MPa

As expected, a-Si deposited by PECVD is more stressed than the LPCVD layer and the stress in both cases is compressive. LPCVD amorphous Si was used for the rest of the bonding experiments to reduce the amount of cracking and delamination of the a-Si layer and to increase the bond strength.

The other bonding issue encountered was non-uniformity of pressure. The first attempt to make the pressure uniform was to use a four sample configuration on the chuck as shown in Figure 5.9.

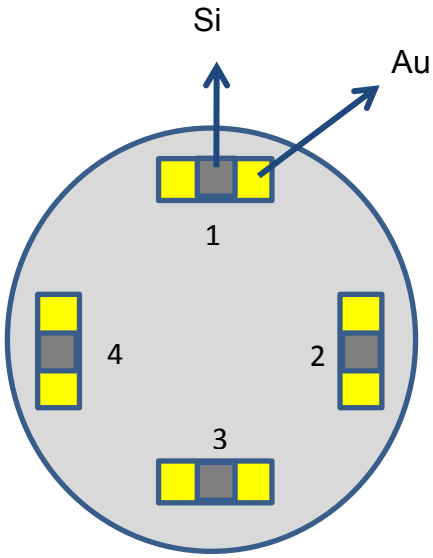
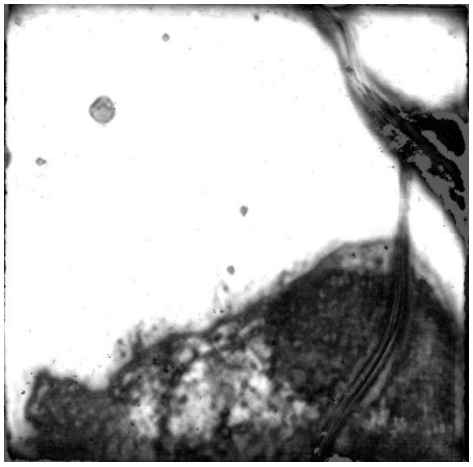
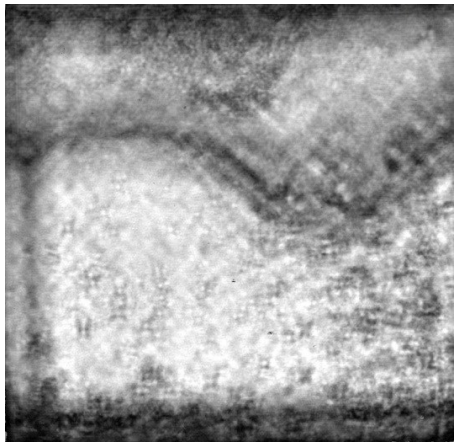


Figure 5.9. Four sample configuration used on the chuck in order to improve pressure uniformity.

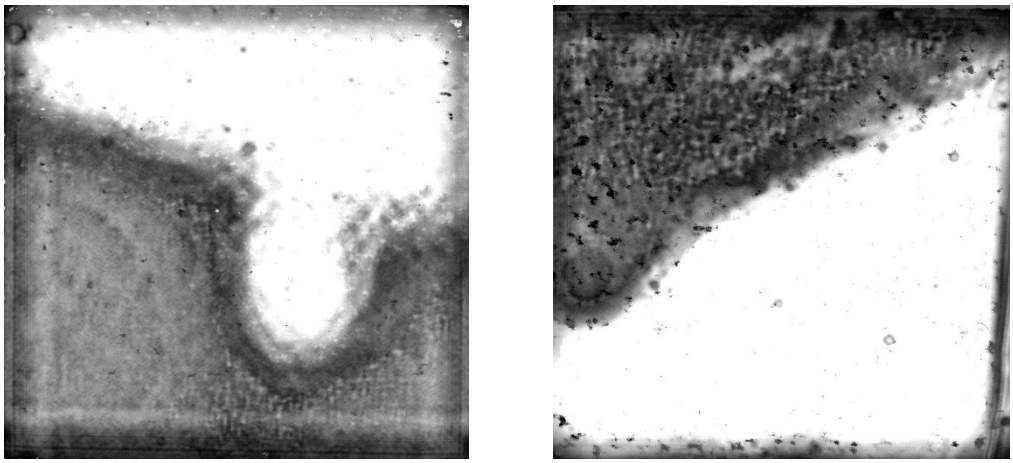
SAM results from the four samples preheated at 350° for 20 min and bonded at 400°C for 30 min are illustrated in Figure 5.10. Similar to previous results, all samples showed partial bonding. Bonding non-uniformity appears to be due to a lack of flatness of the bonder chucks.



Sample 1



Sample 2



Sample 3 Sample 4

Figure 5.10. SAM results for the four sample configuration (LPCVD a-Si) shown in Figure 5.9.

To improve pressure uniformity across the chuck using a minimum number of samples, five samples were placed on the chuck as shown in Figure 5.11. SAM results for the five samples preheated at 350°C for 20 min and bonded at 400°C for 30 min are shown in Figure 5.12.

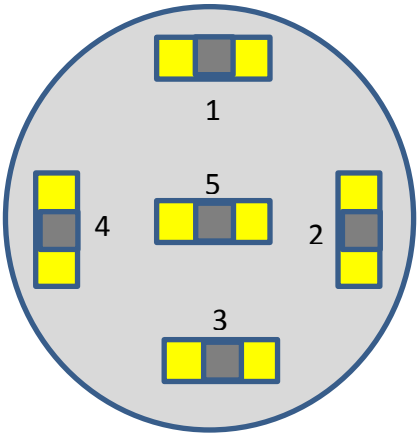
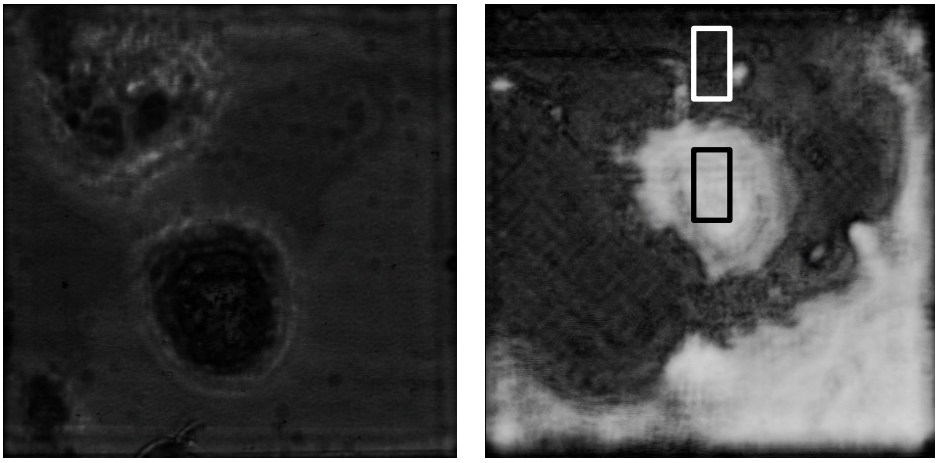


Figure 5.11. Five sample configuration used on the chuck to improve pressure uniformity.

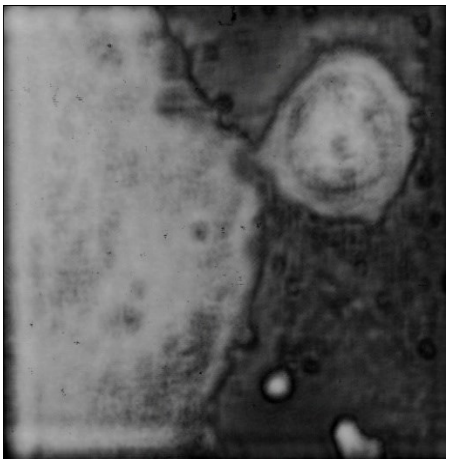
Sample 1 in Figure 5.12 appears to be completely bonded, while samples 2, 3, 4 and 5 show what appear to be approximately 34%, 50%, 53% and 92% unbonded areas

(bright regions), respectively. The only sample which detached during cleaving was sample 5 which was in the middle of the chuck.

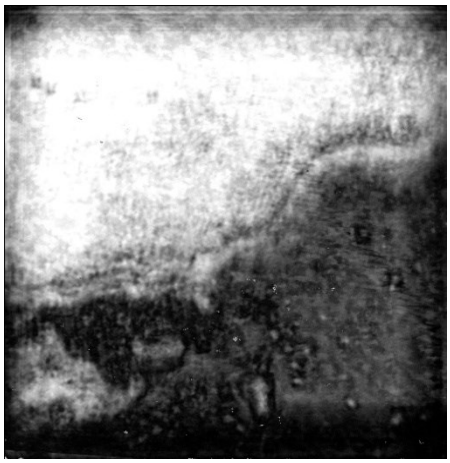
SEM cleaved cross section samples were prepared from sample 2 in Figure 5.12, from the regions denoted by the black and white rectangles. It should be noted that the "unbonded" portions of the sample did not delaminate during cleaving, which indicates that a bond had actually formed. The microstructure of the "well bonded" region (white rectangle) consists of regions of bright and dark contrast (Figure 5.13a). The dark regions are essentially all Si and the bright regions are essentially all Au. The Si regions appear to be crystalline (confirmed by TEM in subsequent paragraphs). The so-called "unbonded" region (black rectangle) is, in fact, bonded, but the microstructure is coarser (Figure 5.13b) relative to the "well bonded" region (Figure 5.13a). The contrast effects in the SAM images (Figure 5.19) can be explained in terms of the different microstructures in Figure 5.20.



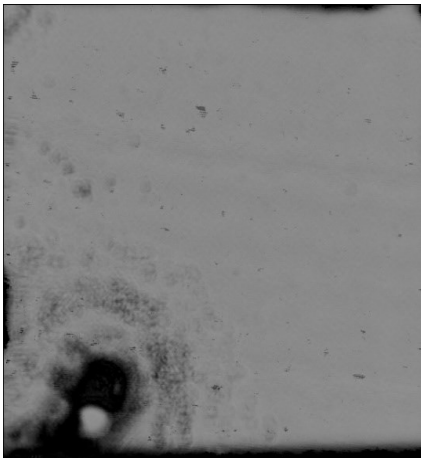
Sample 1 Sample 2



Sample 3



Sample 4



Sample 5

Figure 5.12. SAM results for the a-Si (LPCVD) eutectic bonded sample with the five sample configuration.

The bonded region is shown schematically in Figure 5.14. There are two types of structures at the bonded interface when viewed right-to-left: (1) c-Si/Au/Si/TiW/c-Si and (2) c-Si/Au/TiW/c-Si. There is an additional interface for the first structure, which means that more of the sound waves will be reflected back and, as such, these regions will appear brighter in a SAM image. Comparison of the images in Figure 5.13 shows that the “well bonded” regions have a larger fraction of the second structure compared

with the “unbonded” regions. Therefore the “well bonded” regions will appear darker in the SAM images, although both the “well bonded” and “unbonded” regions are indeed bonded. In addition, no void or crater formation was observed for any of the bonded samples; however, solder spill out could not be avoided.

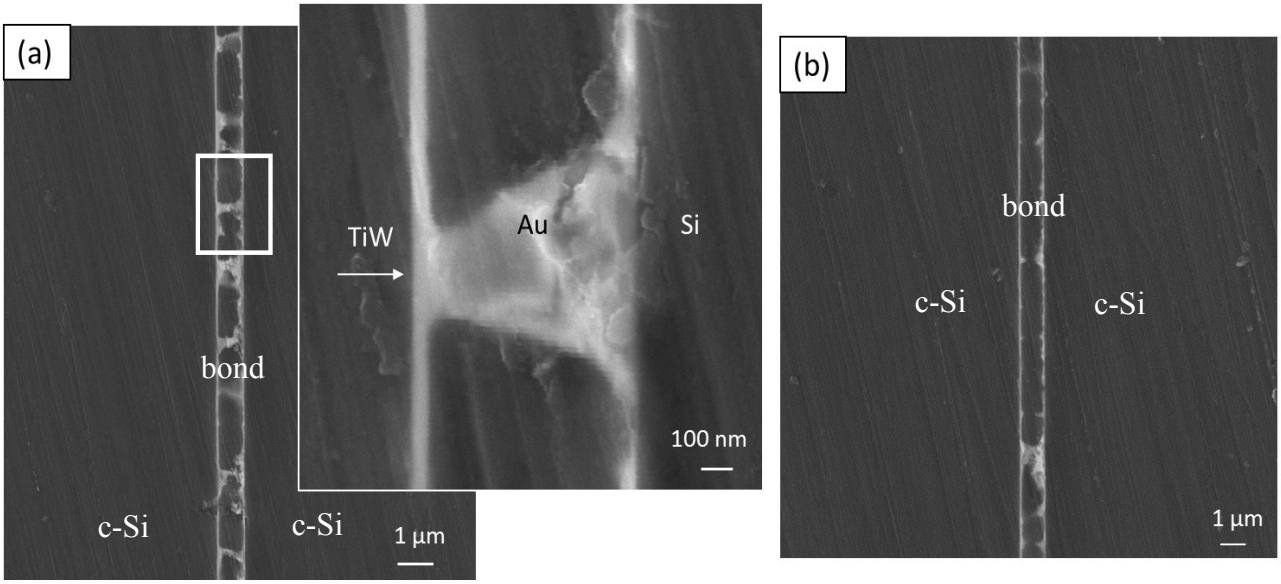


Figure 5.13. SEM SE images of cleaved cross sections of sample 2 in Figure 5.12. (a) Region shown by white rectangle and (b) region shown by black rectangle in Figure 5.12.

Another interesting feature of the bonds is that an Au layer is present on the opposite side of the bond, i.e., it is separated from the TiW adhesion layer by the crystallized Si. This is due to the layer exchange mechanism, which was discussed in Chapter 4, Section 4.1.

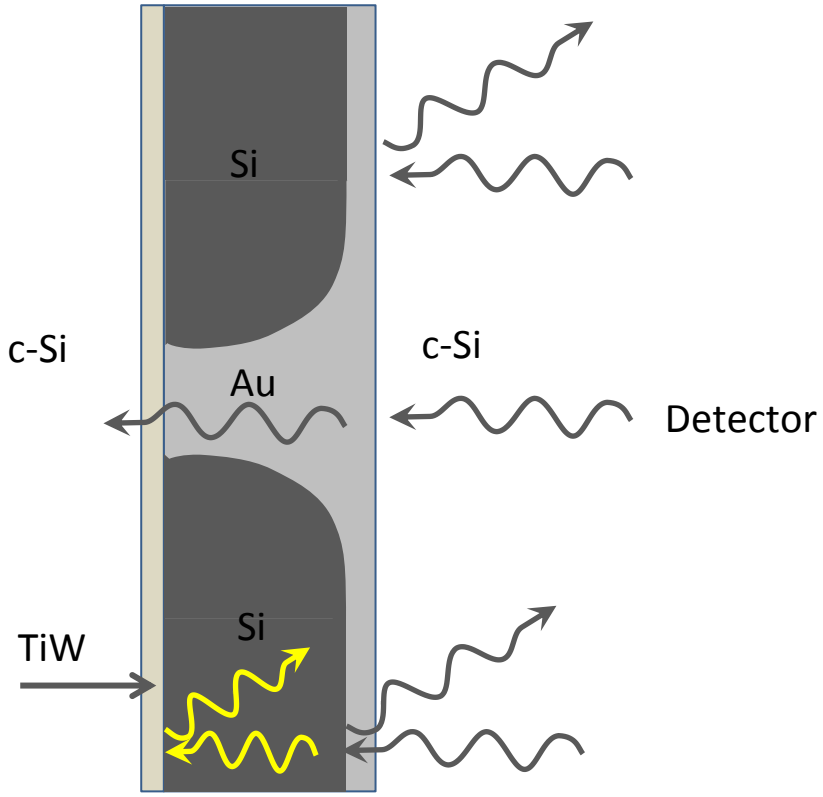
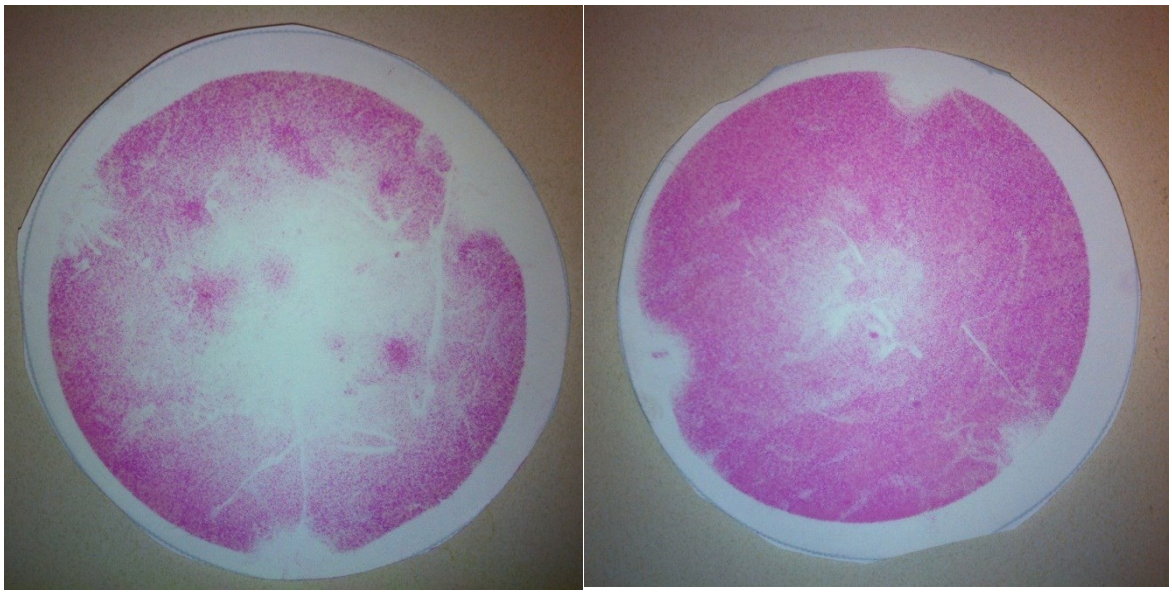


Figure 5.14. Schematic image of bonded interface and sound wave reflection from the Au/c-Si interfaces. The reflections are detected by the detector and therefore areas with more reflections appear bright in SAM images compared with areas with fewer or no reflections.

To optimize the bonds, the issue of partial bonding needed to be solved. The bonder required some modifications in order to improve pressure uniformity. Graphite sheets were used beneath both the upper and lower chuck. In order to test the bonder before and after installing the graphite sheets, pressure paper was employed. Pressure paper is a tactile surface pressure indicating film that shows the pressure distribution and magnitude between any two contacting or impacting surfaces. When placed between two contacting or mating surfaces, this thin plastic film instantaneously and permanently captures the pressure profile by a color change. The color is directly proportional to the amount of force applied. A uniform and consistent pink color

across the pressure paper represents desirable and uniform pressure distribution. The result of the pressure paper test is shown in Figure 5.15. A major difference before and after using graphite sheets is observed in terms of pressure uniformity. Therefore graphite sheets were installed under the upper and lower chucks and kept there for the rest of the bonding experiments. However, the effect of using graphite sheets to achieve pressure uniformity is more pronounced for full wafer bonding; therefore, small sample bonding was not repeated after installing the graphite sheets.



without graphite sheet with graphite sheet

Figure 5.15. Pressure paper test before and after using graphite sheets in the bonder. The image on the right shows more uniform pressure distribution compared with the image on the left with localized high pressure spots. The three white regions on the edges are the locations of the spacers.

Eutectic bonding was repeated with the new bonding conditions (five configuration set-up using graphite sheets in the bonder). SAM results are shown in Fig 5.16. The coarser microstructure areas were calculated as 16%, 40% and 36% from left to right in Figure 5.16, respectively. Spill out could not be avoided in eutectic bonding of small

samples. Large partially bonded areas developed because of spill out, leaving an inadequate amount of melt between the two surfaces to form a complete bond.

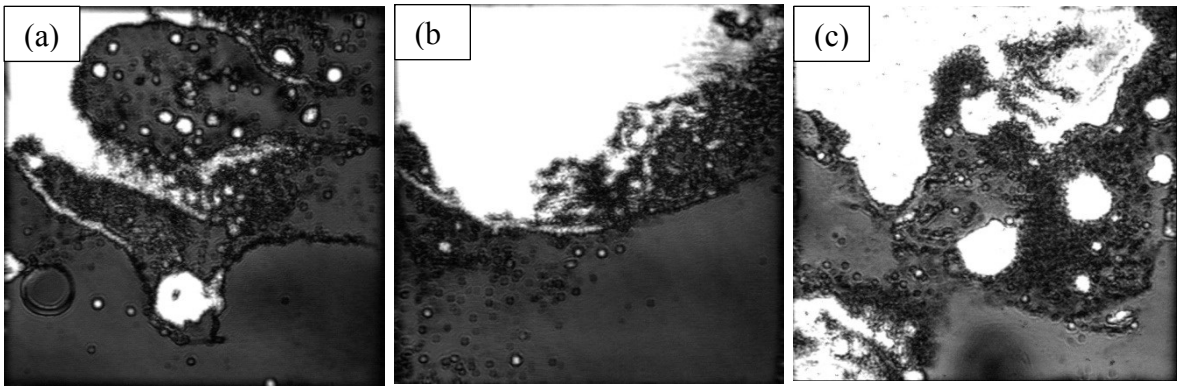


Figure 5.16. SAM images of three eutectic a-Si/Au bonded samples preheated at 350°C for 20 min and bonded at 400°C for 30 min. The sample locations on the chuck were location 1 as shown in Figure 5.11.

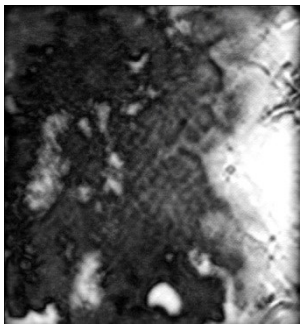
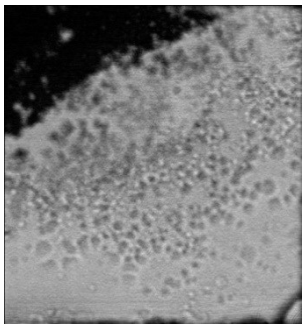
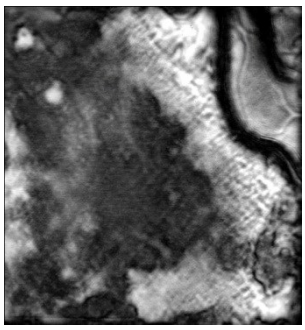
5.1.2. c-Si

In order to compare bonds formed using a-Si and c-Si, the same experiments were done without depositing the a-Si layer on the Si wafers. c-Si samples were bonded under the same condition as a-Si samples for comparison. Table 5.4 shows the SAM results of bonding c-Si samples.

Figure 5.17 shows BSE cross section SEM images from sample 1 (c-Si bonded at 400°C) in Table 5.4. All sample pieces remained attached after dicing. As observed in Figure 5.17(a), large craters had formed at the Au/c-Si interface. The range of crater depth was between 8 and 15 µm. Figure 5.17(b) shows a non-crater area. There are large dark areas both in the craters and non-crater areas. The images in Figure 5.17 were taken at fairly high electron acceleration voltage (25 kV); therefore, the interaction volume in the specimen is relatively large (about 0.17 μm^3) as calculated by Casino software [113] and it is difficult to determine if the black regions are voids or a phase. SEM SE images were taken from another crater-containing location of the same sample at an acceleration voltage of 1 kV (Figure 5.18); more surface detail is visible and the

dark areas are clearly not voids. AES point analysis was performed on 3 points within the crater area, as shown in Figure 5.18. Figure 5.19 shows AES spectra taken from points 1, 2 and 3.

Table 5.4. SAM results for a-Si samples bonded at 400 and 425°C (t= 30 min, P= 0.0133 MPa and bonder pressure of 2×10^{-8} MPa)

T=400°C	 Sample 1 Bonded area: 61% Shear strength: 8 MPa	 Sample 2 Bonded area: 17% Shear strength: 7 MPa
T=425°C	 Sample 3 Bonded area: 45% Shear strength: 6 MPa	 Sample 4 Bonded area: 53% Shear strength: 9 MPa

Points 1 and 3 are pure Si, while point 2 shows almost pure Au. According to the phase diagram, Si and Au have very limited solubility in one another and do not form any compounds.

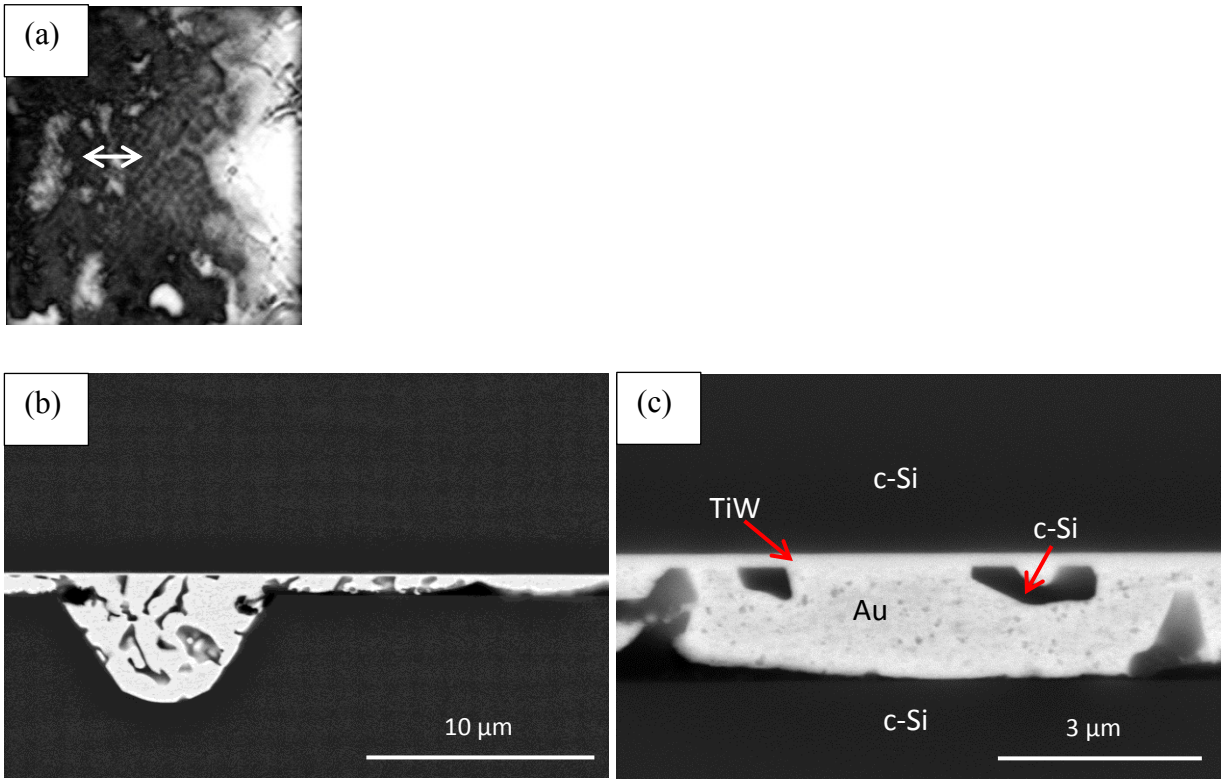


Figure 5.17. Cross section BSE SEM images (25 kV) from (b) crater and (c) non-crater area in c-Si sample preheated at 350°C for 20 min and bonded at 400°C for 30 min. The images were taken from the region indicated by the line shown in the SAM image (a) (sample 1).

In order to confirm the observations, AES mapping was performed on a crater area as shown in Figure 5.20(a). The distribution of the elements in the Si map (Figure 5.20(b)) and Au map (Figure 5.20(c)) corresponds to the dark and bright areas in the SEM image (Figure 5.20(a)), respectively.

Sample 2, which was the duplicate of sample 1 (c-Si bonded at 400°C), was also diced into 4 equal pieces, but 2 of the 4 pieces were located in the bright area of the SAM image and detached during dicing.

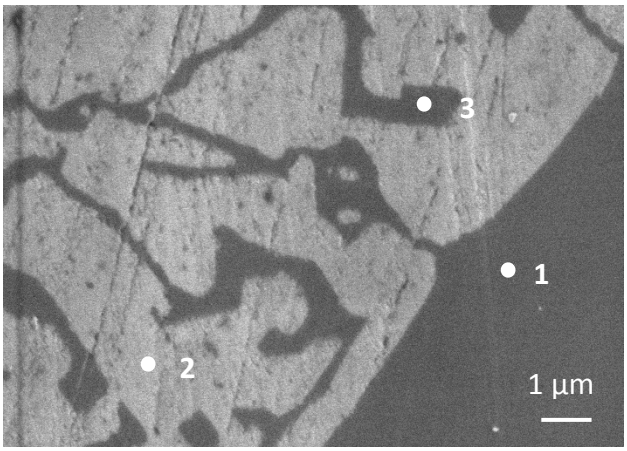


Figure 5.18. SEM SE cross section image taken at 1 kV from the crater area in the c-Si sample bonded at 400°C for 30 min (sample 1).

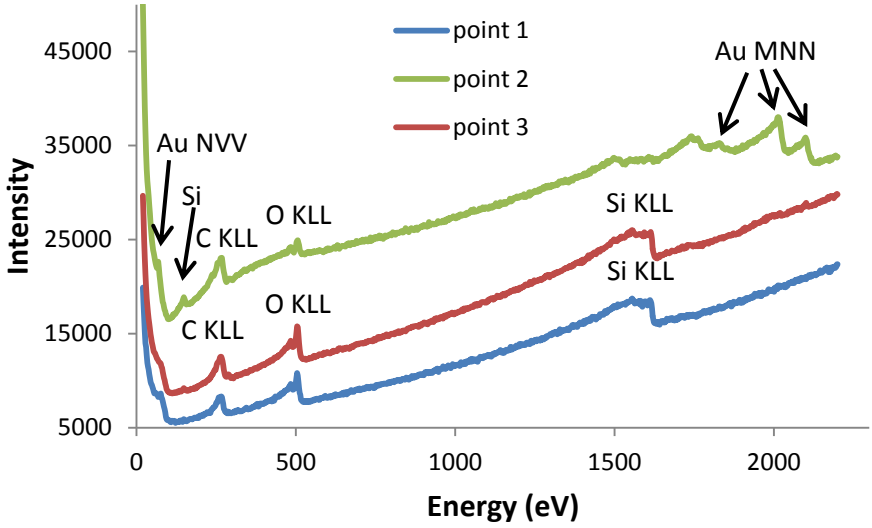


Figure 5.19. AES spectra obtained from points 1, 2 and 3 in Figure 5.18.

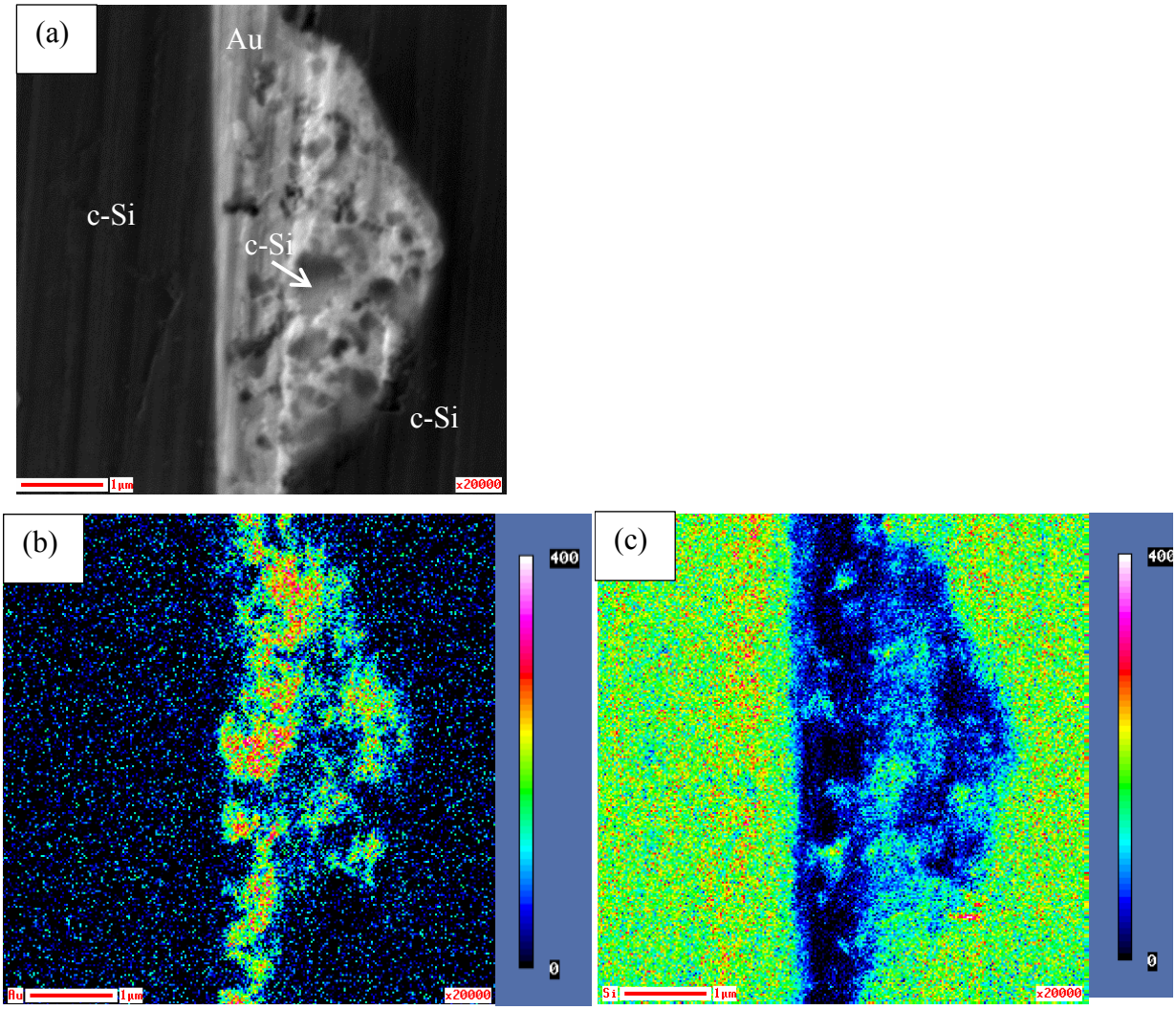


Figure 5.20. (a) SEM SE cross section image of the crater area from the c-Si sample bonded at 400°C for 30 min. AES maps for Au (b) and Si (c) (sample 1).

Figure 5.21 shows plan view SEM SE images of sample 2 (c-Si) with low shear strength (bright areas in SAM image), which resulted in bond detachment. The bright squares in this micrograph are the craters that formed inside the c-Si. Dark areas inside the bright squares are dissolved Si from the substrate, which crystalized inside the crater again. The dark areas can be observed in the crater cross section images (Figure 5.20 (a)). Since Au is soft, the sample was sheared from the top of the crater on the Au side. Well-bonded samples with high shear strength could not be sheared without damage

to the samples; therefore, comparison could not be made between high and low strength samples.

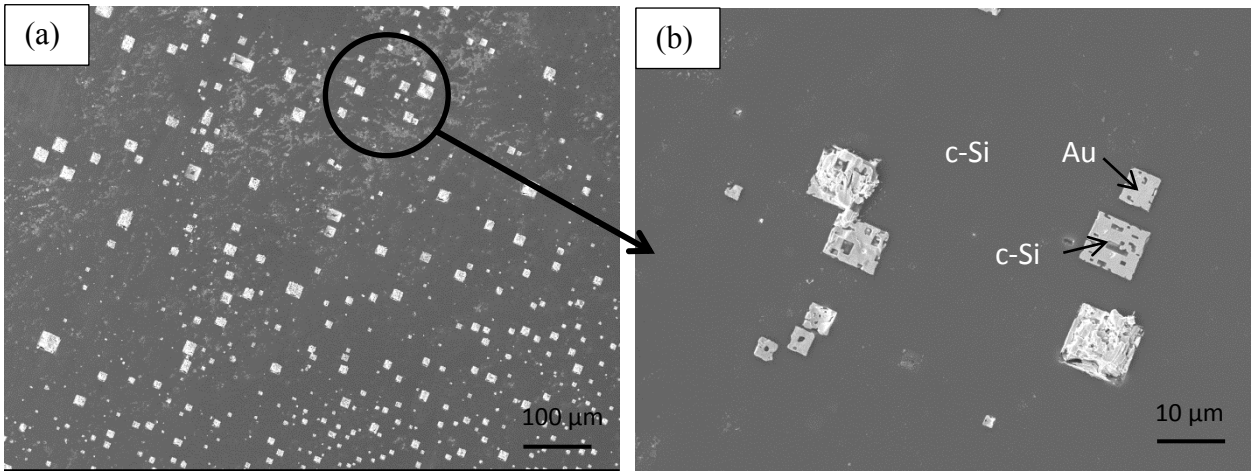


Figure 5.21. Plan view SEM SE images from detached Au/c-Si pieces bonded at 400°C for 30 min (sample 2): (a) low magnification and (b) high magnification.

Sample 3 (c-Si) was bonded at 425°C for 30 min. Cross section images of the region indicated by the arrow in Figure 5.22(a) are shown in Figure 5.22(b) and 5.22(c).

The average size of the craters is larger in comparison with samples 1 and 2, because of the higher process temperature and increased Si dissolution. Similar cross section microstructures were observed for sample 4 (duplicate of sample 3 (c-Si bonded at 425°C)). Plan view images of detached pieces (sample 3 – regions appearing bright in the SAM image) after dicing are shown in Figure 5.23. Several craters with different sizes are visible. The size of the craters was measured using Image J software. The average cross sectional diameter of the craters in Figure 5.23(a) (50 µm), from a sample which was bonded at 425°C, are clearly larger compared with the sample in Figure 5.21(a) (15 µm) because of higher dissolution rates at higher temperature. The measurements were done for a total of 6 craters per sample and the standard deviations were 9.8 µm and 2.4 µm, respectively. A plan view image of one of the

craters in Figure 5.23(a) is shown in Figure 5.23(b). The crater is faceted, with facets along (111) planes which are resistant to dissolution because of their low surface energy.

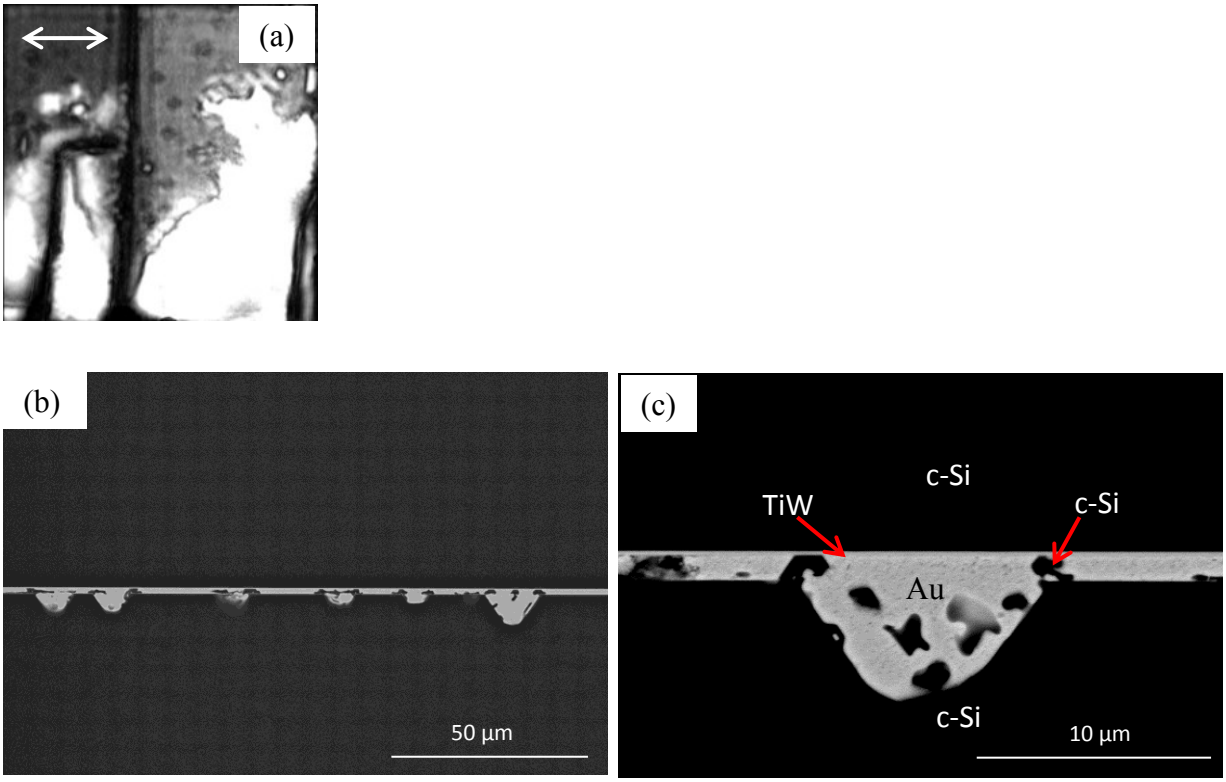


Figure 5.22. Cross section BSE SEM images (25 kV) from the interface of Au/c-Si sample 3 bonded at 425°C for 30 min; taken from the region indicated by the arrow in the SAM image (a): (b) low magnification and (c) high magnification.

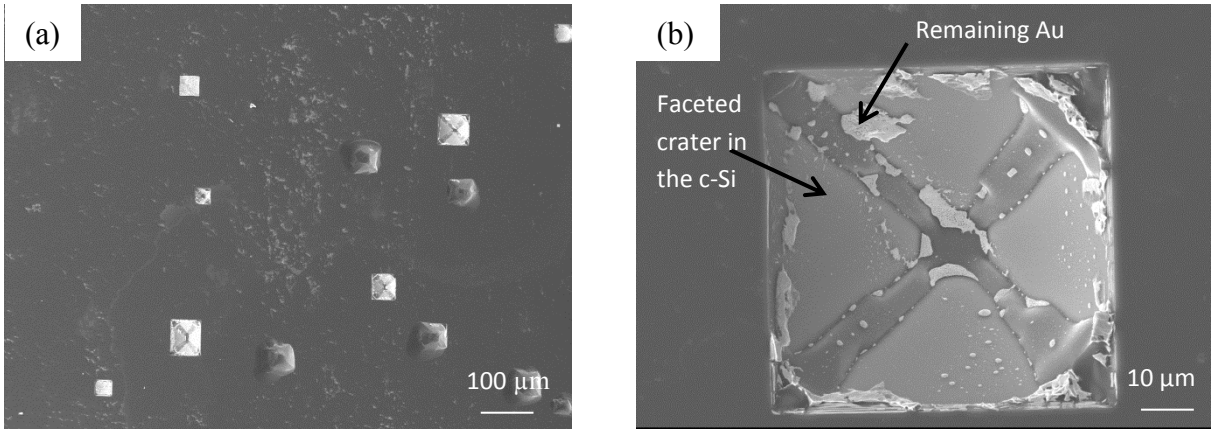


Figure 5.23. Plan view SEM SE images from detached pieces bonded at 425°C for 30 min (sample 3): (a) low magnification and (b) high magnification.

c-Si eutectic bonding was performed with the new bonding conditions (five configuration set-up using graphite sheets in the bonder). SAM images, from three bonded samples are shown in Figure 5.24. For eutectic bonding, the same heating schedule was used as for the a-Si samples, i.e., the samples were preheated at 350°C for 20 min and bonded at 400°C for 30 min. Compared with the a-Si samples (Figure 5.16), fewer and smaller bright contrast regions are present. The percentages of bright contrast areas are <5% of the total bonded area. Figure 5.25 shows SEM images of a cleaved cross section from the area denoted in Figure 5.24(b). A thin, continuous Au layer (less than the thickness of the 100 nm TiW layer), as well as faceted craters, are visible at the interface. The average depth and width of the craters are 2 µm and 7 µm, respectively, and the craters are filled with Au. Some of the Au has spilled out from the bonded region during bonding, which was confirmed by optical microscopy.

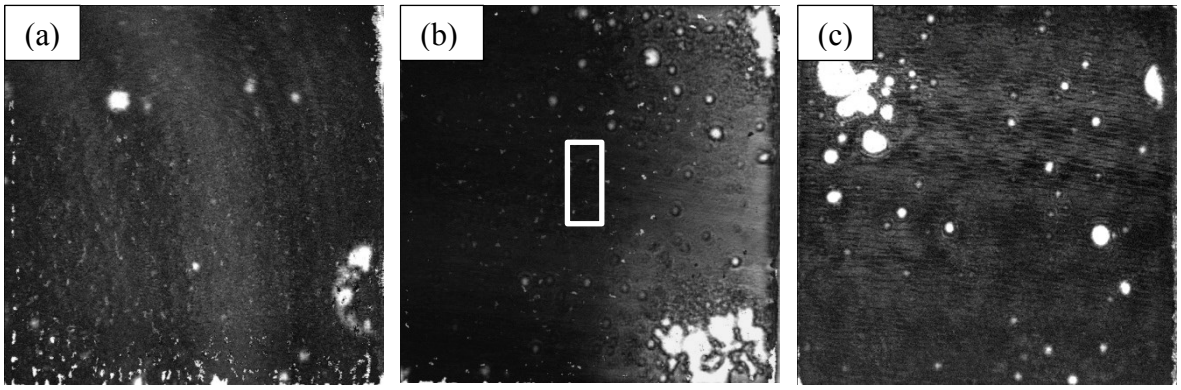


Figure 5.24. SAM images taken from three of the five c-Si/Au eutectic bonded samples (preheated at 350°C for 20 min and bonded at 400°C for 30 min).

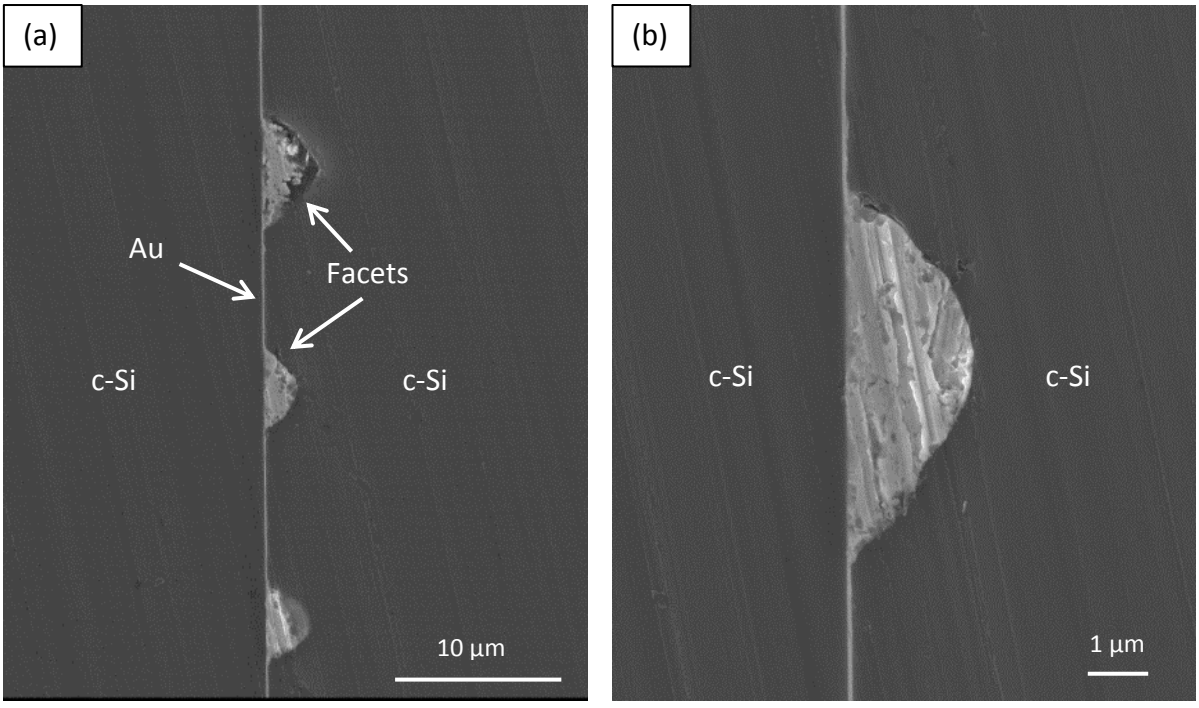
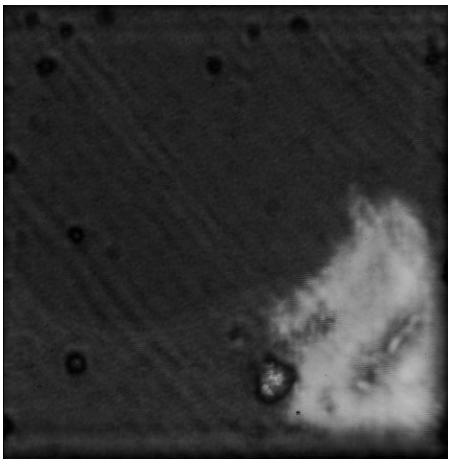


Figure 5.25. SEM SE images of cleaved Au/c-Si eutectic bonded sample: (a) low magnification image and (b) higher magnification image.

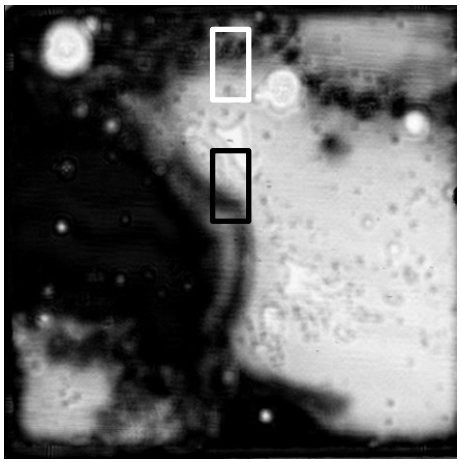
5.2. Au-Si solid state bonding

5.2.1. a-Si

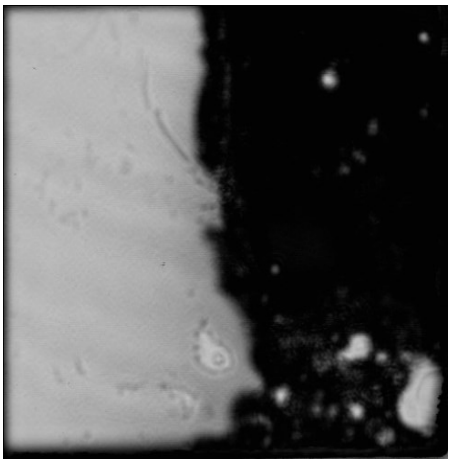
The five sample configuration was used for bonding a-Si samples in solid-state, as well. The solid-state bonded samples were heated to 350°C for 20 min with no preheating. Figure 5.26 shows SAM images from the five bonded samples.



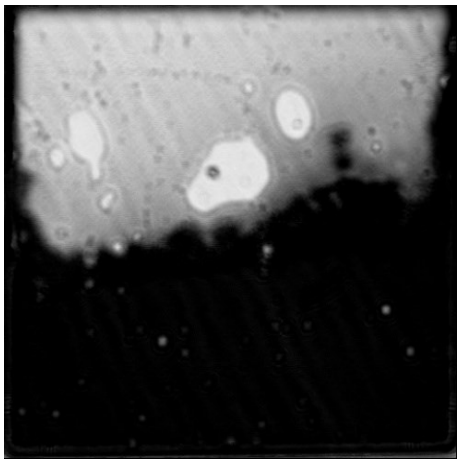
Sample 1



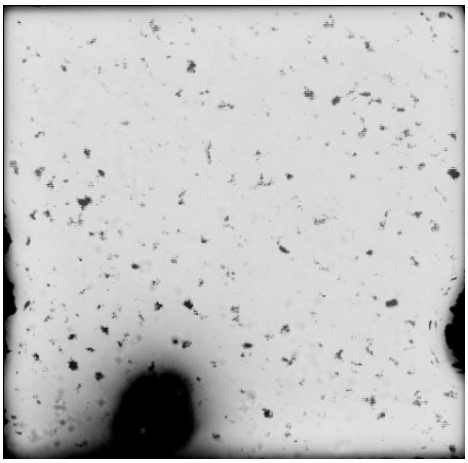
Sample 2



Sample 3



Sample 4



Sample 5

Figure 5.26. SAM results of the a-Si solid-state bonded sample with the five sample configuration.

Comparing Fig 5.26 with Figure 5.20, similar results were obtained from solid-state bonded samples as with eutectic bonded samples. The percentage of bright areas in SAM images (coarse microstructure) for samples 1 to 5 were 4%, 44%, 47%, 45% and 93%, respectively.

In order to evaluate the effect of solid-state bonding duration, two sets of a-Si/Au samples were bonded for 10 min and 20 min at 350°C. Each test was repeated three times to improve reliability. The five sample configuration was used and the location of sample 1 in Figure 5.11 was chosen for observation since it had the best pressure distribution among 5 samples. SAM results for the three a-Si samples bonded at 350°C for 10 min in the sample 1 location are shown in Figure 5.27. The pressure uniformity has improved and fewer unbonded areas are observed. The coarse microstructure (bright) areas in Figure 5.27 were measured as 4%, 5% and 14% from left to right, respectively. To observe the effect of bonding time on solid-state bonding, 3 a-Si/Au samples were bonded at 350°C for 20 min with the same five sample configuration. Figure 5.28 shows the SAM results for the three samples at location 1. The bright area

percentages in the SAM images were reduced, i.e., values of 1%, 7% and 5% from left to right in Figure 5.28 were obtained, respectively. For solid-state bonding there is no liquid formation, so time and temperature are two important parameters for interdiffusion. At a fixed temperature, longer bonding times will result in more interdiffusion of Au and Si and a more continuous bond will form in that case; compare Figure 5.27 and Figure 5.28. Figure 5.29 shows SEM SE cross section images of the region indicated in Figure 5.28(b). The microstructure is very similar to that in the dark regions of the eutectic bonded a-Si samples (Figure 5.20(a)). The main difference is that layer exchange is more localized in the solid-state bonded samples.

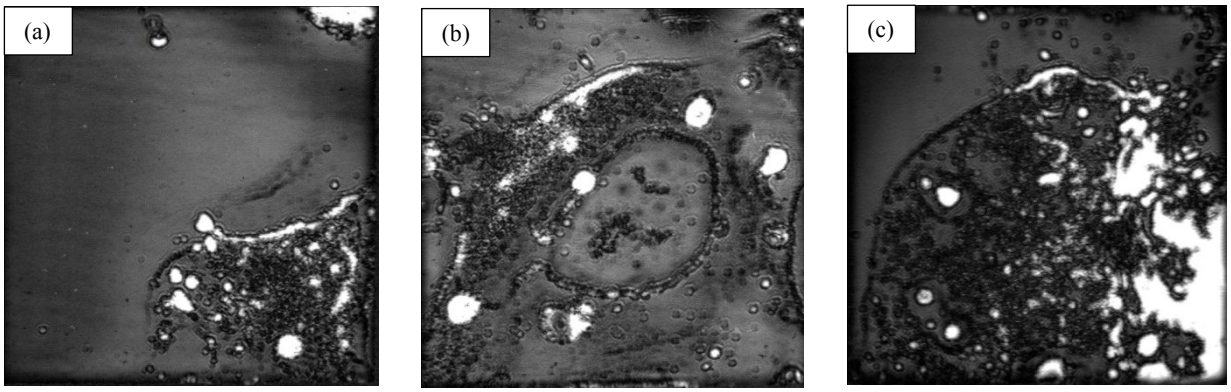


Figure 5.27. SAM images of three a-Si/Au samples that were solid-state bonded at 350°C for 10 min. The sample location on the chuck was position 1 in Figure 5.11.

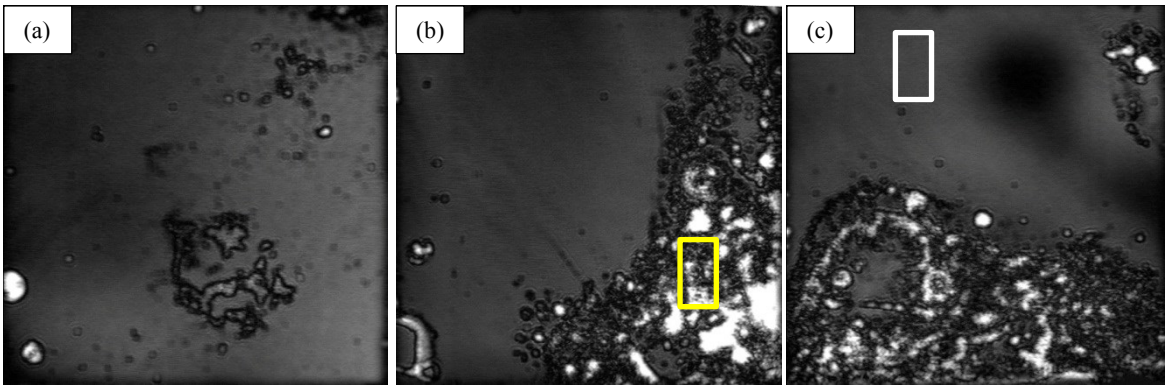


Figure 5.28. SAM images of three a-Si/Au samples solid-state bonded at 350°C for 20 min. The samples were positioned at location 1 on the chuck in Figure 5.11.

Since the cross section sample shown in Figure 5.29 was prepared by cleaving the sample, Si which is brittle appears smooth while ductile Au has a rough fracture surface. In order to study the interface in more detail, a FIB sample of the region shown in Figure 5.28(c) was prepared and examined in TEM (Figure 5.30). EDX analysis was done on several points and the analysis shows that the brighter contrast regions are Si (appear to be crystalline), while the darker contrast regions are primarily Au with Si dispersed within them. Layer exchange is clearly visible in Figure 5.30, but was not completed in the 20 min bonding time. SAD patterns were obtained from the large Si grains; one example is shown in Figure 5.30(b). The patterns were indexed to diamond cubic Si; no amorphous regions were detected. The dark regions in the SAM images have more areas with three interfaces than areas with four interfaces (see Figure 5.14), which reduce the amount of sound reflected as discussed for Figure 5.14.

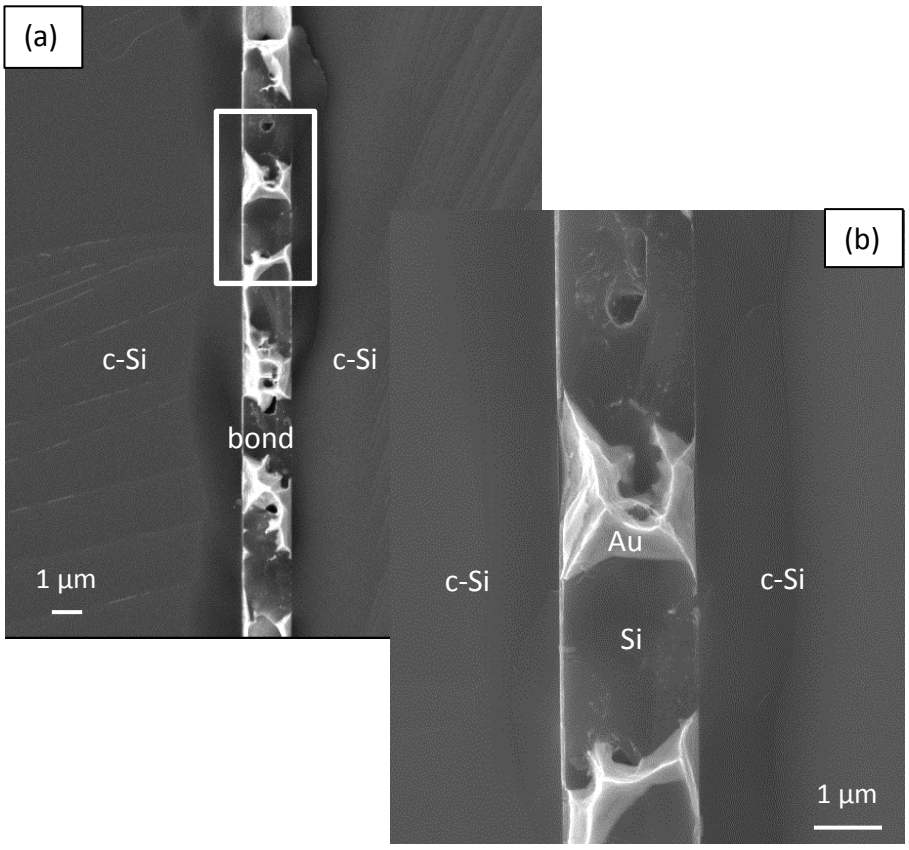


Figure 5.29. SEM SE cross-section images from region indicated by the yellow rectangle in Figure 5.28(b): (a) Low magnification image and (b) higher magnification image of region indicated in (a).

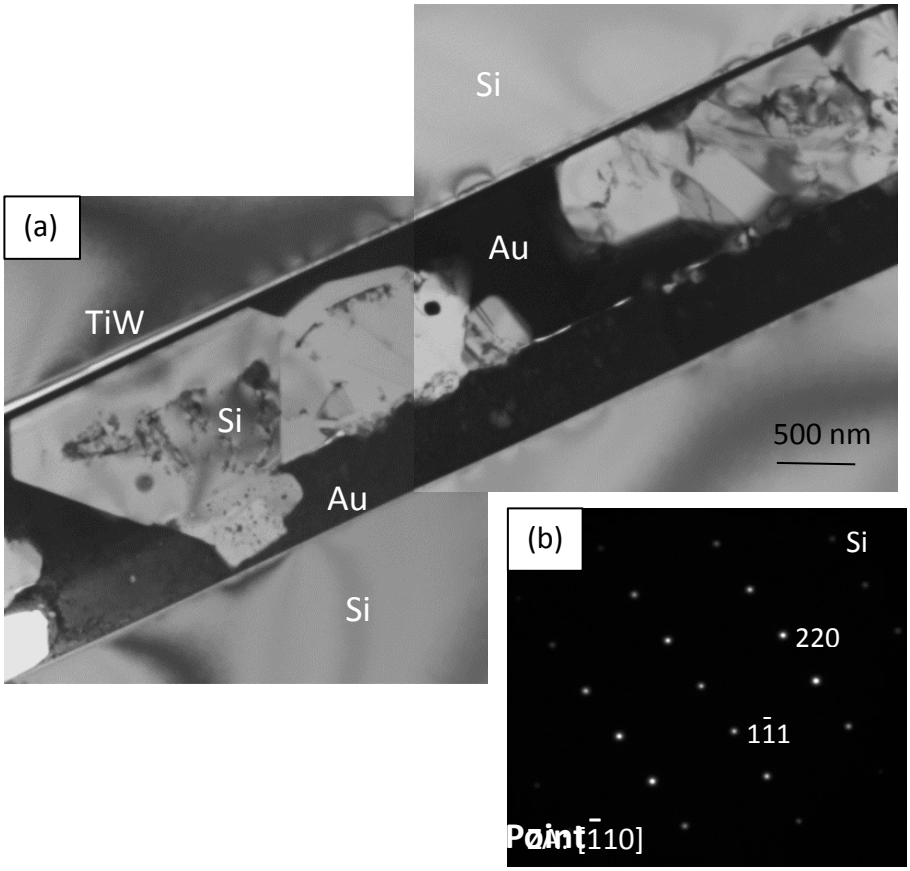


Figure 5.30. (a) TEM BF image of FIB sample prepared from the region indicated in Figure 5.28(c). (b) SAD pattern from one of the Si grains.

5.2.2. c-Si

Solid-state diffusion bonding was performed for c-Si samples as well. Figure 5.31 shows SAM images taken from three samples bonded at 350°C for 20 min. The samples were taken from location 1 on the chuck in Figure 5.11. A few small bright contrast regions (<2% of the total area) are present in the images. Figure 5.32 shows SEM images of a

cleaved cross section sample prepared from the region indicated in Figure 5.31(b). The bond is quite uniform, with the exception of numerous faceted craters at the solder/Si interface. The craters are much smaller in comparison with the eutectic bonded c-Si samples (Figure 5.25). The average depth and width of the craters are 150 and 300 nm, respectively, compared with 2 μm and 7 μm, respectively, for the eutectic bonded samples.

To observe the bond in more detail, a FIB sample was prepared from the region indicated in Figure 5.31(a); the corresponding TEM BF images are shown in Figure 5.33. Two craters and columnar Au grains are visible. An SAD pattern was obtained from one of the craters (Figure 5.33(b)) and was indexed to Au. EDX analysis also confirmed that the craters only contained Au. The craters are located at the end of Au grain boundaries, which indicates that Au preferentially diffuses through the grain boundaries to the Au/c-Si interface. This result is similar to that obtained for the Au/c-Si diffusion couples.

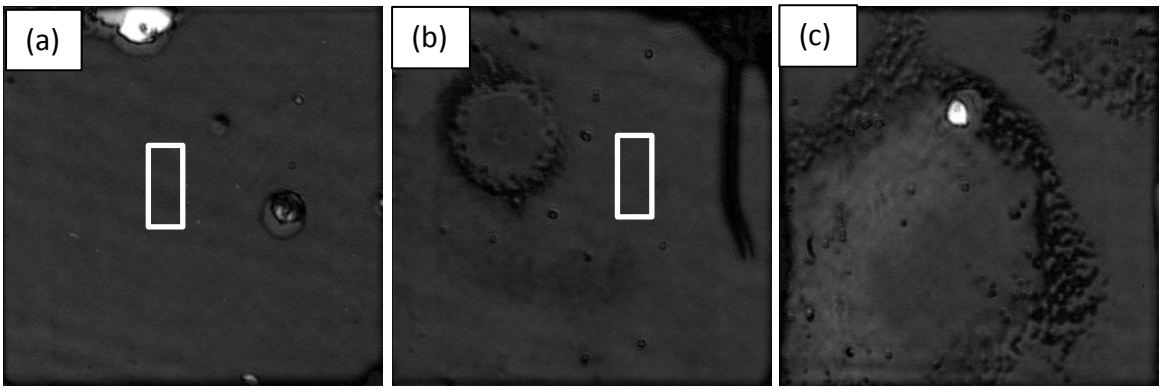


Figure 5.31. SAM images of three of five solid-state diffusion bonded Au/c-Si samples (heated to 350°C for 20 min).

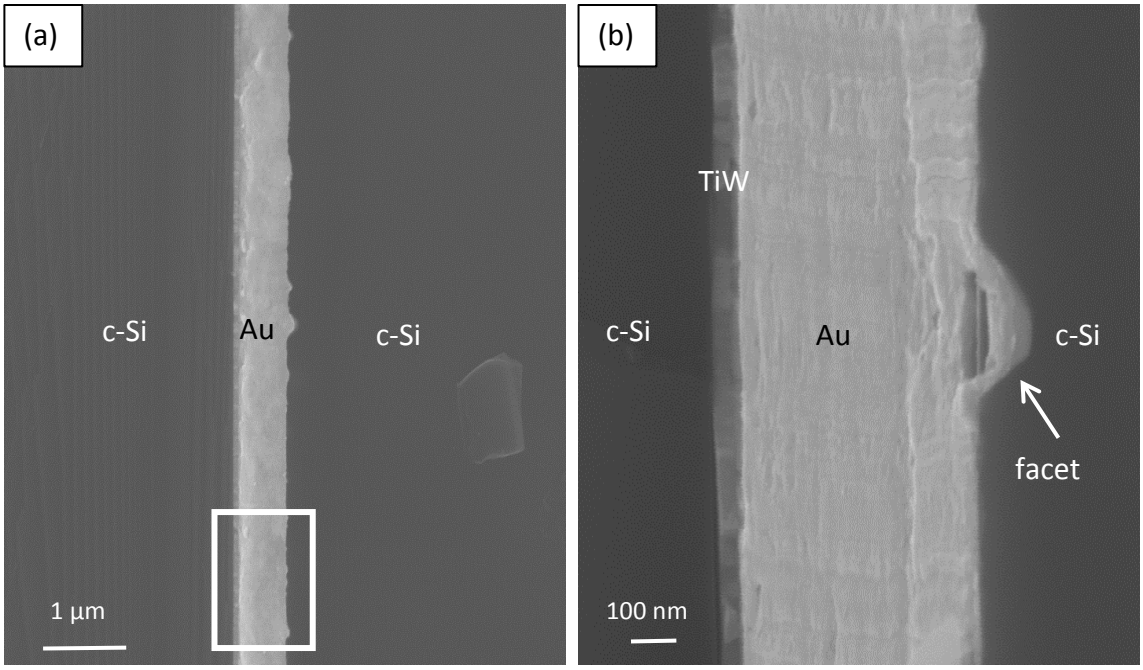


Figure 5.32. SEM SE cross-section images of the region indicated in Figure 5.31(b): (a) Low magnification image and (b) higher magnification image of region indicated in (a).

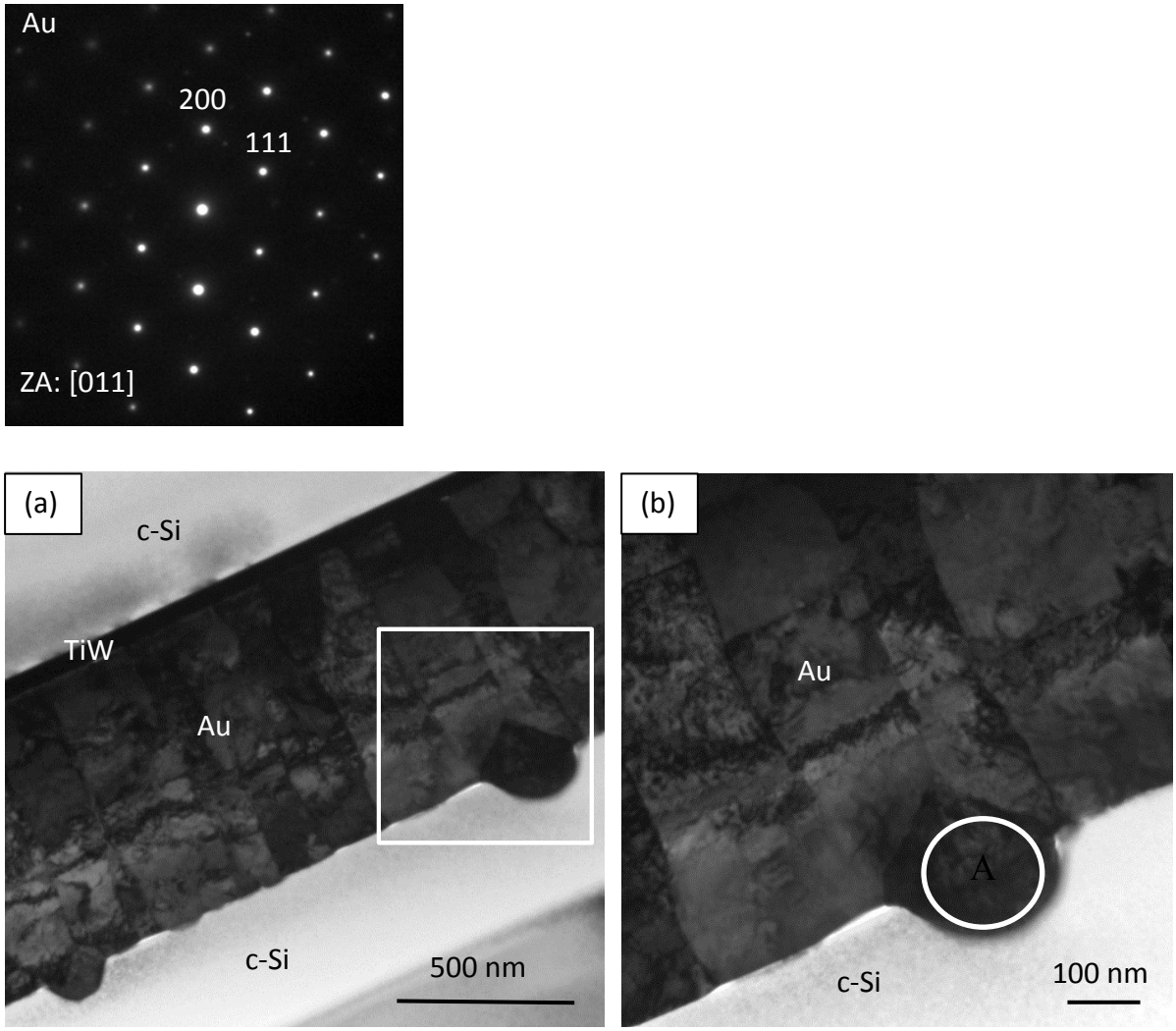


Figure 5.33. TEM BF images of FIB sample prepared from region indicated in Figure 5.31(a): (a) Low magnification image and (b) higher magnification image of region in (a); SAD pattern of Au particle is also shown.

5.3. Evaluation of bond strength

5.3.1. a-Si

Quantitative analysis of bond strength was performed through shear testing. For each bonding condition, five samples were shear tested. The maximum load of the shear

tester was 100 kg, so that the maximum measurable shear strength for the samples was 15.31 MPa. Figure 5.34 shows a plot of shear strength vs. percentage of dark areas in the SAM images for a-Si eutectic and solid-state diffusion bonded samples. Both plots show a similar trend, i.e., shear strength increases with increasing fraction of dark regions in the SAM images. The dark contrast regions have a finer bond microstructure compared with the bright contrast regions, which accounts for the trend in shear strength. For both the solid-state and eutectic bonded a-Si samples, one of the bonds did not fail. In these cases, the Si die failed while the bond remained intact. The maximum shear strengths in Figure 5.34 correspond to these conditions (15.2 MPa for solid-state bonding and 13.2 MPa for eutectic bonding).

Based on the shear strength results, the microstructural analysis and spill out issues (eutectic bonding only), solid-state bonding is preferable for the a-Si samples. In addition, the lower bonding temperature reduces the likelihood for device damage.

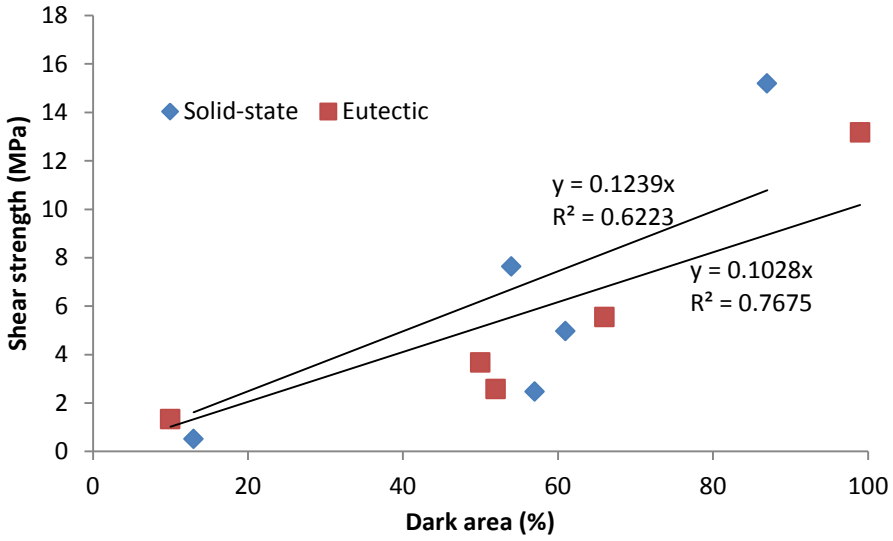


Figure 5.34. Shear strength vs. bonded area percentage for eutectic and solid-state bonded samples.

5.3.2. c-Si

For the c-Si samples, the average shear strength for the eutectic bonded samples was 4.2 MPa, but none of the solid-state bonded samples failed even at the maximum load (100 kg). The superior mechanical properties coupled with the finer bond microstructure make solid-state bonding an attractive alternative to eutectic bonding.

5.4. Summary

This chapter dealt with eutectic and solid state bonding of small samples. It was shown that if the bonding pressure is increased above a critical value, cracks will form. Too high a bonding temperature will lead to spill out of the melt formed and partial bonding as well. The residual stress in a-Si deposited by PECVD was compared with a-Si deposited by LPCVD and due to the high stress levels for PECVD deposited a-Si, the deposition method was changed to LPCVD deposited a-Si to minimize cracking and delamination. The use of graphite sheets in the bonder appeared to improve the uniformity of the bonds achieved.

It was shown that the bright contrast areas in SAM images are actually bonded areas with coarser microstructure compared with dark contrast areas which have a finer microstructure. The coarse microstructure offers more reflective surfaces. Since SAM works in reflection mode, more reflected signals will be detected from the coarse microstructure generating bright contrast regions in the SAM images. For both a-Si and c-Si, solid state bonding resulted in finer microstructures along with higher shear strengths due in part to the lower wafer bonding process temperature.

Chapter 6

Full Wafer Bonding Results

Chapter 6 - Full Wafer Bonding Results

As mentioned in Chapter 5, well-bonded samples were obtained for both a-Si and c-Si samples in terms of bond coverage, shear strength and bond yield. The next objective was to bond entire wafers with a minimum number of voids and craters. Full a-Si and c-Si wafers were bonded and compared. Both solid-state and eutectic bonding were performed.

6.1. a-Si eutectic bonding

Patterned Au wafers were used for bonding purposes. Similar to small sample bonding, full wafers were preheated to 350°C and then bonded at 400°C. Preheating was performed for 20 min; however, 30 min was considered to be too long for bonding by Micralyne so 15 min was chosen for bonding at 400°C. The pressure was recalculated according to the bonding area difference between small samples and full wafers, as discussed in Section 3.2. Figure 6.1 shows the SAM results for a-Si eutectic bonding.

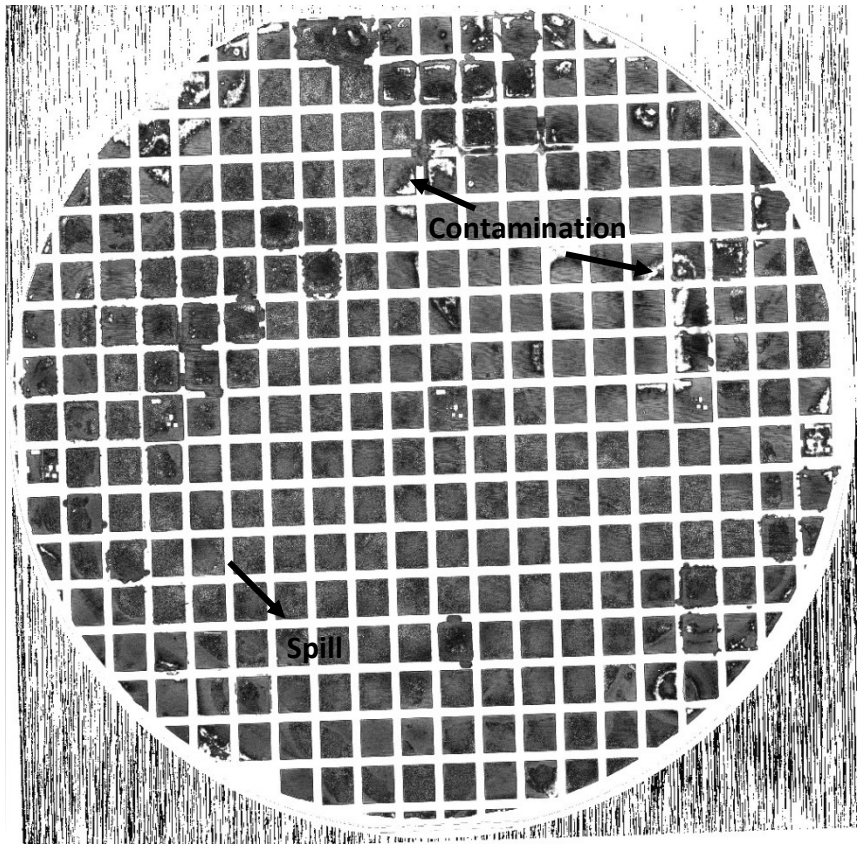


Figure 6.1. SAM results for full wafer eutectic bonding of a-Si with HF cleaning prior to bonding. The sample was preheated to 350°C and then bonded at 400°C.

Figure 6.1 shows impurities in the bonded area, as indicated by arrows. Some solder spill out (also shown in Figure 6.1) is observed where the patterned Au lines cannot be distinctively seen. The rest of the wafer seems to be well-bonded.

The oxide layer was removed by HF cleaning, but there are other contaminants (probably organic) which need to be removed. An SC1 clean was used prior to HF cleaning in order to remove the organic contamination. The SAM results for a full wafer bond after SC1 and HF cleaning are shown in Figure 6.2. Bond uniformity has improved significantly with only a very small amount of contamination. Spill out of solder could not be completely avoided (shown by arrow in Figure 6.2).

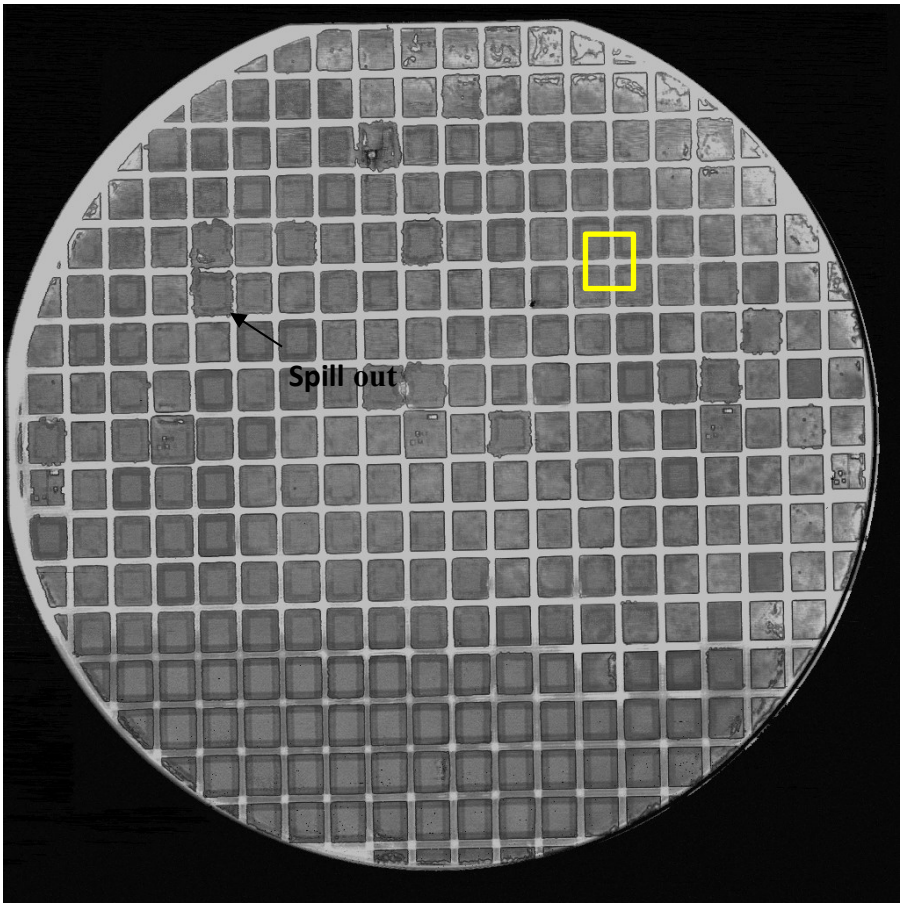


Figure 6.2. SAM image for full wafer eutectic bonding of a-Si with SC1 and HF cleaning prior to bonding. The sample was preheated to 350°C and then bonded at 400°C.

A cross section of the bonded area (rectangle shown in Figure 6.2) is shown in Figure 6.3. The cross section has been polished using FIB methods. The distribution of black particles (Si) inside the bright matrix (Au) can clearly be observed. The beginning of the layer exchange process is apparent in Figure 6.3. The bonding time was not sufficient to see complete layer exchange. In order to show the distribution of Au and Si in the cross section and distinguish the regions from voids, AES mapping was performed and confirmed the dark areas in the Au matrix are Si as shown in Figure 6.4. Elemental mapping can be used to show the positions of elements and phases with varying composition, contaminants, etc. Here, higher concentrations are yellow and orange, whereas lower concentrations are magenta to blue.

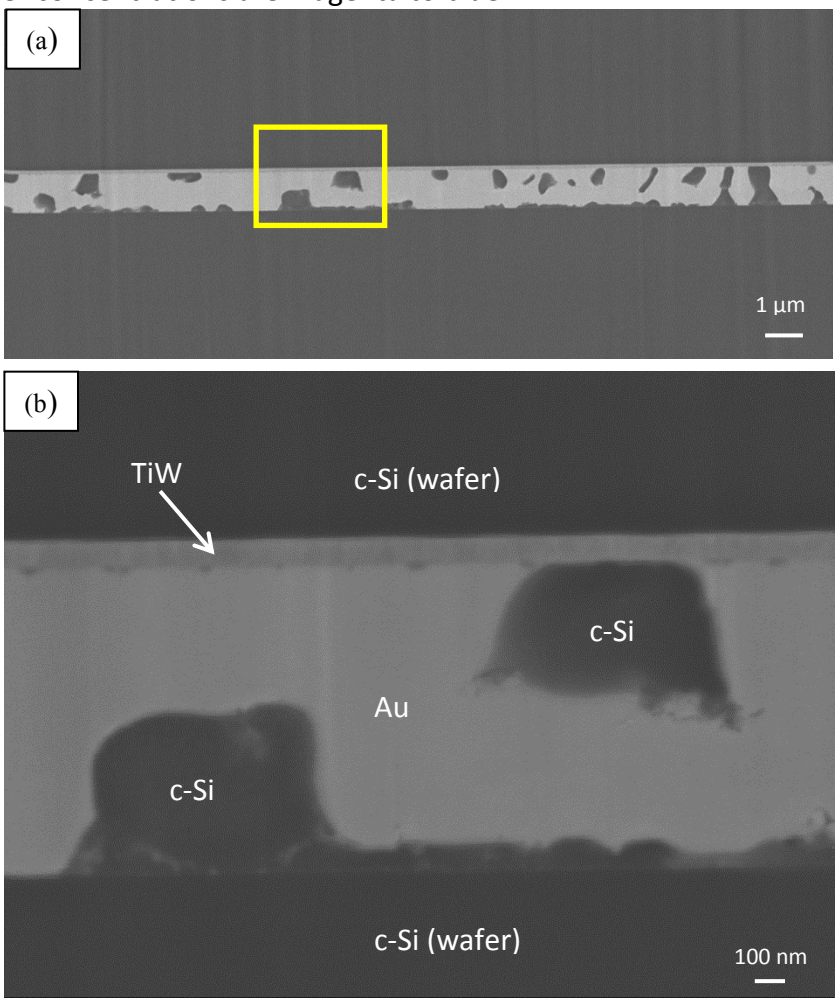


Figure 6.3. Microstructure of a-Si bonded sample preheated at 350°C for 20 min and bonded at 400°C for 15 min. (a) Low magnification and (b) higher magnification images of the rectangle area in Figure 6.2.

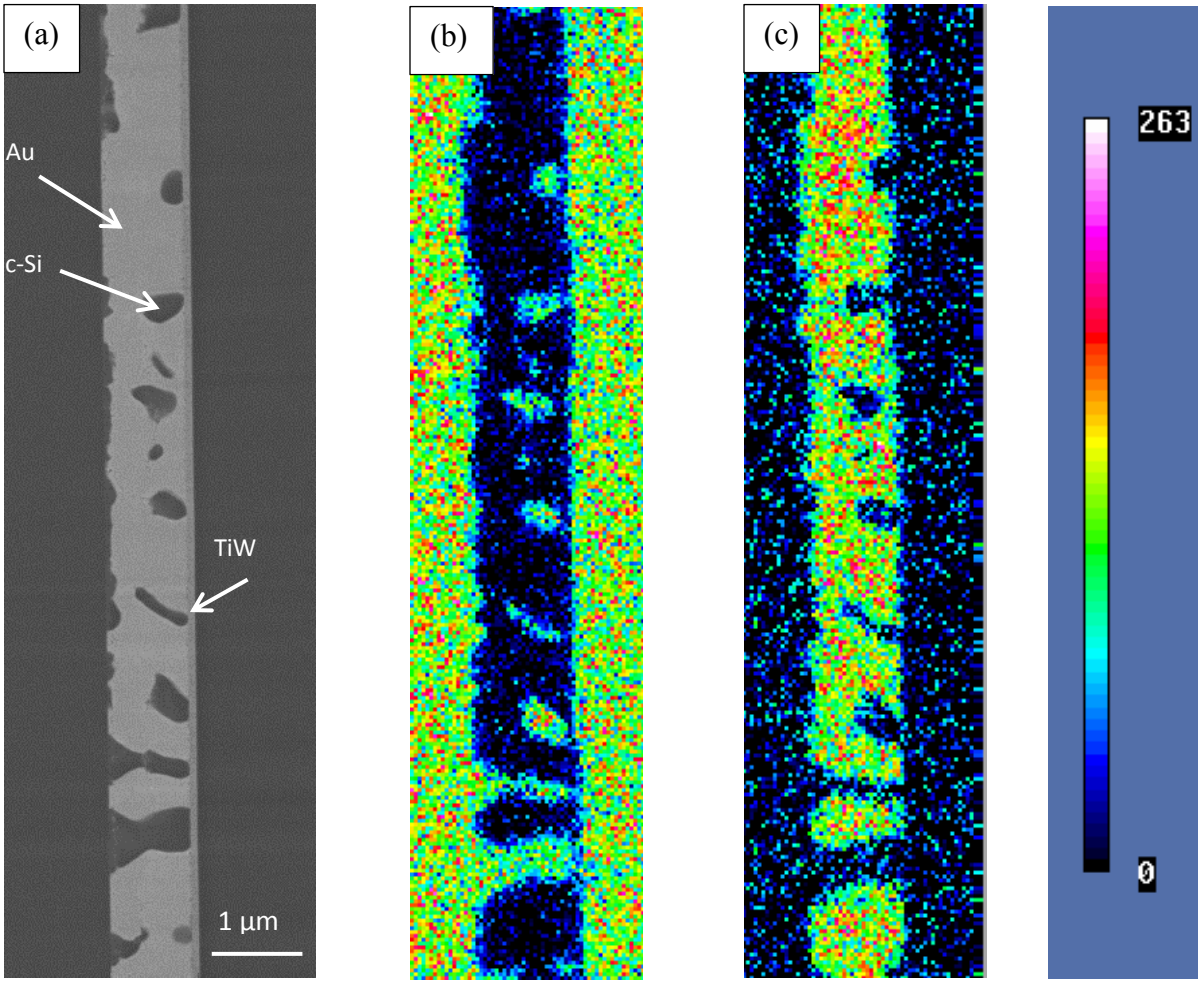


Figure 6.4. AES maps taken from the (a) SE SEM cross section image. (b) Si map and (c) Au map of an a-Si eutectic bonded sample preheated to 350°C for 20 min and bonded at 400°C for 15 min.

6.2. a-Si solid-state bonding

Solid-state bonding of a-Si was also performed to compare with the eutectic bonding results. The samples were bonded at 350°C for 20 min. A SAM image of the bonded pair is illustrated in Figure 6.5. Compared with the eutectic bonded wafers, solid state bonding shows much better uniformity across the bond area. The unbonded bright areas in Figure 6.5 are the result of tweezer damage during wafer handling prior to bonding. A cross section of the area indicated by the rectangle in Figure 6.5 is shown in Figure 6.6.

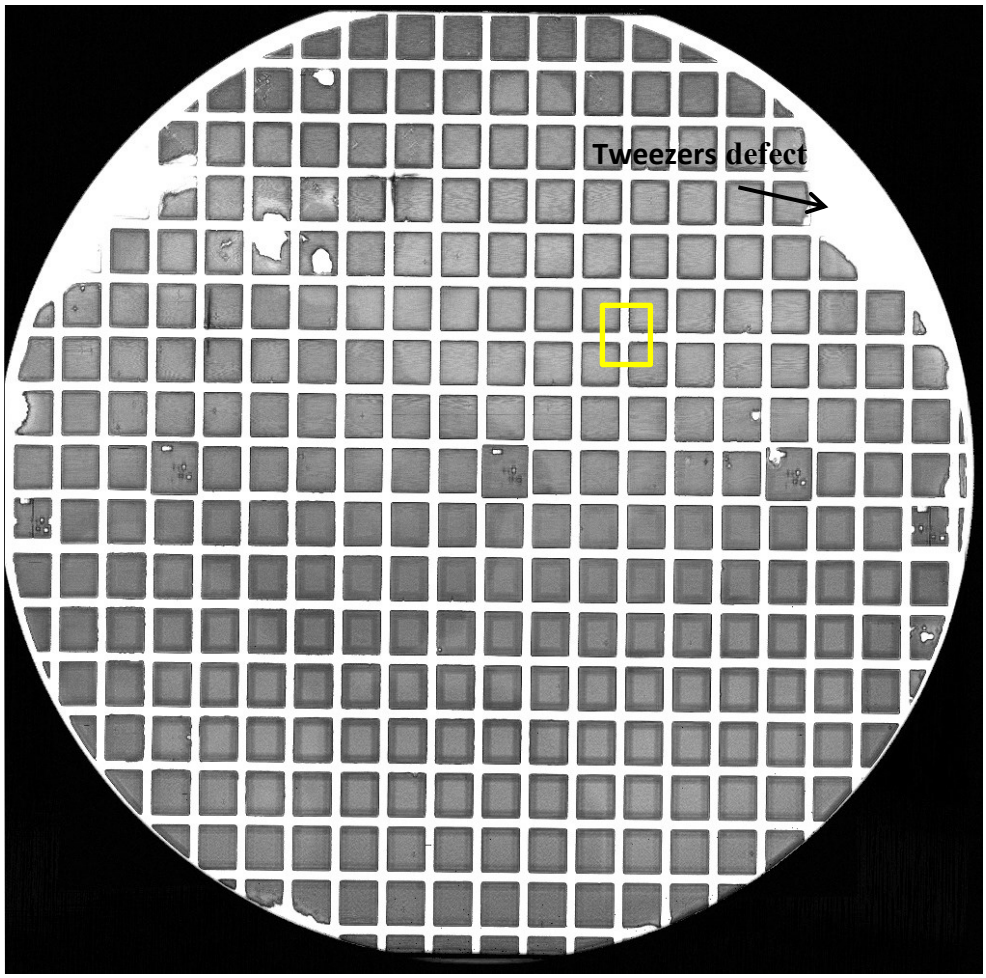


Figure 6.5. SAM image for full wafer solid-state bonding of a-Si with SC1 and HF cleaning prior to bonding. The sample was bonded at 350°C for 20 min.

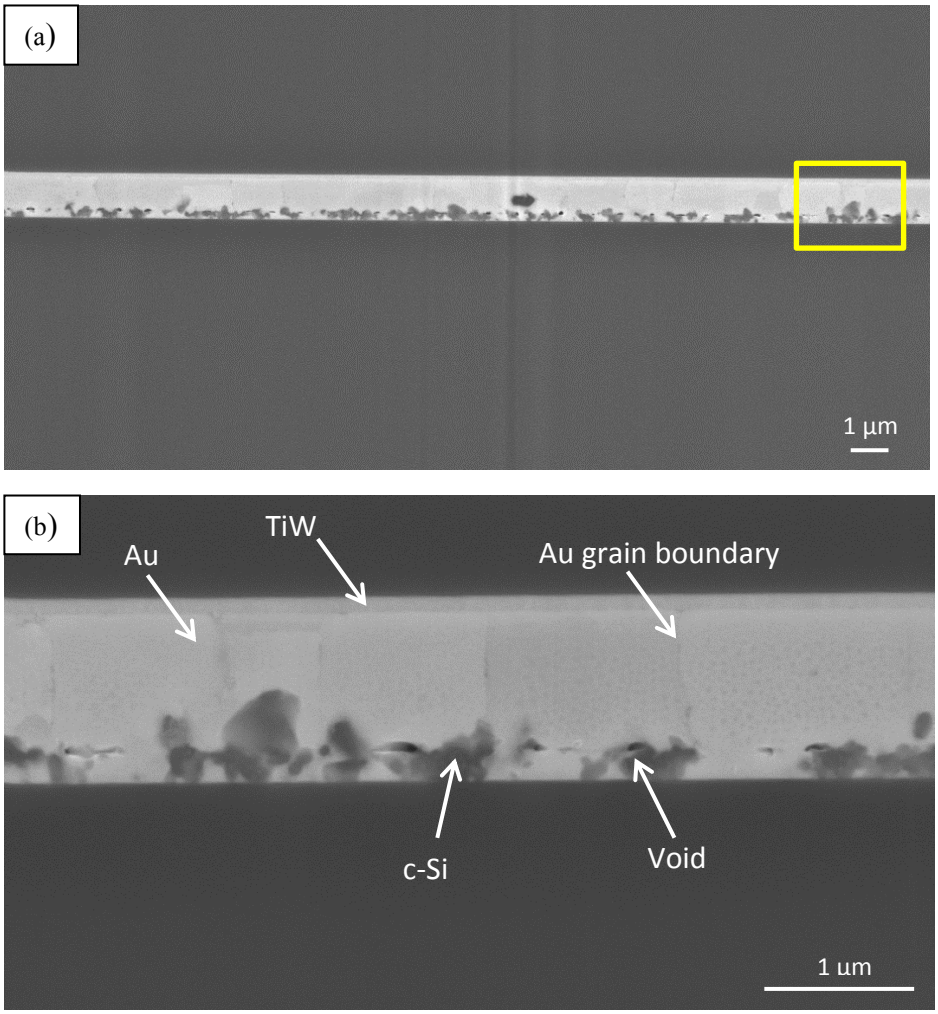


Figure 6.6. Microstructure of a-Si bonded sample bonded at 350°C for 20 min. (a) Low magnification and (b) higher magnification images of the rectangle area in Figure 6.5.

There was no liquid formed during solid state bonding, so that the Au grain boundaries are still visible in Figure 6.6(b). The Si grains are much smaller compared with the grains formed during eutectic bonding and the bonding time and temperature were not sufficient to permit diffusion of Si all the way to the other side of the Au layer. There are some voids visible at the original Au/a-Si interface, which are probably a result of surface roughness and the fact that there was no liquid to fill the gaps between two wafers during bonding. Since no voids were formed in the Au/a-Si diffusion couples after annealing (Figure 4.5), there is a low possibility that these voids

are Kirkendall voids. The SAM resolution is about 2.5 µm, so any voids smaller than that are not resolvable in the SAM images. Similar voids were observable in the SEM images of small a-Si solid-state bonded samples (Figure 5.28). AES mapping also confirmed the distribution of Au and Si as shown in Figure 6.7.

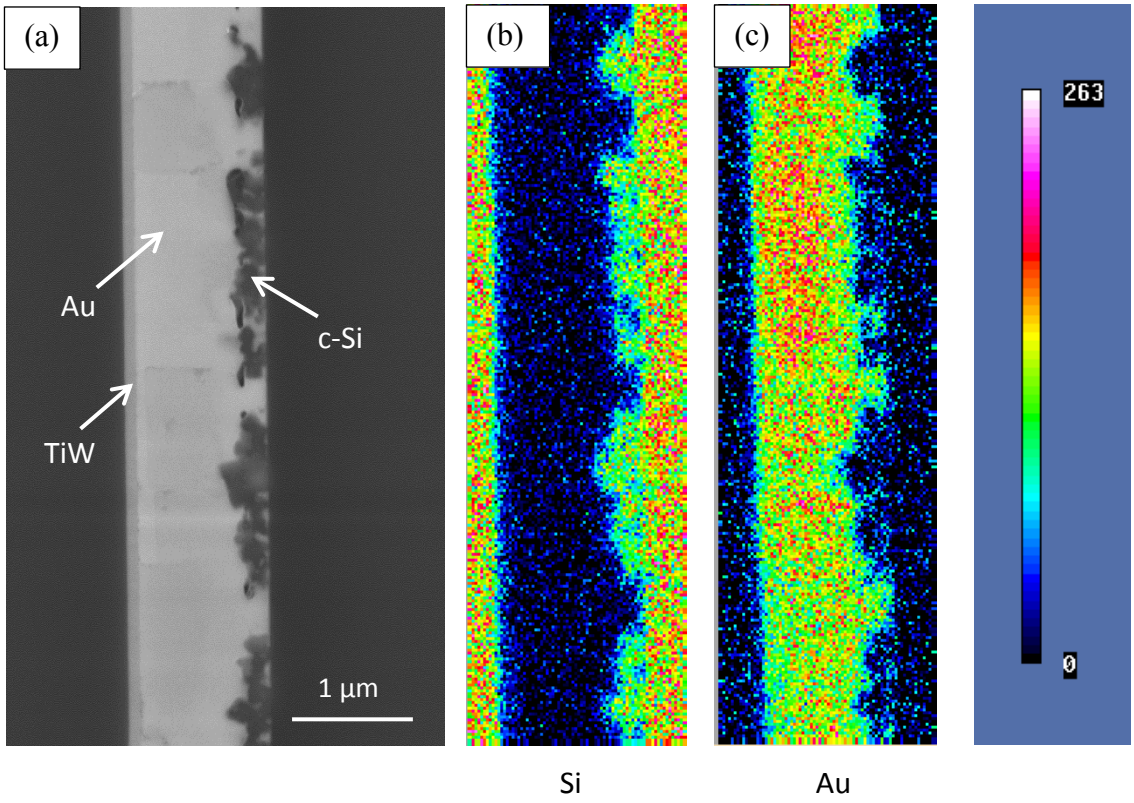


Figure 6.7. AES maps taken from the (a) SE SEM cross section image. (b) Si map and (c) Au map of a-Si solid-state bonded sample bonded at 350°C for 20min.

6.3. c-Si eutectic bonding

A blank Si wafer was used to bond a patterned Au coated Si wafer in order to compare bond uniformity, yield and strength with Si wafers with a-Si layers. A SAM image of a c-Si bonded pair is shown in Figure 6.8. The SAM image is similar to the one for a-Si eutectic bonding (Figure 6.2), but the cross section microstructure is quite different. The microstructure is shown in Figure 6.9, which was taken from the rectangle region shown in Figure 6.8. Spill out is also present in the c-Si eutectic bonded samples. Large

craters are present at the Au/c-Si interface as is expected in the Au/c-Si system. The average size of the craters was 1-3 µm. The appearance of the Si grains in Figure 6.9 is very similar to voids, since the SEM images were taken at 25 kV. Using a lower accelerating voltage (Figure 6.10), more surface morphology detail is revealed and the dark areas are clearly Si grains and not voids. AES mapping was performed on the sample cross section and the results confirmed that the black regions are Si. In Figure 6.11(b) the green section is Au-rich and in Figure 6.11(c) the brighter particles inside the craters are Si-rich.

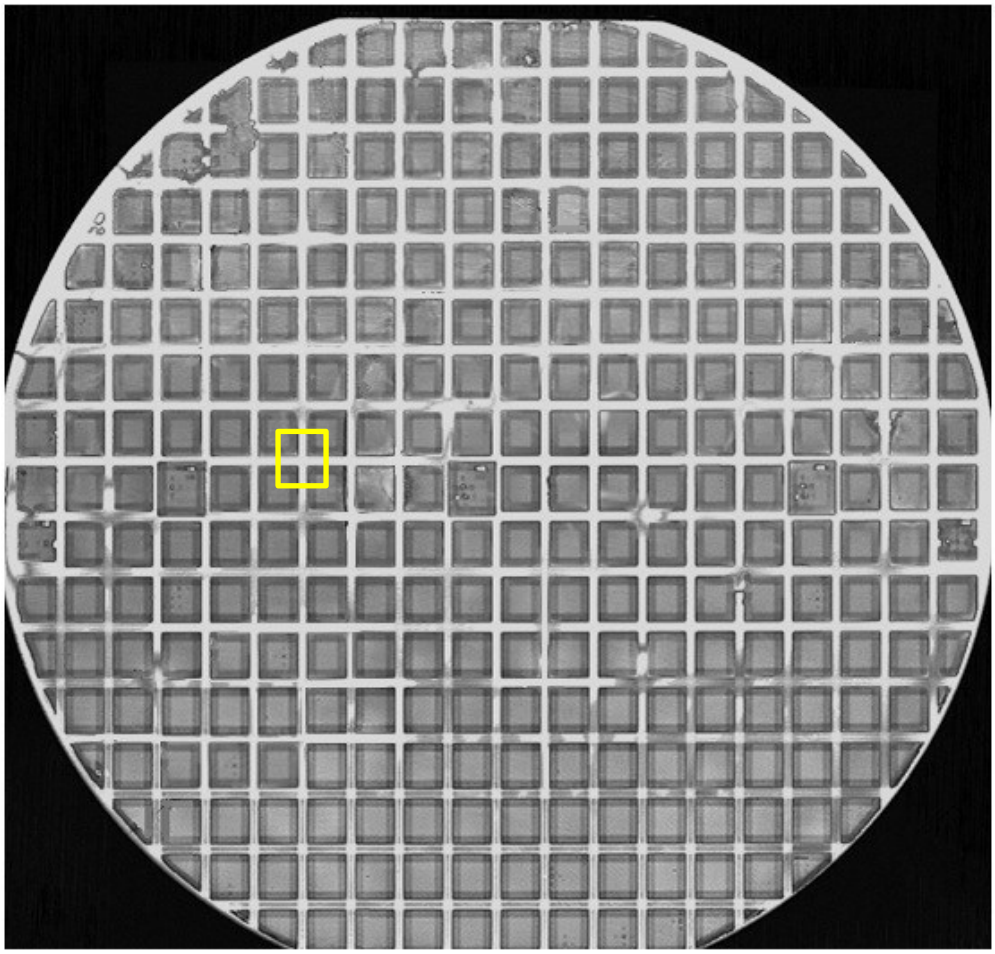


Figure 6.8. SAM image for full wafer eutectic bonding of c-Si with SC1 and HF cleaning prior to bonding.

The black spots on the surface of the Au regions in Figure 6.9 (b) appear to be carbon contamination, which was confirmed by AES of the surface. Carbon contamination was

removed by sputtering prior to AES mapping. Figure 6.12 shows AES mapping from a non-crater area which confirms the formation of Si grains in the Au layer.

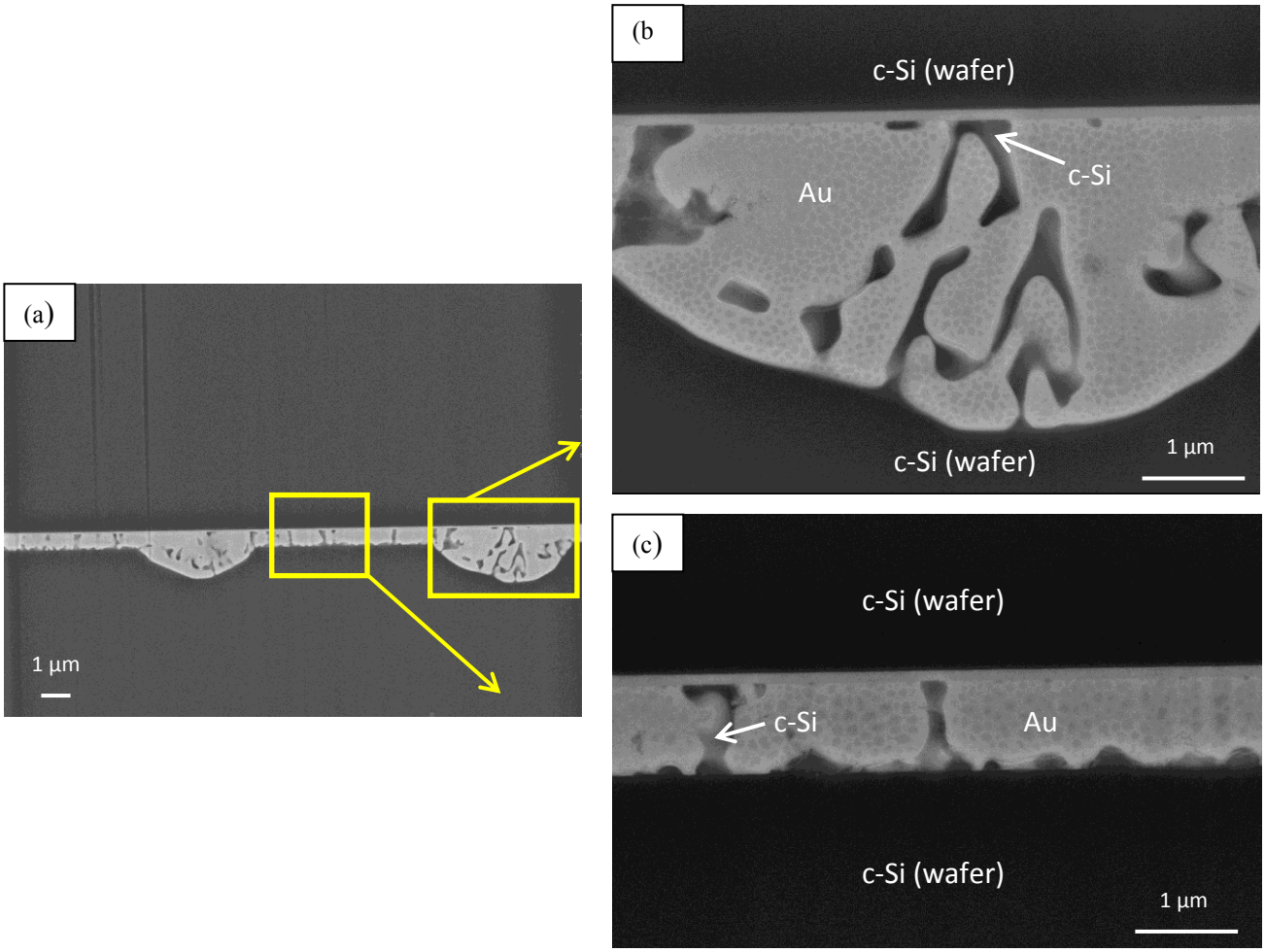


Figure 6.9. SEM SE cross section images of c-Si sample eutectic bonded at 350°C for 20 min taken from the region indicated in Figure 6.8. (a) Low magnification image, (b) high magnification image of the crater area and (c) high magnification image of non-crater area.

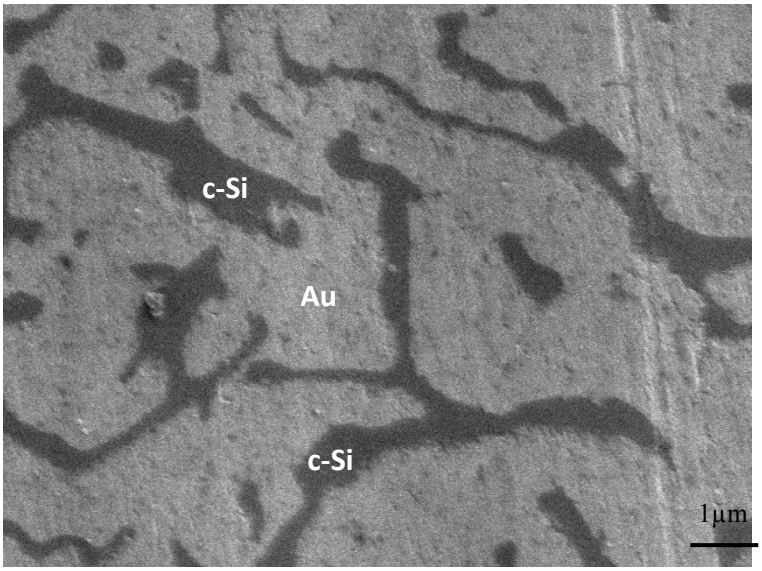


Figure 6.10. SEM SE cross section image (1 kV) of crater area in eutectic bonded c-Si sample (bonded at 350°C for 20 min).

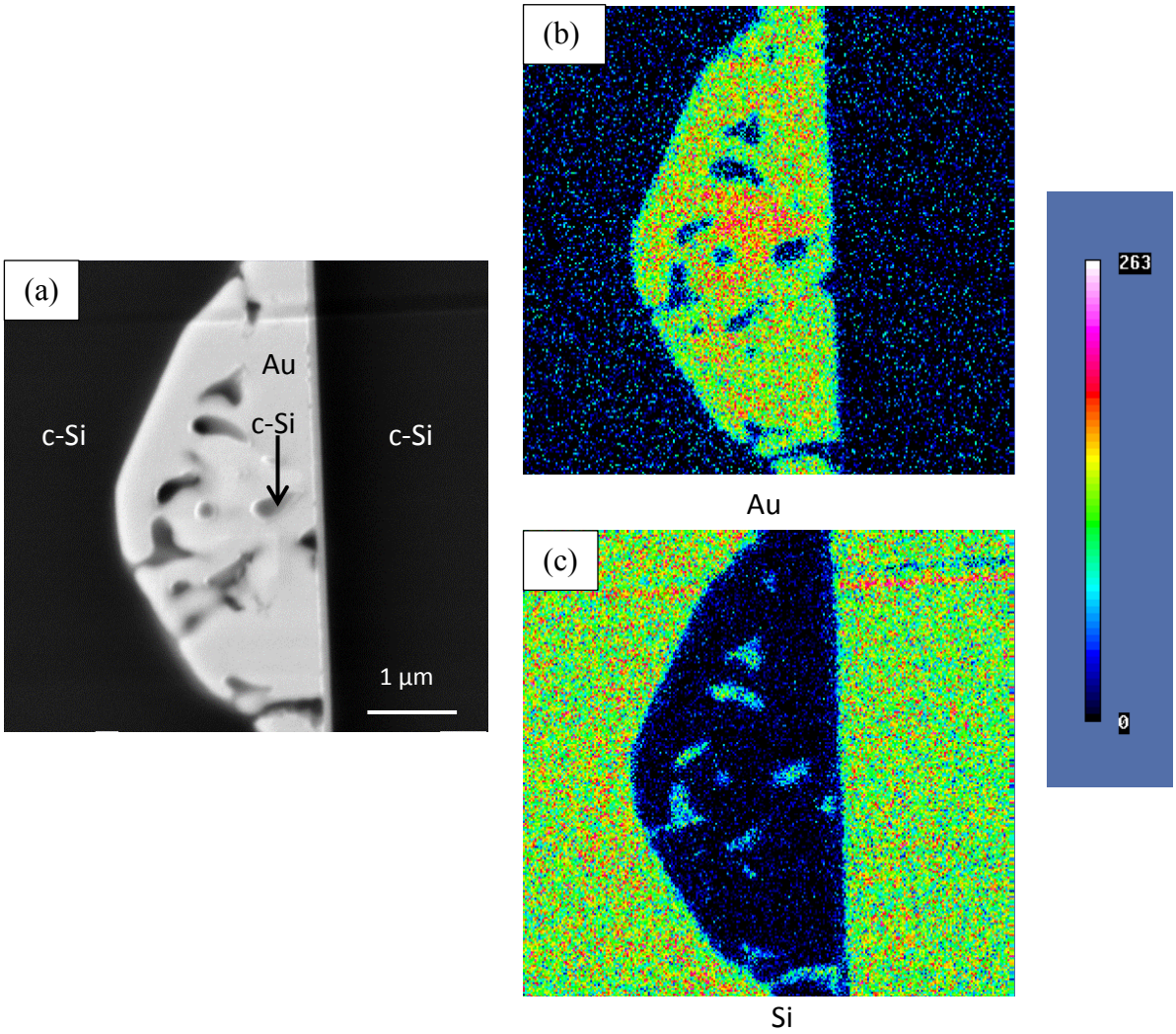


Figure 6.11. AES maps taken from the (a) SE SEM cross section image of the sample bonded at 350°C for 20 min. (b) Au map and (c) Si map of a crater area in the c-Si eutectic bonded sample.

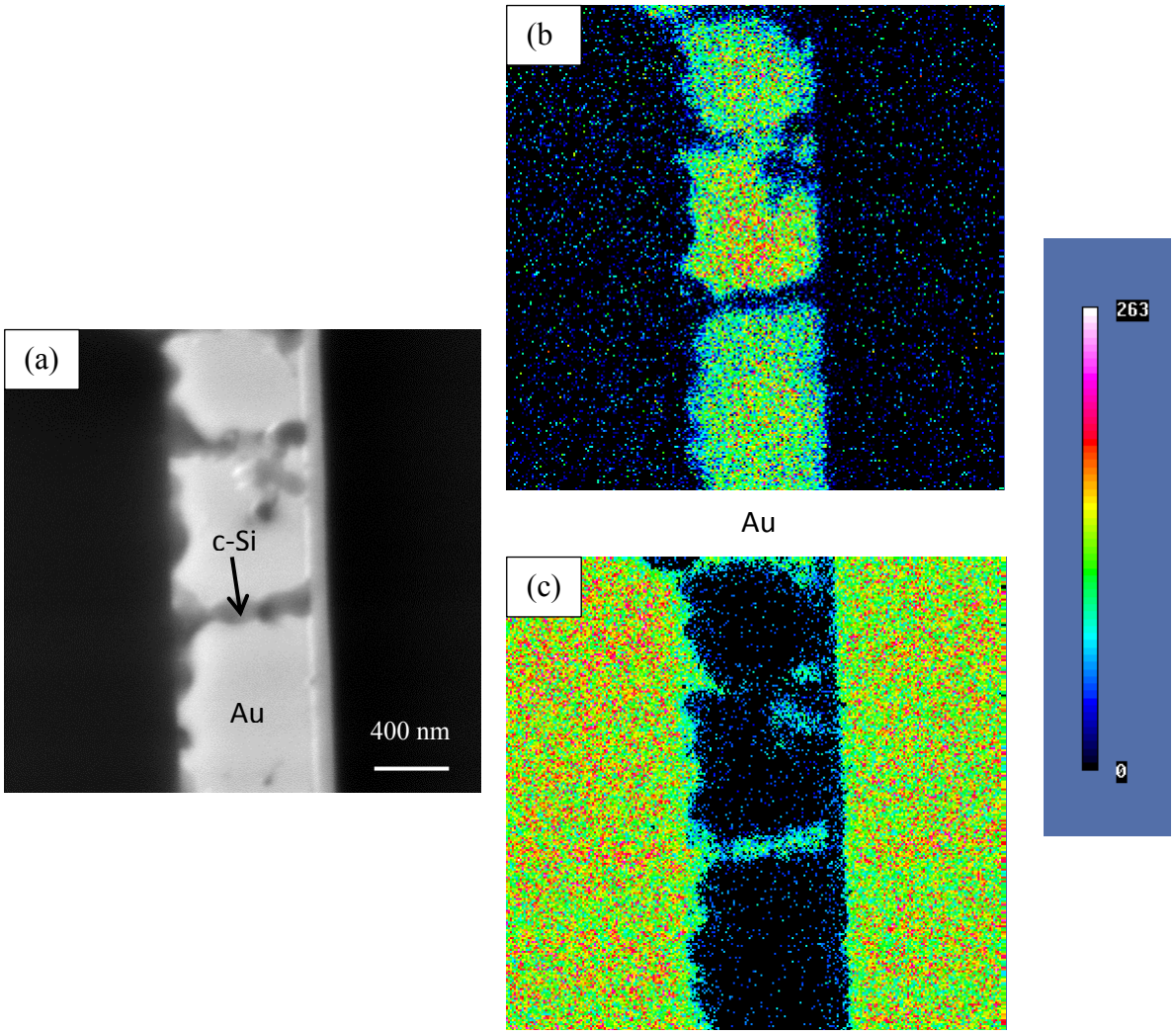


Figure 6.12. AES map taken from the (a) SE SEM cross section image of the sample bonded at 350°C for 20 min. (b) Au map and (c) Si map of a non-crater area in the c-Si eutectic bonded sample.

6.4. c-Si solid-state bonding

Solid-state c-Si bonding was performed at 350°C for 20 min. The same bonding pressure that was used for solid-state a-Si bonding (0.06 MPa) was applied here. SAM images are shown in Figure 6.13. The bonding experiment was repeated two times, but similar SAM results were obtained. For both wafers, there is a large unbonded area in the middle of the wafer. Pieces from the centre region completely detached during wafer dicing. The pressure was increased to 0.12 MPa and the SAM image is shown in Figure 6.14. The unbonded area became smaller but still exists. Increasing the pressure above the 0.12 MPa resulted in wafer breakage.

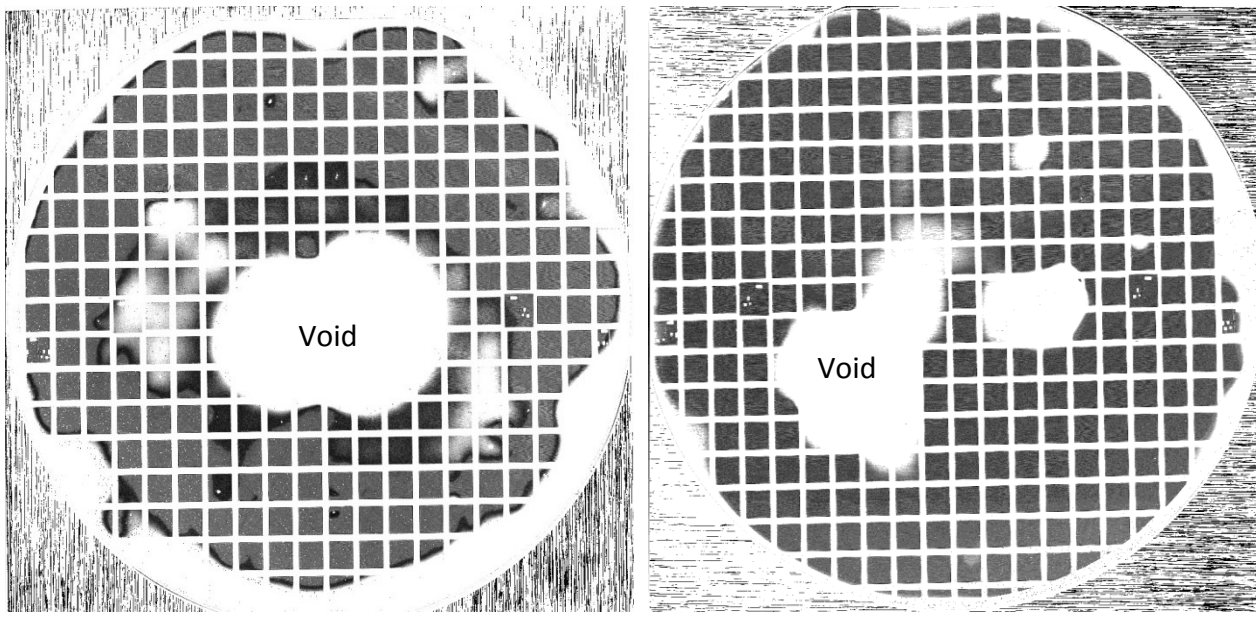


Figure 6.13. SAM images of c-Si solid state pairs bonded at 350°C for 20 min s. The bond test was repeated at a pressure of 0.06 MPa.

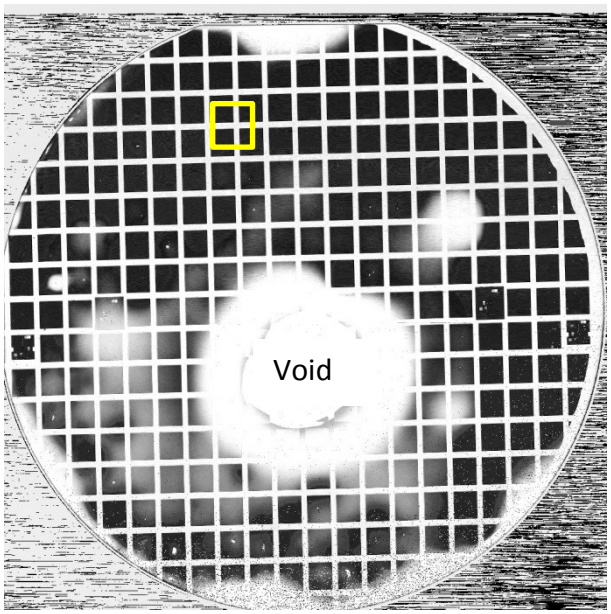


Figure 6.14. SAM image for c-Si solid state pair bonded at 350°C for 20 min at a pressure of 0.12 MPa.

A cross section sample of the area, indicated by the rectangle in Figure 6.14, was prepared and is shown in Figure 6.15. The size of the craters is considerably smaller compared with the eutectic bonded c-Si. The average size of the craters was less than 200 nm. The columnar microstructure of Au can be observed in Figure 6.15(b) and there are no large Si particles visible in the cross section at these magnifications. AES mapping of Au and Si was done on the cross section sample and the results are shown in Figure 6.16. The distribution of elements shows mostly Au at the interface.

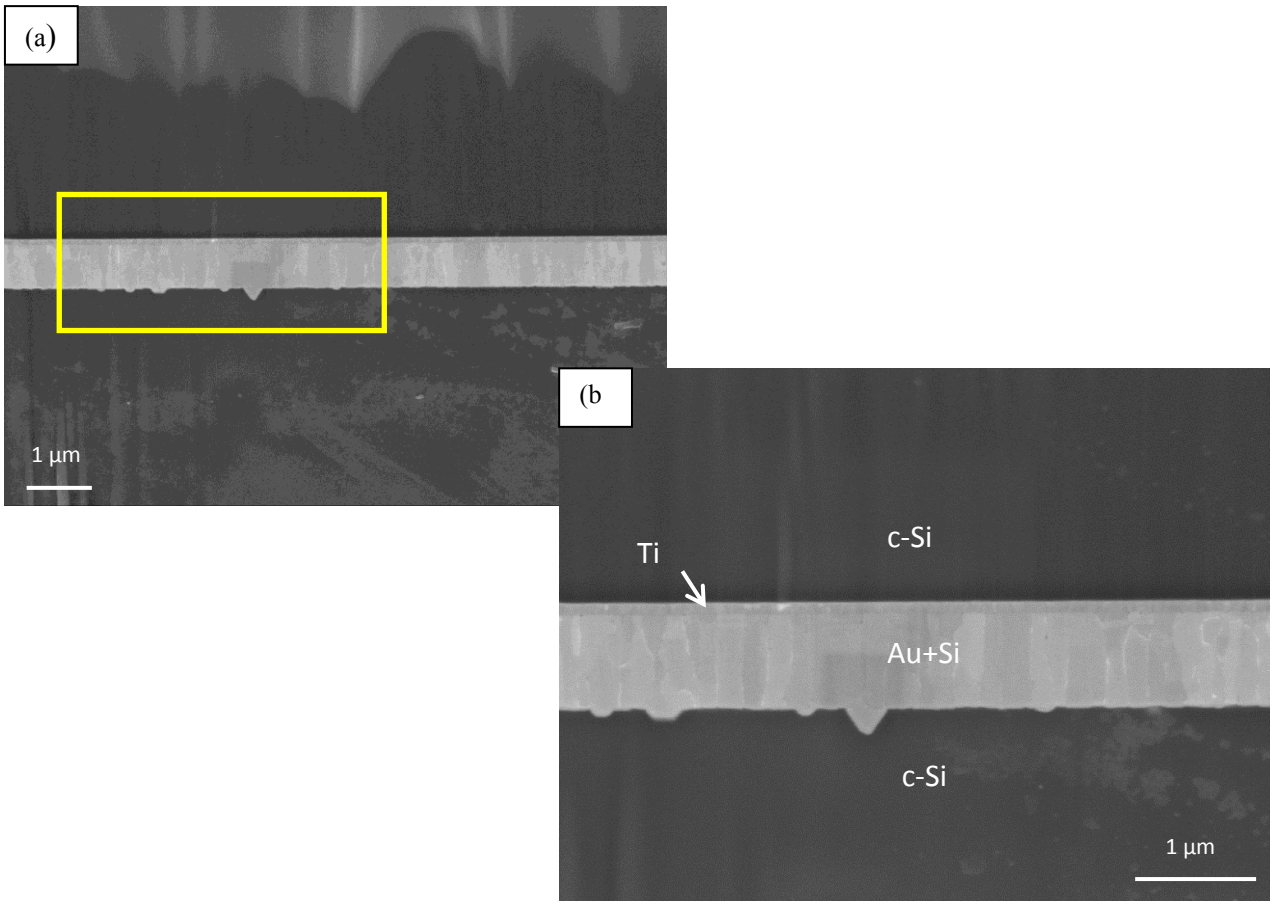


Figure 6.15. SEM SE cross section images of solid-state c-Si bonded sample region shown in Figure 6.14, bonded at 350°C for 20 min. (a) Low magnification image and (b) higher magnification image of the rectangle area in (a).

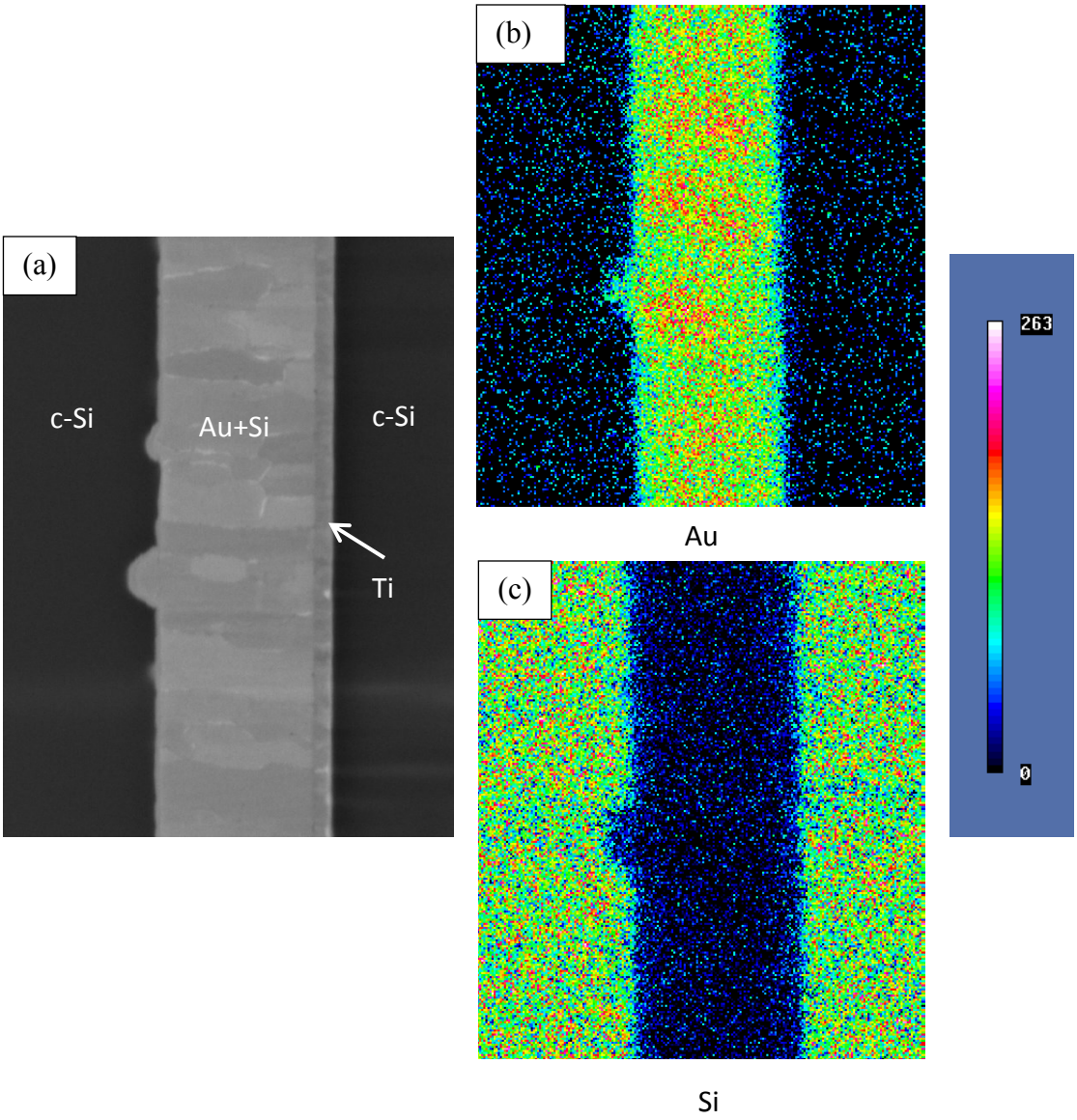


Figure 6.16. AES map taken from the (a) SE SEM cross section image. (b) Au map and (c) Si map of c-Si solid-state bonded sample.

6.5. Shear testing

Shear testing was performed on different samples for comparison. For each bonding configuration, 4 samples were chosen for shear testing. The Student's t-distribution method, shown in Equation (6.1) [114] was used to find the suitable sample size for shear testing.

$$t = \frac{\bar{X} - \mu}{\frac{S}{\sqrt{n}}} \quad (6.1)$$

where

$\bar{X}$ is the mean of the sample population

μ is the mean of the total population

S is the standard deviation of the sample population

n is the sample size

t can be found for a specific degree of confidence in the T table [114]. The difference between mean shear strength was calculated for a total population of 3 and 4 and also for a sample size of 4 and 5 as 17% and 7% respectively. The larger the population, the more accurate results that are obtained; however, the difference between results from sample size 4 and 5 is negligible. Due to time limitations and the number of samples that could be tested, a sample size of 4 was chosen for the current shear test experiments.

The shear strength for the a-Si eutectic bonded samples, without SC1 cleaning prior to bonding, was measured and compared with a-Si eutectic bonded samples, with SC1 cleaning prior to bonding. The results are plotted in Figure 6.17. The average shear strength of the samples cleaned with SC1 was 17.7 MPa while the samples not cleaned with SC1 showed an average shear strength of 13.1 MPa. Samples were selected from well-bonded parts of the wafer. These results show the effectiveness of cleaning on the shear strength, as well as the bond uniformity, which was demonstrated in Section 6.1.

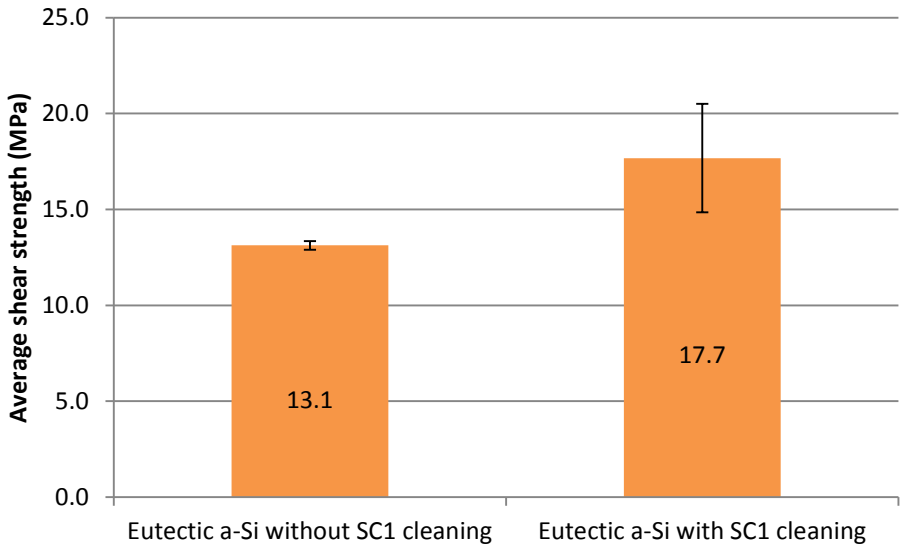


Figure 6.17. Average shear strength comparison of a-Si eutectic bonded samples with and without SC1 cleaning prior to bonding.

The a-Si samples prepared via eutectic bonding and solid-state bonding were also compared in terms of shear strength. The results are shown in Figure 6.18. The average shear strength for solid-state bonded a-Si is 17.0 MPa, while the average shear strength is 17.7 MPa for eutectic bonded a-Si. Since the results are similar, using solid-state bonding is preferable because of lower process temperatures, higher bond strength and no spill out issues.

The shear strengths were also measured for solid-state and eutectic c-Si bonded samples and are shown in Figure 6.19. The average shear strength for solid-state bonded c-Si was 26.6 MPa while for eutectic bonded c-Si it was 13.5 MPa. These results are expected as the eutectic bonded c-Si samples had larger craters and a coarser microstructure (Figure 6.9) compared with the solid-state bonded c-Si samples, which had a finer structure and relatively small craters (Figure 6.15). The finer scale microstructure should improve the mechanical robustness for packaging.

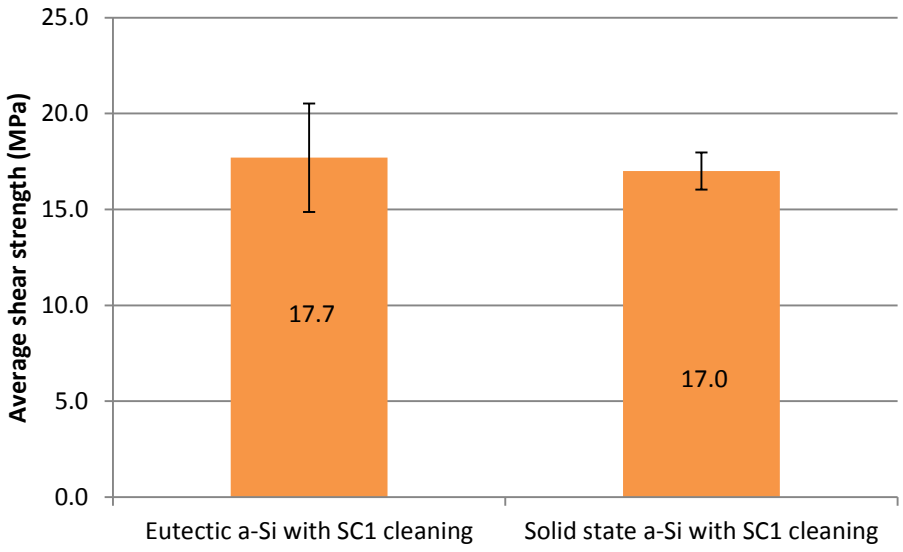


Figure 6.18. Average shear strength comparison of a-Si eutectic bonded samples with solid-state bonded samples.

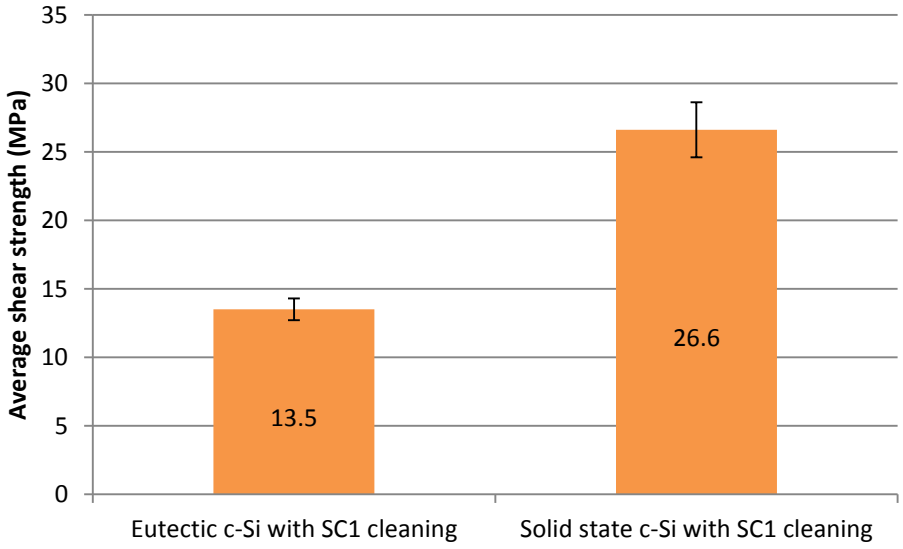


Figure 6.19. Shear strength comparison of a-Si eutectic bonded sample with solid-state bonded samples.

Comparison of the a-Si and c-Si samples, joined through eutectic bonding, shows similar results; shear strength of 13.1 MPa with a standard deviation of 0.66 MPa for a-

Si samples and a shear strength of 13.5 MPa with a standard deviation of 1.59 MPa for c-Si.

For solid-state bonding, the average shear strength for solid-state bonded c-Si (26.6 MPa) was far higher than the average shear strength for a-Si (17 MPa). One possible reason may be the formation of small craters in c-Si samples, which can act as mechanical locks and increase the shear strength of the bond. Also, Si grains in solid-state c-Si samples are much smaller than the grains formed in a-Si, which may strengthen the bonds. However, it should be pointed out again that the samples were selected from well-bonded areas on each wafer. Large voids, present in the c-Si solid state bonded samples, are not acceptable in terms of robustness and mechanical strength and may be localized stress concentration points leading to bond failure in the package. Shear strengths of 9.2-15.3 MPa were reported by E. Jing [48] for Au/c-Si eutectic wafer bonding. The data obtained in this work is also in that range. S. Bushra [10] also reported average shear strengths of 7-20 MPa for Au/c-Si eutectic wafer bonding.

6.5. Summary

This chapter focused on full wafer bonding of Au/a-Si and Au/c-Si using eutectic and solid state methods. The a-Si samples attached using eutectic bonding had uniform bonds across the wafer; however, localized spill out could not be avoided. Using SC1 cleaning prior to HF cleaning provided a reduction in surface contamination and improved bonding. Solid-state bonding of a-Si samples demonstrated uniform bonding without spill out; however, small amounts of voiding at the interface of the two wafers after bonding was observed due to surface roughness and lack of liquid formation in solid-state bonding. The bond achieved using c-Si eutectic bonding was uniform across the wafer; however, the formation of large craters in the c-Si was unavoidable. Full wafer bonding using the c-Si solid state method resulted in large void formation and unbonded areas between the two wafers, which did not improve by increasing the bonding pressure. Shear strength results on the well-bonded areas of the wafers

indicated similar results for eutectic and solid-state bonding for a-Si; however, higher shear strengths for solid state bonding of c-Si compared with eutectic bonding was obtained due to the finer microstructure for the former. In both cases, solid-state bonding is preferable because of lower process temperatures, higher bond strength and no spill out issues.

Chapter 7

In-Situ TEM Experiments

Chapter 7 - In-Situ TEM Experiments

7.1. Introduction to In-situ TEM

In-situ transmission electron microscopy (TEM) provides the ability to observe and record events as they occur in real time. In order to observe the layer exchange mechanism, step-by-step, annealing experiments were performed in-situ in a Hitachi H9500 Environmental TEM, operating at 300 kV.

7.2. Imaging modes

There are two basic modes of imaging in the TEM: bright field (BF) and dark field (DF). Probably the most widely used condition is BF imaging. For BF imaging, an aperture is placed in the back focal plane of the objective lens in a way that only the undiffracted electron beam is selected for image formation. Both the undiffracted beam and the objective aperture should lie along the optic axis of the microscope to reduce spherical aberration in the final image. For DF imaging, only the selected diffracted electron beam contributes to the final image. For DF imaging, the diffracted beam and the objective aperture lie along the optical axis of the microscope, again to reduce spherical aberration in the final image.

Three Au (50 nm)/a-Si (60 nm)/c-Si diffusion couple samples were prepared by FIB methods and annealed at three different temperatures of 250, 300 and 350°C. TEM BF cross section images of the FIB polished sample before annealing are shown in Figure 7.1. The dark layer in the Figure 7.1 is the Au layer and the lighter color layer just beside it is the a-Si layer. Similar to observations in Section 4.1.1, interdiffusion of Au and Si occurred even at room temperature (shown by arrow in Figure 7.1) as a result of the unstable structure of a-Si. The FIB samples were made 2 days before starting the in-situ annealing experiments. A sample was then put into the TEM chamber and the vacuum was established before heating was started to the desired temperature.

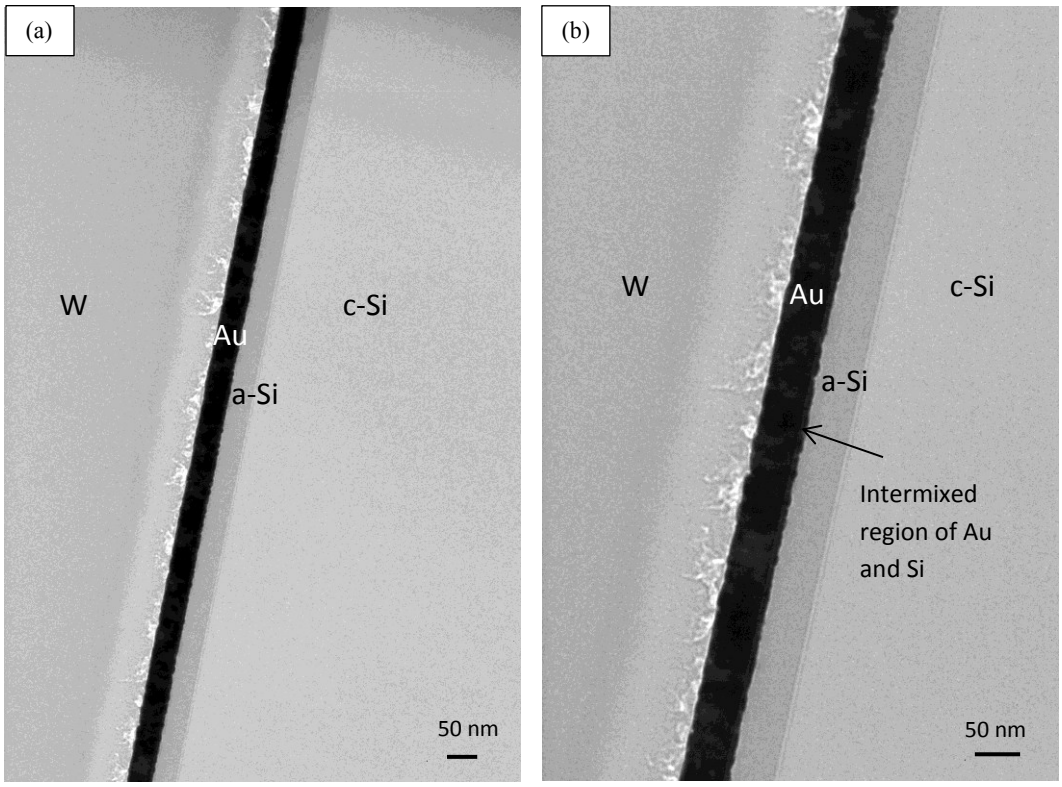


Figure 7.1. BF TEM cross section images of FIB polished Au/a-Si/c-Si sample before annealing. (a) Low magnification and (b) higher magnification images.

7.3. Annealing at 250°C

A FIB sample was heated to 250°C in 10 min. Only a few images were taken during this 10 min period, since image drift was significant during heating. Figure 7.2 shows an image of the sample taken after 600 s during the 10 min heating to 250°C. As can be observed, more interdiffusion has happened and the Au/a-Si interface is shifting as well. After the temperature stabilized and image drifting subsided, imaging was started. BF images were taken at 1 s intervals. There was some drifting of the sample, which could not be avoided.

As mentioned in Chapter 2, Au acts as a catalyst for the crystallization of a-Si. This results in crystallization temperatures as low as 250°C compared with the regular crystallization temperature of a-Si (around 700°C). There are two microscopic theories for explaining the catalytic effect of metals in contact with a-Si. Hiraki [115][116]

showed that in order to observe crystallization, four or more monolayers of Au need to be deposited on a-Si. He concluded that some kind of bulk metal must have formed. The bulk metal forms a free electron gas. The wave function of this free electron gas will extend into the a-Si covalent band and weaken the bonds. As a result, crystallization happens more quickly.

The second model was proposed by Tu [99]. He proposed an interstitial model for near noble transition metals. Inserting this metal atom into an interstitial position of the Si lattice will lead to the transfer of an electron from the covalent bond surrounding this atom to the metal. The result is weakening of the bonds around it and enhancement of crystallization.

MIC was studied in different systems by in-situ TEM [117][118][79][119][120] .The driving force behind MIC is the reduction in the free energy of Si by transformation from a-Si to c-Si. As MIC is based on diffusion mechanisms, it is expected to be time dependent.

Figure 7.3 shows some examples of images taken at 250 s intervals. Comparing Figure 7.2 and Figure 7.3 (a), which were taken at 600 s and 850 s, respectively, it is clear that the amount of diffusion of Au in a-Si increases with increasing annealing time. At 850 s, the formation and crystallization of the first c-Si grain in the Au layer was observed in the area of interest. Crystallization started at the Au/a-Si interface and inside the Au layer.

Figure 7.3 (b), taken at 1100 s, shows the growth of the c-Si grain, which at the same time pushes the Au atoms into the a-Si layer. More diffusion of Au in a-Si can be seen around this c-Si grain. Figure 7.3 (c), taken at 1350 s, shows the continuous growth of the c-Si grain and the migration of Au into the a-Si layer.

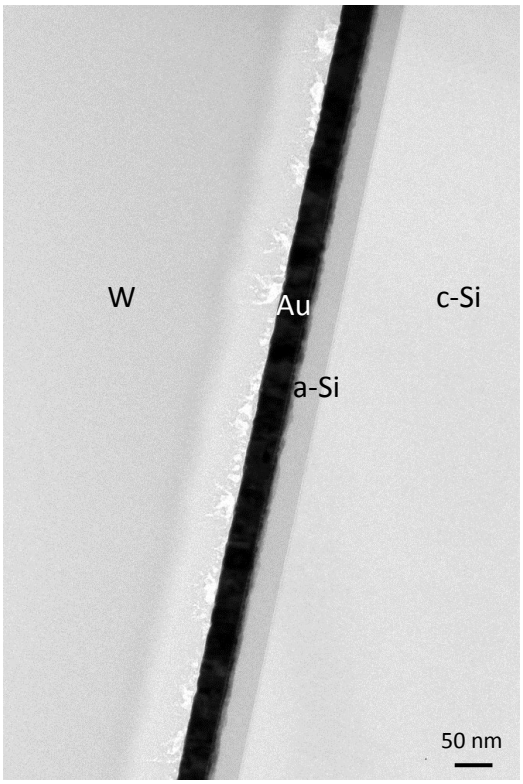
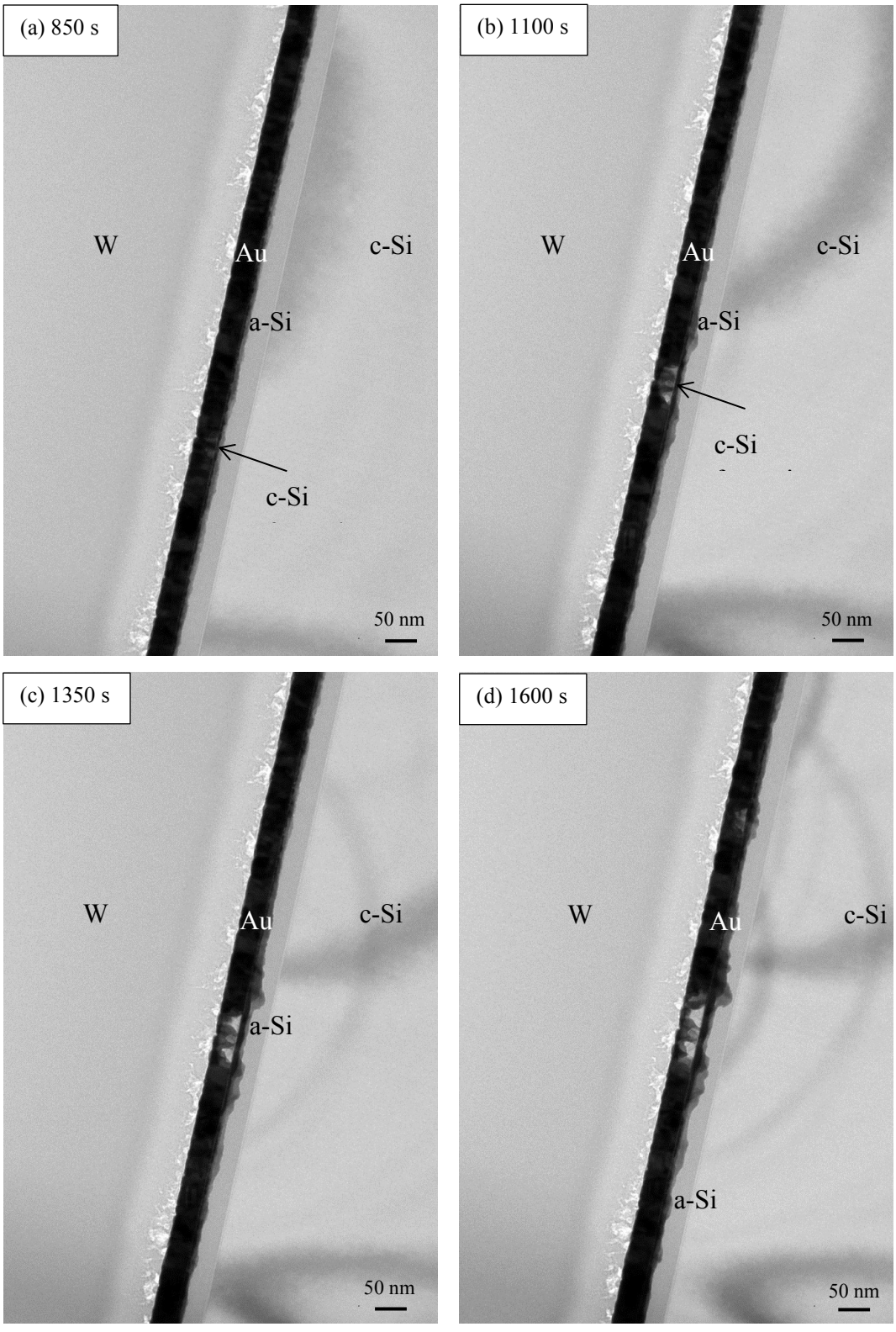
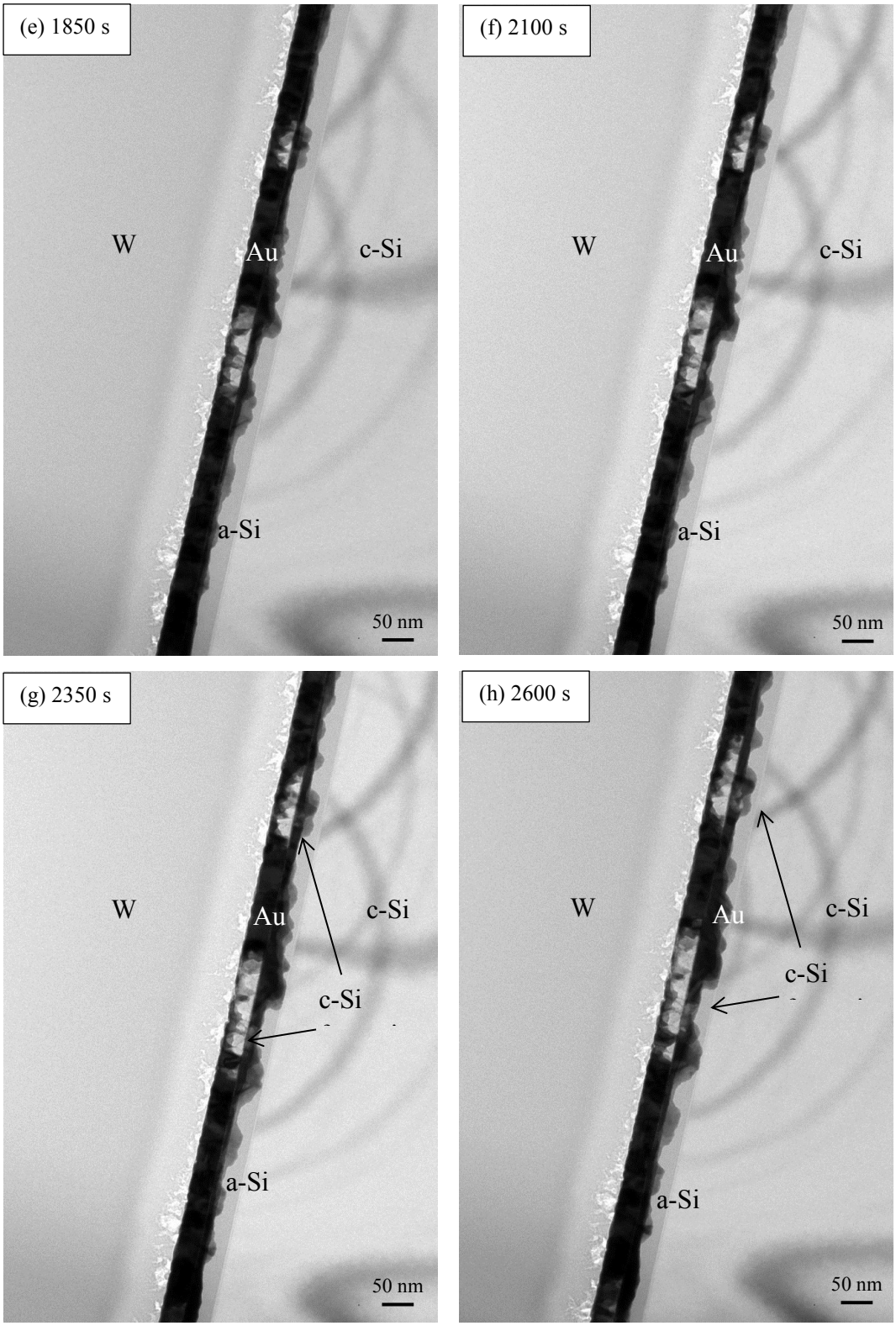
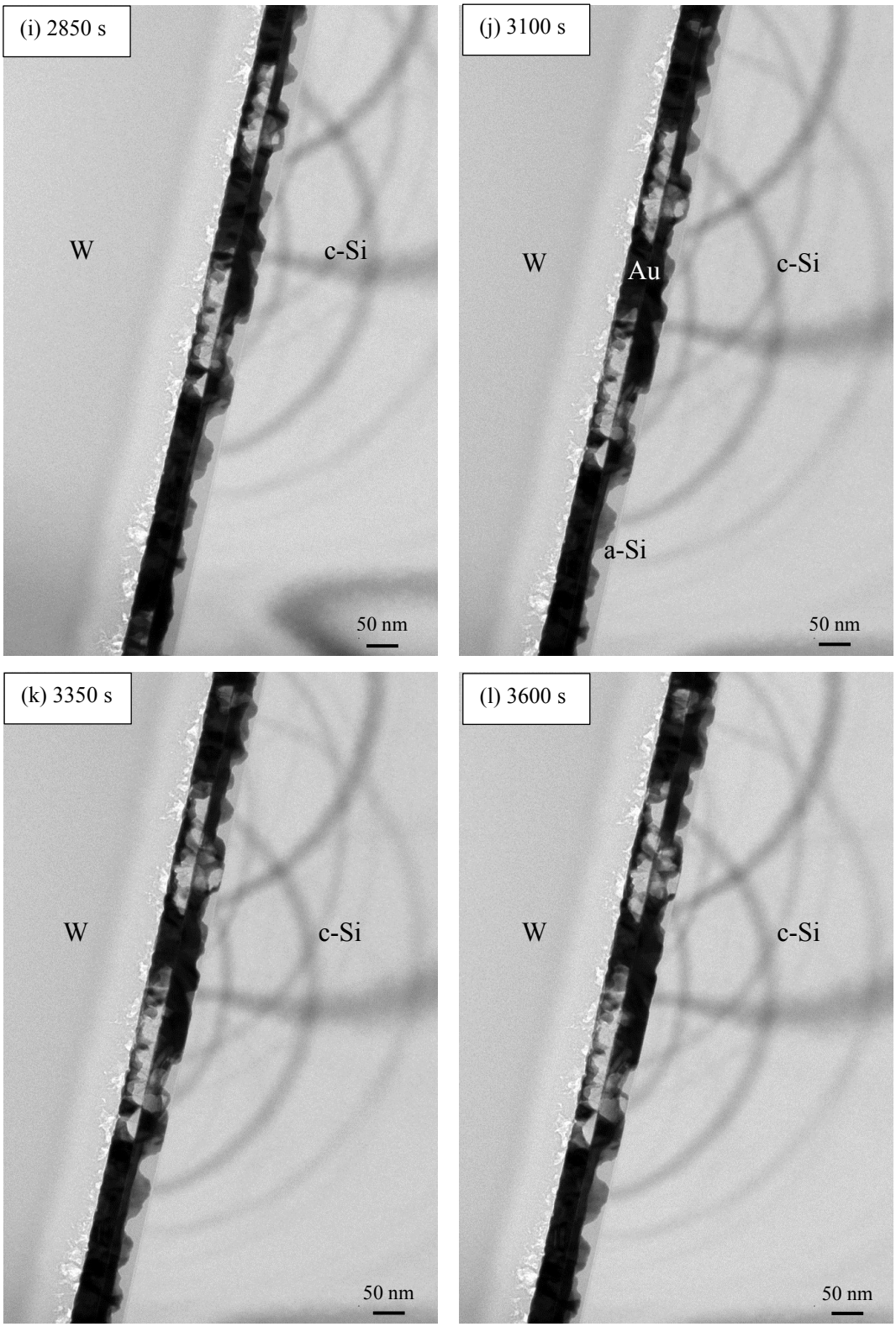
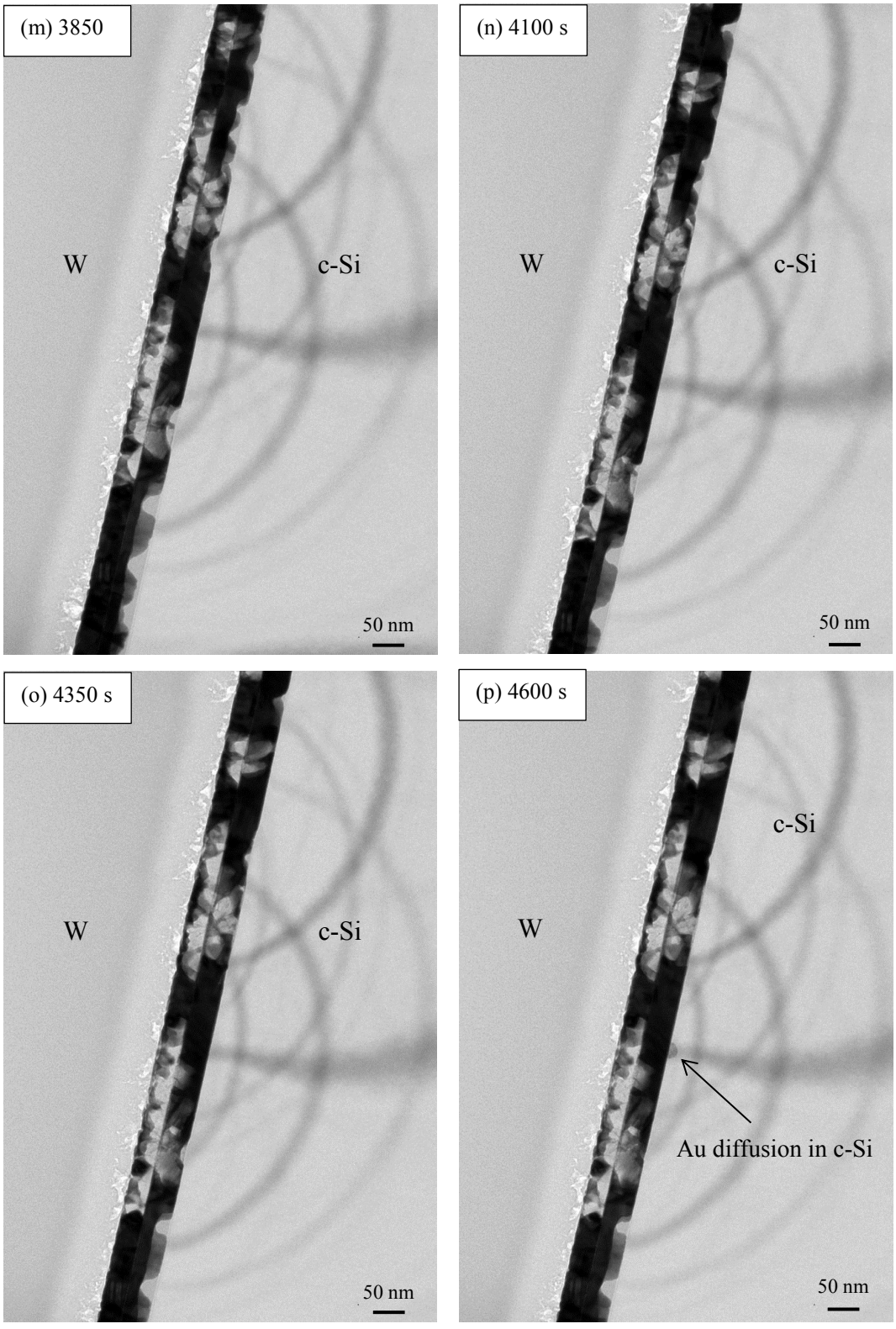


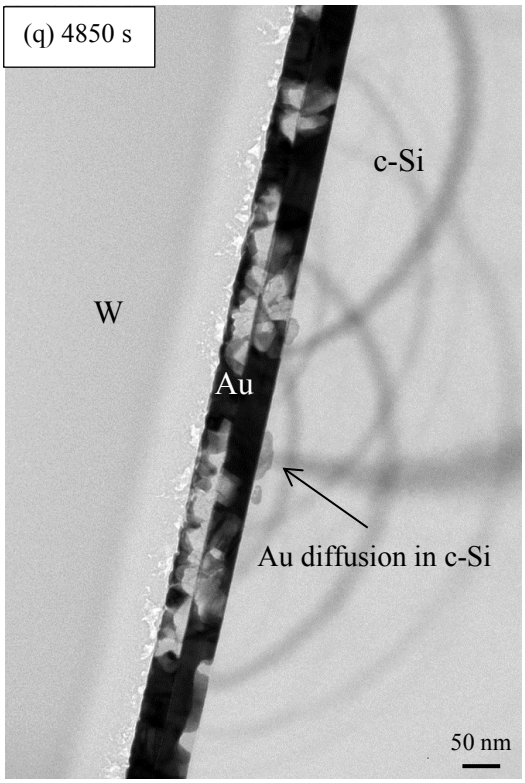
Figure 7.2. BF TEM cross section image of FIB polished Au/a-Si/c-Si sample after reaching 250°C in 600s.

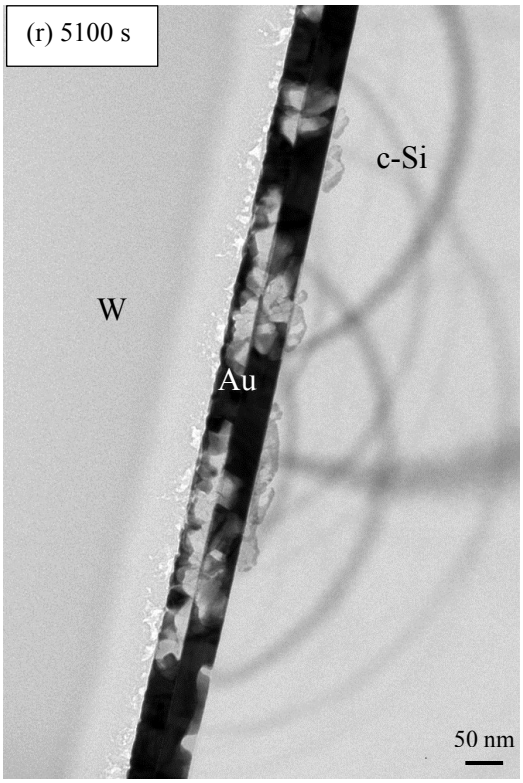

(a) 850 s
W
Au
c-Si
a-Si
c-Si
50 nm
(b) 1100 s
W
Au
c-Si
a-Si
c-Si
50 nm
(c) 1350 s
W
Au
c-Si
a-Si
50 nm
(d) 1600 s
W
Au
c-Si
a-Si
50 nm


(e) 1850 s
W
Au
c-Si
a-Si
50 nm
(f) 2100 s
W
Au
c-Si
a-Si
50 nm
(g) 2350 s
W
Au
c-Si
c-Si
a-Si
50 nm
(h) 2600 s
W
Au
c-Si
c-Si
a-Si
50 nm


(i) 2850 s
W
c-Si
50 nm
(j) 3100 s
W
Au
c-Si
a-Si
50 nm
(k) 3350 s
W
c-Si
50 nm
(l) 3600 s
W
c-Si
50 nm


(m) 3850
W
c-Si
50 nm
(n) 4100 s
W
c-Si
50 nm
(o) 4350 s
W
c-Si
50 nm
(p) 4600 s
c-Si
W
Au diffusion in c-Si
50 nm


(q) 4850 s
c-Si
W
Au
Au diffusion in c-Si
50 nm


(r) 5100 s
c-Si
W
Au
50 nm

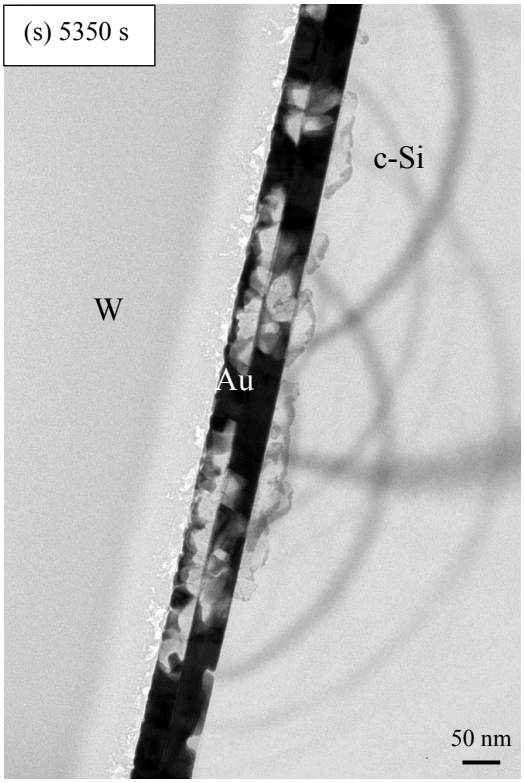

(s) 5350 s
c-Si
W
Au
50 nm

Figure 7.3. BF cross section TEM images of Au/a-Si/c-Si sample annealed at 250°C for (a) 850 s, (b) 1100 s, (c) 1350 s, (d) 1600 s, (e) 1850 s, (f) 2100 s, (g) 2350 s, (h) 2600 s, (i) 2850 s, (j) 3100 s, (k) 3350 s, (l) 3600 s, (m) 3850 s, (n) 4100 s, (o) 4350 s, (p) 4600 s, (q) 4850 s, (r) 5100 s and (s) 5350 s.

At 1600 s, the formation of a second c-Si grain was observed which is shown by the black arrows in Figure 7.3 (d). In addition, more Au diffusion in the a-Si layer happened as a result of the formation of the c-Si grain and Au rejection. At 1850 s (Figure 7.3 (e)), at the location shown by the black arrow, Au has diffused all the way into the a-Si layer and has reached the a-Si/c-Si interface. Rather than diffusing into c-Si, Au diffuses laterally in a-Si, as shown in Figure 7.3 (f) taken at 2100 s, since a-Si has a more open structure than c-Si. The growth of c-Si grains and the diffusion of Au in a-Si continue to happen at 2350 s, as shown in Figure 7.3 (g). The appearance of first c-Si grain in the a-Si layer occurred at 2600 s (Figure 7.3 (h)), shown by the arrows, which corresponds to the first c-Si grain reaching the free surface. After this point the grain grows not only laterally but also into the a-Si layer. From the 2850 s (Figure 7.3 (i)) to 4350 s (Figure 7.3 (o)), the growth of c-Si grains in both the Au and a-Si layers continues and, at the same time, Au diffuses laterally in the a-Si layer without diffusing into c-Si. At 4600 s (Figure 7.3 (p)), the entire a-Si has crystallized and layer exchange has happened to a large extent. At this point, the first appearance of Au diffusion into c-Si is observed. This is shown by the arrow in Figure 7.3 (p). From 4600 s (Figure 7.3 (p)) to the end of the experiment, the major observable change was additional diffusion of Au in c-Si.

A model is proposed for a-Si MIC and is illustrated in Figure 7.4. Step 1 involves interaction between Au and a-Si, Au diffusion and precipitation in a-Si and crystallization at the Au/a-Si interface. Although the phase diagram shows no solubility for Au and Si (c-Si) in each other (Figure 7.4 (a)), dissolution of Au in a-Si is relatively high due to the high density of defects present in a-Si.

During sputtering of Au on a-Si, the a-Si substrate temperature can rise to as high as 200°C. This can lead to the formation of an Au and Si mixed region at the Au/a-Si interface (Figure. 7.1 (b)). Sputtering, along with the temperature rise, can result in the formation of localized metastable phases. A wide variety of compositions (from 10 at.% Si to 90 at.% Si) have been observed by many researchers [121]. It was shown by Chromik et al. [121] that heating above 270°C will result in decomposition of metastable silicides to the equilibrium components of Au and c-Si. The c-Si nuclei formed in the mixed layer will later grow within the Au layer. The observations in Figure 7.3 indicate that c-Si grows faster within the Au layer compared with the a-Si layer. This behaviour could be explained in light of the interfacial strains created at the c-Si and a-Si interface. From thermodynamic stand point the driving force for transformation of a-Si to c-Si could be expressed as Equation 7.1.

$$\Delta G^{a-Si \rightarrow c-Si} = \Delta G^{Chem} + \Delta G^{Mech} \quad (7.1)$$

ΔG^{Chem} is the reduction in the energy of the system due to creation of the missing bonds and increase in the order of the Si structure and acts as a driving force in favor of the reaction. On the other hand, ΔG^{Mech} is a positive energy term that act as inhibitor for crystallization. This energy is created due to mismatch of density of a-Si and c-Si (5% density increase on going from a-Si to c-Si) and it is stored in the interfacial stress fields in both a-Si and c-Si. This stress field plays a crucial role in the kinetics of crystallization of a-Si. If the mechanical stress created during transformation is not released by plastic deformation or dislocation creation, accumulation of this stress at some point will lead to permanent halt of transformation. Considering that Si exhibits negligible plastic deformation, this strain needs to be accommodated elastically on both sides of the interface. As Au has a lower much lower yield stress compared to a-Si, it can deform easily to accommodate interfacial stresses.

The loosened Si atoms leave the a-Si layer (step 1 in Figure 7.4 (b)) and join the stable nuclei through the Au layer likely along grain boundaries (Step 2 in Figure 7.4 (b)). Through continued diffusion, the nuclei grow in all directions in the Au layer until they

reach the Au free surface. The nuclei continue to grow laterally afterwards. Growth of the Si grains in the Au layer will push the Au toward the a-Si layer.

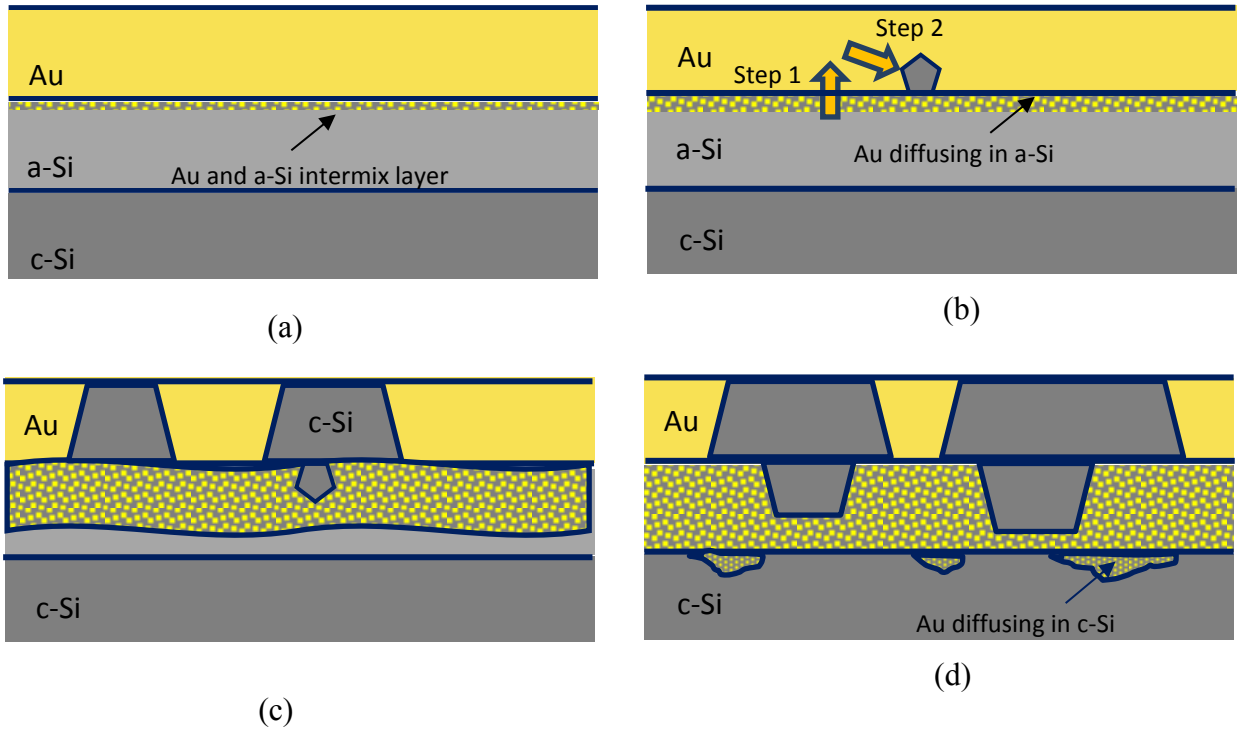


Figure 7.4. Schematic of the steps in the layer exchange mechanism for Au/a-Si/c-Si during annealing. (a) Initial wafer stacking before annealing. The intermixed layer is formed due to sputtering. (b) Formation of c-Si nuclei due to possible decomposition of metastable phases. The growth of nuclei continues by joining Si atoms through the Au layer. (c) C-Si growth in the Au layer. Eventually the concentration of Au in a-Si reaches a point where crystallization starts in the a-Si layer. (d) Au concentration in a-Si layer reaches the saturation point and pushes the extra Au into c-Si.

When the Au concentration in the a-Si layer reaches a certain level (this level was not quantitatively measured in this project), the remaining a-Si layer will crystalize in the a-Si layer (Figure 7.4 (c)). The Si nuclei form at the a-Si/Au interface, at a location adjacent to previously formed Si grains in the Au layer, which are preferential nucleation sites due to a similar crystal structure. The formation of more c-Si grains in

the a-Si layer and the growth of other Si grains in the Au layer will result in Au being pushed into the c-Si layer (Figure 7.4(d)).

7.4. Annealing at 300°C

A similar FIB sample was fabricated and heated to 300°C in 10 min. Figure 7.5 shows the FIB sample before annealing. Small interdiffusion areas are present at the Au/a-Si layer interface at room temperature (indicated by the arrow).

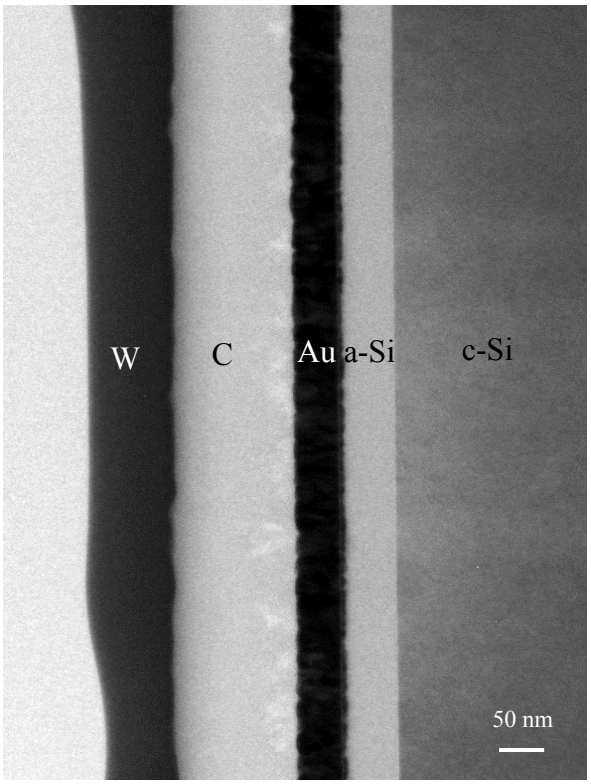


Figure 7.5. BF TEM cross section image of FIB polished Au/a-Si/c-Si sample before annealing.

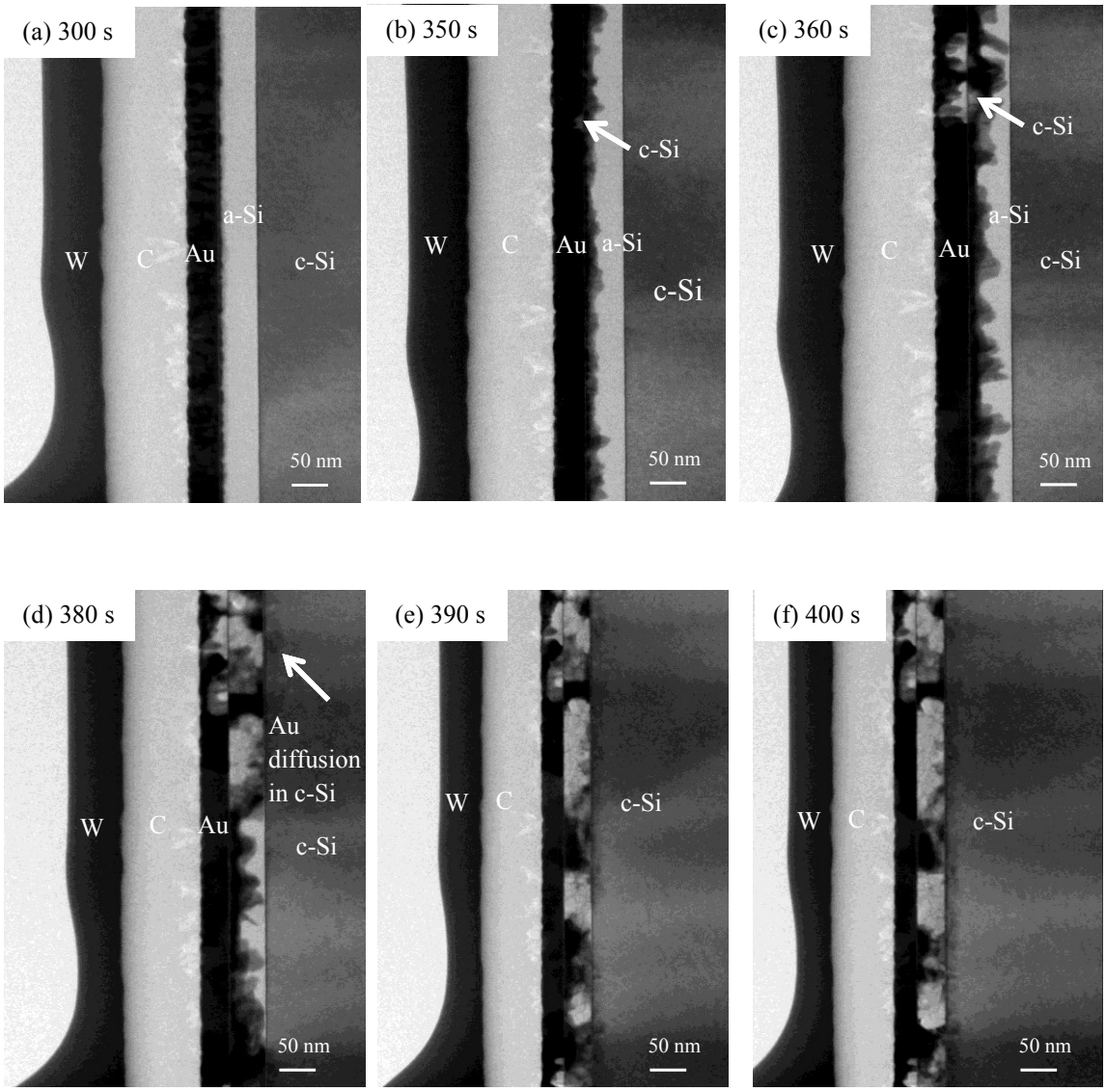
Images were taken at 1s intervals. Figure 7.6 (a) shows the image taken at 300 s during the 10 min sample heating stage. The diffusion depth of Au in a-Si can be observed more clearly in this image. The reaction rate at 300°C is faster compared with the previous 250°C annealing results and most of the a-Si crystallization happened during the 10 min heating stage.

At 350 s, the appearance of the first c-Si grain is observed, as shown by the arrow, in Figure 7.6 (b). The high diffusion rate of Au in a-Si is evident by comparing Figure 7.6 (a) with Figure 7.6 (b). Figure 7.6 (c) is taken 10 s after the image in Figure7.6 (b) and shows the high growth rate of c-Si grains. Drifting could not be avoided during sample heating.

Another interesting phenomenon observed in the annealed sample at 300°C, compared with the images for the sample annealed at 250°C, is the higher nucleation rate for c-Si at higher temperature. For the images taken from the sample annealed at 250°C, a few nuclei form during annealing and these grow and join together. However, for the sample annealed at 300°C, several c-Si nuclei form.

The same mechanism for layer exchange at 250°C sample occurs at 300°C, with the difference being the higher nucleation rate at 300°C. At higher temperature, the rate of Au diffusion in the a-Si layer is higher compared with samples annealed at 250°C which results in a large amount of Au in the a-Si layer in a short time (about 350 s). The effect of strain produced from c-Si formation is less pronounced in the presence of high amount of Au in a-Si; therefore, crystallization in a-Si starts shortly after crystallization within the Au layer at 300°C (at 370 s, Figure 7.6 (c)). Subsequently, most of the a-Si crystallization and growth takes place inside a-Si layer.

The higher diffusion rate of Au in a-Si layer at 300°C vs 250°C results in faster transport of Au atoms across this layer (diffusion time of 380s vs 4600s, respectively) Figure 7.6(d). During the remaining annealing time, the Si crystals grow and more Au diffuses into the c-Si layer.


(a) 300 s
W
C
Au
a-Si
c-Si
50 nm
(b) 350 s
c-Si
W
C
Au
a-Si
c-Si
50 nm
(c) 360 s
c-Si
a-Si
W
C
Au
c-Si
50 nm
(d) 380 s
Au
diffusion
in c-Si
W
C
Au
c-Si
50 nm
(e) 390 s
W
C
c-Si
50 nm
(f) 400 s
W
C
c-Si
50 nm

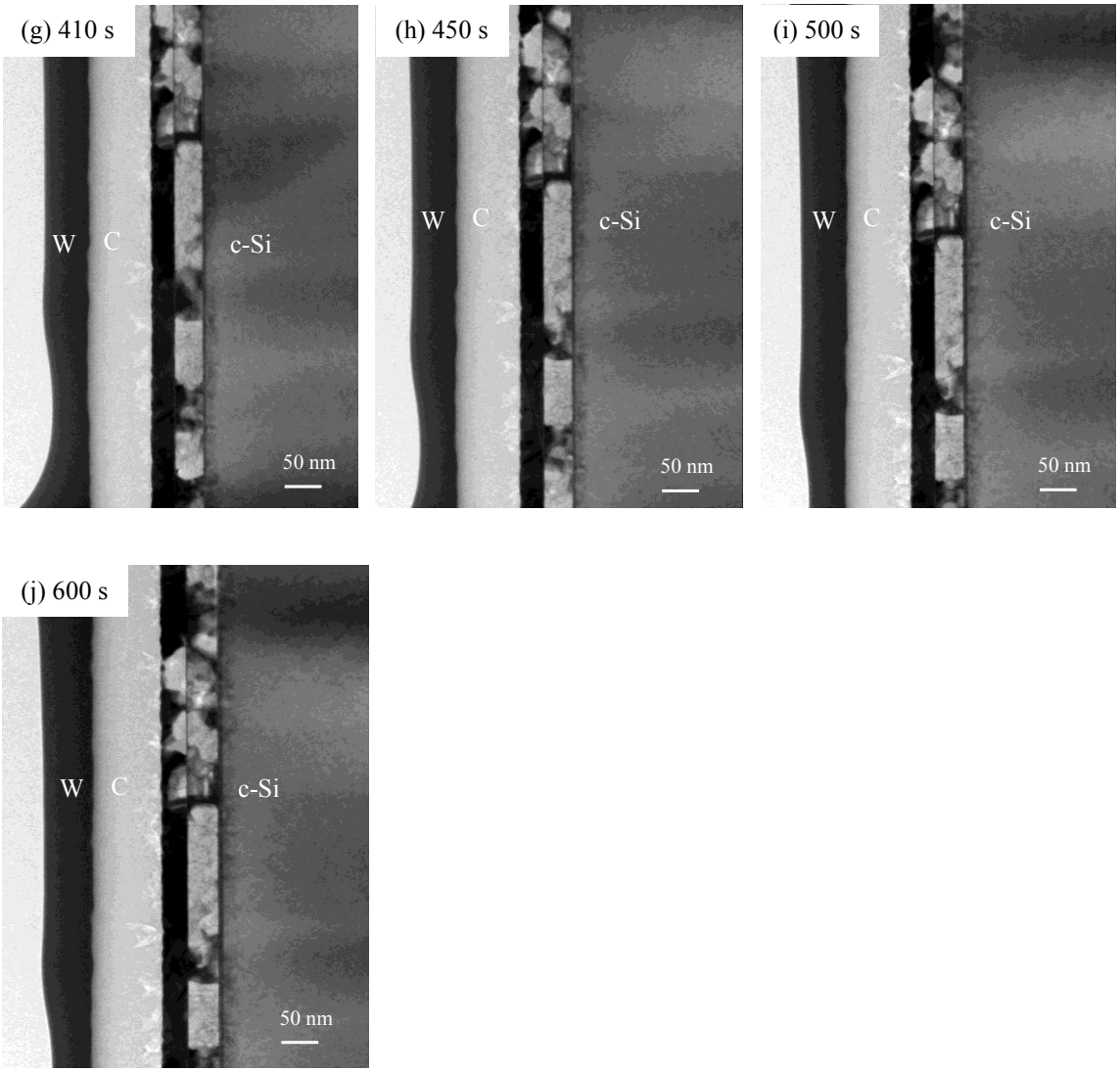


Figure 7.6. BF cross section TEM images of Au/a-Si sample during pre-heating to 300°C at (a) 300 s, (b) 350 s, (c) 360 s, (d) 380 s, (e) 390 s, (f) 400 s, (g) 410 s, (h) 450 s, (i) 500 s and (j) 600 s.

7.5 Summary

In-situ TEM imaging was performed on Au/a-Si/c-Si samples in order to better understand the layer exchange mechanism in the Au/Si system. Annealing was performed at 250°C and 300°C to compare the reaction rates. From the observations, there appears to be an intermixed layer at the Au/a-Si interface of the as-deposited sample. This intermixed layer is formed during Au sputtering onto the a-Si layer, which can also result in the formation of metastable phases. These metastable phases transform into equilibrium phases during heating. This transformation is the source for the first nuclei formation inside that intermixed layer. Due to the increase in strain during the formation of c-Si, the nuclei prefer to grow in a softer phase (Au) rather than in a-Si. The rate of nucleation at 300°C is higher compared to 250°C. Gold eventually reaches and diffuses into the c-Si layer.

Chapter 8

Conclusions and Recommendations for Future Work

Chapter 8 - Conclusions and Recommendations for Future Work

8.1. Main conclusions

This final chapter summarizes the work during this project and summarizes the main conclusions and results obtained.

The work focused on Au and Si wafer bonding for microelectronic packaging applications and compared the microstructure, mechanical properties and bond yield for a-Si and c-Si during bonding. Eutectic bonding was chosen between various methods of bonding due to the high strength bonds obtained, good hermeticity and the lack of sensitivity to the surface conditions.

In Chapter 4, the diffusion properties and the microstructures formed during annealing of Au/a-Si/c-Si and Au/c-Si samples were demonstrated and explained in detail. As expected, annealing the Au/c-Si diffusion couple resulted in the formation of craters at the Au/c-Si interface due to the preferential dissolution of c-Si. Depending on the temperature and duration of annealing, different sizes of craters were obtained. TEM analysis of the crater area indicated that they were filled with Au. Although forming gas was used for annealing the samples, a layer of Si oxide was detected on the Au surface.

For industrial applications, the presence of large craters can damage the active devices on the wafers and should be limited as much as possible. Since a-Si does not exhibit preferential dissolution, a-Si was deposited on c-Si to limit the formation of craters. During annealing, a-Si is not stable due to its high free energy and it needs to stabilize itself by crystallization. The crystallization temperature for a-Si is very high (around 700°C); however, the presence of Au acts as a catalyst for the crystallization process and reduces the temperature to about 200°C. During annealing, nucleation and growth of c-Si was observed, starting from Au/a-Si interface and growing into the Au layer. The a-Si layer eventually crystallized completely by diffusion of Au into it.

In Chapter 5, the results of small sample bonding were demonstrated. Both a-Si and c-Si were utilized for wafer bonding for comparison. Initial bonding results with a-Si indicated partial bonding, cracking, low bonding repeatability, low shear strength and spill out for eutectic bonding. A range of bonding parameters were tried and the results were verified. Although the wafers were HF cleaned prior to bonding, contamination was observed in the bonded areas.

Due to large amount of cracking observed within the a-Si layer deposited by PECVD ,as a result of the high residual stresses induced by PECVD, the deposition method was changed to LPCVD to reduce the residual stresses in a-Si. Layers deposited by both methods were compared in terms of surface roughness using AFM, which showed a smother surface in the case of LPCVD. The residual stresses for LPCVD vs. PECVD deposited a-Si were also estimated by Raman spectroscopy, which confirmed the higher stress levels in PECVD a-Si.

The wafer bonder is typically designed for full wafer bonding, not small samples. As such, pressure uniformity was difficult to achieve for small samples. Different configurations and numbers of samples placed on the bonding chuck led to different bond coverage for the small samples. Using a 5 sample configuration yielded the best bond coverage among the options tried and this configuration was applied for the rest of the bonding experiments.

In order to understand the difference between the bright areas (assumed to be unbounded) vs. dark areas (assumed to be bonded) in the SAM images, cross section samples were prepared from the two regions and imaged using SEM. The images taken from the bright areas indicated the presence of coarser microstructures which provide more interfaces for sound wave reflections. However, the dark areas represented a finer microstructure, which let the sound waves pass through without detection by the transducer. In terms of mechanical properties, a finer microstructure is preferred and was a goal of this work. As suggested by industry, graphite sheets were implemented inside the bonder beneath the chuck to help obtain pressure uniformity. Better bond

uniformity was observed after implementation for bonding of small samples; however, spill out could not be avoided. To solve this problem, solid state bonding was performed at 350°C. Bonding results indicated more uniform bonding with few observable bright areas (coarse microstructure) in SAM images. Cross sections samples were made from both eutectic and solid state bonded a-Si samples and analyzed by SEM and TEM. The observations were similar to the diffusion couple results. Crystallization of a-Si occurred within Au layer. This mechanism is known as layer exchange and is well understood for the Al/a-Si (Al induced crystallization) system; however, it had not been explained for Au/a-Si system. A model was proposed in this work for Au/a-Si layer exchange mechanism. Due to the lower bonding temperature and duration, layer exchange partially happens during solid state bonding.

Bonding of c-Si samples were also performed using eutectic and solid state methods. In both cases, the formation of craters was observed; however the average size of the craters formed in eutectic bonding were about 2-3 times larger than the craters formed during solid state bonding.

Shear testing was performed on eutectic and solid state a-Si and c-Si bonded samples and the results were compared. For a-Si samples, shear strengths of 13.2 MPa and 15.2 MPa were obtained for eutectic and solid state bonding, respectively. None of the c-Si samples detached even at the maximum load. From the results, it seems that solid state bonding is a better option for bonding both a-Si and c-Si samples. Advantages include lower bonding temperature, less spill out and higher mechanical strength.

The parameters optimized for small sample wafer bonding were applied to full wafer bonding. Eutectic and solid state bonding of a-Si and c-Si full wafers were performed. Solid state and eutectic bonding of a-Si samples resulted in uniform bonding all over the wafer. Some spill out was observed in the eutectic bonded wafers. In solid state bonded pairs, due to the lack of liquid formation to fill the roughness gap between two wafers, small voids were present at the interface of the two wafers. Eutectic bonding of c-Si samples resulted in a uniform bond across the wafer; however, voiding in the

centre area of the wafers could not be avoided in solid state bonding. Increasing the bonding pressure did not help to reduce this voiding. After bonding, wafers were diced into smaller samples and shear tests were conducted on them. The shear test strengths for a-Si samples bonded using both eutectic and solid state methods were similar; however, solid state bonding of c-Si yielded higher shear strengths compared with the eutectic method (26.6 MPa vs 13.5 MPa). Similar to small sample results, solid state bonding is preferred.

In-situ TEM analysis was performed on Au/a-Si/c-Si samples at 250°C and 300°C to understand the layer exchange mechanism in Au-Si system. From the as-deposited images there was an intermixed layer at the Au/a-Si interface. Part of this intermixed layer formed during Au sputtering onto the a-Si layer, which can also result in formation of metastable phases. Samples sitting at room temperature for a week before start of in-situ experiment resulted in increase of this intermix layer thickness. The metastable phases led to the formation of the first nuclei inside intermixed layer. It was observed that for both annealing temperatures the nuclei tended to form within the Au layer. One possible reason is the strain induced by the formation of c-Si grains (due to the difference in a-Si and c-Si densities), which is more easily accommodated in the Au layer which is a more ductile phase than a-Si layer. When the Au concentration in the a-Si layer reached a specific level, Si crystallization started in the a-Si layer as well. The rate of nucleation at 300°C was higher compared to 250°C. Continued annealing led to diffusion of Au into Si substrate.

8.2. Recommendations for future work

Recommendations for future work include optimization and improving bonding process and detailed quantitative diffusion analysis using in-situ TEM to determine the diffusion coefficient and activation energy for Au diffusion in a-Si and Si diffusion in Au. The formation of metastable phases needs to be confirmed and more detailed analysis on the layer exchange mechanism should be performed as well

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