High-κ Complex Oxides for Advanced Gate Dielectric Applications Grown by Atomic Layer Deposition

by

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Abstract

As conventional SiO_2 gate dielectric thickness shrank to a few atomic layers, gate dielectric tunneling increased dramatically. The primary way to reduce tunneling is to increase film thickness, which decreases capacitance. High-dielectric-constant (high-κ) oxides were introduced to maintain capacitance density while film thickness was increased. A reliable interface between the high-κ oxide and semiconductor is crucial for good transistor performance. High-κ oxides suffer from lower carrier mobility, degraded reliability and threshold voltage instability compared to silicon dioxide. High-κ binary oxides (HfO_2, ZrO_2 and Al_2O_3) have been have been studied extensively for high-κ gate dielectric applications. Complex oxides offer a higher degree of flexibility to tackle the major shortcoming of high-κ oxides. In this work, hafnium zirconate, hafnium aluminate and zirconium aluminate thin films were grown on silicon, gallium nitride and indium phosphide for advanced gate dielectric applications using plasma enhanced atomic layer deposition. Metal-oxide-semiconductor capacitor devices were fabricated to study dielectric properties, device performance and semiconductor-gate dielectric interfacial quality. All the devices revealed very low density of interfacial traps and small capacitance-voltage hysteresis. Hafnium zirconate had the best performance with ultra-low D_{it} of 2.61×10^{10} cm^{-2} eV^{-1} on silicon and 8.62×10^{11} cm^{-2} eV^{-1} on indium phosphide mainly due to the combination of low growth substrate temperature (100°C) and high post-fabrication heat treatment temperature (510°C).

Furthermore, very low density of interfacial traps proved that there was a reliable interface between the high-κ complex oxide and the semiconductor. The hafnium zirconate dielectric also had the highest capacitance density and lowest leakage current. The leakage current was dominated by direct tunneling in hafnium zirconate. The conduction and valence band offsets of the hafnium zirconate gate dielectrics on InP were measured and compared to pure zirconia using an x-ray photoelectron spectroscopy method. Hafnium zirconate structures showed wider band gap and larger conduction band offset but smaller valence band offset compared to pure zirconia. This was attributed to the increase in valence band width with hafnia addition, which in turn reduced the hafnium zirconate gate dielectric's valence band offset. The band structure line-up is type I with band offsets of 3.53 eV for electrons and 1.03 eV for holes in $Hf_{0.25}Zr_{0.75}O_2$/InP heterojunctions.

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TABLE OF CONTENTS

TABLE OF FIGURES

List of Abbreviations:

ALD: Atomic Layer Deposition

CBO: Conduction Band Offset

CL: Cody-Lorentz

CMOS: Complementary Metal–Oxide–Semiconductor

CV: Capacitance-Voltage

CVD: Chemical Vapor Deposition

DT: Direct Tunneling

EOT: Equivalent Oxide Thickness

FET: Field-Effect Transistor

HAO: Hafnium Aluminate

HZO: Hafnium Zirconate

IV: Current-Voltage

MOSCAP: Metal-Oxide-Semiconductor capacitor

MOSFETs: Metal-Oxide-Semiconductor Field-Effect-Transistors

MSE: Mean Square Error

PEALD: Plasma-Enhanced Atomic Layer Deposition

STO: $SrTiO_3$

SE: Spectroscopy Ellipsometry

SEM: Scanning Electron Microscopy

TALD: Thermal Atomic Layer Deposition

TDMAHf: tetrakis(dimethylamido)hafnium

TDMAZr: tetrakis(dimethylamido)zirconium

TEM: Transmission Electron Microscopy

TMA: trimethyl aluminum

TL: Tauc-Lorentz

TAT: Trap Assisted Tunneling

VBO: Valence Band Offset

XPS: X-ray Photoelectron Spectroscopy

ZAO: Zirconium Aluminate

1 INTRODUCTION

1.1 BACKGROUND

The capability of **s**emiconductor industry to continue scaling electronic devices is limited the presence of quantum mechanical tunneling effects [1]. As conventional SiO_2 (grown by the thermal oxidation of silicon) gate dielectric thickness decreased to a few atomic layers thickness, gate dielectric tunneling leakage increased significantly. Increasing the gate dielectric thickness, in order to suppress the tunneling leakage, causes the capacitance to drop. To compensate for the increasing dielectric thickness and to maintain the same capacitance density of ultra-thin silicon dioxide high-dielectric-constant (high-κ) binary oxides were introduced [2]. Fig. 1-1 illustrates the scaling down of MOS transistors from 1972 to 2004.

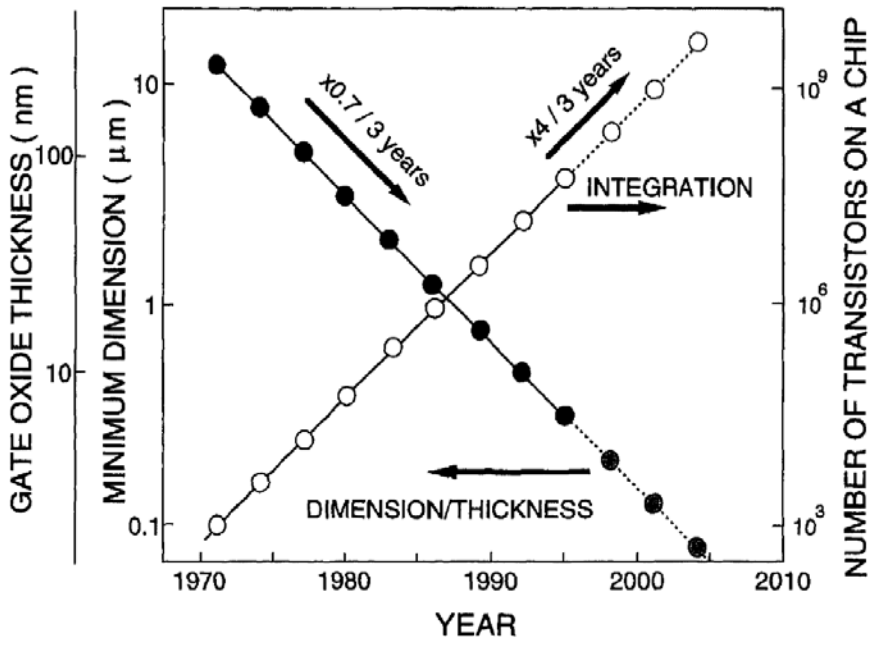


Figure 1-1 MOS transistor scaling from 1972 to 2004 [3].

High κ dielectrics have to be deposited (unlike SiO_2). The technology developed to accomplish this has also impacted III-V compound semiconductor device fabrication since these semiconductors do not grow a robust native oxide like silicon. In general, the discussion on these high κ oxides applies to both Si and III-V devices except where specified.

HfO_2, ZrO_2 and Al_2O_3 high-κ dielectrics have been studied extensively as a replacement for conventional SiO_2 gate dielectric. These

oxides have high dielectric constant, large conduction band offset, and very good kinetic and thermodynamic stability [4]. However, all the aforementioned high-κ binary oxides suffer from poor dielectric-semiconductor interfacial quality, threshold voltage instability, degraded reliability and low carrier mobility compared to SiO_2 [1,2]. Complex oxides have been studied extensively for electronic applications such as memory, spintronic, resistive switching, tunnel junction and thermoelectric devices [5–7]. Moreover, complex oxides offer a higher degree of flexibility and tuning [5]. High-κ complex oxides offer advantages over binary high-κ oxides for gate dielectric applications, while providing a degree of freedom to overcome the shortcomings.

1.2 LITERATURE REVIEW

1.2.1 High-κ Gate Dielectrics: History, Requirements and Shortcomings

Complementary metal oxide semiconductor (CMOS) field effect transistors (FET) are the most important solid state electronic devices due to continued performance improvement according to Moore's observation[1]. Gordon Moore noticed that number of transistors on the integrated circuits doubles every two year. As a result, feature size decreases exponentially with time [8]. Moore's observation still holds but

[1] Commonly known as Moore's law

is facing many challenges. The major problem with the gate dielectrics arose in 2004 when the SiO_2 gate dielectrics were only 1.4 nm thick [9] and the gate leakage current exceeded 1A/cm^2. Fig. 1-2 illustrates the dramatic gate dielectric leakage current increase with shrinking gate oxide thickness. Most devices in this era suffered from large power dissipation. Furthermore, such ultra-thin gate dielectrics suffered from lower reliability, reproducibility and break down time. These factors lead to the replacement of the gate dielectric [4].

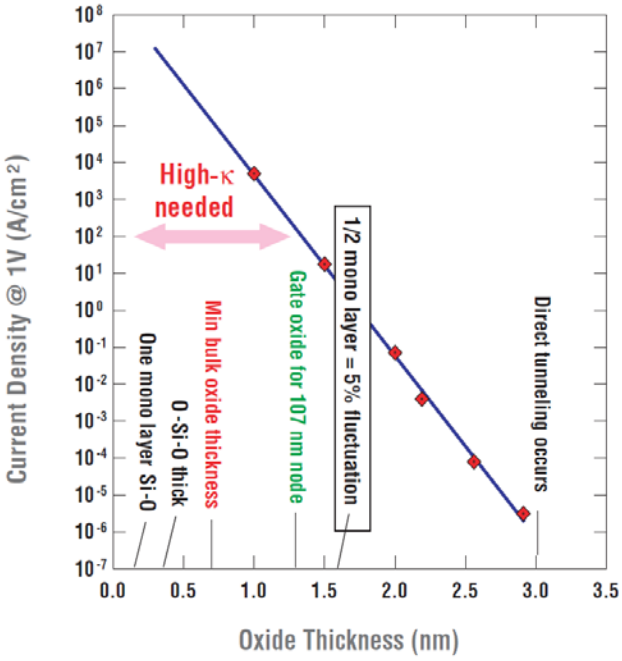


Figure 1-2 Gate dielectric leakage current increases exponentially with gate oxide thickness shrinkage [10].

Leakage current decreases exponentially with increasing gate dielectric thickness. Increasing the gate dielectric thickness addresses the leakage issue but the capacitance decreases (according to equation 1-1) and the performance of field effect transistors is strongly dependent on the gate dielectric capacitance.

$$C = \frac{\kappa \varepsilon_0 A}{t} \qquad (1\text{-}1)$$

Here ε_0 is free space permittivity, κ is relative permittivity, t is the gate dielectric thickness and A is dielectric area. High-κ dielectrics were introduced to compensate for the increase in gate dielectric thickness. Figure 1.3 compares SiO_2 and high-κ gate dielectrics schematically in which electrons from gate tunnel through the gate oxide into the conduction band (CB) of silicon channel. Evidently, high-κ dielectrics can be deposited thicker compared to silicon dioxide and having the same capacitance density due to higher relative dielectric constant (according to equation 1-1).

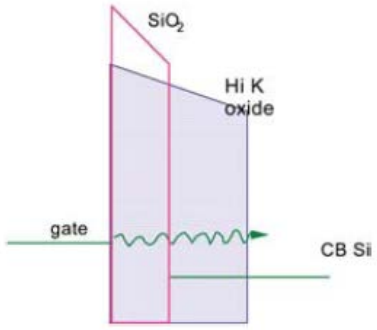


Figure 1-3 Schematic comparison between in SiO_2 gate dielectrics and high-κ gate dielectrics [4].

1.2.1.1 Main requirements high-κ gate dielectrics

1.2.1.1.1 High-κ:

Dielectric constant is a material property and is highly dependent on crystal structure. The main issue with high-κ oxides is that they tend to have lower band gap (than SiO_2) and narrow band gap materials cannot possibly provide enough band offset to suppress gate dielectric leakage. The 2001 edition of International Technology Roadmap for Semiconductors (ITRS) mentioned a band offset >1eV is needed to suppress the gate dielectric leakage current [11]. Furthermore, high-κ dielectrics are susceptible to a higher concentration of electrically active defects compared to SiO_2. The flat band voltage is commonly obtained from the following equation,

$$V_{fb} = \Phi_{ms} + \frac{Qt}{\kappa\varepsilon_0} \qquad (1\text{-}2)$$

Where Φ_{ms} is the work function difference between the gate metal and channel, Q is trapped charge or interfacial fixed charge, ε_0 is free space permittivity, and κ and t are relative permittivity and gate oxide thickness, respectively. Evidently, κ and V_{FB} are inversely related and as a result higher dielectric constant lowers the flat band voltage. Figure 1.4 depicts the common trend of energy gap with dielectric constant. Interestingly, wide band gap dielectrics tend to have lower dielectric constant.

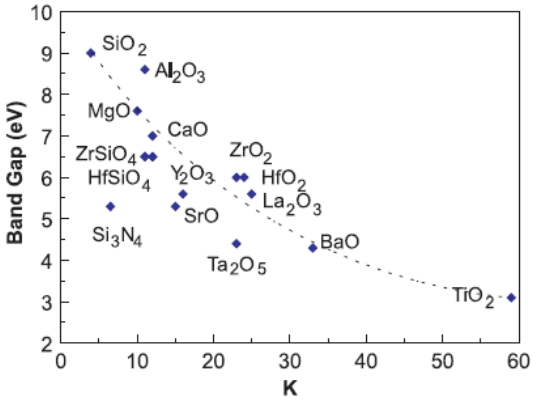


Figure 1-4 Schematic comparison between in SiO_2 gate dielectrics and high-κ gate dielectrics [2].

1.2.1.1.2 Band offset:

High-κ gate dielectrics should have band offsets >1eV over the semiconductor channel to suppress the tunneling leakage current [11]. Figure 1.5 depicts the band offset of well-known dielectrics on GaAs. This highlights the importance of materials selection for high-κ gate dielectrics, since dielectric constant is not the only important factor. Some of the other important materials selection criteria are discussed in the following sections.

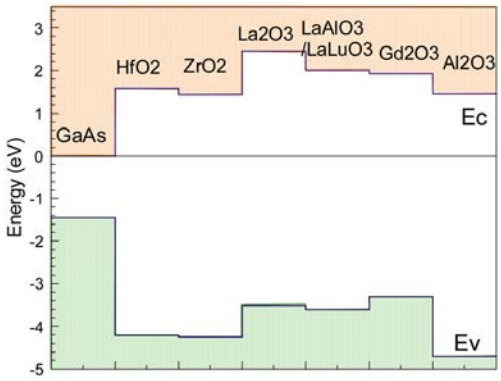


Figure 1-5 Band offsets of gate dielectric candidates over GaAs [12].

1.2.1.1.3 Thermodynamic stability:

Thermodynamic stability means that the gate dielectric should not react with the semiconductor. ZrO_2 has a higher dielectric constant than HfO_2 but forms the low-κ $ZrSi_2$ compound during post fabrication heat

treatment [13]. Additionally, the gate oxide should not react with the working atmosphere. La_2O_3 has a high dielectric constant and relatively wide band gap but forms hydrates readily with water vapor in the atmosphere [14].

1.2.1.1.4 Kinetic stability:

Kinetic stability means that the desired structure should not be susceptible to any transformation during fabrication and operation. Atomic layer deposited high-κ gate oxides are commonly amorphous and amorphous structure has superior electrical characteristics compared to polycrystalline structures. Therefore, the gate dielectric should remain amorphous during fabrication and operation to prevent crystallization.

1.2.1.1.5 Interfaces quality:

Interfacial defects form mid-band gap trap states and remove free carriers. $SrTiO_3$ (STO) and Si have negligible lattice mismatch and as a result STO grows heteroepitaxially on Si. The trap density of $SrTiO_3$/Si is $6.4x10^{10}$ $cm^{-2}.eV^{-1}$ [15]. However, STO does not provide the required band offset on silicon. Accordingly, STO enabled FET devices suffer from high gate dielectric leakage current [12].

Gate dielectric-semiconductor interfacial quality dominates device performance [16]. Interfacial defects acting as trap states destabilize the threshold voltage. Figure 1.6 depicts schematically the interfacial defect

(dislocation) formed due to lattice mismatch and the related trap states in the band diagram.

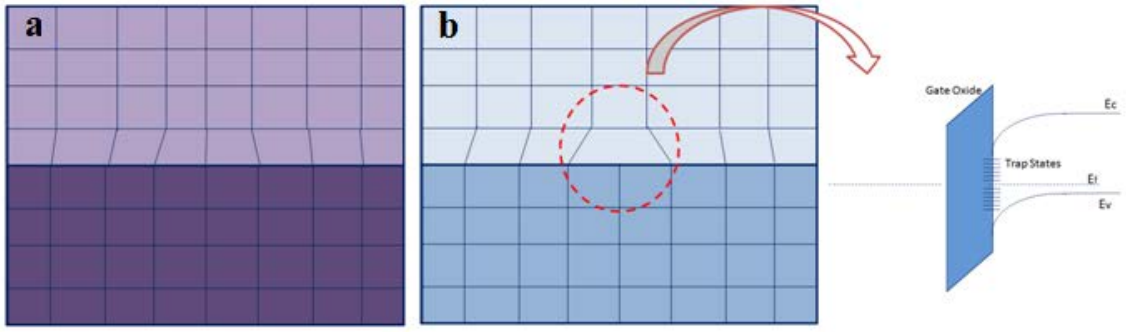


Figure 1-6 (a) Schematic view of heteroepitaxial growth and (b) the higher degree of mismatch relaxed through formation of interfacial faults.

1.2.1.1.6 Bulk defects:

Bulk defects also from copious trap states and deteriorate electrical characteristics of the gate dielectric. Trapped charges shift the FET threshold voltage. Also, their concentration varies in time which leads to an unstable threshold voltage. Furthermore, trapped charges may act as a source of scattering for channel carriers and diminish the mobility of carriers in the channel. Bulk defects also may provide current leakage paths

and increase gate dielectric leakage accordingly. Lastly, bulk defects are not desirable and reduce the break down voltage and the time to break down.

1.2.1.2 Major shortcomings of high-κ gate dielectrics

1.2.1.2.1 Threshold voltage instability:

The flat band voltage is generally obtained from capacitance-gate voltage plot according to equation 1-2. Flat band voltage is directly related to the threshold voltage according to following equation (for P-type body),

$$V_t = V_{fb} + 2\phi_B + \frac{\sqrt{4qN_a\varepsilon_s\phi_B}}{C_{ox}} \qquad (1\text{-}3)$$

Where V_t is the threshold voltage, Φ_B is difference between bulk intrinsic and doped channel Fermi levels, q is elementary charge, N_a is dopant concentration in semiconductor, ε_s is semiconductor dielectric constant, and C_{ox} is gate dielectric capacitance. Evidently, V_t and V_{fb} are directly related and as a result, any instability in flat band voltage causes threshold voltage instability.

1.2.1.2.2 Degraded carrier mobility:

Carriers in FET channels act similar to a 2D electron gas. Channel carrier mobility is dominated by columbic interactions at low electric fields, by phonon scattering at moderate electric fields and surface roughness at

high electric fields. According to Mathieson's rule the total mobility of channel carriers can be expressed according to equation 1-4.

$$1/\mu=1/\mu_C+1/\mu_{PH}+1/\mu_{SR} \qquad (1\text{-}4)$$

Here μ, μ_C, μ_{PH}, and μ_{SR} stand for total carrier mobility, columbic, phonon, and surface roughness components of the carrier mobility, respectively. Figure 1-7 illustrates the carrier mobility with respect to electric field and reveals various carrier mobility regimes in low, middle, and high electric fields.

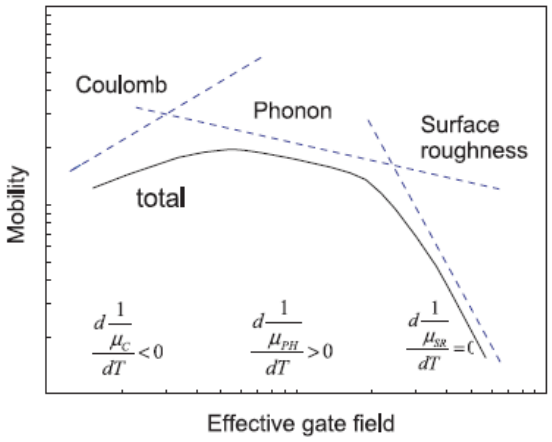


Figure 1-7 Carrier mobility with respect to effective gate field [4].

1.2.1.2.3 Large charge trapping:

The nature of the charge trapping defects varies depending on the gate dielectric material. Typically, oxygen vacancies and oxygen interstitials (oxygen related defects) are dominant charge trapping defects in high-κ oxides. Post-heat treatment can reduce the density of trapped charges. Using density functional theory (DFT), Li and Robertson showed that post-fabrication heat treatment in fluorine and nitrogen atmospheres passivate oxygen related defects in $LaAlO_3$ [17]. Addition of glass former oxides might also help suppressing the oxygen related defects and increase the crystallization temperature. Such additives are commonly low-κ materials and accordingly degrade the dielectric properties of gate oxide. Moreover, introducing new additives causes formation of new interfaces and increases bulk defect concentration accordingly.

1.2.2 ALD of Oxides

Oxide thin films can be deposited by variety of physical vapor and chemical vapor deposition techniques [18–20]. The 2007 edition of International Technology Roadmap for Semiconductors (ITRS) named the atomic layer deposition (ALD) technique as a method for growing high-κ gate dielectric oxides [21]. The ALD technique utilizes organometallic precursors as the source for the cation and divides the deposition of one

layer into two self-terminating reactions [22]. Each cycle includes the organometallic precursor pulsed in and purged out followed by the oxidant specie pulsed in and purged out (See Figure 1.8) [22,23]. Water vapor, plasma oxygen and ozone have been used as oxidant specie in atomic layer deposition [24]. Plasma enhanced ALD (PEALD) uses plasma oxygen as the oxidizing agent while water vapor is the main oxidant specie in thermal ALD (TALD). ALD is a self-limiting thin film growth technique with sub nanometer thickness control and very high degree of conformality [22,24,25].

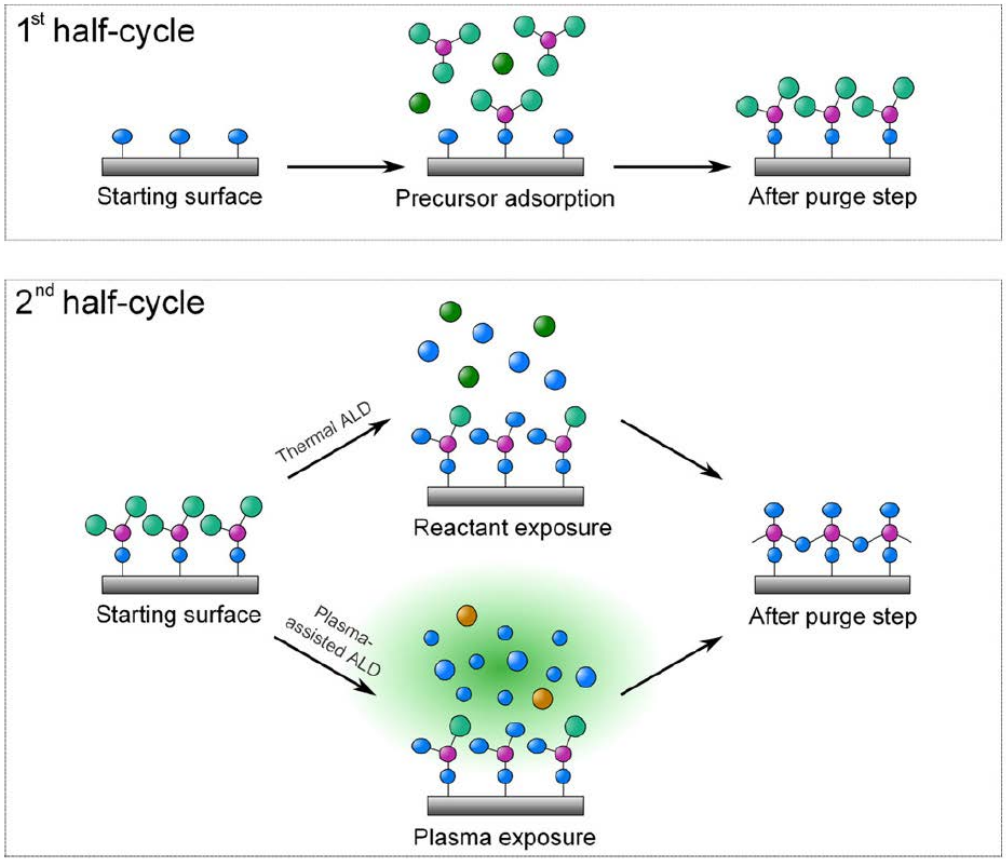


Figure 1-8 Schematic representation of one atomic layer deposition cycle [26].

ALD is well-known for its very good thickness and composition precision and reliability [27]. Good control over thickness and composition is crucial for deposition of high-κ gate oxides. ALD is uniquely capable of low-temperature deposition which relieves the interfacial stress mainly due

to thermal expansion coefficient mismatch between channel and gate oxide [27].

The ALD processing temperature range is commonly known as the ALD window. The reactants either condensate or cannot overcome the surface reaction energy barrier at lower temperatures [28]. On the other hand, the reactants might decompose or desorb at higher temperatures [28]. A schematic of the ALD window is illustrated in Figure 1.9.

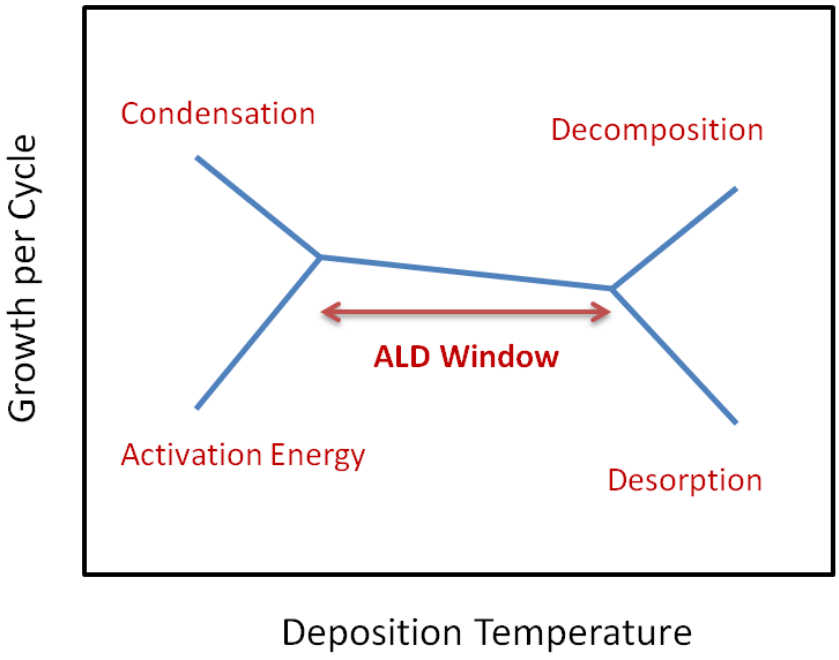


Figure 1-9 Schematic of ALD window with possible growth per cycle behavior [29].

Ideally, after each complete cycle one single layer forms on the substrate. This helps with precise control over the film thickness and deposition rate. This is more intricate for ternary oxides as there are at least two cations. Accordingly, the ALD cycle of a ternary oxide includes two organometallic precursors and one oxidant specie. Furthermore, initiating or terminating with A or B cation affects the electronic properties of the films.

The semiconductor-gate dielectric interface is, arguably, the most important region in the FET devices. This region effectively determines the carrier mobility and band bending efficiency. The Si/SiO_2 interface has a very low density of interfacial defects (D_{it} ~ 10^{10} cm^{-2} eV^{-1}). However, the ultra-low density of interfacial traps at the Si/SiO_2 interface could not be duplicated for high-κ/Si interfaces mainly due to the vast differences in crystal symmetry and coordination of silicon and high-κ oxides [16,30]. High-κ dielectrics are also of great interest for Ge and III-V based devices as these materials do not grow a robust and pin-hole free native oxide like silicon.

Plasma enhanced atomic layer deposition (PEALD) has been used commercially for the growth of high-κ gate oxides [31,32]. Furthermore, the semiconductor surface is not completely covered during the first cycles of the dielectric deposition and consequently the plasma could damage and/or

oxidize the semiconductor surface. As a result, the equivalent oxide thickness (EOT) and D_{it} rises. On other hand, in thermal ALD steam is being used as oxidant specie and water vapor does not react directly with substrate during high-κ oxide growth. However, thermal ALD (TALD) grown gate oxides show inferior electrical characteristics mainly due to a higher concentration of bulk defects [31]. Residual oxidants are readily detected in the TALD grown oxides mainly because of water surplus during growth [33,34]. Residual oxidant species cause abundant oxygen related defects during post-fabrication heat treatment [33]. Films grown using other oxidant species such as ozone and plasma oxygen did not have such bulk defects (e.g. oxygen interstitials) [35].

1.2.2.1 Al_2O_3

Aluminum oxide (alumina) is the most studied ALD grown material among all the oxides mainly due to its technological importance. Alumina has high permittivity, very good electrical insulation and relatively strong adhesion to different substrates. Furthermore, the alumina ALD mechanism is considered as representative of other ALD reactions [28,36]. Alumina has a wide bandgap (~8.7 eV), high band offset (>1eV) on silicon and relatively high dielectric constant (~9) [23]. It also has very high thermodynamic, chemical and thermal stability which makes it attractive for many

applications including microelectronic devices [37], solar energy devices [38], magnetic recording heads [39], and wear-resistance coatings [40]. Since alumina is thermodynamically and kinetically stable on silicon and many III-V semiconductors, it has been studied as a gate oxide in Metal-Oxide-Semiconductor (MOS) transistors [41]. Alumina has also been used extensively in non-volatile random access memories [42,43] due to its superb dielectric properties. The ALD growth of alumina has been studied extensively. Although, many precursors have been employed for the ALD growth of alumina, trimethyl aluminum (TMA) is the most cited precursor [44,45]. ALD deposition of alumina using TMA precursor and water as the oxidant is described by the following half-reactions:

$$Al\text{-}OH^{*} + Al(CH_3)_3 \rightarrow Al\text{-}O\text{-}Al\text{-}\ (CH_3)_2{}^{*} + CH_4 \qquad (1\text{-}5)$$

$$Al\text{-}CH_3{}^{*} + H_2O \rightarrow Al\text{-}OH^{*} + CH_4 \qquad (1\text{-}6)$$

1.2.2.2 HfO_2

Hafnium oxide (hafnia) has been grown by ALD for commercial high-κ dielectric applications. Hafnia has a high dielectric constant (20), high band gap (5.8eV), high band offset (>1eV) and very good thermal and kinetic stability on silicon. Hafnia has a monoclinic crystal structure at room temperature and atmospheric pressure but transforms to tetragonal at elevated temperatures. Interestingly, the tetragonal phase has a much higher

dielectric constant than the monoclinic phase. Eventually, ALD deposited hafnia was employed in the 45-nm node in 2007 by Intel Corp. [46]. ALD grown high-κ dielectric oxides was also used in the 32-nm and 22-nm nodes [47,48]. Choi *et al*. did a comprehensive review of the development of high-κ gate dielectric hafnia [49]. A variety of metalorganic precursors have been utilized for ALD growth of hafnia including tetrakis(diethylamino)hafnium [50], $HfCl_4$ [51], tetrakis(ethylmethylamide) hafnium [52], and tetrakis(dimethylamide) hafnium [53].

1.2.2.3 ZrO_2

Zirconium and hafnium both belong to the column IV in the periodic table and display very similar physical and chemical properties. Furthermore, zirconia and hafnia also have very similar properties and crystal structure [2,4,13,54]. Zirconia has a monoclinic crystal structure at room temperature and transforms into tetragonal at elevated temperature. On the other hand, zirconia has a slightly lower band gap (5.8 eV) but higher dielectric constant (25-30). Zirconia is not as stable as hafnia on silicon and forms low-κ $ZrSi_2$ during post fabrication heat treatment [55]. A variety of zirconium precursors have been developed for ALD of ZrO_2, such as tetrakis(ethylmethylamino) zirconium [56] and $ZrCl_4$ [57].

1.2.3 Complex Oxides

According to the 2008 International Technology Roadmap for Semiconductors (ITRS) complex oxides include "transition metal oxides alone or in combination with group II or lanthanides" [21]. This is in contrast with classic text book definitions of complex oxides which defines complex oxides as at least ternary in nature and distinctively distinguished from binary oxides [58,59].

The dielectric constant of HfO_2 and ZrO_2 depend on their crystal symmetry [13,60]. First-principles density functional theory calculations predicts a very high dielectric constant for the tetragonal phase, while a moderate dielectric constant for the monoclinic phase [13]. The tetragonal phase is only thermodynamically stable at elevated temperatures and atmospheric pressure. Hafnium zirconate has a highly stabilized tetragonal phase and a higher dielectric constant compared to end phase [13,54]. Furthermore, adding alumina helps to increase the band gap, and consequently might help to reduce the gate dielectric leakage current which is important for wide band gap semiconductors used for power applications. In conclusion, complex oxides provide the rare opportunity and degree of freedom to tailor a high-κ gate oxide for each individual semiconductor.

1.3 OBJECTIVES OF THIS WORK

Atomic layer deposition has been widely recognized as the ideal technique for growing high-κ gate dielectrics. The technique is now being commercially used for the deposition of high-κ gate dielectrics. The first layers of the film formation is critical for film properties. A fundamental understanding of nucleation and growth mechanisms helps with controlling the film properties and modifying them for desired applications. Furthermore, the semiconductor-gate dielectric interface is arguably the most important region of the FET device. This region controls carrier mobility and eventually device performance. Understanding the interaction of the organometallic precursor and oxidant specie with the semiconductor during the initial cycles helps with understanding and modifying this region. The oxidant specie plays an important role in both bulk and interface quality of the ALD grown gate oxide.

While there are many investigations comparing thermal and plasma enhanced ALD grown high-κ gate dielectrics, there is no systematic study of mixing the two techniques for optimum electrical characteristics. In this report an in-depth electrical characterization and comparison of high-κ dielectrics (HfO_2 and ZrO_2) grown by PEALD, TALD and mixed structures is presented. Furthermore, there are many investigations comparing PEALD grown binary

high-κ oxides, but there is no systematic study of high-κ ternary oxides for advanced gate dielectric applications. In this report an in-depth electrical characterization and comparison of high-κ ternary oxides ($HfZrO_x$, $ZrAlO_x$, and $HfAlO_x$) grown by low temperature PEALD for advanced gate dielectric applications is presented. These complex oxides are fabricated into metal-oxide-semiconductor capacitors and electrically characterized to determine the dielectric properties, leakage current and interface quality of the semiconductor-gate oxide

1.4 OUTLINE OF THESIS

In this chapter a brief introduction on history, requirements and shortcomings of high-κ dielectrics is presented. Moreover, ALD deposition of oxides including alumina, hafnia, zirconia and complex oxides is introduced. Chapter two outlines the experimental procedure used for deposition and characterization of high-κ gate dielectrics. In chapter three the effect of oxidant specie is presented. In this chapter, thermal and plasma enhanced ALD techniques are being compared. The mixture of the two techniques is studied for optimum electrical properties. Chapter four is on the deposition and characterization of high-κ ternary oxides ($HfZrO_x$, $ZrAlO_x$, and $HfAlO_x$). Optical and electrical properties of these oxides on various semiconductors is studied and presented in this chapter. The overall conclusion of this report is in chapter five.

2 EXPERIMENTAL PROCEDURES

This Chapter covers the materials and methods utilized to deposit and characterize high-κ gate dielectrics, as well as, the fabrication procedure and electrical characterization details of metal-oxide-semiconductor capacitor (MOSCAP) devices.

2.1 ALD CHAMBER

High-κ oxide deposition was carried out in an ALD-150L (Kurt J. Lesker). The ALD-150L has dual steam and remote plasma capabilities, well suited for both thermal and plasma enhanced ALD. Figure 2-1 shows a picture of the ALD system. The sample is first loaded into the load-lock to avoid ALD reactor contamination. The load-lock is pumped down to 10^{-7} Torr before transferring the sample inside the ALD reactor.

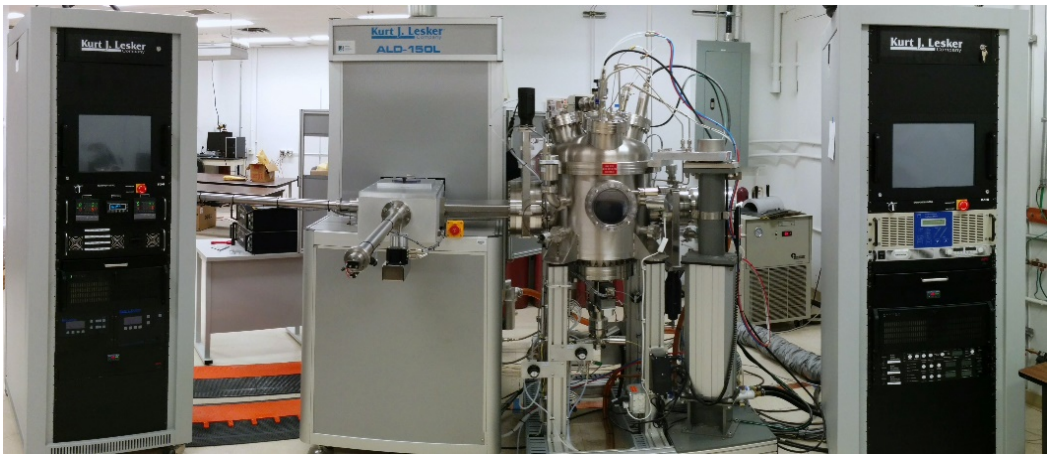


Figure 2-1 The view of the ALD system in our lab.

A schematic view of the ALD system is illustrated in Figure 2-2. The ALD-150L reactor has high-speed valves which facilitate dose times as low as 0.02 s and has very efficient precursor usage. Moreover, Ar or N_2 inert gasses are constantly streamed in the reaction lines to avoid any backflow of the byproducts or contamination of the system. To achieve sufficient precursor vapor pressure the precursor ampoules are heated. It is noteworthy to mention that vapor pressure is exponentially related to temperature according to Clausius-Clapeyron equation, thus the ALD procedure is very sensitive to precursor temperature. The mass flow control (MFC) valves open up during precursor dose time for the assigned time and the Ar gas carries and delivers the precursor vapor to the reactor.

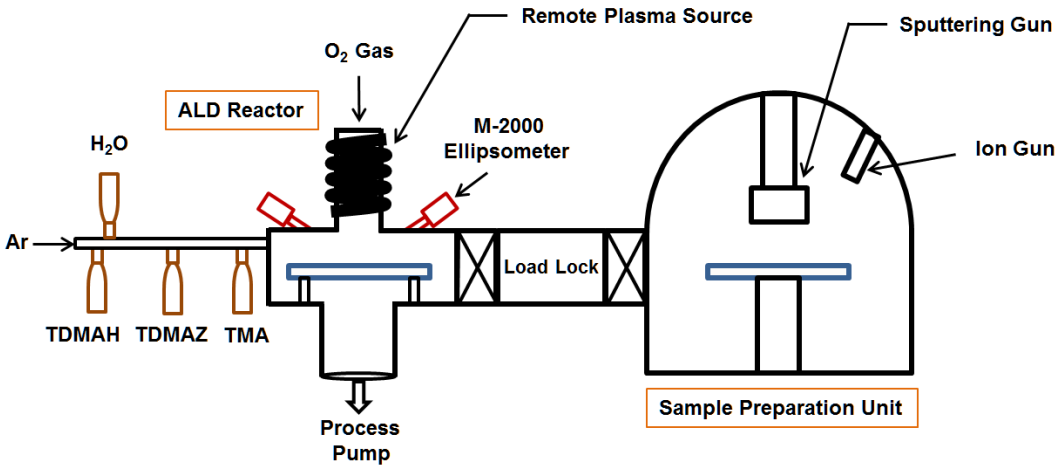


Figure 2-2 The schematic view of the ALD system in our lab [29].

The flow of inert (Ar) gas at 500-600 sccm protects the *in-situ* spectroscopic ellipsometry windows and ALD reactor walls from any deposition. Also, a 10 sccm flow of argon prevents any back streaming of the byproducts into the reaction lines which are not in use. A 250 sccm flow of argon through the plasma source protects the plasma source from back flow during the thermal ALD procedure. The remote oxygen plasma is created by an inductively coupled plasma source with 600 W power. The plasma enhanced ALD is carried out at a vacuum of 1.1 Torr. The combination of the aforementioned pressure and plasma power ensures the successful formation of remote oxygen plasma [61].

2.2 *IN-SITU* SPECTROSCOPIC ELLIPSOMETRY

Spectroscopic ellipsometry determines the thickness and the optical properties (n and k) of the thin films with precision down to fraction of an Angstrom. In spectroscopic ellipsometry the reflected wave's phase and amplitude is measured and compared with the incident wave. Using the Fresnel equation the raw spectroscopic ellipsometry data is converted into two parameters according to equation 2-1: the phase change, Ψ and the amplitude ratio, Δ.

$$\rho = \frac{r_p}{r_s} = tan\Psi . e^{i\Delta} \qquad 2\text{-}1$$

Here r_s and r_p are perpendicular (s) and parallel (p) components of complex amplitude reflection coefficients of the reflected light [62,63]. Figure 2-3 depicts the schematic view of the light interacting with a medium in ellipsometry.

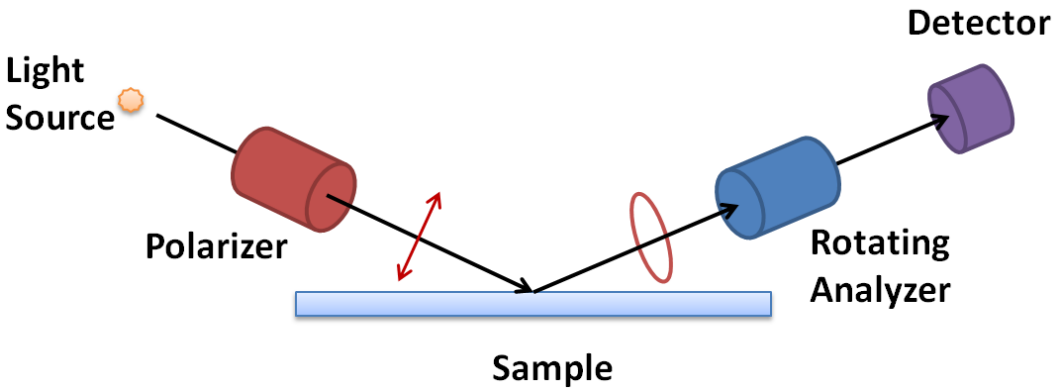


Figure 2-3 A schematic illustration of a typical ellipsometry set up [29].

Finally, the acquired data is compared to a mathematical model. The measured values are used to fit the thickness and optical properties of the optical model iteratively until the lowest mean square error (MSE) is obtained. In the course of this research, a J.A.Woollam M-2000DI spectroscopic ellipsometer (SE) is utilized to monitor the thickness

evolution and optical properties of the growing oxide in real time. Figure 2-4 shows schematically how spectroscopic ellipsometer works. *In-situ* SE (iSE) is a powerful tool for studying the growth of ALD films in real-time [64].

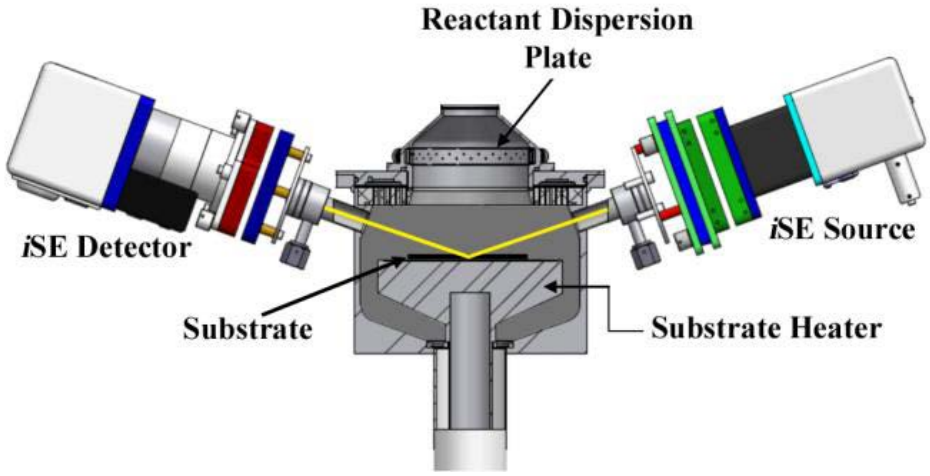


Figure 2-4 Schematic illustration of the in-situ spectroscopic ellipsometry mounted on ALD reactor [65].

The ellipsometry data (ψ and Δ) are acquired over the photon wavelength range of 0.19 – 1.69 μm at a fixed incident photon angle of 70°. Complete EASE v4.50 software (J.A.Woollam Co. Inc.) is used to analyze the ellipsometry data. Both Cody-Lorentz (CL) and Tauc-Lorentz (TL) models have been used extensively for optical modeling of oxides

[66,67]. However, the Tauc-Lorentz model gives lower mean square error (MSE), and consequently was used as optical model for complex oxide thin films in this report.

2.3 X-RAY PHOTOELECTRON SPECTROSCOPY (XPS)

X-ray photoelectron spectroscopy (XPS) is an analytical technique for surface analysis which can resolve the chemical state, elemental composition and electronic state of the elements. XPS measures the kinetic energy and intensity of the emitted photoelectrons to analyze the elemental concentration of the surface layers. Stoichiometry can dramatically affect the electronic properties of the complex oxides. Moreover, oxidation states of A and B cations in complex oxides play an important role in its electronic properties. In addition, XPS might help to identify type, concentration, and chemical state of the residual precursor impurities. Ultimately, XPS can be used to determine the band offset between the gate dielectric and the channel.

XPS shines a monochromatic X-ray beam, typically Al-Kα, on the specimen surface to study the surface properties. The high energy X-ray beam is absorbed by the specimen surface and photoelectrons are generated according to photoelectric effect. The XPS spectrum is

practically the count rate of the detected photoelectrons versus their binding energy ($E_{binding}$) according to Rutherford equation:

$$E_{binding}=E_{photon} - (E_{knietic}+ \varphi) \qquad 2\text{-}2$$

Here $E_{kinetic}$, E_{photon}, and φ are the emitted photoelectrons' kinetic energy, the incident photon energy, and work function of the specimen, respectively. Each element generates a characteristic XPS spectrum. Furthermore, the binding energy could also depend on the oxidation state. One specific element at higher oxidation state can reveal higher binding energy compared to the same element at lower oxidation state, mainly due to the additional columbic attraction between the nuclei and the electrons. The detection limit of XPS is in the range of 0.1-1.0 at. %. In this report, X-ray photoelectron spectroscopy (XPS) measurements were performed at the Alberta Center for Surface Engineering and Science (ACSES) using the ULTRA (Kratos Analytical) AXIS 165 XPS spectrometer. A monochromatic Al-Kα radiation (hν = 1486.6 eV) at 210 W was used as the x-ray source. XPS data was collected from an area of ~300μm×700μm under ultrahigh vacuum (10^{-9} Torr). The step energy of 0.1 eV was applied for high-resolution data collection. The surface charging effects was counterbalanced with using a charge neutralizer. The Casa XPS software was utilized to analyze the XPS data. Finally, using a nonlinear Shirley

background model the background was eliminated. Carbon 1s binding energy (284.8 eV) was used as reference to calibrate the XPS data.

2.4 SCANNING ELECTRON MICROSCOPY

Scanning electron microscopy (SEM) scans a focused beam of electrons at the sample surface to create an image. Interaction of the focused electron beam with the specimen generates multiple signals, including secondary and back scattered electrons, which are utilized to form the image. The lens of the microscope turns the points on the specimen into discs (known as Airy disc) in the image plane. If two discs are closer than a theoretical threshold (theoretical resolution: equation 2-3) they cannot be distinguished as two separate points. Theoretical resolution is directly proportional to the de-Broglie wavelength of the electron beam which is much shorter than optical wavelengths and as a result has much better resolution.

$$r_{theoritical} = \frac{0.61\lambda}{\alpha} \qquad 2\text{-}3$$

Where $r_{theoretical}$, λ and α represent theoretical resolution, wavelength and the collection angle, respectively. In TEM resolution follows the 2-3 relationship. On the other hand, in SEM resolution is limited by electron beam width and interaction volume.

A field emission electron source has a very sharp tip and a very high electric fields is applied to the tip. The gigantic electric field at the tip facilitates tunneling of the electrons. The field emission electron source typically needs very high vacuum and provides higher current density, smaller cross over, higher brightness, lower energy spread and longer life time compared to the conventional thermionic electron sources. The cross section of the MOSCAP devices were investigated using field emission scanning electron microscopy (Zeiss, Sigma FE-SEM).

2.5 SAMPLE PREPARATION AND DEVICE FABRICATION

The MOS capacitors (MOSCAPs) were fabricated on p-type (100) silicon, n+ type gallium nitride (Kyma, Inc.) and n-type (100) indium phosphide (MTI, Inc.). High purity argon (5.0 purity, Praxair) was utilized as carrier gas in the ALD reactor. Tetrakis(dimethylamido)-zirconium (Sigma Aldrich >99.99%), tetrakis(dimethylamido)-hafnium (Sigma Aldrich >99.99%) and trimethyl-aluminum (Sigma Aldrich >99.99%) were utilized as precursors for zirconium, hafnium and aluminum, respectively. Figure 2-6 illustrates the molecular structure of tetrakis(dimethylamide) zirconium (TDMAZ) and tetrakis(dimethylamino) hafnium (TDMAH) used as an ALD source for Zr and Hf, respectively. The alternating precursor pulse width/purge times

were in order: oxygen plasma (2/10 s), water vapor (0.5/10 s), aluminum (0.02/5 s), zirconium (0.04/5 s) and hafnium (0.04/5 s).

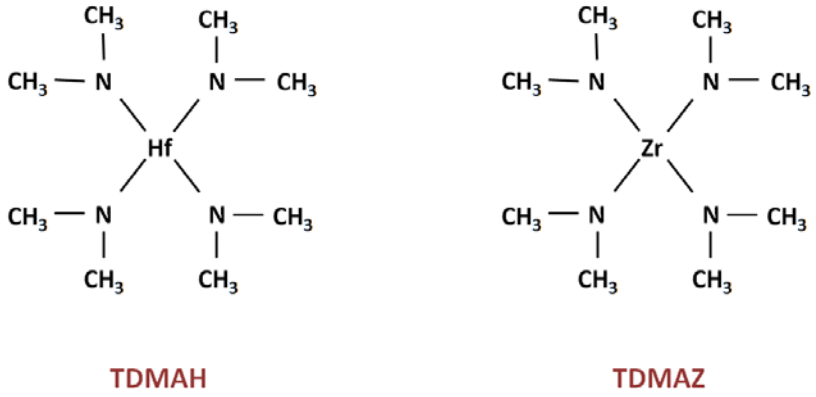


Figure 2-5 Chemical structure of the tetrakis(dimethylamino) hafnium (TDMAH) and tetrakis(dimethylamide) zirconium (TDMAZ), utilized as ALD precursors for Hf and Zr, respectively [29].

Substrate temperature was maintained at 100 °C and chamber pressure was kept at 1.07 Torr during film growth. All remote plasma pulses were done at 600 W and 13.56 MHz. Top contacts (Cr or Ru) were deposited using DC magnetron sputtering and patterned by conventional lithography into planar MOSCAP structures. AZ 5214 positive photoresist was used with MF319 developer for lithography procedure. AZ 5214 was dropped on the specimen surface and then the specimen was spun at 500 rpm for 10 s followed by another spinning at 4000 rpm for 45 s. Then, it was baked for 1 min at 100 °C followed by a 3 s exposure

under 60.7 $mW.cm^{-2}$ illumination. This is followed by a final bake at 115 °C for 40 s and a flood exposure at 60.7 $mW.cm^{-2}$ for 1 min. Finally, the specimen were developed in MF 319 for 25 s. The MOSCAPs were then heat treated at 400 °C (Cr) or 510 °C (Ru), depending on the top contact metal, for 15 min under forming gas (95%N_2+5%H_2) to activate the device and anneal out the defects. Figure 2-6 shows the top view of a planar MOSCAP device.

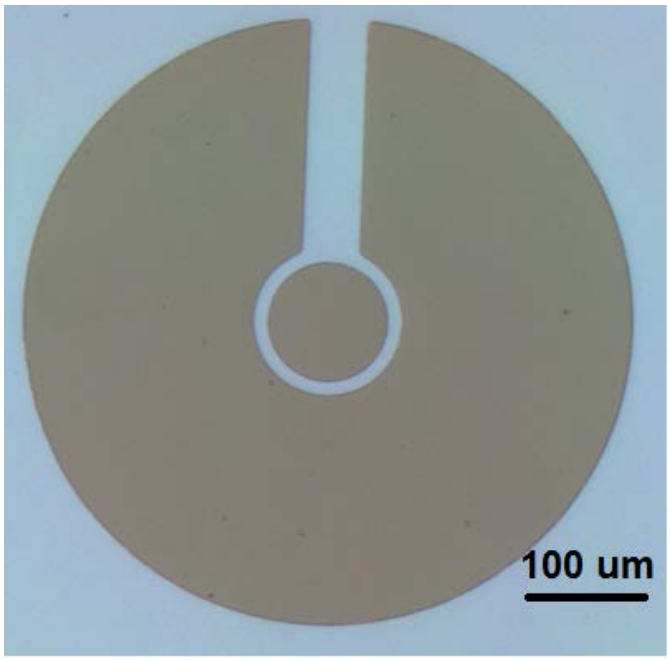


Figure 2-6 The top view of the planar MOSCAP devices.

2.6 ELECTRICAL MEASUREMENTS

A Keithley 4200 SCS analyzer was utilized to carry out the electrical measurements. The capacitance of the MOSCAP devices was measured with sweeping gate voltage at various frequencies. Furthermore, the parallel conductance of the devices was also measured with sweeping gate voltage at various frequencies. Finally, the gate dielectric leakage current was measured with sweeping gate voltage.

3 THERMAL VERSUS PLASMA ENHANCED ALD

This chapter compares electrical characteristics of thermal and plasma enhanced ALD grown high-κ gate dielectrics. Furthermore, a mixture of two techniques is studied for optimum electrical characteristics studying metal-oxide-semiconductor capacitor (MOSCAP) devices.

3.1 INTRODUCTION

A well-defined and atomically abrupt interface with insignificant silicon oxidation is mandatory for optimal performance of metal-high k oxide-semiconductor (MOS) structure [68]. However, the ultra-low density of interfacial traps (D_{it}~ 10^{10} cm^{-2} eV^{-1}) in Si/SiO_2 interface is difficult to reproduce at high-κ/Si interfaces mainly due to large differences in the atomic crystal coordinates of silicon and high-κ oxides [16,30]. Since the gate oxide/semiconductor interface is the most crucial region of a MOS device [16,69] interface quality dictates electrical characteristics of the MOS structure.

Deposited oxide thin films have interesting properties for advanced electronic applications such as optoelectronics, non-volatile memory, tunnel junction, and spintronics [5–7,70]. Oxide thin films have been deposited by variety of physical vapor and chemical vapor deposition techniques [18–20]. The ALD technique utilizes organometallic precursors as the source for

the cation and divides the deposition of one single layer into two self-terminating reactions [22,25]. Each cycle includes the organometallic precursor pulsed in and purged out followed by the oxidant specie pulsed in and purged out. Plasma enhanced ALD uses plasma oxygen as the oxidant agent while water vapor is the main oxidant specie in thermal ALD. Plasma enhanced atomic layer deposition (PEALD) is used commercially for the growth high-κ gate dielectrics [31,32]. Prior to high-κ dielectric deposition, native oxide must be removed to improve equivalent oxide thickness (EOT). ALD deposits are pin-hole free [71,72], but in first cycles of PEALD the precursor is chemisorbed to the surface but will not fill all the available sites due to steric hindrance [73–75]. The upcoming plasma oxygen will replace the organic ligands with oxygen and possibly oxidizes and/or causes surface defects. Substrate oxidation degrades the EOT and degrades the D_{it} [76]. III-V substrates affected even more, compared to silicon, as they do not grow a robust and protective oxide [77]. Correspondingly, in thermal ALD steam oxidizes the highly reactive chemisorbed organometallic precursor but will not react directly with substrate during dielectric growth. However, gate dielectrics grown by thermal ALD (TALD) have inferior electrical characteristics compared to PEALD films due to the higher concentration of bulk defects [31]. Residual oxidants are readily detected in the TALD as-deposited films due to the

surplus of water during deposition [33,34]. These residual oxidant species precipitate oxygen defects during post-heat treatment of MOS devices [33]. Interestingly, when ozone or plasma oxygen are used as the oxidant, instead of water vapor, such species (e.g. oxygen interstitials) are not detected in subsequent characterization [35].

The combination of two techniques might help to resolve this issue. Starting with TALD can protect the substrate from oxygen plasma after switching to PEALD. TALD films are susceptible to higher concentration of bulk defects including oxygen related defects. Oxygen vacancies cause numerous trap states [5,7] and, in turn, are the main component of trap assisted tunneling in high-κ gate leakage current [78]. Starting with TALD and then switching to PEALD helps with keeping the total number of bulk defects low, while maintaining a high quality interface. Even state-of-the-art analytical techniques are generally incapable of quantifying the oxygen stoichiometry and concentration in high-κ dielectric films to better than ~ 1 at%. Such a defect concentration, if uniformly distributed, translates into a large defect density > 10^{20} cm^{-3}. Consequently, electrical measurements are commonly used to infer the presence, concentration and nature of the defects in high-κ dielectric thin films [78,79].

While there are many papers that compare TALD and PEALD grown high-κ gate dielectrics, there is no systematic study of mixing the two techniques for optimum electrical characteristics. In this chapter an in-depth electrical characterization and comparison of high-κ dielectrics (HfO_2 and ZrO_2) grown by PEALD, TALD and mixed structures is presented.

3.2 RESULTS AND DISCUSSION

3.2.1 Gate Dielectric Thickness Evolution

In-situ spectroscopic ellipsometry was utilized to investigate the thickness evolution of the high-κ gate dielectrics during growth. A Tauc-Lorentz model was used to build an optical model for analyzing the raw ellipsometry data. The ellipsometry resolved the thicknesses of 7.88 and 8.78 nm for specimen with 60 cycles of thermal and plasma enhanced ALD zirconia, respectively. Interestingly, growth per cycle (GPC) of 0.131 and 0.132 nm were determined for thermal and plasma enhanced ALD, respectively, at 100 °C on silicon with native oxide. Assuming a constant GPC, the plasma enhanced ALD grown zirconia is 0.86 nm thicker than expected value (0.132 nm x 60 cycles). Fig. 3-1 depicts the thickness evolution of (a) plasma enhanced ALD and (b) thermal ALD with time for zirconia from *in-situ* ellipsometry.

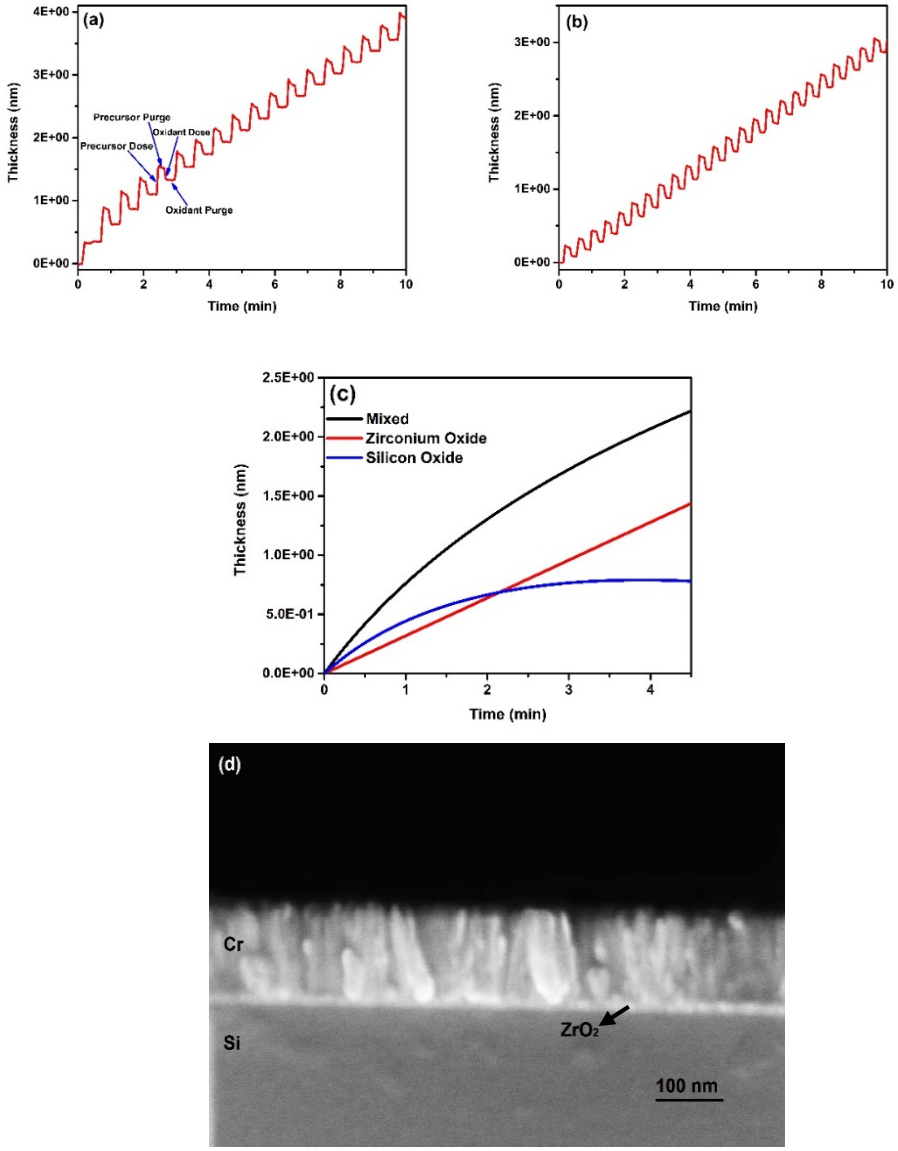


Figure 3-1 Real time thickness evolution of PEALD (a) and TALD (b) ZrO_2 thin films during growth (determined from in-situ ellipsometry using a Tauc-Lorentz model). (c) Resolving contributions of zirconium oxide and silicon oxide in PEALD grown ZrO_2 thin films assuming constant

GPC for ZrO_2. (d) FE-SEM cross section of the MOSCAP device with 60 cycles of PEALD grown ZrO_2.

Each individual step can be distinguished during an ALD cycle and studied independently in Fig. 3-1(a). The first cycles of plasma enhanced ALD have a higher GPC which gradually drops to 0.132 (nm) at approximately fourteen cycles. Conversely, thermal ALD has a steady growth per cycle from the first cycle. After the first cycle, the surface is not completely covered yet with the metalorganic molecules due to steric hindrance of the organometallic ligands and, as a result, oxygen plasma can oxidize the silicon readily [73,80]. The silicon oxide unit cell is larger than the unit cell of silicon in the growth direction and adds to the GPC of ZrO_2 in the ellipsometry results. Assuming a constant GPC for plasma enhanced ALD grown ZrO_2 (0.132 nm), the silicon oxidation was determined in Fig. 3-1(c). Evidently, silicon oxidation starts quickly and gradually slows down with growing ZrO_2 and eventually plateaus at 0.8nm. Fig. 3-1(d) illustrates the FE-SEM cross section of the MOSCAP device with 60 cycles of plasma enhanced ALD grown ZrO_2 (d).

Although, ALD is well known for pin-hole free thin films [80,81] but plasma oxygen can diffuse readily through the underlying layer even at 100

°C [82]. Atomic oxygen faces a lower thermodynamic barrier for diffusion compared to an oxygen molecule. Additionally, it takes a critical film thickness to inhibit oxygen diffusion completely. A. Afshar *et al*. reported that 45 cycles of thermal ALD grown alumina can protect a underlying silver layer completely from oxidation by plasma oxygen at 100 °C [82].

3.2.2 XPS Study

The XPS results for the zirconium 3d (a) TALD and (b) PEALD in as-deposited ZrO_2 films are shown in Figure 3-2. The FWHM of Zr peaks in both Fig. 3-2(a) and (b) confirm the presence of pure zirconium oxide and no sub oxide peak or any shoulder peak is recognizable. Fig. 3-2(c) and (d) illustrate the silicon substrate 2p peaks for TALD and PEALD as-deposited ZrO_2 films, respectively. The PEALD grown film have a higher silicon oxide concentration compared to TALD films (42 at% to 20 at%, respectively). The XPS signal exponentially decays with thickness and the silicon oxide forms on the interface, and as a result is disproportionately strong compared to the silicon substrate signal. Accordingly, the XPS result is a qualitative proof for the higher degree of substrate oxidation in PEALD growth compared to TALD growth.

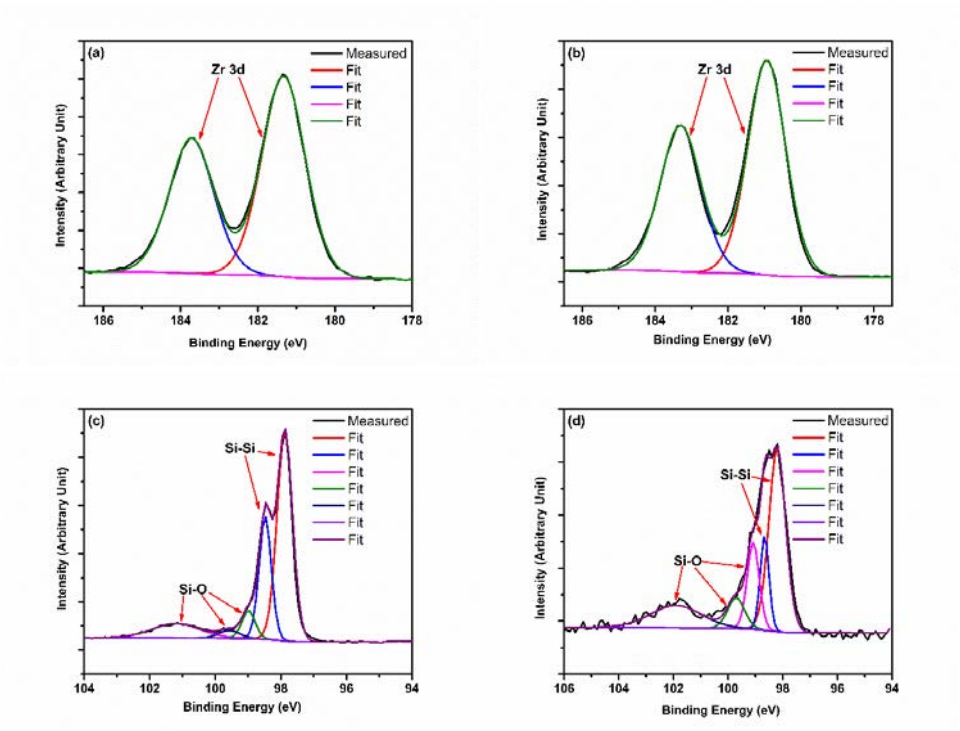


Figure 3-2 XPS results for Zr 3d for (a) TALD and (b) PEALD grown as-deposited zirconia films. Figure 3 (c) and (d) Si 2p substrate XPS peaks for TALD and PEALD grown as-deposited ZrO_2, respectively.

3.2.3 Capacitance Study

Fig. 3-3 (a-d) depicts the frequency dependent capacitance-voltage characteristics for ZrO_2 MOSCAPs. Keeping the total number of ZrO_2 cycles fixed (60 cycles), the number of TALD cycles are (a) 0, (b) 10, (c) 20, and (d) 60. Fig. 4(e) and (f) illustrate the CV characteristics for HfO_2 with (e) 0 and (f) 10 TALD, respectively. Also, the legend in Fig. 3-3 indicates the frequency of CV measurement. The capacitance

density in accumulation (large negative bias) first enhances and then diminishes sharply with increasing TALD cycles. In PEALD the substrate oxidation degrades the EOT and D_{it} [76] while in TALD remaining oxidant groups will turn into bulk defects during post-fabrication heat treatment [33]. As expected, having the whole 60 cycles deposited with thermal ALD will lead to copious bulk defects and capacitance instability in accumulation (Fig. 3-3(d)). Starting with 30 cycles of TALD and then switching to PEALD also reveals almost the same characteristics (data not shown here). TALD grown dielectrics generally have a lower dielectric constant mainly due to higher defect concentration [31]. The specimen with 10 cycles of TALD zirconia followed by 50 cycles of PEALD zirconia has the highest accumulation capacitance density (0.88 $\mu F/cm^2$). The relatively steep transition to accumulation in all CV characteristics suggest high quality interfaces for the MOSCAPs. Deep depletion can be detected from the finite slope at positive gate biases. Reaching deep depletion is a major indicator that the Fermi level is not pinned and that it moves into the other half of the band gap [83,84]. Furthermore, the frequency dispersion prior to entering accumulation, decreases systematically with the increasing number of thermal ALD cycles.

The hump before entering accumulation is mainly attributed to mid-gap D_{it} response [83,85]. The mid-gap D_{it} typically corresponds to semiconductor surface damage [86]. Consequently, increasing number of thermal ALD cycles can protect the semiconductor surface from the subsequent plasma oxygen. The hafnium oxide films also follow the same pattern. Furthermore, the low frequency (5K, 10K and 20K) capacitance of HfO_2 increases with increasing thermal ALD cycles which indicates better interfacial quality. Furthermore, the specimen displays a significantly lower frequency dispersion in accumulation with increasing thermal ALD cycles up to twenty cycles. Above twenty cycles of TALD the bulk defects dominate the CV response and amplify the frequency dispersion.

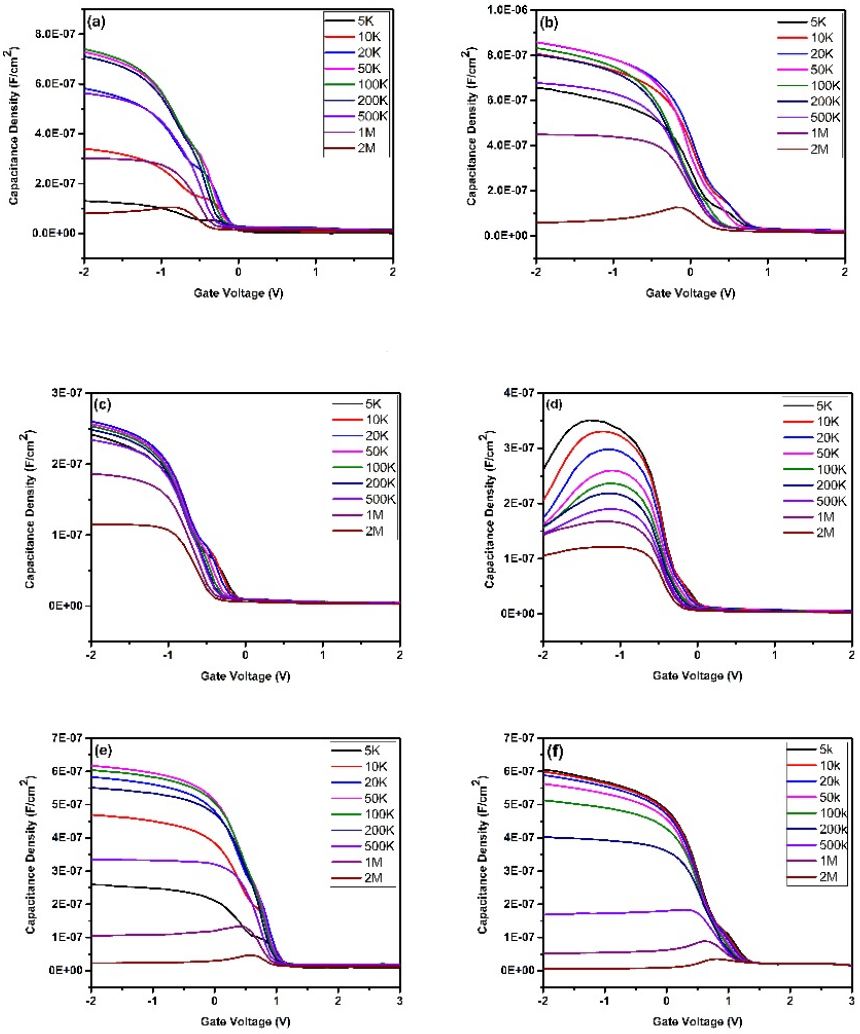


Figure 3-3 CV characteristics between -2V and 2 V of ZrO_2 gate dielectric MOSCAPs with (a) 0 and (b) 10, (c) 20 and (d) 60 cycles of thermal ALD. CV characteristics of between -2V and 3 V of HfO_2 gate dielectric MOSCAPs with (e) 0 and (f) 10 cycles of thermal ALD (the total number of cycles was kept 60 for all specimens).

3.2.4 Leakage Current

Figure 3-4(a) and (b) illustrate the leakage current of the PEALD and TALD grown zirconia dielectrics as a function of gate voltage. The gate dielectric leakage current densities are 0.045 and 838 $mA.cm^{-2}$ at -1 V gate bias for PEALD and TALD grown zirconia dielectrics. The gate dielectric leakage current is over four orders of magnitude higher for TALD grown zirconia compared to PEALD films. The copious bulk defects in thermal ALD grown zirconia amplifies the leakage current significantly.

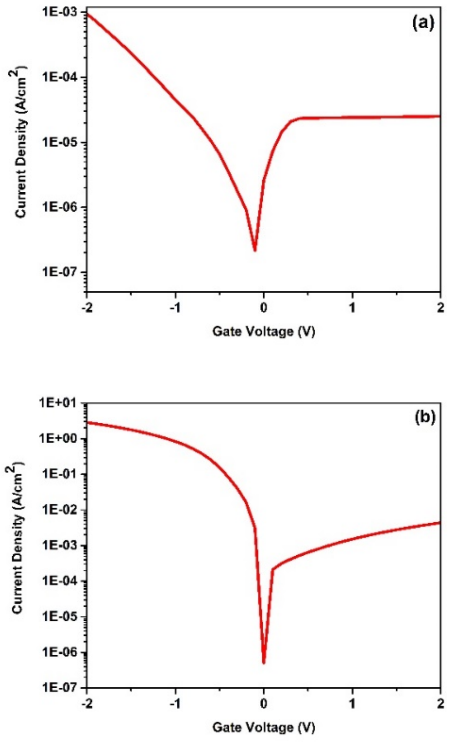


Figure 3-4 IV characteristics between -2V and 2 V of (a) plasma enhanced and (b) thermal ALD grown ZrO_2 MOSCAPs.

The leakage data for PEALD zirconia follows direct tunneling. Direct tunneling (DT) component of current density can be calculated according to following equation in one dimension [76,87,88].

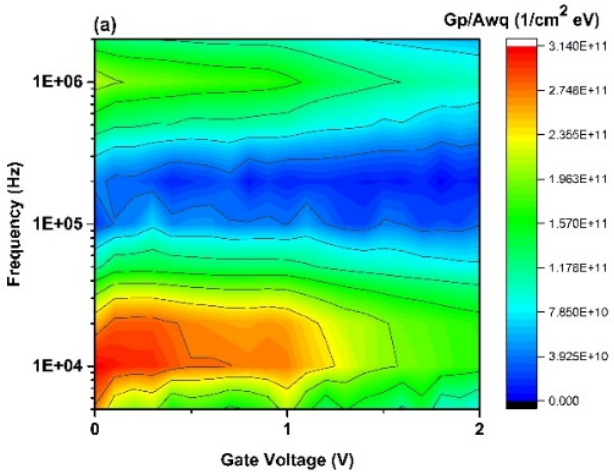
$$J_{DT} = \frac{q^3}{16\pi^2 \hbar \emptyset_{OX}} E^2 . \exp\left(\frac{-4\sqrt{2m^* \emptyset_{Ox}{}^3}}{3\hbar q} E \left(1 - \left(1 - \frac{V}{\emptyset_{OX}}\right)^{\frac{3}{2}}\right)\right) \qquad 3\text{-}1$$

Where m^*, q, ħ, $\emptyset_{Ox}$ and E are the effective mass, elementary charge, the reduced Planck's constant, effective barrier height and the electric field, respectively.

On the other hand, the leakage current for TALD grown films is dominated by trap assisted tunneling. Trap assisted tunneling occurs when carriers tunnel through the dielectric from occupied trap states. The trap centers are intermediate energy states, commonly, formed by defects. TALD grown dielectrics are assumed to have plentiful oxygen related defects mainly due to oxidant groups from abundant water during growth [33,34]. Furthermore, high density of traps can provide a hopping path for leakage.

3.2.5 Interfacial quality

Figure 3-5 depicts the normalized parallel conductance peak values as a function of gate voltage and frequency, where w is the frequency, A the active region area, G_p the parallel conductance, and q the carrier charge. Fig. 3.5(a) and (b) represent normalized parallel conductance of the zirconia MOSCAPs with 0 and 20 TALD cycles, respectively (total number of cycles were 60). The D_{it} can be calculated by multiplying the normalized parallel conductance peak by a factor of 2.5 [89]. The D_{it} at 50 KHz for specimens with 0, 10, 20, and 60 cycles of TALD zirconia were extracted to be $3.1x10^{11}$, $4.3x10^{10}$, $1.8x10^{10}$, and $4.5x10^{10}$ cm^{-2} eV^{-1}, respectively.



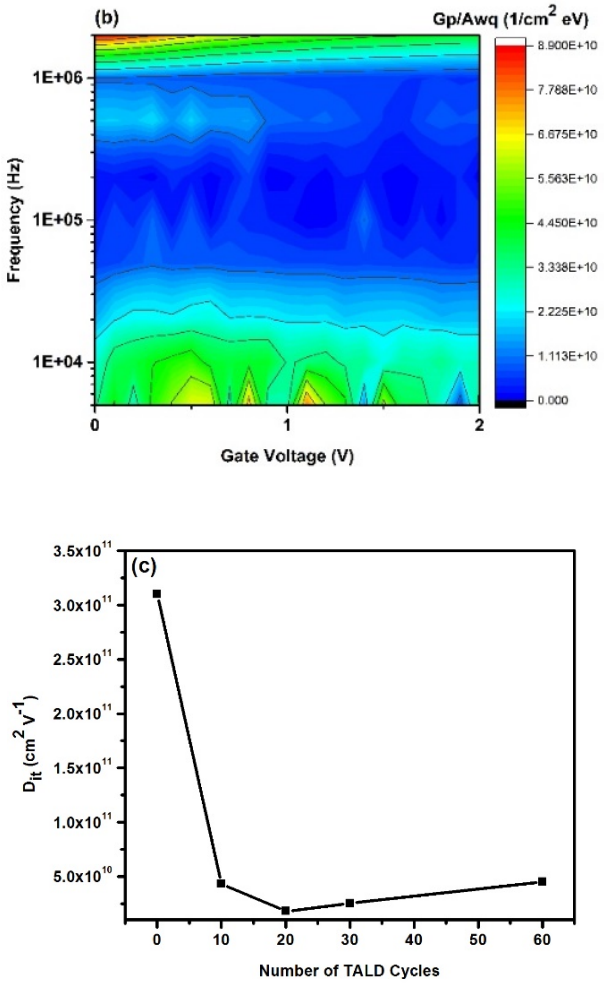


Figure 3-5 Conductance map between 0 V to 2 V and 10 KHz to 2 MHz of ZrO_2 gate dielectric MOSCAPs with (a) 0 and (b) twenty cycles of thermal ALD. (c) Density of interfacial traps with respect to number of TALD cycles (total number of cycles were 60 for all specimens).

The D_{it} results show a very low concentration of interfacial states even in the PEALD grown zirconia which reveals around one order of magnitude lower D_{it} than common high-κ/Si interfaces [4]. The low

concentration of interfacial states implies that the MOSCAP has a high quality of oxide-semiconductor interface. The main reason for this can be attributed to the low deposition temperature which, in turn, reduces the magnitude of thermal expansion mismatch stress. K. Bothe *et al.* reported $4x10^{10}$ cm^{-2} eV^{-1} D_{it} for MOSCAPs with 40 cycles of PEALD zirconia on GaN grown at 100 °C substrate temperature [16]. Additionally, D_{it} systematically decreases with increasing number of thermal ALD cycles and then rises a small amount at higher TALD cycles. This implies that plasma oxygen contributes to the density of interfacial defects. For higher number of TALD cycles the remaining oxidant species generate abundant oxygen interstitials migrate to interface during post-fabrication heat treatment which, in turn, increases the D_{it} [33,34]. The D_{it} of the MOSCAP with 20 cycles of TALD followed by 40 cycles of PEALD is very low ($1.8x10^{10}$ cm^{-2} eV^{-1}) and comparable to the Si/SiO_2 interface mainly due to the combination of low temperature growth and twenty cycles of protective thermal ALD ZrO_2.

The conductance map provides the opportunity for study of the nature of the interfacial defects. It also provides a measure of the efficiency of Fermi level moving in the band gap [90,91]. The normalized parallel conductance shifts over two orders of magnitude as the gate bias is swept

from -0.25 and -1 V for all specimens, which indicates significant band bending with respect to gate bias sweeping.

4 TERNARY OXIDES

This chapter covers the deposition, electrical characterization and comparison of ternary complex oxide high-κ gate dielectrics to binary gate oxides.

4.1 INTRODUCTION

HfO_2, ZrO_2 and Al_2O_3 have been investigated extensively as a replacement for conventional SiO_2 gate dielectric. This is due to their higher dielectric constant, large conduction band offset, and good kinetic and thermodynamic stability [4]. However, high-κ binary oxides suffer from poor dielectric-semiconductor cohesion, high interfacial trap density, threshold voltage instability, degraded reliability and low carrier mobility compared to SiO_2 [1,2]. These shortcomings may be addressed by the introduction of high-κ ternary complex oxides which have a higher degree of flexibility and tuning [5]. Complex oxide thin films have been studied extensively for memory, spintronic, resistive switching, tunnel junction and thermoelectric applications [5–7].

The dielectric constant and band gap of the HfO_2 and ZrO_2 depend strongly on their crystal structure. First-principles study predicts very high dielectric constant (30-40) for the tetragonal phase, while the monoclinic phase has a moderate dielectric constant (20) for both hafnia and zirconia

[13]. At room temperature and atmospheric pressure the monoclinic phase is thermodynamically favorable in bulk zirconia and hafnia. Stabilization of the tetragonal zirconia was previously reported in ultra-thin films [92,93]. Surface energy dominates the Gibbs free energy in low dimensional structures and stabilizes the tetragonal zirconia. Interestingly, stabilization of tetragonal hafnia has not been reported. This is attributed to the very low surface energy difference between tetragonal and monoclinic phases in hafnia compared to zirconia ($0.16 = \frac{\Delta\gamma_{m-t}^{HfO_2}}{\Delta\gamma_{m-t}^{ZrO_2}}$) [93].

Introducing zirconia to hafnia helps with stabilizing the tetragonal phase and consequently enhances the dielectric constant. Furthermore, Gilmore *et al.* reported stabilization of tetragonal zirconia at room temperature by introducing alumina to the mother phase [94,95]. The tetragonal phase can also be stabilized using laminate structures but introducing new interfaces increases defect concentration. R. I. Hegde *et al*. reported incorporation of zirconia into hafnia for advanced gate stack applications using ALD and sputtering deposition techniques [54,60,96]. Incorporation of zirconia enhanced the dielectric constant, decreased the leakage current and interfacial trap states, while lowering the threshold voltage and subthreshold swing of hafnia [13]. Furthermore, adding alumina increases the band gap, and consequently might suppress the gate dielectric

leakage current. C. Mahata *et al.* compared dielectric properties of hafnia and hafnium aluminate. Introducing alumina increased the band gap (from 5.65 to 6.05 eV), while reducing the capacitance density and D_{it} [97]. On the other hand, Y. Lu *et al.* reported the formation of numerous bulk trap states with incorporation of alumina into hafnia using metalorganic chemical vapor deposition (MOCVD) technique [98]. Their results confirmed a dominant Poole-Frenkel leakage current mechanism in hafnium aluminate. Y. Li *et al*. utilized pulsed-laser deposition (PLD) to grow zirconium aluminate thin films [99]. Their results showed slight enhancement in the band gap with introduction of the alumina into zirconia.

Oxide thin films have been deposited by variety of physical vapor and chemical vapor deposition techniques [18–20]. The atomic layer deposition (ALD) technique utilizes organometallic precursors and divides the deposition of one single layer into two self-terminating reactions [22]. ALD provides extremely conformal deposition with thickness control down to the atomic scale [28]. Sequential pulses prevents any gas phase reaction [27]. The 2007 edition of International Technology Roadmap for Semiconductors (ITRS) included the ALD as the technique for growing high-κ gate dielectrics [21]. Complex oxides can be grown using alternate ALD cycles of each individual binary oxide.

While there are many studies of ALD grown binary high-κ oxides, there is no systematic study of high-κ ternary complex oxides for advanced gate dielectric applications. In this chapter, in-depth electrical characterization and comparison of the high-κ complex oxides ($HfZrO_x$, $ZrAlO_x$, and $HfAlO_x$) grown by low temperature PEALD for advanced gate dielectric applications is presented.

4.2 Results and Discussion

4.2.1 Growth and Optical Properties

In-situ spectroscopic ellipsometry was utilized to investigate the thickness evolution of the high-κ complex oxides during growth. A Tauc-Lorentz model was used to analyze the raw ellipsometry data. The ellipsometry resolves the thicknesses of 9.0, 10.4, and 9.9 nm for hafnium zirconate (HZO), hafnium aluminate (HAO) and zirconium aluminate (ZAO) thin films, respectively, after 60 ALD cycles. Figure 4-1(a) shows the thickness evolution of the hafnium aluminate during growth. Alternate hafnia and alumina cycles were used with a total of 60 cycles.

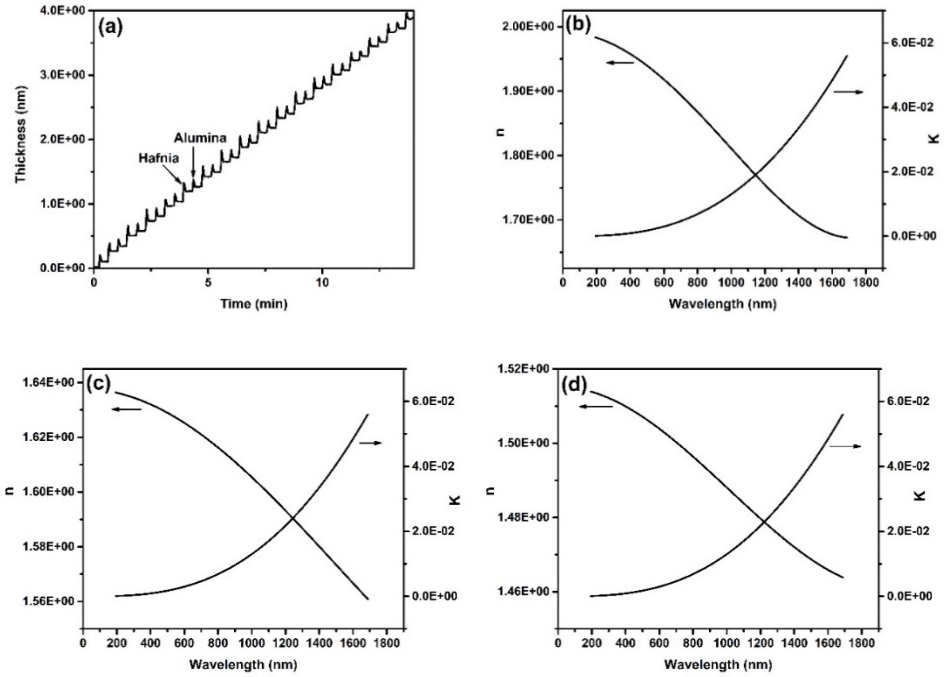


Figure 4-1(a) Thickness evolution of HAO gate dielectric during growth. Refractive index and extinction coefficient of (b) HZO, (c) HAO and (d) ZAO complex oxide dielectrics.

Figure 4-1(b), (c) and (d) illustrate the real component of refractive index and the extinction coefficient for HZO, HAO, and ZAO dielectrics with respect to incident light wavelength. The refractive at 400nm wavelength for HZO, HAO and ZAO are 1.96, 1.63, and 1.51, respectively. The real and imaginary components of complex dielectric constant are n^2-k^2 and 2nk, respectively. The extinction coefficient is much smaller than the real component of the refractive index in the visible spectrum according to Fig.

4-1(b), (c) and (d). Hence, the dielectric constant of high-κ complex oxides at visible spectrum (400-780 nm) is approximately equal to n^2. In conclusion, hafnium zirconate dielectric is expected to have higher capacitance density compared to the other complex oxides. However, it should be noted that solid state devices work at frequencies orders of magnitude lower than visible spectrum.

4.2.2 XPS results

Figure 4-2 shows the XPS results for the zirconium 3d (a) and hafnium 4f (b) in as-deposited hafnium zirconate films. The FWHM of Zr and Hf peaks in both Fig. 4-2(a) and (b) confirm the presence of pure zirconium oxide and hafnium oxide, respectively. Furthermore, no sub oxide peak or any shoulder peak is perceptible. The XPS results confirmed the composition as $Hf_{0.55}Zr_{0.45}O_2$.

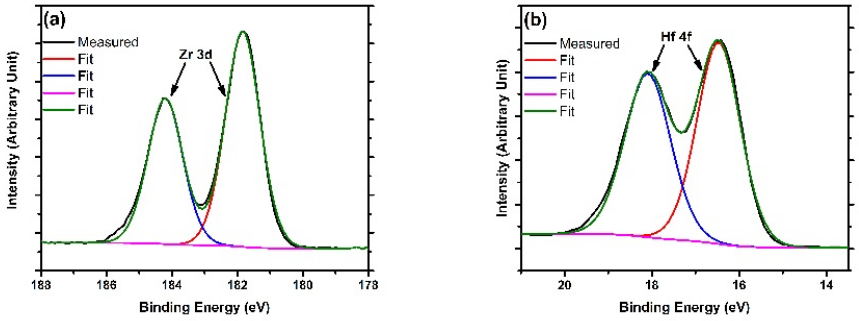


Figure 4-2(a) and (b) show the x-ray photoelectron spectroscopy (XPS) results for Zr and Hf in 15 nm thick hafnium zirconate.

4.2.3 Capacitance Study

Fig. 4-3 depicts the capacitance-voltage characteristics at 100 KHz for (a) hafnium zirconate (HZO), (b) hafnium aluminate (HAO), and (c) zirconium aluminate (ZAO) dielectric MOSCAPs grown on silicon. The HZO, HAO and ZAO have capacitance densities of 2.05, 0.85 and 1.10 μF.cm^{-2} at -2V. The following equations were used to calculate the capacitance and dielectric constant of the high-κ complex oxides.

$$C_{Extracted} = \varepsilon_0 \left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{acc}}{\varepsilon_S} \right)^{-1} \qquad 4-1$$

$$C_{ox} = \varepsilon_0 \frac{\varepsilon_{ox}}{t_{ox}} \qquad 4-2$$

where t_{ox}, C_{ox}, ε_{ox}, ε_s, ε_0, t_{acc}, and $C_{Extracted}$ are oxide thickness, oxide capacitance, oxide dielectric constant, semiconductor dielectric constant, dielectric constant of vacuum, channel thickness, and the measured capacitance [16]. Accordingly, using equation 4-1, the HZO, HAO and ZAO dielectrics have relative dielectric constants of 26.1, 10.9 and 13.9, respectively. The CV characteristics of the dielectrics on silicon reveal insignificant hysteresis which confirms the high quality of the interface and the low density of interfacial traps (D_{it}) [30]. The steep transition to accumulation suggests very effective band bending with respect to the gate voltage and possibly very low subthreshold swing [69,89]. Deep depletion can be detected from the finite slope at

positive gate biases [76]. Reaching deep depletion is the major indicator that the Fermi level is not pinned and actually moves into the other half of the band gap [83,84].

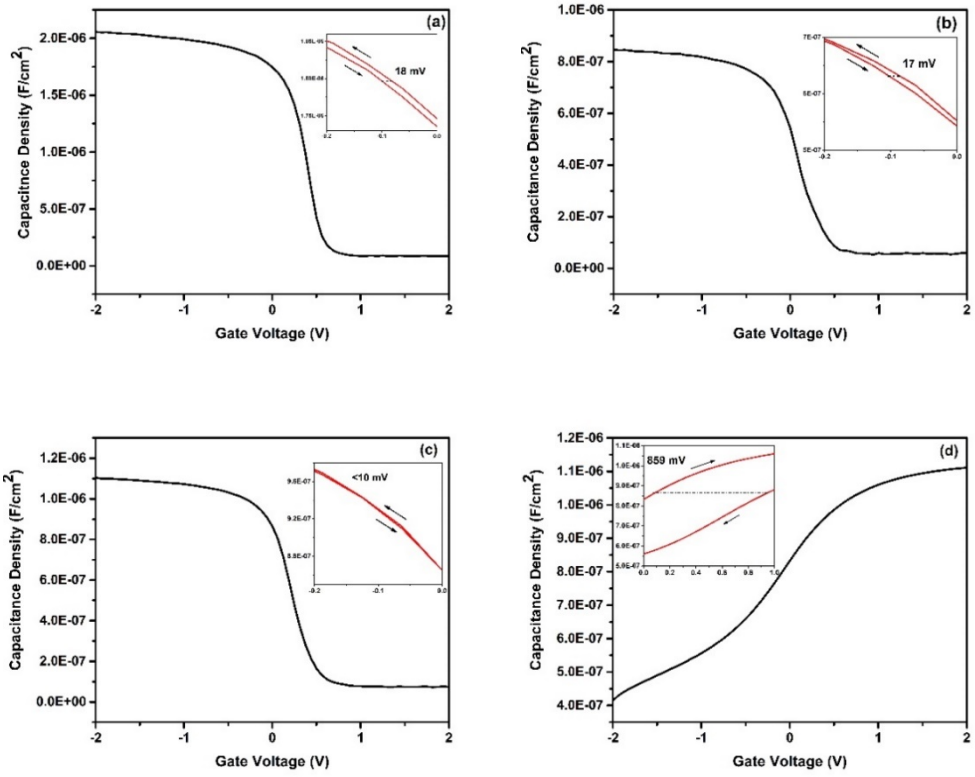


Figure 4-3 CV characteristics between -2V and 2 V of (a) hafnium zirconate, (b) hafnium aluminate and (c) zirconium aluminate gate dielectric MOSCAPs on P-type silicon (100) substrate at 100 KHz. Figure 3(d) illustrates the CV characteristics of between -2V and 2 V of hafnium zirconate gate dielectric MOSCAP on InP at 100 KHz. (Insets: hysteresis of C-V cycles at 100 KHz)

Fig. 4-3(d) illustrates the 100 KHz CV characteristics of a MOSCAP with the hafnium zirconate dielectric grown on n-type (100) indium phosphide. Evidently, the transition to accumulation is not as steep as silicon based MOSCAPs and the hysteresis is also significantly larger which indicates much higher density of interfacial traps.

The capacitance-voltage (CV) characteristics for nanolaminated ($Hf_{1-x}Zr_xO_2$) and stacked (HfO_2/ZrO_2) MOSCAPs on GaN and InP is shown in Fig. 4-4 (a-d) at 10KHz. The total number of plasma enhanced ALD cycles was fixed at 40 cycles for all specimen. Fig. 2(a) and (b) illustrate the CV characteristics of MOSCAPs with stacked and nanolaminated gate dielectrics, respectively, on GaN. The capacitance density in accumulation (large positive bias) is larger for stacked MOSCAP compared to nanolaminated one. The inset in Fig. 2(a) and (b) reveal a very low hysteresis of 35 and 45 mV for stacked and nanolaminated gate dielectrics, respectively, on GaN. The combination of very low hysteresis and steep transition into accumulation in CV characteristics of GaN MOSCAPs suggest a low density of interfacial traps, and as a result a reliable gate dielectric-semiconductor interface. Furthermore, deep depletion can be detected from the finite slope at the negative gate biases. Reaching deep depletion is a strong indication

that the Fermi level is not pinned and moves through the band gap [83,84]. Moreover, Fig. 4-4(c) and (d) depict the CV characteristics of the stacked and nanolaminated structures, respectively, on InP. Evidently, the nanolaminated structure reveals lower hysteresis, steeper transition to accumulation and larger capacitance density in accumulation.

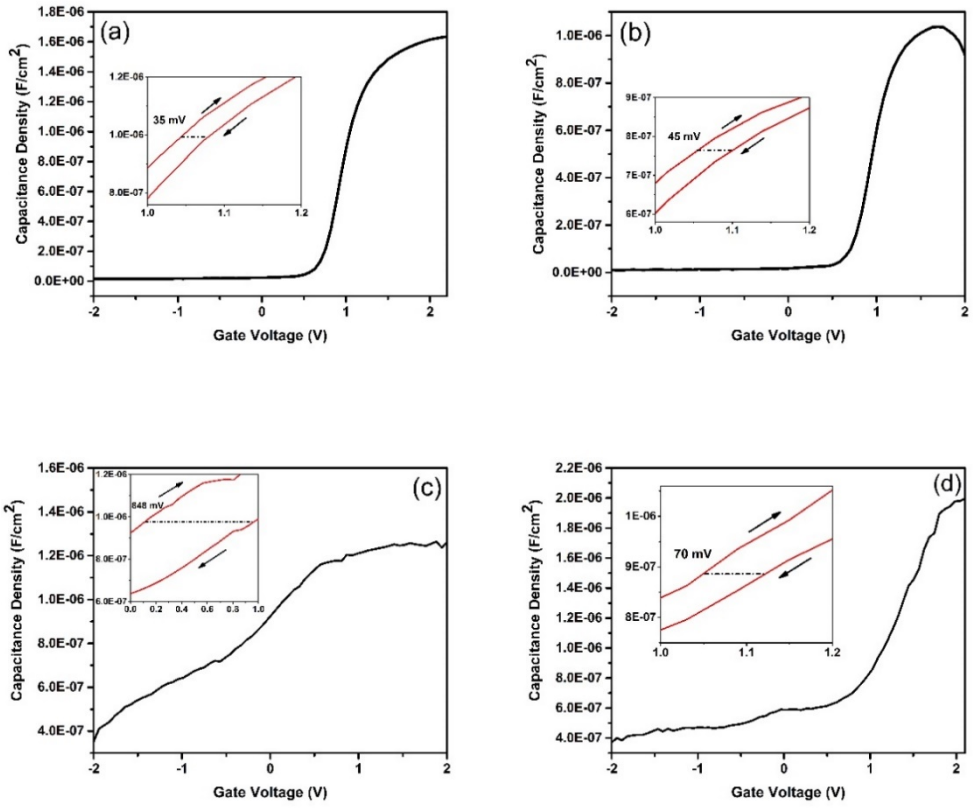


Figure 4-4 CV characteristics between -2V and 2 V of MOSCAPs at 10KHz (a) stacked on GaN, (b) nanolaminated on GaN, (c) stacked on InP and (d) nanolaminated on InP. Inset is the hysteresis in the CV characteristics of GaN and InP MOSCAPs at 10 KHz.

4.2.4 Leakage Current

Figure 4-5 (a) and (b) show the gate dielectric leakage current for hafnium zirconate, hafnium aluminate, and zirconium aluminate dielectric MOSCAPs on silicon and indium phosphide substrates, respectively. Evidently, on both substrates the hafnium zirconate has the lowest dielectric leakage current, while zirconium aluminate has the highest. Interestingly, hafnium zirconate has the lowest band gap among the three. The leakage data for hafnium zirconate follows direct tunneling according to equation 3-1.

On the other hand, hafnium aluminate and zirconium aluminate demonstrate significantly higher dielectric leakage current. Y. Lu *et al.* previously reported the Poole-Frenkel leakage mechanism in hafnium aluminate [98]. Poole-Frenkel leakage suggests the presence of copious defect states. Both HfO_2-Al_2O_3 and ZrO_2-Al_2O_3 systems display almost no miscibility at room temperature [100,101], increasing number of two dimensional defects, while HfO_2 and ZrO_2 are completely miscible [13].

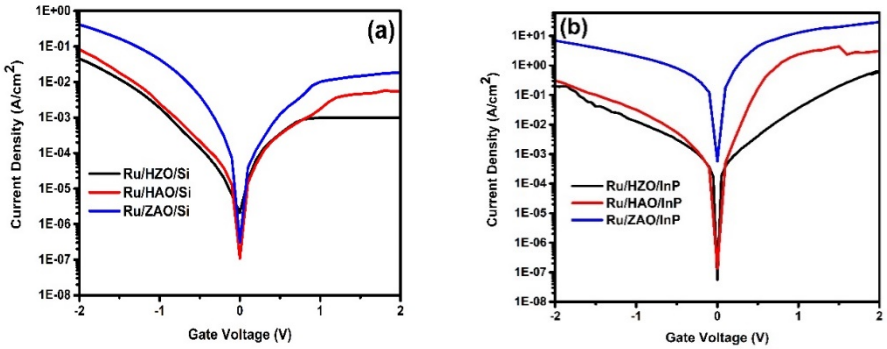


Figure 4-5 The gate dielectric leakage current for hafnium zirconate (HZO), hafnium aluminate (HAO), and zirconium aluminate (ZAO) dielectric MOSCAPs on (a) silicon and (b) indium phosphide substrates.

4.2.5 Interfacial quality

Figure 4-6(a) illustrates the equivalent circuit of the planar MOSCAP at accumulation where C_G, C_{it}, R_{it}, C_{acc}, R_S and Z_{body} are the gate oxide capacitance, capacitance of interfacial trap states, resistance of interfacial trap states, channel capacitance, series resistance and impedance of the substrate, respectively. The series resistance practically represents the channel resistance and can be used to calculate the carrier mobility [30]. Figure 4-6(b) shows the simplified circuit layout of Fig. 4-6(a) where G_p, C_p, and Z_{body} are the parallel conductance, parallel capacitance and impedance of the substrate, respectively. Figure 4-6(c) and (d) depict the normalized parallel conductance (G_p/Awq) with respect to gate voltage and sweeping frequency where w represents

the radial frequency, A the active region area, G_p the parallel conductance, and q the elementary charge for hafnium zirconate dielectric on silicon and indium phosphide, respectively. The nature of the interfacial trap centers can be studied through the conduction map. The efficiency of the Fermi level moving through the band gap with respect to gate voltage can also be studied using this map [90,91]. Normalized parallel conductance rises over two orders of magnitude with sweeping gate voltage from 1 to -0.5 V for hafnium zirconate gate oxide on silicon MOSCAP according to Fig. 4-6(c) which reveals very efficient band bending. Interestingly, the same dielectric has lower efficiency in band bending on indium phosphide. Furthermore, hafnium zirconate has higher frequency dispersion on indium phosphide compared to silicon.

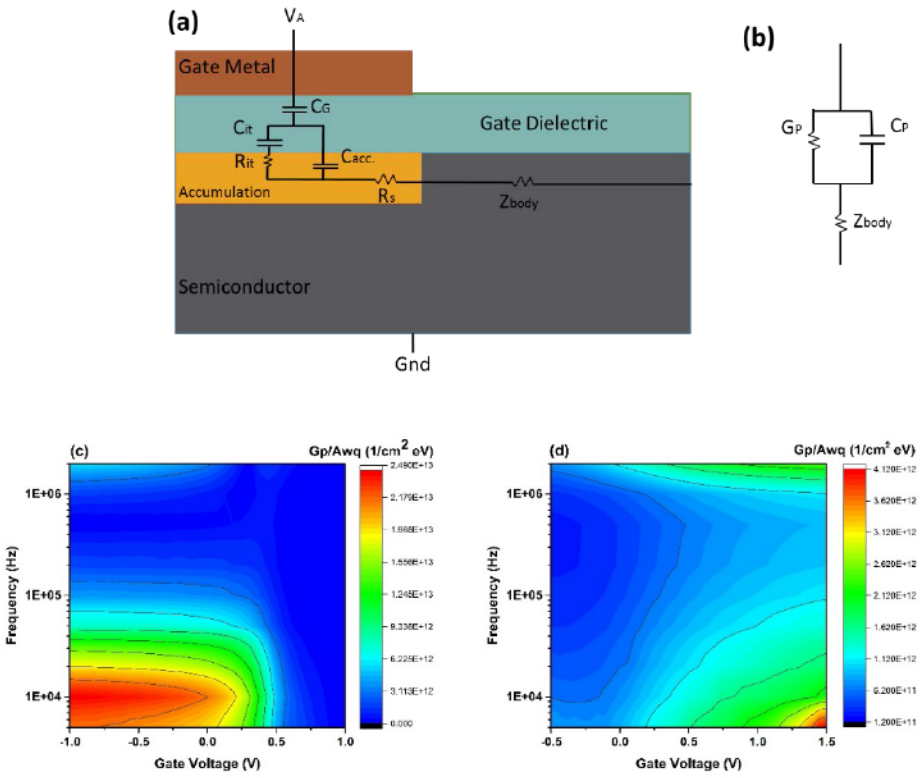


Figure 4-6(a) Equivalent circuit of a planar MOSCAP. (b) Simplified circuit layout of a planar MOSCAP. The parallel conductance (Gp) with respect to gate voltage and sweeping frequency for hafnium zirconate dielectric on (c) silicon and (d) indium phosphide.

The density of interfacial trap states (D_{it}) can be calculated by multiplying the normalized parallel conductance by a factor of 2.5 according to equation 4-3 [89]. The D_{it} calculations for the oxides on silicon at 1V and 100KHz, using parallel conductance, give 2.61×10^{10},

2.95×10^{11}, and 2.71×10^{10} cm^{-2} eV^{-1} density of interfacial traps for hafnium zirconate, hafnium aluminate, and zirconium aluminate, respectively. These D_{it} numbers are very low and comparable to D_{it} measurements for the Si/SiO_2 interface [16,102]. The same method gives roughly two orders of magnitude higher D_{it} numbers for the same dielectrics on indium phosphide which is also comparable to best numbers in literature for III-V semiconductors [76,89].

$$D_{it} = 2.5 \frac{G_P}{Awq} \qquad 4-3$$

The ultra-low concentration of interfacial trap states implies that the oxide-semiconductor interface is of high quality. The main reason for this can be attributed to the low deposition temperature (100 °C) which, in turn, reduces the thermal expansion mismatch stress, and the high post fabrication heat treatment (510 °C) which anneals out the interfacial defects. K. Bothe *et al.* reported 4×10^{10} cm^{-2} eV^{-1} D_{it} for MOSCAPs with a 5.4 nm thick ZrO_2 on GaN grown at 100 °C substrate temperature [16]. The density of interfacial trap states (D_{it}) can also be measured using the hysteresis from CV characteristics (equation 4-4) [16],

$$D_{it} = \Delta V \frac{C_{ox}}{qE_g} \qquad 4-4$$

Where ΔV, C_{ox}, q and E_g stand for hysteresis, gate oxide capacitance, elementary charge and semiconductor band gap, respectively.

The results from the two methods are generally in agreement with each other. According to equation 4-4 the D_{it} is directly proportional to the hysteresis [16]. The D_{it} results from equation 4-4 for our MOSCAPs agrees with the parallel conductance method calculations. Finally, the hafnium zirconate dielectric has an equivalent oxide thickness (EOT) of 1.4 nm. The following table summarizes main properties of complex oxide MOSCAPs.

Table 4-1 electrical properties of complex oxide base MOSCAPs.

	D_{it} from Gp (at 1V inv. and 100KHz) [1/cm^2 eV]	D_{it} from hysteresis (at 1V inv. and 100KHz) [1/cm^2 eV]	Leakage current density (at 1V acc.) [Amp/cm^2]	EOT (at 1V acc. and 100KHz) [nm	ε_{ox} (at 2V acc. and 100KHz)
Ru/30(ZO.HO)/InP	8.62E+11	2.19E+12	3.57E-2	2.944	1.26E+01
Ru/30(ZO.HO)/Si	2.61E+10	2.45E+10	1.73E-3	1.400	2.61E+01
Ru/30(AO.HO)/InP	1.31E+12	1.64E+12	2.71E-1	8.128	5.16E+00
Ru/30(AO.HO)/Si	2.95E+11	2.18E+10	2.46E-3	2.864	1.09E+01
Ru/30(AO.ZO)/InP	7.1E+13	2.80E+12	1.09E+1	6.453	6.38E+00
Ru/30(AO.ZO)/Si	2.71E+10	1.66E+10	4.31E-2	3.803	1.39E+01

4.2.6 Band offset measurements

The band alignment of the gate dielectric and channel plays an important role in MOS transistor operation. The type and degree of band offset at both the conduction and valence band are crucial for a low gate dielectric leakage in CMOS technology. The 2001 edition of International Technology Roadmap for Semiconductors (ITRS) stated that a finite band offset (>1eV) is needed to suppress the leakage current [11]. To determine the valence band offset (VBO), a core-level photoemission-based method was used similar to that of Edge *et al.* [103] and Kraut *et al.* [104,105]. The shallow core-level peaks were acquired to the top of the valence band (VB) for thick (90 cycles) films of ZrO_2 and

nanolaminated ($Hf_{1-x}Zr_xO_2$) on InP substrate. The valence band maximum (VBM) was determined using a linear extrapolation method. To obtain the VBO the resulting binding energy differences between the core-level peaks and valence band maxima (E_v) for the dielectrics and the InP substrate were calculated and combined with core-level binding energy differences for heterojunctions according to equation 4-5. Using the band gap of the gate dielectrics from the ellipsometry results, the conduction band offsets (CBO) were calculated according to equation 4-6.

$$\Delta E_v = (E_{In\ 3d} - E_v)_{InP} - (E_{Zr\ 3d} - E_v)_{Thick\ Dielectric} - (E_{In\ 3d} - E_{Zr\ 3d})_{Dielectric/InP} \quad 4-5$$

$$\Delta E_c = (E_g)_{Dielectric} - (E_g)_{InP} - \Delta E_v \quad 4-6$$

Where $(Eg)_{Dielectric}$ is the bandgap of the gate dielectric, $(Eg)_{InP}$ is the bandgap of indium phosphide, ΔEv is the VBO and the ΔEc is the CBO. Also, E_{In3d}, E_{Zr3d}, and E_V refer to In3d binding energy, Zr3d binding energy and core level valence energies, respectively.

Roughly 15 nm (total 90 cycles) thick gate dielectrics (ZrO_2 and $Hf_{1-x}Zr_xO_2$) were grown on InP and used to obtain the XPS spectra of the bulk structures. The ~1.4 nm (total 10 cycles) gate dielectrics (ZrO_2

and $Hf_{1-x}Zr_xO_2$) were also grown on InP to obtain XPS spectra from both the dielectric oxides and the underlying indium phosphide. Figure 4-7 shows the shallow core-level and VB spectra for (a) substrate InP, (b) thick (~15 nm) ZrO_2 /InP, (c) thick (~15nm) $Hf_{1-x}Zr_xO_2$ /InP, (d) thin (~1.4) nm ZrO2 /InP and (e) thin (~1.4) nm $Hf_{1-x}Zr_xO_2$ /InP heterojunctions that were utilized to determine the band offsets. The insets in figure 4(d) and (e) show the XPS results for the zirconium 3d in as-deposited ZrO_2 and $Hf_{1-x}Zr_xO_2$ films, respectively. The FWHM of Zr peaks in both Fig. 4-7(d) and (e) confirm the formation of zirconium oxide. Furthermore, no sub oxide peak or any shoulder peak is perceptible. Figure 4-7(d) and (e) also show the In 3d XPS peaks with a thin (~1.4nm) dielectric to enhance the X-ray photoelectron signal from the interface. The peaks with a higher binding energy component of In $3d_{5/2}$ and $3d_{3/2}$ are related to In_2O_3.

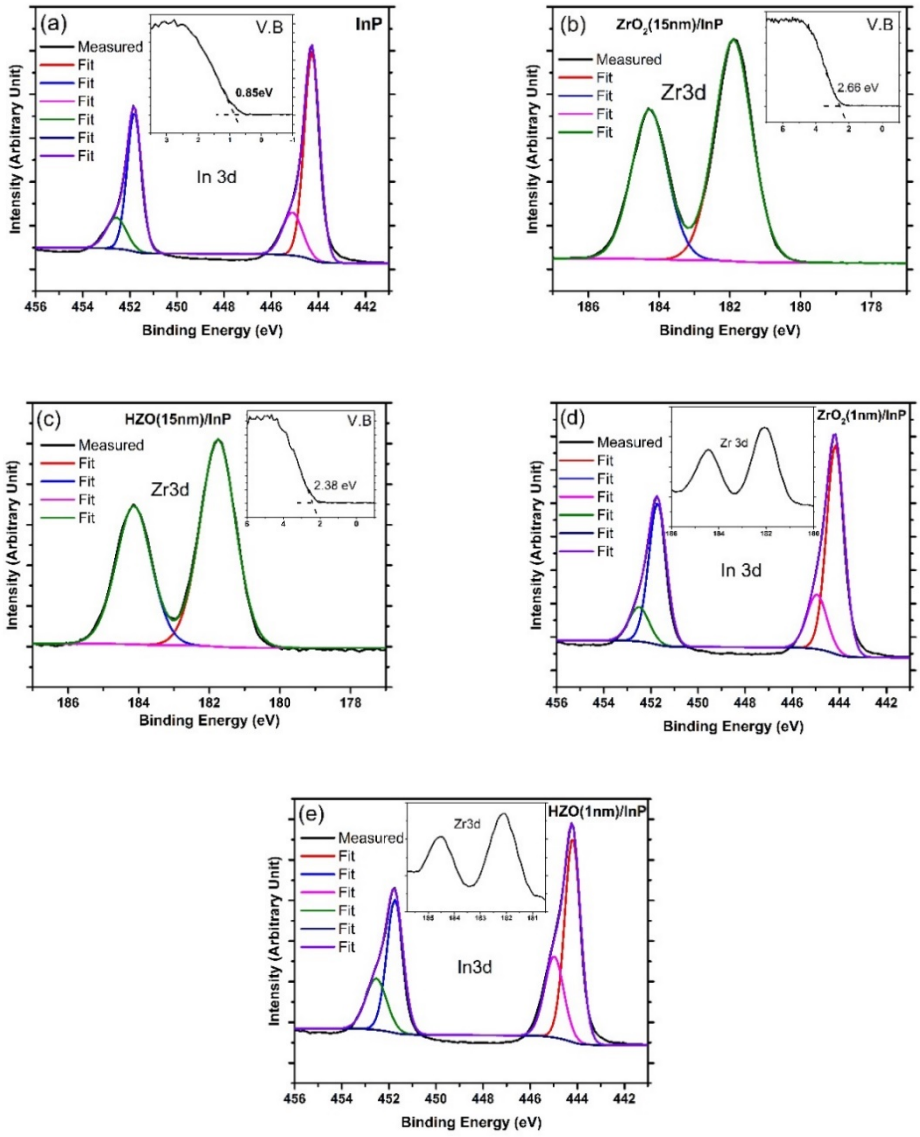


Figure 4-7 Shallow core-level and VB photoelectron spectra for (a) bare n-InP(100), (b) 15 nm ZrO_2 /InP, (c) 15nm $Hf_{1-x}Zr_xO_2$(HZO)/InP, (d) 1.4 nm ZrO_2/InP, and (e) 1.4 nm $Hf_{1-x}Zr_xO_2$(HZO)/InP heterojunctions. The insets show high resolution scans of the VB regions for the bare (a) n-InP(100), (b) 15 nm

ZrO_2 /InP, and (c) 15nm $Hf_{1-x}Zr_xO_2$(HZO)/InP, and also Zr 3d in (d) 1.4 nm ZrO_2/InP, and (e) 1.4 nm $Hf_{1-x}Zr_xO_2$(HZO)/InP heterojunctions.

Figure 4-8 depicts the band structure of the heterojunctions schematically. The VBOs (from equation 4-5) of 1.51 and 1.03 eV were measured for ZrO_2/InP and $Hf_{0.25}Zr_{0.75}O_2$/InP heterojunctions, respectively. Plugging the band gap of the dielectrics from ellipsometry (5.8 and 5.9 eV for ZrO_2 and $Hf_{0.25}Zr_{0.75}O_2$, respectively) into the equation 4-6, the CBOs of 2.95 and 3.53 eV were calculated for ZrO_2/InP and $Hf_{0.25}Zr_{0.75}O_2$/InP heterojunctions. Intriguingly, the nanolaminated structure has a lower VBO while having larger band gap. Hafnia has slightly larger band gap compared to zirconia (0.3 eV) [16,106] and introduction of the hafnia to zirconia will widen the band gap [13]. On the other hand, the larger band gap of hafnia is offset by its larger VB(0.6 eV) [106] compared to zirconia.

In conclusion, introduction of the hafnia widens the band gap and increases the CBO but the VBO shrinks mainly due to the VB width enlarging.

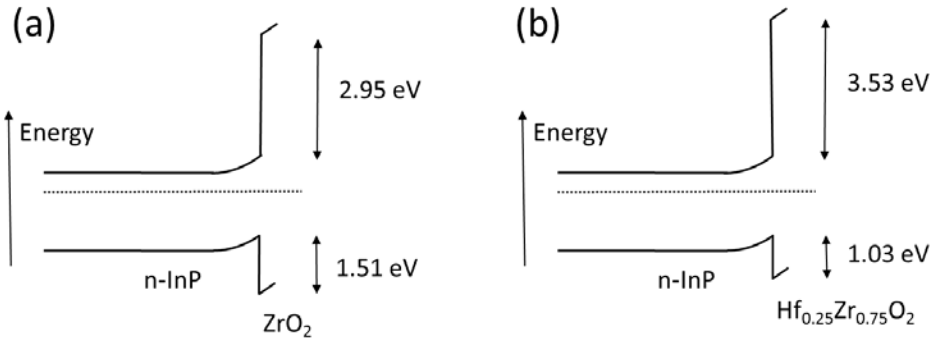


Figure 4-8 Band diagrams for (a) ZrO_2/n-InP(100) and (b) $Hf_{0.25}Zr_{0.75}O_2$ /n-InP(100) heterojunctions.

5 CONCLUSIONS AND FUTURE WORK

This Chapter presents the conclusions and future work for this work.

5.1 CONCLUSIONS

The PEALD and TALD grown high-κ gate dielectrics have substantial differences. PEALD grown oxides show higher capacitance density for the same number of cycles and dramatically lower leakage current while higher density of interfacial traps. On the other hand, TALD grown dielectrics reveal higher bulk defects. The leakage current is dominated by direct tunneling in PEALD grown oxides.

In this work, we developed a process where we started with TALD and then switched to PEALD which protects the substrate surface from plasma oxygen and lowers the D_{it}. Starting with ten cycles of TALD and then switching to PEALD enhanced the capacitance density while decreasing the D_{it}. The reason the capacitance density was increased with ten cycles of TALD could not be resolved unambiguously. The specimen with twenty cycles of TALD had the lowest D_{it} but the capacitance density declined mainly due to inferior electrical characteristics of thermal ALD films. The mid-gap D_{it} lowered systematically with increasing number of thermal ALD cycles. Furthermore, the frequency dispersion in

accumulation decreased significantly with increasing thermal ALD cycles up to twenty cycles.

Hafnium zirconate (HZO), hafnium aluminate (HAO) and zirconium aluminate (ZAO) films were deposited using atomic layer deposition on silicon, indium phosphide and gallium nitride with alternative cycles of each individual binary oxide. MOSCAP devices were fabricated to study dielectric properties and semiconductor-gate oxide interfacial quality. Hafnium zirconate had the lowest leakage current, while having the lowest band gap. The leakage current is dominated by direct tunneling in hafnium zirconate, while hafnium aluminate and zirconium aluminate had significantly higher leakage current. Additionally, HZO had an ultra-low D_{it} of 2.61×10^{10} cm^{-2} eV^{-1} on silicon and 8.62×10^{11} cm^{-2} eV^{-1} on indium phosphide mainly due to the combination of low growth substrate temperature (100°C) and high post-fabrication heat treatment temperature (510°C). The hafnium zirconate gate oxide on silicon had very efficient band bending with respect to gate voltage. Furthermore, hafnium zirconate had higher frequency dispersion on indium phosphide compared to silicon. The hafnium zirconate structure had a wider band gap and larger conduction band offset but smaller valence band offset compared to pure zirconia. This was attributed to the increase in the valence band width with hafnia incorporation, which in turn reduced the hafnium zirconate's valence band

offset. The band offsets of 3.53 eV for electrons and 1.03 eV for holes were measured for $Hf_{0.25}Zr_{0.75}O_2$/InP heterojunctions.

5.2 FUTURE WORK

At the commencement of his Nobel Lecture, Herb Kroemer concluded the way semiconductor heterostructures work by saying, "the interface is the device" [107]. The importance of interfaces for solid state devices is not limited to heterostructures. Semiconductor-gate dielectric cohesion and interface quality practically dictates the transistor performance in MOSFETs [89]. Understanding the nucleation and growth and especially the first cycles of ALD growth of gate dielectrics helps with modifying the interface region and providing better performance in solid state devices. Using first principles study of organometallic precursor and semiconductor interaction and the initial stages of growth helps with better understanding of this region. The density of interfacial trap states gives a good picture on the interface quality but fabricating a MOSFET or thin film transistor and measuring the transistor performance (including carrier mobility) could be used to verify the D_{it} results we obtained from the MOSCAPs.

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