Advances on Fabrication and Application of Through Silicon Via for Radio Frequency Circuits

by

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Abstract

Through silicon via (TSV) has been considered as an astonishing milestone in the evolution of three-dimensional integrated circuit (3D IC), because of its exclusive and pivotal function of providing signal exchanging paths in the horizontal direction to stacked layers efficiently. Unfortunately, Cu (copper) electroplating, the most popular TSV metallization technique, is still not ideal; and the interfacial quality of silicon interposer, i.e. multiple layers of TSVs, is still problematic, which will not only result in device dysfunction but also prohibit its wide spread to other areas.

In this thesis, based on the comparison of advantages and disadvantages of newly emerged alternatives to Cu electroplating, an optimal mechanism which is the vacuum suction of Ag (silver)-based conductive polymer is proposed to achieve the easy, rapid, void-free and low cost TSV metallization. To better understand the vacuum suction process, a variety of vacuum conditions in terms of pressure differences (from 0 to 2 kPa) and durations (1 s, 2 s and 3 s) are tested. It is found that increasing the vacuum level is more effective than extending the vacuum time to produce a higher filling ratio. To fully fill the through vias with diameter of 100 μm and depth of 500 μm, at least 1.6 kPa and 3 s is needed. The volume resistance of fully filled TSVs is measured by running the typical two-point probe test twice and the result indicates the average resistance is lower than 25 Ω. Also, during the temperature increase from 20 °C to 120 °C, the resistance variation is less than 5 %, which implies that their thermal resistance stability is acceptable.

Moreover, through the replacement of conventional redistribution layer (RDL) formed on the chip surface with conductive polymer metallized trenches embedded in the chip body, a new silicon interposer architecture is built, whose fabrication process is simplified and interfacial connection becomes homogeneous and more dependable. More critical parameters including via dimension, conductivity and viscosity are investigated in various vacuum conditions. The filling depth measurement shows that either enlarging the via opening or lowering the conductive polymer's viscosity would be beneficial to the filling process. The resistance characterization result suggests that the C(carbon)-based conductive polymer is not suitable for the TSV metallization as the average resistance of relevant channels is higher than 20 kΩ.

Lastly, the idea that through via structures can be more efficiently metallized through the vacuum suction of conductive polymer, is applied to the development of substrate integrated waveguide (SIW). Through the proper manipulation of the vacuum condition, the metallization level (i.e. filling ratio) of the through via structure becomes rather adjustable; based on which, two prototypes of band-stop SIW filter with partial height via resonator are fabricated in a standard commercial rigid substrate (RO4003C) and a self-made flexible substrate of Polydimethylsiloxane (PDMS) respectively. For the rigid SIW filter, the measured resonant frequency and maximum reflection coefficient are 10.25 GHz and -1.6 dB, which are enough to prove the accuracy of this SIW fabrication method, considering the simulated results are 10.5 GHz and -1 dB. For the flexible SIW filter, relatively good agreements between the measurement (14.6 GHz and -2.3 dB) and the simulation (15 GHz and -1 dB) can also be obtained; in addition, only the resonant frequency is influenced by the bending, as it shifts to 14 GHz and 13 GHz when the bend radius reduces to 35 mm and 12.5 mm respectively.

Preface

This thesis is based on three published or accepted papers.

The work included in Chapter 3 has been published as Yang Qiu, Shichao Yue, Walied A. Moussa, and Pedram Mousavi "**Vacuum-assisted Through Silicon Via Filling Method with Ag-based Epoxy**", *IEEE Transactions on Components, Packaging and Manufacturing Technology*, Pages 1475-1481, Volume 6, Issue 10, 04 October 2016, DOI 10.1109/TCPMT.2016.2610321. Yang Qiu was responsible for the design, fabrication and characterization of the testing samples as well as the manuscript composition. Shichao Yue contributed to part of the design of the testing samples and the manuscript composition. Walied A. Moussa and Pedram Mousavi contributed to part of the manuscript composition. Walied A. Moussa was the corresponding author.

The work included in Chapter 4 has been published as Yang Qiu, Shichao Yue, Walied A. Moussa, and Pedram Mousavi "**Development of Embedded Redistribution Layer-Based Silicon Interposer for 3-D Integration**", *IEEE Transactions on Components, Packaging and Manufacturing Technology*, Pages 399-409, Volume 8, Issue 3, 21 February 2018, DOI 10.1109/TCPMT.2018.2794202. Yang Qiu was responsible for the design, fabrication and characterization of the testing samples as well as the manuscript composition. Shichao Yue contributed to part of the design of the testing samples and the manuscript composition. Walied A. Moussa and Pedram Mousavi contributed to part of the manuscript composition. Walied A. Moussa was the corresponding author.

The work included in Chapter 5 has been accepted as Yang Qiu, Mohammad Mahdi Honari, Shichao Yue, Teng Zhang, Walied A. Moussa, and Pedram Mousavi "**Conductive Polymer Metallized Vias: A New Approach for Substrate Integrated Waveguide Development**", *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 02 November 2018, DOI 10.1109/TCPMT.2018.2879447. Yang Qiu was responsible for the fabrication of the prototypes and the manuscript composition. Mohammad Mahdi Honari was responsible for the design and characterization of the prototypes as well as part of the manuscript composition.

Shichao Yue contributed to part of the manuscript composition. Teng Zhang contributed to part of the fabrication of the prototypes. Walied A. Moussa and Pedram Mousavi contributed to part of the manuscript composition. Yang Qiu was the corresponding author.

Dedication

To my grandpa, Hongguang Qiu.

Acknowledgements

Foremost, I can never adequately express my gratefulness to my parents for everything they have done for me. My beautiful wife, Zehui, nobody has been more important to me than you, so let me hold your hand and let's walk together till the end.

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Abbreviations and Acronyms

3D Three-Dimensional

2D Two-Dimensional

Ave Averaged

Au Gold

BEOL Before End of Line

CB Carbon Black

C_4F_8 Perfluorocyclobutane

CO_2 Carbon Dioxide

CMOS Complementary Metal Oxide Semiconductor

CMP Chemical Mechanical Polish/Planarization

CNC Computer Numerical Control

CNT Carbon Nanotube

CTE Coefficient of Thermal Expansion

Cu Copper

DI Water Deionized Water

DRAM Dynamic Random Access Memory

DRIE Deep Reactive Ion Etching

FEOL Front End of Line

FPGA Field Programmable Gate Array

HMDS Hexamethyldisilazane

IC Integrated Circuit

ITRS International Technology Roadmap for Semiconductors

IPA Isopropyl alcohol

LPCVD Low Pressure Chemical Vapor Deposition

MEMS Microelectromechanical System

MSEM Molten Solder Ejection Method

MFI Mechanically Flexible Interconnect

N_2 Nitrogen

NMES Nanoelectromechanical System

NMES Nanoelectromechanical System

PCB Printed Circuit Board

PDMS Polydimethylsiloxane

PECVD Plasma Enhanced Chemical Vapor Deposition

PMMA Polymethylmethacrylate

PPI Pixel Per Inch

PVD Physical Vapor Deposition

RDL Redistribution Layer

RT Room Temperature

RV Reflow-Vacuum

RF Radio Frequency

SAC305 Sn-96.5%, Ag-3.5%, Cu-0.5% (weight ratio)

SD Standard Deviation

SEM Scanning Electron Microscope

SF_6 Sulfur Hexafluoride

Si Silicon

SIW Substrate Integrated Waveguide

SiO_2 Silicon Oxide

Ta Tantalum

TaN Tantalum Nitride

Thr Theoretical

Ti Titanium

TiN Titanium Nitride

TiW Titanium Tungsten

TSV Through Silicon Via

UV Ultraviolet

W Tungsten

WV Wave Soldering-Vacuum

Zn Zinc

Unit

Ω Ohm

kΩ Kiloohm

cm Centimeter

mm Millimeter

µm Micrometer

nm Nanometer

N Newton

MPa Megapascal

kPa Kilopascal

mJ Millijoule

s second

min Minute

h Hour

°C Celsius

Pa·S Pascal·Second

Nomenclature

Φ_c Percolation Threshold

ε_r Permittivity

$tan\delta$ Loss Tangent

R Resistance

ρ Resistivity

L Length along the current direction

A Cross section area

V_{TSV} Voltage applied to a single TSV

I_{TSV} Current passes through a single TSV

R_{TSV} Resistance of a single TSV

R_{Total} Total resistance of two chained TSVs

$R_{TotalCu}$ Total resistance of two chained TSVs with Cu

R_{Link} Resistance of the link part between two TSVs

ρ_{Link} Resistivity of the link part between two TSVs

ρ_{TSV} Resistivity of TSV

L_{Link} Length of the link part between two TSVs

L_{TSV} Length of a single TSV

Φ_{Link} Diameter of the link part between two TSVs

Φ_{TSV} Diameter of TSV

A_{Link} Cross section area of the link part between two TSVs

A_{TSV} Cross section area of TSV

P_{dr} Driving pressure

P_{atm}, P_a Atmosphere pressure

P_{back}, P_b Pressure at the back of the testing vehicle

T_{feed} Feeding time

R_{mid} Resistance of the middle part between two channels

R_{oa} Overall resistance of two chained channels

R_{ch} Resistance of a single channel

R_{cu} Overall resistance of two chained channels with copper

R_{al} Overall resistance of two chained channels with aluminum

Chapter 1: Introduction

1.1 Problem Statement

As predicted by the international technology roadmap for semiconductors (ITRS, currently it is international technology roadmap for devices and systems, IRDS), the performance and productivity of microelectronics have been improved continuously over the last forty years, thanks to the countless advances on lithography and device technologies [1, 2]. However, after the size shrinks below the 28 nm node, the famous Moore's Law, i.e. scaling down of transistors, has almost reached the physical limit; meanwhile, the cost benefit of fabricating smaller components starts to vanish [3, 4]. To fulfil the continuous demands of better performance, smaller size and more functions, 3D integration which is capable of forming highly integrated systems by vertically stacking and connecting various components [5-7], has been developed [8-10]. Among all 3D integration techniques, TSV has been considered as the heart and the future direction [11-13], which is attributed to its vital role of constructing the communication channel between each pair of layers in the most efficient style [14]. However, some problems concerning its fabrication, connection and application are still untackled [15, 16].

Cu electroplating, the most widely adopted approach for TSV metallization, has been accused of low efficiency [17, 18], as the typical process duration is more than 2 h (the deposition of seed is taken into consideration). Moreover, when the via's aspect ratio goes higher, more time will be required and voids might appear in the via [19]. Also, additives should be added to the electrolyte to improve the plating quality. Noticeably, most commercial electrolytes contain copper sulfate, sulfuric acid, chloride ions and organic particles. Thus, special care should be taken either in or after the plating process to avoid environmental hazards.

Inside a full 3D IC stack, different layers are usually fabricated individually. One of the most vulnerable parts is the connection reliability between each pair of TSVs (i.e. silicon interposer) that are located within different two layers, as the nonuniform topography and misalignment at the contact interface is not easy to demolish, especially for the case that a number of TSVs have to

pair [20]. Furthermore, the utilization of various materials on different layers will deteriorate this situation because of the mismatch of thermal, chemical and electrical properties [21, 22].

At present, the successful adoption of TSVs in high volume manufacturing is restricted to complementary metal oxide semiconductor (CMOS) image sensors [23, 24], field programmable gate array (FPGA) [25-27], dynamic random access memory (DRAM) with wide input/output (I/O) [28-30] as well as microelectromechanical systems (MEMS) [31-33]. From the point of view of structure and fabrication, substrate integrated waveguide (SIW), one of the most popular and advantageous devices in radio frequency (RF) circuits [34, 35], actually has remarkable and striking similarities to them, since it typically contains a number of small through vias and/or slot trenches that need to be metallized in shielded dielectric substrates [36]. Although these dielectric substrates are typically made of polymer or ceramic rather than silicon, and sometimes they can be flexible, Cu electroplating is still the most popular metallization option. Thus, the fabrication process of SIW might suffer from the aforementioned disadvantages.

1.2 Objectives

Because the TSV metallization suffers from the disadvantages of Cu electroplating, the first objective is to

1) Develop a new approach for the rapid, simple and void-free TSV metallization.

A good connection between two attached layers is critical to their intercommunication, but the existing connection architecture of stacked TSVs are not reliable enough. Thus, the second objective is to

2) Develop a new connection architecture to improve the interfacial quality between two stacked TSVs for 3D integration.

The metallization of vias in SIW is also achieved through Cu electroplating, this means that the same issues including low speed, complexity and risk of environmental pollution exist. Therefore, the third objective is to

3) Apply the new TSV metallization approach to the development of SIW for RF circuits.

1.3 Methodology

To shorten the TSV metallization time and to simplify the TSV fabrication process flow, this research employs an approach where Ag-based conductive polymer (composite) is directly driven into through vias by the vacuum suction and stays inside after the curing process. To validate the filling ability of this approach, the testing sample is diced along several specific axes to entirely expose the cross section of each TSV for the measurement of the filling depth. For the validation of the filling quality, two fully filled TSVs in the testing sample are chained using the same filling material and probed twice to cost-efficiently characterize the TSV's volume resistance, thermal stability and bonding strength to Cu.

The new interposer architecture is built based on the substitution of bonding pads and traces with conductive polymer-filled trenches that are embedded in the substrate body. The design and the fabrication of all chips remain the same. Each electrical path that passes through two layers becomes naturally continuous (homogenous), which results in higher connection quality at the interface, because each pair of TSVs with the trench that is sandwiched by them are metallized simultaneously with the same material. The validation of the filling ability and quality can be conducted in the same way as described above.

For SIW, the vacuum driven conductive polymer can be used to metallize the vias in non-silicon substrates. More importantly, through the accurate control of the vacuum level and the vacuum duration, the distance that the conductive polymer travels in the via becomes adjustable. As a proof of concept, two single-layer ridge SIW filters are fabricated on a self-made flexible substrate of PDMS and a standard commercial rigid laminate respectively.

1.4 Organization

Following chapters detail the new approach for TSV metallization, the new silicon interposer architecture and the new developing process of SIW, as per the aforementioned objectives and corresponding methodology.

Chapter 2 provides the background information and relevant literature on several core aspects. In which, the typical TSV fabrication process flow, the comparison of two types of Cu

electroplating, many emerging TSV metallization approaches over the last decade, fundamental of conductive polymer, *etc.* can be found.

Chapter 3 explains the new TSV metallization methodology from all perspectives, such as the selection of a proper conductive polymer for the vacuum suction, the fabrication procedures of testing vehicle and relevant challenges, the filling depth under different vacuum conditions, the adhesion between conductive polymer and Cu.

Chapter 4 follows up the previous chapter closely, detailing the new silicon interpose structure in a similar way including its development and validation. In addition, more vacuum suction related parameters are investigated to figure out the limit of the vacuum suction process.

Chapter 5 presents an interesting and meaningful application of the conductive polymer metallized through via structures in substrate integrated waveguides (SIWs) rather than traditional MEMS devices. Two SIW filter prototypes are fabricated as a proof of concept.

Chapter 6 demonstrates the wafer level TSV metallization.

Chapter 7 summarizes this work and highlights its novelties and contributions. Also, future directions are indicated.

"Things always get worse before they get better."

-- The Dark Knight

Chapter 2: Literature Review

In this chapter, the background information is provided and the relevant literature is discussed. The typical structure with fabrication process of TSV is detailed, followed by specific information on Cu electroplating. Emerging advances on TSV metallization including new materials and related methodologies are then reviewed. Fundamentals of conductive polymer are established at last.

2.1 TSV

As an interconnection technique, 3D integration makes it possible for multiple layers of electronic devices which have been fabricated individually to be stacked together vertically at either wafer or chip level [37-41]. The most obvious feature of modern 3D integrated devices is the vertical interconnects that are formed inside the body of each layer, which is called TSV. The primary benefit that comes from this vertical structure is that the interconnection length can be efficiently reduced [42-45], compared with wire bonding, flip chip and several other techniques. Thus, continuous demands of higher density of working components with more functions, better performance with less power consumption, *etc.* in the modern IC industry can be fulfilled.

TSV can be explained simply as, a combination of drilling and filling techniques, in which vias are first opened in silicon-based substrate, then metallized with conductive materials to deliver electric current from top to bottom, and vice versa [46]. A popular classification criterion of TSV is based on at which stage it is fabricated compared with front end of line (FEOL, which is first portion of IC fabrication and generally covers up all components in terms of transistors, capacitors, resistors, *etc.* except for metal interconnect layers.) and back end of line (BEOL, which is the second portion of IC fabrication and right opposite to FEOL, i.e. all individual components get interconnected with metal interconnect layers). In which, it can be via first, via middle and via last [47]. Figure 2.1, Figure 2.2 and Figure 2.3 show these three cases.

1) Via first. TSVs are fabricated at the beginning, then FEOL is formed, the last step is BEOL. Commonly, the aspect ratio of TSVs is high (from 5 to 10) and they are more suitable for die to die integration [12].

2) Via middle. The first step is to form FEOL, after that TSVs come, lastly it is BEOL.

3) Via last. FEOL and BEOL is completed sequentially at first, TSVs are formed at the end. In this case, both high and low (from 1 to 5) aspect ratios are available. TSVs with low aspect ratio are commonly used for die to substrate integration [12].

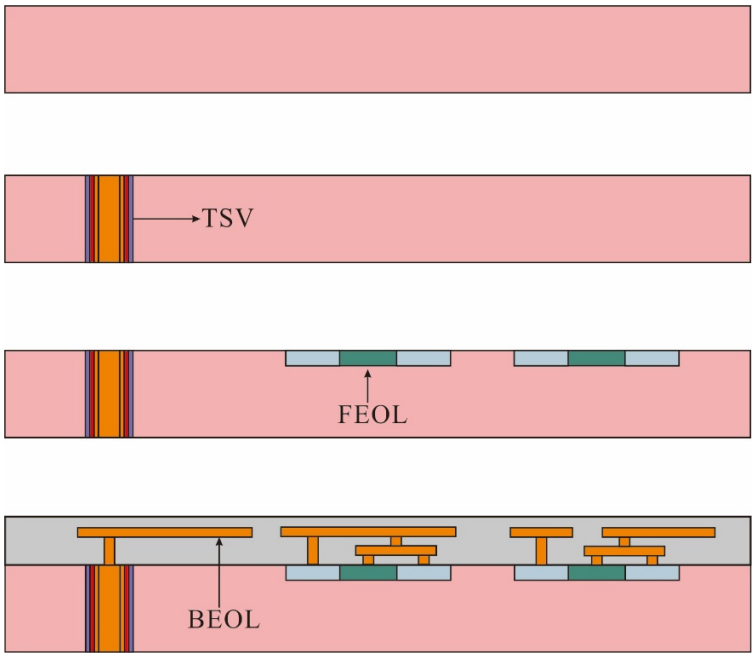

Figure 2.1 A schematic demonstration of the via first process. All vias are formed at the first stage, before FEOL and BEOL.

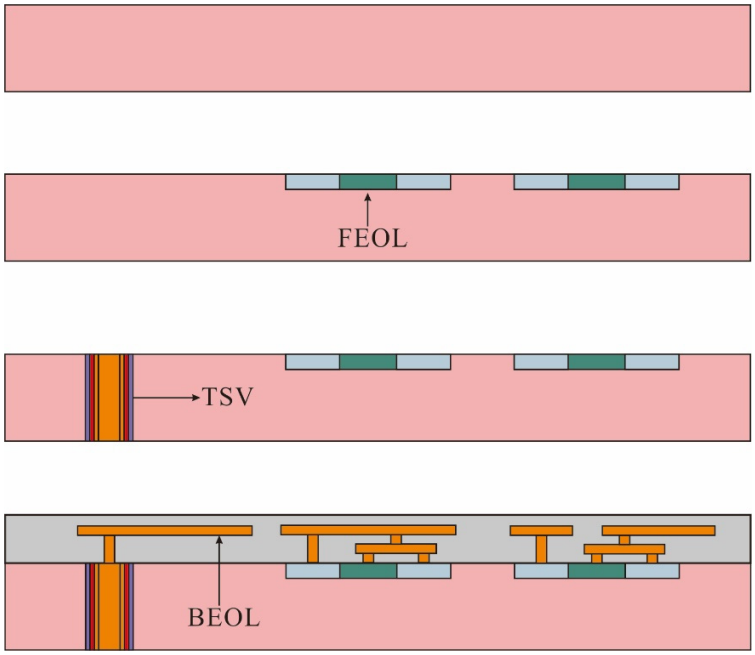

Figure 2.2 A schematic demonstration of via middle process. All vias are formed at the middle stage, after FEOL but before BEOL.

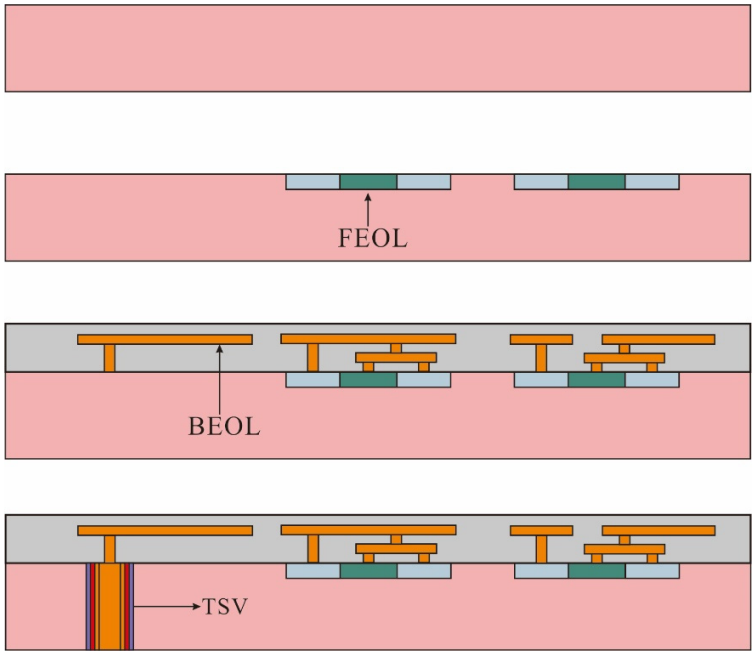

Figure 2.3 A schematic demonstration of via last process. All via are formed at the last stage, after BEOL.

Several methods have been used to open vias in the wafer, which are plasma etching [48-51], laser drilling or ablation [52-54] and electrochemical etching [55, 56], but a number of requirements should be met regardless, including good selectivity between Si and etching mask, full control of via diameter and depth, smooth sidewall (it promotes the coverage of each layer, improves the metallization quality and reduces the stress concentration during thermal dispassion) and high efficiency. The most commonly used process for via opening at present is plasma etching [57]. The via filling is more challenging than it looks in fact, as multiple layers with different functions are supposed to be formed inside. As demonstrated in Figure 2.4, TSV is typically made up of four layers, which are insulator, barrier, seed and conductor.

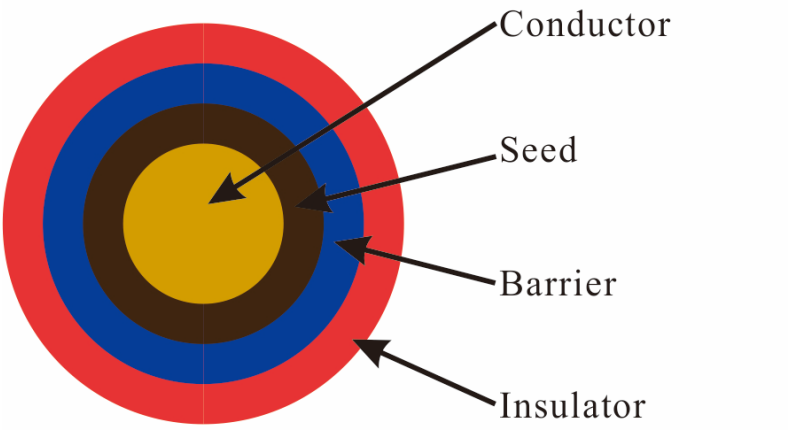

Figure 2.4 A schematic demonstration of a Cu-based TSV. Usually it is made up of four layers.

1) Insulator. The function of this layer is to prohibit the short circuit between adjacent TSVs. Depending on packaging requirements and fabrication limits, the materials with relevant methods used to achieve this goal are not the same [58]. In Table 2.1, they are listed. One of the most important factors is the processing temperature. Compared with (thermal) oxidation, low pressure chemical vapor deposition (LPCVD) and plasma enhance chemical vapor deposition (PECVD) have lower process temperature. However, some typical requirements including good sidewall coverage, low thickness variation, acceptable growing speed, *etc*. should be well fulfilled.

Table 2.1 A summary of various dielectrics that have been used as insulator.

Material	Method	Temperature (°C)	Stage	Reference
SiO_2	Oxidation	800 - 1200	Via first	[59, 60]
	LPCVD	500 - 800	Via first	[59, 61]
	PECVD	150 - 400	Via last	[59]
SiN	LPCVD	700 - 800	Via first	[61]
	PECVD	150 - 400	Via last	[59, 61]
Polymer	Spin-coating	120, 250	Via last	[62, 63]

2) Barrier. This layer is not mandatory, but as long as Cu-based material is used to metallize TSV, a layer of titanium (Ti), titanium nitride (TiN), tantalum (Ta), Titanium Tungsten Alloy (TiW) or tantalum nitride (TaN) formed by vapor deposition would be strongly recommended [64-69], as Cu particles will diffuse into Si and SiO_2 parts because of the electromigration effect, causing short circuits. The requirements for this layer are strong adhesion to Cu and insulator, good sidewall coverage, enough shield, *etc.*

3) Seed. When the wafer is thin enough for through etching, i.e. vias will be opened all the way through the wafer body, the seed layer is not required to totally cover the sidewall, as the conductor layer can grow from the bottom to the top of the via during the electroplating process [70] (this part will be explained later in Section 2.2). Thus, it can be deposited by traditional sputtering techniques [71, 72]; another way is to bond it to a carrier wafer, on which a thin metal film has been deposited already [73]. For thick wafers, the through etching is not easy or efficient to achieve, especially when vias are required to have high aspect ratio. Thus, in fact the etching operation will stop at a desired depth and result in blind vias. The excess thickness will be thinned through chemical mechanical polish/planarization (CMP) at the end. In this situation, a conformal metallic seed layer with good uniformity and enough coverage should be

deposited on the sidewall and the bottom of the vias before the electroplating process. This is one of the challenges for blind vias, since conventional thin film sputtering techniques are not ideal enough for high aspect ratio vias (because it is hard to drive Cu atoms into the bottom of the vias) [74, 75].

4) Conductor. As the major component of TSV, the main function of this layer is to provide the electrical connection to the stacked layers, which makes the vertical signal exchange possible. As an amount of electrical energy will be converted into thermal energy, and there exists a mismatch of coefficient of thermal expansion (CTE) between Si (2.6 ppm/K^{-1}) and SiO_2 (0.4 ppm/K^{-1}) [76], the basic requirements for the materials that are used to metallize TSV are low resistivity, capability of void-free filling and stability during temperature increase. Doped poly-Si, tungsten (W) and Cu are the commonly used conductive materials employed to metallize TSV; they are compared in the Table 2.2.

Table 2.2 A summary of different materials that have been used as conductor. Their selection is mainly dependent on the resistivity and the stage.

Material	**Resistivity (Ω·cm)**	**CTE (ppm/K^{-1})**	**Method**	**Stage**	**Reference**
Poly-Si	$1.8\text{-}2.0\times10^{-4}$	2.9	CVD	Via first	[76, 77]
W	4.2×10^{-6}	4.5	CVD	Via middle, Via last	[78-80]
Cu	1.8×10^{-6}	16.6	Electroplating	Via middle, Via last	[81, 82]

2.2 Cu Electroplating

The conductive material filling process is the most significant step in TSV fabrication, which a great deal of attention should be paid to, because the conductor quality will entirely determine whether TSV is able to function properly to support the communication among vertically stacked layers [83]. Although, doped poly-Si and W can be utilized to metallize TSV as stated before and

they even have their own advantages in some cases [78]; at present, the most popular material is electroplated Cu [84, 85], based on the facts below.

1) Compared with poly-Si and W, Cu has lower resistivity. From the perspective of reducing power consumption and avoiding structure failure caused by temperature increase, Cu should be preferred.

2) The Cu electroplating process is almost the same with that used for other metal interconnect fabrication [86], such as traces and pads on a printed circuit board (PCB).

After the barrier and seed deposition, the wafer will be soaked into an electroplating solution, i.e. electrolyte, which provides the source of Cu. Driven by the current, Cu ions will settle on the areas which have electrical contact with the seed through the following electrochemical reaction.

$$Cu^{2+} + 2e^{-} = Cu\ (solid) \tag{2.1}$$

A brief demonstration of the electroplating process is demonstrated in Figure 2.5. In fact, to keep the Cu ion concentration at a fixed level, new electrolyte will have to be pumped into the electroplating poor constantly; meanwhile, to remove the unwanted byproducts, used electrolytes will have to be pumped out.

From the perspective of reducing cost and uplifting yield, thick wafers usually will be partially etched. Thus, the conformal electroplating will be performed to metallize TSV, which is shown in Figure 2.6. To start with, the thick wafer is partially etched using deep reactive ion etching (DRIE). After that, the seed layer is deposited onto the sidewall and the bottom of the vias. The barrier and the insulator are not discussed here. During the electroplating process, Cu ions will accumulate on the seed layer as stated before. The blind via is going to close along its radius. Theoretically, when the thickness of Cu layer is equal to the via radius, the 100% filling ratio will be achieved. However, the practical electrical filed distribution is not homogeneous around small features; also for the solution concentration within the via, there is a local gradient along its axis direction; consequently Cu ions are more likely to settle on the neck and block the via before its whole body is fully filled, which is how the void forms. To tackle this problem, additives including suppressors (they reduce the plating speed on the top) and accelerators (increase plating speed at the bottom) are added to

the electrolyte to balance the difference in plating rates [87]. Once the via is closed, CMP technique will be applied to remove the overburden layer and thin the wafer to the desired thickness.

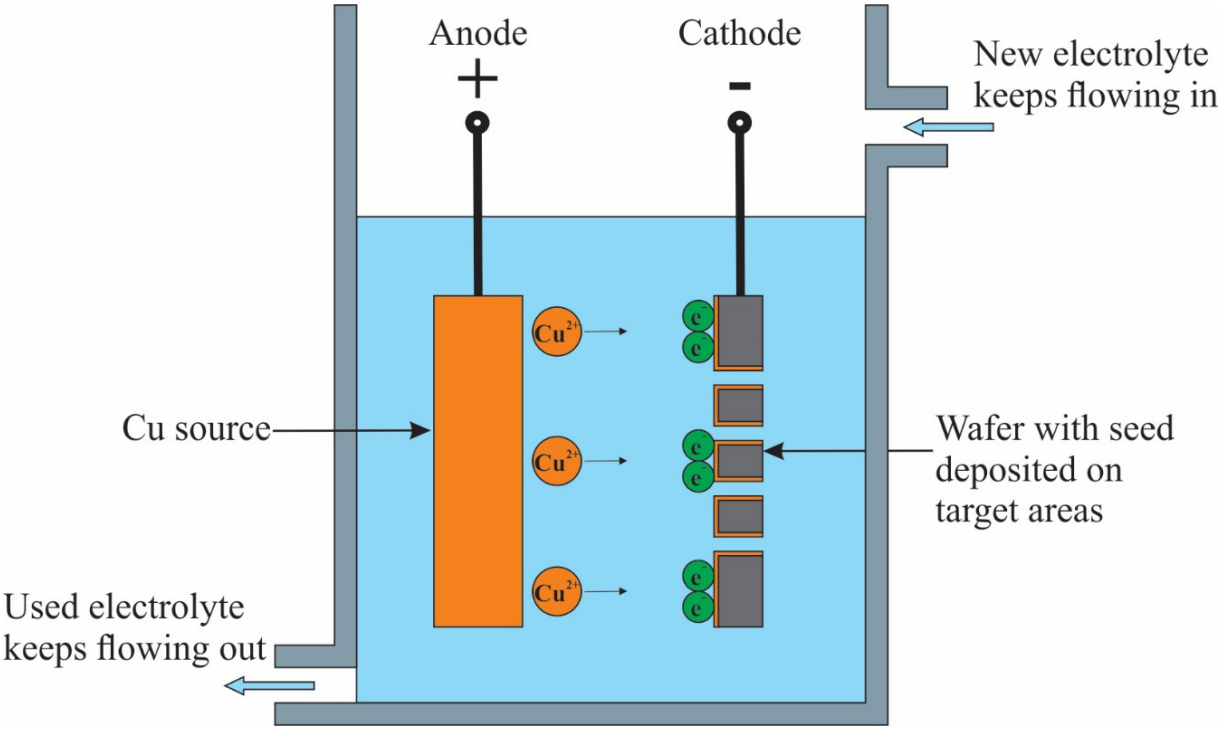

Figure 2.5 A schematic demonstration of a typical Cu electroplating setup for TSV metallization. The target wafer is connected to the anode and the Cu source is connected to the cathode. New electrolyte keeps going in and old electrolyte keeps going out.

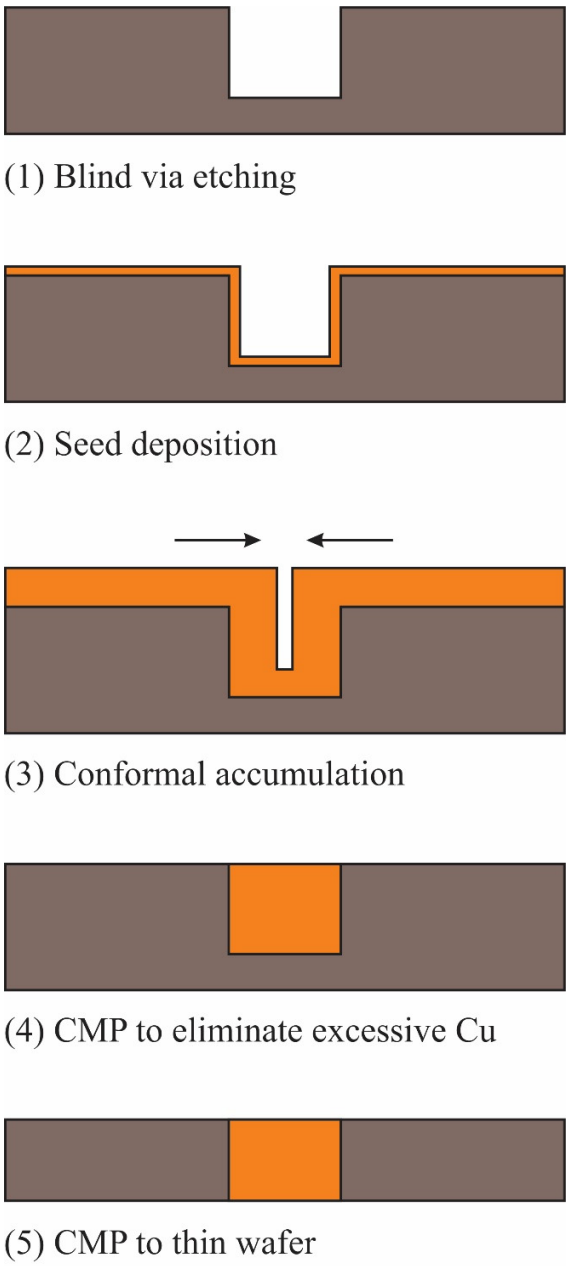

Figure 2.6 A schematic demonstration of the conformal Cu electroplating process. From which, thick wafers can be beneficial. Blind vias are filled conformally. CMP is essential to remove the excess Si and the overburden.

For thin wafers, the entire etching can be realized, which means through vias can be patterned. After the deposition of the insulator and barrier layers, there are two options to form the seed. The

first one is to employ conventional sputtering techniques; in which case, it is not mandatory to ask for the full coverage of the sidewall, because new Cu ions can use the Cu layer that are previously deposited as the new seed to accumulate on. The second option is to bond the target wafer to a carrier wafer, on which the seed has been formed already. Figure 2.7 explains this situation. First, the target wafer is thoroughly etched. Then it is bonded to the carrier wafer (a thin layer of Cu has been deposited on it prior to the bonding process). During the electroplating process, the electrochemical reaction Cu ions stack on this layer vertically instead of conformally, which means the vias will be filled from the bottom. After the 100% filling ratio is reached, the carrier wafer will be removed. CMP is still required to smooth the surface for the following integration process.

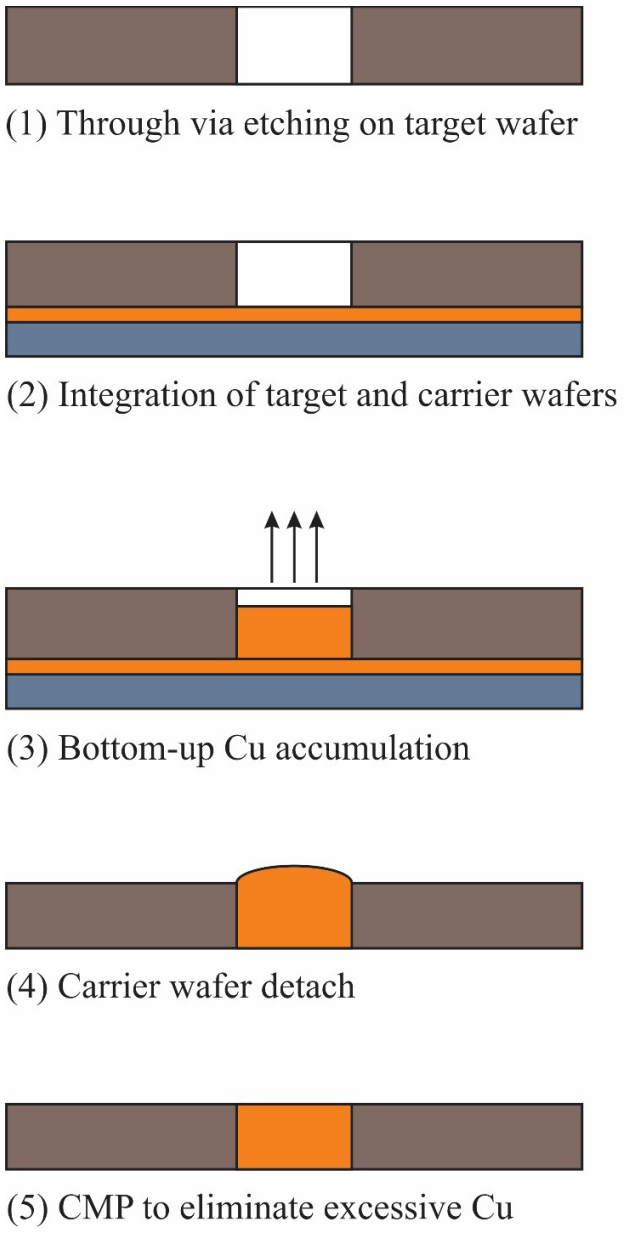

Figure 2.7 A schematic demonstration of the bottom-up Cu electroplating process. Through vias are filled vertically. CMP is essential to remove the overburden.

Compared with the conformal electroplating, the bottom-up one places few strict limits on the seed quality; apart from that, it is easier to realize the void-free filling; and the CMP time is shorter. However, its downside is fairly clear, which is the filling time is longer since the Cu ions cannot accumulate on the sidewall.

It should be pointed out that, Cu electroplating has become the most popular approach for the TSV metallization, but it still suffers from specific drawbacks.

1) All Cu that accumulates on the target region or hole in the form of thin film or bulk, comes from the transportation and deposition of Cu ions. The typical process time is more than 2 h if the deposition of the seed layer is taken into consideration. Thus, this process is time consuming (actually this is the biggest disadvantage) [17, 18], and it will become more difficult and need longer time when the aspect ratio goes higher. It has been reported that, the cost of electroplating alone is nearly one third of the total cost of TSV fabrication [88].

2) As shown in Table 2.2, the CTE of Cu is 5.7 times greater than that of Si wafer. This means their deformations will be different when they experience the same temperature increase or decrease [89, 90]. When this deformation gap exceeds the relevant limit, the dysfunction caused by the delamination or the crack will appear.

3) The good quality of the seed, in terms of small thickness variation and deep coverage on the sidewall, has a positive effect on the following deposition of Cu ions. However, an amount of efforts should be made to ensure that [75].

4) As mentioned before, due to the inevitable distortion of electrical field and the concentration gradient of Cu ions, the vias might have been closed before their body is fully filled. To solve this problem, chemical additives including suppressors (they are polymers that can block the surface of the deposited Cu and decrease the diffusion speed of Cu ions) and accelerators (they usually contain sulfide and thiol like functional groups which act a charge transfer site for the reduction of Cu^{2+} to Cu^{+}) need to be added to the electrolyte [3, 91]. However, this optimal plating environment increases the process complexity.

5) Commercial electrolytes may result in environmental issues as they commonly contain copper sulfate, sulfuric acid, chloride ions and other organic elements [92, 93].

2.3 Alternatives to Cu Electroplating

Recently to overcome the disadvantages of Cu electroplating, researchers have invented a number of alternatives to metallize TSV.

The first category is based on metallic materials which have relatively low melting point. Young-Ki Ko *et al.* proposed two ways to apply pressure difference between upper and lower side of Si wafer to drive molten tin-silver-copper (Sn-Ag-Cu) solder, SAC305 (wt %, Sn-96.5, Ag-3, Cu-0.5), into through vias with diameter of 30 μm and depth of 100μ to 200 μm. Both of methods were able to shorten the filling time into 4s [94]. Similarly, Y.K. JEE *et al.* squeezed pure zinc (Zn) and Sn-Zn alloy in molten status into blind via holes with the help of positive gas pressure. It was found that a filling pressure higher than 3 MPa during the via filling was needed to ensure no voids were trapped [95]. By employing a customized RF-MEMS switch, Shinpei Ogawa *et al.* succeeded in ejecting molten Sn-Ag solder droplets with diameter of 45 μm into via holes at the speed of 200 drops per second [96]. The cross-sectional image of TSV that was fabricated through this approach indicated the 100% filling ratio was achievable when the via diameter was 150 μm.

One drawback of these molten metal involved filling methods is, the high temperature budget should be provided to turn those filling materials into liquid state from solid state before the filling process and be maintained during the filling process, which not only complicates the filling setup but also puts other functional components which have already been built at risk. To avoid this high temperate budget, Behnam Khorramdel *et al.* investigated the feasibility of applying inkjet printer (Dimatix^{TM} DMP-2800) to filling blind vias with an Ag-based nano-particle ink (NPS-J, Harima Chemicals Group Inc.) [97]. By adjusting the parameters in terms of substrate temperature, delay and number of droplets/layers, a conductive layer with middle part thickness of 6.5 μm was on the sidewall of vias with outer diameter of 80 μm and depth of 115 μm. N. Quack *et al.* performed a similar study on using golden (Au) -based nanoparticle ink (NPG-J, Harima Chemicals Group Inc.) to fill TSVs [98]. The inkjet printing setup was mainly based on a MicroFab MJ-AT 60 μm diameter nozzle that were mounted on a custom-built inkjet printer. TSVs with radii from 25 μm to 50 μm had been successfully filled without voids.

An interesting filling method was developed by S. Schröder *et al.* based on wire bonding technique [99]. The metallization was achieved by directly inserting the bond wire into the via hole, which stemmed from the standard wire bonding process; liquid Benzocyclobutene (BCB,

Cyclotene 3022-46) was then squeezed into the hollow cavity to form the insulator. The characterization indicated TSVs that were fabricated on 625 μm thick Si wafer with aspect ratio up to 20 could be filled. Also, A. Fischer *et al.* performed a study on high aspect ratio TSV fabrication using nickel (Ni) wires controlled by magnetic force [100]. To more be specific, Ni wires placed on the wafer surface were drawn to the location of the magnet underneath and stood themselves perpendicularly and went into the target via holes according to the magnet movement. This genetic assembly method enabled the fabrication of TSVs with aspect ratio up to 24.

Described by David Benfield *et al.*, another fast approach was to squeeze conductive polymers (adhesives) through a fine-tipped syringe into the vias [101-103]. By adjusting the time and pressure on the adhesive dispenser, four commercialized conductive adhesives with varying viscosities and particle sizes and distributions had proven to be able to fill vias with different dimensions.

Compared with Cu electroplating, these alternatives described above were able to shorten the metallization time as they were supposed to be and avoid the application of harmful electrolyte. However, it is not hard to figure out that they all have drawbacks, such as unstable filling quality, complexity and high cost. Worse, the utilization of those approaches is based on the disappearance of other functional parts and the quality degrades of other fabrication procedures. For instance, the polymer-based insulator should be abandoned when the conductor is made of solder or pure Zn due to the high temperature budget. Table 2.3 and Table 2.4 summarizes their fundamentals and disadvantages.

Table 2.3 A summary alternatives to Cu electroplating.

Method	Filling Material	Via Dimension (μm)			Resistance (Ω)	Filling Duration (s)	Total Duration (s)	Disadvantage
		Depth	Radius	AR				
Reflow/ Vacuum	SAC305 solder	220	30	~ 7.3	N/A	0.4	N/A	1. The high temperature (250°C, 280°C) used to melt the filling material may damage the functional components which have been fabricated on the sample. 2. The wetting layer is needed, which takes hours to deposit. 3. The filling material can be oxidized easily since there is no protective atmosphere.
Wave/ Vacuum						0.5		
Positive gas pressure	Pure Zn / Zn-based alloy	150	50	3	N/A	N/A	N/A	1. The high temperature (430°C) used to melt the filling material may damage the functional components which have been fabricated on the sample. 2. The wetting layer is needed, which takes hours to deposit 3. The sample should be dipped in the molten bath, thus it is hard to achieve selective filling.
RF-MEMS	Sn-Ag solder	300	150	2	N/A	N/A	N/A	1. The RF switch is difficult to fabricate. 2. Each via should be located accurately before the filling process. 3. The high temperature (> 200°C) used to melt the filling material may damage the functional components which have been fabricated on the sample. 4. The wetting layer is needed, which takes hours to deposit.
Dimatix inkjet printing	Ag-based ink	115	80	~ 1.4	N/A	> 30	N/A	1. Each via should be located accurately before the filling process. 2. The solution evaporation generates large voids in the via. 3. The achievable via size is limited by the printer nozzle size. 4. The whole system is expensive.

Table 2.4 A summary of second four alternatives to Cu electroplating (continued).

Method	Filling Material	Via Dimension (μm)			Resistance (Ω)	Filling Duration (s)	Total Duration (s)	Disadvantage
		Depth	Radius	AR				
Inkjet printing at UC Berkeley	Au-based ink	100	25 to 100	4 to 1	0.05	N/A	N/A	1. Each via should be located accurately before the filling process. 2. The high temperature (250°C) used to melt the Au nano particles may damage the functional components which have been fabricated on the sample. 3. The achievable via size is limited by the printer nozzle size. 4. The whole system is expensive.
Flip Chip	Au wire	625	30	~ 20.8	0.075	N/A	N/A	1. Each via should be located accurately before the filling process. 2. The achievable via size is limited by the wire diameter. 3. The cavity between the via sidewall and the via core should be filled with BCB, which is not straightforward. 4. The whole system is expensive.
Magnet	Ni Wire	250	35	~ 7.1	0.04	66 to 81	N/A	1. The achievable via size and distribution is limited by the magnetic size. 2. The cavity between the via sidewall and the via core should be filled with BCB, which is not straightforward. 3. The whole system is expensive.
Syringe	Conductive polymer	300	100	3	N/A	N/A	N/A	1. The via diameter is greater than usual to accommodate the syringe tip. 2. Each via should be located accurately and double filled, which is not straightforward. 3. Air can be trapped within the via.
			200	1.5	0.4117			
			300	1	1.2525			
		500	100	5	2.4399			
			200	2.5	0.5191			
			300	~ 1.7	0.2088			

2.4 Conductive Polymer

Due to their high resistivity (or low conductivity) which typically ranges from 10^{10} Ω·cm to 10^{15} Ω·cm [104-117], polymers have been originally and widely adopted as the insulating component in electrical and electronic devices. However, by mixing them with conductive ingredients including carbon black, graphene, graphite, metal particles, metallic salts, *etc.*, their conduction can be changed dramatically. Based on this idea, a vast number of conductive polymers (they are composites and different from intrinsically conductive polymers such as polyaniline, polythiophene, polypyrrole, *etc.*) have been invented since 1950s [118]. Considerable attention has been paid to them, thanks to their economic importance, environmental stability [119], high processability as well as chemical resistance. Many of them with resistivity ranging from 10^{-6} Ω·cm to 10^{2} Ω·cm have been successfully commercialized and applied to various fields such as electronic devices [120], electromagnetic interference shielding [121] and sensing element [122, 123].

A widely accepted theory on conductive polymers is the percolation theory, since many of them exhibit the percolation characteristic [124-128]. An easy way to put this is while blending the insulating polymer with conductive fillers, the composite's conductivity will witness a dramatic jump (usually several orders of magnitude), facing an insulator/conductor transition at a particular point if a small number of fillers are added. The critical amount of fillers necessary to facilitate a continuous conductive network and consequently turn the insulator into the conductor is referred to the percolation threshold which is often noted as Φ_c, as illustrated in Figure 2.8. As the conductive fillers' concentration keeps increasing, conductive networks will continue growing but with a slow rate [129]. For various fillers and host polymers, good agreements have been found between experimental data and theoretical model [130-132]. The Φ_c for spherical and randomly dispersed fillers including carbon black and metallic particles ranges from 10% to 20%, which is consistent with the 16% given by the classic percolation theory [133, 134]. Although higher aspect ratio conductive particles such as carbon nanotube (CNT) or graphene nanosheet (GNS) have larger surface areas which are beneficial to the formation of conductive networks, their percolation thresholds in fact are higher. This is attributed to their agglomeration behavior during processing in host polymers [135]. It should be noted that several perquisites must be fulfilled before the percolation theory is applied.

1) The fillers should be in the shape of sphere.

2) The fillers should have approximately the same size in a dispersed phase.

3) The fillers' conductivity should be isotropic.

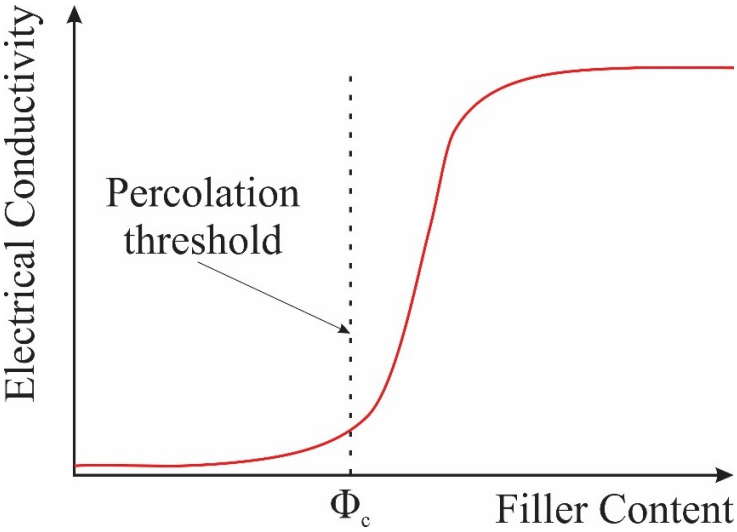

Figure 2.8 A brief description of the percolation phenomenon. The electrical conductivity can witness a dramatic uplift when the filler content reaches the percolation threshold.

Various techniques are able to manufacture the conductive polymer composites, but to be compatible with the industrial practices, the melt mixing methods including twin-screw extrusion, internal mixing and injection molding are more often chosen. During the mixing process, two aspects should be well balanced. On one hand, sufficient mixing is needed to result in a homogeneous mixture. Thus, stirring with strong power and long time is likely to happen. On the other hand, this strong power will generate shear force and lead to breakage of existing networks. It should be pointed out that the content of fillers should be kept as low as possible if it is able to produce acceptable conductivity, otherwise the mixing process will become difficult, and other properties including flexibility and transparency will start to disappear. There are several ways to decrease the percolation threshold, which are mainly based on the use of additives, the adjustment

of processing conditions and the optimization of the size, distribution and porosity of fillers [136, 137].

2.5 Conclusion

A review of the literature relevant to the main topics of this thesis is provided by this chapter. The typical structure and fabrication process flow of TSV in 3D integration is introduced at first; then the conformal and bottom-up Cu electroplating approaches for the TSV metallization are described, which is followed by the summary of their drawbacks; after that, several emerging alternatives to Cu electroplating are briefly discussed and their advantages and disadvantages are compared; in addition, some fundamental information on the manufacturing process of the conductive polymer is presented.

"Hope is what makes us strong. It is why we are here. It is what we fight with when all else is lost."

-- God of War III

Chapter 3: Conductive Polymer Metallized TSV

A methodology for rapid, void-free and low-cost TSV metallization is presented in this chapter. By comparing advantages and disadvantages of newly emerged alternatives to Cu electroplating, an optimal metallization mechanism is generated, which is the vacuum suction of the conductive polymer. Then the conductivities and applications of different commercial conductive polymers have been summarized for the selection of the candidate filling material. After a filling platform is built up to achieve the generation, maintenance and control of the pressure difference, the detailed testing vehicle microfabrication process is discussed, with relevant challenges and solutions included. Lastly, the TSV resistance is measure and the characterization of the resistance thermal stability and the bonding strength is performed.

3.1 Introduction

Since the physical limit of transistor scaling approaches and the benefits that current IC industry can gain from decreasing dimensions are confronted with a downtrend, conventional 2D integration has met the bottleneck. To fulfil the demand of higher density of working parts with more functions, better performance, less power consumption and lower cost, 3D integration comes up on stage. TSV, among all 3D integration techniques, has been regarded as the heart, due to its importance in efficiently linking vertically stacked functional layers and providing them with communication paths.

As demonstrated in Figure 3.1, TSV is usually made of insulator, barrier, seed and conductor. As the most important component, the conductor provides the electrical connections to the vertically stacked components and makes the vertical signal exchange possible. The conductive material filling process, also known as metallization, is the most significant part in TSV fabrication, because this process exactly determines the conductor's quality and defines whether TSV can support signal exchanges between two functional layers.

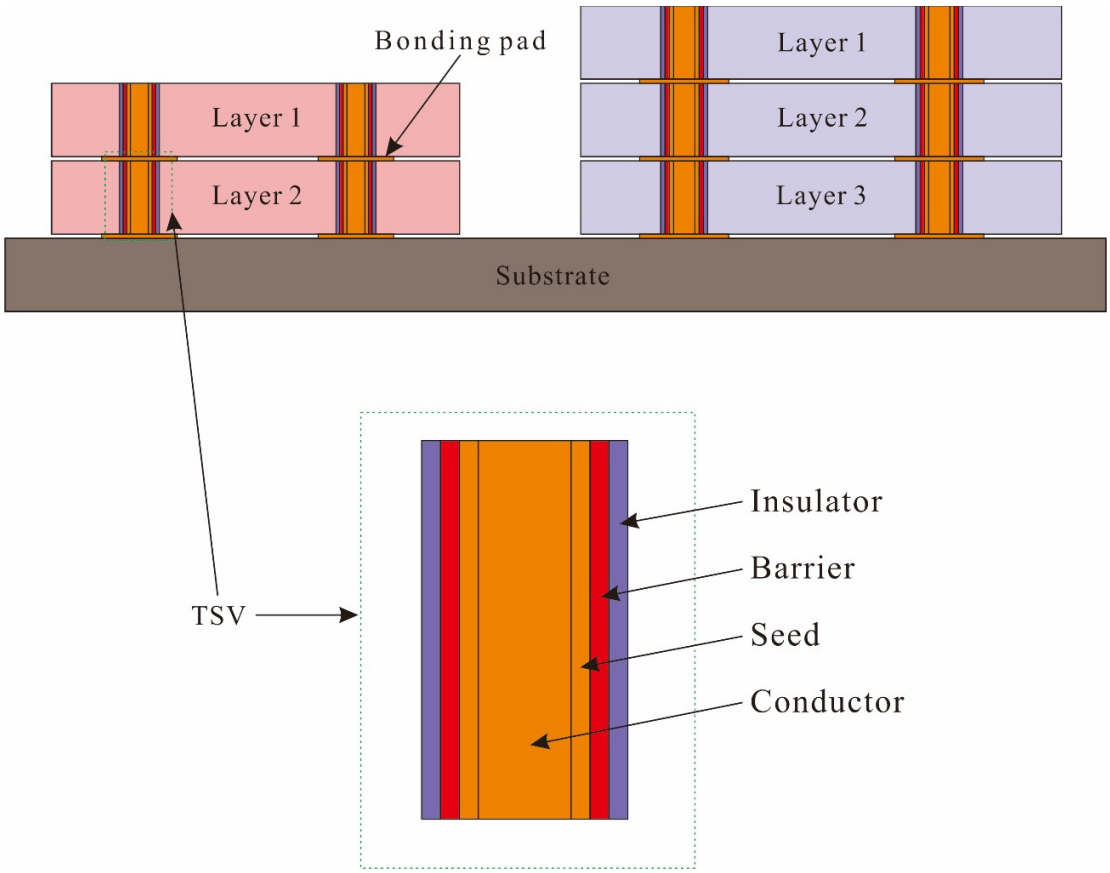

Figure 3.1 A schematic demonstration of how to use TSVs to achieve the vertical connection among stacked layers.

3.2 TSV Metallization

3.2.1 TSV Metallization Methodology Selection

As has been detailed in Chapter 2, in order to accelerate the metallization which is the most important and costly step during TSV fabrication (because it has the longest process duration and the cost of it accounts for nearly one third of the total cost of the TSV fabrication) [138], a great deal of effort has been taken to develop new approaches. Unfortunately, their drawbacks and incompatibility with other fabrication techniques cannot be ignored. Based on the filling mechanism and material, they are summarized as follows.

1) Pressure difference + Solder.

For solder, pure metal and alloy, the biggest drawback is a high temperature budget (higher than 200 °C) should be provided to melt them before they are sucked (or squeezed) into the vias by a negative (or positive) pressure difference. It should be pointed out that, a wetting layer should be formed on sidewall and bottom to enhance the adhesion between these metallic materials and Si.

2) Inkjet printer + Metallic ink.

Each via should be aligned with the printer nozzle accurately before the filling process; during each inkjetting operation, only one via can be proceeded. Thus, these methods in fact are not efficient enough and merely suitable for the chip level filling. Besides, cavities may occur in the via due to the solution evaporation.

3) Flip chip or Magnet + Metallic wire.

Clearly, by directly inserting metallic wires, vias with extremely high aspect ratio (up to 20) can be metallized in a short time. However, a proper gap between the via sidewall and the wire should be maintained to ensure the wire can be inserted smoothly. The same with inkjet printing, every via has to be located and filled separately, which indicates low efficiency and incompatibility with the wafer level filling.

4) Syringe + Conductive polymer.

Similarly, it has the low efficiency issue, because each via should be located separately and filled manually from both sides. Then, the achievable minimum via diameter (or the highest aspect ratio) is determined by the syringe tip size.

Compared with the pressure difference, the expense on inkjet printer, flip chip or magnet is higher, as these facilities are not easy to build. The application of syringe is capable of releasing the financial burden; but the sacrifice of efficiency cannot be ignored. From the perspective of protecting existing components, metallic inks or conductive polymers should be preferred, as the thermal issues generated in the high temperature melting process can be avoided. Enough solution should be added to the printing ink to lower the viscosity, which is beneficial to the printing

performance. But at this point, there is no efficient or reliable cure to eliminate the cavities related to solution evaporation in the via. Hence, it can be found that, the combination of pressure difference and conductive polymer would be more suitable for the purpose of fast metallization.

3.2.2 Vacuum Suction Platform Buildup

As illustrated in Figure 3.2(a), a customized suction head is built for the vacuum suction of the conductive polymer. A square hole with side length of 10 cm, i.e. vacuum chamber, is opened on the top. After inserted into the suction chamber, the testing vehicle would contact an O-ring which has been placed at the bottom to remove any pressure leakages. Before each suction operation, enough conductive polymers should be poured onto the top, covering the via array (the design of the testing vehicle will be discussed in Section 3.2.4). The suction head is connected to a multi-function fluid dispenser (Nordson EFD Ultimus™, Figure 3.2(b)) which is used to generate a reduced pressure on the backside (P_{back}) and control its duration. Right attached to the dispenser outlet is two air suction filters (SMC®) which are supposed to absorb the metallization material (if there is any). Because the topside pressure stabilizes at the atmospheric pressure (P_{atm}), conductive polymers will be sucked into vias by the pressure difference (P_{dr}) which can be defined as

$$P_{dr}=P_{atm}-P_{back}. \tag{3.1}$$

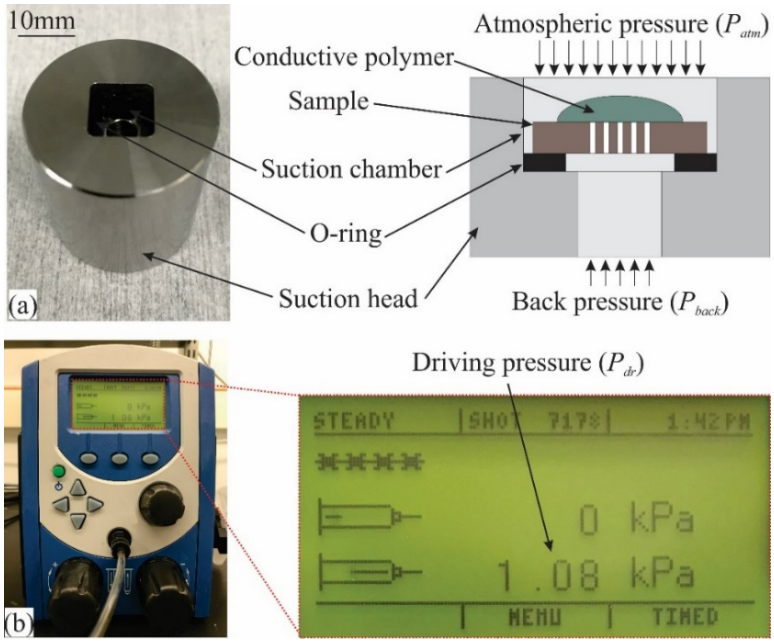

Figure 3.2 The vacuum filling platform. (a) The detail of the suction head. The pressure difference between its top and bottom drives the conductive polymer into the via. (b) The precision fluid dispenser. The driving pressure can be controlled precisely.

3.2.3 Conductive Polymer Selection

Since the invention in 1950s [118], conductive polymers (composites) have attracted considerable attention over the last decades due to their economic importance, ease of manufacturing, environmental stability [119], high processability as well as chemical resistance. Merely from the point of view of synthesis, even though sometimes chemical reactions may be involved [139], the majority of them are obtained by physically blending an insulating polymer host with conductive fillers including carbon nanotube (CNT), carbon black (CB), graphene, Ag particle and metal-based salt, which is similar to the silicon doping process in semi-conductor industry. With resistivity ranging from 10^{-6} to 10^{2} Ω·cm, some of them have been successfully commercialized and applied to various fields such as electronic devices [120], electromagnetic interference shielding and sensing elements [121-123]. They have been summarized and displayed in Figure 3.3. It is not difficult to see that compared with the C-based conductive polymers, the Ag-based ones generally have lower resistance, despite the fact that simply changing the physical shape of the fillers can result in variations in their conductivities.

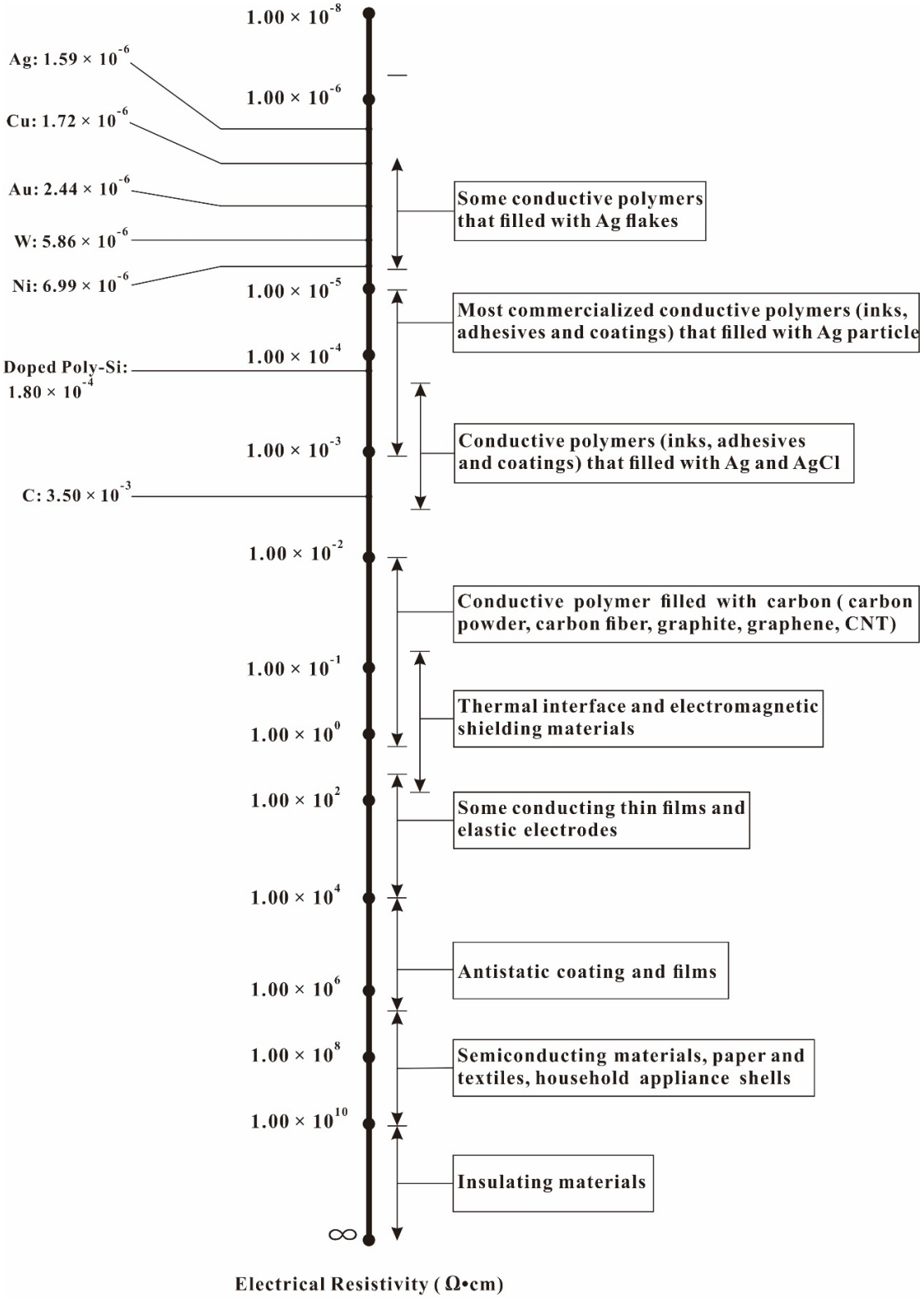

Figure 3.3 A summary of the electrical conductivity and typical application of commercial conductive polymers.

An Ag-based polymer, whose filler is Ag spheres and host material is epoxy, is selected as the metallization material. In Table 3.1, some of its parameters have been specified by the manufacturer. The selection is made based on the following aspects.

1) Price.

The prices of different conductive polymers can vary. A higher price usually means a higher conductivity. Based on our budget, an acceptable price range is lower than \$5/g. This aspect is the most important, affecting 50% of our decision-making process.

2) Conductivity (or resistivity).

The role of TSVs is to provide vertically electrical paths as signal exchanging channels to staked layers. To lower the power consumption and to reduce the heat, a low resistivity should be preferred. Thus, as discussed above, Ag-based conductive polymers are more suitable for the TSV metallization. A suitable resistivity should be between 1×10^{-3} to 1×10^{-5} Ω·cm, as this range covers most Ag-based conductive polymers. This aspect affects 30% of our decision-making process.

3) Viscosity.

Similarly, the viscosities of different conductive polymers can vary. When the other two conditions can be fulfilled, the viscosity should be as low as possible (but there is no specific requirement, an acceptable range is lower than 300 Pa·s), to make it easy to suck the conductive polymer into the vias. This aspect affects 20% of our decision-making process.

It is worth noting that the resistivity can be expressed as sheet resistivity and volume resistivity according to the corresponding characterization method. Typically, the default sheet thickness is 1 mil which is equal to 25 μm. Their relationship can be described as

$$\textit{Sheet resistivity} = \textit{Volume resistivity} / \textit{Film thickness} \tag{3.2}$$

Table 3.1 A summary of manufacturer specified parameters of 1210 Ag-based epoxy.

Product Name	Viscosity	Sheet Resistivity	Price
1210 Ag epoxy	3×10^6 (cps)	Less than 100 (mΩ/square)	$2/g

3.2.4 Testing Vehicle Fabrication

To fabricate the testing vehicles, 4-inch, 525 ± 20 μm thick, single side polished prime Si wafers (orientation <100>, p type, resistivity of 10 to 20 Ω·cm) are employed due to the following reasons.

1) All microfabrication steps are undertaken in the nanoFAB at the University of Alberta. Most facilities are suitable for 4-inch and 6-inch wafers. In order to reduce the risk of wafer damage during manual handling, the smaller diameter is preferred.

2) As mentioned in Chapter 2, the massive production in IC industry tends to embrace thin wafers (usually less than 500 μm) to shorten the etching time, to reduce the total fabrication cost and to enhance the etching quality; but here thick wafers are used to gain high aspect ratio TSVs to figure out the limit of this filling methodology.

3) The wafer etching platform (PlasmaPro 100 Estrelas, Oxford Instruments) has been designed to ensure a wide range of applications in MEMS, from smooth sidewall process to high etch cavity etches and high aspect ratio processes to tapered via etches, which indicates no backside etching is needed, hence the single side polish is enough.

4) There are no specific requirements on orientation, dopant and resistivity. Thus, any wafers meet the above three requirements can be the candidate.

A simple demonstration of the testing vehicle fabrication process flow can be obtained from Figure 3.4. However, the practical fabrication involves many steps and sub-steps which are important to the final fabrication result. The following part is trying to describe all details including all steps and considerations behind them.

1) The wafer needs to be fully cleaned at first by soaking them in the Piranha solution for 15 mins. The Piranha solution is a mixture of sulfuric acid (H_2SO_4, concentration is higher than 98%) and hydrogen peroxide (H_2O_2, concentration is 50%) with volume ratio of 3:1. The organic and metal contaminations on the wafer surface will be removed and it becomes hydrophilic. Then the hexamethyldisilazane (HMDS) treatment is performed to further improve the photoresist adhesion.

2) SiO_2 is typically used as the etching mask. According to the etching selectivity between Si and SiO_2, its minimum thickness that is able to stand the through etching is about 1 μm which may take 6 h to 8 h to grow (at 1000 °C) through wet oxidation (based on our trial experiments and data sheet that is provided by the nanoFab staff). By adding a layer of photoresist on top of it can be an efficient way to reduce its thickness, but the downside is the whole process becomes more complicated as SiO_2 should be grown and patterned at first. Instead, a thick layer of photoresist alone is used. The tradeoff is this thickness may cause uniformity issues. Thus, several precautions should be taken.

The positive-tone photoresist AZP4620 is spin-coated on the polished side with spinning speed of 500 revolutions per minute (rpm) for 10 s and 2000 rpm for 25 s (these settings are based on our trials experiments and the nanoFab staff's experience). The first spinning setup is mainly used to distribute the photoresist over the surface; with a stronger centrifugal force that is provided by the second spinning setup, the excessive photoresist will spin off the edges until the desired thickness 12.5 μm is achieved. Afterwards, a two-stage soft baking is performed. First, the wafer will be baked at 100 °C for 90 s in a nitrogen (N_2) environment; second, N_2 is removed and the time is reduced to 60 s. Lastly, the wafer needs to be stored in a dark box (this can avoid ultraviolet (UV) light) at room temperature for 24 h.

3) The etching windows are first opened by the optical lithography with an exposure of 730 mJ. Then, the exposed wafer will be soaked in the developer solution (diluted AZ400K) with gentle shaking for 2 mins until all designed features can be witnessed. The theoretical exposure time is 12 s based on the exposure power of the mask aligner. However, in practice it needs to be extend to 13 s considering the UV light leakage

cannot be avoided. Figure 3.5 presents several features after the developing process under different exposures. Of difficulty is to recognize their shapes because there is no clear or sharp boundary between the exposed and unexposed areas; instead, whatever can be seen is blurry and distorted, especially for round corners.

After the correct exposure and development, both sides of the wafer need to be rinsed with DI wafer for three times to remove any residue generated in the developing process. It is essential to inspect all features under a microscope to make sure the good lithograph quality is received. The developing time might have to be extended lightly if a number of wafers have been developed due to the consumption of functional particles in the developer.

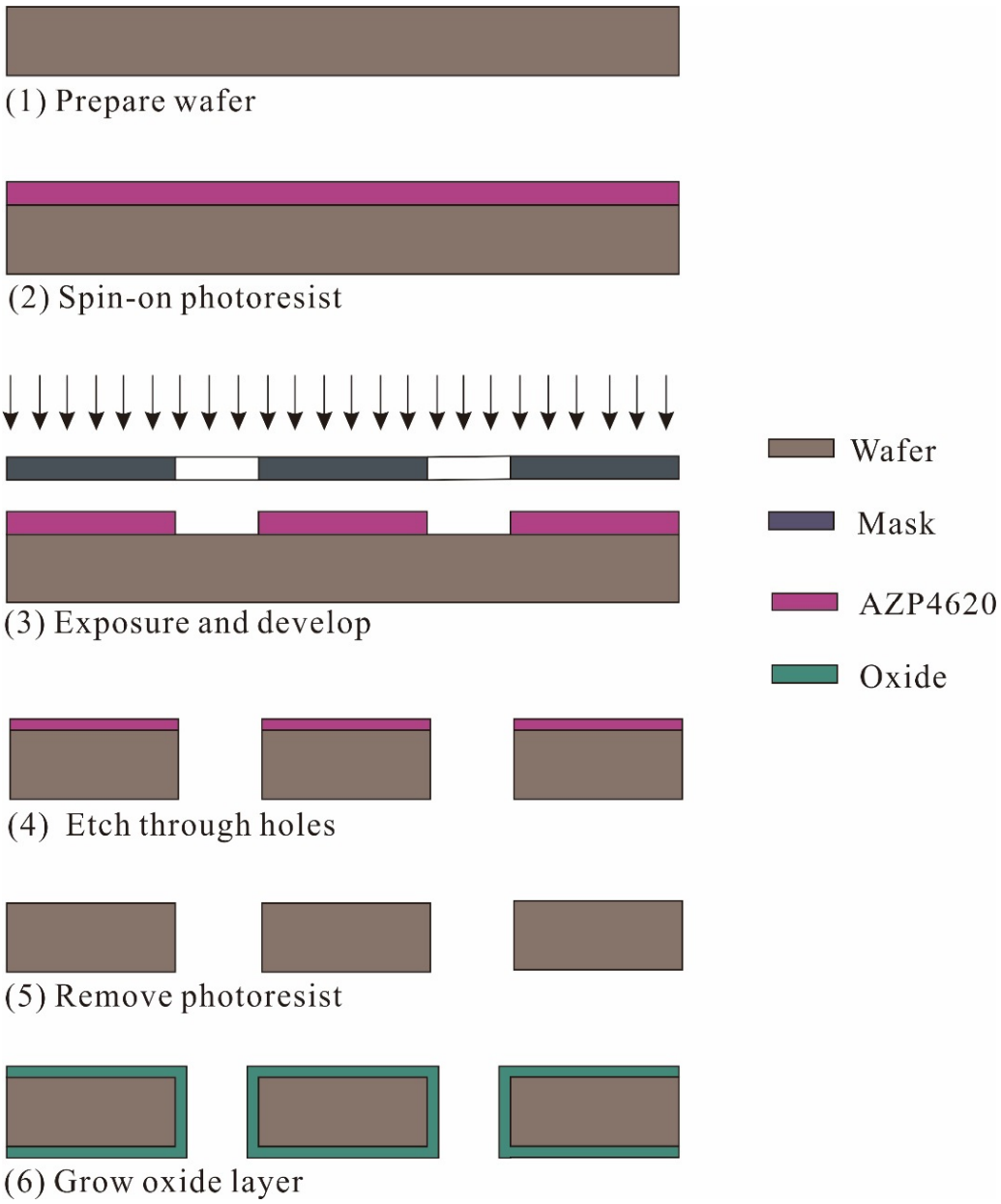

Figure 3.4 A brief description of the fabrication process of the testing vehicle. The positive-tone photoresist, AZP4620 with thickness of 12.5 μm is used as the etching mask.

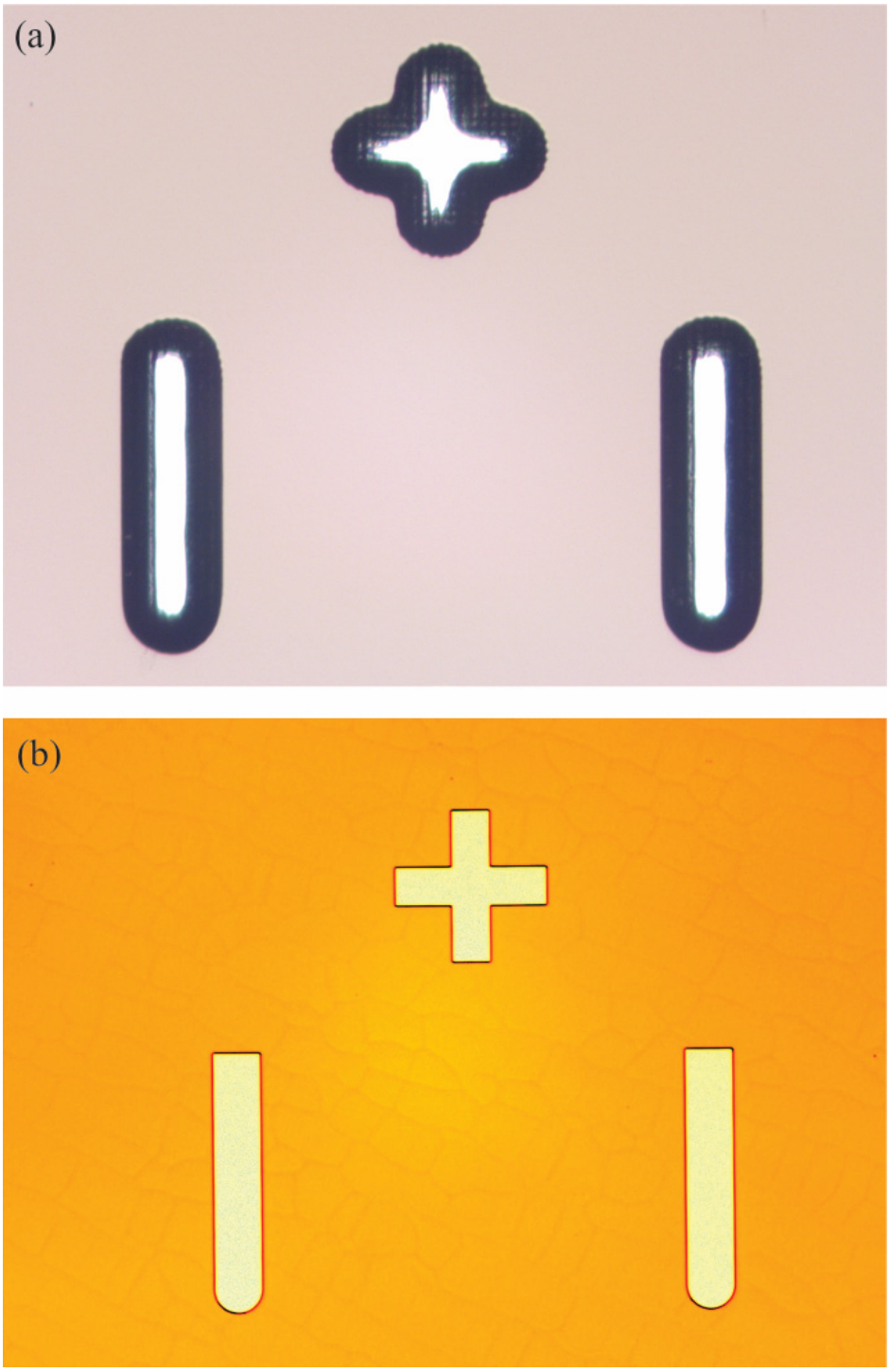

Figure 3.5 A comparison of several features after the developing process under different exposure conditions. (a) The exposure time is not enough. Features' outline is not sharp or clear. (b) The correct exposure is applied. Features' boundary is clear and there are not blurry regions.

4) Since the thick wafer is used, it is well-advised to utilize the deep reactive ion etching (DRIE) to produce high aspect ratio vias. The target water needs to be bonded to a carrier wafer using crystal bond to make sure the particle bombardment will not cause any break. The through vias in 500 μm wafer are accomplished by 750 cycles of BOSCH process. In each cycle, the first phase is sulfur hexafluoride (SF_6) chemically "attacking" the wafer from a vertical direction, resulting in a standard isotropic etching; the second phase is octafluorocyclobutane (C_4F_8) source gas generating an inert passivation layer on the sidewall and bottom of all vias, which is only able to protect the whole wafer from upcoming chemical reactions but not ion (physical) bombardments. As a consequence of this two-phase process, the sidewall becomes undulating with an amplitude of about 100 nm to 500 nm. In this case, such surface roughness can be ignored as the via diameter is 100 μm. To achieve the separation of the target wafer and the carrier wafer, they will be soaked in hot water (80 °C) for 10 mins, then the target wafer will be transferred into a photoresist stripper to remove the residual photoresist.

5) A thin SiO_2 layer is grown on the surface through wet thermal oxidation to isolate all vias and the wafer surface. First, the wafer is carefully placed into a furnace and heated up to 1000 °C with water vapor (95 °C) carried by N_2 flow which is set at 6 L/min; then both heating and N_2 flow is kept for 90 mins. The thickness of the SiO_2 generated after this process is about 500 nm.

Figure 3.6 provides a close look at the wafer after the DRIE process. Aside from designed vias, some relatively larger holes are also spreading over the wafer randomly. The reason for these defects is that small particles and air bubbles have been trapped underneath the photoresist in the spin-coating process. Of less risk is the chip level application of vacuum pressure as explained before, the wafers will be subsequently diced into individual specimens after all vias are successfully formed and isolated. Furthermore, it is easier to perform the following measurements. In the dicing process, a high speed rotary diamond blade, lubricated and cooled by a water jet, is used to dice the wafer into smaller sections.

Figure 3.6 A close look at vias formed on a wafer after DRIE. Apart from desired vias, defects (bigger holes close to the edge) can be found too.

Figure 3.7, Figure 3.8 and Figure 3.9 present the detail of the testing vehicle. After the dicing, all specimens will have a square outline with side length of 10 mm to fit into the suction chamber. On each specimen, 25 vias are located in the central region, forming a 5 by 5 array. All vias have the same diameter of 100 μm, this means their aspect ratio is fixed at 5. The distance between two adjacent vias is set to 500 μm.

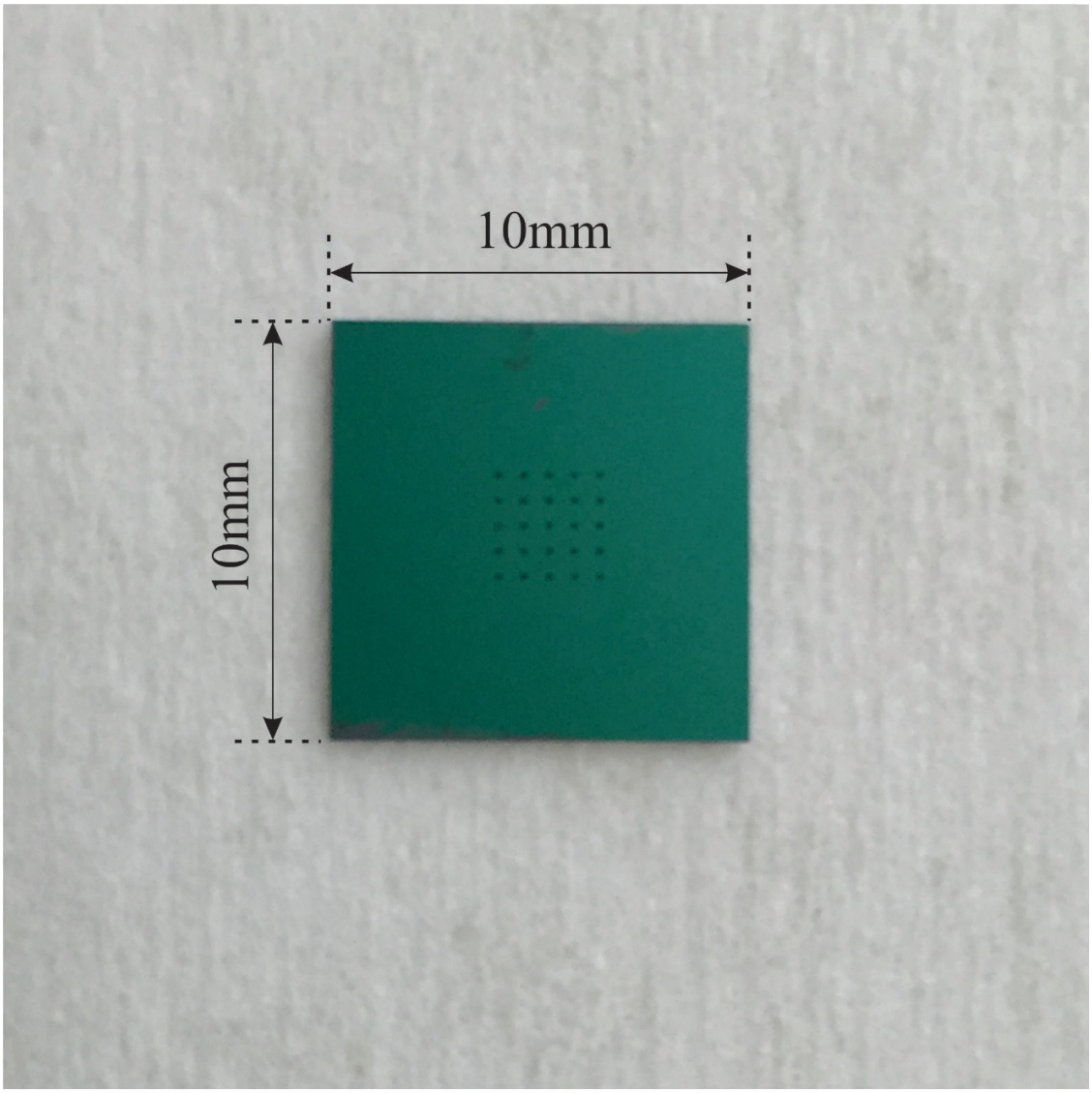

Figure 3.7 The testing vehicle. All testing vehicles are in a square shape with side length of 10 mm. The green color indicates the existence of SiO_2.

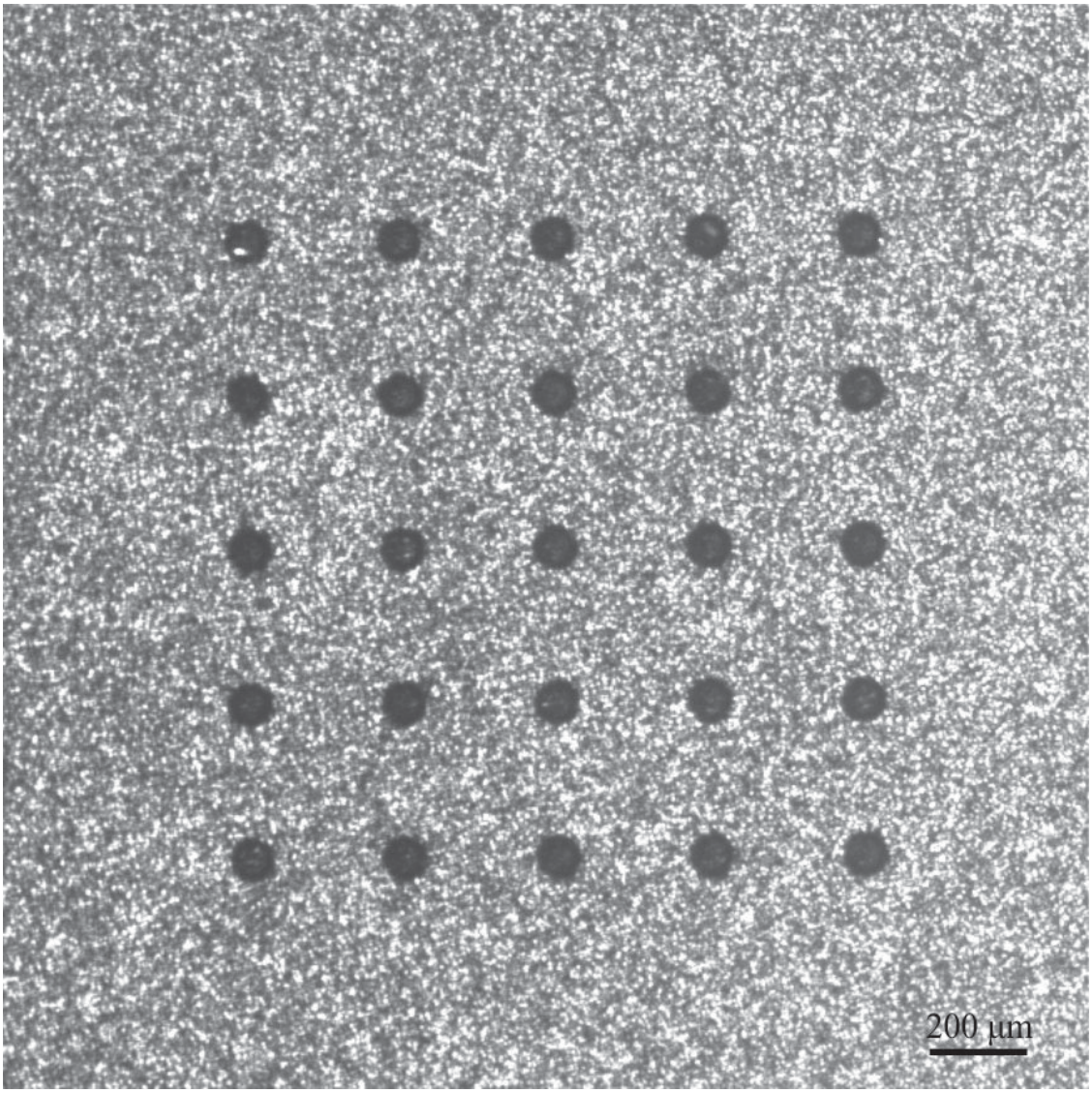

Figure 3.8 A close look at the 5 by 5 TSV array located in the central region under a microscope.

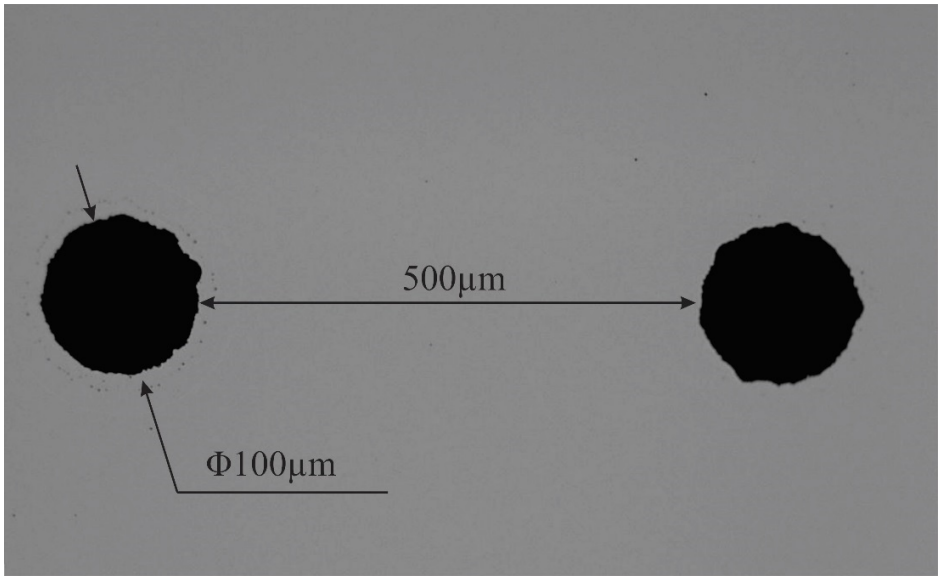

Figure 3.9 A close look at two adjacent vias in the via array. The via diameter is 100 μm and the pitch is 500 μm.

3.2.5 TSV Metallization

An action can be taken to avoid the testing vehicle damage is to lower the pressure difference and correspondingly extending its duration in a reasonable range. In this part, a set of pressure differences that range from 0.2 kPa to 2 kPa and varying feeding times (T_{feed}) including 1 s, 2 s, and 3 s are examined.

First of all, the testing vehicle is cleaned by rinsing its both sides with acetone, isopropyl alcohol (IPA) and DI water once sequentially. A syringe is then used to squeeze enough conductive epoxy onto the polished side, covering the via array. As long as it is inserted to the suction chamber, the vacuum suction and the time countdown would begin. When all combinations are finished, all testing vehicles will be stored in an environment chamber (Figure 3.10) full of N_2 gas and heated at 100 °C for 1 h. During this period, the solution contained in the conductive epoxy will evaporate, this means the volume shrinkage will occur. Thus, it is necessary to maintain enough material on the top to make sure no cavity can form. Once the curing process is completed, the overburden layer on the top is removed by scratching the surface with a shape blade. Also, any excess materials appear on the other side (if there is any) should be removed. A DI water rinsing step is performed

to remove the debris. To realize the 100% polymerization, all testing vehicles will be put back to the environment chamber and cured at the same temperature for another 2 h. In this period, the volume shrinkage continues growing but with a much lower speed. The data sheet that we received from the manufacturer indicates that there is no volume shrinkage after the curing process. But based on our observation, in the first curing process (1 h), the volume shrinkage is between 5% and 10%; in the second curing process (2 h), the volume shrinkage is between 0 and 2%. We ignore the volume shrinkage that appears in the second curing process.

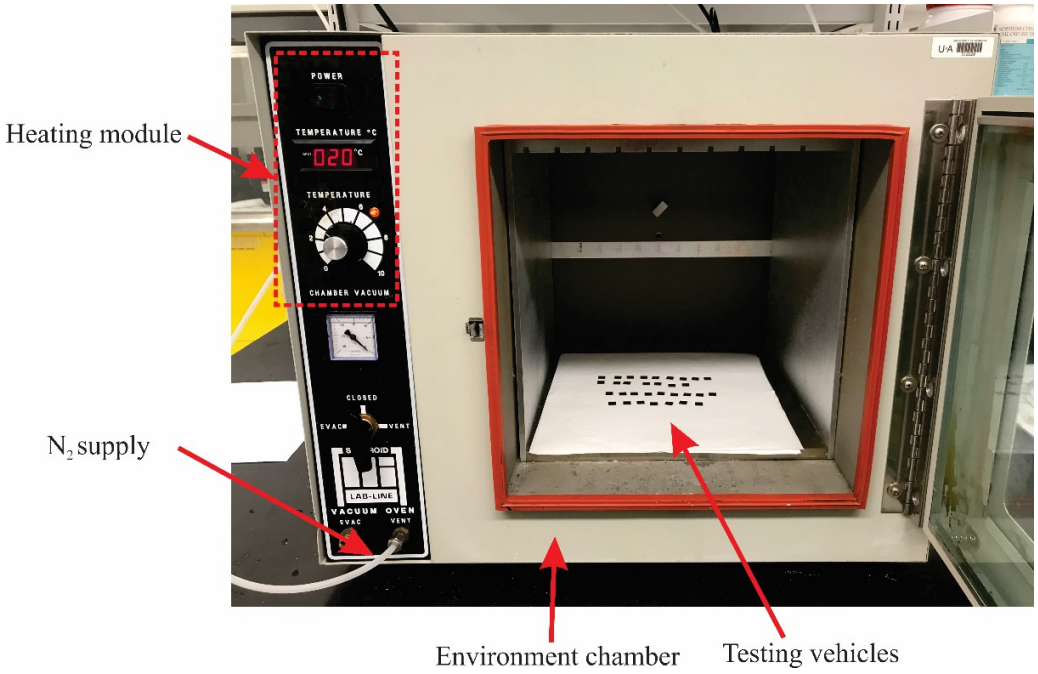

Figure 3.10 The environment chamber used to cure testing vehicles. N_2 is used to avoid the oxidation of the conductive polymer.

3.3 Characterization

3.3.1 Filling Depth

Considering random errors may exist, the suction operation is repeated on five testing vehicles for each combination of pressure difference and duration, and their results will be averaged for the analysis and discussion. After the entire filling process is completed as detailed before, all testing

vehicles are diced into pieces along any axis formed by any five vias in the same row or column to exposure their cross sections using a precision silicon dicing saw; then their filling depth can be measured under the microscope. Figure 3.11 describes how the dicing should be performed for a better observation. Given the fact that the cut width (double dash line in red) is around 45 μm according to the information provided by the nanoFab staff, the practical cut trajectory is shifted from the central line to make sure at least half of the via can remain on the testing vehicle. A sample is provided in Figure 3.12. Each golden shinny dot represents a filled via. The dicing operation has demolished approximately half of it.

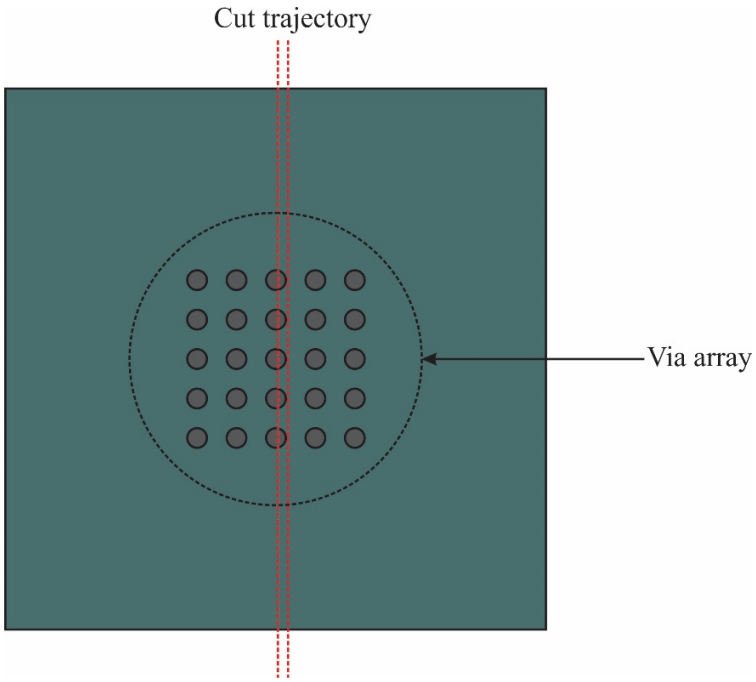

Figure 3.11 A schematic demonstration of the dicing stratgery. The cut with which is around 50 μm should be taken into consideration, thus the cut path is shifted.

The filling result is summarized in Figure 3.13. Three colors including blue, red and green stand for different durations in terms of 1 s, 2 s and 3 s respectively. Generally, either increasing the pressure difference or extending the duration is able to allow for a higher filling depth. When

the pressure difference approaches 1.6 kPa and lasts for 3 s, the 100% filling ratio will almost appear. As long as it increases to 1.8 kPa or higher, only 1 s will be enough to fully fill the vias.

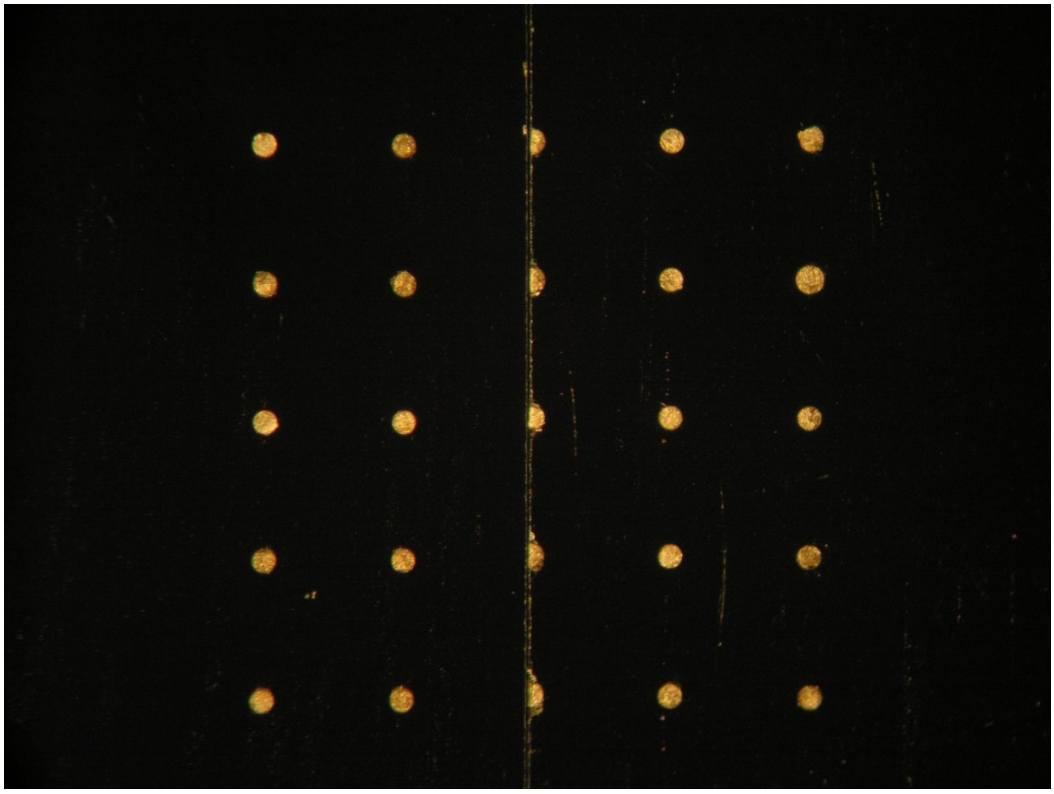

Figure 3.12 A close look at diced a testing vehicle. The cut almost eliminates half of a via.

It is not hard to witness that the pressure difference is more efficient to boost the filling depth, since the results under the same pressure difference but after different durations are not that distinguishable. Apart from that, a longer duration in some cases will not necessarily result in a greater filling depth. An explanation is the errors in pumping and timing systems of this fluid dispenser. Another one might come from the Ag-based epoxy itself. As have been discussed in Chapter 2, the conductive polymer composites are typically stemmed from the physical mixing of conductive fillers and host polymers; it is not possible to ensure each tiny part (such as per 0.01 g) of the final mixture contains the same number of conductive fillers or host polymers. Worse, the nonuniformity becomes more noticeable when the target area is in the order of μm or nm. In this

case, if the composite that is filled into the via contains more epoxy (which is the fundamental cause of volume shrinkage after the curing process), it will travel a longer distance toward the bottom after a longer duration is offered at the beginning; but after the curing process, more volume shrinkages might occur to cancel this increase. The example provided in Figure 3.14 can explain this phenomenon. The left via is filled under the pressure difference of 1.6 kPa for 3 s. Because its sidewall from Level A to Level C is covered by the residue, it is reasonable to conclude that the filling material has been successfully driven to Level C once, even though the final filling ratio ends up at Level A. For the right via, the same pressure difference is maintained for only 1 s, but it still has a higher filling ratio.

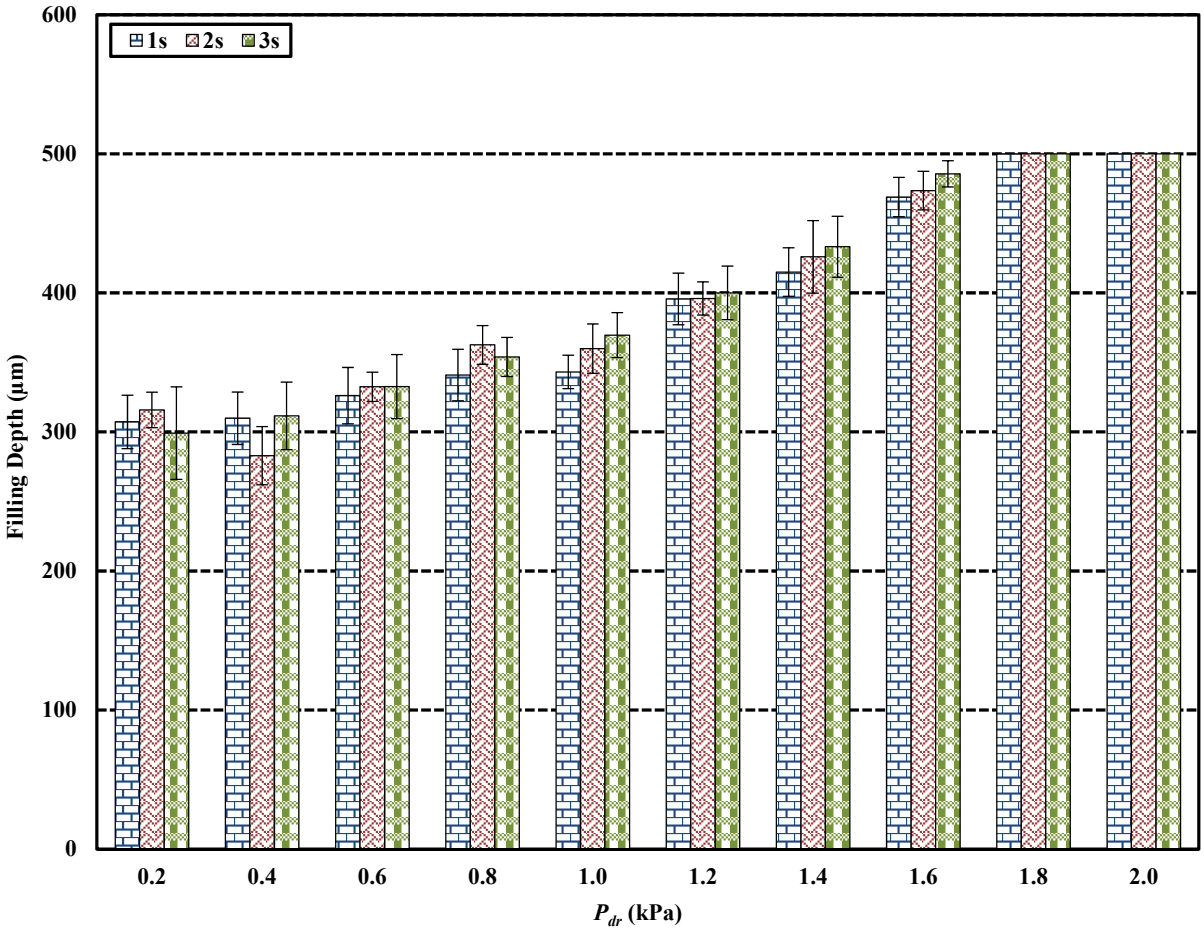

Figure 3.13 A summary of filling depths under different combinations of pressure difference and duration.

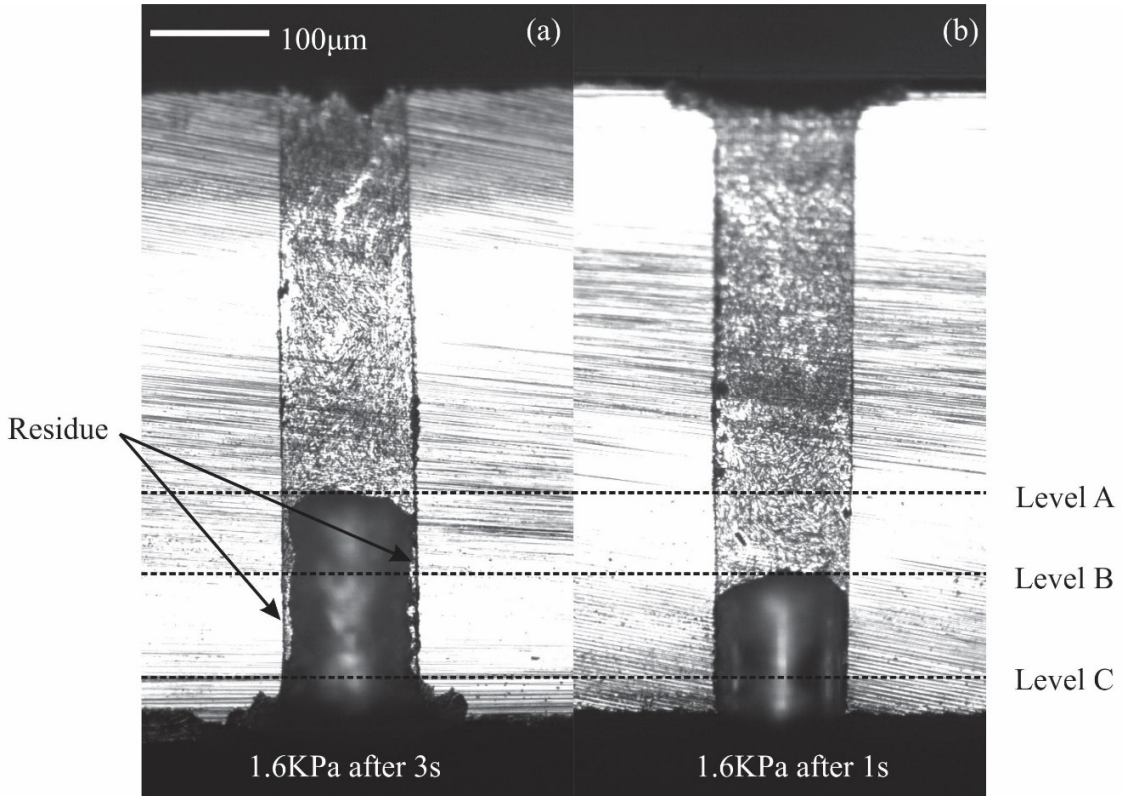

Figure 3.14 A cross section view of two vias filled under the same pressure difference but different lasting durations. (a) The pressure difference lasts for 3 s. (b) The vacuum pressure lasts for 1 s.

3.3.2 Resistance

With respect to the TSV resistance measurement, usually it can be performed in two ways, both of which employ the 4-point probe concept to eliminate the contact resistance to obtain more accurate result. As given by Figure 3.15, the first one is to probe the topside and backside simultaneously using two pairs of probes, one pair is for the voltage V_{TSV} and the other is for the current I_{TSV}, then its resistance R_{TSV} can be calculated using

$$R_{TSV} = V_{TSV} / I_{TSV} \tag{3.3}$$

The advantage of the direct probing is the measuring process is straightforward, but the downside is its incompatibility with the typical 4-point probe measuring equipment, since these two pair probes are supposed to contact with two different surfaces. As illustrated in Figure 3.16, one solution is to connect two TSVs using a metal trace at their backside and perform the typical 4-point probing twice to obtain the total resistance R_{Total} and the linking part resistance R_{Link}. Assuming these chained two TSVs are the same and ignoring the contact resistance between the probes and testing vehicle, R_{TSV} can be expressed as

$$R_{TSV} = (R_{Total} - R_{Link}) / 2. \tag{3.4}$$

One requirement should be fulfilled for either direct probing or indirect probing is that the TSV opening should be large enough to accommodate two probe tips at the same time. For all TSVs fabricated in this project, there is no choice but to embrace the 2-point probe, since their diameter merely allows for one probe tip. In theory, the metal trace can be directly deposited onto the testing vehicle through standard microfabrication in terms of mask printing, metal sputtering, spin-coating of photoresist, UV light exposure and metal etching. Another option is to bond the entire testing vehicle to a Si substrate (sometimes it can be a PCB), on which such procedures have been performed already. Here, a more efficient way to obtain the connection is to use the same conductive epoxy. As given by Figure 3.17, the measuring process starts with repeating the vacuum suction operation aforementioned until enough filling materials appear on the backside; after the curing process, a sharp blade is used to scratch both sides in order to remove the excessive material. After that, several groups of adjacent TSVs within the TSV array are randomly chosen and connected on the backside using the same Ag-based epoxy squeezed out from a fine syringe tip. Then, the same curing process is performed to cure the link part. In the next step, the resistance of the link part is measured using a standard 2-point ohmmeter (Keithley 2400 Digital Sourcemeter) under a microscope. The last step is flipping the testing vehicle and measuring the total resistance.

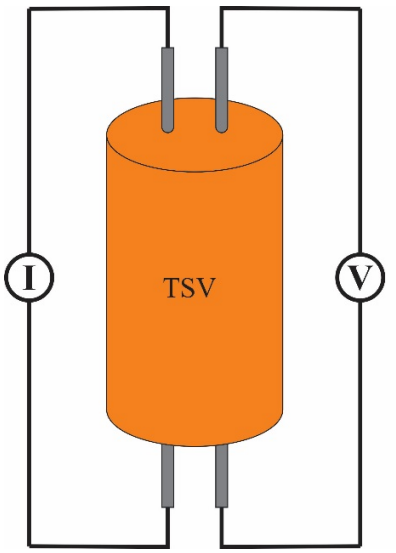

Figure 3.15 A schematic demonstration of the direct probing process of the TSV resistance.

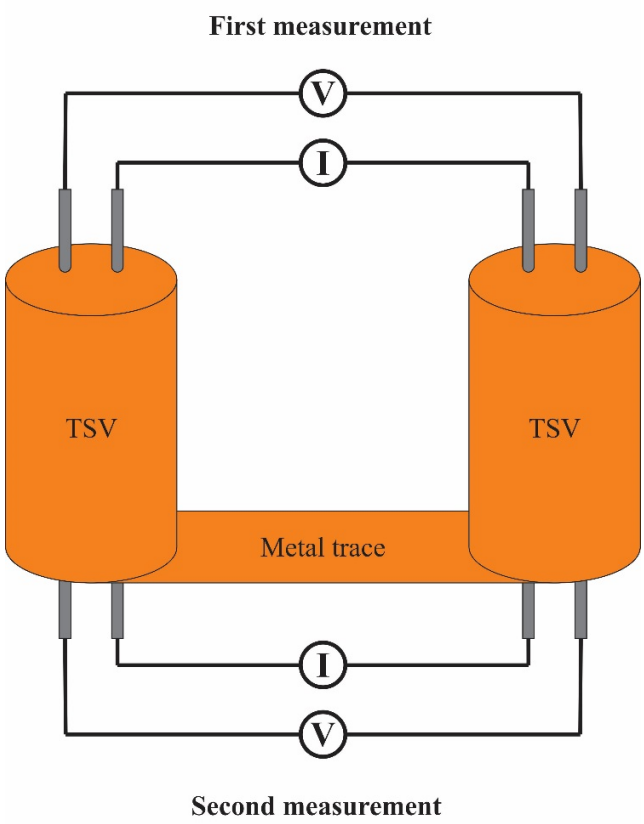

Figure 3.16 A schematic demonstration of the indirect probing process of the TSV resistance.

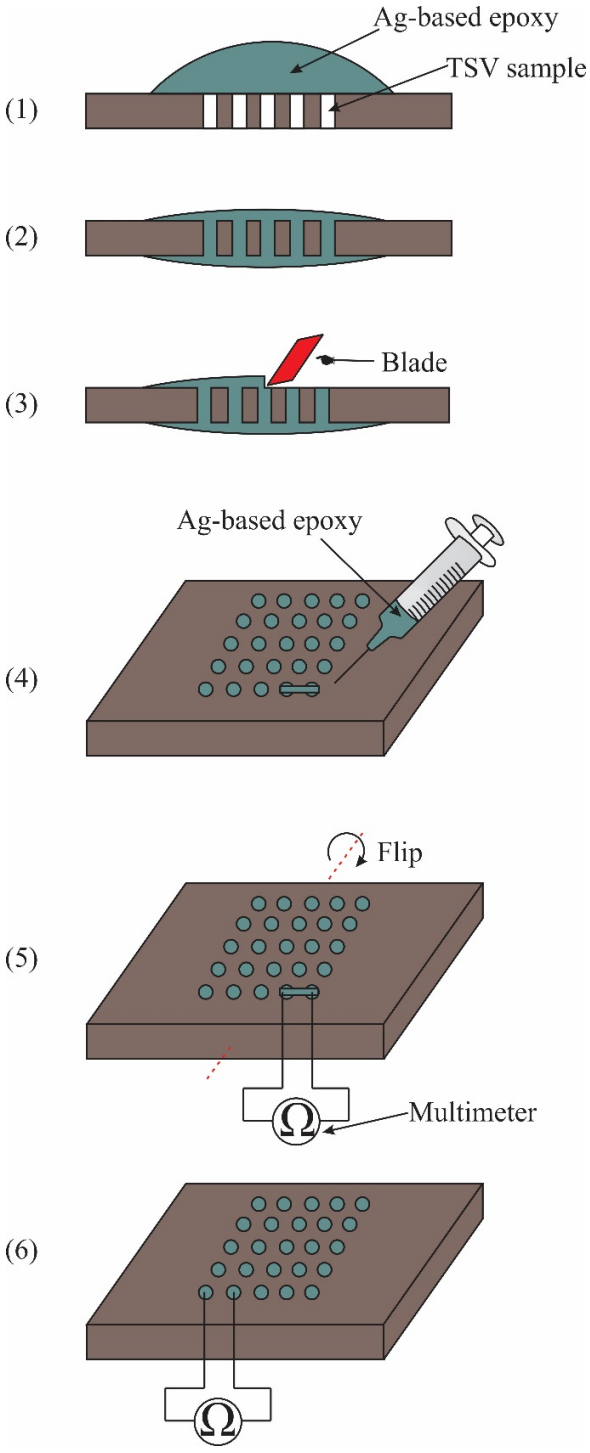

Figure 3.17 A schematic demonstrate of the efficient way to measure the TSV resistance. Two adjacent TSVs are connected using the same conductive polymer. (1)-(3) Fully fill the TSV array and remove the excessive material on both sides. (3) Connect two TSVs. (4) First measurement. (5) Second measurement.

In the resistance measuring process, totally 28 groups of TSVs are randomly selected and inspected. Figure 3.18 details all their measuring results; the average, maximum and minimum values of R_{Total}, R_{Link} and R_{TSV} are summarized in Table 3.2. It can be found that in most groups, R_{TSV} is higher than R_{Link}. As shown in Figure 3.19, a simplified model is built up to explain this phenomenon, in which the link part is assumed to have a semi-cylinder shape and two full cylinders located at each end stand for the two linked TSVs. When the structure is made of the same material and has a uniform cross section, its theoretical volume resistance can be defined by Pouillet's Law

$$R = \rho \times L / A, \tag{3.5}$$

where R is the volume resistance, ρ represents the volume resistivity, L and A stand for the length along the current flow and the corresponding cross section area [140]. The link part and TSVs are made of the same material, thus

$$\rho_{Link} = \rho_{TSV}, \tag{3.6}$$

where ρ_{Link} and ρ_{TSV} are the volume resistivities of the linking part and TSV. The distance between two adjacent TSVs is fixed at 500 μm, which is equal to the depth of the TSV, so

$$L_{Link} = L_{TSV}, \tag{3.7}$$

where L_{Link} and L_{TSV} are the lengths of linking part and TSV. Considering the shape of the link part and TSV,

$$A_{Link} = \pi \times (\Phi_{Link})^2 / 8, \tag{3.8}$$

$$A_{TSV} = \pi \times (\Phi_{TSV})^2 / 4, \tag{3.9}$$

where A_{Link} and A_{TSV} are the cross section areas of the linking part and TSV; Φ_{Link} and Φ_{Link} are their diameters. Figure 3.20 shows the detail of the syringe tip under a microscope, whose inner diameter is roughly 270 μm, i.e. Φ_{Link} = 270 μm. By putting (3.6), (3.7), (3.8) and (3.9) into (3.5), the relationship between R_{TSV} and R_{Link} can be expressed as

$$R_{TSV} = 3.6 \times R_{Link}. \tag{3.10}$$

This matches well with the real situation, since the average values of R_{Link} and R_{TSV} from the real measurements are 8.45 Ω and 23.39 Ω.

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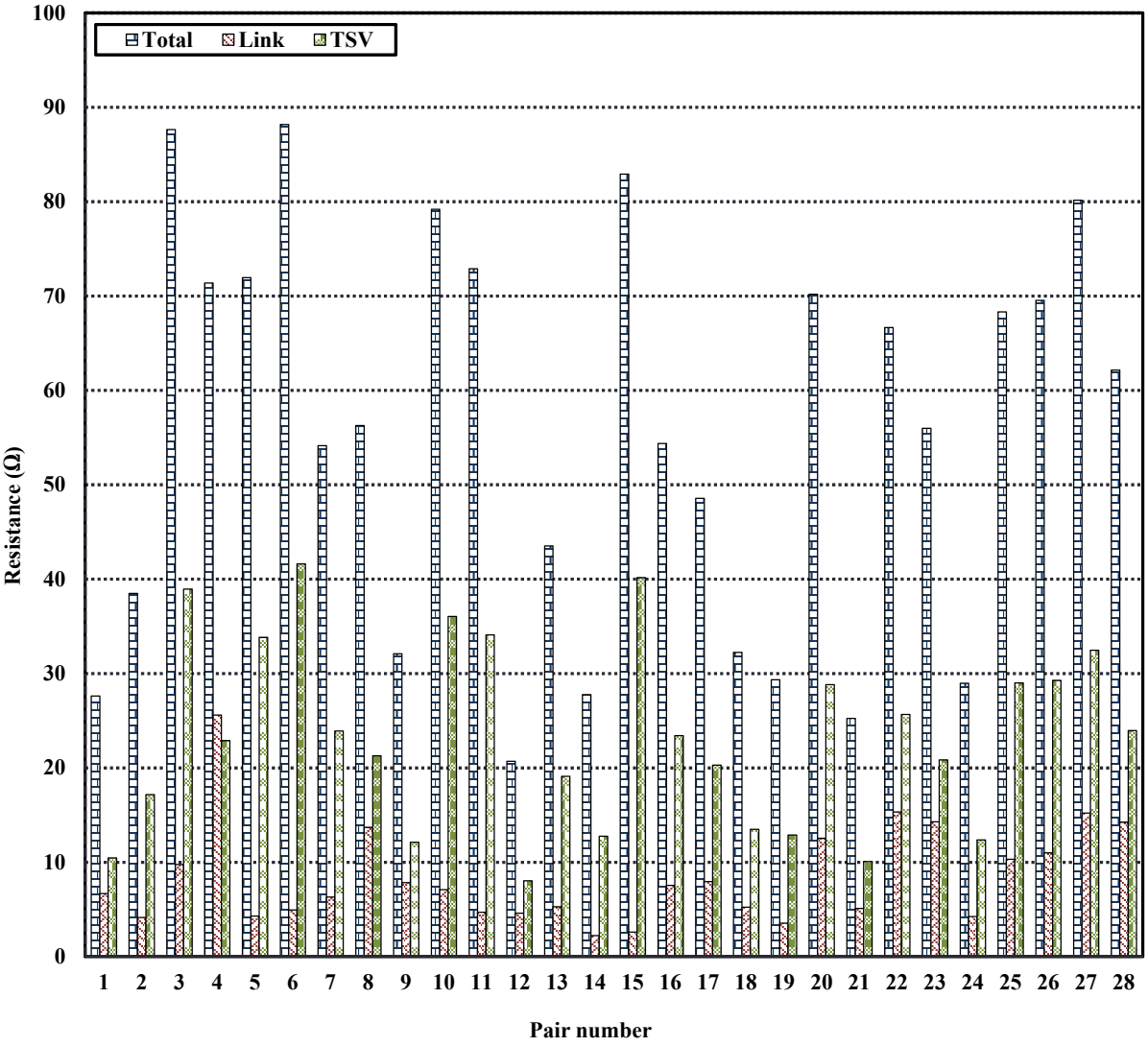

Figure 3.18 A summary of resistances of 28 pairs of TSV.

Table 3.2 A brief summary of the TSV resistance obtained from measurements and calculations.

Resistance (Ω)	R_{Total}	R_{Link}	R_{TSV}
Theoretical	0.36	0.04	0.16
Average	55.24	8.45	23.39
Maximum	88.19	25.61	41.62
Minimum	20.71	2.23	8.04
Standard Deviation	21.29	5.25	9.91

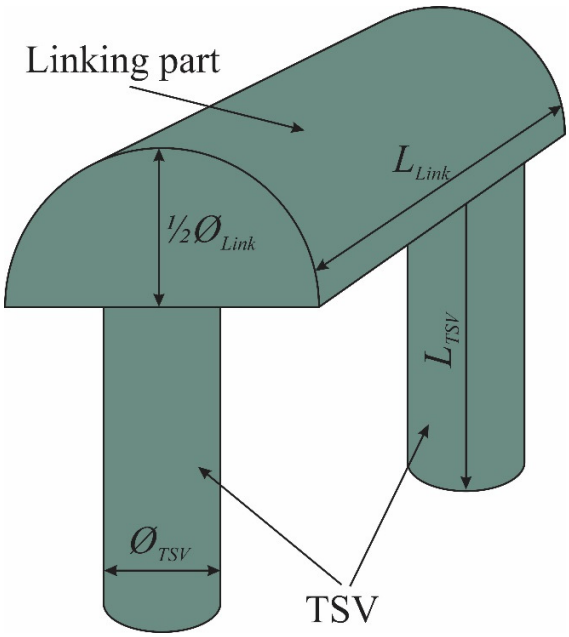

Figure 3.19 A simplified model of two chained TSVs. The whole structure is made of the same conductive polymer.

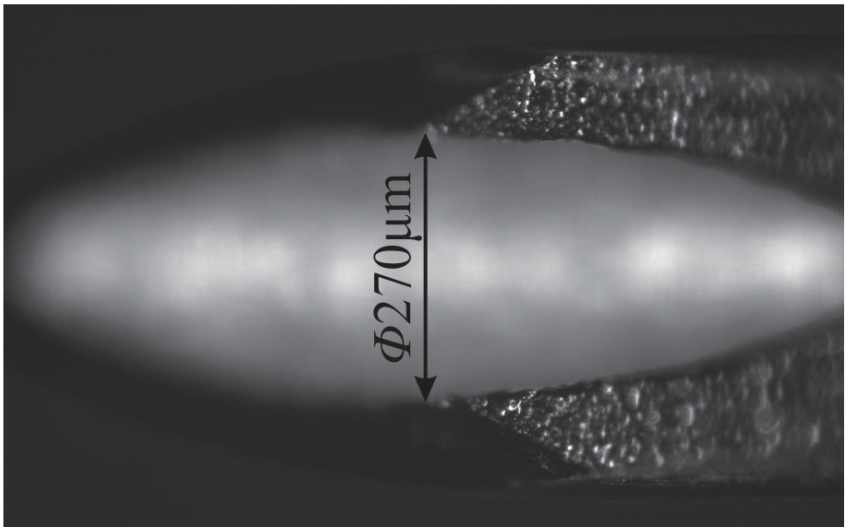

Figure 3.20 A close look at the syringe tip. The inner diameter is 270 μm.

A noticeable phenomenon, which has also been mentioned in [101], is that the calculated resistance is different from the measured resistance. The main reason is that the measurement of their conductivity is typically performed in an ideal environment; but in practical applications, many factors including heating, shear force, chemicals, *etc.* cannot remain the same, which will uplift the practical resistance. The second reason is the contact resistance that is embedded in the 2-point probing process. The fabrication errors in terms of overetch, underetch, sidewall roughness, *etc.* would also contribute to the difference.

3.3.3 Conductivity Thermal Stability

In the previous studies of metal-based TSVs, a portion of attention has been paid to the filling ability, deposition quality and efficiency [88, 141-143]. One factor has been barely inspected is the TSV's resistance thermal stability, because for most metals that are commonly applied for the connection purpose in MEMS devices, including Cu, Al, Au and Ag, their resistivity change that is caused by only one degree temperature increase or decrease is less than 1%, based on the fact that their temperature coefficients of resistivity are in the range of 3.4×10^{-3} $(°C)^{-1}$ to 6.8×10^{-3} $(°C)^{-1}$ [144]. But such information on this Ag-based epoxy is not specified, from the point of view of reliability and safety, values of R_{Total} at different temperature points are supposed to be measured.

5 out of 28 testing vehicles are randomly selected for this measurement which starts at room temperature (RT, 20 °C) and ends up at 180 °C. At each measuring point, they are maintained on the hotplate (Fisher Scientific^{TM} Isotemp^{TM}) for 1 min in order to ensure the full temperature synchronization and the two probes should remain contacting the pair of TSVs for 1 min before collecting the data. Figure 3.21 displays their results. At the first observing point, their original resistances are different, ranging from 21.19 Ω to 74.71 Ω. During the heating process, resistance increases can be witnessed from each testing vehicle; but as long as the temperature does not exceed 120 °C, taking their original values into consideration, these increases are negligible, as the most significant one (from testing vehicle 2) is only 2.95 Ω, only 5% of its original resistance (71.01 Ω). However, when the temperature climbs to 140 °C, a clear upward trend starts to show up, since the growth is around 10 % for almost all testing vehicles. After that, this upward trend continues and becomes dramatic, as all resistances shoot up to a level higher than 110 Ω at 180 °C. Based on these results, a rough estimation of the operating temperature range of this Ag-based epoxy is from 20 °C to 120 °C; and outside this range its electrical property may experience dramatic degrades.

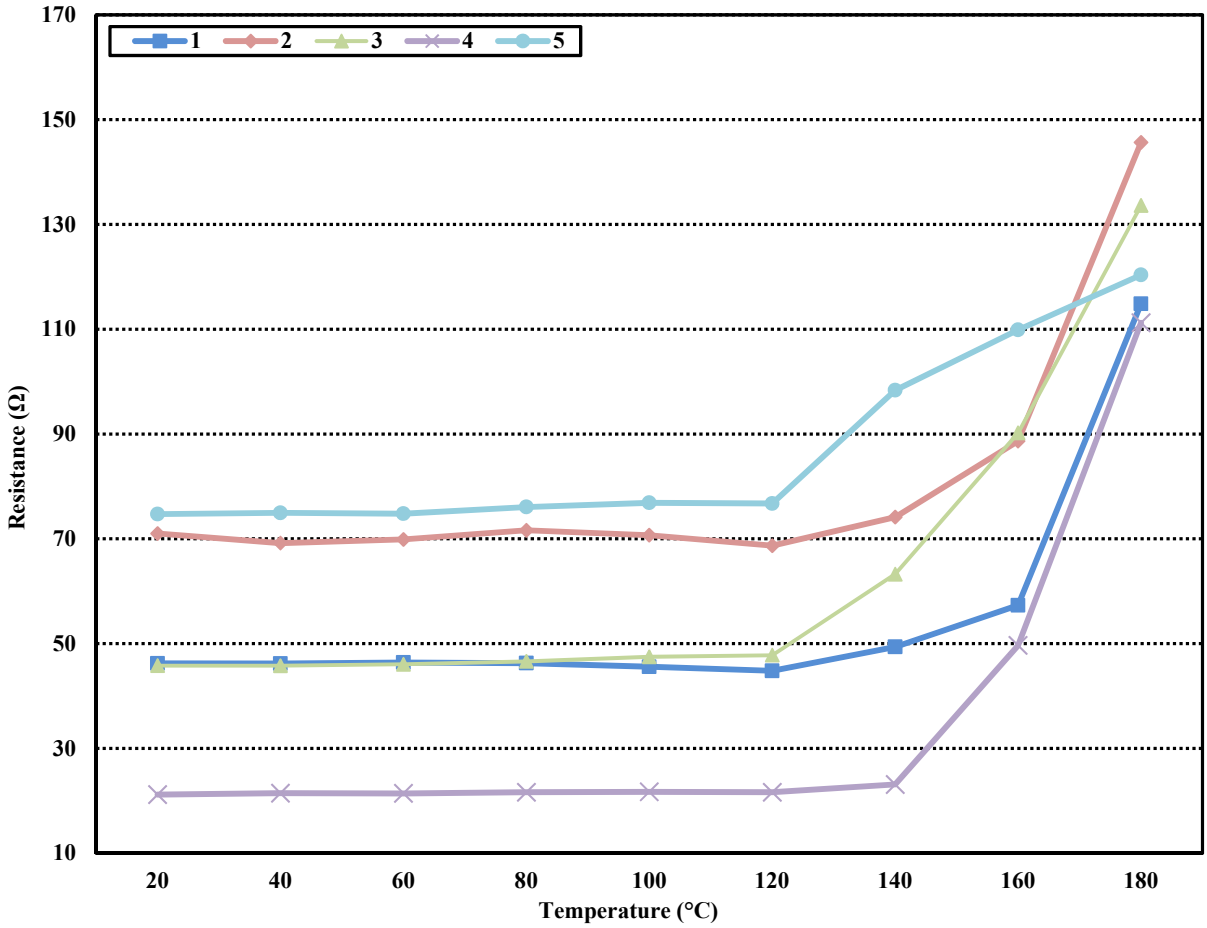

Figure 3.21 A summary of the total resistance (R_{Total}) of five samples measured at different temperature points.

3.3.4 Connection Stability

As has been introduced in Chapter 2, the bonding pad which comes from the deposition and pattern of a thin metal layer should cover the top and bottom of each TSV after its body is fully filled and surface is well polished, to improve the electrical connection quality in the vertical direction. The bonding strength of this conductive epoxy to metal materials has not been tested before, so the risk of unacceptably high contact resistance might exist.

As described in Figure 3.22, a quick investigation is conducted. The first step is to measure the total resistance of two chained TSVs as usual. Next, a thin Cu layer with thickness of 1 μm is deposited on the top through the physical sputtering. Instead of using the conventional

photolithograph procedure to form the bonding pads, one way is using a sharp blade to remove the excess Cu material around the two chained vias. Lastly, the new total resistance $R_{TotalCu}$ at 20 and 120 °C is measured. The basic thought behind this test is that: by simplifying the bonding pads and chained TSVs into a series circuit and considering the volume resistance of this Cu layer is negligible, no significant difference between R_{Total} and $R_{TotalCu}$ should be noticed if there is no severe adhesion defect at the bonding interface.

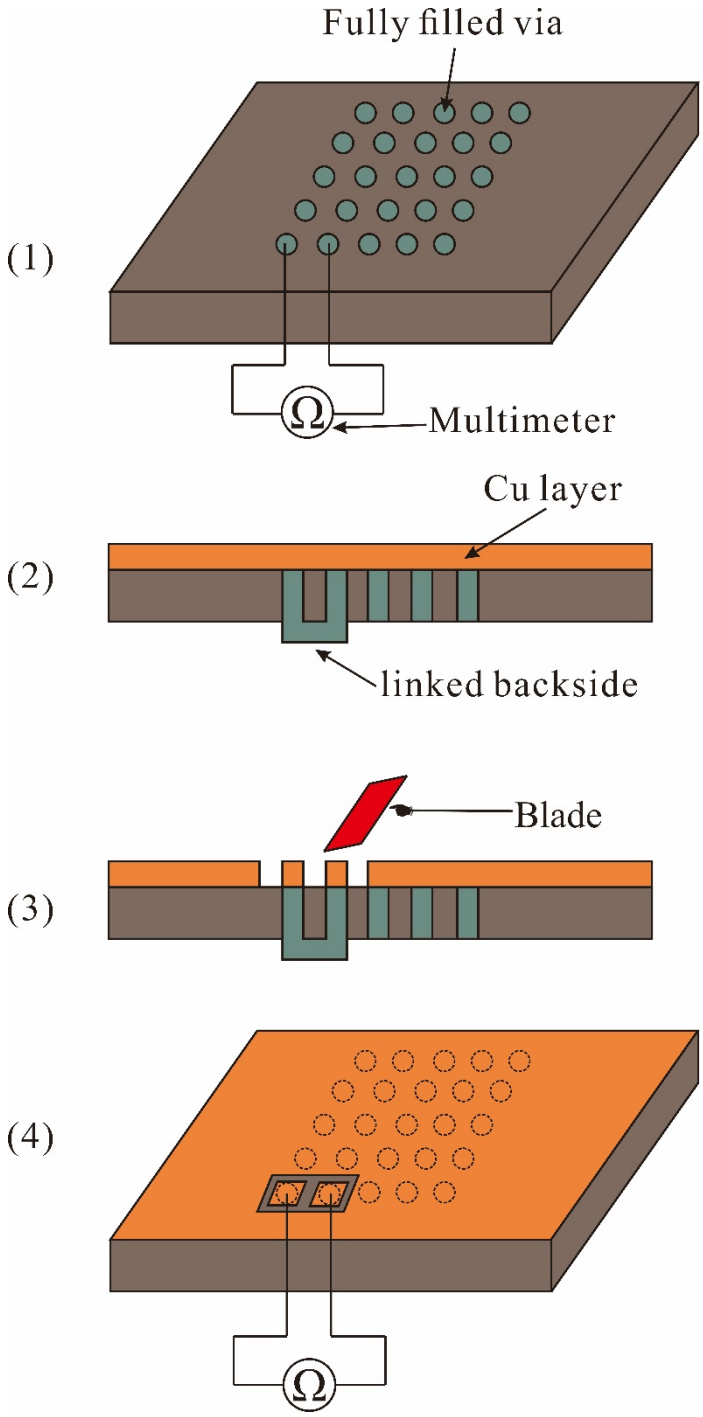

Figure 3.22 A schematic demonstration of how to perform the adhesion test rapidly. (1) First measurement without the Cu layer. (2) Cu layer deposition. (3) Remove the excessive Cu to expose the top. (4) Second measurement. The Cu layer and two chained TSVs can be treated as a series circuit.

In Figure 3.23, three bars in each cluster stand for the total resistance without Cu layer at RT, with Cu layer at RT and with Cu pad at 120°C respectively. It can be seen that for each sample, at RT the total resistance is slightly affected by the Cu pad as no significant increase or decrease appears. This indirectly proves that the adhesion quality is acceptable. When temperature shot up to 120°C, no obvious changes appear either, this implies that the difference in CTE would not result in any electrical or mechanical failures when temperature is in a certain range.

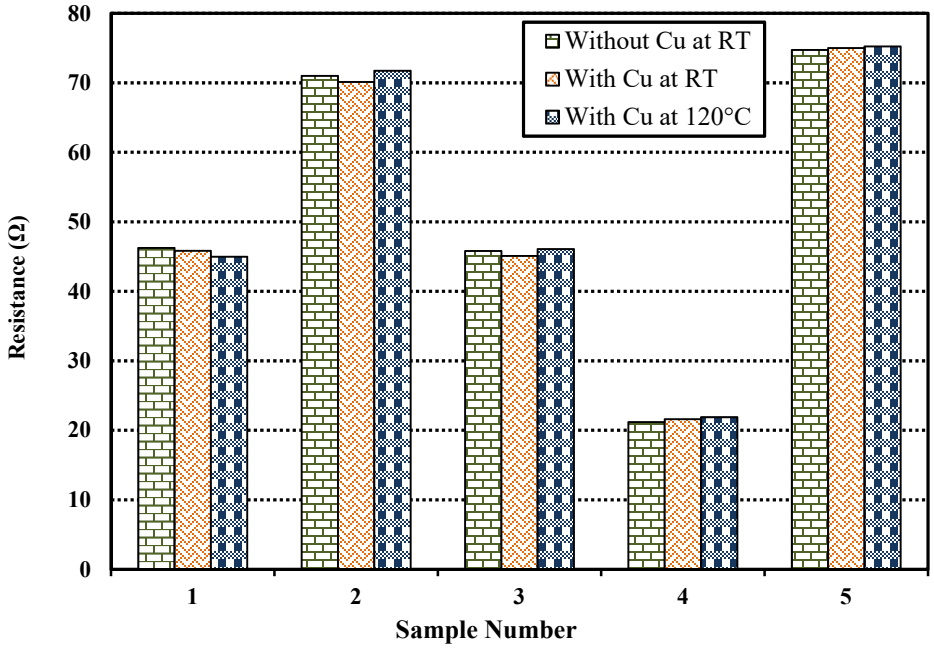

Figure 3.23 The total resistance of five testing vehicles measured without the Cu layer at RT (green), with the Cu layer at RT (yellow) and with the Cu layer at 120 °C (blue).

3.4 Conclusion

In this chapter, a high speed process is developed to metallize TSV with Ag-based epoxy in a vacuum environment. Experimental results indicate that increasing the vacuum level is more efficient than extending the duration to attain a higher filling ratio. Compared with the conventional Cu electroplating, the entire filling process is simplified and askes for 3 s only (if 1.6 kPa pressure difference is applied); more importantly no additives are needed to realize the 100% filling ratio and no environmental pollution is caused during the whole process. Also, an easier way to measure the TSV resistance is discussed; the average resistance is 23.39 Ω, which is

consistent with the theoretical model. Lastly this Ag-based epoxy's resistivity stability during temperature increase and bonding strength to Cu-based bonding pads are tested and accepted results are received.

"Gordy's gone, man. I will be outside. Good luck."

-- Black Hawk Down

Chapter 4: Embedded RDL Silicon Interposer

As a close follow-up to the TSV related work discussed in previous chapter, a new architecture of silicon interposer with faster fabrication rate and more reliable interfacial connection quality for 3D integration is proposed through replacing conventional RDLs (redistribution layers) with conductive polymer filled trenches that are embedded between two layers. Both Ag-based and C-based conductive polymers with different viscosities and conductivities are investigated under a set of vacuum suction conditions for various via and trench dimensions. Their thermal stability and bonding strength to typical metal materials are tested afterwards.

4.1 Introduction

Driven by requirements of more functions [145], smaller geometry [146], higher bandwidth [147], lower latency [148], less power consumption [149], 3D integration has been widely adopted in modern IC industry [150]. Among all 3D integration techniques, silicon interposers which are made up of RDLs and TSVs have been regarded as a remarkable milestone in the evolution of M/NEMS [151-154], because of their functions as follows.

1) Combining chips with different geometries and integrating interfaces into a single stack, which is capable of accelerating the speed of following integration operations [155].

2) Providing different layers with electrical channels in vertical and horizontal directions, which guarantees the signal exchange among all functional components.

3) Redistributing the I/O to a larger area, which is beneficial to the following assembly and the thermal dissipation.

Figure 4.1 shows a detailed explanation of how to realize the interconnection among vertically stacked devices. When two TSVs from two layers can perfect overlap at the packaging interface, no matter they have the same diameter or not, usually their diameter are too small to provide

enough contact area for acceptable electrical connection. Thus, metal bonding pads are always needed, for not only enhancing the connection quality but also simplifying the following packaging process. A more common situation is, they cannot be perfectly overlapped since their locations have a conflict with other functional elements, and the size of bonding pads is insufficient to compensate such a gap. To solve this problem, metal traces are formed to bridge them. The combination of all metal bonding pads and traces that are formed on the top of TSVs is one of the major components of RDL.

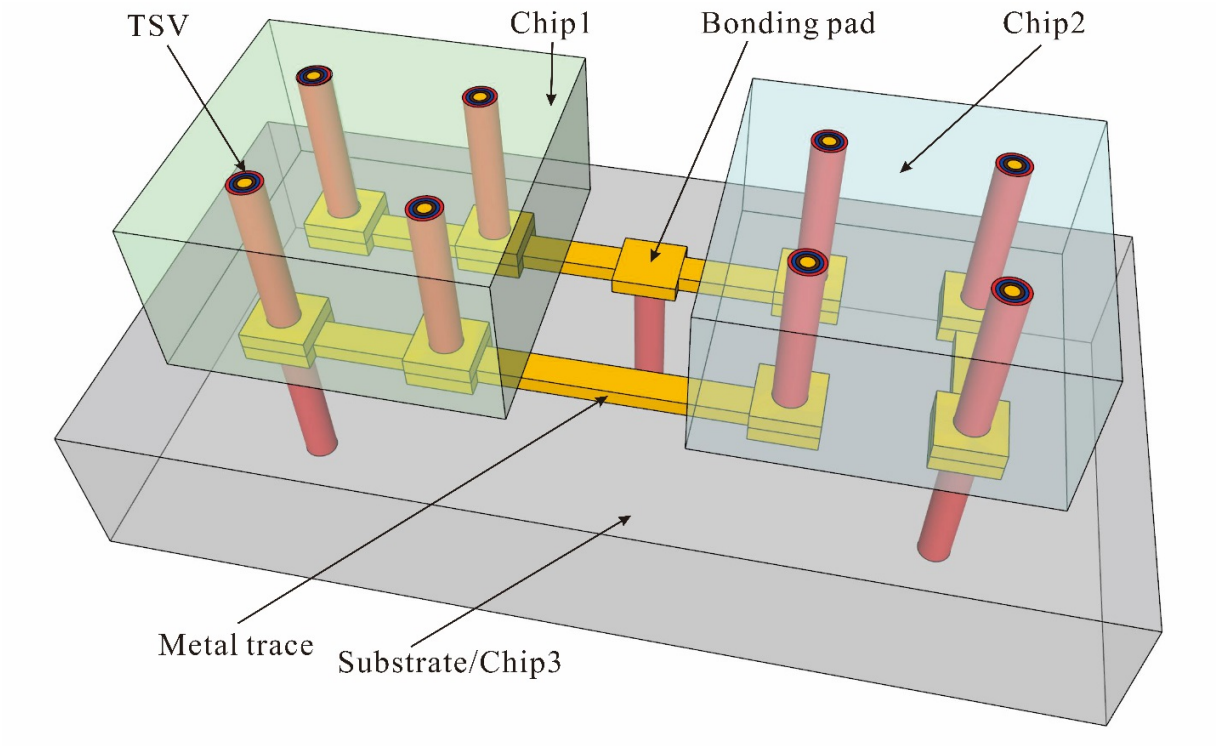

Figure 4.1 A schematic demonstrate of the typical silicon interposer. Chip1 and Chip2 are mounted on the substrate. Their mutual communication is based on TSVs, bonding pads and traces.

Unfortunately, from the point of view of fabrication, either RDL or TSV used in active Si wafers has a number of issues, which make the 3D IC implementation problematic. Of particular concern is the unreliable connection between two vertically stacked metal bonding pads. First, the nonuniform topography and the misalignment at their contact interface is not easy to eliminate,

especially for the case that a large number of metal bonding pads are supposed to pair at the same time [20]. Furthermore, the utilization of different materials is often inevitable, this will make such situation even worse due to the mismatch of their thermal, chemical and electrical properties [21, 22]. The second part comes from the Cu electroplating which has become the most widely used way to metallize TSV. Disadvantages in terms of long processing duration, environmental pollution, *etc.* have been explicitly discussed in Section 2.2.2.

Over the past decades, various flexible interconnects have been successfully developed for the optimization of interfacial connection. For example, Muhannad S. Bakir *et al.* proposed to form curved Cu leads on a low modulus polymer layer with air bubble trapped underneath for gigascale integration [156]. The result suggested that the maximum compliance in vertical direction could be controlled through modifying the polymer layer's thickness. About 500 μm thick polymer layer was able to provide 50 μm of compliance at 8 mN. Hyung Suk Yang *et al.* invented an interconnect structures that possessed high compliances in both in-plane and out-of-plane directions. With a tapered design and curved profile, their beam structures were able to fully use the stand-off height of 20 μm with no damage or significant yield undergoing after solder reflow [157]. A similar idea of employing micro cantilevers to allow for good interfacial connecting quality was proposed by Ivan Shubin *et al.* As a benefit of using pure metal material, the interfacial resistance was lower than 1 Ω without the help of reflowing bumps. Moreover, their cantilevers were able to compensate the vertical mismatch up to 30 μm [158].

For these flexible interconnects, their shape plays a critical role in realizing the performance. Thus, all aspects of it should be carefully engineered to minimize the stress that the beam structures will experience and to assure that they will not be constricted in any way during the deformation process [157]. In this work, we thus propose a new interposer architecture with less fabrication complexity and more reliable interconnection quality for 3D integration. To be more specific, as shown in Figure 4.2, apart from conventional vias that pass through the substrate body, trenches are patterned on the substrate surface; each trench connects one end of the corresponding through via, building up an elbow like structure. After the chip is mounted to the substrate, all sealed 3D channels that are formed by vertical vias and horizontal trenches will be metallized by the vacuum suction of the conductive polymers, since this kind of materials are commonly in liquid state, hence they will not ask for any temperature budgets compared with solder or alloy; also unlike printing

inks, less or no solution is contained in them, which means a higher filling ratio. These trenches that are embedded at the mounting interface are supposed to replace the traditional RDL to achieve the electrical connection and the I/O rearrangement horizontally. The advantage of this new silicon interposer is that any potential disconnections and contact resistances at the interface will disappear because all connecting paths, i.e. 3D channels, are metallized in a simple operation with the same material. Moreover, all modifications are made to the substrate, the design and fabrication of chips are not influenced at all.

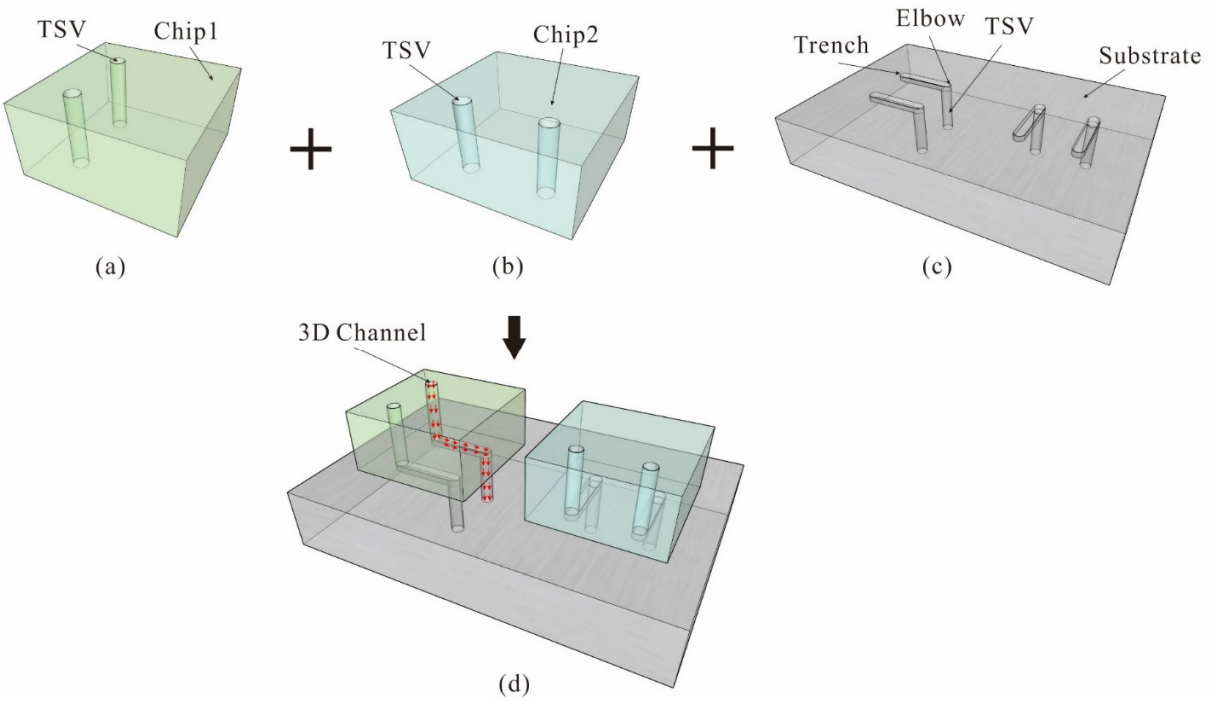

Figure 4.2 A schematic demonstration of the proposed silicon interposer architecture for 3D integration. (a) No change is made to Chip1. (b) No change is made to Chip2. (c) Elbows structures are formed on the substrate. (d) Channels are formed after the integration.

4.2 Interposer Fabrication

4.2.1 Conductive Polymer Selection

C-based particles in terms of carbon nanotube, carbon fiber, carbon black, graphene, graphite *etc.*, are commonly used to equip host polymers with conductivity due to their relatively low price and high compatibility; while the downside is that the extreme agglomeration behavior of C-based particles will result in high resistivity (10^2 Ω·cm to 10^{-2} Ω·cm) and poor fluidity (300 Pa·s or higher). Another large category is based on metal materials including Ag or Cu spheres, Ag flakes, many kinds of metal salts, *etc*. Regardless of their prices, the advantage is that they can have low resistivity (10^{-2} Ω·cm to 10^{-5} Ω·cm) and good fluidity (lower than 300 Pa·s) at the same time. In this work, a C-based conductive polymer and a new Ag-based conductive polymer (their basic information of them has been summarized in Table 4.1) are tested, based on the following reasons.

1) We want to test more materials to make sure our vacuum suction is not exclusive to only one material.

2) We want to investigate different viscosities and resistivities.

4.2.2 Testing Vehicle Fabrication

To fabricate testing vehicles, 4-inch, 500 ± 10 μm thick, double side polished prime Si wafers (orientation <100>, p type, resistivity of 1 to 10 Ω·cm) are employed. The fabrication process flow of testing substrates (Figure 4.3) is similar to that of (single-layer) TSV testing vehicles described in Section 3.2.4, hence the following part will mainly concentrate on their difference and several important points.

1) The wafer must be soaked in the Piranha solution for 30 mins and rinsed with DI water for three times for the purposed of cleaning. Then to enhance the following spin-coating performance, the HMDS treatment is applied.

2) In the spin-coating process, any protruding or cavity (trench or via) features have a negative influence on the spin-coating quality of photoresist in terms of adhesion, thickness and uniformity. In this case, an efficient solution to this problem is to perform an etchback process to open vias after trenches have been formed. To start with, the positive-tone photoresist AZP4620 is employed again as the trench etching mask.

Considering no through etching is needed, its thickness is reduced to 6 μm to receive good spin-coating quality. Then it is followed by the two-stage soft baking and the dehydration processes.

3) As explained above, the trench etching windows is opened at first by the optical lithography process. Then, the exposed wafer will be developed in diluted AZ400K with gentle shaking for 2 mins until all features can be witnessed. The DI water rinsing is needed to remove the residual.

4) The DRIE (deep reactive ion etching) is employed to form the trenches on the surface. 100 cycles of BOSCH process are enough for the trench patterning. It might be worth noting here is the cycle number is not strictly proportional to the desired etching depth. Typically, the first one third of depth has the fastest etching speed since it is closest to the ion bombardment; the middle part has a moderate etching speed as the bombardment becomes less powerful and ions start to fight each other; with the striking effect keeps reducing, the via bottom part has the lowest etching rate.

5) The wafer needs to be flipped for another layer of AZP4620 with thickness of 12.5 μm.

6) The same optical lithography process is repeated then.

7) After 750 cycles of BOSCH process, the through via is formed on the wafer, linking the trench on the other side as planned.

8) The insulator is made of SiO_2 with thickness of 500 nm formed by thermal wet oxidation.

The testing chip fabrication is almost the same, except no trenches are needed, which will not be discussed any more in this chapter. In theory, the chip can be mounted on the substrate by employing ultrasonic acoustic vibrations (ultrasonic bonding), powerful electrostatic fields (anode bonding, this technique is usually used for glass-Si bonding) or adhesives at their contact interface. Based on the following reasons, the adhesive is preferred in this case.

1) Either the high frequency friction during the vibration or the high voltage used to generate the powerful electrical field can damage the functional components.

2) The employment of adhesive will simplify the packaging procedure; most importantly, thanks to its conformability, the nonuniformity in geometry at the interface will be offset if a suitable load can be applied to press the stack.

Table 4.1 A summary of manufacturer specified parameters of three conductive polymers used for the TSV metallization.

Material Number	Name	Filler	Host	Viscosity (Pa·s)	Resistivity (Ω·cm)	Appearance
M1	Ausbond® 3811	Ag	Epoxy	60-500	6.25×10^{-3}	Viscous silver liquid
M2	Ausbond® 3813	Ag	Epoxy	100-300	7.5×10^{-3}	Highly viscous silver liquid
M3	G6-Epoxy™ G6E-P	C	Epoxy	145-155	5	Thick dark paste

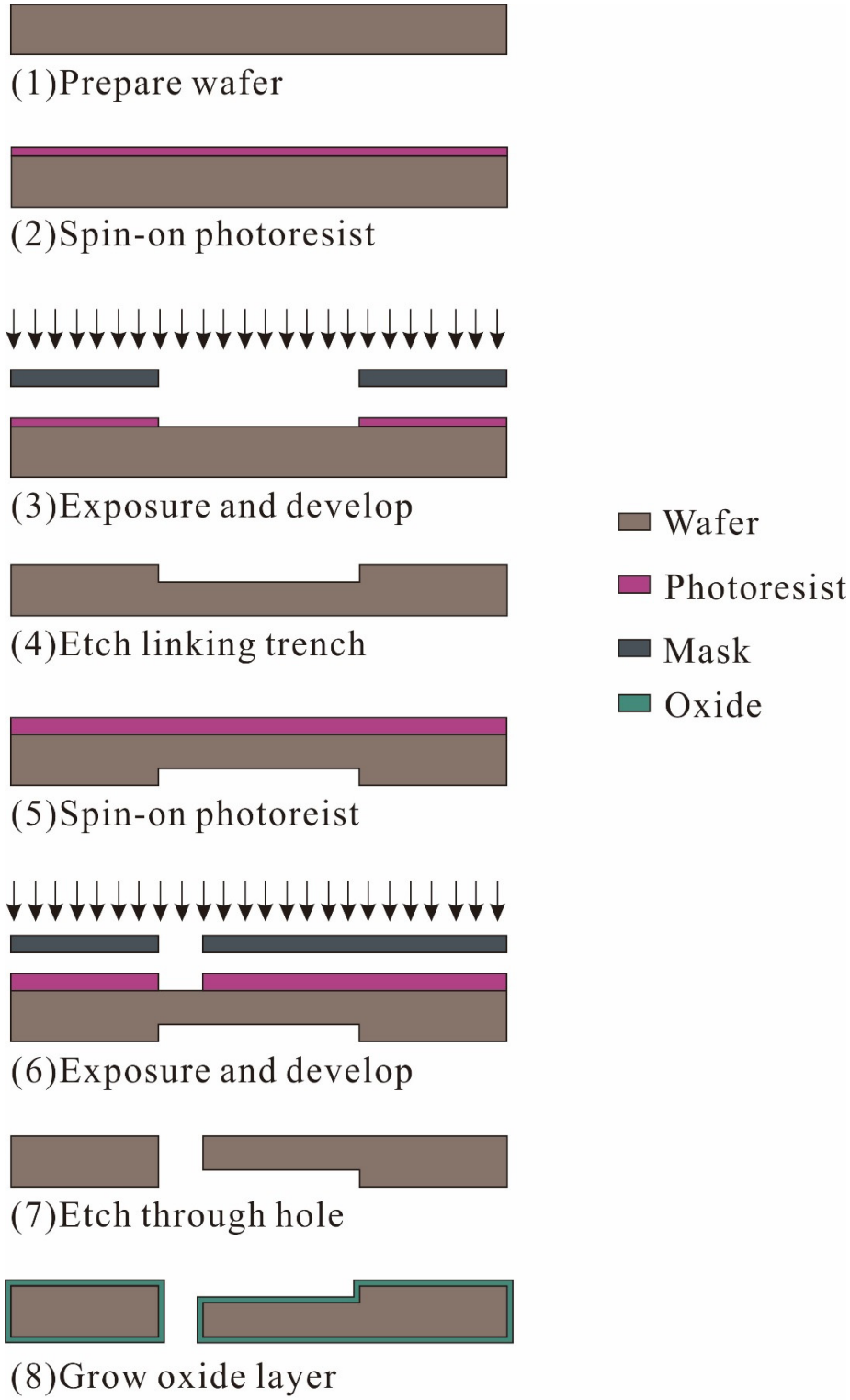

Figure 4.3 A brief description of the substrate fabrication process. The positive-tone photoresist, AZP4620 is used twice as the etching mask.

A thin layer of fluoropolymer called CYTOP® CTL-809M is spin-coated on the chip top, which is going to offer enough adhesion with stable electrical insulation and corrosion resistance [159, 160]. Its original thickness is set to 5 μm, whilst the adjustment could be achieved by changing the spinning parameters. A number of precautions should be taken to prevent it from flowing into any vias and trenches.

1) First, through the standard spin-coating procedure, this adhesive is applied to the chip top merely (no adhesive is on the top or the bottom of the substrate).

2) Then, the high pressure N_2 gas is blown into the via from the other side to drive the unwanted materials out.

3) Lastly, the chip is cured at 100 °C on a hotplate (Fisher Scientific™ Isotemp™) for 1 min to pre-solidify the adhesive.

The integration of chip and substrate is carried out on a flip chip (FINEPLACER® pico ma) to obtain good accuracy, as shown in Figure 4.4. Details are described below. It should be clarified that the substrate can be enlarged to accommodate more chips by simply replicating the flip chip process, although having the same size is able to accelerate the aligning process.

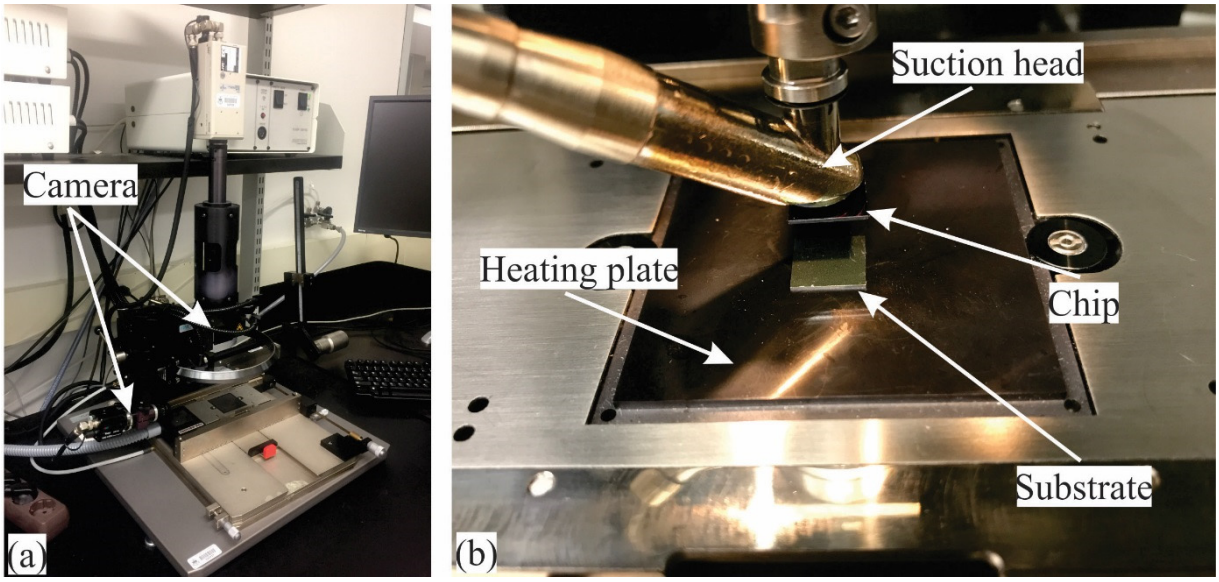

Figure 4.4 A flip chip used for the integration. (a) The overview of the equipment. (b) The detail of the suction head and the heating plate.

1) First, one substrate is placed in the center of the heating plate which has been heated to 180 °C.

2) Then the suction head picks up the chip and brings it to the area above the substrate; adjustments are made based on vertical and horizontal visions provided by two cameras until they are aligned.

3) After that, the suction head can go down and push the chip to the substrate vertically. The pushing load which is 1.5 N along with the heating (180 °C) should remain for 1 min to achieve the pre-bonding.

4) Lastly, the stack is removed from the heating plate and stored at room temperature for 12 h to achieve full bonding.

In order to figure out the limit of this filling mechanism, channels with different dimensions in terms of via diameters and lengths are fabricated. According to the via diameter, all testing substrates and chips are categorized into two sets, i.e. 100 μm in set1 and 150 μm in set2. The width and depth of all trenches from the same set are equal to the via diameter, but their length

varies from 500 μm to 800 μm. Thus, the highest aspect ratio is 18. Detailed dimensional description can be found in Table 4.2.

Table 4.2 The detailed dimensional description about stacks (unit is μm).

Set	Via Depth	Via Diameter	Trench Width/Depth	Trench/Channel Length			
				Group1	Group2	Group3	Group4
1	500	100	100/100	500/1500	600/1600	700/1700	800/1800
2	500	150	150/150				

The fabrication result of testing substrates from set1 can be found in Figure 4.5. All of them are in the same square shape with side length of 10 mm. Four crosses that are placed nearby are alignment marks for the purpose of accurate integration. On each substrate, four trenches and vias are linked to build four elbows in the central region. Figure 4.6 shows the detail of elbows in difference groups. It is easy to notice that the via diameters at joints are slightly enlarged and their outlines are not as sharp as trenches or alignment marks. The main reason is the notching effect [161]. As shown in Figure 4.7, four vias are formed correspondingly on each chip; square holes that are close to left and right edges are alignment marks which will be used in the dicing process.

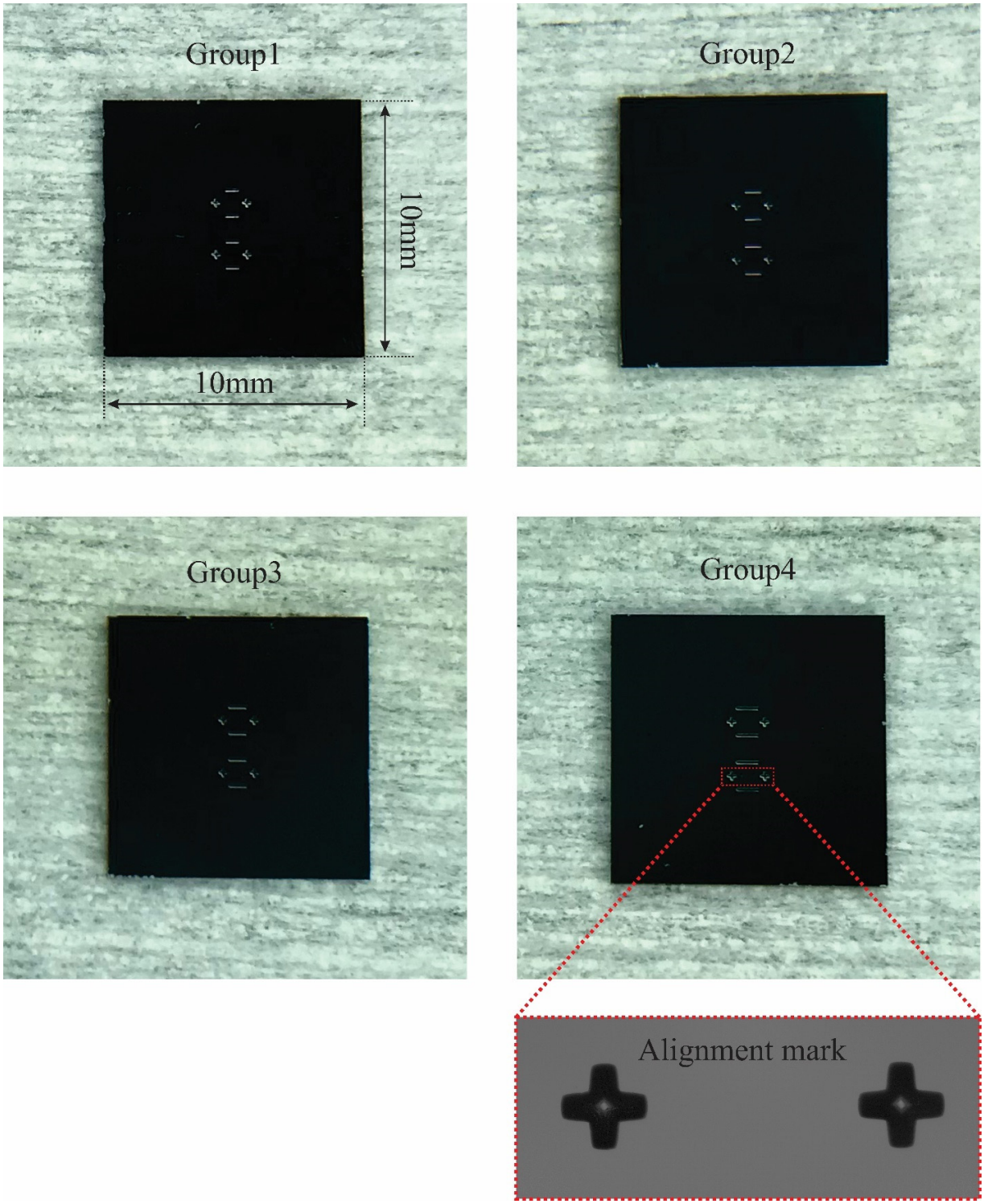

Figure 4.5 The testing substrate from each group in Set1. They are all in a square shape with side length of 10 mm. Four trenches in the same group are the same. The cross features are used as the alignment mark for the integration.

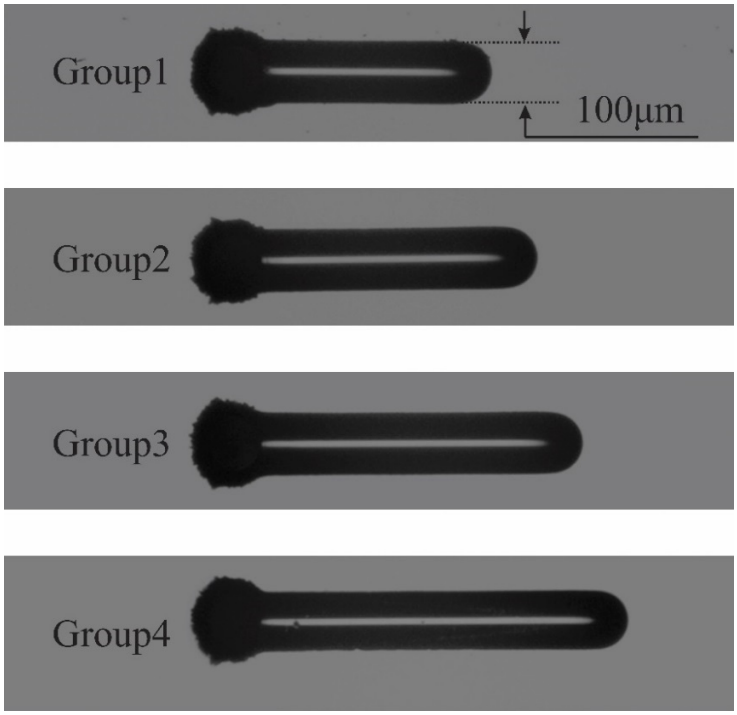

Figure 4.6 A close look at the trench from each group in Set1. They have the same width but different lengths. All through vias are slightly overetched.

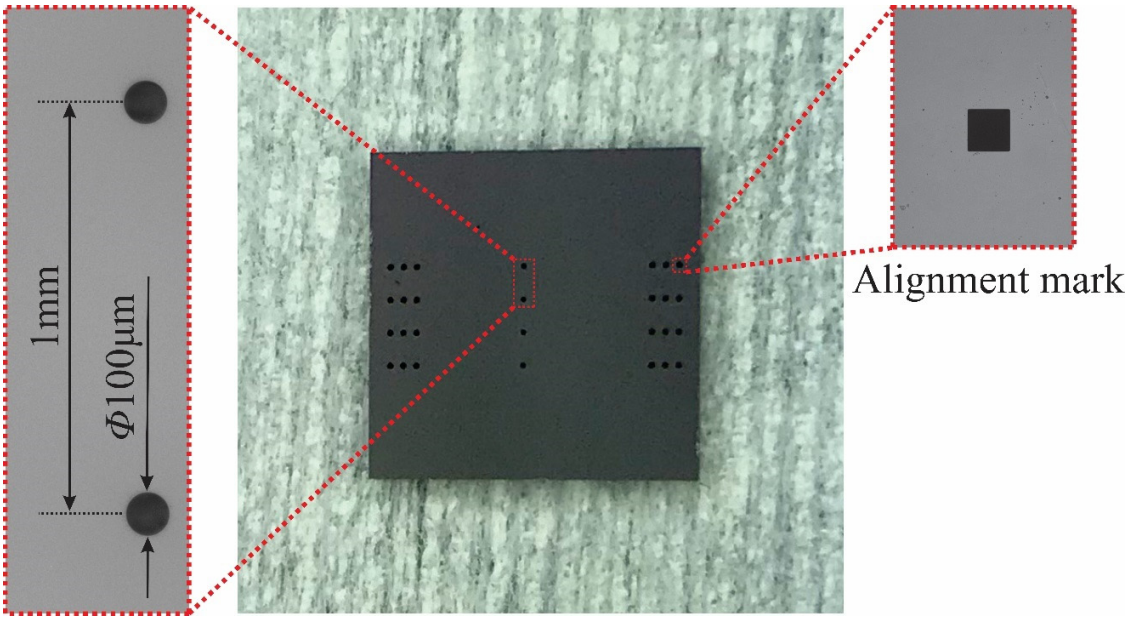

Figure 4.7 The detail of the chip from Group1 in Set1. All square holes close to the edges are used as the alignment mark for the dicing.

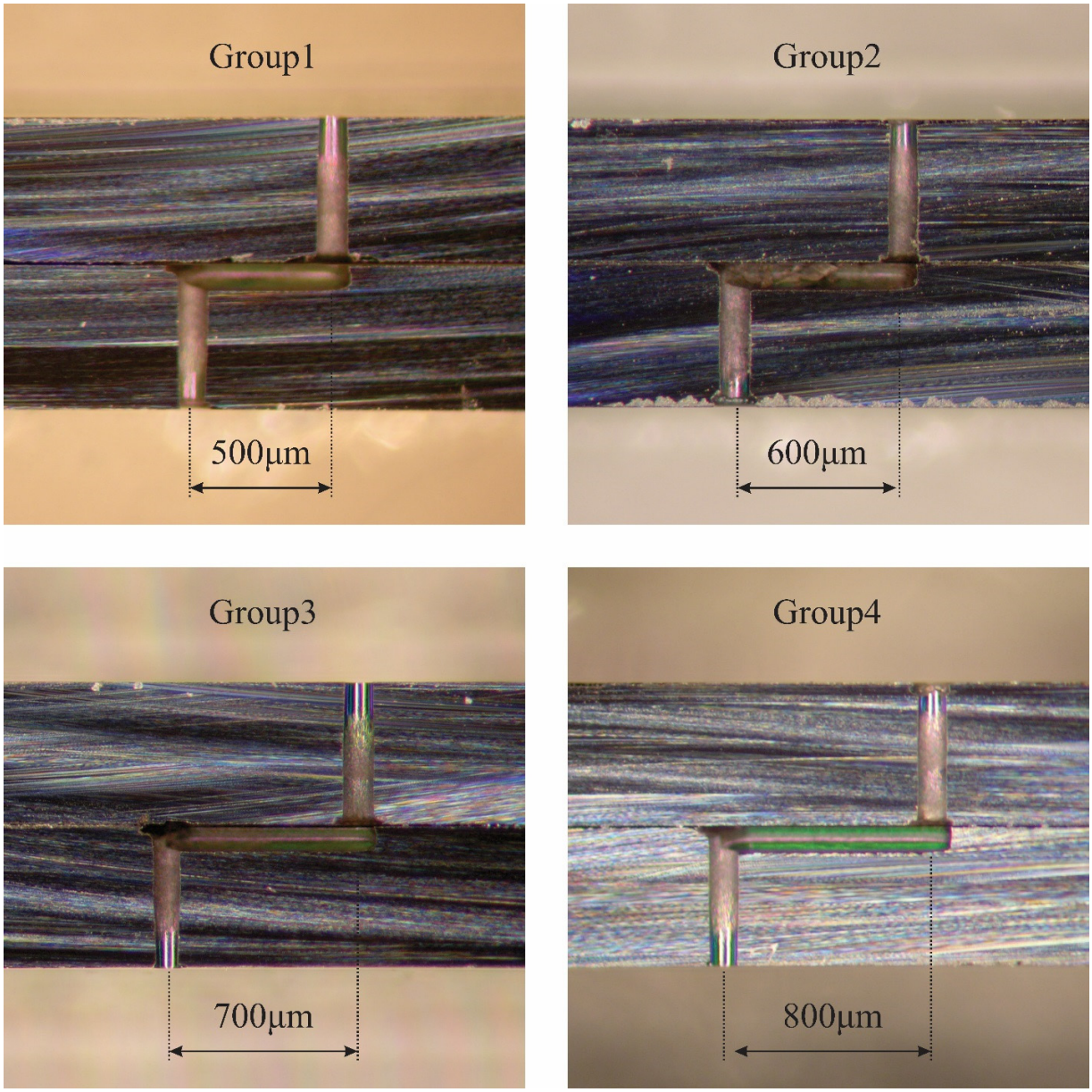

Figure 4.8 A cross section view of the final stack from each group in Set. Their only difference is the trench length.

4.2.3 Silicon Interposer Metallization

The same vacuum suction platform that has been demonstrated in Section 3.2.2 is used again for the metallization of stacks. For each combination of P_{dr} and T_{feed}, the suction operation is repeated for three times at 20 °C. After that, all stacks are cured for 30 mins at 120 °C to obtain

the 100% polymerization. The overburden layer should not be removed in this period to make sure their top would not be affected by the volume shrinkage.

4.3 Characterization

4.3.1 Filling Depth

Figure 4.9 to Figure 4.16 display the filling results. Three colors are employed to differentiate the three filling materials (red-M1, green-M2 and blue-M3) and four filling patterns in each color represent four durations (2 s, 4 s, 6 s and 8 s). Several fundamental conclusions could be drawn.

1) When either P_{dr} or T_{feed} keeps increasing, the filling depth could always maintain a growing trend. P_{dr} is more effective, since every time when it goes up to the next level, the filling depth would witness a sharp uplift; but when P_{dr} is fixed at a certain level, the growth caused by the time extension becomes indistinguishable, especially when the channel has a smaller cross section area.

2) The filling ability would decrease with the viscosity, as the filling depth always experiences a drop between 300 μm and 400 μm when the filling material changes from M1 to M2 or from M2 to M3 under the same P_{dr} and T_{feed}.

3) The channel with larger cross section area would be easier to fill. More specifically, when the via diameter is 150 μm, the shortest channel could be fully filled by all three materials and M2 is still effective unless it extends to 1800 μm. But as long as the via diameter shrinks to 100 μm, the 100% filling ratio could be found in the shortest channel only.

It should be pointed out that the expected growth in some cases is replaced by a noticeable decrease. One explanation of this abnormal phenomenon could be the structural nonuniformity that is caused by the internal surface roughness, etching defects and bonding misalignment. Another one comes from the conductive polymer. Since the physical mixing cannot guarantee every tiny part (such as per 0.01 g) of it is perfectly the same, if the part contains more evaporateable materials is sucked into the channel accidentally, the overwhelm volume shrinkage might cancel the initial increase after the curing process.

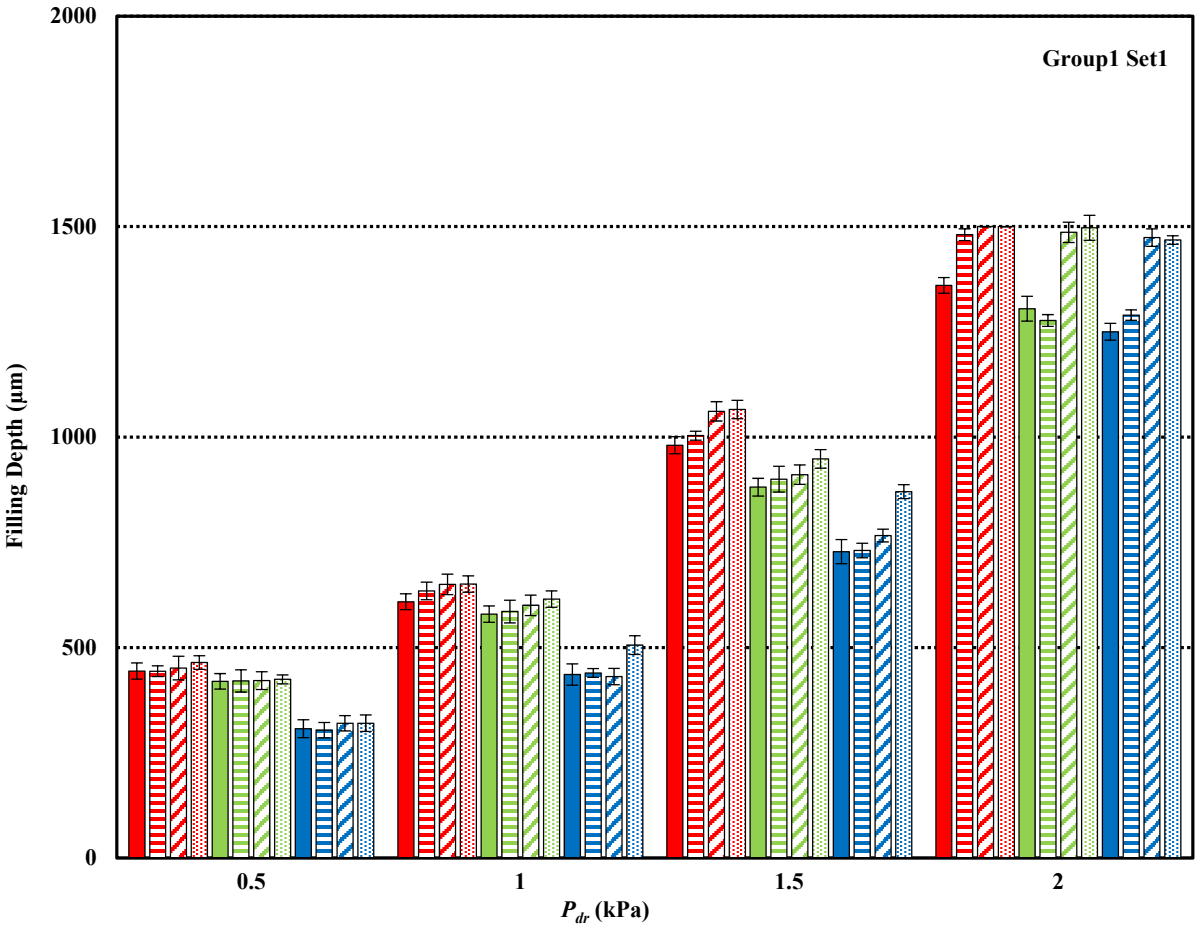

Figure 4.9 The filling result of all channels from Group1 in Set1 (via diameter of 100 μm) under different combinations of driving pressure and feeding time.

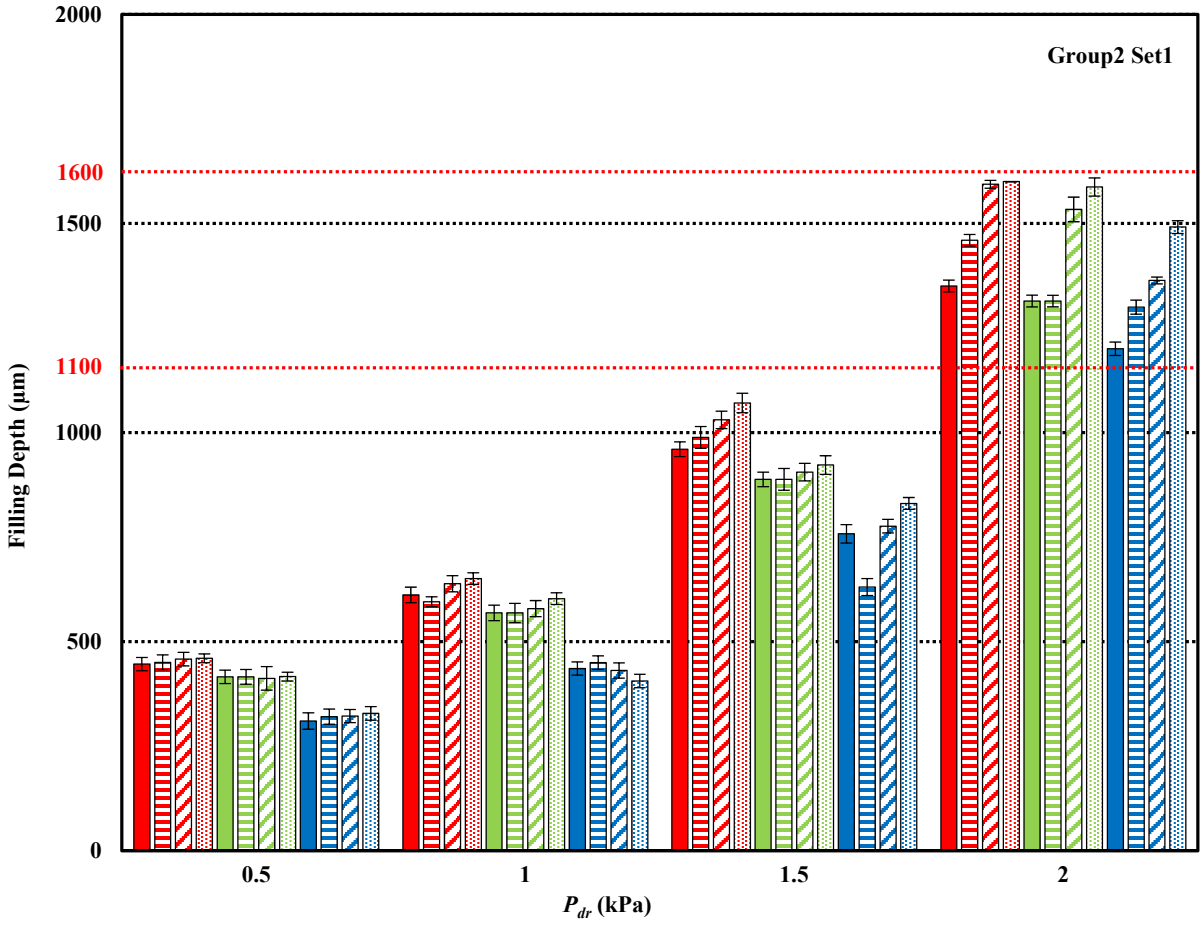

Figure 4.10 The filling result of all channels from Group2 in Set1 (via diameter of 100 μm) under different combinations of driving pressure and feeding time.

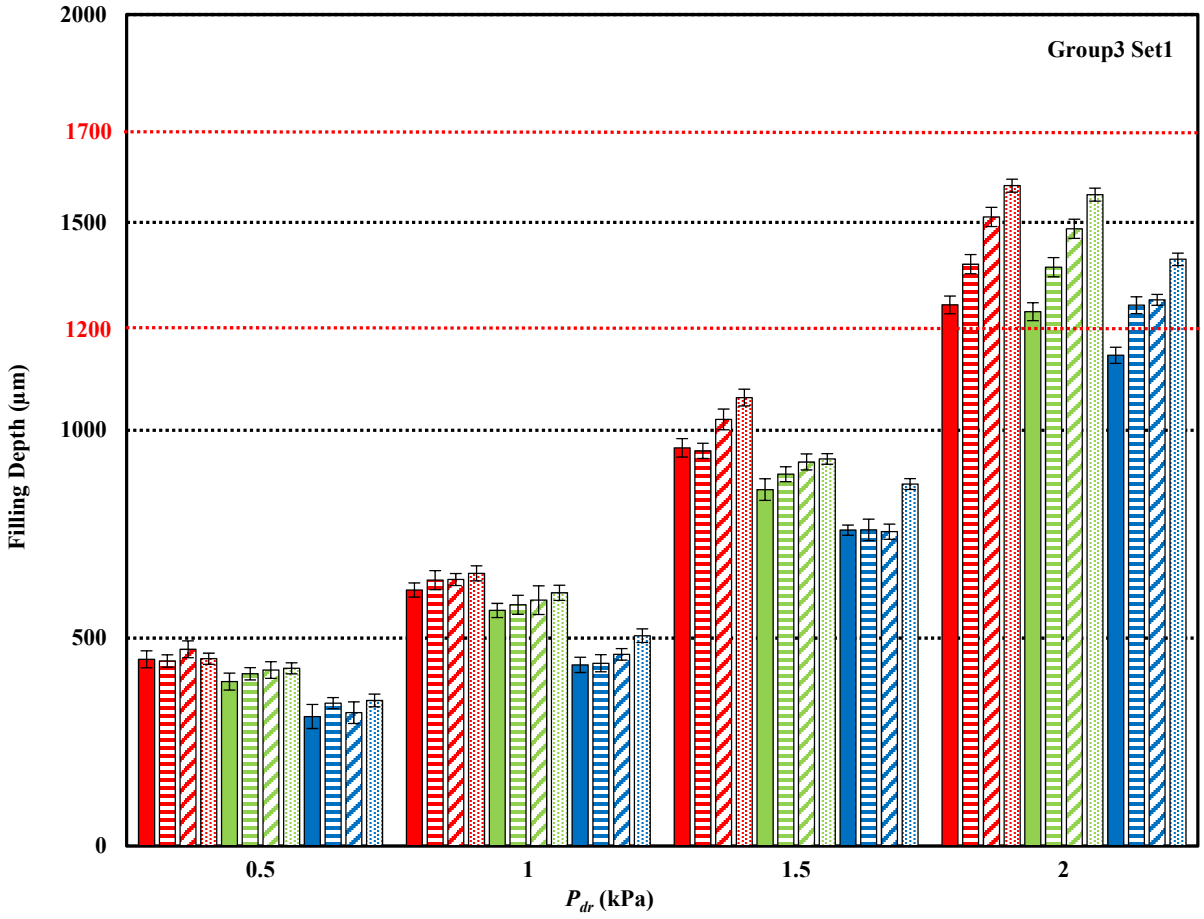

Figure 4.11 The filling result of all channels from Group3 in Set1 (via diameter of 100 μm) under different combinations of driving pressure and feeding time.

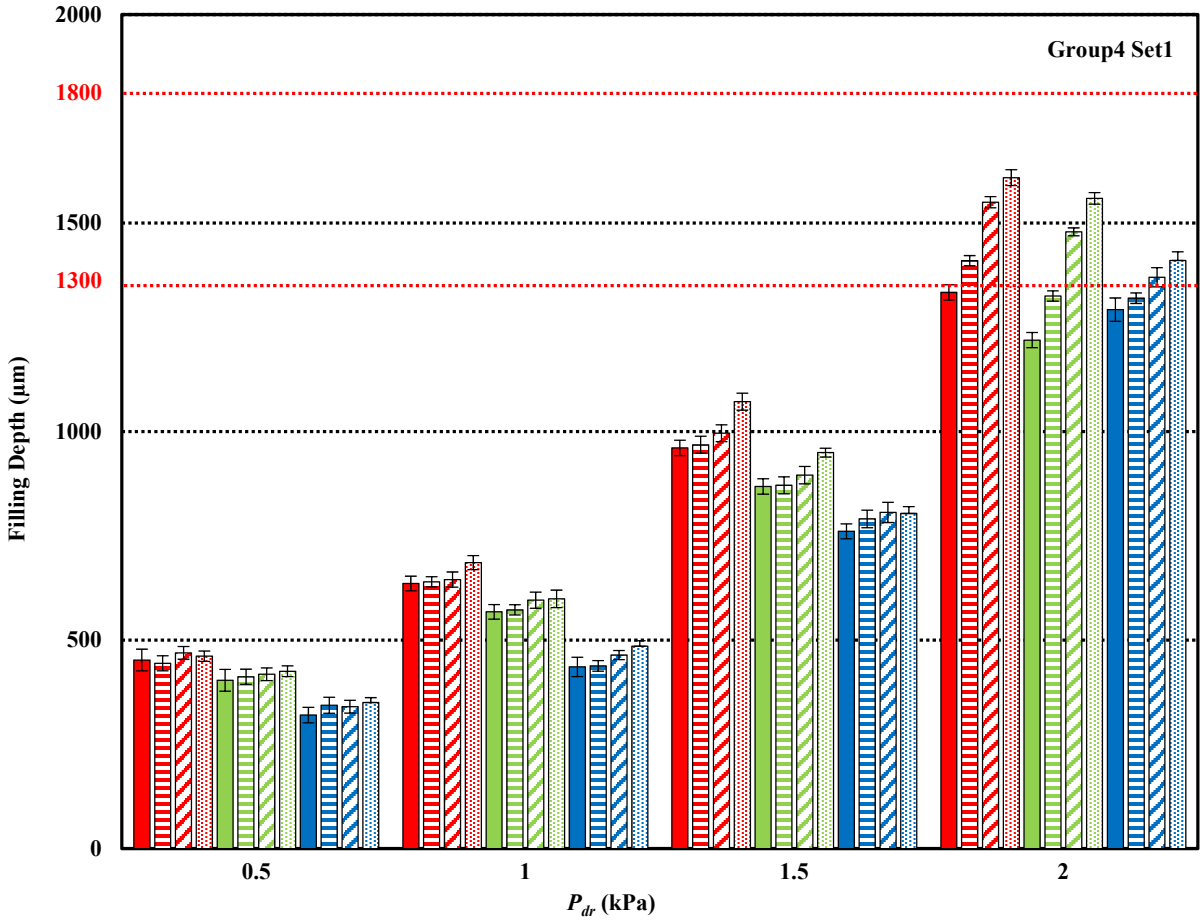

Figure 4.12 The filling result of all channels from Group4 in Set1 (via diameter of 100 μm) under different combinations of driving pressure and feeding time.

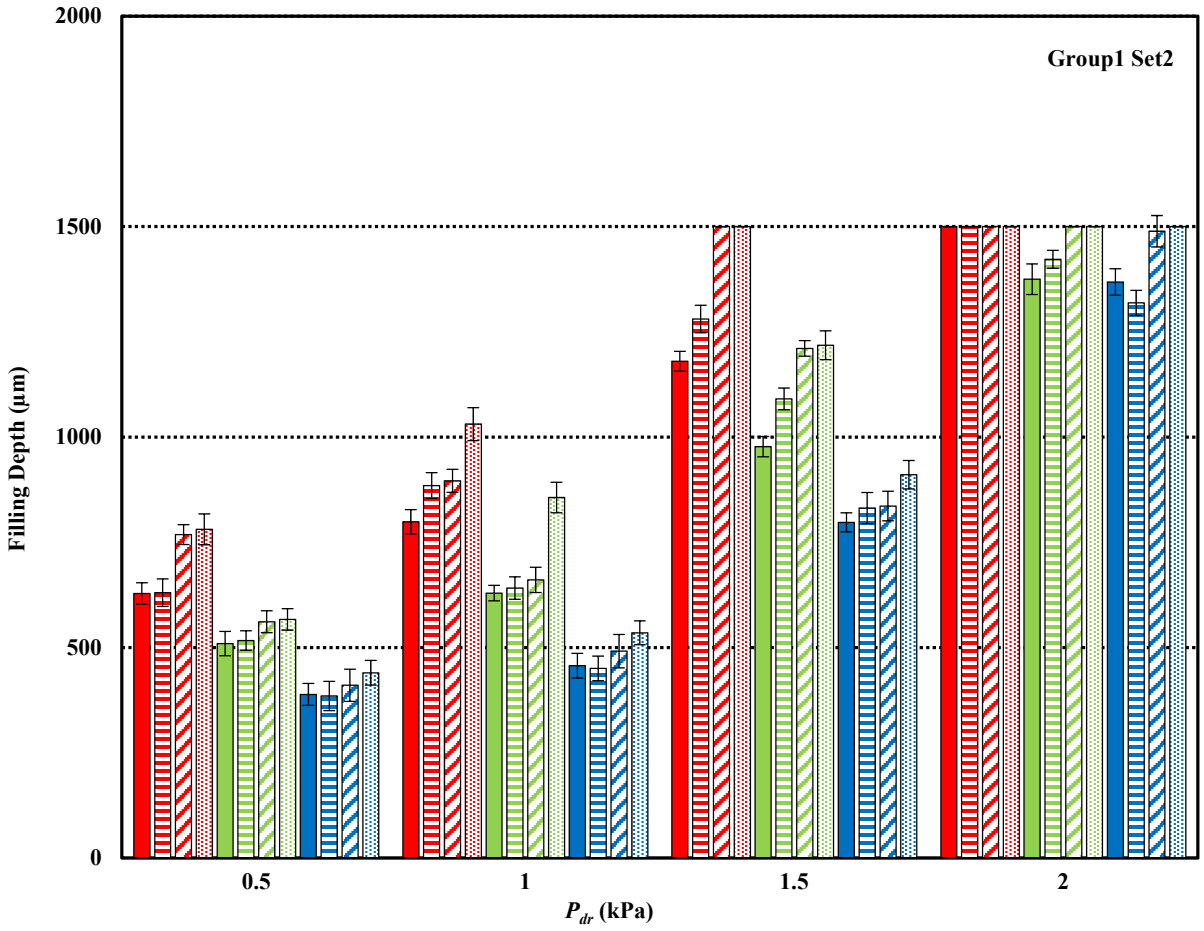

Figure 4.13 The filling result of all channels from Group1 in Set2 (via diameter of 150 μm) under different combinations of driving pressure and feeding time.

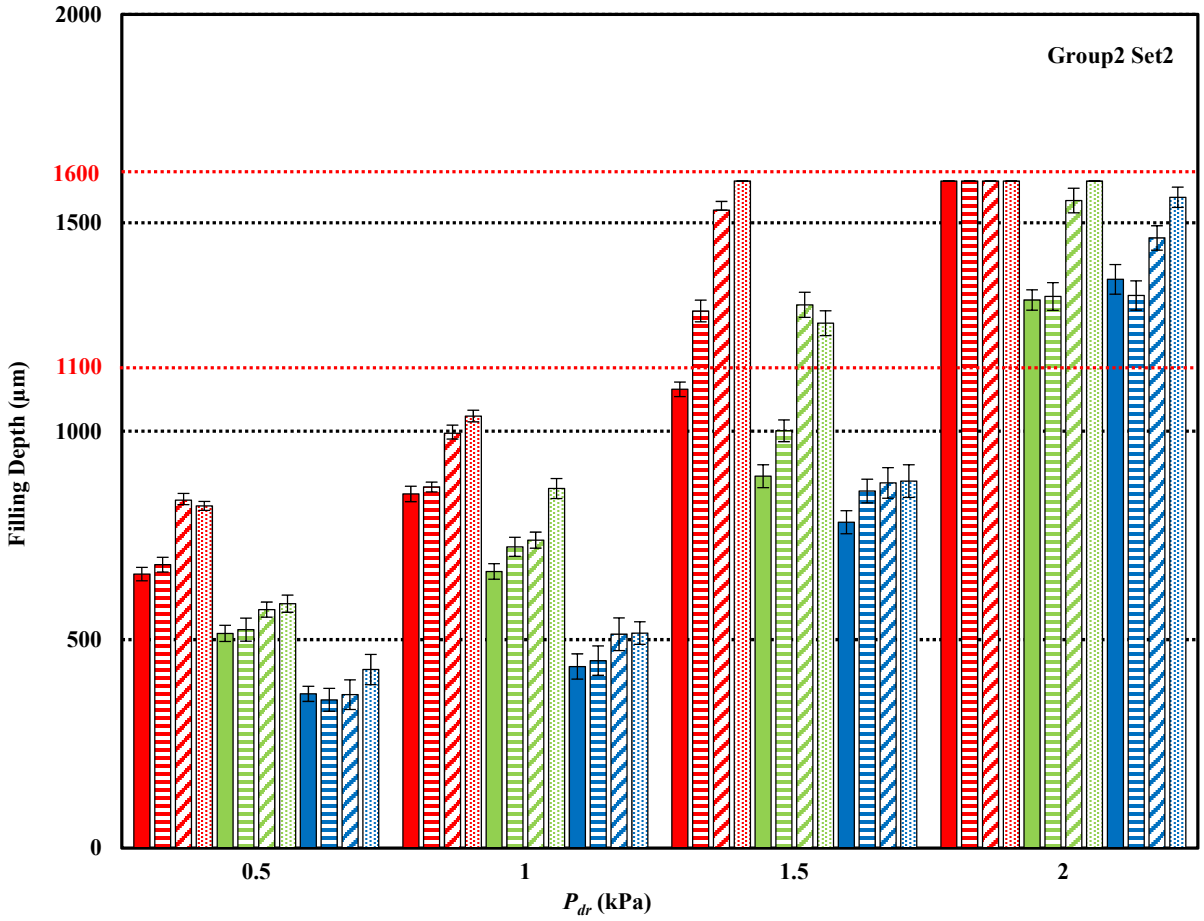

Figure 4.14 The filling result of all channels from Group2 in Set2 (via diameter of 150 μm) under different combinations of driving pressure and feeding time.

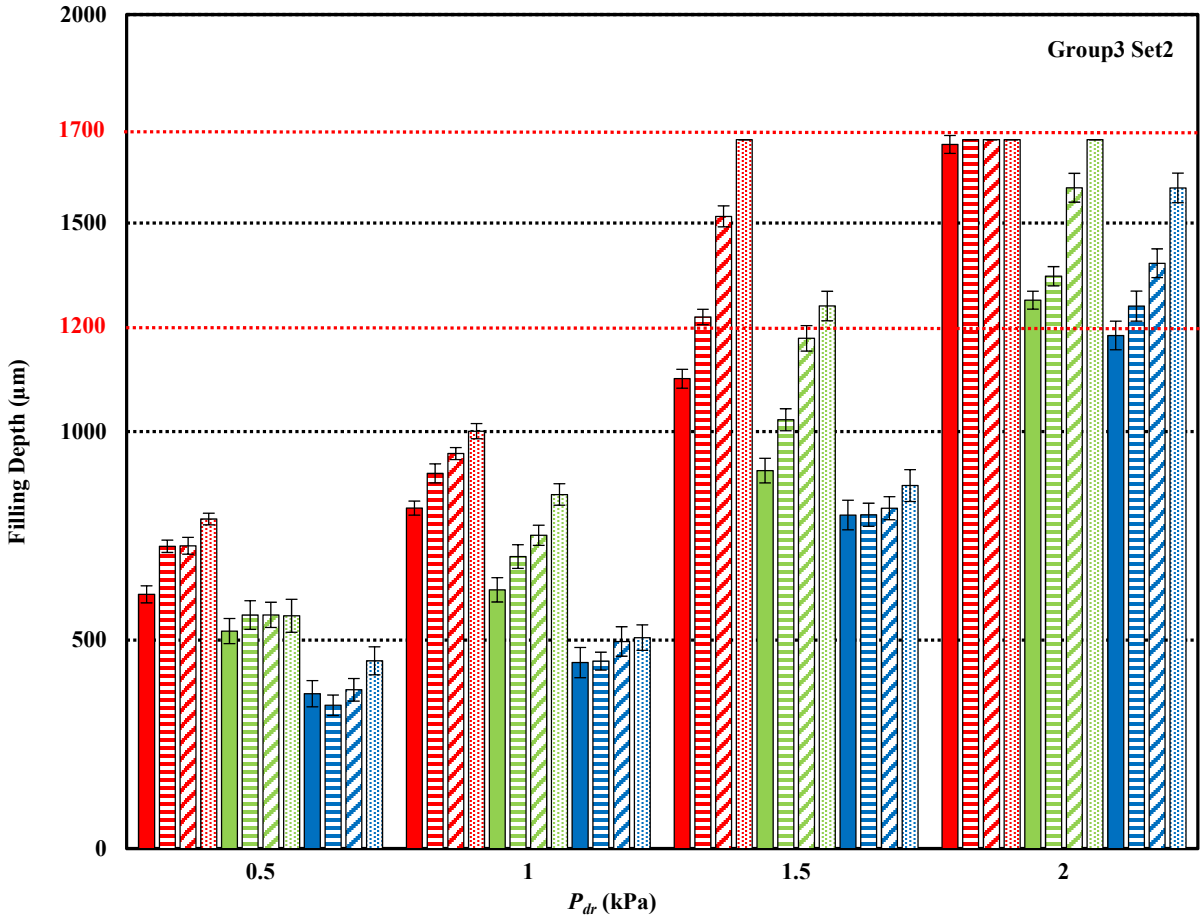

Figure 4.15 The filling result of all channels from Group3 in Set2 (via diameter of 150 μm) under different combinations of driving pressure and feeding time.

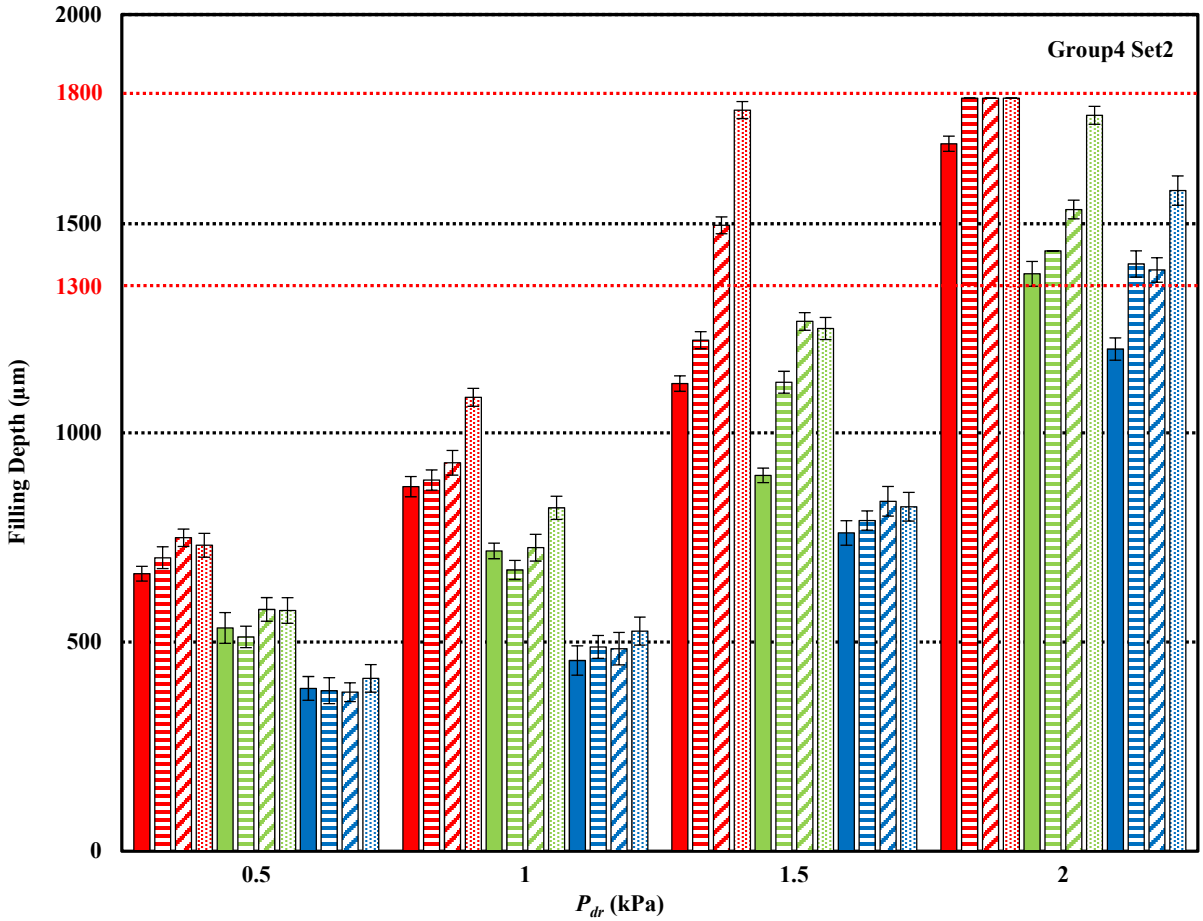

Figure 4.16 The filling result of all channels from Group4 in Set2 (via diameter of 150 μm) under different combinations of driving pressure and feeding time.

4.3.2 Resistance

Because the via opening in this work is too small to accommodate two probes, there is no choice but to choose the 2-point probe again. The resistance measuring process is demonstrated in Figure 4.17.

1) First, enough conductive polymers need to be poured on the top to cover all four vias. 10 kPa of pressure difference is used then to make sure the full filling can be achieved. As long as enough conductive polymers appear on the back, the suction operation will be stopped.

2) All stacks are cured in the environment chamber full of N_2 gas at 120 °C for 30 mins to obtain the 100% polymerization.

3) Both sides are scratched manually by a sharp blade to remove the overburden; then the DI water is used to flush the residual.

4) Two adjacent channels are connected by the same conductive polymer squeezed out from a fine syringe. The same curing process is repeated to cure the link part afterwards.

5) A multimeter (Keithley 2400 Digital Sourcemeter) is used to measure the middle part's resistance R_{mid}. Once it is completed, the stack is flipped over.

6) The multimeter is used again to obtain the overall resistance R_{oa}.

By ignoring the contact resistance between the probes and channels, the relationship among R_{oa}, R_{mid} and the channel's resistance R_{ch} could be governed by

$$R_{ch} = (R_{oa}-R_{mid})/2. \tag{4.1}$$

When the structure is made of one material and has a uniform cross section, its theoretical volume resistance can be defined by Pouillet's law

$$R = \rho \times L/A, \tag{4.2}$$

R is the volume resistance, ρ represents the volume resistivity, L and A stand for the length along the current flow and the related cross section area [140]. In this case, one channel is made up of three components in terms of two vias and one trench, whose lengths and cross section areas might be different, so the calculation should be correspondingly divided into three parts; but the volume resistivity is fixed since it is dependent on the filling material.

15 pairs of channels have been chained and measured for each dimension. Their theoretical (Thr), averaged (Ave), standard deviation (SD) values are shown in Table 4.3 and Table 4.4. Basically, no matter which filling material is used, the measurement displays an upward trend during the length growth in both sets. The average resistances of M1and M2 filled channels in set1 are close, both of them are in the range of 35 Ω to 55 Ω. If the via diameter expands to 150 μm, they reduce into 30 Ω to 40 Ω. If M3 is used, the minimum average value which is obtained from group1 in set 2 would be 29.68 kΩ. Typically, the resistance of fully filled TSVs vary from 0.02 Ω to 350 Ω [162-164], thus this C-based filling material might not be ideal for chips which are sensitive to the power consumption and the heat dissipation.

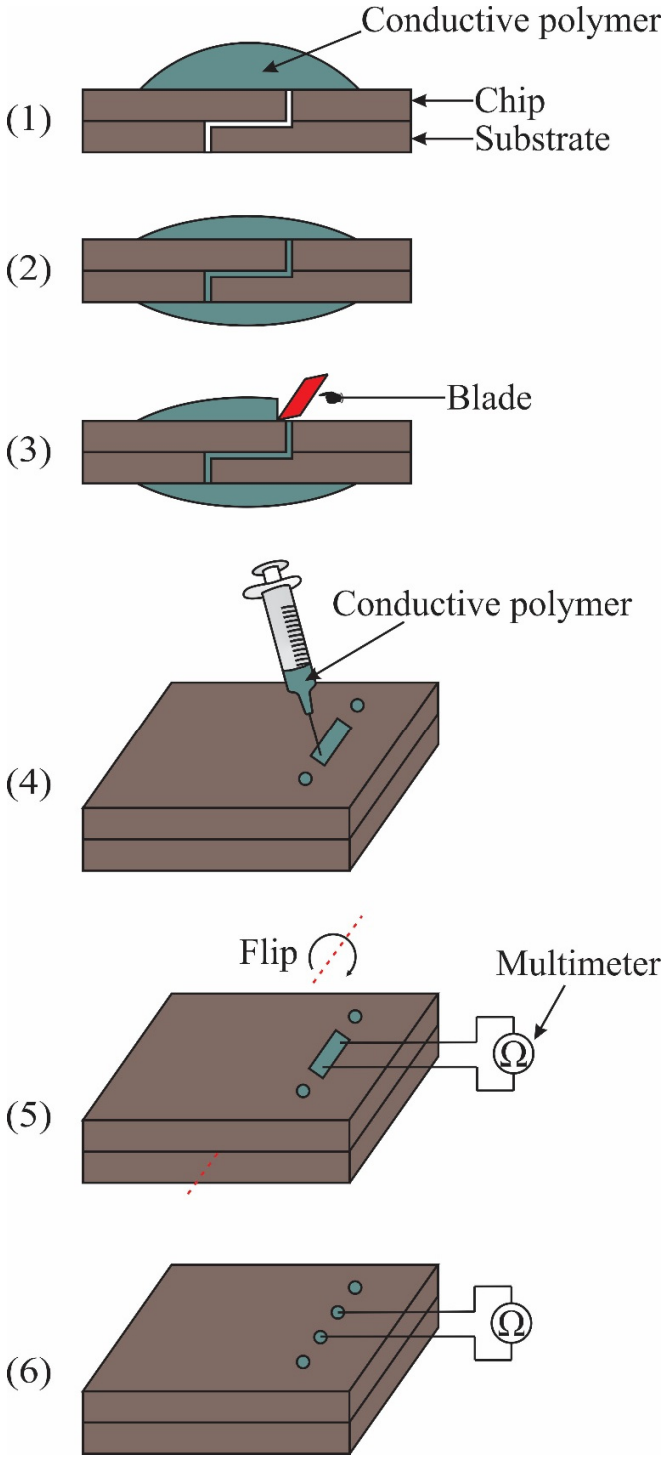

Figure 4.17 A schematic demonstrate of the efficient way to measure the channel resistance. Two adjacent channels are connected using the same conductive polymer. (1)-(3) Fully fill the channel and remove the excessive material on both sides. (3) Connect two channels. (4) First measurement. (5) Second measurement.

Table 4.3 A summary of theoretical, averaged and standard deviation values for channels in Set1.

Group	M1 (Ω)			M2 (Ω)			M3 (kΩ)		
	Thr	Ave	SD	Thr	Ave	SD	Thr	Ave	SD
1	11.08	45.14	8.95	13.30	47.36	19.22	8.87	46.56	10.21
2	11.71	41.55	12.72	14.05	46.01	14.53	9.36	47.67	22.48
3	12.33	49.74	26.31	14.80	49.67	17.63	9.87	65.72	20.25
4	12.96	55.70	25.94	15.55	53.14	15.26	10.37	79.79	31.34

Table 4.4 A summary of theoretical, averaged and standard deviation values for channels in Set2.

Group	M1 (Ω)			M2 (Ω)			M3 (kΩ)		
	Thr	Ave	SD	Thr	Ave	SD	Thr	Ave	SD
1	4.92	29.36	17.21	5.91	30.12	9.08	3.94	29.68	9.61
2	5.20	32.14	23.32	6.24	29.17	10.53	4.16	36.56	16.01
3	5.48	38.33	15.39	6.58	37.66	11.85	4.39	45.43	15.70
4	5.76	39.54	18.55	6.91	37.05	11.42	4.61	44.12	16.59

In theory, the channel resistance should be proportional to its length; whilst occasionally reversed outcomes appear. As explained before, the nonuniformity in the structure and filling material is supposed to be responsible for that. Additionally, it is worth mentioning that there is a noticeable gap between the theoretical and measured resistances. In fact, such phenomenon can also be found in the applications of many conductive polymers [101-103]. The reason is their resistivities are that usually characterized under an ideal condition (in terms of humidity, temperature, measuring equip, *etc.*) which can barely be maintained during the practical utilization.

4.3.3 Connection Stability

For all three filling materials, the information on their resistivity thermal stability and bonding strength to metal materials is not specified. Thus, the relevant investigation is necessary. Here to perform resistance thermal stability test, stacks are placed on a hotplate (Fisher Scientific™ Isotemp™) and their overall resistance at different temperatures are measured using the 2-point probe. Then, a metal layer (both Cu and Al are tested in this case) with thickness of 1 μm is sputtered on the unchained side, followed by another 2-point probing process to measure the new

overall resistance. As has been discussed in Section 3.3.3, the metal layer and underneath channels form a series circuit; as the metal layer has rather negligible volume resistance, any increases in the overall resistance would be only resulted from the adhesion defect(in terms of interfacial disconnection and contact resistance), metal oxidation, cleanliness, *etc.* Thus, no obvious changes would be an efficient indicator of good adhesion quality.

Only M1 and M2 are tested in this section because of their better electrical performance. The highest temperature is set to 150 °C. At each observing point, the temperature should be sustained long enough (1 min would be enough based on our observation) to receive the full synchronization. For each filling material, two stacks (overall resistances are noted as R_1 and R_2) are randomly chosen for the deposition of Cu and Al (new overall resistances are noted as R_{cu} and R_{al}). In Figure 4.18, although the two stacks filled with M1 establish a difference in the overall resistance at the beginning, none of them has experienced any changes that are more than 10% during the temperature increase, therefore it is reasonable to conclude this material's resistivity is thermally stable. After the Cu or Al layer is included in the second measurement, what could be observed is a low degree of change (less than 5%). This outcome indirectly discovers that an acceptable adhesion has been established. Figure 4.19 presents the result obtained from M2. It is clear neither the temperature increase nor the addition of metal layer has a recognizable effect on the overall resistance, so the same conclusions could be drawn.

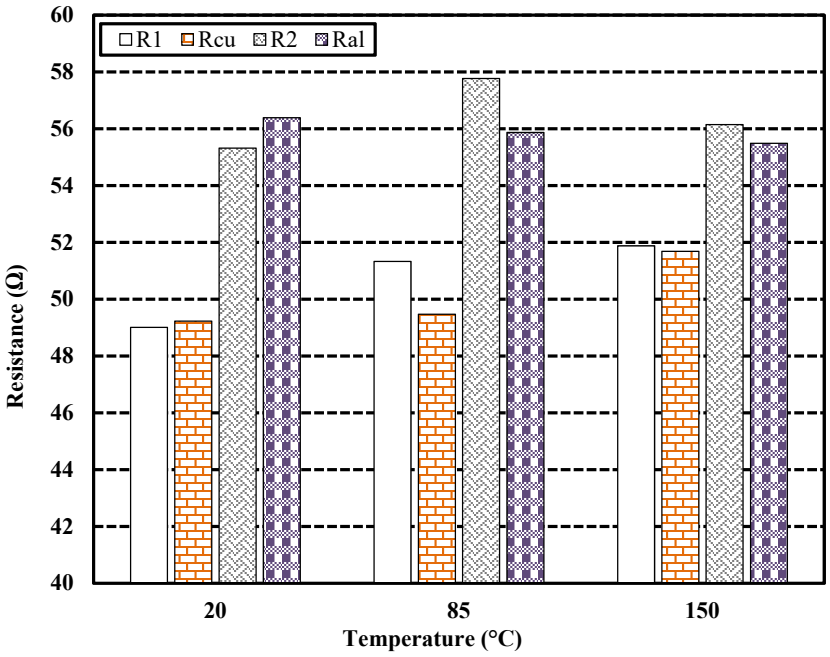

Figure 4.18 The total resistance of two channels filled with M1 measured at different temperatures with and without the metal layer.

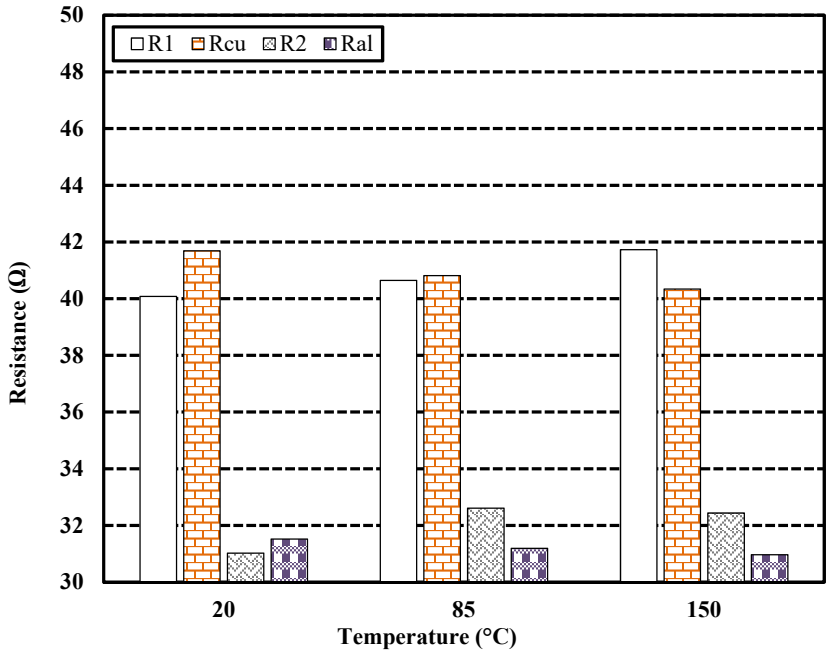

Figure 4.19 The total resistance of two channels filled with M2 measured at different temperatures with and without the metal layer.

4.4 Conclusion

A novel silicon interposer based on embedded trenches is successfully built for 3D integration. Instead of traditional electroplated Cu, Ag-based and C-based conductive polymers are employed to metallize these trenches along with multiple layers of TSVs in order to accelerate the metallization process and enhance the electrical connection quality at the bonding interface. Varying channel cross sections and lengths are investigated under different driving pressures and durations. It is found that a higher filling ratio would be easier to obtain when the stronger driving pressure instead of the longer feeding time is applied. The resistance of Ag-based conductive polymers filled channels is between 30 Ω and 55 Ω, suggesting they are more ideal for the electrical connection that needs low power demand and good heat dissipation. Also, their resistivity stability and bonding strength to Cu and Al are proven to be promising during the temperature increase from 20 °C to 150 °C.

"The measure of a man is what he does with power."

-- Plato

Chapter 5: Single-Layer Ridge SIW Filter

The idea of utilizing vacuum driven conductive polymer to fill through via structures is applied to the fast and simple fabrication of substrate integrated waveguide (SIW) devices. The metallization level in a diversity of vias is studied. Based on that, two single-layer ridge SIW filters are fabricated on a self-made flexible substrate of PDMS and a standard commercial rigid laminate respectively. Performance tests are carried out under different deformations.

5.1 Introduction

Thanks to their capability of integrating different types of passive and active components into a reasonably small and planar piece, SIWs have been regarded as a promising candidate for the research and development (R&D) of modern RF (especially microwave and millimeter-wave) systems [165-168]. Typically, a SIW device can be fabricated by embedding two rows of conducting posts or slots (electric sidewalls or fences) into a dielectric substrate with each side covered by a metallic barrier layer [169], as shown in Figure 5.1. The structure design along with fabrication process of a SIW device is similar to that of many Si-based devices that have been mentioned in Section 1.1, except that the substrate is usually polymer-based or ceramic-based.

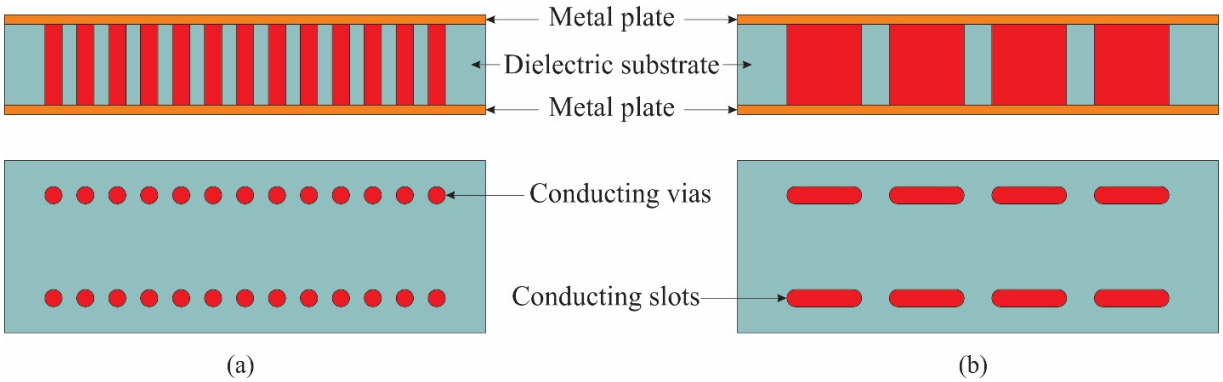

Figure 5.1 A schematic demonstration of two typical SIWs. (a) Electric sidewalls are made up of via arrays. (b) Electric sidewalls are made up of slot arrays.

Currently, a great portion of attention in this field is paid to how to optimize the design to obtain better structural compactness and enhanced performance. Thus, a variety of topologies including folded [170-172], half-mode [173-175], dielectric-loaded [176], ridged [177-179] and their derivations [180, 181], have been developed, as shown in Figure 5.2.

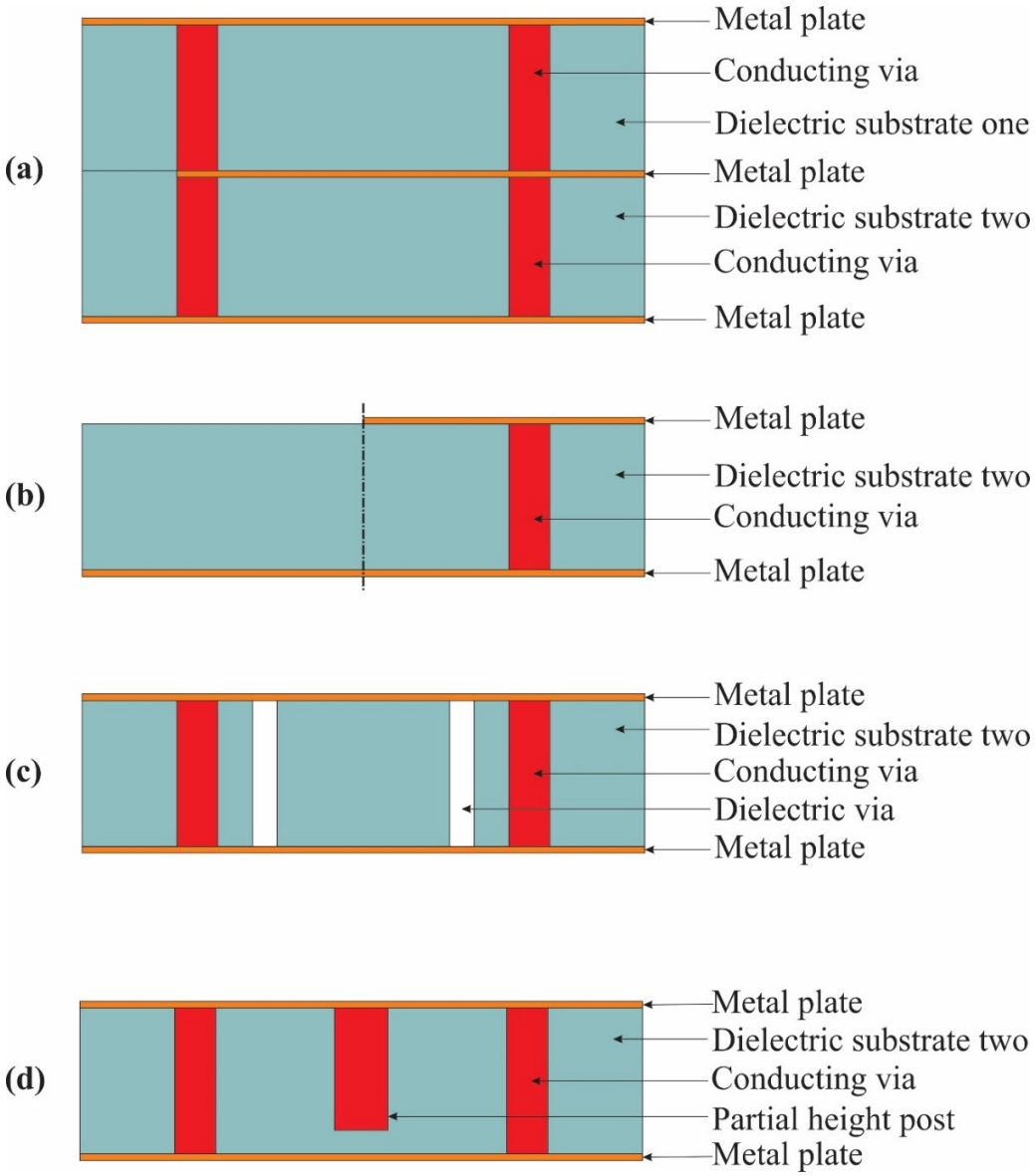

Figure 5.2 A schematic demonstration of four topographies of SIW. (a) Folded SIW. (b) Half-mode SIW. (c) Dielectric loaded SIW. (d) Ridged SIW.

Compared with the design process in terms of model build-up, material selection, characterization, *etc.*, which have already been improved by adequate commercial general-purpose software and semi-empirical equations [182-186], one fact on the fabrication side has barely been revealed in literature is that, Cu electroplating, the most frequently used approach for the metallization of via arrays and other tuning components, is problematic [187, 188]. First, all Cu

materials appear in the vias intrinsically come from the transportation and deposition of a large number individual Cu ions, so typically the plating process takes more than for 2 h (the seed deposition process is taken into consideration) [81]. Second, intrinsically the transportation of Cu ions is dependent on the electrical field that is formed between the target substrate (cathode) and Cu resource (anode). However, the gradient of electrical field and plating solution inevitably exist in the via, which makes Cu ions settle down around the neck more quickly than the bottom, this means the via might have been closed before it is totally filled, i.e. internal void [189]. When the via's aspect ratio goes higher (or different aspect ratios appear on one substrate), the internal void is more likely to occur. Third, chemical additives can be added to the electrolyte to address these problems, but the process complexity will increase. Fourth, the copper sulfate, sulfuric acid, chloride ions other organic elements contained in the electrolyte may result in severe environmental hazards [92, 93].

In this chapter, an innovate approach for SIW metallization is proposed based on the previous two chapters. More specifically, all conducting components including vias and resonator(s) in SIWs are filled by vacuum driven conductive polymers instead of electroplated Cu, hence the metallization process could be simplified and shortened. More interestingly and meaningfully, the via metallization level becomes adjustable through the precise control of the vacuum level and the lasting period. As a proof of concept, two prototypes of band-stop ridge SIW filter are designed, fabricated and tested.

5.2 Rigid SIW Filter

5.2.1 Rigid SIW Filter Design

As one of the key building blocks in modern communication systems, band-stop filter plays a major role of rejecting the unwanted signals and passing the desired signals [190, 191]. To explain this SIW metallization method and fully demonstrate its capability in terms of post diameter and height and substrate material, two partial height post band-stop SIW filters are developed. The first one is in a self-made flexible substrate made of PDMS (Sylgard® 184, Dow Corning Corp., permittivity ε_r=2.9, loss tangent $tan\delta$=0.0074) and works at 15 GHz with bandwidth of 1 GHz; the second one is in a standard rigid laminate RO4003C (Rogers Corp., ε_r=3.38, $tan\delta$=0.0021~0.0027)

and its central frequency is 10.5 GHz with bandwidth of 1 GHz. To the best of our knowledge, the partial height structure is usually formed by vertically bonding the main substrate to at least one extra substrate [192-194], as shown in Figure 5.3. Aside from the issues caused by the employment of Cu electroplating, one obvious downside is that the design of the partial height post cannot be purely performance oriented, because its height is confined by the main substrate's thickness. Worse, such multi-layer configuration is not ideal for flexible devices, as the mechanical or electrical connection at the bonding interface might not survive when they conform to an irregular surface.

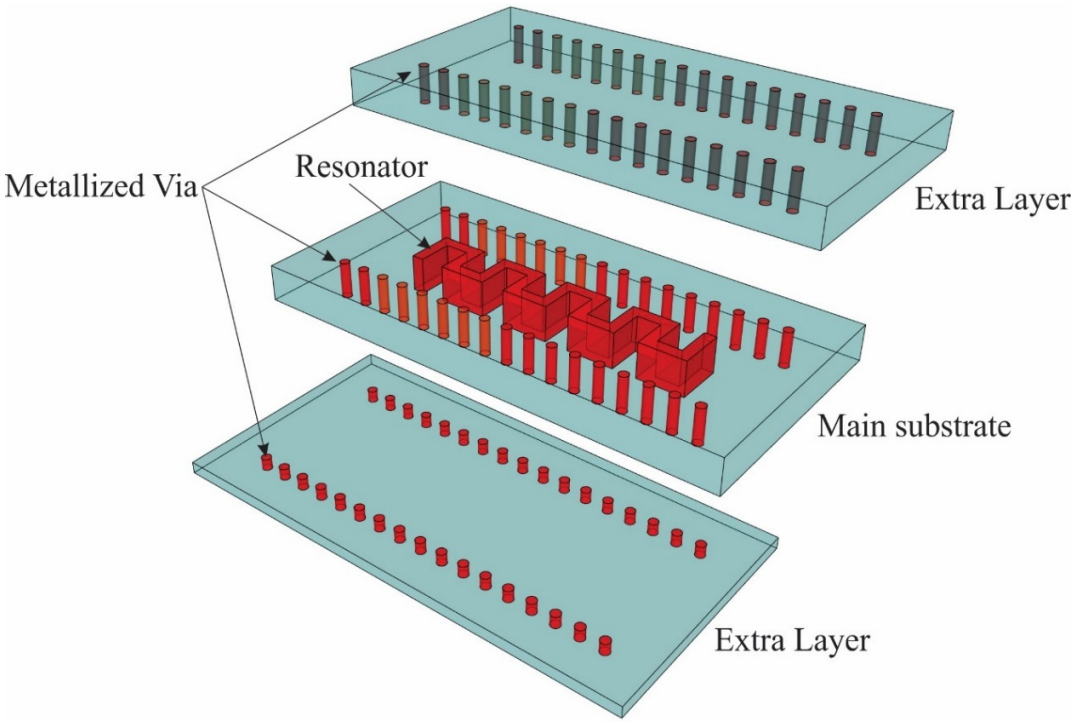

Figure 5.3 A view of a typical ridge SIW. The ridge scenario is created by the stacking of multiple layers. The resonator is only fabricated in the main substrate.

But under the circumstance that the conductive polymer's viscosity is in a suitable range, through the precise adjustment of the vacuum level and its lasting duration, we find the via' metallization depth could be controlled; hence both filters are able to have a single-layer configuration. Figure 5.4(a) and Figure 5.4(b) display the basic design from difference angles.

Although differences in mechanical and electrical properties of these two substrates exist, the corresponding filters share a similar design. In both substrates, two rows of full height small posts spread along the length and one big partial height post, i.e. the ridge-like resonator, is offset from the center. In theory, the resonant frequency of this type of filters is primarily determined by the partial height; however, it may be affected as well by the post's offset respect to the center of SIW, because it is able to adjust the coupling strength. Once the metallization is completed in the flexible substrate, its bottom will be covered by a cross like barrier layer made of Cu (for the shielding purpose) and its top will be totally shielded. For the rigid substrate, these two barrier layers need to be switched according to our simulation results. All geometric information is summarized in Table 5.2 and Table 5.2.

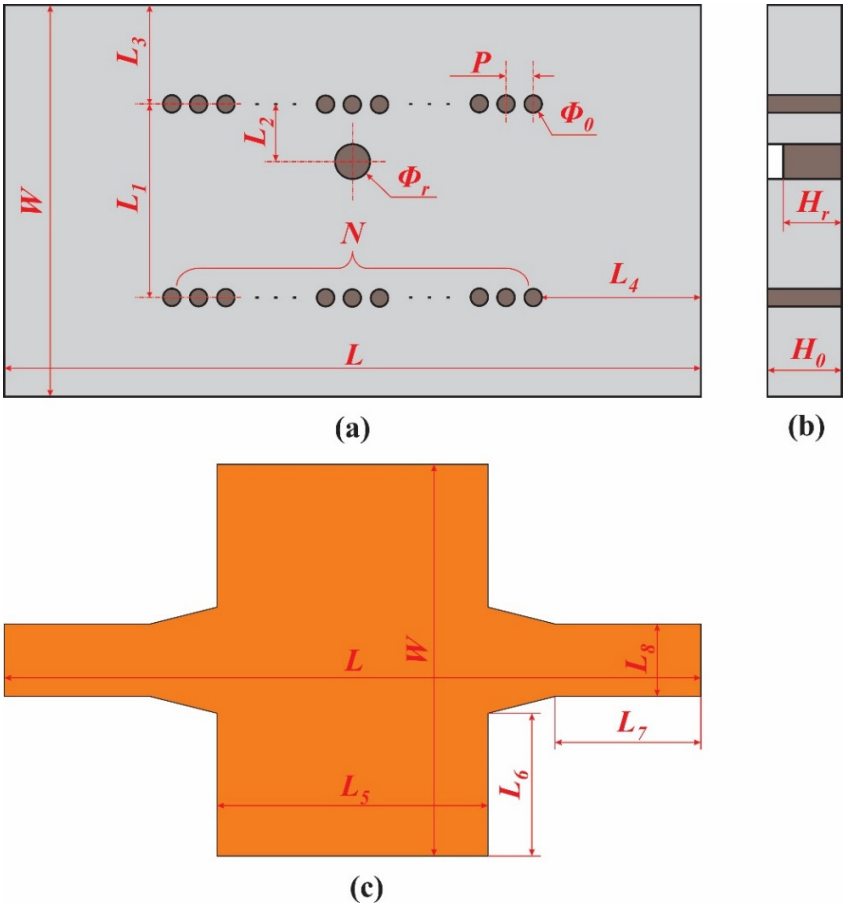

Figure 5.4 Basic design of ridge SIW filter. (a) Front view of the substrate. (b) Left view of the substrate. (c) Cross-like barrier layer.

Table 5.1 Dimensional information on single layer ridge SIW filters (unit is mm).

Substrate	L	W	H_0	L_1	L_2	L_3	L_4	L_5	L_6
Sylgard® 184	30	19	1	11.2	2	3.9	15	10	10
RO4003C	35	21	1.52	13.5	1.75	3.75	17.5	10	15

Table 5.2 Dimensional information on single layer ridge SIW filters (continued).

Substrate	L_7	L_8	L_9	Φ_0	Φ_r	H_r	N	P
Sylgard® 184	6.85	7	2.7	0.4	0.8	0.80	17	0.6
RO4003C	7.8	5.5	3.4	0.5	1	1.4	20	0.75

5.2.2 Conductive Polymer Selection

Even though sometimes chemical reactions may be involved, a vast number of conductive polymer composites on the market are manufactured through the physical mixing of conductive fillers with host polymer (which is typically nonconductive but can be intrinsically conductive in some cases). We investigate nearly a hundred of commercial products and summarize their conductivities and relevant applications in Table 5.3. It might be necessary to clarify that we create this table based on the data sheets that we receive from the manufacturer or we find on the Internet. Moreover, it is not practical to go through all commercial conductive polymers, so the list is not exhaustive. We find different kinds of carbon particles especially single wall or multi wall carbon nanotubes, graphene, *etc.* have been intensively used due to their high compatibility and low price [195-198]. However, their extreme agglomeration behavior might result in overly high resistivity (higher than 10^2 Ω·cm) and viscosity (higher than 300 Pa·s) [199, 200]. On the contrary, a smaller quantity of metal materials, especially Ag spheres, flakes and salts are adequate to equip the final mixture with higher conductivity thanks to their high conductivity nature.

The function of sidewalls in SIW devices is to shoulder the current or wave transmission. Thus, first of all, the metallization material is supposed to possess enough electrical conductivity. In addition, a proper viscosity is another important condition that should be fulfilled. Because the

suction effect applied to the substrate has to increase when it is too viscous, which should be avoided for the substrate protection purpose; on the other hand, as long as it is not thick enough to minimize the free falling caused by the gravity force, the partial height metallization will be less achievable or even disappear. In this part, a silver-graphene doped epoxy (Table 5.4) is chosen as the metallization material. Thanks to their geometric difference, graphene particles are able to embed into the voids among silver particles, creating extra electrical paths. Compared with the pure graphene doped polymers that have the equivalent conductivity, the amount of graphene particles in this case can be reduced.

Table 5.3 A brief summary of conductivity and application of different materials.

Application	**Resistivity (Ω·cm)**
Insulating materials	$\infty \sim 1\times10^{10}$
Semiconducting materials, paper, textiles, household appliance shells	$1\times10^{10} \sim 5\times10^{6}$
Antistatic coating and films	$5\times10^{6} \sim 1\times10^{4}$
Some conductive thin films and elastic electrodes	$1\times10^{4} \sim 1\times10^{1}$
Thermal interface and electromagnetic shielding materials	$5\times10^{1} \sim 6.5\times10^{-2}$
Conductive polymer based on carbon	$1.5\times10^{0} \sim 1\times10^{-2}$
Conductive inks, adhesive and coatings based on Ag	$6\times10^{-3} \sim 2\times10^{-4}$
Conductive polymer based on Ag	1×10-3 ~ 1×10-5

Table 5.4 Several parameters of the conductive polymer used for ridge SIW filter metallization.

Name	**Filler**	**Host**	**Viscosity**	**Conductivity**	**Appearance**
G6E-SG	Graphene and Silver	Epoxy	110~120 Pa·s	1×10^{-4} Ω·cm	Two-component smooth paste

5.2.3 Vacuum Suction Platform Buildup

The same vacuum suction platform that has been mentioned in Section 3.2.2 is used again to conduct the suction operation. In order to assure that there is no air leakage, a rubber layer is

adhered to the top of the suction head. It should be mentioned is that only for the flexible SIW filter, a rigid supportive substrate made of acrylic (McMaster-Carr®) with the same via distribution but larger (20%) diameter will be placed underneath to prevent it from collapse during the suction process. A schematic demonstration in Figure 5.5 can well describe this situation. The pressure applied to the topside is consistently equivalent to the atmospheric pressure P_a (~101 kPa) and the backside pressure P_b is reduced by the dispenser, the pressure difference between them is exactly the driving pressure P_{dr} that sucks the metallization material into the vias. Their relation can be governed by

$$P_{dr}=P_a-P_b. \tag{5.1}$$

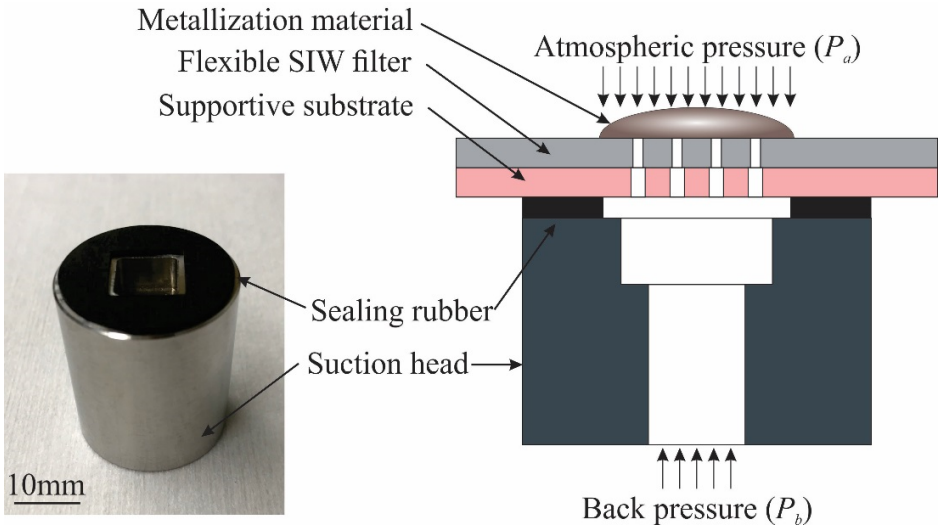

Figure 5.5 A demonstration of the customized vacuum suction head.

5.2.4 Filter Fabrication in Flexible Substrate

Figure 5.6 schematically describes the flexible filter's fabrication process. Here the classical Sylgard® 184 is used to fabricate the flexible substrate, because it is important to outline a universal fabrication process for such kind of flexible SIW devices.

1) PDMS substrate fabrication. To our best knowledge, the thickness of 1 mm is far beyond the limit of spin-coating process, so the classical casting idea is used. First,

PDMS prepolymer and cure agent are weighed (wt % 10:1) and mixed by stirring for 5 mins. Second, the above-configured precursor is stored in a vacuum chamber for degas at room temperature for 30 mins until all air bubbles are removed. Third, the precursor is poured on a 1-inch thick acrylic sheet (McMaster-Carr®) and compressed by another one with extra weight 5 kg. Four glass slides (Fisher Scientific®,1 mm thick) that have been placed at the interface are supposed to control the final thickness. Last, this whole setup is transferred to an environment chamber and heated at 50 °C for 18 hours. The whole setup is shown in Figure 5.7. This low temperature and longtime curing profile is beneficial to the stress release.

2) Via patterning. A universal vector graphic editing software named CorelDraw® is used to create the filter's outline; then an air-assisted CO_2 laser cutter (Versa Laser®, as shown in Figure 5.8) will read the design file and pattern the substrate accordingly. Several basic settings used for the laser cutting are: mode-vector, power-26%, speed-6% and pixel per inch (PPI)-300, as shown in Figure 5.9. After that, the substrate should be rinsed with acetone, isopropyl alcohol (IPA) and DI water sequentially to remove the residuals.

3) Ridge resonator filling. The substrate will be placed on the vacuum suction platform after enough metallization material is squeezed onto the big via's top out from a fine syringe. We test a set of driving pressures and feeding times to figure out the best combination for the desired partial height. After that, the substrate will be transferred back to the environment chamber and cured at 80 °C for 3 h.

4) Overburden removal. The top is scratched by a sharp blade manually to remove the overburden. Then, the substrate should be rinsed with acetone, IPA and DI water sequentially to remove all residuals.

5) Via array filling. The same via filling process is repeated. Since they are supposed to be metallized entirely, this time there is no need to proceed any tests. A relatively higher driving pressure and longer feeding time can be applied. As long as the metallization material appears on the back, the vacuum suction would be stopped.

6) Overburden removal. This time both top and bottom need to be scratched manually to remove all overburdens.

7) Barrier layer patterning. CorelDraw® is utilized again to create the barrier layers' outline; then they will be patterned out from a commercial Cu foil tape (Kraftex®) on an automatic paper/plastic cutting machine (Silhouette CAMEO®), as shown in Figure 5.10 and Figure 5.11.

8) Final treatment. After the barrier layers are bonded to the surface, the substrate needs to be heated by a hot air blower at 60 °C for 20 s to promote the adhesion.

5.2.5 Filter Fabrication in Rigid Substrate

The fabrication process of the rigid filter is similar to that of the flexible filter, except a certain number of modifications have to be made.

1) The rigid substrate is RO4003C which is purchased from Rogers Corp. directly. Its original barrier layers need to be eliminated by immersing it into the Cu etchant solution (MG Chemicals®) for 1 h at room temperature. After that, the substrate will be rinsed with DI water to remove all residuals.

2) The via pattering is completed on a computer numerical control (CNC) router with fine tooling (diameter of 0.46mm), because the CO_2 laser is not power enough to pattern this kind of ceramic-based substrate.

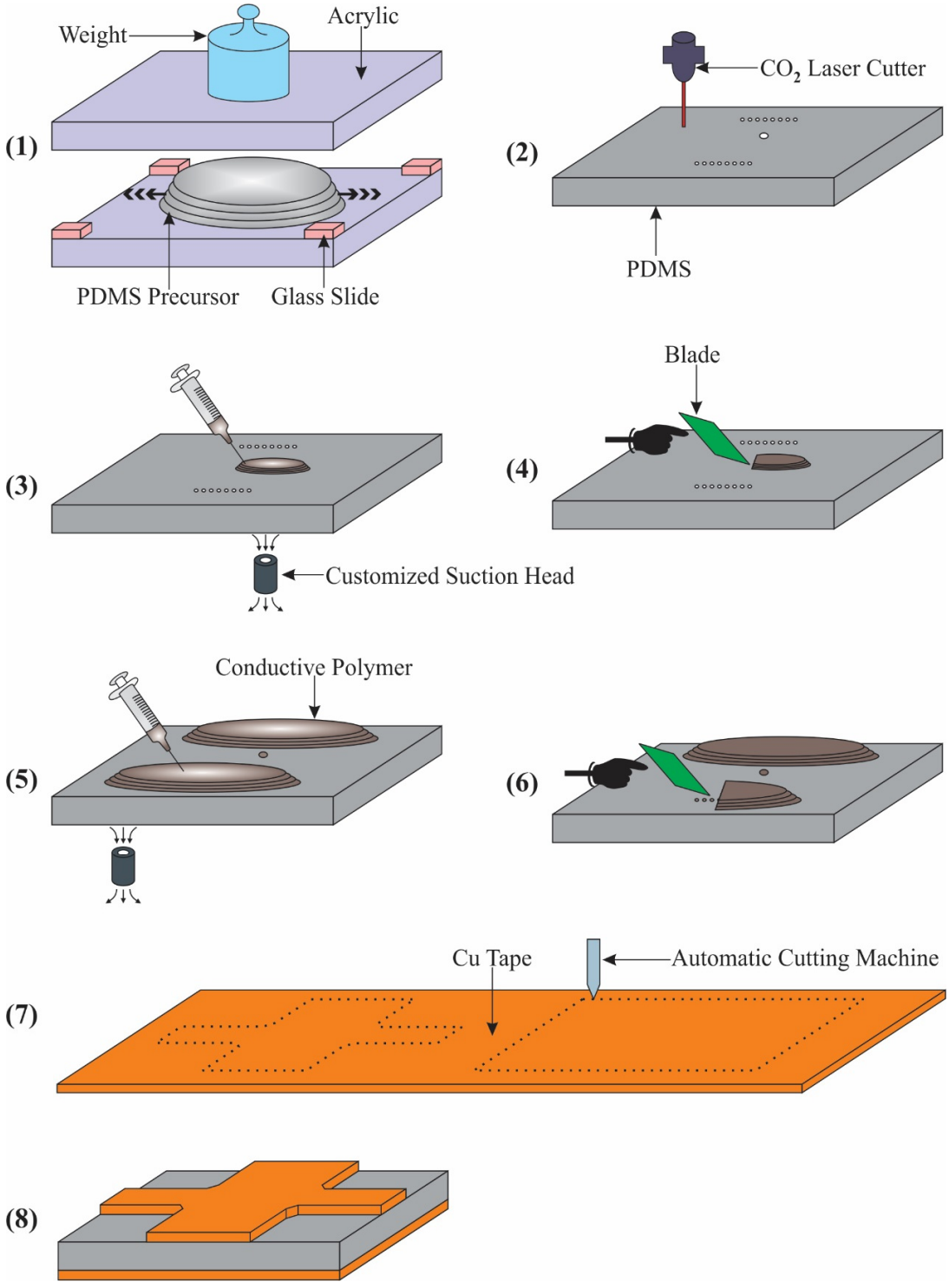

Figure 5.6 A schematic demonstration of the fabrication process of the ridged SIW filter on the single-layer PDMS substrate.

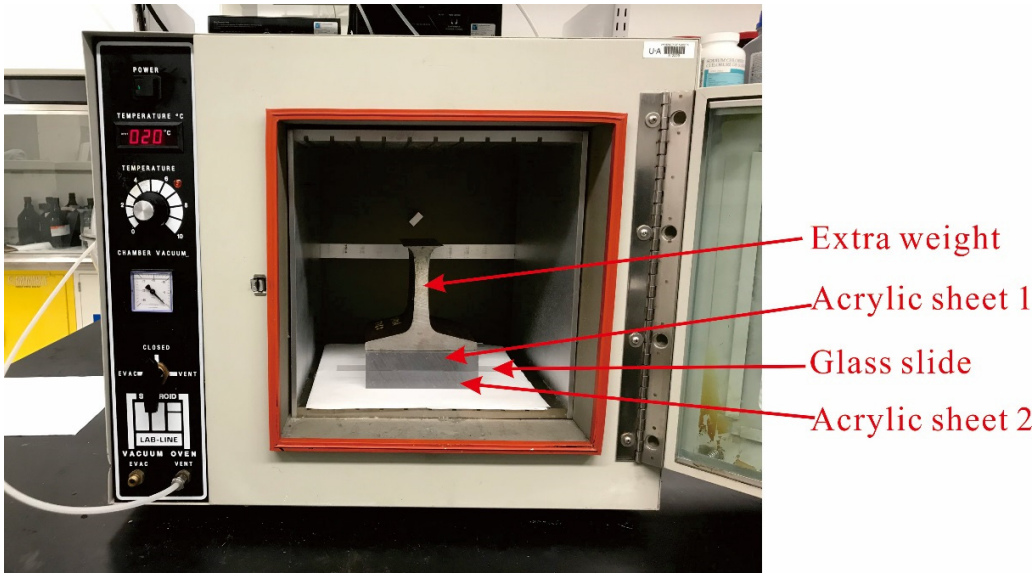

Figure 5.7 An overview of the setup used for the PDMS substrate fabrication. Two acrylic sheets will squeeze the PDMS and its final thickness will be controlled by the glass slide inserted at the interface.

Figure 5.8 An overview of the CO_2 laser cutter used for the via patterning.

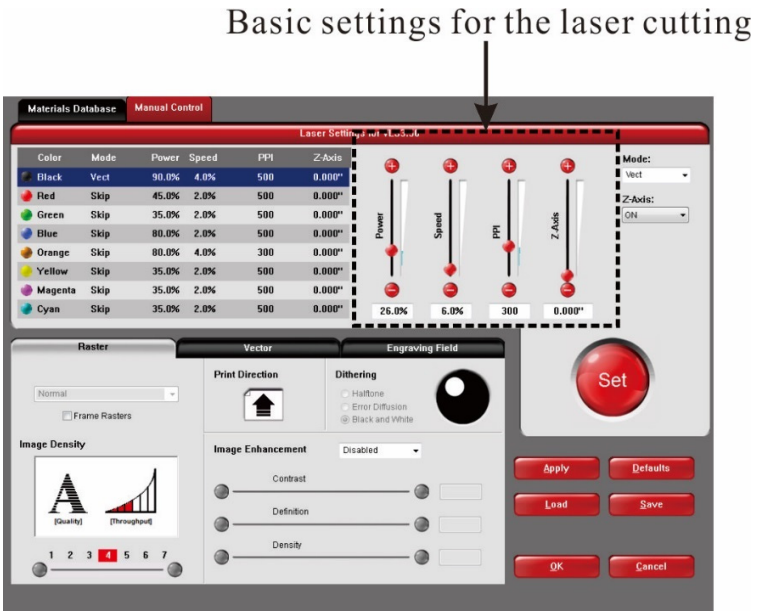

Figure 5.9 The user interface of the laser cutter. Several important settings for the laser are mode-vector, power-26%, speed-6% and PPI-300.

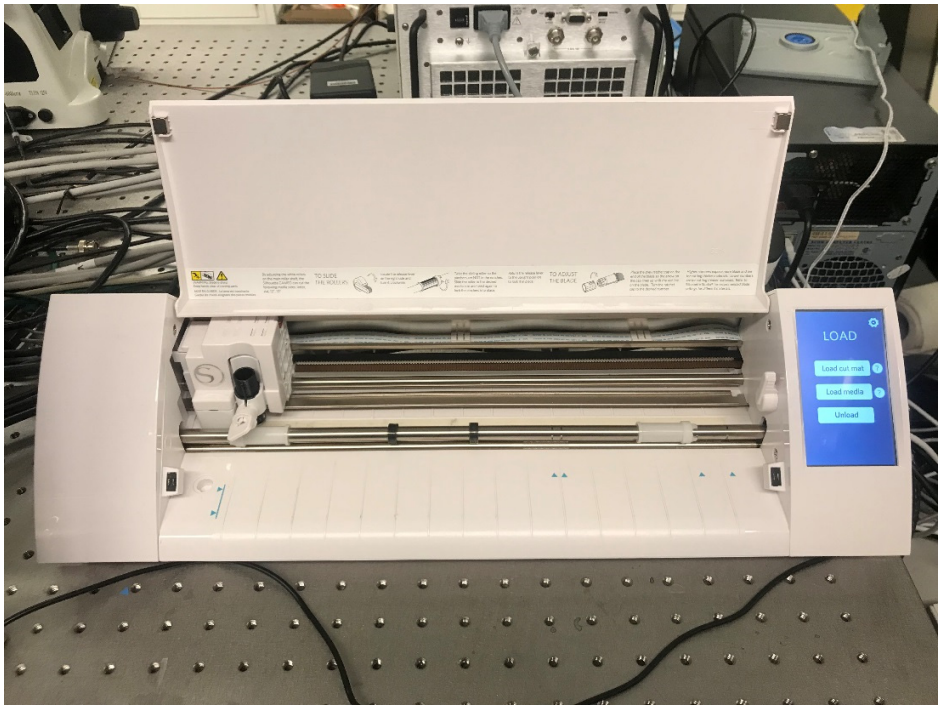

Figure 5.10 The automatic paper/plastic cutting machine.

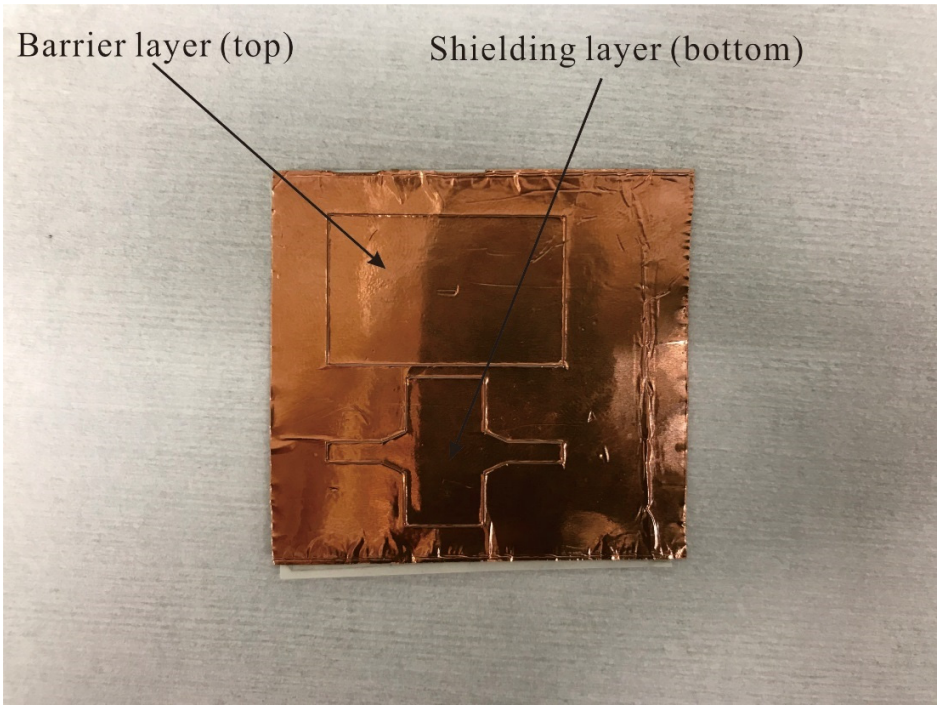

Figure 5.11 A close look at the barrier layers cut out from the Cu foil.

5.3 Characterization

5.3.1 Metallization Level

For the ridge resonator in both substrates, in order to rapidly measure its partial height in the substrate without causing any damage, a two-dimensional surface topography profiler (Alpha-Step® IQ) is employed. As given in Figure 5.12, during the measuring process, a fine detecting probe will be at first placed in zone1, then scratch the surface horizontally (from zone1 to zone3) with an extremely low preload to obtain the step height H_{step}. After that, the partial height H_{part} can be calculated using the equation

$$H_{part}=H_0-H_{step}. \tag{5.2}$$

Figure 5.13 provides a cross section view of the ridge resonator in the rigid substrate. Clearly, no voids can be found in the via. The final results of metallization level have been summarized in

Figure 5.14 to Figure 5.17. A set of colors are applied to differentiate the lasting durations. ON the flexible substrate (1 mm thick), for the vias with diameter of 0.4 mm, 2.5 kPa and 1 s is enough to drive the conductive polymer through them entirely; 0.8 kPa and 1.2 s is suitable to well realize the partial height metallization for the ridge resonator. As the diameter increases to 0.5 mm on the rigid substrate (1.52 mm thick), the vias become easier to fill as the metallization level under the same vacuum condition is constantly higher. Their full metallization asks for 3 kPa and 2 s. A suitable combination for the ridge resonator's metallization is 1.2 kPa and 0.3 s.

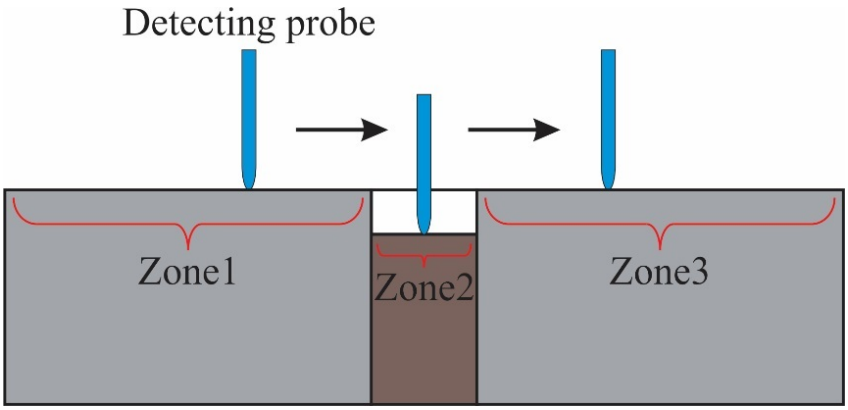

Figure 5.12 A schematic demonstration of the surface probing process. The partial height is calculated based on the height difference among three zones.

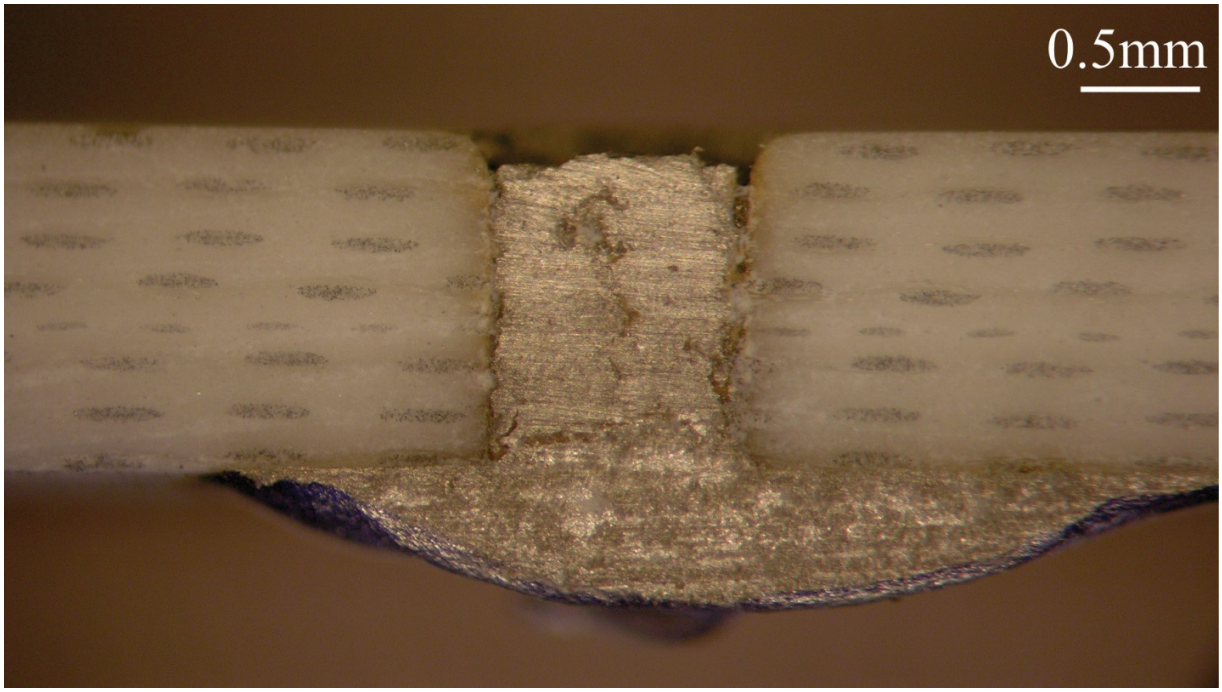

Figure 5.13 A cross section view of the partial height post in the rigid substrate. No obvious voids can be witnessed inside.

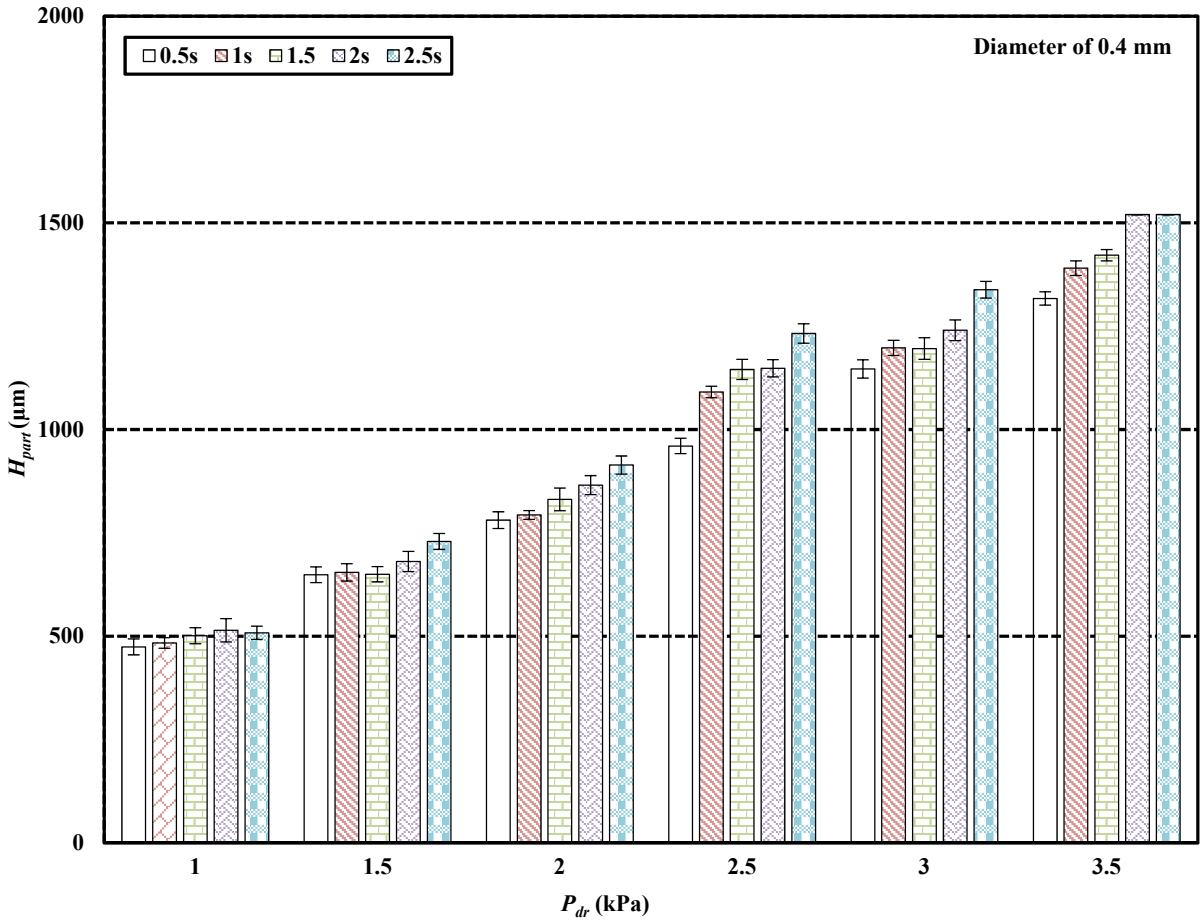

Figure 5.14 The metallization result of the via with diameter of 0.4 mm under different combinations of driving pressure and feeding time.

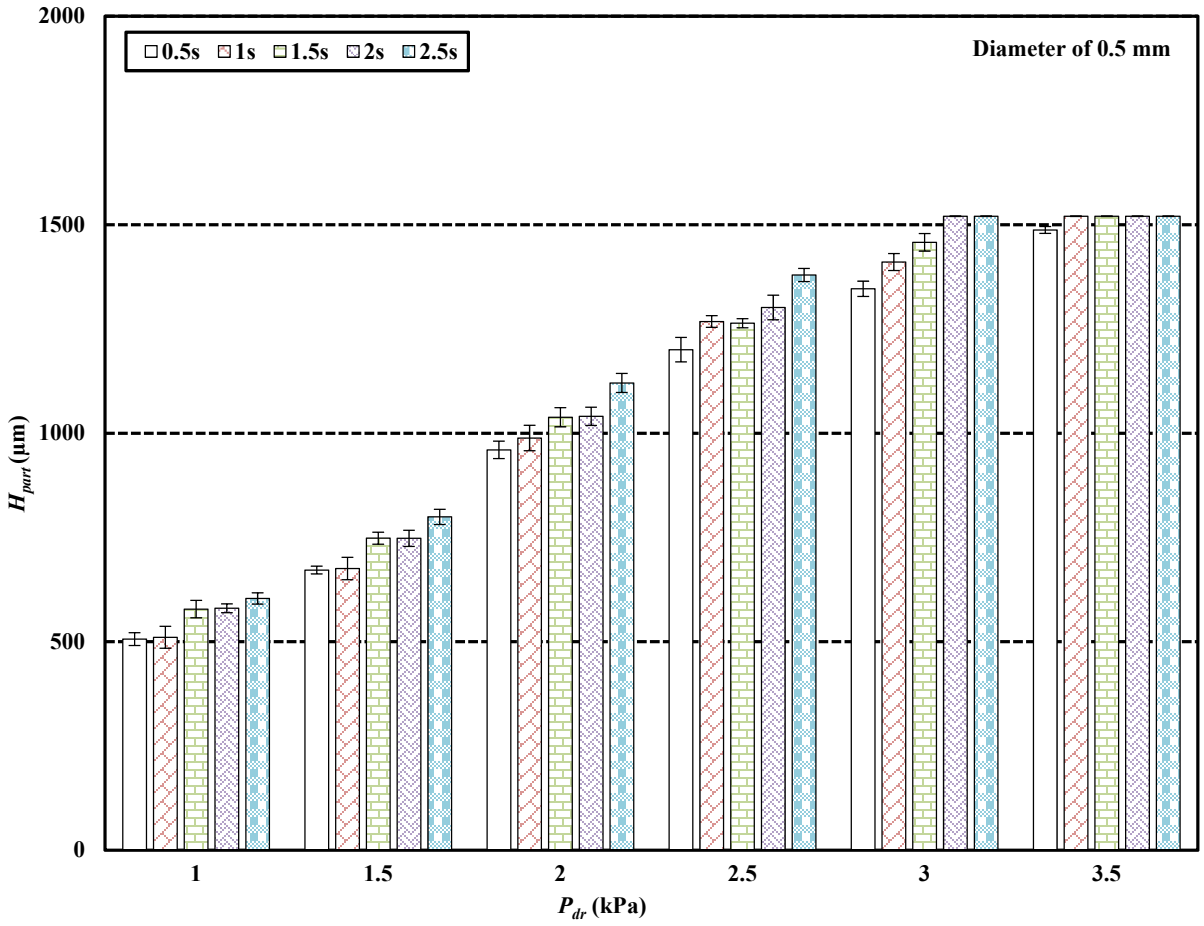

Figure 5.15 The metallization result of the via with diameter of 0.5 mm under different combinations of driving pressure and feeding time.

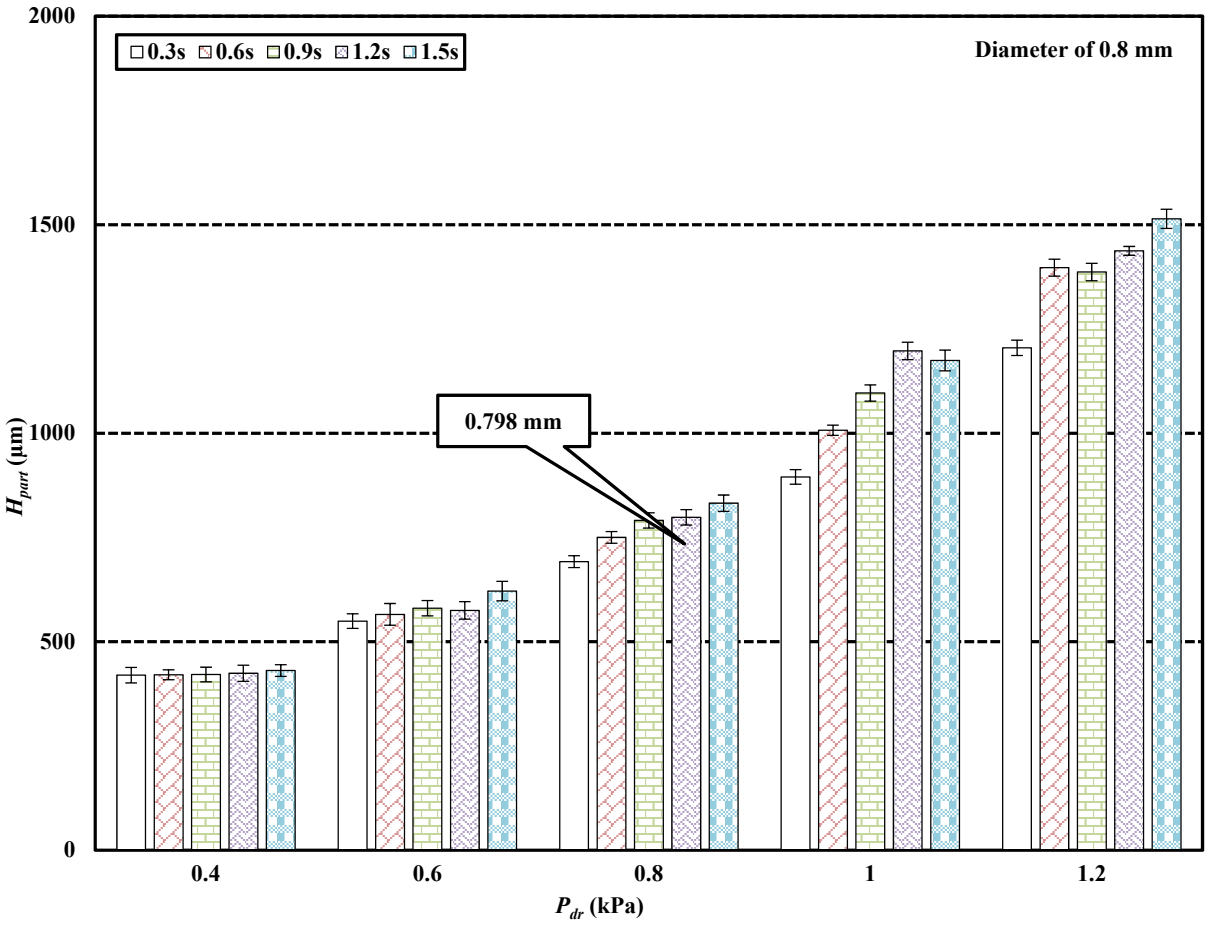

Figure 5.16 The metallization result of the via with diameter of 0.8 mm under different combinations of driving pressure and feeding time.

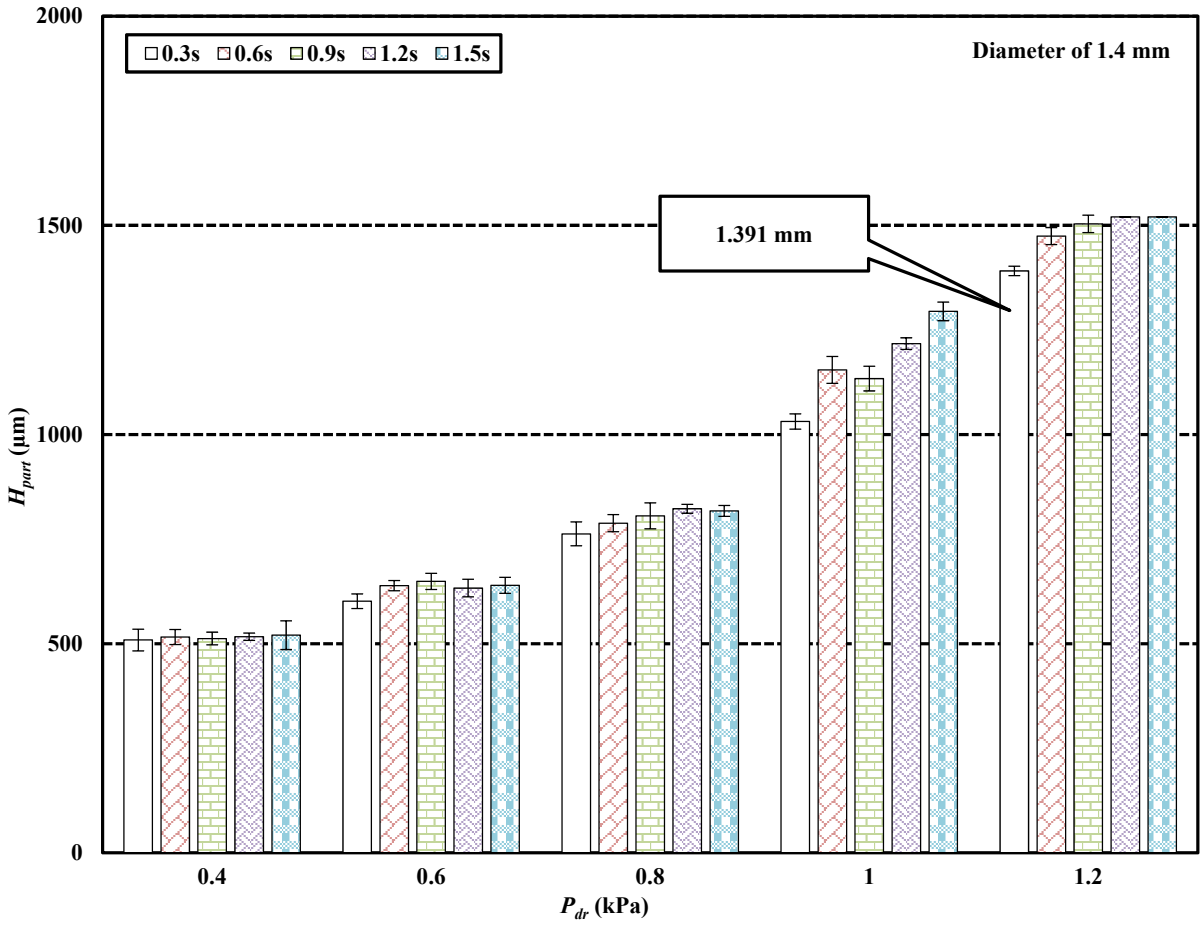

Figure 5.17 The metallization result of the via with diameter of 1 mm under different combinations of driving pressure and feeding time.

5.3.2 Filter Characterization

From Figure 5.18(a), it is easy to see the fabricated flexible filter is in the rectangular shape and has the single-layer configuration as designed. More importantly, it can be easily bent by two fingers, which can be revealed by Figure 5.18(b) and Figure 5.18(c). The rigid filter has the similar rectangular outline, as shown in Figure 5.19.

Two SMA connectors (TE Connectivity Ltd.) are soldered onto the barrier layer directly in order to achieve the connection between the filter and a vector network analyzer (R&S®, ZVA 67) which is employed for the characterization purpose. First, a parameter study is conducted on the rigid substrate, to investigate the influence of the partial height on the filter's performance. After

that, the measurement is carried out on both flexible and rigid filers as normal, i.e. they are in their naturally flat status with no bending. Last, two extra measurements are performed on the flexible filter, as described below.

1) Case 1. The flexible filter is attached to a glass beaker whose diameter is around 70 mm, as given in Figure 5.20(a).

2) Case 2. The flexible filter is attached to a glass beaker whose diameter is around 25 mm, as given in Figure 5.20(b).

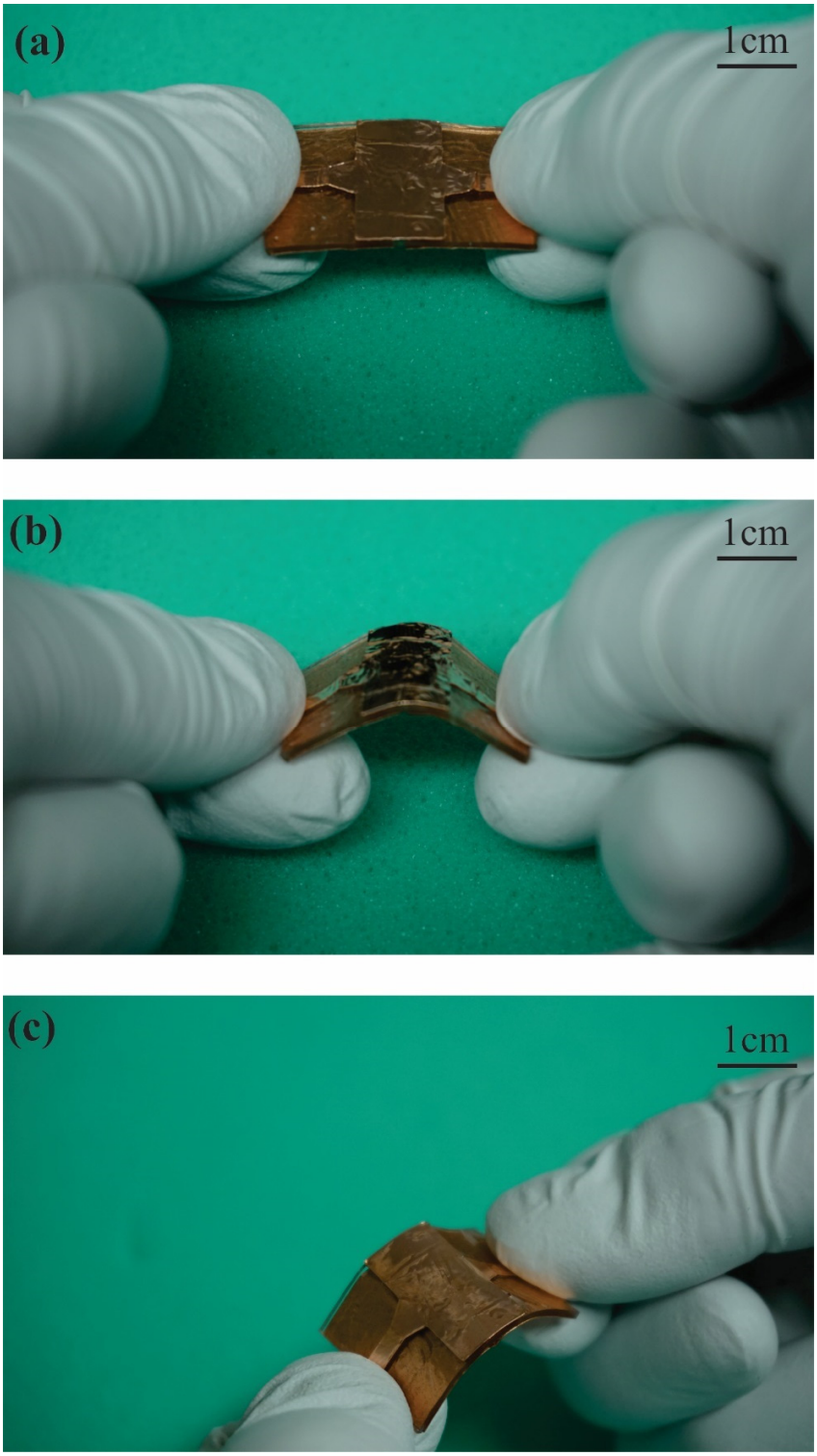

Figure 5.18 The fabricated flexible filter. (a) The flexible filter is in the rectangular shape as designed. (b) and (c) The flexible filter can be easily bent by two fingers.

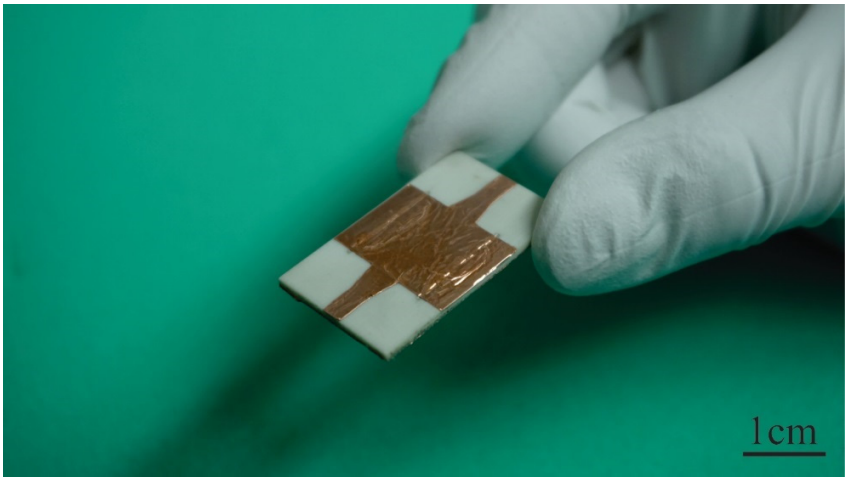

Figure 5.19 A close look at the fabricated rigid filter. The while area indicates the original barrier layer has been removed.

To start with, a parameter study of the partial height is performed based on the rigid substrate. As shown in Figure 5.21, as the partial height grows from 1.3 mm to 1.35 mm, the corresponding maximum reflection coefficient (S_{11}) increases from -4 dB to -1 dB. After that, it seems to have a limited influence, because no significant increase or decrease can be witnessed. On the contrary, the resonant frequency (S_{21}) maintains a downward trend, starting at nearly 12 GHz and ending up at 9 GHz, and this downward trend becomes more obvious while the partial height approaches the substrate's thickness. More specifically, the resonant frequency shifts only 0.5 GHz when the partial height grows from 1.3 mm to 1.35 mm, then it drops from 10.5 GHz to 9 GHz after the third 0.05 mm height growth. The record of the maximum reflection coefficients and the resonant frequencies correspond to different partial heights are presented in Table 5.5.

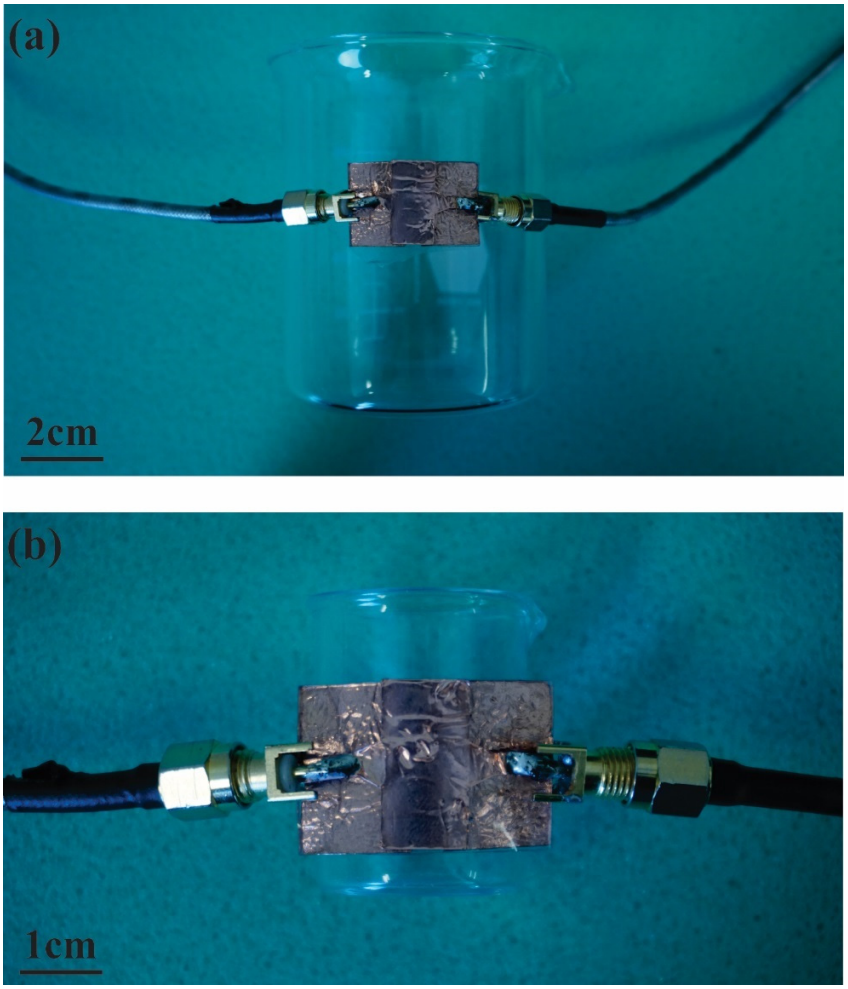

Figure 5.20 The flexible filter is tested under different bending conditions. (a) The flexible filter is attached to a big beaker with diameter of 70 mm. (b) The flexible filter is attached to a small beaker with diameter of 25 mm.

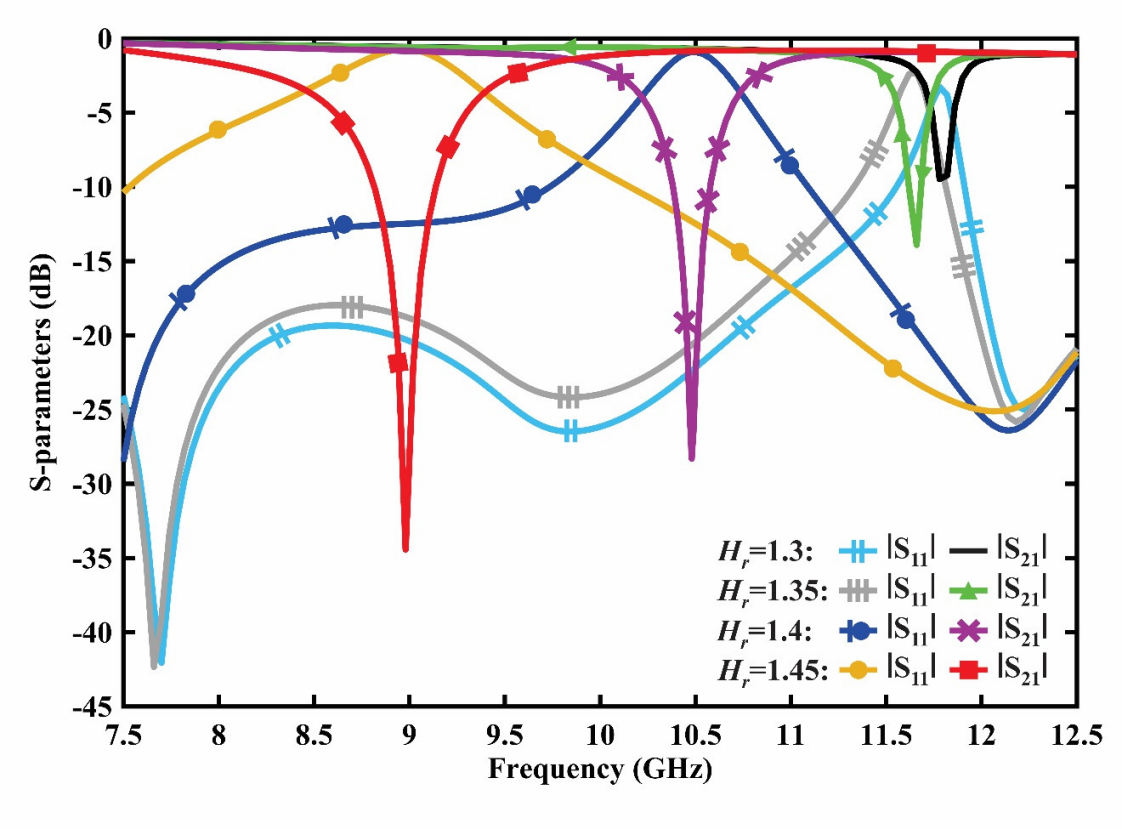

Figure 5.21 The simulated S-parameters of the rigid filter with various partial heights. When the partial height increases from 1.3 mm to 1.45 mm, the resonant frequency keeps shifting to the lower level, but the maximum reflection coefficient seems to be fixed at -1 dB.

Table 5.5 A summary of simulated results of the maximum reflection coefficients and the resonant frequencies of the rigid SIW filter correspond to different partial heights.

Partial Height (mm)	Maximum Reflection Coefficient (dB)	Resonant Frequency (GHz)
1.30	-4.0066	11.8750
1.31	-2.4018	11.6750
1.32	-2.2844	11.6750
1.33	-1.5660	11.4750
1.34	-1.5557	11.4250
1.35	-1.3165	11.3500
1.36	-1.3047	11.2750
1.37	-1.2926	11.2500
1.38	-0.9486	11.0500
1.39	-0.9994	10.9500
1.40	-0.9033	10.5000
1.41	-0.9103	10.4750
1.42	-0.9076	10.4250
1.43	-0.9231	10.3000
1.44	-0.8783	9.4500
1.45	-0.8281	9.2500

The measured performance of the rigid filter (partial height is 1.4 mm) is presented in Figure 5.22. It is not hard to notice that the practical resonant frequency goes down to a lower level of 10.2 GHz. According to the simulated result in Table 5.5, this suggests the fabricated partial height should be between 1.43 mm and 1.44 mm. As the designed partial height is 1.4 mm, the fabrication error is less than 3 %, which can well prove the accuracy of this via metallization approach. Although the theoretical maximum insertion loss is close to -1 dB at 10.5 GHz, the measurement shows it is about -2 dB in practice. Several reasonable explanations for these mismatches are listed below.

1) The conductive polymer's electrical properties such as conductivity, permittivity, *etc.* which are used for the design and the simulation, are typically characterized by the supplier in an ideal environment. During the real utilization, however, they can barely be sustained, which means that the material degrade cannot be avoided. Actually, such phenomenon has been reported in the literature [101-103].

2) The barrier layer is pasted to the substrate, which is different from the sputtering or the electroplating process. Thus, the adhesion between the barrier layer and the vias might be problematic.

3) The connection between the SMA connector and the filter might not be good enough.

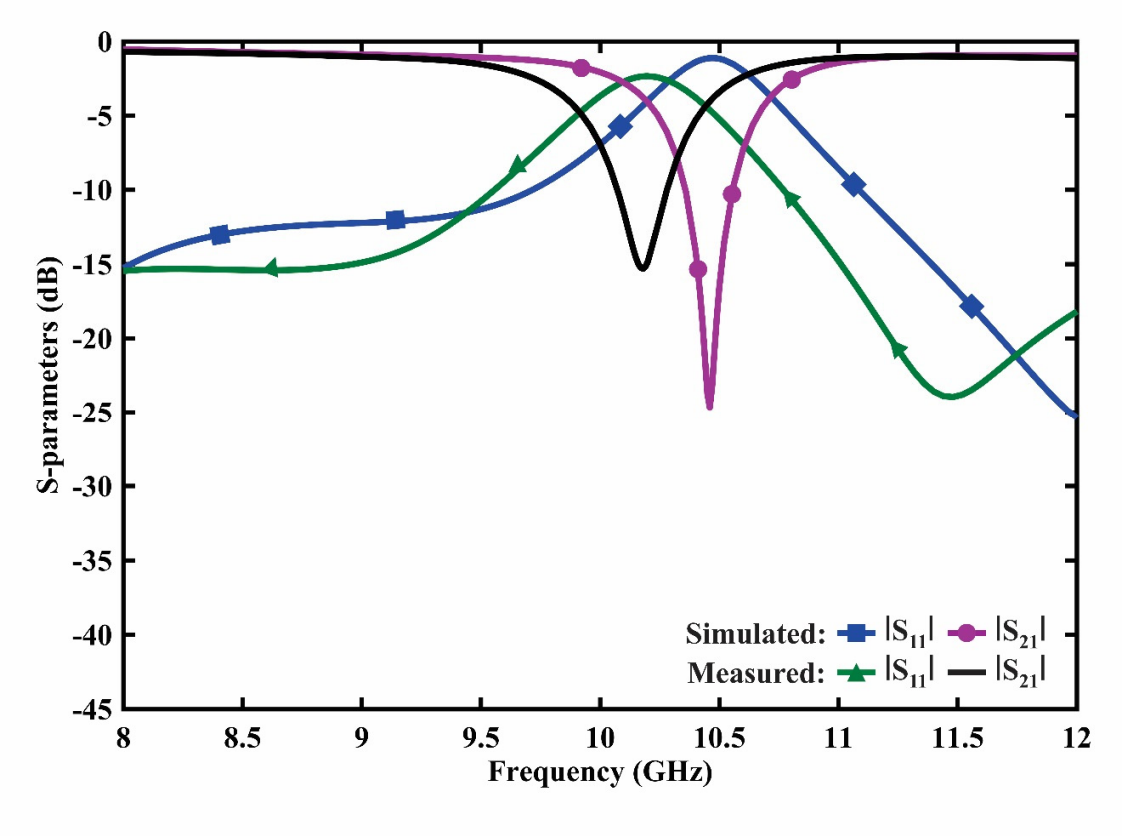

Figure 5.22 The simulated and measured S-parameters of the rigid filter. The partial height of the measured rigid filter is 1.4 mm.

With respect to the flexible filter, the similar mismatches exist between the simulated and the measured performances under the bending free condition. As presented in Figure 5.23, the measured resonant frequency drifts to 14.6 GHz from the simulated 15 GHz; the practical maximum insertion loss is about -2.3 dB, which is higher than the theoretical value (about -1 dB). Also, in this case, a detailed parameter study on the partial height is performed, the result is included in Table 5.6. The negligible difference between the simulated and the measured resonant frequencies again confirms the accuracy of the vacuum suction, because the fabricated partial height should be close to 0.81 mm accordingly. Figure 5.24 depicts the measured resonant frequency and the reflection coefficient under different bending conditions. The former is brought down from 14 GHz to 13 GHz as the bend radius reduces from 35 mm to 12.5 mm. However, the latter stabilizes at -2.3 dB in all three cases. Several reasons are listed below.

1) The bending increases the distance between two vias in the same row, which results in the extension of the length and the shrinkage of the width of the via row.

2) The adhesion between the conductive polymer and the via sidewall is partially damaged by the bending.

3) Some parts of the barrier layers are peeled off after the deformation of the PDMS substrate.

4) The bending might affect the connection between the barrier layers and the SMA connectors.

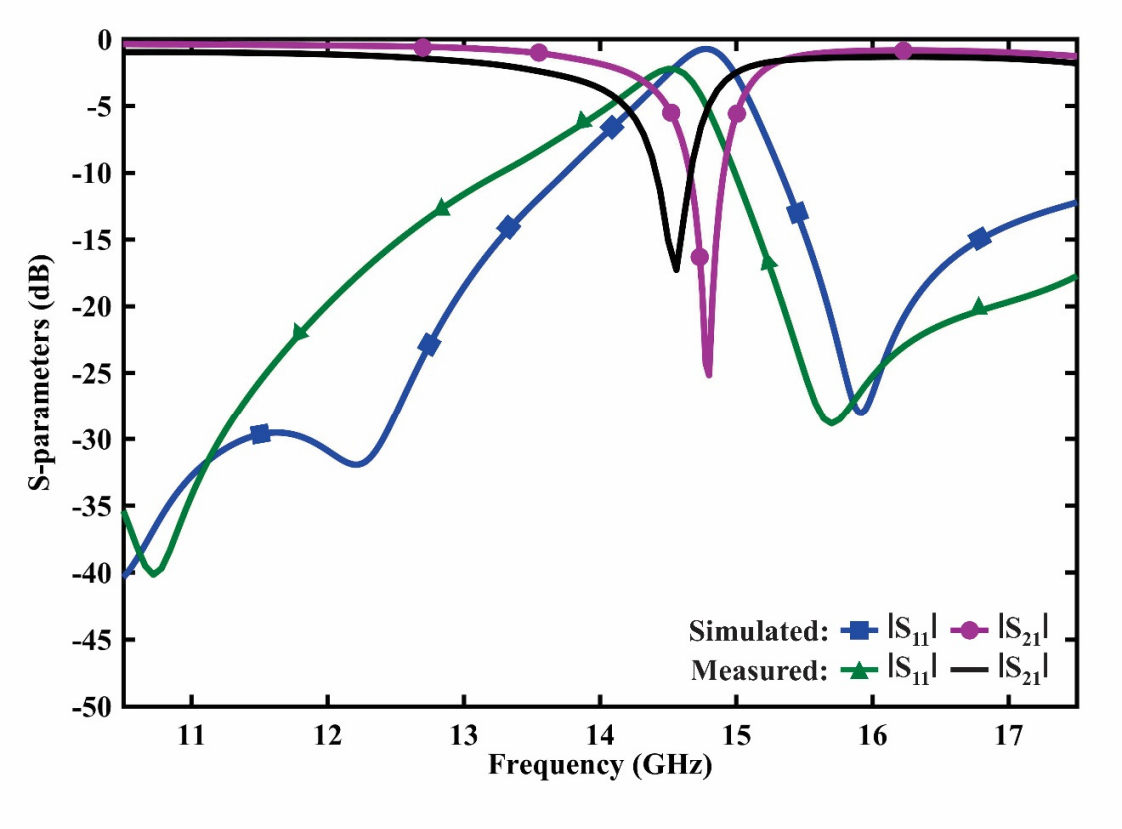

Figure 5.23 The simulated and measured S-parameters of the flexible filter without bending. The corresponding partial height is 0.8 mm.

Table 5.6 A summary of simulated results of the maximum reflection coefficients and the resonant frequencies of the flexible SIW filter correspond to different partial heights.

Partial Height (mm)	Maximum Reflection Coefficient (dB)	Resonant Frequency (GHz)
0.75	-2.0708	15.3500
0.76	-1.6007	15.2500
0.77	-1.444	15.1500
0.78	-1.3073	15.0500
0.79	-1.1404	14.9000
0.80	-1.0190	14.8000
0.81	-0.8860	14.6000
0.82	-0.8226	14.4000
0.83	-0.7888	14.2000
0.84	-0.7804	13.9500
0.85	-0.7763	13.6500

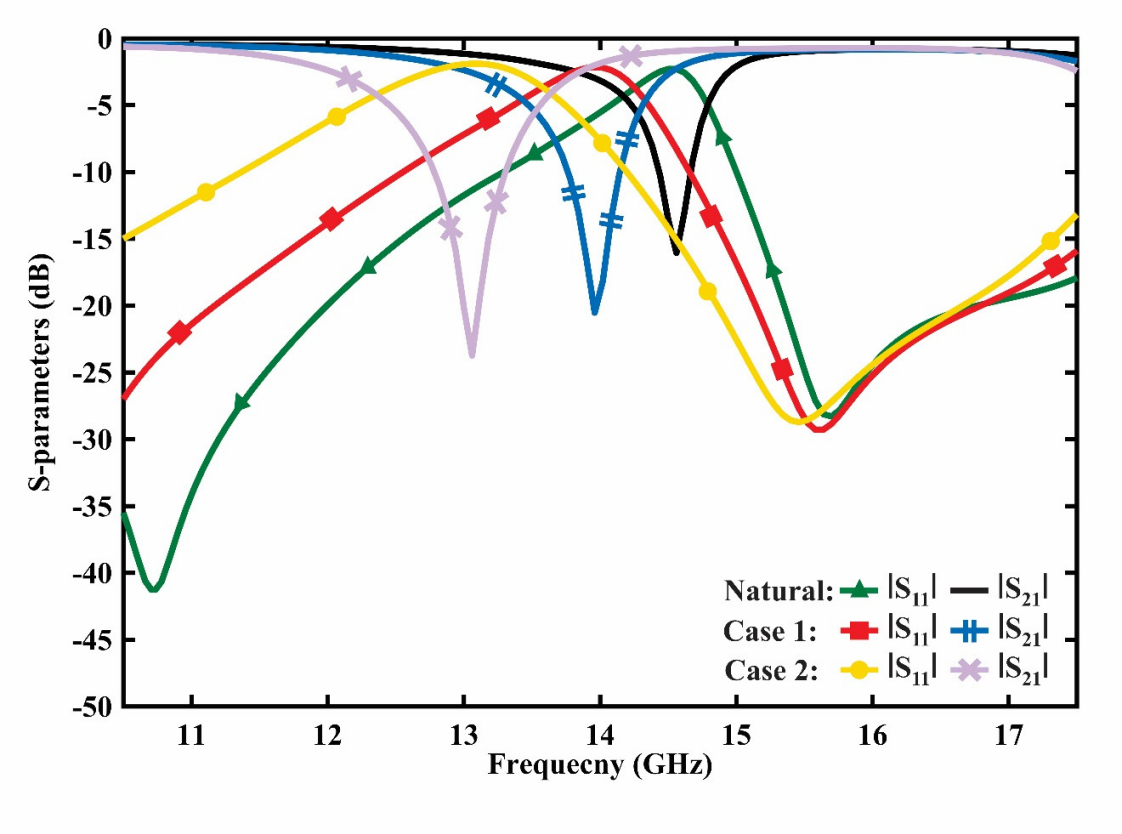

Figure 5.24 The measured S-parameters of the flexible filter under different bending conditions. The natural status can be treated as the bent radius is infinity.

It should be noted that to calculate the loaded and unloaded quality factors, the losses due to low conductivity of the conductive polymer and the loss of the transition and transmission lines must be de-embedded. Then, the loaded quality factor is obtained by

$$Q_l = \frac{f_0}{\Delta f_{3dB}} \tag{5.3}$$

where f_0 and Δf_{3dB} are the resonant frequency and the 3 dB bandwidth of the filter's response. To include the input-output loading effects, an external quality factor is defined as

$$Q_e = \frac{Q_l}{10^{|S_{21}(dB)|/20}} \tag{5.4}$$

where $|S_{21}(dB)|$ is the insertion loss of the filter. Therefore, the unloaded quality factor of the filter is calculated as:

$$Q_u = \frac{Q_l Q_e}{Q_e - Q_l} \tag{5.5}$$

5.4 Conclusion

A new SIW metallization method is successfully developed. The conductive polymer instead of electroplated Cu is used to fill the via arrays and resonators under a vacuum condition to accelerate the metallization process. Varying via diameters and depths are investigated under different suction conditions. Based on that, two prototypes of band-stop SIW filter with partial height post are successfully fabricated on PDMS and RO4003C. Good agreements between the simulated and the measured results are obtained, which prove the feasibility of this method for the future development of SIW devices.

"26, this is 25. Is that you shooting up the technicals?"

-- Black Hawk Down

Chapter 6: Wafer Level TSV Metallization

All silicon via metallization experiments in Chapter 3 and Chapter 4 are performed on the chip level, since all wafers have been diced after the via formation. However, it might be necessary to scale it up to the wafer level to boost the efficiency.

6.1 Vacuum Suction Platform Buildup

A cost-efficient way to reach this goal is to enlarge the size of the suction head. As given by Figure 6.1, the new suction head is made by stacking three pieces of acrylic plates (McMaster-Carr®) with circular openings. The opening sizes are 1.5 inch, 3.5 inch and 5.5 inch respectively, which are supposed to accommodate standard 2-inch and 4-inch wafers. The manufactured suction head is shown in Figure 6.2. Other components of the platform remain the same as described in Section 3.2.2.

6.2 Wafer Level TSV Metallization

A quick verification is performed on the 4-inch wafer samples that have been mentioned in Chapter 3 using the same silver and graphene doped epoxy that has been mentioned in Chapter 5. It is necessary to mention that the pressure difference distribution over the wafer might be uneven, especially at the beginning when the vacuum pump in the multi-function fluid dispenser is turned on and the equilibrium is not reached yet, which will affect the filling depth. Thus, after each combination of pressure difference and duration is completed, the wafer is virtually divided into four sections according to their distances to the wafer center for the filling depth and resistance data collection, as shown in Figure 6.3.

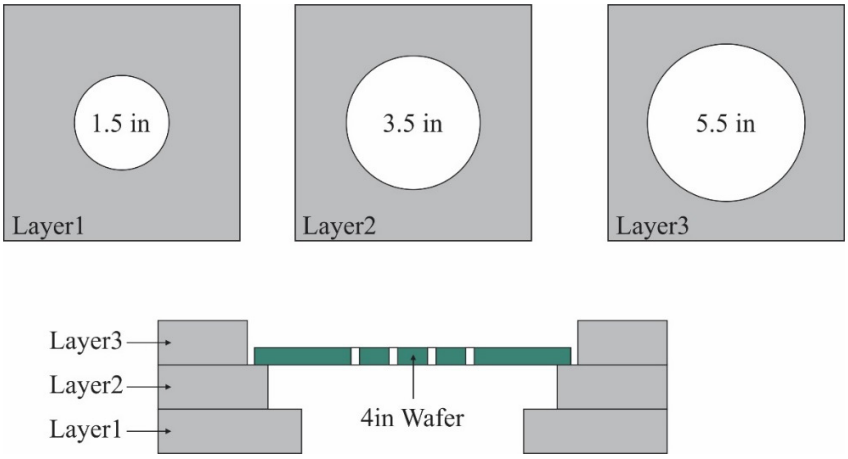

Figure 6.1 A schematic demonstration of how to build the new vacuum suction head.

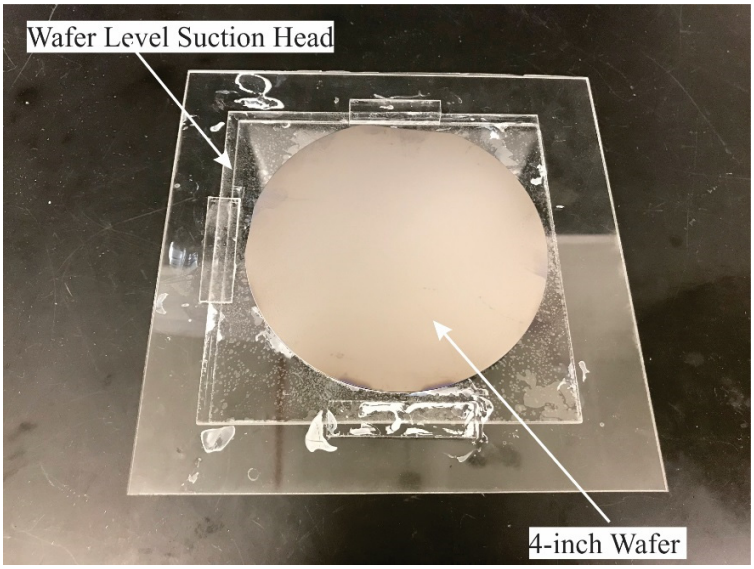

Figure 6.2 A close look at the vacuum suction head for the wafer level metallization. The acrylic sheets are bonded using acetone. A 4-inch wafer is placed on the top.

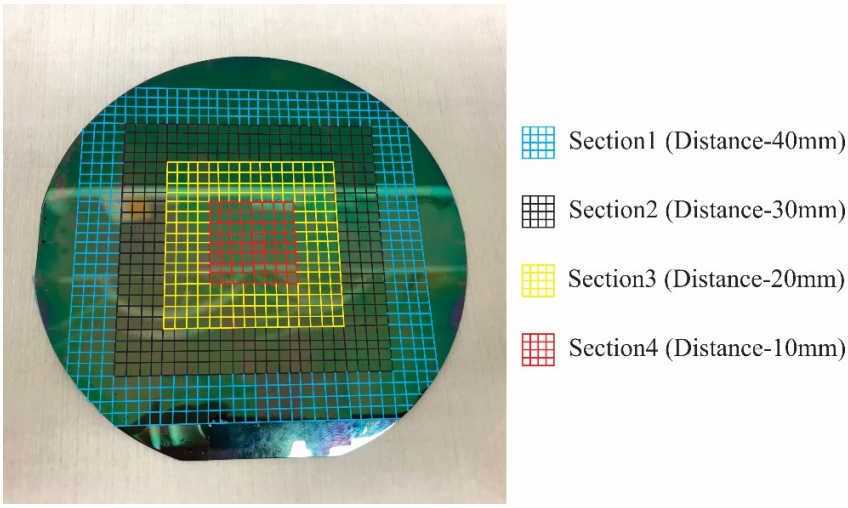

Figure 6.3 A brief explanation of how to divide the wafer. The wafer is virtually divided into four sections based on their distance to the center.

6.3 Characterization

Three vacuum pressures and three durations are verified, which are 1 kPa, 1.2 kPa, 1.4 kPa and 1 s, 2 s, 3s respectively. The filling results are presented in Figure 6.4, Figure 6.5 and Figure 6.6. Several conclusions can be drawn as follows.

1) The increase of either pressure difference or duration can promote the filling ratio.

2) When the pressure difference or the duration is fixed, the filling ratio will increase from Section1 to Section4, which confirms that the vacuum pressure is not uniform over the whole wafer at the beginning, and it increases if the location is closer to the wafer center.

3) When the vacuum pressure is 1 kPa, the vias cannot be entirely filled in 3 s regardless where it is. When the vacuum pressure increases to 1.2 kPa, only the vias in Section2, Section3 and Section4 can be entirely filled in 3 s. When the vacuum pressure increases to 1.4 kPa, the 100% filling ratio can be reached in 2 s all over the wafer.

4) The effect of the non-uniform vacuum pressure on the filling depth can be ignored, as the practical TSV metallization process is not sensitive to the duration that is shorter than 1 min.

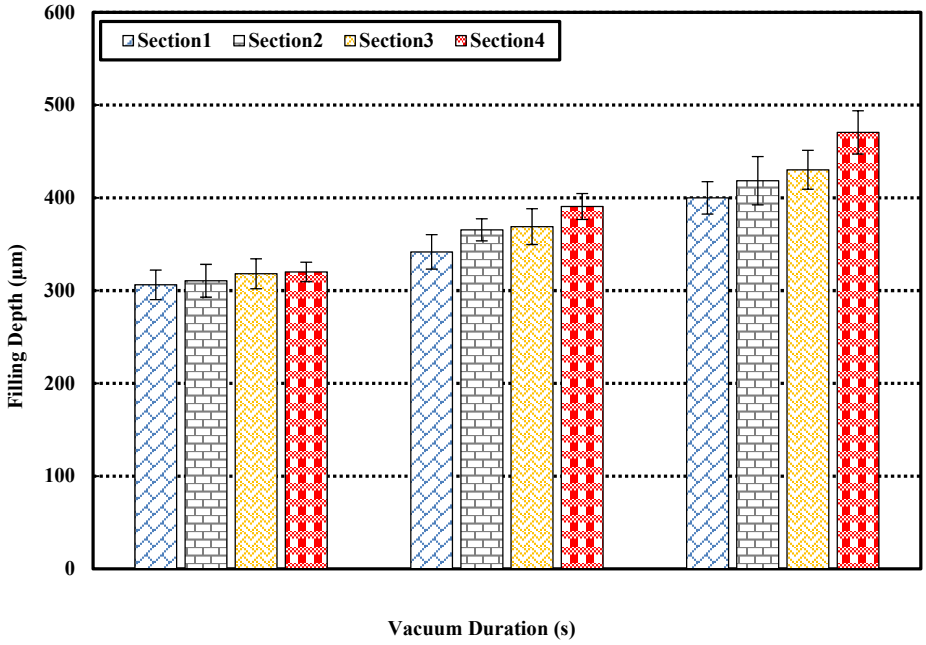

Figure 6.4 A summary of filling depths under pressure difference of 1 kPa.

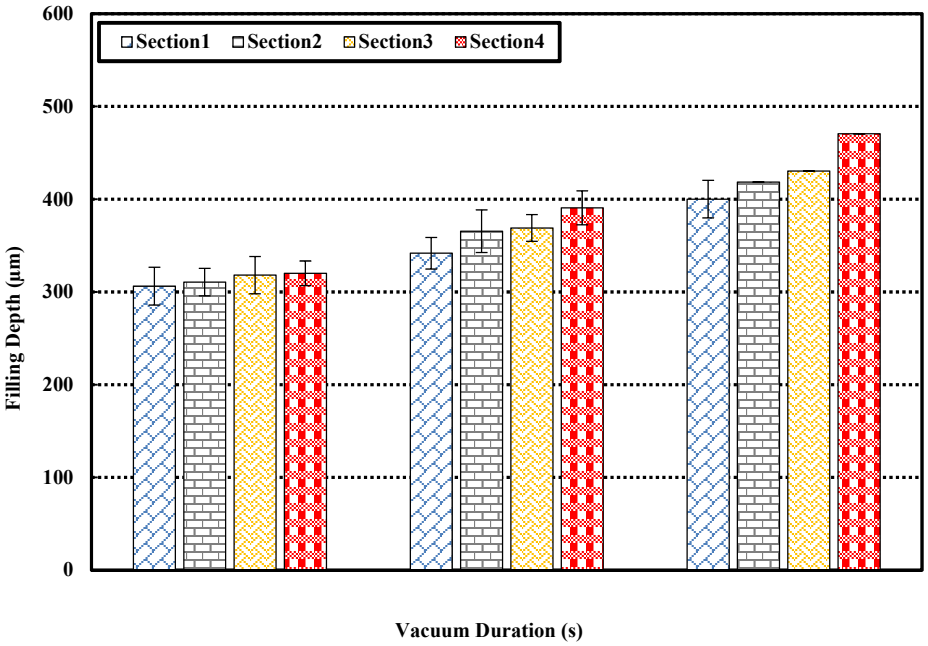

Figure 6.5 A summary of filling depths under pressure difference of 1.2 kPa.

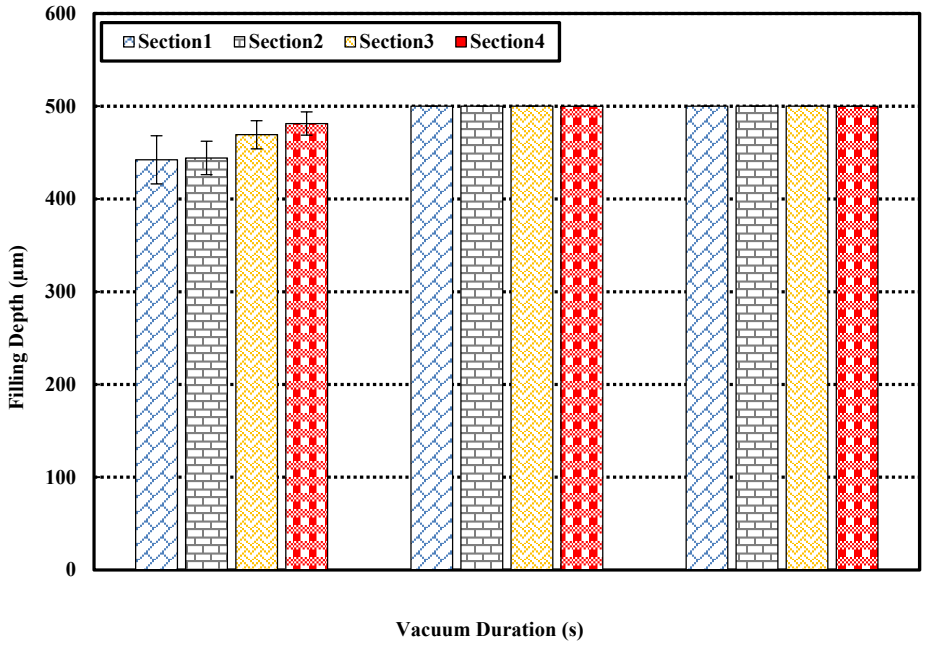

Figure 6.6 A summary of filling depths under pressure difference of 1.4 kPa.

For the TSV resistance, 15 groups of TSVs (two chained TSV in each group) from each section are measured (Keithley 2400 Digital Sourcemeter). The result is summarized in Figure 6.7. It can be found that the average values of the TSV resistance from Section1 to Section4 decrease from 13 Ω to11 Ω approximately.

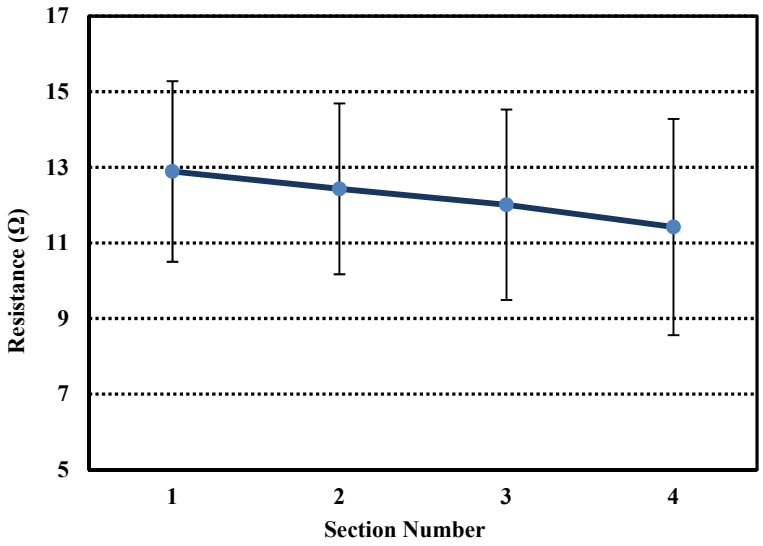

Figure 6.7 The average resistance and relevant standard deviation of TSVs in different sections.

"The moment that often mattered the most, the moment when you truly found out who they were, was often their last one."

-- Person of Interest

Chapter 7: Conclusion and Future Work

7.1 Conclusion

Generally, this thesis has successfully solved several problems on TSV for 3D integration and applied TSV to the development of SIW for RF circuits.

Chapter 3 details a new method to achieve the fast and dependable TSV metallization. In which, the vacuum driven Ag-based epoxy instead of electroplated Cu is employed as the metallization material; several positive outcomes therefore have been obtained. First, the TSV fabrication process is simplified, because the seed or the barrier layer is no longer necessary and the 100 % filling ratio can be achieved without any additives. Second, the TSV metallization is shortened, as the conductive polymer can thoroughly fill the via in 3 s when the pressure difference is 1.6 kPa. Third, the Ag-based epoxy is proven to have relatively low resistance, acceptable thermal stability and bonding strength to Cu.

Chapter 4 pushes the idea of metallizing TSV with the conductive polymer further, as a new silicon interposer architecture which can be treated as connected multiple layers of TSVs is created. By replacing the conventional RDL with trenches that are formed in the die body, RDL and TSV can be fabricated simultaneously, more easily and more quickly. In addition, the risk of connection failure at the interface is eliminated. More relevant characterizations related to the trench dimension and the conductive polymers are performed, which lays the groundwork for the future application and optimization.

In Chapter 5, based on the new metallization method, TSV has been successfully applied to the development of SIW for RF circuits. First, the SIW device fabrication process is shortened and simplified. Second, through the accurate control of the vacuum condition, the partial height metallization becomes achievable, which makes it possible for the ridge resonator to be built in a single layer substrate.

7.2 Future Work

In spite of the contributions have been listed above, more comprehensive work still needs to be done, as outlined below.

First, although TSV can stand the high resistance in some cases, the conductivity of the metallization material is still supposed to be as low as possible. In fact, the practical conductivity of many commercial conductive polymers is still lower than that of the metal materials that are commonly used in M/NEMS, such as Cu, Al and Ag. Thus, the improvement in their conductivity should be made, which may include the development of new conductive fillers, the optimization of the blending process. At this point, a more efficient way to receive the balance between the low resistance and the short processing duration can be depositing a thicker seed layer (10 % to 50 % of the total thickness, through PVD and/or electroplating) into the via before the suction of the conductive polymer.

Second, in Section 5.3.1, we test 20 combinations of pressure difference and feeding time to find the most suitable one for the fabrication of each partial height via. This process is not efficient. Thus, a theoretical model of the suction operation needs to be built to better predict the suitable vacuum level and duration for any filling ratio.

Third, the fabrication of a certain number of devices usually asks for the bonding of dozens of layers indeed, the two-layer case covered by Chapter 3 is barely enough. Thus, it will be necessary to test the metallization methodology on a greater number of layers.

Fourth, apart from the SIW filter, the same methodology is worthy of more tests on other SIW devices in order to improve its compatibility and reliably.

“你们啊，不要想……喜欢……这…欸弄个大新闻，说现在已经钦定了，再把我批判一番。”

“一个人的命运啊，当然要靠自我奋斗，但是也要考虑到历史的行程。”

-- 江泽民

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