Modular Multilevel Converters with Multi-Frequency Power Transfer

by

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Abstract

The MMC is the dominant voltage-sourced converter technology for HVDC systems including terrestrial power transmission and offshore wind power integration. It is also a state-of-the-art solution for emerging MVDC applications such as bipolar dc distribution and grid integration of renewable energy resources. Significant research has been recently targeting the development of new MMC-based topologies that can reap the benefits of the conventional dc-ac MMC in dc grids and hybrid ac/dc power systems. Notable examples include dc-dc converters, multi-port converters, line power flow controllers and power tapping stations.

This thesis introduces the concept of multi-frequency power transfer in MMCs where the magnetics windings are multi-tasked to carry currents with multiple frequency components, namely dc and fundamental frequency. Core dc flux cancellation is imposed by appropriate orientation of the individual windings. This novel power transfer mechanism can eliminate redundant energy conversion through partial-power-processing while offering increased flexibility in converter port power flows. Based on the multi-frequency power transfer concept, new MMC-based topologies are proposed that are well suited for MVDC and HVDC grids and hybrid ac/dc systems.

Firstly, a new class of single-stage modular multilevel dc-dc converter, termed the M2DC-CT, is proposed for applications requiring either high or low dc stepping ratios. By placing center-tapped transformer windings in series with the arms in each phase leg, the advantages of minimized ac arm currents and absence of dc voltage stress between windings are simultaneously obtained unlike in prior art. Modeling and

analysis gives insight into the M2DC-CT multi-frequency power transfer characteristics and suitable converter controls are developed. Converter operation is validated through simulation and experiment.

Secondly, a dual MMC structure is presented that achieves multi-frequency power transfer by tying together the three mid-points of the converter-side center-tapped transformer windings to form an additional dc port. This creates a bipolar MMC with the ability to balance the dc pole power flows in bipolar dc grids. The employed center-tapped transformer has a Volt-Ampere rating that is the same as a conventional grid interfacing transformer. Dynamic controls formulated in the $\alpha\beta$-frame provide tight regulation of the port power flows while ensuring balanced capacitor voltages. The independent pole balancing capability is confirmed through simulation of detailed MVDC-level and HVDC-level PSCAD models and rigorous experimental testing on a scaled-down laboratory prototype.

Thirdly, the aforementioned multi-frequency dual MMC structure is proposed for use as a three-port MMC. It allows simultaneous dc-dc and dc-ac conversions between an ac grid and two dc systems, which is distinctly different from the earlier bipolar dc grid application. The $\alpha\beta$ controls developed earlier are easily extended for the three-port application by assigning appropriate reference signals. Steady-state and dynamic operation of the three-port dual MMC topology is validated by simulation with a HVDC-level PSCAD model and extensive experimental tests.

Lastly, a detailed comparative assessment of three-port MMCs for high-power applications is conducted. The proposed three-port dual MMC structure and three-port version of the M2DC-CT are compared against two other existing three-port MMCs, on the basis of efficiency, semiconductor effort, internal energy storage and magnetics. Both MVDC and HVDC case studies are examined including several different power flow cases, with provisions for fault blocking. The results indicate the use of multi-frequency power transfer can enable significant reductions in converter operating losses and cost relative to prior art, depending on the application.

Preface

This thesis is an original work by Yuan Li under the supervision of Dr. Gregory Kish. Some parts of this thesis have been published as journal and conference publications and have been reorganized for clearer presentation.

Chapter 2 has been published as:

- Y. Li and G. J. Kish, "The Modular Multilevel DC Converter with Inherent Minimization of Arm Current Stresses," in *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 12787-12800, 2020.

Chapters 3 and 4 have been published as one conference paper and a journal paper:

- Y. Li, D. Liu and G. J. Kish, "Generalized DC-DC-AC MMC Structure for MVDC and HVDC Applications," in *IEEE 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2019, pp. 1-8.

- Y. Li, D. Liu and G. J. Kish, "A Dual MMC Chain-Link Structure for Multi-Frequency Power Transfer," in *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 14601-14614, 2022.

Chapter 5 has been published as:

- Y. Li, and G. J. Kish, "Comparative assessment of multi-port mmcs for high-power applications," in *IEEE Access*, vol. 10, pp. 22049–22060, 2022.

To my mother, father and girlfriend

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Abbreviations

AC Alternating Current.

CCL Circulating Current Loop.

DAB Dual Active Bridge.

DC Direct Current.

F2F-MMC Front-to-Front MMC.

FB Full-Bridge.

FBSM Full-Bridge Submodule.

HB Half-Bridge.

HBSM Half-Bridge Submodule.

HV High-Voltage.

HVAC High-Voltage AC.

HVDC High-Voltage DC.

HVDC-AT HVDC-Auto Transformer.

IGBT Insulated-Gate Bipolar Transistor.

LCC Line-Commutated Converter.

M2DC Modular Multilevel DC Converter.

M2DC-CT Modular Multilevel DC Converter with Center-tapped Transformer.

MMC Modular Multilevel Converter.

MV Medium-Voltage.

MVDC Medium-Voltage DC.

p.u. Per-Unit.

P3T Partial-Power-Processing Transformer.

PI Proportional-Integral.

PR Proportional-Resonant.

SM Submodule.

TPC Three-Port Converter.

TP-MMC Three-Port Version of Multi-Frequency Dual MMC Structure.

TP-CT Three-Port Version of M2DC-CT.

TP-AT Three-Port Version of HVDC-AT.

TP-F2F Three-Port Version of F2F-MMC.

VSC Voltage-Sourced Converter.

Chapter 1

Introduction

Ongoing concerns about climate change associated with the growing demand for sustainable electrical energy system have in recent years led to the significant increase on the share of electricity produced from renewable energy sources in the power system. In such a large electrical system that allows the interconnection between the remote power plants and power grids, the challenges related to power transmission over long distances have gained importance, particularly in areas with continental dimensions, such as China, Canada, Brazil, Russia and Europe.

HVDC technology is an economic alternative to ac power transmission due to its lower power losses over very long distances. At present, there is an increasing number of voltage-sourced converter based HVDC transmission systems being planned and built around the world. The development of HVDC technology is expected to facilitate the integration of scattered renewable energy resources in the power system such as offshore wind farms. However, the existing point-to-point transmission systems have some limitations in deriving fractional amount of power along the main power corridor. On the other hand, the benefits of interconnection of one or more electrical systems such as increased reliability and optimized costs of electricity production also drive the expansion of power grids. Looking forward, an evolution from traditional two-terminal HVDC links to more complex multi-terminal dc networks using MVDC and HVDC links is anticipated [1]. Indeed, the Zhangbei-1 project recently commissioned in China as the first global installation of a multi-terminal HVDC grid aimed to meet the expected higher demand during Beijing 2022 Winter Olympic Games [2]. In addition to the idea of a dc supergrid [1], research effort has been focused on overlaying existing ac grids with backbone dc grids or hybrid (mixed) ac/dc microgrids for its potential to improve power transfer capability and overall system stability [1, 3]. The future highly meshed multi-terminal hybrid ac/dc networks will rely on dc-dc and dc-ac power electronic converter topologies for system interconnects, power tapping

and power flow control [4].

MMC technology can achieve high efficiencies over 99% and also has advantages such as low harmonics, high modularity and good scalability compared with other voltage source converters [5]. Therefore, it is a state-of-the-art solution for dc-ac conversion in MVDC and HVDC systems. Notably, it is the dominant power converter solution in terrestrial VSC-based HVDC and offshore wind power integration [6–9]. More recently, significant research has been focused on developing new and novel topologies that reap the benefits of the popular dc-ac MMC. These include dc-dc MMC and multi-port MMC (with integrated ac grid interface) topologies for broad application in hybrid ac/dc grids including MVDC and HVDC systems, e.g., [10–19]. The structures in [10–19] series-stack low-voltage submodules similar to the conventional dc-ac MMC, however, they exploit internal circulating ac power in addition to the classical ac power injection at the MMC midpoint node. Key advantages of these emerging MMC topologies include compact converter structures, savings in converter capital cost, and reduced operating losses. Building on this burgeoning line of research, this thesis proposes new MMC topologies that exploit the concept of multi-frequency power transfer, enabled by transformers that multi-task by imposing the windings to carry currents with multiple frequency components. This novel power transfer mechanism opens the door to a host of exciting MMC applications in dc grids and hybrid ac-dc power systems including new dc-dc and dc-dc-ac MMC solutions.

1.1 HVDC and MVDC System Configurations

Fig. 1.1 depicts possible configurations for monopolar MMC systems. An asymmetrical monopolar MMC configuration is shown in Fig. 1.1a, where the dc current returns through the ground or a metallic return path. It represents the most cost-effective solution as only a single cable or overhead line is required. However, to achieve equal transmission capacity, transformer and cables for asymmetrical monopolar configuration must be designed to withstand twice the rated voltage (to ground) compared to its symmetric monopolar counterpart. To satisfy the need for bulk-power interconnection and minimize the dc insulation levels required, VSC-based HVDC transmission systems are usually designed to be symmetrical monopolar configuration. Symmetrical monopoles have positive and negative dc cables (as bipoles) but the system is operated as a single unit (as a monopole). Two-level VSC-based HVDC uses capacitors permanently connected in series at each converter station withstanding the pole to pole voltage, to establish a zero potential point for the control system. The earth point is located between the two cables or overhead lines of the converter in

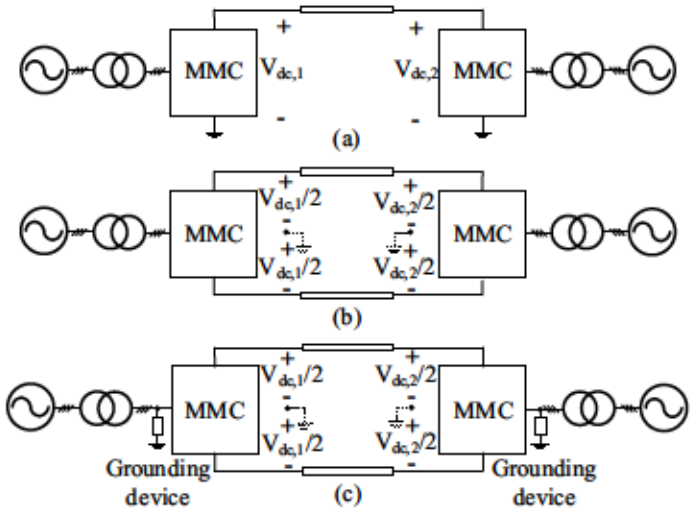

Figure 1.1: Monopolar configuration for MVDC and HVDC systems: (a) asymmetrical monopolar MMC, (b) symmetrical monopolar MMC, (c) symmetrical monopolar MMC with ac side ground device

VSC-based symmetrical monopolar configurations, with no direct current entering the ground point but returning through the cable. In contrast, the MMC-based symmetrical monopolar HVDC does not need to be grounded via main dc link capacitors as capacitors have been assigned into the submodules (see Fig. 1.1b) [20]. Although symmetrical monopolar configuration is widely used in HVDC and MVDC projects (e.g., [6, 9, 21, 22]), it has several disadvantages in practical applications:

- In case of dc cable failure or dc line-to-ground fault, the entire power transfer is lost.
- The pole balancing would not be guaranteed due to mechanical damage or ageing of the cable [15] and after dc line-to-ground fault.
- Tapping power between one single cable and the ground is not possible.

Previous works focus on providing ac side grounding using additional grounding equipment to imitate bipolar operation, see Fig. 1.1c [23, 24]. The symmetrical monopolar MMC can adopt high resistance grounding at the neutral point for the interface transformer with Δ/Y arrangement (Y-connection on the MMC side). The neutral point grounding resistance may be only available in the medium-voltage and low-voltage applications due to large dc magnetic bias [24]. For Y/Δ arrangement (Δ-connection on the MMC side), artificially neutral point can be created by several methods such as star point reactor [23] and a zig-zag ground transformer [24]. The two pole power can be controlled independently if a suitable ground return path is

provided as shown in Fig. 1.1c. The star point reactor will consume massive reactive power and have insulation challenge for high voltage applications [24]. In any aforementioned method, it requires additional grounding device and has to be rated additionally.

An alternative solution is to use bipolar configuration as shown in Fig. 1.2a, which is common for multi-pulse LCC-based HVDC. This configuration offers a higher reliability and flexibility compared to Fig. 1.1b due to independently control of the positive and negative pole power injections. In addition, the system can export power at reduced loading using the healthy cable due to the pole-to-ground fault or single cable failure. However, the transformers utilized in a bipolar MMC system are required to withstand the dc bias voltage between windings caused by the series-stacking of MMCs, as illustrated by Fig. 1.2a.

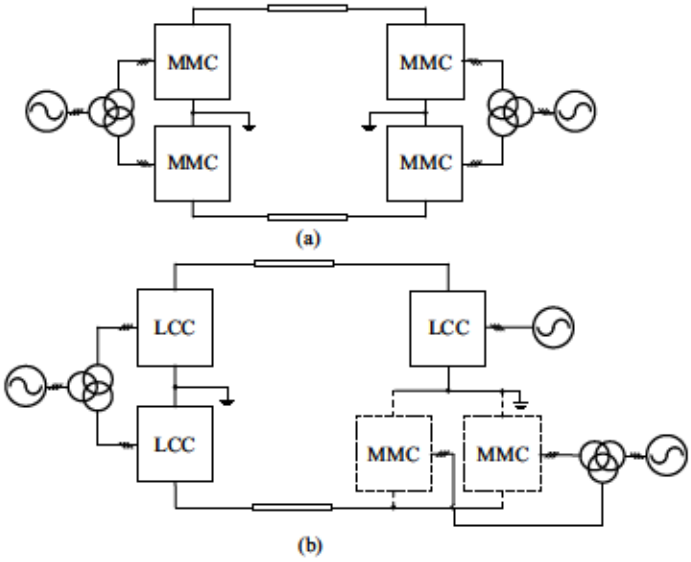

Figure 1.2: Bipolar configuration for MVDC and HVDC systems: (a) bipolar MMC, (b) bipolar hybrid LCC and MMC

Hybrid bipolar HVDC configurations such as shown in Fig. 1.2b are gaining research interests to obtain the advantages of both topologies [25, 26]. The hybrid bipolar HVDC configuration shown in Fig. 1.2b employs a pure LCC as rectifier and a serial LCC-VSC hybrid inverter station. The highest voltage level and capacity of currently operating projects are ±1100 kV and 12 GW for LCC-based HVDC transmission [27], and ±500 kV and 3 GW for MMC-based HVDC transmission [9]. For meeting the high power demand of LCC, multiple MMC converters (represented with dashed lines) in Fig. 1.2b are paralleled.

1.2 Review of State-of-the-art MMC-Based DC-DC Topologies for MVDC and HVDC

The aforementioned configurations are point-to-point MVDC and HVDC interconnections. Looking forward, an evolution from traditional two-terminal HVDC links to more complex multi-terminal HVDC grids is anticipated. Moreover, deploying a mixture of MVDC and HVDC systems would allow dc networks to exploit a wide range of voltage levels. Thus, dc-dc converters are one of the important building blocks of future dc grids [16, 28, 29]. They enable interconnection of different dc systems for power flow control, and can be augmented with advanced features such as dc fault blocking. Utilizing classical switched-mode dc-dc converters for HVDC applications is not practical due to the high current and voltage stresses for the semiconductors. The lack of modularity and scalability is another drawback. Much research attention has been focused on the development of dc-dc MMCs that series-cascade many low-voltage SMs to build up to the high operating voltages required. These dc-dc MMCs are inspired by the well known dc-ac MMC [5] that has gained widespread acceptance for HVDC, MVDC and flexible ac transmission system applications. The dc-ac MMC enjoys high modularity and scalability, low filtering requirements, and high efficiencies due to low equivalent switching frequency of the semiconductors.

The first dc-dc MMCs to arise for HVDC application were based on the DAB topology [30]. The generalization of this concept using two three-phase MMCs is presented in Fig. 1.3a. Primary (p) and secondary (s) MMCs are coupled on their ac sides via a transformer in a manner firstly proposed in [31]. The p and s arms comprise N_p and N_s series cascaded SMs, which can be HB or FB type, as shown in Fig. 1.3d; the latter can be used to accommodate dc link polarity reversals. This topology is sometimes referred to as a F2F-MMC. The F2F-MMC with half-bridge SMs provides galvanic isolation between dc terminals and has inherent dc-fault blocking capability due to the use of two separate MMCs. Many works on modeling, control and topology development of F2F-MMCs have been published, e.g., [32–36]. Similar to the two-stage F2F-MMC, another topology using DABs and MMC concepts is the cascaded multi-converter DAB [37]. The HV structure is built by paralleling or cascading low-power, low-voltage DAB converters as elementary cells. The high insulation requirement of the transformer for cascaded multi-converter DAB limits their use to the medium voltage range.

The two-stage isolated dc-ac/ac-dc conversion process in Fig. 1.3a requires full processing of the input power, i.e. $P_{ac} = P_{dc}$, inevitably leading to low utilization of installed SMs and higher losses. In an effort to reduce the losses, state-of-the-art

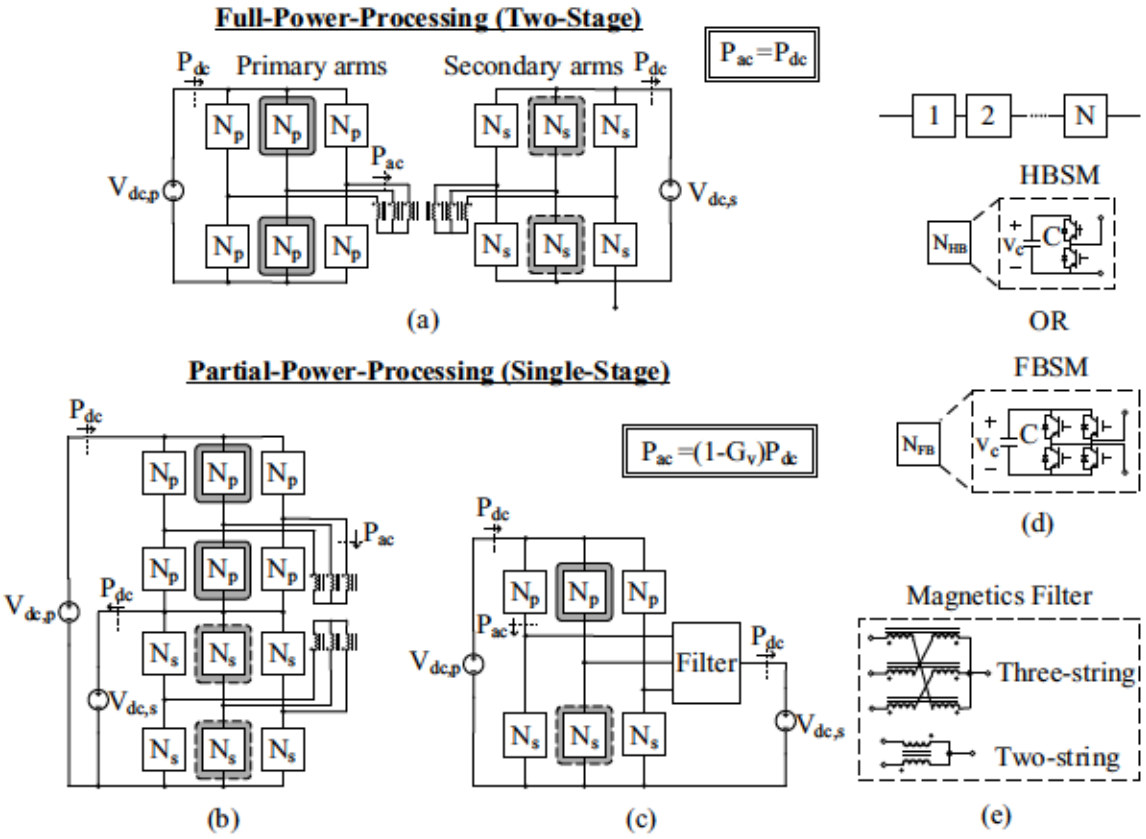

Figure 1.3: Exemplar dc-dc converters based on MMC: (a) F2F-MMC, (b) HVDC-AT [10], (c) M2DC [11, 12, 14], (d) SM circuits, (e) magnetics filter implementations

modular multilevel dc-dc converters have been proposed that exploit circulating ac power between switching cells to maintain balanced capacitor voltages and achieve a single-stage dc-dc conversion [16, 28, 29]. The HVDC-AT and M2DC in Figs. 1.3b and 1.3c are representative examples of the broader classes of partial-power-processing MMCs. Both facilitate dc-dc conversion by shuttling ac power between p and s arms using internal ac currents to ensure the capacitor power balance. The ac power processed by the M2DC and HVDC-AT depends on the dc step ratio, $G_v = V_{dc,s}/V_{dc,p}$, which is a fraction of the input dc power: $P_{ac} = (1-V_{dc,s}/V_{dc,p})P_{dc}$. For example, a dc step ratio of 0.5 provides a 50% reduction in the total number of SMs and associated operating losses for the same dc power transfer [38].

In Fig. 1.3b, the only difference from Fig. 1.3a is that $V_{dc,p}$ and $V_{dc,s}$ share a common reference point due to the series-stacking of the MMCs. The resulting dc-dc MMC structure is the HVDC-AT [10]. In contrast, the M2DC [11, 12, 14], shown in Fig. 1.3c, uses two arms with different number of SMs and a *filter* block. The M2DC is attracting much interest from academia and industry for HVDC systems, e.g., [39, 40].

The *filter* is added in Fig. 1.3c to enable dc power transfer by facilitating the flow of (only) dc currents while preventing circulating ac components from propagating to dc sides. Possible implementations include magnetics as shown in Fig. 1.3e for two-string and three-string M2DCs, passive filters, and additional submodules [16]. This filter is necessary for dc-dc power transfer between the dc ports and differentiates the M2DC from the conventional dc-ac MMC. This is a hallmark of the CCL power transfer mechanism [41]. The HVDC-AT instead exchanges the M2DC filter magnetics for a partial-power-processing ac transformer. Therefore, the HVDC-AT is so-called P3T type dc-dc MMC as its ac transformer is rated only for a portion of the nominal power transfer of the converter. CCL and P3T refer to the different dc-dc power transfer mechanisms being employed by the partial-power-processing topologies in Fig. 1.3. Other topologies that exploit internal ac power circulation to achieve partial-power-processing can be found in [42–47], however, they are partly modified versions of the HVDC-AT and M2DC.

Hereafter, the F2F-MMC will serve as the MMC reference topology for isolated two-stage dc-dc conversion topology, while the M2DC and HVDC-AT will serve as reference topologies for non-isolated partial-power-processing dc-dc MMC topologies. These converters have relative advantages and disadvantages when considering from a practical point of view, and there is not one topology that is suitable for all scenarios. A few literatures have investigated this research aspect. A fair cost comparison of the three dc-dc MMCs on semiconductor utilization effort, fault blocking capability, and efficiency regardless of the technology of installed semiconductors is carried out in [10, 41, 48–50]. However, some factors such as magnetic dc insulation requirement are not accounted. Table 1.1 summarizes the the main operational properties of the three topologies. The M2DC and HVDC-AT offer significant potential savings due to less ac power processed by the converter relative to the F2F-MMC. These savings come at the expense of relinquishing galvanic separation between dc terminals. The galvanic separation is the main characteristic that distinguishes isolated and non-isolated dc-dc MMC topologies. However, dc fault blocking that stops a fault on one dc system propagating to the other dc system can be achieved by using the requisite number of full-bridge SMs in the p arms [51]. Other submodule configurations, such as those studied in [52], can be utilized to potentially further reduce converter losses while maintaining fault interrupting capability. Dc circuit breaker is an alternative solution for interrupting dc fault currents [9, 22]. The main drawbacks of each topology are also listed in Table 1.1. The extremely high current on secondary arm of the M2DC is a significant challenge for high step ratio applications such as HVDC-MVDC grid interconnection and HVDC line power tapping. Some works have focused on control

Table 1.1: Characteristics of Two-Stage and Partial-Power-Processing DC-DC MMCs in Fig. 1.3

Parameter	**Two-Stage**	**Partial-Power-Processing**	
	F2F-MMC	HVDC-AT	M2DC
AC power processing, P_{ac}/P_{dc}	1	$1 - G_v$	$1 - G_v$
Galvanic separation	Yes	No	No
Fault blocking when fault on HV side	Yes	Yes*	Yes*
Fault blocking when fault on LV side	Yes	Yes	Yes
Magnetics footprint/weight	Larger	Small	Smaller
Dc voltage stress on magnetics	Yes	Yes	No
High dc step ratio suitability	Good	Good	Poor
Main drawbacks	Relatively high Loss and cost	Bulk and costly ac transformer	Extremely large arm currents for low G_v

* Requires sufficient FBSMs in primary arms

methods to reduce the ac currents needed in the M2DC for a given P_{dc} [53, 54], however, the resulting ac currents will still be inherently large when $V_{dc,p}$ and $V_{dc,s}$ are significantly different. The HVDC-AT does not have this problem because the ac transformer allows the arms ac currents to differ, but it will suffer from large dc voltage stresses between transformer windings. The resulting insulation requirements will cause increased cost and weight of the converter, which is a significant issue for applications where space is limited, for example, when designing dc collector systems for offshore wind farms with pure dc power systems [29, 55].

1.3 Motivation

Fig. 1.4a shows the dc and fundamental frequency (ac) currents within a single phase leg of each MMC for the dc-dc F2F-MMC in Fig. 1.3a. The dc and ac current (and power) flows are shown with red and blue arrows, respectively. Each phase leg in Fig. 1.4a enacts the same ac power transfer mechanism as the conventional dc-ac MMC. That is, the transformer connected at the midpoint of each phase leg carries only ac current (represented by blue arrows in Figs. 1.4a). The primary and secondary arms see different ac currents (ac_1 and ac_2). The SM capacitor power in each arm is self-balanced for dc-ac power conversion. That is, dc power absorbed (or generated) by each arm is balanced by average power that is generated (or absorbed) via synthesized

ac quantities. Each pair of MMC arms in primary and secondary side represents a MMC phase leg, where the number of SMs in each arm of one phase leg are the same. The dc and ac power transfers occur at separate nodes of each MMC structure. The ideal dc-ac conversion process provides natural cancellation of fundamental ac frequency voltages across each phase leg. This natural voltage cancellation is a salient feature of the modulation scheme, as it prevents a net fundamental frequency ac voltage from being imposed across the dc rails of the converter.

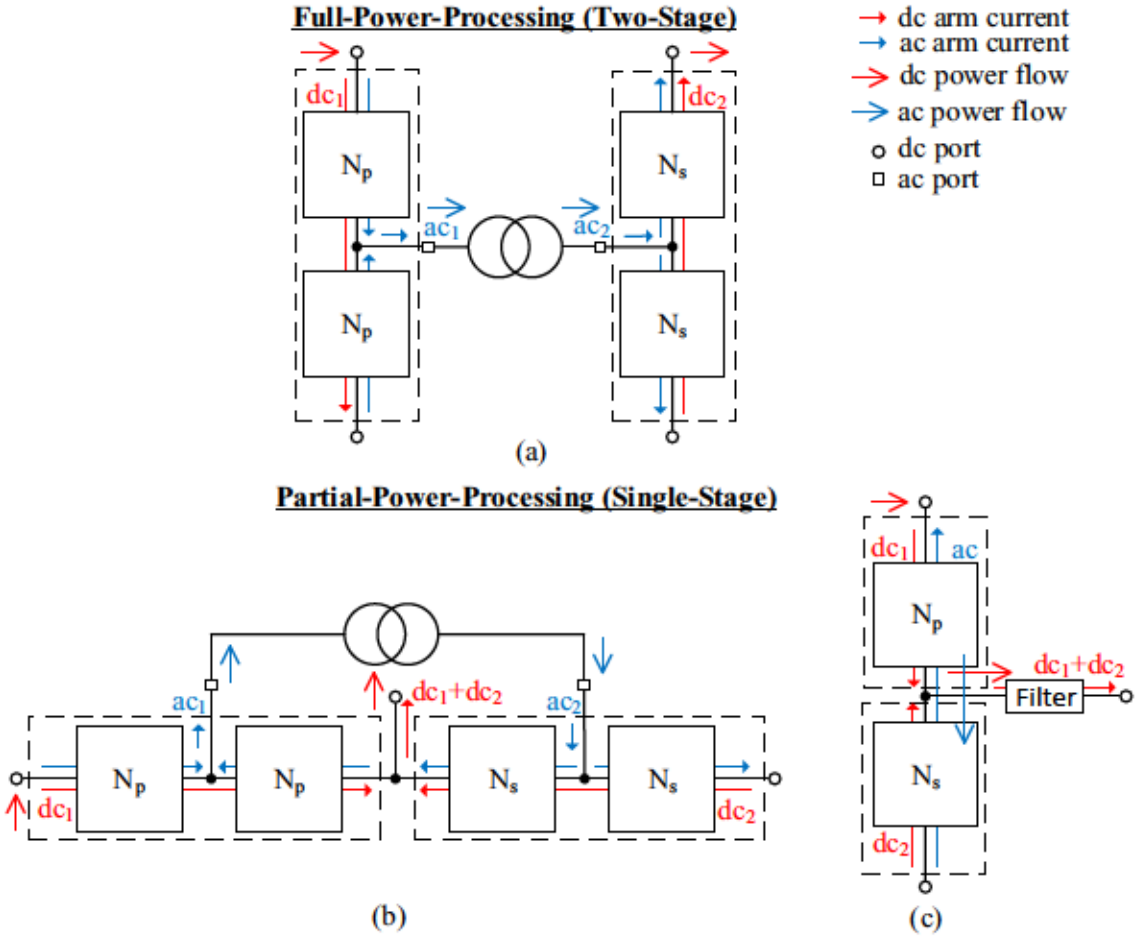

Figure 1.4: Single frequency power transfer in a single phase leg of MMCs: (a) dc-dc F2F-MMC in Fig. 1.3a, (b) dc-dc HVDC-AT in Fig. 1.3b. Multi-frequency power transfer in a single phase leg of MMC: (c) dc-dc M2DC in Fig. 1.3c

Now consider Fig. 1.4b that shows the dc and fundamental frequency (ac) current (and power) flows within a single phase leg of each MMC for the dc-dc HVDC-AT in Fig. 1.3b. Observe that the dc currents flowing between MMCs (represented by red arrows) in Fig. 1.4b are different from that in Fig. 1.4a, as two MMCs are being series-stacked in the HVDC-AT. The dc power is transferred through the midpoint between two MMCs. The MMC arms see unequal dc currents (dc_1 and dc_2) with opposite

directions as shown in Fig. 1.4b. Unlike in Fig. 1.4a, the SM capacitor power in each MMC arm in Fig. 1.4b cannot be self-balanced due to unequal dc currents between arms. In order to achieve steady-state SM capacitor power balance, average ac power is transferred between p and s arms through an ac transformer as shown in Fig. 1.4b (blue arrows), hence it is termed P3T type dc-dc MMC. Similar to Fig. 1.4a, each pair of arms in primary and secondary side represents a MMC phase leg. The dc and ac power transfers occur at separate nodes of each MMC structure.

Single frequency operation where dc and ac power transfers occur at separate nodes, as shown in Figs. 1.4a and 1.4b, is standard practice in MMCs. Now, consider Fig. 1.4c that shows the dc and fundamental frequency (ac) current (and power) flows for a single phase leg of the dc-dc M2DC in Fig. 1.3c. Here, only a single MMC structure (two phase arms) is needed. Similar to HVDC-AT, the SM capacitor power in each arm of the M2DC cannot be self-balanced as the MMC arms see unequal dc currents with opposite directions (dc_1 and dc_2). But instead of using a partial power processing transformer, the M2DC imposes a common circulating ac current between adjacent arms to exchange the ac power needed for charge balance of the SM capacitors, see arrows in Fig. 1.3c, hence it is termed CCL type dc-dc MMC. The two arms in one phase leg can in general have different number of SMs, N_p and N_s. Unlike the F2F-MMC and HVDC-AT in Figs. 1.4a and 1.4b, multi-frequency power transfer (both dc and ac) happen at the converter midpoint node of the M2DC. The amount of ac power exchanged between arms is the same as the HVDC-AT, yielding similar reductions in cost and losses relative to the F2F-MMC. The M2DC requires a filter (see Fig. 1.3e for common implementations) to provide a large fundamental frequency impedance to prevent ac currents from being injected into the dc output.

Utilizing single-stage CCL and P3T power transfer mechanisms offer advantages over adopting conventional dc-ac MMCs for two-stage dc-dc conversion. However, the existing non-isolated dc-dc MMCs still have drawbacks such as excessive current stresses at low stepping ratios and bulky and costly magnetics. Moreover, the capabilities of circulating ac current and multi-frequency power transfer have not yet been fully utilized in existing MMC topologies. By exploiting multi-tasking transformer enabled multi-frequency power transfer, there lies the opportunity to explore new applications where single-stage dc-dc MMC offer some advantages compared to using two MMCs operated in a front-to-front manner.

This thesis develops new MMC topologies that benefit from multi-frequency power transfer as postulated in Fig. 1.5. Firstly, Fig. 1.5a shows an alternative solution for non-isolated dc-dc MMC. Recall the M2DC in Fig. 1.4c exploits internal circulating ac currents and multi-frequency power transfer to achieve single-stage dc-dc conversion.

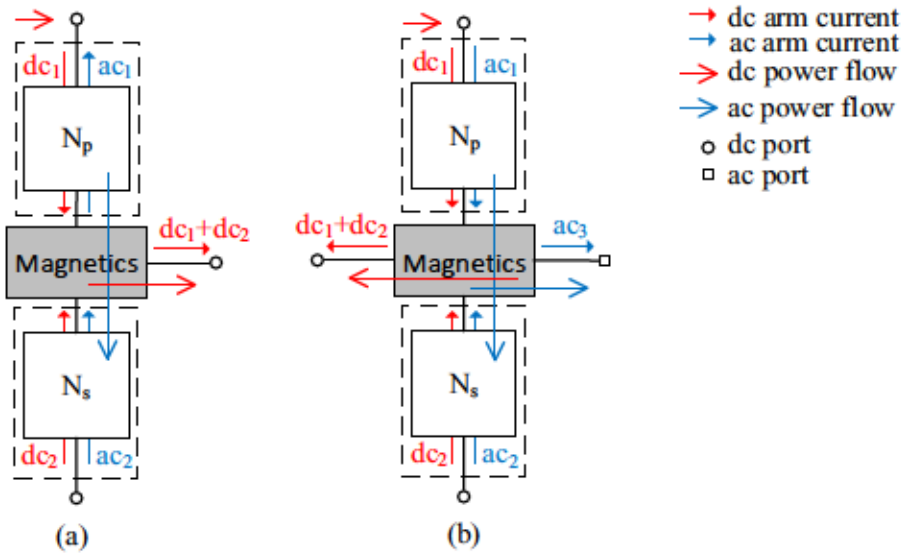

Figure 1.5: Multi-frequency power transfer in a single phase leg of MMCs: (a) dc-dc MMC that circulates different ac current (ac_1 and ac_2) between arms, (b) flexible dc-dc-ac MMC structure

However, the circulating ac currents are common to each pair of arms with identical direction and magnitude (see blue arrows in Fig. 1.4c). This results in extremely large arm ac currents for large dc step ratios, as indicated in Table 1.1. To solve this issue in Fig. 1.5a, the common mode circulating ac currents in each arm for SM power balancing have the same direction but different magnitudes (ac_1 and ac_2). Consequently, multi-frequency power transfer happens at the MMC midpoint node for both i) internally circulating ac power and ii) output dc power. This requires the postulated box comprising magnetics in Fig. 1.5a to have abilities of

1. Providing ac voltage matching between arms via transformer action;

2. Having winding currents with multiple frequency components while ensuring core dc flux cancellation;

3. Preventing propagation of ac currents to the dc output network.

Secondly, the concept of multi-frequency power transfer also opens the door to flexible dc-dc-ac MMC structures as postulated in Fig. 1.5b. That is, both ac and dc output power transfers occur at the MMC standard ac terminal. The ac current ac_3 enables the ac power transfer to the grid, while the dc current $dc_1 + dc_2$ enables dc power transfer to the output dc network. The circulating common mode ac current (ac_1 and ac_2) enables exchange of average ac power between two arm in each phase leg to ensure SM capacitor power balance. Exciting new MMC applications in dc

grids and hybrid ac/dc power systems can be derived based on this multi-frequency dc-dc-ac MMC structure, as will be shown in the thesis.

1.4 Thesis Scope

This research focuses on the development and application of new multi-frequency MMC topologies that build on the original dc-ac MMC concept. The high level objectives of this research can be stated as follows.

- Developing MMC structures that can benefit from multi-frequency power transfer including dc-dc MMC and dc-dc-ac MMC structures;
- Developing control schemes for the proposed MMC topologies;
- Identifying potential applications in mixed ac/dc grids including MVDC and HVDC systems that could profit from use of the proposed MMC structures;
- Performing comparative assessment of the proposed and emerging MMC topologies for high power applications.

Chapter 2 introduces a new class of non-isolated dc-dc MMC that allows the arms to carry different ac currents (see Fig. 1.5a). The proposed dc-dc MMC is further extended to a three-port MMC with external ac grid connectivity. Building upon this multi-frequency power transfer concept, Chapter 3 introduces a flexible dc-dc-ac MMC structure (see Fig. 1.5b), which is first investigated as a bipolar MMC with pole balancing capability for use in bipolar dc grids. Chapter 4 then studies use of the proposed dc-dc-ac MMC as a three-port converter for interconnecting different dc and ac systems. Chapter 5 provides a comparative assessment of the three-port MMCs for high-power operation and potential applications are identified. Each of these chapters discuss motivation, previous literature, research objectives and proposed solution and contributions individually. Chapter 6 discusses the overall contributions of the research and future work.

Chapter 2

Modular Multilevel DC Converter with Inherent Minimization of Arm Current Stresses

Dc-dc converters are one of the important building blocks of future dc grids [28, 29, 56]. They enable interconnection of different dc systems for power flow control, and can be augmented with advanced features such as dc fault blocking. Utilizing classical switched-mode dc-dc converters for HVDC applications is not practical due to the high current and voltage stresses for the semiconductors. The lack of modularity and scalability is another drawback.

Recently, research attention has been focused on the development of dc-dc MMCs that exploit the series-cascading of many low-voltage IGBT-based SMs to build up to the high operating voltages required [16]. The dc-dc MMC topologies retain the modularity and scalability features of the dc-ac MMC structure while facilitating energy conversion between two dc systems by different power transfer mechanisms. Generally, there are two principal ways of interconnecting dc systems using the MMC: two cascaded dc-ac stages with an intermediate ac link (i.e. dc-ac/ac-dc) or single stage dc-dc converters. The two principal ways also can be categorized as isolated and non-isolated topologies, respectively.

The large current stress and transformer winding isolation requirement issues of the existing non-isolated dc-dc MMC topologies (i.e. [11–14]) discussed in Section 1.2 will be well elaborated in this chapter. A new class of non-isolated dc-dc MMC that merges the best traits of the existing non-isolated dc-dc MMC topologies, based on Fig. 1.5a, is then presented in this chapter. Converter operation and dynamic controls are validated by simulation and experiment. The proposed dc-dc MMC uses a novel multi-frequency power transfer mechanism enabled by transformers that multi-task by imposing the windings to carry currents containing multiple frequency

components. It has the following advantages compared with existing non-isolated dc-dc MMC topologies.

- Ability to minimize ac currents and semiconductor effort across wide range of dc step ratios
- Avoidance of inter-winding dc voltage stresses for the magnetics.

2.1 AC Current Stress Issue in Existing DC-DC MMCs

The M2DC and HVDC-AT in Fig. 1.3 are partial-power-processing topologies. The amount of ac power processing is $P_{ac} = (1-G_v)P_{dc}$, where P_{ac} is the average ac power exchanged between p and s arms, $G_v = V_{dc,s}/V_{dc,p}$ is the dc step ratio and P_{dc} is the dc power transfer. P_{ac} is needed to satisfy charge balance of the SM capacitors, and is facilitated by ac currents that flow within the converters [57].

Figs. 2.1a and 2.1b show the dc and fundamental frequency components of the arm currents and voltages for a single phase leg of the M2DC (ref. Fig. 1.3c) and HVDC-AT (ref. Fig. 1.3b), respectively. The p and s arms comprise N_p and N_s series cascaded SMs, which can be HB or FB type, as shown in Fig. 1.3d. Higher order harmonics are neglected to focus on the ideal dc-dc conversion process. Each phase leg accommodates $P_{dc} = V_{dc,p}I_{dc,s}$.

Figs. 2.1a and 2.1b also lend insight into arm current stresses for the M2DC and HVDC-AT. For both topologies, the p arms support dc current $I_{dc,p}$ while the s arms support $(G_v^{-1} - 1)I_{dc,p}$. The dc currents are an unavoidable consequence of the P_{dc} demand. v_{ac} and i_{ac} are necessary to transfer average ac power between p and s arms in both the M2DC and HVDC-AT for capacitor charge balancing, i.e., satisfying P_{ac} criteria. However, the arms ac modulation differs between topologies. The HVDC-AT can impose different ac voltages between p and s arms by appropriate selection of transformer turns ratio n. This design parameter can be exploited to minimize ac current stresses of both p and s arms for any value of G_v. The M2DC has no such inherent capability and therefore suffers from higher ac current stresses.

Each primary arm (the same as secondary arm) in Fig. 2.1 must satisfy steady-state power balance criteria as

$$v_p^{dc} i_p^{dc} + \frac{1}{2}\hat{v}_p\hat{i}_p \cos\left(\theta_v - \theta_i\right) = 0, \tag{2.1}$$

where $v_p(t) = v_p^{dc} + \hat{v}_p \cos(\omega t + \theta_v)$ and $i_p(t) = i_p^{dc} + \hat{i}_p \cos(\omega t + \theta_i)$. For ease of analysis, it is assumed (i) arm inductors and transformer leakage inductance are

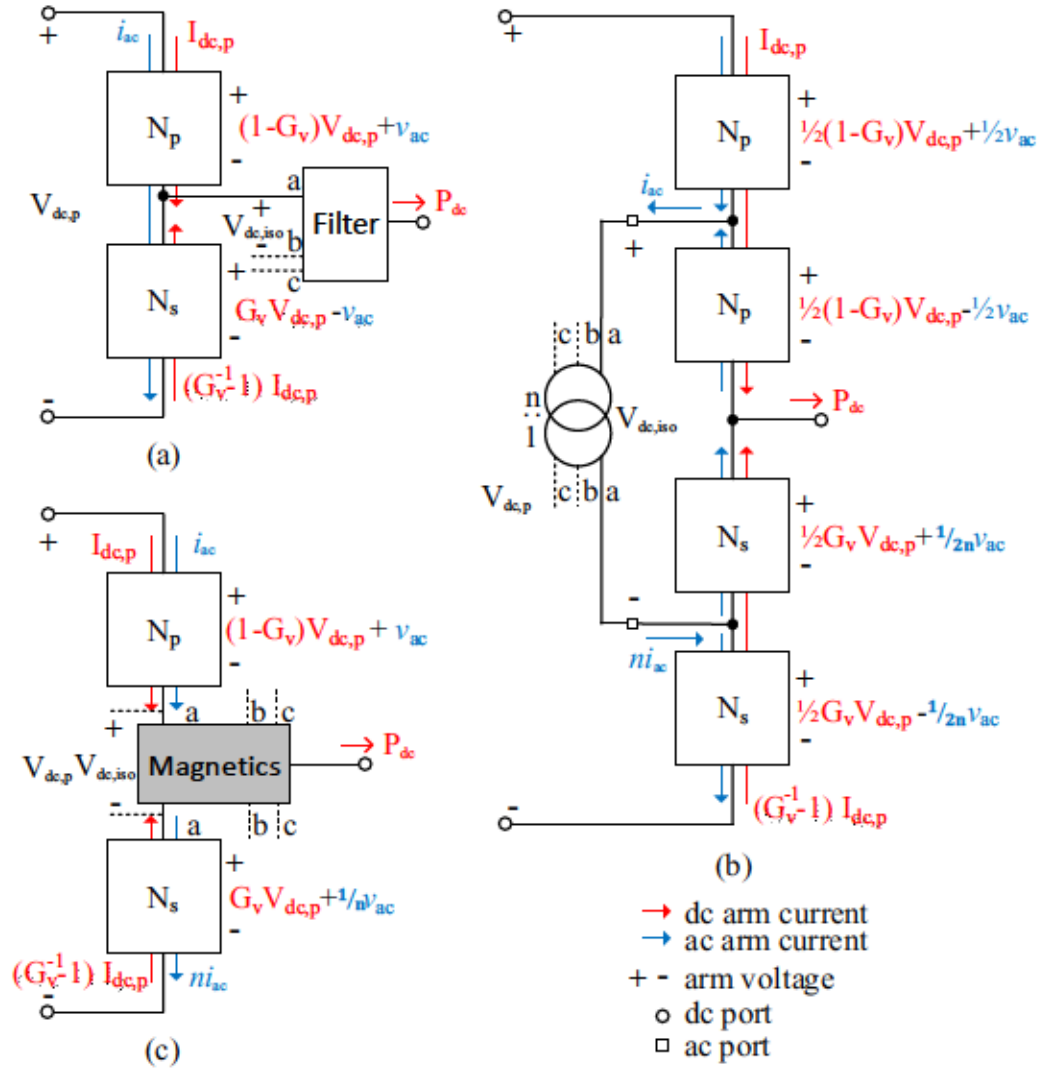

Figure 2.1: Dc and fundamental frequency quantities in a single leg for (a) M2DC in Fig. 1.3c, (b) HVDC-AT in Fig. 1.3b, (c) conceptualized topology with ideal features

Table 2.1: Inter-Winding DC Voltage Stress and Arm AC Current (p.u.) of DC-DC MMCs in Figs. 2.1a-c

	M2DC in Fig. 1.3c	HVDC-AT in Fig. 1.3b	Topology in Fig. 2.1c
$V_{dc,iso}$	0	$1/2V_{dc,p}$	0
$\hat{i}_p^{ac}/i_p^{dc}$	$2, \quad (0.5 \le G_v < 1)$ $2(1-G_v)/Gv, \quad (0 < G_v < 0.5)$	2	2
$\hat{i}_s^{ac}/i_s^{dc}$	$2G_v/(1-G_v), \quad (0.5 \le G_v < 1)$ $2, \quad (0 < G_v < 0.5)$	2	2

small, i.e., converter vars consumption is negligible, and therefore $\cos(\theta_v - \theta_i) \approx -1$, and (ii) losses are negligible. Recalling the dc components of p and s arm voltages are $(1 - G_v)V_{dc,p}$ and $G_v V_{dc,p}$ respectively, the arms ac current stresses for both the M2DC and HVDC-AT are then

$$\frac{\hat{i}_p}{i_p^{dc}} \approx 2(1 - G_v)\frac{V_{dc,p}}{\hat{v}_p} \qquad \frac{\hat{i}_s}{i_s^{dc}} \approx 2(G_v)\frac{V_{dc,p}}{\hat{v}_s}, \tag{2.2}$$

which have been normalized to the dc current of each arm. The p.u. ac current stresses depend on the dc step ratio G_v and also the peak ac voltage magnitude for the arm.

(2.2) motivates the maximization of ac arm voltages to minimize the ac currents. Assuming use of HBSMs, the simultaneous minimization of ac currents for p and s arms requires $\hat{v}_p = (1 - G_v)V_{dc,p}$ and $\hat{v}_s = G_v V_{dc,p}$, yielding 2 p.u. ac current in each arm. However, due to the absence of an internal ac transformer, the M2DC cannot achieve this optimal outcome as both arms must have the same ac voltage magnitude. The largest possible ac voltage for the M2DC arms is limited to the minimum dc voltage of either arm, i.e., $\hat{v}_p = \hat{v}_s = min\{(1 - G_v)V_{dc,p},\ G_v V_{dc,p}\}$ [51]. Combining this constraint with (2.2), the resulting normalized ac currents for p and s arms of the M2DC are given in Table 2.1. The optimal minimum 2 p.u. current can only be achieved at $G_v = 0.5$. For $G_v < 0.5$, the p arms exhibit > 2 p.u. ac current stress, while for $G_v > 0.5$ the s arms exhibit > 2 p.u. ac current stress.

Unlike the M2DC, the HVDC-AT in Fig. 2.1b uses an ac transformer to link p and s arms and can independently achieve maximal values $\hat{v}_p = (1 - G_v)V_{dc,p}$ and $\hat{v}_s = G_v V_{dc,p}$ in (2.2) by setting $n = (1 - G_v)/G_v$. Therefore, the HVDC-AT can achieve the minimum 2 p.u. ac current stress in all arms, across all values of G_v, as indicated in Table 2.1.

The preceding analysis offers insight into the fundamental operating characteristics of the M2DC and HVDC-AT. These features are direct consequences of their CCL and P3T power transformer mechanisms. In summary,

1. The HVDC-AT must tolerate large dc voltage stress ($V_{dc,iso} = 0.5V_{dc,p}$) between transformer windings, regardless of dc step ratio, which inevitably leads to increased size and weight of its transformer. However, the HVDC-AT can achieve the ideal minimum 2 p.u. ac current stresses for all arms regardless of G_v value.

2. The M2DC has no dc voltage insulation stress for the filter windings regardless of G_v value. However, it is plagued by increased ac current stresses for $G_v \neq 0.5$, which inevitably leads to increased semiconductor cost and higher conduction losses.

A new dc-dc MMC that merges the best traits of both topologies, i.e., lower ac current stresses for HVDC-AT and lower magnetics size and weight for M2DC, is conceptualized in Fig. 2.1c (and similarly Fig. 1.5a).

2.2 Proposed M2DC-CT

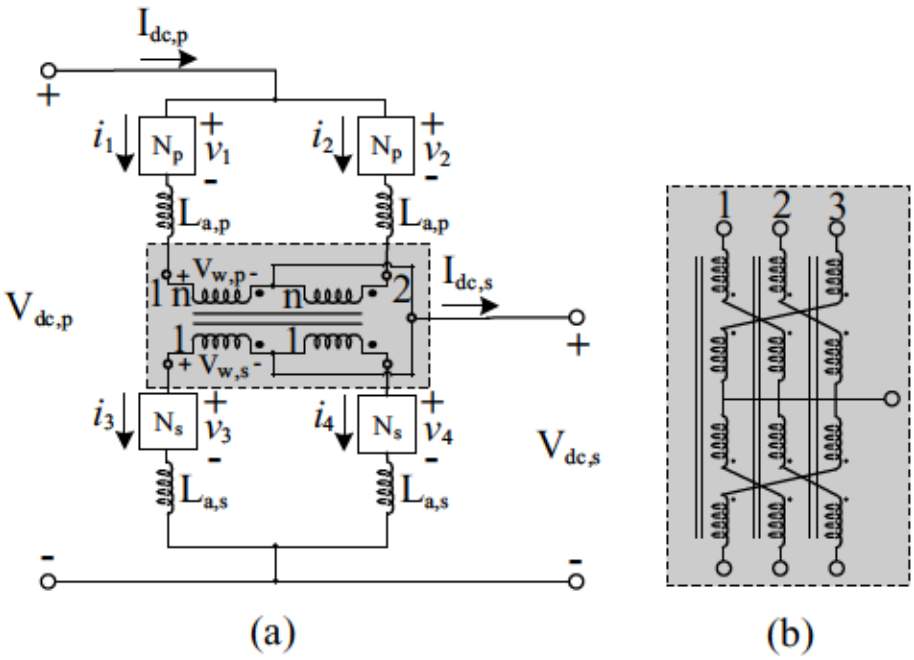

Figure 2.2: (a) Proposed two-string M2DC-CT (b) Magnetic structure suitable for three-string M2DC-CT

Fig. 2.2a proposes a new class of dc-dc MMC that satisfies the desired features of Fig. 2.1c by exploiting a center-tapped multi-winding transformer. Inter-arm ac voltage matching similar to the HVDC-AT is achieved by placing the transformer windings in series with the p and s arms. The lack of inter-winding dc voltage stress similar to the M2DC is achieved by locating the transformer at the converter midpoint, i.e., the transformer is flanked by p and s arms. The windings center-taps are linked together to allow power transfer to the dc output. Consequently, multi-frequency power transfer happens at the MMC midpoint node for i) internally circulating ac power and ii) output dc power. This novel multi-frequency power transfer mechanism requires the windings to carry both dc and ac currents, however, similar to the M2DC filter, the windings orientation provides core dc flux cancellation. The use of transformers in MMCs that handle dc and ac currents is an area of research interest [36, 58–62]. A more detailed design of the transformer that achieves dc flux

cancellation can be found in [59]. A detailed model of the similar transformer is derived in [63] for design propose. Hereinafter, the topology in Fig. 2.2a is referred to as the M2DC-CT as it utilizes the M2DC structure with an integrated center-tapped transformer.

The M2DC-CT in Fig. 2.2a consists of two interleaved phase legs and utilizes a single-phase ac transformer. The proposed two-string dc-dc MMC can be readily extended to a three-phase implementation by using a suitable magnetic structure that also achieves dc core flux cancellation, for example, as shown in Fig. 2.2b based on zig-zag transformer. Two-string and three-string variants have identical operating principles and thus this chapter focuses on the former. Three-string M2DC-CT will be discussed in Section 2.8.

2.3 Converter Analysis

2.3.1 Principle of Operation and Mathematical Modeling

Similar to the M2DC and HVDC-AT, the M2DC-CT is a partial-power-processing dc-dc MMC where $(1 - G_v)\%$ of P_{dc} is shuttled between p and s arms as average ac power. The M2DC-CT uses a new power transfer mechanism that is a hybrid of CCL and P3T mechanisms employed by the M2DC and HVDC-AT, respectively. The subsequent modeling and analysis assumes: (i) converter voltages and currents comprise dc and fundamental frequency components, (ii) energy conversion is lossless, and (iii) HBSMs are employed and thus $G_v = V_{dc,s}/V_{dc,p} \in [0, 1]$. The dc power throughput is $P_{dc} = V_{dc,p} I_{dc,p}$.

Figure 2.3 presents a time-averaged circuit model of the M2DC-CT. L_m, L_x are the magnetizing and leakage inductances for the transformer, and L_a, R_a are the arm inductance and resistance. Arm currents and voltages in Fig. 2.2a are denoted by $[i_1\ i_2\ i_3\ i_4]$ and $[v_1\ v_2\ v_3\ v_4]$, respectively. These physical quantities can be mapped into new abstract variables as illustrated by Fig. 2.3, by summing and subtracting quantities according to

$$[i_{t1}\ i_{t2}\ i_{c1}\ i_{c2}]^T = \mathbf{T_i}[i_1\ i_2\ i_3\ i_4]^T \tag{2.3}$$

$$[v_{t1}\ v_{t2}\ v_{c1}\ v_{c2}]^T = \mathbf{T_v}[v_1\ v_2\ v_3\ v_4]^T, \tag{2.4}$$

where

$$\mathbf{T_i} = \frac{1}{4}\begin{bmatrix} 2 & 2 & 2 & 2 \\ 4 & 4 & -4 & -4 \\ -1 & 1 & -\frac{1}{n} & \frac{1}{n} \\ -4n & 4n & 4 & -4 \end{bmatrix} \quad \mathbf{T_v} = \frac{1}{4}\begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \\ -1 & 1 & -n & n \\ -1 & 1 & n & -n \end{bmatrix}. \tag{2.5}$$

This mapping assigns transformer turns ratio $n = (1 - G_v)/G_v$ because it yields the minimum arm ac current stresses, as explained in section 2.1. Fig. 2.3 shows

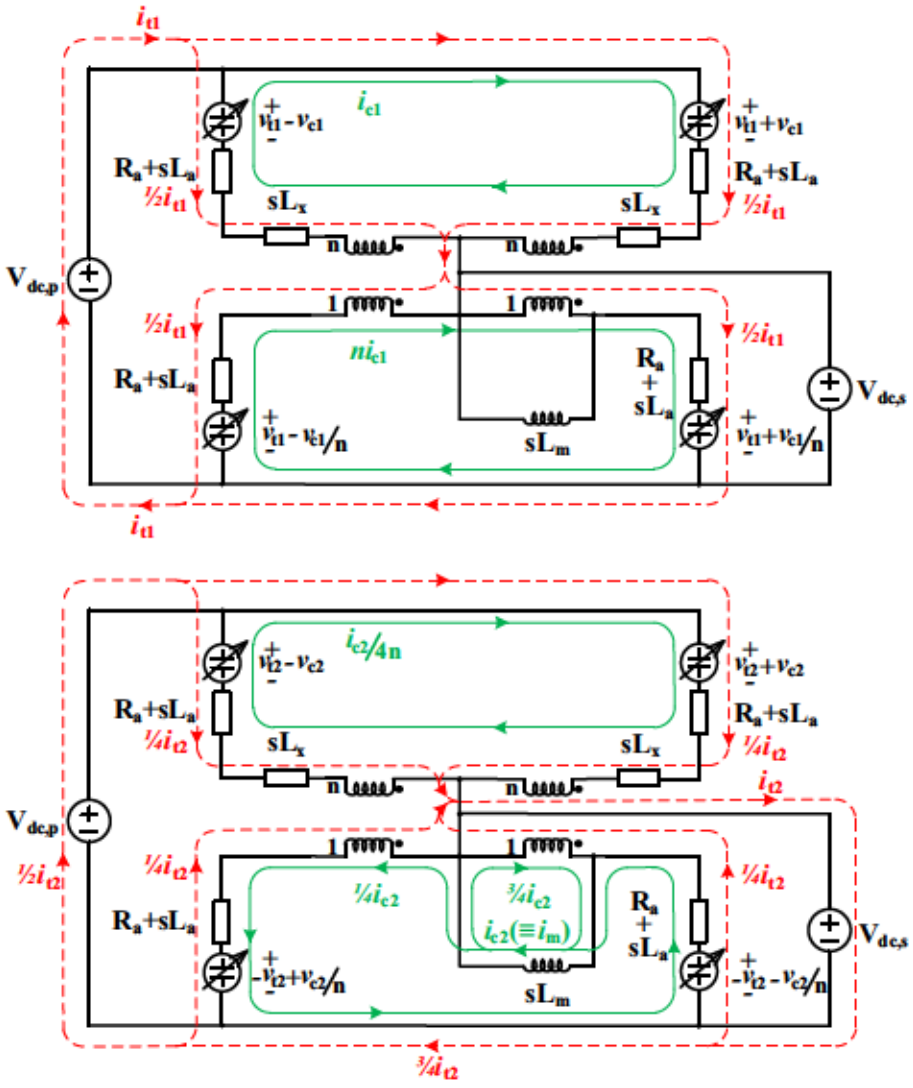

Figure 2.3: Time-averaged circuit model for M2DC-CT in Fig. 2.2a

the paths of $[i_{t1}\ i_{t2}\ i_{c1}\ i_{c2}]$ where subscripts t and c denote terminal and internal circulating currents, respectively. Each arm voltage is comprised of $[v_{t1}\ v_{t2}\ v_{c1}\ v_{c2}]$ as

shown. This mapping is based on previous works [41] where its been shown to offer decoupling of frequency content for currents and voltages.

The dc current paths are shown with red lines while internal circulating ac currents are represented using green lines in Fig. 2.3. The dc components in i_{t1} and i_{t2} represent power transfer between input and output dc networks, where $i_{t1} = I_{dc,p} - I_{dc,s}/2$ and $i_{t2} = I_{dc,s}$. Ideally, the dc components of i_{t1} and i_{t2} split evenly amongst the four arms. Requesting non-zero $I_{dc,s}$ (and hence a P_{dc} demand) will invoke a dc power imbalance between p and s arms, which ultimately causes a deviation in capacitor voltages from their nominal values. The fundamental frequency component of i_{c1} can be regulated to counteract this power imbalance and thus ensure balanced capacitor voltages, i.e., i_{c1} is the i_{ac} in Fig. 2.1c responsible for capacitor charge balancing. i_{c2} is a fundamental frequency current that sees the transformer magnetizing inductance, and thus is very small in practice. Ideally, the dc currents i_{t1} and i_{t2} split evenly amongst four arms. Thus, the magnetizing current only contains i_{c2} as shown in (2.6) due to windings orientation.

$$i_m = i_{c2} \tag{2.6}$$

Dynamic equations can be derived from Fig. 2.3, yielding

$$[(n^2+1)L_a + L_x]\frac{di_{c1}}{dt} = -(n^2+1)R_a i_{c1} - 2v_{c1} \tag{2.7}$$

$$(\frac{nL_m}{2} + \frac{nL_a}{4} + \frac{L_a}{4n} + \frac{L_x}{4n})\frac{di_{c2}}{dt} = -\frac{n^2+1}{4n}R_a i_{c2} - 2v_{c2} \tag{2.8}$$

$$(L_a + \frac{L_x}{2})\frac{di_{t1}}{dt} = -R_a i_{t1} - 2v_{t1} + V_{dc,p} \tag{2.9}$$

$$(L_a + \frac{L_x}{2})\frac{di_{t2}}{dt} = -R_a i_{t2} - 4v_{t2} + 4V_{dc,p} - 4V_{dc,s}. \tag{2.10}$$

(2.7)-(2.10) reveal that arm voltages $[v_{t1}\ v_{t2}\ v_{c1}\ v_{c2}]$ enable control of their respective currents, e.g., v_{t2} drives i_{t2}.

2.3.2 Arm Capacitors Power Balancing Process

To transfer dc power from input to output, the M2DC-CT must internally transfer $(1 - V_{dc,s}/V_{dc,p})$ p.u. of P_{dc} as average ac power between p and s arms. This is similar to the M2DC and HVDC-AT. The ac power processing is needed to satisfy capacitor charge balance for the arm capacitors. To elucidate this process, consider the steady-state power balance criteria for arms 1 and 3 in Fig. 2.2

$$(V_{dc,p} - V_{dc,s})\frac{I_{dc,p}}{2} + \frac{1}{2}\hat{v}_1\hat{i}_1\cos(\theta_{v1} - \theta_{i1}) = 0 \tag{2.11}$$

$$V_{dc,s}\frac{(I_{dc,p}-I_{dc,s})}{2}+\frac{1}{2}\hat{v}_3\hat{i}_3\cos(\theta_{v3}-\theta_{i3})=0, \tag{2.12}$$

where $\hat{v}_1$, $\hat{i}_1$ and $\hat{v}_3$, $\hat{i}_3$ are the fundamental frequency peak amplitudes of voltage and current for arms 1 and 3. As shown in Fig. 2.3, the ac quantities (those with subscript c) supported by these arms are v_{c1}, v_{c2} and i_{c1}, i_{c2}. However, in practice (i) $\hat{v}_{c1} << \hat{v}_{c2}$ as a relatively small v_{c1} is needed to drive rated i_{c1} with typical values of arm choke and leakage inductance L_a, L_x (ref. (2.7)), and (ii) $\hat{i}_{c2} << \hat{i}_{c1}$ as magnetizing inductance L_m is very large (ref. (2.8)) which suppresses i_{c2}. These simplifying approximations imply

$$\hat{i}_1\approx\hat{i}_{c1}\quad \hat{i}_3\approx n\hat{i}_{c1}\quad \hat{v}_1\approx\hat{v}_{c2}\quad \hat{v}_3\approx\frac{\hat{v}_{c2}}{n}. \tag{2.13}$$

Applying these approximations to (2.11)-(2.12), along with lossless relationships $V_{dc,s}=G_vV_{dc,p}$ and $I_{dc,p}=G_vI_{dc,s}$, yields

$$(1-G_v)V_{dc,p}\frac{I_{dc,p}}{2}+\frac{1}{2}\hat{v}_{c2}\hat{i}_{c1}\cos(\theta_{v1}-\theta_{i1})=0 \tag{2.14}$$

$$-(1-G_v)V_{dc,p}\frac{I_{dc,p}}{2}+\frac{1}{2}\hat{v}_{c2}\hat{i}_{c1}\cos(\theta_{v3}-\theta_{i3})=0. \tag{2.15}$$

(2.14)-(2.15) confirm arms 1 and 3 must exchange an average ac power equal to $0.5(1-G_v)P_{dc}$ for capacitor charge balancing. The key ac quantities responsible for this power transfer are the fundamental frequency components of v_{c2}, i_{c1}.

2.3.3 Arms Current Stresses

Based on (2.14)-(2.15), the peak ac current seen by p and s arms assuming converter internal vars consumption is small is

$$\hat{i}_{c1}\approx\frac{P_{dc}(1-G_v)}{\hat{v}_{c2}}. \tag{2.16}$$

$\hat{i}_{c1}$ can be minimized by maximizing ac arm voltage $\hat{v}_{c2}$, which is consistent with (2.2). For the M2DC-CT with HBSMs, the maximal value of $\hat{v}_{c2}$ is limited to the minimum dc voltage component of p and s arms

$$\hat{v}_{c2}\le\min\{(1-G_v)V_{dc,p},\ nG_vV_{dc,p}\}. \tag{2.17}$$

To maximize the ac voltage for both p and s arms across all values of G_v, the transformer turns ratio is chosen as

$$n=(1-G_v)/G_v, \tag{2.18}$$

Then, $\hat{v}_{c2}$ can be expressed as

$$\hat{v}_{c2} = (1 - G_v) V_{dc,p} M_{c_2}, \tag{2.19}$$

where $M_{c_2} \in [0, 1]$ is the ac modulation index. Recalling (2.16), the ratio of fundamental frequency to dc current carried by p and s arms (e.g., arms 1 and 3 in Fig. 2.2a) is

$$\frac{\hat{i}_1}{\frac{I_{dc,p}}{2}} = \frac{\hat{i}_3}{\frac{I_{dc,p}}{2}\left(\frac{1-G_v}{G_v}\right)} = \frac{2}{M_{c2}}. \tag{2.20}$$

When maximizing ac arm voltages, i.e., $M_{c_2} = 1$, the ac current stresses for the M2DC-CT is 2 p.u. in both p and s arms. This corresponds to the optimal conditions in Fig. 2.1c.

2.4 Converter Controls

Open-loop control of M2DC-CT does not maintain balanced SM capacitor voltages during varying power flow requirements. Fig. 2.4 proposes a dynamic controller for the two-string M2DC-CT to address the operational challenges. Table 2.2 summarizes the corresponding control objectives based on the discussion in section 2.3: i) resulting dynamics are (ideally) decoupled, and ii) only one frequency component exists in each state variable, given by (2.7)-(2.10), which corresponds to a distinct converter power transfer mechanism. The controls are apportioned into two different blocks: (i) output power regulation, and (ii) capacitor voltage balancing, where

- The output power regulation scheme regulates the dc component of i_{t2} to provide the desired dc power throughput P_{dc} via PI control
- The capacitor voltage balancing scheme has two cascaded control loops: i) an outer voltage loop that regulates the dc component of sum and difference capacitor voltages $\Sigma v_{cap,t1}/\Delta v_{cap,t2}$ via PI control to their set-points, and ii) an inner current loop that regulates i_{t1}/i_{c1} via PI control / PR control. The closed-loop response of i_{t1}/i_{c1} is designed to be significantly faster than $\Sigma v_{cap,t1}/\Delta v_{cap,t2}$. For example, the closed-loop response for i_{t1}/i_{c1} can be on the order of milliseconds and the closed-loop response for $\Sigma v_{cap,t1}/\Delta v_{cap,t2}$ on the order of hundreds of milliseconds. Where

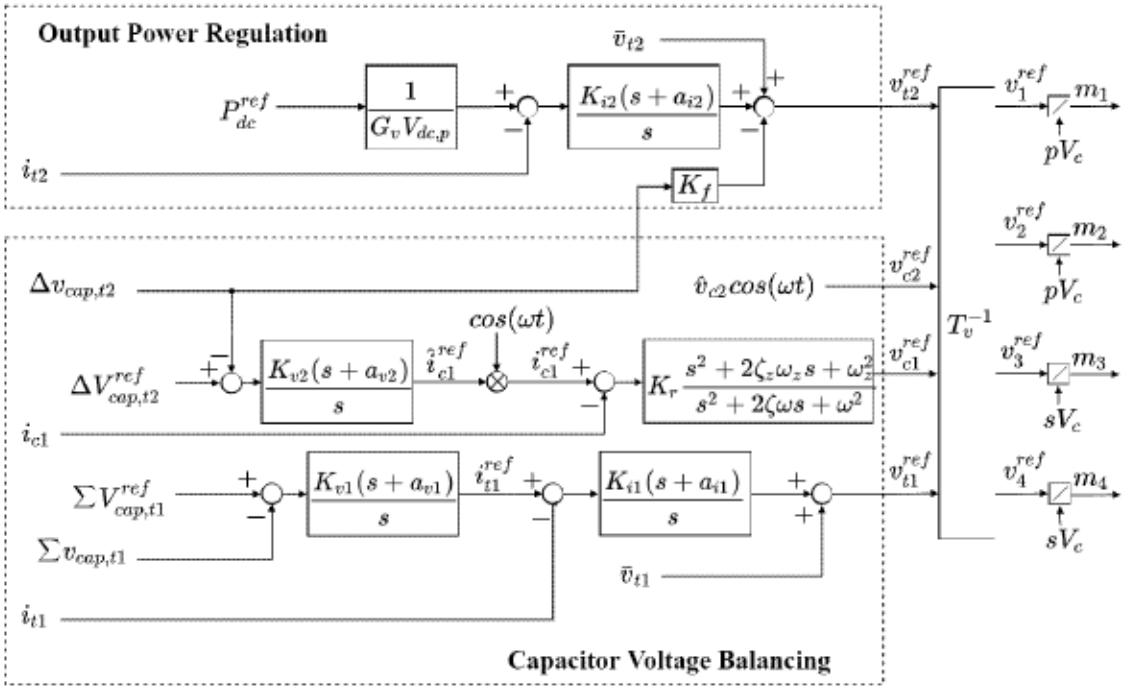

Figure 2.4: Proposed dynamic controls for the M2DC-CT

Table 2.2: Control Objectives for M2DC-CT Currents

Current	Frequency Component	Control Goal
i_{t1}	dc	$\Sigma v_{cap,t1}$ regulation
i_{t2}	dc	P_{dc} regulation
i_{c1}	fundametal frequency (ac)	$\Delta v_{cap,t2}$ regulation

$$\begin{bmatrix} \Sigma v_{cap,t1} \\ \Delta v_{cap,t2} \end{bmatrix} = \frac{1}{4}\begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \end{bmatrix}\begin{bmatrix} \Sigma v_{c,1,j} \\ \Sigma v_{c,2,j} \\ \Sigma v_{c,3,j} \\ \Sigma v_{c,4,j} \end{bmatrix}. \tag{2.21}$$

The $\Delta v_{cap,t2}$ capacitor voltage balancing loop ensures any dc imbalance between p and s arms is regulated to zero via feedback control of the fundamental frequency component of i_{c1}. This ac current interacts with ac arm voltage v_{c2} to exchange the requisite average ac power between arms, as given by (2.14)-(2.15). In contrast, the $\Sigma v_{cap,t1}$ capacitor voltage balancing loop can charge/discharge all capacitor voltages together by appropriate control of the dc component of i_{t1}. $\Sigma V_{cap,t1}^{ref} = 0.25(p+s)V_c$

and $\Delta V_{cap,t2}^{ref} = 0.25(p-s)V_c$, where V_c is the nominal SM capacitor voltage.

The dynamic controller produces control terms v_{c1}^{ref}, v_{c2}^{ref}, v_{t1}^{ref}, v_{t2}^{ref} which are transformed into physical arm voltages based on (2.4). The nominal dc values of v_{t1} and v_{t2} are expressed as follows:

$$\bar{v}_{t1} = \frac{1}{2}V_{dc,p} \quad \bar{v}_{t2} = \frac{1}{2}(1-2G_v)V_{dc,p} \tag{2.22}$$

Assuming the number of SMs in primary and secondary arm are p and s, respectively. The capacitor voltage states $[\Sigma v_{c,1,j}\ \Sigma v_{c,2,j}\ \Sigma v_{c,3,j}\ \Sigma v_{c,4,j}]$ are regulated by capacitor voltage balancing controller to be dc valued as

$$[\Sigma V_{c,1,j}\ \Sigma V_{c,2,j}\ \Sigma V_{c,3,j}\ \Sigma V_{c,4,j}]^T = V_c \cdot [p\ p\ s\ s]^T \tag{2.23}$$

where V_c is the nominal SM capacitor voltage. The arm modulating signals for each arm are denoted by $[m_1\ m_2\ m_3\ m_4]$. The relation between the physical arm voltages $[v_1\ v_2\ v_3\ v_4]$ and arm modulating signals $[m_1\ m_2\ m_3\ m_4]$ is defined as

$$[v_1\ v_2\ v_3\ v_4]^T = [m_1\ m_2\ m_3\ m_4] \cdot [pV_c\ pV_c\ sV_c\ sV_c]^T, \tag{2.24}$$

2.5 Simulation Results

This section presents the simulations results for the two-string M2DC-CT based on Fig. 2.2a. Simulations are conducted in PSCAD/EMTDC using a detailed equivalent switching model. Voltage balancing of capacitors within each arm is achieved using the sort and selection method. Three steady-state operating scenarios corresponding to different values of conversion ratio G_v are simulated:

1. $V_{dc,p} = 400$ kV, $V_{dc,n} = 50$ kV ($G_v = 0.125$), $P_{dc} = 75$ MW.
2. $V_{dc,p} = 400$ kV, $V_{dc,n} = 200$ kV ($G_v = 0.5$), $P_{dc} = 400$ MW.
3. $V_{dc,p} = 400$ kV, $V_{dc,n} = 300$ kV ($G_v = 0.75$), $P_{dc} = 400$ MW.

As representative examples showing the dynamic control validation of two-string M2DC-CT, two operating scenarios corresponding to two conversion ratio G_v are simulated:

1. $V_{dc,p} = 400$ kV, $V_{dc,n} = 50$ kV ($G_v = 0.125$), from $P_{dc} = 0$ MW to $P_{dc} = 75$ MW at t = 0.05 sec and from $P_{dc} = 75$ MW to $P_{dc} = -75$ MW at t = 0.25 sec.
2. $V_{dc,p} = 400$ kV, $V_{dc,n} = 100$ kV ($G_v = 0.25$), from $P_{dc} = 0$ MW to $P_{dc} = 200$ MW at t = 0.05 sec and from $P_{dc} = 200$ MW to $P_{dc} = -200$ MW at t = 0.25 sec.

For each simulation cases, the i) primary and secondary dc currents, ii) primary and secondary arm currents, iii) primary and secondary arm voltages, iv) exemplar SM capacitor voltages in each arm and v) abstract mapped arm currents are plotted.

2.5.1 Design Considerations

The following discussion highlights key converter design considerations for the simulated case study of $G_v = 50/400 = 0.125$. Similar design principles would apply for other dc step ratios. The two-string M2DC-CT is designed as an HVDC/MVDC interconnect with 400/50 kV dc ratio ($G_v = 0.125$) and 75 MW rated dc power transfer. The dc step ratio $G_v = 0.125$ implies selecting $n = 7$ from (2.18) to minimize the ac current in each arm. The primary and secondary arms in Fig. 2.2a must support dc voltages of 350 kV and 50 kV, respectively. Considering also the SM capacitor voltage rating is 2 kV and that HBSMs are used to maximize the synthesized ac arm voltages, the number of SMs in primary and secondary arms are chosen to be 350 and 50, respectively. Thus, each of the primary and secondary side windings of the center-tapped transformer are rated for 222.7 kV_{rms} and 31.8 kV_{rms} (assuming a modulation index of 0.9), respectively. The primary windings need to carry 0.094 kA_{dc} and approximately 0.208 kA_{pk} ac at rated power transfer, which corresponds to 0.174 kA_{rms} winding current rating. Similarly, the transformer secondary windings need to carry 0.656 kA_{dc} and approximately 1.458 kA_{pk} ac, which corresponds to 1.222 kA_{rms}. The resulting transformer VA rating is approximately 77.5 MVA.

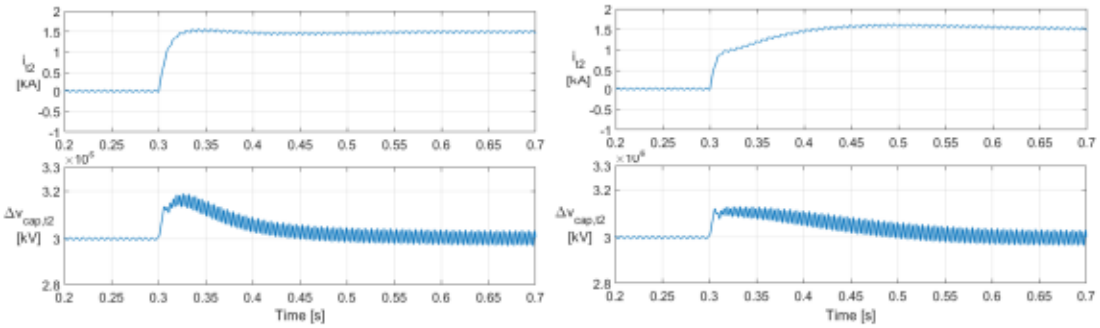

Figure 2.5: M2DC-CT waveforms for step-change in P_{dc}^{ref} from 0 MW to +75 MW at t = 0.3 sec with feed-forward gain $K_f = 0.12$ and $K_f = 0$

It is worth mentioning that the dynamic phasor model of M2DC derived in [65] identifies an inter-state dynamic coupling between i_{t2} and $\Delta v_{cap,t2}$. Therefore, feed-forward gain K_f is added in Fig. 2.4 to decouple i_{t2} and $\Delta v_{cap,t2}$ dynamics, and thus improve current dynamics of M2DC-based topologies [41]. This is demonstrated by Fig. 2.5. Observe it_2 no longer exhibits a first-order type response after setting $K_f =$

0.12. Additionally, the settling time for it_2 has also decreased by the appropriately selection of K_f.

Table 2.3: Simulation Parameters for M2DC-CT with $V_{dc,p} = 400$ kV, $V_{dc,n} = 50$ kV ($G_v = 0.125$) and $P_{dc} = 75$ MW

Converter Parameters	Value
Primary and secondary dc voltages, $V_{dc,p}/V_{dc,n}$	400 kV/50 kV
Conversion ratio, G_v	0.125
Input power, P_{dc}	75 MW
Fundamental frequency, ω	$2\pi 150$[1] rad/s
Primary/secondary arm no. of SMs, N_p/N_s	350/50 (HBSMs)
Primary/secondary arm SM capacitor, C_p/C_s	2 mF/14 mF
Primary/secondary arm choke, $L_{a,p}/L_{a,s}$	60 mH/1.2 mH
Nominal SM capacitor voltage, V_c	2 kV
Line impedance, L_s, R_s	40.5 mH, 1.65 Ω
Transformer Parameters	**Value**
Transformer power rating, S_w	77.8 MVA
Turns ratio, n	7:1
Primary/secondary winding voltages, V_p/V_s	247.5 kV/35.4 kV (rms)
Leakage inductance, L_x	10 mH
Magnetizing current	1%
Controller Parameters	**Value**
K_{i1}, K_{i2}, a_{i1}, a_{i2}, K_f	50, 1.5, 10, 20, 0.12
K_{v1}, K_{v2}, a_{v1}, a_{v2}	0.045, 0.006, 15, 30
K_r, ζ, ζ_z, ω_z	10, 0.1, 1.2, 942 rad/s
$\bar{v}_{t1}$, $\bar{v}_{t2}$, $\hat{v}_{c2}$	200 kV, 150 kV, 45 kV
$\Sigma v^{ref}_{cap,t1}$, $\Delta v^{ref}_{cap,t2}$	400 kV, 300 kV

A key benefit of the multi-string M2DC-CT is that the return path for circulating ac currents does not include the dc input line. That is, fundamental frequency currents remain internal to the converter structure. The SM capacitances are picked to yield peak-to-peak capacitor voltage ripples of around 5% for the p and s arms. The arm reactor has a value of 10% on the system impedance base. Note that the arm chokes in s arms differ from that in p arms due to the different current distribution in each arm. The primary and secordary side dc line inductors are selected in a way that both peak-to-peak current ripples are below 10% [50]. The parameters for the controllers are selected to give settling times of around 100 ms for the dc output current i_{t2} and

[1]The fundamental ac frequency is set to 150 Hz in consistent with other industry studies due to the trade-off between switching losses and magnetic size [64]

150 ms for the capacitor voltages $\Sigma v_{cap,t1}$ and $\Delta v_{cap,t2}$. Simulation parameters for $G_v = 0.125$ are given in Table 2.3.

2.5.2 $G_v = 0.125$ Waveforms

Fig. 2.7 show simulation results of the converter operating at $V_{dc,p} = 400$ kV, $V_{dc,n} = 50$ kV, $P_{dc} = 75$ MW. The ac component in primary and secondary arm is 210 A_{pk} and 1.45 kA_{pk}. Thus, the 150 Hz component of the mapped arm current i_{c1} is 210 A_{pk}. The i_1, i_2 (p arm currents) and i_3, i_4 (s arm currents) waveforms verify the total dc power transfer is shared equally between strings, as each string carries the same average current. The identical dc current in both strings ensure core dc magnetic flux cancellation due to windings orientation. Thus, the magnetizing current i_{c2} (ref. (2.6)) as shown in Fig. 2.7 has a negligibly small 150 Hz component (as expected) due to the large transformer magnetizing impedance but has no dc component. The fundamental frequency currents are 180° phase-shifted between strings, yielding ac current cancellation at the dc terminals as expected. However, the naturally occurring second harmonic currents in each string do not cancel, but, rather, sum together at the dc rails. Therefore, $I_{dc,p}$ and $I_{dc,s}$ contain a small second harmonic component. The summation of second harmonic currents at the dc input and dc output rails is uniquely different from the conventional three-phase dc/ac MMC, where second harmonic currents naturally circulate between phase legs. However, the three-phase M2DC-CT implementation won't have the second harmonic currents at the dc input and dc output rails as demonstrated in Section 2.8. i_{t2} has a dc component of 1.5 kA which is the outcome of P_{dc} control, as $I_{dc,s} = i_{t2}$. i_{t1} has a dc component of -562.5 A where $I_{dc,p} = i_{t1} + i_{t2}/2$.

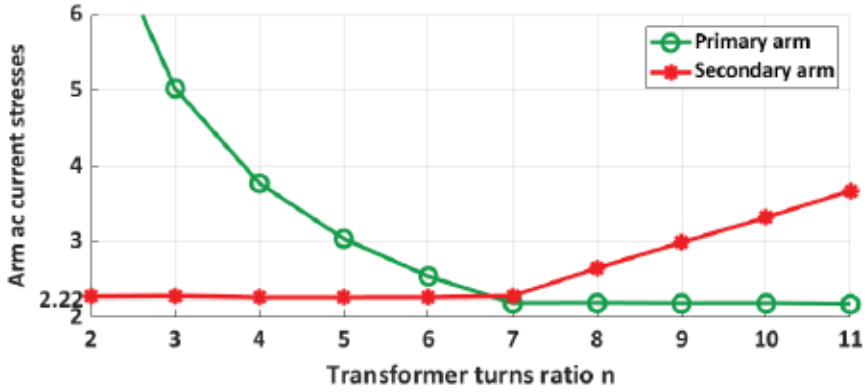

Figure 2.6: The primary and secondary arm current stress of M2DC-CT operating at $V_{dc,p} = 400$ kV, $V_{dc,n} = 50$ kV, $P_{dc} = 75$ MW with different transformer turns ratio

Additional simulations of two-string M2DC-CT with 400/50 kV dc ratio and 75 MW rated dc power transfer has been carried out by using transformer turns ratio other than $n = 7$. As expected, the results imply that the proposed dc–dc converter is utilized most efficiently when the ratio of input to output voltage is close to the transformer turns ratio $n - 1$ as shown in Fig. 2.6.

2.5.3 $G_v = 0.5$ Waveforms

Fig. 2.8 show simulation results of the converter operating at $V_{dc,p} = 400$ kV, $V_{dc,n} = 200$ kV, $P_{dc} = 400$ MW. For minimizing the ac current in each arm, the transformer turns ratio are chosen to be $(Gv^{-1} - 1) = 1$ based on (2.18). The primary dc current $I_{dc,p} = 1$ kA, while the secondary dc current $I_{dc,s} = 2$ kA. Thus, the dc and ac components in each arm is 0.5 kA_{dc} and 1.14 kA_{pk}. i_{t2} has a dc component of 2 kA, as $I_{dc,s} = i_{t2}$. i_{t1} has a dc component of 0 kA where $I_{dc,p} = i_{t1} + i_{t2}/2$. The 150 Hz component of i_{c1} is 1.14 kA_{pk}. The primary and secondary arms must support dc voltages of 200 kV and 200 kV, respectively. The peak primary arm and peak secondary arm ac voltages are around 180 kV_{pk} ($M_{c2} = 0.9$).

2.5.4 $G_v = 0.75$ Waveforms

Fig. 2.9 show simulation results of the converter operating at $V_{dc,p} = 400$ kV, $V_{dc,n} = 300$ kV, $P_{dc} = 400$ MW. For minimizing the ac current in each arm, the transformer turns ratio are chosen to be $1/Gv - 1 = 1/3$ based on (2.18). The primary dc current $I_{dc,p} = 1$ kA, while the secondary dc current $I_{dc,s} = 1.5$ kA. Observe the primary arms for $G_v = 0.5$ and $G_v = 0.75$ have equal dc and peak ac current stresses. However, the secondary arms exhibit lower peak current stresses for $G_v = 0.75$ as $I_{dc,s}$ has decreased from 2 kA ($G_v = 0.5$) to 1.33 kA ($G_v = 0.75$). i_{t2} has a dc component of 1.33 kA, as $I_{dc,s} = i_{t2}$. i_{t1} has a dc component of 0.33 kA where $I_{dc,p} = i_{t1} + i_{t2}/2$. The 150 Hz component of i_{c1} is 1.14 kA_{pk}. The primary and secondary arms must support dc voltages of 200 kV and 200 kV, respectively. The peak primary arm and peak secondary arm ac voltages are around 180 kV_{pk} ($M_{c2} = 0.9$).

In summary, the behaviour of the M2DC-CT is similar to the conventional dc/ac MMC, where second harmonic ac currents naturally circulate between phase legs [66]. This can be seen with the capacitor voltage waveforms. SM capacitor voltages $v_{c,1}$, $v_{c,2}$, $v_{c,3}$, $v_{c,4}$ are dominantly fundamental ac and dc valued as expected, however, contains a small second harmonic component. The second harmonic component in arm currents i_1, i_2, i_3, i_4 are incited by capacitor ac ripple voltage. Similar to the dc/ac MMC, a multi-string (two-string in this case) architecture is needed to ensure

net fundamental ac current cancellation (fundamental ac current are phase-shifted by 180° between strings) between at the dc input and output rails of the converter. However, the second harmonic ac currents in two strings of the M2DC-CT have the same phase, thus, cannot cancel at the dc input and output rails. Simulation results validate that primary dc current $i_{dc,p}$ and secondary dc current $i_{dc,s}$ are dominantly dc valued as expected and naturally contain a small second harmonic components (300 Hz). Moreover, fundamental ac current cancellation occurs independent of step ratio G_v. These harmonic currents are not responsible for primary energy transfer between arms and therefore can be suppressed via suitable control action. The use of supplemental converter controls to mitigate undesirable second harmonics is a well established practice for the dc/ac MMC [57].

The i_1, i_2 (p arm currents) and i_3, i_4 (s arm currents) waveforms in Figs. 2.7-2.9 verify that the M2DC-CT can realize inherent minimization of ac arm currents similar to the HVDC-AT. Apart from the simulated cases above, Table 2.4 provides the per-unitized current stresses for the M2DC-CT at G_v range from 1/8 to 7/8. Both primary

Table 2.4: Frequency Analysis of Simulated M2DC-CT Arm Currents and Calculated M2DC Arm Currents at Rated Power

	M2DC-CT [Simulated]		M2DC [calculated for comparison]	
	Primary	Secondary	Primary	Secondary
G_v	(p.u.)	(p.u.)	(p.u.)	(p.u.)
1/8	2.188	2.286	**15.556**	2.222
2/8	2.211	2.280	**6.667**	2.222
3/8	2.201	2.279	**3.704**	2.222
4/8	2.174	2.272	2.222	2.222
5/8	2.179	2.275	2.222	**3.704**
6/8	2.203	2.267	2.222	**6.667**
7/8	2.211	2.257	2.222	**15.556**

and secondary ac arm currents in the M2DC-CT are near the 2 p.u. minimal value, as given by Fig. 2.1c (and also by (2.20) assuming $M_{c2} = 1$). The idealized 2 p.u. result was obtained by (i) neglecting resistive losses, (ii) assuming unity modulation index, and (ii) neglecting converter internal vars consumption. However, in practice the actual ac currents will be slightly larger as shown in the first row of Table 2.4. For comparison, Table 2.4 also lists the current stresses calculated for a conventional M2DC at G_v range from 1/8 to 7/8 assuming the same modulation index as in simulation for the M2DC-CT but under lossless conditions. For example, the primary arms see drastically higher current stresses (15.556 p.u.) at $G_v = 1/8$, as predicted

by Table 2.1. The results confirm that the proposed M2DC-CT is able to minimize arm current stresses at all dc step ratios, while the conventional M2DC suffers from increased current stresses when $G_v \neq 0.5$ (as indicated by bold numbers). This is consistent with the analysis in Fig. 2.1.

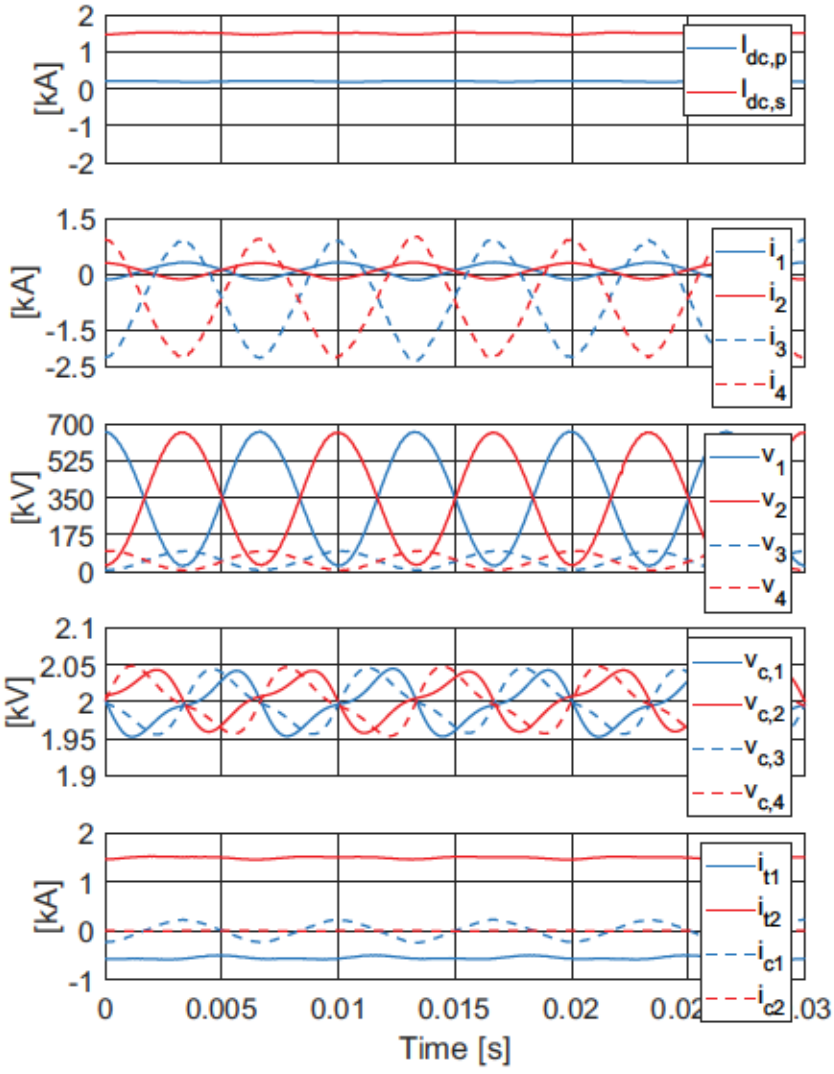

Figure 2.7: Steady-state M2DC-CT current and voltage waveforms for $G_v = 0.125$

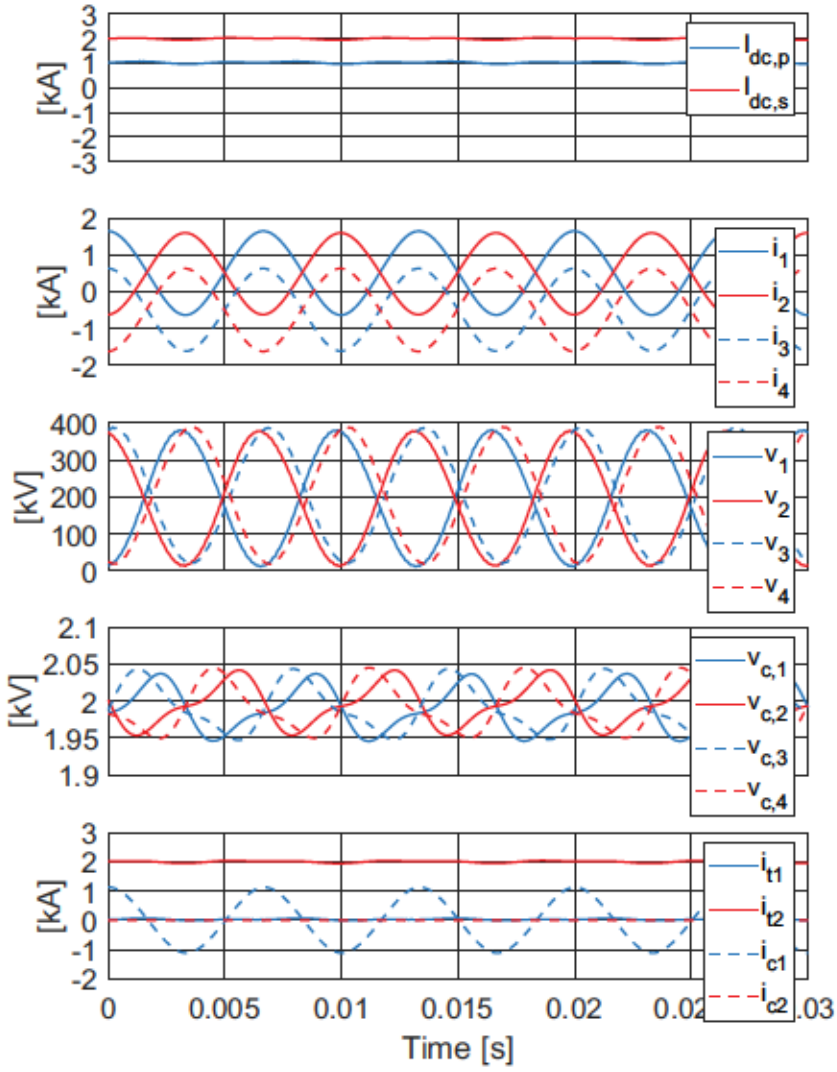

Figure 2.8: Steady-state M2DC-CT current and voltage waveforms for $G_v = 0.5$

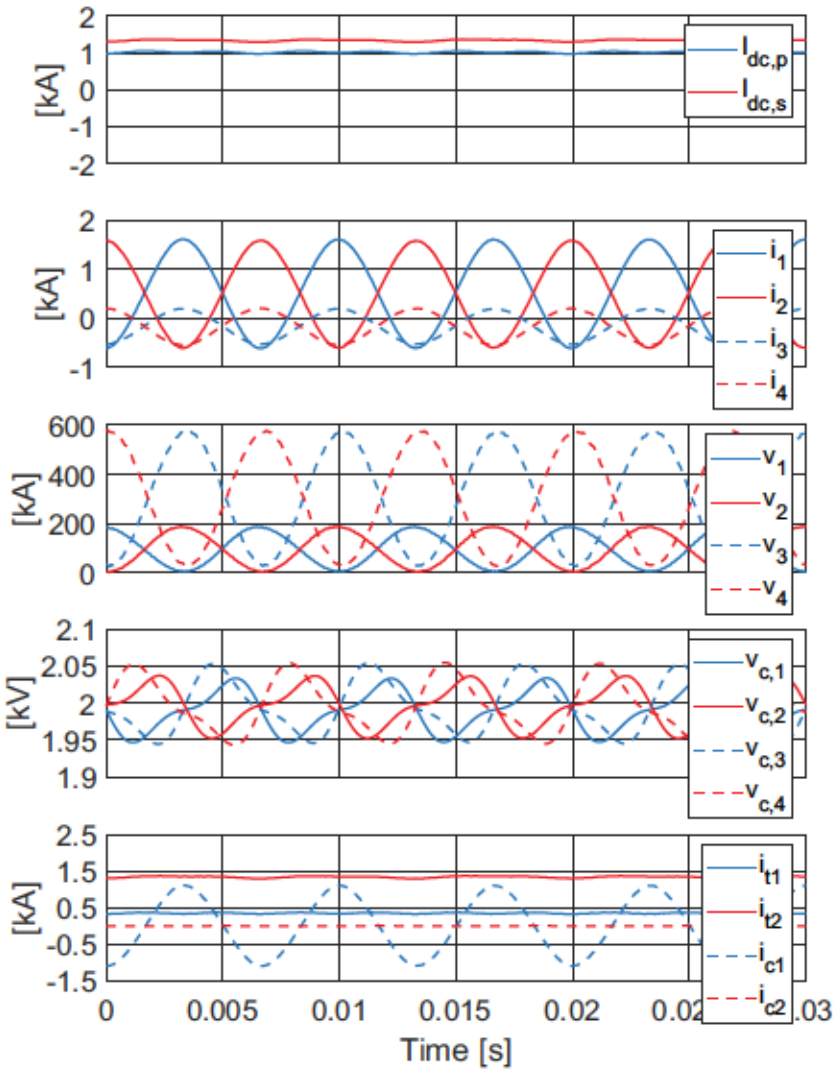

Figure 2.9: Steady-state M2DC-CT current and voltage waveforms for $G_v = 0.75$

2.5.5 Step-change Waveforms

Fig. 2.10 shows two transient responses of the converter operating at $V_{dc,p} = 400$ kV, $V_{dc,n} = 50$ kV ($G_v = 0.125$): P_{dc}^{ref} changed from 0 MW to +75 MW at $t = 0.05$ sec and P_{dc}^{ref} changed from +75 MW to -75 MW at $t = 0.25$ sec. Fig. 2.11 shows two transient responses of the converter operating at $V_{dc,p} = 400$ kV, $V_{dc,n} = 100$ kV ($G_v = 0.25$): P_{dc}^{ref} changed from 0 MW to +200 MW at $t = 0.05$ sec and P_{dc}^{ref} changed from +200 MW to -200 MW at $t = 0.25$ sec. Observe two step-changes display nearly identical dynamics. In each case, secondary dc current $i_{dc,s}$ maintains a characteristic first-order response. The slight deviations in $v_{c,1}$, $v_{c,2}$ (p arm SM capacitor voltages) and $v_{c,3}$, $v_{c,4}$ (s SM capacitor voltages) at $t = 0.05$ sec and $t = 0.25$ sec are due to the polarity reversal in dc power transfer. However, they are kept at their nominal average value of 2 kV by regulating the circulating ac current i_{c1} despite the large step-change in $P_{dc,s}$. The i_{c2} waveform that only contains ac component at all time verify the total dc power transfer is shared equally between strings, yielding dc flux cancellation within the core during step-changes in $P_{dc,s}$. These results verify the efficacy of the proposed dynamic controller.

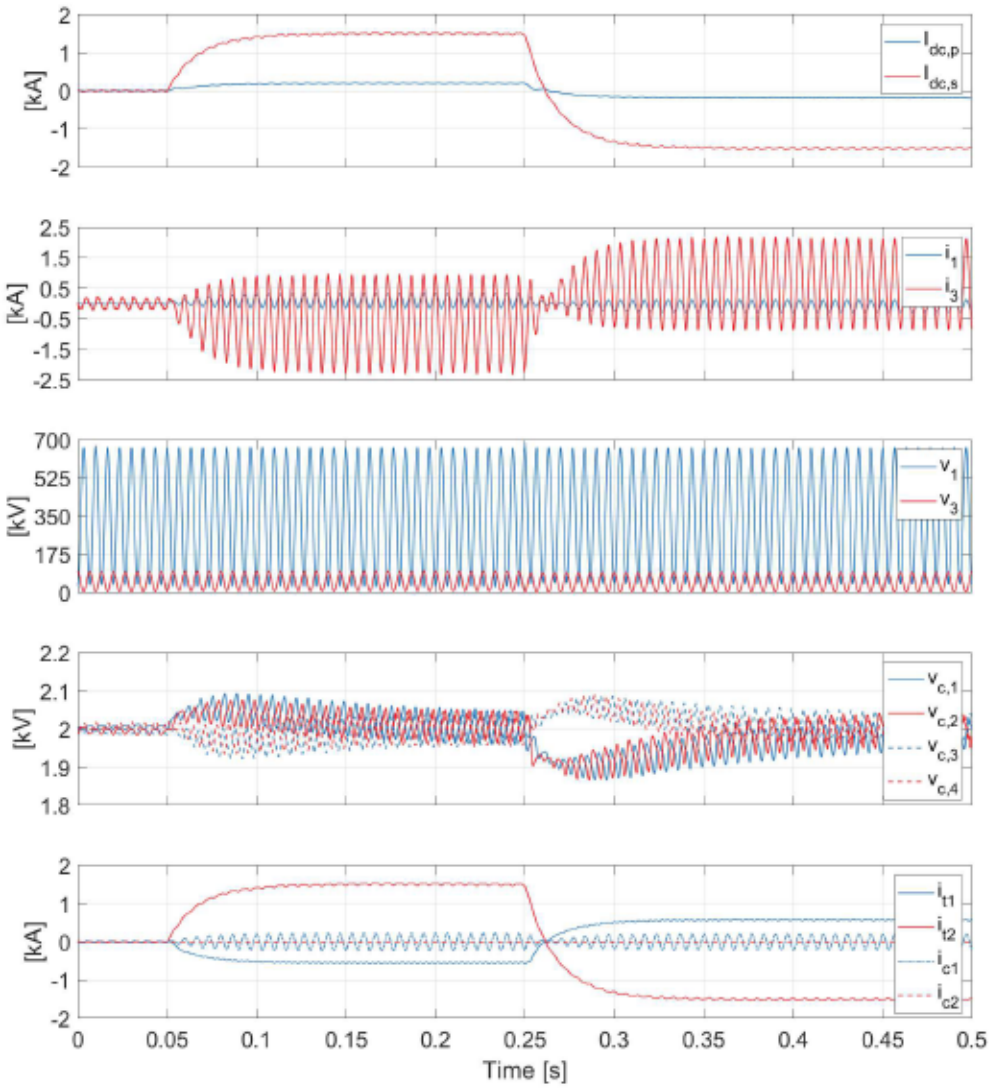

Figure 2.10: M2DC-CT waveforms of $G_v = 0.125$ for step-change in P_{dc}^{ref} from 0 MW to +75 MW at $t = 0.05$ sec. and from +75 MW to -75 MW at t = 0.25 sec

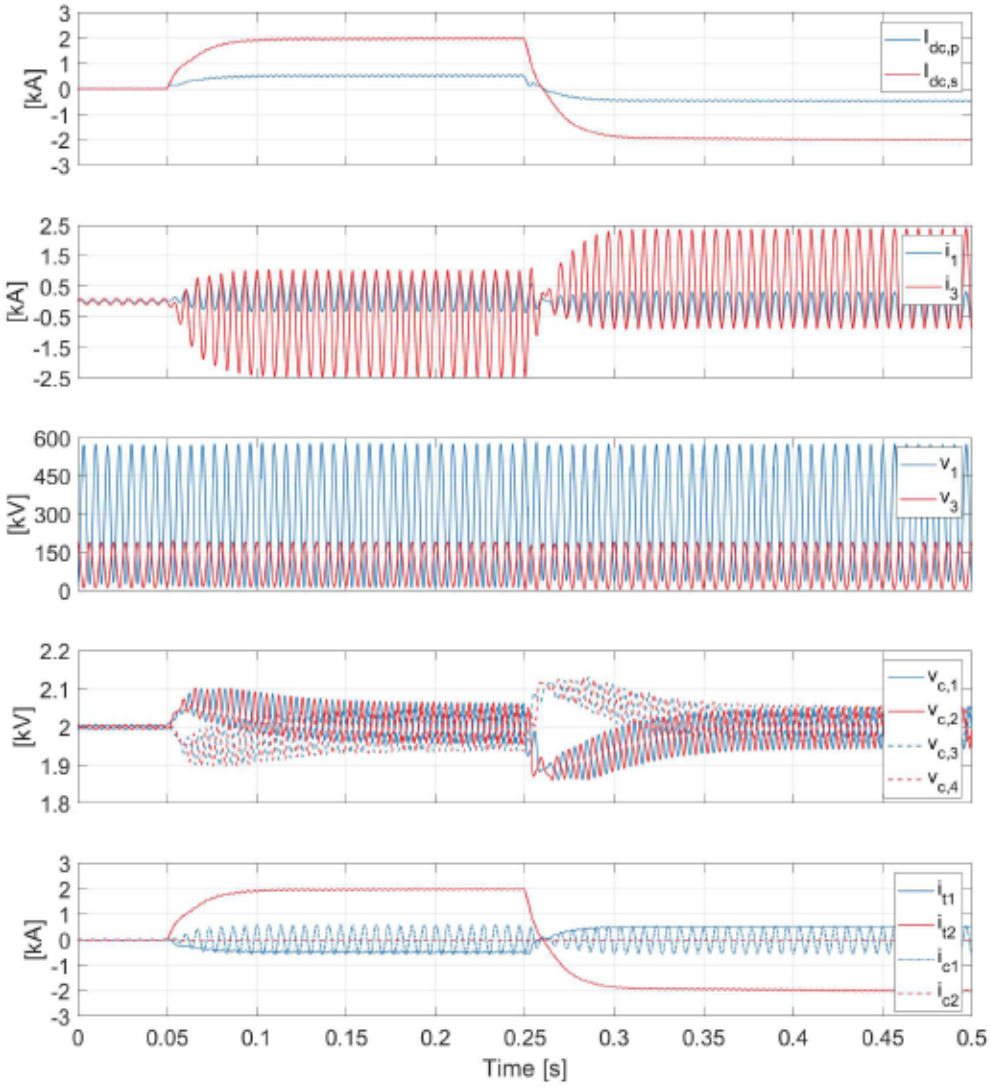

Figure 2.11: M2DC-CT waveforms of $G_v = 0.25$ for step-change in P_{dc}^{ref} from 0 MW to +75 MW at $t = 0.05$ sec. and from +75 MW to -75 MW at t = 0.25 sec

2.6 Experimental Validation

Experimental results are presented for a scaled-down 250/85 V, 1.25 kW laboratory prototype of the two-string M2DC-CT. The main objectives are to verify (i) that ac currents for both primary and secondary arms can be minimized in practice, and (ii) the practical efficacy of the proposed dynamic controller. The experimental setup and converter schematic are shown in Fig. 2.12 and Fig. 2.13, respectively. HBSMs and real-time controllers from Imperix are used. Experimental parameters are given in Table 2.5. A transformer with $n = 1.95$ is used which corresponds to $G_v = 0.34$ as per (2.18). The ac frequency is 150 Hz for consistency with the simulation results.

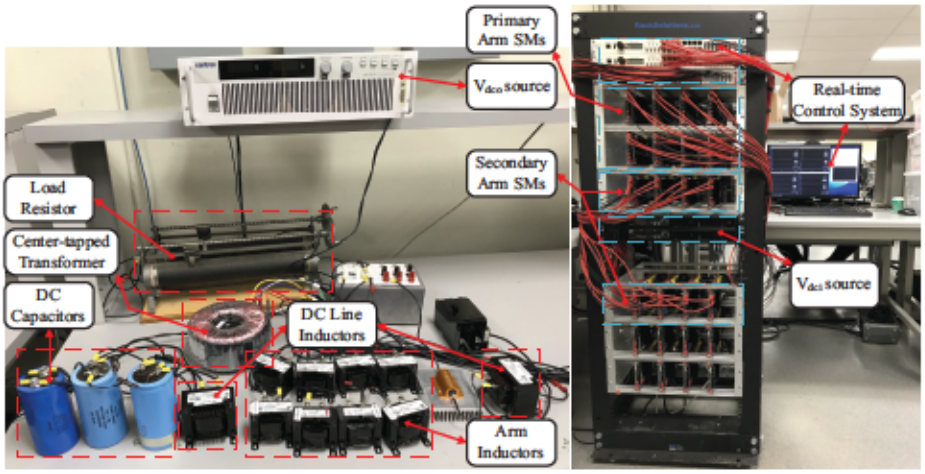

Figure 2.12: M2DC-CT experimental setup

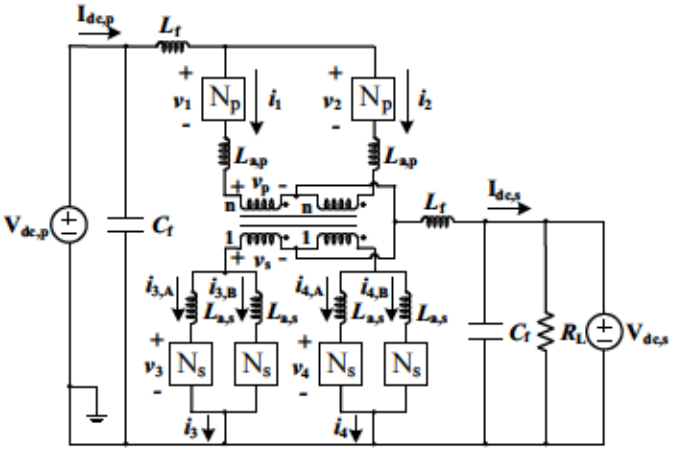

Figure 2.13: M2DC-CT experimental schematic

In Fig. 2.13, each primary arm consists of four series-cascaded SMs. Each (composite) secondary arm consists of two parallel-connected s arms (A and B), each comprising two series-cascaded SMs. Therefore, all arms have four SMs in total.

Operating at $G_v = 250/85$ results in the (composite) secondary arms having approximately twice the dc current and half the dc voltage as the primary arms, and therefore the s arms are paralleled as shown so that all SMs in the converter have by design approximately the same V,I stress.

Table 2.5: Experimental Parameters for Two-String M2DC-CT

Converter Parameters	Value
Primary and secondary dc voltages, $V_{dc,pi}/V_{dc,s}$	250 V/85 V
Conversion ratio, G_v	0.34
Input power, P_{dc}	1.25 kW
Fundamental frequency , ω	2π150 rad/s
Primary/secondary arm no. of SMs, N_p/N_s	4/2 (HBSM)
Primary/secondary arm SM capacitor, C_p/C_s	5 mF/5 mF
Primary/secondary arm choke, $L_{a,p}/L_{a,s}$	2 mH/1 mH
Nominal SM capacitor voltage, V_c	85 V
Line impedance, L_f	2.5 mH
DC bus capacitor, C_f	3 mF
Transformer Parameters	**Value**
Transformer power rating, S_w	1.5 kVA
Turns ratio, n	1.95:1
Primary/secondary winding voltages, V_p/V_s	117 V/60 V (rms)
Leakage inductance, L_x	0.085 mH
Magnetizing inductance, L_m	1.516 H
Controller Parameters	**Value**
SPWM carrier frequency, f_{sw}	7 kHz
Sample frequency, f_{sample}	7 kHz
K_{i1}, K_{i2}, a_{i1}, a_{i2}, K_f	0.5, 0.5, 20, 25, 0.2
K_{v1}, K_{v2}, a_{v1}, a_{v2}	2.8, 40, 0.8, 25
K_r, ζ, ζ_z, ω_z	15, 0.1, 1.2, 942 rad/s
$\bar{v}_{t1}$, $\bar{v}_{t2}$, $\hat{V}_{c2}$	125 V, 40 V, 76.5 V
$\Sigma v_{cap,t1}^{ref}$, $\Delta v_{cap,t2}^{ref}$	340 V, 0 kV

2.6.1 Steady-State Performance

Fig. 2.14 shows the steady-state arm voltages v_1, v_3 along with arm currents i_1, $i_{3,A}$ at rated dc power transfer. Fig. 2.15 shows the steady-state arm current and SM capacitor voltage waveforms. With $V_{dc,p} = 250$ V and $V_{dc,s} = 85$ V, arm 1 must support 165 V_{dc} while arm 2 supports 85 V_{dc}. Therefore, using only HBSMs, the 150 Hz component of v_1 will be approximately twice (165/85=1.95 times precisely) that of v_3. This is confirmed in Fig. 2.14. The center-tapped ac transformer with $n = 1.95$ provides the necessary voltage matching between primary and secondary arms, which enables minimization of the ac arm currents. The dc and 150 Hz components of i_1 and $i_{3,A}$ are by design approximately equal, as confirmed by Fig. 2.14. The dc and 150 Hz components of i_3, i_4 are by design approximately twice that of i_1, i_2, as confirmed by Fig. 2.15, due to the paralleling of s arms in Fig. 2.13. The primary dc current $I_{dc,p}$ and secondary dc current $I_{dc,s}$ contain a small second harmonic component as expected. Interleaving strings will improve ac filter of dc input and output nodes.

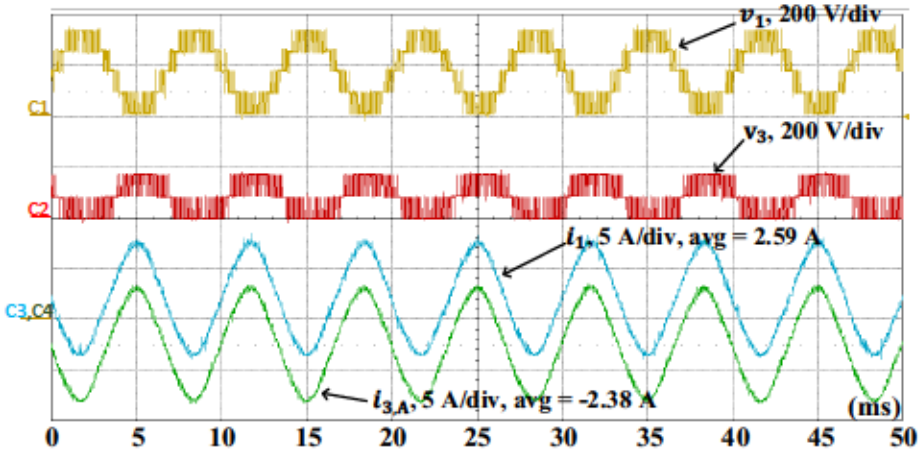

Figure 2.14: M2DC-CT steady-state arm voltages v_1, v_3 and arm currents i_1, $i_{3,A}$ at $P_{dc}^{ref} = 1.25$ kW; experimental waveforms captured by oscilloscope

Table 2.6: Frequency Analysis of Experimental M2DC-CT Currents at Rated Power

M2DC-CT [experimental]	DC	150 Hz
Primary arms	2.59 A	5.72 A_{pk} (2.21 p.u.)
Secondary arms	4.76 A	11.28 A_{pk} (2.37 p.u.)
M2DC [calculated for comparison]	DC	150 Hz
Primary arms	2.5 A	10.78 A_{pk} (4.31 p.u.)
Secondary arms	4.85 A	10.78 A_{pk} (2.22 p.u.)

Table 2.6 lists the magnitudes of arms dc and fundamental frequency (150 Hz) currents for the M2DC-CT at $P_{dc} = 1.25$ kW. Both primary and secondary ac arm currents are near the ideal 2 p.u. minimal value, similar to the simulation case study results in Table 2.4. This confirms the M2DC-CT can in practice achieve ac current minimization for all arms. For comparison, Table 2.6 also lists the current stresses calculated for a conventional M2DC assuming the same modulation index as in experiment but under lossless conditions. The 4.31 p.u. ac current carried by the primary arms is much higher (nearly double) relative to the secondary arms.

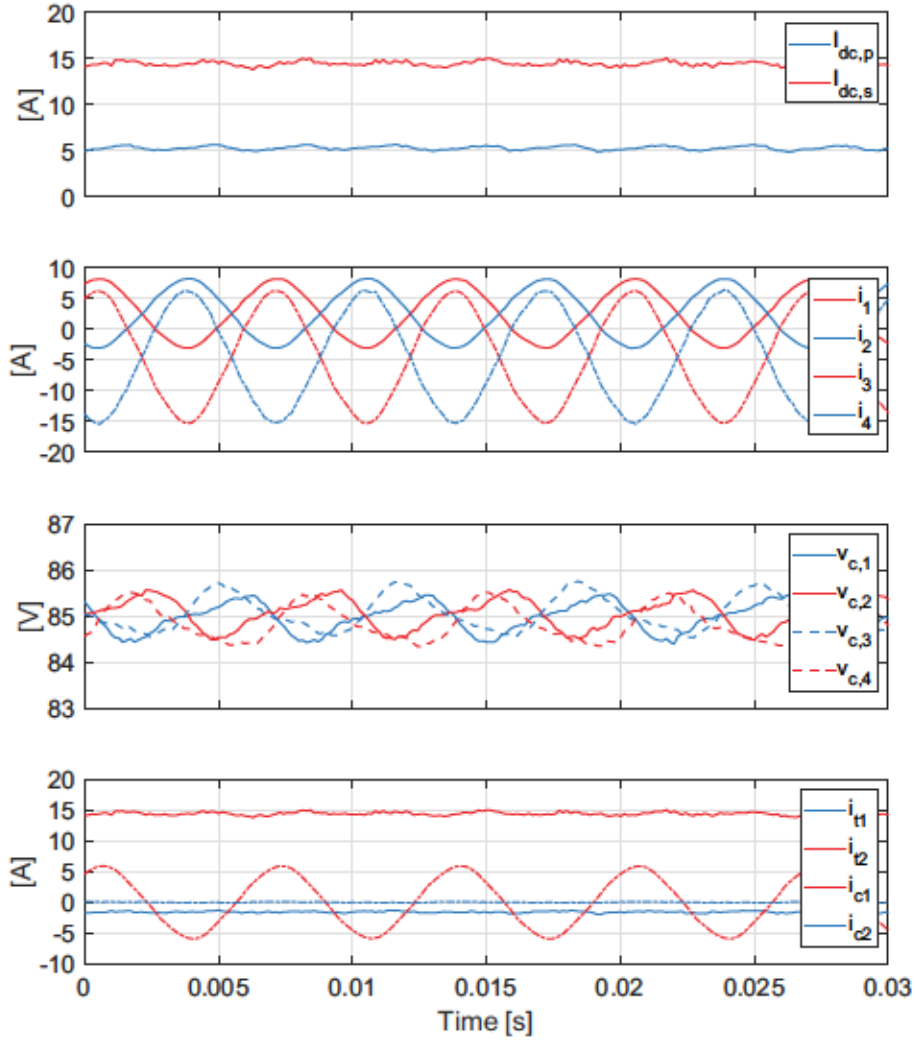

Figure 2.15: M2DC-CT steady-state current and voltage waveforms at $P_{dc}^{ref} = 1.25$ kW. experimental waveforms recorded using real-time control software with $f_{sample} = 7$ kHz

2.6.2 Dynamic Performance

The dynamic response of the M2DC-CT to step-changes in P_{dc}^{ref} from 1.25 kW to 0.25 kW and from 0.625 kW to 1.25 kW are shown in Figs. 2.16 and 2.17, respectively.

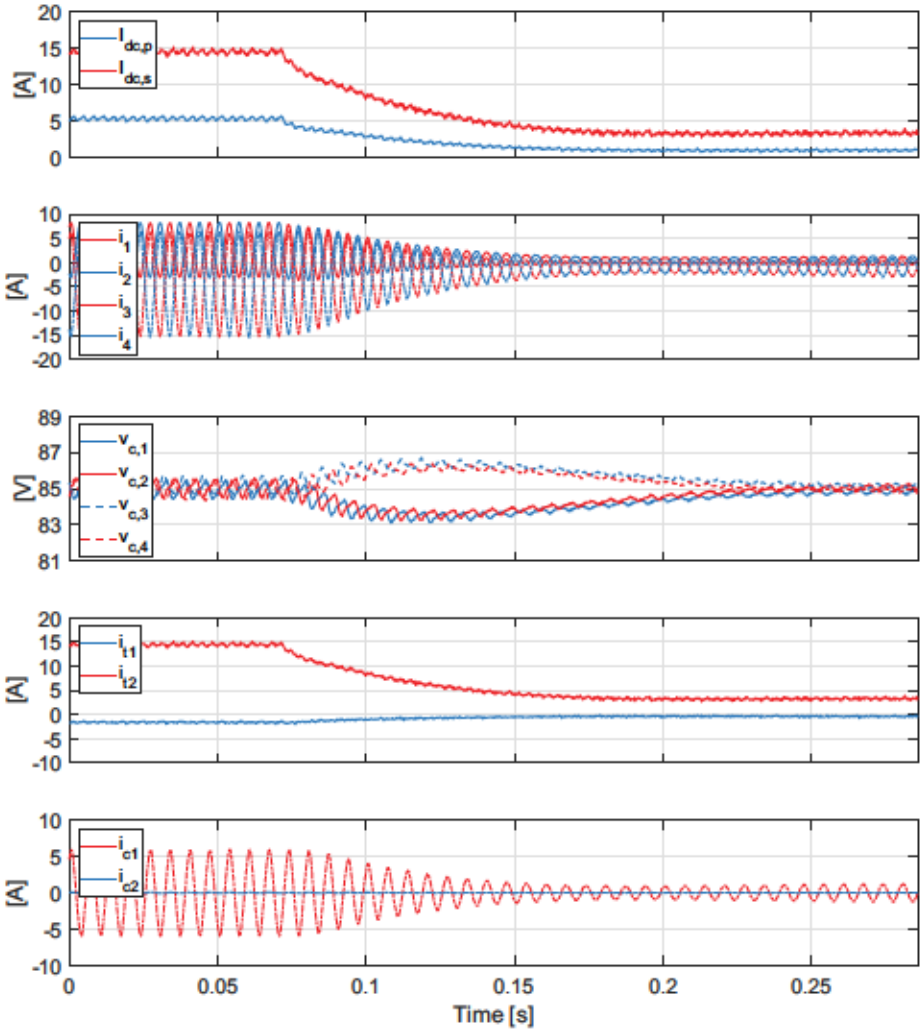

Figure 2.16: M2DC-CT dynamics with a step change of P_{dc}^{ref} from 1.25 kW to 0.25 kW at $t = 0.07$ sec; experimental waveforms recorded using real-time control software with $f_{sample} = 7$ kHz

These results validate the dynamic controller proposed in Fig. 2.4. The reduction (and increase) in P_{dc} demand in Fig. 2.16 (and Fig. 2.17) initially causes a dc voltage imbalance between SM capacitors in the primary and secondary arms, i.e., $\Delta v_{cap,t2}$ deviates from its reference value. The controller re-establishes balanced capacitor

voltages by requesting the requisite decrease (and increase) in the 150 Hz component of i_{c1}. The i_{c2} waveform that only contains small ac component at all time verify the total dc power transfer is shared equally between strings, yielding dc flux cancellation within the core during step-changes in $P_{dc,s}$. These results also verify the efficacy of the transformer filtering functionality as large fundamental frequency impedance is added in the i_{c2} path.

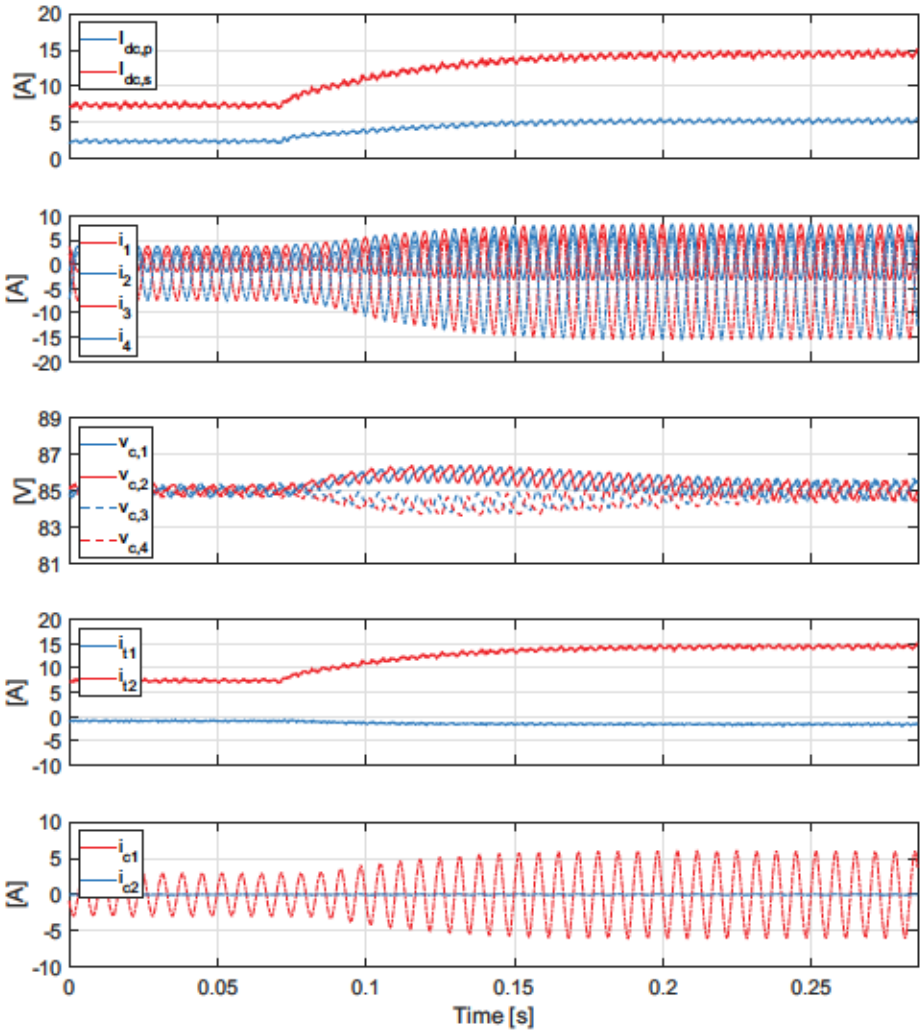

Figure 2.17: M2DC-CT dynamics with a step change of P_{dc}^{ref} from 0.625 kW to 1.25 kW at $t = 0.07$ sec; experimental waveforms recorded using real-time control software with $f_{sample} = 7$ kHz

2.7 Comparison of M2DC-CT with Existing DC-DC MMCs

Three representative two-string dc-dc MMCs in Fig. 2.18a-c and the proposed two-string M2DC-CT in Fig. 2.18d have diverse structures and power transfer mechanisms. Subscripts p and s denote primary and secondary sides, respectively. P_{dc} denote average power injections at the input dc port. The p and s phase arms comprise N_p and N_s series cascaded SMs, which can be HB or FB type, as shown in Fig. 2.18e. The M2DC-CT leverages a novel multi-frequency power transfer mechanism enabled

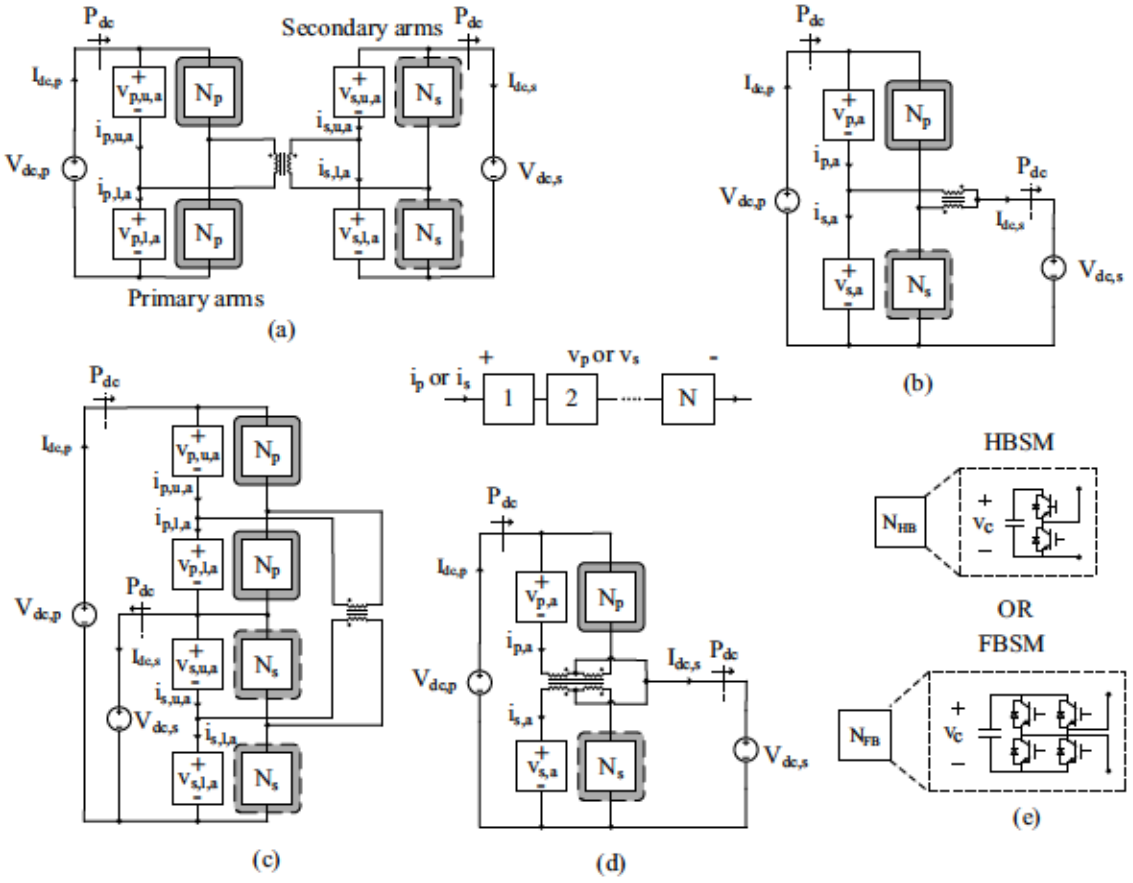

Figure 2.18: Two-string dc-dc MMCs under study: (a) F2F-MMC, (b) M2DC [11, 12, 14], (c) HVDC-AT [10], (d) M2DC-CT, (e) composition of individual phase arms

by an internal center-tapped transformer that is a hybrid of the P3T (for HVDC-AT) and CCL (for M2DC) mechanisms. Consequently, the M2DC-CT is able to merge the best traits of the HVDC-AT and M2DC; namely, inherent minimization of arm ac current stresses and elimination of dc voltage stress between internal transformer windings. This comes, though, with the caveat of the transformer windings carrying

both dc and ac currents. However, it will be shown in Section 2.7.3 that the absence of inter-winding dc voltage stress yields an overall reduction in transformer area product relative to the HVDC-AT, and hence overall lower magnetics size and weight (and ultimately cost).

Some MMC-based topologies are examined and compared in [10, 41, 48–50, 67]. However, they neither conduct a fair comparison nor a complete comparison of existing MMC topologies. For example, all comparisons did not include dc insulation issues of the transformers used in MMC topologies. This section firstly compares arm current stresses, semiconductor effort and magnetics requirements on a per-unitized basis over a broad range of conversion ratios for the two-string M2DC-CT, M2DC and HVDC-AT. These are all partial-power-processing dc-dc MMCs. Results are also compared to the conventional two-stage F2F-MMC for reference. Two-string and three-string variants have identical operating principles and thus will have identical comparison results. The case study analysis considers a converter with $V_{dc,p} = 400$ kV, $P_{dc} = 75$ MW and $f = 150$ Hz for consistency with the simulations in Section 2.5. A wide range of dc step ratios is considered with $G_v \in [0.1, 0.9]$ (in increments of $+0.1$). Converter losses for all four topologies are then calculated. Such comparative assessment can be adopted for any MMC-based topologies. Based on results of the comparative analysis, key applications for the M2DC-CT are identified. Note that in this section the superscripts with the respective converter name are added in order to provide a better distinction.

2.7.1 Fault Blocking Implications

In HVDC applications, fault blocking capability is an important requirement to maintain high transmission security and reliability [68]. The F2F-MMC in Fig. 2.18a inherently offers bidirectional fault blocking due to the galvanic separation property of the intermediate ac transformer. The previous discussion reveals that the partial-power-processing dc-dc MMCs in Figs. 2.18b-d have less ac power processed by the converter. However, this comes at the expense of losing the capability of inherent bidirectional fault blocking due to lose of galvanic separation. To conduct a fair comparison, bidirectional fault blocking capability for the partial-power-processing dc-dc MMCs needs to be considered. Two possible dc fault scenarios that can occur are depicted, taking for illustration example the M2DC:

1. The inability to block primary side dc faults stems from the uncontrolled propagation of fault currents through the lower IGBT anti-parallel diodes in each HBSM, as shown in Fig. 2.19a. Additional FBSM or other SMs with bipolar

voltage injection capability should be utilized to inject reverse voltage equal to the secondary dc voltage $V_{dc,s}$. This enables the control of the fault current by blocking switches. The secondary arm on the other hand does not require FBSMs and only needs sufficient HBSMs to support the secondary dc voltage. The required voltage for the secondary arm is equal to secondary dc voltage $V_{dc,s}$.

2. In case of a secondary side dc fault as shown in Fig. 2.19b, sufficient HBSMs are required in the primary arm in forward direction to block the fault on secondary dc side. The required voltage is equal to primary dc voltage $V_{dc,p}$. The secondary arm does not require to support any voltage. Thus, the M2DC-CT with FBSMs can inherently block faults located in the secondary side dc network.

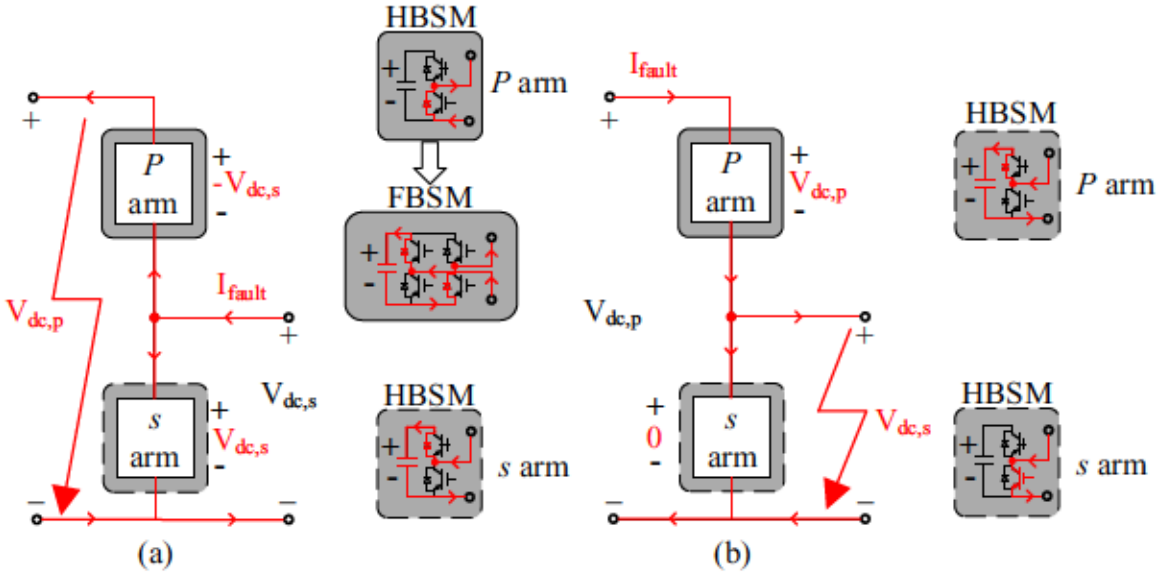

Figure 2.19: Blocking capability requirements of the partial-power-processing dc-dc MMCs in case of (a) primary side dc fault and (b) secondary side dc fault, where the dc fault currents are indicated by red lines

Table 2.7 summarizes the arm voltage requirements of the dc-dc MMCs in Figs. 2.18 to achieve fault blocking on both primary and secondary dc sides. The red text indicates FBSMs are necessary for the required arm voltage generation. The aim of comparative analysis is to highlight their inherent properties that make them particularly suitable or unsuitable for different applications. As mentioned earlier, each converter arm requires sufficient blocking capability in both forward and reverse directions to block dc faults in both the primary and secondary dc sides. Therefore, partial-power-processing dc-dc MMCs are designed with hybrid-cell MMC arms consist of both FB and HB SMs, where necessary. In addition to the dc fault interrupting

Table 2.7: v_{arm} Generation Requirements for DC-DC MMCs of Figs. 2.18b-d with and without Bidirectional Fault Blocking Capability (Red Text Denotes FBSMs)

	[min, max] voltage injection required	
	With fault blocking capability at secondary dc side	With bidirectional fault blocking capability
v_{arm}	F2F-MMC	
v_p	$[0,\ \frac{1}{2}V_{dc,p} + \hat{v}_p]$	$[0,\ \frac{1}{2}V_{dc,p} + \hat{v}_p]$
v_s	$[0,\ \frac{1}{2}G_vV_{dc,p} + \hat{v}_s]$	$[0,\ \frac{1}{2}G_vV_{dc,p} + \hat{v}_s]$
v_{arm}	HVDC-AT	
v_p	$[0,\ \frac{1}{2}(1-G_v)V_{dc,p} + \hat{v}_p]$	$[-\frac{1}{2}G_vV_{dc,p},\ \frac{1}{2}V_{dc,p} + \hat{v}_p]$
v_s	$[0,\ \frac{1}{2}G_vV_{dc,p} + \hat{v}_s]$	$[0,\ \frac{1}{2}G_vV_{dc,p} + \hat{v}_s]$
v_{arm}	M2DC & M2DC-CT	
v_p	$[0,\ (1-G_v)V_{dc,p} + \hat{v}_p]$	$[-G_vV_{dc,p},\ V_{dc,p} + \hat{v}_p]$
v_s	$[0,\ G_vV_{dc,p} + \hat{v}_s]$	$[0,\ G_vV_{dc,p} + \hat{v}_s]$

capability, utilizing FBSMs provides freedom to control the maximum arm ac voltage regardless of the available dc voltage. This is commonly done in dc-dc MMC topologies, e.g. [7, 50, 51], which can enable the reduction of arm ac current. However, utilizing FBSMs result in a higher number of power devices and commensurately higher power loss. It is worth noting that other SM configurations, such as those studied in [52], can be utilized to potentially further reduce converter losses while maintaining fault interrupting capability. Dc circuit breaker is an alternative solution for interrupting dc fault currents [9, 22]. Optimization of fault blocking and cost is considered outside the scope of this paper. Thus, both design requirements are considered: i) converters with sufficient FBSMs to enable bidirectional fault blocking capability and ii) converters with HBSMs that can inherently block faults located in the secondary side dc network.

2.7.2 Current Stresses and Semiconductor Effort

A sufficiently high number of SMs are needed in each converter arm, N_{arm}, to generate the required arm voltage v_{arm}, where subscript $arm \in p, s$. Note that in Fig. 2.2a, $p \in 1, 2$ and $s \in 3, 4$. The fundamental frequency component of the arm voltage, $\hat{v}_{arm}$, dictates the fundamental frequency ac currents flowing within the converter. Assuming lossless energy conversion, the steady-state average power absorbed by each arm in MMC-based topologies must be equal to zero as the SMs contain only capacitive energy storage, e.g., $P_1 = \frac{1}{T}\int_0^T v_1 i_1 dt = 0$ in Fig. 2.2a. The arm currents

and voltages comprise dc and fundamental frequency ac components. Harmonic power balance [11] necessitates the dc power absorbed by an arm, P_{arm}^{dc}, must be balanced by average power absorption at fundamental frequency, P_{arm}^{ac},

$$P_{arm}^{ac} = P_{arm}^{dc}, \tag{2.25}$$

where

$$P_{arm}^{ac} = \frac{1}{2}\hat{v}_{arm}\hat{v}_{arm}\cos(\theta_{v_{arm}} - \theta_{i_{arm}}) \tag{2.26}$$

$$P_{arm}^{dc} = v_{arm}^{dc} i_{arm}^{dc}, \tag{2.27}$$

and placeholder subscript $arm \in p, s$. Variables $\hat{v}_{arm}$, $\hat{i}_{arm}$ and v_{arm}^{dc}, i_{arm}^{dc} are the (peak) fundamental frequency ac and dc components of the arm voltages and currents, e.g., i_1 and v_1 in Fig. 2.2a. Assuming peak ac arm voltages $\hat{v}_p$ and $\hat{v}_s$ are generated at p and s arms, respectively, the peak ac current seen by p and s arms in MMC-based topologies are

$$\hat{i}_p = 2\frac{P_p^{dc}}{\hat{v}_p\cos(\theta_{v_p} - \theta_{i_p})},\ \hat{i}_s = 2\frac{P_s^{dc}}{\hat{v}_s\cos(\theta_{v_s} - \theta_{i_s})} \tag{2.28}$$

$\hat{i}_p$ and $\hat{i}_s$ can be minimized by maximizing arm ac voltages $\hat{v}_p$ and $\hat{v}_s$. For dc-dc MMCs with HBSMs, the maximal value of $\hat{v}_{arm}$ of each converter are limited to

$$\hat{v}_p^{F2F-MMC} = \frac{1}{2}V_{dc,p}, \quad \hat{v}_s^{F2F-MMC} = \frac{1}{2}G_v V_{dc,p} \tag{2.29}$$

$$\hat{v}_p^{HVDC-AT} = \frac{1}{2}(1-G_v)V_{dc,p}, \quad \hat{v}_s^{HVDC-AT} = \frac{1}{2}G_v V_{dc,p} \tag{2.30}$$

$$\hat{v}_p^{M2DC} = \hat{v}_s^{M2DC} = \begin{cases} G_v V_{dc,p} & G_v \leq 0.5 \\ (1-G_v)V_{dc,p} & G_v > 0.5 \end{cases} \tag{2.31}$$

$$\hat{v}_p^{M2DC-CT} = (1-G_v)V_{dc,p}, \quad \hat{v}_s^{M2DC-CT} = G_v V_{dc,p} \tag{2.32}$$

The bidirectional fault blocking requirements for the HVDC-AT, M2DC and M2DC-CT lead to the employment of the FBSMs in the primary MMC, as discussed in the section before. Thus, more headroom for maximizing the ac voltages is available for primary arms (see red text in Table 2.7). Consequently the available headroom of the primary arm is utilized to further minimize the current stresses. Note that if the generated arm ac voltage is greater than arm dc voltage, solely FBSMs are employed in that arm to ensure SM capacitor balance can be satisfied [69]. For the secondary arm, no additional FBSM are utilized. Thus, the maximal value of $\hat{v}_{arm}$ of each converter with FBSMs are limited to

$$\hat{v}_p^{F2F-MMC} = \frac{1}{2}V_{dc,p}, \quad \hat{v}_s^{F2F-MMC} = \frac{1}{2}V_{dc,s} \tag{2.33}$$

$$\hat{v}_p^{HV\,DC-AT} = \begin{cases} \frac{1}{2}(1-G_v)V_{dc,p} & G_v \leq 0.5 \\ \frac{1}{2}G_v V_{dc,p} & G_v > 0.5 \end{cases}, \quad \hat{v}_s^{HV\,DC-AT} = \frac{1}{2}G_v V_{dc,p} \tag{2.34}$$

$$\hat{v}_p^{M2DC} = \hat{v}_s^{M2DC} = G_v V_{dc,p} \tag{2.35}$$

$$\hat{V}_p^{M2DC-CT} = \begin{cases} (1-G_v)V_{dc,p} & G_v \leq 0.5 \\ G_v V_{dc,p} & G_v > 0.5 \end{cases}, \quad \hat{V}_s^{M2DC-CT} = G_v V_{dc,p} \tag{2.36}$$

The number of SMs required in a converter arm N_{arm} can be estimated by the nominal voltage V_c of the SM capacitors and the maximum (peak) value of arm voltage v_{arm} that has to be generated as per Table 2.7

$$N_{arm} = k_s \frac{\max(v_{arm})}{V_c}, \tag{2.37}$$

where k_s is an additional safety factor that is set to 120% in this study. FBSMs are needed only if a negative arm voltage is required (as indicated by red text in Table 2.7). The number of FBSMs required is

$$N_{FB,arm} = k_s \frac{|\min(v_{arm})|}{V_c} \tag{2.38}$$

Therefore, the number of HBSMs is

$$N_{HB,arm} = N_{arm} - N_{FB,arm} \tag{2.39}$$

The semiconductor effort λ is a measure of the power rating of the switches that have to be installed per Watt of real input power [68, 70]. It is expressed on a per-unit basis as the ratio of the sum of all the semiconductors' apparent power ratings to the dc power throughput.

$$\lambda = q \cdot \frac{\sum_{j=1}^{N_{arm}} V_c i_{arm(pk)}}{P_{conv}} \tag{2.40}$$

The peak arm current $i_{arm(pk)}$ is used due to the fact that this is the maximum current the semiconductors have to be able to switch, where subscript $arm \in p, s$. q is the number of arms. P_{conv} is the converter rated power. The switch rating of FBSMs will be two times of HBSMs due to the fact that FBSM consists of 4 semiconductors.

Figs. 2.20 and 2.21 plot the absolute peak currents of each topology with HBSMs for primary and secondary arms, normalized to the dc input current of each phase leg. For the primary arms, all topologies have the same peak current stress except for the M2DC, which sees very high stresses as G_v decreases below 0.5. This is because the M2DC lacks a transformer for ac voltage matching between arms. For the secondary arms, the M2DC-CT and HVDC-AT achieve the lowest peak current stresses while the current stresses for the M2DC go up as G_v increases above 0.5, reaching a maximum

value of over 6 times larger than both the M2DC-CT and HVDC-AT at $G_v = 0.9$. The F2F-MMC has the highest stresses as it is not a partial-power processing topology. All topologies see large secondary arm current stresses at low G_v due to the inherently high dc currents seen by these arms. Based on these results, the semiconductor effort normalized to dc power transfer P_{dc} is plotted in Fig. 2.24. The M2DC-CT and HVDC-AT have the lowest overall semiconductor effort across all dc step ratios. The M2DC has equal semiconductor effort only at $G_v = 0.5$; it has higher values at all other step ratios. The F2F-MMC has constant semiconductor effort owing to its two-stage isolated dc-dc structure with separate MMCs.

Figs. 2.22 and 2.23 plot the absolute peak currents of each topology with FBSMs for primary and secondary arms, normalized to the dc input current of each phase leg. Based on these results, the semiconductor effort with FBSMs normalized to dc power transfer P_{dc} is plotted in Fig. 2.25. The bidirectional fault blocking requirement impacts the primary arm peak current stress except for the F2F-MMC when $G_v > 0.5$ and the secondary arm peak current stress for the M2DC when $G_v > 0.5$. As a result, the HVDC-AT, M2DC and M2DC-CT have the same overall semiconductor effort when $G_v > 0.5$, while the M2DC still have the highest semiconductor effort at low G_v. The F2F-MMC doesn't have to use FBSMs to enable bidirectional fault blocking capability. Thus, it has the same constant semiconductor effort as in Fig. 2.24.

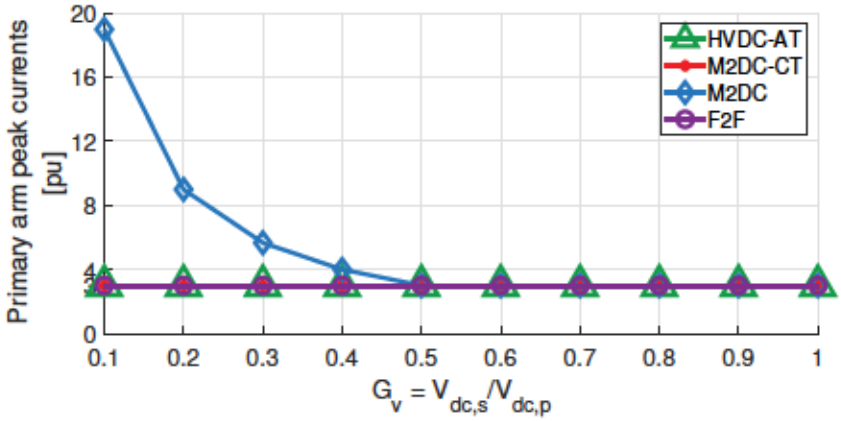

Figure 2.20: Primary arms absolute peak current stresses, at rated power transfer and with maximum arm ac voltage utilization (all currents are normalized to dc input current of each phase leg); four converters utilize HBSMs in all arms

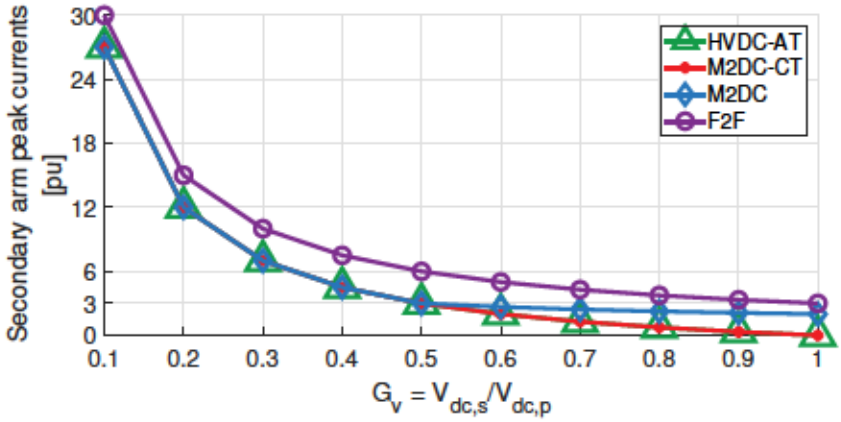

Figure 2.21: Secondary arms absolute peak current stresses, at rated power transfer and with maximum arm ac voltage utilization (all currents are normalized to dc input current of each phase leg); four converters utilize HBSMs in all arms

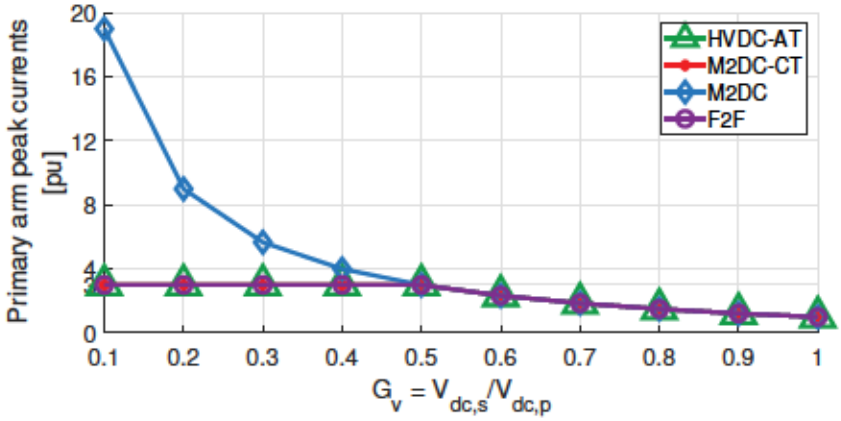

Figure 2.22: Primary arms absolute peak current stresses, at rated power transfer and with maximum arm ac voltage utilization (all currents are normalized to dc input current of each phase leg); HVDC-AT, M2DC and M2DC-CT utilize FBSMs to enable bidirectional fault blocking capability; F2F-MMC utilizes HBSMs

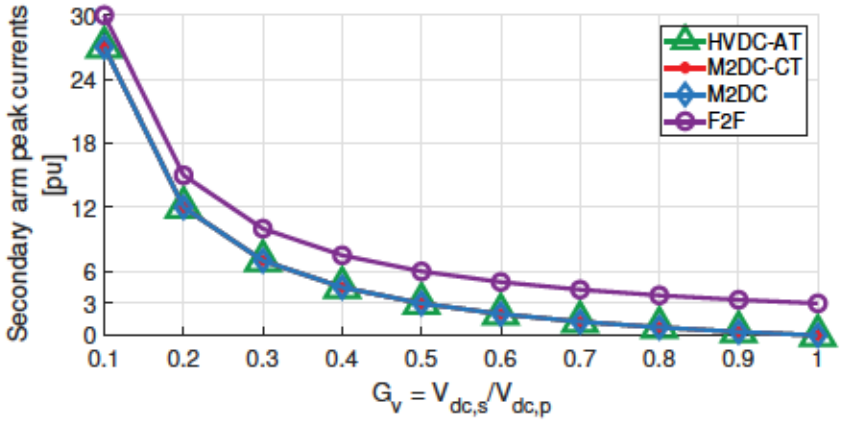

Figure 2.23: Secondary arms absolute peak current stresses, at rated power transfer and with maximum arm ac voltage utilization (all currents are normalized to dc input current of each phase leg); HVDC-AT, M2DC and M2DC-CT utilize FBSMs to enable bidirectional fault blocking capability; F2F-MMC utilizes HBSMs

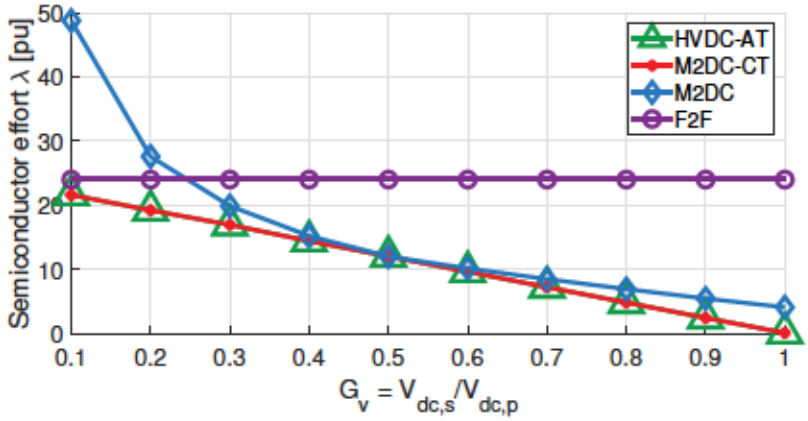

Figure 2.24: Converter semiconductor efforts, at rated power transfer and with maximum arm ac voltage utilization (semiconductor efforts are normalized to dc power transfer P_{dc}); four converters utilize HBSMs in all arms

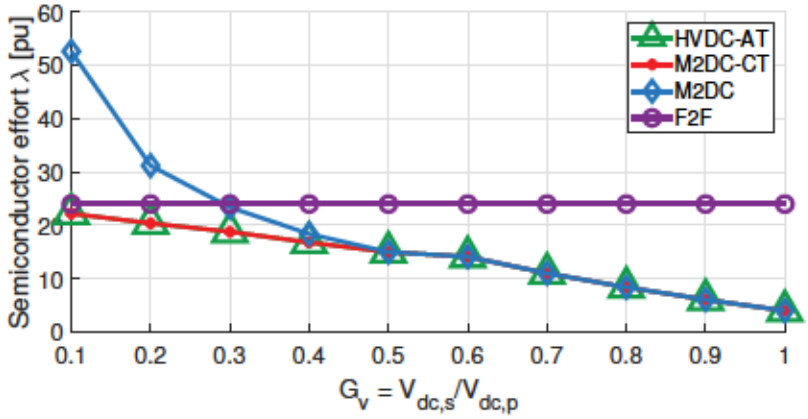

Figure 2.25: Converter semiconductor efforts, at rated power transfer and with maximum arm ac voltage utilization (semiconductor efforts are normalized to dc power transfer P_{dc}); HVDC-AT, M2DC and M2DC-CT utilize FBSMs to enable bidirectional fault blocking capability; F2F-MMC utilizes HBSMs

2.7.3 Magnetics Core Area Product

This section quantifies the impact of core power handling capability, S_c, and inter-winding dc voltage stress, $V_{dc,iso}$, on the size, weight and cost of the magnetics. The transformer in the HVDC-AT carries ac current while the coupled inductor in the M2DC carries dc current. The design of the coupled inductors in the M2DC can be carried out similarly to the design of transformers [50]. The center-tapped transformer in the M2DC-CT carries both dc and ac currents. The M2DC and M2DC-CT magnetics provide core dc magnetic flux cancellation due to windings orientation [11, 36, 38, 58–61]. $V_{dc,iso}$ is determined for asymmetric monopole or bipole configurations in Fig. 2.1. S_c is calculated by summing the product of the rms voltage and rms current for each winding [71]

$$S_c = S_{w,p} + S_{w,s} \tag{2.41}$$

Note that core power handling capability S_c is different from the magnetics Volt-Ampere rating S_w, where

$$S_w = S_{w,p} \tag{2.42}$$

S_c requirement of the magnetics with HBSMs and FBSMs are firstly plotted in Fig. 2.26 and 2.27, respectively. For converters with HBSMs, the F2F-MMC transformer core power is constant while the M2DC transformer core power is the lowest overall. S_c for the M2DC-CT center-tapped transformer is 18.4% higher than the HVDC-AT transformer core power at all dc step ratios. This is because the center-tapped transfomer has a higher overall rms current rating. At very low dc step ratios, the center-tapped transformer in the M2DC-CT has the highest core power. For converters with FBSMs, S_c for the HVDC-AT becomes the lowest for $G_V > 0.65$.

$V_{dc,iso}$ requirement of the magnetics are plotted in Fig. 2.26. $V_{dc,iso}$ of four converters with FBSMs is identical to that with HBSMs. For the inter-winding dc voltage stresses, $V_{dc,iso} = 0.5V_{dc,p}$ for the HVDC-AT at all values of G_v while $V_{dc,iso}$ for the F2F-MMC goes up as G_v decreases. However, $V_{dc,iso} = 0$ for the M2DC and M2DC-CT.

The core area product A_p is a figure of merit to compare the costs of the magnetic components and relates to the size of magnetics [50]. It is directly proportional to S_c and inversely proportional to the core window utilization factor, K_u, which is a number less than one that models the amount of core window area utilized by copper [71]. K_u depends on insulation requirements including any dc voltage stress that exists between windings. $K_u = 0.4$ is used in [71] to approximate transformer designs without dc voltage isolation requirements, and therefore this value is used for the M2DC and M2DC-CT. For the HVDC-AT and F2F-MMC, assuming HV cable is used as the

insulation mechanism to accommodate inter-winding dc isolation requirements [72], K_u is modified to account for the corresponding copper fill reduction as follows

$$K_u = 0.4 \cdot \frac{\pi R_w^2}{\pi (R_w + d_{ins})^2}, \tag{2.43}$$

where R_w is the cable conductor radius and d_{ins} is the required cable insulation thickness. Data for R_w and d_{ins} considering different HV levels from [73] is used. Exact calculation of the area product A_p requires a detailed magnetics design. The magnetic structure is typically designed based on a trade-off between size, cost and efficiency, following the procedure of magnetic structure determination, insulation design, core material selection and magnetic loss analysis [74, 75]. Given the comparative analysis considers a total of (4 different converters)$\times$(9 different dc step ratios)=36 different magnetic structures, generating an optimal design for all cases is outside the scope of this thesis. Rather, the goal is to provide a relative comparison of A_p for the different topologies that accounts for the impacts of S_c and K_u (the latter of which is influenced by $V_{dc,iso}$). Thus, in calculating the area product, other transformer parameters such as operating frequency are set to be the same for all topologies.

Fig. 2.29 shows the calculated A_p for the four topologies with HBSMs, normalized to the area product of the F2F-MMC for reference. The area product for the M2DC is the lowest among all topologies because $V_{dc,iso} = 0$ and it has the lowest S_c. The M2DC-CT has the next lowest A_p. The HVDC-AT always has larger A_p than the M2DC-CT. There is a 50% reduction in A_p for the M2DC-CT relative to the HVDC-AT. This is in fact a constant outcome regardless of dc step ratio, as the required dc isolation voltage for the M2DC-CT and HVDC-AT does not depend on G_v.

Fig. 2.29 shows the calculated A_p for the four topologies with FBSMs, normalized to the area product of the F2F-MMC for reference. Unlike topologies with HBSMs, the area product for the HVDC-AT becomes the smallest among all topologies for large G_v. The reason behind this is the HVDC-AT has the lowest magnetics apparent power for large G_v. However, the M2DC still has the smallest A_p for $G_v < 0.85$ and the M2DC-CT has the next lowest.

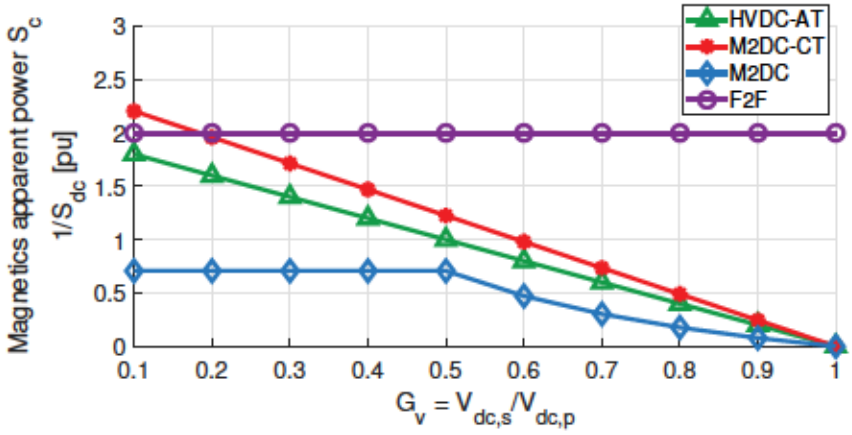

Figure 2.26: Magnetics core apparent power rating normalized to dc power transfer P_{dc}; four converters utilize HBSMs in all arms

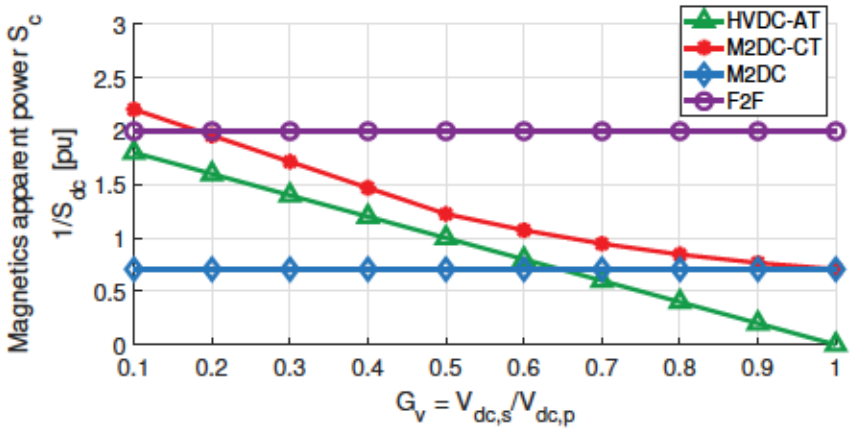

Figure 2.27: Magnetics core apparent power rating normalized to dc power transfer P_{dc}; HVDC-AT, M2DC and M2DC-CT utilize FBSMs to enable bidirectional fault blocking capability; F2F-MMC utilizes HBSMs

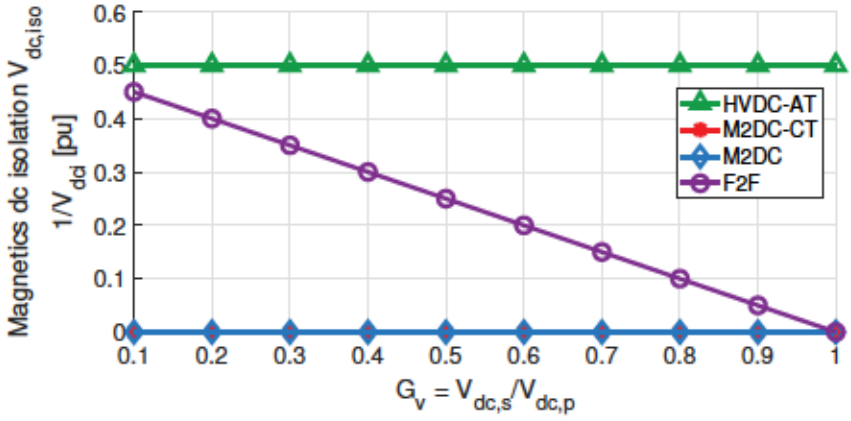

Figure 2.28: Magnetics inter-winding dc voltage isolation requirements normalized to $V_{dc,p}$ for asymmetric monopole or full bipole configurations

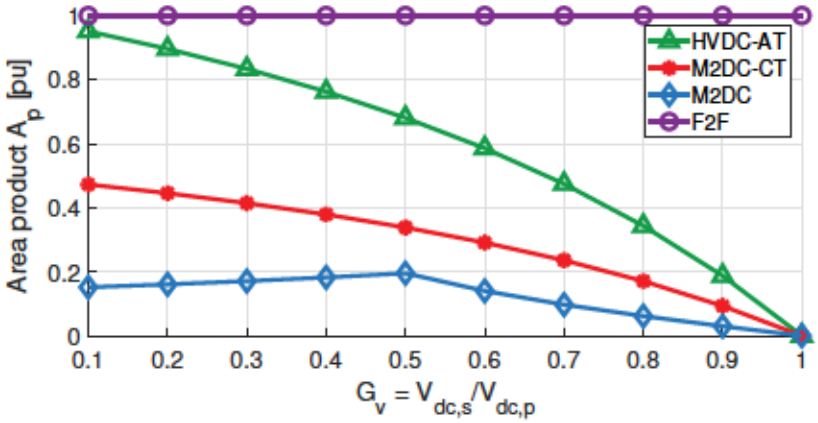

Figure 2.29: Magnetics core area product normalized to F2F-MMC's area product; four converters utilize HBSMs in all arms

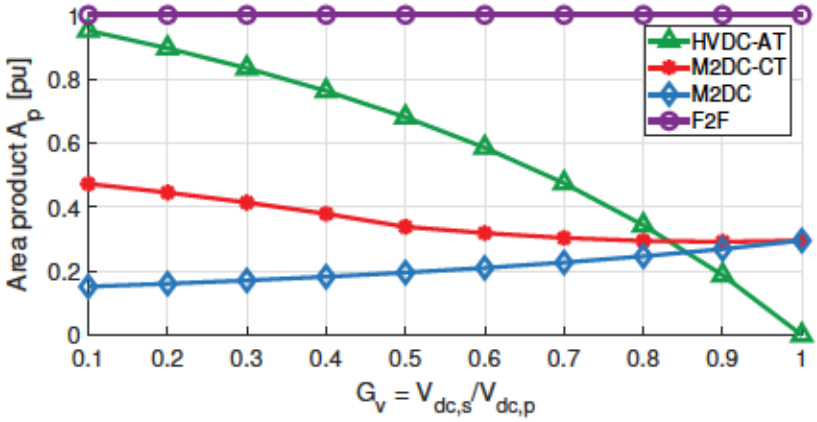

Figure 2.30: Magnetics core area product normalized to F2F-MMC's area product; HVDC-AT, M2DC and M2DC-CT utilize FBSMs to enable bidirectional fault blocking capability; F2F-MMC utilizes HBSMs

2.7.4 Converter Losses

This section calculates the losses of the four dc-dc converter topologies. The conduction and switching losses of the semiconductors as well as winding and core losses of the magnetics are considered as dominant losses in the converters.

Semiconductor losses

The semiconductor conduction and switching losses are calculated using a similar method as in [13, 50, 51]. Each HBSM contains two IGBTs T1 and T2 and two diodes D1 and D2. During one fundamental period, each converter arm will conduct positive and negative current, represented by subscripts $-$ and $+$, respectively.

$$i_{arm,+}(t) = \begin{cases} i_{arm}(t), & if\ i_{arm}(t) > 0 \\ 0, & else \end{cases} \tag{2.44}$$

$$i_{arm,+}(t) = \begin{cases} 0, & if\ i_{arm}(t) < 0 \\ -i_{arm}(t), & else \end{cases} \tag{2.45}$$

Duty cycle $\alpha_{arm}(t)$ determines if a HBSM is on-state in this arm. On the contrary, the complement $(1 - \alpha_{arm}(t))$ determines if a HBSM is off-state in this arm. In other words, the duty cycle determines which part of a HBSM (T1, T2, D1 or D2) is on-state and therefore produces conduction and switching losses. This is essential due to the fact that IGBTs and diodes exhibit different forward resistances and switching energies. The duty cycle of the converter arm at a given point in time t is

$$\alpha_{arm}(t) = \frac{|v_{arm}(t)|}{N_{sm,arm} V_c} \tag{2.46}$$

Note that $N_{sm,arm}$ different from the N_{arm} as per (2.37). The conduction and switching losses of a FBSM can easily be estimated by multiplying the losses of the HBSM with 2. Thus, the duty cycle of converter arms that utilize both HB and FB SMs can estimated by using newly defined number of semiconductor $N_{sm,arm}$

$$N_{sm,arm} = N_{HB,arm} + 2N_{FB,arm} \tag{2.47}$$

Consequently, the average conduction losses of each semiconductor in this arm are calculated by weighting the conduction losses with the number of SMs in on-state and off-state

$$P_{L,cond,arm,T1} = \frac{1}{T} \int_0^T \alpha_{arm}(t) \cdot (V_{T,0} + R_T i_{arm,-}(t)) \cdot i_{arm,-}(t) dt \tag{2.48}$$

$$P_{L,cond,arm,D1} = \frac{1}{T}\int_0^T \alpha_{arm}(t)\cdot(V_{F,0} + R_F i_{arm,+}(t))\cdot i_{arm,+}(t)dt \tag{2.49}$$

$$P_{L,cond,arm,T2} = \frac{1}{T}\int_0^T (1-\alpha_{arm}(t))\cdot(V_{T,0} + R_T i_{arm,+}(t))\cdot i_{arm,+}(t)dt \tag{2.50}$$

$$P_{L,cond,arm,D2} = \frac{1}{T}\int_0^T (1-\alpha_{arm}(t))\cdot(V_{F,0} + R_F i_{arm,-}(t))\cdot i_{arm,-}(t)dt \tag{2.51}$$

$$P_{L,cond,arm,sm} = P_{L,cond,arm,T1} + P_{L,cond,arm,D1} + P_{L,cond,arm,T2} + P_{L,cond,arm,D2} \tag{2.52}$$

where $V_{T,0}$, $V_{F,0}$, R_T and R_F are the forward voltage drops of IGBTs and diodes, respectively. T is fundamental frequency period. The semiconductor switching losses are estimated as:

$$P_{L,sw,arm,T1} = \frac{\bar{f}_{sw,arm}}{T}\int_0^T E_{T,on}(V_c, i_{arm,-}(t)) + E_{T,off}(V_c, i_{arm,-}(t))dt \tag{2.53}$$

$$P_{L,sw,arm,D1} = \frac{\bar{f}_{sw,arm}}{T}\int_0^T E_{D,rr}(V_c, i_{arm,+}(t))dt \tag{2.54}$$

$$P_{L,sw,arm,T2} = \frac{\bar{f}_{sw,arm}}{T}\int_0^T E_{T,on}(V_c, i_{arm,+}(t)) + E_{T,off}(V_c, i_{arm,+}(t))dt \tag{2.55}$$

$$P_{L,sw,arm,D2} = \frac{\bar{f}_{sw,arm}}{T}\int_0^T E_{D,rr}(V_c, i_{arm,-}(t))dt \tag{2.56}$$

$$P_{L,sw,arm,sm} = P_{L,sw,arm,T1} + P_{L,sw,arm,D1} + P_{L,sw,arm,T2} + P_{L,sw,arm,D2} \tag{2.57}$$

where $E_{T,on}$, $E_{T,off}$ and $E_{D,rr}$ are the turn-on and turn-off energies of IGBTs, and the reverse recovery energy of the diodes obtained at the condition of I_{ref} and V_{ref}, respectively.

$$E(V_c, i_{arm}(t)) = E\cdot\frac{V_c}{V_{ref}I_{ref}}\cdot i_{arm}(t) \tag{2.58}$$

$\bar{f}_{sw,arm}$ is the average frequency of switching actions for one arm which depends on the peak fundamental arm ac voltage $\hat{v}_{arm}$, fundamental frequency f, the nominal SM capacitor voltage V_c and number of semiconductor N_{arm}. Additionally, a safety factor k_{sw} that takes the additional switching actions needed for SM capacitor voltage balancing into account is set to 1.2.

$$\bar{f}_{sw,arm} = k_{sw}\cdot f\cdot\frac{2\hat{v}_{arm}}{N_{arm}V_c} \tag{2.59}$$

Since the semiconductor losses calculation is dependent on technology, the Mitsubishi CM1200HC-90R HVIGBT with a rating of 4500 V and 1200 A is used for all topologies. IGBTs are paralleled as needed to accommodate arm currents that exceed switch ratings, e.g., at low G_v for the M2DC. The converters operate at $f =$ 150Hz.

Magnetics losses

In the following, a method to approximate the magnetics losses is proposed that does not require detailed core design[2] (for the reasons stated in section 2.7.3) but still accounts for changes in area product due to inter-winding dc voltage stresses. The core loss, $P_{L,core}$, and copper loss, $P_{L,copper}$, are the two types of losses in a magnetic structure. Assumptions are made for estimating these loss components as follows:

- $P_{L,core}$ and $P_{L,copper}$ are usually designed to be similar to maximize efficiency [76, 77], and thus they are assumed to be the same;
- Total magnetic losses ($P_{L,core}$ and $P_{L,copper}$) increase with the transferred power [50], and it is estimated to be 0.5% of the magnetic Volt-Ampere rating [13, 51].

The combined copper and core losses for magnetics in the M2DC and M2DC-CT are thus approximated as

$$P_{L,copper} + P_{L,core} = 0.5\% \cdot S_w. \tag{2.60}$$

Loss estimate (2.60) is suitable for the M2DC and M2DC-CT where there is no dc voltage stress between windings on the core and hence no extra insulation requirements. However, it would not account for an increase in the size and weight of the magnetic core that results from increased area product, due to extra insulation requirements needed to accommodate inter-winding dc voltage stresses. This core volume increase would cause the core losses to go up for the same power rating [78]. Therefore, to estimate the total magnetics losses for the HVDC-AT and F2F-MMC, (2.60) is modified as follows

$$P_{L,copper} + P_{L,core} = 0.5\% \cdot S_w \cdot \left(\frac{A_p}{A_{p,nom}}\right)^k, \tag{2.61}$$

where A_p is the actual area product of the magnetic structure and $A_{p,nom}$ is the area product of the magnetic structure with the same power rating but without extra dc insulation requirement (i.e., with $V_{dc,iso} = 0$). Coefficient $k = 0.75$ represents the core volume-area product relationship [71].

Fig. 2.31 plots the computed converter losses as well as the resulting efficiency for the HVDC-AT, M2DC-CT, M2DC and F2F-MMC with HBSMs. The switching losses for the HVDC-AT, M2DC-CT and M2DC are nearly identical, however, only the HVDC-AT and M2DC-CT achieve the lowest conduction losses across all dc step ratios. The M2DC experiences increased conduction losses for $G_v \neq 0.5$; specifically, it sees extremely high losses for $G_v << 0.5$ and high losses as G_v approaches unity.

[2]For information on power converter transformer design, references [74, 76] can be consulted

This is due to the increased arm current stresses at these operating points, as shown in Figs. 2.20 and 2.21. However, the M2DC enjoys the lowest magnetics losses across all dc step ratios. The magnetics losses for the M2DC-CT falls somewhere between the M2DC and HVDC-AT. The efficiency plot in Fig. 2.31 reveals the M2DC has the highest efficiency around $G_v = 0.5$, due to relatively low magnetics losses, but at lower and higher dc step ratios the efficiency drops off because of increased conduction losses. Except for dc step ratios ranging from around 0.5, the M2DC-CT has the highest efficiency.

Fig. 2.32 plots the computed converter losses as well as the resulting efficiency for the HVDC-AT, M2DC-CT, M2DC and F2F-MMC with FBSMs. The switching losses for the HVDC-AT, M2DC-CT and M2DC are nearly identical, however, only the HVDC-AT and M2DC-CT achieve the lowest conduction losses across all dc step ratios. Unlike the M2DC with HBSMs, the conduction losses of the M2DC with FBSMs decreases for $G_v > 0.5$, due to the additional headroom provided by FBSMs for maximizing arm ac voltages. The magnetics losses of the M2DC and M2DC-CT with FBSMs increase for $G_v > 0.5$ compared with the results in Fig. 2.31. Consequently, the efficiency plot in Fig. 2.32 reveals the HVDC-AT instead of the M2DC-CT has the highest efficiency for $G_v > 0.8$ when FBSMs are employed. However, the M2DC-CT with FBSMs still has the highest efficiency for $G_v < 0.8$. The M2DC with FBSMs has nearly identical efficiency as the M2DC-CT with FBSMs for dc step ratios ranging from 0.5 to 0.8.

2.7.5 Discussion and Implications

The non-isolated M2DC, HVDC-AT and proposed M2DC-CT were compared in terms of arms peak current stresses, semiconductor effort, magnetics core area product and converter losses. The isolated F2F-MMC was included in the comparison for reference. The key outcomes are:

- The M2DC-CT and HVDC-AT have the lowest overall peak current stresses for the arms and has the lowest total semiconductor effort, across all dc step ratios.
- The core area product for the M2DC-CT is larger than the M2DC but always lower than the HVDC-AT, with the M2DC-CT achieving around a 50% reduction relative to the HVDC-AT across all dc step ratios. This translates to considerable reduction in magnetics size and weight (and consequently lower losses).
- The M2DC shows superior performance at around $G_v = 0.5 \pm 0.1$ in terms of

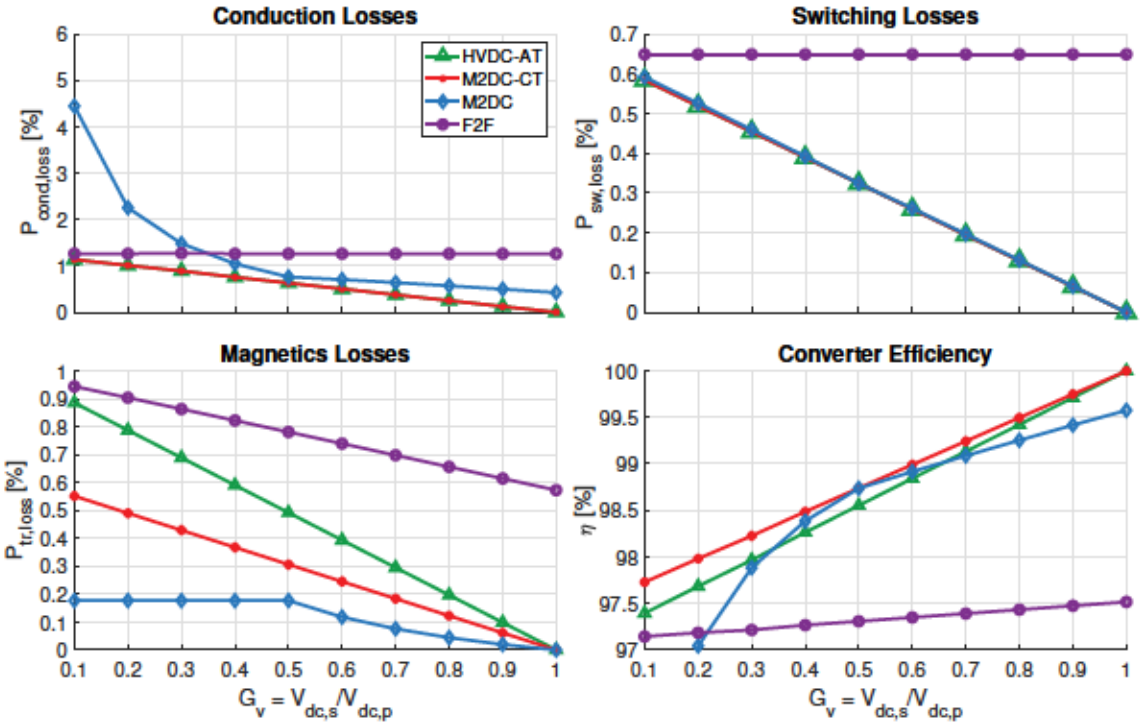

Figure 2.31: Losses (normalized to dc power transfer P_{dc}) and efficiency analysis; four converters utilize HBSMs in all arms

efficiency and magnetic requirement. However, outside this range of dc step ratios, the M2DC-CT has the highest efficiency due to minimized ac currents and reduced size of magnetic structure. The HVDC-AT also has good efficiency and magnetics requirements for G_v approaching unity, but its losses and magnetics requirements suffer as G_v decreases below 0.5.

- Enabling fault blocking for the M2DC and M2DC-CT will lead to larger core area product for large dc step ratios, and hence more magnetic losses. Consequently, the HVDC-AT has the highest efficiency and smallest magnetics for G_v approaching unity ($G_v > 0.8$).

From on these observations, potential applications are identified for the M2DC-CT as follows that are categorized based on the required dc step ratio.

Lower values of G_v ($V_{dc,s} << V_{dc,p}$)

The benefits of the proposed M2DC-CT are most pronounced at low dc step ratios where the (i) M2DC becomes impractical due to very high current stresses, and (ii) the HVDC-AT suffers from large size and weight of the magnetics, becoming comparable to the full rated F2F-MMC transformer. The HVDC-AT and M2DC-CT

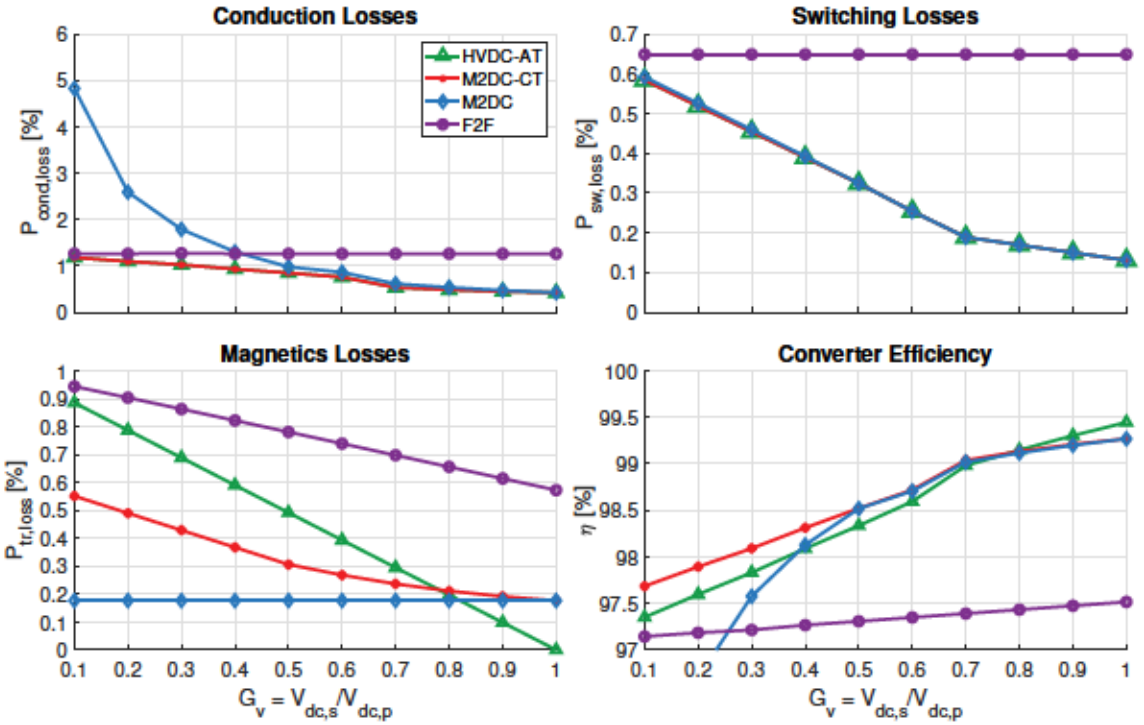

Figure 2.32: Losses (normalized to dc power transfer P_{dc}) and efficiency analysis; HVDC-AT, M2DC and M2DC-CT utilize FBSMs to enable bidirectional fault blocking capability; F2F-MMC utilizes HBSMs

have similar conduction and switching losses in this region, but the bulky transformer in the HVDC-AT makes its efficiency marginally lower than the M2DC-CT. This factor becomes important for applications where space is limited, for example, when designing dc collector systems for offshore wind farms with pure dc power systems where converter station footprint, weight, efficiency and cost are critical [29, 55]. Furthermore, a higher transformer ac-stage frequency leads to a significant reduction of the transformer size and weight. Using medium frequency transformer has became a trend for increasing the power density for dc-dc power converters [79]. However, the possibility of size reduction by increasing the operating frequency will be limited by insulation requirement [64, 80]. Thus, the M2DC-CT will become an attractive alternative for dc-dc power conversion that using medium frequency transformers due to no dc insulation stress.

Applications that require lower values of G_v, i.e., $G_v < 0.4$, where the M2DC-CT is well suited include

- HVDC-to-MVDC grids interconnects;
- Connecting offshore wind MVDC collector networks with onshore HVDC sta-

tions as shown in Fig. 2.33a;

- HVDC power tapping with MVDC bus output as shown in Fig. 2.33b.

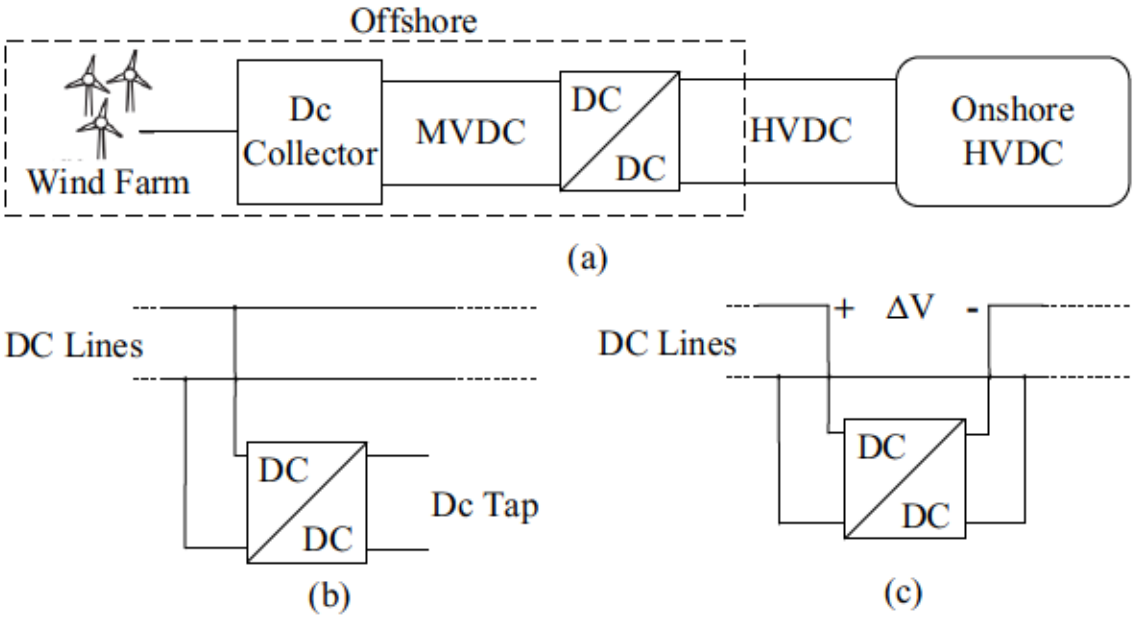

Figure 2.33: M2DC-CT structure used as (a) connecting offshore wind MVDC collector networks to onshore HVDC stations, (b) HVDC power tapping, (c) dc line power flow controller

Higher values of G_v ($V_{dc,s} \approx V_{dc,p}$)

The M2DC-CT is also an attractive option at high dc step ratios where it has the highest efficiency and the size and weight of its magnetics become somewhat comparable to the M2DC. However, weight and footprint of the converter system are usually not critical for applications where space is not limited, e.g., for HVDC grids interconnection [29]. Thus, the M2DC-CT (and the HVDC-AT) offers an alternative solution to the M2DC with higher efficiency but marginally larger magnetics.

Applications that require higher values of G_v, i.e., $G_v >> 0.6$, where the M2DC-CT is a competitive option include

- Interconnecting HVDC (or MVDC) systems of similar voltages;
- Dc line power flow controllers where only incremental series dc voltage injection (ΔV) by p arms is needed[3] and bidirectional fault blocking is not required, see Fig. 2.33c.

[3]Dc line voltage is supported by s arms

2.8 Three-String M2DC-CT as Three-Port Converter

In this section, the two-string M2DC-CT in Fig. 2.2a is extended to a three-string implementation by using a double zig-zag transformer arrangement as shown in Fig. 2.34a. This modification allows the two-port M2DC-CT to be adapted for external three-phase ac grid connectivity by adding grid side transformer winding as shown in Fig. 2.34b. The three-port M2DC-CT allows dc-dc-ac energy transfer (between two dc systems and a nearby ac grid). The multi-frequency power transfer (dc and ac) occurring at the MMC midpoint is enabled by double zig-zag transformer with grid side transformer winding as shown in Fig. 2.34c. The double zig-zag arrangement is needed to ensure core dc flux cancellation. The dc and ac current flows are shown with red and blue arrows, respectively. The MMC arms see unequal dc currents (dc_1 and dc_2) with opposite directions as shown in Fig. 2.34c. In addition to transfer circulating ac power ($ac_1 - ac_2$ in Fig. 2.34c) and output dc power ($dc_1 + dc_2$) in two-string M2DC-CT, additional ac power ac_3 is transferred to the grid at the MMC midpoint node in three-string with external ac grid connectivity.

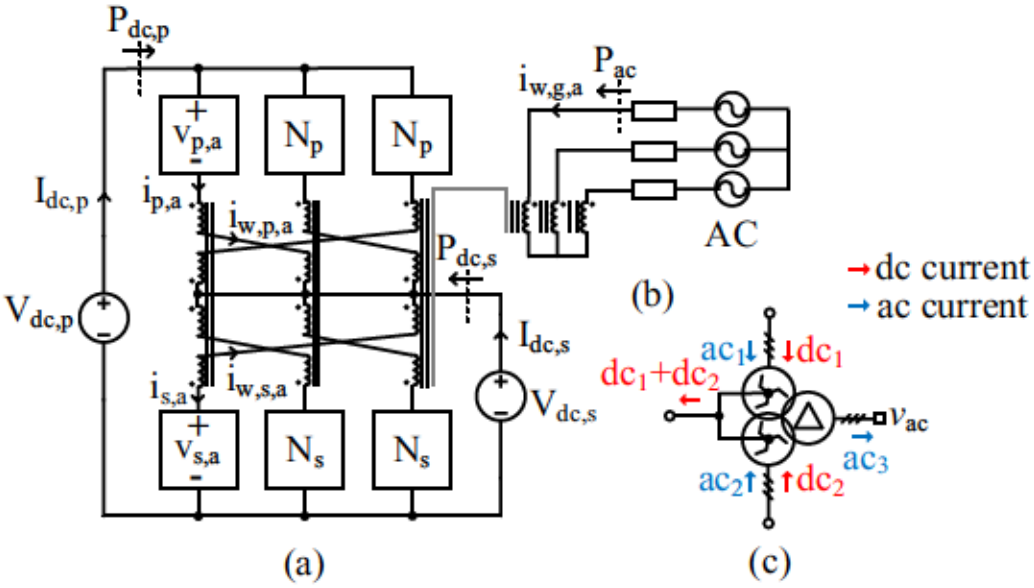

Figure 2.34: (a) Two-port three-string M2DC-CT (b) grid side transformer winding for three-port dc-dc-ac energy transfer (c) three-phase transformer winding configuration with dc and ac current flows

2.8.1 Simulated Waveforms of Three-Port M2DC-CT

Fig. 2.35 shows simulation results for three-phase M2DC-CT with external ac grid connectivity operating at $V_{dc,p} = 400$ kV, $V_{dc,s} = 200$ kV ($G_v = 0.5$), $V_{ac,LL(rms)} = 220$ kV, $P_{dc,p} = 400$ MW, $P_{dc,s} =$ -300 MW and $P_{ac} =$ -100 MW. Fig. 2.36 shows simulation results for three-phase M2DC-CT with external ac grid connectivity operating at $V_{dc,p} = 400$ kV, $V_{dc,s} = 40$ kV ($G_v = 0.1$), $V_{ac,LL(rms)} = 220$ kV, $P_{dc,p} = 300$ MW, $P_{dc,s} =$ -75 MW and $P_{ac} =$ -225 MW. Simulations are conducted in PSCAD/EMTDC using a detailed equivalent switching model. Voltage balancing of capacitors within each arm is achieved using the sort and selection method. Only HBSMs are required. The zig-zag transformer in Fig. 2.34 enables both dc and ac power transfers. That is, converter-side common-mode dc currents in each phase sum together at the zig-zag neutral point while positive (and negative) sequence ac winding currents propagate to the grid via transformer action. The transformer windings requires to carry both dc and ac currents, however, the windings orientation provides core dc flux cancellation. The simulations confirm the zig-zag transformer can be adopted for both dc output filter and ac power transfer with grid. Filter efficacy is verified by the very low fundamental frequency content of $i_{dc,s}$. Unlike two-string M2DC-CT, observe primary dc current $i_{dc,p}$ and secondary dc current $i_{dc,s}$ for the three-phase DC-MMC is now free of second harmonic component. This benefit is a result of net second harmonic ac current cancellation (phase-shifted by 120° between strings) at the dc input rails of the converter. By choosing the transformer turns ratio based on (2.18), both primary and secondary fundamental ac arm currents in Figs. 2.36 and 2.35 are near the optimal 2 p.u. value (relative to arm dc currents).

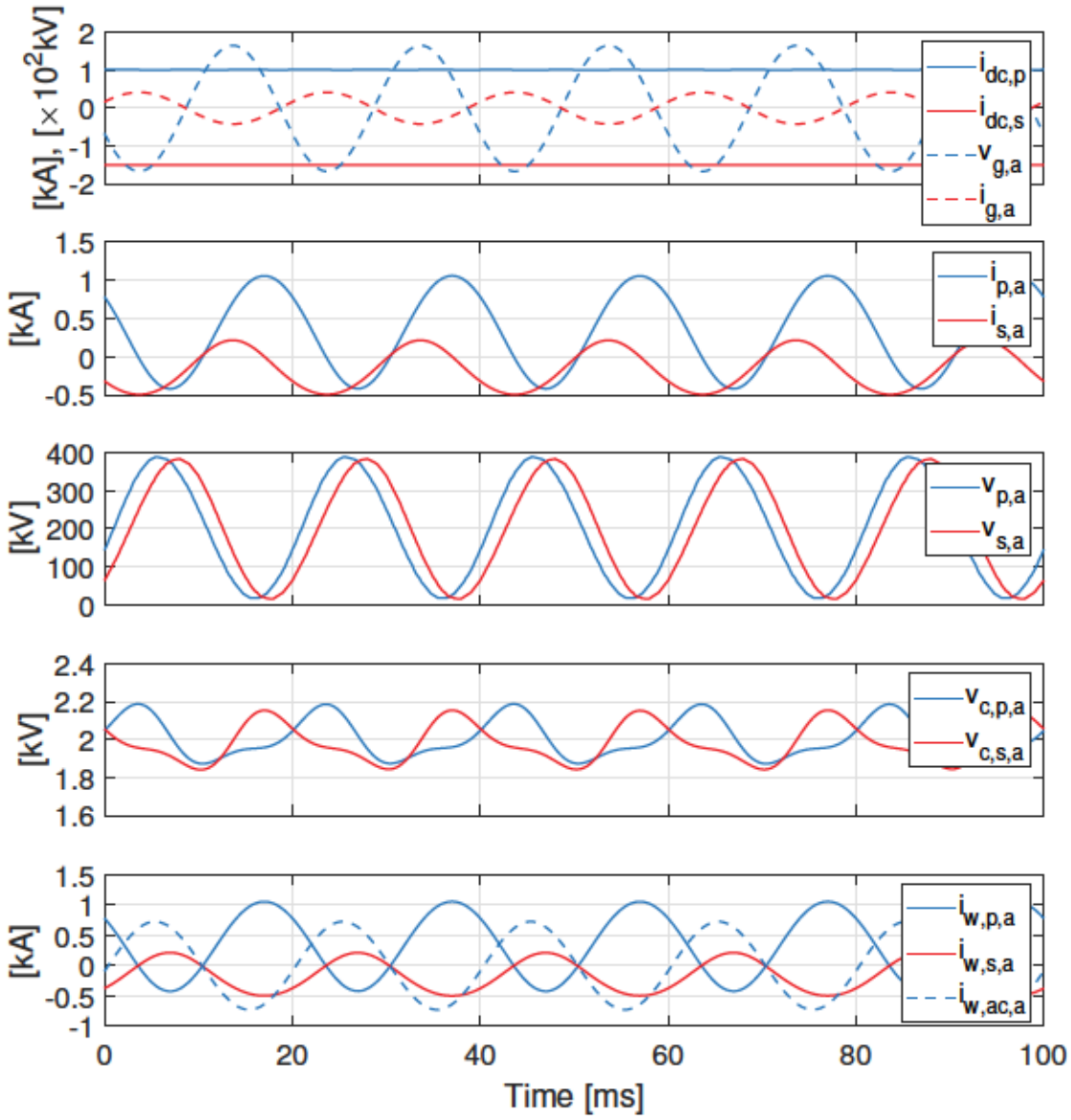

Figure 2.35: Steady-state three-port M2DC-CT current and voltage waveforms, where $V_{dc,p}$ = 400 kV, $V_{dc,s}$ = 200 kV, $V_{ac,LL(rms)}$ = 220 kV, $P_{dc,p}$ = 400 MW, $P_{dc,s}$ = -300 MW and P_{ac} = -100 MW

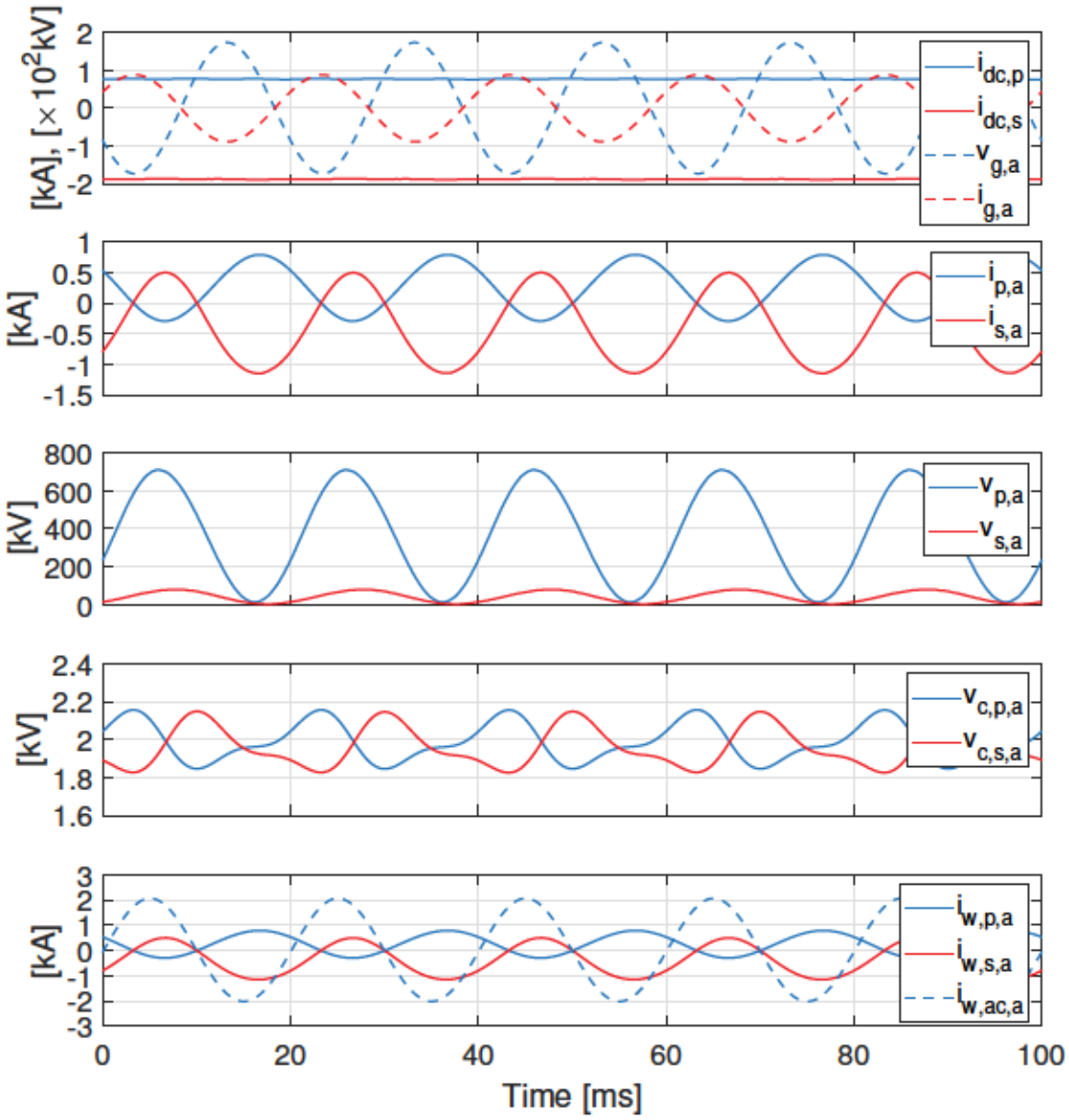

Figure 2.36: Steady-state three-port M2DC-CT current and voltage waveforms, where $V_{dc,p} = 400$ kV, $V_{dc,s} = 40$ kV, $V_{ac,LL(rms)} = 220$ kV, $P_{dc,p} = 300$ MW, $P_{dc,s} =$ -75 MW and $P_{ac} =$ -225 MW

2.9 Chapter Summary

A new class of partial-power-processing dc-dc MMC is presented that merges the best traits of the M2DC and HVDC-AT. This new converter, termed the M2DC-CT, exploits a multi-winding center-tapped transformer to minimize ac arm currents for a wide range of dc step ratios while simultaneously avoiding any dc voltage stress between windings. These features cannot be simultaneously obtained with the HVDC-AT nor the M2DC, and come with the caveat of the transformer carrying both dc and ac currents. However, a comparative analysis reveals that the transformer core area product is always lower than the HVDC-AT due to elimination of inter-winding dc voltage stress, yielding an approximate 50% reduction at all dc step ratios. This implies significant savings in magnetics size and weight. Based on a derived mathematical model, a dynamic controller is proposed for the M2DC-CT that regulates dc power transfer while ensuring balanced capacitor voltages. The M2DC-CT operation and dynamic controls are validated through PSCAD/EMTDC simulations and laboratory experiments for a scaled-down 250/85 V, 1.25 kW prototype. It is suitable for dc-dc applications requiring high or low dc step ratios, for example,

1. HVDC-to-MVDC grids interconnects;
2. Connecting offshore wind MVDC collector networks to offshore HVDC stations;
3. HVDC power tapping with MVDC bus output;
4. Interconnecting HVDC systems of similar voltages;
5. Dc line power flow controllers where only incremental series dc voltage injection is needed.

In the proposed two-string M2DC-CT, which is based on the premise of Fig. 1.5a, multi-frequency power transfer happens at the MMC midpoint node for i) internally circulating ac power and ii) output dc power. Building upon this novel multi-frequency power transfer mechanism, a three-string M2DC-CT with integrated ac grid connectivity is introduced. This three-port structure allows simultaneous energy transfer between two dc systems and a nearby ac grid, an attractive feature for ac power systems overlaid with dc grids or for mixed ac/dc grids.

Chapter 3

Multi-Frequency Dual MMC Chain-Link Structure for Bipolar DC Systems

The growing global trend of integrating renewable energy resources such as wind turbines and photovoltaics into the legacy ac grid is giving rise to mixed ac/dc power systems. Innovative concepts such as ac overlaid meshed dc systems, often referred to as supergrids, allow higher utilization of existing ac infrastructure while improving reliability and flexibility [81]. These supergrids are likely to evolve over time from the interconnection of many smaller independent systems. During this development process, existing HVAC grids will be upgraded or integrated to the HVDC grids to enhance their power transfer capability and system stability. Consequently, HVDC and MVDC systems will become increasingly intertwined with existing ac grids.

As been discussed in Section 1.1, symmetrical monopolar and bipolar dc configurations are mainly utilized in recent MMC projects for increased transmission power and reliability. The former has been the dominant scheme for offshore wind power projects (e.g. [8]). The latter configuration is well suited for onshore dc systems (e.g. [9]) where high reliability and increased power levels are often demanded. The bipolar MMC offers independent control of two dc poles, however may require multiple MMCs [82, 83]. The symmetrical monopolar MMC offers a cost-effective solution to satisfy the need for bulk-power interconnection and to minimize the dc insulation levels required. However, the two dc pole voltage levels may not balance all the time. Previous work has been focus on providing ground return path for the symmetrical monopolar MMC using extra grounding devices to imitate bipolar operation [23, 24].

The three-port M2DC-CT presented in Fig. 2.34 allows multi-frequency power transfer between two dc systems and a nearby ac grid at the converter midpoint node, similar to Fig. 1.5b. However, the magnetics solution in Fig. 2.34c requires a

relatively complicated transformer arrangement, and the windings always carry both dc and ac currents regardless of the port power flows. To improve on this solution, this chapter proposes a multi-frequency dual MMC structure that uses three converter-side center-tapped windings and ties together their midpoints to form an additional dc port. The resulting multi-frequency structure is shown to yield a novel bipolar MMC that allows fully independent control of the dc pole power injections to accommodate unbalanced conditions. Similar to the M2DC-CT, dc flux cancellation is imposed in the transformer core. More importantly, the employed center-tapped transformer has a Volt-Ampere rating that is the same as a conventional grid interfacing transformer, and thus the pole balancing capability is obtained without incurring any penalty in magnetics rating. A unified control scheme is developed that independently controls dc and ac terminals power transfers for the proposed multi-frequency dual MMC while keeping steady-state submodule capacitor voltages balanced. Converter operation and dynamic controls are validated by simulation and experiment.

3.1 Existing MMC Structures for Bipolar DC Systems

Consider the bipolar MMC structure shown in Fig. 3.1 [82, 83], where two MMCs interface with the ac grid via a three-phase three-winding transformer. This three-port setup is the well-known dc-dc F2F-MMC topology (first proposed in [31]) augmented with an ac grid connection, with equal dc port voltages $V_{dc,p} = V_{dc,n}$. The dc and ac power flows are shown with red and blue arrows, respectively. The MMCs in Fig. 3.1 use classical transformer action to transfer ac power at their respective midpoint nodes. That is, the transformer connected at the midpoint of each MMC carries only ac current (represented by blue arrows in Fig. 3.1). In case where the load demand of the dc poles is unbalanced ($dc_1 + dc_2 \neq 0$ in Fig. 3.1), each MMC regulates its respective pole dc power injection and the unbalanced dc current flow to the ground through the midpoint of the two MMCs. The bipolar MMC structure in Fig. 3.1 also has other advantages such as high reliability, excellent scalability, and dc fault ride-through capability (when using appropriate SM type) [83]. The MMCs typically use HBSMs, although FBSMs can be employed for enhanced features such as maintaining healthy pole operation and providing reactive power grid support during dc side fault events. $V_{dc,p}$, $V_{dc,n}$, v_{ac} in Fig. 3.1 are all galvanically separated, however, the ac grid interfacing transformers must tolerate a large dc voltage bias (50% of $V_{dc,p} + V_{dc,n}$) between windings [56]. This leads to increased size, weight and core design complexity for the transformer [84].

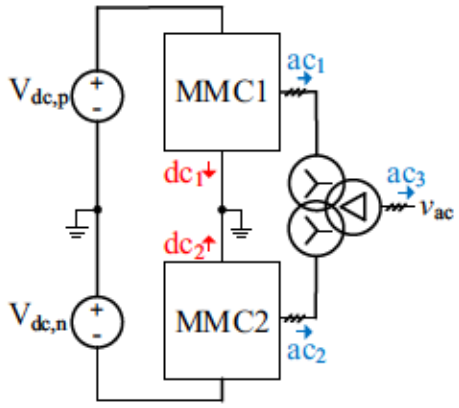

Figure 3.1: Dual MMC structure for bipolar $+V_{dc,p}/-V_{dc,n}$ dc system based on F2F-MMC with transformer

The single frequency operation in Fig. 3.1 where dc and ac power transfers occur at separate nodes is standard practice in MMCs. The three-phase M2DC-CT with ac grid connectivity introduced in Section 2.8 enables both dc and ac (multi-frequency) power transfer at the MMC midpoint node. This flexible dc-dc-ac MMC structure can be deployed for bipolar dc configuration, as shown in Fig. 3.2. This is achieved by multi-tasking the transformer, where multi-tasking refers to the transformer winding currents having multiple frequency components at the converter side. That is, converter-side common-mode dc currents (represented by red arrows in Fig. 3.2) in each phase sum together at the zig-zag neutral point while positive (and negative) sequence ac winding currents (represented by blue arrows in Fig. 3.2) propagate to the grid via transformer action. The M2DC-CT proposed in Chapter 2 is best suited for applications requiring high or low dc step ratios. The bipolar M2DC-CT in Fig. 3.2 is thus not an ideal option as $V_{dc,p} = V_{dc,n}$ corresponds to a moderate dc step ratio of 0.5. Moreover, the complicated and costly winding arrangement make it less attractive.

Some recent works are exploiting the same concept of multi-frequency power transfer in single MMC setup, termed multi-frequency bipolar MMC, to gain increased power flow flexibility and improved component utilization. To elucidate, consider the single MMC setup in Figs. 3.3a and 3.3b, where both dc and ac power transfers can occur at the MMC midpoint node. The bipolar MMC structure in Fig. 3.3a uses a conventional transformer and *Filter* block[1] to enable ac and dc power transfers [19, 67, 85]. It is identical to the symmetrical monopolar MMC configuration with additional ground device in Fig. 1.1d. Unbalanced loading of the dc poles can be readily accommodated by driving the necessary dc balancing current through the *Filter*. In-

[1]Possible implementations include magnetics, passive filters and additional SMs [16]

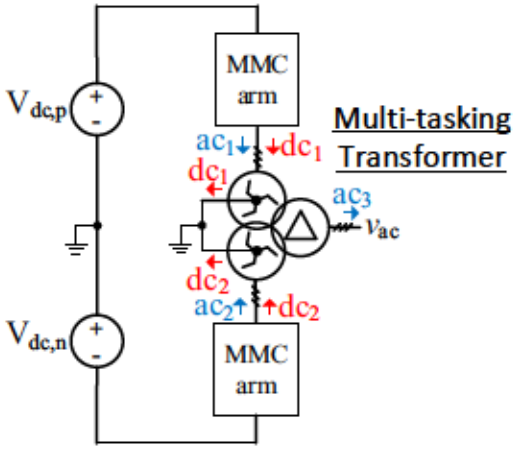

Figure 3.2: Single MMC structure for bipolar $+V_{dc,p}/-V_{dc,n}$ dc system based on M2DC-CT with multi-tasking zig-zag transformer in series with the converter arms

terestingly, the MMC & *Filter* constitute the dc-dc M2DC [11, 12, 14] while the MMC & transformer is the conventional dc-ac MMC.

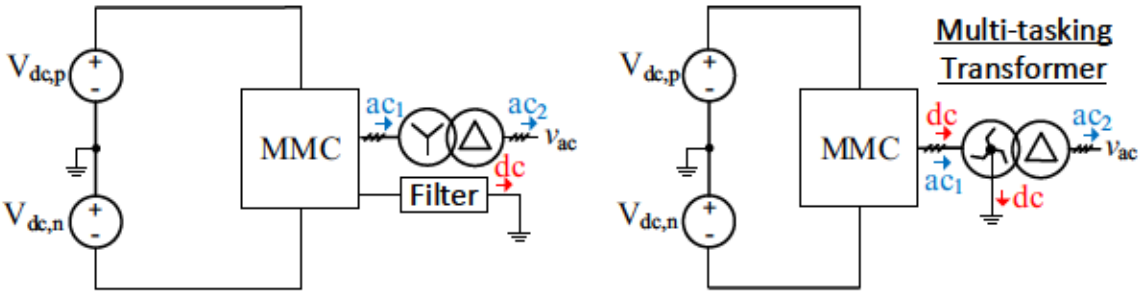

Figure 3.3: Single MMC structure for bipolar $+V_{dc,p}/-V_{dc,n}$ dc system based on: (a) M2DC with transformer [19, 67, 85], (b) MMC with multi-tasking zig-zag transformer [17, 18]

The bipolar MMC structure in Fig. 3.3b improves upon Fig. 3.3a by using a zig-zag transformer that cleverly combines the functions of the transformer and *Filter* [17, 18]. This is also achieved by multi-tasking the zig-zag transformer. In this case, the transformer is not in series with the converter arm. The transformer windings on the converter side must carry both dc and fundamental frequency ac currents, as shown in Fig. 3.3b with the red and blue arrows. Dc flux cancellation is imposed in the core as long as the dc currents in each zig-zag winding are the same, which is ensured via control [17]. In fact, the idea of using a zig-zag transformer connection to create multi-frequency power systems is not new [86, 87]. Consequently, the *Filter* block in Fig. 3.3a is eliminated. And, perhaps most importantly, the total Volt-Ampere rating

of the zig-zag transformer is the same as the transformer in Fig. 3.3a [17].

3.2 Proposed Bipolar Dual MMC Structure

Figs. 3.3a and 3.3b use identical MMC structures but the latter avoids a costly and bulky filter by multi-tasking a zig-zag transformer with multiple frequency components (without incurring any penalty in transformer Volt-Ampere rating). Therefore, Fig. 3.3b remains the only cost-effective MMC option that uses the multi-frequency power transfer mechanism in bipolar dc applications, although the requisite zig-zag transformer has a more complicated winding arrangement and thus higher manufacturing cost [17]. This gives researchers and industry little choice in converter selection and design. Therefore, a primary motivator of this chapter is to seek an alternative MMC structure that retains the benefits of Fig. 3.3b but offers a relatively simpler magnetics implementation.

This section proposes a multi-frequency dual MMC chain-link structure for bipolar configuration as shown in Fig. 3.4. *Chain-link* refers to the series cascading of many switching cells within an MMC structure [31]. Unlike prior art that uses single MMC setup, two parallel-connected MMCs operated in a differential fashion are used in the proposed MMC structure. The multi-frequency power transfer is achieved by multi-tasking a three-phase three-winding transformer with center-tapped (wye) windings on the converter side. Like zig-zag transformer in Figs. 3.3b, converter-side common-mode dc currents (represented by red arrows in Fig. 3.4) in each phase sum together at the transformer neutral point while positive (and negative) sequence ac winding currents (represented by blue arrows in Fig. 3.4) propagate to the grid via transformer action.

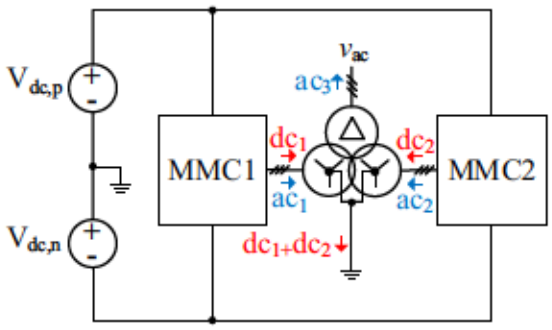

Figure 3.4: Proposed multi-frequency dual MMC chain-link structure for bipolar $+V_{dc,p}/-V_{dc,n}$ dc systems

The circuit schematic of the proposed bipolar dual MMC (Fig. 3.4) is shown in

Fig. 3.5. The transformer features one primary side winding and two secondary side windings for each phase. The primary windings are connected to the ac grid, while the

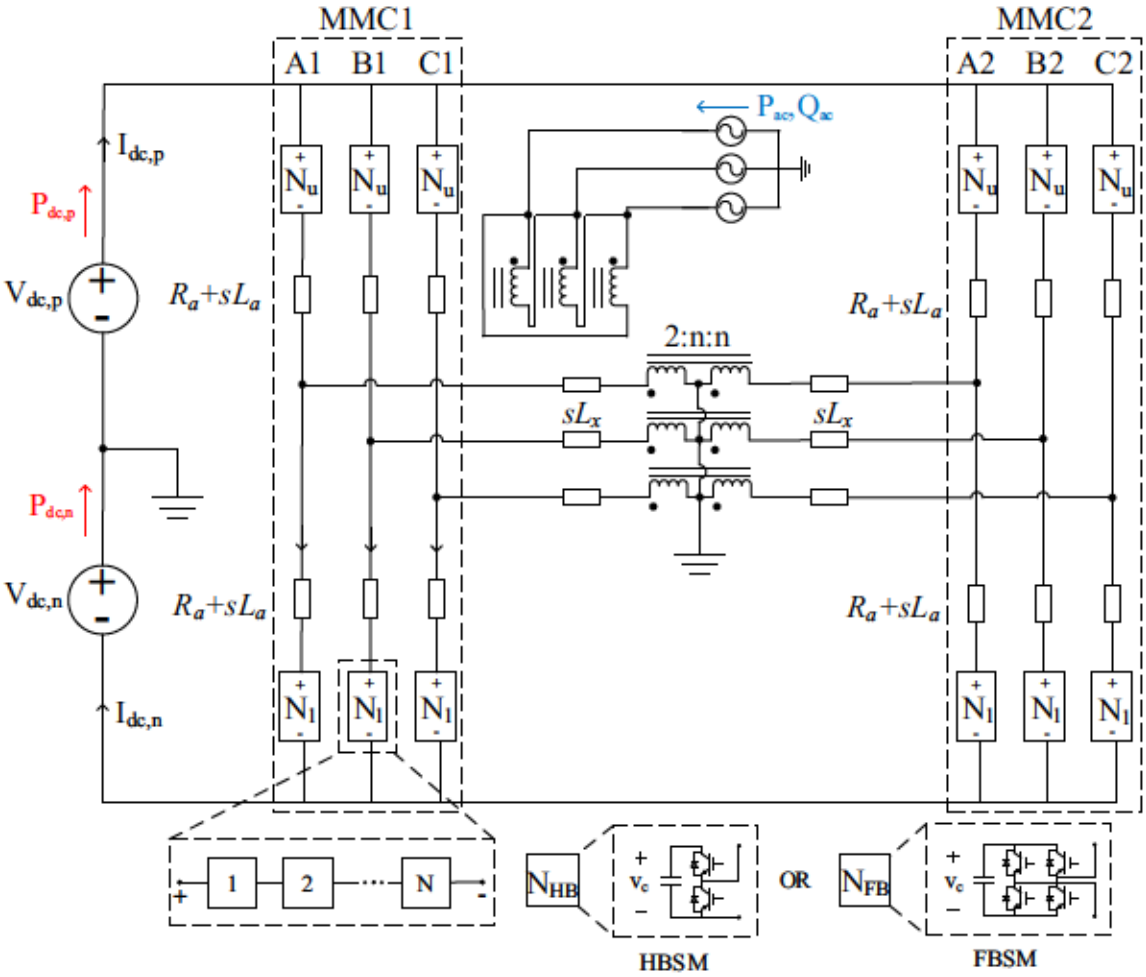

Figure 3.5: Proposed bipolar dual MMC circuit schematic

secondary windings with center-taps are connected to the converter. By connecting the common neutral wye-point of the transformer to the midpoint of the dc inputs, a dc balancing current can be injected as needed to balance the loading of the dc poles. This enables multi-frequency power transfer capability as the MMC midpoints can inject multiple frequency components. That is, fully independent control of dc pole power injections $P_{dc,p}$ and $P_{dc,n}$ can be achieved for enhanced reliability. P_{ac} and Q_{ac} are the three-phase ac grid power injections. The transformer windings are not subjected to dc voltage stresses, unlike traditional multi-pulse bipolar configurations, e.g., the bipolar circuit in Fig. 3.1. However, the transformer windings have to carry both dc and ac currents. The center-tap windings on the converter side have an equal number of turns but are wound in opposite directions around the transformer core

(represented by the dots) to provide core dc magnetic flux cancellation. The use of transformers in MMCs that handle dc and ac currents and have similar dc flux cancellation is an area of research interest [36, 58–62]. The transformer in Fig. 3.5 further features i) relative simplicity and lower in cost relative to the zig-zag transformer used in Fig. 3.3b as it only requires a symmetrical center-tap connection on each converter side winding [58], ii) identical Volt-Ampere rating relative to standard ac grid interfacing transformer in conventional MMC applications (ref. section 3.2.1), and iii) relatively small zero-sequence impedance allowing fast control of dc dynamics. This first reported use of a similar push-pull transformer arrangement with MMCs was in [58] for energy storage integration. Other works using similar concepts for lower voltage and power converter applications have since started to emerge [88–91].

Three-phase MMCs are used in Fig. 3.5, where each phase leg is comprised of two arms: an upper arm (and lower arm) with N_u (and N_l) cascaded SMs. The conventional HBSM is sufficient for standard operation. However, as with the traditional dc-ac MMC, FBSMs can be used to control the maximum arm ac voltage regardless of the available dc voltage in addition to providing dc fault interrupting capability [7, 50, 51]. But it will result in a higher number of power devices and commensurately higher power loss. Therefore, HBSMs are employed in this chapter.

3.2.1 Transformer Center-tapped Windings Current Stresses

The transformer grid side winding carries only fundamental frequency ac current at all times. Hence, it only needs to be rated for the grid side rms current, which is the same as the ac transformer used in conventional dc-ac MMC with the same power rating. This section will investigate the current stress of the converter-side center-tapped windings. In this analysis, i) the two dc pole voltages $V_{dc,p}$ and $V_{dc,n}$ are assumed to be equal and thus by design the number of SMs in upper and lower arms are the same and ii) the rated port power injections are $\{P_{ac}, Q_{ac}\} \in (-1, 1)$ p.u. and $\{P_{dc,p}, P_{dc,n}\} \in (-0.5, 0.5)$ p.u.. Assuming for ease of analysis that reactive power transfer is negligible, ac port power injection P_{ac} can be expressed as

$$P_{ac} = -(P_{dc,p} + P_{dc,n}) \tag{3.1}$$

The center-tapped winding currents can in general have both dc and ac components, thus the total center-tapped rms winding current of phase $a1$ can be approximated by

$$I_{a,trans,a1(rms)} = \sqrt{\left(\frac{I_{dc,p} - I_{dc,n}}{6}\right)^2 + \left(\frac{P_{ac}}{3V_{a,trans,a1(rms)}}\right)^2}, \tag{3.2}$$

where transformer secondary side voltage of phase a1 $V_{a,trans,a1(rms)} = (V_{dc,p}+V_{dc,n})/\sqrt{2}$ assuming maximum ac voltage utilization (unity modulation index).

Fig. 3.7 shows the calculated transformer center-tapped rms winding current across all possible port power transfers for the proposed bipolar dual MMC. Three different power flow scenarios are indicated by A,B,C in Fig. 3.7 as illustrative examples, based on the notation defined in Fig. 3.6 and Table 3.1. A,B,C correspond to pure dc-ac, pure dc-dc and dc-dc-ac power transfers, respectively. P_{ac} can be determined by (3.1). Dc-dc-ac power transfer is defined as when the center-tapped transformer winding currents have multiple frequency (both dc and ac) components. Although the transformer windings are subjected to both dc and ac current stresses, the total rms rating is $\leq$ 1 p.u. (which corresponds to rated rms current for a conventional ac transformer) across all power flow scenarios for bipolar dual MMC, as verified by Fig. 3.7. This is because as transformer windings at converter side start to carry dc current, there will be a corresponding reduction in ac grid current carried by the transformer. Consequently, the power rating of the transformer in bipolar dual MMC is equal to that of a conventional two-winding ac transformer, i.e., no penalty in transformer Volt-Ampere rating is incurred for the proposed bipolar dual MMC.

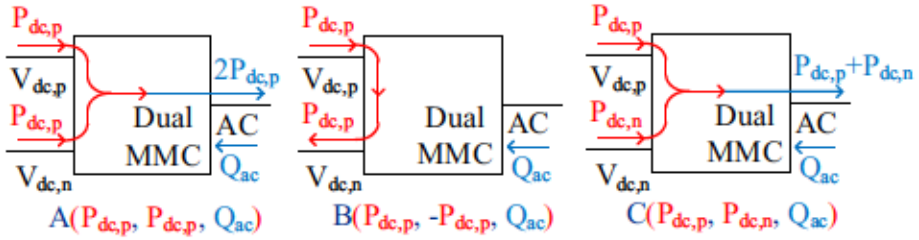

Figure 3.6: Bipolar MMC power flow scenarios under study

Table 3.1: Notation for Port Power Flow Scenarios in Fig. 3.6

Scenario	Port power flow notation
Pure dc-ac power transfer	A($P_{dc,p}$, $P_{dc,p}$, Q_{ac})
Pure dc-dc power transfer	B($P_{dc,p}$, -$P_{dc,p}$, Q_{ac})
Dc-dc-ac power transfer	C($P_{dc,p}$, $P_{dc,n}$, Q_{ac})

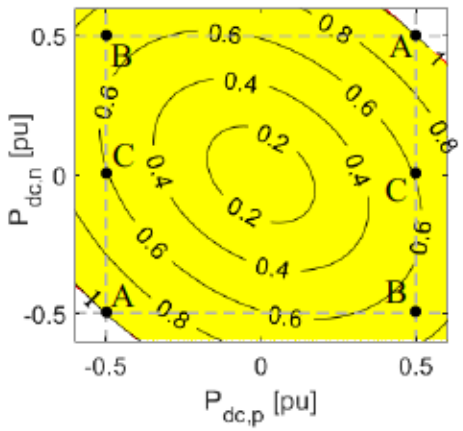

Figure 3.7: Calculated transformer center-tapped rms winding current for all possible port power transfers; The rms current is normalized to rated rms current of an ac transformer used in conventional dc-ac MMC with the same power rating

3.3 Comparison of Multi-frequency Bipolar MMC Structures

This section compares key characteristics of the three multi-frequency bipolar dual MMCs: bipolar M2DC in Fig. 3.3a, bipolar Zigzag-MMC in Fig. 3.3b, and the proposed bipolar dual MMC in Fig. 3.4 (hereinafter referred to as bipolar MF-Dual-MMC). The bipolar M2DC-CT in Fig. 3.2 is not compared here due to the complicated and costly winding arrangement. The results are summarized in Table 3.2, normalized to the requirements of the bipolar M2DC.

3.3.1 Power Transmission Capacity

The following conditions are set to compare the bipolar M2DC, bipolar Zigzag-MMC and bipolar MF-Dual-MMC.

- Dc port voltages for bipolar $+V_{dc,p}/-V_{dc,n}$ are the same.
- The capacitance, voltage and current ratings of individual submodule are the same.

The M2DC and Zigzag-MMC use a single MMC setup to achieve multi-frequency power transfer, while the MF-Dual-MMC parallels two MMCs operating in a differential fashion. Therefore, the number of submodules used in the MF-Dual-MMC as well as the total power rating of the semiconductors has to be installed are twice as that of other two MMC structures. Nevertheless, the power transmission capacity of the MF-Dual-MMC will also be doubled. Due to the same current and voltage stress

for individual submodule, three MMC structures will have the identical semiconductor power losses (i.e. conduction and switching losses) per submodule [92].

For three MMC structures to transfer same amount of power, reduced MMC submodule current stresses can be achieved in the MF-Dual-MMC. Restricted by the maximum current limit of IGBT, the MMC system can achieve large capacity power transmission mostly by stacking more SMs in series to achieve higher dc voltage level. The highest voltage level and capacity of currently operating projects are ±1100 kV and 12GW for LCC-based HVDC transmission [27], and ±500 kV and 3 GW for VSC-based HVDC transmission [9]. At present, hybrid HVDC projects (pure LCC as a rectifier and serial-connected LCC and VSC as inverter) is gaining research interests and will be applied in the future Baihetan State Grid ±800 kV HVDC project [25, 26]. This gives rise to the usage of parallel-connected MMC topologies for meeting the requirement of extremely high capacity power transmission. The dual MMC setup of the MF-Dual-MMC also provides an alternative solution to reduce the voltage levels and hence reduce the cost of insulation and over voltage design [21]. Therefore, the M2DC and Zigzag MMC is suitable for applications that has relatively lower current operation such as: i) HVDC power tapping with MVDC bus and ac grid output and ii) MVDC distribution system. The MF-Dual-MMC is suitable for applications that requires comparably higher current operation capability such as: i) Hybrid (VSC and LCC) HVDC (or MVDC) transmission systems; ii) hydro applications where generators' insulation constraints do not allow for an arbitrary increase in the operating voltages above a certain level [93] and iii) wind power applications where the voltage level of wind power transmission system can be significantly reduced while short-time large wind power can be transmitted out [94].

3.3.2 Multi-tasking transformer

The M2DC uses a conventional three-phase transformer to enable ac power transfer, while a filter is added to enable dc power transfer. The filter is subjected to the transformer voltage on the converter side and dc current would flow through each winding of filter (i.e. two-thirds of rated dc pole current for bipolar configuration). The Zigzag-MMC and MF-Dual-MMC cleverly combine the functions of the transformer and filter. The separate filter block is eliminated. The multi-tasking transformer windings of the Zigzag-MMC and MF-Dual-MMC on the converter side carry both dc and ac component. Dc flux cancellation is imposed in the core as long as the dc currents in each zig-zag or center-tap winding are the same (ensured via control). It is sufficient to rate them for just the ac component and the multi-tasking

Table 3.2: Comparison of Multi-Frequency Bipolar MMC Structures

	M2DC (Figs. 3.3a)	Zigzag-MMC (Figs. 3.3b)	MF-Dual-MMC (Fig. 3.4)
No. of SMs	1 p.u.	1 p.u.	2 p.u.
Total SM power rating	1 p.u.	1 p.u.	2 p.u.
Power transmission capacity	1 p.u.	1 p.u.	2 p.u.
Ac grid voltage v_{ac}	1 p.u.	1 p.u.	2 p.u.
Galvanic separation	Partial*	Partial*	Partial*
Dc fault isolation	Yes**	Yes**	Yes**
Availability/Reliability	Lower	Lower	Higher
Magnetics power rating	Higher	Lower	Lower
Windings current	ac	ac+dc	ac+dc
Magnetics insulation requirement	Low	Low	Low
Magnetics design	Simple	Complex	Simple
Averaged semiconductor losses	1 p.u.	1 p.u.	1 p.u.
Magnetics losses	Higher	Lower	Lower

* Only between dc and ac grid; ** Requires sufficient FBSMs

transformer does not have to be rated to cope with any dc flux. Most importantly, the power ratings of the transformers used in Zigzag-MMC and MF-Dual-MMC are identical to the M2DC. Consequently, the total power rating of the magnetics (transformer and filter) as well as magnetic losses in the M2DC will be higher. It is worth mentioning that three-phase windings on the converter side of the bipolar F2F-MMC are subjected to large dc voltage stress with respect to the ground. The different dc potentials of transformer windings will lead to inter-winding dc voltage stress[2], which leads to higher insulation requirements [84]. On the contrary, there is no transformer inter-winding dc voltage stress on the converter side for the M2DC, Zigzag-MMC and MF-Dual-MMC.

On the other hand, the three phase legs in each MMC operating in a differential fashion will double the ac voltage across the transformer windings at the converter side relative to the case where a single phase leg is used. Consequently, the voltage of three-phase ac grid v_{ac} can be interconnected to the MF-Dual-MMC will be doubled compared with the M2DC and Zigzag-MMC. This gives freedom to design the transformer with a lower turns ratio.

[2]The bipolar F2F-MMC will have 320 kV inter-winding dc voltage stress for a ±320 kV bipolar dc system

3.3.3 Reliability

In HVDC applications, fault blocking is usually an important requirement to maintain high transmission security and reliability. In a meshed system, it is also important to disconnect the correct (i.e. faulted) line but keep the remaining system operational. Like conventional MMC, the MMC structures in Fig. 3.4 and the proposed MF-Dual-MMC can block faults at ac grid side using solely HBSMs. However, dc fault blocking requires each arm to have sufficient blocking capability in both forward and reverse directions. Replacing all or some of FBSMs with submodules capable of dc-fault blocking ability (hybrid-submodule) such as FBSMs can be the most practical and feasible solution to enable MMC capable of dc-fault blocking ability [50, 51, 83, 92]. This dc fault blocking method is general and can be applied to the MMC structures discussed in this chapter. The fault blocking capability of the multi-frequency MMC structure for three-port application will be validated in Section 4.5.

In utility applications, the availability of power converters is of great importance. Parallel-connected MMC in the MF-Dual-MMC allow each MMC to process up to 0.5 p.u. ac power independently, which will be demonstrated later in Section 3.6.4. If one MMC fails, the other MMC can continue operation for single frequency ac power transfer with a reduced output power. This will significantly enhance the system reliability and reduce the repair and replacement cost of each failure [95]. In addition, MMC with large current operation capability can provide support for the stable operation of power system due to its potential to participate in fault suppression and recovery instead of locking during the fault [96].

3.4 Converter Analysis and Unified Dynamic Controls

The proposed bipolar dual MMC structure where both ac and dc currents are simultaneously injected at the MMC midpoint node can be viewed as an elementary dc-dc-ac structure shown in Fig. 3.8. In the next chapter, new MMC application will be derived based on this elementary dc-dc-ac MMC structure. Therefore, a common modeling and control strategy for the dual MMC chain-link elementary structure is studied in this section to gain an understanding of the operation and control requirements for different MMC applications. Terminals d1, d2 and d3 are the connection of the elementary dc-dc-ac structure to the external dc networks.

Since the three-winding transformer has a turns ratio of 2:n:n, the voltages at the MMC midpoint nodes $\mathbf{v}_{abc,1}$, $\mathbf{v}_{abc,2}$ and the grid side winding voltage $\mathbf{v}_{abc,g}$ are related

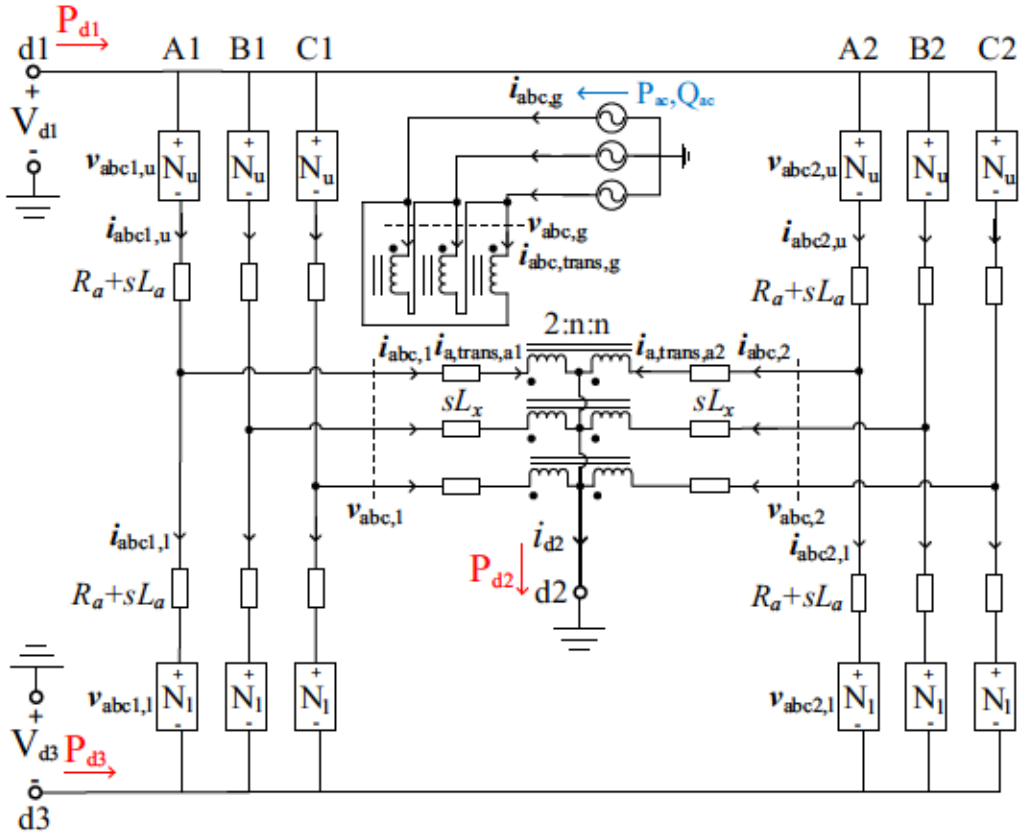

Figure 3.8: Elementary multi-frequency dc-dc-ac MMC structure circuit schematic with notation

by

$$\mathbf{v}_{abc,1} = -\mathbf{v}_{abc,2} = \frac{n}{2} \cdot \mathbf{v}_{abc,g}, \tag{3.3}$$

where bold quantities represent vectorized ac rms phasors. The ac components in $\mathbf{i}_{abc,1}$ and $\mathbf{i}_{abc,2}$ contribute to the ac power transfer on the grid side and are independent of each other, while the dc components in $\mathbf{i}_{abc,1}$ and $\mathbf{i}_{abc,2}$ are used for the dc power transfer through the center-tap connection. It is thus more convenient to express all voltages and currents in the $\alpha\beta 0$ stationary reference frame. The voltages in the stationary reference frame are given by

$$\mathbf{v}_{\alpha\beta,1} = -\mathbf{v}_{\alpha\beta,2} = \frac{n}{2} \cdot \mathbf{v}_{\alpha\beta,g} \tag{3.4}$$

$$v_{0,1} = v_{0,2} = v_{0,g} = 0 \tag{3.5}$$

3.4.1 Converter Power Transfer Mechanisms

Figs. 3.9 and 3.10 show the current paths for two independent power transfer mechanisms in the proposed three-phase MMC topologies. Fig. 3.9 illustrates power transfer

between the ac grid and the sum of dc ports while Fig. 3.10 depicts the power transfer between dc ports. The arm quantities $\mathbf{x} \in \{\mathbf{v}, \mathbf{i}\}$ are broken into sum components (i.e. terms common to each arm) and difference components (i.e. terms differential to each arm), as commonly done in MMC analysis [57], defined here by

$$\begin{bmatrix} \mathbf{x}_{abc,\Sigma} \\ \mathbf{x}_{abc,\Delta} \end{bmatrix} = \begin{bmatrix} 0.5 & 0.5 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} \mathbf{x}_{abc,u} \\ \mathbf{x}_{abc,l} \end{bmatrix}. \tag{3.6}$$

The two center-tapped windings on the converter side can be considered to be two independent wye windings with their star points connected together. This allows the two converter currents $\mathbf{i}_{abc,1}$ and $\mathbf{i}_{abc,2}$ to be controlled independently of each other. However, the dc components of $\mathbf{i}_{abc,1}$ and $\mathbf{i}_{abc,2}$ ($i_{0,\Delta 1}$ and $i_{0,\Delta 2}$, respectively) must be regulated to be the same using current control to ensure dc flux cancellation in the magnetic core. Only one phase leg is shown within each MMC in Figs. 3.9 and 3.10 for simplicity. The $\alpha\beta$ currents are indicated by the solid blue lines and zero sequence (dc) currents are indicated by red lines, with the resulting average powers being absorbed by each arm represented by the coloured arrows. The converter differential currents and grid side winding current are related by

$$n \cdot (\mathbf{i}_{\alpha\beta,\Delta 1} - \mathbf{i}_{\alpha\beta,\Delta 2}) = -\mathbf{i}_{\alpha\beta,g} \tag{3.7}$$

$$i_{0,g} = 0 \tag{3.8}$$

$$i_{0,\Delta 1} = i_{0,\Delta 2} = \frac{i_{d2}}{6} \tag{3.9}$$

where $i_{d2} = i_{dc,p} - i_{dc,n}$ for the bipolar MMC in Fig. 3.5.

Power transfer between ac grid and sum of dc ports

Fig. 3.9 shows the current paths for power transfer between ac grid and sum of dc ports. $\mathbf{i}_{\alpha\beta,\Delta 1}$ and $\mathbf{i}_{\alpha\beta,\Delta 2}$ in Fig. 3.9 have the same magnitude but opposite direction to distribute the ac load equally between the two MMCs. However, the two currents can be regulated unequally to distribute different amount of ac power to the grid if required. The grid side winding current consists of only the $\alpha\beta$ components and so $i_{0,g} = 0$. Thus, the power supplied by the grid is proportional to $\mathbf{i}_{\alpha\beta,\Delta 1} - \mathbf{i}_{\alpha\beta,\Delta 2}$

$$P_{ac} = \frac{3n}{2} Re\{\mathbf{v}_{\alpha\beta,g} \cdot (\mathbf{i}_{\alpha\beta,\Delta 1} - \mathbf{i}_{\alpha\beta,\Delta 2})^*\} \tag{3.10}$$

$$Q_{ac} = \frac{3n}{2} Im\{\mathbf{v}_{\alpha\beta,g} \cdot (\mathbf{i}_{\alpha\beta,\Delta 1} - \mathbf{i}_{\alpha\beta,\Delta 2})^*\}. \tag{3.11}$$

The three-phase power P_{ac} supplied by the grid will drive the zero sequence currents $i_{0,\Sigma 1}$ and $i_{0,\Sigma 2}$ in the two MMCs. It will transfer power between the dc ports and the

grid. The dc power absorbed by the arms in MMC1, $P_{\Sigma 1}$, is given by (3.12), and it is identical for MMC2 (given that same amount of ac power is distributed equally between the two MMCs)

$$P_{\Sigma 1} = -3i_{0,\Sigma 1} \cdot (V_{d1} + V_{d3}) = P_{\Sigma 2} = -3i_{0,\Sigma 2} \cdot (V_{d1} + V_{d3}). \tag{3.12}$$

where $V_{d1} = V_{dc,p}$ and $V_{d3} = V_{dc,n}$ for the bipolar MMC in Fig. 3.5. To ensure steady-state SM capacitor power balance, criteria in (3.13) must be fulfilled .

$$P_{\Sigma 1} = P_{\Sigma 2} = -\frac{P_{ac}}{2} \tag{3.13}$$

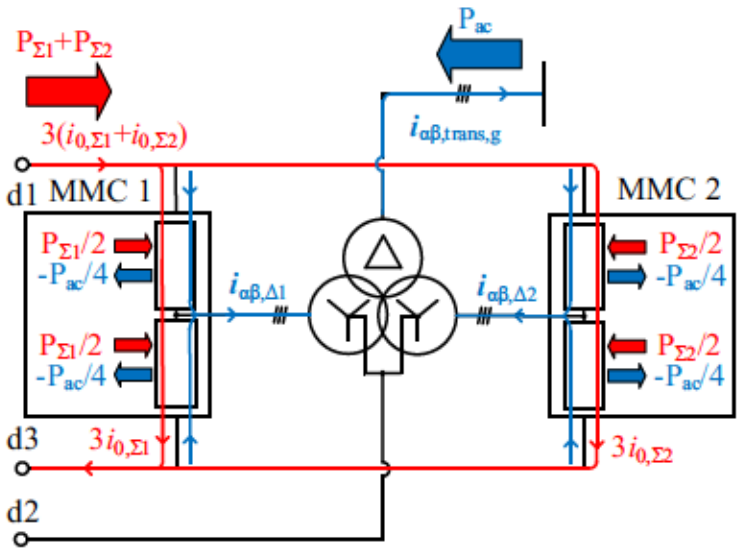

Figure 3.9: Power transfer mechanisms with solid blue lines (and red lines) denoting $\alpha\beta$ (and zero sequence) quantities between ac grid and sum of dc ports

Power transfer between dc ports

Fig. 3.10 shows the current paths for power transfer between the dc ports. The zero sequence currents of the two MMCs (3.9) through d2 split equally between the midpoint of the two MMCs to ensure dc flux cancellation in the core. The zero sequence currents of the two MMCs contribute to the dc power transfer from dc port d1 to d2 and from d3 to d2. The three dc ports are connected in different ways to the external dc networks for different MMC applications. The dc power transferred to d2 port is

$$P_{d2} = P_{d1} + P_{d3} = \frac{3}{2}(i_{0,\Delta 1} + i_{0,\Delta 2}) \cdot V_{d1} + \frac{3}{2}(i_{0,\Delta 1} + i_{0,\Delta 2}) \cdot V_{d3} \tag{3.14}$$

For the proposed bipolar MMC in Fig. 3.5 , the dc power transferred to d2 port is the difference in steady-state power exchange between positive and negative dc poles

$$P_{d2} = P_{dc,p} - P_{dc,n} \tag{3.15}$$

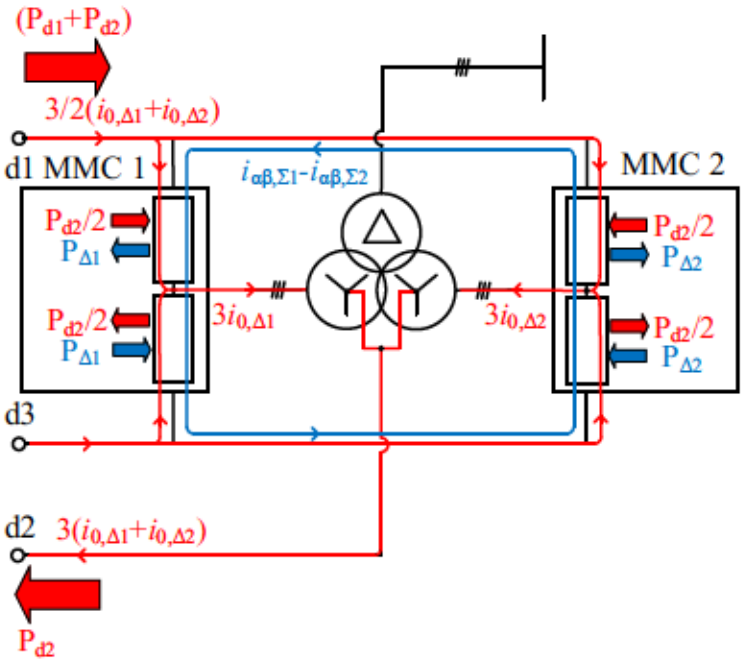

Figure 3.10: Power transfer mechanisms with solid blue lines (and red lines) denoting $\alpha\beta$ (and zero sequence) quantities between dc ports

The dc power transfer to the d2 port will cause dc power imbalance between the upper and lower arms of the MMCs (ref. the small red arrows in Fig. 3.10). This ultimately causes a deviation in arm capacitor voltages from their nominal values. The fundamental frequency component of $\mathbf{i}_{\alpha\beta,\Sigma1}$ and $\mathbf{i}_{\alpha\beta,\Sigma2}$ can be regulated to counteract this power imbalance and, thus, ensure balanced capacitor voltages. The current paths for $\mathbf{i}_{\alpha\beta,\Sigma1}$ and $\mathbf{i}_{\alpha\beta,\Sigma2}$ are indicated by the blue lines in Fig. 3.10. They have the same magnitude but opposite direction. The power transferred from upper arm to the lower arm due to $\mathbf{i}_{\alpha\beta,\Sigma1} - \mathbf{i}_{\alpha\beta,\Sigma2}$ are indicated by small blue arrows. To ensure steady-state SM capacitor power balance, the criteria in (3.16) must be fulfilled

$$P_{\Delta1} = P_{\Delta2} = \frac{P_{d2}}{2}, \tag{3.16}$$

where $P_{\Delta1} = P_{\Delta2} = (P_{dc,p} - P_{dc,n})/2$ for bipolar MMC in Fig. 3.5. The active and reactive power transferred from upper arm to lower arm in MMC1 and MMC2 are given by (3.17)-(3.20)

$$P_{\Delta1} = -\frac{3}{2} Re\{\mathbf{v}_{\alpha\beta,\Delta1} \cdot \mathbf{i}^*_{\alpha\beta,\Sigma1}\} \tag{3.17}$$

$$Q_{\Delta 1} = -\frac{3}{2} Im\{\mathbf{v}_{\alpha\beta,\Delta 1} \cdot \mathbf{i}^*_{\alpha\beta,\Sigma 1}\} \tag{3.18}$$

$$P_{\Delta 2} = -\frac{3}{2} Re\{\mathbf{v}_{\alpha\beta,\Delta 2} \cdot \mathbf{i}^*_{\alpha\beta,\Sigma 2}\} \tag{3.19}$$

$$Q_{\Delta 2} = -\frac{3}{2} Im\{\mathbf{v}_{\alpha\beta,\Delta 2} \cdot \mathbf{i}^*_{\alpha\beta,\Sigma 2}\}. \tag{3.20}$$

Note that $\mathbf{v}_{\alpha\beta,\Delta 1}$, $\mathbf{v}_{\alpha\beta,\Delta 2}$ are the synthesized differential arm voltages (not to be confused with grid voltage $\mathbf{v}_{\alpha\beta,g}$).

3.4.2 Proposed Unified Dynamic Controller

Expressing the converter voltages and currents in the $\alpha\beta$ stationary reference frame is advantageous for control as i) the resulting dynamics are ideally decoupled, and ii) each control variable has only one frequency component, which corresponds to a distinct converter power transfer mechanism. The objectives of the control system are summarized in Table 3.3, based on the power transfer mechanisms described in Section 3.4.1. The active/reactive power injections at the ac port are set by regulating the fundamental frequency component of $\mathbf{i}_{\alpha\beta,\Delta 1} - \mathbf{i}_{\alpha\beta,\Delta 2}$. The average power transferred to dc port d2 is achieved by regulating the dc component of $i_{0,\Delta 1} + i_{0,\Delta 2}$. For SM capacitor voltage regulation, the total sum and difference of the individual capacitors within the upper and lower arms are firstly defined for each MMC as

$$\Sigma V_c = 3\Big(\sum_{j=1}^{N_u} V_{c,j} + \sum_{j=1}^{n_l} V_{c,j}\Big) \tag{3.21}$$

$$\Delta V_c = 3\Big(\sum_{j=1}^{N_u} V_{c,j} - \sum_{j=1}^{n_l} V_{c,j}\Big). \tag{3.22}$$

The average value of ΣV_c (and ΔV_c) is regulated by controlling the dc components of $i_{0,\Sigma 1}$ and $i_{0,\Sigma 2}$ (and fundamental frequency components of $\mathbf{i}_{\alpha\beta,\Sigma 1}$ and $\mathbf{i}_{\alpha\beta,\Sigma 2}$).

The proposed unified dynamic control scheme achieving the aforementioned control objectives for MMC applications is given in Fig. 3.12. There is one outer power control loop, two outer capacitor voltage regulation loops and two inner current control loops. Only the inner current controllers for MMC1 are shown as MMC2 employs identical controls.

Port power flow controls

The outer power control loop and inner MMC current control loops allow independent control of power transfer between any combination of the dc and ac ports. PI

Table 3.3: Control Objectives for Converter Currents in Figs. 3.9 and 3.10

Current	Frequency Component	Control objective
$\mathbf{i}_{\alpha\beta,\Delta 1} - \mathbf{i}_{\alpha\beta,\Delta 2}$	fundamental ac	P_{ac}, Q_{ac} regulation
$i_{0,\Delta 1} + i_{0,\Delta 2}$	dc	P_{d2} regulation
$i_{0,\Sigma 1}$, $i_{0,\Sigma 2}$	dc	ΣV_c regulation
$\mathbf{i}_{\alpha\beta,\Sigma 1}$, $\mathbf{i}_{\alpha\beta,\Sigma 2}$	fundamental ac	ΔV_c regulation

compensators are used to obtain the $\mathbf{i}_{\alpha\beta,\Delta 1} - \mathbf{i}_{\alpha\beta,\Delta 2}$ needed to achieve P_{ac}^{ref} and Q_{ac}^{ref}. The ac current references are determined by relations (3.10) and (3.11). The dc reference of the proposed bipolar MMC for $i_{0,\Delta 1}^{ref} + i_{0,\Delta 2}^{ref}$ is set by the desired value for $P_{dc,p}^{ref} - P_{dc,n}^{ref}$ through respective relations (3.14) and (3.15).

The inner current control loops use PR compensators to ensure steady-state tracking of fundamental frequency control variables in addition to second order harmonic suppression. The reference fundamental frequency current $\mathbf{i}_{\alpha\beta,\Delta 1}^{ref} - \mathbf{i}_{\alpha\beta,\Delta 2}^{ref}$ produced by the outer power loop is split equally and sent to the PR compensators for MMC1 and MMC2. The polarity of MMC2 current reference is reversed due to (3.4). The relationship between modulation index $\mathbf{m}_{\alpha\beta,\Delta 1}$ and current $\mathbf{i}_{\alpha\beta,\Delta 1}$ is given by (3.23) and is identical for MMC2

$$(L_a + 2L_x)\frac{d\mathbf{i}_{\alpha\beta,\Delta 1}}{dt} = -R_a\mathbf{i}_{\alpha\beta,\Delta 1} - 2(V_{d1} + V_{d3}) \cdot \mathbf{m}_{\alpha\beta,\Delta 1} - n\mathbf{v}_{\alpha\beta,g} \tag{3.23}$$

The inner current control loops also use PI compensators to track the dc control variables. The reference dc value of $i_{0,\Delta 1}^{ref}$ for MMC1 is set to be half of $i_{0,\Delta 1}^{ref} + i_{0,\Delta 2}^{ref}$ demand. The same applies to $i_{0,\Delta 2}^{ref}$ for MMC2. This ensures equal sharing of the total dc power transfer between MMCs. This is important as the dc values of $i_{0,\Delta 1}$ and $i_{0,\Delta 2}$ should always be identical to ensure core dc flux cancellation. The relationship between modulation index $m_{0,\Delta 1}$ and current $i_{0,\Delta 1}$ is given by (3.24) and is identical for MMC2

$$(L_a + 2L_x)\frac{di_{0,\Delta 1}}{dt} = -R_a i_{0,\Delta 1} - 2(V_{d1} + V_{d3}) \cdot m_{0,\Delta 1} \tag{3.24}$$

The unified dynamic controller structure in Fig. 3.12 can be readily adapted for the proposed bipolar MMC in Fig. 3.5 by assigning appropriate reference signals, as shown in Fig. 3.11. The control schemes including outer capacitor voltage regulation loops and inner current control loops are identical for the proposed bipolar MMC.

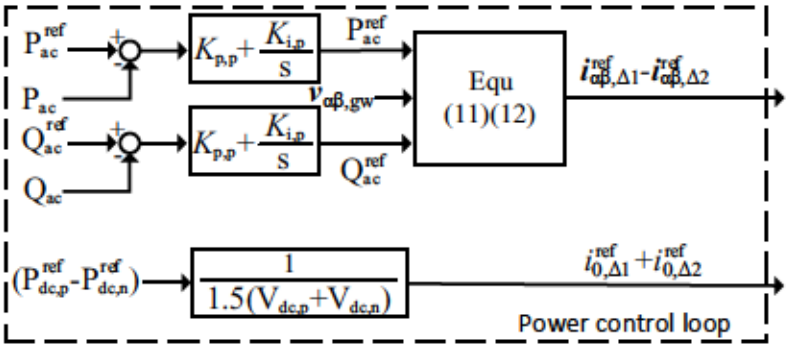

Figure 3.11: Outer power control loop of Fig. 3.12 for the proposed bipolar MMC in Fig. 3.5

Capacitor voltage balancing controls

Voltage balancing of the SM capacitors should be satisfied during both steady-state and transients. This is achieved by setting $\Sigma V_c^{ref} = 3(N_u + N_l)V_c^{ref}$ and $\Delta V_c^{ref} = 3(N_u - N_l)V_c^{ref}$ in the capacitor voltage balancing loop for both MMCs, where V_c^{ref} is the nominal SM capacitor voltage.

PI compensators are utilized to ensure steady-state tracking of dc control variables for ΣV_c control. The output from ΣV_c control loops, $i_{0,\Sigma1}^{ref}$ and $i_{0,\Sigma2}^{ref}$, are fed as reference to the PI compensators for MMC1 and MMC2, respectively. The relationship between modulation index $m_{0,\Sigma1}$ and current $i_{0,\Sigma1}$ is given by (3.25) and is identical for MMC2

$$2L_a\frac{di_{0,\Sigma1}}{dt} = -2R_a i_{0,\Sigma1} - 2(V_{d1}+V_{d3})\cdot m_{0,\Sigma1} + (V_{d1}+V_{d3}). \tag{3.25}$$

PR compensators are used to provide steady-state tracking of fundamental frequency control variables for ΔV_c control. The references for $\mathbf{i}_{\alpha\beta,\Sigma1}^{ref}$ and $\mathbf{i}_{\alpha\beta,\Sigma2}^{ref}$ are calculated by solving (3.17)-(3.20) based on the required $P_{\alpha\beta,\Sigma1}^{ref}$, $P_{\alpha\beta,\Sigma2}^{ref}$, respectively. The second order harmonic currents in $\mathbf{i}_{\alpha\beta,\Sigma1}$ and $\mathbf{i}_{\alpha\beta,\Sigma2}$ are suppressed by adding an extra term in the PR compensators. $Q_{\alpha\beta,\Sigma1}^{ref}$ and $Q_{\alpha\beta,\Sigma2}^{ref}$ are set to zero to ensure no reactive power is unnecessarily circulated between arms, thereby minimizing the ac currents and hence maximizing power transfer capacity and efficiency. The relationship between modulation index $\mathbf{m}_{\alpha\beta,\Sigma1}$ and current $\mathbf{i}_{\alpha\beta,\Sigma1}$ is given by (3.26) and is identical for MMC2

$$L_a\frac{d\mathbf{i}_{\alpha\beta,\Sigma1}}{dt} = -R_a\mathbf{i}_{\alpha\beta,\Sigma1} - (V_{d1}+V_{d3})\cdot\mathbf{m}_{\alpha\beta,\Sigma1}. \tag{3.26}$$

Control variables $\mathbf{m}_{abc,\Sigma}$, $\mathbf{m}_{abc,\Delta}$ are related to arm modulating signals $\mathbf{m}_{abc,u}$, $\mathbf{m}_{abc,l}$

by

$$\begin{bmatrix} \mathbf{m}_{abc,u} \\ \mathbf{m}_{abc,l} \end{bmatrix} = \begin{bmatrix} 1 & 0.5 \\ 1 & -0.5 \end{bmatrix} \begin{bmatrix} \mathbf{m}_{abc,\Sigma} \\ \mathbf{m}_{abc,\Delta} \end{bmatrix}. \tag{3.27}$$

The form of the PI and PR compensators used in this work are given by

$$G_{PI}(s) = K_p + \frac{K_i}{s} \tag{3.28}$$

$$G_{PR}(s) = K_p + \frac{K_{r1}s}{s^2 + \omega_1^2} + \frac{K_{r2}s}{s^2 + \omega_2^2}. \tag{3.29}$$

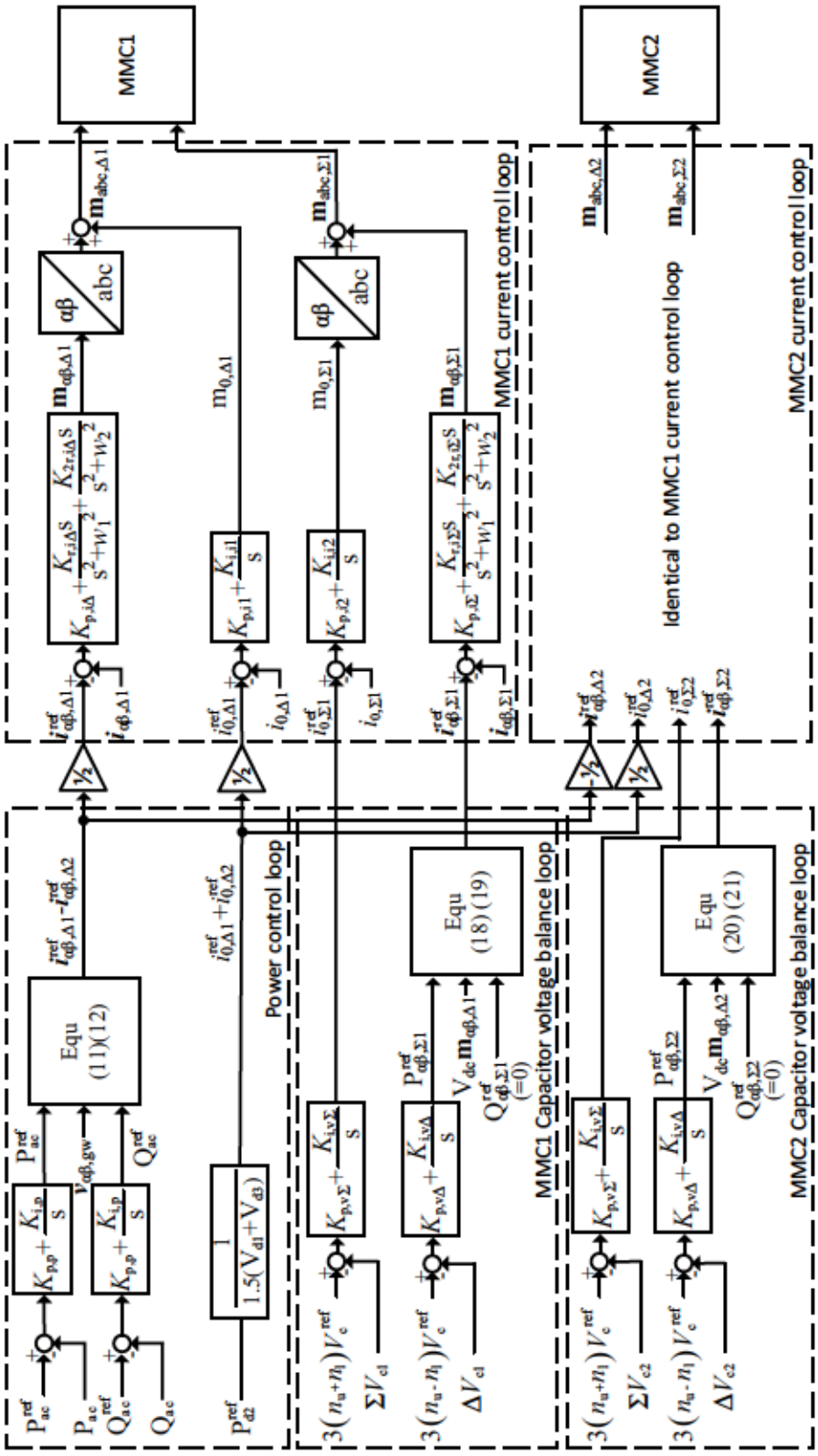

Figure 3.12: Unified dynamic control scheme for the elementary multi-frequency dc-dc-ac MMC chain-link structure of Fig. 3.8

3.5 Simulation Results

The operating principle and proposed dynamic controls for the bipolar MMC in Fig. 3.5 are verified by PSCAD/EMTDC simulations. Simulations are conducted using a detailed equivalent switching model. Voltage balancing of capacitors within each arm is achieved using the sort and selection method. Simulation parameters are given in Table 3.4. The parameters for the controllers are selected to give settling times of around 150 msec for ac and dc power demands and within 100 msec for the capacitor voltages ΣV_c and ΔV_c. The submodule capacitor voltage (V_c^{ref}) is rated at 2 kV with half-bridge configuration. The arm reactor has a value of around 10% on

Table 3.4: Simulation Parameters for Bipolar Dual MMC in Fig. 3.5

Converter Parameters	±20kV bipolar MMC	±200kV bipolar MMC
Rated power	72 MW	1200 MW
$V_{dc,p}/V_{dc,n}$	20 kV	200 kV
Number of SMs per arm, N_u, N_l	20 (HBSM)	200 (HBSM)
SM capacitor voltage, V_c^{ref}	2 kV	2 kV
SM capacitance, C_{sm}	5 mF	7 mF
Arm inductance, L_a	5 mH	40 mH
Fundamental frequency, f	60 Hz	60 Hz
Transformer parameters	Value	
Power rating, S_w	72 MVA	1200 MVA
Turns ratio, n	0.738	
Primary winding voltages, V_p	34.5 kV_{rms}	345 kV_{rms}
Secondary winding voltages, V_s	12.73 kV_{rms}	127.3 kV_{rms}
Leakage reactance	10%	
Magnetizing current	1%	
Controller parameters	Value	
$K_{p,p}$, $K_{i,p}$	0.01, 14.3	0.00015, 0.21
$K_{p,v\Sigma}$, $K_{i,v\Sigma}$	$1.6e^{-4}$, $1.3e^{-3}$	$5.5e^{-4}$, $4e^{-3}$
$K_{p,v\Delta}$, $K_{i,v\Delta}$	0.2, 0.5	0.02, 2
$K_{p,i\Sigma}$, $K_{r,i\Sigma}$, $K_{2r,i\Sigma}$	0.5, 1.5, 100	1, 3, 200
$K_{p,i\Delta}$, $K_{r,i\Delta}$, $K_{2r,i\Delta}$	0.5, 40, 10	2, 50, 90
$K_{p,i1}$, $K_{i,i1}$	$3e^{-4}$, $8.3e^{-3}$	$1.6e^{-5}$, $7.7e^{-5}$
$K_{p,i2}$, $K_{i,i2}$	0.02, 0.2	0.01, 0.4
ΣV_c^{ref}, ΔV_c^{ref}	240 kV, 0 kV	2400 kV, 0 kV
ω_1, ω_2	377 rad/s, 754 rad/s	

the system impedance base so that the voltage required to control output current is less than 10%. Note that the arm chokes in s arms are identical to that in p arms

even that the current distribution in each arm are not the same for all power flow scenarios. The SM capacitances are picked to yield peak-to-peak capacitor voltage ripples of around 18% for the upper and lower arms. The well known SM capacitor voltage sort and selection algorithm ensures voltage balancing amongst individual capacitors within each arm. The fundamental frequency is 60 Hz. The bipolar MMC in Fig. 3.5 is designed to interface a bipolar ±20kV MVDC system with a 34.5 kV MVAC system and a bipolar ±200kV HVDC system with a 345 kV HVAC system, where each pole can operate independently at a power rating of 36 MW and 600 MW, respectively.

3.5.1 Three-winding Transformer Design

The following discussion highlights key transformer design considerations for the simulated case studies of a bipolar ±20kV MVDC system with a 34.5 kV MVAC system. Similar design principles would apply for the bipolar ±200kV HVDC system with a 345 kV HVAC system.

Each arm in Fig. 3.5 must support dc voltages of 10 kV for bipolar ±20kV MVDC system. Considering also the SM capacitor voltage rating is 2 kV and that half-bridge SMs are used to maximized the synthesized ac arm voltages, the number of SMs in each arms is chosen to be 20. Thus, the voltages of the center-tapped winding at the converter side are rated for 12.73 kV_{rms} (assuming a modulation index of 0.9). The winding voltages at the grid side of the transformer are rated for 34.5 kV_{rms}. Consequently, the transformer turns ratio is approximately 0.738. The secondary center-tapped windings need to carry multi-frequency current components, namely dc and fundamental ac frequency. The frequency analysis of center-tapped winding currents for exemplar power flow scenarios are shown in Table 3.5. The transformer center-tapped windings at the converter side need to carry at most 0.94 kA_{rms}, which is in Scenario A(0.5, 0.5, 0). This coincides with the analysis in Fig. 3.7. The resulting transformer power rating is approximately 72 MVA.

Table 3.5: Frequency Analysis of Center-Tapped Winding Currents for Bipolar ±20kV MVDC System

Scenario	DC current	60 Hz current	RMS
A(0.5, 0.5, 0)	0	1.33 kA_{pk}	0.94 kA_{rms}
C(0.5, 0, 0)	0.3 kA	0.67 kA_{pk}	0.56 kA_{rms}

Since the modeling and analysis in Section 3.4.2 assume the magnetizing current

is negligible, the magnetizing inductance of the transformer used for simulation case study is chosen to be very large to have less than 1% magnetizing current. The leakage reactance of the transformer is chosen to be 0.1 p.u. similar to the grid interfacing transformer in [97]. Together with the transformer leakage reactance, the total series reactance is in the range of 0.2 p.u. The transformer windings at the grid side are connected in delta to block the zero-sequence voltages generated by the converter.

3.5.2 ±20 kV Bipolar MVDC System

Fig. 3.13 shows the dynamic response waveforms considering three different combinations of port power flows scenarios for a 20 kV bipolar MMC with a 34.5 kV MVAC system: i) dc and ac port power injections, ii) dc port currents, iii) exemplar upper and lower arm currents in two MMCs, iv) exemplar SM capacitor voltages in two MMCs and v) transformer winding currents in phase a are plotted. The port power flow notation from Table 3.1 is used in describing the scenarios. Firstly, from $t = 0$ to $t = 0.1$ sec, the power transferred from the negative dc pole $P_{dc,n}$ is held at zero and only the positive dc pole consumes 36 MW active power. At the same time, the grid consumes 36 MVar reactive power. This is power flow scenario C(-0.5, 0, -0.5). Then, at $t = 0.1$ sec, 72 MW active power is injected from the grid and split equally between the positive and negative dc poles. This is power flow scenario A(-0.5, -0.5, 0). Then, starting at $t = 0.5$ sec, 36 MW active power is delivered from the positive dc pole only. This is power flow scenario C(0.5, 0, 0).

Figs. 3.14 and 3.15 show steady-state results considering power flow scenario A(-0.5, -0.5, 0) and C(0.5, 0, 0) in Fig. 3.13: i) dc port currents, ac grid voltage and current in phase a, ii) exemplar upper and lower arm currents in two MMCs, iii) exemplar SM capacitor voltages in two MMCs and iv) transformer winding currents in phase a are plotted. The upper and lower arm currents in MMC1 $i_{a1,u}$, $i_{a1,l}$ and in MMC3 $i_{a1,u}$, $i_{a1,u}$ have slightly difference (ref. Fig. 3.14) due to small number of SMs in each arm Nu, N_l.

The positive and negative dc pole currents $i_{dc,p}$ and $i_{dc,n}$ as shown in Fig. 3.13 are dominantly dc values as three-phase implementation provides fundamental ac and second harmonics current cancellation at the dc rails of the converter. $i_{dc,p}$ and $i_{dc,n}$ are not always identical, verifying independent operation of each dc pole.

The capacitor voltages $v_{c,a1,u}$, $v_{c,a1,l}$ (upper and lower arms of phase a in MMC1) and $v_{c,a2,u}$, $v_{c,a2,l}$ (upper and lower arms of phase a in MMC2) remain well regulated in the three power flow scenarios. The SM peak-to-peak capacitor voltage ripples is below 18% for the upper and lower arms in all three scenarios. Transformer core

dc flux cancellation is achieved owing to the center-tap windings arrangement. This can be seen with the transformer winding currents in phase a $i_{a,trans,a1}$, $i_{a,trans,a2}$, $i_{a,trans,g}$. The center-tapped winding carries both dc and ac currents in C(-0.5, 0, 0.5) and C(0.5, 0, 0), but sees only ac current in A(-0.5, -0.5, 0). However, the transformer winding current at the grid side $i_{a,trans,g}$ carry only ac current. The green and black curves are the measured instantaneous value and calculated rms value of the transformer's secondary center-tapped winding, respectively. The rms value of the winding current $i_{a,trans,a1(rms)}$ is the highest during rated pure dc-ac conversion (A(-0.5, -0.5, 0)), and decreases in all other power flow scenarios. This coincides with the analysis in Fig. 3.7. Thus, the transformer in the ±20 kV bipolar MMC is rated at 72 MVA to enable full independent bipole operation (each pole can process up to 36 MVA), which would be the same rating as a grid interfacing transformer for conventional dc-ac MMC.

3.5.3 ±200 kV Bipolar HVDC System

Fig. 3.16 shows the dynamic response waveforms considering three different combinations of port power flows scenarios for a 200 kV bipolar MMC with a 345 kV HVAC system, where each pole can operate independently at a power rating of 600 MW. The power transfer scenarios are reversed relative to Fig. 3.13. Firstly, from $t = 0$ to $t = 0.1$ sec, the power transferred from the negative dc pole $P_{dc,n}$ is held at zero and only the positive dc pole transfers 36 MW active power to the ac grid. At the same time, the grid consumes 36 MVar reactive power. This is power flow scenario C(0.5, 0, -0.5). Then, at $t = 0.1$ sec, 72 MW active power is consumed at the grid and split equally between the positive and negative dc poles. This is power flow scenario A(0.5, 0.5, 0). Then, starting at $t = 0.5$ sec, 36 MW active power is consumed at the positive dc pole only. This is power flow scenario C(-0.5, 0, 0).

Figs. 3.17 and 3.18 show steady-state results considering power flow scenario A(0.5, 0.5, 0) and C(-0.5, 0, 0) in Fig. 3.16: i) dc port currents, ac grid voltage and current in phase a, ii) exemplar upper and lower arm currents in two MMCs, iii) exemplar SM capacitor voltages in two MMCs and iv) transformer winding currents in phase a are plotted. Unlike in Fig. 3.13, the upper and lower arm currents in MMC1 $i_{a1,u}$, $i_{a1,l}$ and in MMC3 $i_{a1,u}$, $i_{a1,u}$ are identical (ref. Fig. 3.17). The transformer in the ±200 kV bipolar MMC is rated at 1200 MVA to enable full independent bipole operation (each pole can process up to 600 MVA), which would be the same rating as a grid interfacing transformer for conventional dc-ac MMC. This can be seen with the transformer winding currents in phase a. The rms value of the winding current

$i_{a,trans,a1(rms)}$ is the highest during rated pure dc-ac conversion ($A(0.5, 0.5, 0)$), and decreases in all other power flow scenarios.

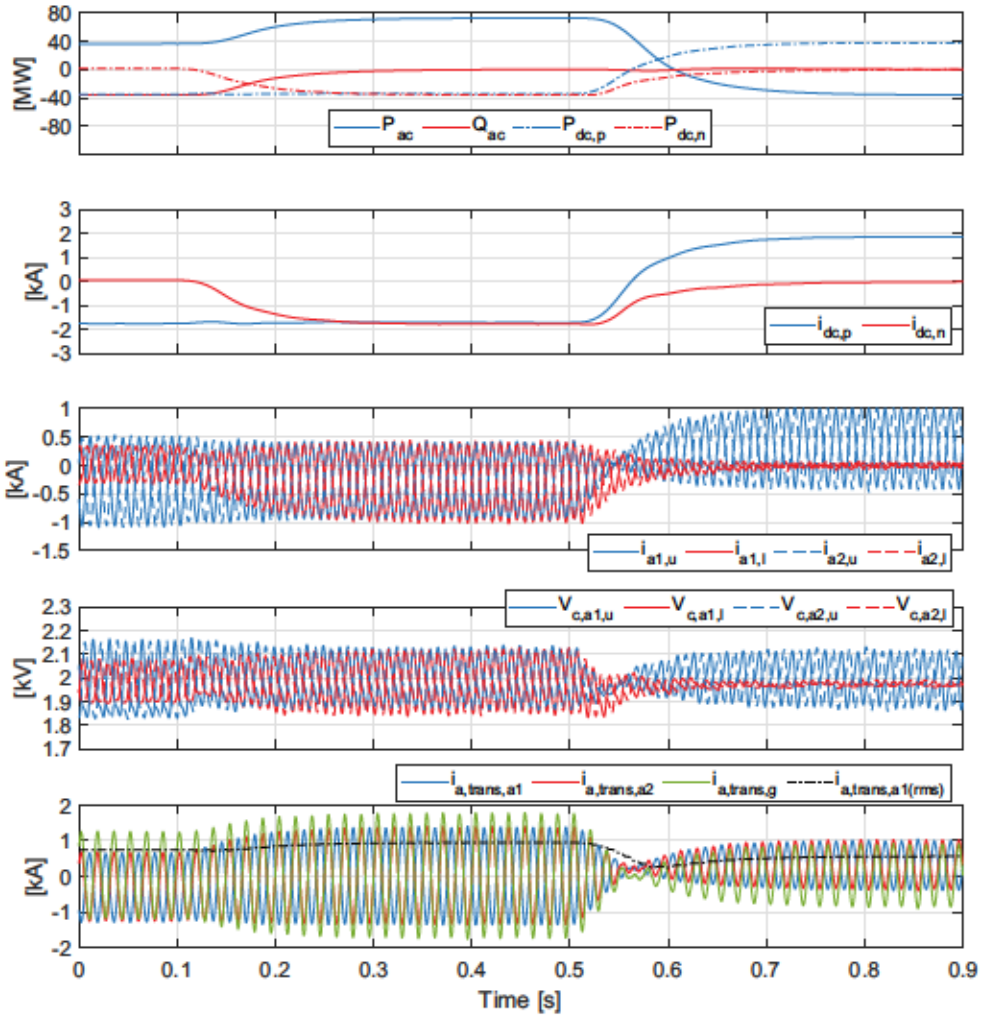

Figure 3.13: PSCAD waveforms of ±20 kV bipolar MMC are shown in subplots for (i) C(-0.5, 0, -0.5) from $t = 0$ to 0.1 sec; (ii) A(-0.5, -0.5, 0) from $t = 0.1$ to 0.5 sec; and (iii) C(0.5, 0, 0) from $t = 0.5$ to 0.9 sec

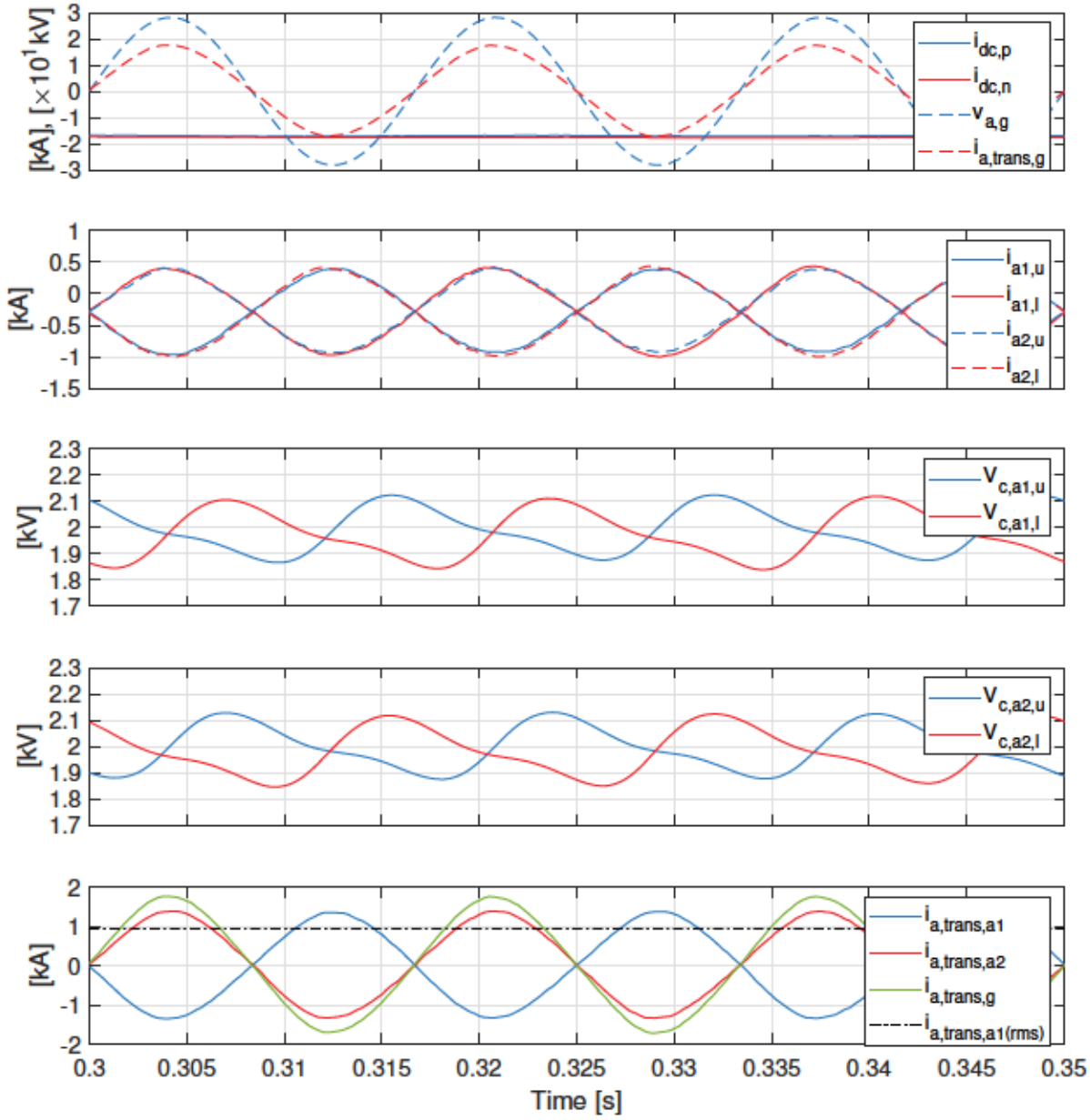

Figure 3.14: PSCAD steady-state waveforms of ±20 kV bipolar MMC are shown in subplots for A(-0.5, -0.5, 0)

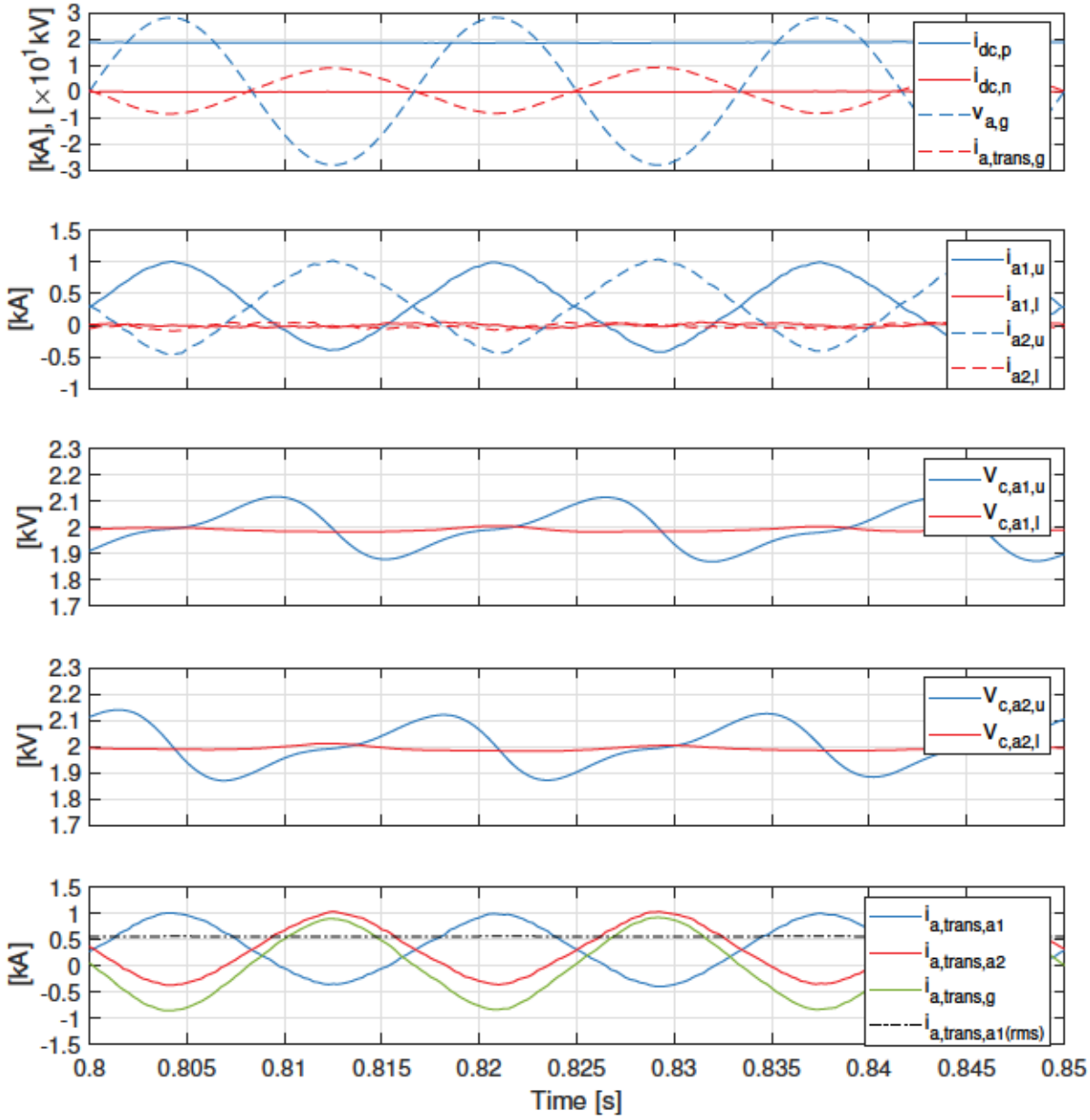

Figure 3.15: PSCAD steady-state waveforms of ±20 kV bipolar MMC are shown in subplots for $C(0.5, 0, 0)$

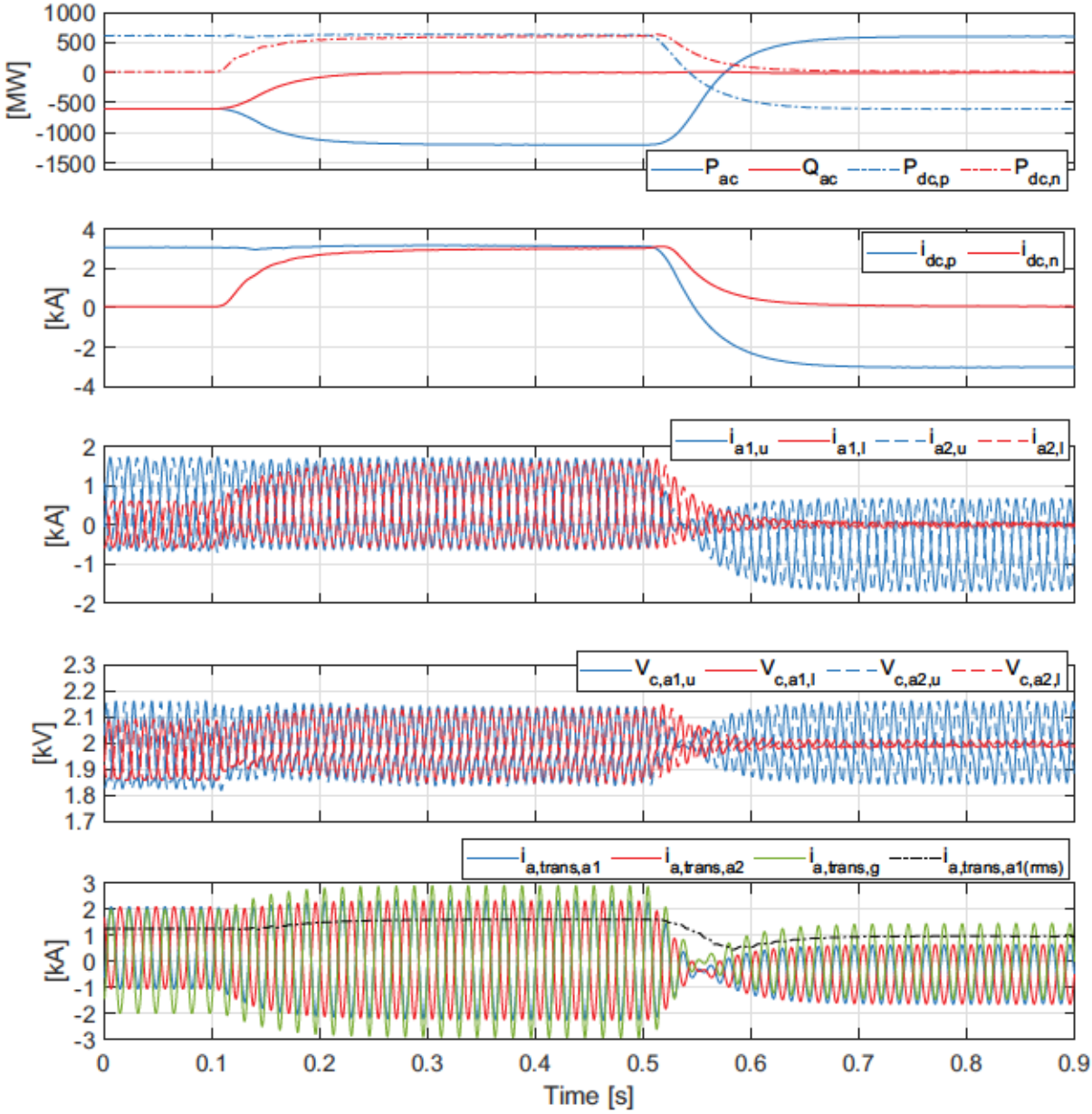

Figure 3.16: PSCAD waveforms of ±200 kV bipolar MMC are shown in subplots for (i) C(0.5, 0, -0.5) from $t = 0$ to 0.1 sec; (ii) A(0.5, 0.5, 0) from $t = 0.1$ to 0.5 sec; and (iii) C(-0.5, 0, 0) from $t = 0.5$ to 0.9 sec

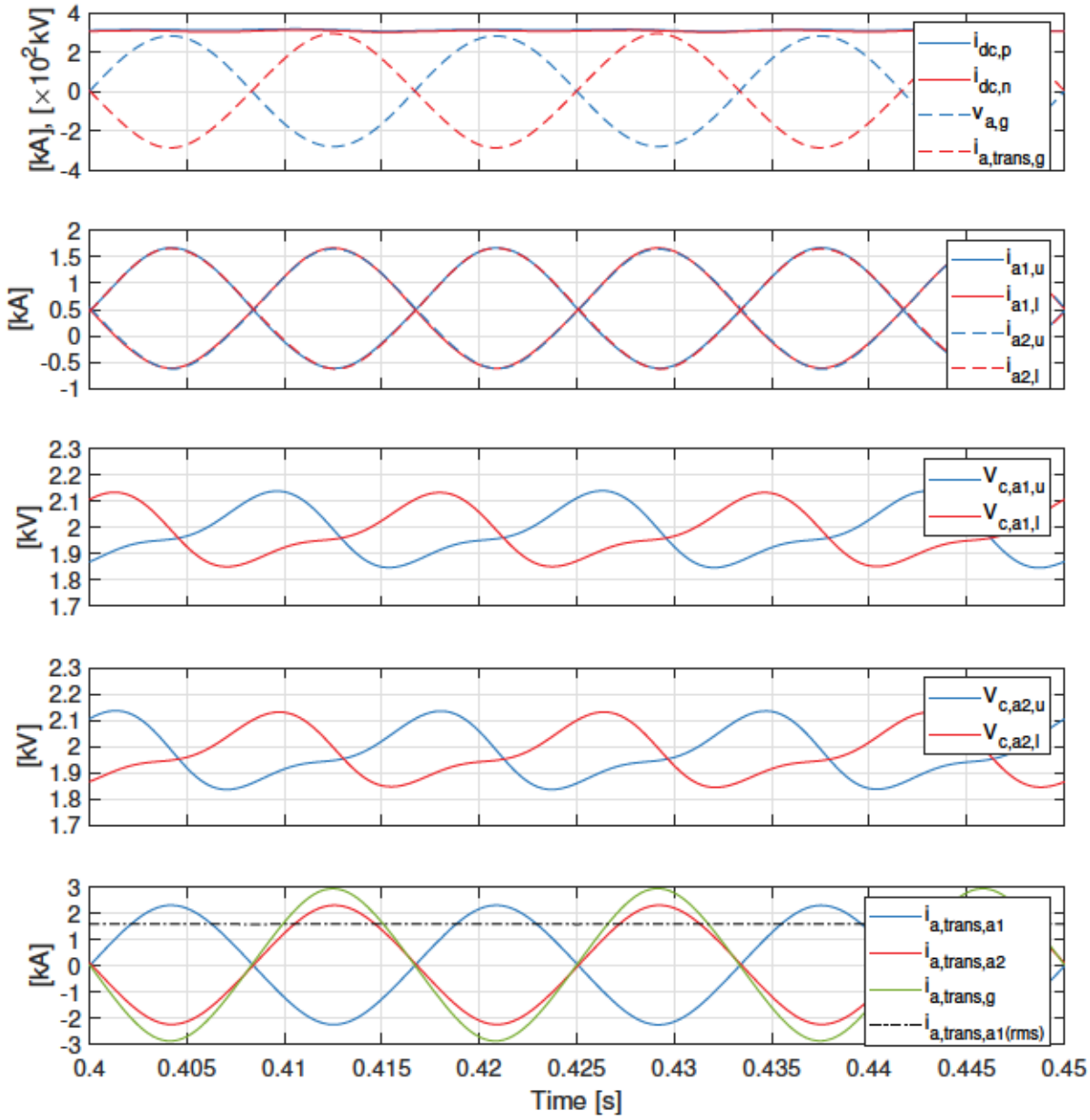

Figure 3.17: PSCAD steady-state waveforms of ±200 kV bipolar MMC are shown in subplots for $A(0.5, 0.5, 0)$

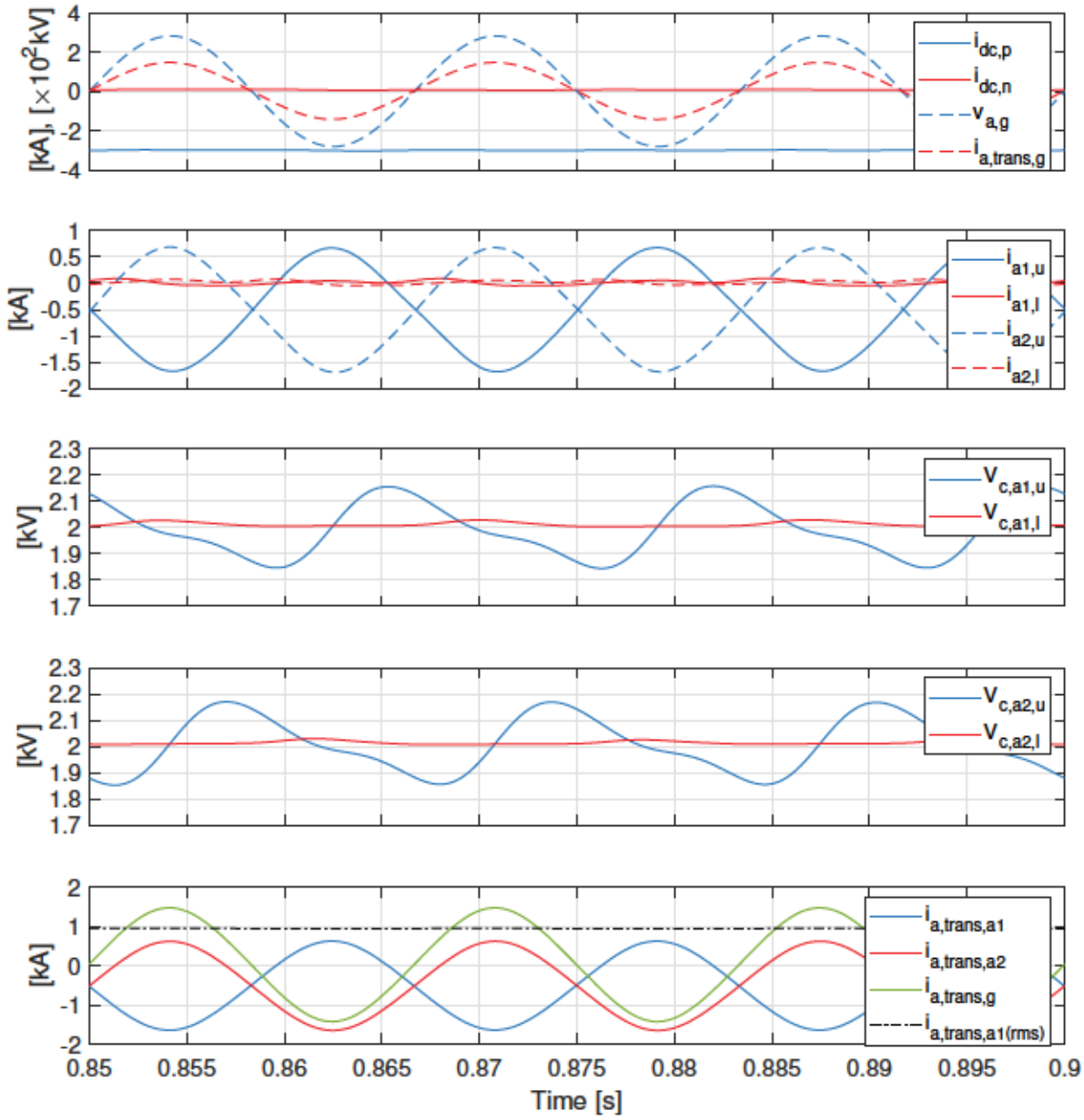

Figure 3.18: PSCAD steady-state waveforms of ±200 kV bipolar MMC are shown in subplots for C(-0.5, 0, 0)

3.6 Experimental Results

Experimental results are presented for a scaled-down ±85 V, 3.4 kW laboratory prototype of the bipolar dual MMC structure. The experimental setup allows bidirectional power flow on all ports. The operating principle and dynamic controls for the bipolar MMCs are validated. The experimental setup is shown in Fig. 3.19 and parameters are given in Table 3.6. The controls in Fig. 3.12 are implemented on a real-time controller platform from Imperix. Each arm uses two half-bridge SMs with $V_c^{ref} = 85$ V. The well known SM capacitor voltage sort and selection algorithm ensures voltage balancing amongst individual capacitors within each arm. The parameters for the controllers are selected to give settling times of around 150 msec for ac and dc power demands and within 200 msec for the capacitor voltages. Three single-phase 1.5 kVA center-tapped transformers with n = 1.026 (4.5 kVA for three-phase) are used. The maximum power rating of the dual MMC setup is 3.4 kW due to power supply limitation. The port power flow notation from Table 3.1 is used. Experimental waveforms are recorded using real-time control software with $f_{sample} = 25$ kHz.

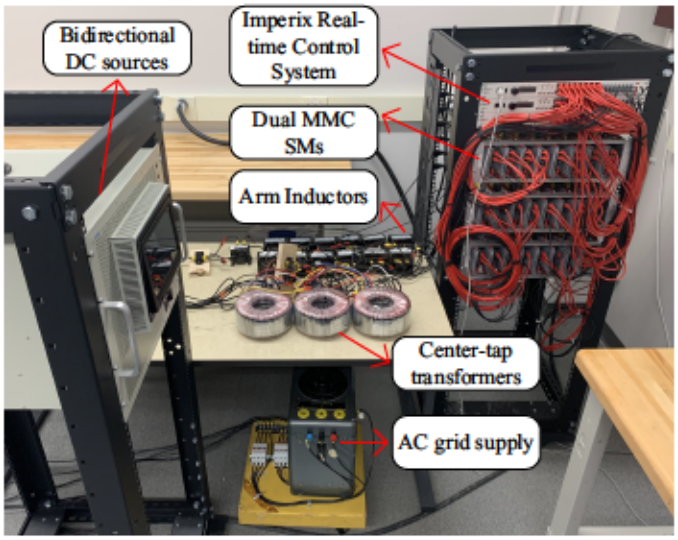

Figure 3.19: Experimental setup for the bipolar MMC topology in Fig. 3.5

Table 3.6: Experimental Parameters for Bipolar Dual MMC in Fig. 3.5

Converter Parameters	Value
Rated power	3.4 kW
$V_{dc,p}/V_{dc,n}$	85 V
Number of SMs per arm, N_u, N_l	2 (HBSM)
SM capacitor voltage, V_c^{ref}	85 V
SM capacitance, C_{sm}	5 mF
Arm inductance, L_a	2.5 mH
Fundamental frequency, f	60 Hz
Transformer parameters	**Value**
Transformer model	Hammond 1182T60P
Power rating, S_w	4.5 kVA
Turns ratio, n	1.026
Primary/Secondary winding voltages, V_p/V_s	117 V/ 60 V (rms)
Leakage inductance L_x	0.085 mH
Magnetizing inductance L_m	1.516 H
Controller parameters	**Value**
SPWM carrier frequency, f_{sw}	10 kHz
Sample frequency, f_{sample}	25 kHz
$K_{p,p}$, $K_{i,p}$	0.3, 20
$K_{p,v\Sigma}$, $K_{i,v\Sigma}$	0.001, 0.01
$K_{p,v\Delta}$, $K_{i,v\Delta}$	0.1, 2
$K_{p,i\Sigma}$, $K_{r,i\Sigma}$, $K_{2r,i\Sigma}$	0.1, 0.5, 5
$K_{p,i\Delta}$, $K_{r,i\Delta}$, $K_{2r,i\Delta}$	0.2, 0.5, 5
$K_{p,i1}$, $K_{i,i1}$	0.003, 0.08
$K_{p,i2}$, $K_{i,i2}$	0.003, 0.02
ΣV_{cap}^{ref} , ΔV_{cap}^{ref}	1020 V, 0 V
ω_1, ω_2	377 rad/s, 754 rad/s

3.6.1 Practical Considerations

Due to practical aspects, the ac grid supply of experimental setup in Fig. 3.19 is not pure 60 Hz power supply. The exemplar ac grid voltage in phase a $v_{a,g}$ contains 300 Hz component as shown in Fig. 3.20. These scenarios do not occur in the simulation where ideal conditions are imposed. As an example, the impact of grid voltage $\mathbf{v}_{abc,g}$ with 300 Hz harmonic component on MMC arm currents $i_{a1,u}$, $i_{a1,l}$, $i_{a2,u}$, $i_{a2,l}$ is illustrated in Fig. 3.20. In scenario A(-0.5, -0.5, 0), each dc pole consumes 1.7 kW from the ac grid, i.e. $P_{dc,p} = P_{dc,n} = -1.7$ kW, and thus $P_{ac} = 3.4$ kW.

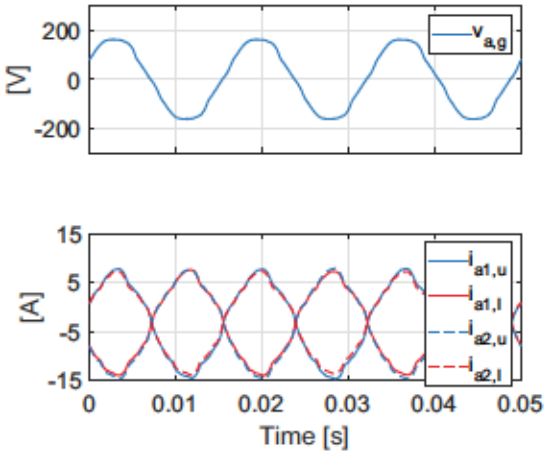

Figure 3.20: Experimental waveforms of ac grid voltage in phase a; experimental MMC arm ac currents for steady-state power flow scenarios: A(-0.5, -0.5, 0), where 300 Hz voltage ripples exist in $\mathbf{v}_{abc,g}$

To eliminate the 300 Hz ripple in MMC arm currents, such as that shown in Fig. 3.20, a 60 Hz band-pass filter for all corresponding controller ($\mathbf{v}_{abc,g}$) is added. This strategy is implemented for all experimental scenarios. The efficacy of band-pass filter is demonstrated in Fig. 3.21.

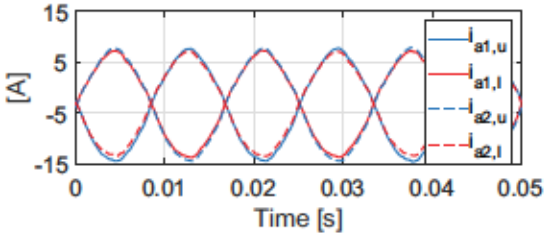

Figure 3.21: MMC arm ac currents with 60 Hz band-pass filter for steady-state power flow scenarios: A(-0.5, -0.5, 0)

3.6.2 Steady-State Performance

Six power flow scenarios as shown in Fig. 3.22 are used to demonstrate the capabilities of the proposed bipolar MMC with unified control scheme. Experimental waveforms of the bipolar MMC for six steady-state power flow scenarios are shown in Figs. 3.23-3.28.

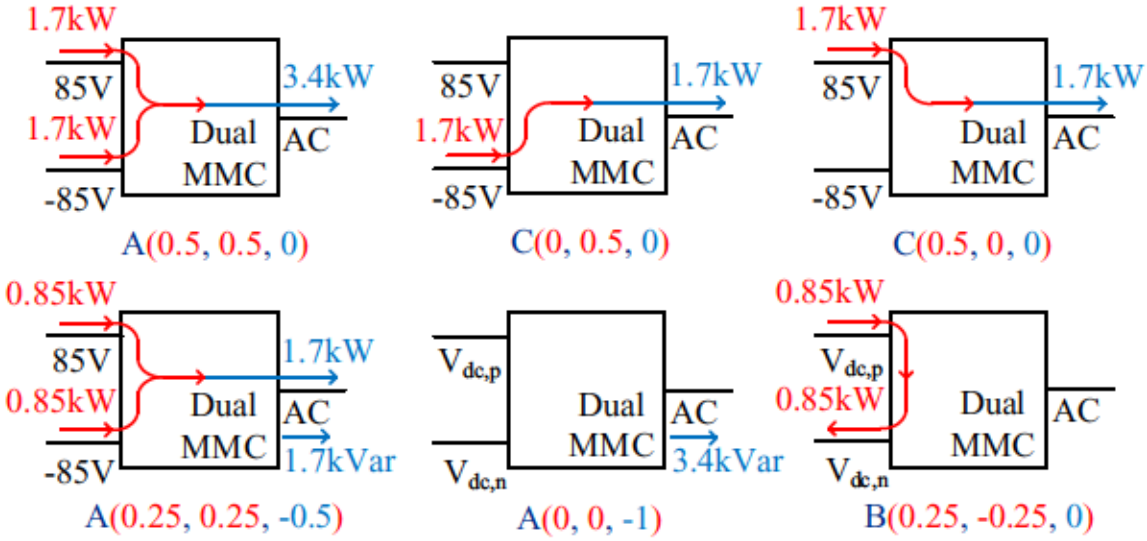

Figure 3.22: Experimental bipolar MMC steady-state power flow scenarios under study

In scenario $A(0.5, 0.5, 0)$ (ref. Fig. 3.23), each dc pole delivers 1.7 kW to the ac grid, i.e. $P_{dc,p} = P_{dc,n} = 1.7$ kW, and thus $P_{ac} = -3.4$ kW. The grid reactive power injection is set to zero. With dc pole voltages $V_{dc,p} = V_{dc,n} = 85$ V, this rated power transfer results in 20 A_{dc} current for each pole $i_{dc,p}$ and $i_{dc,s}$ as shown in Fig. 3.23. The grid voltage $v_{a,g}$ and grid current $i_{a,g}$ have opposite phases to denote the grid absorbing real power. The capacitor voltages (representative waveforms shown for upper and lower arms of phase a in MMC1) are well balanced. All four SM capacitor voltages of phase a in MMC1 (two in the upper arm and two in the lower arm) are shown in Fig. 3.23. It can be seen that the SM capacitor voltage sort and selection algorithm ensures voltage balancing within each arm. The center-tapped transformer winding in Fig. 3.23 carries only ac current as expected, while the arm currents have dc and fundamental frequency parts.

Figs. 3.24 and 3.25 show steady-state results for power flow scenarios $C(0, 0.5, 0)$ and $C(0.5, 0, 0)$, respectively. These are multi-frequency operating points where the arms process unequal powers. This can be seen with the capacitor voltage waveforms. That is, in Fig. 3.24 the upper arm capacitor voltages have negligible ripple as $i_{dc,p} = 0$

while in Fig. 3.25 the lower arm capacitor voltages have negligible ripple given $i_{dc,s} = 0$. This validates independent pole operation in a bipolar system. In both scenarios, center-tap winding currents at the converter side $i_{trans,a1}$ and $i_{trans,a2}$ contain both dc and ac components. The dc components of $i_{trans,a1}$ and $i_{trans,a2}$ are always kept the same by the controllers. Consequently, the flux produced by dc currents in the core cancel out with each other at the converter side due to windings orientation. The winding current in phase a at the grid side $i_{a,trans,g}$ only has ac component.

Figs. 3.26 and 3.27 show steady-state results for power flow scenarios A(0.25, 0.25, -0.5) and A(0, 0, -1), respectively. In Fig. 3.27 (scenario A(0, 0, -1)), no real power is transferred between any ports and hence $i_{dc,p}$ and $i_{dc,s}$ are zero. The capacitor voltage waveforms in Figs. 3.26 and 3.27 are differ from Figs. 3.23-3.25 due to extra reactive power consumption.

In scenario B(0.25, -0.25, 0) (ref. Fig. 3.28), no power is transferred between bipolar dc system and ac grid. Positive dc pole delivers 1.7 kW to the negative dc pole, i.e. $P_{dc,p} = 1.7$ kW, $P_{dc,n} = -1.7$ kW, and thus $P_{ac} = 0$ kW. With dc pole voltages $V_{dc,p} = V_{dc,n} = 85$ V, this rated power transfer results in 10 A_{dc} current for each pole $i_{dc,p}$ and $i_{dc,s}$. The center-tap winding currents at the converter side $i_{trans,a1}$ and $i_{trans,a2}$ contain only dc components.

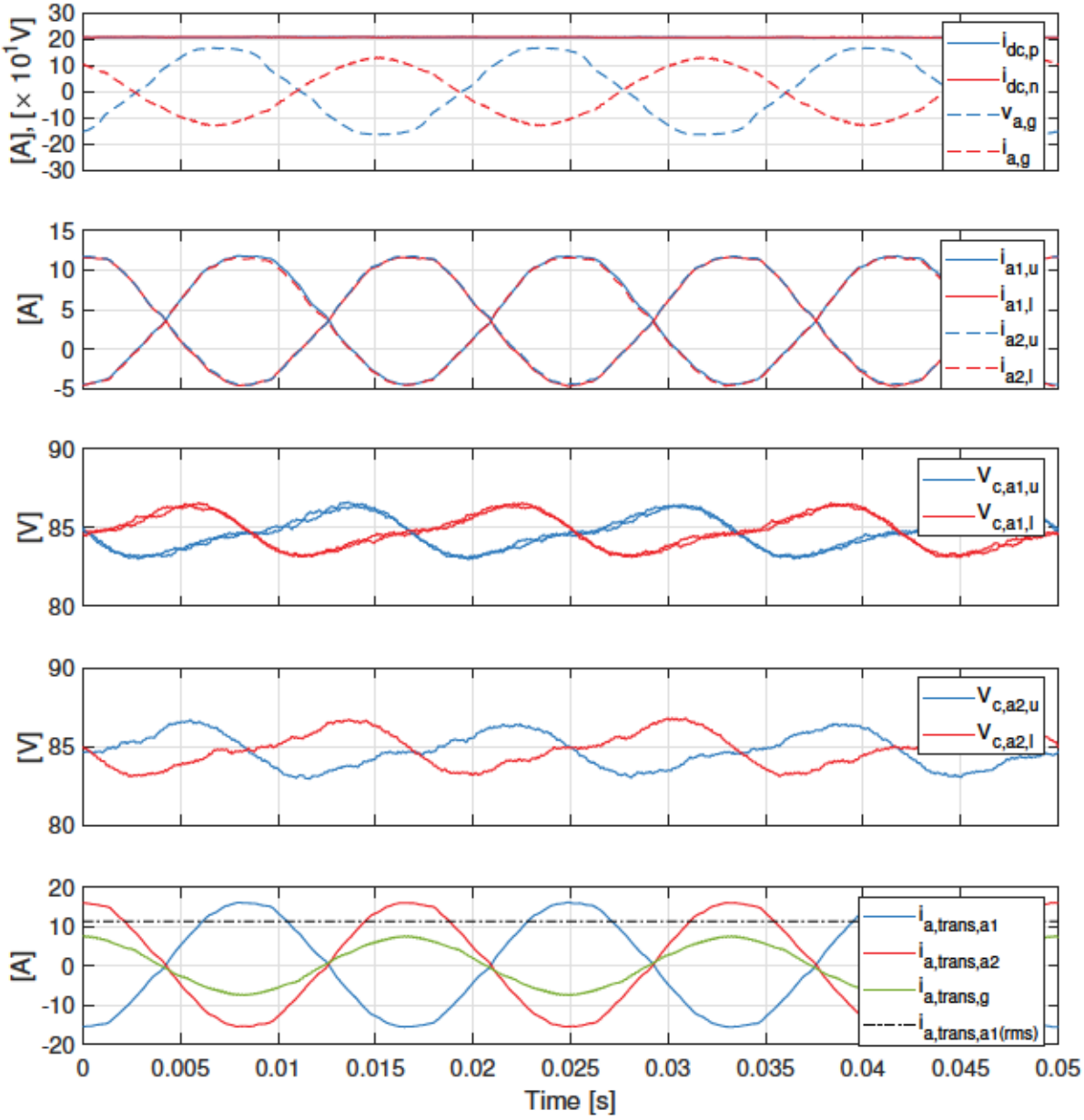

Figure 3.23: Experimental waveforms of bipolar MMC for steady-state power flow scenarios: $A(0.5, 0.5, 0)$

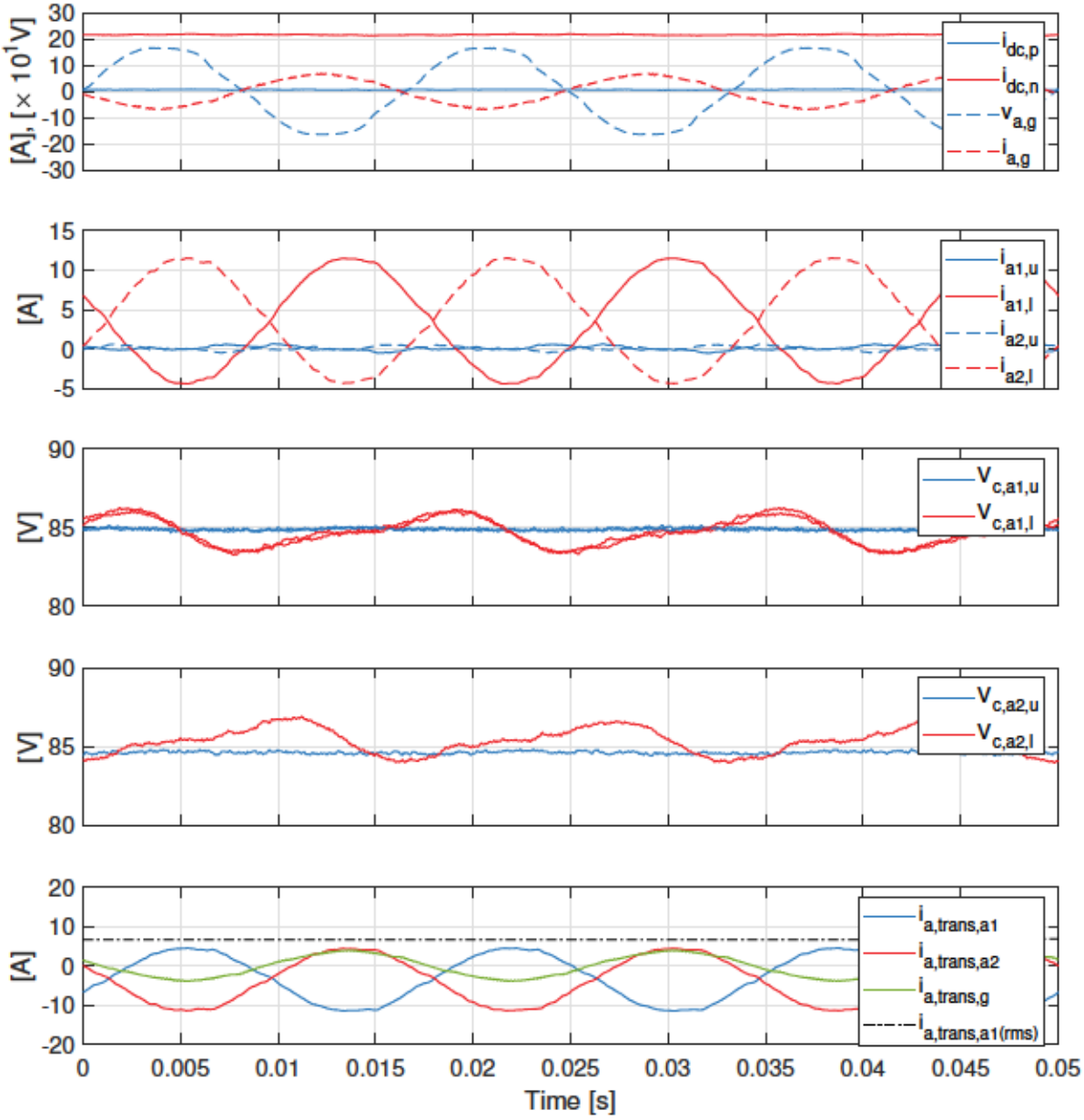

Figure 3.24: Experimental waveforms of bipolar MMC for steady-state power flow scenarios: $C(0,\ 0.5,\ 0)$

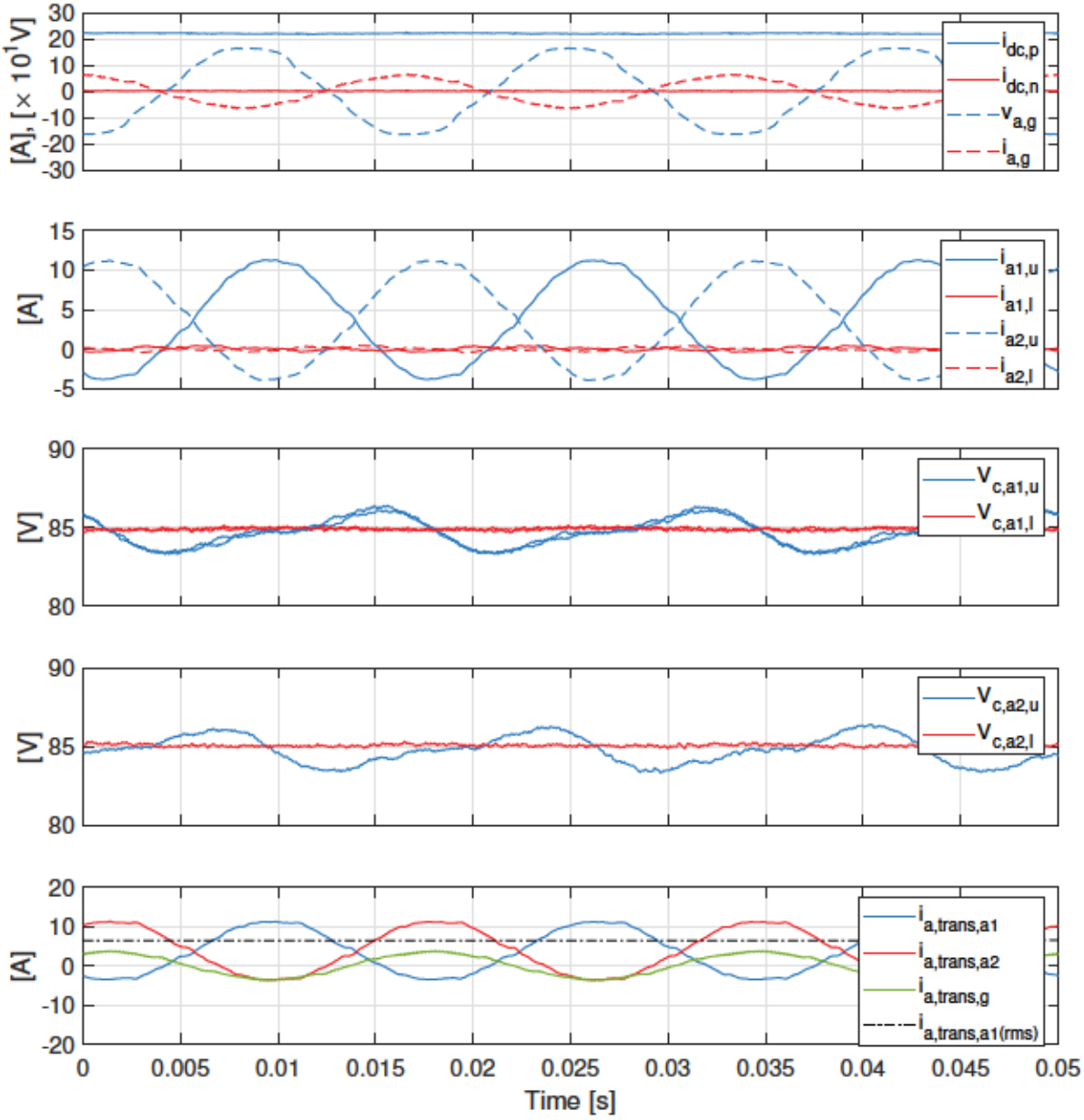

Figure 3.25: Experimental waveforms of bipolar MMC for steady-state power flow scenarios: $C(0.5, 0, 0)$

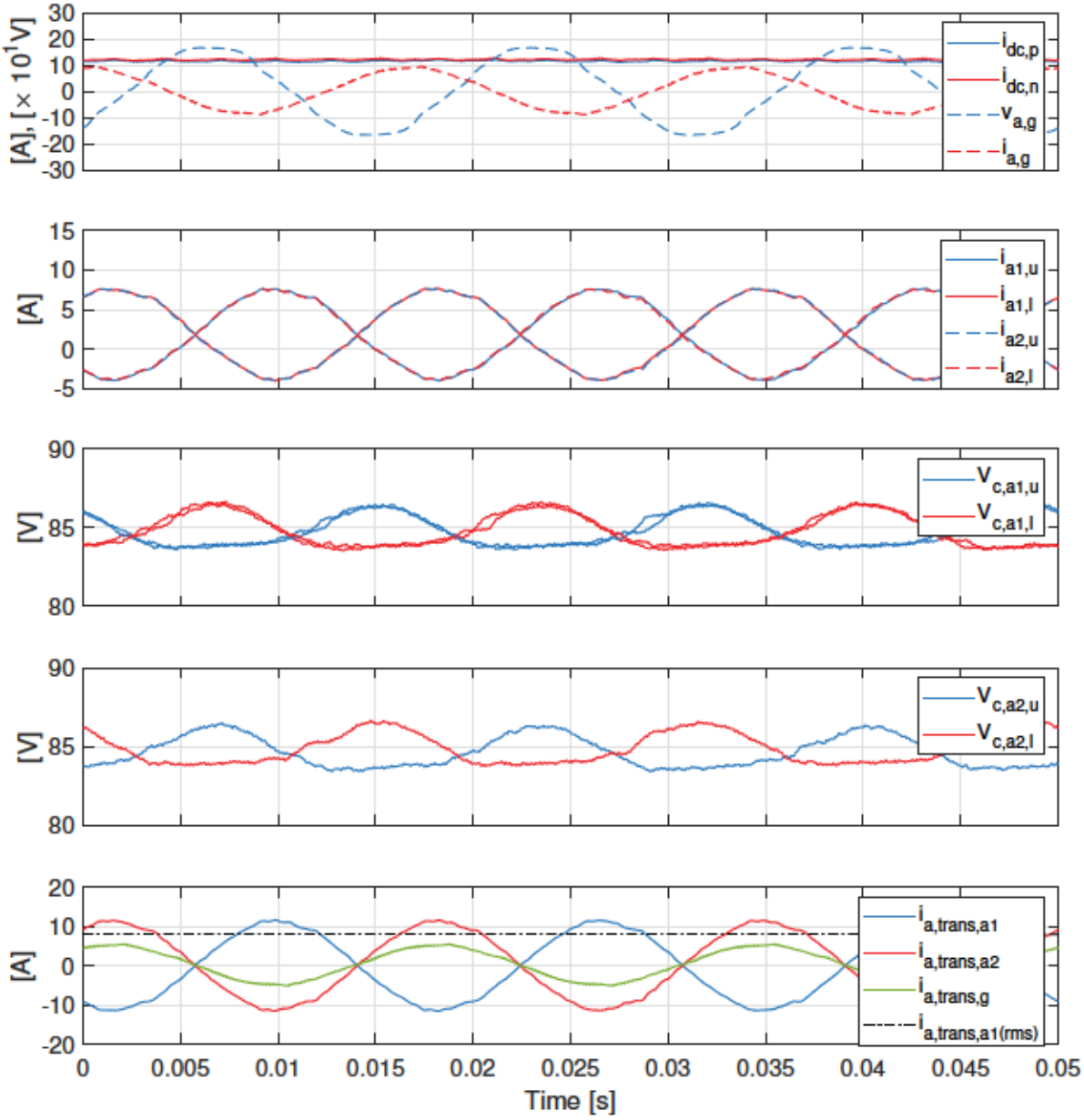

Figure 3.26: Experimental waveforms of bipolar MMC for steady-state power flow scenarios: $A(0.25, 0.25, -0.5)$

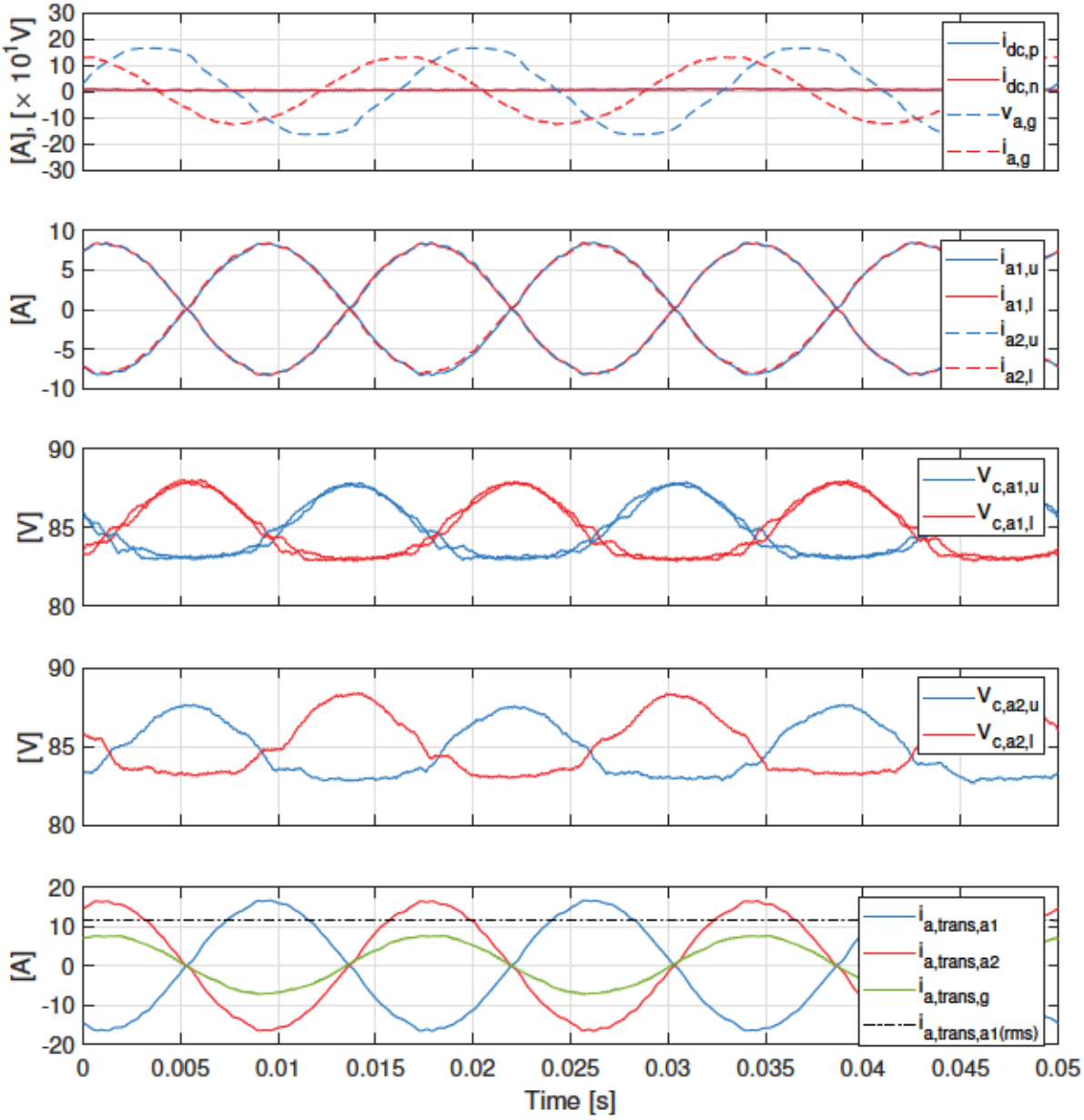

Figure 3.27: Experimental waveforms of bipolar MMC for steady-state power flow scenarios: $A(0, 0, -1)$

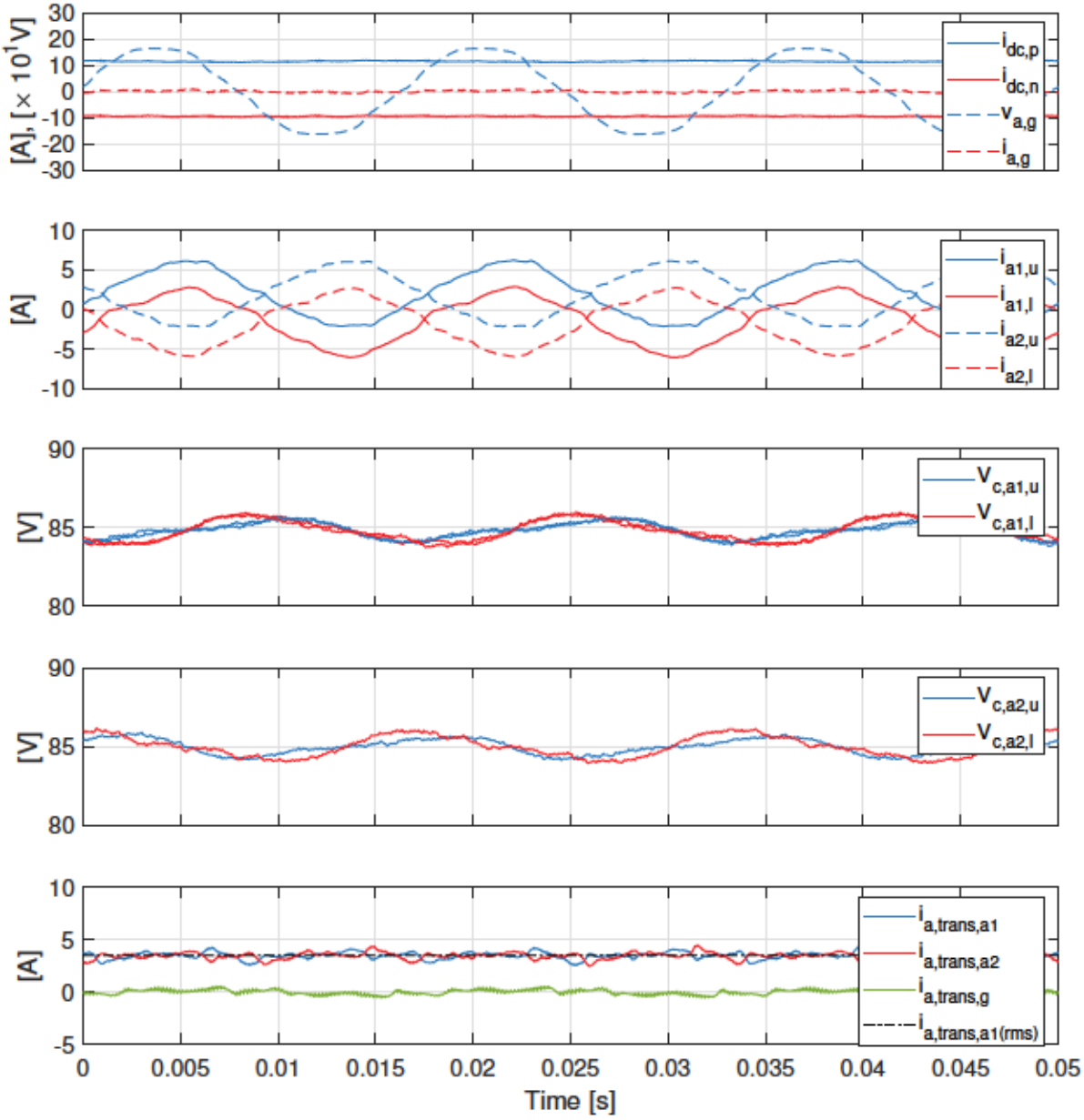

Figure 3.28: Experimental waveforms of bipolar MMC for steady-state power flow scenarios: $B(0.25, -0.25, 0)$

3.6.3 Dynamic Performance

Three power flow scenarios as shown in Fig. 3.29 are used to demonstrate the dynamic response of the bipolar MMC for changing loading conditions.

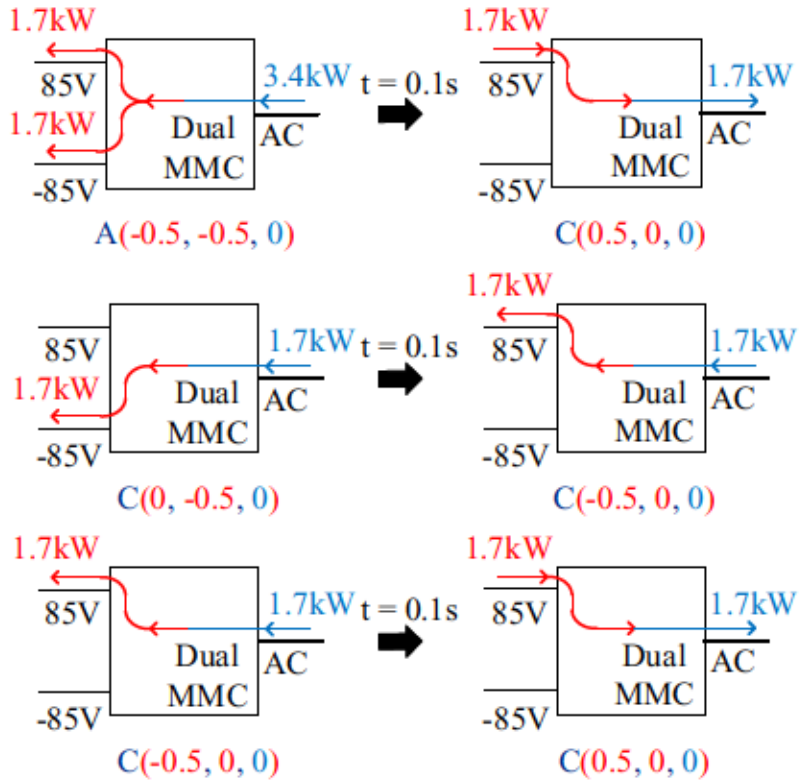

Figure 3.29: Experimental bipolar MMC dynamic response under study

As been discussed in section 3.6.2, both dc poles can operate independently at a power rating of 1.7 kW. This section further validate that balanced capacitor voltages between arms are maintained for changing loading conditions. The change in power demand of each pole initially causes a dc voltage imbalance between SM capacitors in the upper and lower arms, i.e., $V_{c,a1,u}$ and $V_{c,a1,l}$ deviate from their reference values. The controller re-establishes balanced capacitor voltages by requesting the requisite change in the fundamental frequency components of $\mathbf{i}_{\alpha\beta,\Sigma1}$ and $\mathbf{i}_{\alpha\beta,\Sigma2}$. The maximum rms current in the transformer center-tapped winding $i_{a,trans,a1(rms)}$ occurs when both dc poles operate at rated power. This verifies that the center-tapped transformer employed in the proposed bipolar MMC can be rated the same as a standard grid interface transformer in conventional dc-ac MMC application. The transformer a1 current $i_{trans,a1}$ in each plot also verifies the center-tapped transformer does not saturate, as dc flux cancellation is achieved in the core.

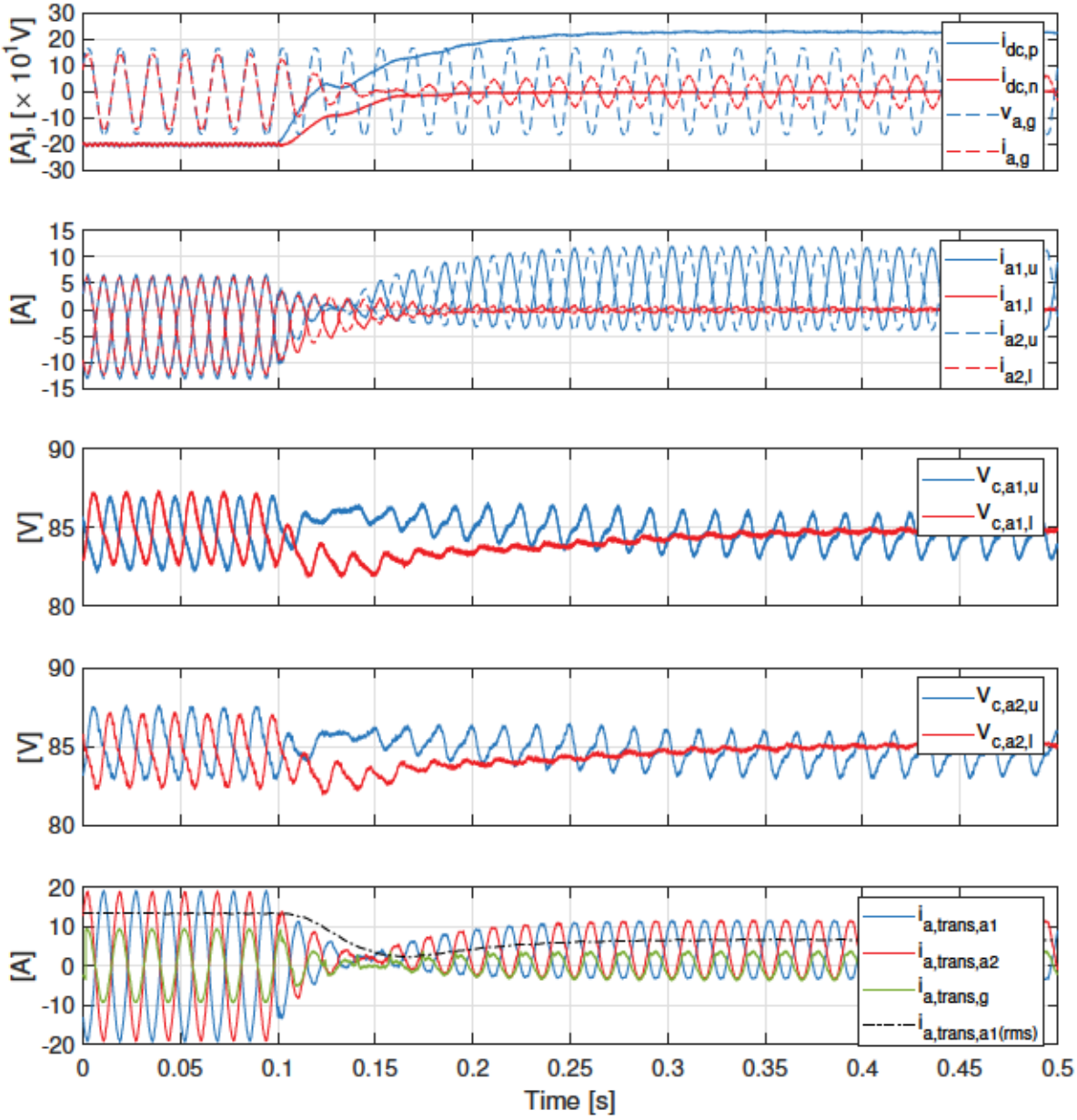

Figure 3.30: Experimental waveforms of bipolar MMC for transient power flow scenarios: from C(0, -0.5, 0) to C(-0.5, 0, 0)

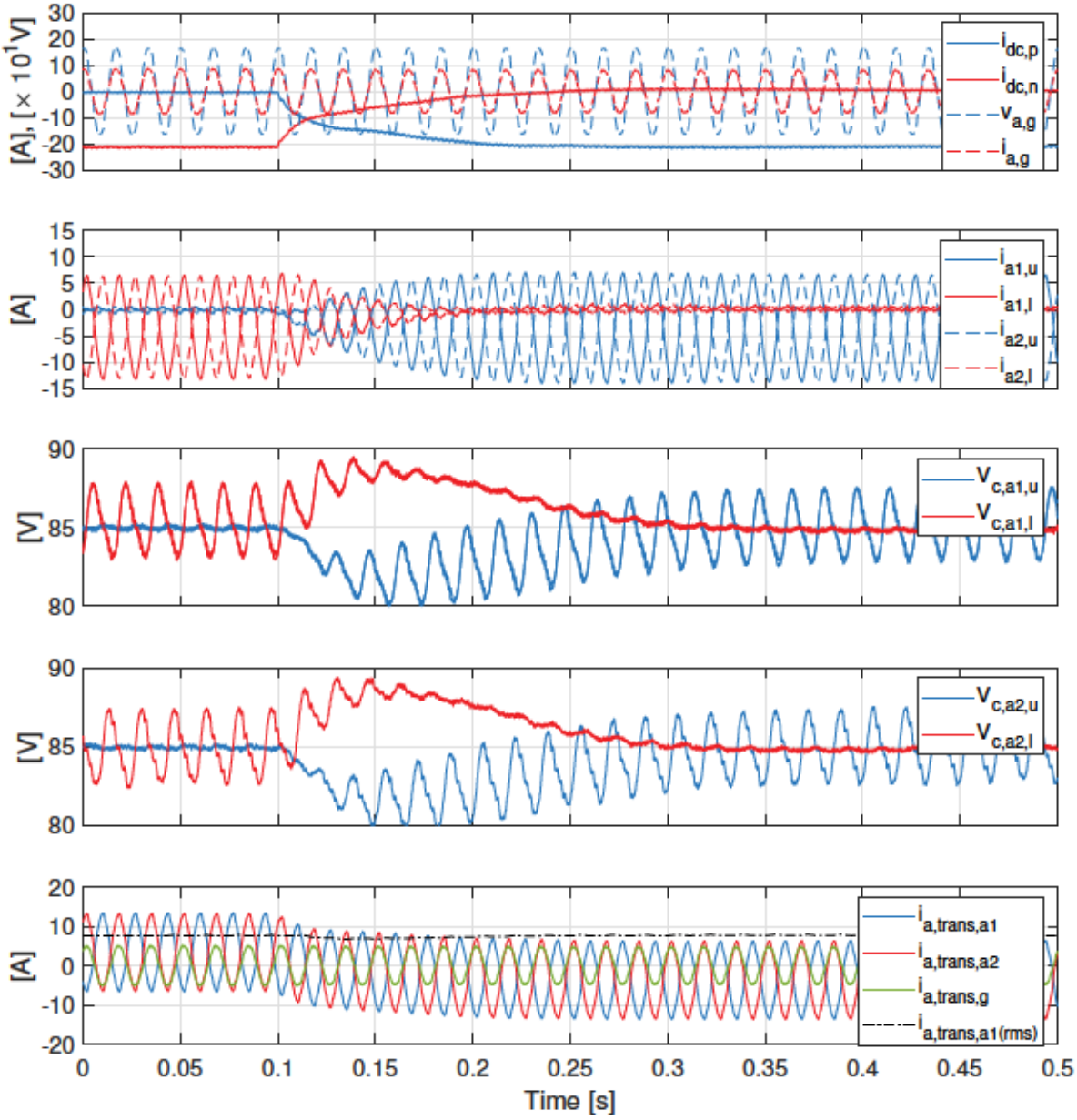

Figure 3.31: Experimental waveforms of bipolar MMC for transient power flow scenarios: from A(-0.5, -0.5, 0) to C(0.5, 0, 0)

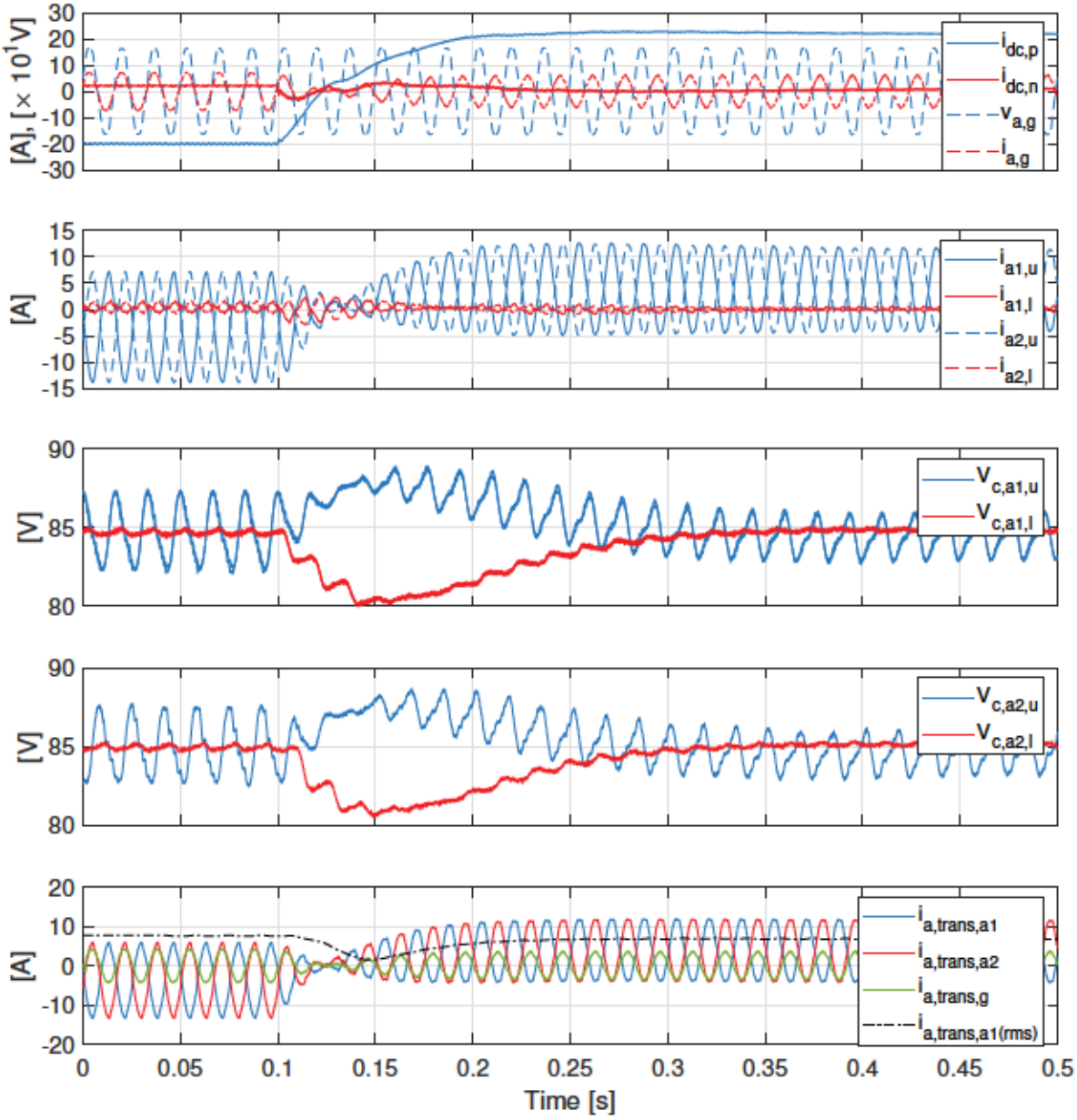

Figure 3.32: Experimental waveforms of bipolar MMC for transient power flow scenarios: from C(-0.5, 0, 0) to C(0.5, 0, 0)

3.6.4 Independent MMC Operation

Fig. 3.34 demonstrates that both MMCs in the proposed bipolar can operate independently. This is power flow scenario $A(0.25, 0.25, 0)$ as shown in Fig. 3.33. Initially, MMC1 processes 1.7 kW (0.5 p.u.) and then MMC1 ramps down to zero while MMC2 is ramped up from zero to process 1.7 kW (0.5 p.u.). The grid current $i_{a,g}$ remains constant during the dynamic. This shows that the bipolar MMC allows each MMC to process up to 0.5 p.u. power independently. If one MMC fails, the other MMC can continue operation for ac power transfer with a reduced output power and hence can help improve system reliability. This redundancy is not possible to achieve with bipolar MMCs in Fig. 3.3.

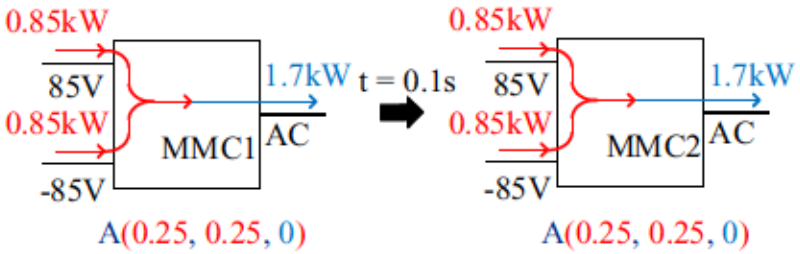

Figure 3.33: Experimental bipolar MMC dynamic response for independent MMC operation

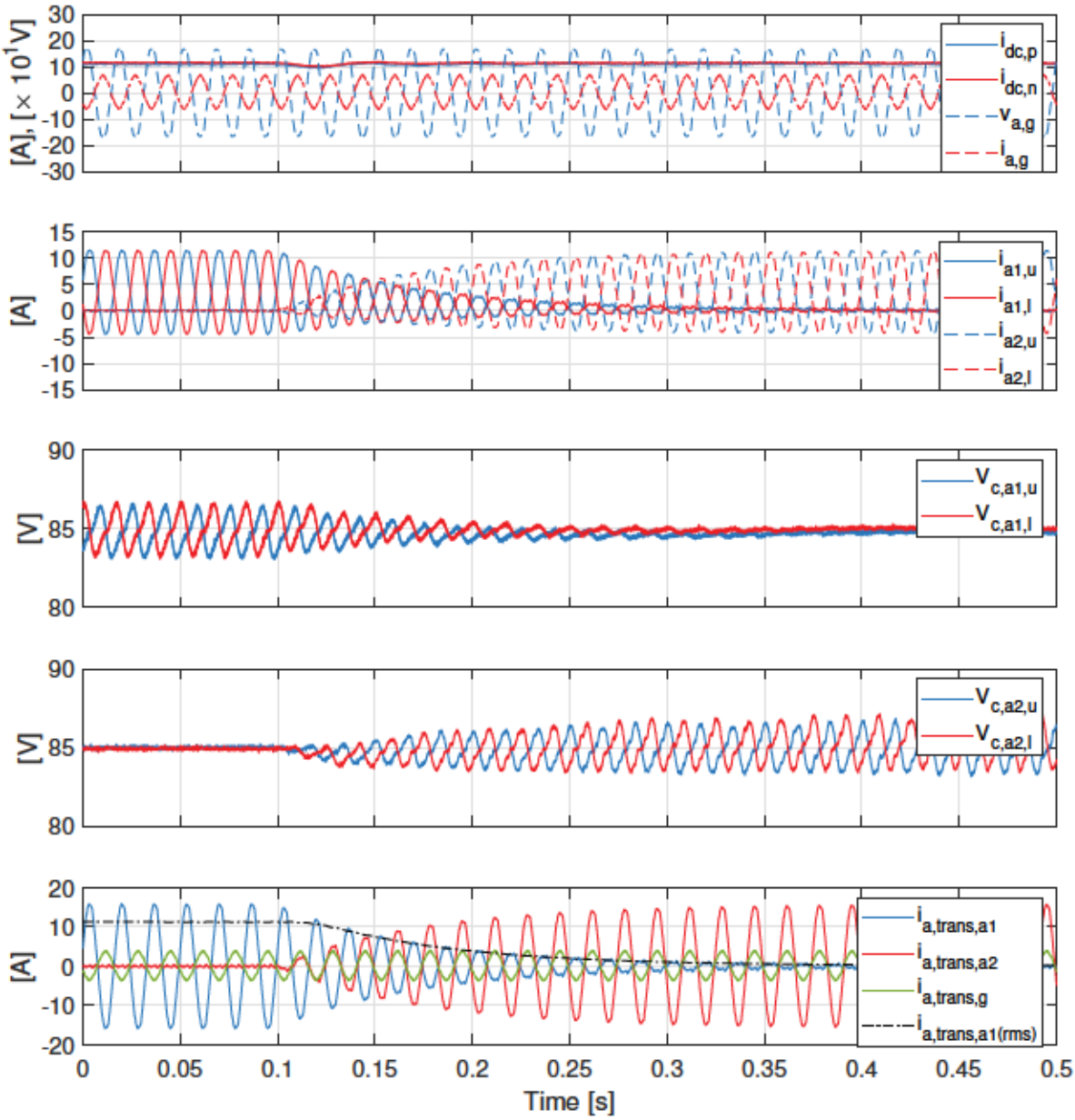

Figure 3.34: Experimental waveforms of bipolar MMC for transient power flow scenarios: from $A(0.25, 0.25, 0)$ where 0.5 p.u. power processed by MMC1 to $A(0.25, 0.25, 0)$ where 0.5 p.u. power processed by MMC2

3.7 Discussion on Practical Consideration for Magnetics

The transformer used in the proposed dual MMC structure is equivalent to a conventional grid interface transformer with center-tapped windings on the converter side and does not have to be rated to cope with any dc flux[3]. Three-phase transformers are widely used for ac transmission and distribution systems. For HVDC transmission, the converter transformer also plays a role in the converter station structure as connecting the ac grids to the dc transmission lines. Dc bias, losses, vibration and harmonic noise of the transformer used in HVDC converter should be specially considered [98, 99]. Otherwise, they may lead to some engineering projects' operation failures. The transformer used in important transmission and generator applications are usually designed as single-phase core-type to ensure a robust operation [100, 101]. For transformer with more than 500 kV is required, two units are cascaded in series to produce the required voltage. The three-phase transformer used in the proposed dual MMC structure can also be designed as three individual single-phase transformer to enhance the reliability of the transformer, which is validated in simulation and experiment (see Sections 3.5 and 3.6). On the other hand, in the actual bipolar dc operation, if the topology of the system only uses one pole at an end which forms the circuit with the ground, the dc bias current will flow through the neutral point and enter into the windings, which contributes to the undesirable vibration [101]. However, the dc bias current due to unbalanced dc pole power will not cause core dc flux in the proposed bipolar dual MMC[4].

[3] Although an extra dc current component exists in the windings, analysis in [58, 60, 62] reveals that it is sufficient to rate them for just the ac component

[4] Additional manufacturer tests on the dc flux cancellation should be performed when it is implemented in high voltage applications

3.8 Chapter Summary

This chapter introduces a multi-frequency dual MMC structure that improves upon the three-port M2DC-CT from Chapter 2. The resulting multi-frequency structure yields a novel bipolar MMC that allows fully independent control of the dc pole power injections to accommodate unbalanced conditions for bipolar dc systems. The two MMCs are parallel-connected and center-tapped transformer windings are used at the converter side that can handle both dc and ac currents, while imposing dc flux cancellation in the core. Most importantly, the power rating of the three-winding transformer is equal to that of a conventional two-winding ac transformer, i.e., no penalty in transformer Volt-Ampere rating is incurred for the proposed bipolar dual MMC.

A comparison of the bipolar dual MMC structure against existing multi-frequency bipolar MMC structures is conducted to highlight their contrasting features. The bipolar dual MMC structure uses a relatively simpler three-winding transformer with center-tapped transformer windings at the converter side, as opposed to a zig-zag connection. The proposed structure interleaves two MMCs in contrast to previously reported series and single MMC arrangements, thus offering increased design flexibility for MVDC and HVDC applications where higher current and/or lower insulation requirements are essential. It also can bring advantages in terms of converter reliability as two independent MMCs are employed. Although two parallel MMCs are utilized, the proposed dual MMC setup can by appropriate design achieve the same total semiconductor losses as the single MMC structures when transferring the same amount of power.

The proposed bipolar dual MMC structure operation is analyzed and modeling results inform on development of a unified dynamic control structure for the elementary multi-frequency dual MMC structure. PSCAD/EMTDC simulation results using the switched model and extensive experimental results from a 3.4 kW prototype validate the ability to maintain power balance of SM capacitors at varying power transfers by way of circulating ac currents. The converter is also validated experimentally to allow each dc pole and each MMC to independently process up to 0.5 p.u. power.

Chapter 4

Three-Port MMC Derived from Multi-Frequency Dual MMC Structure

Mixed ac-dc power systems can utilize multi-port converters to control power flows between the different dc and ac grids, e.g., to inject power extracted from offshore wind turbines to the onshore ac load centres [67]. Moreover, multi-port converters can enable power exchange between existing interconnected networks via HVDC or MVDC links. In this thesis, the term *multi-port* denotes a converter system with multiple dc and/or ac voltage ports. In this chapter, three-port converters for routing power between two different monopolar dc networks and an ac system are specifically studied.

Power electronic dc-dc and dc-ac converter stages are the key building blocks of multi-port converters. The dc-dc converters can in general be galvanically isolated or non-isolated [56], and voltage-sourced converter or line-commutated converter technologies can be used for dc-ac conversion [102]. The simplest way to form a multi-port converter is to combine separate dc-dc and dc-ac converters, but this imposes multi-stage power conversion that can lead to lower efficiency and higher cost [103]. Alternatively, unnecessary conversion stages can be avoided by merging dc-dc and dc-ac stages into a single converter arrangement. This can increase system efficiency and provide a more compact footprint. Such multi-port converters are increasingly being studied for various applications like renewable power integration, electric vehicles, uninterruptible power supply systems, and hybrid energy storage systems, e.g. [91, 104, 105]. However, limited work has been carried out on high-voltage and high-power multi-port topologies due to the increased structural and control complexity relative to their lower voltage and power counterparts.

MMC-based multi-port systems are well suited for application in mixed ac/dc

grids containing HVDC and MVDC systems. Dc-dc converter topologies that exploit established MMC technology to accommodate high voltage and power applications have emerged in recent years [16, 29, 56]. Multi-port MMCs can be created by augmenting dc-dc MMCs with a dc-ac stage. In this chapter, a three-port MMC for routing power between two different monopolar dc networks and an ac system is derived from the multi-frequency dual MMC structure studied in Chapter 3. The three-port dual MMC uses the same three-winding transformer with center-tapped connection at the converter side windings. Unlike the previous bipolar application where the two dc ports have equal voltages, the two dc systems in the three-port MMC have different voltage levels and each dc port can process more than 0.5 p.u. of power. The unified control scheme proposed in Chapter 3 is extended for the three-port dual MMC to independently control two dc and one ac terminals power transfers while keeping submodule capacitor voltages balanced. Fault blocking of three-port dual MMC is studied with simulation cases. Converter operation and dynamic controls are validated by simulation and experiment.

4.1 Evolution of Three-port MMCs

Chapter 3 focused on a bipolar MMC configuration with pole voltages $V_{dc,p}$ and $V_{dc,n}$ (most often $V_{dc,p} = V_{dc,n}$). The four representative bipolar MMC configurations (circuit with solid lines) are summarized in Figs. 4.1a-b[1] [82, 83], 4.1c, 4.1d [16], 4.1e [17, 18] where $V_{dc,1}$ and $V_{dc,2}$ represent the primary and secondary side dc voltages, respectively. Fully independent control of positive and negative dc pole power injections can be achieved for enhanced reliability. By redefining the dc connections in Fig. 4.1a, a three-port MMC system can alternatively be realized (circuit with dashed lines, $V_{dc,1}$ and $V_{dc,2}$ denoting separate dc systems) for power transfer between two dc systems and an ac grid [67, 106]. This dc-dc-ac MMC structure (circuit with bold lines) is the well-known dc-dc F2F-MMC topology (first proposed in [31]) augmented with an ac grid connection. In this chapter, dc-dc-ac MMC structure refers to the elementary MMC structure for dc-dc-ac power transfer. $V_{dc,1}$, $V_{dc,2}$, v_{ac} in Fig. 4.1a are all galvanically separated, however, the power being transferred between any combination of dc and ac ports is always processed by both MMCs and the transformer.

Now consider the dual MMC setup in Fig. 4.1b where the only difference from Fig. 4.1a is that $V_{dc,1}$ and $V_{dc,2}$ share a common reference point. The resulting three-port converter (circuit with dashed lines) is the HVDC-AT [10] augmented with an

[1]Bipolar MMC configuration (circuit with solid lines) in Fig. 4.1b is identical to the bipolar MMC configuration in Fig. 4.1a, but its three-port version is different

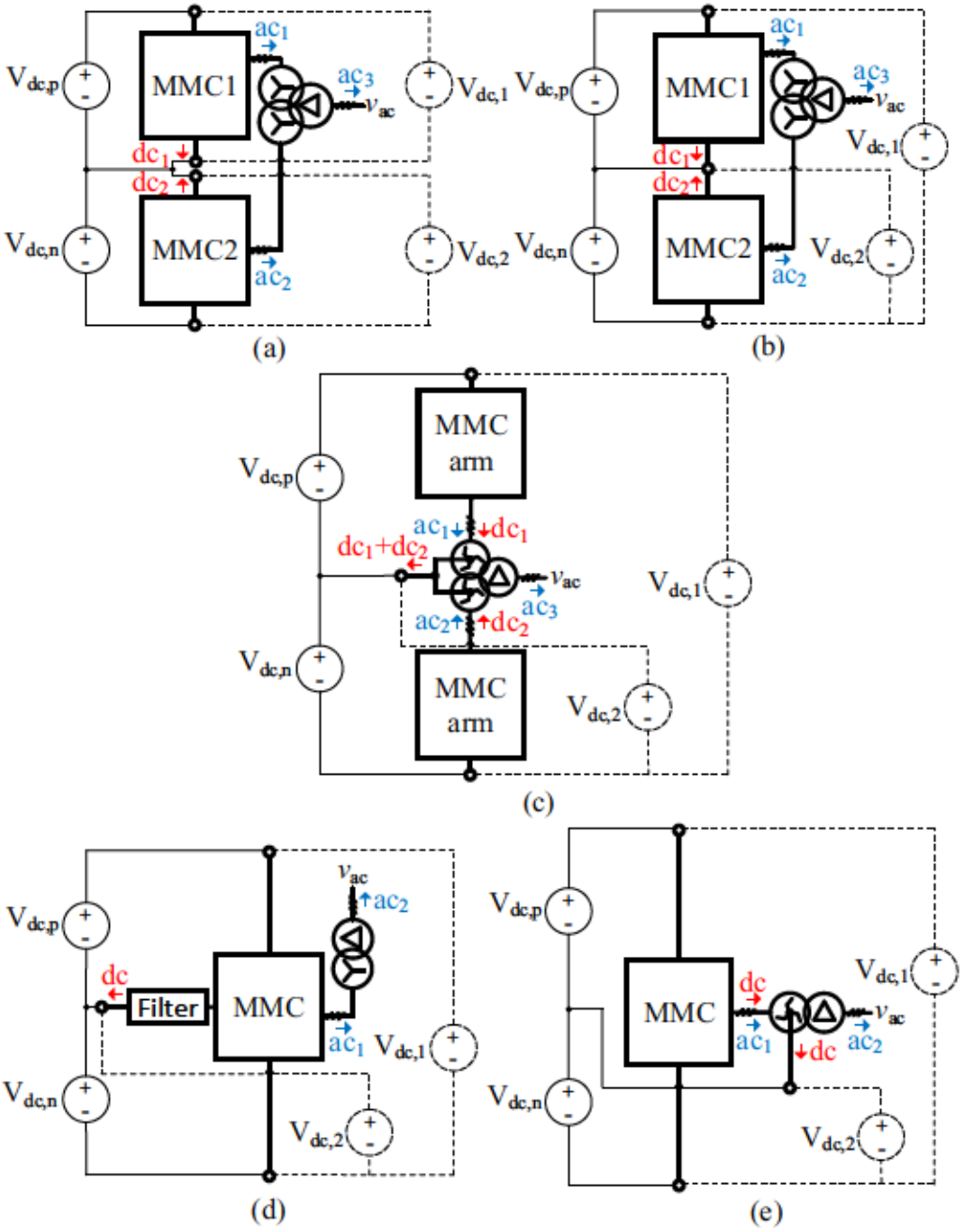

Figure 4.1: Dual and single dc-dc-ac MMC structures (circuit with bold lines), where solid (and dashed) lines denote electrical connections for bipolar $+V_{dc,p}/-V_{dc,n}$ (and three-port $V_{dc,1}$, $V_{dc,2}$) dc systems, based on: (a) F2F-MMC with transformer, (b) HVDC-AT with transformer, (c) M2DC-CT with multi-tasking zig-zag transformer in series with the converter arms, (d) M2DC with conventional grid interfacing transformer, (e) MMC with multi-tasking zig-zag transformer

ac grid connection [4, 106, 107].[2] But the resulting bipolar MMC setup (circuit with

[2]Such three-port MMC structure can be adapted for an arbitrary number of dc ports [4, 107]

solid lines) remains identical to the bipolar setup in Fig. 4.1a. The sharing of MMCs between $V_{dc,1}$ and $V_{dc,2}$ in Fig. 4.1b yields a partial-power-processing three-port DC-AT with single-stage dc-dc conversion. This eliminates redundant energy conversion in comparison to the three-port F2F-MMC in Fig. 4.1a. The caveat is that galvanic separation between $V_{dc,1}$ and $V_{dc,2}$ in Fig. 4.1b is relinquished. The ac grid interfacing transformers in the three-port F2F-MMC and three-port HVDC-AT must tolerate a large dc voltage bias between windings [56]. This stress is 50% of $V_{dc,1}$ for the HVDC-AT. This leads to increased size, weight and core design complexity for the transformer [84].

The dc-dc-ac MMC structures (circuit with bold lines) in Figs. 4.1a and 4.1b, regardless of bipolar or three-port application, use classical transformer action to transfer ac power at their respective midpoint nodes. That is, the transformer connected at the midpoint of each MMC carries only ac current (represented by blue arrows in Figs. 4.1a, 4.1b). Observe that only dc currents flow between MMCs (represented by red arrows in Figs. 4.1a, 4.1b). Chapter 3 also introduced three bipolar MMC configurations (circuit with solid lines) that exploited multi-frequency power transfer, shown here in Figs. 4.1c, 4.1d, 4.1e, where both dc and ac power transfers can occur at the MMC midpoint node. The benefits of the two-port M2DC-CT proposed in Chapter 2 are most pronounced at low dc step ratios, and thus the three-port version of M2DC-CT in Fig. 4.1c (circuit with dashed lines) may become an attractive alternative for HVDC and MVDC applications with low dc step ratios.

Figs. 4.1d and 4.1e (circuit with dashed lines) use the same single MMC structures but the latter avoids a costly and bulky filter by multi-tasking a zig-zag transformer with multiple frequency components (without incurring any penalty in transformer Volt-Ampere rating). Therefore, Fig. 4.1e (circuit with dashed lines) is considered a state-of-the-art multi-frequency bipolar MMC, although the requisite zig-zag transformer has a more complicated winding arrangement and thus higher manufacturing cost [17]. Similar to dc-dc-ac MMC structures in Figs. 4.1a, 4.1b, 4.1c, the multi-frequency dc-dc-ac MMC structures of Figs. 4.1d and 4.1e (circuit with bold lines) can be deployed for three-port systems (circuit with dashed lines, separate dc systems $V_{dc,1}$ and $V_{dc,2}$). The three-port application in Fig. 4.1e is identified for the first time in this work, although it bears operational similarity with the three-port M2DC in Fig. 4.1d [19, 67, 85].

4.2 Proposed Three-port Dual MMC Structure

The elementary dc-dc-ac MMC structure proposed in Chapter 3 is repeated in Fig. 4.2 (circuit with bold lines), where the MMCs share a common dc link. The bipolar dual MMC structure proposed in Chapter 3 is shown in Fig. 4.2a (circuit with solid lines). By making changes to the dc port connections, a three-port dual MMC for routing power between two dc systems, $V_{dc,1}$ and $V_{dc,2}$, and a three-phase ac grid, v_{ac}, is derived in Fig. 4.2b (circuit with dashed lines). The two MMCs share a common dc port, $V_{dc,1}$. The common neutral wye-point of the transformer is connected to a lower voltage dc port, $V_{dc,2}$. The voltages of the two dc ports in three-port MMC in Fig. 4.2b are different, unlike in Fig. 4.2a where the two dc ports have equal voltages. Dc system $V_{dc,1}$ in Fig. 4.2b can process more than 0.5 p.u. of power. The topology allows simultaneous dc-dc and dc-ac conversions between an ac grid and two dc systems. The dc port power injections are denoted by $P_{dc,1}$ and $P_{dc,2}$, associated with two dc systems of different voltage levels. Similar to Fig. 4.2a, multi-frequency power transfer capability is achieved in Fig. 4.2b as the MMC midpoints can inject multiple frequency components. The transformer windings must carry both dc and ac currents. However, the center-tap windings on the converter side have an equal number of turns but are wound in opposite directions around the transformer core (represented by the dots) to provide core dc magnetic flux cancellation.

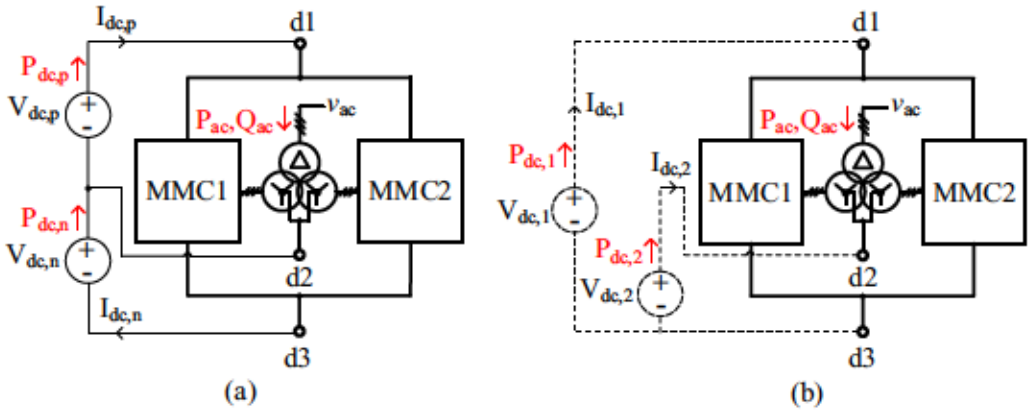

Figure 4.2: Elementary multi-frequency dc-dc-ac MMC structure, where solid and dashed lines respectively denote electrical connections for (a) bipolar $+V_{dc,p}/-V_{dc,n}$ dc systems, (b) three-port $V_{dc,1}$, $V_{dc,2}$ dc systems

By exploiting multi-frequency power transfer, Fig. 4.2b offers some benefits over their conventional single-frequency counterparts: i) partial-power-processing is maintained, ii) transformer Volt-Ampere rating can be reduced in vast majority of power flow scenarios, as will be demonstrated in Chapter 5, and iii) large dc voltage bias

between transformer windings can be eliminated. The proposed three-port MMC configuration where both ac and dc currents are simultaneously injected at the MMC midpoint node is shown in Fig. 4.3. Three-phase MMCs are used in Fig. 4.3, where each phase leg is comprised of two arms: a primary arm (and secondary arm) with n_p (and n_s) cascaded SMs. In the following, p and s refer to any primary and secondary arms, respectively. The conventional HBSM is sufficient for standard operation. However, as with the bipolar MMC in Fig. 4.2a, FBSMs can be used to control the maximum arm ac voltage regardless of the available dc voltage in addition to providing dc fault interrupting capability [7, 50, 51]. But it will result in a higher number of power devices and commensurately higher power loss. Dc fault blocking of three-port MMC with FBSMs will be investigated in Section 4.5.

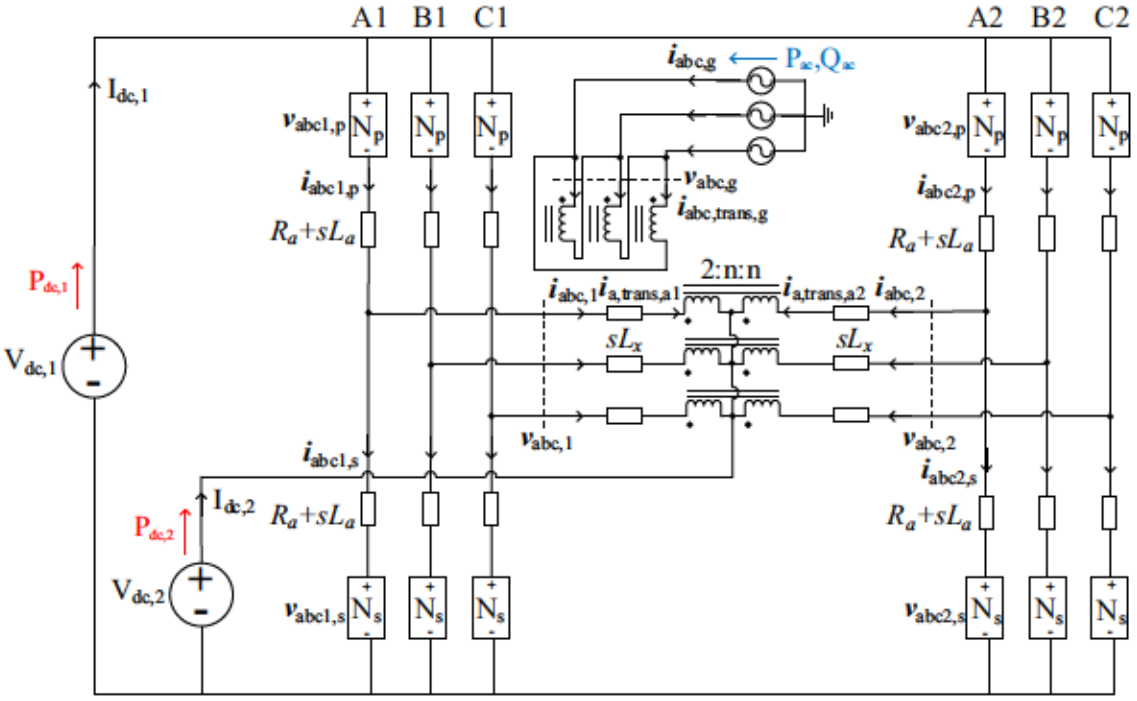

Figure 4.3: Proposed three-port dual MMC circuit schematic

The unified dynamic controller structure in Fig. 3.12 of Section 3.4.2 can be easily adapted for the proposed three-port MMC in Fig. 4.3. The control schemes for the bipolar dual MMC including outer capacitor voltage regulation loops and inner current control loops are identical to the proposed three-port MMC (ref. Fig. 3.12). The outer power control loop for the three-port dual MMC are shown in Fig. 4.4.

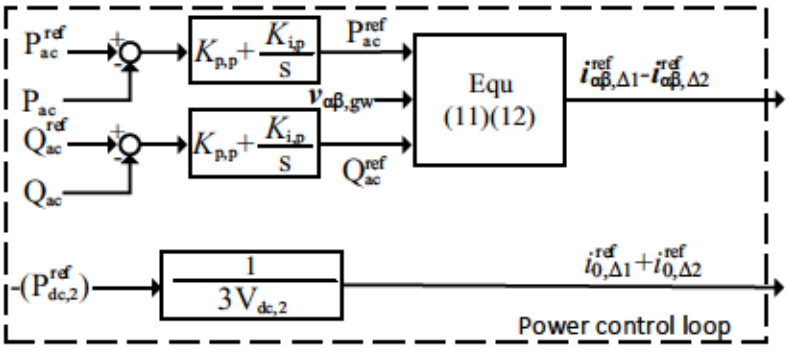

Figure 4.4: Outer power control loop of Fig. 3.12 for proposed three-port MMC in Fig. 4.3

4.3 Transformer Center-tapped Windings Current Stresses

The transformer grid side winding in Fig. 4.3 carries only fundamental frequency ac current at all times. Hence, it only needs to be rated for the grid side rms current, which is the same as the ac transformer used in conventional dc-ac MMC with the same power rating. This section will investigate the current stress of the converter-side center-tapped windings. The following assumptions are imposed, i) the secondary dc port voltage $V_{dc,2}$ is half of the primary dc port voltage $V_{dc,1}$ and thus by design the number of SMs in primary and secondary arms are the same, ii) the preceding SM design assumption ($N_p = N_s$) yields a three-port MMC with dc-dc conversion ratio $V_{dc,1}/V_{dc,2} = 2$, and iii) the rated port power injections are $\{P_{dc,1},\, P_{ac},\, Q_{ac}\} \in (-1, 1)$ p.u. and $\{P_{dc,2}\} \in (-0.5, 0.5)$ p.u.. Assuming for ease of analysis that reactive power transfer is negligible, ac port power injection P_{ac} can be expressed as

$$P_{ac} = -(P_{dc,1} + P_{dc,2}) \tag{4.1}$$

The primary and secondary dc current can be expressed as

$$I_{dc,1} = \frac{P_{dc,1}}{V_{dc,1}},\; I_{dc,2} = \frac{P_{dc,2}}{V_{dc,2}} \tag{4.2}$$

The center-tapped winding currents can in general have both dc and ac components, thus the total center-tapped rms winding current of phase a1 can be approximated by

$$I_{a,trans,a1(rms)} = \sqrt{\left(\frac{I_{dc,2}}{6}\right)^2 + \left(\frac{P_{ac}}{3V_{a,trans,a1(rms)}}\right)^2}, \tag{4.3}$$

where transformer secondary side voltage of phase a1 $V_{a,trans,a1(rms)} = V_{dc,1}/\sqrt{2}$ assuming maximum ac voltage utilization (unity modulation index).

Fig. 4.6 shows the calculated transformer center-tapped rms winding current across all possible port power transfers for the three-port MMCs, respectively. Four different power flow scenarios are indicated by A,B,C1,C2 in Fig. 4.6 as illustrative examples, based on the notation defined in Fig. 4.5 and Table 4.1. A,B,C1,C2 correspond to pure dc-ac, pure dc-dc and two multi-frequency power transfers, respectively. Multi-frequency power transfer is defined as when the center-tapped transformer winding currents have multiple frequency (both dc and ac) components, where

$$\max\{|P_{dc,1}|, |P_{dc,2}|, |P_{ac}|\} = |P_{dc,1}| \quad for \quad C1 \tag{4.4}$$

$$\max\{|P_{dc,1}|, |P_{dc,2}|, |P_{ac}|\} = |P_{ac}| \quad for \quad C2 \tag{4.5}$$

The center-tapped rms winding current in the three-port MMC is only slightly higher than 1 p.u. for some multi-frequency power transfer cases in scenarios C2. The maximum center-tapped rms winding current occurs at $C2$(0.5, 0.5, 0) and $C2$(-0.5, -0.5, 0) as shown in Fig. 4.6, which is 1.06 p.u.. However, the center-tapped rms winding current is < 1 p.u. in the vast majority of power flow scenarios (e.g. A(1, 0, 0), B(0.5, 0.5, 0), $C1$(1, -0.5, 0) in Fig. 4.6). Therefore, the three-winding transformer used in Fig. 4.3 should be rated at $\times$1.06 p.u. as a grid interfacing transformer for conventional dc-ac MMC to enable three-port multi-frequency power transfer. This will be verified by simulation results.

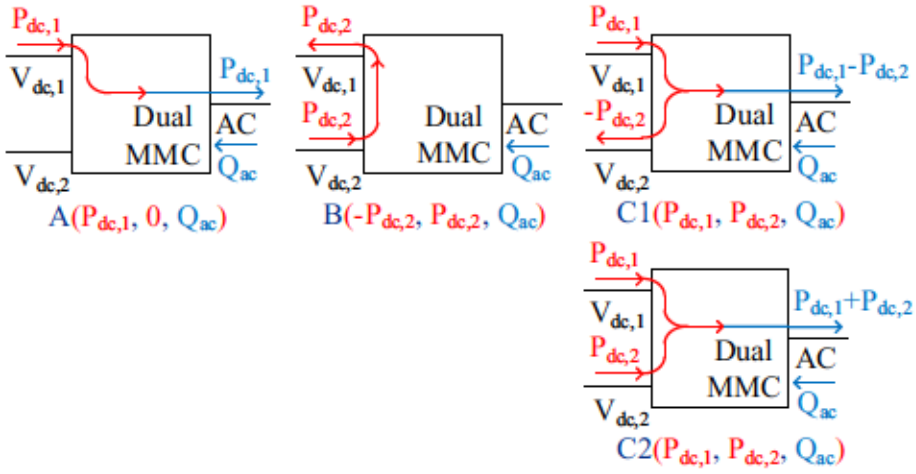

Figure 4.5: Three-port MMC power flow scenarios under study

Table 4.1: Notation for Port Power Flow Scenarios in Fig. 4.5

Scenario	Port power flow notation
Pure dc-ac power transfer	A($P_{dc,1}$, 0, Q_{ac})
Pure dc-dc power transfer	B(-$P_{dc,2}$, $P_{dc,2}$, Q_{ac})
Multi-frequency power transfer	C1($P_{dc,1}$, $P_{dc,2}$, Q_{ac})
Multi-frequency power transfer	C2($P_{dc,1}$, $P_{dc,2}$, Q_{ac})

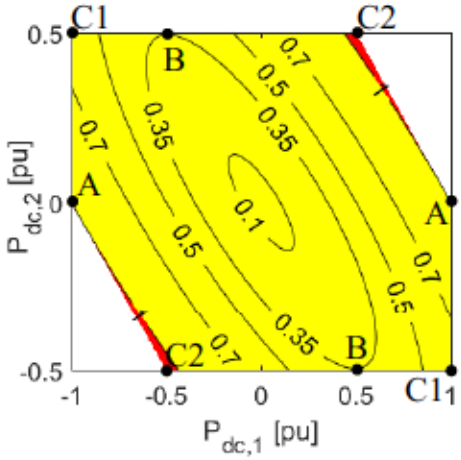

Figure 4.6: Calculated transformer center-tapped rms winding current for all possible port power transfers; The rms current is normalized to rated rms current of an ac transformer used in conventional dc-ac MMC with the same power rating

4.4 Simulation Results

The operating principle and proposed dynamic controls for the three-port MMC in Fig. 4.3 is verified by PSCAD/EMTDC simulations. Simulations are conducted using a detailed equivalent switching model. Voltage balancing of capacitors within each arm is achieved using the sort and selection method. The three-port MMC in Fig. 4.3 is designed to interface a 400 kV/200 kV three-port MVDC system with a 345 kV HVAC system. Simulation parameters are given in Table 4.2. The parameters for the controllers are selected to give settling times of around 150 msec for ac and dc power demands and within 100 msec for the capacitor voltages ΣV_c and ΔV_c. The SM capacitor voltage (V_c^{ref}) is rated at 2 kV with half-bridge configuration. The well known SM capacitor voltage sort and selection algorithm ensures voltage balancing amongst individual capacitors within each arm. The three-winding transformer used in three-port MMC is rated at 1200MW×1.06 based on analysis in Section 4.3 to enable three-port power transfer. The secondary center-tapped winding voltages of

the transformer used in 400 kV/200 kV three-port MMCs are rated for 127.3 kV_{rms}. The arm reactor has a value of around 10% on the system impedance base so that the voltage required to control output current is less than 10%. Note that the arm chokes in s arms are identical to that in p arms even that the current distribution in each arm are not the same for all power flow scenarios. The SM capacitances are picked to yield peak-to-peak capacitor voltage ripples of around 18% for the primary and secondary arms. The fundamental frequency is 60 Hz.

Table 4.2: Simulation Parameters for Three-port MMC in Fig. 4.3

Converter Parameters	400kV/200kV three-port MMC
Rated power	1200 MW
$V_{dc,1}/V_{dc,2}$	400 kV/200 kV
Number of SMs per arm, N_p, N_s	200 (HBSM)
SM capacitor voltage, V_c^{ref}	2 kV
SM capacitance, C_{sm}	7 mF
Arm inductance, L_a	40 mH
Fundamental frequency, f	60 Hz
Transformer parameters	**Value**
Power rating, S_w	1272 MVA[3]
Turns ratio, n	0.738
Primary winding voltages, V_p	345 kV_{rms}
Secondary winding voltages, V_s	127.3 kV_{rms}
Leakage reactance	10%
Magnetizing current	1%
Controller parameters	**Value**
$K_{p,p}$, $K_{i,p}$	0.00015, 0.21
$K_{p,v\Sigma}$, $K_{i,v\Sigma}$	$5.5e^{-4}$, $4e^{-3}$
$K_{p,v\Delta}$, $K_{i,v\Delta}$	0.02, 2
$K_{p,i\Sigma}$, $K_{r,i\Sigma}$, $K_{2r,i\Sigma}$	1, 3, 200
$K_{p,i\Delta}$, $K_{r,i\Delta}$, $K_{2r,i\Delta}$	2, 50, 90
$K_{p,i1}$, $K_{i,i1}$	$1.6e^{-5}$, $7.7e^{-5}$
$K_{p,i2}$, $K_{i,i2}$	0.01, 0.4
ΣV_c^{ref}, ΔV_c^{ref}	2400 kV, 0 kV
ω_1, ω_2	377 rad/s, 754 rad/s

Figs. 4.7 and 4.11 show the dynamic response waveforms considering six different combinations of port power flows scenarios for a 400 kV/200 kV three-port MMC with a 345 kV MVAC system: i) dc and ac port power injections, ii) dc port currents,

[3]The transformer in the 400 kV/200 kV three-port MMC is rated at 1272 MVA to enable three-port operation, which would be $\times 1.06$ p.u. as a grid interfacing transformer for conventional dc-ac MMC (see Fig. 4.6)

iii) exemplar primary and secondary arm currents in two MMCs, iv) exemplar SM capacitor voltages in two MMCs and v) transformer winding currents in phase a are plotted. The port power flow notation from Table 4.1 is used in describing the scenarios. In Fig. 4.7, from $t = 0$ to $t = 0.1$ sec, 1200 MW power is transferred from $V_{dc,1}$ to the ac grid at unity power factor. This is power flow scenario A(1, 0, 0). From $t = 0.1$ to $t = 0.5$ sec, 1200 MW power is still transferred from $V_{dc,1}$ but now splits equally between $V_{dc,2}$ and the ac grid (unity power factor). This is power flow scenario $C1$(1, -0.5, 0). Starting at $t = 0.5$ sec, 600 MW power is transferred from $V_{dc,1}$ to $V_{dc,2}$ while 300 MVar reactive power is consumed by the ac grid. This is power flow scenario B(0.5, -0.5, -0.25).

In Fig. 4.11, from $t = 0$ to $t = 0.1$ sec, 600 MW power is transferred from $V_{dc,2}$ to $V_{dc,1}$. This is power flow scenario B(-0.5, 0.5, 0). From $t = 0.1$ to $t = 0.5$ sec, 900 MW and 300 MW power is transferred from $V_{dc,1}$ and $V_{dc,2}$, respectively, to the ac grid (unity power factor). This is power flow scenario $C2$(0.75, 0.25, 0). Starting at $t = 0.5$ sec, 600 MW power is transferred from $V_{dc,1}$ and $V_{dc,2}$, respectively, to the ac grid (unity power factor). This is power flow scenario $C2$(0.5, 0.5, 0).

Figs. 4.8, 4.9 and 4.10 show steady-state results considering three power flow scenario A(1, 0, 0), $C1$(1, -0.5, 0) and B(0.5, -0.5, -0.25) in Fig. 4.7. Figs. 4.12, 4.13 and 4.14 show steady-state results considering three power flow scenario B(-0.5, 0.5, 0), $C2$(0.75, 0.25, 0) and $C2$(0.5, 0.5, 0) in Fig. 4.11. In all steady-state waveforms: i) dc port currents, ac grid voltage and current in phase a, ii) exemplar primary and secondary arm currents in two MMCs, iii) exemplar SM capacitor voltages in two MMCs and iv) transformer winding currents in phase a are plotted.

Simulation results validate that primary dc current $i_{dc,1}$ and secondary dc current $i_{dc,2}$ are dominantly dc valued as expected due to three-phase fundamental and second harmonic ac currents cancellation at primary and secondary dc rails. The capacitor voltages $v_{c,a1,p}$, $v_{c,a1,s}$ (primary and secondary arms of phase a in MMC1) and $v_{c,a2,p}$, $v_{c,a2,s}$ (primary and secondary arms of phase a in MMC2) remain well regulated in the three power flow scenarios and during the step change in power flows. The SM peak-to-peak capacitor voltage ripples is below 18% for the primary and secondary arms in all three scenarios. The $i_{a1,p}$ and $i_{a1,s}$ (p and s arm currents in MMC1) and $i_{a2,p}$ and $i_{a2,s}$ (p and s arm currents in MMC2) waveforms verify the total power transfer is shared equally between two MMCs all power flow scenarios, as each MMC carries the same average current. For example, the three-port MMC operates as a single-stage dc-dc converter during B(-0.5, 0.5, 0) in Fig. 4.12, where $i_{a,trans,a1}$ and $i_{a,trans,a2}$ have identical dc component. This ensures transformer core dc flux cancellation is achieved owing to the center-tap windings arrangement. This can also be seen with

the transformer winding currents at grid side in phase a $i_{a,trans,g}$. $i_{a,trans,g}$ that only contains ac component at all time verify the total power transfer is shared equally between MMCs, yielding dc flux cancellation within the core during step-changes in power flow demands.

In Fig. 4.7, although same amount of power is transferred from dc port $V_{dc,1}$ (1200 MW), the power processed by the three-port MMC is different in two scenarios A(1, 0, 0) and $C1$(1, -0.5, 0). The primary arm currents have identical values in both scenarios, see $i_{a1,p}$ and $i_{a2,p}$. On the other hand, the secondary arm SM capacitor voltage $V_{c,a1,p}$ and $V_{c,a1,s}$ becomes nearly dc valued from $t = 0.1$ to $t = 0.5$ sec in Fig. 4.7, as during this operating condition ($C1$(1, -0.5, 0)) the secondary arms do not carry any current, see $i_{a1,s}$ and $i_{a2,s}$. This is an interesting observation and will be discussed in Chapter 4.

The transformer in the 400 kV/ 200 kV three-port MMC is rated at 1272 MVA to enable three-port operation ($\{P_{dc,1}, P_{ac}, Q_{ac}\} \in (-1, 1)$ p.u. and $\{P_{dc,2}\} \in (-0.5, 0.5)$ p.u), which would be $\times 1.06$ p.u. as a grid interfacing transformer for conventional dc-ac MMC. This can be seen with the transformer winding rms currents in phase a. The rms value of the winding current $i_{a,trans,a1(rms)}$ is the highest during multi-frequency power transfer conversion ($C2$(0.5, 0.5, 0) in Fig. 4.14), and decreases in all other power flow scenarios (see Table 4.3).

Table 4.3: Transformer Winding RMS Currents in Phase A $i_{a,trans,a1(rms)}$

Scenario	$i_{a,trans,a1(rms)}$ (kA)
Pure dc-ac power transfer A(1, 0, 0)	1.57
Pure dc-dc power transfer B(-0.5, 0.5, 0)	0.5
Multi-frequency power transfer $C1$(1, -0.5, 0)	0.93
Multi-frequency power transfer $C2$(0.75, 0.25, 0)	1.59
Multi-frequency power transfer $C2$(0.5, 0.5, 0)	1.66

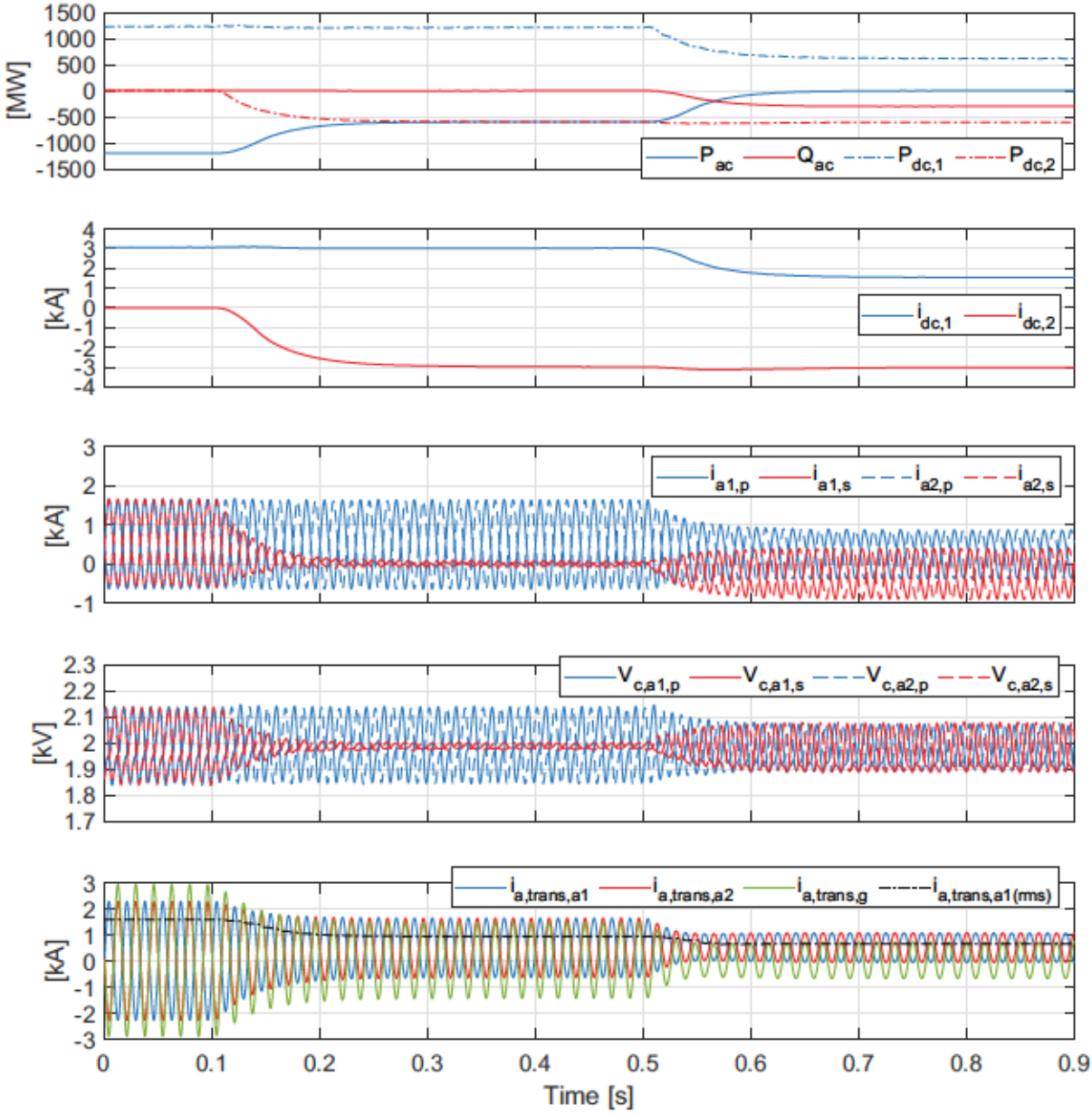

Figure 4.7: PSCAD waveforms of proposed 400 kV/ 200 kV three-port MMC are shown in subplots for (i) $A(1, 0, 0)$ from $t = 0$ to 0.1 sec; (ii) $C1(1, -0.5, 0)$ from $t = 0.1$ to 0.5 sec; and (iii) $B(0.5, -0.5, -0.25)$ from $t = 0.5$ to 0.9 sec

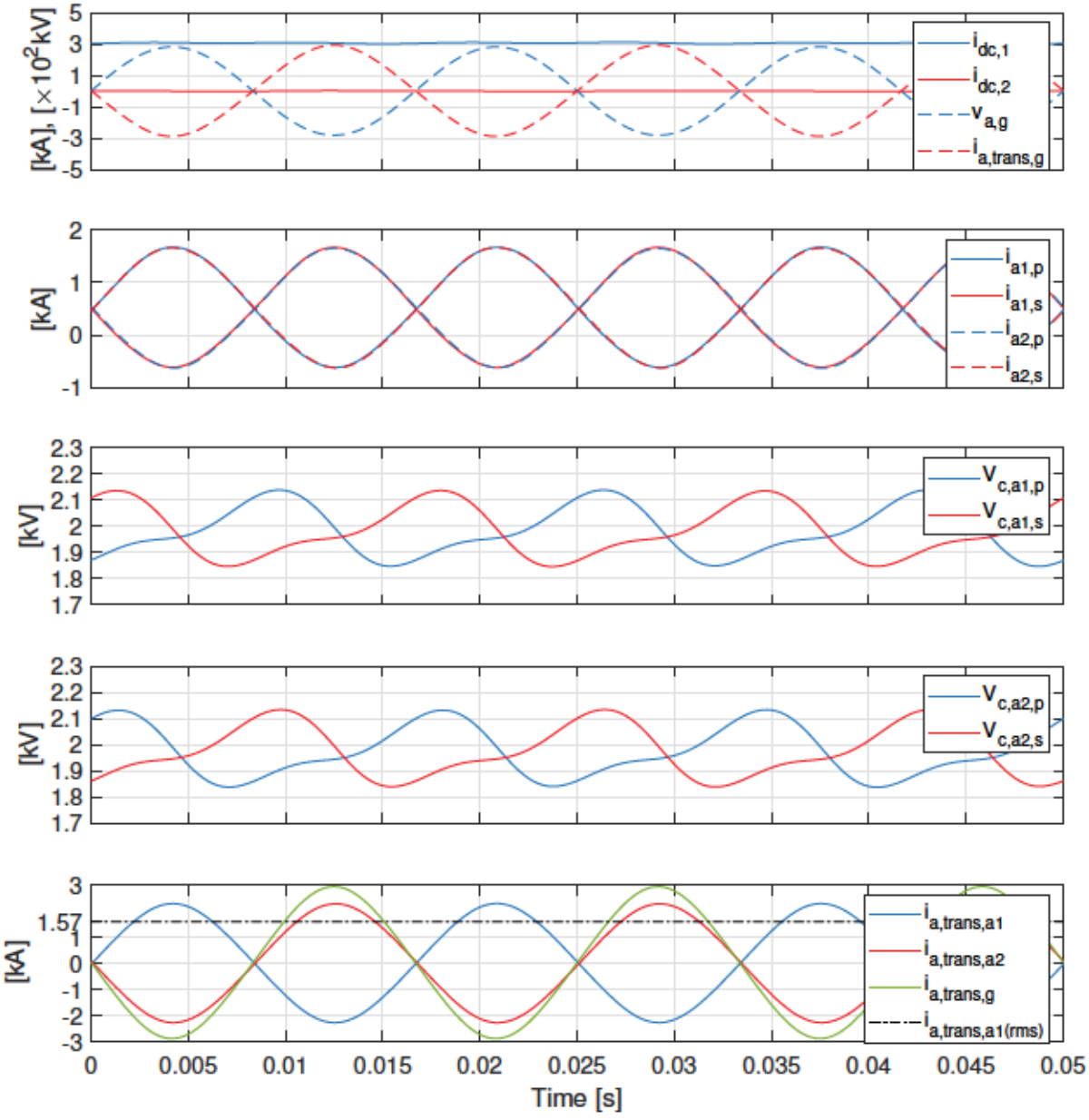

Figure 4.8: PSCAD steady-state waveforms of 400 kV/ 200 kV three-port MMC are shown in subplots for $A(1, 0, 0)$

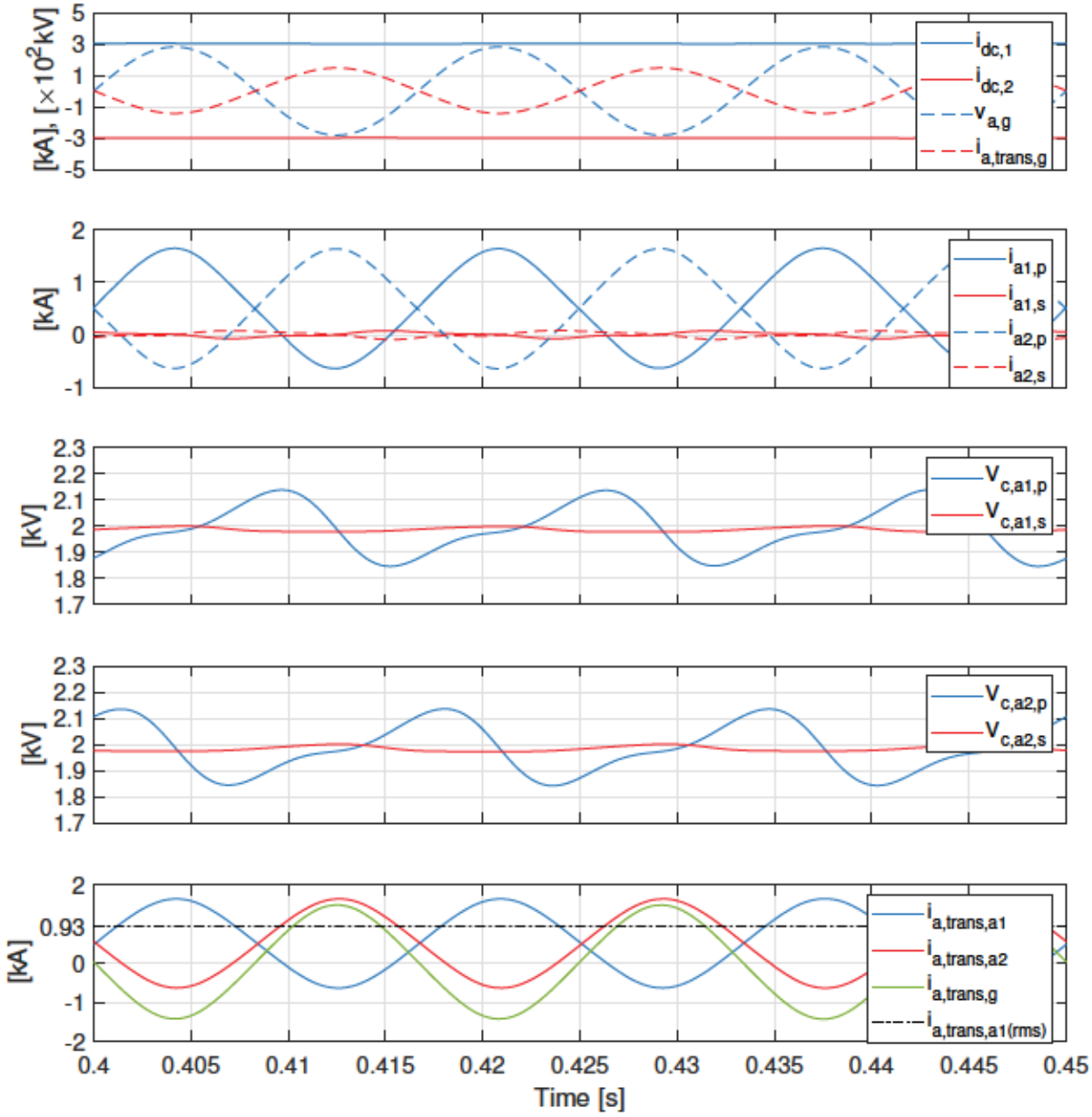

Figure 4.9: PSCAD steady-state waveforms of 400 kV/ 200 kV three-port MMC are shown in subplots for $C1(1, -0.5, 0)$

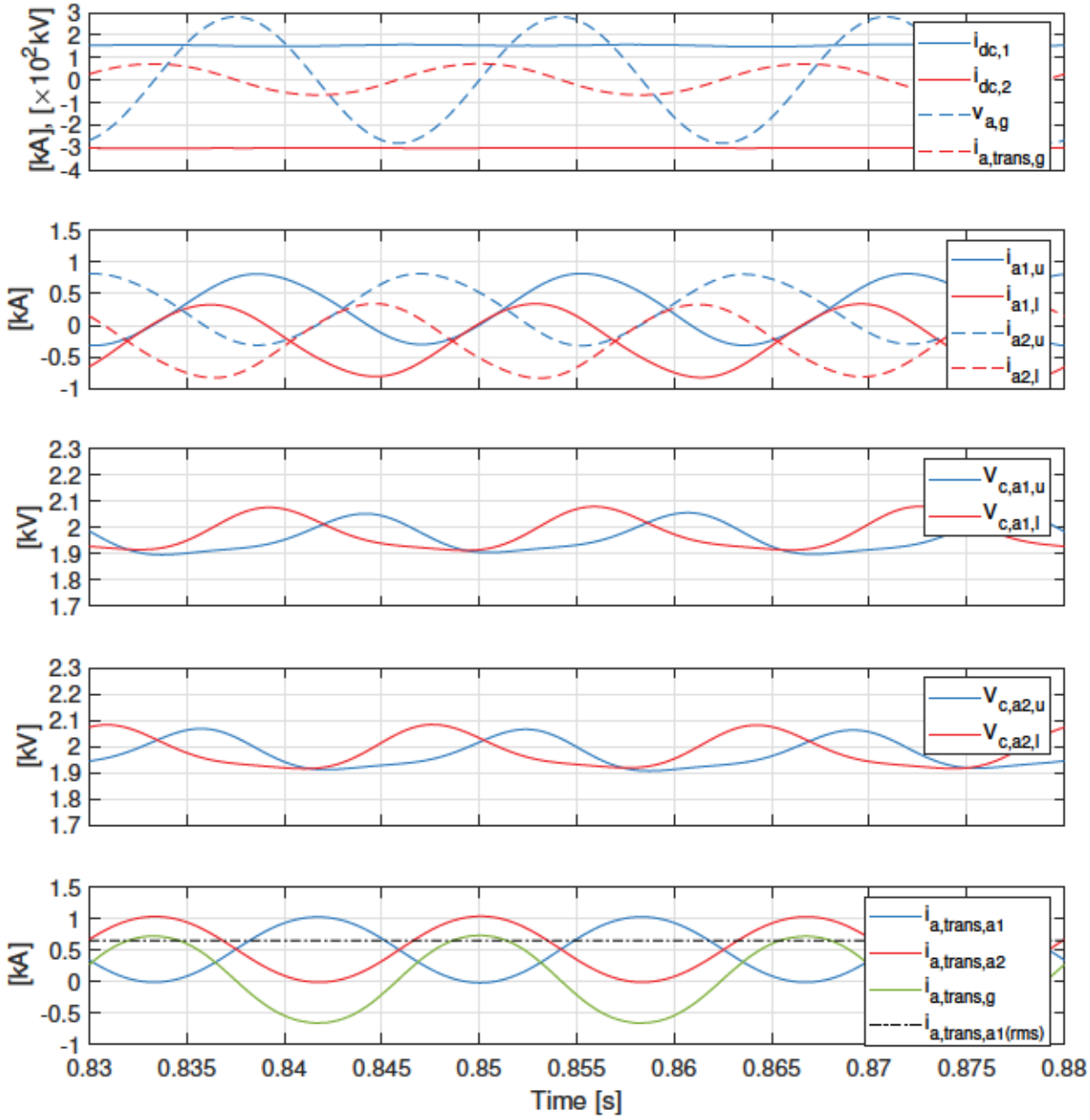

Figure 4.10: PSCAD steady-state waveforms of 400 kV/ 200 kV three-port MMC are shown in subplots for B(0.5, -0.5, -0.25)

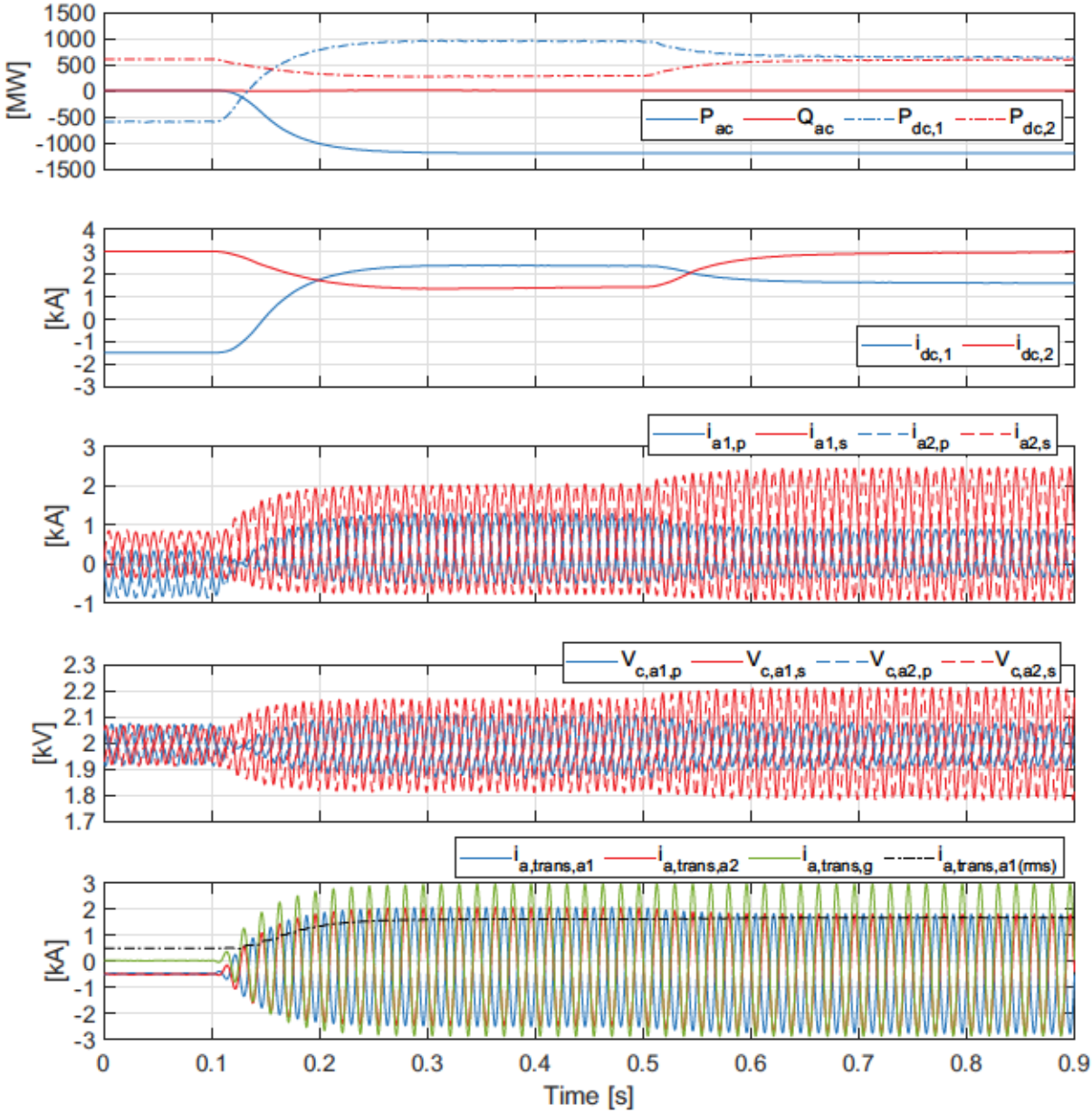

Figure 4.11: PSCAD waveforms of 400 kV/ 200 kV three-port MMC are shown in subplots for (i) B(-0.5, 0.5, 0) from $t = 0$ to 0.1 sec; (ii) $C2$(0.75, 0.25, 0) from $t = 0.1$ to 0.5 sec; and (iii) $C2$(0.5, 0.5, 0) from $t = 0.5$ to 0.9 sec

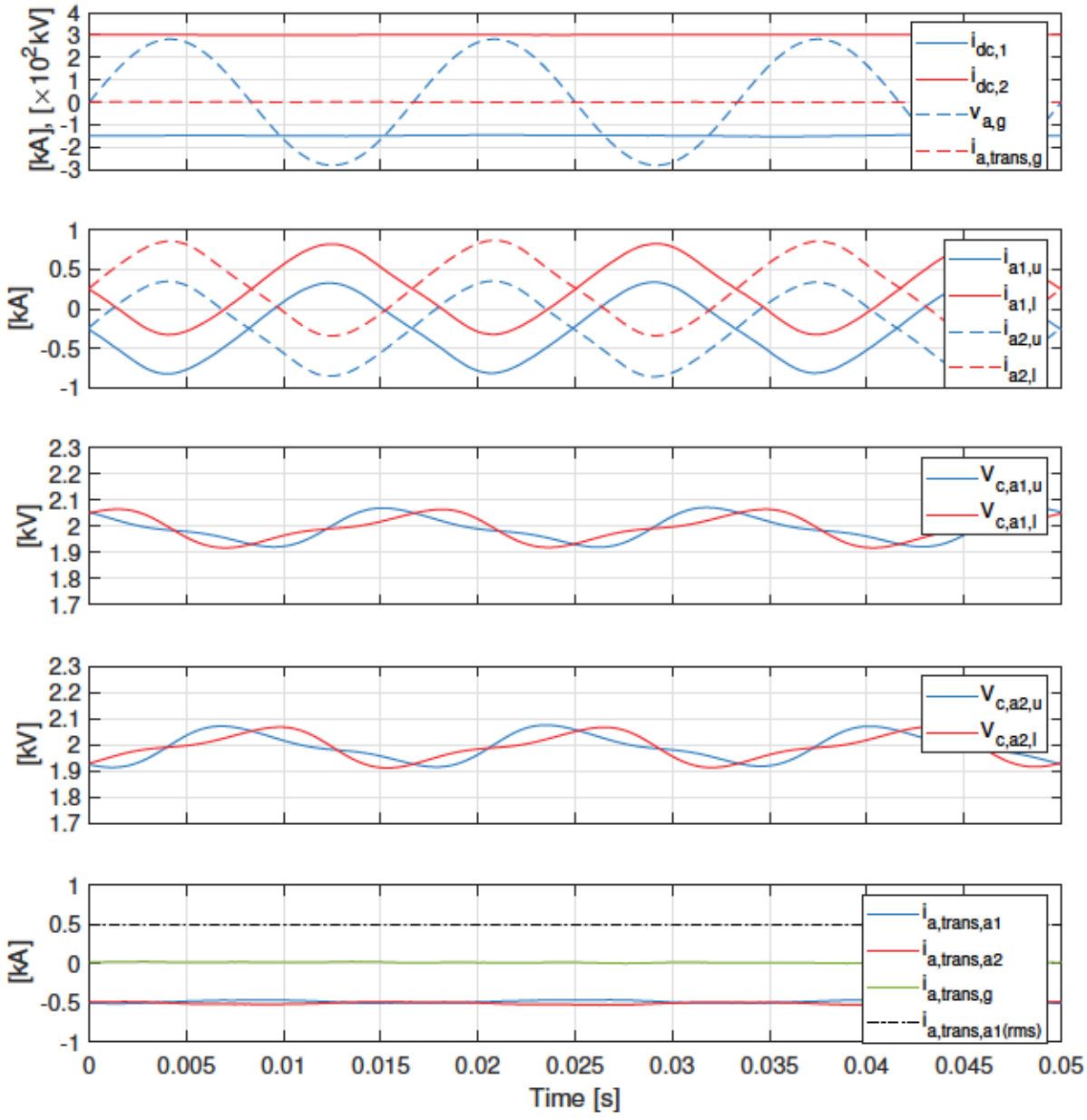

Figure 4.12: PSCAD steady-state waveforms of 400 kV/ 200 kV three-port MMC are shown in subplots for B(-0.5, 0.5, 0)

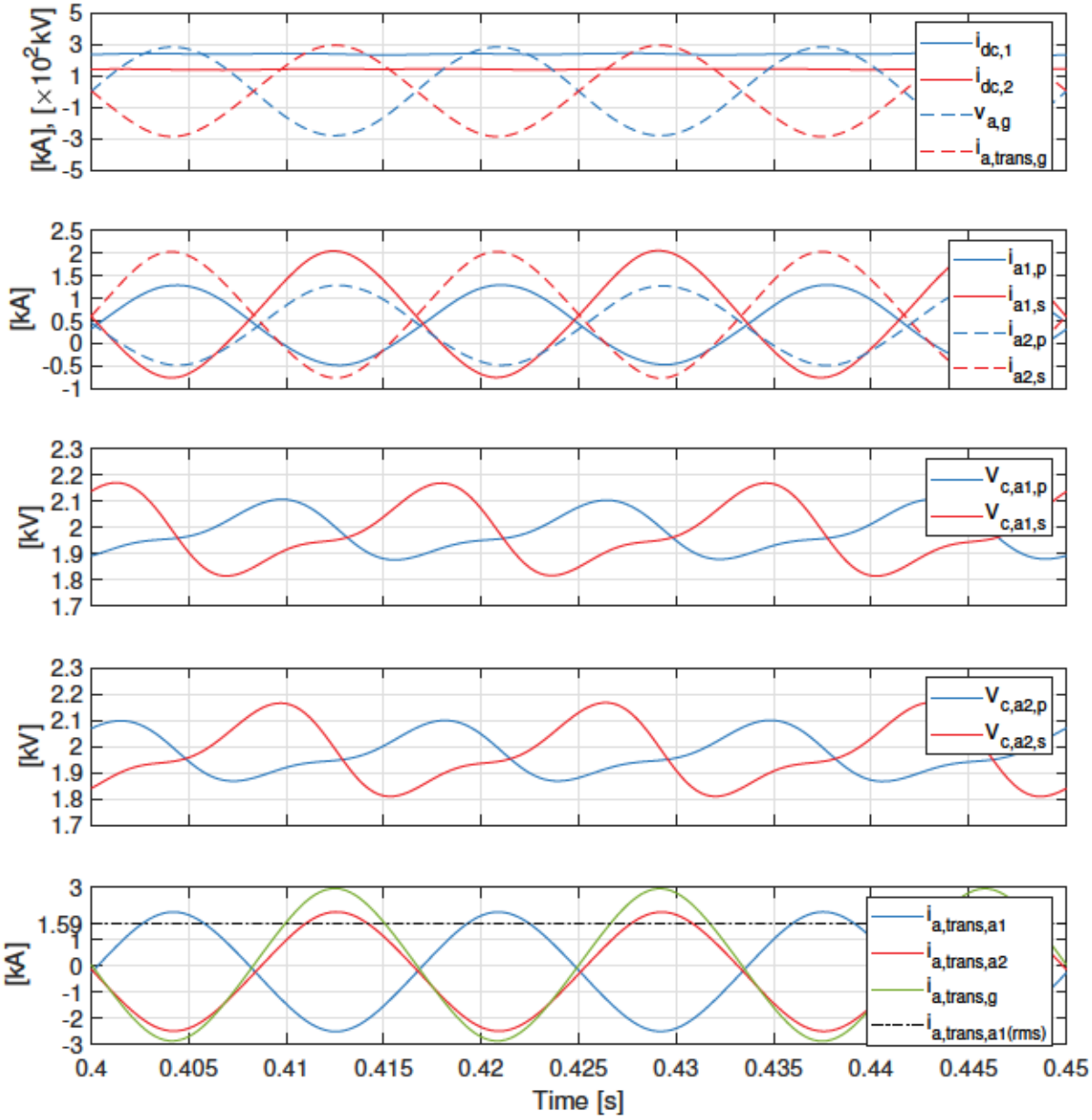

Figure 4.13: PSCAD steady-state waveforms of 400 kV/ 200 kV three-port MMC are shown in subplots for $C2(0.75, 0.25, 0)$

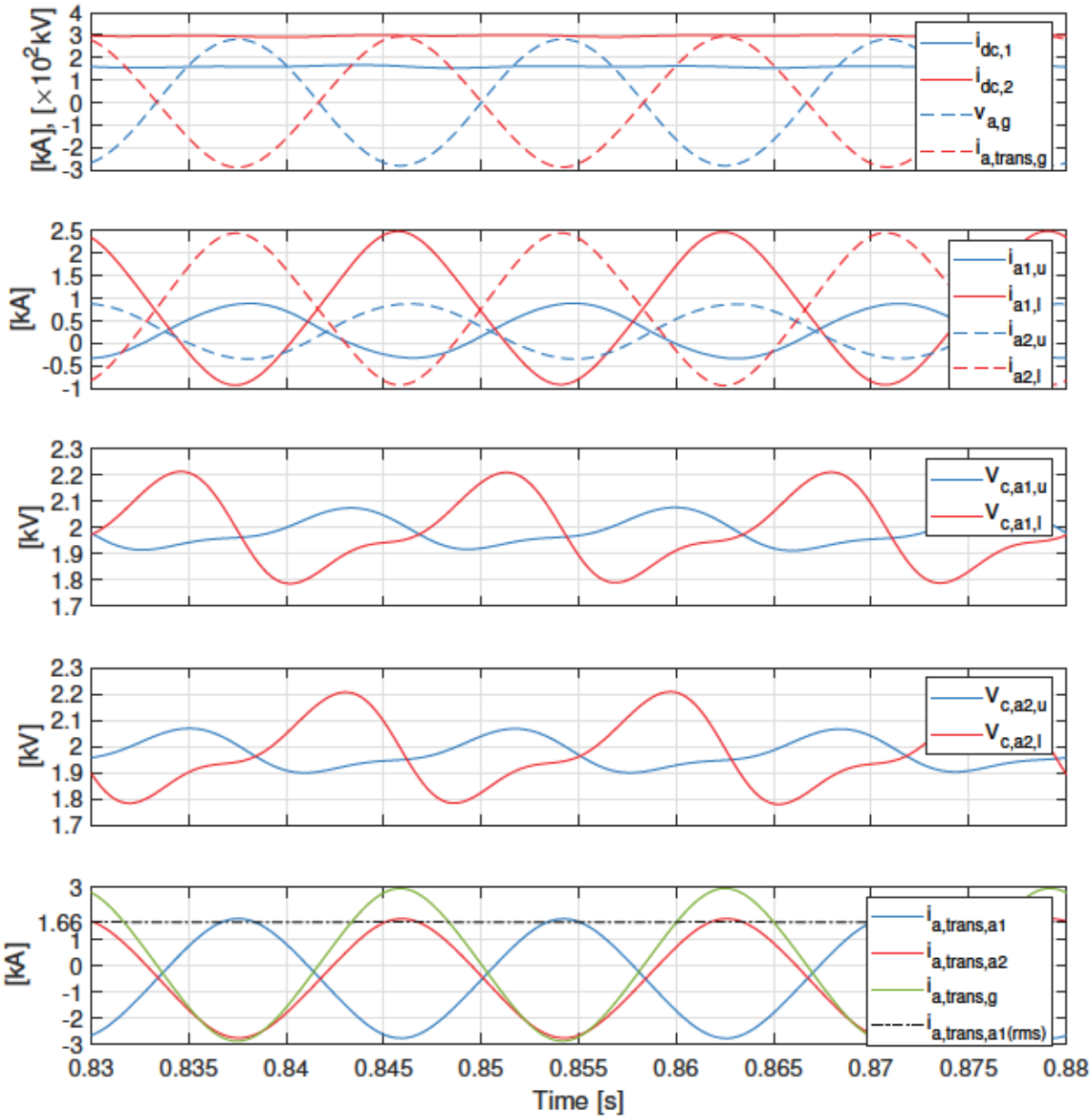

Figure 4.14: PSCAD steady-state waveforms of 400 kV/ 200 kV three-port MMC are shown in subplots for $C2(0.5, 0.5, 0)$

4.5 Fault Blocking Implications

Simulation case studies are presented in this section to validate the external fault blocking capability for the proposed three-port MMC in Fig. 4.3 by employing FBSMs. The fault blocking capability can also be enabled by employing FBSMs for the bipolar dual MMC in Chapter 3. Simulations are conducted using a detailed equivalent switching model.

When a pole-to-ground dc fault occurs in a three-port MMC, the fault current path not only comes from the healthy dc port, the ac grid also feeds the dc fault. Hence, with the addition of the grid-side winding, the three-port MMC-based on F2F-MMC[4] in Fig. 4.1a loses dc fault blocking capability. All five topologies in Fig. 4.1 need enough FBSMs to block faults at the dc ports. The three-port MMCs can block ac grid phase-to-ground fault with only HBSMs. Thus, three case studies are preformed in this section:

- DC_1 pole-to-ground fault[5]
- DC_2 pole-to-ground fault
- AC grid phase-to-ground fault[6]

Simulation parameters are the same as simulation cases in Section 4.4 given in Table 4.2, except for the SM type. Table 4.4 summarizes the arm voltage requirements of the three-port MMC in Fig. 4.3 to achieve fault blocking on all ports. The red text indicates FBSMs are necessary for the required arm voltage generation. Therefore, the number of FBSMs and HBSMs employed in each arm are given in the Table.

When pole-to-ground fault happens on dc_1, the HBSMs are not applicable to block the fault in this case as the current will feed to the primary dc side through the diodes of SMs in the primary arm. By employing FBSMs in the primary arm, each MMC can generate sufficient negative voltages $v_{a1,p}$ and $v_{a2,p}$ as shown in Fig. 4.15 to block the dc currents flowing into the faulty line. The secondary arm $v_{a1,s}$ and $v_{a2,s}$ only need to generate positive voltages. Following the fault all switched are blocked and arm currents $i_{a1,p}$, $i_{a1,s}$, $i_{a2,p}$ and $i_{a2,s}$ are suppressed to zero. The SM capacitor voltages shown in Fig. 4.15 are kept constant during the fault as power transfer between dc and ac ports is interrupted.

[4]The dc-dc F2F-MMC inherently offers bidirectional fault blocking due to the galvanic separation property of the intermediate ac transformer

[5]MMC with FBSMs not only can block the dc fault ($V_{dc,1} = 0$ or $V_{dc,2} = 0$), but also can continue operating under the reduced dc voltage to regulate its output current to the ac side, for example, to support the healthy ac grid and provide fast fault recovery and system restart [108]

[6]Control strategies for riding through less severe asymmetric ac faults can be found in [109, 110]

Table 4.4: v_{arm} Generation Requirements and Submodule Requirements for Three-port Dual MMC of Fig. 4.3 to Ensure Fault Blocking on All Ports (Red Text Denotes FBSMs)

	[min, max] voltage injection required
v_p	$[-V_{dc,s} - \hat{v}_p,\ V_{dc,p} + \hat{v}_p]$
v_s	$[-\hat{v}_s,\ \frac{1}{2}V_{dc,s} + \hat{v}_s]$
	HBSMs and FBSMs required
$N_{HB,p}$	100
$N_{FB,p}$	200
$N_{HB,s}$	100
$N_{FB,s}$	100

When pole-to-ground fault happens on dc_2, the HBSMs are not applicable to block the fault in this case as the current will feed to the secondary dc side through the diodes of SMs in the secondary arm. By employing FBSMs in the secondary arm, each MMC can generate negative voltages $v_{a1,s}$ and $v_{a2,s}$ as shown in Fig. 4.16 to block the dc currents flowing into the faulty line.

When phase-to-ground (phase a) fault happens on ac grid, the control system of three-port MMC is capable of controlling the current flow similar to ac port fault in conventional dc-ac MMC. Both the primary and secondary arms need to generate positive voltages as shown in Fig. 4.17. Thus, three-port MMC with HBSMs is sufficient to block the phase-to-ground fault happens on ac grid.

It is worth mentioning that SMs are all blocked in the aforementioned cases to interrupt the fault current. The proposed three-port MMC with FBSMs is also able to ride-through the external faults by adopting appropriate fault ride-through strategies, e.g., [83, 111].

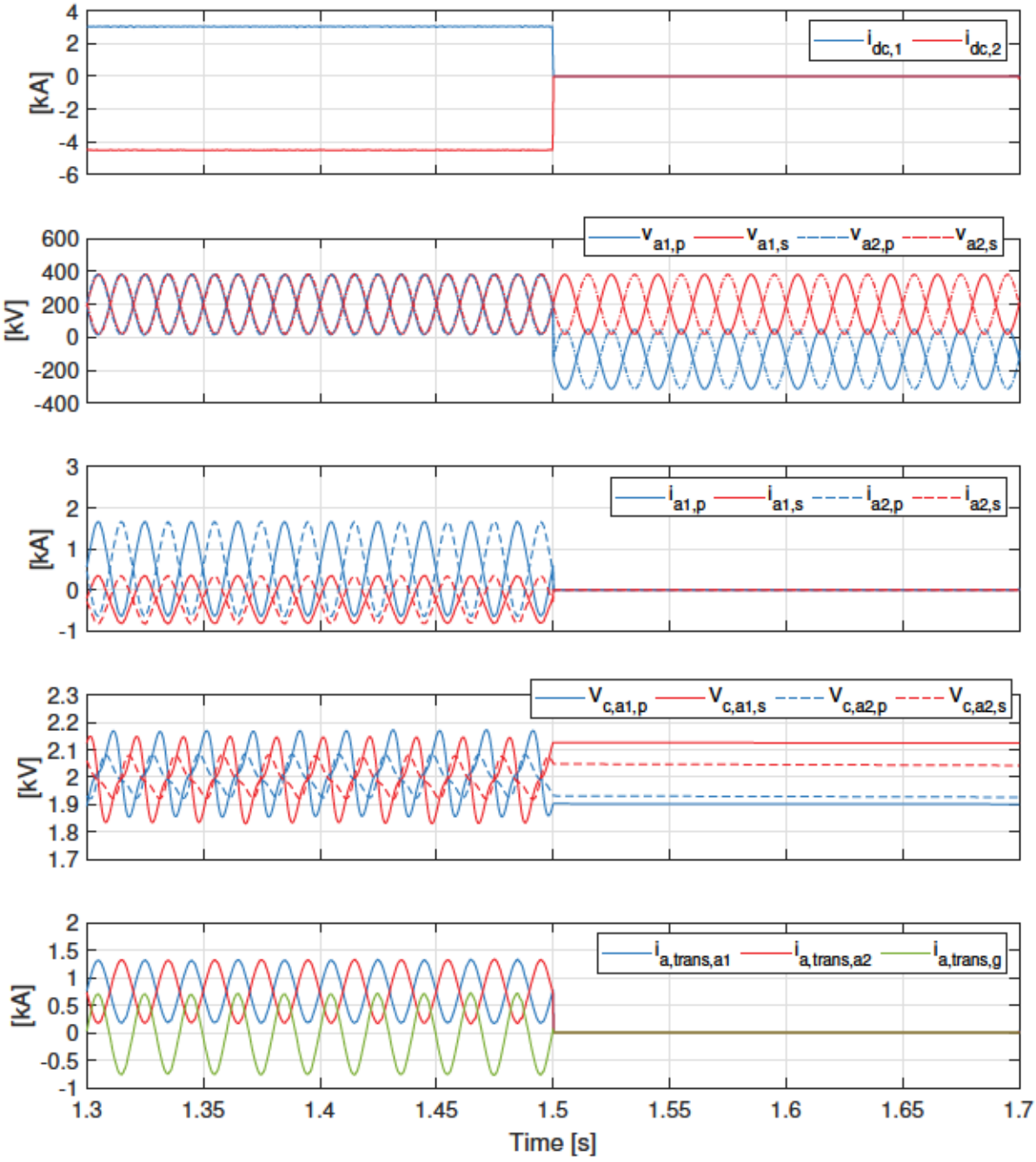

Figure 4.15: Simulation result for dc pole dc_1: 400 kV to ground fault when three-port MMC is equipped with sufficient FBSMs in the arms (blocking action)

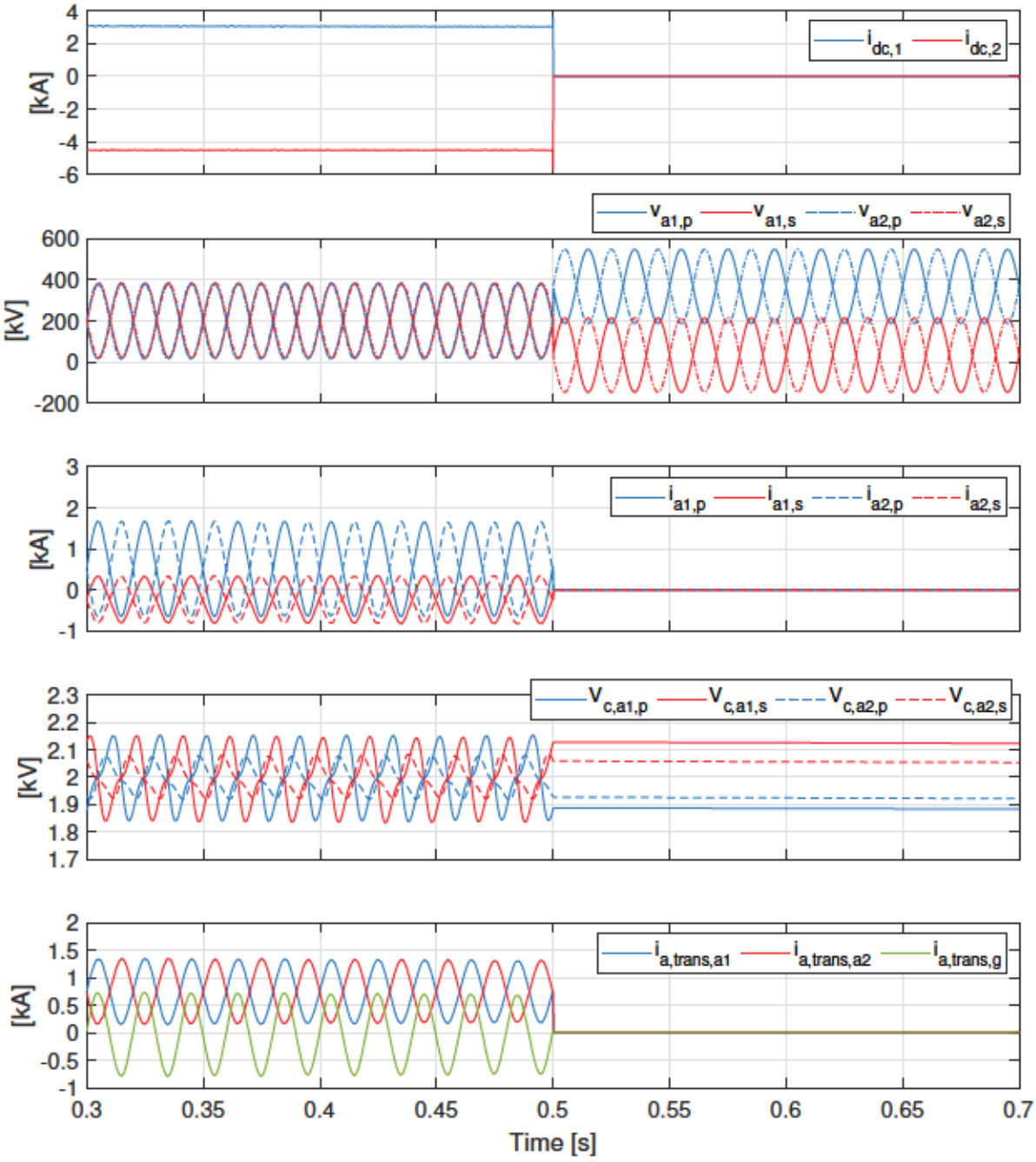

Figure 4.16: Simulation result for dc pole dc_2: 200 kV to ground fault when three-port MMC is equipped with sufficient FBSMs in the arms (blocking action)

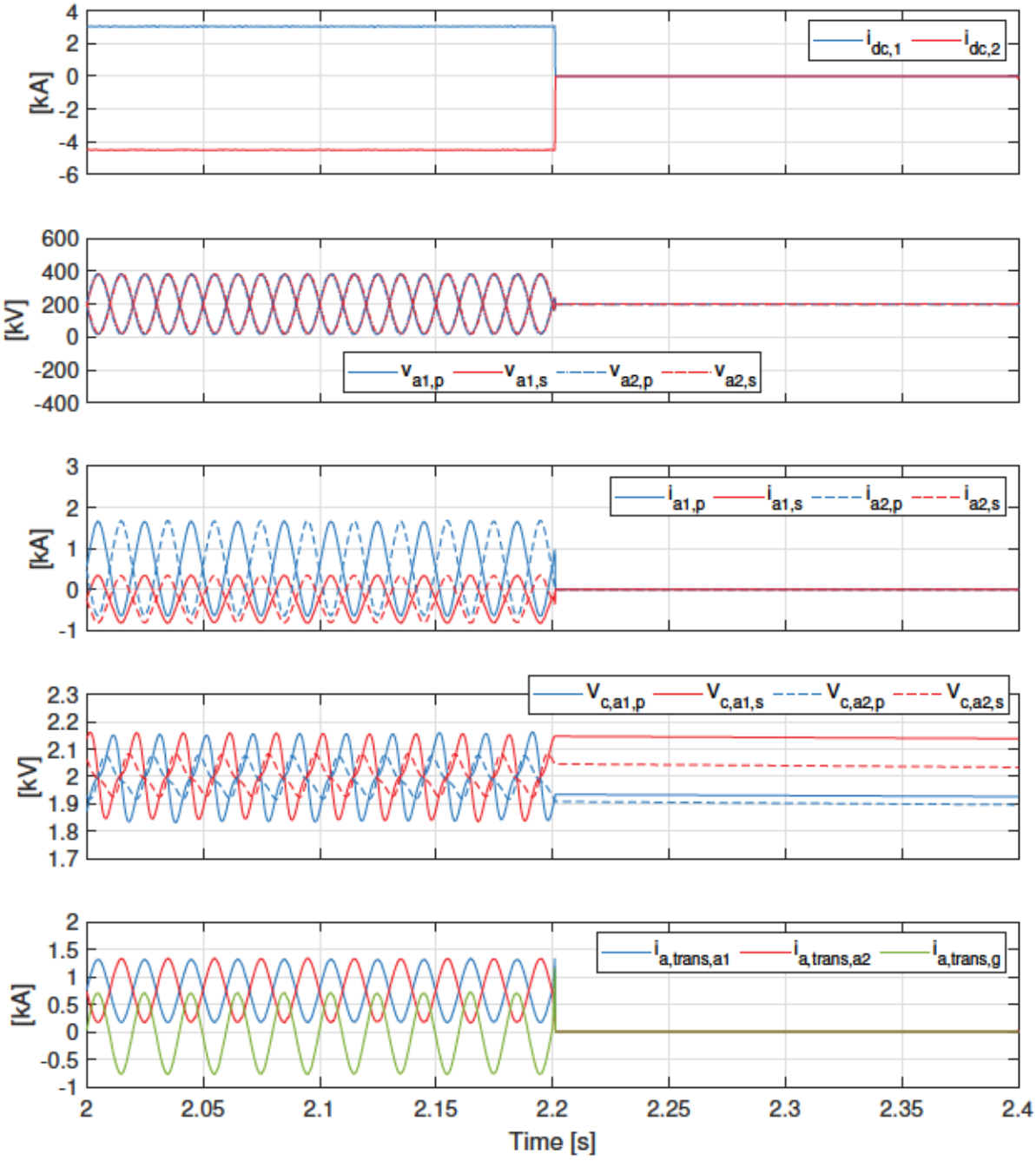

Figure 4.17: Simulation result for ac grid: phase a to ground fault when three-port MMC is equipped with sufficient FBSMs in the arms (blocking action)

4.6 Experimental Results

Experimental results are presented for a scaled-down 170 V/85 V, 3.4 kW laboratory prototype of the three-port MMC structure. The experimental setup allows bidirectional power flow on all ports. The operating principle and dynamic controls for the three-port MMCs are validated. The experimental setup is shown in Fig. 3.19 and parameters are given in Table 4.5.

Table 4.5: Experimental Parameters for Three-port MMC in Fig. 4.3

Converter Parameters	Value
Rated power	3.4 kW
$V_{dc,1}/V_{dc,2}$	170 V/85 V
Number of SMs per arm, N_u, N_l	2 (HBSM)
SM capacitor voltage, V_c^{ref}	85 V
SM capacitance, C_{sm}	5 mF
Arm inductance, L_a	2.5 mH
Fundamental frequency, f	60 Hz
Transformer parameters	**Value**
Transformer model	Hammond 1182T60P
Power rating, S_w	4.5 kVA
Turns ratio, n	1.026
Primary/Secondary winding voltages, V_p/V_s	117 V/ 60 V (rms)
Leakage inductance L_x	0.085 mH
Magnetizing inductance L_m	1.516 H
Controller parameters	**Value**
SPWM carrier frequency, f_{sw}	10 kHz
Sample frequency, f_{sample}	25 kHz
$K_{p,p}$, $K_{i,p}$	0.3, 20
$K_{p,v\Sigma}$, $K_{i,v\Sigma}$	0.001, 0.01
$K_{p,v\Delta}$, $K_{i,v\Delta}$	0.1, 2
$K_{p,i\Sigma}$, $K_{r,i\Sigma}$, $K_{2r,i\Sigma}$	0.1, 0.5, 5
$K_{p,i\Delta}$, $K_{r,i\Delta}$, $K_{2r,i\Delta}$	0.2, 0.5, 5
$K_{p,i1}$, $K_{i,i1}$	0.003, 0.08
$K_{p,i2}$, $K_{i,i2}$	0.003, 0.02
ΣV_{cap}^{ref}, ΔV_{cap}^{ref}	1020 V, 0 V
ω_1, ω_2	377 rad/s, 754 rad/s

The controller parameters for the experimental 170V/85V three-port MMC in Fig. 4.2b are identical to that for the experimental $\pm$ 85V bipolar MMC in Fig. 4.2a. The unified control scheme in Fig. 3.12 with appropriate reference signals in 4.4 are implemented on a real-time controller platform from Imperix. Each arm uses two half-bridge SMs with $V_c^{ref} = 85$ V. The SM capacitor voltage sort and selection al-

gorithm ensures voltage balancing amongst individual capacitors within each arm. The parameters for the controllers are selected to give settling times of around 150 msec for ac and dc power demands and within 200 msec for the capacitor voltages. The band-pass filter introduced in Section 3.6.1 is implemented for all experimental scenarios for the three-port MMC. Three single-phase 1.5 kVA center-tapped transformers with n = 1.026 (4.5 kVA for three-phase) are used. The maximum power rating of the dual MMC setup is 3.4 kW due to power supply limitation. The port power flow notation from Table 4.1 is used.

4.6.1 Steady-State Performance

Six power flow scenarios as shown in Fig. 4.18 are used to demonstrate the capabilities of the proposed three-port MMC with unified control scheme in Fig. 3.12 with modified power control loop in 4.4. Experimental waveforms of three-port MMC for six steady-state power flow scenarios are shown in Figs. 4.19-4.24.

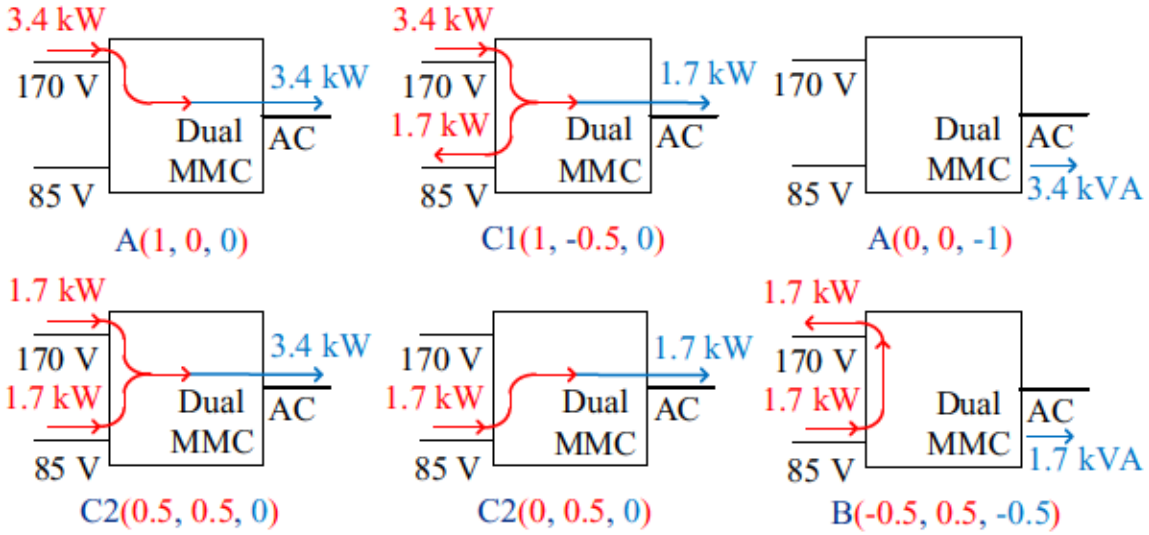

Figure 4.18: Experimental three-port MMC steady-state power flow scenarios under study

In scenario $A(1,\ 0,\ 0)$ (ref. Fig. 4.19), only dc port 1 delivers 1.7 kW to the ac grid, i.e. $P_{dc,1} = 3.4$ kW, and thus $P_{ac} = -3.4$ kW. The grid reactive power injection is set to zero. With dc port voltages $V_{dc,1} = 170$ V, this rated power transfer results in 20 A_{dc} current for dc port 1 $i_{dc,1}$ as shown in Fig. 4.19. The grid voltage $v_{a,g}$ and grid current $i_{a,g}$ have opposite phases to denote the grid absorbing real power. The capacitor voltages (representative waveforms shown for primary and secondary arms of phase a in MMC1) are well balanced. All four SM capacitor voltages of phase

a in MMC1 (two in the primary arm and two in the secondary arm) are shown in Fig. 4.19. It can be seen that the SM capacitor voltage sort and selection algorithm ensures voltage balancing within each arm. The center-tapped transformer winding in Fig. 4.19 carries only ac current as expected, while the arm currents have dc and fundamental frequency parts.

Fig. 4.20 shows steady-state results for power flow scenarios $C1$(1, -0.5, 0), where the power delivered from dc port 1 split equally between dc port 2 and the ac grid. Although same amount of power is transferred from dc port $V_{dc,1}$ (3.4 kW), the power processed by the three-port MMC is different in two scenarios A(1, 0, 0) and $C1$(1, -0.5, 0). The reason is that secondary arm current $i_{a1,s}$ decreases to zero in $C1$(1, -0.5, 0). This indicates that higher efficiency can be achieved when power flow is optimized between the ports in a three-port MMC. On the other hand, the secondary arm SM capacitor voltage $V_{c,a1,p}$ and $V_{c,a1,s}$ becomes nearly dc valued.

Fig. 4.21 shows steady-state results for power flow scenarios A(0, 0, -1), where ac grid consumes 3.4 kVA reactive power. The grid voltage $v_{a,g}$ and grid current $i_{a,g}$ have same phases to denote the grid absorbing reactive power. The arm currents in Fig. 4.21 are identical to that in Fig. 4.19. The SM capacitor voltages in A(0, 0, -1) have a different shape compared with that in A(1, 0, 0) due to phase shift between arm voltage and currents.

Figs. 4.22 and 4.23 show steady-state results for power flow scenarios $C2$(0.5, 0.5, 0) and $C2$(0, 0.5, 0), respectively. These are multi-frequency operating points where the arms process unequal powers. This can be seen with the capacitor voltage waveforms. That is, in Fig. 4.22 the primary arm capacitor voltages have smaller ripple than the secondary arm while in Fig. 4.23 the secondary arm capacitor voltages have negligible ripple given $i_{dc,s} = 0$. In both scenarios, center-tap winding currents at the converter side $i_{trans,a1}$ and $i_{trans,a2}$ contain both dc and ac components. The dc components of $i_{trans,a1}$ and $i_{trans,a2}$ are always kept the same by the controllers. Consequently, the flux produced by dc currents in the core cancel out with each other at the converter side due to windings orientation. The winding current in phase a at the grid side $i_{a,trans,g}$ only has ac component.

In scenario B(-0.5, 0.5, -0.5) (ref. Fig. 4.24), no active power is transferred between two dc systems and ac grid. Dc port 2 delivers 1.7 kW to dc port 1, i.e. $P_{dc,2} = 1.7$ kW, $P_{dc,1} = -1.7$ kW, and thus $P_{ac} = 0$ kW. With dc pole voltages $V_{dc,1} = 170$ V, this rated power transfer results in 20 A_{dc} current for two dc ports $i_{dc,1}$ and $i_{dc,s}$. The center-tap winding currents at the converter side $i_{trans,a1}$ and $i_{trans,a2}$ contain only dc components.

As expected, the rms value of the winding current $i_{a,trans,a1(rms)}$ is the highest

during multi-frequency power transfer conversion ($C2(0.5, 0.5, 0)$ in Fig. 4.22), and decreases in all other power flow scenarios (ref. Table 4.3).

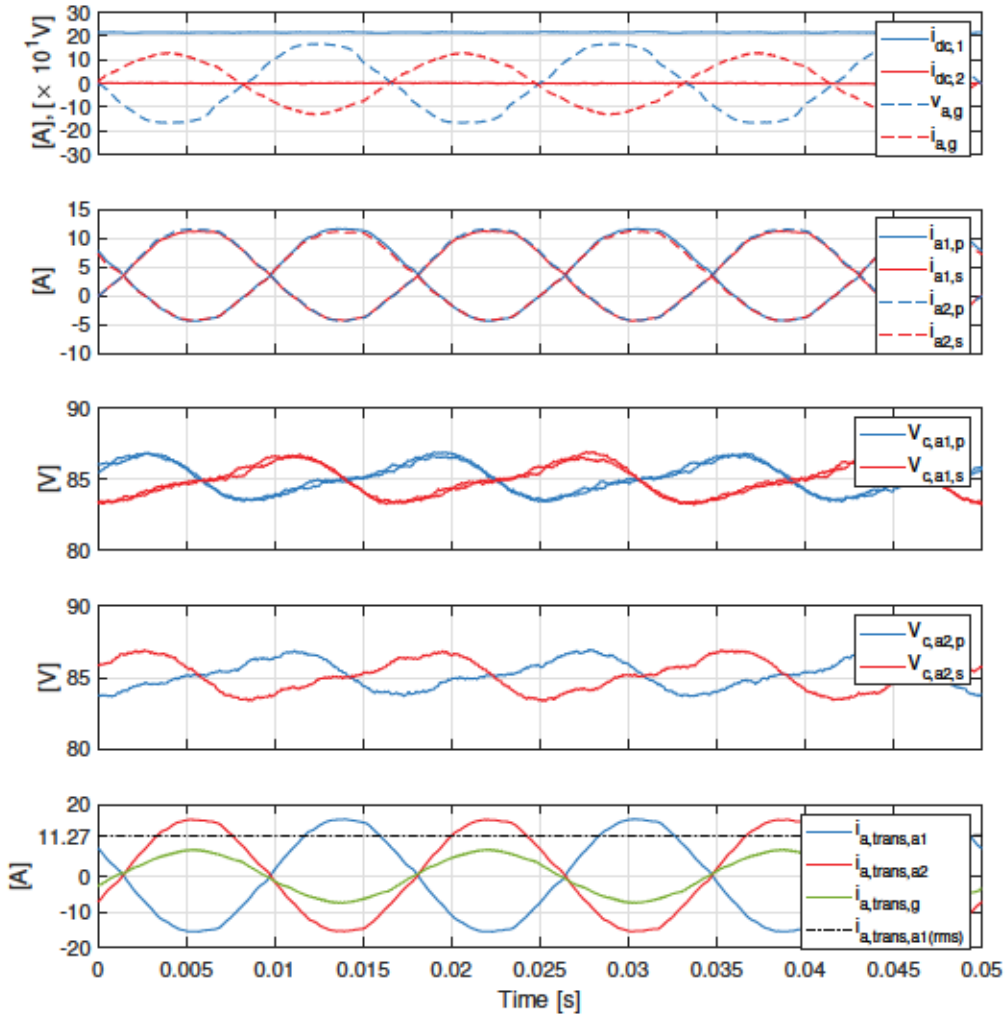

Figure 4.19: Experimental waveforms of three-port MMC for steady-state power flow scenarios: $A(1, 0, 0)$

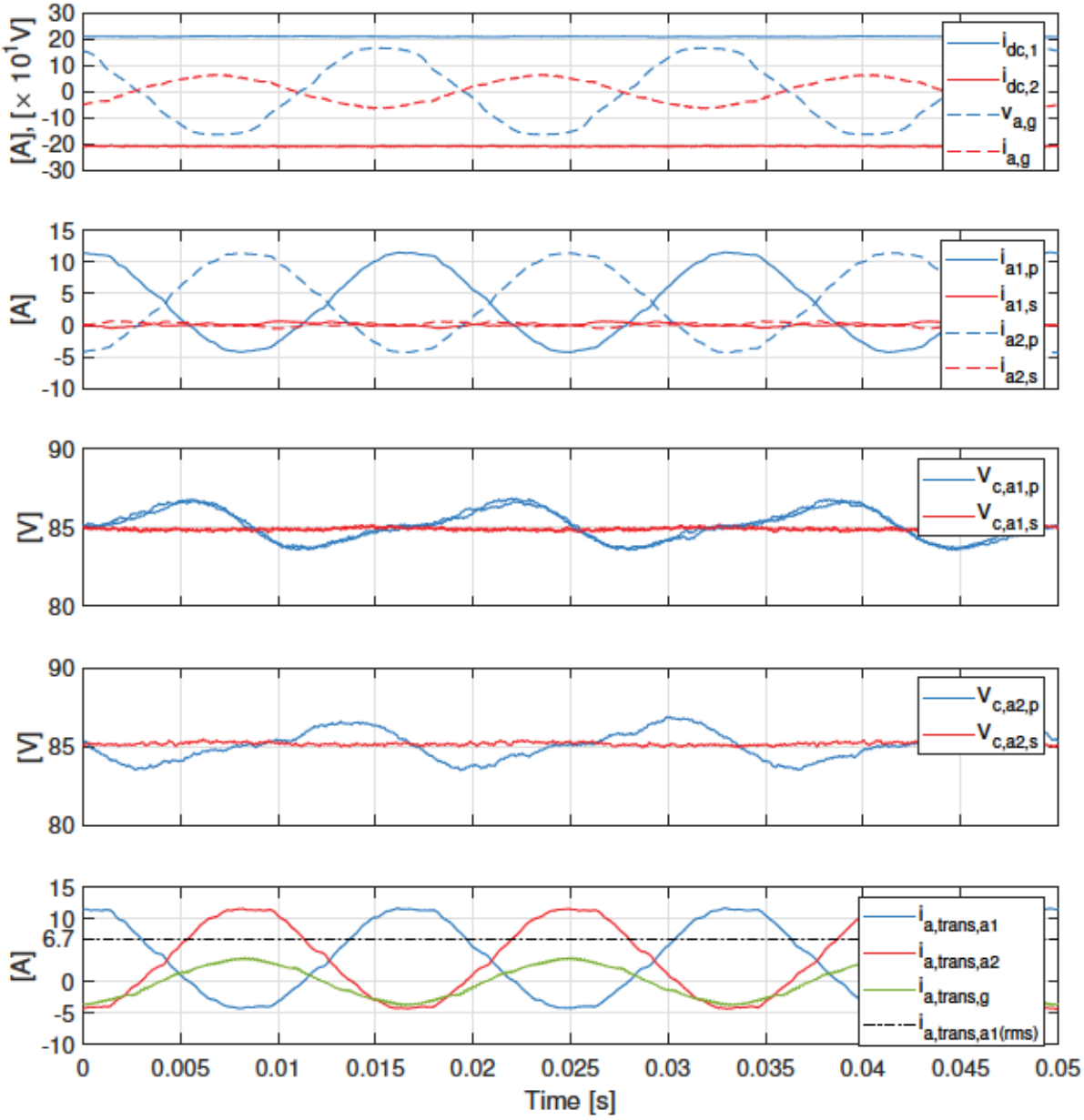

Figure 4.20: Experimental waveforms of three-port MMC for steady-state power flow scenarios: $C1(1, -0.5, 0)$

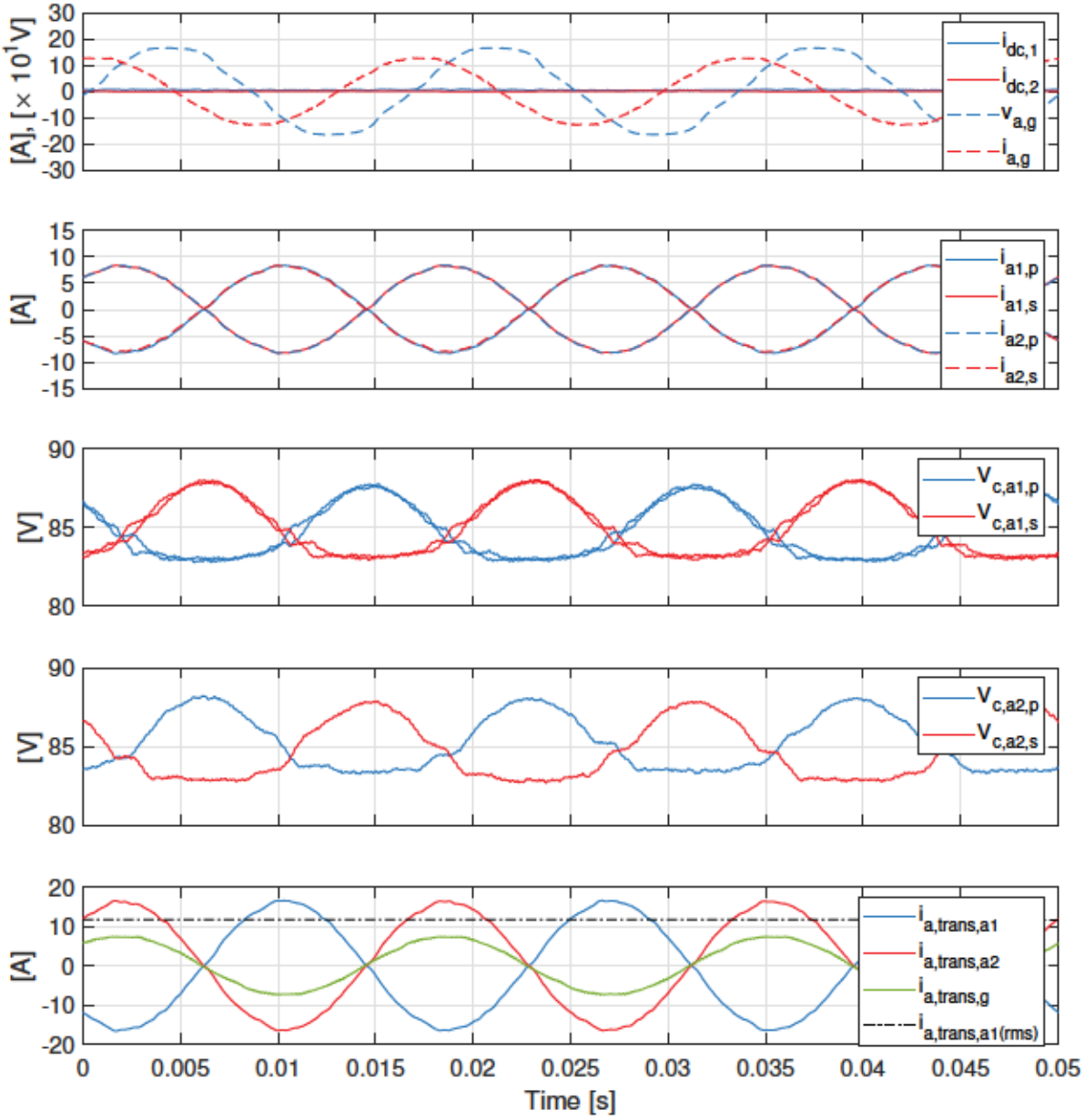

Figure 4.21: Experimental waveforms of three-port MMC for steady-state power flow scenarios: $A(0, 0, -1)$

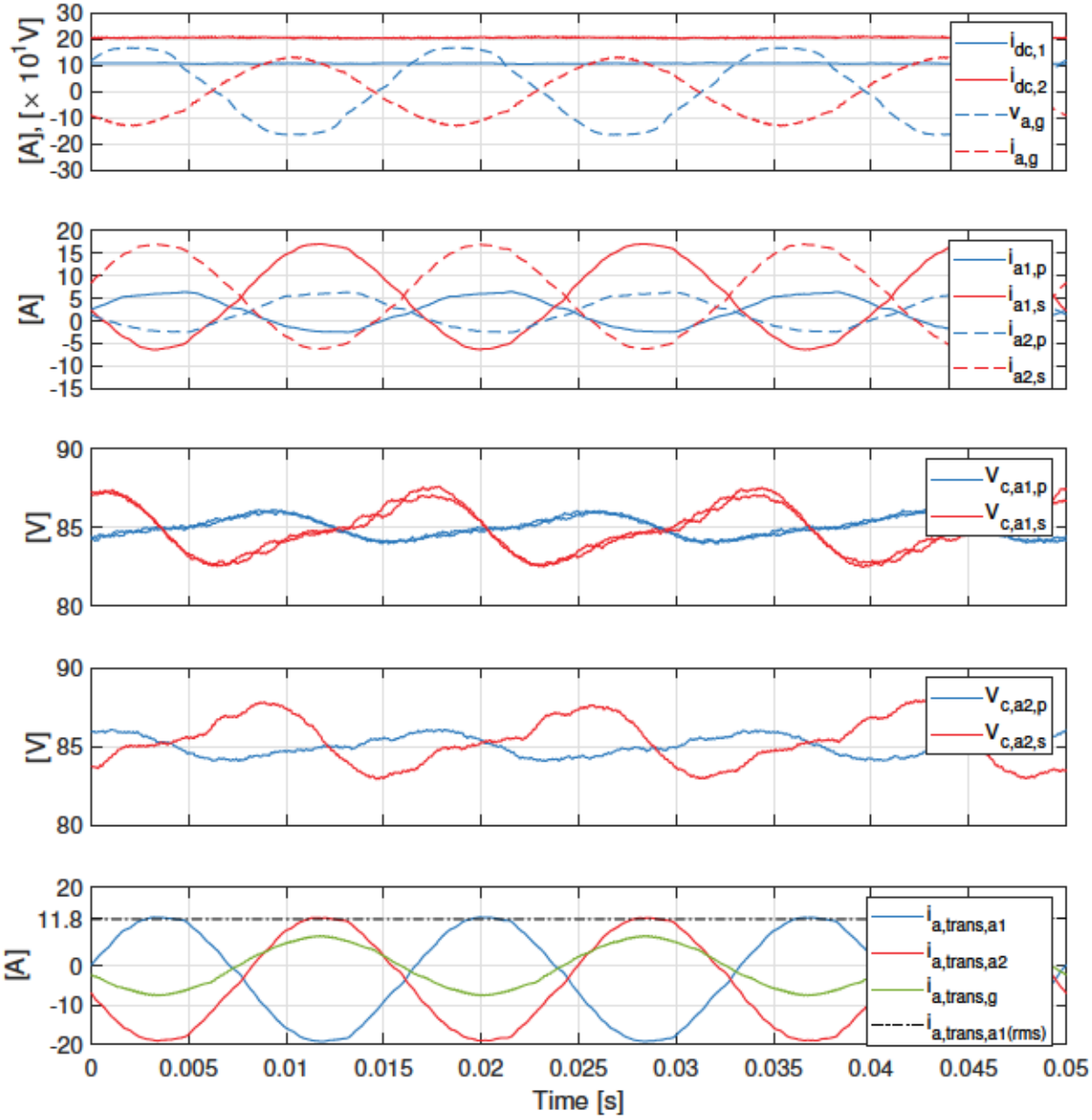

Figure 4.22: Experimental waveforms of three-port MMC for steady-state power flow scenarios: $C2(0.5, 0.5, 0)$

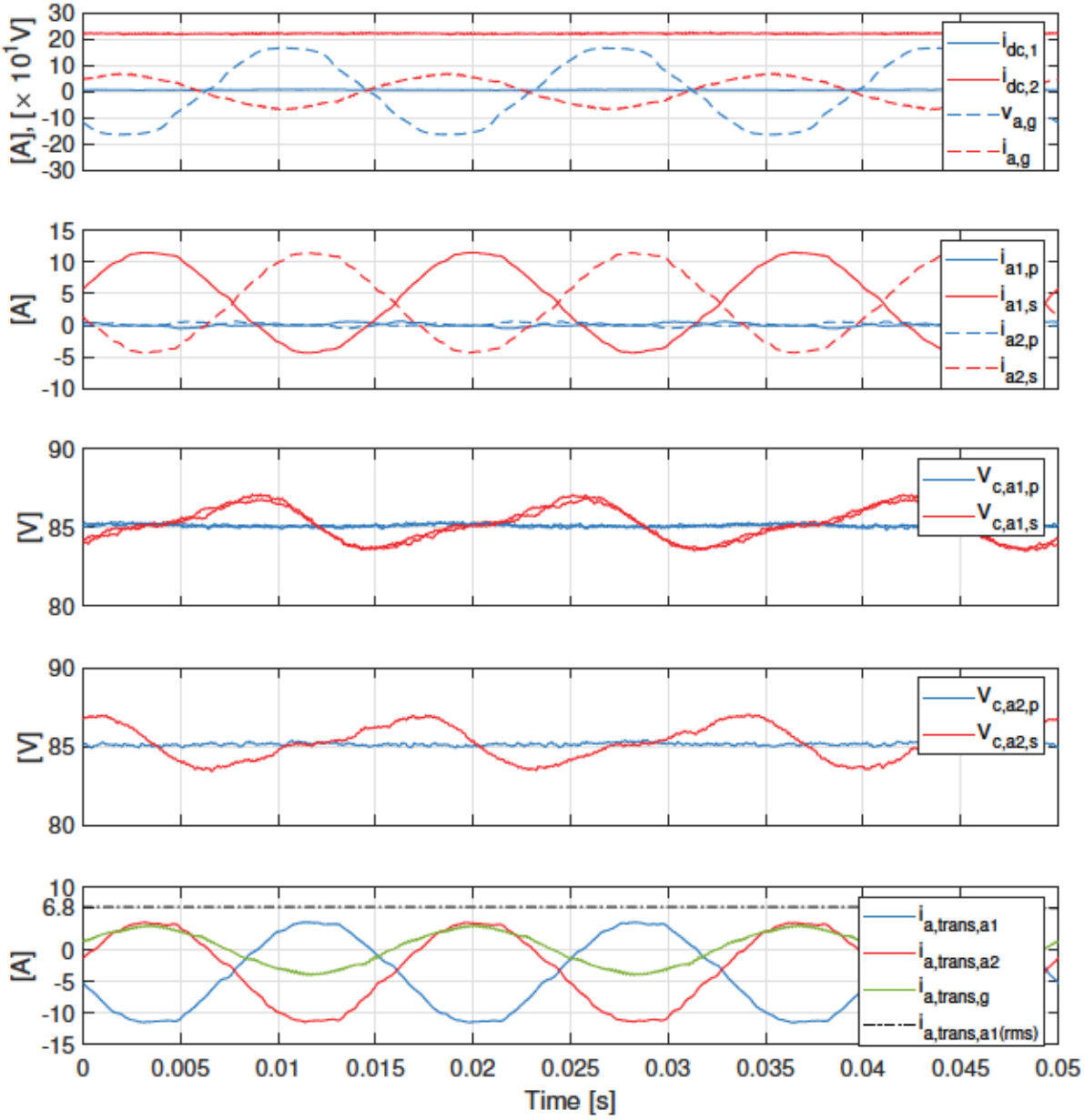

Figure 4.23: Experimental waveforms of three-port MMC for steady-state power flow scenarios: $C2(0, 0.5, 0)$

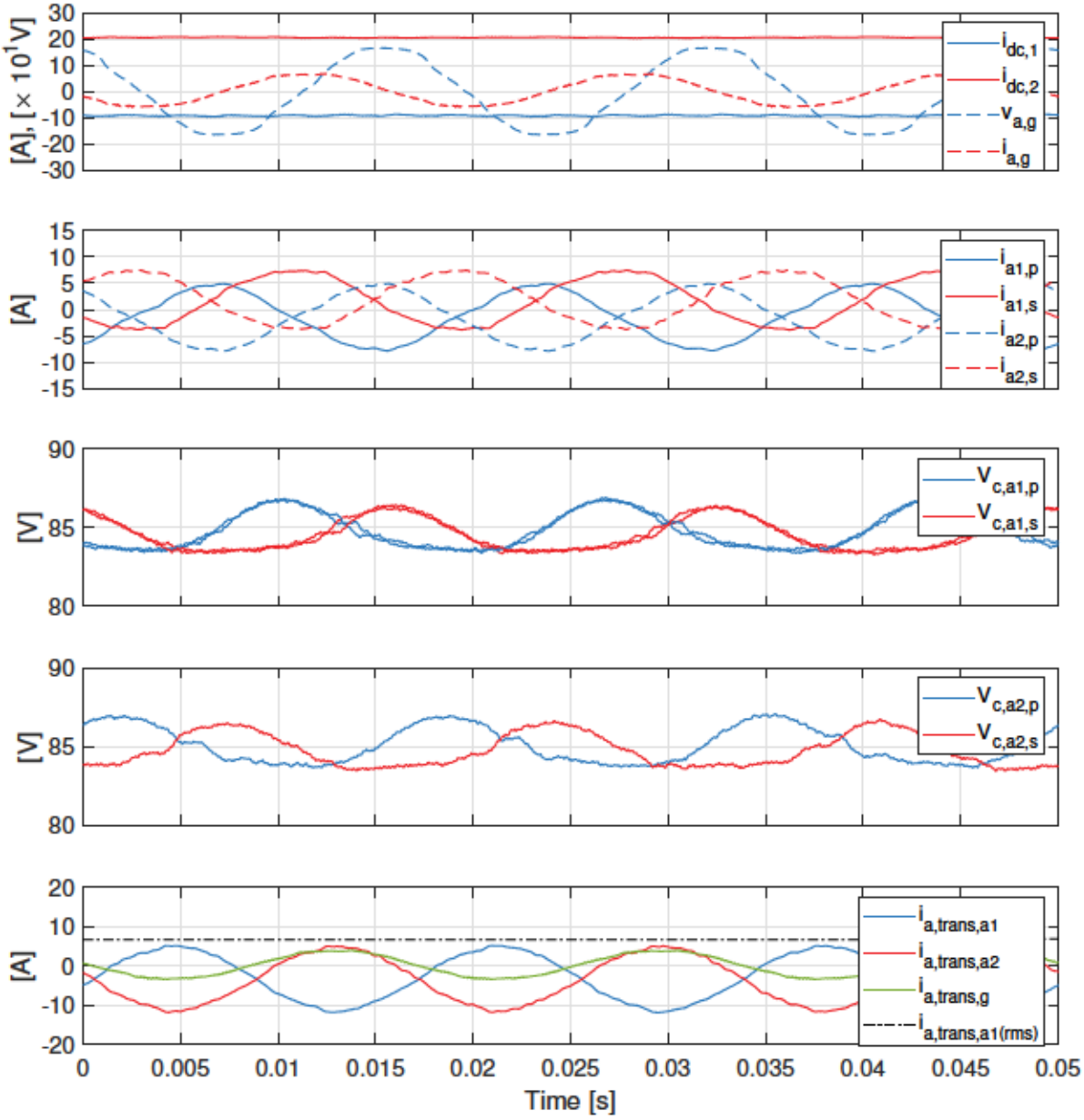

Figure 4.24: Experimental waveforms of three-port MMC for steady-state power flow scenarios: B(-0.5, 0.5, -0.5)

4.6.2 Dynamic Performance

Three power flow scenarios as shown in Fig. 4.25 are used to demonstrate the dynamic response of the three-port MMC for changing loading conditions.

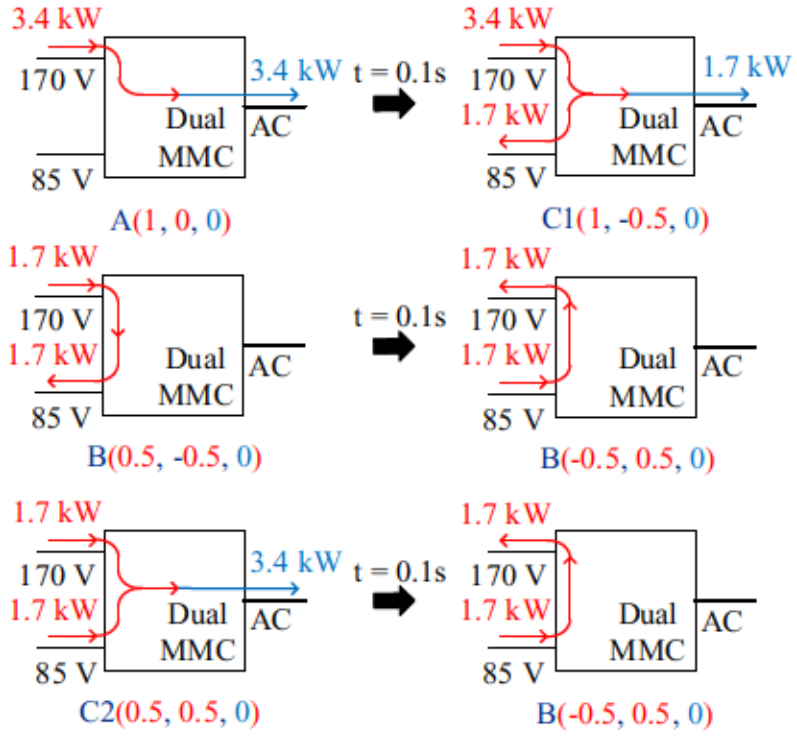

Figure 4.25: Experimental three-port MMC dynamic response under study

This section further validates balanced capacitor voltages between arms are maintained for changing loading conditions. The change in power demand of each pole initially causes a dc voltage imbalance between SM capacitors in the primary and primary arms, i.e., $V_{c,a1,p}$ and $V_{c,a1,s}$ deviate from their reference values. The controller re-establishes balanced capacitor voltages by requesting the requisite change in the fundamental frequency components of $\mathbf{i}_{\alpha\beta,\Sigma1}$ and $\mathbf{i}_{\alpha\beta,\Sigma2}$. The $i_{a1,p}$ and $i_{a1,s}$ (p and s arm currents in MMC1) and $i_{a2,p}$ and $i_{a2,s}$ (p and s arm currents in MMC2) waveforms verify the total power transfer is shared equally between two MMCs. For example, the three-port MMC operates as a single-stage dc-dc converter during B(0.5, -0.5, 0) and B(-0.5, 0.5, 0) in Fig. 4.27, where $i_{a,trans,a1}$ and $i_{a,trans,a2}$ have identical dc component. This ensures transformer core dc flux cancellation is achieved owing to the center-tap windings arrangement. This can also be seen with the transformer winding currents at grid side in phase a $i_{a,trans,g}$. $i_{a,trans,g}$ that only contains ac component at all time verify the total power transfer is shared equally between MMCs, yielding dc flux cancellation within the core during step-changes in power flow demands.

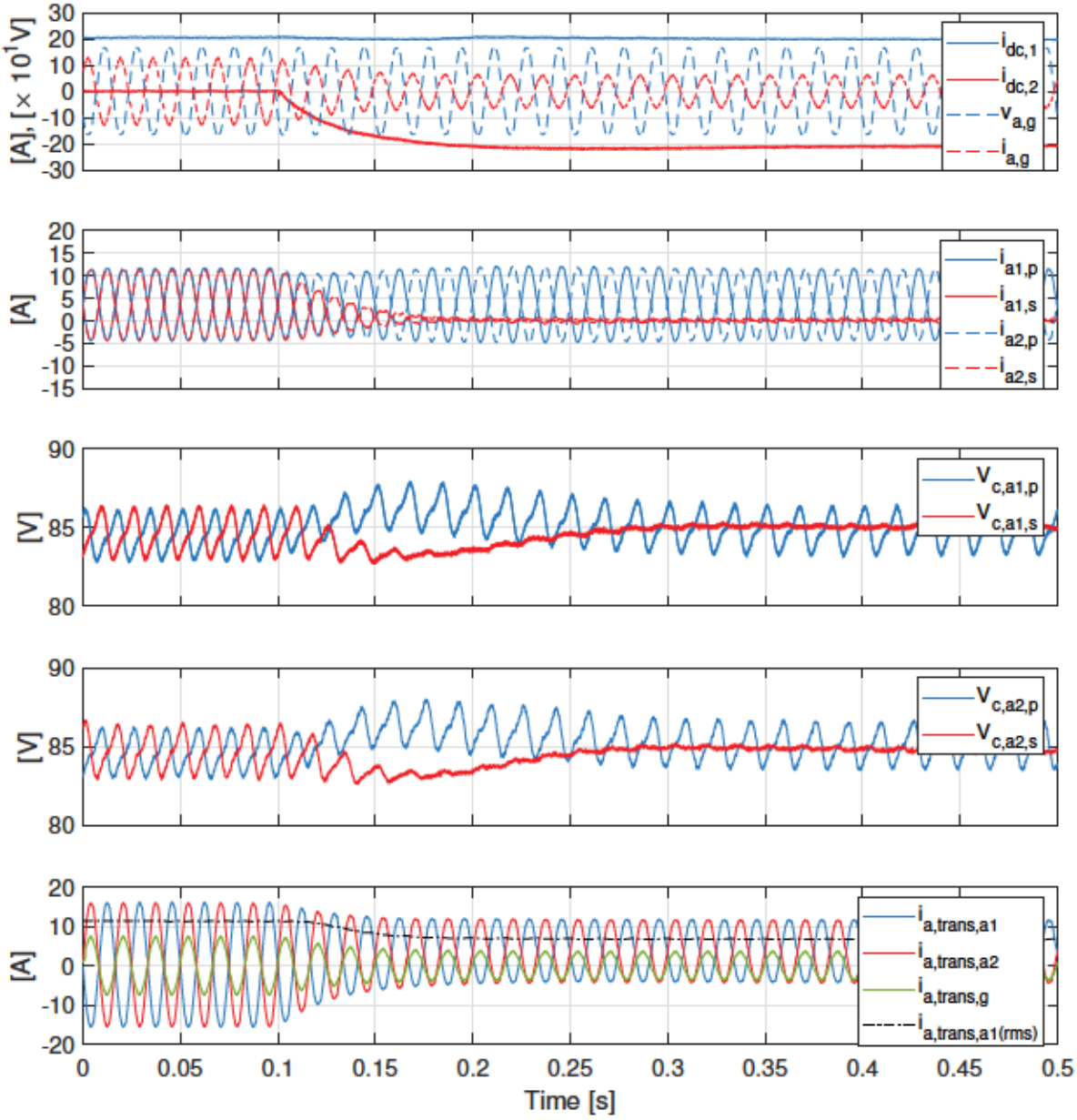

Figure 4.26: Experimental waveforms of three-port MMC for transient power flow scenarios: from $A(1, 0, 0)$ to $C1(1, -0.5, 0)$

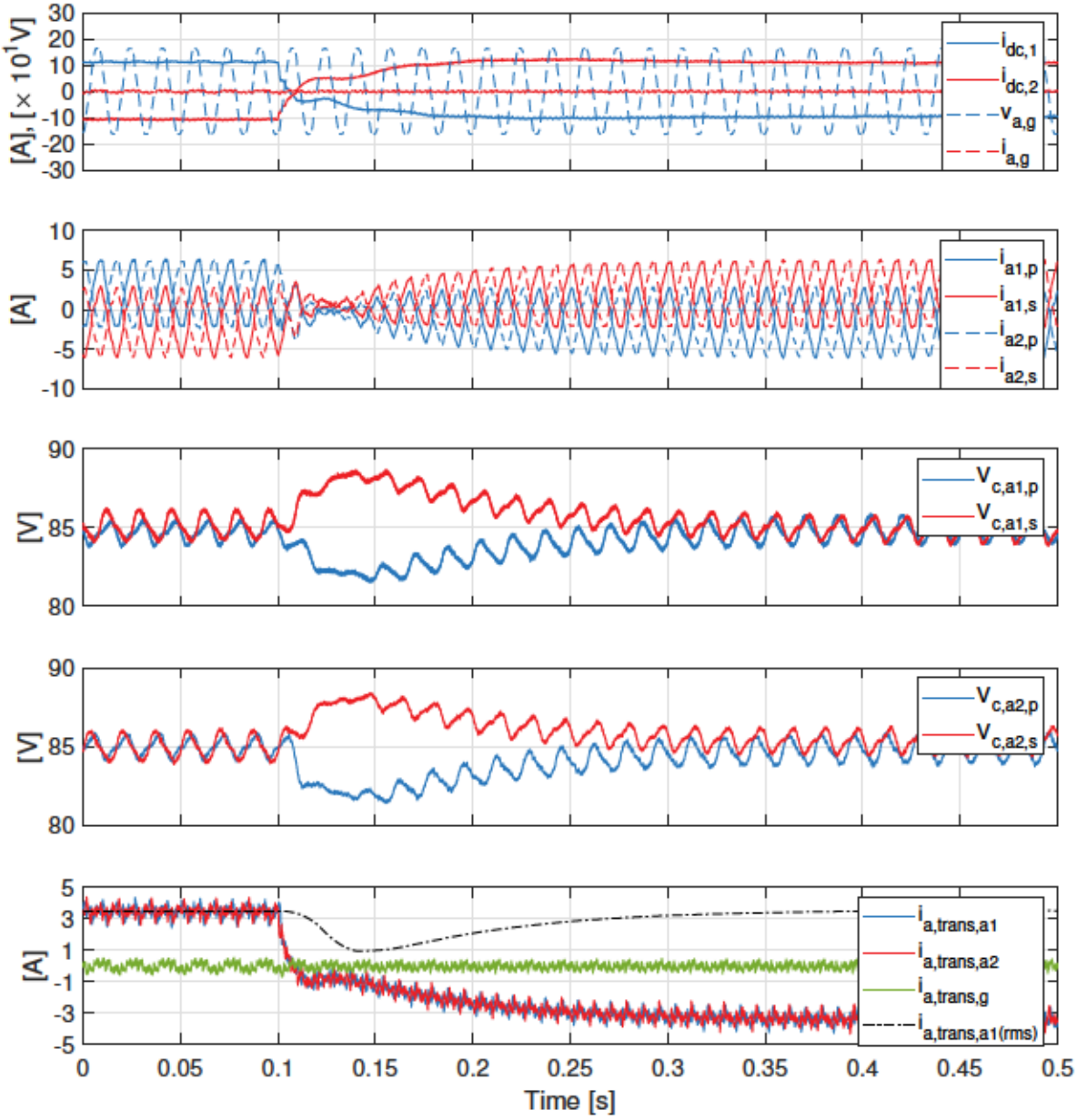

Figure 4.27: Experimental waveforms of three-port MMC for transient power flow scenarios: from B(0.5, -0.5, 0) to C(-0.5, 0.5, 0)

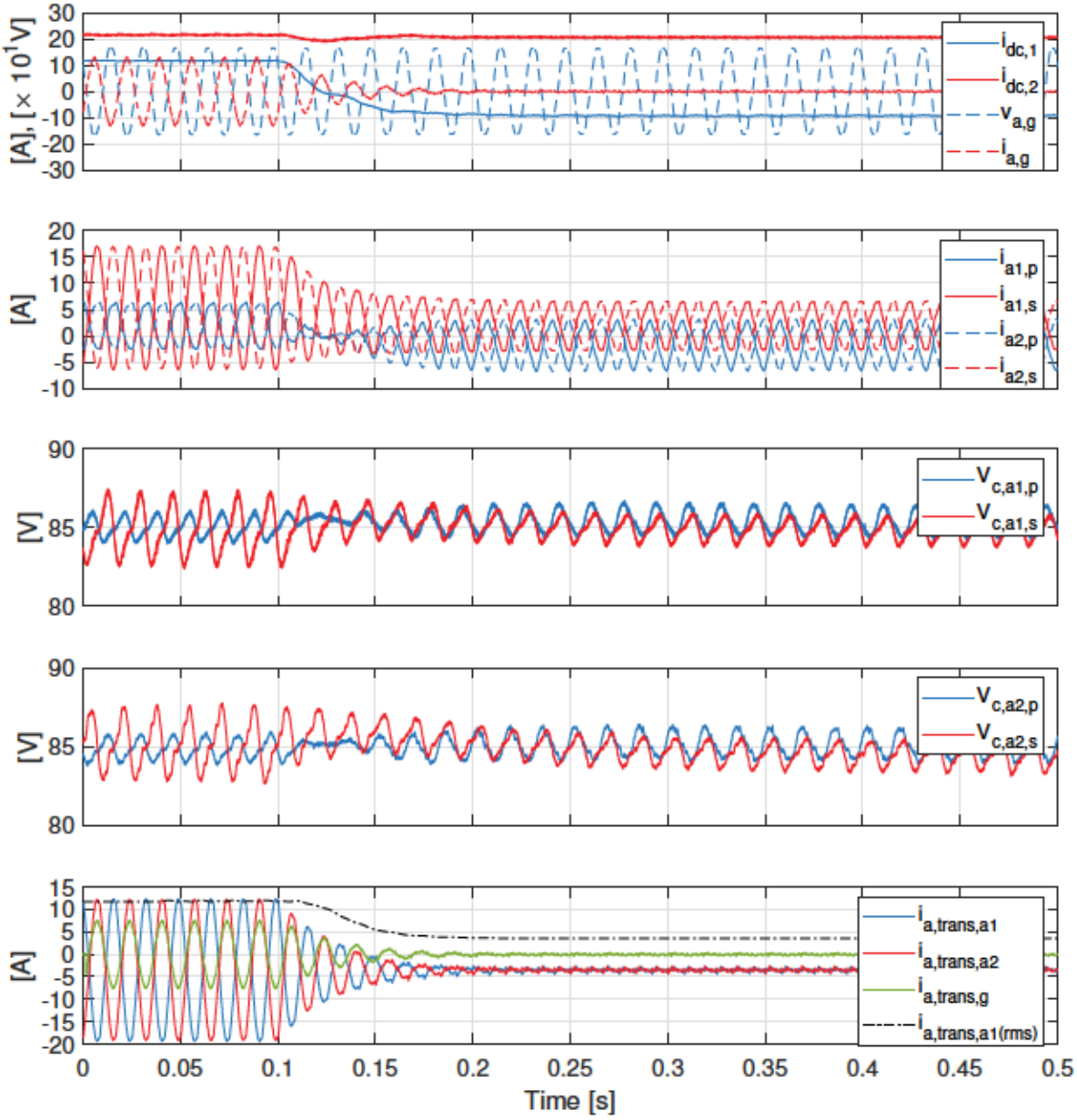

Figure 4.28: Experimental waveforms of three-port MMC for transient power flow scenarios: from $C2$(0.5, 0.5, 0) to B(-0.5, 0.5, 0)

4.6.3 Independent MMC Operation

Fig. 4.30 demonstrates that the MMCs in the proposed dual (parallel) structure can operate independently. This is power flow scenario $A(0.5, 0, 0)$ as shown in Fig. 4.29. Initially, MMC1 processes 1.7 kW (0.5 p.u.) and then MMC1 ramps down to zero while MMC2 is ramped up from zero to process 1.7 kW (0.5 p.u.). The grid current $i_{a,g}$ remains constant during the dynamic. This shows that the dual MMC structure allows each MMC to process up to 0.5 p.u. power independently. If one MMC fails, the other MMC can continue operation for ac power transfer with a reduced output power and hence can help improve system reliability. This redundancy is not possible to achieve with three-port MMCs in Fig. 3.3. However, this independent MMC operation is only valid for pure dc-ac power flow scenario A due to dc flux cancellation requirement. Fig. 4.31 demonstrates the second power flow scenario $C1(0.75, -0.5, 0)$, where dc power split equally between two MMCs to ensure dc flux cancellation and ac power only processed by MMC1.

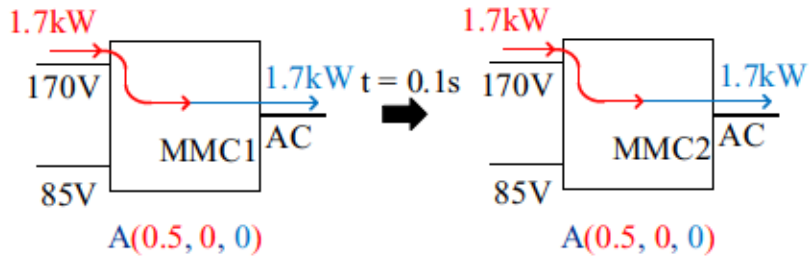

Figure 4.29: Experimental three-port MMC dynamic response for independent MMC operation

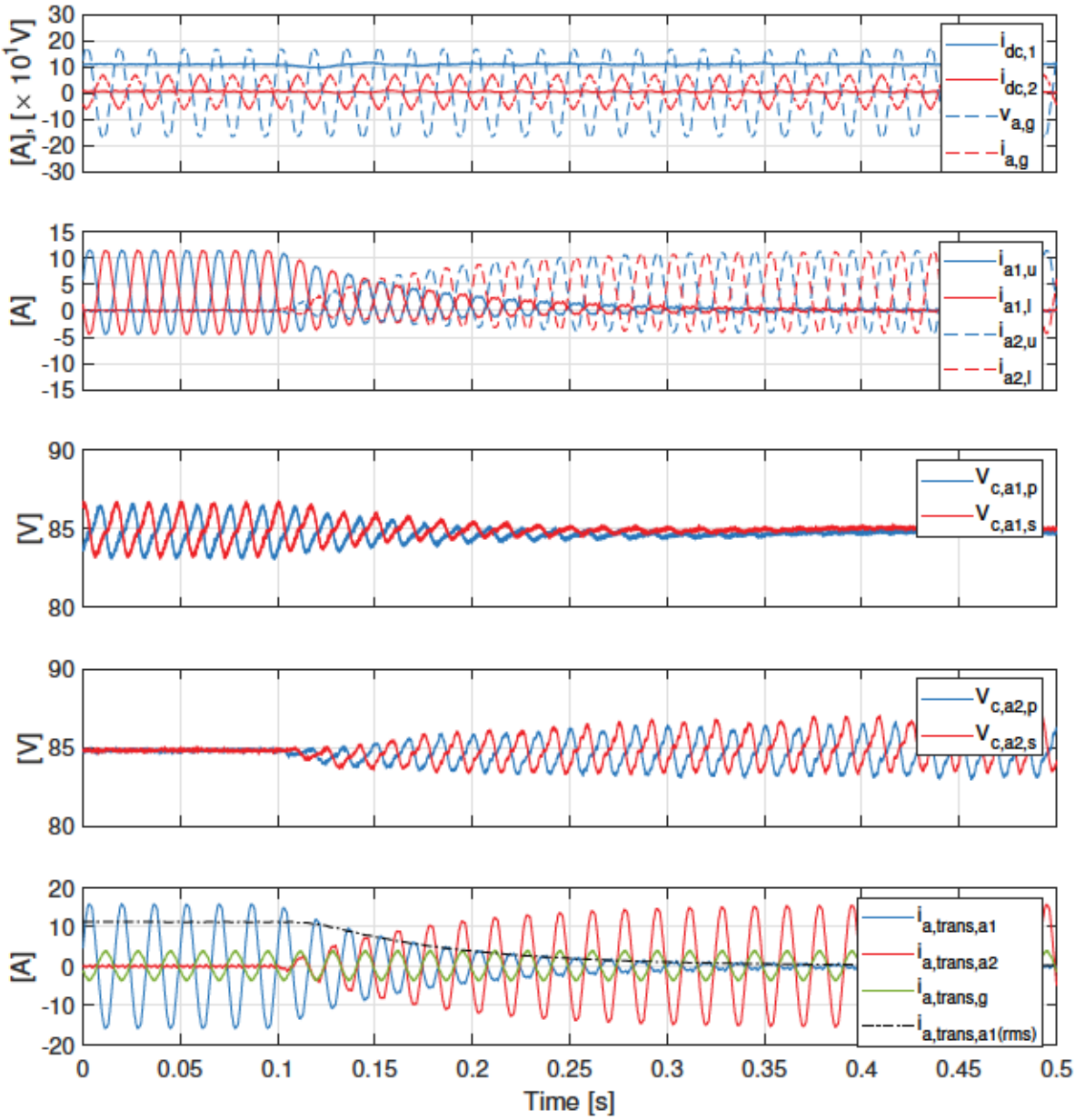

Figure 4.30: Experimental waveforms of three-port MMC for transient power flow scenarios: from $A(0.5, 0, 0)$ where 0.5 p.u. power processed by MMC1 to $A(0.5, 0, 0)$ where 0.5 p.u. power processed by MMC2

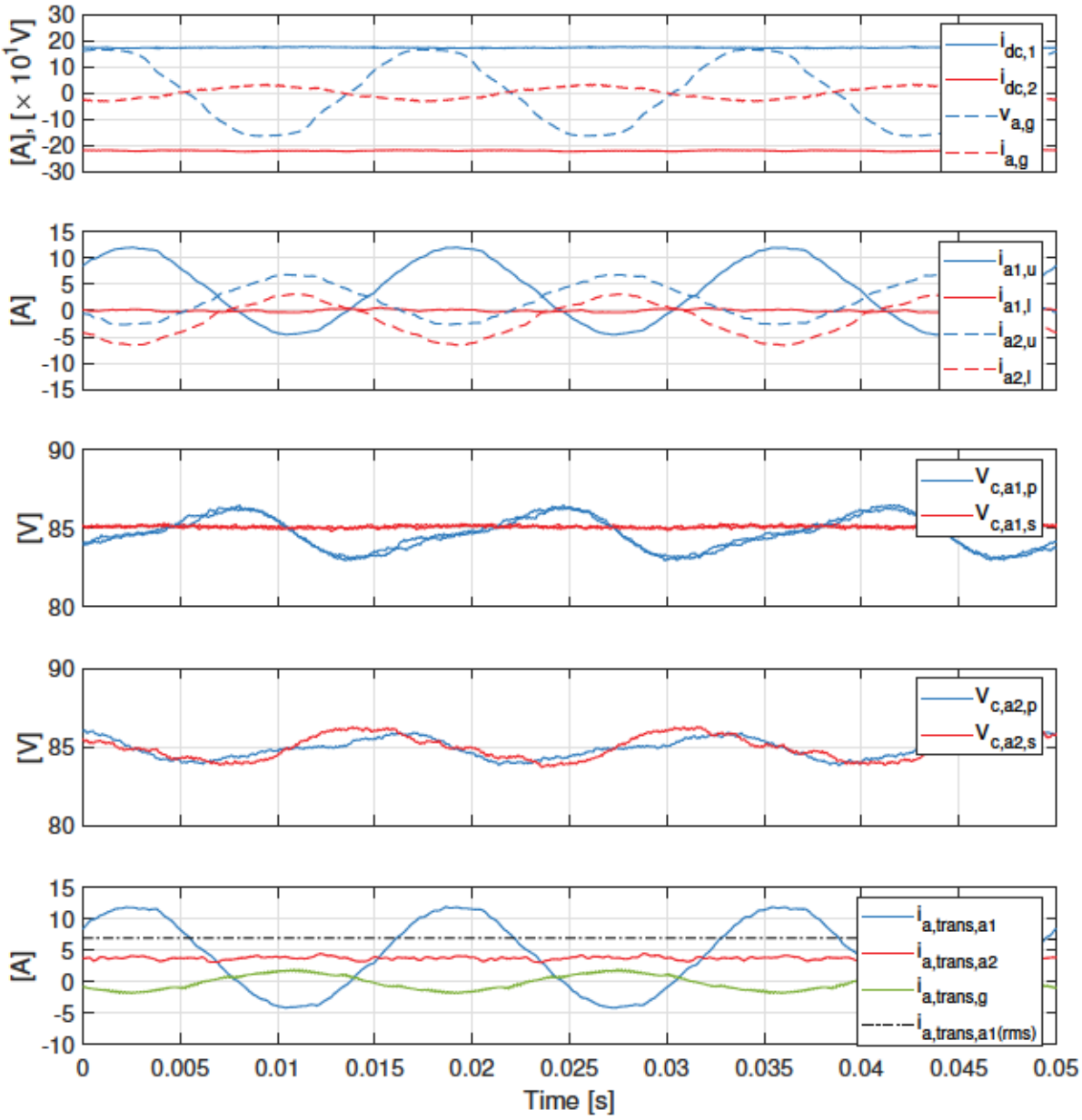

Figure 4.31: Experimental waveforms of three-port MMC for transient power flow scenarios: $C1(0.75, -0.5, 0)$ where both MMCs process 0.25 pu dc power and only MMC 1 processes 0.25 p.u. ac power processed

4.7 Chapter Summary

A three-port MMC that can act as a central hub for routing power between two different dc networks and an ac grid is introduced in this chapter. It is based on the multi-frequency dual MMC chainlink strucutre proposed in Chapter 3. By exploiting multi-frequency power transfer, the three-port MMC offers some benefits over their conventional single-frequency counterparts: i) partial-power-processing is maintained, ii) transformer Volt-Ampere rating can be reduced in some power flow scenarios, and ii) large dc voltage bias between transformer windings can be eliminated. The MMCs are parallel-connected and center-tapped transformer windings are used at the converter side that can handle both dc and ac currents, while imposing dc flux cancellation in the core.

The $\alpha\beta$-frame controls developed in Chapter 3 are extended for the three-port application by assigning appropriate reference signals. PSCAD/EMTDC simulation results using the switched model and extensive experimental results from a 3.4 kW prototype validate the bidirectional three-port power flow on all ports and the unified control scheme. External fault blocking capability of the three-port dual MMC is validated by three simulation case studies including dc pole-to-ground and ac phase-to-ground faults. The simulation and experimental results also indicate that lower power is processed by the converter when power flow is optimized between the ports in a three-port MMC.

Chapter 5

Comparative Assessment of Three-Port MMCs for High-Power Applications

A flurry of research activity into new MMC topologies that harness the circulating ac power concept for SM capacitor charge balancing is being witnessed. Chapter 2-4 provide new topological contributions within this space. Some works have carried out into comparisons of emerging MMC topologies [10, 41, 48–50]. However, they either do not provide a fair comparison or they fail to conduct a complete comparison of emerging MMC topologies. Some three-port MMCs are also examined and compared in [67], but the comparison is limited to a couple of basic design scenarios and so few general conclusions are drawn. To the author's best of knowledge, the existing publications provide limited insight into the actual design, viability and overall performance of three-port MMCs that exploit the circulating ac power concept for a wide range of different application scenarios. Moreover, dc voltage stress on magnetics windings is a crucial factor, especially in high voltage applications. However, all existing comparisons did not account for the impacts of magnetics inter-winding dc voltage stress on the comparison results.

This chapter aims to provide a detailed comparative assessment of the three-port MMC discussed in Chapter 4 against other viable three-port MMC topologies for high power applications. The methods introduced in Section 2.7 are adopted for comparative assessment of the three-port MMCs. Four representative three-port MMC topologies are chosen for the study due to their contrasting internal power processing characteristics. Three different network scenarios are investigated that include HVDC and MVDC applications, covering several different power flow cases. The MMC topologies are compared in terms of semiconductor effort, internal energy storage, magnetics requirements and losses. The results are extensively discussed

and general conclusions are summarized. The range of applications in which each topology should optimally be employed is determined.

5.1 Three-port MMCs Under Study

Figs. 5.1a-d show the four different three-port MMCs selected for study: the three-port MMC-based on F2F-MMC (TP-F2F), M2DC-CT (TP-CT) proposed in Chapter 2, HVDC-AT (TP-AT) and multi-frequency dual MMC (TP-MMC) proposed in Chapter 4. These exemplar topologies are chosen as they represent different classes

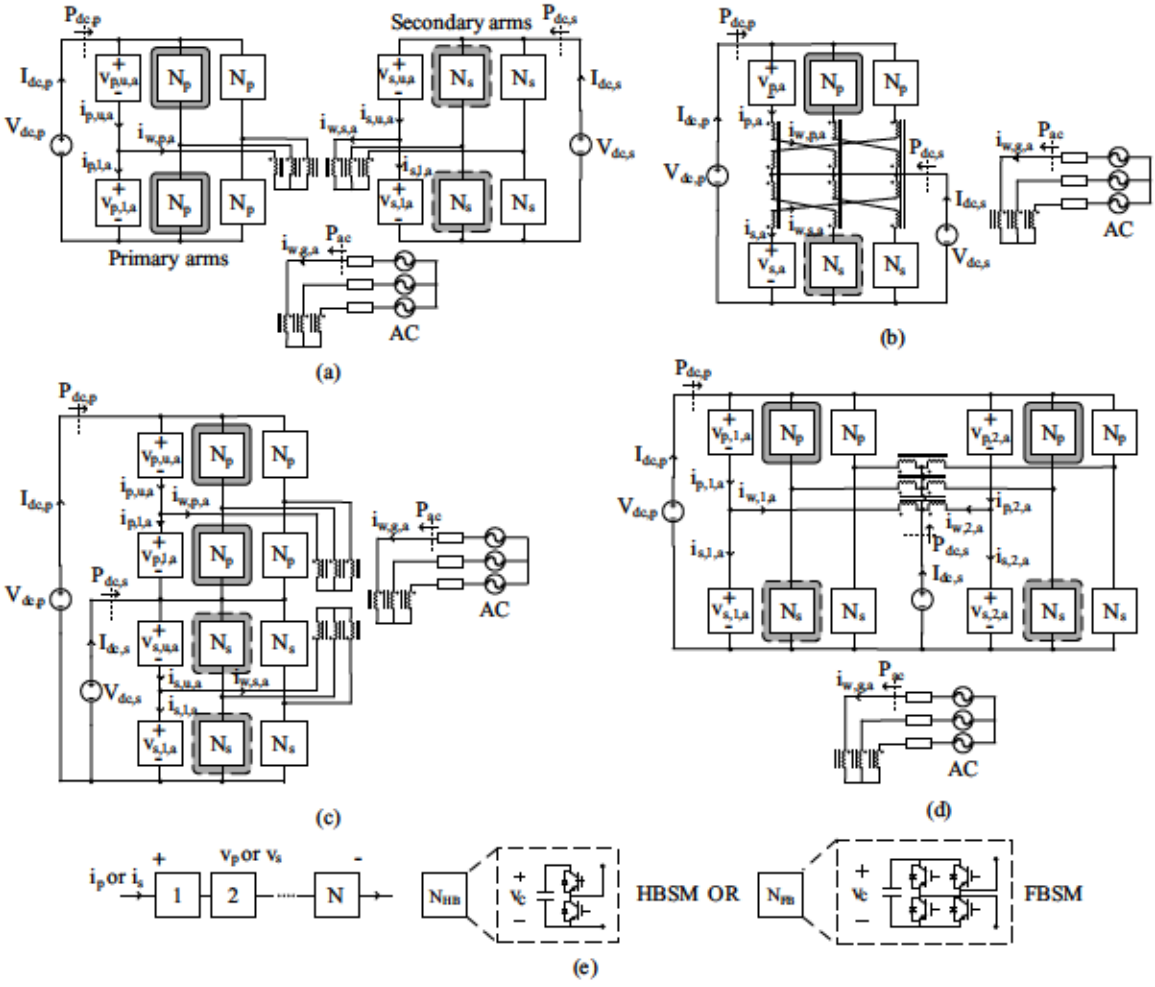

Figure 5.1: Three-port MMCs under study: (a) TP-F2F [10, 112], (b) TP-CT, (c) TP-AT [4, 106, 107, 113], (d) TP-MMC [114], (e) composition of individual phase arms

of three-port MMCs with contrasting internal power processing characteristics. The three-port MMC topologies in Figs 4.1c and 4.1e and other three-port MMCs, e.g. [17,

19, 83, 107], are not compared here as they share strong structural similarly to the four representative topologies. Each three-port MMC interfaces two dc systems. Note that, in contrast to Chapter 4, primary and secondary dc side voltages are represented by $V_{dc,p}$ and $V_{dc,s}$, respectively. Subscripts p and s denote primary and secondary sides, respectively. $P_{dc,p}$, $P_{dc,s}$ and P_{ac} denote average power injections at the dc and ac ports. Assuming for ease of analysis that reactive power transfer is negligible, ac port power injection P_{ac} can be expressed as

$$P_{ac} = -(P_{dc,1} + P_{dc,2}) \tag{5.1}$$

The primary and secondary dc current can be expressed as

$$I_{dc,1} = \frac{P_{dc,1}}{V_{dc,1}},\ I_{dc,2} = \frac{P_{dc,2}}{V_{dc,2}} \tag{5.2}$$

The p and s phase arms comprise N_p and N_s series cascaded SMs, which can be HB or FB type, as shown in Fig. 5.1e. Assuming lossless energy conversion, the steady-state average power absorbed by each arm in Figs. 5.1a-d must be equal to zero as the SMs contain only capacitive energy storage, e.g., $P_p = \frac{1}{T}\int_0^T v_p i_p dt = 0$ in Fig. 5.1b. The arm currents and voltages comprise dc and fundamental frequency ac components. Harmonic power balance [11] necessitates the dc power absorbed by an arm, P_{arm}^{dc}, must be balanced by average power absorption at fundamental frequency, P_{arm}^{ac},

$$P_{arm}^{ac} = P_{arm}^{dc}, \tag{5.3}$$

where

$$P_{arm}^{ac} = \frac{1}{2}\hat{v}_{arm}\hat{i}_{arm}\cos(\theta_{v_{arm}} - \theta_{i_{arm}}) \tag{5.4}$$

$$P_{arm}^{dc} = V_{arm}I_{arm}, \tag{5.5}$$

and placeholder subscript $arm \in \{p, s\}$. Variables $\hat{v}_{arm}$, $\hat{i}_{arm}$ and V_{arm}, I_{arm} are the (peak) fundamental frequency ac and dc components of the arm voltages and currents in Fig. 5.1e. In the subsequent sections, (5.5) is used to explore the average power processing characteristics of the phase arms within the different three-port topologies. The power handling requirements of the different transformer windings will also be examined, as influenced by port power flow demands.

For all three-port topologies, dc step ratio, G_v, is defined as

$$G_v = \frac{V_{dc,s}}{V_{dc,p}}. \tag{5.6}$$

5.2 Power Processing Characteristics

An overview of the internal power processing characteristics of the four topologies is provided in sections 5.2.1 and 5.2.2, where the converters are categorized based on their contrasting characteristics. In the subsequent sections, (5.3) is used to explore the average power processing characteristics of the phase arms within the different three-port topologies. The power handling requirements of the different transformer windings will also be examined, as influenced by port power flow demands.

5.2.1 Power processing characteristics of topologies with conventional ac transformer: TP-F2F and TP-AT

The TP-F2F and TP-AT in Figs. 5.1a and 5.1c are similar with respect to utilizing a conventional ac transformer between MMCs. The TP-F2F is realized by adding a third winding (for ac grid interface) to the well known dc-dc F2F-MMC [106, 112]. Alternatively, the two MMCs can be series stacked on their dc sides, which leads to the non-isolated TP-AT topology Fig. 5.1c [4, 106, 107, 113]. The TP-F2F and TP-AT both use transformer action to transfer ac power between the MMCs and grid. However, their internal converter power processing characteristics are different due to the different ways in which the MMCs are interconnected.

For the TP-F2F, the average power processed by the semiconductor switches in the p and s arms depends on port power flow conditions

$$P_p^{dc} = \frac{1}{6}P_{dc,p},\ P_s^{dc} = \frac{1}{6}P_{dc,s}. \tag{5.7}$$

The six p (and s) arms must collectively process the full dc power transfer associated with $V_{dc,p}$ (and $V_{dc,s}$). This is due to use of separate dc/ac MMC stages.

Based on (2.25) and assuming for ease of analysis that reactive power transfer is negligible, the power processed by the p side winding $S_{w,p,a}$, s side winding $S_{w,s,a}$, and grid side winding $S_{w,g,a}$ for phase a of the TP-F2F transformer is

$$S_{w,p,a} = \left|\frac{P_{dc,p}}{3}\right|,\ S_{w,s,a} = \left|\frac{P_{dc,s}}{3}\right|,\ S_{w,g,a} = \left|\frac{P_{ac}}{3}\right|. \tag{5.8}$$

The results of (5.8) indicate the transformer must be rated to handle the full rated power transfer between ports. This outcome for the TP-F2F is a consequence of the two-stage dc-ac/ac-dc conversion process.

In contrast to the TP-F2F, the TP-AT can realize reduced semiconductor and magnetics power processing requirements. This is because the two MMCs are now series-stacked on their dc sides, i.e. $V_{dc,p}$ is formed in part by $V_{dc,s}$, and hence fewer

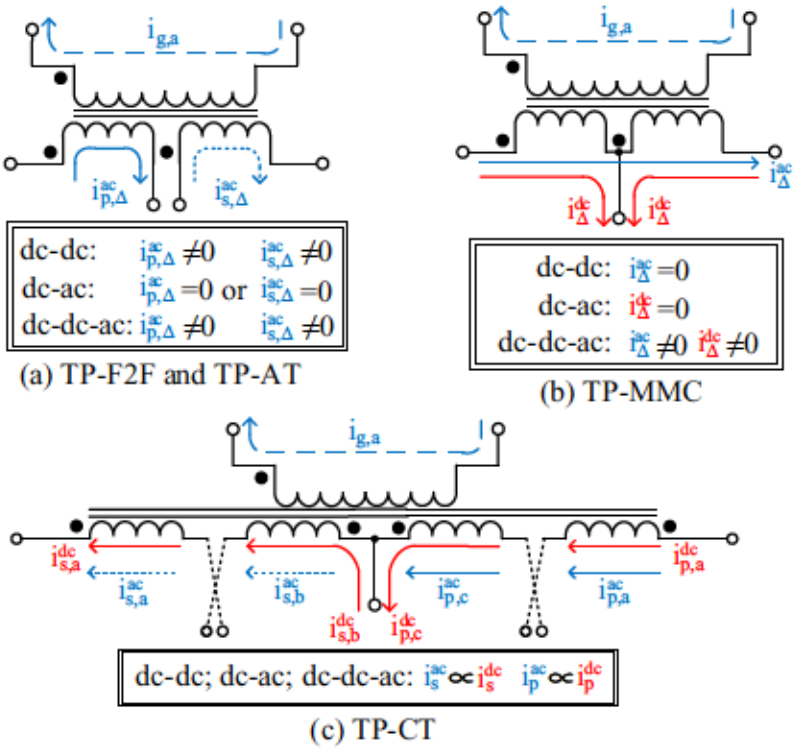

Figure 5.2: Frequency components of transformer winding currents for (a) TP-F2F and TP-AT, (b) TP-MMC, (c) TP-CT

total semiconductors are needed to support the same dc port voltages. Also, the dc ports are no longer decoupled through an ac link and consequently the transformer can realize partial power processing. The average power processed by the p and s arms in the TP-AT is

$$P_p^{dc} = \frac{1}{6}(1 - G_v)P_{dc,p}, \;\; P_s^{dc} = \frac{1}{6}(G_v P_{dc,p} + P_{dc,s}), \tag{5.9}$$

The results of (5.9) depend on dc step ratio G_v defined in (5.6). This is an outcome of the partial power processing property of the TP-AT. Contrasting (5.9) with (5.7) reveals the dc powers processed by the arms in the TP-AT can be reduced relative to the TP-F2F, depending on G_v and the port power flows.

The amount of power transferred by the p, s and grid side windings for phase a of the TP-AT transformer is

$$S_{w,p,a} = \left|\frac{(1 - G_v)P_{dc,p}}{3}\right|, \;\; S_{w,s,a} = \left|\frac{G_v P_{dc,p} + P_{dc,s}}{3}\right|$$

$$S_{w,g,a} = \left|\frac{P_{ac}}{3}\right|. \tag{5.10}$$

Converter-side windings ratings $S_{w,p,a}$ and $S_{w,s,a}$ in the TP-AT both depend on the dc step ratio, however, $S_{w,g,a}$ indicates the grid-side winding must always process

the rated ac port power similar to the TP-F2F case. Comparing (5.10) with (5.8) confirms the power processed by the TP-AT transformer converter-side windings can be reduced relative to the TP-F2F, depending on G_v and the port power flows.

The frequency components for phase a winding currents of the TP-F2F and TP-AT transformers are illustrated in Fig. 5.2a, including the impact of port conversion modes (i.e. whether dc-dc, dc-ac and three-port dc-dc-ac[1] conversions are taking place). Abstract currents $i^{ac}_{p,\Delta} \triangleq i^{ac}_{p,u,a} - i^{ac}_{p,l,a}$ and $i^{ac}_{s,\Delta} \triangleq i^{ac}_{s,u,a} - i^{ac}_{s,l,a}$ are defined here to highlight the ac current paths in the transformer. As expected, only fundamental frequency ac current exists as both converters use classical transformer action to shuttle power between the MMCs and grid. However, the TP-F2F and TP-AT have different internal power processing characteristics as shown by (5.7),(5.8) and (5.9),(5.10). This is because the TP-AT employs single-stage dc-dc conversion due to its partial power processing structure.

5.2.2 Power processing characteristics of topologies with multitasking transformers: TP-CT and TP-MMC

The TP-CT and TP-MMC in Figs. 5.1b and 5.1d also realize partial power processing for dc-dc conversion, similar to the TP-AT. However, whereas the TP-AT (and TP-F2F) use the ac transformer solely to transfer average ac power between p and s MMCs, the TP-CT and TP-MMC multitask their transformers to enable additional internal power transfer mechanisms beyond classical transformer action. This *multitasking* requires the transformer winding currents to have multiple frequency components. In the TP-CT and TP-MMC, the converter-side windings carry both dc and ac currents. However, due to the windings orientations, dc flux cancellation is imposed in the transformer cores [84, 114].

The TP-CT in Fig. 5.1b uses a zig-zag arrangement for the converter-side windings to realize core dc flux cancellation. Alternatively, the TP-MMC in Fig. 5.1d uses center-tapped windings on the converter-side to realize dc flux cancellation [114]. The TP-MMC requires dual MMCs in a differential configuration; a single-ended configuration could be realized with more complicated converter-side windings arrangement, such as in [17, 67]. However, the internal power processing characteristics would remain identical, and thus the TP-MMC in Fig. 5.1d is selected for analysis.

Figs. 5.2b and 5.2d illustrate the frequency components for phase a transformer winding currents of the TP-MMC and TP-CT, respectively, including the impact of

[1]Dc-dc-ac refer to conversion process where both dc-dc and dc-ac power transfers happen simultaneously

power conversion modes. In Fig. 5.2b, the frequencies of the center-tapped winding currents depend on the power conversion mode. Only dc (or fundamental frequency ac) components exist in the converter-side windings for pure dc-dc (and pure dc-ac) conversion, while both frequency components are present for three-port conversion. This is elucidated by defining abstract currents $i_{\Delta}^{dc} \triangleq i_{p}^{dc} - i_{s}^{dc}$ and $i_{\Delta}^{ac} \triangleq i_{p}^{ac} - i_{s}^{ac}$ to decouple frequency components. In contrast, the TP-CT zig-zag windings in Fig. 5.2c must always carry both dc and fundamental frequency ac currents, regardless of the power conversion mode. This is because the converter-side windings in Fig. 5.1b are placed in series with the phase arms.

Due to the commonality of partial power processing, the average powers processed by the p and s arms in the TP-CT and TP-MMC are the same as for the TP-AT, see (5.9).[2] The power processed by the grid side transformer winding in the TP-CT and TP-MMC, $S_{w,g,a}$, is also the same as for the TP-AT (and also the TP-F2F), see (5.10). However, because the converter-side transformer windings in the TP-CT and TP-MMC multitask by carrying multiple frequency components as discussed above, the power processing of these windings are different from the TP-AT and the TP-F2F.

The amount of power transferred by the p and s converter-side windings for phase a of the TP-CT transformer is

$$S_{w,p,a} = \sqrt{\frac{3}{2}} \cdot \frac{(1 - G_v) P_{dc,p}}{3}, \; S_{w,s,a} = \sqrt{\frac{3}{2}} \cdot \frac{G_v P_{dc,p} + P_{dc.s}}{3} \tag{5.11}$$

These values are higher than the TP-AT results of (5.10) by a factor of $\sqrt{3/2}$. This leads to a commensurately higher core power rating, and is due to higher rms currents in the TP-CT converter-side transformer windings. But this comes with the benefit of eliminating inter-winding dc voltage stresses that plague the TP-AT, leading to overall reduced core area-product (and associated losses) for the TP-CT magnetics. Further details on this trade-off can be found in [84].

In the TP-MMC, the center-tapped winding in each phase is shared between p and s arms. To maintain notational consistency with other topologies, the power rating of the winding on the upper and lower side is represented as $S_{w,p,a}$ and $S_{w,s,a}$, respectively. The power handling requirements of the center-tapped winding for phase a is

$$S_{w,p/s,a} = \frac{1}{2} \frac{\sqrt{(P_{dc,p} + P_{dc,s})^2 + k P_{dc,s}^2}}{3},$$

[2]For TP-CT, denominator of (5.9) should be 3 as it has $3p$ (and $3s$) arms

where

$$k = \frac{1}{2}\frac{\left(\frac{\hat{v}_{arm}}{V_{dc,p}}\right)^2}{G_v^2}. \tag{5.12}$$

The TP-MMC is the only three-port topology in Fig. 5.1 where the magnetics do not provide voltage matching between phase arms, i.e. a turns ratio does not link p and s phase arms. Consequently, the power rating of the converter-side center-tapped winding depends on the choice of modulated ac arm voltage, $\hat{v}_{arm}$, for a given G_v, as represented by k in (5.12). More discussions on this design consideration will be included as part of the comparative analysis in the subsequent sections.

5.3 Assessment Criteria

5.3.1 Current Stresses and Semiconductor Effort

A sufficiently high number of SMs are needed in each converter arm, N_{arm}, to generate the required arm voltage v_{arm}, where subscript $arm \in \{p, s\}$. The fundamental frequency component of the arm voltage, $\hat{v}_{arm}$, dictates the fundamental frequency ac currents flowing within the converter. Based on (5.3)-(5.4), and assuming peak ac arm voltages $\hat{v}_p$ and $\hat{v}_s$ are generated at p and s arms, respectively, the peak ac current seen by p and s arms in all three-port topologies are

$$\hat{i}_p = 2\frac{P_{p,dc}}{\hat{v}_p \cos(\theta_{v_p} - \theta_{i_p})},\ \hat{i}_s = 2\frac{P_{s,dc}}{\hat{v}_s \cos(\theta_{v_s} - \theta_{i_s})} \tag{5.13}$$

$\hat{i}_p$ and $\hat{i}_s$ can be minimized by maximizing ac arm voltages $\hat{v}_p$ and $\hat{v}_s$ [84, 115]. Note that if the generated arm ac voltage is greater than arm dc voltage, solely FBSMs are employed in that arm to ensure SM capacitor balance can be satisfied [69]. In this work, the maximal value of $\hat{v}_p$ and $\hat{v}_s$ of each converter are limited to

$$\hat{v}_p^{MP-F2F} = \frac{1}{2}V_{dc,p}, \quad \hat{v}_s^{MP-F2F} = \frac{1}{2}V_{dc,s} \tag{5.14}$$

$$\hat{v}_p^{MP-AT} = \frac{1}{2}(1 - G_v)V_{dc,p}, \quad \hat{v}_s^{MP-AT} = \frac{1}{2}V_{dc,s} \tag{5.15}$$

$$\hat{v}_p^{MP-MMC} = \frac{1}{2}V_{dc,p}, \quad \hat{v}_s^{MP-MMC} = \frac{1}{2}V_{dc,p} \tag{5.16}$$

$$\hat{v}_p^{MP-CT} = (1 - G_v)V_{dc,p}, \quad \hat{v}_s^{MP-CT} = V_{dc,s} \tag{5.17}$$

The dc-dc F2F-MMC inherently offers bidirectional fault blocking due to the galvanic separation property of the intermediate ac transformer. However, with the addition of the grid-side winding in Fig. 5.1a, the TP-F2F loses dc fault blocking

capability as the external ac grid can now source fault current. Consequently, a sufficient number of FBSMs have to be installed in the arms to enable the TP-F2F to provide bidirectional dc fault blocking. In all three-port topologies, each converter arm requires sufficient blocking capability in both forward and reverse directions to block dc faults in both the primary and secondary dc sides. Simulation results for employing FBSMs in TP-MMC to block external faults are given in Section 4.5. In addition to the dc fault interrupting capability, utilizing FBSMs provides freedom to control the maximum arm ac voltage regardless of the available dc voltage. As been discussed in Section 2.1, MMC topologies that utilizes common arm ac circulating current may suffer from extremely large arm current for low dc step ratio. This is commonly done in dc-dc MMC topologies, e.g. [7, 50, 51], which can enable the reduction of arm ac current. FBMSs are thus chosen here to conduct a fair comparison of the four three-port topologies. The three-port MMC inherently have the fault blocking capability on ac side as the conventional dc-ac MMC. Table 5.1 summarizes the arm voltage requirements of the three-port MMCs in Fig. 5.1 to achieve fault blocking on all ports. The red text indicates FBSMs are necessary for the required arm voltage generation.

Table 5.1: v_{arm} Generation Requirements for Three-Port MMCs of Fig. 5.1 to Ensure Fault Blocking on All Ports (Red Text Denotes FBSMs)

	[min, max] voltage injection required
v_{arm}	TP-F2F
v_p	$[-\hat{v}_p,\ \frac{1}{2}V_{dc,p} + \hat{v}_p]$
v_s	$[-\hat{v}_s,\ \frac{1}{2}V_{dc,s} + \hat{v}_s]$
v_{arm}	TP-AT
v_p	$[-\frac{1}{2}V_{dc,s} - \hat{v}_p,\ \frac{1}{2}V_{dc,p} + \hat{v}_p]$
v_s	$[-\hat{V}_s,\ \frac{1}{2}V_{dc,s} + \hat{v}_s]$
v_{arm}	TP-MMC and TP-CT
v_p	$[-V_{dc,s} - \hat{v}_p,\ V_{dc,p} + \hat{v}_p]$
v_s	$[-\hat{v}_s,\ \frac{1}{2}V_{dc,s} + \hat{v}_s]$

Note that if the generated arm ac voltage is greater than arm dc voltage, solely FBSMs are employed in that arm to ensure SM capacitor balance can be satisfied [69]. The maximal values of $\hat{v}_p$ and $\hat{v}_s$ of each three-port MMC are limited to

$$\hat{v}_p^{TP-F2F} = \frac{1}{2}V_{dc,p}, \qquad \hat{v}_s^{TP-F2F} = \frac{1}{2}V_{dc,s} \tag{5.18}$$

$$\hat{v}_p^{TP-AT} = \frac{1}{2}(1 - G_v)V_{dc,p}, \quad \hat{v}_s^{TP-AT} = \frac{1}{2}V_{dc,s} \tag{5.19}$$

$$\hat{v}_p^{TP-MMC} = \frac{1}{2}V_{dc,p}, \quad \hat{v}_s^{TP-MMC} = \frac{1}{2}V_{dc,p} \tag{5.20}$$

$$\hat{v}_p^{TP-CT} = (1 - G_v)V_{dc,p}, \quad \hat{v}_s^{TP-CT} = V_{dc,s} \tag{5.21}$$

The number of SMs required in a converter arm N_{arm} can be estimated by the nominal voltage V_c of the SM capacitors and the maximum (peak) value of arm voltage v_{arm} that has to be generated as per Table 5.1

$$N_{arm} = k_s \frac{max(v_{arm})}{V_c}, \tag{5.22}$$

where k_s is an additional safety factor that is set to 120% in this study. FBSMs are needed only if a negative arm voltage is required (as indicated by red text in Table 5.1). The number of FBSMs required is

$$N_{FB,arm} = k_s \frac{|\min(v_{arm})|}{V_c} \tag{5.23}$$

Therefore, the number of HBSMs is

$$N_{HB,arm} = N_{arm} - N_{FB,arm} \tag{5.24}$$

The semiconductor effort λ is often used as a measure of the power rating of switches that has to be installed per Watt of P_{conv} [68, 70, 84]. The switch rating of FBSMs will be two times of HBSMs due to the fact that FBSM consists of 4 semiconductors.

5.3.2 Submodule Capacitive Stored Energy

The total capacitive stored energy E_{cap} is the energy per megawatt (MW) stored in the MMC converter [97]. SM capacitance can be different between p and s arms for the three-port MMCs. This is because the power processed by the arms in a three-port converter can be different. The capacitive stored energy E_{cap} in $arm \in \{p, s\}$ is

$$E_{cap,arm} = \frac{\frac{1}{2} \cdot N_{arm} C_{arm} V_c^2}{P_{conv}} \tag{5.25}$$

where N_{arm}, C_{arm} and V_c are total number of SMs, individual SM capacitance in $arm \in \{p, s\}$ and nominal SM capacitor voltage, respectively.

The submodule capacitance required to achieve a certain capacitor peak-to-peak voltage ripple Δv_c may be predicted by considering the total energy stored in each arm. It is related to the capacitive energy peak-to-peak variation over one fundamental cycle ΔE_{cap} [50]:

$$C_{arm} = \frac{\Delta E_{cap,arm}}{N_{arm} V_c^2 \cdot \Delta v_c} \tag{5.26}$$

For fixed values of $\Delta E_{cap,arm}$, N_{arm} and V_c, lower values of submodule capacitance reduces the converter cost but results in higher voltage ripples. In this study, C_p and C_s values are selected to yield peak-to-peak capacitor voltage ripples Δv_c of around 16% at rated power transfer [116, 117]. Thus, the total energy stored in the converter can be calculated from the total capacitor energies in each arm as

$$E_{cap} = q(E_{cap,p} + E_{cap,s}) \tag{5.27}$$

where $q = 6$ for the TP-F2F, TP-AT and TP-MMC; and $q = 3$ for the TP-CT. In the conventional dc-ac MMC, a total capacitive stored energy of 30-40 kJ/MW yields a submodule peak-to-peak capacitor voltage ripple in the range of 20% [116, 117].

5.3.3 Power Losses

It is assumed that conduction and switching losses are the primary sources of semiconductor losses in each converter. An average losses calculation method introduced in Section 2.7 is chosen to calculate the semiconductor losses of the four three-port converter systems in Fig. 5.1. A detailed breakdown of calculations involved for conduction and switching losses used in this chapter can be found in [50, 51]. Due to the symmetry of the converters, conduction and switching losses are estimated separately for each arm by considering the voltages and currents of one submodule and then summed up the losses to determine the total losses of the converter.

Since the semiconductor losses calculation is dependent on technology, the Mitsubishi CM1200HC-90R HVIGBT with a rating of 4500 V and 1200 A is used for all topologies. As the current carried by the semiconductors substantially increases for lower conversion ratios, IGBTs are paralleled as needed to accommodate arm currents that exceed switch ratings [50]. The converters operate at $f = 60$ Hz due to ac grid connection.

In addition to converter switching and conduction losses, this chapter use a method similar to [51, 84] to approximate the magnetics losses. This method approximates losses as 0.5% of the transformer Volt-Ampere rating. For three-port MMC, the transformer Volt-Ampere rating is the maximum of the amount of power transferred by the primary p, secondary s and grid side g windings

$$S_w = \max\{S_{w,p}, S_{w,s}, S_{w,g}\} \tag{5.28}$$

The combined copper and core losses for magnetics in the three-port MMCs are thus approximated as

$$P_{L,copper} + P_{L,core} = 0.5\% \cdot S_w. \tag{5.29}$$

5.4 Case Study Three-Port Scenarios

This section carries out a comparative analysis of the four three-port converter topologies in Fig. 5.1. Three different three-port scenarios (A, B and C) are considered as shown in Fig. 5.3, where each scenario is further broken down into three sub cases based on different port power flow demands. These scenarios consider both HVDC and MVDC applications. The following parameters are fixed in all scenarios: $V_{dc,p}$ = 400 kV, $V_{ac,LL(rms)}$ = 220 kV. The following comparison assumes that: i) reactive power transfer to the grid is negligible, and ii) the three-phase ac grid is balanced positive sequence.

Scenario A considers the interconnection of two HVDC grids with different nominal voltages and one HVAC grid. $V_{dc,s}$ is set to 200 kV, which corresponds to dc step ratio $G_v = 0.5$. All ports are rated for $P_{conv} = 400$ MW.

Scenario B is a variation of Scenario A where $V_{dc,s}$ = 320 kV, yielding a dc step ratio $G_v = 0.8$ and reflecting two HVDC grids with more similar nominal voltage levels. All ports are rated for $P_{conv} = 400$ MW.

Scenarios A and B consider exclusively HVDC voltage levels for the dc systems. In contrast, Scenario C investigates interfacing a 40 kV MVDC system with the 400 kV HVDC system. This will explore implications of a relatively low dc step ratio $G_v = 0.1$. All ports are rated for $P_{conv} = 300$ MW.

In Fig. 5.3, Scenarios A, B and C are further divided into three sub cases based on different power flows between the three ports. Specifically,

1. Cases $A1$, $B1$, $C1$: $P_{dc,p}$ as ± 1 p.u., and α (or per-unitized P_{ac}) is varied between 0 and 1, red lines;

2. Cases $A2$, $B2$, $C2$: $P_{dc,s}$ as ± 1 p.u., and α (or per-unitized P_{ac}) is varied between 0 and 1, green lines;

3. Cases $A3$, $B3$, $C3$: P_{ac} as ± 1 p.u., and β (or per-unitized $P_{dc,p}$) is varied between 0 and 1, blue lines.

Cases $A1, B1, C1$ and $A2, B2, C2$ reflect the ac system tapping power from dc ports. Cases $A3, B3, C3$ can be viewed as an external dc system ($V_{dc,p}$) tapping power from the other ports. Notation $\pm$ denotes positive/negative power flows.

Based on the scenarios in Fig. 5.3, four three-port converters in Fig. 5.1 are compared in terms of semiconductor efforts, efficiency, internal stored energy and magnetic requirements. To provide a fair comparison, all three-port converters are designed to provide fault blocking capability at the dc and ac ports by using the necessary number

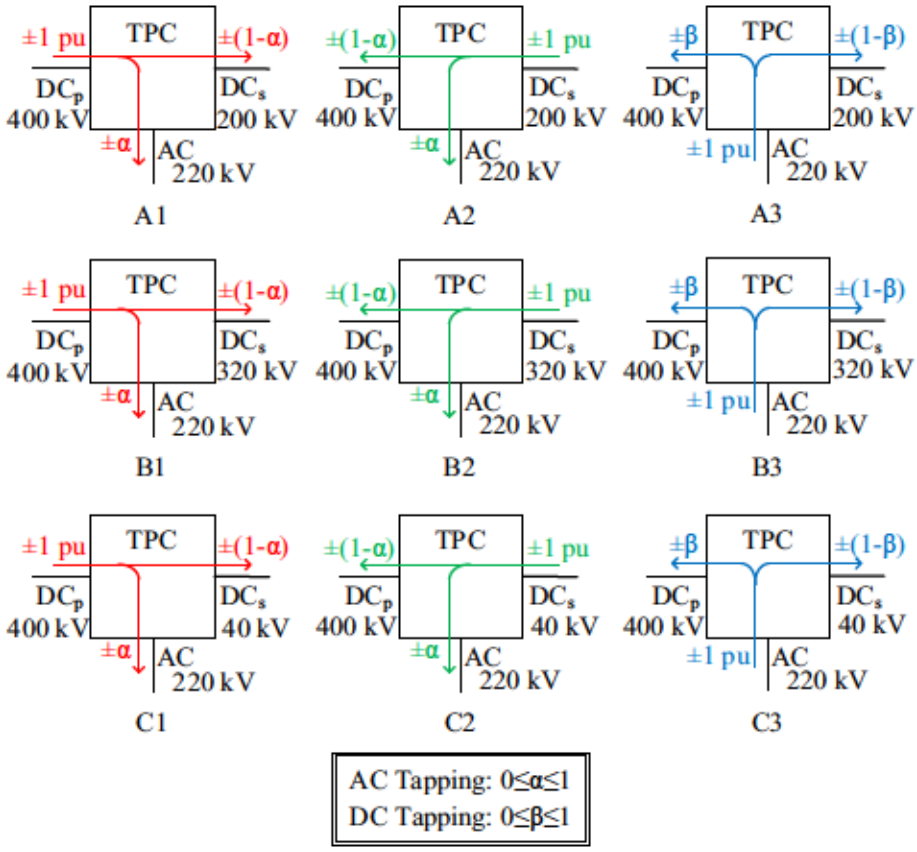

Figure 5.3: Three-port converter (TPC) scenarios under study, where $V_{dc,p} = 400$ kV and $V_{ac,LL(rms)} = 220$ kV are held constant, and (i) Scenarios $A1, A2, A3$ have $G_v = 0.5$, $P_{conv} = 400$ MW, (ii) Scenarios $B1, B2, B3$ have $G_v = 0.8$, $P_{conv} = 400$ MW, (iii) Scenarios $C1, C2, C3$ have $G_v = 0.1$, $P_{conv} = 300$ MW

of FBSMs in the arms. The comparison results are organized into three sections as follows:

- Section 5.5 contrasts key comparison results for the four three-port MMCs.
- Section 5.6 compares magnetics used in four three-port MMCs and their impacts on converter overall losses.
- Section 5.7 contrasts three-port and two-port conversion processes.

5.5 Comparison of Four Three-port MMCs

Fig. 5.4a shows the converter losses, semiconductor efforts, required apparent power ratings of magnetics and the total capacitive stored energies for the TP-F2F, TP-AT, TP-MMC and TP-CT considering the nine different power flow cases in Fig. 5.3.

The bar graphs are organized into three rows to separate scenarios A, B, C, and are further apportioned into columns to separate sub cases 1,2,3, e.g., the first column comprises cases $A1, B1, C1$. The first two columns correspond to tapping 400α MW ac power (cases $A1, A2, B1, B2$) and 300α MW ac power (cases $C1, C2$) from the dc ports, where $\alpha \in [0, 1]$. The third column corresponds to tapping 400β MW dc power (cases $A3, B3$) and 300β MW dc power (case $C3$) from the other ports, where $\beta \in [0, 1]$. The bar graphs summarize results for some key values of α and β, due to space limitations. For ease of comparison, the bar graph results are normalized as follows: λ by P_{conv}, S_w by $2P_{conv}$, and losses by P_{conv}.

Figs. 5.4b,c,d show the three-port converter topology with the lowest overall losses for every operating point in Scenarios A, B, C, respectively, for all possible values of α and β. Results are plotted $P_{dc,s}$ versus P_{ac} where $P_{dc,p} = -(P_{dc,s} + P_{ac})$. In each plot, the operating areas are divided into 6 segments (by the dotted lines) corresponding to the different power flow sub cases, where red, blue, green and black represents the TP-F2F, TP-AT, TP-MMC andTP-CT, respectively.

The four three-port topologies are divided into two categories as discussed in sections 5.2.1 and 5.2.2. The TP-F2F and TP-AT are grouped together based on their use of classical transformer action for inter-arm power transfers. The TP-CT and TP-MMC are grouped together because they both multi-task their transformers to achieve additional power transfer mechanisms. However, the TP-AT, TP-CT and TP-MMC all practice partial power processing. Therefore, the TP-AT shares some performance similarities with the TP-CT and TP-MMC even though they are not categorized together. The reason is that the TP-AT, TP-MMC and TP-CT all have the same amount of power being processed by the semiconductor switches in the p and s arms (see (5.9)). However, their transformers still process different amounts of power, ultimately resulting in different performance outcomes between them.

5.5.1 Ac power tapping

The first two columns in Fig. 5.4a compare the four different three-port MMCs for tapping different amounts of ac power from the dc ports, considering different dc step ratios $G_v = \{0.5, 0.8, 0.1\}$. There is a significant reduction in overall losses for the TP-AT, TP-MMC and TP-CT relative to the TP-F2F for $G_v = 400/200 = 0.5$ (cases $A1, A2$) and $G_v = 400/320 = 0.8$ (cases $B1, B2$). The TP-F2F also experiences higher semiconductor efforts, magnetic requirements and capacitive energy storage requirements. This outcome is due to the higher average power processed by the magnetics as well as the semiconductor switches for the TP-F2F, see (5.7)-(5.10),

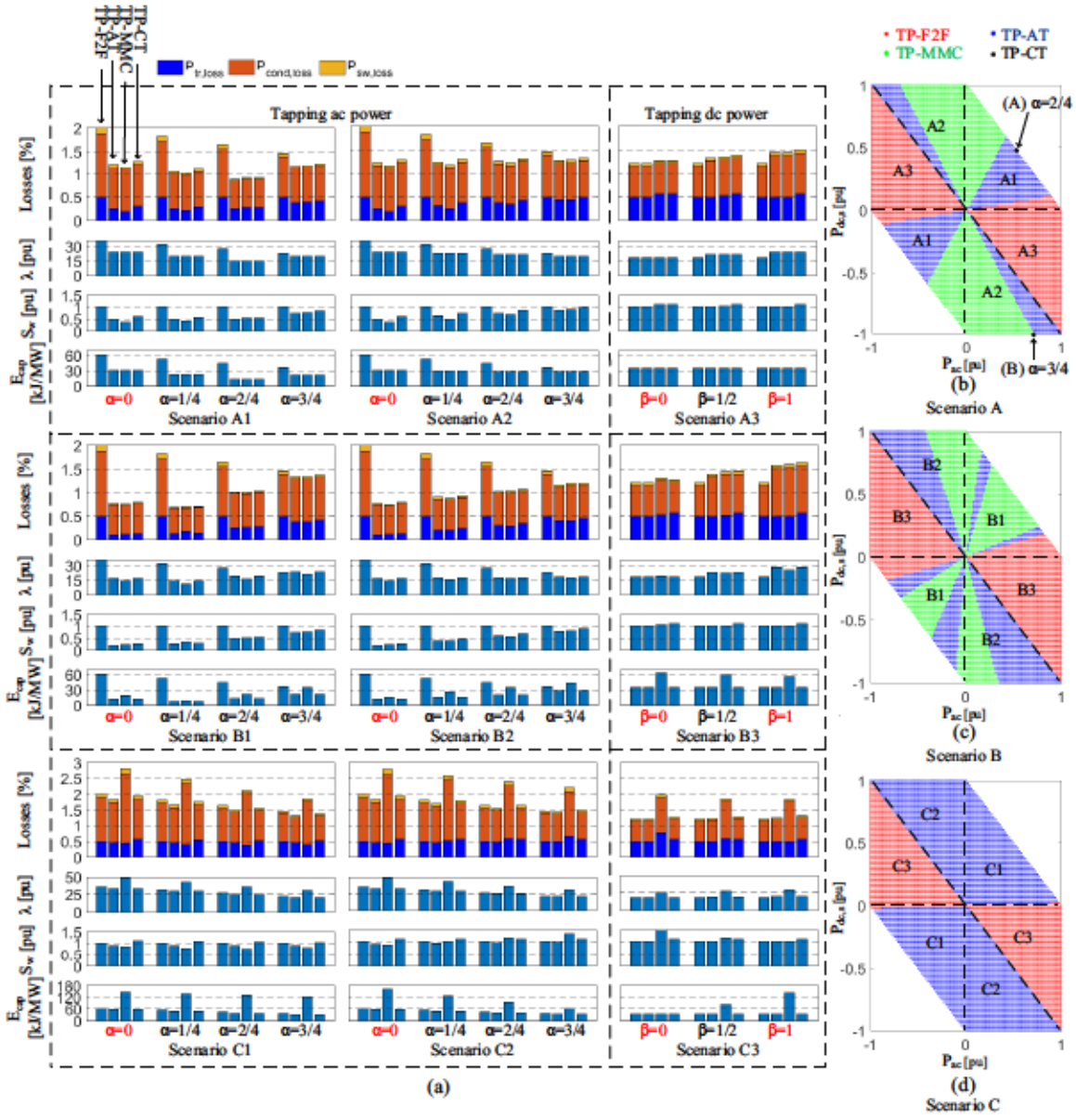

Figure 5.4: Results of comparative analysis for power flow cases in Fig. 5.3. (a) Bar graphs showing results for key values of α and β: semiconductor effort λ (normalized to P_{conv}), magnetics total Volt-Ampere rating S_w (normalized to $2P_{conv}$), capacitive stored energy E_{cap} and losses (normalized to P_{conv}). (b)(c)(d) topologies with lowest overall losses for all possible power flows in scenarios A, B, and C, respectively

due to the lack of partial power processing. The three-port topology with the lowest overall losses for every operating point in Scenarios A and B is shown in Figs. 5.4b[3] and 5.4c. respectively. Fig. 5.4b shows that in regions $A1$ and $A2$ (and $B1$ and

[3]To elucidate the connection with Fig. 5.3, two exemplar operating points in Fig. 5.4b are marked as point A ($\alpha = 2/4$ in region $A1$) and B ($\alpha = 3/4$ in region $A2$)

$B2$) the TP-MMC and TP-AT have the highest efficiencies, barring a small set of power flow conditions adjacent to region $A3$ (and $B3$) where the TP-F2F has lower losses. Although the TP-CT does not appear in Figs. 5.4b and 5.4c, it's important to highlight its performance is nearly identical to the TP-AT, regardless of dc step ratio, as quantified by the results in Fig. 5.4a. The TP-CT suffers from a slightly lower efficiency due to its slightly higher magnetics requirements, as the TP-CT transformer always handles both dc and ac currents while the TP-AT transformer handles only ac currents, see Figs. 5.2a and 5.2c. Figs. 5.4b and 5.4c show the benefits of the TP-MMC are most pronounced at $G_v = 0.5$ (cases $A1, A2$). The TP-AT exhibits increasingly higher efficiency as the dc step ratio increases from $G_v = 0.5$ (cases $A1, A2$) to $G_v = 0.8$ (cases $B1, B2$). This is seen by the reduction in green area (and corresponding increase in blue area) when contrasting Figs. 5.4b and 5.4c. In scenario B, the relative higher capacitive stored energy of the TP-MMC also makes it less attractive compared with the TP-AT.

The significant reduction in losses for the TP-AT, TP-MMC and TP-CT relative to the TP-F2F starts to diminish as the dc step ratio becomes smaller, seen in Fig. 5.4a for cases $C1, C2$ where $G_v = 400/40 = 0.1$. The power processed by the p and s arms for the TP-AT, TP-MMC and TP-CT are nearly the same as the TP-F2F as G_v approaches zero, see (5.7) and (5.10). Specifically, the extremely high current stresses in the TP-MMC at very low G_v makes its losses and capacitive stored energy even higher than the TP-F2F. The total stored energy for the TP-MMC in scenario C is over 140 kJ/MW. This is because the TP-MMC lacks a transformer for inter-arm ac voltage maximization that hinders low G_v application; the relationship between the arms ac current and voltage is given by (5.13). Fig. 5.5 shows the impact of arm ac voltage variations on the overall losses of the TP-MMC in Scenario C. The losses can be reduced by adjustment of $\hat{v}_{arm}$ based on power flow cases. For example, 200 kV can be considered as the optimal arm ac voltage for $\alpha = 3/4$ in case $C1$. In scenario C, $\hat{v}_{arm}$ is set to 100 kV for achieving relatively low losses in all cases. Among the four multiport topologies, the TP-AT has the lowest overall losses in cases $C1$ and $C2$, see Fig. 5.4d.

In summary, for power flow cases $A1, A2, B1, B2, C1, C2$ corresponding to ac power tapping, the TP-MMC has advantages over the TP-AT around $G_v = 0.5$. However, the TP-AT becomes increasingly more attractive over the TP-MMC as the dc step ratio deviates from $G_v = 0.5$. This is reflected by the change in dominance from green to blue in Figs. 5.4b through to 5.4d.

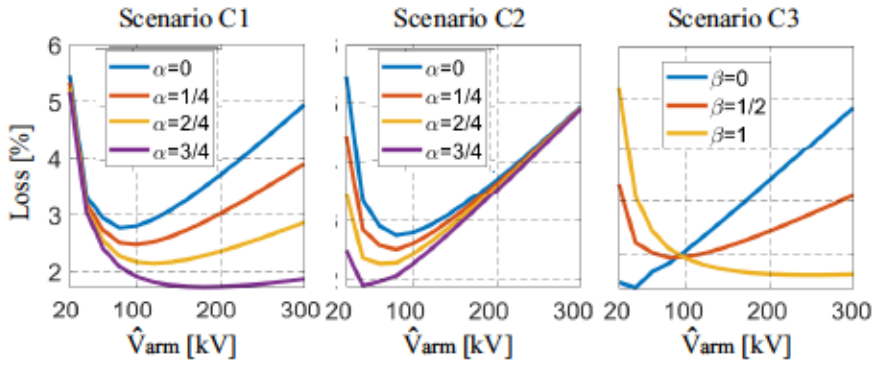

Figure 5.5: Losses of the TP-MMC of Scenario C for different arm ac voltages

5.5.2 Dc power tapping

The third column in Fig. 5.4a investigates the performance of the four topologies for tapping dc power from the other ports (cases $A3, B3, C3$). Interestingly, the TP-F2F has the superior performance across all dc step ratios for these cases (red dominates in regions $A3, B3, C3$ in Figs. 5.4b, 5.4c, 5.4d). The TP-AT, TP-MMC and TP-CT also have good performance, except for the TP-MMC in case C3. The TP-F2F has especially good efficiency when power is transferring between $V_{dc,p}$ and the AC port, as indicated by red text $\beta = 1$ in Fig. 5.4a. The results indicate the two-stage MMC structure of Fig. 5.1a is likely the preferred three-port topology for dc power tapping when interfacing HVDC and MVDC systems with a local ac grid.

5.6 Implications of Magnetics Solutions

The three-port MMCs in Fig. 5.1 utilize different magnetics solutions. The TP-F2F and TP-AT can use conventional three-phase three-winding ac transformers, which can be designed similar to conventional grid interfacing transformer. The transformer in the TP-MMC is a three-phase two-winding transformer, however, it has an open ended winding with a center tap on the converter side. The TP-CT utilizes transformer with dual zig-zag windings and an extra winding to create an ac grid interface. The TP-MMC has arguably the lowest complexity design while the TP-CT design is likely the most complex.

It is important to highlight the TP-F2F and TP-AT transformers must support dc voltage stresses between the two converter-side windings, while the TP-MMC and TP-CT do not have this issue. The transformer windings dc voltage stresses (relative to the grid side winding, $V_{w,g}$) for the four topologies are summarized in Table 5.2. The TP-F2F has a dc voltage bias of $1/2(V_{dc,p} - V_{dc,s})$ between primary

and secondary windings, while the TP-AT has a constant value of $1/2V_{dc,p}$. This is a notable drawback of the TP-AT as the converter-side windings must be insulated to tolerate 50% of the highest dc port voltage between them, regardless of the dc step ratio. The TP-MMC and TP-CT do not have any dc voltage stresses between primary and secondary windings. The additional dc voltage stresses between windings for the TP-F2F and TP-AT lead to increased magnetics size, weight and core design complexity.

Table 5.2: Magnetics Inter-Winding DC Voltage Stress Relative to Grid-Side Winding

	$V_{w,p}$	$V_{w,s}$	$V_{w,g}$
TP-F2F	$1/2\ V_{dc,p}$	$1/2\ V_{dc,s}$	0
TP-AT	$1/2\ (V_{dc,p} + V_{dc,s})$	$1/2\ V_{dc,s}$	0
TP-MMC	$V_{dc,s}$	N/A	0
TP-CT	$V_{dc,s}$	$V_{dc,s}$	0

The comparison in section 5.5 approximated the magnetics losses as 0.5% of the transformer total Volt-Ampere rating [51]. The inter-winding dc voltage stresses were not considered, similar to other comparative works [50, 51, 106]. That is, it did not account for an increase in the magnetic losses that results from increased size of the magnetics core, due to extra insulation requirements needed to accommodated inter-winding dc voltage stresses. Therefore, this section contrasts key comparison results for the four three-port MMCs that account for extra insulation requirements needed to accommodated inter-winding dc voltage stresses. The method introduced in 2.7.3 is used. The core area product A_p is used to quantify the impact of core power handling capability S_c and inter-winding dc voltage stress $V_{dc,iso}$ on the size, weight, cost and losses of the magnetics. For three-port MMC, the core power handling capability is the sum of the amount of power transferred by the primary p, secondary s and grid side g windings

$$S_c = S_{w,p} + S_{w,s} + S_{w,g} \tag{5.30}$$

K_u is modified to account for the corresponding copper fill reduction as follows for three-winding transformer used in three-port MMC

$$K_u = \frac{S_{w,p}}{S_c} K_{u,p} + \frac{S_{w,s}}{S_c} K_{u,s} + \frac{S_{w,g}}{S_c} K_{u,g} \tag{5.31}$$

Where $K_{u,p}$, $K_{u,s}$ and $K_{u,g}$ is window utilization factor obtained from (2.43) for windings at primary, secondary and grid side, respectively.

To estimate the total magnetics losses for the three-port MMCs where there is dc voltage stress between windings on the core, (5.29) is modified as follows

$$P_{copper,loss} + P_{core,loss} = 0.5\% \cdot S_w \cdot \left(\frac{A_p}{A_{p,nom}}\right)^k, \tag{5.32}$$

where A_p is the actual area product of the magnetic structure and $A_{p,nom}$ is the area product of the magnetic structure with the same power rating but without extra dc insulation requirement (i.e., with $V_{dc,iso} = 0$). Coefficient $k = 0.75$ represents the core volume-area product relationship [71].

The four three-port converter losses that accounts for the impacts of inter-winding dc voltage stresses are given in Fig. 5.6 considering the nine different power flow cases in Fig. 5.3. The three-port converter topology with the lowest overall losses are also plotted for every operating point in Scenarios A, B, C, respectively, for all possible values of α and β.

The insight from Fig. 5.6 suggests that accounting for inter-winding dc voltage stresses result in

- The TP-MMC becoming more attractive when tapping ac power (cases $A1$, $A2$, $B1$, $B2$) due to reduced magnetics size and associated losses;
- The TP-AT transformer having higher losses across all dc step ratios, potentially shifting preference to the TP-CT for certain power flow cases $C1, C2$.

5.7 Contrasting Two-port and Three-port Power Conversion

This section compares the losses and cost of realizing a three-port system using two options: (a) separate two-port dc-dc and dc-ac MMCs, and (b) one three-port MMC. The two-port dc-dc HVDC-AT [106] and the TP-AT in Fig. 5.1c are assumed in this case study comparison, along with the conventional two-port dc-ac MMC.

Fig. 5.7 illustrates an example scenario where DC_s (200 kV) and AC (220 kV) systems send an equal amount of power (200 MW) to DC_p (400 kV). Fig. 5.7b corresponds to the TP-AT in scenario $A1$ of Fig. 5.4a with $\alpha = 2/4$ (i.e. 50% of the power sourced from the ac port). In contrast, Fig. 5.7a uses the HVDC-AT and conventional dc-ac MMC. Note in Fig. 5.7a that operation of the HVDC-AT and MMC are respectively equivalent to power flow case $A2$ of Fig. 5.4a with $\alpha = 0$ (TP-AT operating solely as dc-dc converter) and power flow case $A3$ of Fig. 5.4a with $\beta = 1$

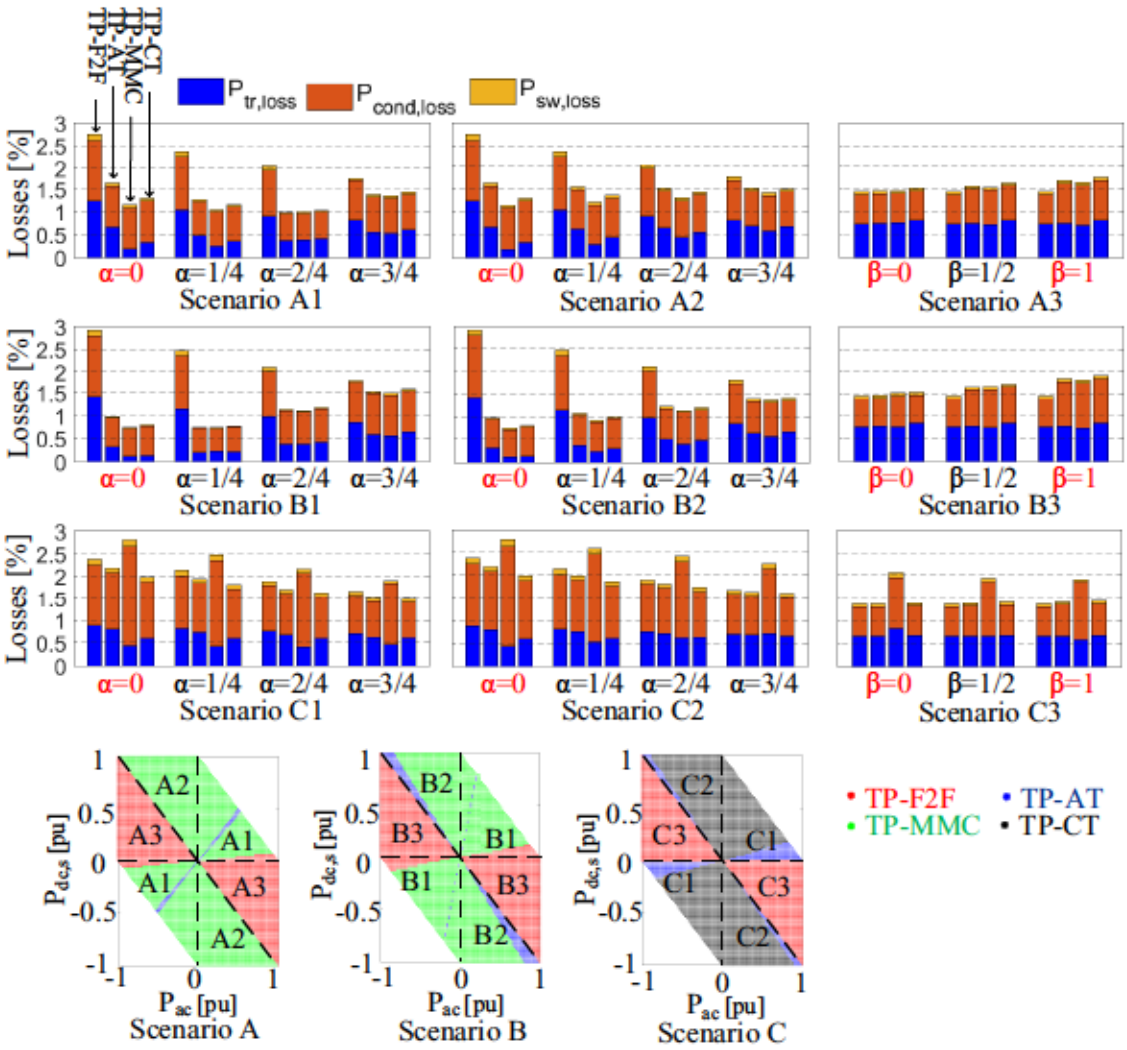

Figure 5.6: Results of comparative loss analysis (normalized to P_{conv}) for power flow cases in Fig. 5.3 considering inter-winding dc voltage stresses and topologies with lowest overall losses for all possible power flows in scenarios A, B, and C, respectively

(TP-F2F operating solely as dc-ac converter). The HVDC-AT is designed with sufficient number and type of submodules to provide black start capability similar to the TP-AT in Fig. 5.7b.

Fig. 5.7 shows that for identical port power flows the TP-AT option has approximately 29% lower losses than the two-port solution that requires multiple converters. Table 5.3 summarizes other key metrics for Fig. 5.7, showing significant reductions in semiconductor effort, magnetics Volt-Ampere rating and capacitive energy storage can also be realized with the TP-AT option. This points to a lower overall converter station footprint for the TP-AT.

The comparison in Fig. 5.7 is carried out to emphasize the potential benefits of

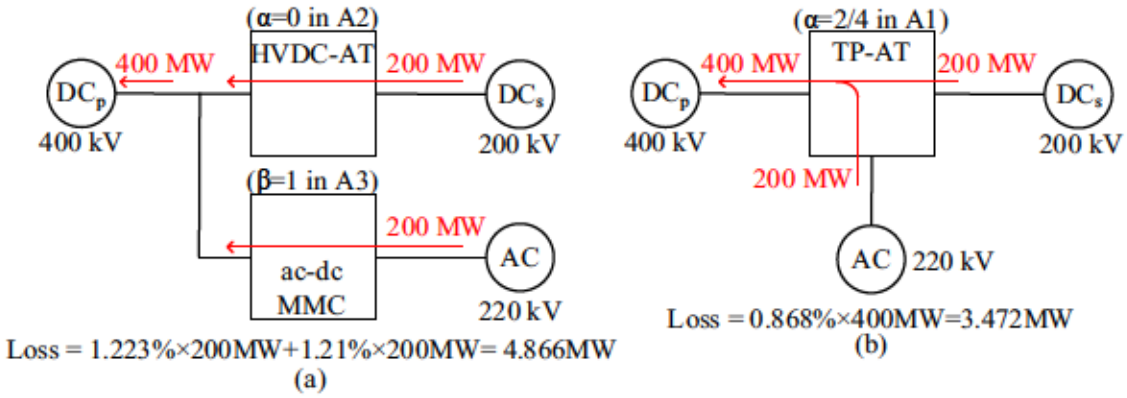

Figure 5.7: Configuration and losses for three-port systems that routes power between two different dc networks and an ac voltage ports using (a) separate two-port MMCs, (b) three-port MMC

Table 5.3: Comparison of Converter Arrangements in Fig. 5.7

	λ [p.u.]	S_w [p.u.]	E_{cap} [kJ/MW]
Two-port solution in Fig. 5.7a	21	0.75	33
Three-port solution in Fig. 5.7b	15	0.5	14

using three-port converters in comparison to deploying separate dc-dc and dc-ac converters. Depending on the application and port power flow demands, three-port converters can be attractive from the perspective of

- reducing overall system losses (roughly 30%);
- reducing investment cost including semiconductor effort, magnetics power rating and internal energy storage (roughly 35-50%).

From on these observations, two applications are identified for the three-port MMCs in Fig. 5.8. Separate dc/ac and dc/dc conversion stages in the dashed boxes of Fig. 5.8a can be replaced with the three-port MMCs in Fig. 5.8b. The feasibility of such three-port converter is being studied for the Synergies at Sea project of two planned offshore wind farms in the North Sea: one in the UK part and a second one in front of the Dutch shore [118] (left dashed box). The right dashed box in Fig. 5.8a can be replaced with the three-port MMC that interconnects two dc systems and one ac tapping station [16].

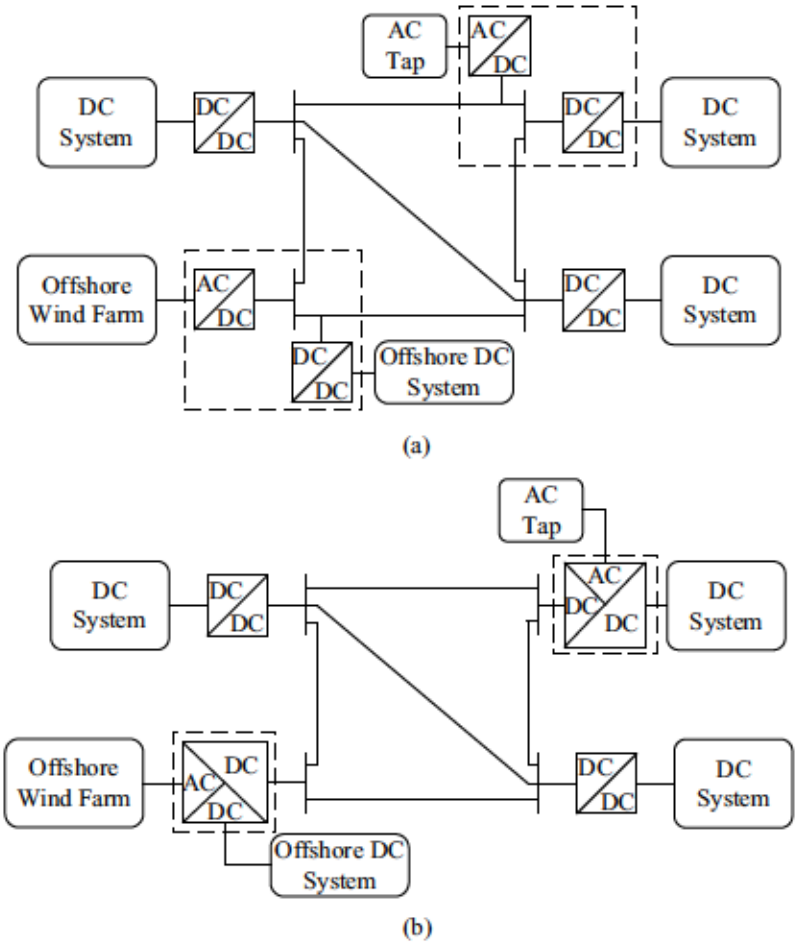

Figure 5.8: (a) Deploying separate dc-dc and dc-ac converters in hybrid ac/dc power systems (b) example application of three-port MMCs in hybrid ac/dc power systems

5.8 Exemplar Simulation Results

This section provides exemplary simulation results using PSCAD/EMTDC to verify the comparative analysis. Fig. 5.9 shows simulation results for the four three-port topologies in scenario $A1$ with $\alpha = 1/4$. With $V_{dc,p} = 400$ kV and $V_{dc,s} = 200$ kV, the upper and lower arms in the primary side of TP-F2F must support 200 kV_{dc} while upper and lower arms in the secondary side must support 100 kV_{dc}. The generated ac arm voltage are 180 kV_{ac} and 90 kV_{ac}. This is confirmed by Fig. 5.9a, where the resulting arm currents are also presented. The TP-MMC in Fig. 5.9c and TP-CT Fig. 5.9d have identical generated arm dc and ac voltages as the TP-F2F. The primary and secondary arms in the TP-AT only need to support 100 kV_{dc} as shown in Fig. 5.9b, with 90 kV_{ac} generated arm ac voltages. The SM capacitor voltages of all toplogies are successfully regulated to 2 kV. The transformer windings in the TP-F2F

and TP-AT for primary, secondary and ac grid side carry only ac currents. However, as expected, the transformer windings of the TP-MMC and TP-CT will carry both ac and dc currents. This is consistent with the analysis in Fig. 5.2.

Fig. 5.10 shows simulation results for the four three-port topologies in scenario $C1$ with $\alpha = 3/4$. With $V_{dc,p} = 400$ kV and $V_{dc,s} = 200$ kV, the arm voltages in the primary and secondary side of four topologies are notably different. The TP-F2F arms supports 200 kV_{dc} and 20 kV_{dc} in the primary and secondary arms respectively, while the TP-AT supports 180 kV_{dc} and 20 kV_{dc} respectively. 360 kV_{dc} and 40 kV_{dc} are generated in primary and secondary arms in the TP-CT to achieve primary dc voltage $V_{dc,p} = 400$ kV. The TP-MMC arms supports 360 kV_{dc} and 40 kV_{dc} in the primary and secondary side, respectively. With $\hat{v}_{arm} = 90$ kV, the TP-MMC have to generate negative arm voltages in the secondary side as shown in Fig. 5.10c.

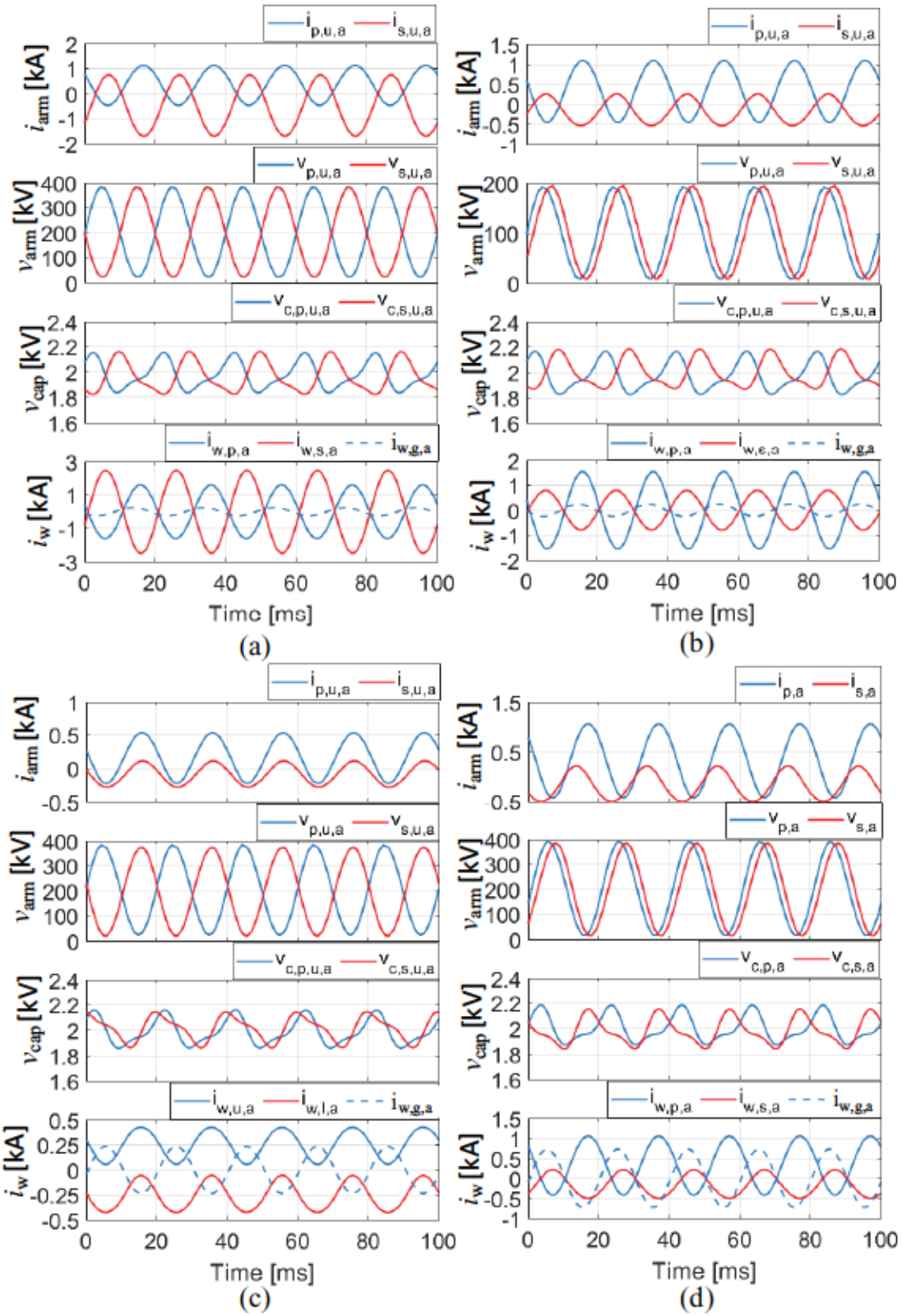

Figure 5.9: Voltage and current waveforms, where $V_{dc,p}$ = 400 kV, $V_{dc,s}$ = 200 kV, $V_{ac,LL(rms)}$ = 220 kV, $P_{dc,p}$ = 400 MW, $P_{dc,s}$ = -300 MW and P_{ac} = -100 MW: (a) TP-F2F, (b) TP-AT, (c) TP-MMC, (d) TP-CT

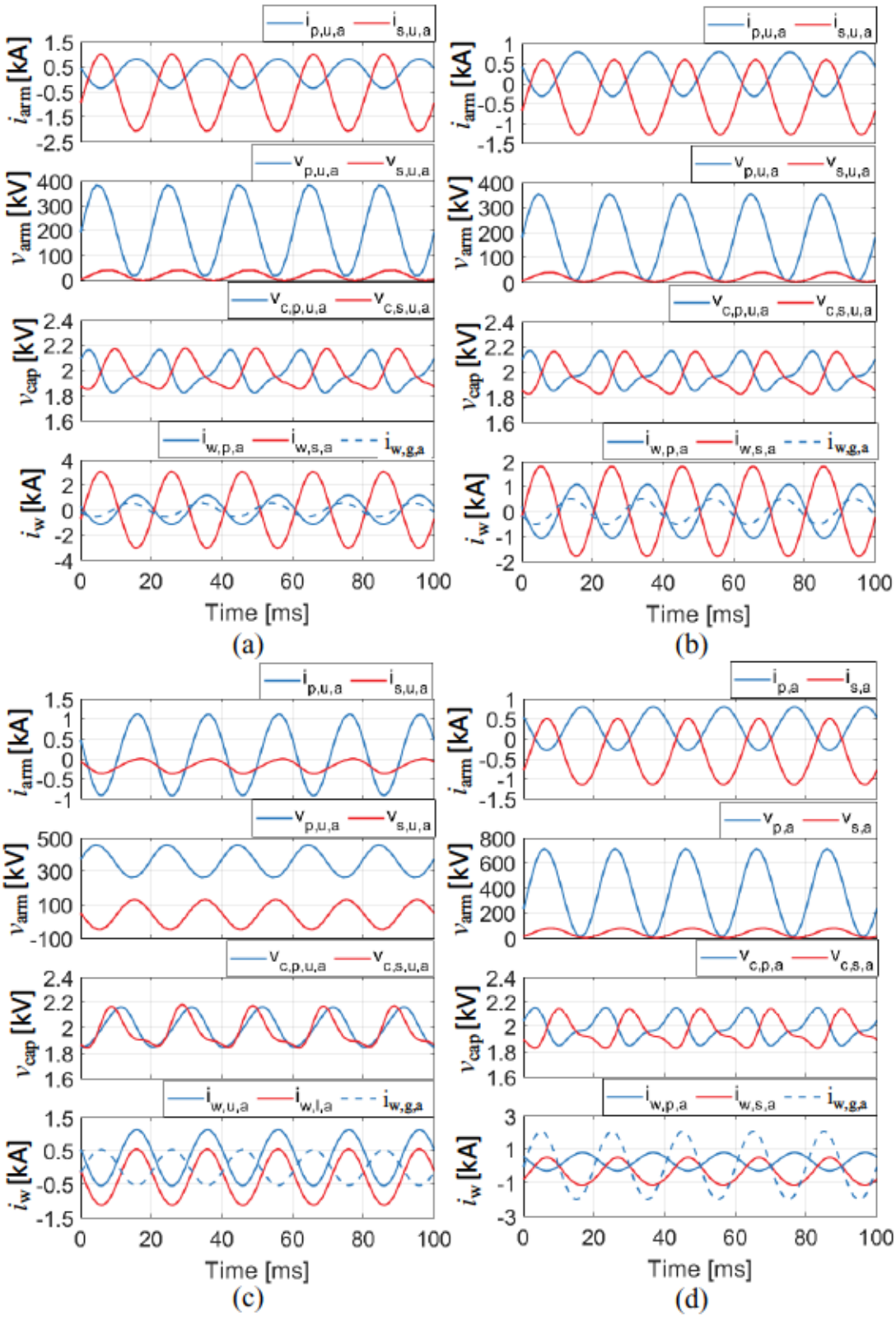

Figure 5.10: Voltage and current waveforms, where $V_{dc,p}$ = 400 kV, $V_{dc,s}$ = 40 kV, $V_{ac,LL(rms)}$ = 220 kV, $P_{dc,p}$ = 300 MW, $P_{dc,s}$ = -75 MW and P_{ac} = -225 MW: (a) TP-F2F, (b) TP-AT, (c) TP-MMC, (d) TP-CT

5.9 Chapter Summary

This chapter carries out a detailed assessment and comparison of four three-port MMCs for high power applications. The main contributions of this chapter are: 1) Classifying and assessing the emerging three-port MMCs based on their internal power transfer mechanisms, organized into two categories (i) three-port MMCs that use conventional transformers, and (ii) three-port MMCs that multitask transformers to realize multi-frequency power transfer mechanisms. 2) Carrying out a detailed comparative study between four representative three-port MMCs in terms of losses, semiconductor effort, energy storage and magnetics, considering a total of nine different power flow cases from three core application scenarios. The converters are designed to have fault blocking capability on all ports. The key findings are:

- The TP-MMC and TP-AT offer the best performance for ac tapping in three-port dc-dc-ac systems with moderate dc step ratios, e.g., 400/200 kV and 400/320 kV, where substantial savings in losses, semiconductors, capacitive energy storage and magnetics can be achieved relative to the TP-F2F. The TP-CT has a similar performance except for a slightly lower efficiency due to higher magnetics losses. The TP-MMC, TP-AT and TP-CT realize these benefits courtesy of partial power processing for the dc-dc stage, although the TP-F2F retains galvanic separation property. The benefits of the TP-MMC are most pronounced at $G_v = 0.5$, while the TP-AT performance becomes better as the dc step ratio deviates from $G_v = 0.5$. The TP-AT becomes the superior choice for ac tapping with low dc system step ratios, e.g., 400/40 kV, where the TP-MMC has prohibitively high current stresses.

- The TP-F2F has the best performance for dc tapping in three-port dc-dc-ac systems, with moderate reductions in losses, semiconductors, capacitive energy storage and magnetics relative to the other topologies depending on the power flows. Its internal transformer makes the TP-F2F well suited for interfacing HVDC and MVDC systems. The TP-F2F is the only three-port topology with galvanic separation between dc ports.

- The TP-CT and TP-MMC are the only three-port topologies without dc voltage stresses between converter-side transformer windings. This can simplify core design and reduce the magnetics size and losses. Accordingly, taking this into account, the TP-CT may become preferable over the TP-AT for ac tapping in three-port dc-dc-ac systems for certain power flow demands.

- A comparison between two-port and three-port converter systems for three-port dc-dc-ac applications shows the latter can achieve significant reductions in losses, semiconductor effort, capacitive stored energy and magnetics rating. Thus, three-port converters can be attractive alternatives to deploying separate two-port converters, helping to reduce converter station footprint and investment cost.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

This section summarizes the core thesis contributions and highlights potential future work.

6.1.1 Contributions

The main contributions of this work are:

1. Modular multilevel dc converter with inherent minimization of arm current stresses (Chapter 2)

   A new class of dc-dc MMC (M2DC-CT) that merges the best traits of current state-of-art non-isolated topologies is presented, which multi-tasks a center-tapped transformer (in series with the converter arms) to enable multi-frequency power transfer. It requires only a fraction of the dc power throughput to be internally circulated as ac power. The converter internal (arm level) power balancing mechanism via the proposed controller are validated by simulation and experiment. Simulation and experimental results also verify the core dc flux cancellation for the center-tapped transformer. Comparative analysis against existing dc-dc MMCs shows the benefits of the M2DC-CT are most pronounced at low and high dc step ratios where it has the highest efficiency and lowest semiconductor effort. This makes the M2DC-CT a good candidate for HVDC-to-MVDC interconnections, HVDC power tapping, interconnecting HVDC (or MVDC) systems with similar voltage levels, and dc line power flow controllers.

2. Multi-frequency dual MMC chain-link structure for bipolar dc systems (Chapter 3)

A multi-frequency dc-dc-ac dual MMC chain-link structure is proposed for bipolar dc systems to accommodate unbalanced dc pole power conditions. Unlike prior art that uses single MMC configuration, two MMCs are paralleled on their dc sides and their ac sides are coupled via a multi-tasking three-winding transformer with center-tapped (wye) converter-side windings. No penalty in transformer Volt-Ampere rating is incurred relative to a conventional two-winding ac transformer even though the windings currents can have multiple frequency components. A unified control scheme in the $\alpha\beta$-frame is developed to independently control power exchange with the ac grid and between the two dc poles while keeping submodule capacitor voltages balanced. The control scheme also allows additional functionalities such as reactive power injection and independent MMC control. The converter operation and control are validated by simulation and extensive experiment results.

3. Three-port MMC derived from multi-frequency dual MMC structure (Chapter 4)

   A three-port MMC that can act as a central hub for routing power between two different dc networks and an ac system is derived from the dc-dc-ac dual MMC structure proposed in Chapter 3. The unified $\alpha\beta$-frame controls are extended for the three-port application by assigning appropriate reference signals. The converter operation and control are validated by simulation and extensive experiment results. In addition, the capability of three-port MMC with FBSMs to block external faults is validated by simulation results.

4. Comparative Assessment of Three-Port MMCs for High-Power Applications (Chapter 5)

   A detailed assessment and comparison of the three-port multi-frequency MMCs against existing three-port MMCs is performed in terms of losses, semiconductor effort, internal energy storage and magnetics requirements. Three different network scenarios are investigated that include HVDC and MVDC applications with the requirement of fault blocking capability, covering several different power flow cases. The results reveal that i) three-port MMCs can be attractive from the perspective of reducing overall system losses and investment cost in comparison to deploying separate dc-dc and dc-ac MMCs, ii) three-port MMCs utilizing multi-frequency concept are good candidates for tapping ac power from the dc ports, and iii) the three-port multi-frequency MMCs becoming more attractive due to reduced magnetics size and associated losses when accounts for

extra insulation requirements needed to accommodated inter-winding dc voltage stresses.

6.2 Future Work

Interesting avenues of potential future work:

- Explore application of the M2DC-CT as a HVDC line power flow controller. This would require a dc step ratio around unity, suggesting the use of hybrid arms with a mixture of half and full bridge submodules to minimize semiconductor effort and maximize conversion efficiency.

- The proposed bipolar and three-port MMCs are capable of blocking ac faults, dc faults and even riding-through external faults by employing full-bridge submodules in the arms. Dc fault ride-through strategies should be developed and experimentally validated to enhance the reliability of the converter.

- The dual MMC structure of bipolar and three-port topologies allows each MMC to process up to 0.5 p.u. ac power independently. However, dc power cannot be transferred between dc ports during single MMC operation due to the inability to achieve dc flux cancellation in the transformer core. The solution is to enable monopole operation. That it, in case the SMs in one arm of the MMC are failed, instead of blocking the whole MMC, the corresponding three arms of two MMCs (six arms in total) can be blocked and afterwards isolated from the main circuit for maintenance. This avoids the dc flux saturation during dc power transfer. The control strategies and extra switch devices for monopole operation should be developed.

- The bipolar MMC derived from multi-frequency dual MMC structure allows independent dc pole power control. Two multi-frequency MMC structures can be coupled through their ac nodes to form a dc-dc converter. It can be used to interconnect two bipolar dc systems with significantly different voltage levels. This topology also allows multiple multi-frequency MMC structures connected in parallel at the low voltage side, to alleviate high current stresses, while offering advantages such as fully independent pole power control, absence of inter-winding dc voltage stress and high dc step ratio suitability.

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