Novel Full Range Soft Switched Single Phase Inverter Design, Optimization and Implementation

by

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Abstract

Single-phase inverters are widely used as an interface between the load (or utility grid) and DC energy resources such as photovoltaic systems or battery storage systems in low-power residential applications. There has been a trend in the industry to increase the power density of the converters, which saves costs by requiring less heatsink, enclosure and fewer components in developing commercial inverters. To improve the power density, normally the switching frequency of the converters is increased, which results in the reduction of passive filter and energy storage requirements of a converter. However, increasing the switching frequency leads to higher switching losses and lower efficiency, which can be avoided if soft-switching topologies are used. In commercial inverters, unlike DC-DC converters, achieving soft-switching is not normally straightforward due to the change in the operating point in a line cycle. This thesis focuses on the design and implementation of high-frequency, high power density, soft-switched single-phase inverters.

A soft-switching topology for a single-phase inverter is introduced, where an auxiliary circuit is added to a single-phase full-bridge DC-AC converter. The auxiliary circuit incorporates two active switches that are magnetically connected to the filter inductor of the inverter output filter. The auxiliary circuit does not add any components in the main power path, and does not need any floating gate driver. The proposed auxiliary circuit does not need any extra passive component, and the required coupling with the main circuit is achieved through a secondary winding on the inverter's output inductor. The coupled inductor's turns ratio provides an extra optimization variable to reduce the voltage stress on the switches and enables the utilization of faster switches. Moreover, a variable-timing method

controls the auxiliary circuit and reduces the conduction losses in the auxiliary switches. Experimental results exhibit a satisfactory performance of an implemented prototype and high switching frequency while maintaining the efficiency over a wide power range.

To provide soft-switching for the full-range of operation in the proposed inverter, a combination of unipolar and bipolar modulation is proposed. In addition, the proposed modulation guarantees soft switching for low duty cycles and non-unity power factors. A thorough loss analysis is performed to compare the losses in hard-switching and soft-switching cases and to justify the utilization of the auxiliary circuit. A design strategy based on this loss analysis is provided to implement an efficient design of the system.

Additionally, core losses in the filter inductor of inverters is studied, and a generalized equation is proposed to calculate the total core losses of inverter inductors for one 60Hz cycle. Utilization of this generalized equation in the design process of the output filter inductor of the inverter increases the speed and accuracy of the design and avoids over-designing of the filters. This core loss calculation method is also used in the loss analysis of the soft-switching inverter to predict an accurate core loss for the soft-switching inverter. Same generalization method is also employed to predict an accurate conduction loss in the inverter in a line cycle.

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Chapter 1

Introduction

Single-phase inverters are widely used in renewable energy systems as an interface between a DC energy source, such as photovoltaic system or battery storage system in low-power residential applications, and the utility grid (or an stand-alone system) [1–5]. There has been a trend in the industry for decades to build high-efficiency inverters with high power density. Increasing the power density of converters saves costs by requiring less physical material and fewer components in developing commercial inverters [6].

To improve power density of the power electronics converters, a design trend is to increase the switching frequency, which results in reduction of passive components size, such as reactive filters and energy storage units of a converter [7]. This is due to the fact that in power electronics switching converters, passive components store and release energy every switching cycle. Therefore, increasing the switching frequency reduces the energy stored in each switching cycle, which reduces the size requirements for passive components. However, increasing the switching frequency leads to higher switching losses that deteriorate the efficiency of the converter, and increases the of the switches. Therefore, increasing the switching frequency and subsequently power density is restricted by switching losses. There are a few switching losses that contribute largely to the significant losses caused by high switching frequencies. One of the most-dominant types of switching losses is the cross-over loss that happen as a result of the cross-over between voltage and current during the switching transition. In a switching cycle, two switching transition happens for each

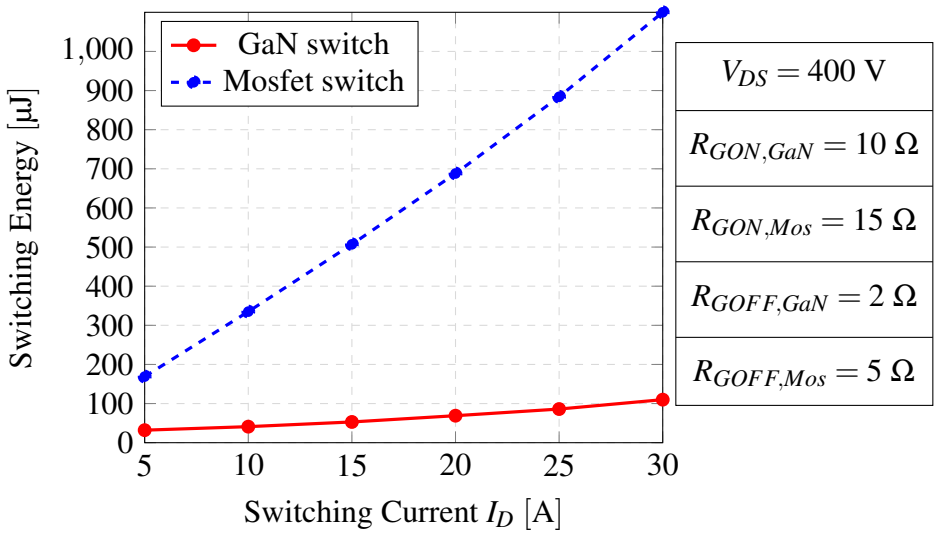


Figure 1.1: Total energy lost in turn-on and turn-off of Mosfet (Vishay SIHB35N60E) and GaN switch (GaN Systems GS66508T).

switch, one when the switch turns on and the other when the switch turns off. Therefore, two cross-overs between voltage and current happen, and each one of these transitions contribute to the switching losses of the converter. These cross-over losses happen as a result of decreasing the speed of the gate driver to avoid the voltage overshoot on the switches due to parasitic inductances in the components and also the printed circuit board (PCB) layout. As the speed of the gate driver is decreased, the voltage overshoot caused by the transient current and parasitic inductances becomes less. This decrease in the gate driver speed is important since it can allow the switches to operate in the safe operating area considering the voltage limit of the switches [6]. Therefore, to avoid losing efficiency, commercial inverters are usually limited to switching frequencies of up to 20kHz [8].

Fig. 1.1 illustrates the energy that is lost in a switching transition versus the current passing through the switches for a 650V Mosfet switch and a 650V Gallium Nitride (GaN) switch. It can be seen that for each switch, increasing the switching frequency can result in an increase in the efficiency drop caused by the hard-switching losses. Therefore, regardless of the switch semiconductor type, hard-switching losses can damage the efficiency and performance of the inverter. For example, in a 2kW and 100kHz buck converter

with 10A in the output, a Mosfet dissipates approximately 65 Watts, which is significant considering the total processed power by the converter. On the other hand, for a 2kW and 500kHz GaN-based inverter approximately 45Watts of power loss is expected. These hard-switching losses damage the efficiency of the inverter. To overcome this challenge in developing high-frequency compact converters, soft-switching methods can be utilized to increase the power density of the converter while obtaining high efficiencies [9]. These soft-switching methods are utilized to eliminate the cross-over losses that happen during the turn-on and turn-off of the switches by consuming relatively smaller power. Most of these methods focus on providing soft-switching through zero-voltage switching (ZVS) during turn-on transition of the switches. ZVS is a soft-switching strategy to ensure that during the turn-on of the switches, drain-source voltage of the switches reach zero before switches turn on and conduct current. Therefore, ZVS eliminates the cross-over between voltage and current transitions when switches turn-on, thus reducing the losses of the switches.

In DC/AC inverters, providing soft-switching for the switches becomes more challenging. This is because during a line cycle of operation, operating point of the inverter continuously changes in all four quadrants and hence, designing a soft-switching inverter requires soft-switching for the switches in all the operating points in a line cycle. In this chapter, existing methods for providing soft-switching for the inverter switches along with their shortcomings are reviewed, and subsequently, a soft-switching strategy with a novel topology and a novel modulation technique is introduced to increase the efficiency, power density and soft-switching range of single-phase inverters.

1.1 Review of Soft-switching Methods in Inverters

There have been extensive research in the literature to realize ZVS for inverter switches. These methods generally can be classified into three types:

- Triangular conduction mode (TCM),

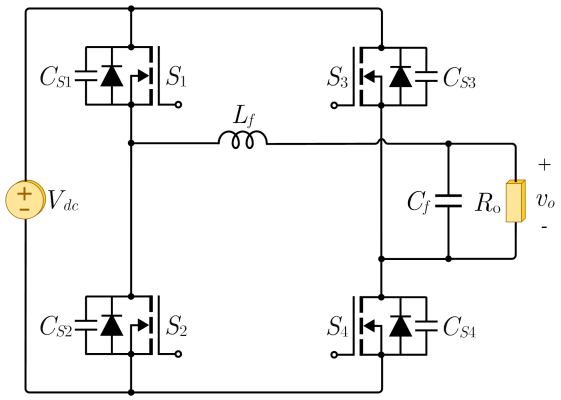


Figure 1.2: A full-bridge inverter circuit diagram.

- DC-side auxiliary circuit,
- AC-side auxiliary circuit.

In this section, these soft-switching methods are explained, and proposed methods in the literature are reviewed.

1.1.1 TCM Methods

TCM Method Operation Principles

First type of soft-switching methods are triangular current mode (TCM) methods. In these methods, generally, current ripple of the filter inductor is controlled in a way that in each switching cycle, filter current either reaches to zero or reaches to a negative value. To explain the TCM strategy for soft-switching, a full-bridge inverter is illustrated in Fig. 1.2. Assuming the output current is positive, in the left leg of the full-bridge, switch S_1 requires soft-switching. To provide ZVS to this switch, when the high current ripple reduces the filter current to zero or a negative value in a switching cycle, S_2 turns off and the deadtime between switches of this leg (S_1 and S_2) starts. During this deadtime, the output filter starts to resonate with the output capacitances of the switches. At the end of this resonance stage and before the deadtime ends, voltage of S_1 should reach zero, and at the end of the deadtime, S_1 should turn-on with ZVS. This process can be seen in Fig. 1.3 for two switching cycles of TCM soft-switching method in a half-bridge leg.

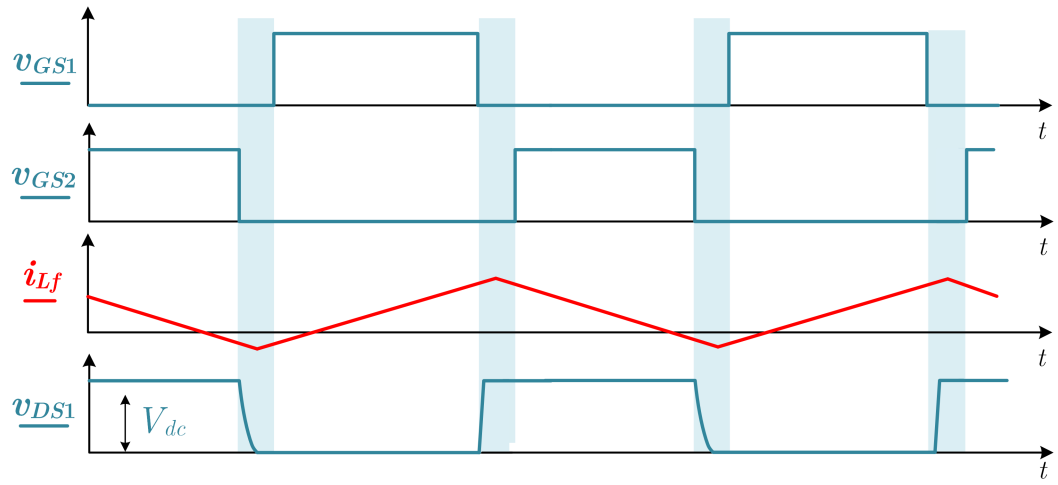


Figure 1.3: TCM soft-switching method operation waveform in two switching cycles for a half-bridge leg.

In TCM methods, there is generally no need for additional circuitry to provide ZVS for the switches. However, in each switching cycle, the time required to reduce the filter current to zero or a negative value should be calculated, resulting in a variable switching frequency due to wide-range of operation points in a line cycle [7, 10–13]. Variable switching frequency in inverters leads to undesired and unpredictable harmonic spectrum in the inverter output that makes the filter design challenging [4]. In non-unity power factors (PFs), the variation range of switching frequency in a line cycle gets much higher and results in a poor current quality, which makes the utilization of TCM method undesirable [14]. Therefore, TCM methods are best suitable for applications with unity PF. Besides, when TCM methods are used, the inductor current ripple is high, which results in higher turn-off losses, core losses and copper losses. In addition, due to the high peak currents passing through the switches and the output filter, components should be designed at higher ratings, which increases the cost of the components. In general, these methods are less attractive in single-phase inverters and are more applicable to three-phase inverters that require more simplicity in the implementation [10, 11, 15].

Review of Existing TCM Soft-switching Methods

In single-phase inverters, all TCM methods use the same operation principle of having high current ripple to change the direction of the switch current. In the literature, different TCM methods have been suggested to reduce the switching frequency variations of the inverters. A few of these methods are discussed in the following paragraphs.

In [7], three TCM techniques were utilized in a single-phase inverter, and their results were compared with each other. These three TCM current control techniques are:

- Boundary current mode (BCM), where a constant negative peak is set so that when the current reaches to this value, the next switching transition starts. Therefore, the period of switching cycle is dependant on the filter inductor voltage value.

- Constant hysteresis current mode (CHCM), where a constant ripple is set for each switching transition. This constant ripple guarantees that current in each switching cycle reaches to a negative value to achieve ZVS.

- Variable hysteresis current mode (VHCM), where the upper and lower limit of the current controller are determined based on each operating point, and therefore, the current band varies in each switching cycle.

In [7], it is reported that the utilized BCM method has switching frequency varying from 33kHz to 325kHz in a line cycle, CHCM method from 33kHz to 190kHz and VHCM method from 33kHz to 95kHz. Between these three current control techniques, BCM method causes the highest variation of the switching frequency, and CHCM has the highest RMS current passing through the filter.

In [12], a critical conduction mode (CRM) method is utilized for a GaN full-bridge, where switching transition starts when the current reaches zero, and when the switching transition happens, the voltage of the switch that needs soft-switching starts to decrease to reach zero. This method also results in a variable frequency in the range of 300kHz to 1MHz.

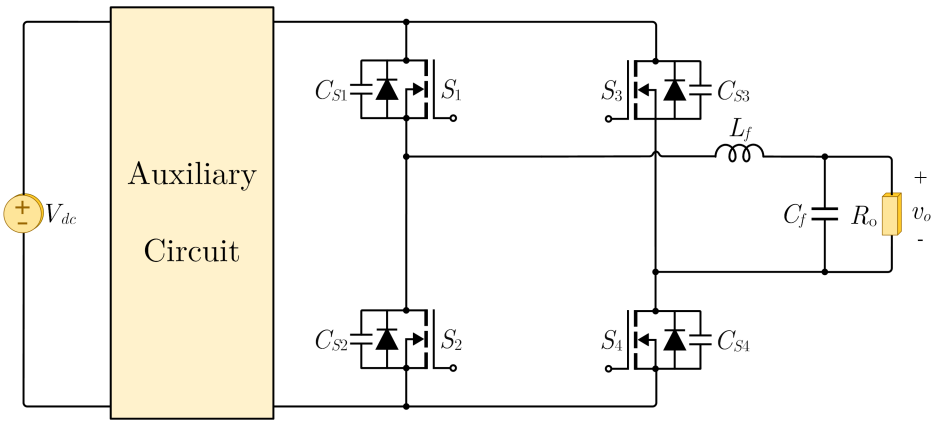


Figure 1.4: Circuit diagram of DC-side soft-switching methods.

In [13], a hybrid current control technique is implemented, where in higher duty cycles, a BCM-based method is used that has low RMS current value compared to other methods. However, in lower duty cycles, near zero-crossing, BCM current control technique results in the switching frequency. Therefore, it is suggested that in low duty cycles, the negative peak current should be increased like CHCM and VHCM methods, which have much lower switching frequency variation compared to BCM method.

As stated before, all three current control techniques are base on TCM current control, leading to variable switching frequency and high peak and RMS currents, higher losses and higher design requirements.

1.1.2 DC-side Auxiliary Circuit Methods

DC-side Auxiliary Circuit Methods Operation Principles

In the second type of ZVS methods, ZVS is provided through an auxiliary circuit placed in the DC-side of the inverter, as seen in Fig. 1.4. This auxiliary circuit is usually comprised of both active and passive components inserted between the DC bus and main switches of the inverter to drive the voltage of the full-bridge switches to zero during switching transitions [16–18]. Resonant DC-link (RDCL) and active clamped resonant dc-link (ACRL) inverters are two subcategories of DC-side soft-switching inverters, which have the disadvantage of increasing the voltage stress on the DC bus. Besides, as the auxiliary circuit is in the main

power path, power loss in the auxiliary circuit can lower the efficiency considerably [9]. In addition, the high DC-link resonant frequency in RDCL inverters causes undesirable sub-harmonics [19].

Review of Existing DC-side Auxiliary Circuit Methods

As seen in Fig. 1.4, DC-side auxiliary circuit methods have active and passive components installed between the DC-bus and the inverter. In the following paragraphs, some of the existing methods with a DC-side auxiliary circuit are reviewed.

In [16, 17], two RDCL methods with almost similar structures are utilized to provide ZVS for full-bridge switches. In both structures, the auxiliary circuit is composed of a resonant inductor, a resonant capacitor, a clamping capacitor and an auxiliary switch circuit. However, the arrangement of these components are different in each method. In [16], the clamping capacitor is located in series with the auxiliary switch as seen in Fig. 1.5. When the auxiliary switch turns on, the voltage on the resonant capacitor is clamped to the summation of DC-bus voltage and the clamping capacitor voltage. During the deadtime in the switching transition, the auxiliary switch turns off, and the output capacitors of the leg switches start to resonate with the resonant DC-link. At the end of the resonant stage, the voltage on the switches of the leg reaches zero, the body diodes are turned on, and the switches can turn on with ZVS.

In [17], the clamping capacitor is in series with the resonant inductor, as seen in Fig. 1.6. The advantage of this circuit compared to the other method is that the voltage stress on the switches equals to the DC-bus voltage, compared to the method in [16]. The operation principle of this method is almost the same as the method proposed in [16].

In both of these DC-side auxiliary ZVS inverters, there are four additional components needed for the auxiliary circuit. Also, in these circuits, auxiliary circuits are in the main power path. Therefore, high currents pass through the components. Moreover, the auxiliary switch has a high duty ratio to decrease the voltage stress of the full-bridge switches.

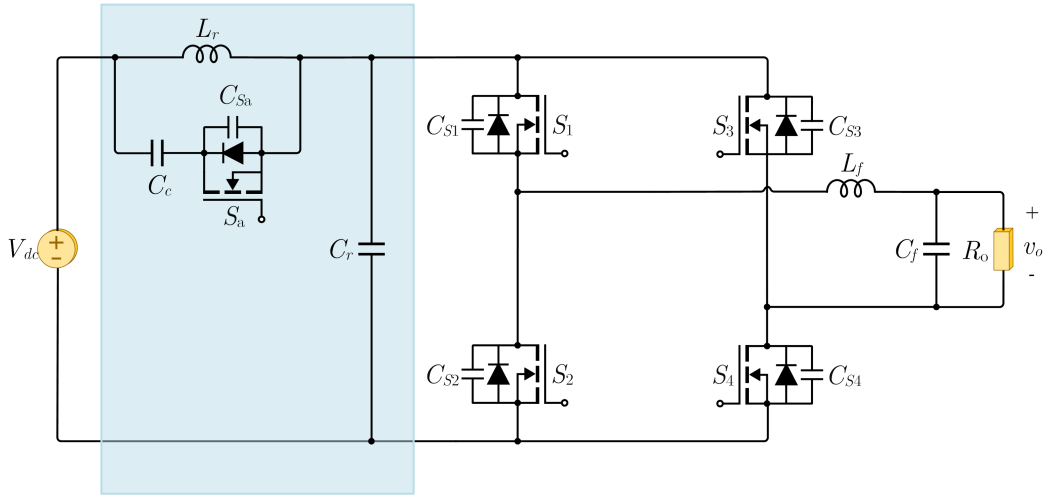


Figure 1.5: The DC-side auxiliary soft-switching topology in [16].

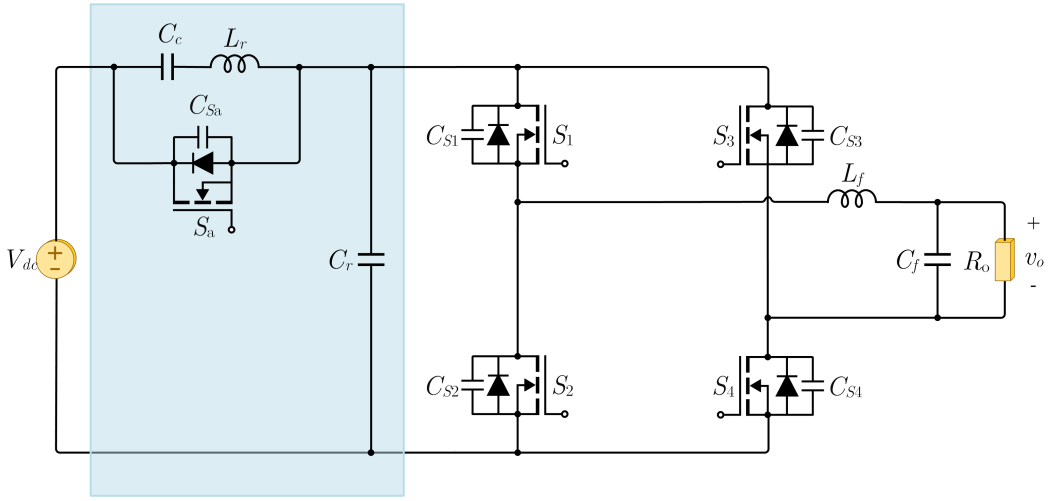


Figure 1.6: The DC-side auxiliary soft-switching topology in [17].

This high duty cycle results in high conduction losses. On the other hand, the resonant inductor conducts a current with high ripple resulting in both conduction and core losses in the inductor. The other disadvantage of these methods is the stress and undesirable sub-harmonics in the DC-link.

1.1.3 AC-side Auxiliary Circuit Methods

AC-side Auxiliary Circuit Methods Operation Principles

In the third type of ZVS methods, an auxiliary circuit is installed in the AC-side of the inverter to provide ZVS without changing the DC-bus voltage, as seen in Fig. 1.7 [20–26].

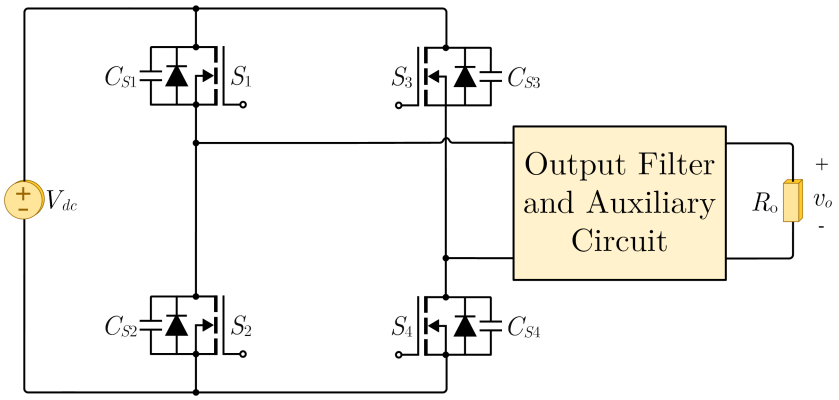


Figure 1.7: Circuit diagram of AC-side soft-switching methods.

In AC-side ZVS methods, a transition period is created by the auxiliary circuit to provide ZVS through a resonance stage, which is shorter than a switching cycle. The resonance usually happens between an inductor in the auxiliary circuit and the output capacitors of the switches. This auxiliary circuit, usually changes the $\frac{di}{dt}$ passing through the inverter terminal, which enables the current direction change in a shorter time than a switching cycle. Therefore, in this type, variable switching frequency is not required, which makes it suitable for applications with non-unity PFs. Some auxiliary circuits based on this method have been presented in the literature that are discussed in the following paragraphs.

Review of Existing AC-side Auxiliary Circuit Methods

In [20], an auxiliary resonant commutated pole (ARCP) is incorporated in a half-bridge leg as the auxiliary circuit. In this method, for each leg, two auxiliary switches along with a resonant inductor is inserted between the middle of the DC-link and middle of the half-bridge leg. This method can be expanded for a full-bridge inverter as shown in Fig. 1.8. In this method, before the switching transition starts, one of the auxiliary switches are turned on to charge the resonant inductor. During the deadtime in the switching transition, the resonant inductor starts resonating with the capacitors of the leg switches. In the resonant stage, the voltage of the switch that needs ZVS reaches zero, and after that it can be turned-on with soft-switching. Therefore, this AC-side auxiliary circuit removes the auxiliary circuit from the main power path, which results in lower conduction losses. Also, it doesn't change

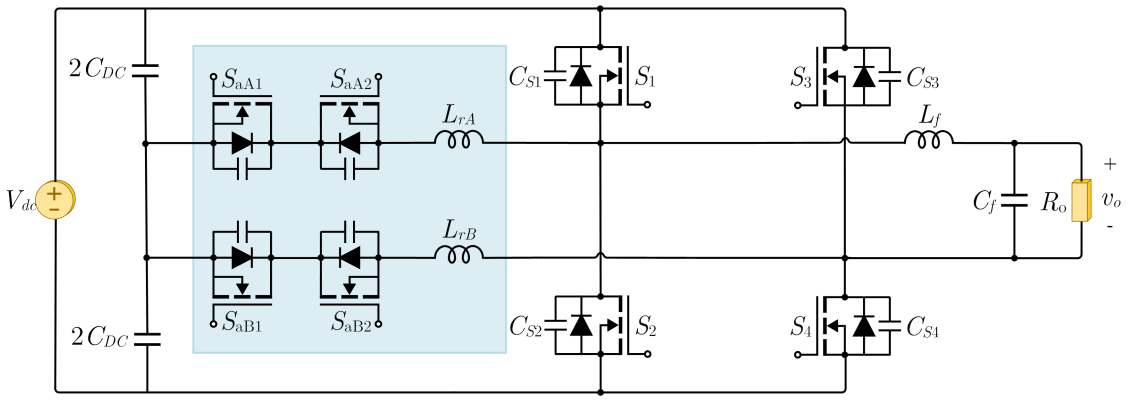


Figure 1.8: The AC-side auxiliary soft-switching topology in [20].

the DC-link voltage during the operation of the inverter. However, the ARCP circuit needs six additional components for a full-bridge inverter, and the resonant inductors reduce the power density of the inverter.

In [22], a soft-switching inverter is utilized with high efficiency and also reactive power capability. However, this method requires a high number of components for its auxiliary circuit, and has a complex magnetic structure. Besides, the switching frequency of 15kHz is selected that results in implementation of a low power density inverter. Another inverter with high number of auxiliary components is implemented in [23] to achieve soft-switching with low total harmonic distortion (THD). An AC-side auxiliary circuit with low number of components is presented in [24]. Although ZVS is achieved for full-bridge switches, the inverter can only operate with bipolar modulation technique, which has higher THD in the output compared to unipolar modulation. Although the designed prototype is tested in different PFs, 40kHz switching frequency of the inverter still suffers from low power density, and its auxiliary circuit adds another magnetic component, which further decreases the power density. It is worth mentioning that, auxiliary switches still need isolated gate drives.

In [25], a coupled-inductor based circuit is presented as the AC-side auxiliary circuit. In this circuit, in addition to a resonant inductor, only two switches are used to provide soft-switching for all four switches of the full-bridge as seen in Fig. 1.9. Moreover, a

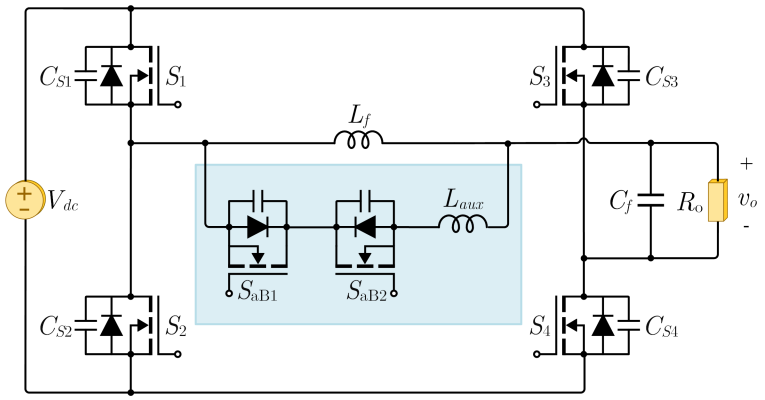


Figure 1.9: The AC-side auxiliary soft-switching topology in [25].

hybrid modulation technique is presented in this paper to achieve low THD and naturally adaptive auxiliary circuit current. However, in this circuit, the source pin of the switches are floating which requires isolated gate drivers. Besides, the presented hybrid modulation technique, similar to unipolar modulation technique, cannot provide soft-switching at low duty cycles in a line cycle due to the lack of enough energy provided to the inductor to excite the auxiliary circuit in a required time without interfering with the function of the full-bridge inverter. Losing soft-switching at low duty cycles might be justifiable in the unity PF. However, in non-unity PFs, where low duty cycles coincide with higher currents, the hard-switching losses would be considerable. Therefore, the converter is best suitable for unity power factor applications [25].

1.2 Proposed Soft-switching Method

In this thesis, a full-range zero-voltage-transition (ZVT) high-Frequency single-phase inverter is presented. The proposed inverter is composed of a full-bridge inverter and an ZVT auxiliary circuit on the AC-side.

1.2.1 Proposed Topology

The auxiliary circuit is comprised of two active switches and a resonant inductor that is coupled with the filter inductor as a coupled inductor as seen in Fig. 1.10. Therefore,

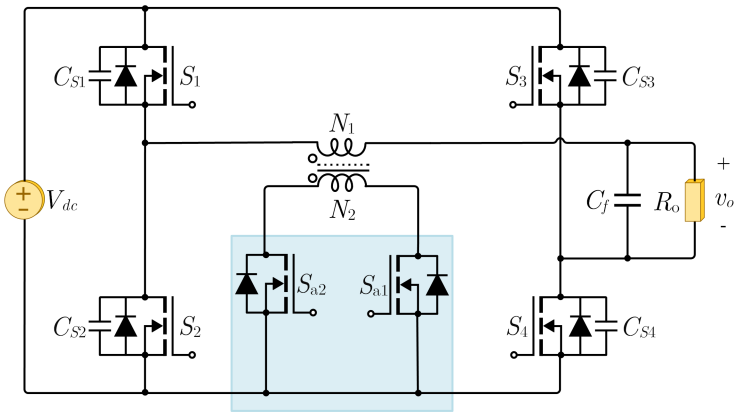


Figure 1.10: The proposed AC-side auxiliary soft-switching topology.

there are only two added components in the auxiliary circuit. Source pins of the auxiliary switches are connected to the dc-link ground. Therefore, the auxiliary circuit can be implemented using a minimum number of components as no isolated gate driver or additional magnetic components is needed, which leads to lower circuit complexity and cost [27]. The auxiliary circuit provides ZVS for full-bridge converter switches, while its switches are turned on and off with zero current switching (ZCS). The auxiliary switches are not in the main power path and their voltage stress is reduced by selecting the turns ratio of the coupled-inductor, which enables the use of switches with lower blocking voltage limit. Also, unlike the TCM methods, switching frequency doesn't vary with the operation point.

1.2.2 Proposed Modulation Technique

To achieve soft-switching for switches in full-range of operation including low duty cycles and non-unity PFs, a modulation technique based on combining unipolar and bipolar modulation techniques is proposed. Moreover, a variable timing strategy for the auxiliary switches is used that only requires sensors for the output voltage and output current of the inverter. Controlling the auxiliary switches with variable timing prevents the unnecessary operation of the auxiliary circuit and minimizes the RMS current in the auxiliary circuit.

1.3 Loss Analysis and Design of Output Filter Inductor of an Inverter

One of the major contributors to the total loss of the inverter, is the losses that happen in the magnetic components, which should be analyzed to optimize the design. Improved generalized Steinmetz equation (iGSE) and is proposed in [28] to predict the core losses of a piece-wise linear flux-density waveform. This method is used in this thesis to calculate core losses of the inverter inductor in a line cycle of operation accurately, and this method is used to design the inverter inductor. In addition, iGSE method is used to find a generalized equation for the core losses in the inverter inductor. This generalization results in an equation that can be used to find the core losses in a line cycle of operation of an inverter inductor regardless of the modulation technique. Therefore, loss analysis of the inverter magnetics can be calculated accurately, and this results in an efficient and easier design of the inverter inductor. Also, for the proposed inverter this generalized equation is employed to predict an accurate core loss in the loss analysis process of the design.

For the conduction losses, a generalized equation for calculation of the current passing through the inductor is derived. This generalized equation, along with an accurate inductor resistance calculation, calculates the total conduction losses of the inverter inductor accurately. Based on the loss calculations of the inverter inductor, a design methodology is proposed to minimize the total losses of the inverter inductor.

1.4 Thesis Objectives

The main objective of this thesis is to propose a full-range soft-switching single-phase inverter to increase the efficiency and power density of high-frequency inverters. To achieve this goal, a novel soft-switching inverter topology and modulation strategy are proposed to achieve full-range soft-switching. Briefly, the dissertation's objectives are:

1. To propose a new topology for soft-switching inverters that requires minimum com-

ponents and doesn't need a variable switching frequency;

2. To propose a new modulation technique for the novel topology to achieve a full-range soft-switching that causes high efficiencies in unity and non-unity power factors;

3. To analyze the operation principles of the proposed inverter in all four quadrants of output voltage and current;

4. To propose a design procedure for the proposed inverter that guarantees soft-switching for all the operating points of the inverter;

5. To derive a generalized equation for the inverter inductor core losses and conduction losses in a line cycle of operation;

6. To analyze the losses of the inverter in both soft-switching mode and hard-switching mode, and to compare the results to prove the superiority of the proposed inverter;

7. To explain a magnetic design method for the filter inductor of inverters considering a line cycle of operation; and

8. To verify the claims of the thesis and the inverter design by providing simulation and experimental results.

1.5 Thesis Outline

In chapter 2, the proposed soft-switching inverter topology is explained. The proposed inverter has an auxiliary circuit installed in the AC-side of a full-bridge inverter. This proposed auxiliary circuit only adds two active switches to the full-bridge inverter. The auxiliary circuit is magnetically coupled to the filter inductor of the full-bridge inverter. Therefore, the proposed inverter achieves high-power density along with high efficiency. The operation principle of the inverter with unipolar modulation strategy is explained, and

a design method is provided. At the end of the chapter, an experimental verification is provided by implementing a prototype of the converter.

Chapter 3 proposes a modulation technique for the proposed inverter in chapter 2, that is combined of unipolar and bipolar modulation strategies. This combined modulation technique improves the range of operating points that can have soft-switching in the inverter. The auxiliary circuit operation is described in all four quadrants of output voltage and output current, which covers all the operating points of the inverter in unity and non-unity power factors. A design method is explained to design a high-efficiency soft-switching inverter with high power density and full-range of soft-switching. A thorough loss analysis is done to exhibit insights on the performance of the proposed soft-switching inverter compared to a hard-switching full-bridge inverter.

In chapter 4, a generalized equation for the core loss of an inverter inductor is derived. This generalized equation, calculates the total core losses of the output inductor of the inverters in a line cycle of operation. This generalized equation can calculate the core losses regardless of the modulation technique. This generalized core loss equation for inverter inductors is employed to find the core losses for the proposed soft-switching inverter. Same generalization has been performed to find the conduction losses of the inverter inductor. Moreover, at the end of this chapter, a loss analysis has been performed on the proposed inverter, and a full-range soft-switching inverter with Mosfet semiconductors is developed. This prototype is a 400kHz, 1.5KW inverter. The experimental results on this prototype are provided to illustrate the performance of the system in full-range of operation.

Finally, chapter 5 summarized the contributions of the thesis and proposes a few possibilities for future research.

Chapter 2

Novel Soft-Switching Single-Phase Inverter Topology

2.1 Introduction

Implementation of a soft-switching strategy for the inverters, increases the efficiency of the inverter, and it can allow the inverter to be operated in higher switching frequencies, which can increase the power density of the inverter. In chapter 1, different strategies for providing soft-switching for inverters were discussed, and as explained, there are soft-switching methods that add additional components to the circuit to act as an auxiliary circuit to provide ZVS for the inverter switches. This section proposes a new auxiliary circuit for a single-phase full-bridge inverter that incorporates two switches that are magnetically coupled to the output filter inductor of the inverter. This auxiliary circuit provides the following features:

- Provides ZVS for the full-bridge switches.
- The auxiliary circuit switches turn off with ZCS.
- The proposed auxiliary circuit only adds two switches and their gate drivers to the full-bridge inverter.
- The auxiliary circuit is not on the main power path. Therefore, auxiliary circuit losses are low.

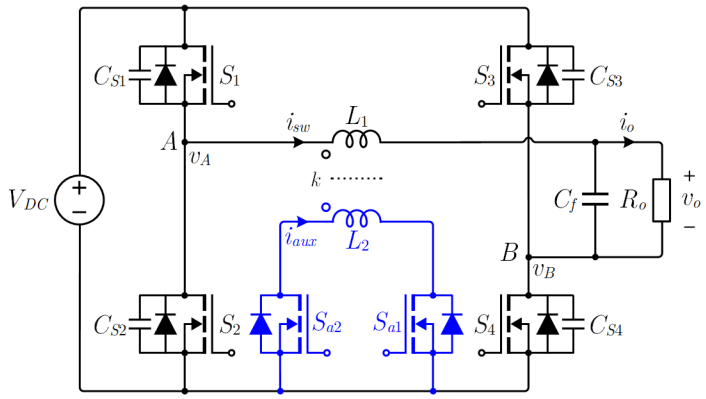


Figure 2.1: Proposed ZVT full-bridge inverter.

- Turns ratio of the coupled inductor adds the possibility of using auxiliary switches with lower voltage stress.
- The structure of the auxiliary circuit eliminates the need for floating gate drives for the added switches.
- A variable timing method is used for modulation of the auxiliary circuit that gives the most efficient way of modulating the switches, which only requires two sensors for the output voltage and current of the inverter.

In this chapter, the proposed topology is described in detail, and the operation principles of the inverter with unipolar modulation technique is discussed. Also, the design process of the proposed inverter is explained, and a 500W, 200kHz prototype with Gallium Nitride (GaN) switches has been developed to verify the claims on the topology.

2.2 Proposed Soft-switching Full-bridge Inverter

Fig. 2.1 shows the circuit configuration of the proposed ZVT single-phase full-bridge inverter. It is composed of a full-bridge inverter and an auxiliary circuit magnetically connected together. In Fig. 2.1, $S_1 \sim S_4$ are the switches of the full-bridge inverter, and C_f is the filter capacitor. The auxiliary circuit is composed of two active switches S_{a1} and S_{a2},

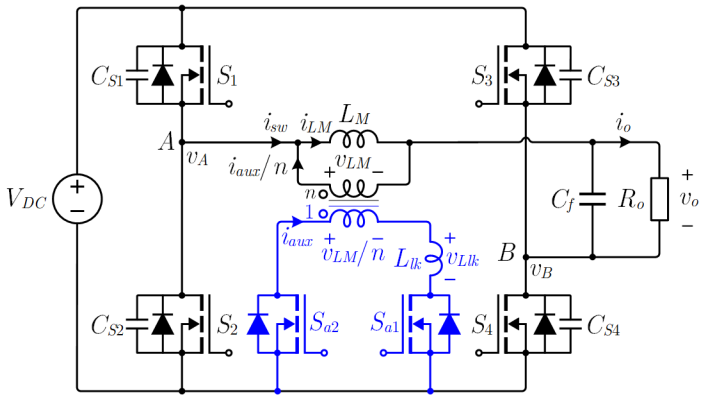


Figure 2.2: Equivalent circuit of the proposed inverter.

integrated into the filter inductor of the full-bridge inverter using a coupled inductor. To simplify the analysis, as shown in Fig. 2.2, the coupled inductor is modeled with a magnetizing inductor L_M, an ideal transformer with turn ratio of n, and a leakage inductor L_{lk} on the auxiliary circuit side. This leakage inductor represents the total leakage inductance of the primary and secondary windings. This is due to the fact that, when the inverter is operating without the auxiliary circuit, the primary leakage inductance acts as series with the magnetizing inductance, and since the primary leakage inductance is small compared to the magnetizing inductance, it can be neglected. On the other hand, when the auxiliary circuit is operating, secondary leakage inductance will be parallel to the magnetizing inductance. Therefore, the total coupled inductor inductance seen from the inverter is the summation of two leakage inductances. In the equivalent circuit of Fig. 2.2, L_M has the role of the inverter filter inductor. Also, L_{aux} is the leakage inductance seen from the primary side.

The comprehensive operation principles of the proposed inverter is discussed in later sections. Here, the overall operation of the proposed circuit is discussed. Regardless of the inverter modulation method or operating point, the general theoretical waveforms of the proposed inverter when $i_o > 0$ are illustrated in Fig. 2.3. As L_M is the inverter's filter inductor, it has two basic demagnetizing and magnetizing stages in which the energy in L_M is released and stored. The overall voltage and current waveforms of L_M are shown in Fig. 2.1 (c) where V_X and $-V_Y$ are determined by the inverter modulation method or inverter

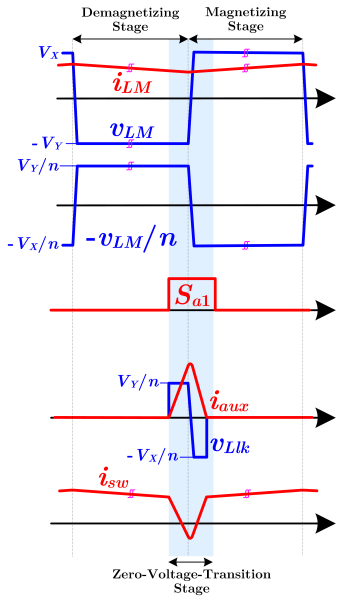
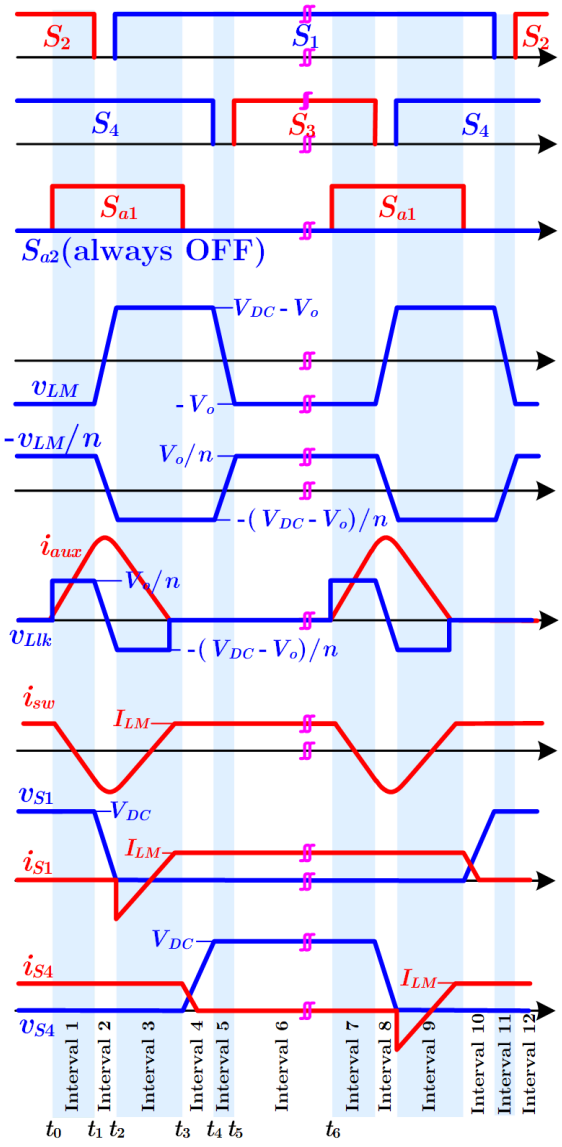


Figure 2.3: General theoretical waveforms of proposed inverter when $i_o > 0$.

operating point. As shown in Fig. 2.1 (b), the voltage of L_M is placed on the secondary side of the ideal transformer with a coefficient of $1/n$. Hence, we have two voltage levels of V_Y/n and $-V_X/n$ on the side of the auxiliary circuit, which are changed during the switching instants. If the auxiliary switch S_a is turned ON before the switching instant, the voltage of V_Y/N would be placed across L_{lk}. Hence, the current of L_{lk} and so i_{aux} is increased linearly. According to current arrows shown in Fig. 2.1 (b), as i_{aux} increases from zero, i_{sw} would be reduced linearly to zero and then flows in the negative direction (shown in waveform of i_{sw} in Fig. 2.1 (c)). This negative current is utilized to obtain ZVS in the inverter's switches. After that, the voltage level of L_M, and so, the voltage level of L_{lk} is changed. The negative voltage of $-V_X/n$ would be applied to the L_{lk}, and the current of i_{aux} is reduced to zero to provide ZCS turn-OFF for the auxiliary switch.

2.3 Soft-switching Inverter Operation Principles

In the unipolar modulation, the inverter operation includes two symmetrical half-cycles. Hence, only the first half-cycle of circuit operation is discussed here. Fig. 2.4 illustrates the



(a)

Figure 2.4: Theoretical waveforms in unipolar modulation at first quadrant ($v_o > 0, i_o > 0$).

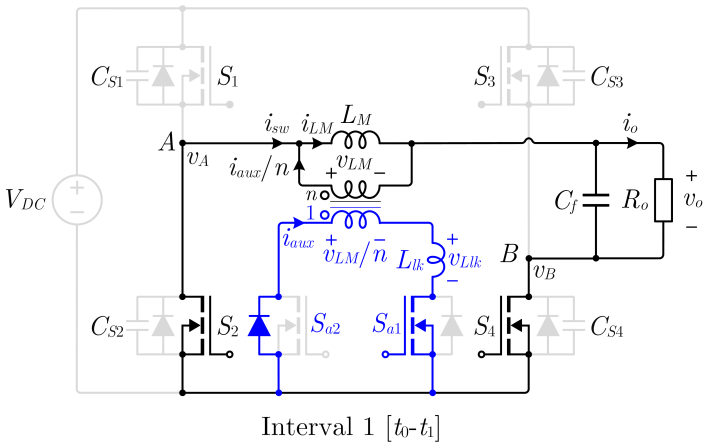


Figure 2.5: Inverter equivalent circuit in interval 1.

related theoretical waveforms for the first quadrant. Before the first interval, it is assumed that no current exists in the auxiliary circuit, S_2 and S_4 are ON and conduct i_{LM}. Besides, all other switches are OFF.

It should be noted that in the analysis, following assumptions are considered:

- The magnetizing inductor L_M is large and i_{LM} is constant during a switching cycle ($i_{LM} = I_{LM}$).
- The filter capacitor C_f is large and v_o is constant during a switching cycle ($v_o = V_o$).

Interval 1 $[t_0 - t_1]$: At t_0, auxiliary switch S_{a1} turns ON under ZCS due to L_{lk}. In this interval, the voltage across L_M is $-V_o$ ($v_{LM} = -V_o$). Hence, by turning S_{a1} ON, the voltage of V_o/n would be placed across L_{lk} ($v_{Llk} = V_o/n$). Consequently, the current of auxiliary circuit i_{aux} is increased linearly as follows:

$$i_{Llk}(t) = \frac{V_o}{nL_{lk}}(t - t_0), \tag{2.1}$$

Since i_{aux} enters the dotted terminal of the secondary side of the ideal transformer, the current of i_{aux}/n would exit the dotted terminal of the primary side as seen in Fig. 2.5, where the equivalent circuit in interval 1 is illustrated. Hence, the current of switches S_2

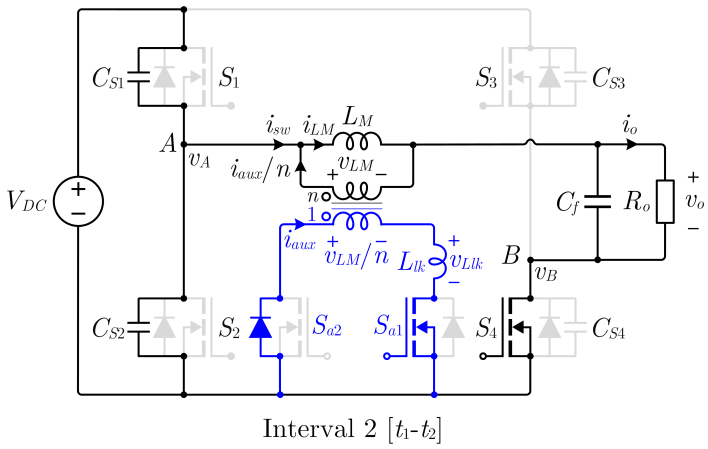


Figure 2.6: Inverter equivalent circuit in interval 2.

and S_4 (i_{sw}) reduces as follows:

$$i_{sw}(t) = I_{LM} - \frac{V_o}{n^2 L_{lk}}(t - t_0). \tag{2.2}$$

According to (2.2), i_{sw} reduces linearly to zero and then increases in the negative direction. Please note that the positive peak value of the auxiliary current i_{aux}, hence, the negative peak value of i_{sw} depends on the circuit operating point. To have a better-shaped harmonic spectrum for the current of i_{sw} passed through the filter, especially in low harmonics, it is desired to have a constant negative peak value for i_{sw}. This feature can be obtained with a variable timing-based strategy for the auxiliary switches. This issue is discussed in the section of design considerations.

Interval 2 $[t_1 - t_2]$: At t_1, S_2 turns OFF, and the negative current of i_{sw} charges C_{S1} and discharges C_{S2} through a resonance between L_{lk}, C_{S1}, and C_{S2}. The equations of i_{aux} and v_{S1} are obtained from:

$$i_{\text{aux}}(t) = \alpha_{uni} \sin\left[\omega_{r,uni}(t - t_2) + \beta_{uni}\right] + I_{LM}, \tag{2.3}$$

$$v_{S1}(t) = V_{dc} - V_o + Z_{r,uni}\alpha_{uni} \cos\left[\omega_{r,uni}(t - t_2) + \beta_{uni}\right], \tag{2.4}$$

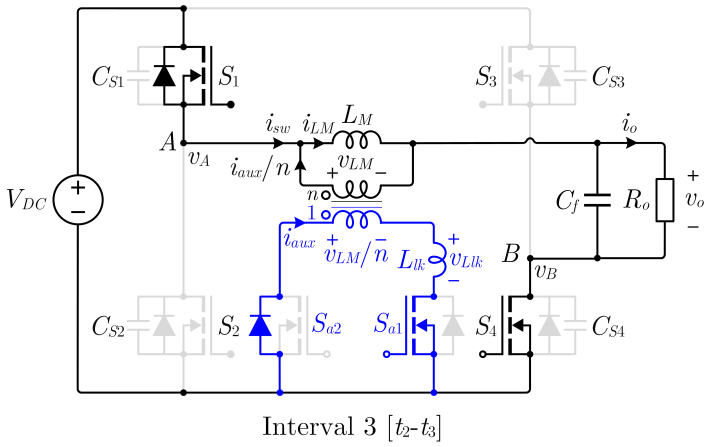


Figure 2.7: Inverter equivalent circuit in interval 3.

where we have:

$$\alpha_{uni} = \sqrt{\left(\frac{V_o}{Z_{r,uni}}\right)^2 + \left(i_{aux}(t_2) - I_{LM}\right)^2}, \tag{2.5}$$

$$\beta_{uni} = tan^{-1}\left(\frac{Z_{r,uni}\left(i_{aux}(t_2) - I_{LM}\right)}{V_o}\right), \tag{2.6}$$

$$Z_{r,uni} = n\sqrt{\frac{L_{lk}}{C_{S1} + C_{S2}}}, \tag{2.7}$$

$$\omega_{r,uni} = \frac{1}{n\sqrt{L_{lk}\left(C_{S1} + C_{S2}\right)}}. \tag{2.8}$$

At the end of this interval, C_{S1} is completely discharged, and its body diode turns ON to provide ZVS turn-ON for S_1. According to (2.4), to guarantee that the S_1 voltage reaches zero, the amplitude of the sinusoidal term $Z_{r,uni}\alpha_{uni}$ is designed more than the DC term $V_{dc} - V_o$. This issue is discussed in the section of design considerations. The equivalent circuit of this interval is shown in Fig. 2.6.

Interval 3 $[t_2 - t_3]$: At t_2, by conducting the S_1 body diode, S_1 turns ON under ZVS. In this interval, the voltage across L_M is $V_{DC} - V_o$ ($v_{LM} = V_{DC} - V_o$), and so, the voltage of $-(V_{DC} - V_o)/n$ would be placed across L_{lk} ($v_{Llk} = -(V_{DC} - V_o)/n$). Consequently, the current of auxiliary circuit i_{aux} is reduced linearly, and meanwhile, the current of i_{sw} increases

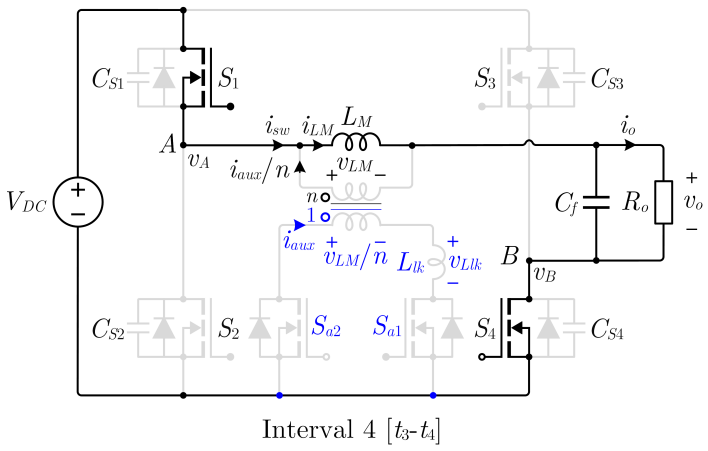


Figure 2.8: Inverter equivalent circuit in interval 4.

linearly. Before the end of this interval, i_{aux} reaches zero, and S_{a2} body diode turns OFF. Therefore, at the end of this interval, S_{a1} turns OFF under ZCS. The equivalent circuit of this interval is illustrated in Fig. 2.7.

To guarantee the ZCS condition of the auxiliary switch at turn-OFF in all the operating points, the conducting-time of the auxiliary switch should be appropriately selected such that the current of i_{aux} is reduced to zero in the full-range circuit operation. This issue is discussed in the section on design considerations.

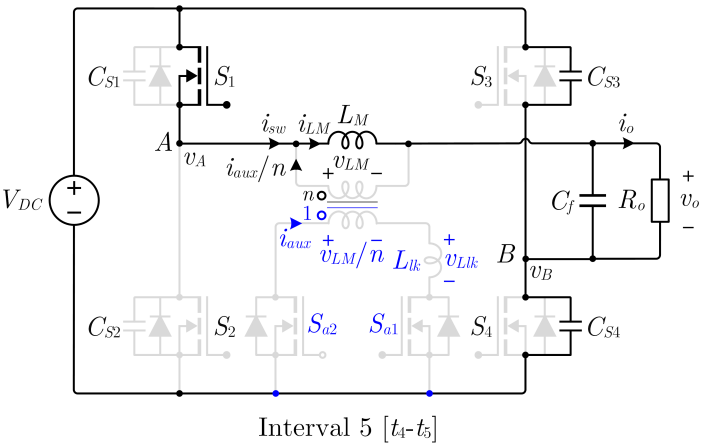


Figure 2.9: Inverter equivalent circuit in interval 5.

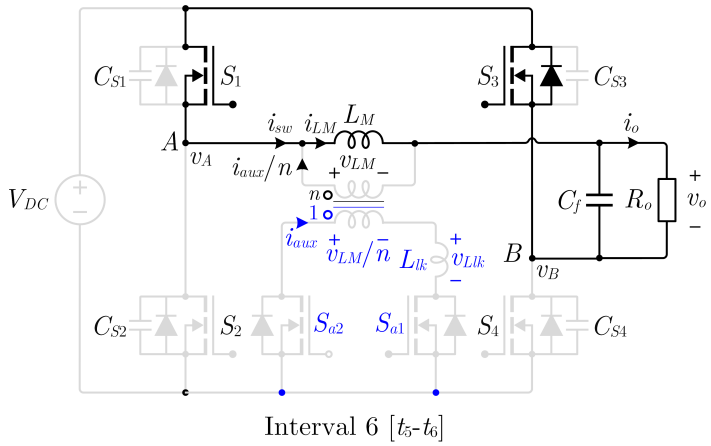


Figure 2.10: Inverter equivalent circuit after interval 6.

Interval 4 $[t_3 - t_4]$: In this interval, S_1 and S_4 are ON. The voltage of $V_{DC} - V_o$ is placed across L_M ($v_{LM} = V_{DC} - V_o$), and L_M is magnetized. The equivalent circuit of this interval is illustrated in Fig. 2.8.

Interval 5 $[t_4 - t_5]$: At t_4, S_4 turns OFF. Therefore, C_{S3} discharges and C_{S4} charges by i_{LM}. At the end of this interval, C_{S3} discharges completely, and S_3 body diode turns ON. The equivalent circuit of this interval is illustrated in Fig. 2.9.

Interval 6 $[t_5 - t_6]$: At t_5, by conducting S_3 body diode, S_3 turns ON under ZVS. In this interval, the voltage of $-V_o$ is placed across L_M ($v_{LM} = -V_o$), and L_M is demagnetized.

At t_6, the next half-cycle of the switching cycle begins which is symmetrical to the operation of the first half-period and its discussion is omitted here. The equivalent circuit of this interval is illustrated in Fig. 2.10.

2.3.1 Soft-switching Limitation with Unipolar Modulation

In the soft-switching process, there is a limitation in the unipolar modulation for the proposed soft-switching strategy. In low duty cycles, turning the auxiliary switches ON can interfere with the main switches and draws unnecessary current. For example, in the first quadrant, when the duty cycle is low, (2.1) can be re-written as,

$$i_{Llk}(t) = \frac{mV_{dc}}{nL_{lk}}(t - t_0). \tag{2.9}$$

where m is the duty cycle.

Since in this equation, m is low, the time needed for drawing a sufficient amount of current will increase. As a result, the time needed for the auxiliary switch to stay ON will increase, and it interferes with the next switching transition. Fig. 2.11 illustrates switching action in unipolar mode in low duty cycles. It can be seen that when the duty cycle is near zero, the distance between two switching transitions is small, which indicates a short distance between two switching actions of the main switches. During this short interval, S_1 won't turn off in time, and when the next switching action in the full-bridge happens, there will be an unnecessary current drawn from the auxiliary circuit. This unnecessary current keeps increasing until S_{a1} turns off, and when S_{a1} turns off, it turns off without ZCS, which leads to even more losses. Therefore, in unipolar mode, when the duty cycle is smaller than a certain value that doesn't allow for the auxiliary circuit to turn-off in time, there will be additional losses. in [25], auxiliary circuit turns off in low duty cycles, and soft-switching is lost. This strategy can lead to considerable cross-over losses in low power factors, when low output voltage aligns with a high output current.

2.4 Soft-switching Inverter Design

To achieve the best performance, converter parameters should be designed optimally. For the proposed converter, there are a few parameters that should be considered in the design process:

2.4.1 Switch Selection

For the full-bridge switches, GaN switches are used. Due to their small parasitic capacitance, the required leakage inductance for charging and discharging the capacitor would be small. Therefore, conduction losses in the auxiliary circuit will be smaller, and it also

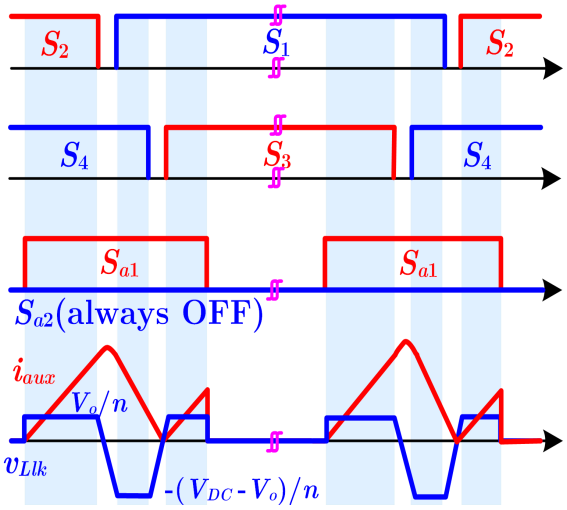


Figure 2.11: Unipolar modulation in low duty cycles when auxiliary circuit causes problem.

results in a more compact converter[29]. GaN Systems GS66506T are the switches chosen for the full-bridge. Small parasitic capacitance of the switches, plays an important part in the resonant stage, which can be seen in (2.8). This value will be used for finding other parameters. Also for auxiliary switches, GaN Systems GS66508T are chosen. This selection decreases the energy lost by the ringings when the switches are off. This can be seen in the following equation,

$$E_{oss} = \int_0^{V_{ds1}} C_{oss1}(V)V\,dV + \int_0^{V_{ds2}} C_{oss2}(V)V\,dV \tag{2.10}$$

This equation shows the stored energy in the output capacitances of the auxiliary switches C_{oss}. By having low output-capacitance auxiliary switches, E will be low, and therefore ringing losses are decreased. Also, by reducing the voltages on the switches ringing losses can be reduced which will be implemented in the next paragraph. However, the value of C_{oss} varies with the drain-source voltage V_{ds}. To make sure that the design is accurate effective values of C_{oss} are used from the data sheet.

2.4.2 Magnetic Design

Design of the coupled inductor is the main part of the design process since it will determine the values of L_{aux}, L_M and turns ratio. L_M, alongside with C_f, are the output LC filter. On

the other hand, L_{aux} is the inductance that resonates with the switch output capacitors. As it can be seen in (2.8), the value of L_{aux} affects the amplitude and the frequency of the resonance stage along with C_1 and C_2. To guarantee that in all the operating points, the voltage of the switches output capacitors reach zero through a resonance cycle, in (2.4), $v_{S1}(t)$ should always reach zero.

$$v_{Cr1}(t) \leqslant 0 => Z_{r,uni}\alpha_{uni} \geqslant V_{dc} - V_o. \tag{2.11}$$

When selecting the turns ratio of the coupled inductor, it should be considered that there are ringings in the auxiliary circuit and these ringings can increase the voltage stress of the switches. Choosing a proper value for the turns ratio decreases the voltage stress on the auxiliary switches and enables the utilization of switches with low output capacitances like 650V GaN switches. This will reduce the losses due to the ringings in the auxiliary circuit as it can be seen in (2.10).

2.4.3 Negative Peak of the Main Switch Current ($I_{sw,neg}$)

The negative peak of the main switches current, $I_{sw,neg}$, is equal to $(i_{aux}(t_2) - I_m)$ and it affects the capacitance discharge rate in the resonance stage. Its value should be greater than zero and equal to a specific value to guarantee the soft-switching condition for switches in all the operating points. Hence, the ZVS range of the converter switches is directly affected by $I_{sw,neg}$. By replacing $(i_{aux}(t_2) - I_m)$ with $I_{sw,neg}$ in (2.5) and (2.6) following equations can be derived.

$$\alpha_{uni} = \sqrt{\left(\frac{V_o}{Z_{r,uni}}\right)^2 + I_{sw,neg}^2}, \tag{2.12}$$

$$\beta_{uni} = tan^{-1}\left(\frac{Z_r I_{sw,neg}}{V_0}\right). \tag{2.13}$$

As it can be seen, α and β depend on both the resonance impedance and $I_{sw,neg}$. Therefore, values of $I_{sw,neg}$ and L_{aux} can have a spectrum of values that can satisfy the ZVS

condition. However, To choose an optimum value to have an efficient converter, different losses are considered.

2.4.4 Charge Time of the Leakage Inductance (t_{ch})

When the auxiliary circuit is activated, its current will increase linearly. To guarantee the ZVS condition, the auxiliary circuit current should reach $I_{sw,neg} + I_m$. The time interval needed by the auxiliary circuit to increase its current up to $I_{sw,neg} + I_m$ should be calculated by the MCU in all operating points online. The needed time is obtained from (2.2). I_m in (2.2) is sensed by a current sensor placed in the output of the converter. Therefore,

$$t_2 - t_1 = t_{ch}, \tag{2.14}$$

$$i_{aux,ch} = I_m + i_{sw,neg}, \tag{2.15}$$

$$t_{ch} = \frac{(L_{aux} i_{aux,ch})}{V_o}. \tag{2.16}$$

Table 2.1: Parameter Values

Parameter	***Value***	***Parameter***	***Value***
V_{dc}	400V	Frequency	200kHz
Power	500W	C_f	10 μF
Line frequency	60Hz	Power Factor	1
C_{oss}	49 pF^*	$I_{sw,neg}$	1A
L_M	200μH	Deadtime	30ns
L_{aux}	2μH	m_{min}	0.13
n_1/n_2	1.5	t_{aux}	600ns

*Effective values of C_{oss} are different.

2.4.5 Active Time of the Auxiliary Circuit (t_{aux})

t_{aux} is the time duration that auxiliary switches are turned-on. The minimum value for t_{aux} is determined by calculating the time required for the auxiliary current to reach its peak and go back to zero after the resonance stage.

$$t_{aux} \geq (t_{ch} + t_{dt} + t_{discharge})_{max} \tag{2.17}$$

Where t_{dt} and $t_{discharge}$ are deadtime and the time required for i_{aux} to reach zero. Therefore, t_{aux} can be selected by calculating the required time by the auxiliary circuit to provide ZVT for the main switches and also to be turned off under ZCS condition.

2.4.6 Soft-switching Range

As V_o decreases, t_{ch} will get higher. However, when V_o is low, t_{ch} would be too high, causing the auxiliary circuit to interfere with the main function of the inverter switches. This leads to high unnecessary current in the auxiliary circuit. To prevent this, in [25], the auxiliary circuit is deactivated for low duty cycles. Since t_{aux} is selected, the time that the auxiliary circuit is ON is known. As a result, the duty cycle that auxiliary circuit starts to interfere with the circuit can be known.

By solving the equations for different possible parameter values system is designed optimally, which accounts for providing soft-switching for all the operating points and also low auxiliary losses, which increases the converter efficiency. These values, alongside the system parameters are reported in Table 2.1.

2.5 Experimental Results

The simulation of the proposed converter is done using the PSIM software and the magnetic component is simulated using Ansys Maxwell. Simulation results show that ohmic losses are decreased due to the variable timing strategy that leads to less RMS values of current. To show the validity of the proposed circuit, a 500W prototype converter oper-

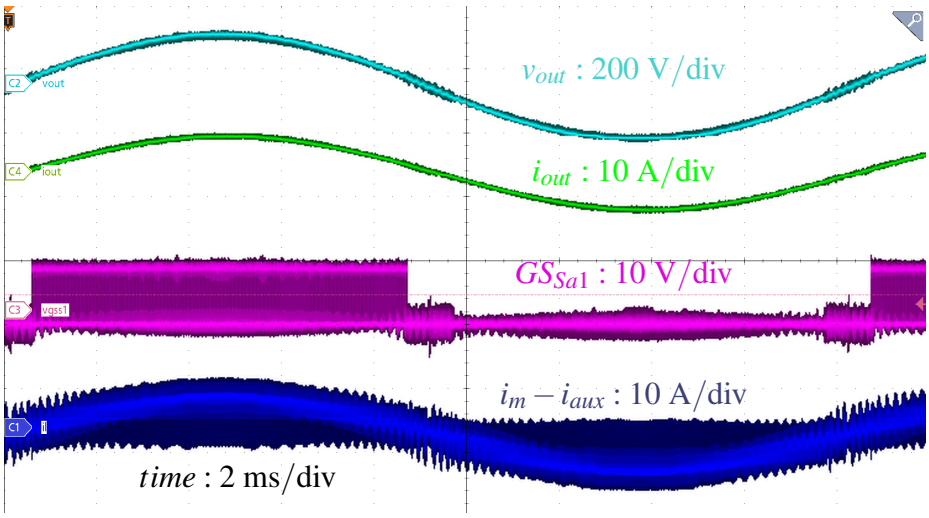


Figure 2.12: Experimental results in a line cycle.

ating at 200kHz is designed and implemented. The input voltage is 400V. The proposed controller is implemented by a Texas Instrument TMS320F28335 DSP. Main switches are GaN Systems GS66506T, and the auxiliary switches are GaN Systems GS66508T. The coupled inductor is designed to have $L_{aux} = 2\mu H$ and $L_M = 200\mu H$. E47/20/16 with 3F3 material is the core for the coupled inductor, and to reduce the ac losses, litz wire is used.

Fig. 2.12 presents the experimental results in a 60Hz cycle. In this waveform, output waveforms, the gate-source signal for S_{a1} and the current passing through the primary side of the inductor are presented. Fig. 2.13 shows the experimental waveforms of the prototype converter in a single switching cycle. It can be seen that the voltage on S_1 reaches zero before it turns-on, and therefore, ZVS is realized for the main switches. Also, in Fig. 2.13, i_m reaches to its former value before turning the transition, which shows that auxiliary switches are turned off at ZCS.

2.6 Summary

A soft-switching inverter based on utilizing an auxiliary circuit is proposed to provide ZVS for the switches of full-bridge inverters in high switching frequencies. It is shown that the

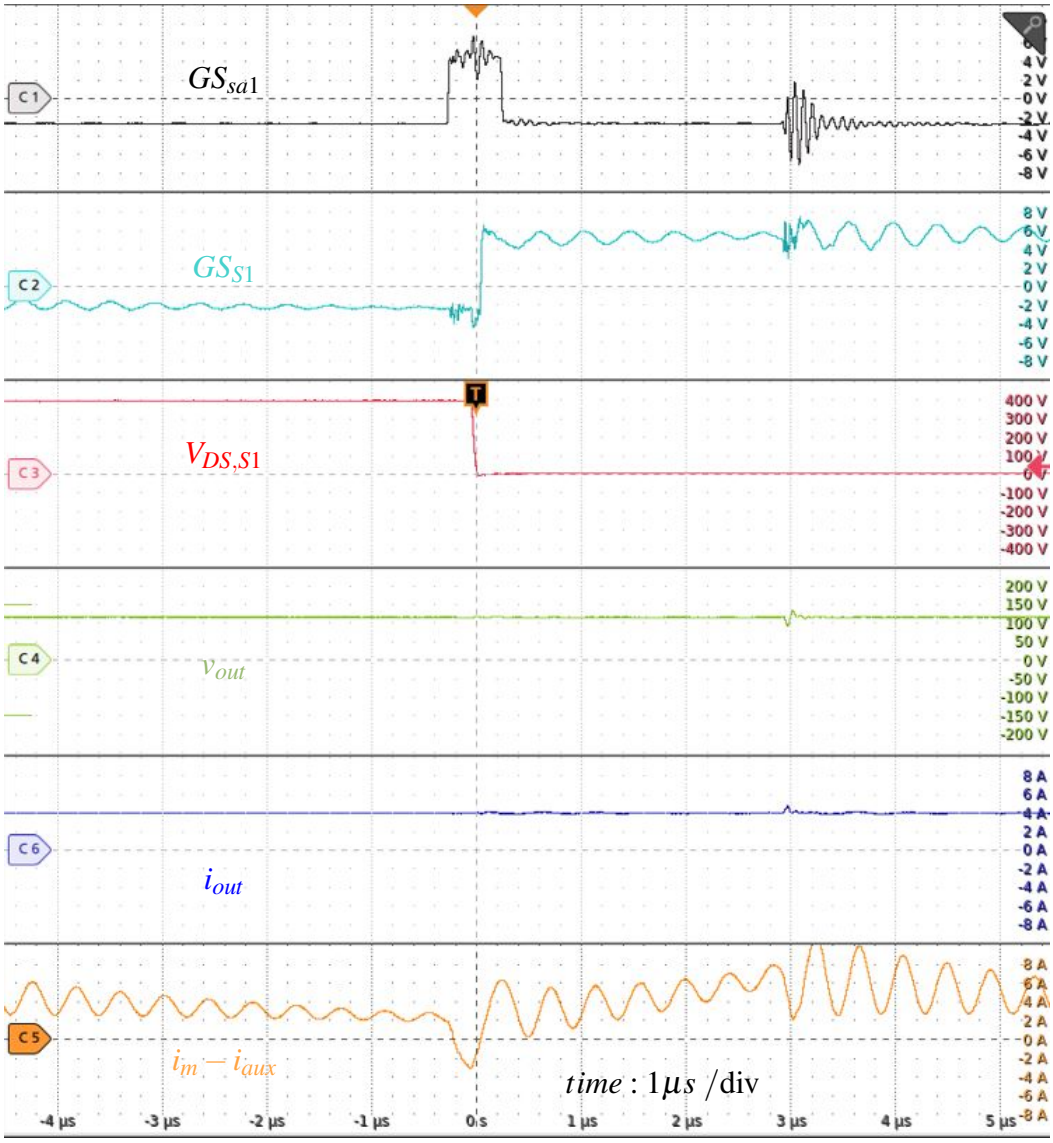


Figure 2.13: Experimental results in a single switching cycle. (V_{out} = 120V, I_{out} = 4.1A)

proposed topology provides soft-switching. The proposed method not only can enhance the converter efficiency, but it is also able to increase the power density comparatively. A full-bridge inverter was designed to verify the claims of this chapter. Although this converter did improve the efficiency and power density, it didn't address the lack of soft-switching in low duty cycles existed in the preceding works.

Chapter 3

Proposed Modulation Technique for A Full-Range Soft-Switching Inverter

3.1 Introduction

As explained in chapter 2, most of the proposed soft-switching techniques for the inverters do not address the need for inverters to operate with high-efficiencies in non-unity power factors. Also, in section 2.3.1, it was explained that for the proposed soft-switching inverter, the unipolar modulation can't provide soft-switching for low duty cycles. Therefore, this modulation technique wasn't suitable for the proposed inverter to operate in non-unity power factors. In this chapter, to address this shortcoming, a combined modulation strategy is proposed that integrates unipolar and bipolar modulation technique. This combined modulation technique overcomes the shortcomings of each modulation techniques in all the operating points of an inverter. Therefore, compared to other soft-switching inverters like [25], The proposed modulation strategy leads to a full-range soft-switching which includes non-unity PFs.

In this chapter, the operation of the auxiliary circuit in all four quadrants of v_o and i_o is explained for both bipolar and unipolar modulation techniques. In section 2.3, the operation principles of the inverter with unipolar modulation was elaborated, and in this chapter, operation principles of the inverter with bipolar modulation is described. Also, the design process for this proposed full-range soft-switching inverter, and how the combined

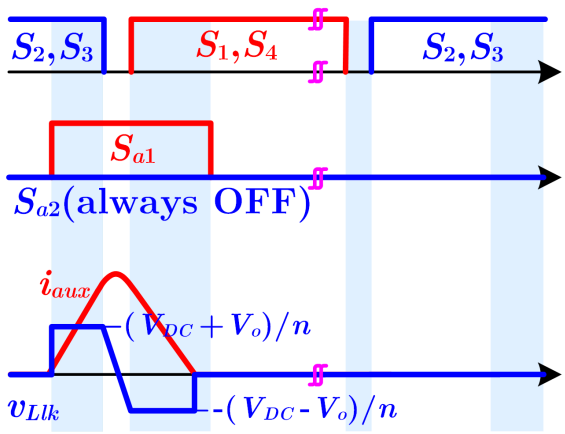


Figure 3.1: Bipolar modulation in low duty cycles.

modulation technique works is discussed. Moreover, a loss analysis has been performed on the proposed inverter to get insights on the performance of the inverter.

3.2 Bipolar Modulation in Low Duty Cycles

As stated in 2.3.1, unipolar modulation can't provide enough time for the auxiliary circuit to change the current direction of the full-bridge switches in low duty cycles. By changing the modulation method to bipolar, soft-switching can be achieved in low duty cycles. This is because bipolar modulation is a two-level modulation, where v_{inv} alternates between V_{dc} and $-V_{dc}$ periodically, and in small duty cycles, this leads to long intervals between switching actions, which can be shown in Fig. 3.1. This increase in time distance allows the utilization of the auxiliary circuit appropriately and turning it off in time without any additional losses. Also, due to insufficient magnetizing force in unipolar mode in low duty cycles, utilization of bipolar PWM reduces the current distortion at zero crossing [30]. Also, combination of these two modulation techniques enables the utilization of the inverter in all power factors. Therefore, before proceeding with bipolar operation principle in the proposed soft-switching inverter, the operation of the auxiliary circuit in these two methods in all four quadrants of v_o vs. i_o should be discussed.

3.3 Circuit Operation in Unipolar Modulation at Four Quadrants of v_o vs. i_o

To achieve full-range soft-switching, auxiliary circuit should provide soft-switching in all four quadrants of output current (i_o) vs. output voltage (v_o). Therefore, each modulation method should enable the auxiliary circuit the ability to provide soft-switching for the full-bridge.

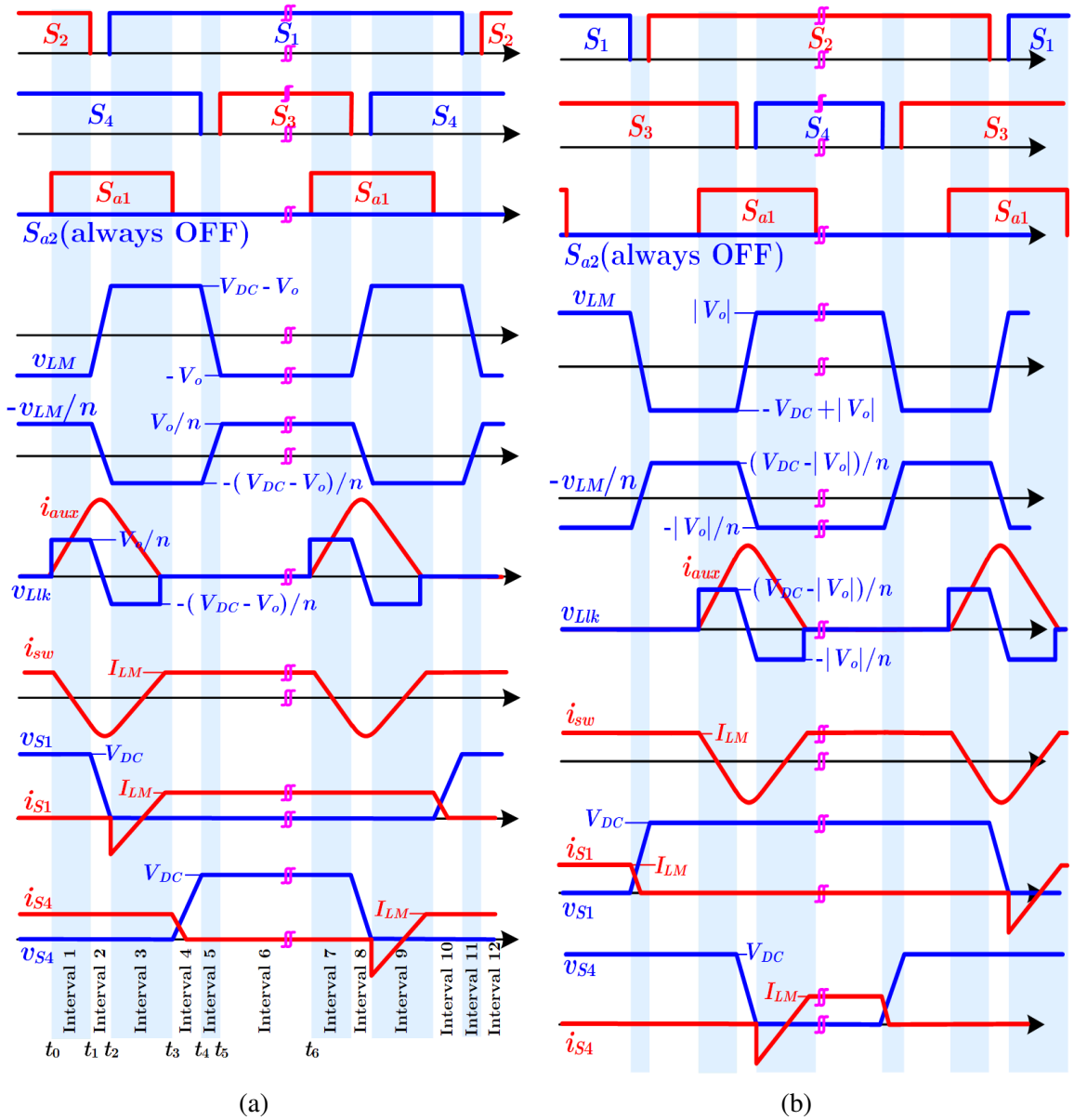
In chapter 2, the circuit operation in unipolar at the first quadrant is discussed, comprehensively. Here, the general operation of the circuit in unipolar modulation at four different quadrants is discussed. Figs. 3.2 and 3.3 show the theoretical waveforms of the circuit in unipolar modulation at four quadrants.

Unipolar Mode, First Quadrant ($v_o > 0, i_o > 0$) [see Fig. 3.2 (a)]: As discussed in chapter 2, in this quadrant, ZVS for switches S_2 and S_3 is naturally provided by i_{LM}, and the auxiliary circuit provides ZVS of switches S_1 and S_4. In this condition, the auxiliary switch S_{a1} is controlled, and S_{a2} is always OFF. Besides, the positive and negative voltage levels applied to the leakage inductor are v_o/n and $-(V_{DC}-v_o)/n$, respectively.

Unipolar Mode, Second Quadrant ($v_o < 0, i_o > 0$) [see Fig. 3.2 (b)]: The condition of this quadrant is similar to the first quadrant discussed above except for the voltage levels applied to the leakage inductor. In this quadrant, the positive and negative voltage levels applied to the leakage inductor are $(V_{DC}-|v_o|)/n$ and $-|v_o|/n$, respectively.

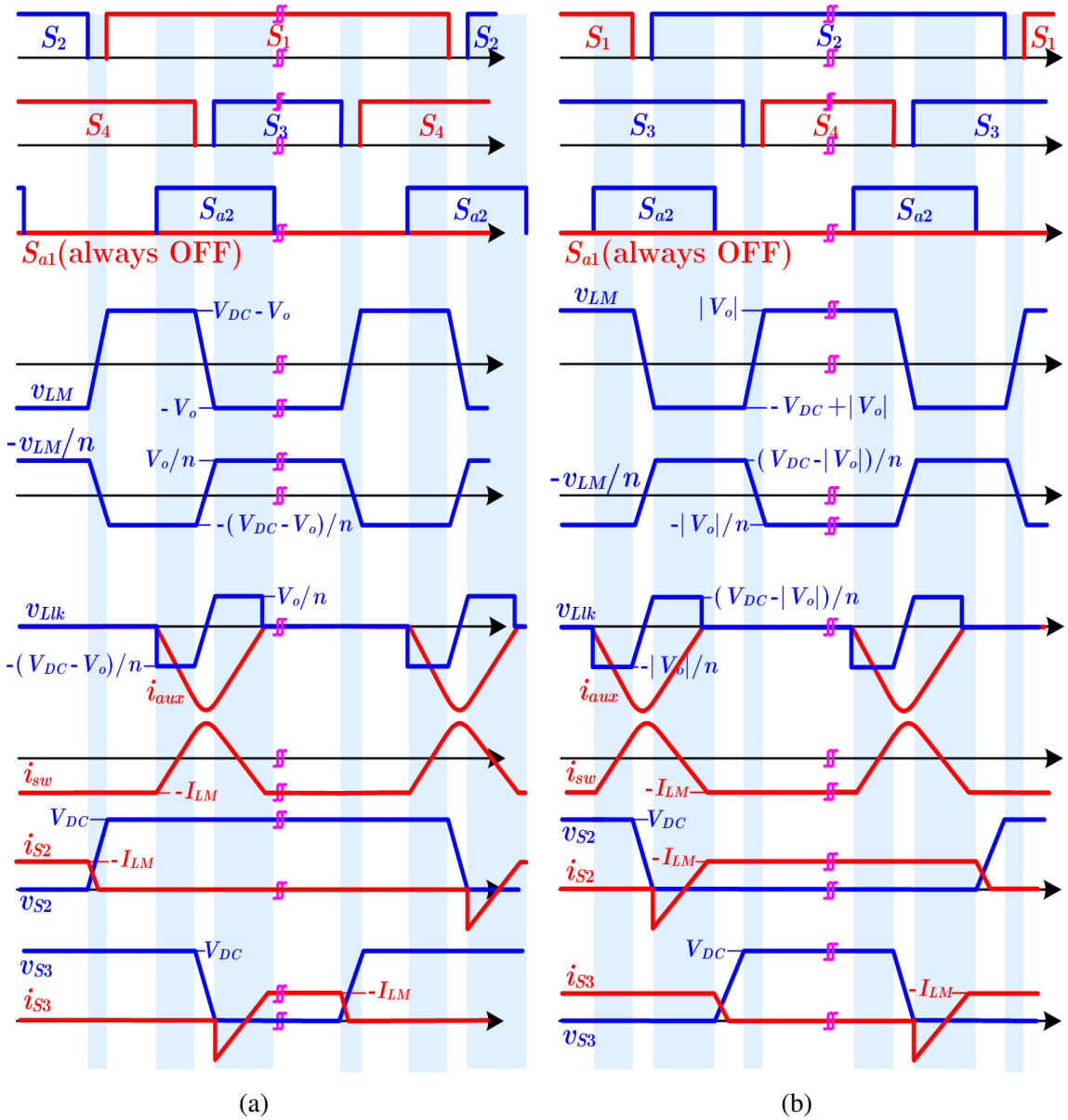
Unipolar Mode, Third Quadrant ($v_o < 0, i_o < 0$) [see Fig. 3.3 (a)]: In the third and fourth quadrants the current polarity of io is negative. Here, auxiliary switch Sa2 is controlled and Sa1 is always OFF, and the current direction in the auxiliary circuit is opposite to the first and second quadrants. In the third quadrant, ZVS for switches S_1 and S_4 is naturally provided by i_{LM}, and the auxiliary circuit provides ZVS of switches S_2 and S_3. Besides, the positive and negative voltage levels applied to the leakage inductor are $(V_{DC}-|v_o|)/n$ and $-|v_o|/n$, respectively.

Unipolar Mode, Forth Quadrant ($v_o > 0, i_o < 0$) [see Fig. 3.3 (b)]: The condition of



(a) (b)

Figure 3.2: Theoretical waveforms in unipolar modulation at (a) first quadrant ($v_o > 0, i_o > 0$). (b) second quadrant ($v_o < 0, i_o > 0$).



(a) (b)

Figure 3.3: Theoretical waveforms in unipolar modulation at (a) third quadrant ($v_o < 0, i_o < 0$). (b) fourth quadrant ($v_o > 0, i_o < 0$).

this quadrant is similar to the third quadrant discussed above except for the voltage levels applied to the leakage inductor. In this quadrant, the positive and negative voltage levels applied to the leakage inductor are v_o/n and $-(V_{DC}-v_o)/n$, respectively.

3.4 Soft-switching Inverter Operation Principles with Bipolar Modulation

Fig. 3.4 (a) illustrates the related theoretical waveforms for the first and second quadrants. Before the first interval, it is assumed that no current exists in the auxiliary circuit, S_2 and S_3 are ON and conduct i_{LM}. Besides, all other switches are OFF.

Interval 1 $[t_0 - t_1]$: At t_0, the auxiliary switch S_{a1} turns ON under ZCS due to L_{LK}. In this interval, the voltage across L_M is $-V_{DC}-V_o$ ($v_{LM}=-V_{DC}-V_o$). Hence, by turning S_{a1} ON, the voltage of $(V_{DC}+V_o)/n$ would be placed across L_{lk} ($v_{Llk}=(V_{DC}+V_o)/n$). Consequently, the current of auxiliary circuit i_{aux} is increased linearly as follows:

$$i_{Llk}(t)=\frac{V_{DC}+V_o}{nL_{lk}}(t-t_0). \tag{3.1}$$

Since i_{aux} enters the dotted terminal of the secondary side of the ideal transformer, the current of i_{aux}/n would exit the dotted terminal of the primary side as seen in Fig. 3.5, where the equivalent circuit in interval 1 is illustrated. Hence, the current of switches S_2 and S_3 (i_{sw}) reduces as follows:

$$i_{sw}(t)=I_{LM}-\frac{V_{DC}+V_o}{n^2L_{lk}}(t-t_0). \tag{3.2}$$

According to (3.2), i_{sw} reduces linearly to zero and then increases in the negative direction.

Interval 2 $[t_1 - t_2]$: At t_1, S_2 and S_3 turn OFF, and the negative current of i_{sw} charges C_{S2} and C_{S3} and discharges C_{S1} and C_{S4} through a resonance between L_{lk} and $C_{S1}\sim C_{S4}$. The equations of i_{aux} and v_{S1} are obtained from:

$$i_{aux}(t)=I_m+\alpha_{bi}sin(\omega_{r,bi}(t-t_2)+\beta_{bi}) \tag{3.3}$$

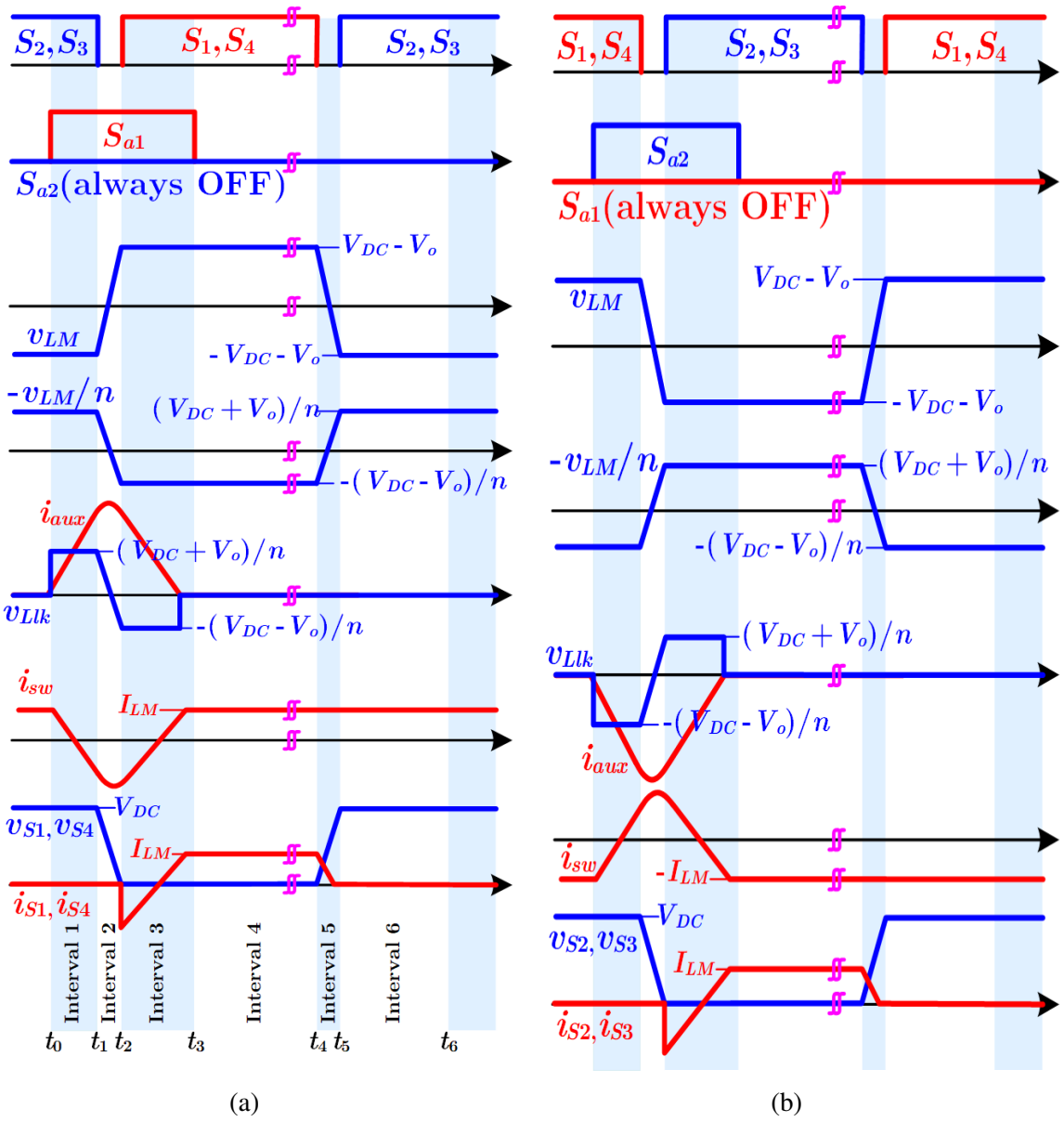


Figure 3.4: Theoretical waveforms in bipolar modulation at (a) first and second quadrants ($v_o > 0, i_o > 0$ and $v_o < 0, i_o > 0$). (b) third and forth quadrants ($v_o < 0, i_o < 0$ and $v_o > 0, i_o < 0$).

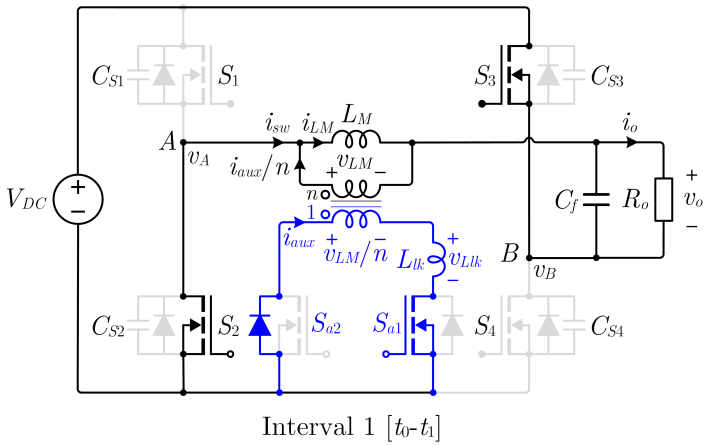


Figure 3.5: Inverter equivalent circuit in interval 1 with bipolar modulation.

$$v_{S1}(t) = \frac{V_{dc} - V_o}{2} + Z_{r,bi}\alpha_{r,bi}cos(\omega_{r,bi}(t - t_2) + \beta_{bi}) \tag{3.4}$$

where we have:

$$\alpha_{bi} = \sqrt{(\frac{V_{dc} + V_o}{2Z_{r,bi}})^2 + (i_{aux}(t_2) - I_m)^2} \tag{3.5}$$

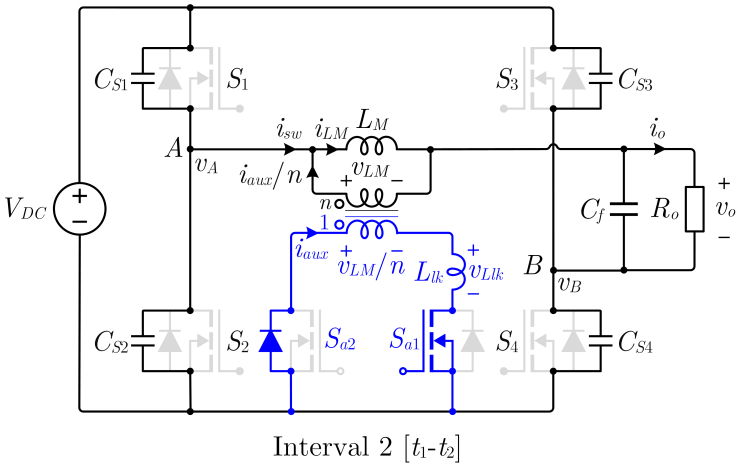
$$\beta_{bi} = \tan^{-1}(\frac{Z_{r,bi}(i_{aux}(t_2) - I_m)}{(\frac{V_{dc}+V_o}{2})}) \tag{3.6}$$

$$Z_{r,bi} = n\sqrt{\frac{\frac{L_{lk}}{2}}{C_{S1} + C_{S2}}} \tag{3.7}$$

$$\omega_{r,bi} = \frac{1}{n\sqrt{\frac{L_{lk}}{2}(C_{S1} + C_{S2})}} \tag{3.8}$$

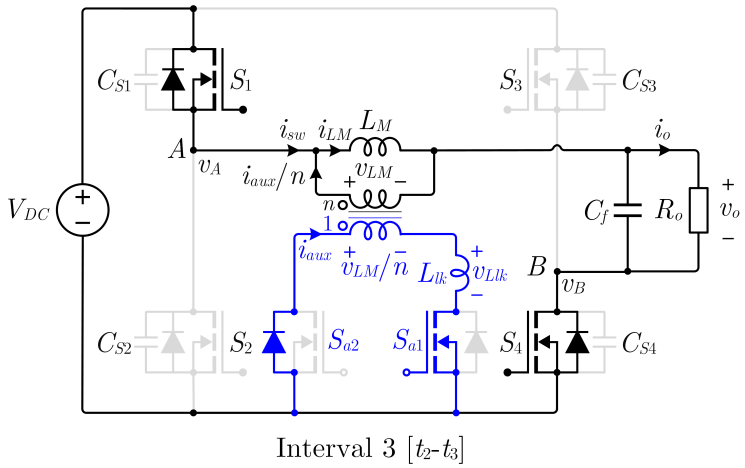
At the end of this interval, C_{S1} and C_{S4} are completely discharged, and their body diodes turn ON to provide ZVS turn-ON for S_1 and S_4. According to (3.4), to guarantee that the S_1 (or similarly S_4) voltage reaches zero, the amplitude of the sinusoidal term $Z_{r,bi}\alpha_{r,bi}$ is designed more than the DC term $(V_{dc} - V_o)/2$. This issue is discussed in the design considerations Section. The equivalent circuit of this interval is shown in Fig. 3.6.

Interval 3 [t_2 – t_3]: At t_2, by conducting the S_1 and S_4 body diodes, S_1 and S_4 turn ON under ZVS. In this interval, the voltage across L_M is $V_{DC} - V_o$ ($v_{LM} = V_{DC} - V_o$), and so, the voltage of $-(V_{DC} - V_o)/n$ would be placed across L_{lk} ($v_{Llk} = -(V_{DC} - V_o)/n$). Consequently, the current of auxiliary circuit i_{aux} is reduced linearly, and meanwhile, the current of i_{sw} increases linearly. Before the end of this interval, i_{aux} reaches zero, and S_{a2} body diode turns OFF. Therefore, at the end of this interval, S_{a1} turns OFF under ZCS. The equivalent circuit of this interval is shown in Fig. 3.7.



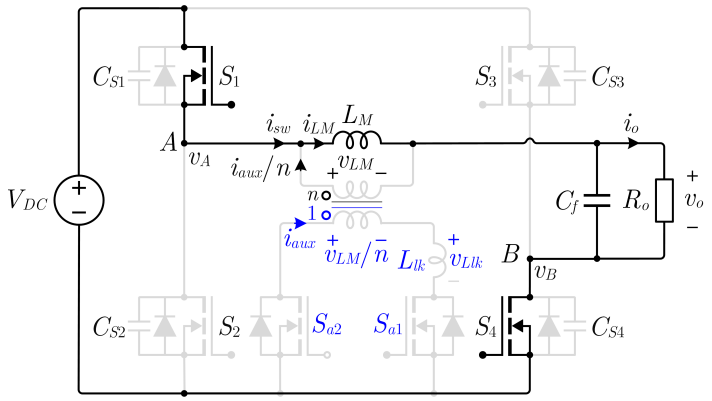
Interval 2 [t_1-t_2]

Figure 3.6: Inverter equivalent circuit in interval 2 with bipolar modulation.



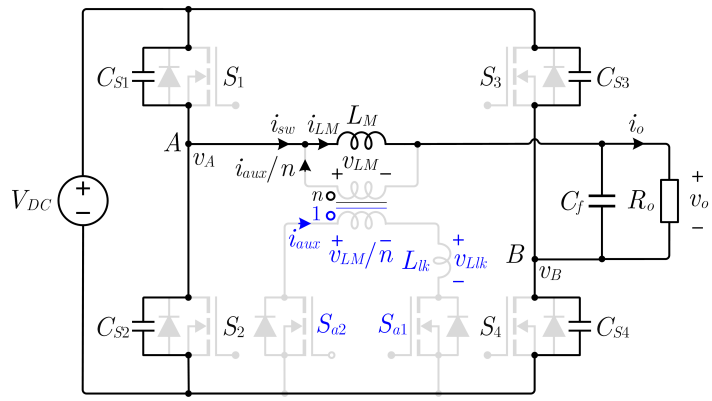
Interval 3 [t_2-t_3]

Figure 3.7: Inverter equivalent circuit in interval 3 with bipolar modulation.



Interval 4 [t_3-t_4]

Figure 3.8: Inverter equivalent circuit in interval 4 with bipolar modulation.



Interval 5 [t_4-t_5]

Figure 3.9: Inverter equivalent circuit in interval 5 with bipolar modulation.

Interval 4 [$t_3 - t_4$]: In this interval, S_1 and S_4 are ON. The voltage of $V_{DC} - V_o$ is placed across L_M ($v_{LM} = V_{DC} - V_o$), and L_M is magnetized. The equivalent circuit of this interval is presented in Fig. 3.8.

Interval 5 [$t_4 - t_5$]: At t_4, S_1 and S_4 turn OFF. Therefore, i_{LM} discharges C_{S2} and C_{S3}, and charges C_{S1} and C_{S4}. At the end of this interval, C_{S2} and C_{S3} discharge completely, and body diodes of S_2 and S_3 turn ON. The equivalent circuit of this interval is illustrated in Fig. 3.9.

Interval 6 [$t_5 - t_6$]: At t_5, by conducting the body diodes of S_2 and S_3, S_2 and S_3 turn

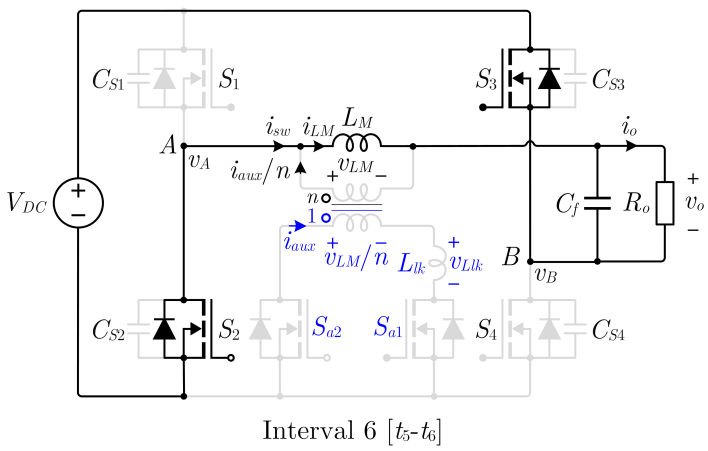


Figure 3.10: Inverter equivalent circuit in interval 6 with bipolar modulation.

ON under ZVS. In this interval, the voltage of $-V_{DC}-V_o$ is placed across L_M ($v_{LM}=-V_{DC}-V_o$), and L_M is demagnetized. The equivalent circuit of this interval is shown in Fig. 3.10.

3.5 Circuit Operation in Bipolar Modulation at Four Quadrants of v_o vs. i_o

In Subsection A, the circuit operation in unipolar at the first and second quadrants is discussed, comprehensively. Here, the general operation of the circuit in bipolar mode at four different quadrants is discussed. Fig. 3.4 shows the theoretical waveforms of the circuit in bipolar modulation at four quadrants.

Bipolar Modulation, First and Second Quadrants ($v_o>0, i_o>0$ and $v_o<0, i_o>0$) [see Fig. 3.4 (a)]: As discussed in Subsection A, in these quadrants, ZVS for switches S_2 and S_3 is naturally provided by i_{LM}, and the auxiliary circuit provides ZVS of switches S_1 and S_4. In this condition, the auxiliary switch S_{a1} is controlled, and S_{a2} is always OFF. Besides, the positive and negative voltage levels applied to the leakage inductor are $(V_{DC}+v_o)/n$ and $-(V_{DC}-v_o)/n$, respectively.

Bipolar Modulation, Third and Forth Quadrants ($v_o<0, i_o<0$ and $v_o>0, i_o<0$) [see

Fig. 3.4 (b)]: In the third and fourth quadrants the current polarity of i_o is negative. Here, auxiliary switch S_{a2} is controlled and S_{a1} is always OFF, and the current direction in the auxiliary circuit is opposite to the first and second quadrants. In the these quadrants, ZVS for switches S_1 and S_4 is naturally provided by i_{LM}, and the auxiliary circuit provides ZVS of switches S_2 and S_3. Besides, the positive and negative voltage levels applied to the leakage inductor are $(V_{DC}+v_o)/n$ and $-(V_{DC}-v_o)/n$, respectively.

3.6 Combined Modulation Technique

In the proposed inverter, a combination of unipolar and bipolar method is used as the modulation strategy of the inverter with a strategy shown in Fig. 3.11. To keep the auxiliary circuit frequency constant, effective switching frequency of bipolar and unipolar techniques are the same. This combined modulation overcomes the shortcomings of each modulation to have a high-performance soft-switching inverter in all the power factors. For unipolar method, the shortcomings are:

- Inability to provide enough time for the auxiliary circuit to provide soft-switching for the full-bridge switches.
- Current distortion near zero duty cycle due to short duty cycles for the switches.

Also for the bipolar mode:

- For a constant effective switching frequency, full-bridge switches operate with double the switching frequency of the switches in unipolar mode. This results in higher switching losses.
- The change between V_{DC} and $-V_{DC}$ on the inverter terminals creates more change on the voltage of the filter inductor.

Therefore, to avoid soft-switching inability of the unipolar mode in low duty cycles, bipolar mode is used, and when the unipolar mode becomes able to provide soft-switching

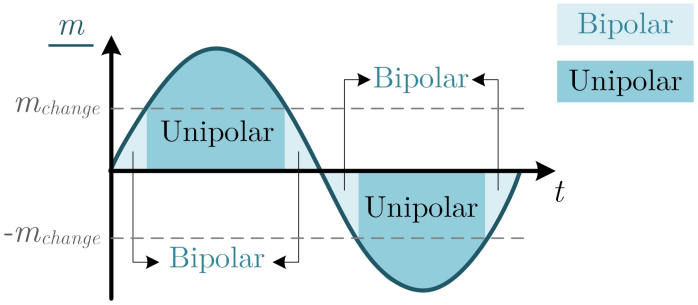


Figure 3.11: Proposed modulation.

through the auxiliary circuit, unipolar mode is used to avoid the higher switching losses of the bipolar modulation strategy.

3.7 Design

To achieve the best performance, converter parameters should be designed optimally. For the proposed converter, there are a few parameters that should be considered in the design process.

3.7.1 Switch Selection

The main parameters that should be considered in selecting a switch in the proposed soft-switching converter, are the parameters of dynamic characteristics (C_{oss}, delays,...) and also gate-charge characteristics (Q_g, Q_{gs},..) of the switch. C_{oss} is significantly important since a small parasitic capacitance, decreases the required leakage inductance for charging and discharging the capacitance as seen in (2.7) and (3.7). Therefore, choosing a switch with small C_{oss} allows the decrease of the leakage inductance to still have a resonance stage impedance (Z_r) that can guarantee the discharge of the charge in the switches. Moreover, a small leakage inductance requires less charging time for the leakage inductance which enables the utilization of the auxiliary circuit in higher frequencies to provide soft-switching to the inverter.

Gate charge characteristics of the switch affect the cross-over loss that can happen in

the switches as (3.19) and (3.21). Switches with lower gate charges, are more suitable to be used in higher switching frequency inverters since their hard-switching losses are less. Utilization of the auxiliary circuit further increases the possible switching frequency of an inverter since a decrease in the switching loss can increase the limit of switching frequency considering the thermal condition of the switches.

It should be noted that, the value of C_{oss} varies with the drain-source voltage V_{ds}. To make sure that the design is accurate, effective values of C_{oss} are used from the data sheet.

3.7.2 Magnetic Design

Design of the coupled inductor in the proposed topology needs various considerations. This is because the coupled inductor design determines the values of L_M, L_{aux} and turns ratio, which affect the main function of the inverter and also the auxiliary circuit operation. The output LC filter is comprised of L_M, alongside with C_f. Values of L_M and C_f are chosen in a way to reduce the harmonic contents in the output load [31]. L_{aux} is the leakage inductance of the coupled inductor that resonates with the switch output capacitances to create a zero-voltage transition. (2.8) shows that the value of L_{aux} affects the amplitude and the frequency of the resonance stage along with C_1 and C_2, which are output capacitances of the switches. To guarantee that in all the operating points, the voltage of the switches output capacitors reaches zero through a resonance cycle, in (2.4) and (3.4), $v_{s1}(t)$ should always reach zero.

$$v_{S1}(t) \leqslant 0 => Z_{r,uni}\alpha_{uni} \geqslant V_{dc} - V_o, \tag{3.9}$$

$$v_{S1}(t) \leqslant 0 => Z_{r,bi}\alpha_{bi} \geqslant \frac{V_{dc} - V_0}{2}. \tag{3.10}$$

Moreover, charging rate of the leakage inductance ($\frac{di}{dt}$) is determined by the value of the designed leakage inductance. Therefore, the leakage inductance value affects the AC conduction loss which is related to the current slope [32]. On the other hand, a higher L_{aux} increases the time that is needed for charging the leakage inductance to the desired value.

Therefore, higher RMS value of the auxiliary current is expected, which adversely affects the DC conduction losses.

To select the turns ratio of the coupled inductor, it should be considered that there is a voltage overshoot on S_{a1} and S_{a1}. Choosing a proper value for the turns ratio decreases the voltage stress on the auxiliary switches and enables the utilization of switches with low output capacitances. The low output capacitance can also reduce the stored energy in the switch parasitic capacitances in the auxiliary circuit.

After determining values for L_{lk}, L_M and turns ratio, a coupled inductor is designed based on the design methodology proposed in the next chapter.

3.7.3 Negative Peak of the Main Switch Current ($I_{sw,neg}$)

The negative peak of the main switch current, $I_{sw,neg}$, is equal to $i_{aux}(t_2) - I_m$, and it affects the capacitance discharge rate in the resonance stage along with Z_r. Same as L_{aux}, value of $I_{sw,neg}$ needs to be selected considering the resonance stage and total losses. By replacing $i_{aux}(t_2) - I_m$ with $I_{sw,neg}$ in (2.5) and (2.6) following equations can be derived.

$$\alpha_{uni} = \sqrt{\left(\frac{V_o}{Z_{r,uni}}\right)^2 + I_{sw,neg}^2}, \tag{3.11}$$

$$\beta_{uni} = tan^{-1}\left(\frac{Z_{r,uni} I_{sw,neg}}{V_o}\right), \tag{3.12}$$

$$\alpha_{bi} = \sqrt{(\frac{V_{dc} + V_o}{2Z_{r,bi}})^2 + I_{sw,neg}^2}, \tag{3.13}$$

$$\beta_{bi} = \tan^{-1}(\frac{Z_{r,bi} I_{sw,neg}}{(\frac{V_{dc}+V_o}{2})}). \tag{3.14}$$

As it can be seen, α and β depend on both Z_r and $I_{sw,neg}$. Therefore, values of $I_{sw,neg}$ and L_{aux} can have a spectrum of values that can satisfy the ZVS condition. To choose a value for these two parameters, minimizing the added losses by the auxiliary circuit losses should be considered.

3.7.4 Charge Time of the Leakage Inductance (t_{ch})

When either S_{a1} and S_{a2} turn on, i_{aux} will increase linearly. To guarantee the ZVS condition, this current should reach $I_{sw,neg} + I_m$. The time interval needed by the auxiliary circuit to increase its current up to $I_{sw,neg} + I_m$ should be calculated by the MCU in all operating points based on the data given by the sensors. The needed time is obtained from (2.2) and (3.2). For example, when the inverter operates in the first quadrant of the unipolar modulation, t_{ch} is found by the following equation.

$$t_2 - t_1 = t_{ch}, \tag{3.15}$$

$$i_{aux,ch} = I_m + i_{sw,neg}, \tag{3.16}$$

$$t_{ch} = \frac{L_{aux} i_{aux,ch}}{V_o}, \tag{3.17}$$

where values of $i_{sw,neg}$ and L_{aux} are predefined in the design, and V_o and I_m should be collected from the sensors in the circuit. Since the current ripple of I_m is small, approximately the output current is sensed. Therefore, there are only two sensors used in the circuit on the output.

3.7.5 Active Time of the Auxiliary Circuit (t_{aux})

The time duration that either of the auxiliary switches are ON. The minimum value for t_{aux} is determined by calculating the time required for the auxiliary current to reach its peak and go back to zero after the resonance stage.

$$t_{aux} \geq (t_{ch} + t_{dt} + t_{discharge})_{max} \tag{3.18}$$

Where t_{dt} and $t_{discharge}$ are deadtime and the time required for i_{aux} to reach zero. Therefore, a constant t_{aux} can be selected by calculating the required time by the auxiliary circuit to provide ZVT for the main switches and also to be turned off under ZCS condition.

3.7.6 Modulation Changing Point (m_{ch})

To select the point where the modulation technique is changed from unipolar to bipolar is where the auxiliary switches can't create a ZVT without interfering with the full-bridge in the unipolar modulation technique.

These equations are used to find the possible set of parameters to guarantee soft-switching in all the possible operating points that doesn't need a variable deadtime. For different feasible values of L_{aux} and $I_{sw,neg}$, an analysis has been done, and different set of values for L_{aux} and $I_{sw,neg}$ has been found that guarantee the soft-switching in every power factor. Out of these possible set of values, the set of values for L_{aux} and $I_{sw,neg}$ has been selected that minimizes the total losses of the auxiliary circuit.

3.8 Loss Analysis

In this section, the converter losses are analysed and its losses are compared to a hard-switching inverter.

3.8.1 Turn-on Cross-over Losses

Turn-on loss of the inverter switches causes the most challenges when increasing the switching frequency.

As this loss happens in the cross-over time between the switch voltage and current, it can be eliminated if ZVS is provided for the switches. For the hard switching case, this loss can be calculated as follows:

$$P_{co,on} = \frac{1}{2} I_{sw(on)} V_{dc} f_{sw} \frac{Q_{GS2} + Q_{GD}}{I_{D\text{river}(turn-on)}}, \tag{3.19}$$

where $I_{sw(on)}$ is the current passing through the switch after it turns on, Q_{GS2} is part of the gate-source charge that is needed to increase the switch current from zero to its final value

($I_{sw(on)}$), and Q_{GD} is gate-drain charge. Also,

$$I_{\text{Driver }(turn-on)} = \frac{V_{Dr} - \left(V_{th} + I_{sw(on)}/g\right)}{R_{g,on}}, \tag{3.20}$$

where V_{Dr} is the driving voltage of the gate-driver, V_{th} is the gate threshold voltage, g is the forward transconductance, and $R_{g,on}$ is the gate-driver resistance for turning the switch on. From these equations it can be understood that the cross-over losses not only depend on the switch characteristics, but also to the gate driver circuit too, which will depend on the overall design of the system. Therefore, for justifying the use of an auxiliary circuit, a loss analysis should be done based on the parameters of each system design.

Using switches with low parasitic capacitances and gate charge (Q_g) can enable the increasing of the switching frequency of the system. However, for each design, hard-switching losses will create a limit after a certain frequency. For example, although GaN switches are known for their superior transient performance, based on [33] in a 1kW, 1MHz GaN full-bridge inverter with DC voltage of 400V, total turn-on cross-over loss can be around 60W, which is 6% of the total power. Therefore, depending on the system design and switching characteristics, utilization of a soft-switching method can be crucial to allow an increase of the switching frequency.

3.8.2 Turn-off Cross-over Losses

Turn-off cross over loss happens in the switching transients while the switch turns off. The equation for turn-off cross-over loss is,

$$P_{co,off} = \frac{1}{2} I_{sw(off)} V_{DD} f_{Sw} \frac{Q_{GS2} + Q_{GD}}{I_{\text{Driver}(turn-off)}}, \tag{3.21}$$

where,

$$I_{\text{Driver }(turn-off)} = \frac{\left(V_{th} + I_{sw(off)}/g\right)}{R_{g,off}}. \tag{3.22}$$

Turn-off cross-over is usually less than the turn-on. This is mostly because of the $R_{g,off}$ being less than $R_{g,on}$.

3.8.3 C_{oss} Losses

In the hard-switching cases, the charge in the output capacitance of the switches (C_{oss}), is discharged in the switch channel while turning on which results in C_{oss} losses. On the other hand, . C_{oss} losses in a hard-switched full-bridge can be calculated by the following equation.

$$P_{Coss} = f_{sw} \int_0^{V_{ds}} C_{oss}(V) V dV. \tag{3.23}$$

Since C_{oss} is non-linear, and it is dependent of the drain-source voltage, to calculate the loss, C_{oss} vs. V_{ds} plot is needed. However, to simplify the calculation, usually datasheets provide the E_{oss} vs V_{ds} plot, which can be used to find the total C_{oss} losses in each voltage level.

$$P_{Coss}(V_{ds}) = f_{sw} E_{oss}(V_{ds}), \tag{3.24}$$

where $E_{oss}(V_{ds})$ is found from the E_{oss} vs V_{ds} plot, which shows the energy that is required to charge the C_{oss} to V_{ds} voltage. However, when ZVS is provided for the full-bridge switches, There is no C_{oss} loss while turning the switches ON, because the charge in the switches transfers to the switch that turns off through a resonance stage.

3.8.4 Conduction Losses

The losses that are dissipated in the components while conducting current are accounted as conduction losses. Therefore, conducting a current through inverter components such as switches and magnetic components leads to these losses. In the proposed converter, these losses arise mainly from the drain-to-source on-resistances of the switches, forward voltage drop of the body diodes and DC and AC resistances of the coupled inductor.

Conduction losses in the switches and diodes can be calculated by analyzing the current passing through them and also by having the component datasheet. If the output current is positive, considering that current ripple doesn't change the current direction ($\frac{di}{2} <= |I_o|$), the conduction loss in the full-bridge switches in a single switching cycle of the full-bridge switches regardless off the modulation technique that is active in the inverter can be written

as,

$$P_{cond} = ((1+m)R_{ds} + (1-m)R_d)\left(I_o^2 + \frac{\Delta i^2}{12}\right) + V_f(1-m)I_o, \tag{3.25}$$

where R_{ds} is the drain-source resistance of the full-bridge switches, and V_f and R_d are the coefficients of the V_{ds} vs I_{sd} of the switch body diodes. Considering the output current is negative, and also that current ripple doesn't change the current direction ($\frac{di}{2} <= |I_o|$),

$$P_{cond} = ((1-m)R_{ds} + (1+m)R_d)\left(I_0^2 + \frac{\Delta i^2}{12}\right) + V_f(1+m)I_0. \tag{3.26}$$

If the ripple causes direction change in the switch currents, the switch conduction loss calculation should be calculated by different equations. However, to reduce the complexity of calculations, in this paper conduction loss calculations are done using (3.25) and (3.26). To calculate the conduction loss in a line cycle, these equations should be calculated for all the switching cycles.

Also, to calculate the current in the auxiliary circuit, resonance stage has been eliminated to avoid the complexity. The equation for auxiliary circuit conduction losses can be written as,

$$P_{cond,sw,aux} = \frac{(t_{ch}+t_{fall})}{T_s}\frac{R_{ds,aux}}{3}(\frac{n_1}{n_2}I_{aux,peak})^2, \tag{3.27}$$

$$P_{cond,d,aux} = \frac{(t_{ch}+t_{fall})}{T_s}(\frac{R_{d,aux}}{3}(\frac{n_1}{n_2}I_{aux,peak})^2 + V_{f,aux}\frac{I_{aux,peak}}{2}). \tag{3.28}$$

Accurate calculation of the total conduction loss in the coupled inductor adds complexity to the analysis, and is not as straight-forward as switch conduction loss. This complexity arises from the high-frequency effects in the winding of the component. These high-frequency losses are losses due to the skin effect and proximity effect in the windings. To calculate these losses for a non-sinusoidal waveform, there are various methods proposed in the literature, which either require finite element analysis [32] or accurate measurements in the system, which requires cumbersome calculations [34]. In this paper, the coupled inductor is modeled accurately in the Ansys software to find the total conduction

losses through a transient simulation and a network analyzer was used to validate the high-frequency losses reported in the simulation results.

3.8.5 Gate-driver Losses

To drive the switches, there should be an energy supplied to charge the switch gate. This energy that charges and discharges the input capacitance of the switch gates during a single switching cycle, is called the gate-driver loss. Gate-driver loss is constant in each switching cycle of the line cycle, and it can be calculated by the following equation for each switch.

$$P_{gate} = V_{dr} Q_G f_{sw}, \tag{3.29}$$

where V_{dr} is the voltage used to drive the gate, Q_G is the total gate charge that is dependent on the switch, and f_{sw} is the switching frequency. For the full-bridge converter, gate-driver losses in the unipolar modulation are calculated as,

$$P_{gate,uni} = 2V_{dr,main} Q_{G,main} f_{sw,uni}. \tag{3.30}$$

Also for the bipolar modulation,

$$P_{gate,bi} = 2V_{dr,main} Q_{G,main} f_{sw,bi}. \tag{3.31}$$

Auxiliary circuit has two switches that in each switching cycle, there is one switch that turns on. Therefore, gate-driver loss of the auxiliary circuit is,

$$P_{gate,aux} = V_{dr,aux} Q_{G,aux} f_{sw}. \tag{3.32}$$

3.8.6 Core Losses

Core losses in the inverter should be calculated for a complete line cycle. To calculate these losses, iGSE method[28] is used in each switching cycle. In this method, core losses can be calculated in a non-sinusoidal waveform. Therefore, in the hard-switching case where there is a triangular waveform, which is a piece-wise linear waveform with no minor loops,

core loss is calculated by the following equation.

$$\overline{P_v} = \frac{k_i(\Delta B)^{\beta-\alpha}}{T} \sum_m \left| \frac{B_{m+1} - B_m}{t_{m+1} - t_m} \right|^{\alpha} (t_{m+1} - t_m), \tag{3.33}$$

$$k_i \cong \frac{k}{2^{\beta+1}\pi^{\alpha-1}\left(0.2761 + \frac{1.7061}{\alpha+1.354}\right)}. \tag{3.34}$$

k, α and β are Steinmetz parameters that are specific to the material that is being used, and B is calculated with the Ampere's law. This equation is calculated in each switching cycle, and then it is calculated over a line cycle. To calculate the core losses in the soft-switching inverter finite-element analysis has been performed by using Ansys Maxwell software. More details on the utilization of the iGSE method on core losses of the inverter inductor in a line cycle of operation is provided in the next chapter.

The losses in both hard-switching and soft-switching inverters in different power factors are calculated using the above equations and also magnetic simulations using Ansys Maxwell software. Comparing the results of these calculation in both hard-switching and soft-switching inverters in different power factors justifies the addition of an auxiliary circuit to provide soft-switching for the full-bridge.

Therefore, the soft-switching inverter can increase the switching frequency limit of the converter, which results in a decrease in the size of passive components of the system, especially magnetic components. Moreover, in a constant frequency hard-switching inverter requires thermal considerations to dissipate the heat from the switches like using heat sinks, which can decrease the power density of the inverter far more than addition of two auxiliary switches and their gate driver components.

3.9 Summary

In this chapter, a full-range soft-switching full-bridge inverter was proposed based on an auxiliary circuit comprising of two switches a coupled inductor. ZVS and ZCS were achieved for the full-bridge switches and the auxiliary circuit, respectively. A combined modulation of unipolar and bipolar modulation techniques was proposed to guarantee the

soft-switching operation in all the operating points, which makes the proposed inverter a full-range soft-switching full-bridge inverter. A variable timing strategy was implemented to modulate the auxiliary switches, which requires only two sensors in the output of the inverter to measure the output current and voltage. This made the auxiliary circuit operation more efficient. The proposed method can increase the efficiency of inverters with different semiconductor technologies such as Mosfet, Gallium Nitride (GaN) and silicon carbide (SiC).

Chapter 4

Accurate Inductor Loss Analysis and Design in Inverters and Experimental Results

4.1 Introduction

To design an efficient power electronics converter, magnetic components are of great importance since they contribute considerably to the total losses of the system. To design an efficient inductor or transformer, losses of the inductor should be accurately calculated. Based on this loss analysis, parameters of a magnetic component is designed to achieve the minimum loss. In DC/DC converters, for example a buck converter, inductor design process is conducted considering the operation of the inductor in the worst-case switching cycle, where the inductor loss is at its maximum. However, in the DC/AC inverters, losses should be considered in a line cycle of operation rather than a switching cycle. The difference is that the amplitude of the current ripple changes over one line cycle which in turn changes the core and conduction losses. Considering only the worst case scenario would result in an over-design or too large of a margin for the temperature rise.

As stated in chapter 1, total inductor losses are divided between core losses and conduction losses. In this chapter, a generalized equation based on [28] and [4] is derived for the core losses of the inverter inductor in a line cycle of operation regardless of the modulation technique. The other major contributor to the inductor losses is the conduction losses.

Conduction losses of the inductor is composed of two major parts: DC conduction loss and AC conduction loss. Same as core loss calculation, a generalized equation is derived to find the DC and AC parts of the current, which then is used to find the conduction losses of the inductor. Based on these loss calculations, a design methodology is proposed for gapped inductors, where the inductor parameters are designed to achieve the minimum losses of the inductor.

In this chapter, for verifying the claims of chapter 3, a prototype is implemented. The prototype is a 1.5kW, 400kHz Mosfet full-bridge inverter. Experimental results show that the implemented inverter benefits from a full-range soft-switching operation. Also, efficiency of the prototype in unity power factor achieves a peak of 96.2% at full-load, which is a 6.4% increase compared to the hard-switching case. Also, tests have been performed on the prototype in non-unity power factor. These tests show that as power factor diverges from zero, the proposed combined modulation technique exhibits better performance from other modulation methods.

4.2 Core Losses in the AC filter inductor

As stated in chapter 1, there are a few methods to calculate core losses in an inductor. However, these methods don't propose an accurate method to calculate the core losses in an inverter filter inductor. There are a few reasons that an accurate core loss calculation for the inverter inductor is important. First of all, it is much faster than finite-element analysis (FEA) simulations, where a large memory and intensive computations are required. Second, in the design procedure of the inverter magnetics, commonly the design is done considering the worst case switching cycle, where the highest ripple occurs to find the core specifications, which results in over-designed the inductors.

To find an equation for the AC inductor core losses, improved generalized Steinmetz equation (iGSE) proposed in [28] is used. iGSE presents an equation that takes core losses that happen by a non-sinusoidal current waveform into account. This is especially impor-

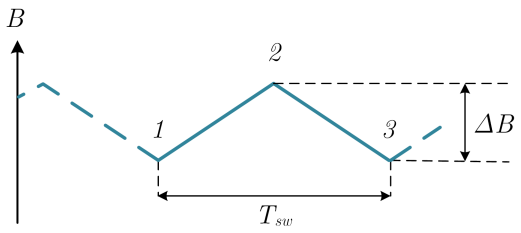


Figure 4.1: A typical piece-wise linear flux density waveform.

tant for switched-mode power supply applications, as most of the waveforms are piece-wise linear. In this section, iGSE method is expanded for a line cycle of inverter operation for different modulation schemes, which is then used in inverter AC filter design to increase the accuracy and speed of the design.

For piece-wise linear waveforms like Fig. 4.1, iGSE method can be simplified as,

$$\overline{P_v(t)} = \frac{k_i(\Delta B)^{\beta-\alpha}}{T_{sw}} \sum_m \left| \frac{B_{m+1} - B_m}{t_{m+1} - t_m} \right|^{\alpha} (t_{m+1} - t_m), \tag{4.1}$$

where

$$k_i = \frac{k}{2^{\beta+1}\pi^{\alpha-1}\left(0.2761 + \frac{1.7061}{\alpha+1.354}\right)}, \tag{4.2}$$

and $\overline{P_v(t)}$ is the instantaneous core loss density with unit of $\frac{\text{mW}}{\text{cm}^3}$. k, α and β are Steinmetz coefficients and can be found in manufacturer's datasheet. T_{sw} is the effective switching cycle duration. In the following section, this equation is used for calculating the core losses in inverter filter inductor.

4.2.1 Core loss Calculation of the Inverter AC Inductor

To apply iGSE to calculation of core losses in the AC filter inductor of an inverter, its formulation should be re-visited based on the inverter operation principle, which is explained in this section. First of all, flux density and change in the flux density can be written as a function of the current passing through the inductor.

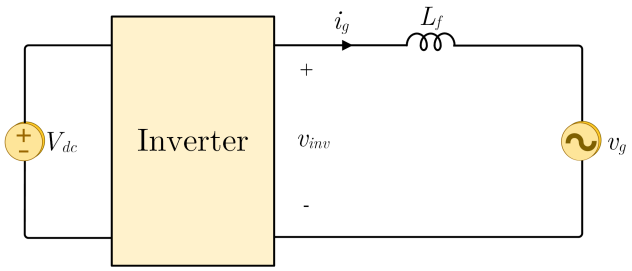


Figure 4.2: Typical grid-connected inverter with an L filter.

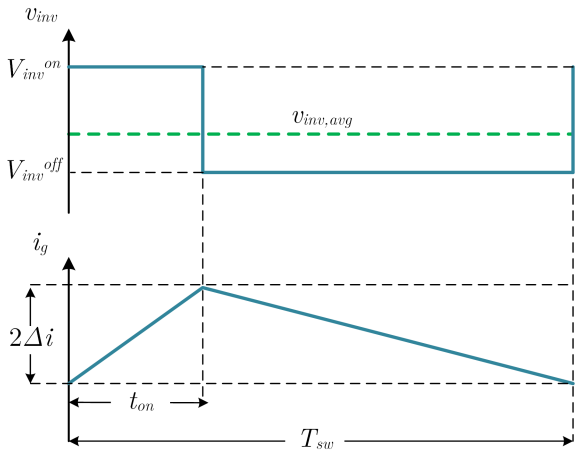


Figure 4.3: Sample of the inverter output voltage and current for one switching cycle.

$$B = \frac{\mu N}{l_c} i, \tag{4.3}$$

$$\Delta B = \frac{\mu N}{l_c} \Delta i, \tag{4.4}$$

where μ is the core permeability considering an ungapped core, N is the number of turns in the inductor, l_c is the effective path length of the inductor and I is the current passing through the inductor.

Based on [4], the ripple in a fixed switching frequency inverter in the steady state operation can be analytically calculated. An inverter connected to the grid through an L_f filter can be seen in Fig. 4.2, where $v_g = \widehat{V}_g \sin(\omega t)$ is the grid voltage, and $i_g = \widehat{I}^* \sin(\omega t - \phi)$ is the grid current. Also, inverter voltage (v_{inv}) and current (i_g) can be illustrated as Fig. 4.3. Based on these equations and figures, following equations are derived in [4] to find a

generalized equation for the current ripple of an inverter,

$$2\Delta i = \frac{T_{sw}}{L_f}\frac{\left(V_{\text{inv}}^{\text{on}} - v_g\right)\left(v_{\text{inv,avg}} - V_{\text{inv}}^{\text{off}}\right)}{V_{\text{inv}}^{\text{on}} - V_{\text{inv}}^{\text{off}}} = \frac{T_{sw}}{L_f}\frac{\left(v_g - V_{\text{inv}}^{\text{off}}\right)\left(V_{\text{inv}}^{\text{on}} - v_{\text{inv,avg}}\right)}{V_{\text{inv}}^{\text{on}} - V_{\text{inv}}^{\text{off}}}, \tag{4.5}$$

$$t_{\text{on}} = T_{sw}\frac{v_{\text{inv,avg}} - V_{\text{inv}}^{\text{off}}}{V_{\text{inv}}^{\text{on}} - V_{\text{inv}}^{\text{off}}}, \tag{4.6}$$

$$t_{\text{off}} = T_{sw}\frac{V_{\text{inv}}^{\text{on}} - v_{\text{inv,avg}}}{V_{\text{inv}}^{\text{on}} - V_{\text{inv}}^{\text{off}}}, \tag{4.7}$$

where $2\Delta i$ is the total change in the current of the inductor. $V_{\text{inv}}^{\text{on}}$ and $V_{\text{inv}}^{\text{off}}$ are the voltage levels in the output of the inverter, and their values depend on the modulation strategy. $v_{inv,avg}$ is the average value of the inverter voltage in a switching cycle and can be expressed by the following equations.

$$\overline{v_{\text{inv}}} = \widehat{V}_{ab}\sin(\omega t + \delta), \tag{4.8}$$

$$\widehat{V}_{ab} = \sqrt{\left(\omega L\widehat{I}^{*}cos(\phi)\right)^2 + \left(\widehat{V}_g + \omega L\widehat{I}^{*}sin(\phi)\right)^2}, \tag{4.9}$$

$$\delta = \tan^{-1}\left(\frac{\omega L\widehat{I}^{*}cos(\phi)}{\widehat{V}_g + \omega L\widehat{I}^{*}sin(\phi)}\right). \tag{4.10}$$

By replacing these equations in (4.4), a generalized equation for total flux density change in inverter inductors can be concluded.

$$\Delta B = \frac{\mu N}{l_c L_f}T_{sw}\frac{\left(V_{\text{inv}}^{\text{on}} - v_g\right)\left(v_{\text{inv,avg}} - V_{\text{inv}}^{\text{off}}\right)}{V_{\text{inv}}^{\text{on}} - V_{\text{inv}}^{\text{off}}}. \tag{4.11}$$

This equation along with (4.6) and (4.7) can be integrated to (4.1) to find a generalized equation for the core losses of the inverter inductor. Therefore, instantaneous core loss density for a switching cycle can be written as follows.

$$\overline{P_v(t)} = \frac{k_i}{T_{sw}}\left((\Delta B)^{\beta}(t_{on})^{-\alpha+1} + (\Delta B)^{\beta}(t_{off})^{-\alpha+1}\right), \tag{4.12}$$

$$\overline{P_v(t)} = \frac{k_i}{T_{sw}}\Bigg((\frac{\mu N}{l_c L_f} T_{sw} \frac{\left(V_{\text{inv}}^{\text{on}} - v_g\right)\left(v_{\text{inv,avg}} - V_{\text{inv}}^{\text{off}}\right)}{V_{\text{inv}}^{\text{on}} - V_{\text{inv}}^{\text{off}}})^{\beta} (T_{sw} \frac{v_{\text{inv,avg}} - V_{\text{inv}}^{\text{off}}}{V_{\text{inv}}^{\text{on}} - V_{\text{inv}}^{\text{off}}})^{-\alpha+1} + (\frac{\mu N}{l_c L_f} T_{sw} \frac{\left(v_g - V_{\text{inv}}^{\text{off}}\right)\left(V_{\text{inv}}^{\text{on}} - v_{\text{inv,avg}}\right)}{V_{\text{inv}}^{\text{on}} - V_{\text{inv}}^{\text{off}}})^{\beta} (T_{sw} \frac{V_{\text{inv}}^{\text{on}} - v_{\text{inv,avg}}}{T_{sw} - V_{\text{inv}}^{\text{off}}})^{-\alpha+1} \Bigg). \tag{4.13}$$

This equation can be simplified as,

$$\overline{P_v(t)} = k_i k_j T_{sw}^{\beta-\alpha} (V_{\text{inv}}^{\text{on}} - V_{\text{inv}}^{\text{off}})^{\alpha-\beta-1} \Bigg((V_{\text{inv}}^{\text{on}} - v_g)^{\beta} \left(v_{\text{inv,avg}} - V_{\text{inv}}^{\text{off}}\right)^{\beta-\alpha+1} + \left(v_g - V_{\text{inv}}^{\text{off}}\right)^{\beta} (V_{\text{inv}}^{\text{on}} - v_g)^{\beta-\alpha+1} \Bigg), \tag{4.14}$$

where

$$k_j = (\frac{\mu N}{l_c L_f})^{\beta} = (\frac{1}{N A_c})^{\beta}. \tag{4.15}$$

To calculate the total losses in a line cycle of the inverter, the instantaneous core loss density in (4.14) is calculated for a half line cycle of operation, which can be performed based on either t or ωt.

$$\overline{P_{v,inv}} = \frac{1}{\pi} k_i k_j T_{sw}^{\beta-\alpha} (V_{\text{inv}}^{\text{on}} - V_{\text{inv}}^{\text{off}})^{\alpha-\beta-1} \int_0^{\pi} \Bigg(\left(V_{\text{inv}}^{\text{on}} - \widehat{V}_g \sin(\omega t)\right)^{\beta} \left(\widehat{V}_{ab} \sin(\omega t + \delta) - V_{\text{inv}}^{\text{off}}\right)^{\beta-\alpha+1} + \left(\widehat{V}_g \sin(\omega t) - V_{\text{inv}}^{\text{off}}\right)^{\beta} \left(V_{\text{inv}}^{\text{on}} - \widehat{V}_{ab} \sin(\omega t + \delta)\right)^{\beta-\alpha+1} \Bigg) d\omega t \tag{4.16}$$

To calculate the core losses of the inverter, core loss density should be multiplied by the volume of the inductor.

$$\overline{P_{inv}} = \overline{P_{v,inv}} \frac{V_c}{1000}. \tag{4.17}$$

In this equation, $\overline{P_{inv}}$ is the total core loss of the inductor in a line cycle of operation, and V_c is the volume of the inductor with a unit of cm^3.

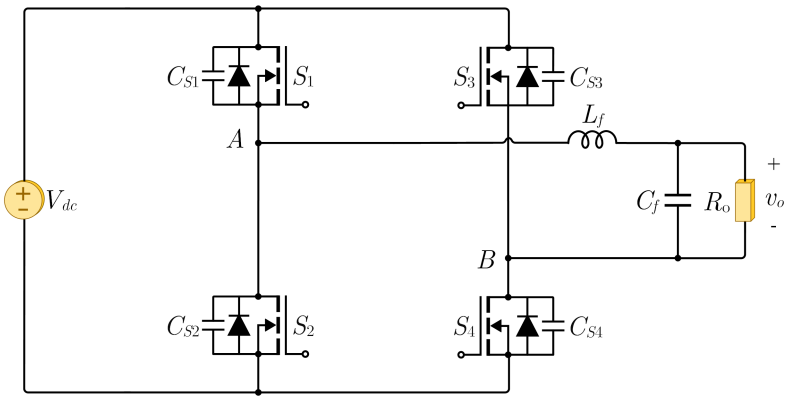


Figure 4.4: A full-bridge inverter.

This equation can be used to find the total losses of an inverter in any system configuration. However, iGSE method does not capture the effect of DC bias on the core loss, which can cause errors in calculating an accurate core loss. In [35], a method is proposed to consider the effect of DC bias in the iGSE method by finding the change in the Steinmetz parameters with DC bias. This work has performed a set of experiments, and found an equation for Steinmetz parameters through curve fitting. Accordingly, to consider DC bias in calculations, modified Steinmetz parameters are integrated in (4.16) as follows.

$$\begin{aligned}\overline{P_{v,inv}} = &\frac{1}{\pi}\int_0^{\pi} k_i(\omega t)k_j(\omega t)T_{sw}^{\beta(\omega t)-\alpha(\omega t)}(V_{\text{inv}}^{\text{on}} - V_{\text{inv}}^{\text{off}})^{\alpha(\omega t)-\beta(\omega t)-1} \\ &\left(\left(V_{\text{inv}}^{\text{on}} - \widehat{V}_g\sin(\omega t)\right)^{\beta(\omega t)}\left(\widehat{V}_{ab}\sin(\omega t+\delta) - V_{\text{inv}}^{\text{off}}\right)^{\beta(\omega t)-\alpha(\omega t)+1} + \right. \\ &\left.\left(\widehat{V}_g\sin(\omega t) - V_{\text{inv}}^{\text{off}}\right)^{\beta(\omega t)}\left(V_{\text{inv}}^{\text{on}} - \widehat{V}_{ab}\sin(\omega t+\delta)\right)^{\beta(\omega t)-\alpha(\omega t)+1}\right) d\omega t\end{aligned} \tag{4.18}$$

In the following paragraphs, to provide examples for core loss calculation with (4.16), a full-bridge inverter, as shown in Fig. 4.4, with both unipolar and bipolar modulations are analyzed.

4.2.2 Core Loss Calculation for Unipolar Modulation

For a full-bridge inverter with unipolar modulation technique and in the positive half-cycle of output voltage, $V_{\text{inv}}^{\text{on}}$ is equal to V_{DC}, and $V_{\text{inv}}^{\text{off}}$ is equal to 0. Therefore, (4.14) is written

for the unipolar modulation technique as follows,

$$\begin{aligned}\overline{P_v(\omega t)} =& k_i k_j T_{sw}^{\beta-\alpha} V_{DC}^{\alpha-\beta-1} \\ & \Bigg(\Big(V_{DC} - \widehat{V}_g \sin(\omega t) \Big)^{\beta} \Big(\widehat{V}_{ab} \sin(\omega t + \delta) \Big)^{\beta-\alpha+1} + \\ & \Big(\widehat{V}_g \sin(\omega t) \Big)^{\beta} \Big(V_{DC} - \widehat{V}_{ab} \sin(\omega t + \delta) \Big)^{\beta-\alpha+1} \Bigg).\end{aligned} \tag{4.19}$$

Also, grid voltage ($\widehat{V}_g$) can be written as a product of modulation index of the inverter (m_{peak}) and the input DC voltage, which results in $\widehat{V}_g = m_{peak} V_{DC}$. Since the filter inductance is small in high frequency inverters, voltage drop on the inductor is relatively small, and could be neglected. Therefore, the instantaneous core loss density equation for a full-bridge inverter with unipolar modulation, could be further simplified as,

$$\begin{aligned}\overline{P_v(\omega t)} =& k_i k_j T_{sw}^{\beta-\alpha} V_{DC}^{\beta} \\ & \Bigg(\big(1 - m_{peak} \sin(\omega t) \big)^{\beta} \big(m_{peak} \sin(\omega t) \big)^{\beta-\alpha+1} + \\ & \big(m_{peak} \sin(\omega t) \big)^{\beta} \big(1 - m_{peak} \sin(\omega t) \big)^{\beta-\alpha+1} \Bigg).\end{aligned} \tag{4.20}$$

To have a better understanding of the instantaneous core loss changes with time, Fig. 4.5 represents the waveform of the normalized instantaneous core loss ($\frac{\overline{P(\omega t)}}{\overline{P_{max}}}$) vs. ωt in a half line cycle of operation. $\overline{P_{max}}$ is the maximum instantaneous loss. This maximum loss for the unipolar mode happens when duty cycle is 0.5. Accordingly, the core loss density and subsequently the core loss in a line cycle of operation, can be found as follows.

$$\begin{aligned}\overline{P_{v,inv}} =& \frac{1}{\pi} k_i k_j T_{sw}^{\beta-\alpha} V_{DC}^{\alpha-\beta-1} \int_0^{\pi} \\ & \Bigg(\Big(V_{DC} - \widehat{V}_g \sin(\omega t) \Big)^{\beta} \Big(\widehat{V}_{ab} \sin(\omega t + \delta) \Big)^{\beta-\alpha+1} + \\ & \Big(\widehat{V}_g \sin(\omega t) \Big)^{\beta} \Big(V_{DC} - \widehat{V}_{ab} \sin(\omega t + \delta) \Big)^{\beta-\alpha+1} \Bigg) d\omega t.\end{aligned} \tag{4.21}$$

Also, the simplified form can be written as,

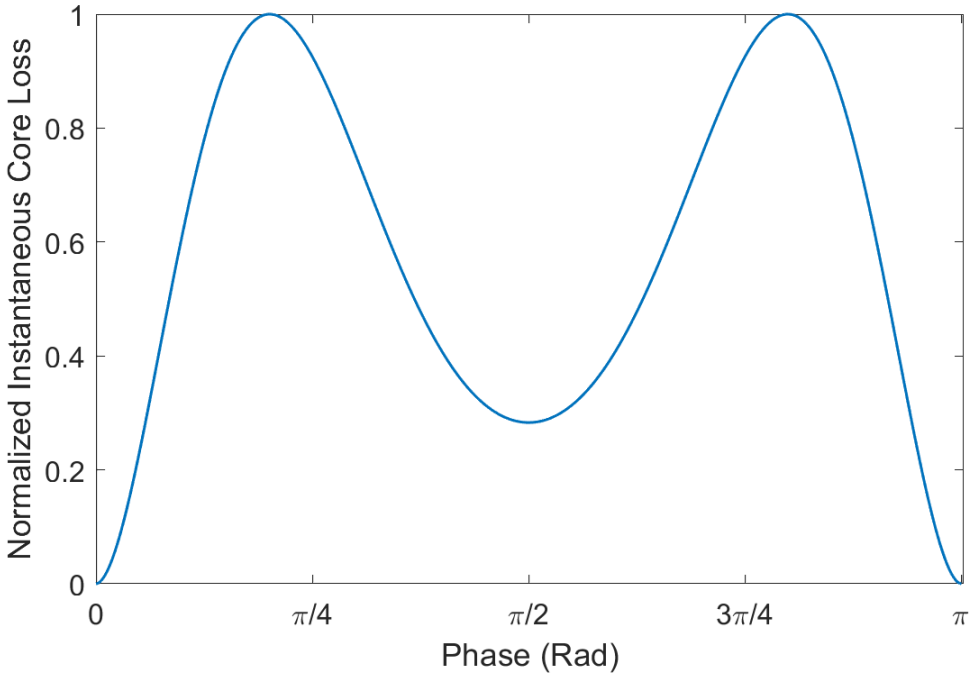


Figure 4.5: Inverter inductor's normalized instantaneous core losses waveform vs. ωt in half line cycle of operation with unipolar modulation.

$$\begin{aligned}\overline{P_{v,inv}} = &\frac{1}{\pi} k_i k_j T_{sw}^{\beta-\alpha} V_{DC}^{\beta} \int_0^{\pi} \\ &\Big(\left(1 - m_{peak}\sin(\omega t)\right)^{\beta} \left(m_{peak}\sin(\omega t)\right)^{\beta-\alpha+1} + \\ &\left(m_{peak}\sin(\omega t)\right)^{\beta} \left(1 - m_{peak}\sin(\omega t)\right)^{\beta-\alpha+1} \Big) d\omega t.\end{aligned} \tag{4.22}$$

There is no closed-form equation that can be derived from the above integral, since the integral can't produce an elementary function. Therefore, this integral should be calculated by numerical methods such as trapezoidal method, midpoint rule and etc. Moreover, based on this simplified equation, core loss of an inverter inductor with the unipolar modulation technique can be divided into two parts, one is only dependent on system specifications and material, and other is the constant values that are defined by the design parameters. Consequently, this equation can be written as,

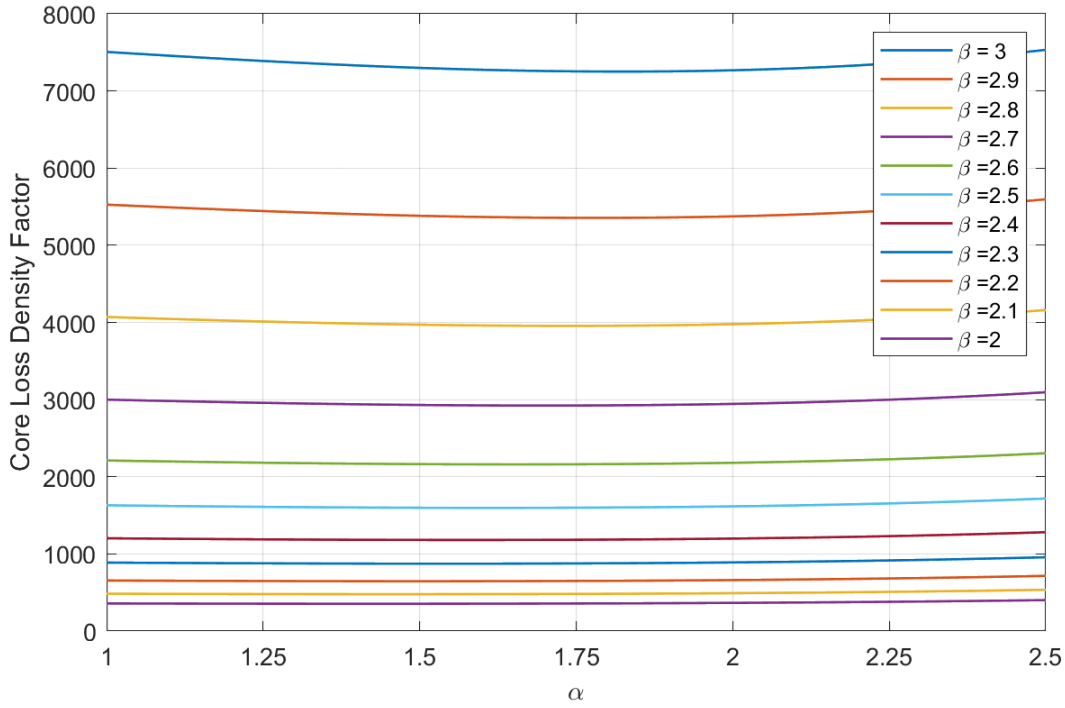


Figure 4.6: $\overline{P_{v,sys}}$ for different set of α and β values in unipolar mode with system specifications of $V_{DC} = 400V$ and $V_o = 240V_{rms}$.

$$\begin{aligned}\overline{P_{v,inv}} =& kk_j \frac{T_{sw}^{\beta-\alpha} V_{DC}^{\beta}}{2^{\beta+1}\pi^{\alpha}\left(0.2761+\frac{1.7061}{\alpha+1.354}\right)} \int_0^{\pi} \\ & \Big(\left(1-m_{peak}\sin(\omega t)\right)^{\beta} \left(m_{peak}\sin(\omega t)\right)^{\beta-\alpha+1} + \\ & \left(m_{peak}\sin(\omega t)\right)^{\beta} \left(1-m_{peak}\sin(\omega t)\right)^{\beta-\alpha+1} \Big) d\omega t, \end{aligned} \tag{4.23}$$

$$\overline{P_{v,inv}} = kk_j T_{sw}^{\beta-\alpha} \overline{P_{v,sys}}, \tag{4.24}$$

where,

$$\overline{P_{v,sys}} = \frac{V_{DC}^{\beta}}{2^{\beta+1}\pi^{\alpha}\left(0.2761+\frac{1.7061}{\alpha+1.354}\right)} \int_0^{\pi} \left(\left(1-m_{peak}\sin(\omega t)\right)^{\beta} \left(m_{peak}\sin(\omega t)\right)^{\beta-\alpha+1} + \left(m_{peak}\sin(\omega t)\right)^{\beta} \left(1-m_{peak}\sin(\omega t)\right)^{\beta-\alpha+1} \right) d\omega t. \tag{4.25}$$

$\overline{P_{v,sys}}$ can be calculated before the design process of the inverter inductor. Therefore, for common system specifications, $\overline{P_{v,sys}}$ is calculated for different set of Steinmetz parameters. Fig. 4.6 shows the value of $\overline{P_{v,sys}}$ in a line cycle of operation for different sets of α and β values. These figures are very helpful in the design process. As k_j is the only parameter that changes in each design iteration. This feature is the basis of the proposed design process in the next section. It should be noted that to account for the effect of DC bias in the equation, k_i becomes a function of DC bias, which is a function of time. Therefore, k_i should be considered while calculating the continuous average of the core loss as a function of time.

4.2.3 Core Loss Calculation of for the Bipolar Modulation

For a full-bridge inverter with bipolar modulation technique, $V_{\text{inv}}^{\text{on}}$ is equal to V_{DC}, and $V_{\text{inv}}^{\text{off}}$ is equal to $-V_{DC}$ regardless of the voltage output. Therefore, same as the bipolar mode, (4.16) is written for the bipolar modulation technique as follows,

$$\overline{P_{v,inv}} = \frac{1}{\pi} k_i k_j T_{sw}^{\beta-\alpha} (2V_{DC})^{\alpha-\beta-1} \int_0^{\pi} \left(\left(V_{DC}-\widehat{V}_g\sin(\omega t)\right)^{\beta} \left(\widehat{V}_{ab}\sin(\omega t+\delta)+V_{DC}\right)^{\beta-\alpha+1} + \left(\widehat{V}_g\sin(\omega t)+V_{DC}\right)^{\beta} \left(V_{DC}-\widehat{V}_{ab}\sin(\omega t+\delta)\right)^{\beta-\alpha+1} \right) d\omega t. \tag{4.26}$$

By replacing $\widehat{V}_g$ with $\widehat{V}_g = m_{peak}V_{DC}$, and neglecting the voltage drop of the inductor, following equation can be derived.

$$\overline{P_{v,inv}} = \frac{1}{\pi} k_i k_j T_{sw}^{\beta-\alpha} (2V_{DC})^{\beta} \int_0^{\pi} \left(\left(\frac{1}{2} - \frac{m_{peak}}{2} \sin(\omega t) \right)^{\beta} \left(\frac{1}{2} + \frac{m_{peak}}{2} \sin(\omega t) \right)^{\beta-\alpha+1} + \left(\frac{1}{2} + \frac{m_{peak}}{2} \sin(\omega t) \right)^{\beta} \left(\frac{1}{2} - \frac{m_{peak}}{2} \sin(\omega t) \right)^{\beta-\alpha+1} \right) d\omega t. \tag{4.27}$$

Instantaneous core losses vs. phase of the output voltage is illustrated in Fig. 4.7. Also, similar to the unipolar modulation, inductor core loss with bipolar modulation can be separated into two parts,

$$\overline{P_{v,inv}} = k k_j \frac{T_{sw}^{\beta-\alpha} (2V_{DC})^{\beta}}{2^{\beta+1} \pi^{\alpha} \left(0.2761 + \frac{1.7061}{\alpha+1.354}\right)} \int_0^{\pi} \left(\left(\frac{1}{2} - \frac{m_{peak}}{2} \sin(\omega t) \right)^{\beta} \left(\frac{1}{2} + \frac{m_{peak}}{2} \sin(\omega t) \right)^{\beta-\alpha+1} + \left(\frac{1}{2} + \frac{m_{peak}}{2} \sin(\omega t) \right)^{\beta} \left(\frac{1}{2} - \frac{m_{peak}}{2} \sin(\omega t) \right)^{\beta-\alpha+1} \right) d\omega t. \tag{4.28}$$

$$\overline{P_{v,sys}} = \frac{(2V_{DC})^{\beta}}{2^{\beta+1} \pi^{\alpha} \left(0.2761 + \frac{1.7061}{\alpha+1.354}\right)} \int_0^{\pi} \left(\left(\frac{1}{2} - \frac{m_{peak}}{2} \sin(\omega t) \right)^{\beta} \left(\frac{1}{2} + \frac{m_{peak}}{2} \sin(\omega t) \right)^{\beta-\alpha+1} + \left(\frac{1}{2} + \frac{m_{peak}}{2} \sin(\omega t) \right)^{\beta} \left(\frac{1}{2} - \frac{m_{peak}}{2} \sin(\omega t) \right)^{\beta-\alpha+1} \right) d\omega t. \tag{4.29}$$

Also, $\overline{P_{v,sys}}$ waveform for different sets of α and β values is illustrated in Fig. 4.8.

4.2.4 Core Loss Calculation for the Combined Modulation

In the combined modulation method, inverter is operating with both of the modulation techniques in each line cycle. As stated in chapter 3, bipolar modulation technique is utilized in small duty cycles, where unipolar modulation technique does not provide enough excitation for the coupled inductor to change the direction of the switch current. This

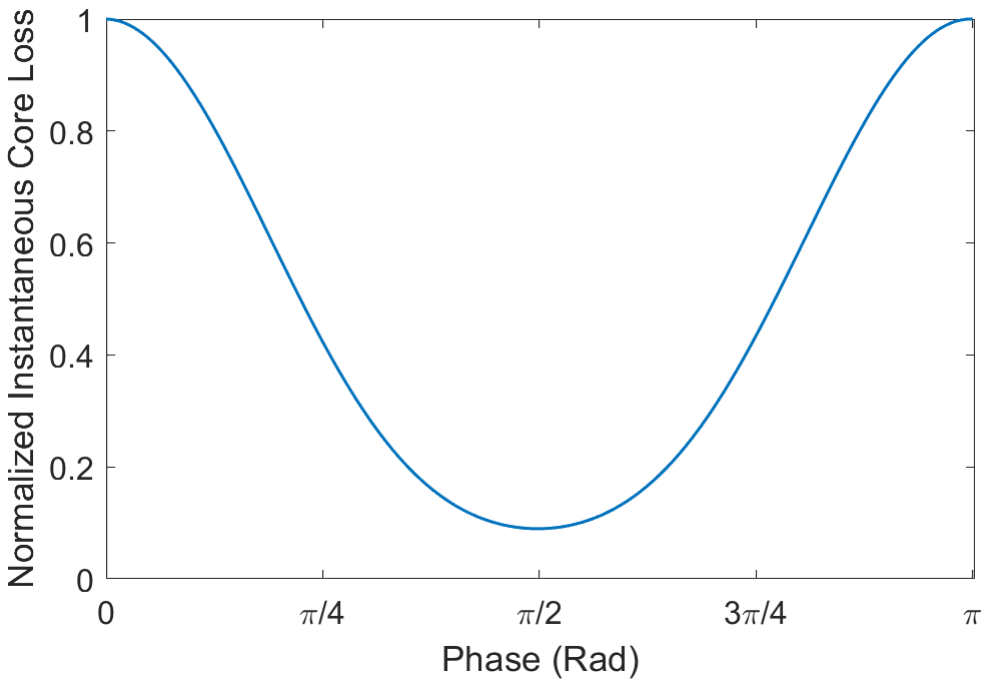


Figure 4.7: Inverter inductor's normalized instantaneous core losses waveform vs. phase in half line cycle of operation with bipolar modulation.

transition between two modulation techniques happen when the duty cycle reaches m_{ch}. Therefore, the core loss density equation in a line cycle can be written as follows,

$$\overline{P_{v,inv}} = \frac{2}{\pi}\left(\int_0^{\sin^{-1}(\frac{m_{ch}}{m_{peak}})} \overline{P_{v,bi}(t)}d\omega t + \int_{\sin^{-1}(\frac{m_{ch}}{m_{peak}})}^{\frac{\pi}{2}} \overline{P_{v,uni}(t)}d\omega t\right), \tag{4.30}$$

where $\overline{P_{v,bi}(t)}$ and $\overline{P_{v,uni}(t)}$ are instantaneous core loss density values for bipolar and unipolar modulations, respectively. To find the core loss density in a line cycle of operation, the integral of (4.26) and (4.21) from $\omega t = 0$ to $\omega t = \frac{\pi}{2}$ is considered.

This equation is used to find the total core losses of the soft-switching inverter inductor in a line cycle of operation. The results of this calculation is utilized in the loss analysis section to compare the performance of the soft-switching inverter to the hard-switching inverter.

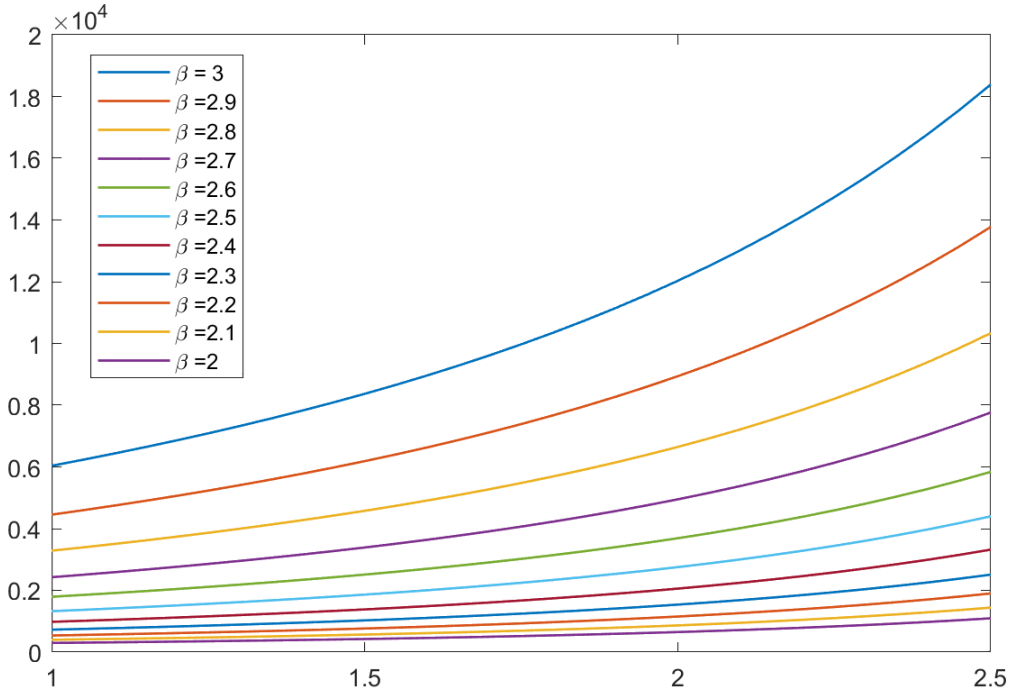


Figure 4.8: $\overline{P_{v,sys}}$ for different set of α and β values in bipolar mode with system specifications of $V_{DC} = 400V$ and $V_o = 240V_{rms}$.

$$\begin{aligned}\overline{P_{v,inv}} = &\frac{2}{\pi} k_i k_j T_{sw}^{\beta-\alpha} V_{DC}^{\alpha-\beta-1} \\ &\left(\int_0^{\sin^{-1}(\frac{m_{ch}}{m_{peak}})} \left(\left(V_{DC} - \widehat{V}_g \sin(\omega t) \right)^{\beta} \left(\widehat{V}_{ab} \sin(\omega t + \delta) \right)^{\beta-\alpha+1} + \right. \right. \\ &\left. \left(\widehat{V}_g \sin(\omega t) \right)^{\beta} \left(V_{DC} - \widehat{V}_{ab} \sin(\omega t + \delta) \right)^{\beta-\alpha+1} \right) d\omega t + \\ &\int_{\sin^{-1}(\frac{m_{ch}}{m_{peak}})}^{\frac{\pi}{2}} 2^{\alpha-\beta-1} \left(\left(V_{DC} - \widehat{V}_g \sin(\omega t) \right)^{\beta} \left(\widehat{V}_{ab} \sin(\omega t + \delta) + V_{DC} \right)^{\beta-\alpha+1} + \right. \\ &\left. \left. \left(\widehat{V}_g \sin(\omega t) + V_{DC} \right)^{\beta} \left(V_{DC} - \widehat{V}_{ab} \sin(\omega t + \delta) \right)^{\beta-\alpha+1} \right) d\omega t \right).\end{aligned} \tag{4.31}$$

In this equation, value of m_{ch} affects the total losses. Considering Figs. 4.5 and 4.7, instantaneous core loss density vs. phase of the line cycle for the line cycle of operation can be calculated, and m_{ch} determines the phase that the transition between unipolar and bipolar modulation methods happens.

The auxiliary circuit, that is presented in Fig. 2.2, changes the current rate in the coupled inductor. This change in the current rate is through the leakage inductance. However, the voltage on the magnetizing inductance remains the same. Due to the fact that the magnetizing inductance is responsible for the core losses, and also leakage inductance doesn't introduce any direct effects to the core loss, the core loss equation does not consider the effect of leakage inductance on the current change rate. However, there will be a voltage drop on the magnetizing inductance when the auxiliary circuit is operating. This voltage drop can be considered negligible by designing the coupled inductor to have a small leakage inductance in the primary side. This is the case in the presented soft-switching inverter. Therefore, the voltage drop on the magnetizing inductance has been considered to be zero. Therefore, core loss equation is almost the same with or without the auxiliary circuit.

4.3 Conduction Losses in the AC filter inductor

Conduction losses in the inductor arise from the resistivity of inductor wires against the current passing through them. There are two types of conduction losses in the inductor. First one is the DC conduction loss, which is a result of DC current passing through the inductor wires. Second one is the AC conduction loss, which is a product of high frequency components of the inductor current. These high frequency components result in skin effect losses and proximity losses. Therefore, the resistivity of the windings are different than the winding resistivity against DC or low frequency components.

In [34], an equation is utilized to find the total conduction losses of the inverter. In this method, DC resistance of the inductor is calculated from the designed winding specifications. For the AC resistance calculation, a factor is multiplied to the DC resistance. This factor depends on the winding structure and the skin depth of the wires. Since the skin depth of the wires is dependent on the frequency, an equivalent frequency is calculated to avoid calculating the resistance and current amplitude for each harmonic component frequency of the inverter. Following equation is provided in [34] to find the total conduction

losses.

$$P_{cu} = R_{DC} I_{DC}^2 + k_c R_{DC} I_{AC}^2, \tag{4.32}$$

$$R_{DC} = \frac{\rho N J \times MLT}{I_{rms}} \left[1 + \alpha_{20} \left(T_{\max} - 20^{\circ}\mathrm{C}\right)\right], \tag{4.33}$$

where k_c is the factor that relates the AC resistance to the DC resistance, ρ is the electrical resistivity of the wire, N is the number of turns, J is the current density of the wire and MLT is the mean-length turn of the core. Based on this equation, along with the winding resistance calculation, AC and DC components of the inductor current is needed to calculate the total conduction losses of the inverter inductor. In the following paragraphs, a generalized equation is derived to find the DC and AC components of the inductor current in inverters.

4.3.1 Generalized DC and AC Current Components in Inverter Inductor

In inverters, inductor current is composed of a 60Hz component and also high frequency current components that are result of switching actions in the inverter. The common inductor current waveform shape in power electronics converters is illustrated in Fig. 4.3. For this waveform, root mean square of the current is calculated by the following equation.

$$I_{rms} = \sqrt{{I_{DC}}^2 + {I_{AC}}^2} = \sqrt{I_{DC}^2 + \frac{(2\Delta i)^2}{12}}. \tag{4.34}$$

In switching converters this equation is used to calculate the RMS of the inductor current in each switching cycle. However, in inverters, all the operating points in a line cycle of operation should be considered to calculate an accurate conduction loss in the inductor. For inverters, since the 60Hz component of the inductor current can be considered constant during a switching cycle. Therefore, I_{DC} in each switching cycle is considered as the value

of the 60Hz component of the current. Also, a generalized equation was found for $2\Delta i$ in (4.5) to find I_{AC}. Replacing these values in (4.34) results in the following equation.

$$I_{rms}(t)=\sqrt{\left(\widehat{I}^{*}\sin(\omega t-\phi)\right)^{2}+\frac{1}{12}\left(\frac{T_{sw}}{L_f}\frac{\left(V_{\text{inv}}^{\text{on}}-\widehat{V}_g\sin(\omega t)\right)\left(\widehat{V}_{ab}\sin(\omega t+\delta)-V_{\text{inv}}^{\text{off}}\right)}{V_{\text{inv}}^{\text{on}}-V_{\text{inv}}^{\text{off}}}\right)^{2}}. \tag{4.35}$$

This equation provides the RMS value of the inductor current in a single switching cycle. Similar to the core loss generalization of section 4.2, the RMS current is calculated in a line cycle of operation by calculating the continuous average of the $I_{rms}^{2}(t)$ in a line cycle, and then taking the square root of the calculated average of $I_{rms}^{2}(t)$.

$$I_{rms}(t)=\sqrt{\frac{1}{\pi}\int_{0}^{pi}\left(\left(\widehat{I}^{*}\sin(\omega t-\phi)\right)^{2}+\frac{1}{12}\left(\frac{T_{sw}}{L_f}\frac{\left(V_{\text{inv}}^{\text{on}}-\widehat{V}_g\sin(\omega t)\right)\left(\widehat{V}_{ab}\sin(\omega t+\delta)-V_{\text{inv}}^{\text{off}}\right)}{V_{\text{inv}}^{\text{on}}-V_{\text{inv}}^{\text{off}}}\right)^{2}\right)d\omega t}. \tag{4.36}$$

After integration, a closed form general equation is derived for accurate calculation of the RMS value of the inductor.

$$I_{DC,inv}{}^{2}=\frac{\widehat{I}^{*2}}{2}, \tag{4.37}$$

$$\begin{aligned}I_{AC,inv}^{2}=&\frac{1}{288\pi}\left(\frac{T_{sw}}{L_f(V_{\text{inv}}^{\text{on}}-V_{\text{inv}}^{\text{off}})}\right)^{2}\left(6\left(2\pi V_{\text{inv}}^{\text{on}\,2}-8V_{\text{inv}}^{\text{on}}\widehat{V}_g+\pi\widehat{V}_g^{2}\right)\left(\widehat{V}_{ab}^{2}+2V_{\text{inv}}^{\text{off}\,2}\right)-\right.\\&\left.16\widehat{V}_{ab}V_{\text{inv}}^{\text{off}}\left(6V_{\text{inv}}^{\text{on}\,2}-3\pi V_{\text{inv}}^{\text{on}}\widehat{V}_g+4\widehat{V}_g^{2}\right)\cos(\delta)+\widehat{V}_g\widehat{V}_{ab}^{2}\left(3\pi\widehat{V}_g-16V_{\text{inv}}^{\text{on}}\right)\cos(2\delta)\right).\end{aligned} \tag{4.38}$$

This generalized equation is used to find the conduction losses of the inverter inductor based on (4.32). Table 4.1 provides the utilization of this generalized equation for unipolar

Table 4.1: DC and AC components of inductor current in inverters with well-known modulation techniques.

Modulation	I_{DC}^2	I_{AC}^2	Simplified I_{AC}^2
Unipolar	$\frac{\widehat{I}^{*2}}{2}$	$\frac{1}{288\pi}\left(\frac{T_{sw}}{L_f V_{DC}}\right)^2\Big(12\pi {V_{DC}}^2\widehat{V}_{ab}^2 - (48+16\cos(2\delta))\widehat{V}_g V_{DC}\widehat{V}_{ab}^2 + 3\pi(2+\cos(2\delta))\widehat{V}_g^2\widehat{V}_{ab}^2\Big)$	$\frac{1}{288\pi}\left(\frac{T_{sw}V_{DC}}{L_f}\right)^2\Big(9\pi m_{peak}^4 - 64m_{peak}^3 + 12\pi m_{peak}^2\Big)$
Bipolar	$\frac{\widehat{I}^{*2}}{2}$	$\frac{1}{288\pi}\left(\frac{T_{sw}}{2L_f V_{DC}}\right)^2\Big(12\pi {V_{DC}}^2\widehat{V}_{ab}^2 - (48+16\cos(2\delta))\widehat{V}_g V_{DC}\widehat{V}_{ab}^2 + 3\pi(2+\cos(2\delta))\widehat{V}_g^2\widehat{V}_{ab}^2 + 24\pi V_{DC}^4 - 96\widehat{V}_g V_{DC}^3 + 12\pi\widehat{V}_g^2 V_{DC}^2 + 96\cos(\delta)V_{DC}^3\widehat{V}_{ab} - 48\pi\widehat{V}_g V_{DC}^2\widehat{V}_{ab}\cos(\delta) + 64\widehat{V}_g^2 V_{DC}\widehat{V}_{ab}\cos(\delta)\Big)$	$\frac{1}{288\pi}\left(\frac{T_{sw}V_{DC}}{L_f}\right)^2\Big(\frac{9\pi}{4}m_{peak}^4 - 6\pi m_{peak}^2 + 6\pi\Big)$

and bipolar modulation techniques. Also, to simplify the equations, the voltage drop on the inductor is considered to be zero. For the combined modulation technique, integration should be performed considering the change in the modulation when duty cycle reaches m_{ch}. Therefore, RMS current of the inductor in a line cycle is:

$$I_{rms}(t)^2 = \frac{\widehat{I}^{*2}}{2} + \frac{2}{\pi}\left(\int_0^{\sin^{-1}(\frac{m_{ch}}{m_{peak}})} \frac{1}{12}\left(\frac{T_{sw}}{2L_f V_{DC}}\right)^2 \left(\left(V_{DC} - \widehat{V}_g \sin(\omega t)\right)\left(\widehat{V}_{ab}\sin(\omega t + \delta) + V_{DC}\right)\right)^2 d\omega t + \int_{\sin^{-1}(\frac{m_{ch}}{m_{peak}})}^{\pi/2} \frac{1}{12}\left(\frac{T_{sw}}{L_f V_{DC}}\right)^2 \left(\left(V_{DC} - \widehat{V}_g \sin(\omega t)\right)\left(\widehat{V}_{ab}\sin(\omega t + \delta)\right)\right)^2 d\omega t\right). \tag{4.39}$$

A simplified closed form of (4.39) is:

$$I_{rms}(t)^2 = \frac{\widehat{I}^{*2}}{2} + \frac{1}{576\pi}\left(\frac{T_{sw}V_{DC}}{L_f}\right)^2 \left(-\left(18\pi + 27\sin^{-1}\left(\frac{m_{ch}}{m_{\text{peak}}}\right)\right) m_{peak}^4 + \left((33m_{ch} - 64)\sqrt{m_{peak}^2 - m_{ch}^2} + 24\sin^{-1}\left(\frac{m_{ch}}{m_{\text{peak}}}\right) - 16\right) m_{peak}^2 - 8m_{peak} + \left(6m_{ch}^3 - 32m_{ch}^2 - 24m_{ch} + 96\right)\sqrt{m_{peak}^2 - m_{ch}^2} + 24\sin^{-1}\left(\frac{m_{ch}}{m_{\text{peak}}}\right)\right). \tag{4.40}$$

Therefore, conduction loss equation is derived for the inverter inductor with unipolar, bipolar and also the combined modulation technique.

4.4 Gapped Inverter Inductor Design Method

This section focuses on the design of a multi-winding inverter inductor with integration of the derived inverter inductor loss equations. To find a design methodology for the inverter inductor, design strategies in [34, 36] are used as foundations of the proposed methodology.

The objective of the design methodology is to find the optimum core size, number of turns and wire specifications for a desired inductance value and temperature rise to have

the minimum losses in the inverter inductor. Before the design process, inverter parameters and specifications of the selected material should be known.

Step1: Core Selection

In the first step, core size is selected based on the chosen material and the desired temperature rise of the inductor. In [36], an equation is derived for the minimum core window winding area and cross sectional area product (A_p).

$$A_p = \left[\frac{\sqrt{1+\gamma} F_i L_f \widehat{I}^{*2}}{B_{\max} K_t \sqrt{k_u \Delta T}} \right]^{\frac{8}{7}}, \tag{4.41}$$

where F_i is the ratio of the RMS current to the peak current of the inductor. B_{max} is the maximum flux density that does not saturate the core. K_t is a coefficient and is equal to 48.2×10^3. k_u is the window utilization factor, and ΔT is the desired temperature rise. γ is the core loss to conduction loss ratio, and for the first try it should be estimated. A decent estimation can be done considering the ripple of the inductor current.

For a multi-winding inductor, A_p is derived as seen in:

$$A_p = \left[\frac{\sqrt{1+\gamma} K_{ip} L_p \widehat{I_p}^{*2}}{B_{\max} K_t \left(k_{up} / \sqrt{k_u} \right) \sqrt{\Delta T}} \right]^{8/7}, \tag{4.42}$$

where the inductance, current and coefficients are written only for the primary winding.

Another method to find the required core size is to use an empirical equation suggested in [34]. In this empirical equation, largest dimension of the inductor (a_{co}) is found based on:

$$S_{\text{tot}} = \sum_{\text{i=1}}^{n} V_{rms,i} I_{rms,i} = A a_{co}^{\sigma} \Rightarrow a_{co} = \left(\frac{S_{\text{tot}}}{A} \right)^{1/\sigma} \tag{4.43}$$

where, σ and A are coefficients found empirically. σ is between $\sigma = 2.8$ and $\sigma = 3.2$. A is in the range of $A = 5 \times 10^6$ to $A = 25 \times 10^6$ for the ferrite cores.

Step2: Loss Budget

In this step, desired temperature rise and surface area of the inductor determine the total loss budget of the inductor.

$$P_{\text{budget}} = P_{\text{cu}} + P_{\text{core}} = h_c A_t \Delta T. \tag{4.44}$$

h_c is the coefficient of heat transfer, and for cores in in switching power supplies a typical value of $h_c = 10\ \text{W}/\text{m}^{2\circ}\text{C}$ is used. Also, A_t is the total surface area of the inductor. If A_t is not available, the following empirical equation [34] is used to estimate the loss budget of the inverter inductor.

$$P_{\text{budget}} = \frac{0.06}{\sqrt{V_c}} \Delta T. \tag{4.45}$$

where V_c is the core volume with the unit of m^3.

For a multi-winding inductor, total losses can be classified as follows,

$$P_{\text{budget}} = \sum_{\text{i=1}}^{n} P_{\text{cu,i}} + P_{\text{core}} \tag{4.46}$$

Step3: Core Loss to Conduction Loss Ratio

In this step, total loss budget found in the last step should be allocated to core loss and conduction loss based on the estimated value for γ.

$$P_{\text{cu}} = \frac{P_{budget}}{1+\gamma}, \tag{4.47}$$

$$P_{\text{core}} = \frac{\gamma P_{budget}}{1+\gamma}, \tag{4.48}$$

Also, it should be noted that the AC conduction loss is not considered in this step. This is due to the fact that compared to the other two losses, AC conduction loss is small, and it depends on the winding structure, which makes its calculation complicated.

Step4: Wire Specifications

To select the wire size, allowed current density in the wire is calculated based on the temperature rise and other known parameters with the following equation.

$$\alpha_w = I_{\text{rms}}/J_o, \tag{4.49}$$

$$J_o = K_t \sqrt{\frac{\Delta T}{k_u(1+\gamma)}} \frac{1}{\sqrt[8]{A_p}}. \tag{4.50}$$

Based on this equation, minimum copper area of a wire is calculated. Since the design is aimed for high-frequency inverters, litz wires are usually used to reduce the AC conduction losses of the inductor. Single strand diameter of the wire is selected to reduce the eddy-current effects of the most dominant high-frequency component of the inductor current.

The optimum distribution of current in the available area is to have the same current density in each winding [36]. Therefore, after finding the current density, the wire area for each winding is found by having the RMS current of the inverter inductor.

Step5: Number of Turns

To find the number of turns (N), two things should be considered. First, winding should fit in the available window area. Therefore, a constraint for increasing number of turns is the available window area. Following equation is the mathematical expression for this constraint.

$$N_{max} = \frac{k_u W_A}{\alpha_{w,ins}}, \tag{4.51}$$

where W_A is the window area and $\alpha_{w,ins}$ is the practical wire area considering the insulation.

Second, N affects both inverter inductor core loss equation as seen in (4.15) and (4.16) and conduction loss equation in (4.32) and (4.33). Therefore, total losses of the inverter inductor can be written as a function of number of turns.

$$P_{tot} = P_{cu} + P_{core} = NF_{cu}(MLT, \alpha_w, L_f, I_{DC}) + (\frac{1}{N})^{\beta} F_{core}(\alpha, \beta, k, V_c, A_c, T_{sw}, V_{DC}, m_{peak}), \tag{4.52}$$

$$F_{cu} = \frac{\rho \times MLT}{\alpha_w} \left[1 + \alpha_{20} \left(T_{\max} - 20^{\circ}\mathrm{C}\right)\right] \frac{\widehat{I}^{*2}}{2}, \tag{4.53}$$

$$F_{core} = \frac{kV_c T_{sw}^{\beta-\alpha}}{A_c^{\beta}} \overline{P_{v,sys}}. \tag{4.54}$$

F_{core} and F_{cu} can be determined by the parameters found in previous steps. The only remaining parameter to be found is the number of turns. To find an optimum number of turns, $\frac{dP_{tot}}{dN} = 0$ is solved. As stated before, in the design process, AC conduction losses are not taken into account.

$$\frac{dP_{tot}}{dN} = 0 \Rightarrow -\beta N^{-\beta-1} F_{core} + F_{cu} = 0 \Rightarrow N_{opt} = \sqrt[\beta+1]{\frac{\beta F_{core}}{F_{cu}}} \tag{4.55}$$

Therefore, an optimum number of turns is found in (4.55). It should be noted that this optimum value should be less than N_{max}.

For a multi-winding inductor, these equations can be re-written in a way to account for the total losses of the inductor.

Step6: Airgap Length

The only remaining parameter to be found is the airgap length of the inductor, which can be found by the following equation.

$$\sum l_g = \frac{\mu_0 A_c N^2}{L_f} - \frac{l_e}{\mu_c} \tag{4.56}$$

After finding the total airgap length, the design iteration is completed.

Step7: Loss Calculation

After finding all the parameters, exact losses of the inductor is calculated in this step. Core loss is found from (4.16) and conduction loss is found from (4.32). After finding these values, γ should be re-calculated to check if the first estimate is accurate. If not, with the new calculated γ design process is repeated to find the optimum design.

Fig. 4.9 demonstrates the flow chart of the proposed design method for the output inductor of the inverter.

4.5 Experimental Results of the Proposed Full-range Soft-switching Inverter

4.5.1 Design and Loss Analysis

After finding the possible and feasible set of values for L_{aux} and $I_{sw,neg}$, inverter losses with each set of values were calculated. The set of values for these parameters have been selected according to these calculation to minimize the losses in the auxiliary circuit as much as possible. L_{aux} of $1.8\mu H$ and $I_{sw,neg}$ equal to 3.5A has been selected. Table 4.2 reports the converter components and their part-number and designed values for inverter parameters.

A coupled inductor has been designed by using the proposed design method with E55/28/21 cores of 3F3 material, and for the windings, litz wires are used. Primary winding has two parallel 12 turns of AWG46 with 1000 strands interleaved with the secondary winding that has 8 turns of AWG46 with 1000 strands. The cross section of the coupled inductor is shown in Fig. 4.10a. The windings are interleaved to decrease the proximity losses and the leakage inductance . To decrease the total losses in the inductor, the distance between the wires in the winding are larger near the air gaps to decrease the fringing losses. Simulation results of the designed inverter show a total loss of 4.89W in the inductor in the worst operating point of the inverter. Fig. 4.10b shows the primary and secondary current in the coupled inductor in the Ansys software. Also, Fig. 4.10c shows the flux density of

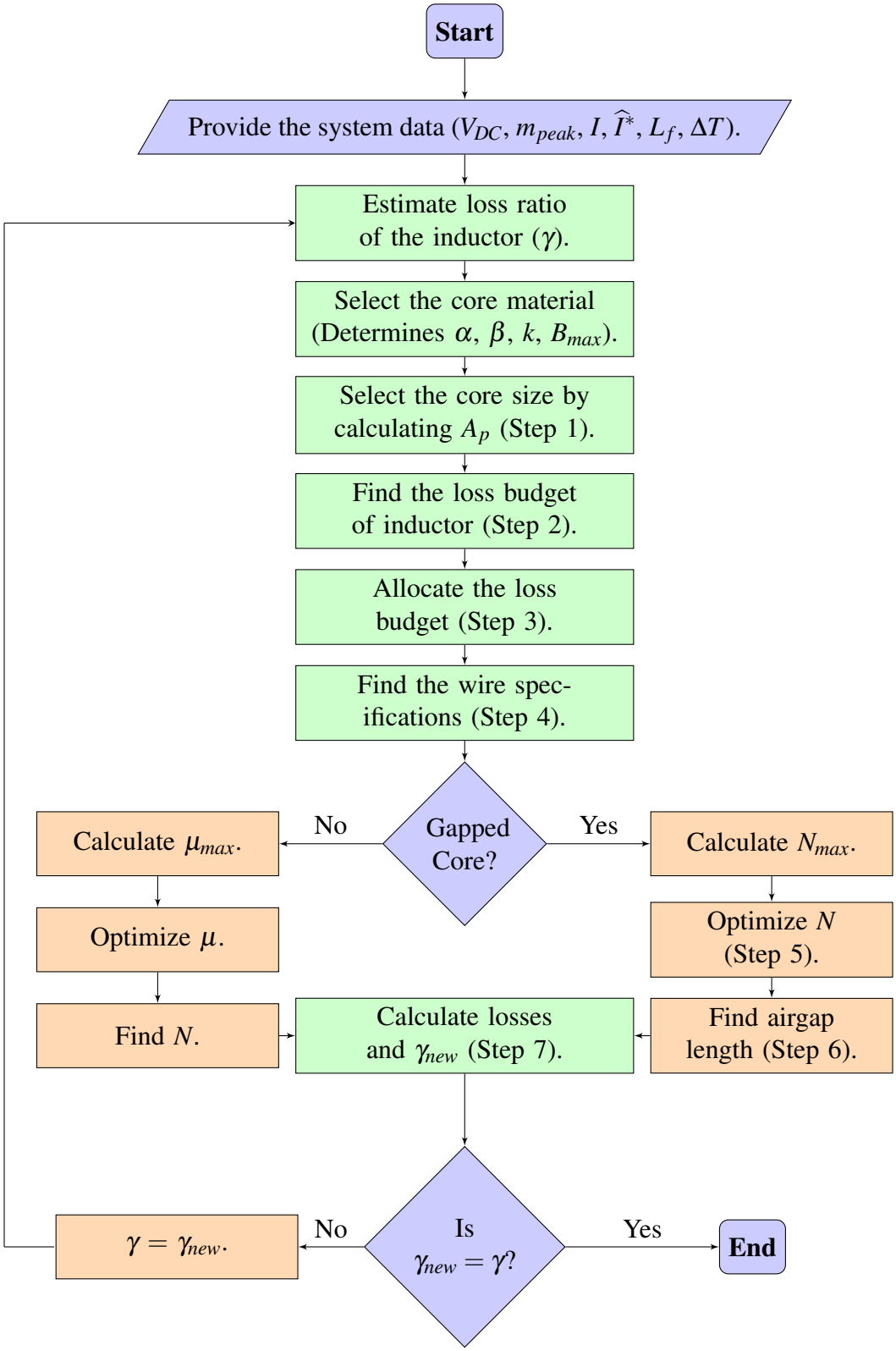
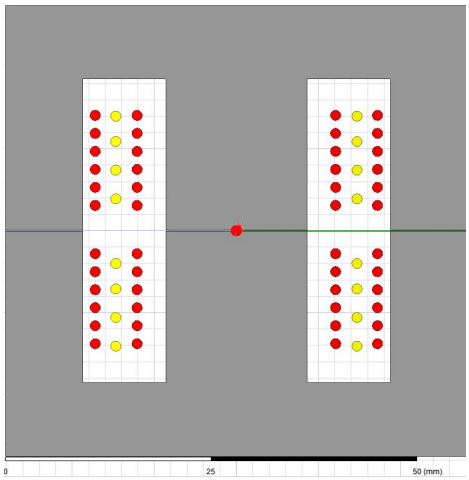
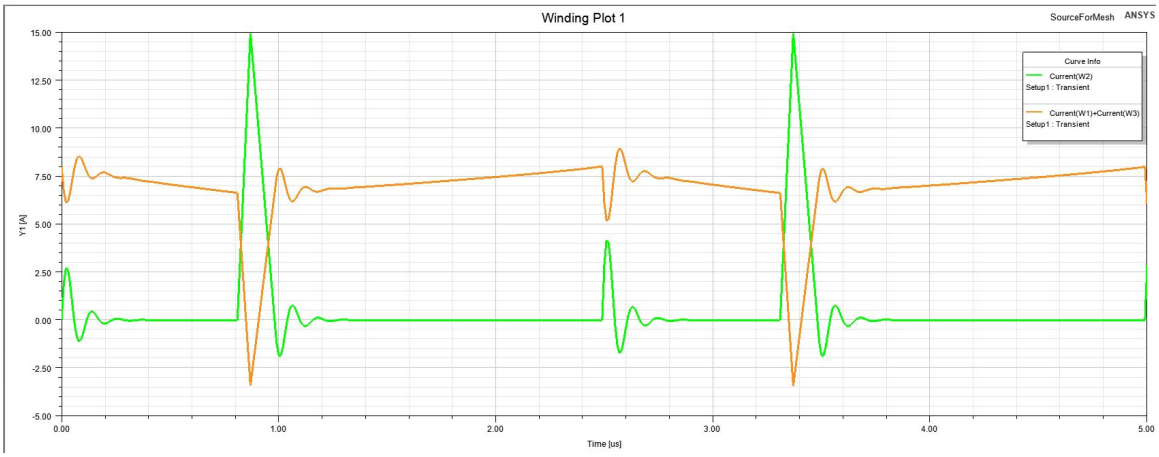


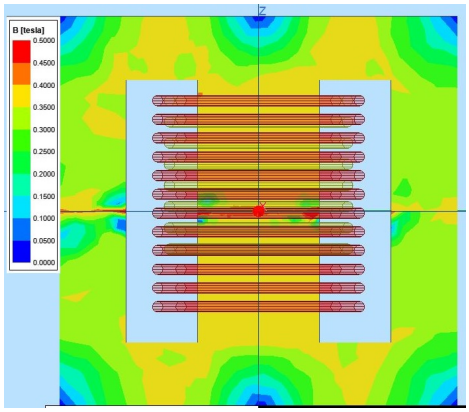
Figure 4.9: Inverter inductor design flow chart.



(a) Cross-section of the designed coupled inductor.

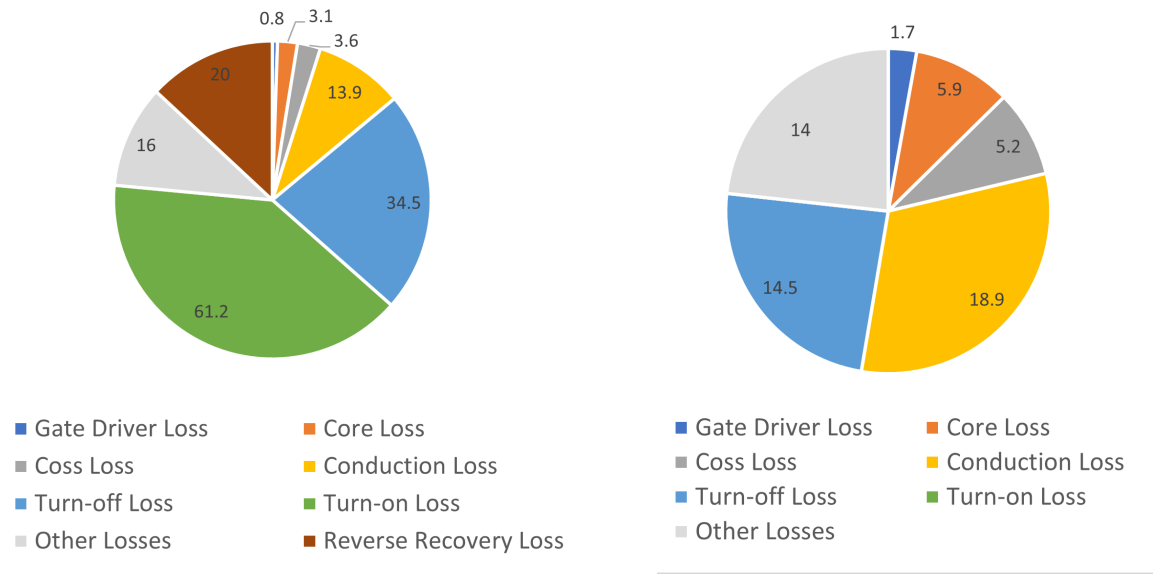


(b) Primary and secondary current in the transient simulation of Ansys.



(c) Flux density in the coupled inductor in worst operation point.

Figure 4.10: Simulation results of the coupled inductor in Ansys software



(a) Hard-switching.

(b) Soft-switching.

Figure 4.11: Loss distribution comparison between the the hard-switching and soft-switching inverters.

the coupled inductor in worst operation point.

With these configurations, values of calculated losses in both hard-switching inverter and soft-switching inverter have been reported as pie charts in Fig. 4.11. These two pie charts show the possible improvement in total losses after eliminating the turn-on cross over losses in soft-switching. It should be noted that these pie charts only show the losses that were calculated in loss analysis section. There are other losses that contribute to the total loss of an inverter like reverse recovery losses that also affect the efficiency of the converter.

4.5.2 Experimental Setup

To verify the performance of the proposed inverter, a prototype with parameters reported in Table 4.2 has been designed and developed. The developed prototype is a 1.5kW and 400kHz full-bridge inverter coupled magnetically to two auxiliary switches by the designed coupled inductor. The inverter controls are implemented on a TMS320F28335 DSP from Texas Instruments. A 400V input DC voltage is provided by a Sorensen SGX500X10C DC

TABLE 4.2
PROTOTYPE SPECIFICATIONS AND COMPONENT VALUES.

Parameter / Component	Value / Part Number
Line Cycle Frequency	60Hz
Output Power	1500 W
Input Voltage (V_{DC})	400 V
Output Voltage (V_o)	240 V
Effective Switching Frequency (f)	400 kHz
Full-bridge Switches ($S_1 \sim S_4$)	SIHB35N60E
Auxiliary Switches (S_{a1}, S_{a2})	SIHB33N60EF
Effective Output Capacitance ($C_{s1} \sim C_{s4}$)	150 pF
Magnetizing Inductance (L_M)	320 μH
Leakage Inductance (L_{aux})	1.8 μH
Turns Ratio (n)	1.5
Filter Capacitor (C_f)	10uF
Modulation Changing Point (m_{ch})	0.3
Auxiliary Switch Pulse Width (Unipolar) ($t_{aux,uni}$)	650ns
Auxiliary Switch Pulse Width (Bipolar) ($t_{aux,bi}$)	400ns
Negative Current Peak ($I_{sw,neg}$)	3A
Deadtime (t_{dt})	80ns
Filter Capacitor (C_f)	10uF

source. Fig. 4.12, shows the implemented prototype picture.

4.5.3 Converter Operation

Fig. 4.13 shows the waveforms of the soft-switching inverter in a line cycle at unity power factor. Output voltage and output current are shown on this figure, and the unipolar and bipolar regions are distinguished on the figure. In bipolar mode, when the absolute value of the modulation index is less than m_{ch}, frequency of the gate signals of the full-bridge switches are twice as the unipolar modulation to get a constant effective switching frequency. Moreover, Fig. 4.14 illustrates the waveforms for an inductive load, which shows that the change between S_{a1} and S_{a2} happens when the current direction changes. Fig. 4.15 is also shown to show the operation of the inverter under a capacitive load.

Figs. 4.16 and 4.17 demonstrate the soft-switching transition in unipolar and bipolar modulation respectively when both V_o and I_o are greater than zero. When I_o is greater

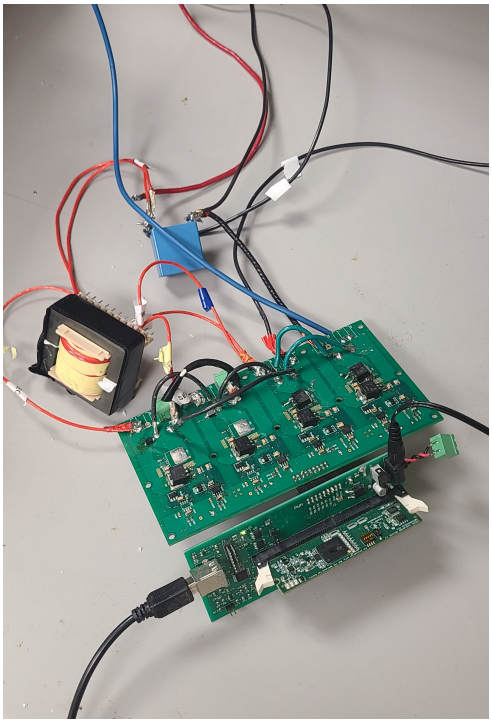


Figure 4.12: Picture of the implemented prototype

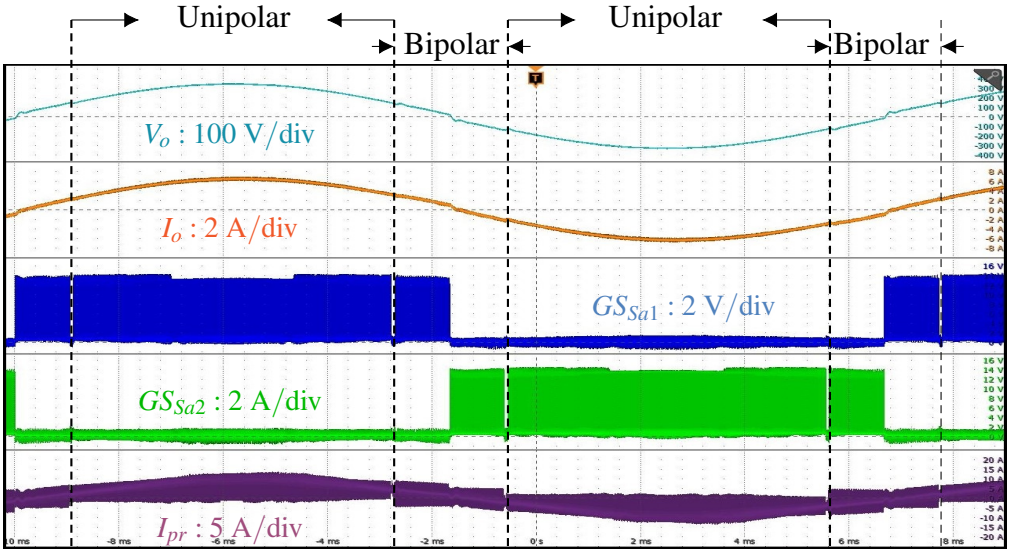


Figure 4.13: Experimental results of a line cycle of operation in unity power factor.

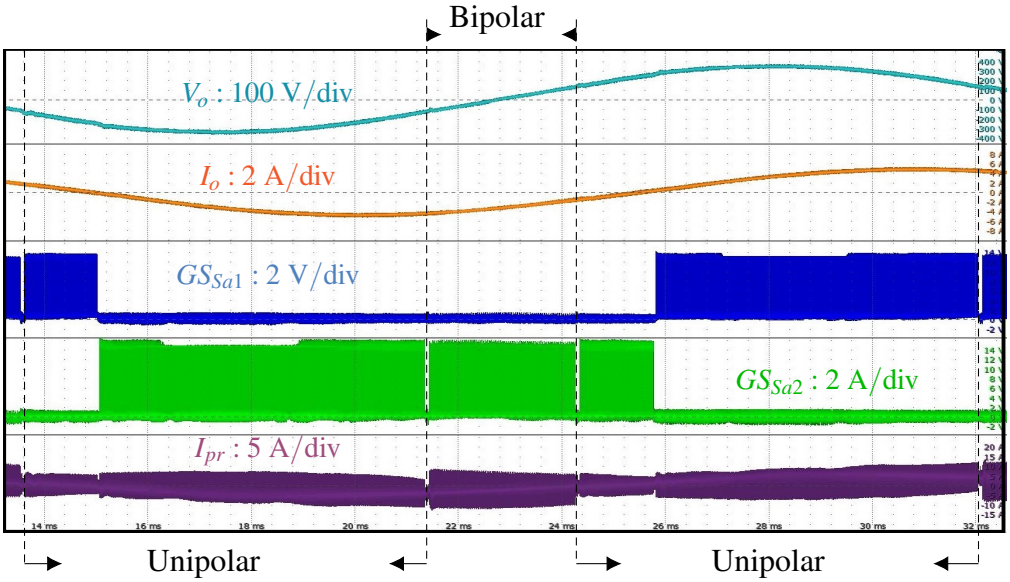


Figure 4.14: A line cycle of operation in 0.6 power factor (inductive).

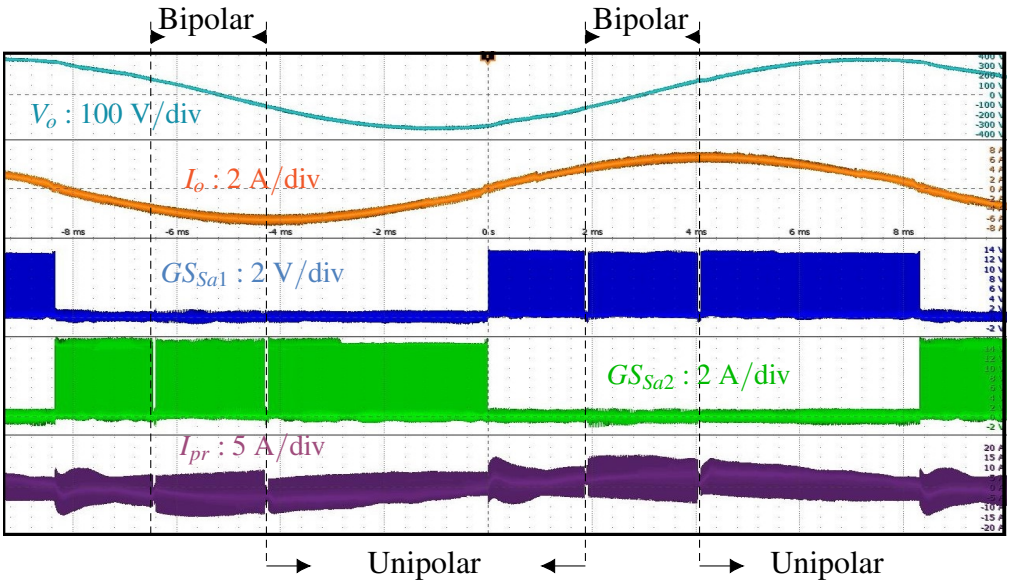


Figure 4.15: A line cycle of operation in 0.4 power factor (capacitive).

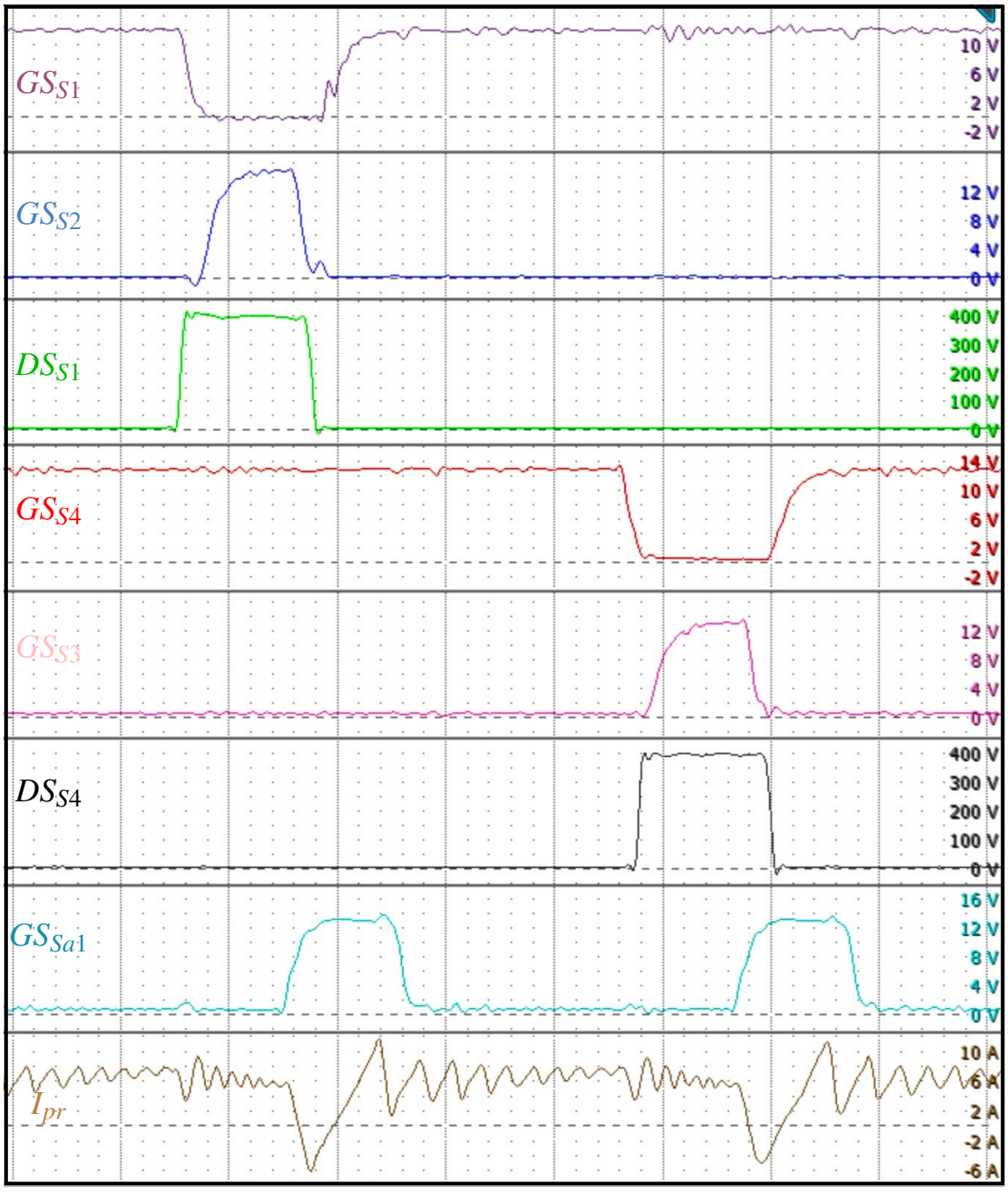


Figure 4.16: ZVS turn-on for S_1 and S_4 when $v_o, i_o > 0$ in unipolar mode (*time* : 600 ns/div).

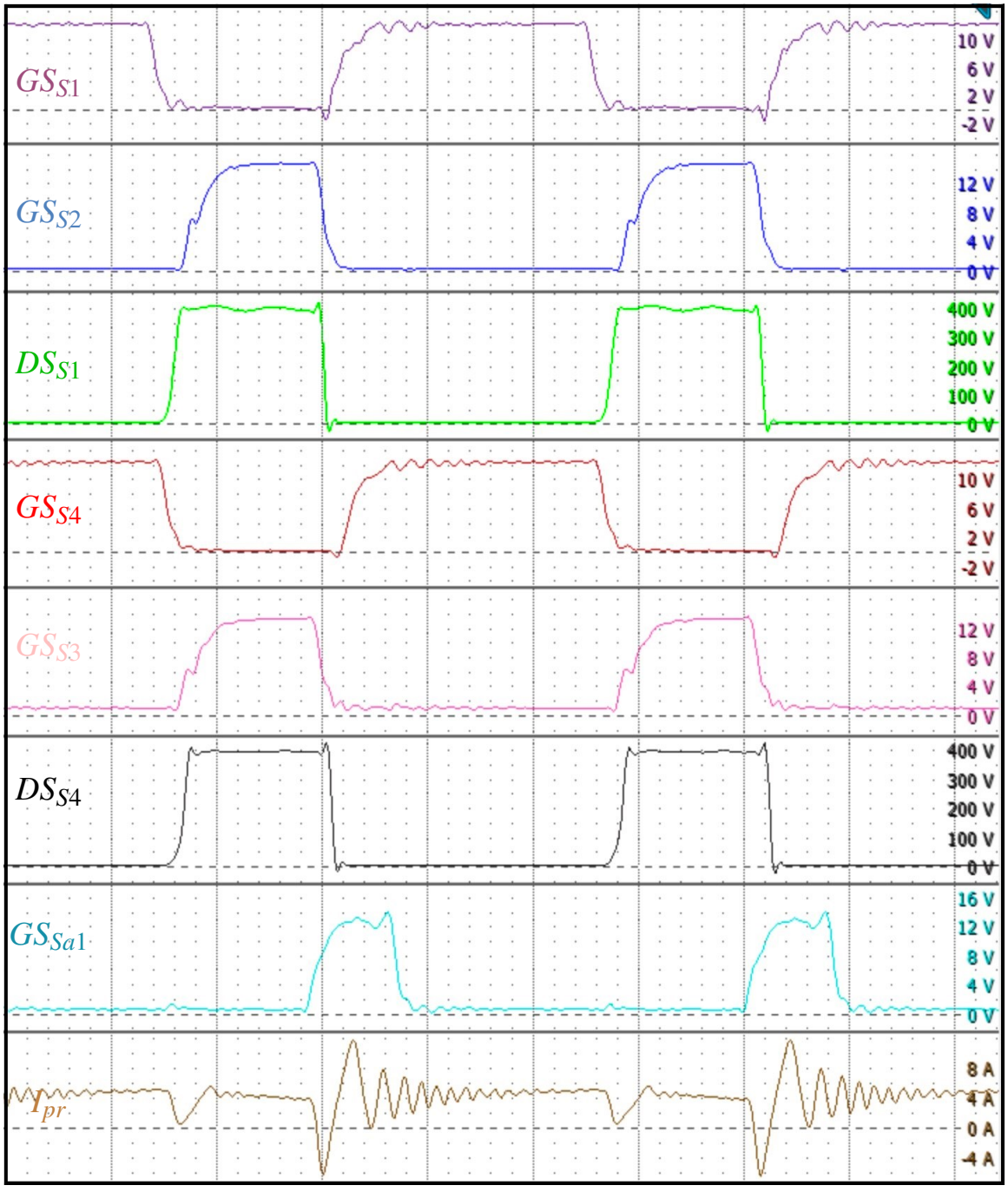


Figure 4.17: ZVS turn-on for S_1 and S_4 when $v_o, i_o > 0$ in bipolar mode ($time$: 600 ns/div).

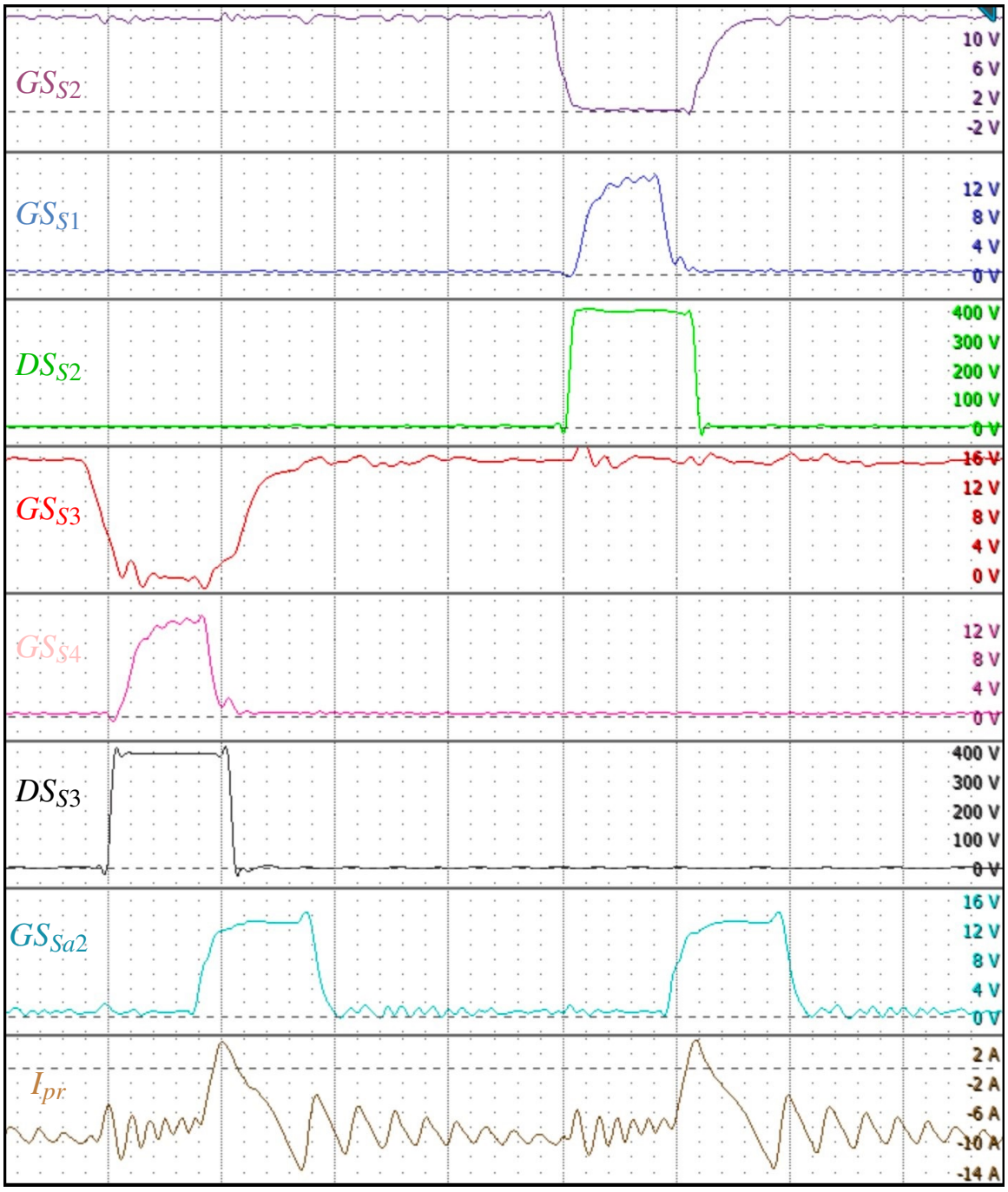


Figure 4.18: ZVS turn-on for S_2 and S_3 when $v_o, i_o < 0$ in unipolar mode (*time* : 600 ns/div).

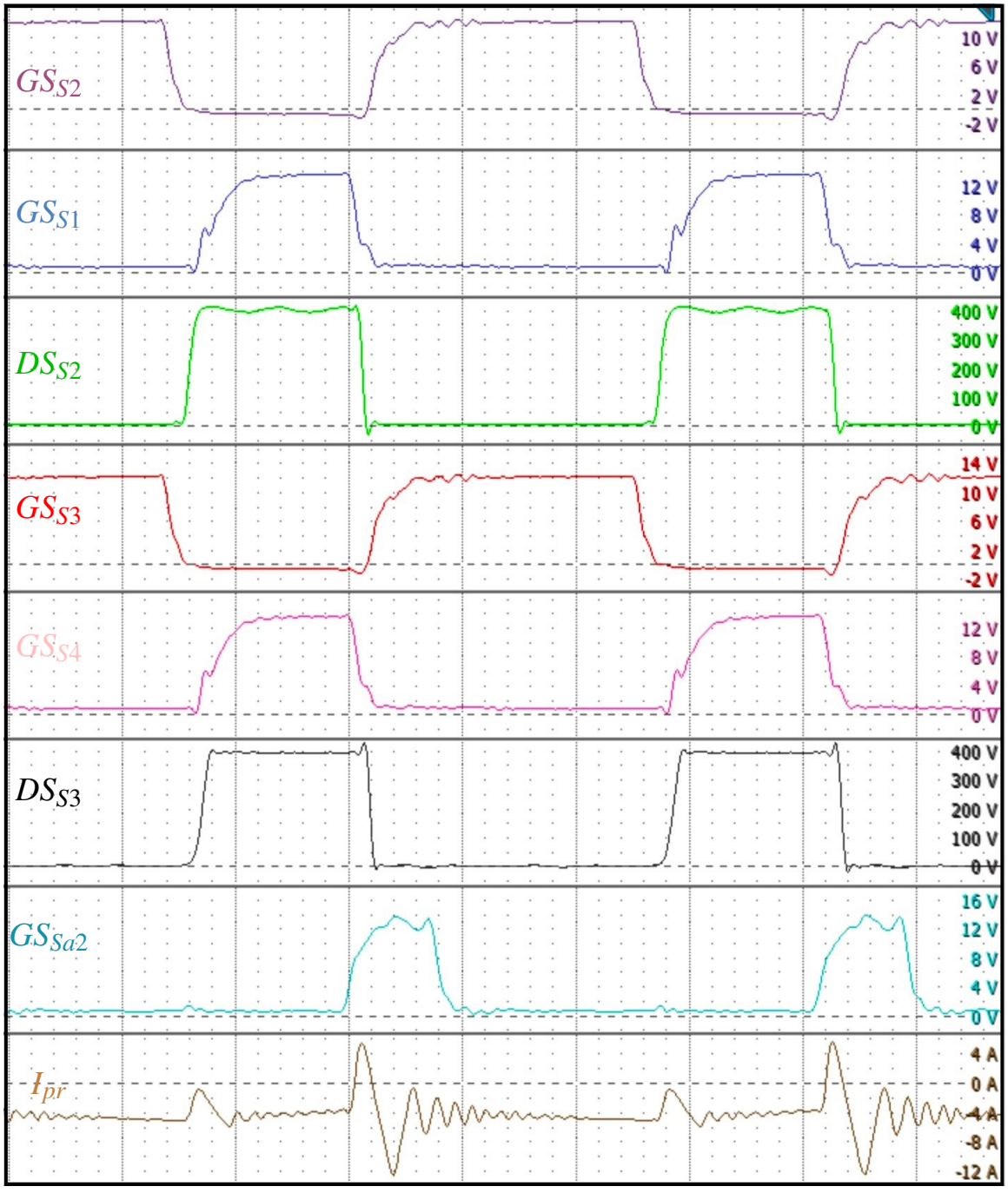


Figure 4.19: ZVS turn-on for S_2 and S_3 when $v_o, i_o < 0$ in bipolar mode ($time$: 600 ns/div).

than zero, switches S_1 and S_4 need soft-switching, and the auxiliary switch responsible for providing this soft-switching is S_{a1}. In Fig 4.16, when S_{a1} is turned on, current passing through the primary of the coupled inductor changes direction, and after S_2 turns off, drain-source voltage of S_1 reaches zero in the deadtime before S_1 turns on, and soft-switching is realized. After that, i_{aux} reaches zero, and S_{a1} turns off with ZCS. The same transition happens for providing soft-switching S_4. For the bipolar mode, same transition happens to provide soft-switching to S_1 and S_4, with the difference being that both switches turn on at the same time but with the higher switching frequency for each switch. On the other hand, when the output current is less than zero, switches S_2 and S_3 need soft-switching and S_{a2} is controlled to provide soft-switching. Figs. 4.18 and 4.19 are the experimental results when V_o is less than zero and I_o is less than zero.

The oscillations existing in the i_{aux} happen as a result of the energy existing the output capacitors of the auxiliary switches. This energy causes ringings between the coupled inductor and the capacitors, which with the internal resistors of the components creates an RLC circuit. These oscillations cause additional losses to the system, which results in a small drop in efficiency that comparing to the benefits of soft-switching method, it can be tolerated. Also, reverse recovery of the switches affects the primary current of the inductor as it can be seen in the figures.

4.5.4 Converter Efficiency

A comparison has been performed between the hard-switching inverter and the soft-switching inverter by comparing the measured efficiencies in different power levels at unity power factor. This comparison can be seen in Fig. 4.20. This figure demonstrates the superior efficiency of the proposed soft-switching method compared to hard-switching inverter when there is a resistive load. In full-load operation at unity power factor, there is a 6.4% increase in the efficiency, which leads to 96.2% efficiency in full-load with soft-switching. This increase in the efficiency also reduces the thermal management requirements in the

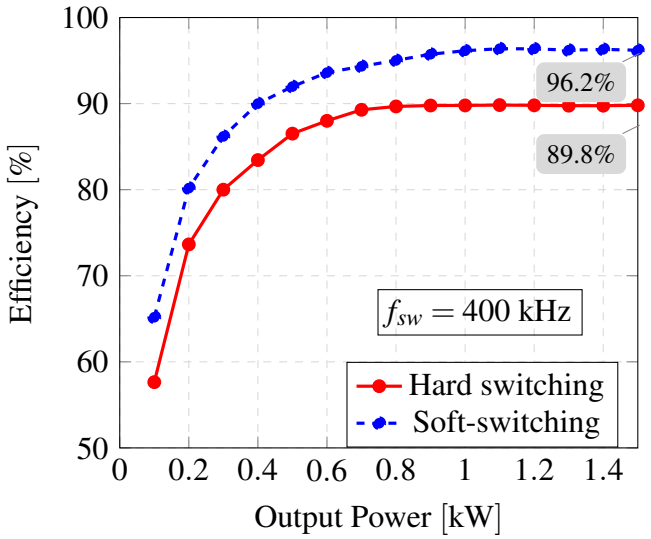


Figure 4.20: Measured efficiency of the converter in unity power factor.

inverter, which helps to reduce the size of the inverter.

Also, to prove the claim on better performance of the inverter in different power factors, a comparison between the hard-switching inverter, proposed soft-switching method, limited soft-switching method with constant timing unipolar modulation and limited soft-switching method with variable timing unipolar modulation has been performed in inductive and capacitive loads. The results are illustrated in Fig. 4.21. This figure shows that as power factor gets further from the unity power factor for a constant apparent power, the proposed soft-switching technique performs much better than the other soft-switching methods, which verifies the claims of the paper. It can be seen in Fig. 4.21 that in unity power factor, all three soft-switching methods are around 96.2%. However, as the output load gets less resistive, the proposed method shows its better performance. When power factor is 0.4 (capacitive), proposed method gives an efficiency of 86.87% in 1kVA apparent power, where, for example, the inverter with variable timing unipolar method shows a 84.3% efficiency.

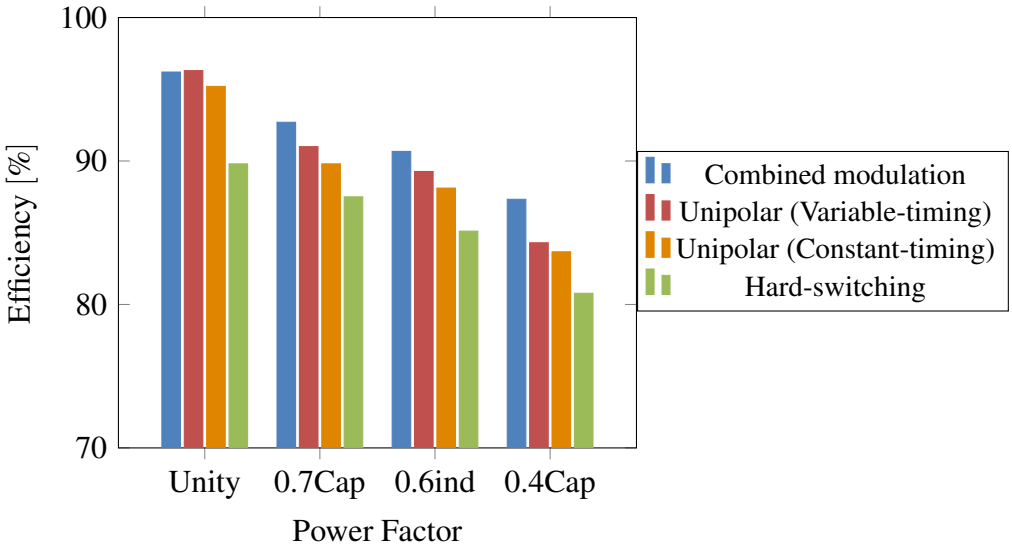


Figure 4.21: Measured efficiency of the converter in different power factors (1kVA apparent power).

4.6 Summary

In this chapter generalized equations for core loss and conduction loss for inverter inductor design are derived. These equations calculate losses of the output filter inductor in a line cycle of operation regardless of the modulation technique. By utilizing these equations in the design procedure of inductors, a design methodology is proposed, where the total losses of the inverter inductor is minimized by selecting optimum number of turns in a gapped inductor. Also, this design methodology avoids the over-design of inverter inductor. This design methodology is used to design the coupled inductor of the inverter.

Also, the results of a 1.5kW, 400kHz prototype converter were reported to justify the theoretical analysis and the proposed modulation technique in chapter 3. For this prototype, Mosfet switches were selected in designing the prototype. A 6.4% increase in the efficiency was achieved compared to the hard-switching inverter in unity PF. Additionally, in non-unity PFs, the proposed modulation technique demonstrated its superiority compared to other modulation methods regarding the efficiency.

Chapter 5

Conclusions, Recommendations, & Future Work

5.1 Conclusions

In this thesis, a soft-switching single-phase inverter has been proposed. Analysis, design and experimental verification of this inverter are also presented. The objective of the proposed soft-switching inverter is to achieve high efficiency in a compact single-phase inverters for a full-range of operation. The main contributions and conclusions of this thesis are summarized below.

(i) Efficiency of the inverter was improved by 6.4% using the proposed auxiliary circuit comprising of only two additional switches and two low side gate drives.

(ii) The range of soft-switching was increased from unity power factor to all the power factors using a novel hybrid modulation technique. This modulation increased the efficiency at the worst case of pf by 7%.

(iii) The losses of the auxiliary circuit was reduced by 1.1% in the unity power factor using a novel variable-timing strategy.

(iv) Generalized equation for the core losses and conduction losses in an inverter inductor was derived regardless of the modulation technique. A design methodology for inverter inductor is proposed based on the loss equations that minimizes the inductor

losses. Based on this design methodology, the coupled inductor of the soft-switching inverter is designed.

(v) A Mosfet-based prototype of the soft-switching inverter with the proposed modulation technique was implemented. The 400kHz switching frequency and 1500W output power prototype show an 6.4% increase in the efficiency in unity power factor. Moreover, tests in non-unity power factors exhibited the full-range soft-switching ability of the converter. In different PFs at least an increase of 6% was reported.

5.2 Future Work

There are a number of directions that this research can be taken to; some of the most promising ones are suggested as follows:

(i) The proposed auxiliary circuit could be investigated for three-phase inverters.

(ii) Soft-switching could be analyzed for transformer-less inverters such as HERIC and H5.

(iii) Inverters with higher switching frequencies could be designed with planar magnetics.

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