Dynamic Electro-Magnetic-Thermal Modeling of MMC-Based DC–DC Converter for Real-Time Simulation of MTDC Grid

Ning Lin, *Student Member, IEEE* and Venkata Dinavahi, *Senior Member, IEEE*

***Abstract*—The model of a modular multilevel converter (MMC) determines the extent of critical circuit information that electromagnetic transient simulations can reveal. In this paper, two MMC models are proposed for efficient real-time hardware-in-the-loop (HIL) emulation on the field-programmable-gate-arrays (FPGA). The nonlinear switch-based model employing the insulated-gate bipolar transistor (IGBT) dynamic curve-fitting model considers factors affecting its transient performance so that device-level behavior such as power loss and junction temperature can be reproduced accurately in the electro-magnetic-thermal simulation of a power converter for its design evaluation. Meanwhile, regarding the MMC submodule as a transmission line stub achieves faster computation speed and enables the formation of a hybrid arm to save FPGA hardware resources. As the large network that the MMC presents is burdensome for real-time execution with a small time-step, circuit simplification based on partitioning and merging is conducted. Hardware implementation of a three-terminal high-voltage direct-current system containing an MMC-based dc–dc converter is carried out and the efficacy of proposed models is validated by comparing HIL emulation results with the offline simulation tool PSCAD/EMTDC.**

***Index Terms*—DC-DC converter, electromagnetic transients, electro-thermal, field programmable gate arrays (FPGA), multi-terminal direct-current (MTDC), modular multilevel converter (MMC), parallel processing, real-time systems, solid-state transformer.**

I. Introduction

THE modular multilevel converter (MMC) has prompted the development of high-voltage direct-current (HVDC) technique for various applications. Operating as a solid-state transformer (SST), the MMC-based DC-DC converter enables the connection of a number of HVDC stations to form a multi-terminal DC (MTDC) system [1], [2]. Meanwhile, it also brings other benefits, such as fault isolation, and power flow control [3]–[5]. The SST is composed of an inverter, a rectifier, and a transformer, which is designed to be physically isolated from the AC grid and can, therefore, operate at a medium frequency to make the SST less bulky [6]. However, such a benefit is accompanied by a corresponding rise of switching frequency and higher switch power loss.

Real-time simulation of HVDC system plays a pivotal role in validating control and protection strategies as well as providing a platform for system performance study [7]–[9]. Simple converter models such as the averaged model can be employed for gaining speed advantage while the accuracy is compromised [10]. Modeling the power converter specifically using the ideal switch model with a fixed low on-state resistance R_{on} and a high off-state resistance R_{off} is sufficient for system-level studies which can show effects such as switch transition and harmonics [11], [12]. However, the preference for high power density by increasing the switching frequency and reducing the converter volume underlines the necessity of acquiring switching power loss for converter design evaluation. Consequently, it is better to include device-level switch models so long as they do not hinder achieving real-time execution. The inability of the ideal model in providing any switching transients precludes it from being employed for electro-magnetic-thermal simulations.

Meanwhile, efforts have been expended in developing control algorithms to reduce IGBT thermal stresses [13], and with switching details, determination of an appropriate algorithm prior to setting up a real converter becomes feasible. Other detailed IGBT models were developed to provide insight into accurate switching waveforms and therefore are frequently referred to for power converter design assessment [14], [15]. Their main drawbacks are low computation efficiency due to the solution of device physics and the tendency of numerical divergence even the converter scale is small. The curve-fitting model is therefore favored in large circuits simulation for electro-thermal analysis where the transient values are programmed in advance or stored in a look-up table (LUT) [16], [17]; yet the versatility of transient waveforms to electromagnetic surroundings needs to be taken into account.

Therefore, a dynamic curve-fitting electro-thermal IGBT model is proposed in this work on the FPGA, so that more device-level information can be revealed in real-time for aforementioned purposes that cannot be achieved by the ideal switch model or detailed models involving a lot device physics. Its static parameters are extracted from the I-V characteristics provided by the manufacturer's datasheet, while the dynamic part is modeled as a function of factors affecting its transient performance.

Manuscript received May 18, 2017; revised August 7, 2017 and October 3, 2017; accepted November 14, 2017. Date of publication November 17, 2017; date of current version April 6, 2018. This work was supported by the Natural Science and Engineering Research Council of Canada (NSERC). Paper no. TPWRD-00679-2017. *(Corresponding author: Ning Lin.)*

The authors are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton AB T6G 2V4, Canada (e-mail: ning3@ualberta.ca; dinavahi@ualberta.ca).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPWRD.2017.2774806

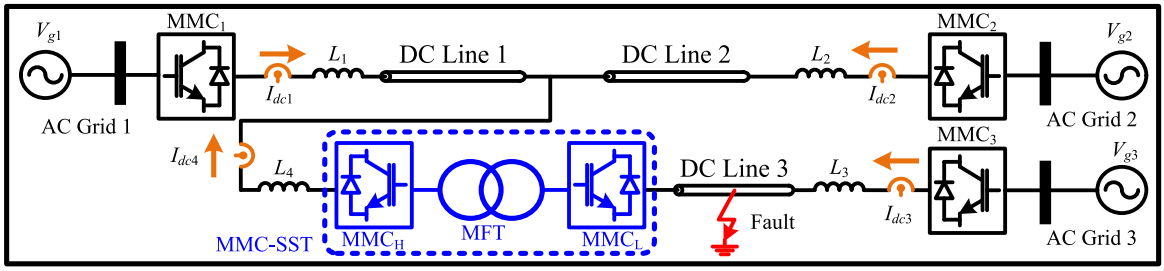

Fig. 1. MMC-based DC-DC converter for MTDC system.

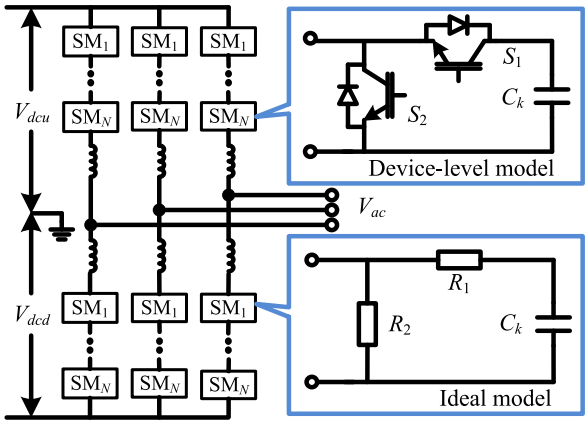

Fig. 2. MMC configuration and its submodule models.

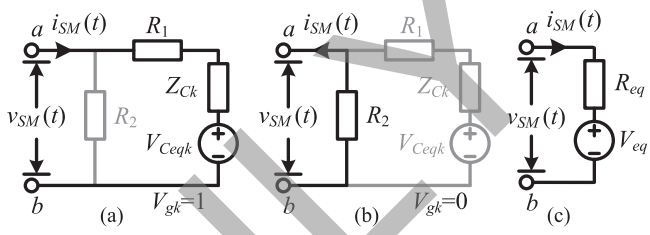

Fig. 3. MMC TLM-stub model: (a) SM on-state/blocked state, (b) SM off-state/blocked state, and (c) general representation.

A hybrid arm is constructed by taking a number of submodules (SMs) as a transmission line modeling (TLM) stub, which, with merits such as lower hardware resource requirement and faster execution speed, is more suitable than the detailed equivalent model (DEM) for HIL emulation.

This paper is organized as follows: Section II introduces two MMC models and the hybrid arm model. In Section III, hardware design of the SST is carried out. Section IV presents HIL emulation results of an MTDC system and their validation. Conclusions are drawn in Section V.

II. Power Converter Modeling

Fig. 1 shows a typical MMC-based front-to-front DC-DC converter integrated into a three-terminal HVDC system, where MMC_1 is the rectifier station, and MMC_2 and MMC_3 are inverter stations. The SST comprises of two MMCs, denoted as MMC_H and MMC_L, and one medium frequency transformer (MFT). The configuration of the MMC is given in Fig. 2, which also shows two half-bridge submodule models: the device-level model employing nonlinear IGBT models, and the ideal model which represents the switches as two-state resistors with distinct off- and on-state resistances.

The model of MMC determines the speed of electromagnetic transient (EMT) simulation. The ideal-switch-based DEM has been proven by EMT tools and is prevalent for achieving faster simulation speed compared with traditional models [18]. It is based on the following equations:

$$R_{eq} = \frac{R_1 R_2 + R_2 Z_{Ck}}{R_1 + R_2 + Z_{Ck}}, \tag{1}$$

$$V_{eq}(t - \Delta t) = \frac{R_2 V_{Ceqk}(t - \Delta t)}{R_1 + R_2 + Z_{Ck}}, \tag{2}$$

where Z_{Ck} and V_{Ceqk} compose the Thévenin equivalent circuit of the submodule capacitor, R_1 and R_2 are resistances of the two complementary switches, and Δt is the simulation time-step. However, it lacks device nonlinearities and is only suitable for system performance preview. On the contrary, nonlinear switch models are highly inefficient for CPU simulation and usually require large amount hardware resource for FPGA implementation due to the iterative nature of the solution. Thus, a hybrid MMC model which features more circuit details and computational efficiency is proposed.

A. MMC TLM-Stub Model (TLM-S)

As shown in Fig. 3(a) and (b), when an arbitrary submodule numbered k is under on-state, the capacitor is being charged through a small resistance, and if the submodule is off, the equivalent circuit is a small resistor. Thus, an on-state resistance is always in the conducting path during operation. The existence of the SM capacitor can be determined by the gate signal of the upper switch, deemed as a binary, i.e., $V_{gk} = 1$ for on-state and $V_{gk} = 0$ for off-state. For the blocked state, simply ordering $V_{gk} = 0$ and $R_2 = R_{off}$ omits the free wheeling diode effect, just as the DEM. To enable correct SM ON/OFF mode of the blocked state, the gate signal is determined by the direction of the arm current i_{SM}: if it flows into the SM through node a, which is defined as the positive direction, then $V_{gk} = 1$; otherwise, $V_{gk} = 0$. This criterion leads to two equivalent circuits similar to Fig. 3(a) and (b). For the former state, the submodule impedance equals to R_{on}+Z_{Ck}, while this value is R_{on} for

the latter. Correspondingly, the capacitor voltage v_{Ck} alternates between $i_{SM} \cdot Z_{Ck} + V_{Ceqk}$ and V_{Ceqk}. Nevertheless, to simulate the high-impedance mode of the blocked state when both diodes are off, v_{SM} and v_C are required to judge whether the upper diode should be turned on. Applying TLM-stub theory [19], the capacitor voltage and its iterative incident pulse v^i_{Ck} can be written as

$$v_{Ck}(t) = V_{gk}(t) \cdot i_{SM}(t) \cdot Z_{Ck} + 2v^i_{Ck}(t), \quad (3)$$

$$v^i_{Ck}(t + \Delta t) = v_{Ck}(t) - v^i_{Ck}(t). \quad (4)$$

The Thévenin equivalent circuit of an SM can be obtained as in Fig. 3(c), where

$$R_{eq}(t) = R_{SM} + V_{gk}(t) \cdot Z_{Ck}, \quad (5)$$

$$V_{eq}(t) = 2V_{gk}(t) \cdot v^i_{Ck}(t). \quad (6)$$

where R_{SM} equals to R_{on} for all states except high-impedance mode when it should be R_{off}.

Then, for an MMC arm containing N submodules, the Thévenin equivalent circuit can be expressed as

$$V_{arm\_eq}(t) = \sum_{k=1}^{N} V_{eqk}(t) = 2\sum_{k=1}^{N}(V_{gk}(t) \cdot v^i_{Ck}(t)), \quad (7)$$

$$R_{arm\_eq} = \sum_{k=1}^{N} R_{eq}(t) = NR_{SM} + Z_{Ck}\sum_{k=1}^{N} V_{gk}(t). \quad (8)$$

B. MMC Nonlinear Switch-Based Model (NSM)

When the operation frequency of MFT increases for a higher power density, the switching frequency should follow, incurring larger IGBT power loss and higher junction temperature. However, MMC models based on the ideal switch are incapable of electro-thermal calculation. Thus, the datasheet-driven dynamic curve-fitting model (DCFM) involving switching transients is proposed.

1) IGBT Dynamic Curve-fitting Model: Piecewise linearizing the IGBT static I-V curves provided by the manufacturer into 6 segments, the collector current in the jth segment can be written as

$$I_C = k_j(T_{vj})V_{CE} - b_j(T_{vj}), \quad (9)$$

where b_j and k_j given in the Appendix are linear functions of junction temperature T_{vj} since data at two different temperatures are available. Taking the IGBT under steady-state as a resistor, its value can then be deduced as

$$r_s = \frac{V_{CE}}{I_C} = \frac{I_C + b_j(T_{vj})}{k_j(T_{vj})I_C}, \quad (10)$$

It should be pointed out that the IGBT off-state accounts for one of the 6 segments. Meanwhile, switching transients must be included as part of the model. In addition to T_{vj}, the rise and fall times generally denoted by $t_{r,f}$ are also affected by factors such as gate resistance R_g, and collector current I_C, each of which, according to device datasheet, can be expressed by a piecewise

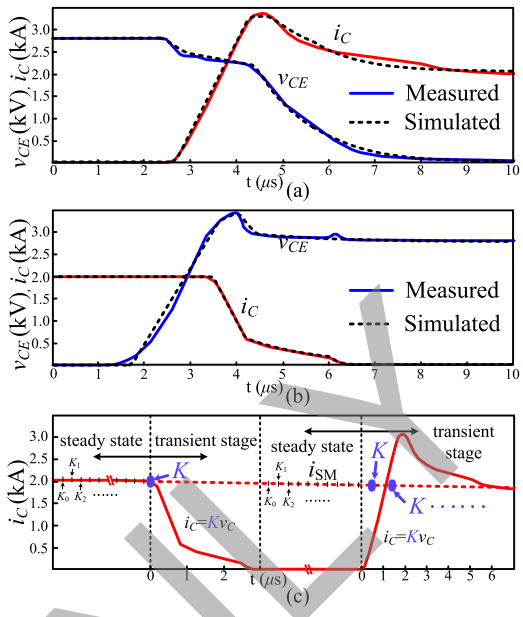

Fig. 4. IGBT transient waveforms from a bridge-structure test circuit: (a) turn-on process, (b) turn-off process, and (c) coefficient K determination.

linear function

$$t_{r,f}(x_i) = A_i x_i + B_i, \quad (11)$$

where x_i represents either T_{vj}, R_g, or I_C, and A_i, B_i are coefficients. However, when two or more factors are combined, the relationship is still nonlinear; therefore, the overall effect can be described by a polynomial function

$$t_{r,f}(x_1, x_2, x_3) = k_0 \cdot \prod_{i=1}^{3}(x_i) + \sum_{i,j=1\to 3}^{i\neq j} k_i x_i x_j + \sum_{i=1}^{3} b_i x_i + b_0, \quad (12)$$

where k_i and b_i are coefficients that are obtained in a way that sets two variables constant and forces the function to be equal to (11) with the remaining variable, i.e.,

$$t_{r,f}(x_i) = t_{r,f}(x_i, x_j, x_k)\,|_{x_j, x_k = C}\ . \quad (13)$$

The values then become available, as listed in the Appendix. Note that the gate driving voltage does not appear in (12) because for specific applications its amplitude is fixed. Nevertheless, it can be added to (12) if the $t_{r,f}$-V_g relationship is provided by the datasheet.

The shape of IGBT transient waveforms is influenced by the test circuit. Thus in Fig. 4(a) and (b), the turn-on and turn-off waveforms of 5SNA 2000K450300 StakPak IGBT module are obtained from a bridge-structure test circuit which provides the same electromagnetic environment to that of an MMC submodule [20], [21] to ensure the applicability of the fitted model. As a result, the diode reverse recovery reflected by current surge in Fig. 4(a) is automatically included in the IGBT transient waveforms. Fig. 5(a) and (b) is the transient model for IGBT in which the output of a per-unit circuit is amplified by

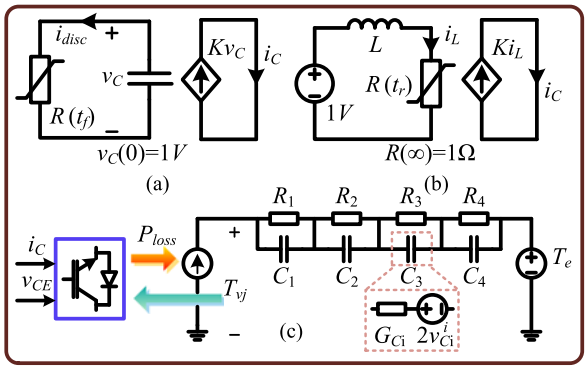

Fig. 5. Dynamic IGBT electro-thermal model: (a) VCCS for descending curves, (b) CCCS for rising curves, and (c) electro-thermal network.

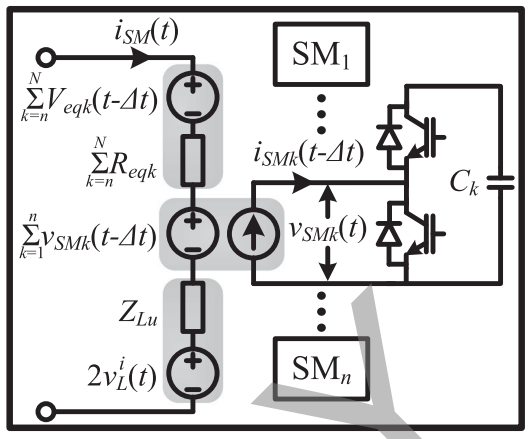

Fig. 6. MMC hybrid arm model with V-I couplings.

K times. The voltage-controlled current source (VCCS) and current-controlled current source (CCCS) are able to reproduce simulated curves that virtually fit with those measured experimentally, as shown in Fig. 4. The descending curves can be modeled as the capacitor voltage of a discharging RC circuit with a time constant τ. Take the collector current for instance, the fall time t_f, defined as the current dropping from 90% to 10% of the initial value along an extrapolated straight line drawn between the time instants when the current is 90% and 60% of its initial value [20], is located on a virtually straight line. To achieve that, the initial capacitor discharging rate i_{disc} should be controlled at

$$i_{disc} = C\frac{dv_C}{dt} = C\frac{(90\% - 10\%)v_C(0)}{t_f}. \tag{14}$$

After v_C drops to about 33% of its initial value, the curvy tail current emerges. Then, the control object shifts to the resistance while the capacitance is kept constant, and in the jth nonlinear segment of the curve, it is

$$i_{Cj} = K \cdot v_{Cj}(0)e^{-\frac{t}{\tau_j}}, \tag{15}$$

where $v_{Cj}(0)$ denotes the initial capacitor voltage of that segment, and coefficient K is the *last steady-state* value for turn-off current, while for turn-on current K is the instantaneous arm current, as shown in Fig. 4(c).

Similarly, the rising curves are realized by an RL circuit. The overshoot is achieved by charging purely the inductor while introducing a time-varying resistor forces the curve to decline with a certain slope. The rise time, defined as the time between instants when the collector current rises from 10% to 90% of the final value, decides the inductance. Since the segment where t_r locates is a straight line, the inductance can be derived as:

$$L = U \cdot \frac{dt}{di} = \frac{t_r(T_{vj}, R_g, I_c) \times 1(V)}{(90\% - 10\%)(A)}. \tag{16}$$

The heat is diffused through an electro-thermal network shown in Fig. 5(c), where the transient thermal impedance equation in the datasheet is modeled as a combination of resistors and capacitors [22]. The IGBT power loss P_{loss} acts as the input current source whose terminal voltage is deemed as the junction temperature, i.e.,

$$T_{vj}(t) = \left(\sum_{i=1}^{4} \frac{P_{loss}(t) + 2v^i_{Ci}(t)G_{Ci}}{G_{Ci} + R_i^{-1}}\right) + T_e, \tag{17}$$

where $T_e = 25°C$ is the ambient temperature, $G_{Ci} = \Delta t/2C_i$, and

$$v^i_{Ci}(t) = \frac{P_{loss}(t) + 2v^i_{Ci}(t - \Delta t)G_{Ci}}{G_{Ci} + R_i^{-1}} - v^i_{Ci}(t - \Delta t) \tag{18}$$

constitutes the EMT model of a capacitor. Then, T_{vj} is fed back to the IGBT model to update its parameters.

2) MMC Hybrid Arm Model: The introduction of nonlinear switch model leads to a more complicated MMC network, for which the aforementioned submodule merging approach is not instantly feasible. Voltage-current source coupling enables submodules to be split from MMC arms, as shown in Fig. 6, where voltage sources are placed on the linear arm side. The hybrid arm can contain a flexible number of split submodules while the rest adopt TLM-S for efficient computation and less hardware utilization when deployed to FPGA. Then, the arm's Thévenin equivalent circuit is

$$\begin{aligned} v_{arm}(t) = {} & i_{SM}(t) \cdot Z_{Lu,d} + 2v^i_L(t) + \sum_{k=1}^{n} v_{SMk}(t - \Delta t) \\ & + i_{SM}(t) \cdot \sum_{k=n+1}^{N} R_{eqk}(t) + \sum_{k=n+1}^{N} V_{eqk}(t - \Delta t), \end{aligned} \tag{19}$$

where $Z_{Lu,d}$ and $2v^i_L$ is the TLM stub model for an arm inductor. v_{SMk} is the voltage coupling of kth submodule, and the number $n \in [1, N\text{-}1]$.

On the nonlinear submodule side, the computation approach relies on switch state. Under steady-state, both switches of the SM are taken as resistors, then

$$\begin{bmatrix} v_{Ck}(t) \\ v_{SMk}(t) \end{bmatrix} = \begin{bmatrix} Z_{Ck}^{-1} + R_1^{-1} & -R_1^{-1} \\ -R_1^{-1} & R_1^{-1} + R_2^{-1} \end{bmatrix} \cdot \begin{bmatrix} v^i_{Ck}(t) \cdot Z_{Ck}^{-1} \\ i_{SMk}(t - \Delta t) \end{bmatrix}, \tag{20}$$

where $v_{SMk}(t)$ is the voltage to be sent to the opposite side. The SM blocked state is a special steady-state, where R_1 and R_2 are determined by the arm current: a positive i_{SM} indicates that the upper diode is on and R_1 is small, otherwise R_2 has a small resistance. During transient state, the IGBT is taken as a controlled current source, and the current in the complementary switch, defined as flowing from collector to emitter is given as:

$$i_C^{'}(t) = i_C(t) \pm i_{SM}(t - \Delta t). \tag{21}$$

Lastly, knowing the branch currents enables the calculation of circuit other variables, such as $v_{Ck}(t)$ and $v_{SMk}(t)$.

The partitioning method induces a unit delay to both sides. At the instant t-Δt, $i_{SM}(t$-$\Delta t)$ is obtained by solving the matrix equation corresponding to the left circuit, and it is sent to the SM. Then, instant t begins. On the SM side, based on $i_{SM}(t$-$\Delta t)$ it just received, $v_{SMk}(t)$ can be derived. Thus, v_{SMk} is one time-step ahead of i_{SM} on the SM side, while the reverse is the case for the MMC arm. Nevertheless, the fact that the circuit computation frequency is much higher than that of the arm current means i_{SM} can be deemed as a constant current source in two neighboring time-steps and its impact on simulation accuracy is negligible.

C. Three-Phase Saturable Transformer Model

The matrix equation [23] for a three-phase transformer is given as:

$$\mathbf{v} = \mathbf{R}\mathbf{i} + \mathbf{L} \cdot \frac{d\mathbf{i}}{dt}, \tag{22}$$

where $\mathbf{R}$, $\mathbf{L}$ are the matrices of winding resistances and inductance, respectively. The discretized form for EMT computation after using Trapezoidal Rule is

$$\mathbf{i}(t) = \mathbf{G}\mathbf{v}(t) + \mathbf{I}_{his}(t - \Delta t), \tag{23}$$

where the iterative history current takes the form of

$$\mathbf{I}_{his}(t) = 2(\mathbf{G} - \mathbf{GRG})\mathbf{v}(t) + (\mathbf{I} - 2\mathbf{GR})\mathbf{I}_{his}(t - \Delta t), \tag{24}$$

$$\mathbf{G} = \left[\mathbf{I} + \frac{\Delta t}{2}\mathbf{L}^{-1}\mathbf{R}\right]^{-1} \frac{\Delta t}{2}\mathbf{L}^{-1}. \tag{25}$$

The nonlinearity caused by saturation is superimposed on the nodal voltage vector solved from the linear network,

$$\mathbf{v}_F = \mathbf{v}_0 - \mathbf{R}_{Thev}\mathbf{i}_{comp}, \tag{26}$$

where $\mathbf{v}_0$ and $\mathbf{v}_F$ are linear and final nodal voltage vectors, $\mathbf{R}_{Thev}$ is the transformer's Thévenin equivalent resistance matrix, and $\mathbf{i}_{comp}$, the compensation current injected into the linear network, is obtained from the saturation curve by Newton-Raphson iteration [24].

D. SST Electromagnetic Transient Model

Fig. 7 is the basic three-phase SST circuit configuration for electromagnetic transient simulation. In each phase, the upper and lower arms of an MMC are connected to a common MFT terminal, and the Norton equivalent circuit is adopted since (23) is based on nodal voltage. The four branches on both sides have the same form of admittance and current contribution. Taking the upper arm for instance, its conductance and current contribution can be computed as:

$$G_{H1/L1} = \left(Z_{Lu} + \sum_{k=n+1}^{N} R_{eq}(t)\right)^{-1}, \tag{27}$$

$$J_{H1/L1} = G_{H1/L1}\left(V_{dcu} - 2v_L^i - \sum_{k=1}^{n} v_{SMk} - \sum_{k=n+1}^{N} V_{eqk}\right), \tag{28}$$

where the DC voltage V_{dcu} corresponds to the upper arm, as shown in Fig. 2. These elements are then combined with inherent elements of the MFT so that the nodal voltage equation of the circuit in Fig. 7 can be solved.

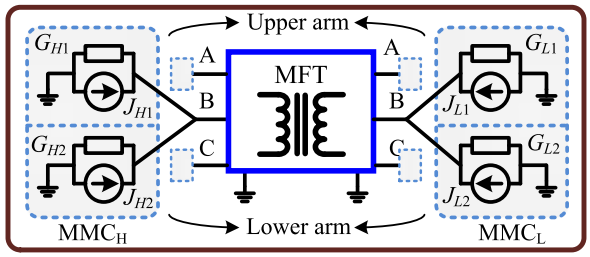

Fig. 7. Three-phase SST electromagnetic transient model.

TABLE I
MMC MODEL SIMULATION SPEED COMPARISON

MMC-	5-s simulation duration			Latency	
Level	DEM	TLM-S	Speedup	DEM	TLM-S
5-L	7.8 s	6.8 s	1.15	76 T_{clk}	64 T_{clk}
11-L	9.2 s	7.7 s	1.19	92 T_{clk}	80 T_{clk}
51-L	17.8 s	13.6 s	1.31	108 T_{clk}	96 T_{clk}
101-L	28.8 s	21.1 s	1.36	116 T_{clk}	104 T_{clk}
501-L	115.0 s	80.1 s	1.44	132 T_{clk}	120 T_{clk}
1001-L	222.0 s	153.4 s	1.45	140 T_{clk}	128 T_{clk}

III. DC–DC CONVERTER HIL EMULATION

The proposed two MMC models are implemented on the Xilinx Virtex-7 VC707 XC7VX485T FPGA platform. As demonstrated in Table I, the TLM-S enables faster simulation by CPU and smaller hardware latency on FPGA, making it more suitable for real-time simulation, particularly when a small time-step is required. For instance, DEM is nearly 30% slower than the proposed TLM-S in simulating a 51-level MMC using a 20-μs time-step when it is run by 64-bit Windows 7 Enterprise SP1 operating system on the 3.40 GHz Intel Core$^{\text{TM}}$i7 CPU and 8.00 GB RAM, while the accuracy of the two models is the same. Moreover, the resource utilization of DEM is much higher than TLM-S, for example, Xilinx Vivado HLS estimates that for an 11-level MMC, one DEM controller takes around 14% of LUT while it is only 4% for proposed TLM-S.

Hardware design of MMC_H is taken as an example because the topology of SST is symmetrical. Vivado HLS which enables

TABLE II
MMC HARDWARE DESIGN SPECIFICATIONS

Module Latency			
Module	Description	Latency	Time-step
NSM	nonlinear SM	35 T_{clk}	500ns
MMCP	1-phase MMC	95 T_{clk}	15 μs
MFT	transformer	205 T_{clk}	15 μs
DQT	abc-dq	78 T_{clk}	15 μs
OLC	outer loop control	110 T_{clk}	15 μs
PLL	phase reference	8 T_{clk}	15 μs
PSC	phase-shift control	1429 T_{clk}	15 μs
THM	thermal network	61 T_{clk}	15 μs

Hardware resource utilization			
Resources	55L-TLM-S (1p)	NSM (1SM)	Total
LUT	45685 (15.05%)	5848 (1.93%)	303600
$LUTRAM$	47 (0.04%)	49 (0.04%)	130800
FF	38749 (6.38%)	3140 (0.52%)	607200
$BRAM$	31.50 (3.06%)	0 (0%)	1030
DSP	426 (15.21%)	32 (1.14%)	2800
$BUFG$	4 (12.5%)	4 (12.5%)	32

C/C++ functions to be synthesized into hardware modules was employed to shorten the design cycle. Signals with the same attribute are grouped in an array, rather than being taken individually, for a significant reduction in hardware resource utilization when C synthesis is conducted. The drawback is that the latency will increase slightly along with the array size. Therefore, such hardware design strategy is mainly adopted in controllers which have a good latency tolerance. The unroll directive provided by the design tool is also chosen for achieving parallelism of signals in an array.

Table II gives hardware design specifics. Around 15% of LUT and DSP are required by the 1-phase 55-level MMC and its controller. With a FPGA clock frequency of 100 MHz, the time-step for PSC should be no less than 13.75 μs according to its 1375 T_{clk} latency, where $T_{clk} = 10$ ns, while it is flexible for the remaining modules other than NSM, so that all of them can be set at 15 μs. The parallelism of the 55-level MMC is purposely weakened to save hardware resources and consequently the latency of TLM-S increases to 95 T_{clk}. Meanwhile, the time step for NSM is 500 ns to ensure the accuracy of switching transients.

Fig. 8 illustrates the general hardware structure of MMC_H, where the input and output ports of MMC and its controller - grouped as one component - are specifically shown, while other functional blocks in the top-level are represented by their simplified forms. As can be seen, manipulating gate-level logics is avoided with Vivado HLS, and only the input and output ports of a component are required during hardware design. Since the hybrid arm is used in the simulation, one MMC contains mainly four blocks, i.e., phase-shift control (PSC) [25], MMC linear part (MMC0), MMC nonlinear submodule (NSM) and the thermal network (THM). Among them, the THM is independent of other modules to shorten the hardware latency: the NSM sends v_{CE} and i_C to THM whenever it completes calculation, and the newest values take effect when the THM starts a new computation cycle; similarly, the THM calculates $t_{r,f}$ and sends them immediately to the NSM. Meanwhile, the 6 arms of an MMC are calculated concurrently, and the outputs G and J are sent to the MFT module where the nodal voltages are sought.

Connecting these modules either by wire or through D flip-flops is achieved by VHDL in Vivado, where the top-level finite state machine defining the operation sequence in Fig. 9 is realized. Once hardware emulation starts, two independent loops run simultaneously. Loop 1 contains solely NSM and repeats every $\Delta t_1 = 500$ ns, while all remaining modules constitute Loop 2 that has a period of $\Delta t_2 = 15$ μs. Thus, this multiple time-stepping scheme avoids compromising switching transients by other hardware modules that must have a large time-step. The carrier waveforms are stored in ROM so that MMC phase-shift control can operate properly. Table II shows that for each loop, the time-step is larger than the maximum latency, so two timers are set: once an exact time-step runs out, a new calculation cycle will begin.

Fig. 10 shows the outer-loop controllers of the SST. MMC_L regulates active and reactive power, while its counterpart is in charge of the MFT AC voltage on the primary side. The control scheme is carried out in d-q frame and is largely the same to other voltage-source converters, except an additional MMC inner loop employing phase-shift control is adopted. The angle θ for Inverse Park's Transformation is the reference which determines the MFT operation frequency. Internal variables with superscripts H and L correspond to the primary and secondary sides of the transformer, respectively.

IV. REAL-TIME HIL EMULATION RESULTS

A. Device-Level Behavior

In the MMC, the static SM current is alternating at a frequency decided by θ and is taken as an example to show its influence on IGBT's turn-on and turn-off times, as shown in Fig. 11(a) and (b). When I_C climbs from 500 A to 3500 A, the turn-on time increases steadily, while the turn-off time first declines from 1300 ns to around 800 ns, and then rises again. Comparison with corresponding values provided by the datasheet proves the accuracy of proposed IGBT transient model, and with more linear segments to approximate the nonlinear $t_{r,f}$-I_C curves, the accuracy of the results can be further improved. Fig. 11(c) gives corresponding energy consumption, both turn-on and turn-off energies E_{on}/E_{off} closely follow datasheet values when identical test conditions are set. A high degree of agreement between simulation and experimental data indicates that the proposed IGBT dynamic curve-fitting model qualifies for MMC simulation to give design guidance. In Fig. 12 and thereafter, simulations are conducted based on the MTDC system in Fig. 1, whose parameters are listed in the Appendix. Stipulating that the switching frequency is kept 10 times higher than that of MFT to ensure MMC output quality, MMC_H lower IGBT operation status in delivering 200 MW to MMC_3 is shown in Fig. 12. The power loss waveforms at two switching frequencies are given in Fig. 12(a), which indicates that with a higher density of power pulses, the latter has a more significant impact on junction temperature. Fig. 12(b) verifies this viewpoint: with switching frequencies of 600 Hz, 1800 Hz and 3000 Hz, the junction temperatures

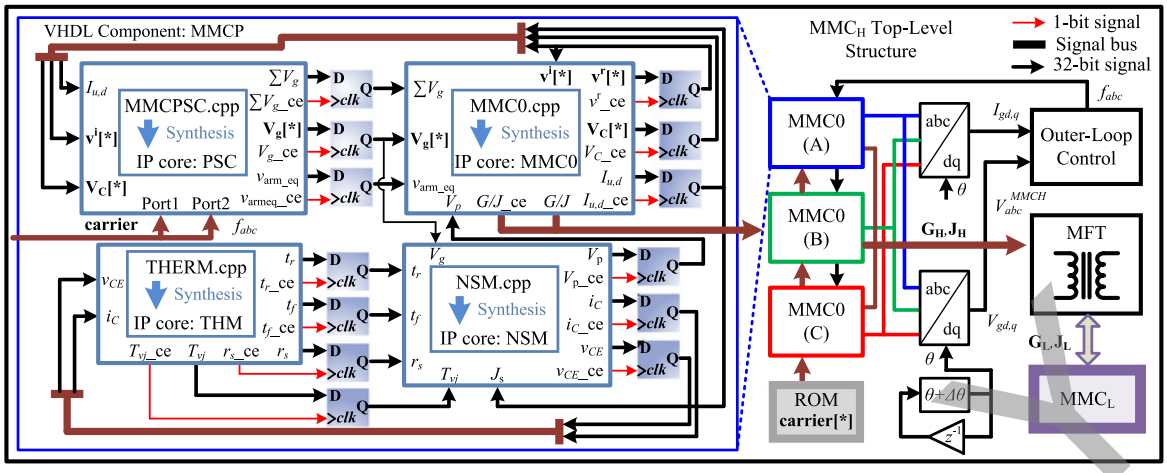

Fig. 8. Top-level hardware structure of MMC_H.

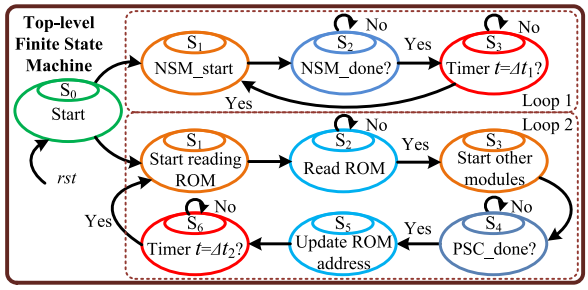

Fig. 9. SST top-level finite state machine.

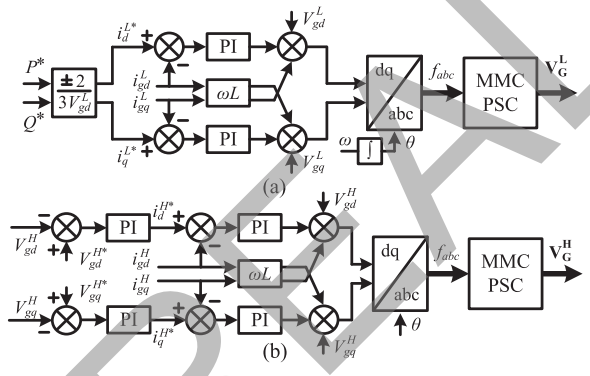

Fig. 10. SST control scheme: (a) MMC_L controller, and (b) MMC_H controller.

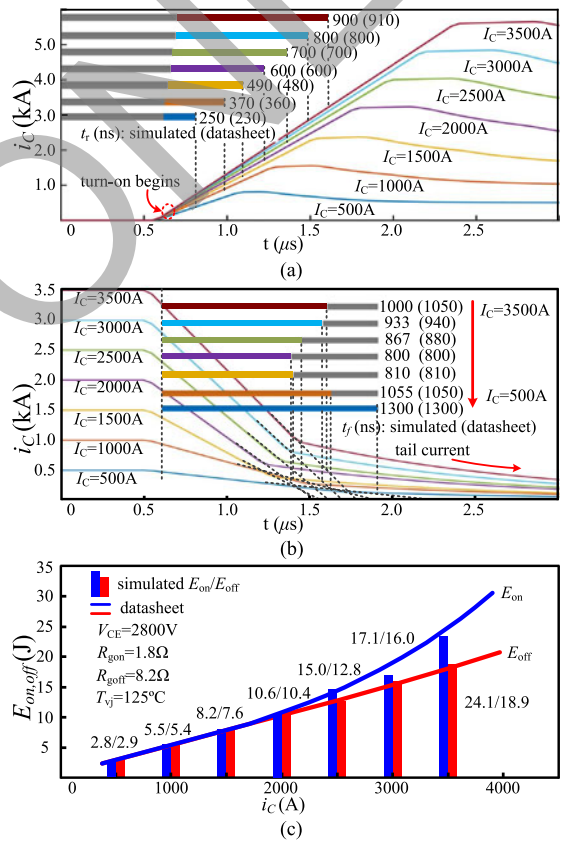

Fig. 11. IGBT transient tests under different collector current at $T_{vj} = 125°C$: (a) turn-on process, (b) turn-off process, and (c) turn-on and turn-off energy.

center around 45°C, 75°C, and 103°C, respectively. The fluctuations in the temperature are caused by the alternating turn-on and turn-off processes, and consequently the higher the switching frequency, the denser the ripples appear. With respect to safe operation, it can be inferred that measures such as using external cooling apparatus and increasing the MMC level are required when $f_{sw} = 3000$ Hz, while natural cooling is sufficient for steady-state operation with $f_{sw} = 600$ Hz. For further validation, the transferred power is reduced to 20 MW, and SaberRD which is always referred to for device-level information is used to simulate a 5-level MMC considering numerical divergence will occur if the number of level is higher. The results inFig. 12(c) demonstrate that the junction temperatures from DCFM and the simulation tool's own IGBT model are largely the same, meaning that the proposed DCFM is as accurate as commercial simulation tools. Fig. 12(d) gives the relation between MMC voltage levels and maximum IGBT junction temperatures, which demonstrates that by increasing the MMC voltage level, a dramatic junction temperature drop can be achieved if $f_{sw} = 3000$ Hz, while the improvement is not significant when f_{sw} is 600 Hz.

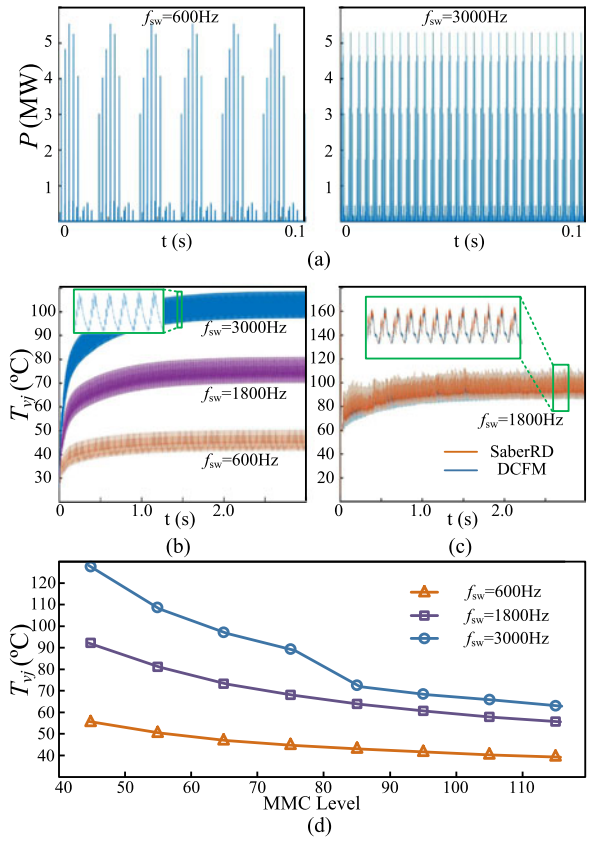

Fig. 12. MMC_H lower IGBT operation status: (a) power loss waveforms for 55L-MMC, (b) junction temperature waveforms for 55L-MMC, (c) 5L-MMC SaberRD validation, and (d) relation between T_{vj} and MMC level.

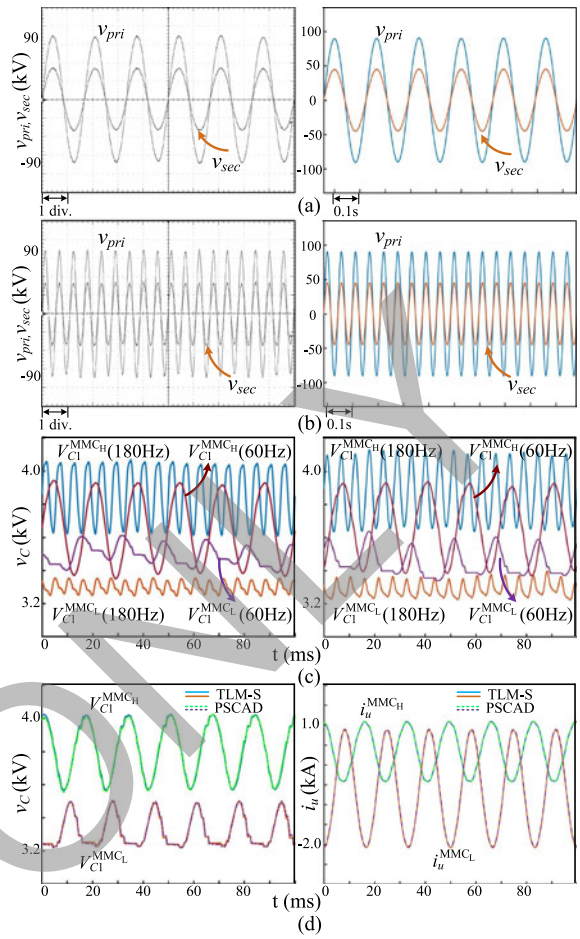

Fig. 13. SST converter-level results (left: HIL emulation; right: PSCAD/EMTDC): (a), (b) MFT primary and secondary voltages at 60 Hz and 180 Hz, (c) SM DC voltage ripples, and (d) ideal MMC models comparison. Oscilloscope horizontal axes setting: 10 ms/div.

B. Converter-Level Performance

The MMC_H control target V_{gd}^{H*} is 90 kV, and the MFT frequency for Fig. 13(a) and (b) are set to be 60 Hz and 180 Hz, respectively. The real-time results from the oscilloscope show that the MFT primary voltages v_{pri} are exactly the control objects. Consequently, on the secondary side, the value is halved to about 45 kV. The SM capacitor voltages are also given in Fig. 13(c), which indicates increasing the MFT frequency leads to smaller sizes of transformers as well as arm inductors and capacitors. Under 60 Hz, SM capacitor voltage ripples for both MMC_H and MMC_L are still larger than those under 180 Hz even though its SM capacitance and arm inductance are 2 to 4 times larger, as shown in the Appendix. As expected, the introduction of more accurate DCFM causes some trivial differences with respect to PSCAD/EMTDC results; however, the average values and variations of these signals are similar. In Fig. 13(d), the arm currents and SM DC voltages are compared between TLM-S and PSCAD/EMTDC, it can be seen that these two types of ideal MMC models fit well.

C. System Tests

Some tests demonstrating the function of SST are carried out as a further validation of proposed MMC models. In Fig. 14, power reversal is conducted, and all power flowing to DC yard is defined as positive. Initially, the power delivered to Station-2 and Station-3 are 300 MW and 100 MW, respectively, thus I_{dc2} and I_{dc4} are approximately 1.5 kA and 0.5 kA, and I_{dc3} maintains around 2 times that of I_{dc4}. At $t_1 = 2$s, the power order in MMC_L begins to ramp from -100 MW to 100 MW, i.e., Station-3 is diverted to a rectifier station, and consequently, Station-2 receives 500 MW power from the other two stations and I_{dc2} finally stabilizes at 2.5 kA. It shows that the DC currents are clear indicators of power variation, because the DC voltage at Station-2 U_{dc2} is precisely controlled at 200 kV. During the reversal process, the MFT currents undergo ramping while its voltages keep constant due to MMC_H's control, as demonstrated by v_{sec}. Another notable feature of SST is fault isolation, which is shown in Fig. 15. Immediately after $t_0 =$ 1s when the fault on DC Line-3 is detected, both MMC_H and MMC_L are ordered to block their driving pulses. As a result, the voltage on both sides of the MFT vanish, indicating that the SST has fault isolation capability. Meanwhile, the power from Station-1 is diverted solely to Station-2 because I_{dc2} has the same amplitude to I_{dc1} and I_{dc4} reduces to 0. Corresponding results from PSCAD/EMTDC confirms these statements, indicating the proposed MMC models can be used for MTDC grid studies.

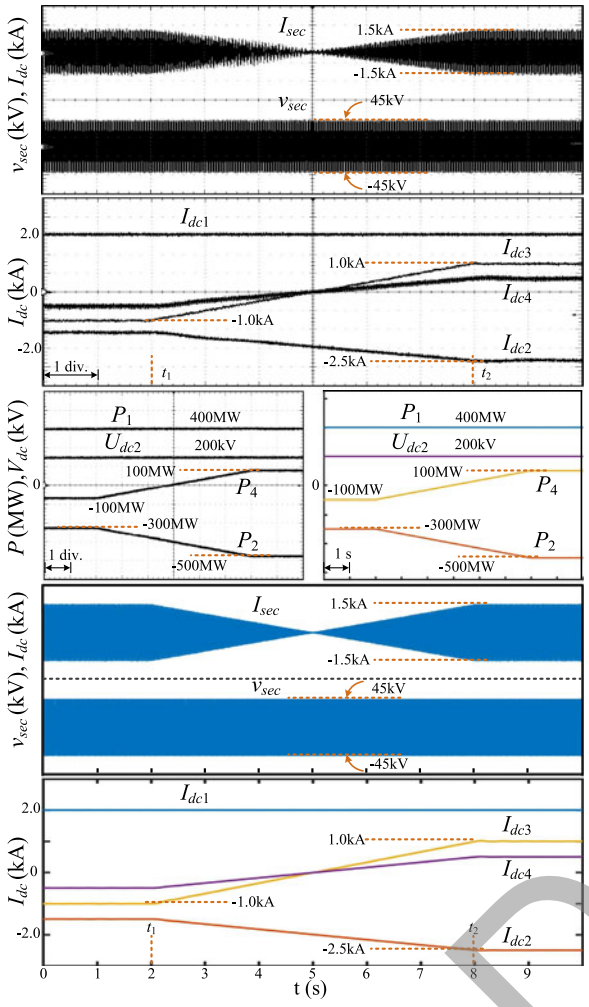

Fig. 14. MTDC system power reversal from HIL emulation (up/left) and PSCAD/EMTDC (bottom/right). Oscilloscope horizontal axes setting: 1s/div.

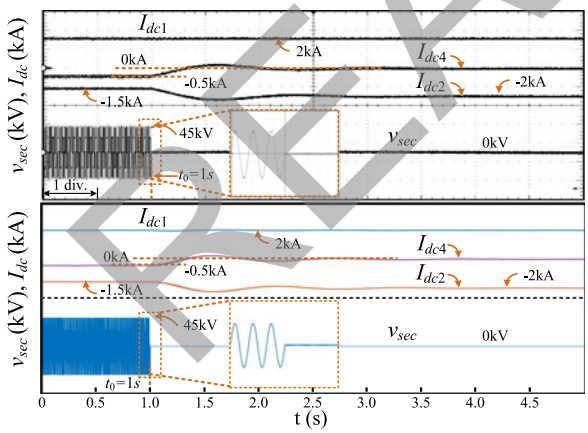

Fig. 15. SST fault isolation test waveforms from HIL emulation (up/left) and PSCAD/EMTDC (bottom/right). Oscilloscope horizontal axes setting: 0.5s/div.

Since the SM blocked state cannot be explicitly shown due to the SST's fault isolation capability, it is proven by applying the improved MMC model and the original TLM-S to MMC_1 in Fig. 1 where a 1Ω line-to-ground fault is imposed on DC Line 1 right after inductor L_1, and corresponding PSCAD/EMTDC

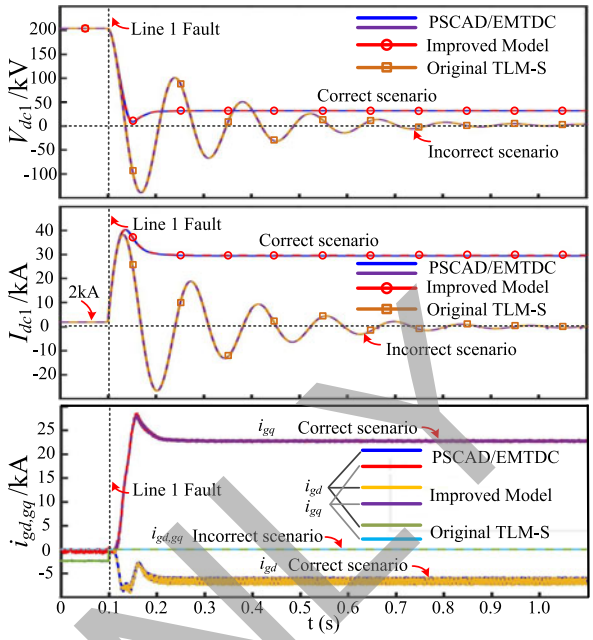

Fig. 16. MMC_1 blocked state test results.

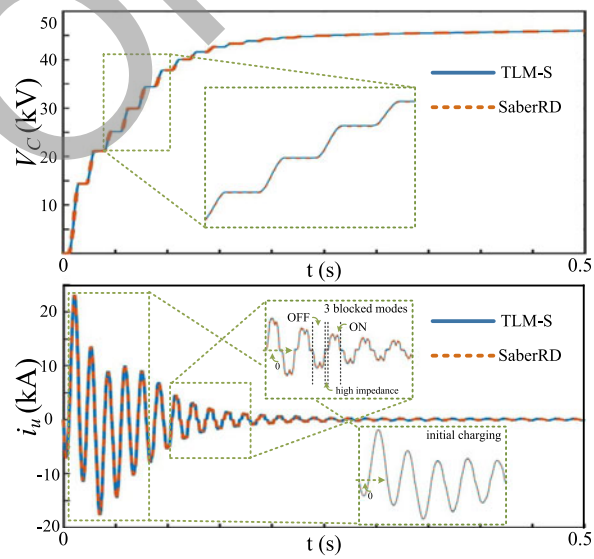

Fig. 17. Passive charging of MMC_1 with opened DC line.

simulations are conducted for validation, as given in Fig. 16. Both models produce the same correct results until $t = 0.1$s when an obvious bifurcation emerges. The improved MMC model yields result identical to that of the traditional model with each IGBT having a free wheeling diode in PSCAD/EMTDC. The AC voltage under this scenario is still being rectified by the diodes so V_{dc1} is about 30 kV, and the fault current stabilizes at around 30 kA. Moreover, in the controller, i_{gd} and i_{gq} deviate from the control target, and their non-zero values prove energy flow between the AC and DC grids. However, with the original TLM-S that fully blocks the MMC, V_{dc1} finally stabilizes at 0 after periods of oscillation, and similar behavior can be observed with the DC current. Meanwhile, i_{gd} and i_{gq} are zero, meaning that no current is flowing from the AC side to the DC side. These

incorrect results are identical to those in PSCAD/EMTDC when a large resistor is inserted between the MMC and DC yard, proving that the original TLM-S has a high-impedance blocked state.

In Fig. 17, the alternation between different SM block states is tested by passive charging of MMC_1 which is operating as an STATCOM, and results from off-line simulation tool are used for comparison. With converter parameters provided as in the Appendix, it can be seen that both the SM capacitor voltages and the upper arm currents are the same. Initially i_u is either positive or negative, indicating the ON and OFF modes of the blocked state. Then, the third state with zero arm current emerges, which indicates that both diodes are OFF and the SM is under high-impedance state.

V. Conclusion

Real-time HIL emulation of a DC-DC converter employing MMC hybrid model for MTDC system is presented. The dynamic curve-fitting model provides guidance on converter design by revealing the device's electro-magnetic-thermal information such as power loss and junction temperature, which facilitates determination of the number of MMC submodules, the MFT's operation frequency, and adoption of external cooling apparatus. The versatility of IGBT curve-fitting model is improved by linking its turn-on and -off times with time constants of RC and RL circuits, and consequently, the transient waveforms can be precisely simulated under various electromagnetic environments. Meanwhile, the MMC TLM-stub model alleviates hardware resource burden and shows its speed advantage in both CPU simulation and HIL emulation on FPGA in conjunction with other complex switch models. Circuit partitioning enables the coexistence of separated nonlinear submodules and the linear MMC circuit even though they have distinct time-steps, and with smaller matrix dimension, a significant speedup can be attained in addition to avoiding numerical divergence. Other than the SST, both models can be applied individually, or jointly by constituting the hybrid model to MMCs in various applications.

Appendix

The 6 piecewise linearized IGBT static model segments are:
1. $I_C >$ 1000A: $k_1 = -4.428T_{vj} + 1567$, $b_1 = -4.263T_{vj} + 1975.5$;
2. $I_C \in (500, 1000]A : k_2 = -2.684T_{vj} + 1113.1, \quad b_2 = -1.867T_{vj} + 1107.4$;
3. $I_C \in (300, 500]A : \quad k_3 = -2.185T_{vj} + 881 b_3 = -1.588, T_{vj} + 772.7$;
4. $I_C \in (200, 300]A$: $k_4 = -1.692T_{vj} + 709, \quad b_4 = -1.179\ T_{vj} + 562.8$;
5. $I_C \in$(0,200]A: $k_5 = 200$, $b_5 = 0$;
6. $I_C <$ 0: $k_6 = 10^{-6}$, $b_6 = 0$.

The IGBT turn-on model's coefficients are:
Segment 1. $k_0 = 0$, $k_1 = 0$, $k_2 = 1$, $k_3 = 0$, $b_0 = 3375$, $b_1 = 1$, $b_2 = -1833.3$, $b_3 = -1.6$;
Segment 2. $k_0 = 0$, $k_1 = 0$, $k_2 = 0$, $k_3 = 0$, $b_0 = 5$, $b_1 = 1$, $b_2 = 0$, $b_3 = 0.24$.

The IGBT turn-off model's coefficients are:
Segment 1. $k_0 = 0$, $k_1 = 0$, $k_2 = 0$, $k_3 = 0$, $b_0 = 1748.3$, $b_1 = 1$, $b_2 = 33.33$, $b_3 = -0.6867$;
Segment 2. $k_0 = 0$, $k_1 = 0$, $k_2 = 0.1$, $k_3 = 0$, $b_0 = 2048.3$, $b_1 = 1$, $b_2 = -200$, $b_3 = -0.6867$;
Segment 3. $k_0 = 0$, $k_1 = 0$, $k_2 = 0$, $k_3 = 0$, $b_0 = 1420$, $b_1 = 1$, $b_2 = 0$, $b_3 = -0.49$.
The IGBT thermal network parameters:
$R_1 = 1.601$ K/kW, $R_2 = 1.765$ K/kW, $R_3 = 0.358$ K/kW, $R_4 = 0.328$ K/kW, $C_1 = 0.362898$ kJ/K, $C_2 = 0.033428$ kJ/K, $C_3 = 0.0167$ 6kJ/K, $C_4 = 0.003049$ kJ/K.
The MTDC system parameters are:
MMC_1 rated power $P_{rec} = 400$ MW, DC line 1 and 2 voltage $V_{dc1,2} = 200$ kV, DC line 3 voltage $V_{dc3} = 100$ kV, $L_{1-4} = 100$ mH.
The SST parameters under 300/180/60 Hz are:
SM capacitance $C_{SM}^{MMC_H}$ =3/12/20 mF, $C_{SM}^{MMC_L}$ =3/5/10 mF, arm inductance $L_{u,d} = 10/15/50$ mH; Y-Y MFT capacity 600 MVar, 110/55 kV; MMC_H 55-level, MMC_L 31-level.
Transmission line parameters: distance 100 km, $r = 0.01\ \Omega$/km, $l = 0.1$ mH/km, $C = 0.2\ \mu$F/km.
The parameters for MMC_1-MMC_3 are: 5-level, $L_{u,d} = 20$ mH, arm inductor resistance $r_{u,d} = 0.1\ \Omega$, $C_{SM}^{MMC_{1-3}} = 10$ mF, grid voltage (L-L, RMS) $V_{g1,2} = 134$ kV, $V_{g3} = 67$ kV.

References

[1] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday, and B. W. Williams, "Quasi two-level operation of modular multilevel converter for use in a high-power DC transformer with DC fault isolation capability," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 108–123, Jan. 2015.

[2] Z. Xing, X. Ruan, H. You, X. Yang, D. Yao, and C. Yuan, "Soft-switching operation of isolated modular DC/DC converters for application in HVDC grids," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2753–2766, Apr. 2016.

[3] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 186–198, Sep. 2013.

[4] R. Li, L. Xu, L. Yao, and B. W. Williams, "Active control of DC fault currents in DC solid-state transformers during ride-through operation of multi-terminal HVDC systems," *IEEE Trans. Energy convers.*, vol. 31, no. 4, pp. 1336–1346, Dec. 2016.

[5] D. Jovcic and H. Zhang, "Dual channel control with DC fault ride through for MMC-based, isolated DC/DC converter," *IEEE Trans. Power Del.*, vol. 32, no. 3, pp. 1574–1582, Jun. 2017.

[6] T. Lüth, M. M. C. Merlin, T. C. Green, F. Hassan, and C. D. Barker, "High-frequency operation of a DC/AC/DC system for HVDC applications," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4107–4115, Aug. 2014.

[7] F. Kong, Z. Hao, S. Zhang, and B. Zhang, "Development of a novel protection device for bipolar HVDC transmission lines," *IEEE Trans. Power Del.*, vol. 29, no. 5, pp. 2270–2278, Oct. 2014.

[8] A. Hassanpoor, A. Roostaei, S. Norrga, and M. Lindgren, "Optimization-based cell selection method for grid-connected modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2780–2790, Apr. 2016.

[9] F. Zhang, W. Li, and G. Joós, "A voltage-level-based model predictive control of modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 5301–5312, Aug. 2016.

[10] U. Karaagac, J. Mahseredjian, L. Cai, and H. Saad, "Offshore wind farm modeling accuracy and efficiency in MMC-based multiterminal HVDC connection," *IEEE Trans. Power Del.*, vol. 32, no. 2, pp. 617–627, Apr. 2017.

[11] H. Saad *et al.*, "Dynamic averaged and simplified models for MMC-based HVDC transmission systems," *IEEE Trans. Power Del.*, vol. 28, no. 3, pp. 1723–1730, Jul. 2013.

[12] N. Ahmed, L. Ängquist, S. Norrga, A. Antonopoulos, L. Harnefors, and H. P. Nee, "A computationally efficient continuous model for the modular multilevel converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 4, pp. 1139–1148, Dec. 2014.
[13] L. Wei, R. J. Kerkman, R. A. Lukaszewski, H. Lu, and Z. Yuan, "Analysis of IGBT power cycling capabilities used in doubly fed induction generator wind power system," *IEEE Trans. Ind. Appl.*, vol. 47, no. 4, pp. 1794–1801, Jul. 2011.
[14] K. Sheng, B. W. Williams, and S. J. Finney, "A review of IGBT models," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1250–1266, Nov. 2000.
[15] B. J. Baliga, "Analytical modeling of IGBTs: Challenges and solutions," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 535–543, Feb. 2013.
[16] D. Xu, H. Lu, L. Huang, S. Azuma, M. Kimata, and R. Uchida, "Power loss and junction temperature analysis of power semiconductor devices," *IEEE Trans. Ind. Appl.*, vol. 38, no. 5, pp. 1426–1431, Sep. 2002.
[17] A. D. Rajapakse, A. M. Gole, and P. L. Wilson, "Electromagnetic transients simulation models for accurate representation of switching losses and thermal performance in power electronic systems," *IEEE Trans. Power Del.*, vol. 20, no. 1, pp. 319–327, Jan. 2005.
[18] U. N. Gnanarathna, A. M. Gole, and R. P. Jayasinghe, "Efficient modeling of modular multilevel HVDC converters (MMC) on electromagnetic transient simulation programs," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 316–324, Jan. 2011.
[19] H. Selhi, C. Christopoulos, A. F. Howe, and S. Y. R. Hui, "The application of transmission-line modelling to the simulation of an induction motor drive," *IEEE Trans. Energy convers.*, vol. 11, no. 2, pp. 287–297, Jun. 1996.
[20] ABB Applying IGBTs, Application Note 5SYA 2053-04. Aug. 2012. [Online]. Available: http://www.abb.com/abblibrary/DownloadCenter/
[21] F. Dugal, E. Tsyplakov, A. Baschnagel, L. Storasta, and T. Clausen, "IGBT press-packs for the industrial market," *Proc. PCIM Eur.*, Nuremberg, pp. 1–8, 2012.
[22] Z. Luo, H. Ahn, and M. A. E. Nokali, "A thermal model for insulated gate bipolar transistor module," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 902–907, Jul. 2004.
[23] V. Brandwajn, H. W. Dommel, and I. I. Dommel, "Matrix representation of three-phase N-winding transformers for steady-state and transient studies," *IEEE Trans. Power App. Syst.*, vol. PAS-101, no. 6, pp. 1369–1378, Jun. 1982.
[24] J. Liu and V. Dinavahi, "A real-time nonlinear hysteretic power transformer transient model on FPGA," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3587–3597, Jul. 2014.
[25] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.

Ning Lin (S'17) received the B.Sc. and M.Sc. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2008 and 2011, respectively. He is currently working toward the Ph.D. degree in the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada. Later, he worked as an Electrical Engineer on FACTS and HVDC control and protection. His research interests include real-time simulation of power electronics, power systems, and field-programmable gate arrays.

Venkata Dinavahi (SM'08) received the Ph.D. degree from the University of Toronto, Toronto, ON, Canada, in 2000. He is a Professor of electrical and computer engineering with the University of Alberta, Edmonton, AB, Canada. His research interests include real-time simulation of power systems, device-level modeling, large-scale systems, and parallel and distributed computing.