A quad-channel 8GS/s 6-bit Successive Approximation Register Analog to Digital Converter

by

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Abstract

To compete in the growing market of integrated circuit design, designers are required to ideally develop circuits which consume less power, occupy lower area, and have a better performance. Yet, the trade-offs between power, area, and performance set limits for the designers. As a result, extensive research has been done to explore possible architectural advancements or to optimize available architectures in order to improve the performance, power, and area (PPA) characteristics of the designs.

To keep up with the increasing need for higher bandwidths, optimization of wireline transceivers has been the target in many researches. In conventional mixed-signal transceivers, most of the equalization techniques were applied to the signal in the analog domain. Moreover, scaling of the CMOS technologies has risen a need for more precise linearity requirements. Thus, ADC-based receivers, providing the chance to conduct equalization in digital domain while benefiting from other advantages of this domain, have become popular over the past years.

ADC-based receivers include a front-end, the power-hungry ADCs, and the digital equalization circuitry. The front-end extends channel's bandwidth, compensates for the loss, and provides copies of the input signal for multiple ADCs - only in time-interleaved structures. Then, one or a set of power-hungry ADCs digitize the signal. In our work, the main focus was to reduce the power consumption of the ADCs and provide a higher bandwidth and linearity (performance), while keeping the area same as previous designs.

We improved the structure and optimized the PPA of an ADC-based receiver. First, this work presents a novel multi-branch cascoded buffer. The results of our

simulations showed a higher -3dB bandwidth and better linearity compared to conventional buffers. In addition, using this structure may lead to almost perfect compensation for gain mismatch. Although, additional circuitry to compensate the mismatch was not implemented in our work, our simulations have proven the idea. Secondly, the StrongArm-based comparator was optimized to achieve its maximum gain-speed product. Afterward, the condition to optimize the $\frac{Gain*Speed}{Power}$ of the structure was obtained. The optimized comparator proved to be 58% faster and consume less than 95% of the previous design's power, while providing a higher gain. Thirdly, the structure of the digital control block was also technically optimized, operating with the same function, proving to be almost 25% faster and consuming less power.

Acknowledgments

During my time at university of Alberta, I have encountered many people who supported me and helped me in completing this work. In this section, I would like to thank all those who help and supported me.

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Abbreviations

ADC	Analog to Digital Converter 7
CAP	Capacitor 41
CAPDAC	Digital-to-Capacitance Converter 30
CTLE	Continuous-Time Linear Equalizer 33
DAC	Digital-to-Analog Converter 29
DFF	D flip-flop 41
diff-pair	Differential pair 34
DNL	Differential Non-linearity 74
ENoB	Effective Number of Bits 74
INL	Integral Non-Linearity 74
MOSFET	metal–oxide–semiconductor field-effect transistor 37
S/H	Sample and Hold 29
SAR	Successive Approximation Register 13
SARADC	Successive Approximation Register Analog to Digital Converter 2
SFDR	Spurious-Free Dynamic Range 74
SNDR	Signal-to- Noise-and-Distortion ratio 74
SNR	Signal-to-Noise Ratio 31
TI	Time Interleaved 7

Chapter 1

Basic Understanding

1.1 Motivation

Data in modern electronic systems is stored and processed in the digital domain. Yet, most of the input of these systems are analog, a digital camera's input, signals that are picked up by a radar, music, sound. etc. Moreover, analog circuits are able to process the analog signals at a low cost. For simple functions such as amplification, simple comparison, and filtering, analog circuits were traditionally more than sufficient. However, complexity of advanced electronic circuits and systems makes analog circuits either costly or impractical.

On the other hand, digital domain provides unlimited Signal-to-noise ratio(SNR), option to store data at almost zero cost, and the chance to carry complex processes. To take advantage of the mentioned capabilities of digital domain, ADCs are used usually at the early stages of the processing system, making them one of the keys to system's success. Nowadays, in many cases, the speed and quality of converters limits the performance of digital systems.

In addition, with the increasing demand for bandwidth caused by internet of things, streaming services, cloud storage, etc, wire-line links at data-centers are required to operate at higher and higher speeds. At the time of writing this work 56Gb/s and 112Gb/s links have already been industrialized. Currently, ADC-based receivers are the only viable solution for links at data-rates which exceeds 50Gb/s [1]–[4].

A comprehensive study [5], conducted in the United States found that data-centers consume approximately 70billion Kwh/year, equivalent to 7BUSD, which drive the research for high-speed low-power systems. In these systems, most of the power is consumed in the power-hungry analog blocks such as ADCs.

As a result of being power hungry widely used block, researches to improve the performance of the A-to-D converters has become a trend in the past years. In almost all cases, the aim is to optimize the performance, power, and area (PPA) of these data converters. Due to high digital dependence and low power consumption, Successive Approximation Register Analog to Digital Converters (SARADCs) are preferred over other Nyquist-rate options.

1.2 Objectives

As explained, lower power consumption, lower area occupation, and higher performance for SARADC-based receivers drives extensive research to reduce the total power consumption of the systems.

In this work, the main objective is to increase the performance of the SARADCs proposed in previous works. In a systematic approach, the main focus was to improve the sub-blocks of the SAR - sampler, inter-leaver, digital logic, etc. - separately and then integrated them as a whole.

Apart from improving the SAR and its sub-blocks, this work hopes to extend the bandwidth of the SARADC-based receiver by improving the front-end structure. At the same time, other aspects like linearity, inherent mismatch, etc are hoped to improve in this work.

1.3 Outline

The thesis is structured into five main chapters as follows:

In chapter 1, the motivation that drove this need for this work is discussed. The

objectives that this work was hoping to achieve were discussed and the outline of the work is being illustrated.

Chapter 2 discusses the concept behind analog to digital conversion. Afterwards, different types are ADCs and their operation are discussed. The performance, power, and area (PPA) characteristics of the structures are compared based on the comparison and literature review and trend in the industry, the base of this work was chosen to be a 6-bit SARADC.

In Chapter 3, the structure of the receiver is illustrated. Each of its blocks, their operation, limitations, and possibilities to improvement are discussed. A novel buffer is presented and compared to the conventional buffers. The buffer provides higher bandwidth, higher linearity, a chance to compensate for mismatch, etc. which are discussed in details in the allocated section. Then the StrongArm latch is optimized based on the equations to achieve the highest PPA in the amplification phase. Also, digital logic of the SAR is modified to achieve lower power consumption and higher resolution in the CAPDAC block. Finally, timing breakdown of one of the previous works [6] is compared with this work.

After describing the improvements, ideas, and simulation results, chapter 4 presents the post-layout characteristics of the SAR and some of SAR sub-block. Afterward, the characteristics of the receiver were then simulated and presented.

Finally, a summary of the work is illustrated in chapter 5. Afterward, the contributions are summarized briefly and possible future works are discussed.

Chapter 2

Background and Literature review

Analog-to-digital converters are the bridge between the Analog domain and Digital domain. These blocks quantize the analog signal in two dimensions, amplitude and time, and convert them to digital codes. The amplitude range of their input is divided into a finite number of levels called quantization levels. When the analog input is between two levels, a quantizer makes an approximate decision. Afterwards, an encoder transforms this approximated quantized level into a binary digital code (symbol). While the quantizer and encoder are operating, the input signal needs to be held. Another circuit, called sample-and-hold (S/H) circuit, holds the input during the quantization, quantizing the input in the time domain.

The amplitude translates to an N-bit binary digital code, output of the encoder. Each bit is either a '0' or a '1' (two possibilities for each bit); therefore, there are 2^N possibilities for each symbol. The higher the number of bits in output digital code, the higher the quantization accuracy of ADC. The principle behind the operation of ADC is demonstrated in Fig. 2.1.

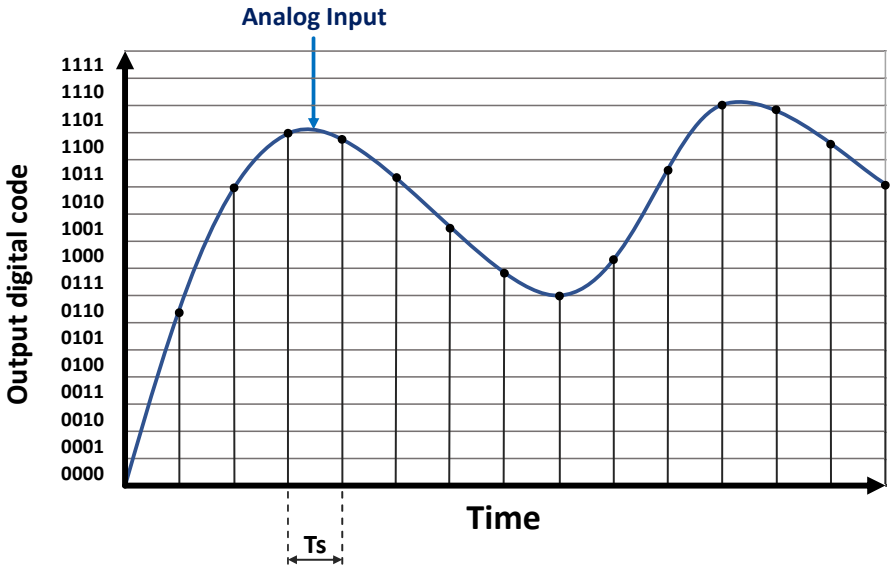


Figure 2.1: Principal of the operation of ADC

Sample-and-hold circuit has two phases, the sampling phase and the holding phase. At first, the circuit tracks the value of the analog input (Sampling phase). Once it starts following the input with an acceptable error, it can hold its value (Holding phase). The clock controlling these phases is designed in a way that provides enough time to track the input signal and hold it long enough to ensure quantization and encoding are done. The minimum time for each clock cycle is the summation of the minimum duration required for phases ($T_S = T_{sample} + T_{hold}$), and the maximum operating frequency of the block is ($F_S = 1/T_S$).

2.1 Basics of ADC and recent advancements

This section provides the reader with the basic knowledge and understanding to follow the enhancements this work has to offer. In this section, the Nyquist theorem is explained, following the resolution, quantization, and its error are elaborated for the reader. Afterward, the most common structures and their functions are discussed in details. After comparing these structures (first order comparison), the recent advancements in the field - i.e. Monotonic switching, Redundancy techniques, Ping-

Pong, mission-mode offset correction, digital interpolation, and hybrid structures - are explained. The ending of the chapter will cover the answer to the question why a 6-bit resolution is the target of this work.

2.1.1 Nyquist Theorem

The Nyquist theorem (sampling theorem) states, 'to capture all the information from a continuous-time signal, the sampling rate must be at least twice the maximum frequency of the input signal'. According to the theorem, as long as the sampling rate is more than twice the maximum frequency component of the signal in frequency domain, input can be recovered from discrete-time symbols without any information loss [7].

Based on the sampling rate, there are two groups of ADCs: Nyquist rate ADCs and oversampling ADCs. In Nyquist rate ADCs, the maximum frequency component of input signal is equal or slightly less than the Nyquist frequency, $F_{Nyquist} = F_{CLK-ADC}/2$. If the input has frequency components higher than $F_{Nyquist}$, Nyquist converters are unable to convert the signal properly. In oversampling ADCs, the maximum frequency of the input is much lower than $F_{Nyquist}$.

2.1.2 Resolution and quantization error

The measurement (quantization) precision is determined by the bits in the output digital code, resolution of the ADC. The greater number of bits in each symbol the more precise the measurement values. For an N-bit ADC, each symbol has 2^N possibilities; therefore, 2^N quantization levels. The step size between two consecutive levels is equal to $V_{LSB} = \frac{V_{Full-scale}}{2N}$, the smallest detectable interval.

When the analog sampled signal is digitized, all the continuous values between $n * V_{LSB}$ and $(n+1) * V_{LSB}$ are mapped to one binary digital code ($0 \leq n \leq 2^N - 1$). The mapping causes a difference between the quantization level and the actual analog input, "quantization error" (Fig. 2.2). This error - an irreversible error – prohibits

the signal from being reconstructed perfectly.

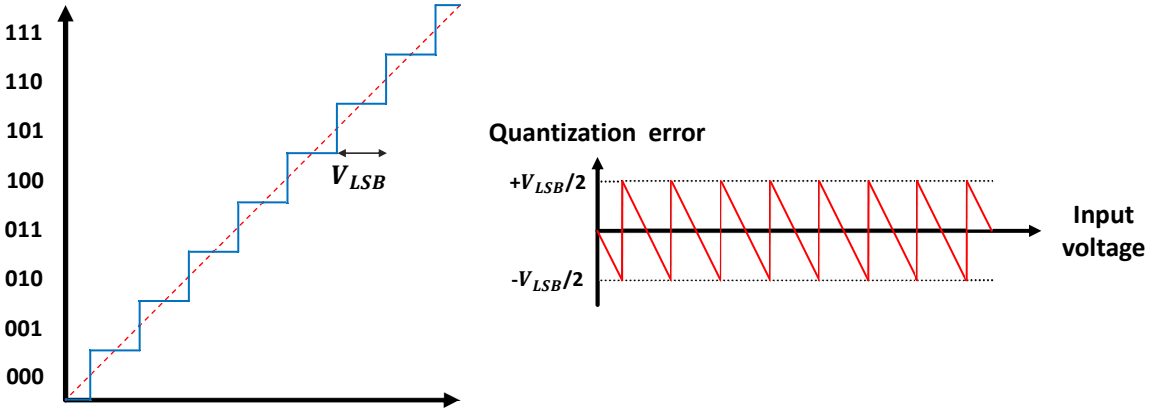


Figure 2.2: Quantization levels and error

2.1.3 Types of ADC

In high-speed application, Nyquist rate ADCs are generally used to digitize the data. For each application, based on its needs and requirements (speed, resolution, delay, throughput, power and area), there a different architecture is used. Each of these architectures has its own advantages and disadvantages. Some of the most common types of ADCs are:

- Flash Analog to Digital Converter (Flash ADC)
- Pipeline Analog to Digital Converter (Pipe-line ADC)
- Successive Approximation Register Analog to Digital Converter (SARADC)
- Timed-Interleaved Analog to Digital Converter (TI-ADC)

This section describes the architectures, their advantages, and disadvantages.

Flash ADC

The simplest A-to-D is a comparator, a one bit A-to-D comparing an input with its reference. A set of paralleled comparators, each connected to a different reference voltage, generate a thermometer code representing the input. An encoder converts

the thermometer code to a binary code. The described configuration is the simplest ADC structure, called flash ADC.

Having a parallel structure, flash ADCs are the fastest ADCs [8]–[10]. An example of a 2-bit flash ADC structure is illustrated in Fig. 2.3. In this structure, a resistor ladder divides V_{ref} into three $(2^3 - 1)$ values (quantization levels). The number of these values is exponentially proportional to the resolution of ADC. Each of the quantization levels connects to the reference of one comparator. The input of all comparators connect to V_{in}. The comparators compare the inputs and generate a thermometer digital array proportional to the analog input. Then, an encoder network generates an equivalent N-bit binary code from the thermometer array. Based on the operation, an N-bit flash ADC has $2^N - 1$ quantization levels, 2^N resistors, $2^N - 1$ comparators, and N binary output bits.

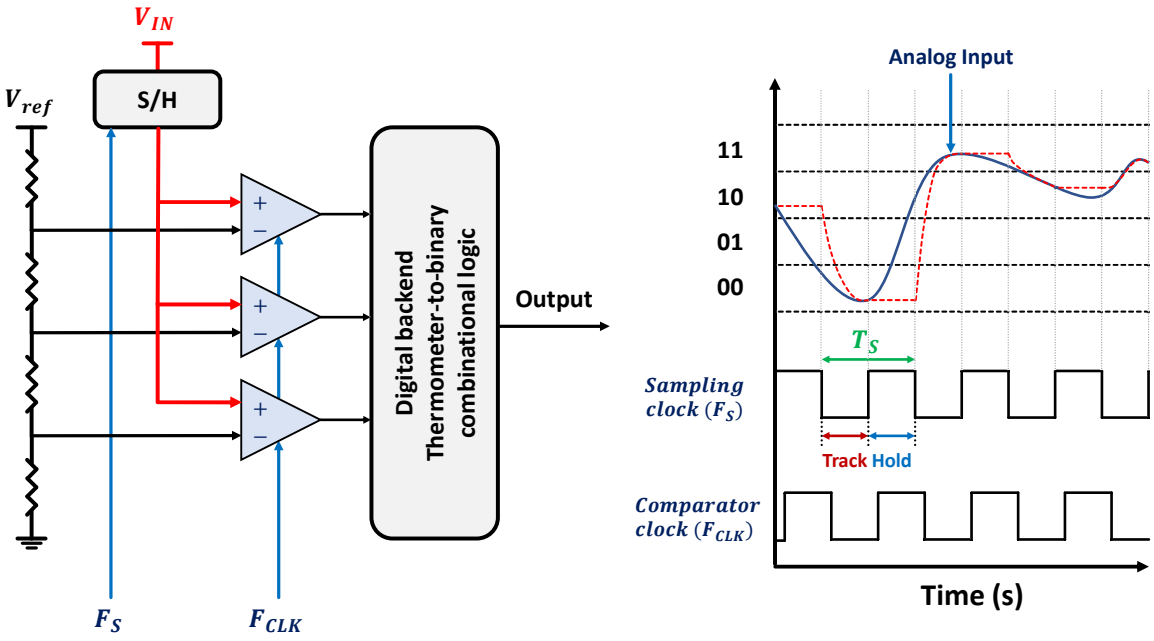


Figure 2.3: Architecture of flash ADC and its operation

The flash ADC converts the Analog input to binary digital code in one clock cycle. Each cycle has two phases (Fig. 2.3): sampling input and holding it, applying it to comparators and determining the binary output and storing it. Both S/H circuit

and comparators operate with the same clock; however, the comparator clock must happen with a delay to ensure proper settling for S/H. Thus, the conversion time is limited by how fast S/H track settles, and the comparator makes decisions. Encoding and storing can take place while the S/H tracks the next input. In the flash structure, all comparators are clocked at the same time and the sequences happens in one cycle, making flash structure the fastest structure.

Being the fastest structure comes with some drawbacks. A N-bit flash ADC requires $2^N - 1$ comparators and a more complex encoder. Each of the comparators requires a unique reference voltage, usually generated by a resistor ladder. This means both area and power grow exponentially as the resolution increases. At the same time, the offset voltage of the comparators becomes an issue as the number of bits grows usually beyond five. On top of these limitations, another issue is the bandwidth of input. Connecting $2^N - 1$ comparators to input, the capacitance increases exponentially, causing a drop in bandwidth. Using multiple S/H circuits and/or clocked comparators, one can take care of the bandwidth limitation. Yet, it introduces jitter as a new issue. Flash ADCs performance is dependent on the S/H circuit's ability to sample input without jitter. Kickback noise is another issue. Some physical aspects in the layout like routings or error in the resistor ladder and its accuracy can also cause some issues. Taking care of all this issues requires lots of accessories, thus increasing power consumption and area occupation, making flash ADCs suitable only for applications with no power or area limitation.

Pipleline ADC

The main disadvantage of flash ADCs is the need for $2^N - 1$ comparators, requiring lots of power and area for a high number of bits. One way to solve the power-area problem is to trade some reduction in speed for a significant improvement in area. For example, one can split a 2N-bit flash ADC into two N-bit flash ADCs. The first N-bit ADC finds the first N most significant bits. Afterward, the circuit amplifies the

residue, and finds the N least significant bits using the fine ADC. To find the residue, the first (coarse) ADC output goes to a rather fast Digital to Analog converter (DAC). Afterwards, the amplifier subtracts the coarse quantization level from the input and amplifies the residue. Then the fine ADC starts the second operation to generate the remaining bits. This structure, illustrated in Fig. 2.4, is called two-step flash ADC.

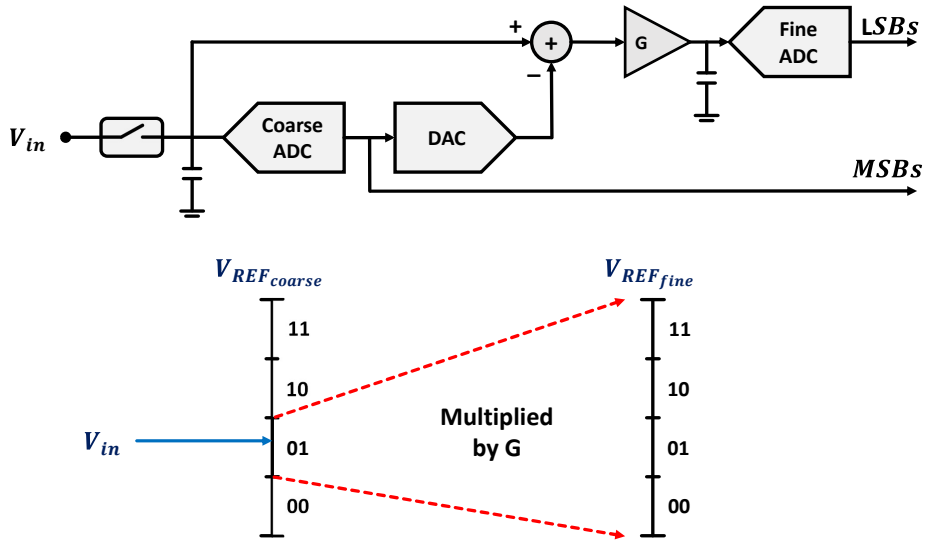


Figure 2.4: Architecture of two-step flash ADC and its operation

In a two step flash ADC, the number of comparators has reduced from 2^{2N} to $2*2^{N}$, therefore a lot of power and area is saved. On top of that, the input capacitance is reduced from 2^{2N} to 2^{N}. The cost for these improvements is the speed of the structure. In addition to signal passing two ADCs (coarse and fine), additional delays are introduced to the signal path by the DAC and amplifier. Thus, the delay of this system is more than twice the flash ADC. However, by Adding N registers, the coarse ADC outputs can be saved. This way, the coarse ADC can make the decision for the next cycle MSB-bits while fine ADC is generating the LSB-bits. This requires another S/H circuit and switching between the ADCs. Doing so, the throughput of the system becomes more or less equal to the flash structure, while the delay of the system remains more than twice the flash structure.

Though providing a low power solution for highspeed ADCs, two-step flash ADCs

come with some disadvantages. The delay to generate the final digital output is unavoidable. Both coarse and fine ADCs require S/H circuits. The residue amplifier's gain needs to be as linear and accurate as possible; otherwise, severe linearity issues comes into the picture. DAC non-linearity is another source that can cause errors in the transfer curve of the ADC.

Assuming that one can replicate the structure accurately and noise is not accumulating, the concept can be applied to any arbitrary number of bits. The extension of two-step ADC is called a pipeline ADC. The architecture of a pipeline ADC is shown in Fig. 2.5.

The coarse stages are similar to two-step ADC's. They consist of an ADC, DAC, subtractor, and residue amplifier. At the very end of the coarse stage series, there is a fine flash ADC which generates the LSBs. DAC, subtractor, and amplifier operations are done usually using a multiplying DAC (MDAC) [11].

The minimum possible value for the number of bits for coarse ADCs and fine ADC is one. Thus, the minimum number of comparators for N bits in pipeline structure (Fig. 2.5) is N comparators. The total delay of the structure is N times the delay of one stage, more or less N times the delay of flash. However, the throughput is almost equal to flash. In pipeline, at the cost of the delay, the number of comparators reduces from $2^N - 1$ to N; thus, the input capacitance, the power consumption, and area occupation reduces significantly compared to flash, making pipeline architecture a suitable option for power-efficient high-speed conversion of wide bandwidth input signals where minimum area occupation is not necessary.

This structure, as good as it sounds, has some drawbacks. In applications that the latency (delay) matters, flash ADCs have a great advantage compared to pipeline structure. In pipeline ADC, the bit generated by the first coarse ADC is not related to the bit generated to other ADCs. To align the outputs of the ADCs in the pipeline structure, the "K"th ADC output has to be shifted $N - K - 1$ times.Therefore, at least $\frac{(n*(n-1))}{2}$ registers are required to have access to the symbol. In addition to the

number of registers, noise accumulation in the series of stages is another issue.

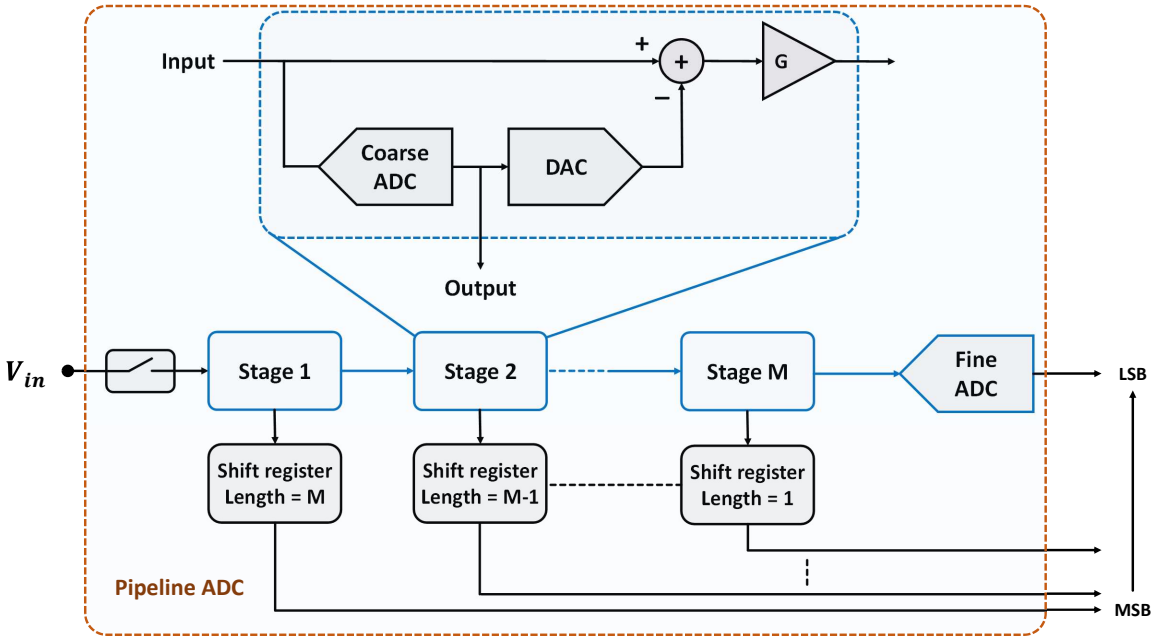


Figure 2.5: Architecture of pipeline ADC

Successive Approximation Register Analog to Digital Converter

In most cases, especially in industry, area and power are the limiting factors, not speed. Another approach to making the structure smaller is to reuse one comparator in the cycles, updating it inputs. The output of the 1-bit ADC (comparator), once the decision is made, goes to a control logic and updates the input/reference value. Once the new input/reference is settled, the comparator is ready to make the next decision. In this structure, the number of comparators reduces from N (pipeline) to only one. This structure (Fig. 2.7) is often called Successive Approximation Register Analog to Digital Converter (SARADC).

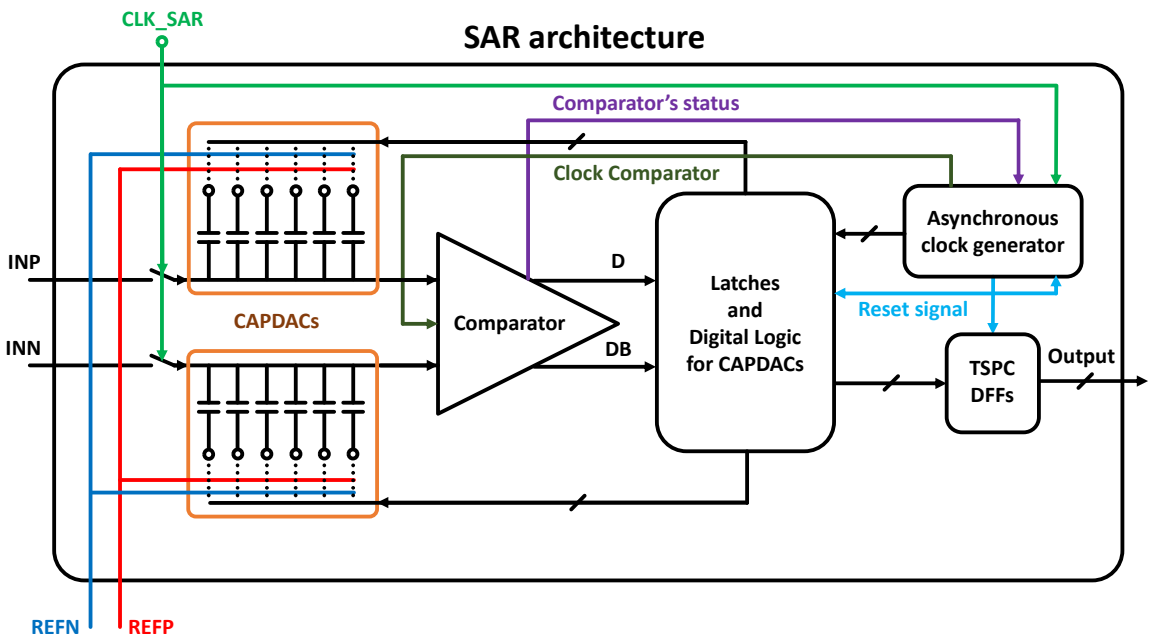


Figure 2.6: Architecture of SARADC

SARADCs usually use a binary search algorithm, illustrated in Fig. 2.7, to generate the N-bit digitized output. Each time the comparator makes a decision, it breaks the range into half, starting with the MSB. If the input is above the middle point of the full-scale range, the comparator generates a '1'. Otherwise, it generates a '0'. After that the input is compared to a new reference, representing the next most significant bit. The trend goes on up to the point that all N-bits are generated. Since SARADCs re-use the same comparator, it will take N comparison cycles to digitize the input to an N-bit binary code. Chapter 3 takes about the architecture in details, its function, blocks, their limitations, and possible improvements in details.

Requiring only one comparator suggests that SARADCs power and area consumption is significantly lower than other ADC structures described up to this point. On the other hand, SARs' delay/throughput is N times the delay of each comparison cycle. The delay of each cycle is equal to the summation of the following:

- Time that the comparator takes to make the decision
- Time that the control logic block takes to update the reference/input

Each cycle's delay being almost equal to the delay of flash structure, both delay and throughput of SARADC is almost N times the flash structure. However, SARADC requires only and only one comparator instead of $2^N - 1$ comparators for an N-bit ADC.

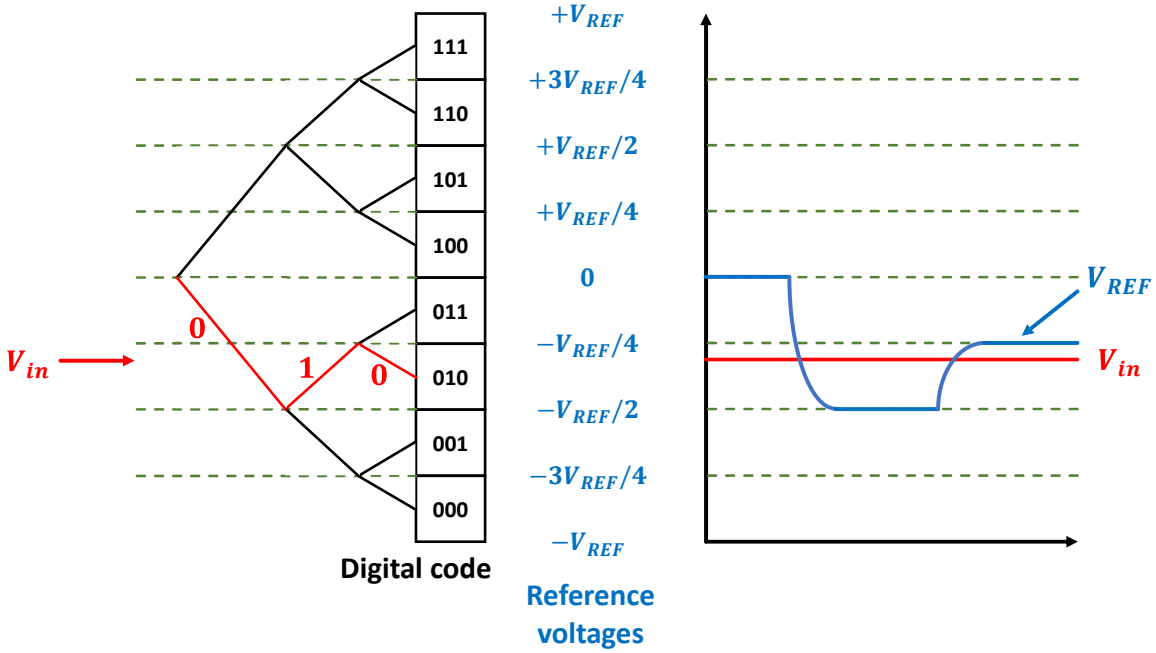


Figure 2.7: SARADC operation

As perfect as it might sound, there some limitations in this structure. This structure requires a S/H circuit, registers, latches, a logic block to control input/reference, etc. The resolution is also limited by the sensitivity of the comparator and the accuracy of controlling input/reference. In addition, having a high resolution requires more cycles and more time. Therefore, the leakage in S/H circuit over that time might give rise to some issues.

Time-Interleaved Analog to Digital Converter

One method to increase the speed of the ADCs is simply to put them in parallel. This way structures can achieve smaller system conversion times. One of the applications of using Time-Interleaved structures is to achieve speeds above the maximum speed of the flash ADCs. By running multiple flashes in parallel (time interleaving

flashes), with a delay in between, higher speeds are achieved. Each ADC has a front-end S/H circuit, clocked with a different delay. If timed correctly, by the time the last ADC is clock, the first ADC's data is ready, and first flash is ready for the next conversion cycle. Having N S/H circuits and N ADCs, ideally, time-interleaved flash (TI-flash) reachs N times the speed of flash ADC. One of the limitations in TI-flash ADCs is the accuracy of timing. Clock jitter in very high frequencies affects the performance significantly.

SAR ADCs can also be interleaved (Fig. 2.8). In the case of SAR ADCs, interleaving makes even more sense. The clock has N-times lower frequency compared to flash structure; therefore, jitter will not cause a significant issue. Operating M times faster, the throughput of time-interleaved SARADCs can reach M/N times the throughput of flash ADCs. When M=N, the digital code is converted at the speed of flash using N-times interleaved SARADC structure. Also, minimum area is likely to be somewhere close to this point [12]. Therefore, only at the cost of delay being N times the typical flash ADC, a lot of power and area will be saved.

In addition, in SARADCs the S/H circuits capacitance is usually a binary capacitor controlled by switches (CAPDAC). As the number of bits grows the CAPDAC size increases exponentially. For example, a 9-bit SARADC's CAP size is $2^9 * C_{unit}$. However, a 6-bit 8-way time-interleaved SARADC, each SAR's CAP size is $2^6 * C_{unit}$. It is obvious that the settling time of the CAPDAC reduces significantly in the TI-SARADC compared to normal SARADC structure for the same number of bits, allowing higher operation speed.

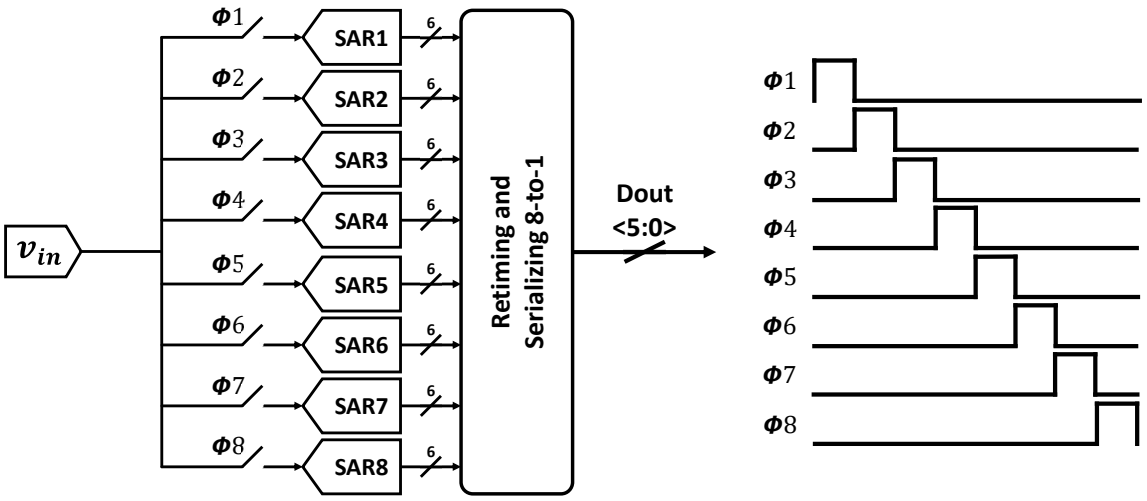


Figure 2.8: Time interleaved SARADC structure

Some ADC structures were explained briefly in this section. Obviously, there are more structures and variations - Interpolating ADCs, Folding ADCs, multiple-bit pipeline ADCs, multiple-bit pipeline ADCs with digital error correction, wide-band delta-sigma ADCs, DC optimized delta-sigma ADCs, and Hybrid ADCs. However, they are not relative to this work; thus, have not been included.

2.1.4 Comparing architectures - first order approximation

All of structures explained in this section are compared in Tab. 2.1. The numbers provided in Tab. 2.1 are only an approximation based on the number of comparators. Each of these designs may have an encoder, a control logic, a CAPDAC, a MDAC, or an amplifier, changing the power consumption, delay, etc. However, this approximation provides a to choose the best architecture based on the needs and limitations.

Architecture	Flash	Two-step flash	Pipeline	SAR
Energy / clock cycle	2^N	$2^{N/2+1}$	N	1
Throughput	1	1	1	$\frac{1}{N}$
Delay	1	2	N	N
Conversion speed	1	0.5	1	$\frac{1}{N}$
Energy / conversion speed	2^N	$2^{N/2+2}$	N	N
Area	2^N	$2^{N/2+1}$	N	1

Table 2.1: First order comparison between different ADC architectures

Tab. 2.1 presents a first order estimation of the energy consumption per cycle, throughput, and conversion speed of different Nyquist ADC architectures. Based on the estimation, Flash ADCs are a suitable choice for high speed applications. Moving toward two-step flash, the energy per cycle is reduced. However, the conversion speed has also reduced to $2^{\frac{N}{2}+1}$, increasing energy per conversion speed. Extending the technique and using several 1-bit comparison cycles, pipeline ADC reduces the total number of comparators to N, however requires additional circuitry in each stage. The need for the additional circuitry limits the speed and increases the power consumption. As a result, the energy per clock cycle is more than N comparators and the speed is less that the speed of the Flash. In the SAR, one single comparator performs the binary search in N cycles; therefore, the power consumption of the is almost equal to one comparator.

Time interleaving the SAR structure, throughput almost equal to flash ADC structure is ideally achieved, assuming M=N. At the cost of increasing the delay of an order of N, the equation for energy consumption per conversion speed changes from 2^N to $\approx N^2$. Therefore, ideally for N¿4 TI-SARADC has more power efficiency. The area occupation equation will also change from 2^N to N, a first order approximation. As a result, it can be concluded that the SAR becomes a suitable choice as the number

of bits increases.

2.2 Recent advancements in ADC design

This section will elaborate a recent trend on high-speed ADCs with the focus on the followings:

- Monotonic switching
- Redundancy
- Alternating comparators aka Ping-Pong
- Offset correction
- Increasing conversion speed - Flash-SAR
- Digital interpolation

2.2.1 Monotonic switching

In 2010, [13] proposed a switching method - monotonic switching - which significantly reduces the power consumption of the SAR structure while reducing the total capacitance in the CAPDAC of the SAR by 50%. The benefits that this switching technique provides pushes this work to utilize the structure.

In the next chapter [Section 3.2.1], the reader will be provided with a detailed explanation that will cover the procedure of the monotonic switching, its power consumption compared to traditional switching, and the layout considerations for implementing the capacitors. In addition, the reader may refer to [13] in case they are interested in additional information about the procedure this switching method follows.

2.2.2 Redundancy

Due to the settling time of the CAPDAC incorrect decisions can be made, which may lead to selection of a search space to which the input does not belong. The pre-selection of a wrong search space before the last cycle, even if the remaining decisions are correct, will result in a difference greater than 1-LSB, reducing the performance of the system.

One of the technical improvements which can improve the performance of the ADC is to conduct the search algorithm in a non-binary format which requires extra steps. This technique is an effective way to relax the settling constraints of the capacitive DACs. In this case, the comparator does not require CAPDAC's voltage value to settle down completely. Generally for high resolution SAR ADCs, the time that takes for the CAPDAC voltages to settle down is larger than additional cycles needed in the non-binary search to resolve equal number of bits. As it is illustrated in Fig, 2.9, providing only 12.5% margin for the worst-case scenario, the SAR requires one an extra 25% conversion time for a cycle. The same concept can be done in a binary-weighted search as illustrated in Fig. 2.9.

In 2010, Chun-Cheng Liu published "A 10b 100MS/s 1.13mW SAR ADC with binary-scaled error compensation" [14]. In this work, using the monotonic switching procedure and adding compensative capacitors and digital error correction logic (additional circuitry), they were able to conduct binary compensation. In this technique, additional binary-scaled capacitors are inserted to the CAPDACs of the SARs, providing compensative voltage values. By shifting the covered range of the search algorithm in additional cycles, the circuit compensates for the error caused by the CAPDAC settling time.

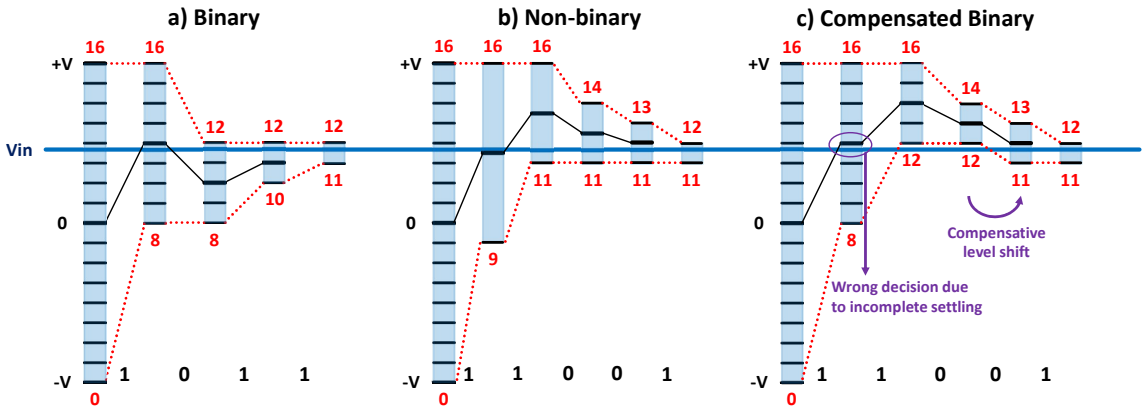


Figure 2.9: Elaboration of redundancy and binary compensation techniques in SAR ADCs [14]

The downsides of these techniques are as follows: Complexity, Increased power consumption, additional area for the compensative capacitors, and requiring additional cycles. All of the disadvantages that comes with redundancy has pushed this work to aim for designing a faster digital control unit to ensure faster settling time for the CAPDAC voltage values.

2.2.3 Alternating comparators

Alternating comparators is a technical advantage which was introduced by Lukas Kull in 2013 [15]. As illustrated in Fig. 2.10, in this technique, two comparators are connected to the capacitive DAC of the SAR, improving the settling time of the voltages seen at the comparator. In this structure the key to the performance of the system is the comparator. Noise profile, decision speed, and many other characters of the system are achieved with the optimize design of the comparator. As explained, this structure and many others require a high performance comparator with fast decision making, high gain, and lower power consumption.

In the SAR structure, when two conditions - redundancy and low-impedance capacitive reference voltage - are met, the settling time of the capacitive DAC will remain very short. As a result, the limit of the cycle speed is set by two main points: decision time of the comparator and the reset time. Reset time is of importance to

ensure that history from the previous state of the comparator does not affect the next - minimum dynamic offset. To achieve this, traditionally, there were two main solutions: very large reset switches or non-negligible reset time. [15] presents a new approach, alternating comparators.

The alternating approach, as illustrated in the Fig. 2.10, operates as follows. At first the first comparator makes the first decision. Meanwhile, the other comparator remains in the reset phase. Once the decision is made by the first comparator, it resets with minimum delay. Assuming the capacitive DAC voltage level updates fast enough, comparator two activates after a very short period of time. This provides the first comparator a window to reset; thus, eliminating the reset time from the critical path for the conversion cycle.

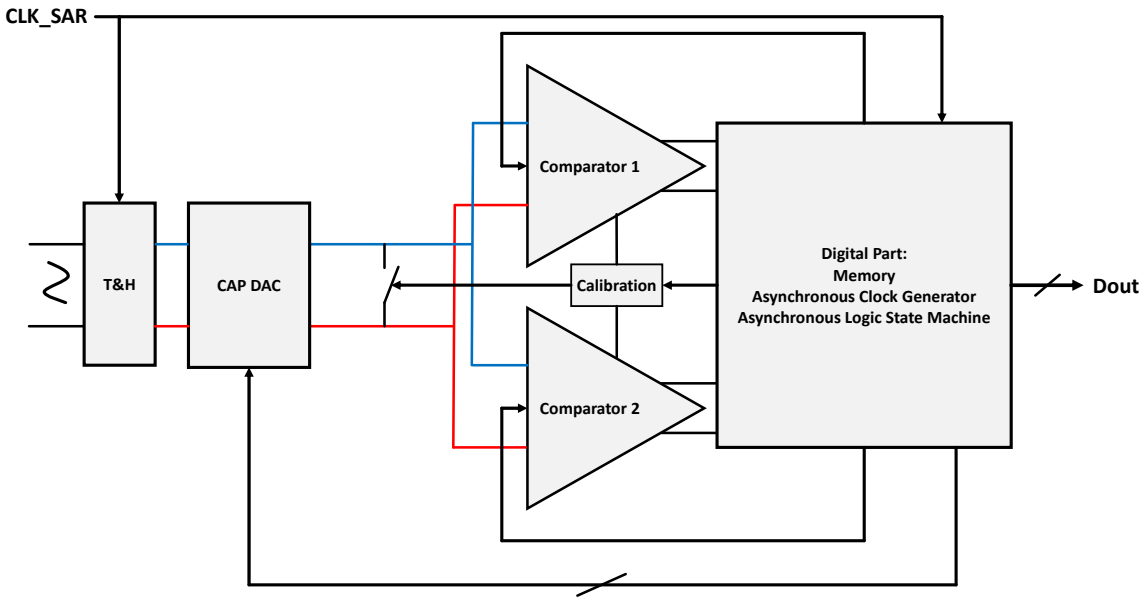


Figure 2.10: Asynchronous SAR ADC overview with alternate comparators [15]

2.2.4 Offset correction

While designing the SARADC, the key component in the block is the comparator, since it set limits on speed, decides the accuracy, and contributes to the power consuption of the SAR. Providing a high conversion speed, requiring a single clock signal, and having a single stage design, in many research applications StrongArm

Latch is chosen as the core of the designs [16].

One of the main characters of the comparator that the researchers care about is the offset of the structure. In the StrongArm Latch, two main reasons affects the offset: process missmatch and dynamic history. To compensate for both, Lucas Kull in [16] reported an offset cancellation technique.

In Kull's approach, another differential pair is paralleled to the diff-pair in the comparator. This new pair is sized smaller (5x) compared to the main pair to reduced the affect of the added pair on gain and noise performance of the comparator. The fast, low-power calibration circuit that controls the smaller sized diff-pair was reported in [17]. [16] uses the same circuitry to update the voltages of the second (smaller diff-pair). Depending on the comparator's decision, bias voltage of the smaller sized diff-pair changes. The amount of change is based on the sizes of the capacitors in the structure. In a structure with alternating comparators, the calibration is done at the end of every second cycle.

In [18], an improved version of the same circuit with a capacitive ladder is presented, Fig. 2.11. In this work, at the end of the cycle inputs are shorted and the comparator makes a decision. Voltage steps for the offset calibration are chosen to be small to increase precision and reduce algorithmic noise [18]. To achieve this, the ladder structure, shown in Fig. 2.11 is used, enabling small parasitic capacitances for switches. The structure is further improved by the charge division mechanism implemented in [18] and elaborated in Fig. 2.11.

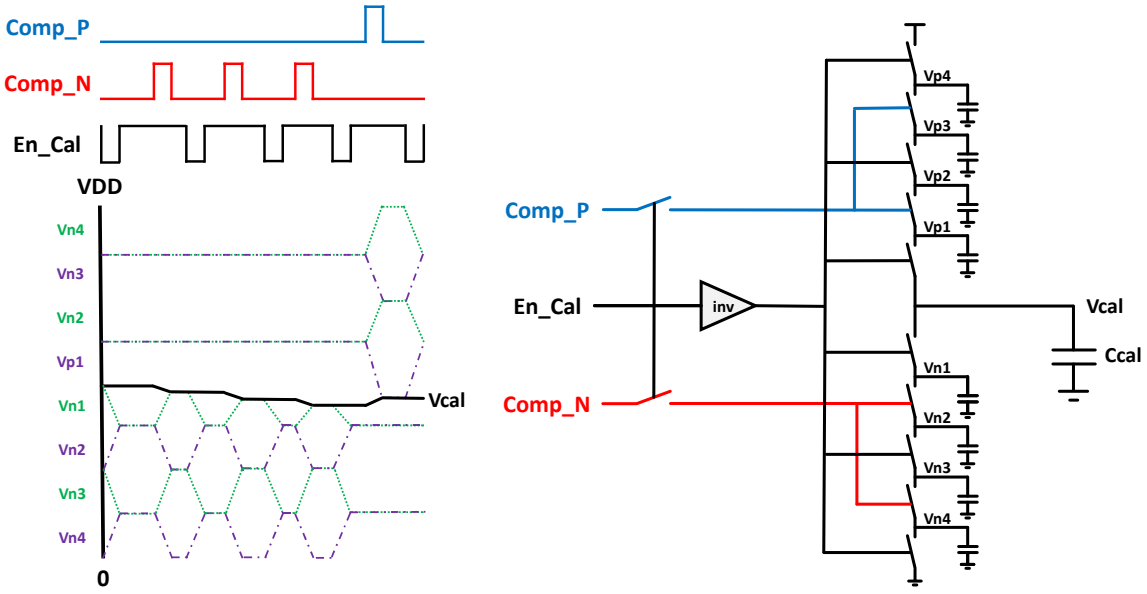


Figure 2.11: Ellaboration of the offset cancellation technique presented in [18]

2.2.5 Increasing conversion speed - Flash-SAR

Flash-SAR structure is a hybrid structure. In many applications, the hybrid structure is reported to improve the conversion speed of the overall structures. As it is a hybrid structure it can benefit from the best key aspects of the both architectures, conducting high-speed operation power efficiently.

As mentioned, Flash ADC architecture is suitable for low-resolution, high-speed operations. On the other hand, SAR is sutaible for high-resolution, low-power applications. Thus, the total resolution can be distributed between the architectures. While adopting a time-interleaved SAR structure for LSB and conducting MSB digitization with Flash, a high-speed, high-resolution ADC can be designed, enabling higher conversion speeds compared to SAR while maintaining the resolution [19].

2.2.6 Digital interpolatin

In 2020, Shovon Dey, reported digital interpolation [6]. In this technique, there are two SAR ADCs covering the same voltage ranges. The references in these ADCs are then shifted by 1-LSB. As a result, the output of these SARs are also shifted by

1-LSB. Based on the polarity of the residue error and digital output of the two SARs covering the input range, a digital block with the logic mentioned in Tab. 2.2

Residue error (Input – digital code)		Selected code	Adjustment
Top ADC	Bottom ADC		
+ve	+ve	Max{Code-Top, Code-Bot}	+1/2LSB
+ve	-ve	Code-Bot	-1/2LSB
-ve	+ve	Code-Bot	+1/2LSB
-ve	-ve	Min{Code-Top, Code-Bot}	-1/2LSB

Table 2.2: Interpolation logic published in [6]

In a probable case were the digital output of of the bottom ADC has $+ve$ residue and the top ADC has $-ve$ residue, by subtracting either 1/2LSB from the bottom ADC or adding it to the SAR ADC, interpolation is done and an extra bit of resolution is generated.

Till now all the technical improvement comes with the added complexity, power, and area consumption. In this work the main focus is to improve the power, performance, and area of the structure prior to applying any of the mentioned improvements.

2.2.7 Walden's figure of merit

A commonly accepted merit for comparing state-of-the-art ADCs is 'Walden's FoM'. [20] defines this FoM and Eq. 2.1 presents it. In this equation, ENoB is the effective number of bits, F_s is the sampling frequency, and ERBW is the effective resolution bandwidth.

$$Walden's\ FoM = \frac{Power}{2^{ENoB} * min\{F_s, ERBW\}} \tag{2.1}$$

It should be noted that the smaller the number of figure of merit means the greater the performance structure. The trend of the Walden's figure of merit (FoM) reported

in the top journals and conferences (measured-silicon and simulation measures) are presented in Fig. 2.12. The Post-layout measures of this work are compared to post-layout and silicon-measurements of previous works. The purple trend-line shows that as the frequency increases the FoM's lower limit increases. The reason behind is that power consumption and frequency are propotional to each other, however as the frequency increases the ENoB decreases for the same structure - effect of noise and distortion.

In [21], it is also mentioned that in frequencies above 500MS/s, for resolutions of 6 to 8-bits, it is very power consuming to meet the resolution and speed at the same time. Thus, the trend-line rises rapidly. Therefore, if any work is below the purple trend-line it means that the design is better, however above the line means, compared to previous works the design's performance - FoM point of view - is worse.

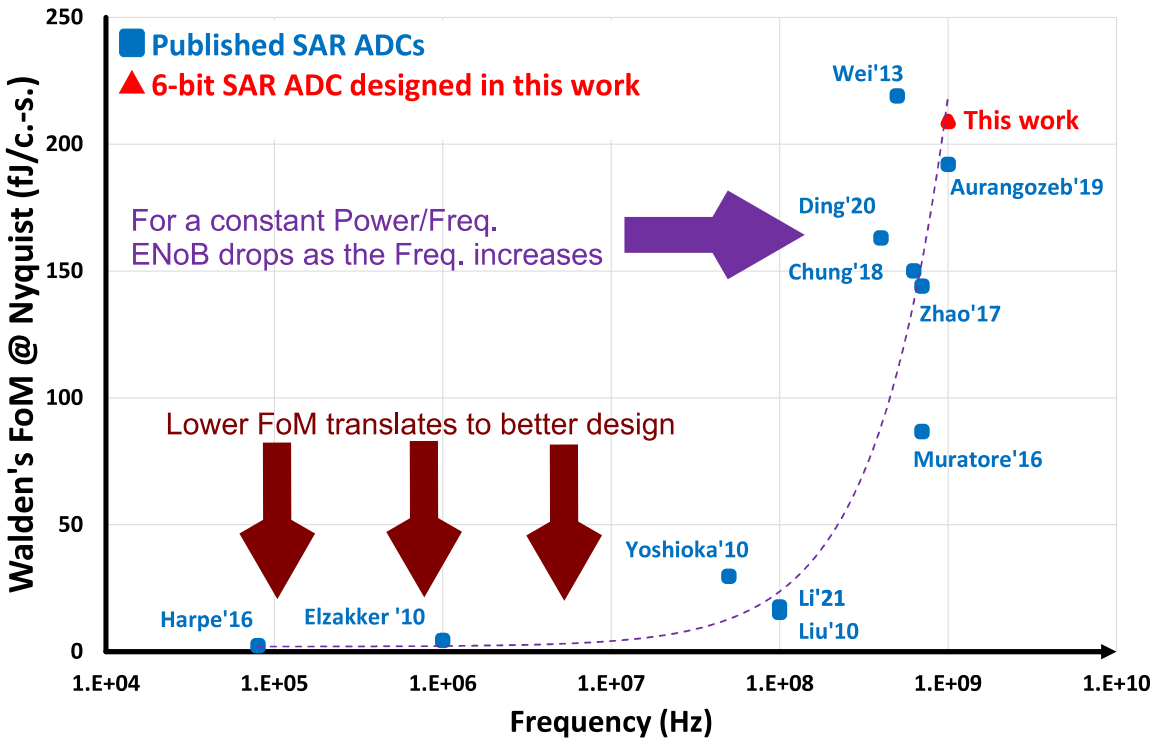


Figure 2.12: Walden FoM of the SAR ADCs published is since 2010 using 65nm (silicon-measured and post-layout measurement) and the trend line of this technology

2.3 ADC for wire-line links

To support the increase of network traffic, serial I/O link data rates have increased to 56Gb/s (28GS/s - PAM-4), 112Gb/s, and beyond [1]–[4]. As the speed rises the symbol time becomes smaller and smaller and Intersymbol interference (ISI) becomes an issue. To deal with ISI, traditionally, equalization was done in the analog domain. The scaling of the CMOS technology has caused linearity issues. Therefore, nowadays, the digitization must be conducted in the digital domain.

The simplest way to increase the speed in the links is to propagate signals is multiple wires. If more speed on a single link is required, signal can be propagated at higher speed. Yet, for frequencies above 20GHz, the channel response drops severely than when compared with lower frequencies. Therefore, higher order modulations like PAM-4 are chosen for signal propagation. With the higher modulations, the same rate of data can be sent and received at lower frequencies. As a result, signals are modulated and propagated on the links to achieve a higher SNR.

To receive a PAM-4 signal, a 2-bit ADC is required to conduct the digitization. To deal with the signal integrity issues equalization (longer equalization) must be conducted in the digital domain. Moreover, lower-speed Ethernet needs approximately 10GS/s signals. To conduct equalization in all the mentioned applications a resolution of 6-8 bits, approximately 5 Effective Number of Bits (ENoB), is required to conduct the equalization [16].

Data rates at 56Gb/s and above at advanced modulation schemes such as PAM-4 require ADC-based receivers to digitize the signal and provide the digital domain with the digitized input of 6 to 8 bits. ADC-based receivers enable digital signal processing for equalization and detection while providing robustness to PVT variations.

One of the downsides of using ADC-based receivers which enable the digital equalization is that they consume relatively more power. This fact motivates the researcher to improve the designs for energy efficient ADC with moderate resolutions. Over the

past years, many have improved the structure by utilizing the benefits extra circuitry provide, mentioned in the previous sections. In this work, we have opted a more basic approach to improve the structure. In our approach, we are optimizing the sub-blocks of the structure and therefor the overall performance.

In [22], Murmann mentions that it is not efficient to use Flash structure in resolutions higher than 5-bits. Meanwhile, time interleaved can achieve the moderate resolutions (4 to 14 bits), while providing high throughput. In the time-interleaved structure, the desired subADC should provide a high $\frac{speed}{area}$ ratio. This ensures that the overall power and area consumption is low. The best energy efficiency in medium resolution applications are provided in SAR ADCs [22]. Thus, in this work, we have decided to use a time-interleaved SAR ADC as the core block for the design.

Motivated to optimize the performance, power, and area consumption (PPA), our main focus in this work is optimizing and improving the PPA of the conventional SAR ADC. This is achieved by optimizing its blocks such as its buffer, comparator, and SAR logic. Further, by using a novel cascoded buffer which enables gain mismatch compensation in the front-end, the bandwidth of the structure was extended further while providing more linearity and room to compensate for mismatch.

In next chapter, focusing on the PPA of the SAR, the design of different blocks of a SARADC-based receiver is explained, each block is improved if possible, and afterward the improved blocks' results are compared with previous works.

Chapter 3

Designing of a SARADC-based receiver

In chapter 2, different ADC structures were briefly described. Among them, SARADC achieves outstanding area and power efficiencies (Tab. 2.1). However, the SARADC's delay and throughput are relatively higher compared to other structures. By interleaving SARADCs, one can achieve a throughput almost equal to the Flash's structure. A throughput almost equal to Flash makes TI-SARADC structure a suitable option for relatively high-speed applications where digitization delay is not the limiting factor. Since the delay is not of much importance in this work, I used SARADC as my receiver's core.

Fig. 3.1 illustrates the structure for TI-SARADC-based receivers. This work, a receiver for a quad-channel transmitter designed by another graduate student, has four input channels. The inputs, after passing channels, are attenuated and suffer from inter-symbol interference (ISI) and other signal integrity issues. At first, a front-end block employs signal equalization and amplification to compensate for channel effects. Once equalized and amplified, buffers create multi-copies of the inputs. Afterward, the SARs, clocked with clock signals with different phases generated by a clock generator, sample each of these copies and digitize it. Once the digitization is done, a serializer serializes the six digital output bits of SARs. At last, six 4-to-1 multiplexers select the output of the desired channel. Finally, buffers propagate the signals to output

drivers.

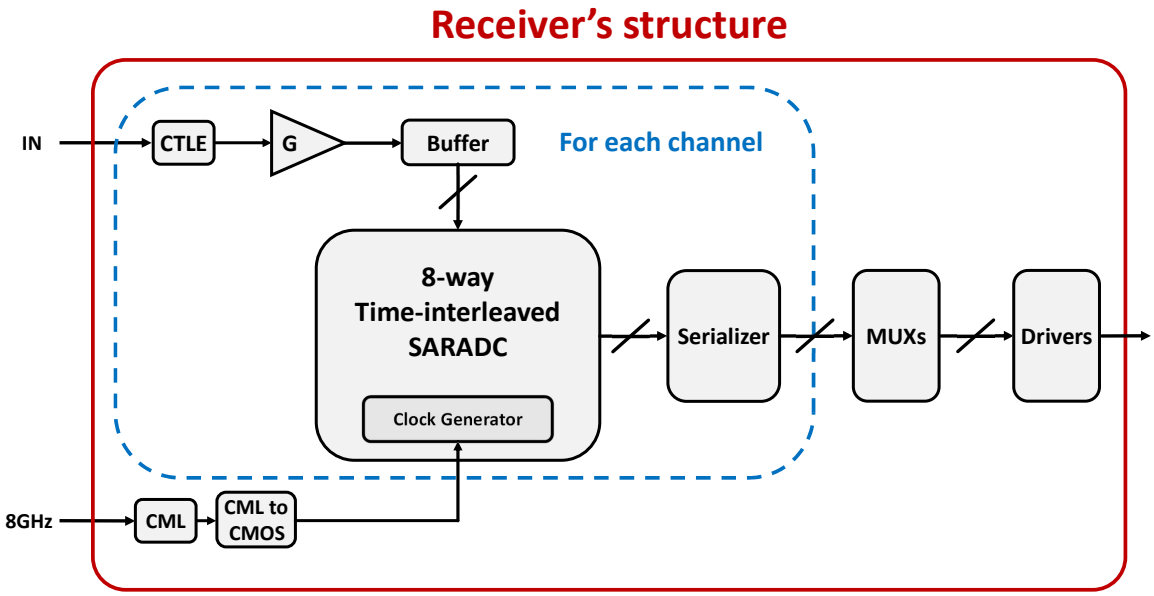


Figure 3.1: multi-channel time interleaved SARADC structure

The front end includes an equalizer to filter unwanted frequencies and an amplifier to accommodate channel loss. In addition to the equalizer and amplifier, for an 8-TI-SAR, a total of eight S/H circuits are required. The capacitance in these S/H circuits is built in a binary-weighted format to enable the binary search conducted by SARADCs. A limiting factor is paralleling all these S/H circuits, which increases the capacitance on one node. To overcome the bandwidth issue, a buffer creates eight copies of the signal and feeds the copies to the CAPDACs separately, reducing RC constant to 1/8 of what it was. After equalizing, amplifying, and generating copies, S/H block starts following the input signal with an RC constant. Once the value is close enough, capacitance can hold the input's voltage, and the SAR block can start the SAR operation.

SAR structure follows a binary search algorithm. Every time the comparator makes a decision, the comparator's reference should update. Thus, an N-bit SAR has N conversion cycles. After each decision, SAR logic updates the inputs of the comparator by controlling switches connected to the binary-weighted capacitors of

the CAPDAC. Therefore, there is a need for a digital block to generate the signals controlling CAPDAC's switches based on the comparator's output. Eight SARs, clocked with different phases, form the TI-SARADC, which samples and digitizes the input.

In this work, the structure has 4-channels. Each channel is connected to an 8-way time-interleaved SARADC, and each SAR produces six digital bits. Thus, the receiver generates 192 bits per nanosecond. Due to the limited number of pins on the IC's package, only six pin can be allocated to the digital outputs. Therefore, a serializer serializes the forty-eight $1GHz$ outputs of each channel to six $8GHz$ outputs. Then, six 4-to-1 multiplexers, using two control bits, select one of the channels and send its six output signals to the pins allocated to the outputs.

In this chapter, I will thoroughly describe the blocks and sub-blocks used in the receiver (Fig. 3.1), their operation, and limitations. Afterward, I will try to improve the performance, power consumption, and/or area consumption of the building blocks, either by proposing new structures or applying technical improvements.

3.1 Front-end

The input signal passes a lossy transmission line (Fig. 3.3); therefore suffers from attenuation, Inter-Symbol Interference (ISI), and other signal integrity issues. At first, to reduce reflection, all channels are terminated with 50 Ohm resistors. The other terminals of termination resistors are connected to one decoupling capacitor to extract inputs' common-mode voltage for future use. Afterward, signal equalization is employed to extend the bandwidth of channels, enabling high-speed operation. Afterward, amplifiers amplify inputs to accommodate the channel's loss. Finally, buffers generate copies of the modified signals for SARADCs' S/H circuits. Fig. 3.2 illustrates front-end's structure up to the buffers.

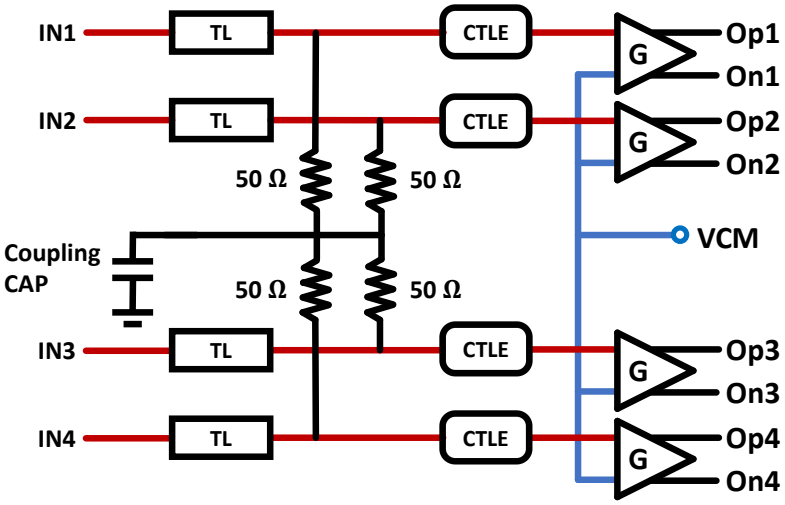


Figure 3.2: Front-end structure before buffering

3.1.1 Equalizer

To counter channel effects (mainly Inter-Symbol Interference), a passive Continuous-Time Linear Equalizer (CTLE) was used after each terminated channel. CTLE is a typical equalizer structure (Fig. 3.5b) used by many applications in receivers. Compared to other equalizers, CTLE configuration has some pros and cons. Pros of this structure are lower power consumption, small sizing, and canceling precursor and Inter-Symbol Interference. However, this structure is hard to tune, does not improve SNR, and crosstalk remains an issue. To expand tuning room of the configuration, one can parallel more switch-resistor branches.

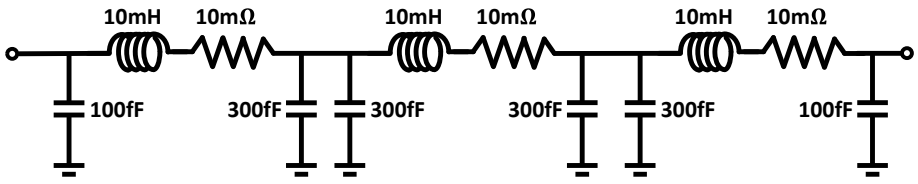


Figure 3.3: Transmission Line's model

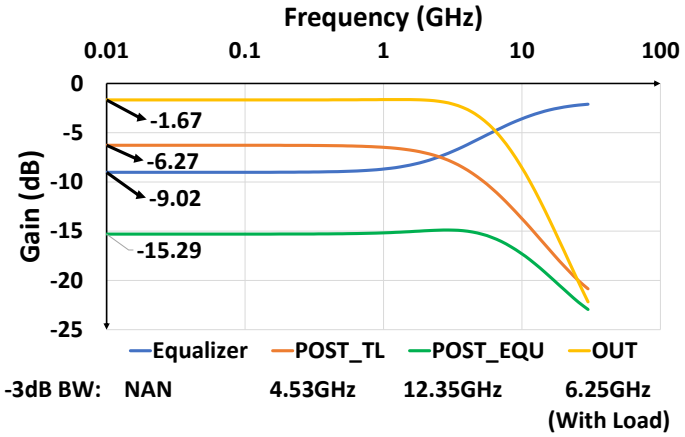
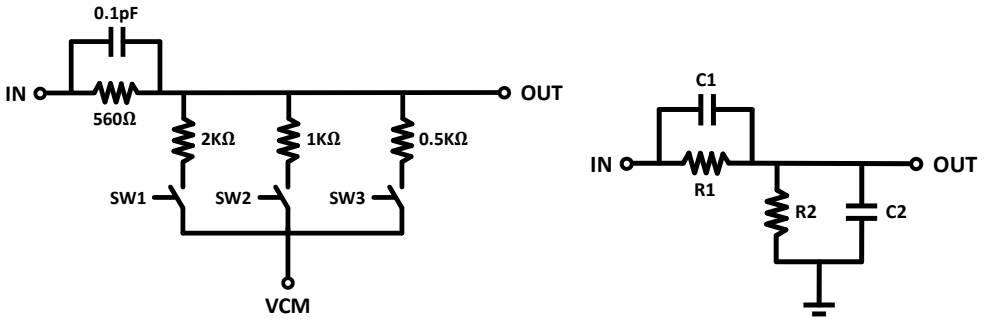


Figure 3.4: Transmission Line, CTLE, and amplifier Frequency response - load is assumed to be 50fF

Fig. 3.3 illustrates the transmission lines model, and the frequency response of the channel is presented in Fig. 3.4. Up to 1GHz, the channel has a gain almost equal to -6.27dB. After 1GHz, the channel's gain starts to drop. -3dB bandwidth of the transmission line model is 4.53GHz. However, the TI-SARADC structure is designed to sample at 8GHz. Input frequencies, at least up to Nyquist frequency, should pass the transmission line, equalizer, and the amplifier with as little distortion and change in frequency response as possible, . Having a higher bandwidth allows more harmonics to pass, and having more harmonics available without attenuation will result in better performance. Thus, it is desired to have higher post-equalization bandwidth. Therefore, equalizer should be designed according to the channel's response, so that their combined frequency response is flattened up to the highest possible frequency.



(a) (b)

Figure 3.5: a)CTLE structure b) CTLE equivalent model

Fig. 3.5a illustrates the passive CTLE used in this work. In the structure, there is a hidden impedance (mainly capacitive), the input impedance of the next block. The input impedance can be simplified to a capacitor ($C2$). Therefore, the CTLE model is simplified into two parallel RC tanks in series. The input signal enters from one end, while the other end is ac ground, and the output is collocated from the middle node. Eq. 3.1.1 describes the transfer function of the equalizer. Based on the transfer function, the values for components were chosen. By applying the CTLE, the post-equalization frequency response is almost flat up to 12.35GHz. Fig. 3.4 illustrates the post-channel, pre-equalization bandwidth, and post-equalization bandwidth. There is a meaningful, desired boost in -3dB BW between post-channel and post-equalization frequency responses, from 4.53GHz to 12.35GHz; however, the gain drops significantly.

$$
\begin{aligned}
\mathbf{H(s)} &= \frac{R_2}{R_1+R_2}\frac{1+R_1C_1S}{1+\frac{R_1R_2}{R_1+R_2}(C_1+C_2)S} \\
\omega_z &= \frac{1}{R_1C_1}, \quad \omega_p = \frac{1}{\frac{R_1R_2}{R_1+R_2}(C_1+C_2)} \\
\mathbf{DC\ gain} &= \frac{R_2}{R_1+R_2}, \quad \mathbf{HF\ gain} = \frac{C_1}{C_1+C_2} \\
\mathbf{Peaking} &= \frac{\mathbf{HF\ gain}}{\mathbf{DC\ gain}} = \frac{\omega_p}{\omega_z} = \frac{R_1+R_2}{R_2}\frac{C_1}{C_1+C_2}
\end{aligned}
\tag{3.1}
$$

3.1.2 Amplifier

After passive equalization and extracting the common-mode voltage of input, an amplifier amplifies each of the input signals to accommodate some of the loss. The amplifier can be a simple diff-pair, one of the inputs of the diff-pair is the signal coming from the equalizer, and the other is the common-mode voltage of the inputs. The two outputs of the diff-pair are connected to the buffer. Fig. 3.6 illustrates the output of the diff-pair for a sinusoidal input with common-mode voltage and peak-to-peak range equal to the transmitter outputs. The bandwidth and frequency response of the diff-pair (loaded) is illustrated in Fig. 3.4. In future works, the passive equalizer and diff-pair can be substituted by an active equalizer.

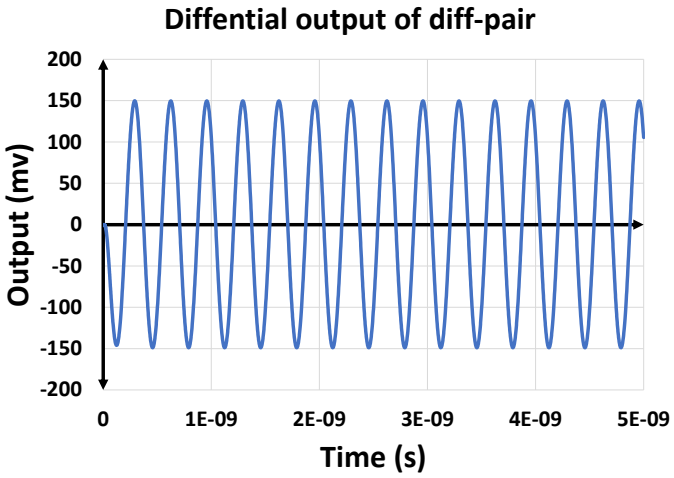


Figure 3.6: Transient output of the diff-pair after transmission line, CTLE, and amplifier

3.1.3 Multi-Branch Cascoded Buffer with proposed gain compensation

In an 8-TI ADC, there are eight CAPDACs. The bandwidth of the structure will be limited if all of the CAPDACs are connected to one node. To extend the bandwidth of the structure, a buffer can generate copies of the signal and feed them to CAPDACs separately.

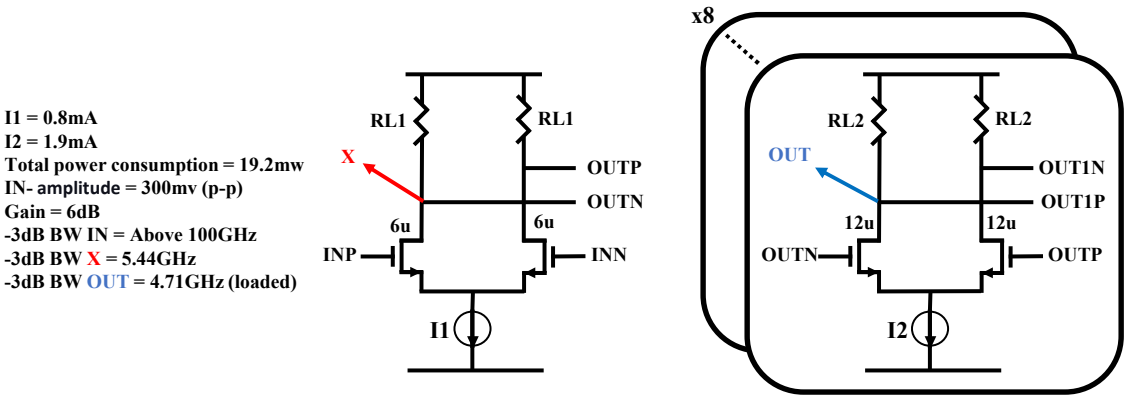


Figure 3.7: Conventional Buffer

Traditionally, two-stage amplifiers are used to create amplified copies of the signal. Fig. 3.7 illustrates the structure of the conventional buffer. The traditional buffer structure has three main poles: a) Input pole, b)Output pole, and c) Node X's pole. We have little control over the input pole and the output pole. One is related to the size of the CAPDAC, and the other is related to the impedance of the previous block. The limiting pole in this structure is the pole of node X, which is related to the output resistance of the first stage and the summation of all capacitance sources of the node. Approximately, node X's pole is equal to $NR_{O1}C_{GS2}$. However, as the number of stages grows, node X's pole moves to lower frequencies and limits the system's performance.

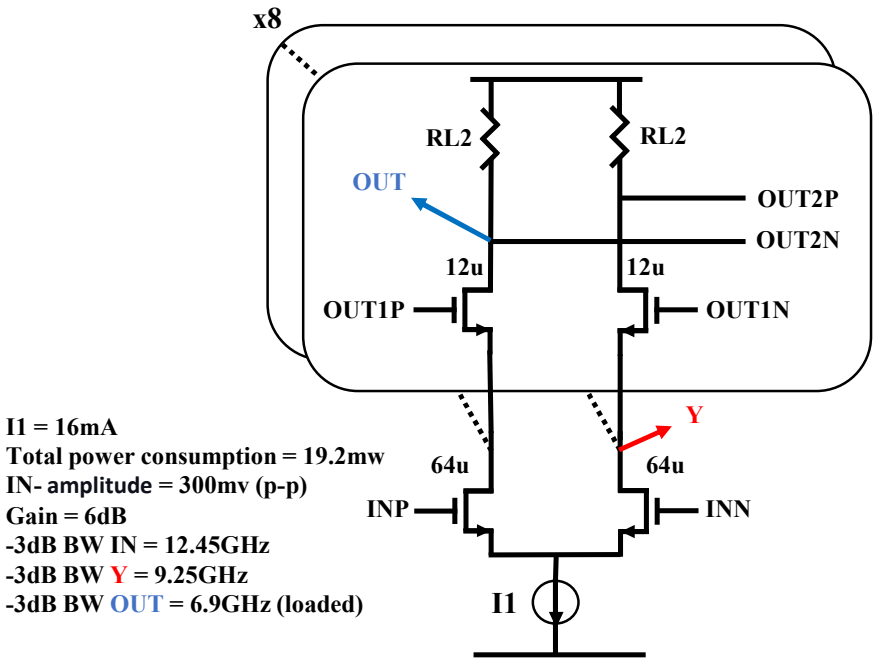
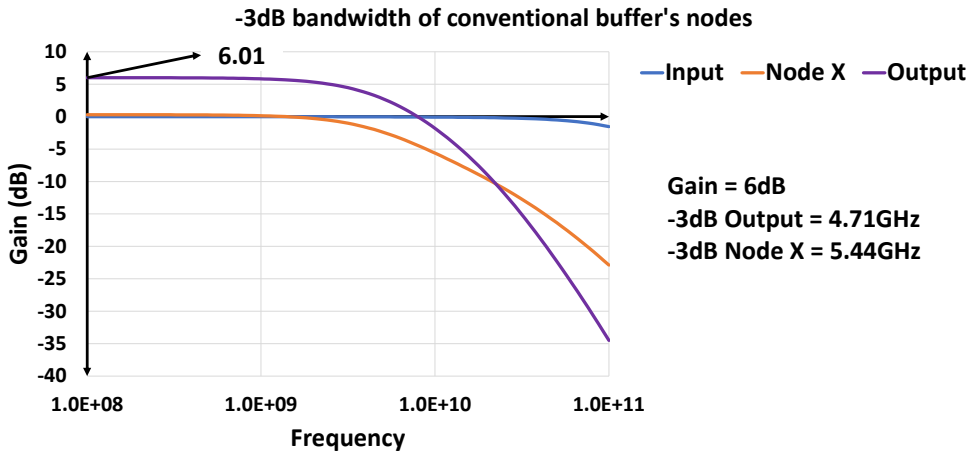


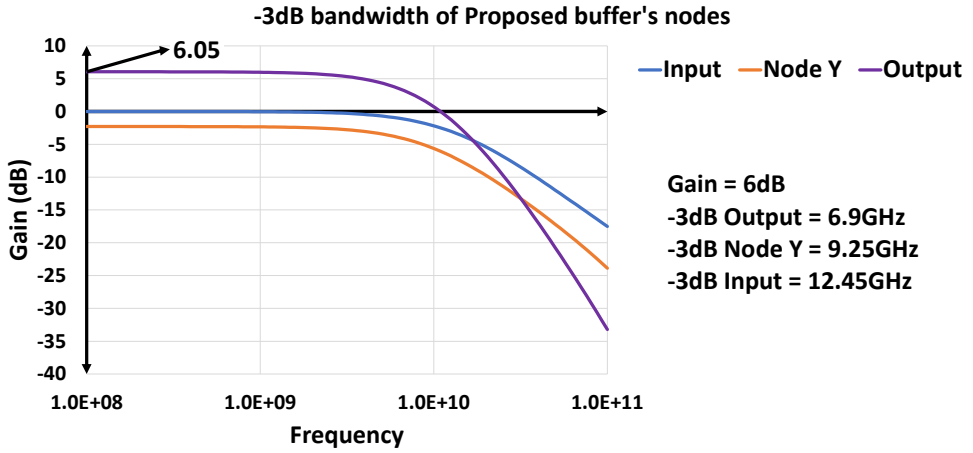
Figure 3.8: cascoded Buffer

Based on Fig. 3.9a results, the pole at node X is limiting the bandwidth. To fix this issue a new buffer is presented. The cascoded buffer (Fig 3.8) also has three poles: a) Input pole, b)Output pole, and c) Node Y's pole. The pole of node Y (Eq. 3.2) is at a much higher frequency. Thus, the structure has two main poles, the input pole and the output pole. Frequency responses of each of the nodes in the cascoded buffer, demonstrated in Fig. 3.9b, shows a 46.5% improvement in output's -3dB bandwidth compared to the conventional structure.

$$
\begin{aligned}
R_{eq} &= r_{o_{M0}} || \frac{1}{g_{m_1}} || ... || \frac{1}{g_{m_N}} \approx \frac{1}{N g_m}, \\
C_{eq} &= C_{dd_{M0}} + C_{GS_1} + ... + C_{GS_N} \approx N C_{GS}, \\
P_Y &= \frac{1}{R_{eq} C_{eq}} \approx \frac{g_m}{C_{GS}}
\end{aligned}
\tag{3.2}
$$



(a)



(b)

Figure 3.9: a)-3dB bandwidth of conventional buffer nodes b) -3dB bandwidth of proposed cascoded buffer nodes

Comparison between cascoded buffer and conventional buffer

Up to this point, I showed that the cascoded buffer has a much higher -3dB bandwidth for equal gain and power consumption. The bandwidth improved from 4.71GHz (traditional buffer) to 6.9GHz (cascoded buffer).

Comparing the cascoded structure (Fig 3.8) and conventional structures (Fig 3.7), it is clear that the number of components (resisters and MOSFETs) is lower in the cascoded buffer, suggesting lower area consumption. Moreover, the cascoded structure only contains one current tail, contributing to less area and power consumption.

In addition to the previous pros, the cascoded buffer has a much better linearity compared to cascaded diff-pairs, the conventional structure. As the third-order intermodulation product of a cascaded topology is worse than a single stage [23]. Simulation results shown in Fig. 3.10.

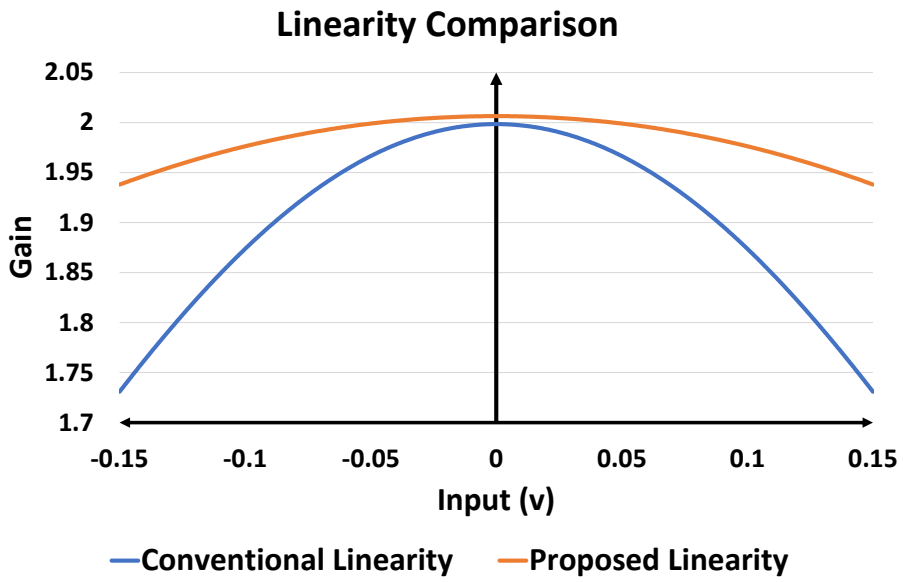


Figure 3.10: Linearity comparison between conventional and proposed cascoded buffer

By controlling and increasing the tail current of the cascoded buffer, a gain equal to 1.97 ± 0.03 was achieved for the cascoded structure. The change in gain translates to 1.5% non-linearity, which is much better than the conventional configuration (8.5%).

Having common-gate transistors in the structure provides more room for improvement. A typical method is to implement a common-mode feedback to equalize the common-mode voltages of the branches. However, an important issue that the designers face is the gain mismatch between the branches. To compensate the mismatch, the voltages of the common-gate transistors can be biased. Therefore, in this project, we suggested using the common-gate biasing voltages to compensate for the inherent gain mismatch and obtain identical gains in the branches.

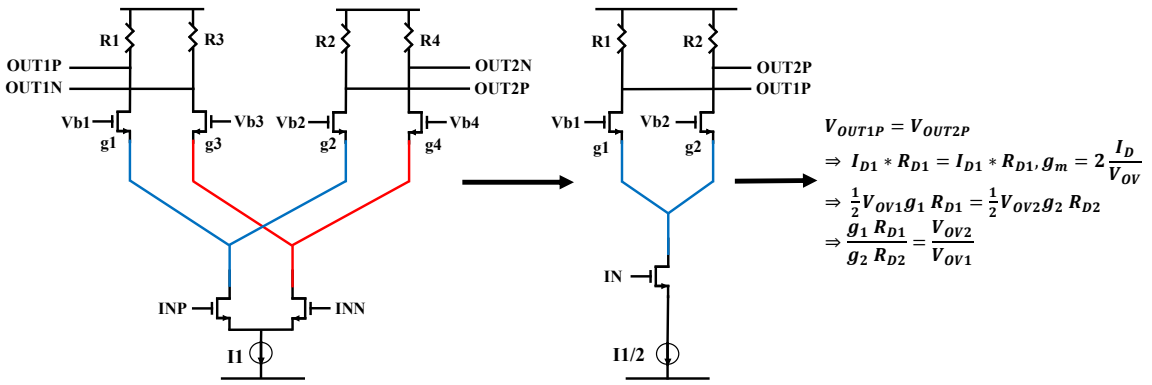
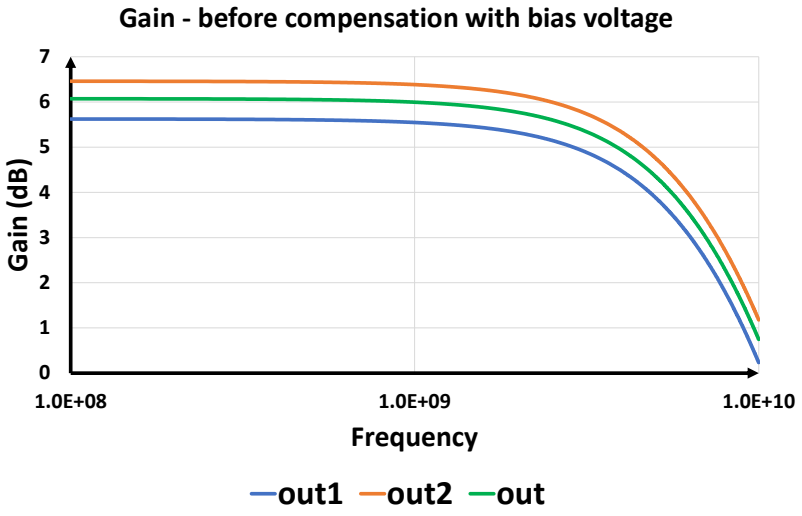


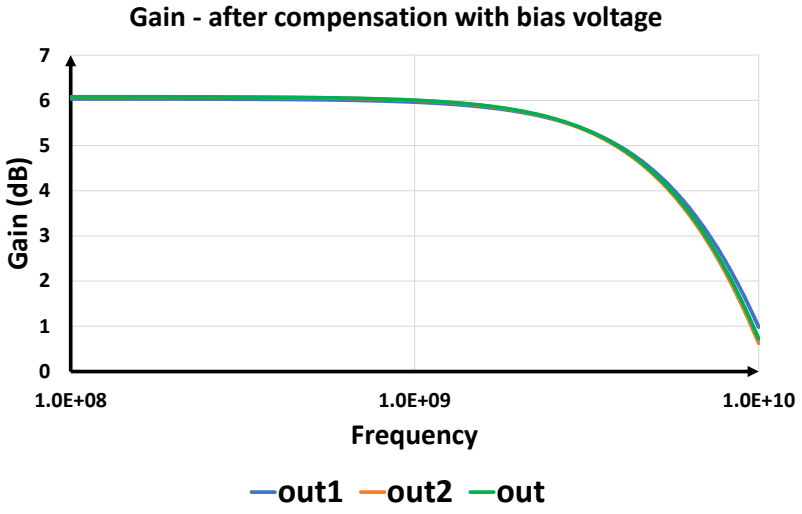
Figure 3.11: gain mismatch correction concept

Fig. 3.11 shows a simplified version of the cascoded buffer with two branches (the half circuit of the structure is shown). The output voltages in the branches are equal to $I_{d(i)} * R_{D(i)}$. Replacing $I_{d(i)}$ with $\frac{1}{2} * g_{m(i)} * V_{OV(i)}$, gain is equal $\frac{1}{2}V_{OV(i)} * g_{m(i)} * R_{D(i)}$. In the equation for the gain, V_{OV} is the only term that can be modified after implementation. Increasing the gate voltages of the common-gate transistor, the gain of its branch increases respective to other branches, and vice versa.

To represent a potential mismatch, in the simulation, we changed the width of one branch to one micron less (11 micron), and in another one one micron more (13 micron) than the other branches. The Fig. 3.12a shows pre-correction gain and Fig. 3.12b shows post-correction gain. Comparing simulation results in the Fig. 3.12a and Fig. 3.12b shows almost ideal compensation for potential inherent mismatch of the circuit.



(a)



(b)

Figure 3.12: a)gain mismatch without controlling biasing voltages b)gain mismatch with controlling biasing voltages

3.2 Optimizing the SARADC

Fig. 3.13 illustrates the structure of the SARADC. The main blocks are the CAP-DACs, Comparator, Asynchronous Clock Generator, Digital Control Block, and D-flip-flops (DFFs) to save the digital code. The main signals are Inputs, Refrences, Comparator's clock, Status signals, Reset signal, and SAR's Clock (CLK_SAR).

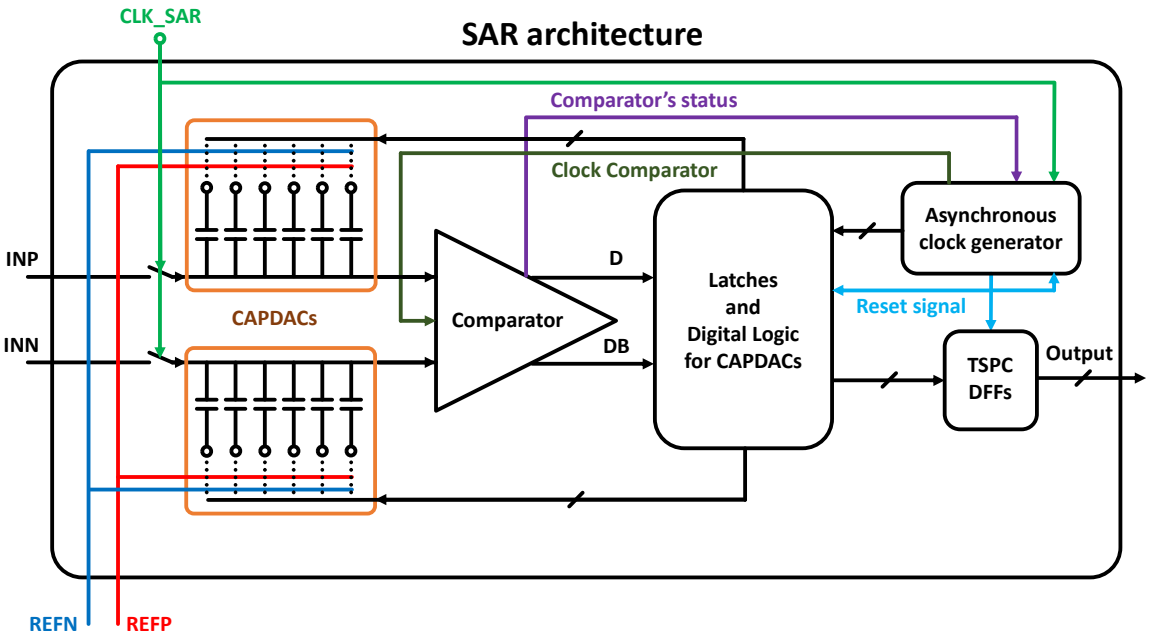


Figure 3.13: SARADC's architecture

In the SARADC, once the copies of input signals are created, the CAPDACs' switch turns on, and the voltages on the CAPDACs start tracking the input signal. Based on the *RC* constant, the voltage of the Switch-CAP goes toward the input voltage. Once the voltage of the switch-CAP is within a tolerable range of the input voltage, the switch turns off. Afterward, the binary search starts. To generate the digital output code, a comparator compares the input with the reference and generates a digital bit each cycle, and saves it in a latch. Then, a digital block updates the input/reference for the next conversion cycle based on the comparator's output. In addition, another block generates the clock of the comparator (asynchronous clock generator). When the decision is made, the clock resets the comparator. Then, the next cycle starts.

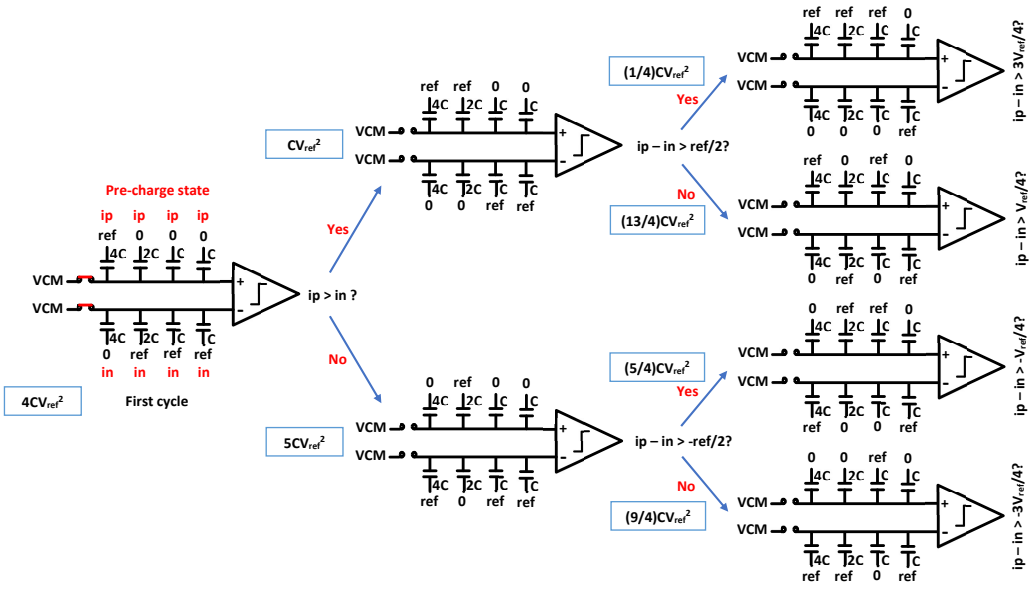
Once the decision of the last cycle is made, DFFs save the digital outputs of each cycle, and the process repeats.

In this section, we explain the function of the blocks, their limitations, and the modifications that have been made in our design. Afterward, the timing breakdown of the crucial signals are described. The system-level design of the SAR, especially the timing breakdown of the blocks, is also discussed in this section.

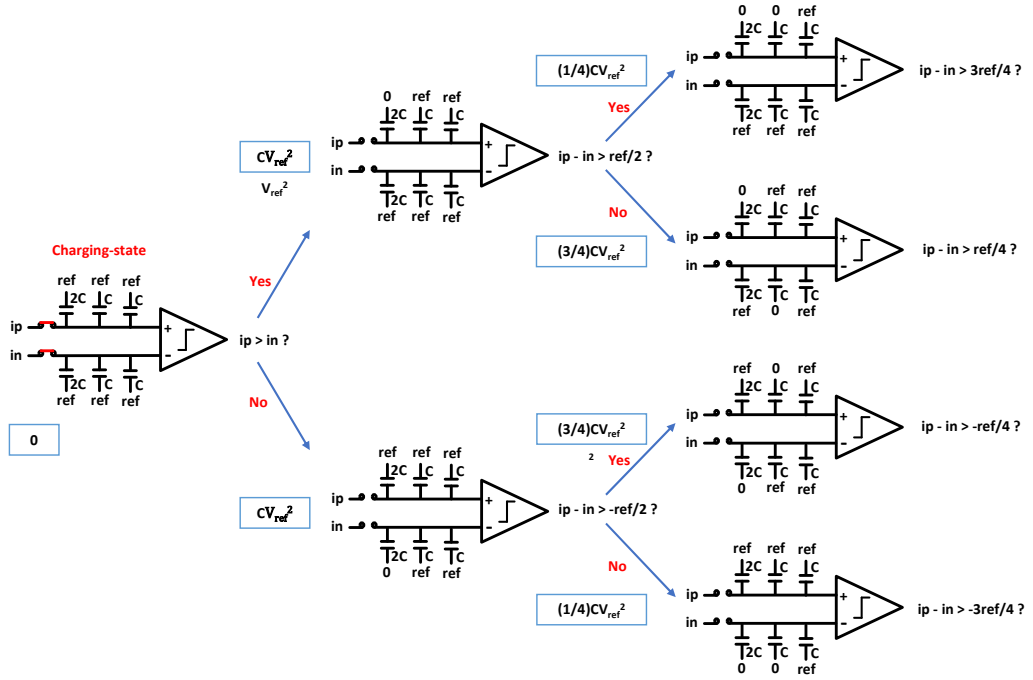
3.2.1 CAPDAC

The first block in the SARADC structure is the CAPDAC. This block tracks inputs in the sampling phase. Once close enough, the sampling switches turn off, and the CAPDAC goes to the holding mode. when the voltage is held, the SAR operation (binary search) begins. Since SAR conducts a binary search, the CAPDAC's structure is built in a binary format.

In our simulations, we used the monotonic switching procedure [13]. This procedure was first introduced by Chun-Cheng Liu, Soon-Jyh Chang, Ying-Zu Lin, and Guan-Ying Huang. In their design they replaced the conventional switching procedure (Fig. 3.14a) with the monotonic procedure (Fig. 3.14b). By using the monotonic procedure, they improved the switching power, reduced the number of switches, and reduced the number of capacitors. Tab. 3.1 compares the normalized power consumption, number of switches needed, number of capacitors, and number of unit capacitors in each capacitor array for conventional and monotonic switching procedures.



(a)



(b) Monotonic Switching Procedure

Figure 3.14: a)Conventional Switching Procedure b)Monotonic Switching Procedure [13]

There are three ways to improve the monotonic procedure further. Fig. 3.15 illustrates an improved version of the monotonic switching procedure. First, to reduce the area and power consumption of the CAPDAC, one can reduce the size of the unit

CAP. The total capacitance decreases and results in both saving area and power. Another way to improve the structure is to get rid of one of the unit CAPs colored gray in Fig. 3.15. Thus, the total capacitance decreases, and less power is consumed. Finally, instead of reducing the voltages on the other ends of CAPs from V_{ref} to 0, done in both [13] and [6], the voltage levels are increased from $ref-$ to $ref+$. Increasing voltages raises the gate voltage of the diff-pair in the comparator. Higher voltages in gates of the comparator described in [24] and used in this work enables the comparator to make decisions at a higher speed.

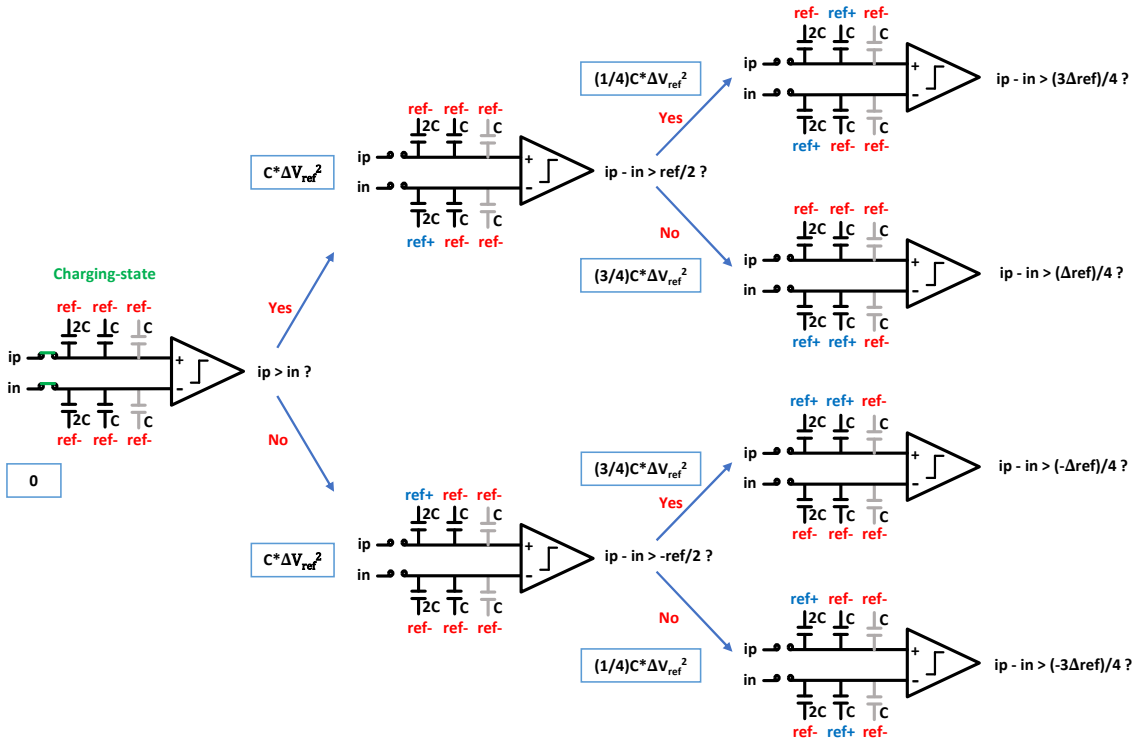


Figure 3.15: Improved Monotonic Switching Procedure

Table 3.1: Comparison of Switching Procedures

Switching Procedure	Normalized Switching Power	No. of Switches	No. of Capacitors	No. of Unit Capacitors in each Array
Conventional	1	$4N+10$	$2N+2$	2^N
Monotonic Switching(Improved)	<0.19	$4N-4$	$2N-2$	$2^{N-1}-2$

The layout of the CAPDAC structure can improve its linearity further. In [13],

sandwich capacitors are introduced. These capacitors have unbalanced parasitic capacitances on their terminals. The outer terminal has considerable parasitics, while the inner terminal of the sandwich structure has almost no parasitics (Fig. 3.16a), which makes the structure a perfect option for Improved monotonic procedure. By reducing the parasitics at 'IP' and 'IN' nodes (Fig 3.15), the capacitance seen at the output of the buffer stage decreases. Thus, the -3dB bandwidth of the buffer structure increases.

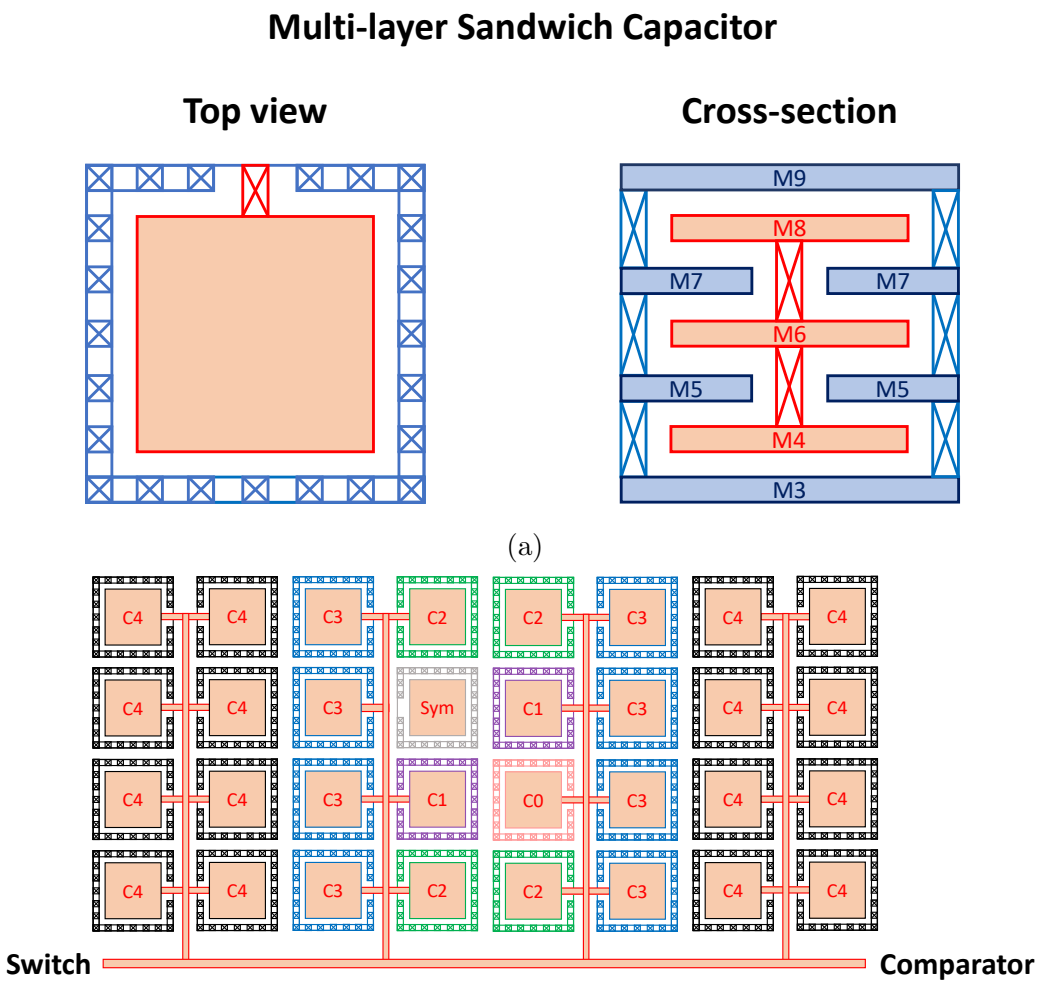


Figure 3.16: a)Sandwich capacitors Structure b)CAPDAC structure

Any mismatch or non-linearity in the capacitances causes the SAR to have worse DNL and/or INL. Therefore, the placement of the unit caps should be as close as

possible, and one can use more than the minimum area to reduce mismatch. Also, the connection of the unit caps should be as it is shown in Fig. 3.16b to ensure better linearity and matching between capacitors after fabrication.

In each cycle, after the decision is made, the digital block updates the voltages of nodes 'IP' and 'IN'. It will take time for nodes 'IP' and 'IN' to settle down, and the settling time is proportional to the RC constant of the nodes. All the binary-weighed capacitors are connected to the the reference voltages $(ref+, ref-)$. The R is the RC constant is the resistance of the switch connected to the capacitor. Every cycle, based on the output of the comparator, one capacitor changes its state from $ref-$ to $ref+$. The worst case to switch to $ref+$ happens at the end of first cycle when the biggest capacitor is changing its state. To reach an acceptable accuracy in this case, the capacitors must update the reference before the rising-edge of the comparator clock, ensuring that the input voltages of the comparator are settled before triggering the comparator. Conrolling the size of the switch, once can control its resistance, thus the RC constant of the switching process. Eq. 3.3 illustrates the math.

$$\begin{aligned} accuracy &= e^{-\frac{t_d}{\tau_5}}, \quad \tau_5 = 2^4 * C_{unit} * R_5, \\ t_d &= -2^4 * C_{unit} * R_5 * ln(accuracy), \\ Example: \quad & t_d \approx 14ps \quad for \quad C_u = 2.5fF,\ R = 50\Omega,\ accuracy = 0.1\% = 0.3v \\ Example: \quad & R \approx 125\Omega \quad for \quad C_u = 2.5fF,\ t_d = 50ps,\ accuracy = 0.01v \end{aligned} \tag{3.3}$$

In the example, the switches' resistance should be equal to or less than 50Ω. To meet 50Ω resistance, switches connected to $ref+$ should be wide enough. Assuming that the response time of the switches is 6ps and, based on rough calculations, the settling time of nodes 'IP' and 'IN' is 14ps, the comparator clock should rise at least 20ps after the signals controlling CAPDAC's switches change. On the other hand, the resistance of the switches connected to $ref-$ can be much higher. These switches operate when the SAR is in the sampling time (125ps). They have more than 50ps

to settle down. Therefore, their resistance can be as high as 125Ω.

Based on calculations, simulations 3.17, and leaving some room for parasitics and PVT effects, NMOS widths were fixed to 4um and PMOS widths were fixed to 26um. The equivalent resistance of these sizes are 123.5Ω for NMOS and 29Ω for PMOS switch when $REF+$ is $950mv$ and $REF-$ is $550mv$.

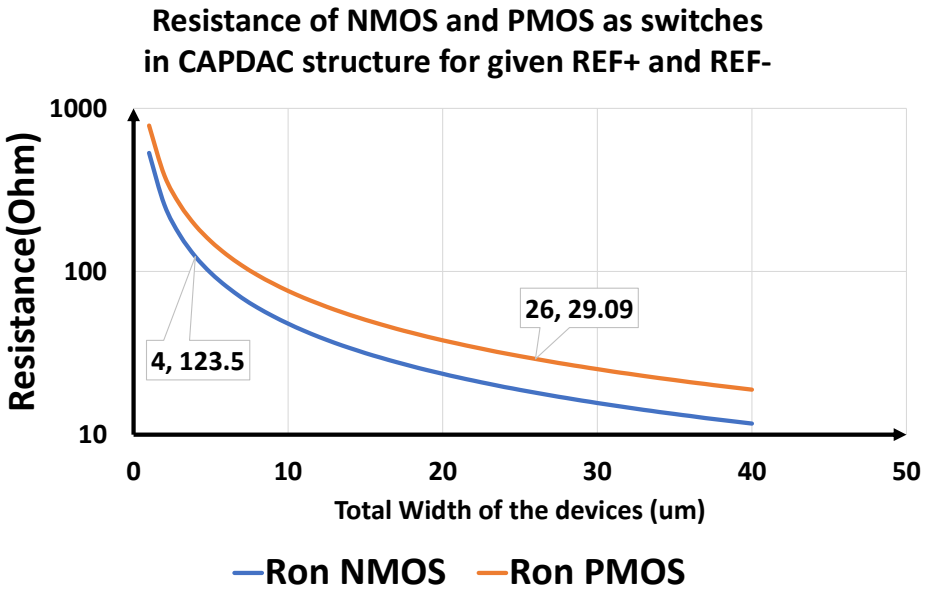


Figure 3.17: Simulating MOS resistance for NMOS and PMOS

3.2.2 Comparator

Analog to digital converters require comparators to quantize or, in some cases, sample their input signals. In our work, the core of the comparator was chosen to be a StrongArm Latch based on [24]. The target speed of the comparator is six conversion cycles in $1ns$ ($6GHz$). Usually, in SARADCs, CAPDACs and digital blocks, not the comparator, occupy the majority of area. However, gain and power consumption of the SAR can be significantly improved by optimizing the comparator.

Fig. 3.18 shows the structure of StrongArm latch [25]. The structure consists of a clocked differential pair, two cross-coupled inverters, and four precharge switches. Comparator provides rail-to-rail outputs at nodes X and Y, based on the polarity of the input (fig. 3.18). As shown in fig. 3.18, the sources of the NMOSs of the inverters

are connected to diff pairs drains, and the switches are connected to the gates of back-to-back inverters (nodes X and Y) and the drains of diff-pair (nodes P and Q).

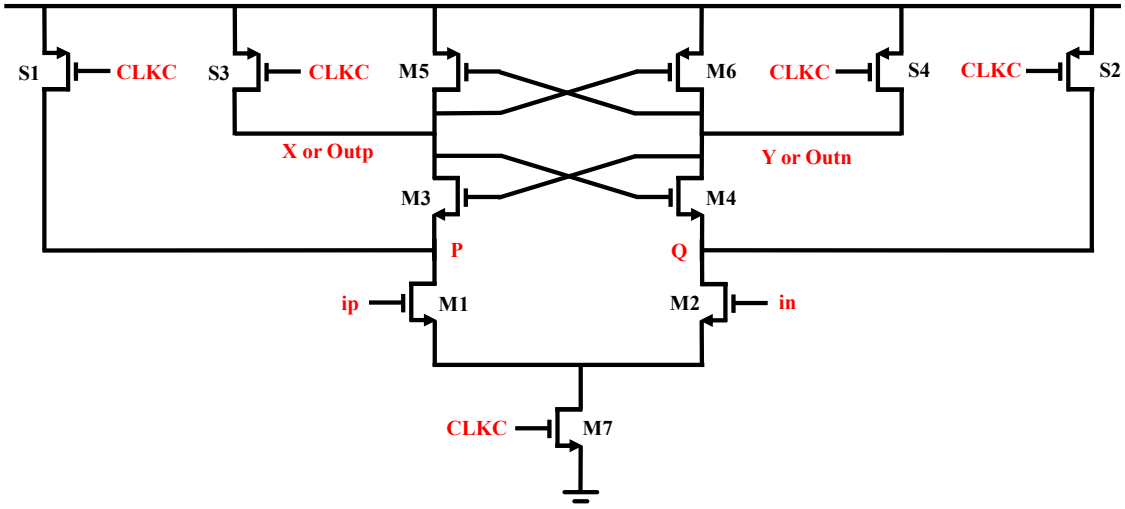


Figure 3.18: The structure of comparator

At first, the switches precharge nodes X, Y, P, and Q to VDD. In this phase known as precharge phase, the clock signal (CLKC) is low. The diff-pair is off, ensuring no static power path while the switches are on. The resistance of the switches should be small enough to precharge the nodes to VDD almost perfectly. If not, the voltage difference between P and Q nodes at the end of the phase (dynamic offset) translates to some input offset affecting the performance of the comparator. On the other hand, increasing the sizes of the switches increasex the capacitances on P, Q, X, and Y nodes, making the conversion speed slower. Therefore, they should be as small as possible, at the same time big enough to handle dynamic offset.

In the next phase, CLKC (comparator's clock) rises, turning off the switches and triggering the diff-pair. In the beginning, P and Q nodes are still precharged to VDD; therefore, back-to-back inverters are off. Based on inputs, voltages on nodes P and Q start to fall from VDD. The difference of voltages on P and Q is proportional to the difference in comparator inputs. The voltages of these nodes continue to fall to roughly $V_{DD} - V_{TH3,4}$. When either P or Q nodes' voltage reaches $V_{DD} - V_{TH3,4}$.

Then, the cross-coupled pair turns on and either X or Y's voltage becomes low (third phase). Assuming $V_{ip} \approx V_{in}$, amplification phase lasts for $\frac{2*C_{P,Q}}{I_{ss}} * V_{TH3,4}$. Assuming $C_P = C_Q = C_{P,Q}$ and current tail being constant during this phase, $|V_P - V_Q| \approx \frac{g_{m1,2}*|V_{ip}-V_{in}|}{C_{P,Q}} * t$. This phase is the amplification phase since it provides a voltage gain approximately equal to Eq. 4.3. [24][25].

$$Gain = \left| \frac{V_P - V_Q}{V_{ip} - V_{in}} \right| \approx \frac{2 * g_{1,2} * V_{TH3,4}}{I_{ss}} \approx \frac{2 * V_{TH3,4}}{V_{OV}} \tag{3.4}$$

These equations illustrate the trade-off between speed and gain (accuracy) of the comparator. To reach a higher speed, $C_{P,Q}$ has to be lower, and I_{SS} should be higher. In addition, having small V_{TH} for M3 and M4 help to reduce the duration of the amplification phase. However, reducing the $V_{TH3,4}$ results in lower gain, and accordingly reduces accuracy and performance. Also, increasing I_{SS}, devices require a bigger V_{OV}, resulting in lower gain, accuracy, and performance. To summarize, equations for delay, speed, and gain are rewritten in details in equations 3.5, 3.6, and 3.7.

$$Delay = \frac{V_{TH_{M_{3,4}}} * \left(C_{dd_{M1,2}\left(\frac{W}{L}\right)} + C_{dd_{S1,2}} + C_{ss_{M3,4}} \right)}{\frac{I_{SS}}{2}} \tag{3.5}$$

$$Speed = \frac{\frac{I_{SS}}{2}}{V_{TH_{M_{3,4}}} * \left(C_{dd_{M1,2}\left(\frac{W}{L}\right)} + C_{dd_{S_{1,2}}} + C_{ss_{M3,4}} \right)} \tag{3.6}$$

$$Gain = \frac{2 * V_{TH3,4}}{V_{GS} - V_{TH}} = \frac{g_{1,2} * V_{TH3,4}}{\frac{I_{SS}}{2}} \tag{3.7}$$

$$Gain * Speed = \frac{g_{m_{M1,2}}}{C_{dd_{M1,2}\left(\frac{W}{L}\right)} + C_{dd_{S_{1,2}}} + C_{ss_{M3,4}}} = \frac{\sqrt{\frac{K'_n * I_{SS}}{L}} * \sqrt{W}}{C_{dd_{M1,2}\left(\frac{W}{L}\right)} + C_{dd_{S_{1,2}}} + C_{ss_{M3,4}}} \tag{3.8}$$

$$\frac{d\left(Gain * Speed\right)}{dW} = \frac{A * (C - B * W)}{2 * \sqrt{W} * (B * W + C)^2}, \quad where:$$

$$A = \sqrt{\frac{K'_n * I_{SS}}{L}}$$

$$B = C_{OV},$$

$$C = C_{dd_{S_{1,2}}} + C_{ss_{M3,4}},$$

$$\frac{d\left(Gain * Speed\right)}{dW} = 0 \quad \Rightarrow \quad W_{opt} = \frac{C}{B}$$

$$W_{opt} = \frac{C_{dd_{S_{1,2}}} + C_{ss_{M3,4}}}{C_{OV}} \Rightarrow \tag{3.9}$$

$$C_{dd_{M_{1,2}}} = C_{dd_{S_{1,2}}} + C_{ss_{M3,4}} + C_{P_{parsitic}} \tag{3.10}$$

In this work, to optimize the gain, speed, and performance of the comparator, based on the equations, we are trying to reach an optimal value for the sizes of the devices. Assuming a constant I_{SS}, gain-speed product can be calculated as a function of the width of the diff-pair transistors, Eq. 3.8. To optimize the gain-speed product, its derivative must be zero. To reach to a condition when $C_{dd_{M_{1,2}}} = C_{dd_{S_{1,2}}} + C_{ss_{M3,4}} + C_{P_{parsitic}}$.

Power consumption is another aspect that has been optimized in this work. Behzad Razavi in [24] calculated the power consumption of StrongArm latch to be $2 * f_{CLKC} * C_P * V_{DD}^2 + f_{CLKC} * C_X * V_{DD}^2 + f_{CLKC} * C_{CLKC} * V_{DD}^2$, where C_{CLKC} is the gate capacitance of all switches and the tail device. In our calculations, we used Behzad

Razavi's equations and assumed VDD to be 1.2v and f_{CLKC} to be $6GHz$. Moreover, the sizes of the back-to-back inverters and switches were chosen based on precharge state and load, so that power consumption can be calculated as a function of W, Eq. 3.11.

$$\begin{aligned} Power &= f_{CLKC} * V_{DD}^2 * ... \\ &\quad * \left(2 * C_{dd_{M1,2}}\left(\tfrac{W}{L}\right) + 2 * C_{dd_{S1,2}} + 2 * C_{ss_{M3,4}} + C_X + C_{CLKC} \right) \\ &= D * W + E, \quad \text{where:} \\ D &= 2 * f_{CLKC} * V_{DD}^2 * C_{OV}, \\ E &= f_{CLKC} * V_{DD}^2 * \left(2 * C_{dd_{S1,2}} + 2 * C_{ss_{M3,4}} + C_X + C_{CLKC}\right) \end{aligned} \tag{3.11}$$

To improve the performance (gain, speed, and power consumption), sizes of M1 and M2 ("W") should be optimized. In optimized state, gain-speed per power consumption reaches its maximum value. In Eq. 3.12, we illustrated how $\frac{Gain*Speed}{Power}$ is a function of W. Using Eq. 3.13, we reached the optimal W with a maximum $\frac{Gain*Speed}{Power}$.

$$\frac{Gain * Speed}{Power} = \frac{A * \sqrt{W}}{(B * W + C) * (D * W + E)} \tag{3.12}$$

$$\frac{d\left(\frac{Gain*Speed}{Power}\right)}{dW} = 0 \quad \Rightarrow \quad W_{opt} = \frac{E}{C}$$

$$W_{opt} = \left| \frac{\sqrt{(BE + CD)^2 + 12BCDE} - BE - CD}{6BD} \right| \tag{3.13}$$

$$C_{dd_{M_{1,2}}} = C_{dd_{S_{1,2}}} + C_{ss_{M3,4}} + C_{P_{parsitic}} + \frac{C_X + C_{CLKC} + C_{X_{parsitic}} + C_{CLKC_{parsitic}}}{2} \tag{3.14}$$

In Eq. 3.13, we can assume term $B << terms C, D, and E$. With this assumption, one can reach equation 3.14, providing a condition where $\frac{Gain*Speed}{Power}$ is approximately at its highest. The best sizing in actual implementation might be a little bit different. In the above equations, we assumed that channel length modulation and body effect are not affecting I_{SS}, g_m or V_{TH}. Doing simulations, accounting for parasitics

and bringing all factors into account, optimum values were found to be close to our calculations.

Tab. 3.2 describes the sizes used previously in [6]. Using our equations, we calculated the sizes of transistors in the structure. The sizes are show in Tab. 3.2. As it is shown in Tab. 3.3 The speed of the comparator improved 58%, while the power consumption was lower and gain was higher. Simulation results are presented in Fig. 3.19

Sizing	Width of the devices (L is 65nm for all devices)						Load
	M7	M1 & M2	S1 & S2	M3 & M4	S3 & S4	M5 & M6	
[6]	6um	12um	12um	8um	8um	12um	Inverter (3nm NMOS & 6nm PMOS)
Our sizes	10um	18um	8um	10um	6um	4um	Inverter (3nm NMOS & 6nm PMOS)

Table 3.2: Comparison of the transistors sizes in StrongArmLatch-based comparator in our work and [6]

Sizing	VCM of IN	Delay for IN=1LSB	Power Consumption	Gm over Id (Gain)
[6]	600mv	38.11ps	905.9uw	8.47
Our sizes (low VCM)	600mv	24.07ps	854.7uw	8.686
Our sizes (High VCM)	900mv	19.26ps	953.9uw	6.714

Table 3.3: Performance of the comparator after optimizing the sizings in this work

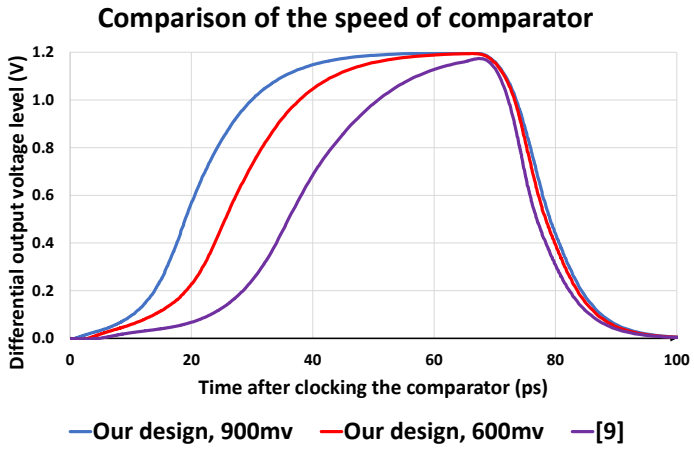


Figure 3.19: Comparison between our design under different input common-mode conditions with [6]

Our goal was to reach six conversion cycles in our implementation in $1ns$. However, with all the assumptions and parasitics after implementation, we did not reach the goal. There are two options to achieve higher conversion speed. The simplest is to increase the tail current, by increasing the tail device size at the cost of lower gain. However, a larger tail, a larger clock feed through. Another way to reach a faster conversion rate is increasing the common-mode voltage of the input, and accordingly the V_{DS} of the tail and its current. M1, M2, and M7 sizes are not changed, thus clock feed through does not increase, but gain drops. In both methods, the comparator becomes faster at the cost of its gain. Yet, the clock feed-through is smaller in the second method, and less area is occupied. Using a higher common-mode input voltage and the new sizing enabled us to hit our speed goal.

3.2.3 Asynchronous Clock Generator

This block generates a set of asynchronous clocks which can be divided in two groups. First, this block generates the clock of the comparator (CLKC). In addition, this block generates N other clock signals going to SAR's digital control logic which the risetime of each translates to the output of their cycle being ready.

The block requires a few inputs. One of which is the clock controlling the S/H switches connected to the CAPDAC. With a short delay, this clock triggers the comparator for the first conversion cycle. Another function of this clock is resetting the other N asynchronous clocks going to digital control units.

After modifying the sizes of switches in our simulation the dynamic offset falls to $0.37mv$, $45ps$ after $CLKC$ becomes '0' (Fig. 3.4). This dynamic offset is tolerable for our work. Therefore, the block must designed in a way that between cycles $CLKC$ remains '0' more that $45ps$.

Time after CLKC falls	25ps	30ps	35ps	40ps	45ps	50ps
Dynamic offset	2.7mv	1.22mv	0.68mv	0.46mv	0.37mv	0.31mv

Table 3.4: Dynamic offset after clock of the comparator falls

One part of the asynchronous clock generator is the circuit that generates the comparator's clock signal ($CLKC$). To generate CLKC, we need another signal describing state of the comparator, whether the comparator has made the decision or the outputs are "equalized". In the previous design [26], an XOR gate was used to generate the comparator's clock signal. In this work, the XOR and its buffer was replaced with an AND gate to improve the speed and power consumption. In the precharge state, both inputs of the AND gate are high; therefore, the output is $'1'$. Once the decision is made, and either of the inputs becomes $'0'$, the output of the AND gate falls to $'0'$. Again, once nodes P and Q charge to VDD (in the next cycle's precharge state), the output of the AND ($comparator's\,status\,signal$) rises, triggering the comparator's clock ($CLKC$) and starting the next conversion cycle.

In addition to *comparator's status*, two other signals are needed to generate $CLKC$. The first is the clock controlling the S/H switch ($CLKS$). Once high, the CAPDAC is sampling the input and $CLKC$ must stay low. While $CLKS$ is low, comparator must make N decisions. Following the last decision, $CLKC$ should stay low until the next sampling time starts. Therefore, $CLKS$, the sixth cycle's clock ("$CLK0$"), and the *comparator's status* signal are "ORed" together and buffered, if necessary, generating $CLKC$.

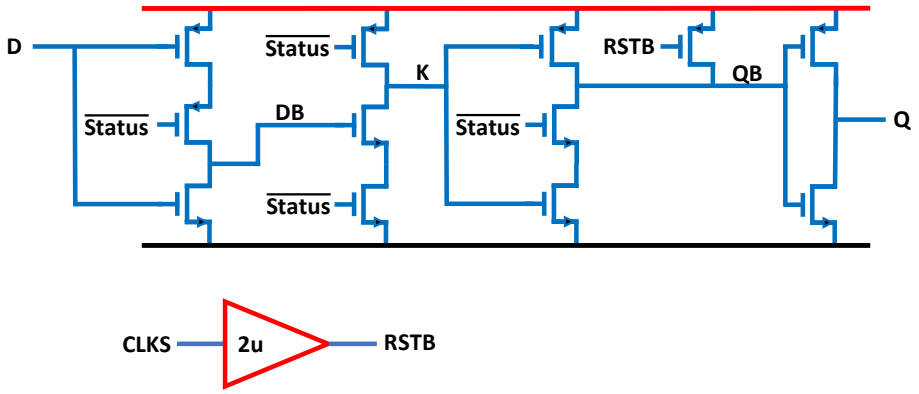


Figure 3.20: Structure of True Single-Phase Clock Flip Flop (TSPC-FF)

In addition to $CLKC$, the structure generates six other asynchronous signals for the digital control logic. [27] presented a true single-phase clock flip-flop-based shift register, generating the six asynchronous clocks (Fig. 3.21). *comparator's status* signal is the clock controlling TSPC-FFs. The input of the first TSPC-FF is VDD and output of each is connected to the next (Fig. 3.21).

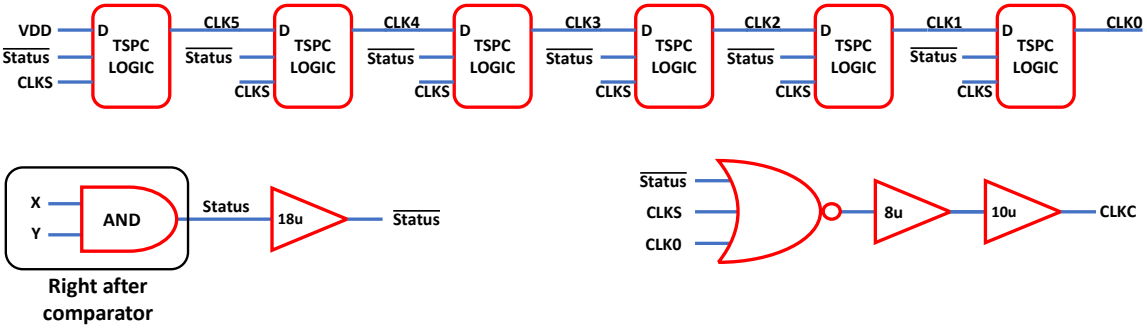


Figure 3.21: Asynchronous Clock Generator structure

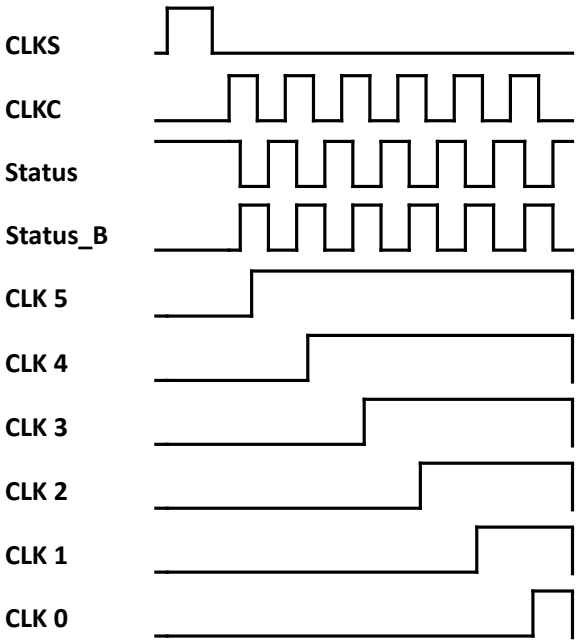


Figure 3.22: Timing diagram of Asynchronous Clock Generator Generator

$CLK5-0$, Fig. 3.22, go to the digital control block. The digital control unit saves the output of the comparator after each cycle. Based on the saved outputs, the digital control block generates signals controlling the CAPDAC's switches. Once the voltages on 'IP' and 'IN' nodes are settled, the comparator is ready to be triggered again. The timing between these steps and their duration is the most important part of the design. The gaps between the steps should be as small as possible, at the same time, far enough to ensure reliability.

3.2.4 Digital Control Block

The CAPDAC's switches change their states based on the comparator's outputs. The CAPDAC has N binary-weighted capacitors with switches that control the voltages across the capacitors. The digital control block generates a set of signals controlling the switches of CAPDAC.

In a 6-bit monotonic switching CAPDAC, used in our simulations, there are ten capacitors in total. Each of the capacitors needs its digital control unit. The structure of all the digital control units is the same. The are different in terms of their clock

signals and whether they are connected to the positive output of the comparator or the negative one. In our work, we modified the structure and performance of a previously used digital control unit [6].

The structure of the digital units used in [6] is shown in Fig. 3.23. In the design of [6], $\overline{CLK0}$ signal resets the unit. Then, $CLK(i)$, generated in the asynchronous clock generator after each comparison cycle, saves the comparators output and enables the digital unit. Then, the two output signals controlling the switches are generated and fed to the CAPDAC. In [6], the units decreases the common mode of the input, causing decision-making to become slower and slower over the cycles.

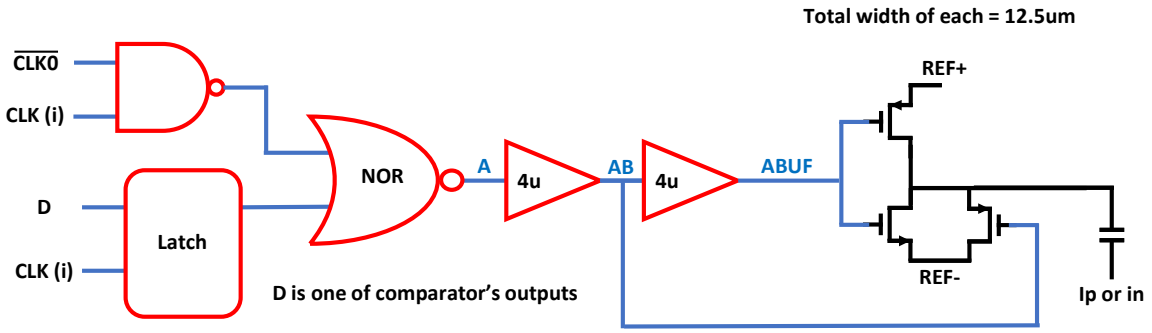


Figure 3.23: Previously used digital units

To save power and area and make the digital unit faster, we proposed the structure illustrated in Fig. 3.24. In our design, we used one output signal instead of two, which results in reducing the paths and their parasitics. In addition, we integrated the function of the NAND gate which its inputs were $\overline{CLK0}$ and $CLK(i)$ into the three-input NOR gate. This helps to reduce the area and power consumption. Also, this structure increases the common-mode voltage of the input, causing decision-making to become faster and faster over the cycles.

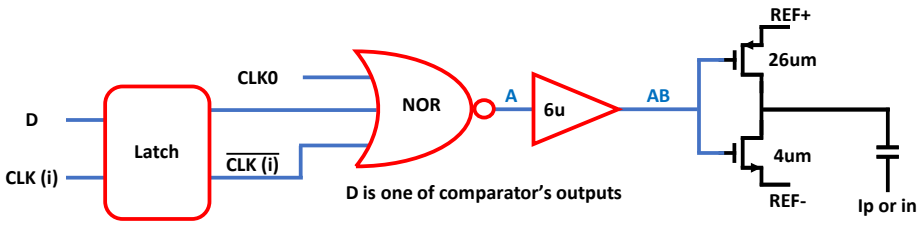


Figure 3.24: Proposed digital units

Comparing the proposed digital unit with the previous version, we achieved a much faster response time (24.2% faster). In the worst-case scenario (MSB), the input of the comparator (node ip or in) reaches 0.5% of its final voltage in $45ps$ (Tab. 3.5). While, [6] achieved the same accuracy after $50.4ps$. The $5.4ps$ faster response enables either increasing the speed of SARADC or reaching 0.01% voltage accuracy for nodes 'IP' and 'IN'. Using our unit, we could save $32.4ps$ over the six cycles. The downside of our structure is making the common-mode voltage higher in the comparator. Therefore, reducing the gain of the comparator.

Digital logic structure	Control signal delay	Reaches 0.5% accuracy at	Power consumption (per SARADC)
Previously used	29.8ps	50.4ps	1.722mw
Proposed structure	24ps	45ps	1.6345mw

Table 3.5: Comparison between previously used and proposed digital block - simulation results in both cases

We assumed there are $15fF$ parasitic capacitors on nodes connected to the switches (AB in Fig. 3.24 and AB and ABUF in 3.23). Tab. 3.5 compares the results of the two designs. As presented in the Tab. 3.5, in our simulation, the power consumption of all units decreased from $1.722mw$ to $1.6345mw$, compared to [6] - simulation results in both cases.

3.3 Timing Breakdown of SAR

The accuracy of the timing between the blocks is another important aspect in the design of SARADC. To ensure a fast, accurate digitization, the following system level

conditions have to be met:

1. Input range and its common-mode should be the desired and optimal values,
2. The outputs should be aligned after conversion,
3. And for the most crucial part of the design, the sub-blocks timing should be perfect.

In our simulation, the output of the cascoded buffer had a common-mode voltage equal to 900mv, designed for the fastest comparator's response time. After digitization by SAR, a set of TSPC-FFs were clocked with signal $CLK0$ within each SAR block and held the digital bits for $1ns$. Next, another set of TSPC-FFs re-time all SAR outputs with a 1GHz clock signal, preparing the data for the serilarizer. Such design meets the first and second conditions. However, the third system-level condition is much harder to meet. In the following paragraphs, we explain the timing of the sub-blocks, their relationships, and conditions to ensure the correct operation.

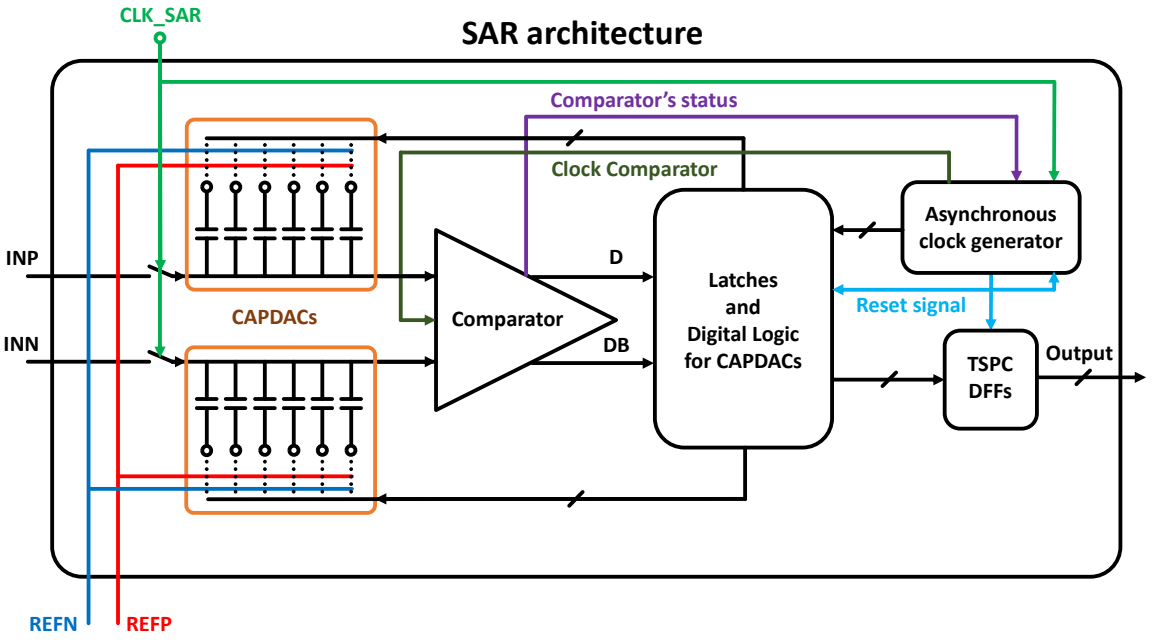


Figure 3.25: SARADC's architecture and relationship of signals and block

At first, the switches controlled by CLK_SAR or $CLKS$ are on, and the CAPDACs

are charging. Once the voltages on inputs of the comparator are settled, the switches turn off. CAPDAC holds the sampled voltage, and the comparator is ready to get triggered. When $CLKS$ is one, all signals and blocks are reset (the comparator's clock is '0', all $CLK(i)$s are pulled down, and the digital units are all in their initial state). Once $CLKS$ changes its state, CAPDACs go to their hold stage. At the same time, the asynchronous clock generator's logic triggers the comparator with a small delay. Then, the comparator makes the decision and a reset-set latch (SR-latch) holds the output until the next cycle.

Afterward, *status* signal, representing the status of the comparator, goes to the asynchronous clock generator and rises $CLK(5)$. $CLK(5)$ triggers a pair of digital control units. Based on the comparator's outputs, the pair change the voltages of the comparator's inputs. Once settled, the comparator's clock ($CLKC$) triggers the next cycle. Simultaneously, the comparator's status signal goes to the asynchronous clock generator, and $CLKC$ turns to '0' with a delay. Then, the comparator resets and *status* signal becomes '1', causing the next rising-edge of $CLKC$. The cycle continues to the point that $CLK0$ becomes '1'. Then, a set of TSPC-DFFs saves the digital code. Finally, the SAR is ready to sample the next symbol. Overall, the below conditions must be met:

- Outputs of the comparator must be ready before $CLK(i)$s' rising edges,
- The delay from the comparator being triggered to CAPDACs' voltages settling down must be shorter than the gap between rising edges of the comparator's clock signal,
- $CLK0$ must rise before the next sampling phase starts (next rising edge of $CLKS$).

Replacing the sub-block with the ones presented in this work, we achieved the results shown in 3.26.

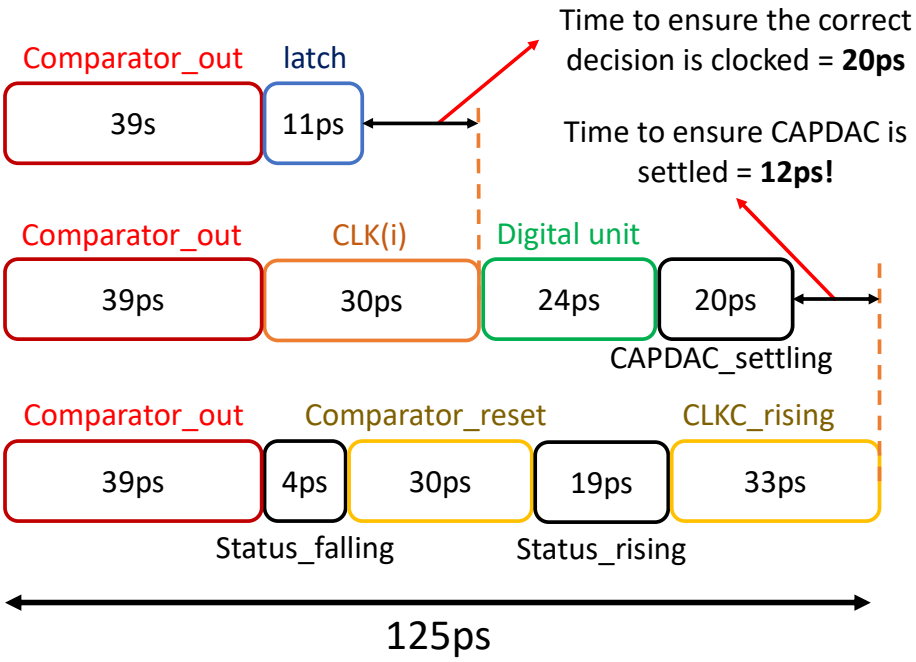


Figure 3.26: The timing breakdown of the improved SARADC, IN = 0.5LSB

Fig. 3.26 is plotted for the condition when IN= half LSB. This input size is the smallest in which the comparator has to make the right decision. The timing breakdown of the structure for the first conversion cycle illustrated that this design has an extra 12ps enabling the CAPDACs' voltages to settle down, which is a great improvement. Also, the latched comparator's outputs were available almost 20ps before the $CLK(i)$'s rising edge, ensuring the reliability of the circuit. It is worth mentioning that this design's comparator with approximate load and parasitics (5fF on P and Q nodes, and 10fF on nodes X and Y) made decisions significantly faster. Also, due to the fast drop in nodes X and Y, *Status* signal changed noticeably faster (4ps) compared to a previous work's result [6] (13ps) - Tab. 3.25. Without improving the asynchronous clock generator, our design made conversion time 23.8ps faster.

SARADC block	Analog power consumption	Digital power consumption	Total conversion time (6bits)
[6]	1.191mw	3.2mw	899ps
improved structure	1.226mw	3.1mw	722ps

Table 3.6: Comparison between conventional SARADC block and improved SARADC

Tab. 3.6 compares the power consumption and total conversion speed of [6] 's SAR and our modified SAR. Using the proposed digital control unit, the digital power consumption of the SAR has decreased. At the same time, the resized comparator drew almost equal power; yet operated much faster (almost 25% faster). Overall, the total power consumption (Digital plus Analog) has decreased in our simulations. In addition to power and speed, the design consumes a little less area (almost equal). As presented, technical improvements and designing based on the equations enabled us to achieve much better power, performance, and area (PPA). SAR characteristics are discussed in the next chapter.

3.4 Time interleaving SARADCs

With front-end, buffer, and proposed SARADC explained, we discuss the 8-way TI-SARADC in this section. Up to the point the signal reaches the SARADC, the CTLE and amplifier have extended the bandwidth, amplified the input, and turned their single-ended input into a differential input signal for ADC. From this point forward, the cascoded buffer provides eight amplified copy of the input. Each copy will be sampled by its SARADC. Afterwards, eight SARADCs start the digitization separately.

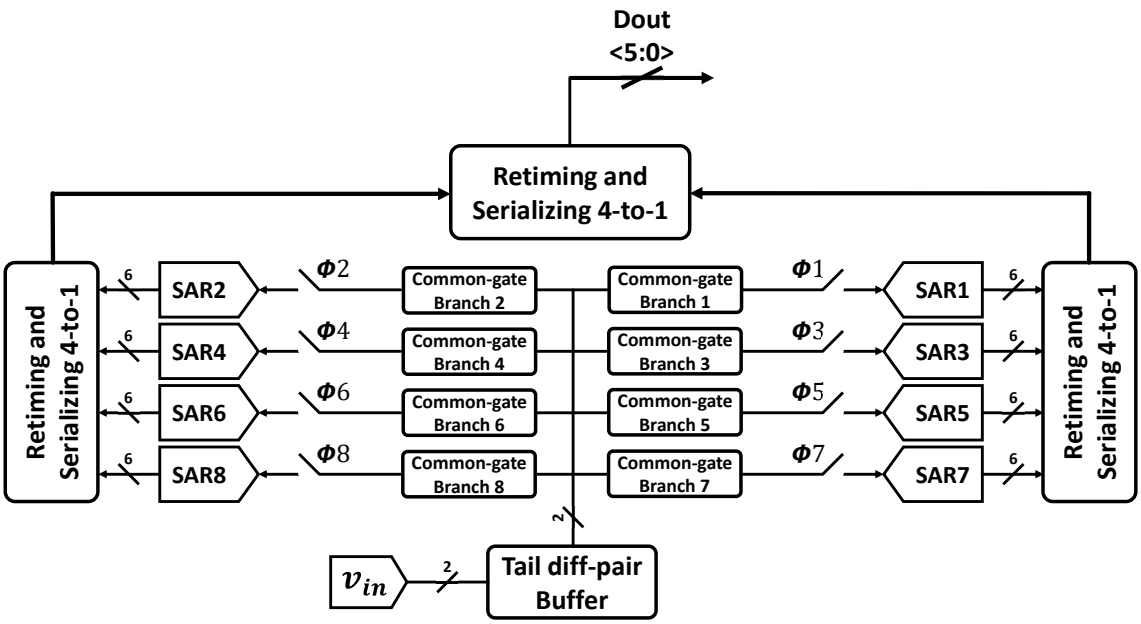


Figure 3.27: Time-interleaved SARADC structure

In our work, each SAR operates at $1GHz$. Therefore, the duration of the operation (sampling time and digitization together) is $1ns$. By sampling the input signal eight times (every $125ps$), the structure operates at $8GS/s$. First SAR samples and starts converting the input to digital bits. $125ps$ later, the second SAR starts sampling. At the end of the sampling time of the eighth SAR, the first SAR has generated and saved all of its digital outputs and is ready to start its next cycle. It is crucial that the outputs of the SAR are available and saved before the next sampling time to ensure correct operation of the TI-SARADC. The structure of the TI-SARADC and clock signals required for SAR to operate is shown in Fig. 3.27. As illustrated, there is a need for a clock generator block.

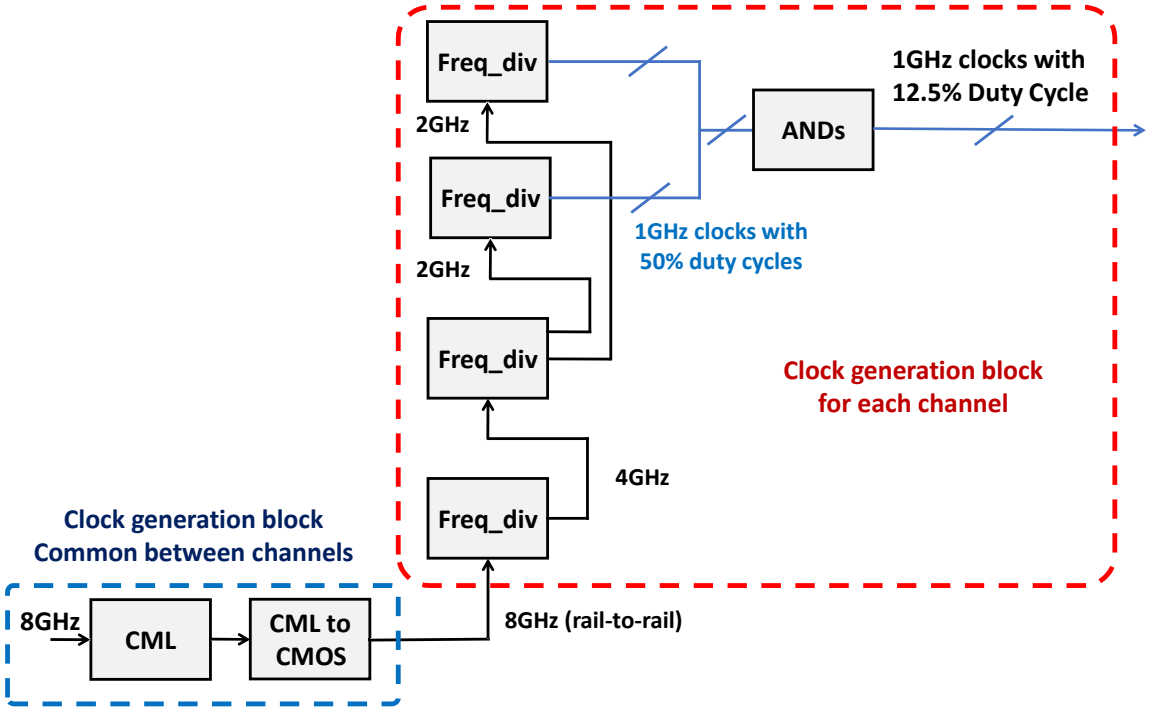


Figure 3.28: Clocks generator for 8-way TI-SARADC

The clock generator block has an $8GHz$ single-tone sinusoidal input signal. The single-tone signal goes to a typical current mode logic (CML) block. Afterward, CML-to-CMOS creates a rail-to-rail $8GHz$ signal, which goes to a logic created out of a set of frequency dividers and AND gates (Fig. 3.28). The outputs of the ANDs were the $1GHz$ signals with 12.5% duty cycle controlling SARs (Fig. 3.29).

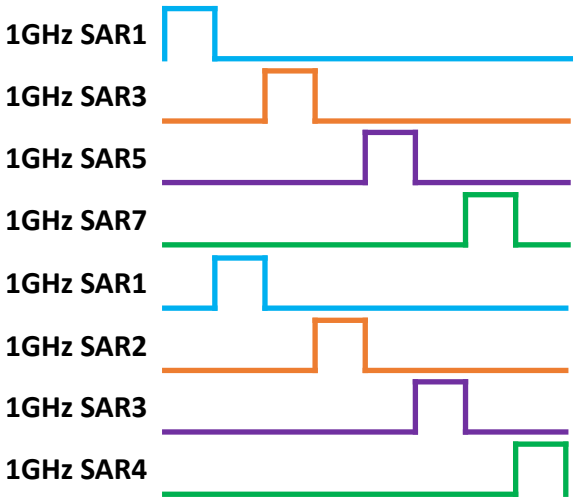


Figure 3.29: Clocks controlling SARs in an 8-way TI-SARADC

All the four channels use the same CML and CML-to-CMOS blocks. In the layout, in chapter 4, a clock tree propagates the $8GHz$ rail-to-rail signal to each channel. The logic marked in blue in Fig. 3.28 generates the eight $1GHz$ clocks (12.5% duty cycles) for each of the channels separately. All four logics used in the channels, the clock tree, the CML, and CML-to-CMOS all together represent "the clock generator block" in our work.

3.5 Serializing digital outputs

The SARADCs operate with different clock signals; therefore, their digital outputs are not aligned. To align the output signals of the SARs, forty-eight D-flip flops were used. The clock signal for DFFs was a buffered version of one of the $1GHz$ clocks with a 50% duty cycle generated in the clock generator. The clock should be rising while SAR-1 is sampling. Once re-timed, the digital bits go to a set of multiplexers (MUXs) clocked with the same $1GHz$ clock signal. After MUXs, digital bits go through another set of re-timing DFFs and MUXs clocked with a $2GHz$ clock signal. Then, DFFs clocked with a $4GHz$ clock re-time them again. Finally, a set of MUXs operating with the same $4GHz$ signal creates six outputs, each with $8GHz$ frequency.

The outputs are then buffered and sent to six 4-to-1 MUXs controlled by off-chip input signals. These off-chip input signals choose the outputs representing one of the channels. Then, outputs of the MUXs are buffered, re-timed if necessary, and sent to the drivers. The drivers, placed near output PADs, are CMLs which have two inputs: positive input connected to one output, and the inverted version of the same output. Also, The resistances in the drains of the diff-pair are 50Ω for matching purposes. The output of the CMLs goes to the PADs.

3.6 Conclusion

In this chapter, we described the SARADC-based receiver designed by [6], its structure, function, and limitations. Trying to improve the structure, we proposed a cascoded buffer and compared it to conventional buffers. The main focus in this work was technically improving the SARADC structure. Based on the equations, we optimized the comparator's sizings for the best performance, and improved the comparator's $\frac{Gain * speed}{Power\ consumption}$ 72.1% compared to [6]. The asynchronous clock generator of SARADC mainly remained the same, except that we used an AND gate instead of XOR. By changing the logic of digital units controlling the CAPDACs switches, we decreased digital control units delay while reducing their power and area consumption. Afterward, two timing breakdown diagrams were presented for a sample input, comparing the SAR used in [6] with our version. Finally, we described the structure of the time-interleaved SARADC and how the data was serialized and sent to the PADs allocated to the outputs.

Chapter 4

Implementation and Results

In chapter 3, the structure of the receiver was explained in details and modifications were applied to them. With the blocks improved, the structure was lay-ed out to compare the post-layout simulation results with the previous works and then sent for fabrication.

Following a systematic approach, the layout is done from the last block all the way to the first. Therefore, the output drivers and serializer sub-blocks (MUXs and DFFs) were done first. However, the layout of the serializer (placement of the MUXs and DFFs) is based on the structure of the eight-times interleaved SARADC. Therefore, the whole block done in this work is the SARADC. Afterward, the buffer was lay-ed out, then the CTLE and amplifier. Finally, other accessories like clock generator block, serializer, and output PADs were placed and routed. The layout of the receiver, and the layout of each channel separately is presented respectively in Fig. 4.1 and Fig. 4.2.

In the following sections, the characterization of the ADC and measurement procedure is firstly explained, while covering SNDR, SFDR, and ENoB. the post-layout effects on each block, the post-layout characteristics of the structure, and improvements compared to previous works are then illustrated.

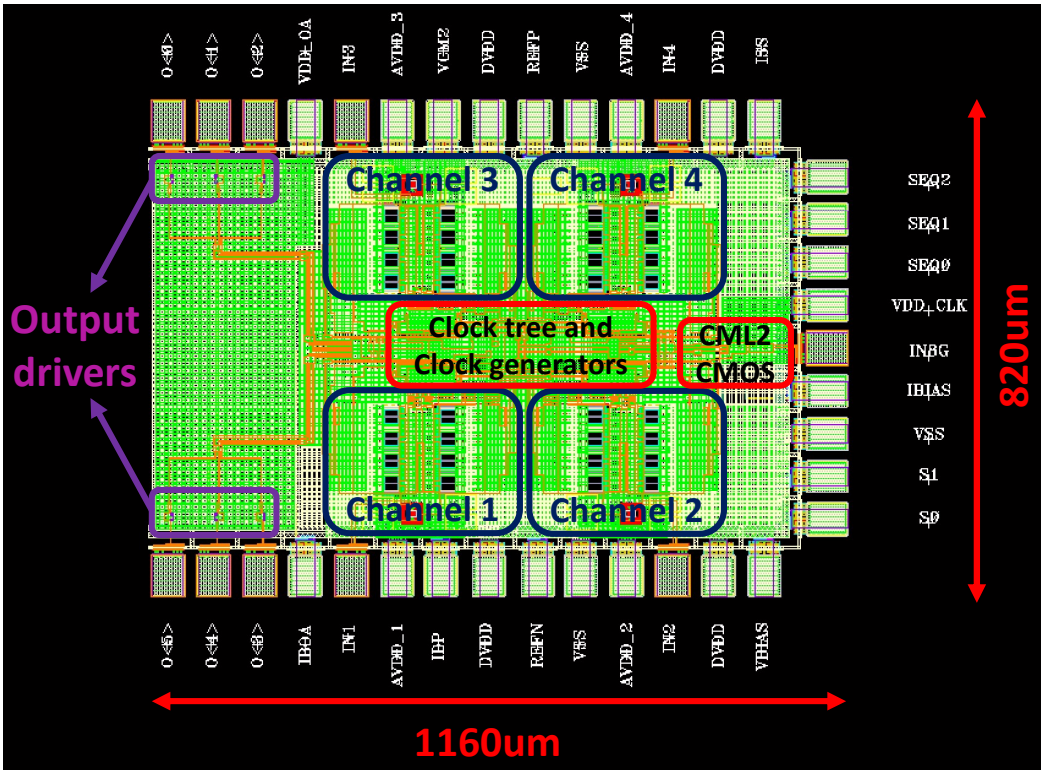


Figure 4.1: Layout of the receiver

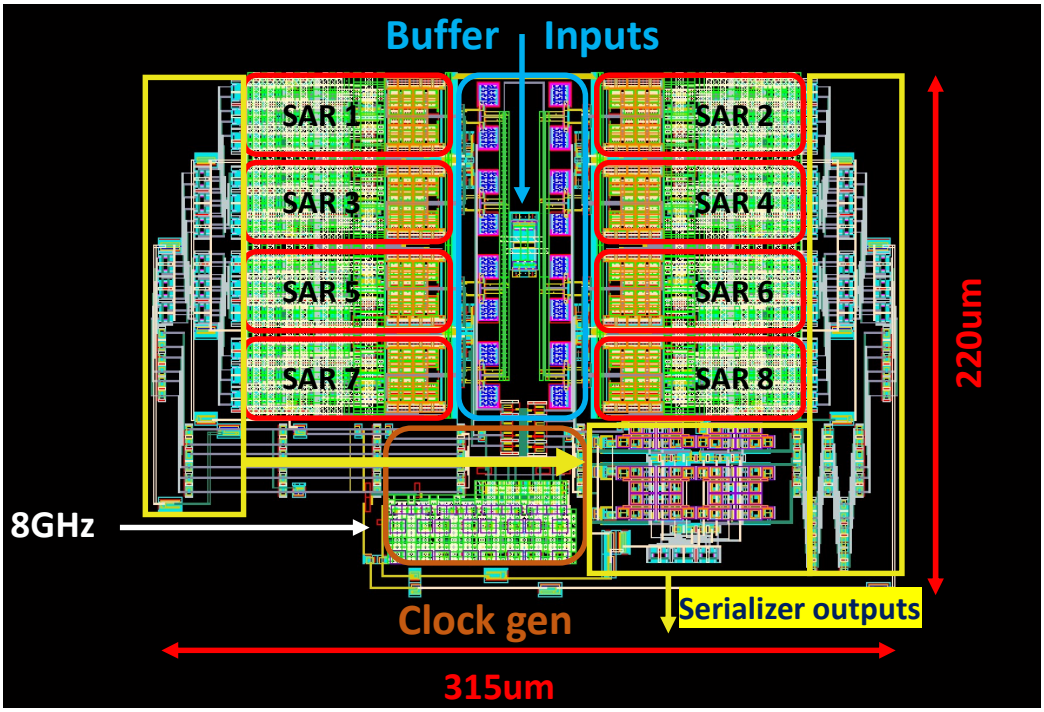


Figure 4.2: Layout of each channel

4.1 characterization and measurement procedure of ADC

The ideal characteristic of an ADC was explained in chapter 2. As the signal is quantized, each unique digital code coresponds to a relatively small range of analog input voltages. All analog inputs in the range resolve to the corresponding level; therefore, there is a quantization error - a finite number of output bits even for an ideal ADC translates to some quantization error.

4.1.1 ADC Resolution and Quantization error

Signal to noise ration

The quantization error is a limiting factor for the Signal to noise ration (SNR) of the ADC. Even in an ideal ADC, the quantization error causes an error like noise. All inputs in between +1/2LSB and -1/2LSB resolve to one code. With the assumption of this error being uncorrelated and having a uniform distribution, the maximum SNR for a full-scale input can be calculated to be [28]:

$$SNR = 6.02 * N + 1.76dB \tag{4.1}$$

Where N is the number of bits in an output digital code. Based on the exact equation for SNR [28], for an ideal ADC, the SNR for an 6-bits output would be 37.88 dB.

All analog to digital converters have additional noise sources and distortion processes which will affect the performance of the ADC. These imperfections are reported in a variety of ways which some will be covered here.

Signal to noise and distortion ratio

This merit is the ratio of the input signal to the rms sum of all spectral components.

$$SNDR = 10log\left[A_m^2\left(\sum_{i=1}^{m-1} A_i^2 + \sum_{i=m+1}^{M/2} A_i^2\right)\right] \tag{4.2}$$

Where M is the number of points in the FFT of a sinusadal input test. m is the number of fundamental frequency bin, and A_m is the amplitude of the bin. Signal to noise and distortion ratio (SNDR) is dependant on input signal frequency and amplitude, and will degrade at higher frequencies.

Effective Number of Bits

Effective Number of Bits (ENoB) is simply the SNDR expressed in a different format - bits.

$$ENoB = \frac{SNDR - 1.76dB}{6.02dB/bit} \tag{4.3}$$

Spurious-Free Dynamic Range

The ratio of the peak input signal to the peak harmonic or spurious component is the Spurious-Free Dynamic Range (SFDR). Spurs can be created at harmonics of the input frequency due to nonlinearity. They can also be seen at subharmonics of the sampling frequency due to mismatch or clock coupling in the circuit. There are also more merits which are not covered here in this section. The reader can refer to [28] for more information.

4.2 Dynamic ADC Testing method

A variety of test can be used to measure the specifications of the ADC. Most of the tests rely on Fourier analysis. In one of the simplest tests, the ADC is derived with a single, low distortion sinusoidal signal. With the FFT of the digital output of the ADC, SNDR, ENOB, SFDR, and Total Harmonic Distortion (THD) can easily be calculated. To test the linearity and static characteristics of the ADC a slow ram input covering all the range of the input signal can be introduced to the circuit.

4.3 Post layout effects on SARADC

SARADC suffering from the post layout effects was expected. While doing the layout, the linearity of the capacitors in the CAPDACs was one of the most important aspects. The integral non-linearity of the SAR depends mainly on three factors: the linearity of the CAPs in the CAPDAC, the systematic mismatch of the components, and the random mismatch in the devices. Two first two factors can be controlled by the designer. To reduce both, the structure had to be as symmetric as possible, and the ration of the binary weighted capacitors had to be as ideal as it could be to reach DNL $<$ 0.5LSB and INL $<$ 1LSB.

Table 4.1: comparison of the post-layout and schematic sizes of the CAPDAC

	Binary weighed capacitances of the CAPDAC					parasitics			
	C(4)	C(3)	C(2)	C(1)	C(0)	substrate	input capacitance of comparator when off	other	total capacitance
Ideal value	40fF	20fF	10fF	5fF	2.5fF	0fF	-	0fF	77.5fF
post-layout values for positive input (IP)	41.49fF	20.76fF	10.27fF	5.1fF	2.6fF	2.92fF	4.1fF	$\approx 4.3fF$	91.54fF
post-layout values for negative input (IN)	41.49fF	20.69fF	10.27fF	5.1fF	2.6fF	2.87fF	4.1fF	$\approx 4.3fF$	91.42fF

As illustrated in Tab. 4.1, the total capacitance of the I/O ports of the CAPDACs in post-layout results increased by 18%. This translates to an increase in the RC constant of the CAPDAC with the load resistance of the buffer (200ohms). The RC constant is equal to $20ps$. As a result, a sampling time equal to 125ps provides more than six RC constants for the CAPDAC voltage to settle down. This means at the end of the sampling phase the held voltage is at most only $\approx 1mv$ away from the copy of the signal.

The comparator had to be as symmetric as possible. In addition to symmetry, after the usage of the first sizes in the layout, due to the sizes of switches, there was a dynamic offset after the precharge phase. Thus, the sizes of the switches were increased to 10 micron to reduce the dynamic offset to a lower value in nodes P, Q,

X, and Y. The sizes of the PMOSs in the latch were also increased to 12 micron to reduce the time constant of the decision making by the latch. The digital block and asynchronous block remained the same.

After applying these points, the parasitics were extracted and post-layout simulations inculing MonteCarlo simulation on the comparator (Fig. 4.3) and different process corners, supply voltages, and temperatures (PVT) on the SAR were done. The post-layout results for different process corners and temperatures equal to -30C, 27C, and 70C for a sample input are illustrated in Fig. 4.4 and Fig. 4.5.

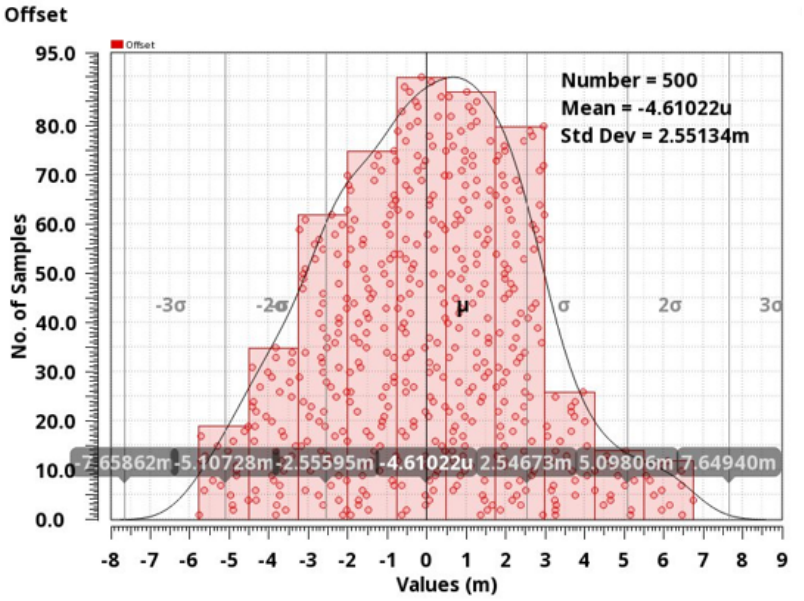


Figure 4.3: MonteCarlo results of the comparator

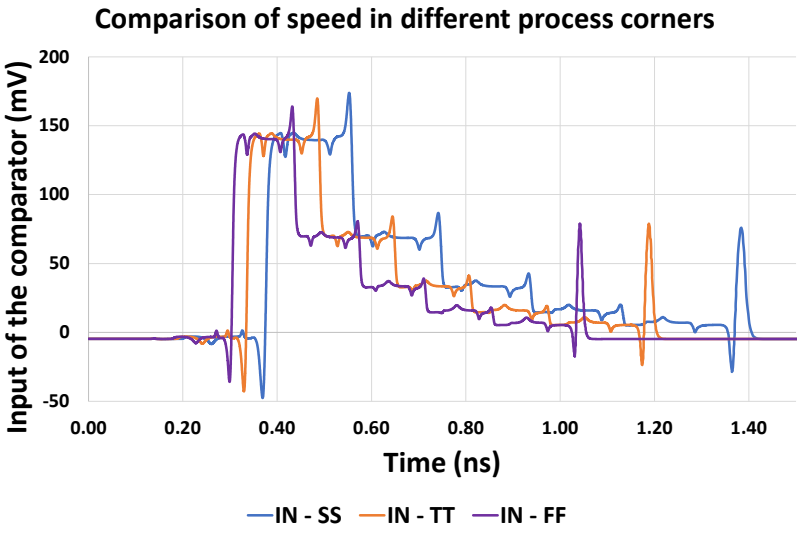


Figure 4.4: Speed comparison for different process corners (FF, TT, and SS) - in typical room temperature

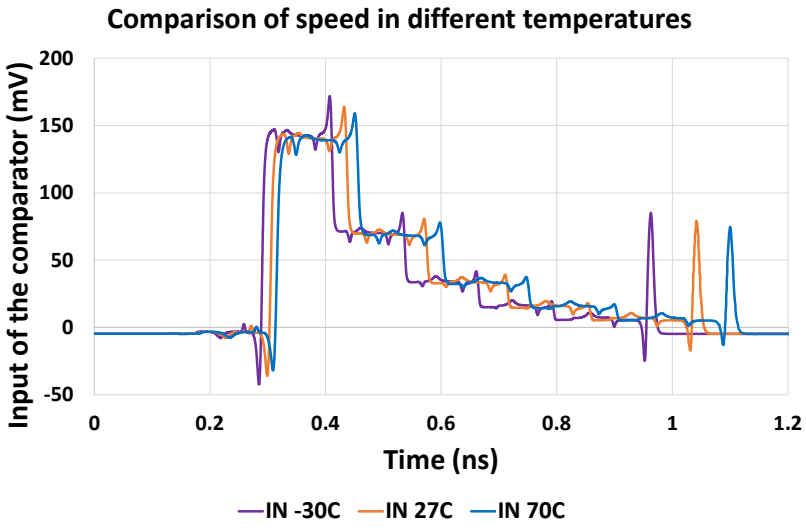


Figure 4.5: Speed comparison for different temperatures (-30C, 27C, and 70C) - TT conrner

In Fig. 4.5, the speed rises as the temperature drops, however the mobility rises with the temperature. Yet, the scattering of the carries increases at a higher rate causing the devices to slower. Fig. 4.6 compares the maximum ('FF' corner and -30C temperature) with the minimum ('SS' corner and 70C temperature). In the best case scenario, the SAR can reach a operating speed as high as 10GS/s. Yet, in the worst case scenario, the maximum possible operation is around 6GS/s in the

post-layout simulations. Increasing the VDD, it is possible to reach almost 7GS/s in the worst case scenario. In the typical process corners and room temperature, the SARs operated at 7GS/s facing no issues.

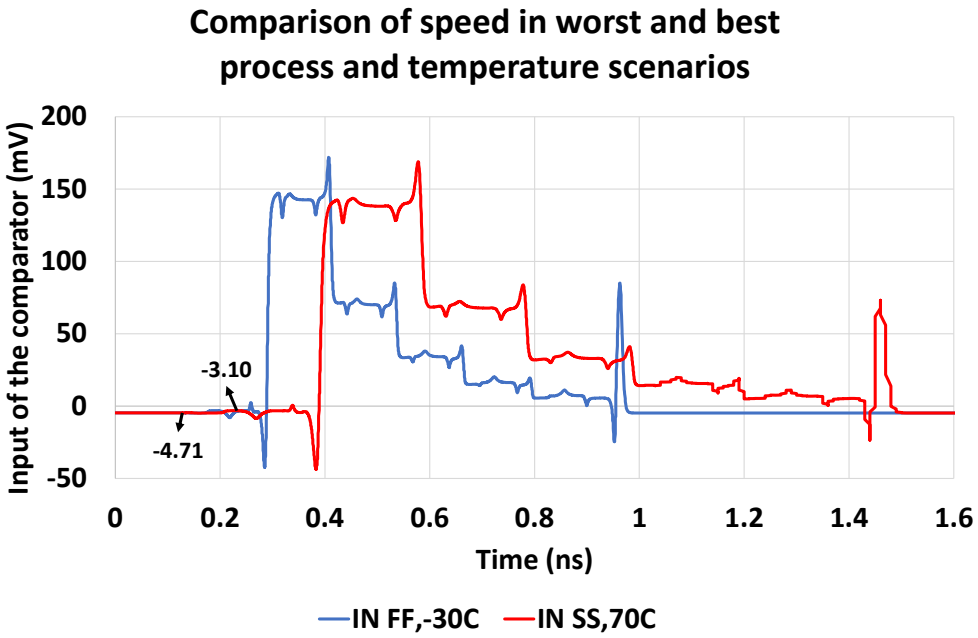


Figure 4.6: maximum and minimum speed in process corners and temperatures

With the capacitance path between CLKC and the inputs of the comparator, the kick back noise comes into the picture. In Fig. 4.6, two voltage values for a sample input (0.5LSB) are shown. Once the sampling phase is finished, the voltage difference on the CAPDACs is equal to 4.71mv. The rising-edge of CLKC causes a non-equal shift in the voltages held on CAPDACs. This effect is called the kickback noise and in extreme cases results in wrong decision. The kickback noise should be as small as possible to ensure correct decision making and better SNDR. Illustrated in Fig. 4.6, the kickback noise is only $1.61mv$ (on sixth of LSB), when input is equal to half LSB.

The characteristics of the SAR (DNL, INL, SNR, SNDR, SFDR, and ENoB), with S/H circuit and clock path, are illustrated in Tab. 4.2 and Tab. 4.7. The characteristics of the SAR are expected to be almost perfect since the capacitors of the CAPDACs were measured to be almost perfectly equal in IP and IN nodes,

and the ratio between them in each CAPDAC was almost binary. However, the characteristics must be measured once again with the effects of the CTLE, amplifier, and buffer.

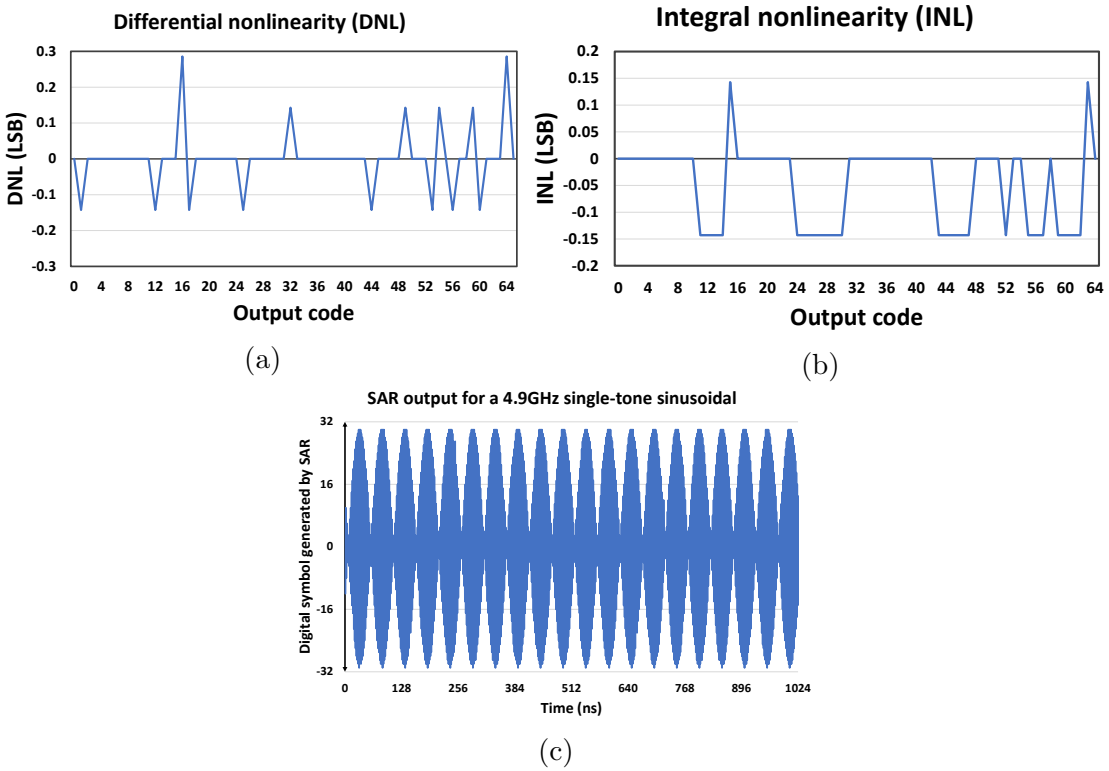


Figure 4.7: Characteristics of the SAR, post-layout simulation results a) Differential non-linearity, post-layout - without mismatch b) Integral non-linearity, post-layout - without mismatch c) Digital output for a single-tone sinusoidal

Table 4.2: Characteristics of the SAR (post-layout)

Characteristics of the SAR	Number of bits	Ideal SNR	SNR	SNDR	SFDR (harmonics 2-5)	ENoB	Analog power	Digital power
Post-layout without buffer	6	37.88dB	34.83dB	34.55dB	50.54dB	5.43	1.23mw	3.1mw

4.4 Front-end

The floor plan of each channel was illustrated in Fig. 4.1. The inputs entered the structure from top and go to the buffer. A set of four SARs were placed at each side of the buffer and each of the branches was placed right near a SAR, to reduce the

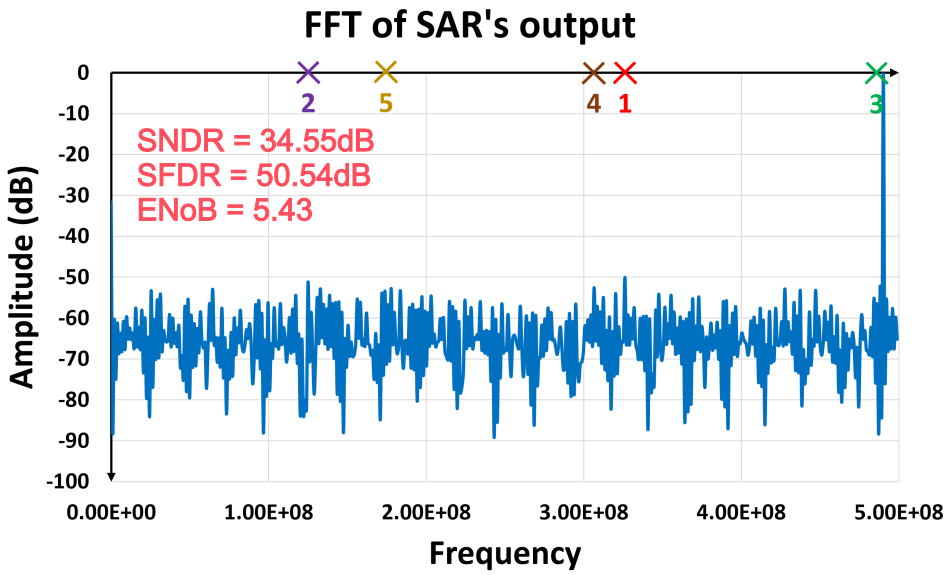


Figure 4.8: Full FFT of the output for a single-tone sinusoidal

parasitic capacitance during the sampling period at the cost of worse mismatch which is compensable. The post-layout characteristics of the buffer (gain, bandwidth, and power consumption) are illustrated in Tab. 4.3.

Table 4.3: Characteristics of the buffer (post-layout)

Characteristics of buffer	Input -3dB frequency	Common-gate -3dB frequency	Output -3dB frequency (loaded with a SARADC)	Power consumption with accessories	Gain	Gain-BW
Values	8.02GHz	44.32GHz	4.15GHz	18.54mW	6.55dB	8.82GHz

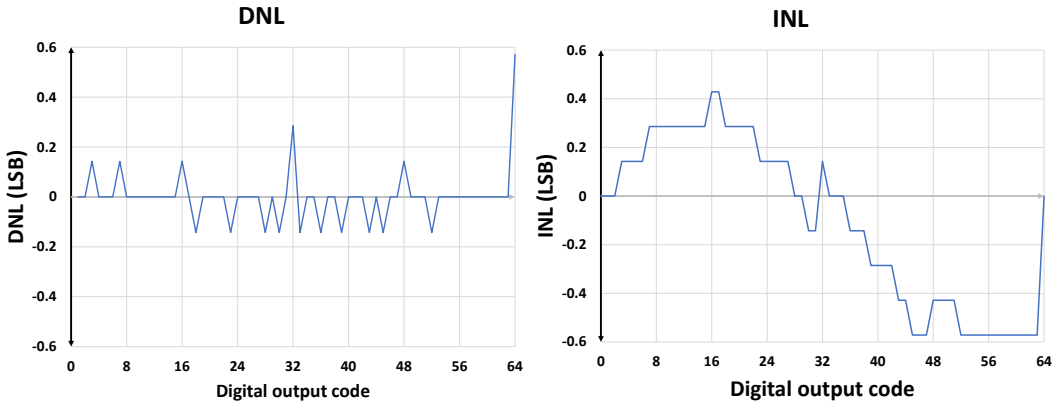
In the post-layout bandwidth of the buffer dropped from 6.9GHz to 4.15GHz. The main cause of the drop is the increase of the capacitance connected to the output nodes. Naturally, to extend the bandwidth using a smaller unit capacitance for the CAPDAC would push the pole to higher frequencies. Another way is to decrease the loading resistor in the buffer structure. To compensate for the gain loss due to reduction of the resistance, more current must be drawn from the power and ground sources - power-bandwidth trade-off.

Note that, the input -3dB bandwidth of the buffer is the -3dB bandwidth of the rest of the circuit (CTLE and amplifier before the buffer). Previously, in the simulation

results the loading capacitance was assumed to be 50fF and the load was 600Ω. However, by increasing the current the leading resistance of the amplifier was reduced to 200Ω and the bandwidth was extended.

4.5 The characteristics of the receiver

The characteristics of the receiver (INL, DNL, SNDR, SFDR, EnoB, area occupation, and power consumption) changed after attaching the front-end. Re-simulating the DNL and INL characteristics with the post-layout of the front-end effects, INL became much worse due to the non-linearity introduced by the front-end. The new DNL and INL characteristics are illustrated in Fig. 4.9. Comparing the results to post-layout simulation results of the SAR, the maximum of the INL became four times of SAR's maximum INL.



(a) (b)

Figure 4.9: Post-layout simulation results without mismatch effect a) Differential non-linearity b) Integral non-linearity

Analyzing the DNL and INL are worst at the very right ends of Fig. 4.9a and Fig. 4.9b. Comparing the measured digital output with ideal form Fig. 4.10, the non-linearity is also visible at the far right end of the graph. The non-linearity is caused mainly by the non-linear transient response of the first amplifier. The first amplifier changed the input (single-ended) to a differential signal. Doing so, the common mode of the diff-pair fluctuates, changing the current and the gain, over the input range.

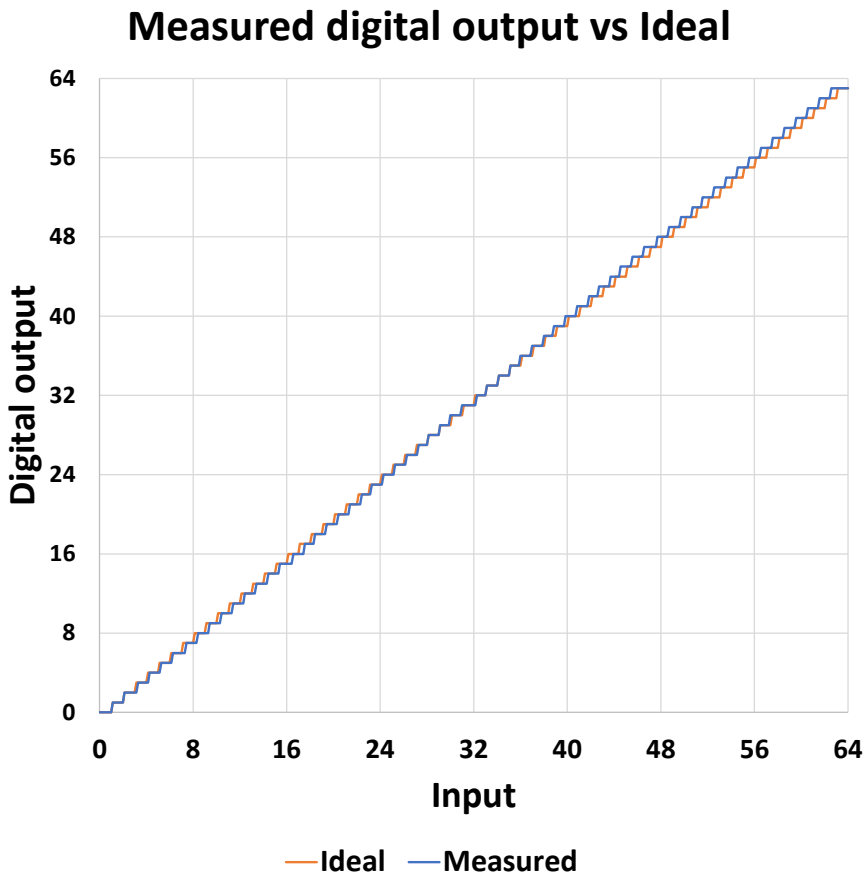


Figure 4.10: Digital output of the receiver - measured vs ideal

To measure the rest of the characteristics, a single tone sinusoidal close to Nyquist rate frequency ($\frac{251}{512} * F_{Nqy} = 3.921875GHz$) was introduced to the receiver. The digital output of the receiver is shown in Fig. 4.11. Fourier transformation of the signal is illustrated in Fig. 4.12 and Tab. 4.4 describes the characteristics of the receiver.

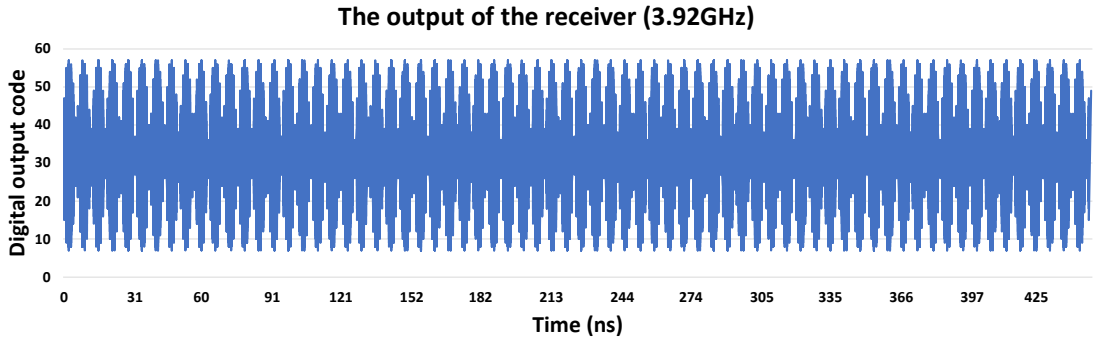


Figure 4.11: Digital output of the receiver to calculate its characteristics

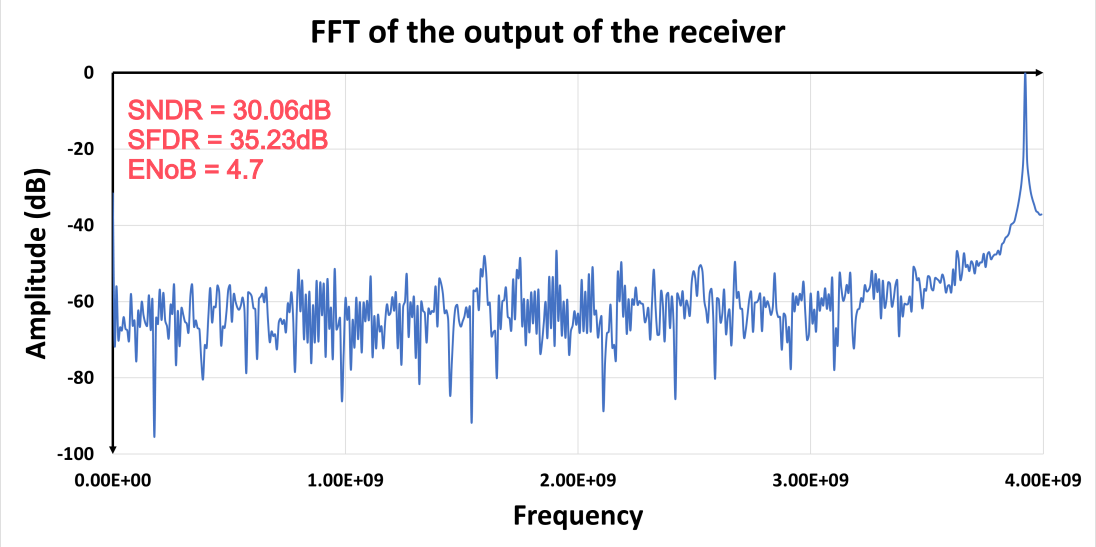


Figure 4.12: Full Fourier Transformation (FFT) of the receiver's output

Comparing Fig.4.12 and Fig.4.8 and Tab.4.2 and Tab.4.4, one can see that the effect of front-end's non-linearity in the FFT plots. Due to the non-linearity introduced by changing the single-ended input to a differential buffered signal, the SFDR has significantly dropped.

Table 4.4: Characteristics of the receiver (post-layout)

Characteristics	SNR ideal	SNR	SNDR	ENoB	SFDR	Analog power: comparator, CTLE, Diff-pair, Buffer	Digital power	Accessories power per channel Serializer, MUXs, Output buffers, and CLK
Post-Layout	37.88dB	32.24dB	30.06dB	4.70	35.23dB	28.38mW	24.8mW	8.46mW

Chapter 5

Conclusion

This chapter provides a summary of the key contributions presented in this dissertation and presents possible future works for the reader. The following sections will provide:

- A summary of the work
- Thesis contribution
- Future works

5.1 Summary

The competition in the industry forces the system level designers to allocate less power budget to power hungry blocks. Therefore, designers are having to optimize the designs to stay within the allocated range specified in the spec requirement with which they are provided. At the same time, speed is another growing factor. As the frequency of data transfer grows, ADC-based receivers are becoming significantly popular, providing the chance for digital equalization and its benefits, to compensate for the high loss in high frequencies.

First, in Chapter 1, we talked about the motivation which drove this work. Chapter two, briefly provided a background knowledge covering the theory behind the operation of ADC, different kinds of ADC and their operation, and a first order com-

parison between ADC architectures. Afterward, end of the chapter Walden's figure of merit was introduced and works published in top conferences and journals since 2010 were compared using Walden's FoM. Comparing the proposed SARADC introduced in this work with the trend-line extracted from previous works, proves this work to be competitive with other designs, while not benefiting from interpolation or redundancy techniques applied in those [29].

Chapter three describes the method of the design for SARADC-based receivers. While from a system level view the structure of SAR or receiver has not been significantly improved, the specifications have improved notably. The chapter starts with front-end, once designed, the focus shifts to optimize the SARADC specifications both is the analog part and the digital logic of the SAR. Timing breakdown of the SAR was presented and compared to previous work for an input level equal to half LSB (worst case scenario). Afterward, the third chapter briefly covers the clock generation and serializer.

Finally, chapter four covers ADC merits, ADC testing, receiver's layout, and affects of the parasitics on the blocks. Following that, PVT simulations are done on SARs. A slow ramp input was introduced to both SAR and the receiver, and INL and DNL graphs were plotted using the Matlab codes included in the appendix and post-layout (C+CC) results extracted from Cadence. In a same approach, introducing a single tone sinusoidal close to the Nyquist rate of the ADC with a prime relation to the F_{Nyq} of the structure, using Matlab codes SNDR, SFDR, ENoB, etc. were plotted for the structure.

Tab. 5.1 compares this work with previous works. Operating at 8GS/s and having a resolution of 6 bits per symbol, consuming low power (almost 60mW per channel, including front-end, serializer, and output driver), and occupying $0.069mm^2$, this work proves to be competitive to previous works.

Table 5.1: Performance summary of the 8-TI SARADC

	[30]	[31]	[32]	[6]	This work
Speed	**0.7GS/s**	**4GS/s**	**5GS/s**	**4GS/s**	**8GS/s**
Resolution	**8**	**8**	**7**	**8**	**6**
Architecture	**Single channel**	**4xTI**	**8xTI**	**4xTI**	**8xTI**
ADC type	**Flash-SAR**	**Pipeline**	**SAR**	**SAR with redundancy and interpolation**	**SAR**
Technology	**65nm**	**65nm**	**55nm**	**65nm**	**65nm**
Supply	**1.2**	**1.2/1.4**	**1.2/1.5**	**1.2**	**1.2**
Power (mW) excluding Front-end	**5.96mW**	**120mW**	**38mW**	**27.76mW**	**43.64mW**
SNDR (dB) @ Nqy.	**41.6**	**44.4**	**35.9**	**39.56**	**30.06**
SFDR (dB) @ Nqy.	**47**	**55**	**45**	**48.21**	**35.23**
Area (mm2)	**0.033**	**1.35**	**0.69**	**0.019**	**0.069**
Walden's FoM @Nyq Freq. (fJ/step)	**86.7**	**219**	**150**	**89.32**	**209**

5.2 Contributions

The list of original accomplishments described in this thesis can be summarized as the following:

- A novel structure was introduced for the buffer. The buffer while consuming same power and providing same gain, compared to conventional structures provides a higher bandwidth. At the same time, since the sizes of the input transistors are required to be relatively larger, the mismatch effect due to its diff-pair is negligible. Controlling voltages of the common gate devices provides a chance to compensate for any inherent mismatch introduced by the common gate devices or the resistors. Meanwhile, the linearity of the proposed buffer was significantly better the conventional methods. In addition to all that has been said, all the current drawn from the supply voltage will translate to output swing, unlike the conventional buffer structure.

- In a novel approach, the equations for the speed and the gain of the amplification phase of the structure of Strong-Arm latch, introduced in [33], was driven. Based on the equations, the optimum sizes for the transistors in the structure was chosen. Then comparing the comparator to the ones used in previous works, the delay of the comparator decreased from 38.11ps to 24.07ps to make the decision when differential input is equal to 1-LSB, while increasing the gain and consuming less power.

- By increasing the common mode of the input, the delay of the comparator decreased even more from 24.07ps to 19.26ps, making it almost two times faster than the structure used in previous works. However, this benefit came with a little drop in gain and slightly increasing the power consumption of the Strong-Arm.

- The structure of the digital units, controlling the voltages across the capacitors in the CAPDACs was also improved. This change in the structure reduced the delay of the digital units from 29.8ps to 24ps in our simulations while consuming less power.

- The timing diagram of the structure showed significant reduction in the total delay of the comparator (Strong-Arm and the logic after that). At the same time, making the digital units faster and resizing the switches will result in more time for the CAPDAC voltage to settle, thus increasing accuracy.

In conclusion, the sub-blocks of the SAR were improved to both consume less power and operate faster. A new structure was proposed in the front-end which achieved a higher bandwidth, better linearity, and enabled room to compensate inherent gain mismatch. Also, the condition for maximum gain*speed for the comparator can be applied to any StrongArm-based comparator, which can improve other works significantly.

5.3 Future Considerations

Applications like data centers, internet of thing (IoT), and consumer electronics increases the need of power reduction for researchers. One way to reduce the total power consumption of the system is to implement the power-hungry analog blocks with significant efficiency. This main focus of this work was on optimizing the sub-blocks of the SARs which resulted in significant improvement in speed-gain-power product in the amplification phase of the comparator, speed-power product of the digital control units, and extending the bandwidth of the buffer for same power consumption and gain. Following a similar approach to improve PPA, one can do either of the followings:

- Optimization of the comparator is not limited only to the amplification phase of the comparator. Following the same approach to amplification phase, the energy product of the regeneration phase of this works comparator can be optimized as well.

- Applying offset correction techniques enables improving this work further, providing the chance to apply interpolation and redundancy techniques to work. This approach will increase the ENoB significantly, while not affecting the power consumption, which will result in a much better Walden figure of merit.

- To improve this work further, one can utilize the possibility of inherent gain-mismatch correction which the buffer provides. A simple way to take advantage of this benefit is to sense the output of SARADC, assuming offset correction techniques are applied. Imagine there are only two SARs and two branches. Introducing a specific input value to the SARs which is right at the border of two different digital symbols. If the distribution of the output digital codes were in equal, it is possible to shift the branches upwards and downwards controlling the gate voltage of the common gate transistors.

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