# Quantum-Mechanical Assessment of Graphene and $MoS_2$ Transistors for Future Radio-Frequency Electronics

by

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# Abstract

Due to aggressive device scaling, the performance and cost-effectiveness of field-effect transistors (FETs) have improved exponentially over the last 60 years, a trend known as Moore's Law. Unfortunately, obstacles have arisen to further scaling, including decreased electrostatic control of the gate from drain-induced barrier lowering. Two major alternatives to planar silicon transistors have been suggested to remedy the electrostatic limitation: the ultra-thin-body silicon-on-insulator (UTB-SOI) transistor and the fin field-effect transistor (FinFET). Furthermore, alternative channel materials have been suggested for future devices, such as carbon-based materials (carbon nanotubes and graphene) and transition-metal dichalcogenides [single-layer molybdenum disulphide (SL $MoS_2$)].

In this work, quantum-mechanical modeling, necessary to capture short-channel and quantum-confinement effects in less-than-20-nm silicon devices and in devices made with new channel materials, is used to investigate the performance potential of graphene transistors, single-layer molybdenum disulphide transistors, and FinFET silicon transistors for RF applications.

The first stage of work quantifies the effect of graphene's lack of a bandgap in limiting its high-frequency performance, an issue recently flagged by Schwierz in *Nature* as being of critical importance for graphene devices to become commercially viable. We show that although there is a substantial decrease in relevant RF performance metrics due to the lack of a bandgap, the operation of graphene transistors can still exceed industry guidelines.

The second stage of work addresses the question of whether devices made from SL

$MoS_2$, a material with a bandgap, can match or exceed the potential of gapless graphene for RF applications. We show that the peak performance of graphene is better, but SL $MoS_2$ gains an edge in low-current applications. We place an emphasis on quantifying the necessary improvement of the contact resistances required with SL $MoS_2$, an important limiting factor in current experimental work. Excellent agreement is observed between our simulated results and available experimental results.

Ongoing work is being conducted to extend our modeling to examine short-channel FinFETs down to 5-nm channel lengths, in conjunction with industrial collaborators. We show results that illustrate the viability of our chosen approach.

I dedicate this work to my wife and partner, Sarah, for her strong and continuous love and support throughout this thesis, and to my parents, for being there every step along the way.

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# Chapter 1

# Introduction

## 1.1 Motivation

The performance and cost-effectiveness of field-effect transistors (FETs) have improved exponentially since their development in the late 1950s [1], a trend known as Moore's Law [2]. The primary reason for the improvement has been the aggressive scaling of the device. As the size of the planar metal-oxide-semiconductor field-effect transistor (planar MOSFET) has decreased, more devices have been integrated into the same area, decreasing the cost per transistor. In addition, smaller transistors have had progressively reduced channel lengths for electron transport, and this has improved the speed and performance of individual FETs. Finally, a reduced supply voltage has been possible with smaller devices, which has helped to lower total chip power consumption.

Unfortunately, obstacles have arisen to further scaling. For example, as the size of the transistor channel decreases, the electrostatic control of the gate on the channel diminishes, and the deleterious action of the drain on the channel increases, an effect known as drain-induced barrier lowering, or DIBL. The emergence of such short-channel effects has detracted from the performance increases gained from device scaling, especially in the area of power consumption.

Research, formalized in the International Technology Roadmap for Semiconductors

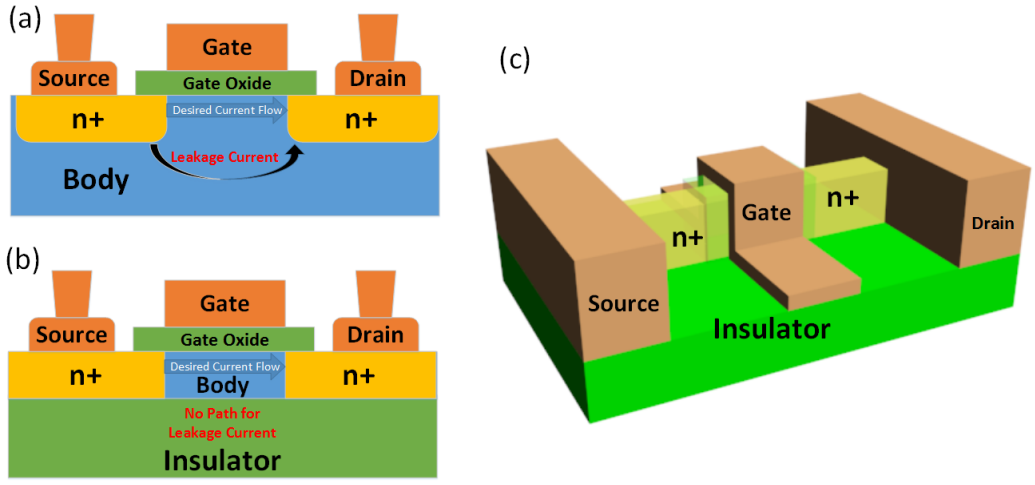



Figure 1.1: (a) A traditional planar MOSFET, (b) UTB-SOI transistor, and (c) FinFET transistor.

(ITRS) [3], has identified two major structural changes that can mitigate short-channel effects. First, the ultra-thin-body silicon-on-insulator (UTB-SOI) architecture severely reduces the thickness of the channel while still retaining a planar structure. Contrary to the planar MOSFET, the channel sits on an insulator, eliminating leakage paths that would have existed through a silicon body. The channel is also made thin, ensuring the gate electric field penetrates more effectively, increasing gate control and reducing DIBL. Second, the fin field-effect transistor (FinFET) moves away completely from the traditional planar architecture by having a gate wrap around a "fin" of silicon. This approach also eliminates the majority of leakage paths by reducing the amount of semiconducting material. The various structures are illustrated in Fig. 1.1; part (a) shows a traditional planar MOSFET, part (b) shows a UTB-SOI device, and part (c) shows an SOI FinFET device[1].

In addition to UTB-SOI and FinFET devices, the ITRS has also suggested the need for

[1]A second FinFET structure, the bulk FinFET, also exists, with the insulator being replaced by silicon in Fig. 1.1 (c). We will only assess SOI FinFETs in this thesis.

research into alternative (novel) channel materials for use in the semiconductor industry. FETs with alternative channel materials are often labeled as being *beyond silicon* [4, 5], due to their potential to continue Moore's law *beyond the scaling of silicon*. The demonstration of carbon nanotubes as a working channel material for a room-temperature field-effect device [6] was the spark which ignited intense interest in the use of beyond-silicon materials in the semiconductor industry. The excellent mechanical, thermal, and electrical properties of nanotubes were able to induce investment and research from major semiconductor companies, including IBM [7]. Of particular note was the incredible mobility of the charge carriers, with measured values for electrons on the order of $100,000$ cm$^2$/Vs [8], orders of magnitude higher than the best values ever attained in silicon electronics ($1,375$ cm$^2$/Vs [9]).

The interest in alternative channel materials further exploded with the Nobel-prize-winning [10] work of Novoselov and Geim, who formed two-dimensional graphene[2] by the mechanical exfoliation of graphite using the so-called "scotch-tape method" [11]. Particularly exciting was the demonstration of intrinsic room-temperature mobilities of $200,000$ cm$^2$/Vs [12], more than double the already impressive mobility of carbon nanotubes, and higher than that of any other semiconductor. This mobility value was even better than that of copper, a metal already known for having an excellent mobility. Furthermore, because transistors fabricated from graphene consist of only a single layer of carbon atoms, the gate control is inherently excellent, and paths for leakage current are eliminated due to the very weak interactions with the underlying substrate. Due to these factors, graphene transistors can be considered as the ultimate form of the UTB-SOI transistor, although made of carbon rather than silicon.

Unfortunately, graphene has several major drawbacks. Graphene is classified as a zero-

[2]In this thesis, we consider GFETs made only with graphene in its single-layer form; hence, "graphene" always means "single-layer graphene," even when not explicitly stated.

gap semiconductor [13], *i.e.*, it does not possess a bandgap [14]. For pristine graphene, this results in current-voltage ($I$-$V$) characteristics that differ from regular MOSFET $I$-$V$ curves, as shown in Fig. 1.2; specifically, graphene exhibits *quasi-saturating* behavior, with only a temporary flattening of the $I$-$V$ characteristics, rather than full saturation [15]. Furthermore, the off-current in graphene is unusually high, resulting in $I_{\text{on}}/I_{\text{off}}$ ratios of only 2 to 20 [16], far worse than the requirements of $10^4 - 10^8$ for digital logic [17, 18]. In order to design digital circuits without prohibitively high stand-by power, a bandgap needs to be introduced into graphene. This feat can be done through the use of bilayer graphene [19], graphene antidot lattices [20], or graphene nanoribbons [21]. Introducing a gap has a cost, as each of these techniques will lower the mobility by lowering the average bandstructure velocity [22], [23], [24].

In order to avoid such issues, it is of interest to find technological applications that take advantage of graphene's incredible speed while avoiding the requirement of high $I_{\text{on}}/I_{\text{off}}$ ratios. The most obvious application is the use of graphene in analog or radio-frequency (RF) circuits[3], where on-off performance is not an essential requirement [25]. However, the lack of current saturation, due to the missing bandgap [16], will still have an impact on analog applications. Quantifying this effect is necessary to fully investigate the potential of this technology.

The successes and failures of graphene have motivated research into other two-dimensional materials. The aim is to find materials that alleviate the shortcomings of graphene, but which still offer the advantages of any structure with a two-dimensional or ultrathin body, such as excellent electrostatic behavior and gate control, and minimized leakage paths to mitigate short-channel effects. The ideal material would yield a device that exhibits both current saturation and a high $I_{\text{on}}/I_{\text{off}}$ ratio, and that retains device speed through high mobility.

[3] In this thesis, we use the terms, "analog," "high-frequency," and "radio-frequency" interchangeably.

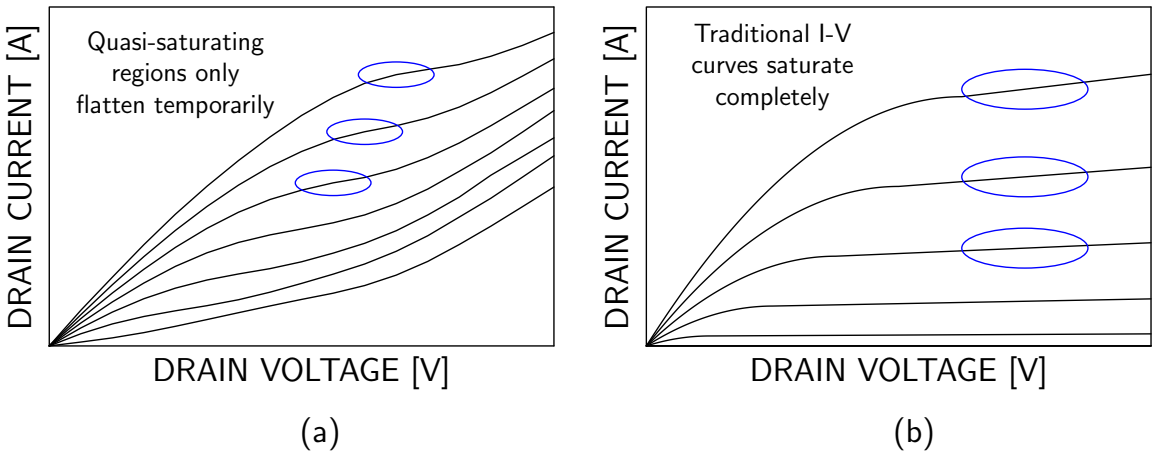



Figure 1.2: (a) Graphene vs. traditional (b) MOSFET $I$-$V$ curves. The graphene $I$-$V$ curves are generated from quantum-mechanical simulations, while the MOSFET $I$-$V$ curves are plotted using the standard piecewise functions [26].

One such material could be single-layer molybdenum disulphide (SL $MoS_2$), a member of the transition metal dichalcogenide family. Members of this family consist of a single layer of transition metal atoms sandwiched between two single layers of chalcogen atoms; certain combinations of atoms form stable structures. SL $MoS_2$ has a bandgap of 1.8 eV [27] and SL $MoS_2$ transistors thus exhibit robust current saturation. However, when compared to graphene, the measured mobility values of SL $MoS_2$ are considerably lower. The lower mobility can largely be attributed to crystal-lattice imperfections from new and unproven material-synthesis techniques, as well as the difficulty in forming low-resistance ohmic contacts; however, the high intrinsic effective mass, observed in even pristine SL $MoS_2$, will fundamentally lead to a lower mobility.

Comparing materials such as graphene and $MoS_2$, and quantifying and understanding the trade-offs between properties such as *high mobility* versus *current saturation*, is of vital importance in making decisions for the future of the electronics industry.

Overall, there is a need to examine device concepts and alternative materials to keep the semiconductor industry moving past the end of Moore's law. Both new material sys-

tems and extensions of silicon (*e.g.*, through the FinFET) require detailed investigation. All possibilities require simulation studies that include the effects of quantum mechanics, which are dominant at the nanoscale. Simulations can benefit new materials by identifying promising contenders and ruling out others, especially given that the technical challenges to fabricate high-quality prototype devices are immense. Simulation studies can also benefit silicon, by identifying quantum effects arising from the confinement of electrons in nanoscale architectures and from the anisotropy of material properties, such as effective mass, both having been historically less important in classical planar MOSFETs.

## 1.2 This Work

This thesis is based on the quantum-mechanical study of nanoscale electronic devices formed from both novel and conventional materials, and it examines how their projected performance compares to the industry-standard roadmap, the ITRS. The specific aims of the research are to utilize numerical models and simulations to accomplish the following tasks:

1. Identify how the lack of an electronic bandgap in graphene affects the operation of graphene field-effect transistors (GFETs) for RF applications.

2. Compare the RF performance of a FET fabricated with monolayer graphene to one utilizing monolayer $MoS_2$ to assess tradeoffs between bandgap and contact resistance in two-dimensional material systems.

3. Apply the knowledge gained in studying low-dimensional alternative materials in order to assess the performance potential of FinFETs over the next 10–15 years, down to 5-nm channel lengths, the end of the scaling roadmap.

The above tasks naturally lead this Ph.D. research to be partitioned into two completed stages and one future stage. The first stage is complete, with a publication in the *IEEE Transactions on Nanotechnology* [28]. The second stage is also complete, with a publication accepted by *IEEE Transactions on Nanotechnology* [29]. The third future stage has thus far produced a robust simulation tool that is being used in an industrial collaboration.

## 1.3 Stages of Work

For the convenience of the reader, we have gathered together an overview of the three stages of work, and for each stage, a summary and a description of the key points are provided below. It is important to note that the intention of the summaries and descriptions below is to convey the *essence* of each stage of work, and interested readers can find the supporting details in the subsequent chapters of this thesis.

### 1.3.1 RF Performance Limits and Operating Physics Arising from the Lack of a Bandgap in Graphene Transistors

**Summary**

We developed a simulation tool to solve the quantum-mechanical non-equilibrium Green's function (NEGF) formalism self-consistently with the Poisson equation, and we used the tool to examine the impact of graphene's lack of a bandgap on its RF performance. The primary impact of a lack of a bandgap on analog performance is the quasi-saturating current-voltage behavior of GFETs, leading to a poor output conductance, which then impacts the transistor's cutoff frequencies. Understanding this issue is of key importance in assessing the long-term commercial viability of GFETs, as recently suggested by Schwierz [16] in *Nature*. Our work was published in the *IEEE Transactions on Nanotechnology* [28].

Fig. 1.3 illustrates the GFET structure we studied. We chose an 18-nm channel length to facilitate direct comparison with current technology nodes specified by the ITRS [30].

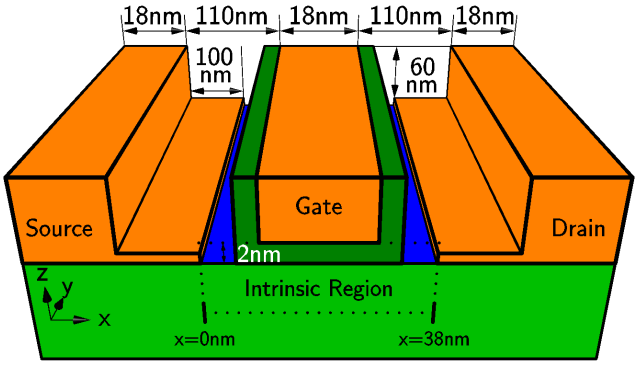



Figure 1.3: Device structure simulated in Chapter 2 of this thesis.

The intrinsic portion of the device was studied via quantum-mechanical simulation, and the impact of the external parasitics were then included with the aid of COMSOL Multiphysics [31]. A quantum-mechanical framework is necessary for the intrinsic device for two reasons. First, for short channel lengths, quantum-mechanical tunneling becomes an important factor in electron transport. Second, the linear dispersion relationship for graphene cannot be captured using semi-classical simulation approaches; semi-classical methods are based on Newtonian dynamics and hence typically require an effective mass derived from the bandstructure, whereas the linear dispersion relationship in graphene results in such an effective mass of infinity. Other effects, such as the influence of the source and drain contacts on transport, and the presence of bound channel states due to quantum-mechanical confinement, are also captured in our quantum-mechanical model.

It is worth adding here that the simulation tool developed in this stage has proven to be incredibly versatile, and it has been adapted and applied to study III-V HEMTs [32] and carbon-nanotube field-effect-transistors (CNFETs) [33]. RF linearity for graphene transistors has also been studied through an approach that uses the simulation tool as a benchmark [34, 35], and *this work has ultimately yielded remarkable agreement with ex-*

*periment [35, Fig. 19], providing a strong validation of both the tool and the techniques used throughout this thesis.*

Over and above the simulation tool, we also derived a series of expressions that relate the underlying physics, governed by the rules of quantum mechanics, to observable quantities relevant to circuit designers, such as the transconductance $g_m$ and the output conductance $g_o$; these are (2.1) and (2.14) in Chapter 2. Such expressions allowed us to distinguish effects arising from the lack of a bandgap from other effects.

**Key Points**

We found that an important bias point for graphene FETs occurs when the drain Fermi level aligns with the channel potential. Symbolically, this condition can be expressed as

$$\boxed{\mu_2 = E_{\text{ch}}} \tag{1.1}$$

as also indicated by (2.11) in Chapter 2, where $\mu_2$ is the drain Fermi level and $E_{\text{ch}}$ is the channel potential, the latter being specified in a GFET by the position of the Dirac point at the midpoint of the channel. The bias point corresponding to this condition yields maximum transconductance $g_m$, minimum total gate capacitance $C_{\text{gg}}$, and minimum output conductance $g_o$, as discussed at length in Chapter 2. For now, we need only note that the maxima and minima in $g_m$, $C_{\text{gg}}$, and $g_o$ then lead to peak values for the extrinsic cutoff frequencies $f_T$ (extrinsic unity-current-gain frequency, in the notation of Chapter 2) and $f_{\text{max}}$ (unity-power-gain frequency).[4]

While condition (1.1) does lead to peak values of the cutoff frequencies, our work shows that these peak values are curtailed in GFETs due to an unusually large output conductance $g_o$. We show that the physics contributing to the large value of $g_o$ are best understood by

[4]With respect to GFETs, in the present discussion, we adhere to the notation of Chapter 2 to distinguish between the extrinsic ($f_T$) and intrinsic ($f_{\text{T,int}}$) unity-current-gain frequencies; elsewhere in this chapter, "$f_T$" is used for both the extrinsic and intrinsic values, with the distinction either being unimportant or clear from the context.

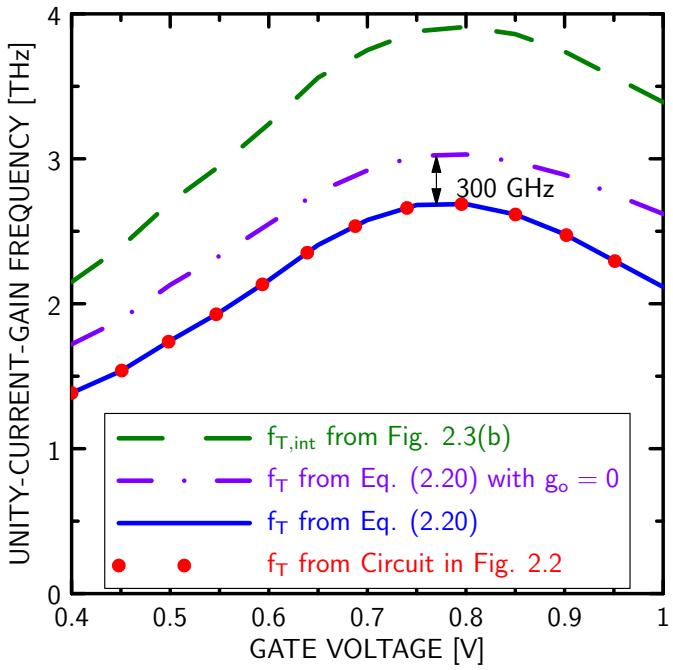



Figure 1.4: Extrinsic unity-current-gain frequency $f_T$ vs. gate voltage $v_G$ as found from (2.20). Values of $f_T$ extracted from the circuit of Fig. 2.2 in Chapter 2 are also shown to validate (2.20), and values of the *intrinsic* $f_{\text{T,int}}$ reproduced from Fig. 2.3(b) are shown for reference.

splitting it into two components,

$$\boxed{g_o \equiv \frac{\partial i_D}{\partial v_D} \equiv g_{\text{ob}} + g_{\text{oq}}.} \tag{1.2}$$

as indicated by (2.14) in Chapter 2, where $\partial i_D$ and $\partial v_D$ represent perturbations in the drain current and drain voltage, respectively, and $g_{\text{ob}}$ and $g_{\text{oq}}$ are the two components of $g_o$. The first component $g_{\text{ob}}$, called the DIBL component, is due to *conventional barrier lowering* from a perturbation in drain voltage, and it is observed in regular MOSFETs. The second component, called the quantum component $g_{\text{oq}}$, is due to *quantum-mechanical tunneling,* which can lead to changes in drain current with drain voltage in graphene, but which is absent in regular MOSFETs. The lack of a bandgap in graphene is the main reason for the

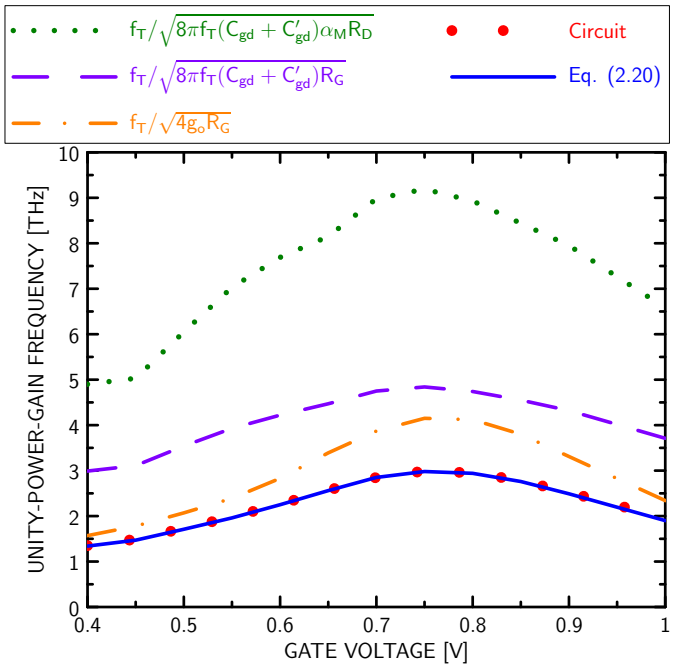



Figure 1.5: Plot of the components of the unity-power-gain frequency $f_{\max}$ according to the expression (2.21) vs. gate voltage $v_G$. Values of $f_{\max}$ obtained from the circuit of Fig. 2.2 in Chapter 2 are also shown to validate (2.21).

second component being so large with this channel material.[5]

Our studies show that the peak $f_T$ could be increased by 300 GHz, while the peak $f_{\max}$ could be doubled, if $g_o$ in GFETs could be reduced to zero. These results are illustrated in Figs. 1.4 and 1.5, respectively.

The results in Figs. 1.4 and 1.5 show that the considerable potential for graphene circuits is diminished by the absence of a bandgap in the electronic structure leading to a poor output conductance, *i.e.*, that at least a part of the performance potential suggested by the excellent mobility is lost due to poor output conductance. Nevertheless, the overall values we found for $f_T$ and $f_{\max}$, *i.e.*, the peak values in Figs. 1.4 and 1.5, exceed the targets set by the ITRS, suggesting that graphene is still a contender as a channel material for future

[5]This second component is expected to be observed in other electronic devices with quantum-mechanical tunneling, and thus the partitioning of the output conductance in (1.2) has use beyond the boundaries of this study.

electronics, despite the poor output conductance.

**Specific Contributions**

Overall, the most important results of this work were a deeper understanding of the mechanism which causes the large output conductance in graphene and a quantification of its impact on RF performance. The specific contributions are listed in Section 4.1.1.

### 1.3.2 Impact of Contact Resistance on the $f_T$ and $f_{\mathbf{max}}$ of Graphene vs. $MoS_2$ Transistors

**Summary**

The use of other two-dimensional channel materials, including SL $MoS_2$ and related transition metal dichalcogenides, is also of interest for future FETs. Such materials exhibit *non*zero bandgaps, enabling FETs to turn off, and therefore offer the potential of digital performance at a level unreachable by graphene. A nonzero bandgap also results in a significantly improved current saturation [27], and hence improved output conductance, in comparison to graphene, offering the possibility of addressing the related shortcomings of graphene for RF applications.

In the second stage, we thus extended our quantum-mechanical simulation tool from the first stage to study $MoS_2$ transistors; the quantum-mechanical approach is necessary for $MoS_2$ in order to account for significant tunneling behavior at short gate lengths. While multi-layer $MoS_2$ (ML $MoS_2$) devices exist in addition to SL $MoS_2$, we focused on the latter, both because it is amenable to analysis and because the environment of an SL $MoS_2$ FET more closely matches the environment of a graphene FET (as discussed further below). However, due to the greatly reduced mean-free path in SL $MoS_2$ vs. graphene (7.5 nm [36] for SL $MoS_2$ vs. over 1 $\mu$m [37] in graphene), phonon scattering had to be incorporated into the NEGF formalism for SL $MoS_2$. Using the same structure for each material, as specified from the ITRS for the 7-nm node [3], and shown in Fig. 1.6, we compared graphene and

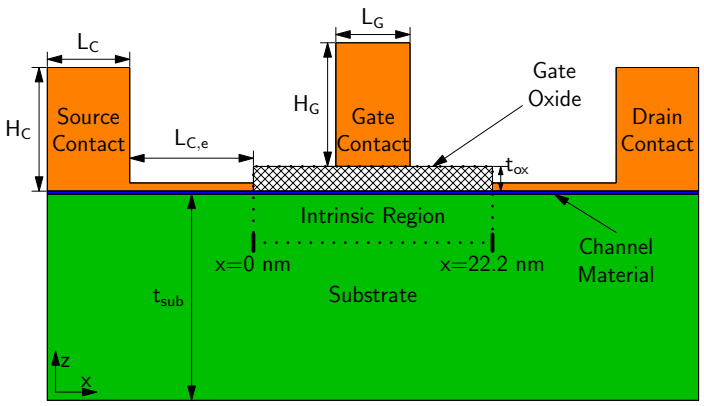



Figure 1.6: Common device structure used in Chapter 3. The dimensions are given in Tables 3.1 and 3.2. The dotted lines show a cross-section of the intrinsic portion of the device, defined as the core of the structure excluding parasitics.

SL $MoS_2$ in terms of RF performance, through the $g_m$, $f_T$, and $f_{\max}$, under different bias conditions. Our work has been accepted by *IEEE Transactions on Nanotechnology* [29].

Current experimental work on SL and ML $MoS_2$ transistors is limited, and is focused on developing acceptable fabrication techniques [38, 39, 40, 41, 42, 43, 44, 45, 46]. Methods to deposit large areas of $MoS_2$ are still unknown; mechanically exfoliated layers cover tiny areas, and attempts at chemical vapor deposition (CVD) produce $MoS_2$ with a large number of defects and contamination [47, 48, 49]. Doping is another challenge [50, 51, 52, 53], though surface doping looks to be a promising technique [54, 55]. Developing ohmic contacts remains a critical challenge [56, 57, 58, 59, 60, 52, 61, 62, 63]. The traditional method of matching the electron affinity in the semiconductor to the metal work function totally fails, as a significant level of Fermi-level pinning is observed [56, 64]; further complicating this situation is the observation that traditional models for Fermi-level pinning do not explain the experimentally observed behavior [65]. As a result of these fabrication issues, only long-gate length $MoS_2$ transistors with large contact resistances have been experimentally studied. In addition, only a few $MoS_2$ circuits have been experimentally studied [66, 67, 68], and to date there have has only been a handful of studies that focus

specifically on the *RF* performance of $MoS_2$ transistors [69, 70, 71].

The early results for $MoS_2$ FETs have remained well below the observed values for graphene. $f_T$ values up to 42 GHz and $f_{\max}$ values up to 50 GHz [70] have been achieved with ML $MoS_2$, while for SL $MoS_2$, the peak values are lower, with a measured $f_T$ of 6.7 GHz and $f_{\max}$ of 5.3 GHz. This outcome can be attributed to the long gate lengths and the fabrication deficiencies listed above, especially the large contact resistance. Therefore, *the main goal of our simulations was to assess the ultimate performance of $MoS_2$ vs. graphene, with contact resistance and scaling (gate length) carefully considered*.

To do this work, we extended the quantum-mechanical device solver from the first stage to the $MoS_2$ material system, using an effective-mass model within the NEGF framework [72, 73, 74]. Several sources of phonon scattering were included into the simulation of $MoS_2$ devices, including both elastic (transverse and longitudinal acoustic) and inelastic (longitudinal optical, homopolar, and Fröhlich interaction) phonons. The simulation approach for graphene remained the same as in the first stage, with the NEGF formalism being solved under the condition of ballistic transport and a tight-binding Hamiltonian. The comparison between graphene and SL $MoS_2$ was aided by the relative similarity of the structures in each system, as both are single-layer materials. Therefore, several of the characteristics of the two systems, such as the electrostatic behavior of the contacts on the channel and the observed parasitic capacitances, can be considered identical for SL $MoS_2$ and graphene, with the fundamental performance and behavior of each material then being determined by the difference of the electronic bandstructures and the quality of the contacts.

To address the issue of scaling, we assumed a short gate-length transistor (corresponding to the 7-nm node) made with both materials, and to address the issue of contact resistance, the reduction of which is critical to make two-dimensional materials viable and which has already been flagged as a limiter of SL $MoS_2$ FETs, we focused on RF perfor-

mance as a function of realizable contact resistance $\rho_C$.

Our approach was verified by comparing to the available experimental data. Trend lines, extrapolated from the values of $f_T$ reported in the literature, were compared to our simulations. Extrapolation was required because our simulation domain was consistent with upcoming technology nodes (7 nm) whereas typical channel lengths for experimental studies on SL $MoS_2$ and graphene are at least an order of magnitude larger.

**Key Points and Specific Contributions**

The details of the comparison are best understood via the discussion in Chapter 3, which we will not attempt to reproduce or capture in the present chapter, since it requires a careful step-by-step development.[6] Rather, we simply note the main conclusion, namely, that the poor quality of SL $MoS_2$ contacts gives graphene a substantial performance edge in terms of *peak* (over all bias conditions) RF performance, whereas once a comparison is made under the constraint of a fixed bias current (*e.g.*, for low-power applications), $MoS_2$ looks far more competitive, with the ability to meet or exceed graphene's benchmarks by achieving contact resistances already exhibited in experimental ML $MoS_2$ structures. The specific contributions related to this result are available in Section 4.1.2.

In the present discussion, we highlight the agreement between experiment and our simulations, as shown by the comparison of $f_T$ to gate length $L_G$ in Fig. 1.7, replicated from Section 3.7.

While in general there have been many experimental studies of graphene and $MoS_2$ devices, the literature available with measured $f_T$ and $f_{\max}$ is limited. For comparison to experiment, we restricted our attention to the $f_T$, where sufficient experimental data is available to establish trends, and since $f_T$ is far less sensitive to device layout in comparison

[6] While the results of Chapter 3 employ a quantum-mechanical simulation approach, the discussion itself does not utilize quantum mechanics; hence, virtually any interested reader of this thesis can easily follow the full discussion in Chapter 3.

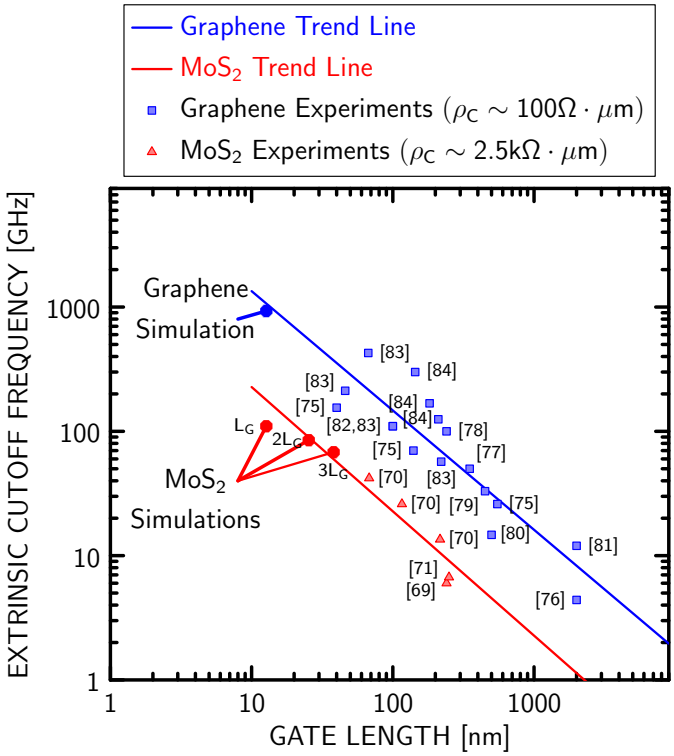



Figure 1.7: Experimental data for peak $f_T$ vs. gate length $L_G$ for $MoS_2$ and graphene devices, with our simulation results superimposed. Experimental data for graphene is from [75, 76, 77, 78, 79, 80, 81, 82, 83, 84], and experimental data for $MoS_2$ is from [70, 69, 71]. The trend line for graphene applies for a contact resistance $\rho_C \sim 100\ \Omega \cdot \mu\text{m}$ and that for $MoS_2$ applies for $\rho_C \sim 2.5\ \text{k}\Omega \cdot \mu\text{m}$.

to $f_{\text{max}}$.

Fig. 1.7 shows a summary of available experimental results of peak $f_T$ vs. $L_G$ for $MoS_2$ and graphene devices; for the purpose of the present comparison, where only trends are of interest, we need not distinguish between experimental values found from single- vs. multi-layer structures. We have superimposed our own single-layer simulation results on this graph, found for devices with gate lengths on or about that for the 7-nm technology node (corresponding to a gate length of 12.7 nm).

Consider first the results for graphene. Since the majority of the graphene experimental $f_T$ values have been achieved with a contact resistance on the order of 100 to 200 $\Omega \cdot$

$\mu$m [83, 79, 82], we have added our simulated graphene $f_T$ for a 7-nm node device, having a gate length of 12.7 nm, with an assumed contact resistance of 100 $\Omega \cdot \mu$m. It is important to note that our simulation result includes all quantum-mechanical effects in the device *and* the effect of device parasitics, particularly the contact resistance $\rho_C$. As shown in Fig. 1.7, our simulation result shows good agreement with the trend line found from a linear regression against the graphene data.

There is far less data available on the $f_T$ for $MoS_2$, making it difficult to reliably extract a scaling trend. A starting point is a study [70] that included an examination of $f_T$ vs. $L_G$; this work, in which $\rho_C = 2.5$ k$\Omega \cdot \mu$m, showed a strong $1/L_G$ scaling behavior for $MoS_2$ devices. The $1/L_G$ scaling behavior can be combined with the best experimental $f_T$ values at a number of gate lengths, extracted from [70, 69, 71], to draw a trend line for $MoS_2$ in Fig. 1.7. The line is anchored at a point specified by an average of the experimental data, and it provides an idea of where the $f_T$ values for $MoS_2$ devices should lie at shorter gate lengths, provided $\rho_C \sim 2.5$ k$\Omega \cdot \mu$m, the value used in all but one of the experiments; in that one experiment, $\rho_C$ is slightly higher at $3.1$ k$\Omega \cdot \mu$m, a detail that can be overlooked for the purpose of our comparison. We have additionally superimposed our simulation data for the $f_T$ of $MoS_2$ devices at shorter gate lengths; in doing so, we chose $\rho_C = 2.5$ k$\Omega \cdot \mu$m to be consistent with the experiments, and in addition to showing the result for $L_G$=12.7 nm, applicable to the 7-nm ITRS node, we have added simulation data for the peak $f_T$ at twice and three times this gate length. The simulation results, which again include both quantum-mechanical effects in the channel and the impact of device parasitics, are consistent with the experimental trend line.

*The agreement between our simulation approach and experimental trends* in Fig. 1.7 not only lends strong support to our work in stage II, *i.e.*, to the specific conclusions regarding the RF performance of SL $MoS_2$ vs. graphene (summarized in Section 4.1.2), but also *lends strong support to the modeling approach used throughout this thesis*. In mak-

ing this observation, it is important to bear in mind that the agreement was found for two different materials, accounting for *both* quantum-mechanical transport in the channel *and* device parasitics, and with the key parasitic anchoring the curves (the contact resistance) *chosen (not fitted)* to be consistent with experiment.[7]

### 1.3.3 Future Work: Understanding FinFETs to the End of the Roadmap

**Summary**

The experimental agreement in Fig. 1.7, and in [35, Fig. 19], illustrate the utility and predictive power of the tool developed for the studies in this thesis. Motivated by such agreement, for future work, we will apply the expertise gained from the quantum-transport projects on two-dimensional materials to study the behavior of transistor devices relevant to the semiconductor industry. Silicon FinFETs represent the technology most relevant to the semiconductor industry for the next several years.

Due to their thinness, quantization effects are important in FinFETs, and due to the short channel lengths of today's transistor technologies, so is quantum-mechanical tunneling. Being able to understand how quantum effects scale is necessary in order to better design processes for future technology nodes, and a knowledge of the device physics is necessary for circuit design, especially for RF applications. The addition of phonon scattering, a key driver to determining the mobility of a material, is also critical to fully understand scaling. Without the inclusion of quantum-mechanical effects or phonon scattering, any calibration to FinFETs will not have a physical basis, and will therefore be unable to pre-

[7] It is worth adding a note regarding the first data point at $L_G = 12.7$ nm for SL $MoS_2$ in Fig. 1.7. While further study is no doubt required, we believe this data point, which lies strictly a bit below the trend line, may be reflecting a reality; scaling of $MoS_2$ devices will not follow the expected trend established by long-channel devices (the $1/L_G$ scaling trend line in Fig. 1.7), but will droop below it *unless* the contact resistance is improved from the value of $\rho_C \sim 2.5\ \mathrm{k\Omega} \cdot \mu\mathrm{m}$ applicable to today's long-channel experimental results. A high $\rho_C$ causes the device parasitics to dominate $f_T$ at short channel lengths, offsetting improvements that could otherwise be obtained with further $L_G$ downscaling.

dict scaling behavior. To date, no physics-based tool which includes quantum-mechanical effects, phonon scattering, and calibration to real technology exists for FinFETs. Such a tool would be useful to quickly assess the impact of modifications to the fin structure or material systems. In this final stage of work, we propose an extension to our quantum-mechanical simulation tool that can be used to understand the device physics of FinFETs, to reproduce the terminal characteristics of real devices, and to predict scaling behavior, with a focus on RF performance, as with the two-dimensional materials we already considered.

**Key Points**

Like with the two-dimensional materials of the first two studies, the primary advantage of FinFETs is due to the improved electrostatic control of the channel, this time through wrap-around gates in addition to a thin channel. Major manufacturers, including IBM [85], Intel [86], and TSMC [87] have all moved their semiconductor processes to FinFET technology, and hence FinFETs represent the state-of-the-art in semiconductor technology.

The proposed future work is already underway, with our quantum-mechanical simulation tool already successfully extended to simulate a silicon FinFET. As a starting point, the solver has been modified to utilize an effective-mass Hamiltonian in two or three dimensions, using a coupled mode-space approach [88]. For tall fins, where the height of the fin is much larger than the fin width, the two-dimensional approach is sufficient, while the three-dimensional approach is appropriate for nanowire devices with shorter fins.

We will incorporate our phonon scattering framework, first used in the simulation of $MoS_2$ transistors; work to incorporate this with the coupled mode-space Hamiltonian is underway. The impact of phonon scattering is expected to diminish as the channel length of devices shrink; however, it is an open question as to what extent this will happen.

By leveraging the expertise gained from the studies involving graphene and $MoS_2$, we also have the framework necessary to interpret the results from the more complicated fin

structure; specifically, the boxed expressions in Chapter 2 for quantities such as $g_m$ and $g_o$ apply to all field-effect transistors and provide a general framework for a comparison of devices from detailed quantum-mechanical simulation results.

Future modifications will include the effects of surface roughness, strain, and other channel materials (*i.e.* silicon germanium SiGe) [89]. The aim of such improvements to our solver will be to better match the performance of current FinFET technologies at the 10-nm node, and to use this calibration to predict the performance of FinFETs at the end of the ITRS roadmap.

Calibrations will be performed with the help of low-temperature measurements through an industrial collaboration with IBM. Input from our industrial collaborators at Qualcomm will be used as guidance to ensure that the studies are of high-impact.

# Chapter 2

# RF Performance Limits and Operating Physics Arising from the Lack of a Bandgap in Graphene Transistors

## 2.1 Introduction

Since first being used for a field-effect transistor (FET) in 2004 [11], graphene has recently gained great attention as a possible channel material for high-frequency devices. The advancement of graphene transistor technology has been rapid, with the time from initial studies to a functioning GHz-speed radio-frequency (RF) transistor being nearly three times as fast as with carbon nanotubes (CNs) [16]. Currently, the fastest graphene FET (GFET) has a projected intrinsic $f_{\mathrm{T,int}}$ of 1.4 THz [90], compared with a record of 153 GHz for an array-based carbon-nanotube FET (CNFET) [91].

While several issues still exist in the fabrication of GFETs—such as the creation of high-quality monolayer transistors over a large area [92] and the reduction of access resistance between the channel (under the gate) and the source and drain contacts [90]—a feature unique to GFETs is the lack of an electronic bandgap [14, 93]. The lack of a bandgap leads to a lack of current saturation and hence a pronounced output conductance, which in turn is deleterious to the RF performance [93].

Several methods have been suggested to introduce a bandgap into graphene devices,

including the use of graphene cut into the form of nanoribbons [21], graphene formed with an antidot lattice [20], and graphene in bilayers [22]. Alongside such experimental work, simulation can be used to better understand the physics of transistor operation and the limitations on transistor performance imposed by the lack of a bandgap.

Early work on the simulation of graphene-based transistors focused on nanoribbon devices (possessing a bandgap) rather than those made with wide graphene sheets (having zero bandgap), and they utilized a semiclassical top-of-the-barrier model [23]. The first quantum-mechanical simulation studies began in 2007 [94, 95], and they again focused on nanoribbon transistors; published works on the RF potential of nanoribbon FETs include those that have considered device scaling [96, 97], Schottky-barrier operation vs. MOSFET-like operation [98], and bias optimization [99]. Quantum-mechanical work based on wide graphene sheets has been limited and has focused on studying $pn$-junctions [100] and Schottky-barrier devices [101, 102]; there has yet to be an in-depth quantum-mechanical study on the high-frequency performance of wide graphene sheets under MOSFET-like operation.

This work considers the RF potential of graphene transistors with MOSFET-like operation, with a particular focus on the absence of a bandgap. We use a fully quantum-mechanical approach to carefully describe the physics that determine the key RF metrics when there is no bandgap, including the transconductance, gate-input capacitance, and output conductance. We are also able to quantify the extent to which the lack of a bandgap limits the unity-current-gain and unity-power-gain frequencies. Our work hence allows us to provide an alternative and more detailed description of the device physics and implications of zero bandgap than recently discussed via the semiclassical approaches in [103] and [104]. Our approach is also more suited to study the performance potential of short-channel GFETs (having channel lengths below 20 nm) than approaches utilizing drift-diffusion models [105, 106] or Monte Carlo methods [107], since the latter methods

exclude or approximate quantum-mechanical effects present in short channels. However, it should be noted that drift-diffusion and Monte Carlo approaches do have the ability to account for scattering. While scattering is most important for long channels, the inclusion of scattering in future quantum-mechanical work will be necessary to get a more complete view of the transport in short channels. Scattering effects in quantum-mechanical models have only previously been considered in the context of Schottky-barrier operation using finite-difference discretized Hamiltonians [101, 102].

Our simulations are guided by the specifications for *RF CMOS millimeter-wave (10-100 GHz) technology* in the International Technology Roadmap for Semiconductors (ITRS) for the year 2015 [30]. Of course, graphene FET fabrication techniques have yet to mature to an extent needed to achieve the ITRS requirements; we use the ITRS specifications only as a benchmark for GFET technology going forward, as we did in [108, 109] for CNFETs. Guided by the ITRS, we employ a gate length of 18 nm and an equivalent oxide thickness (EOT) of 0.75 nm.

The simulation is carried out in two steps. First, our own self-consistent quantum-mechanical solver for GFETs (developed at the University of Alberta [33, 32]) is used to find the intrinsic characteristics of the device under ballistic conditions; we employ the method of non-equilibrium Green's functions (NEGF) together with the Poisson equation. Second, an electrostatic simulation is performed on an open-pad structure in COMSOL multiphysics [31] in order to determine the parasitic capacitances; we combine this data with theoretical values for the contact resistances in order to form an extrinsic circuit, which is then used to determine the extrinsic figures of merit.

The main outcome of our work is the extraction of both intrinsic and extrinsic RF figures of merit, together with a clear connection of their behavior to the device physics based on a fully quantum-mechanical approach. Of particular interest is the impact of a zero bandgap on the output conductance, which we show can dominate the RF behavior. Suggestions are

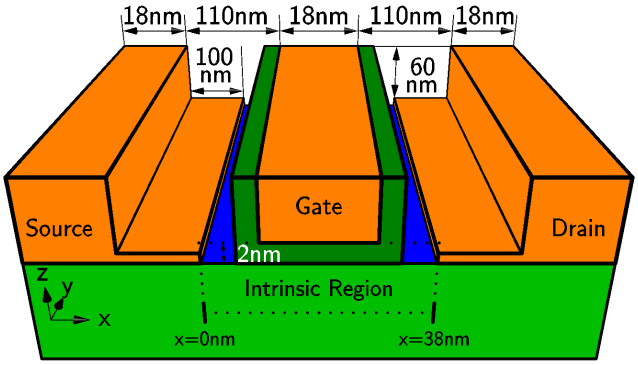



Figure 2.1: Device simulated in this study. The gate length is 18 nm and 2 nm of $Al_2O_3$ is used as the gate oxide. A cross-section of the intrinsic region is indicated by the dotted lines. The source and drain geometries are symmetric with respect to the gate. The positions $x = 0$ and $x = 38$ nm, which delimit the intrinsic portion of the device, are labeled for later reference.

also made for the proper biasing of graphene FETs to achieve optimum RF performance, which we show is more than adequate to keep pace with the ITRS [30], despite the lack of a bandgap.

Section 2.2 of this chapter briefly outlines the simulation approach. Intrinsic results are presented in Section 2.3, extrinsic results are presented in Section 2.4, and the conclusions are presented in Section 2.5.

## 2.2 Approach

### 2.2.1 Device Structure

The device structure utilized for the simulations is shown in Fig. 2.1. Key device dimensions are indicated in the figure and $Al_2O_3$ (relative permittivity $\epsilon_r = 9.8$) is used as the gate oxide. The choice of $Al_2O_3$ is motivated by its excellent promise as a possible high-$k$ dielectric compatible with graphene and its regular use in experimental work [12, 110, 111]. We use 2 nm of $Al_2O_3$ to replicate the ITRS EOT of 0.75 nm with $SiO_2$ [30]. The graphene

in the source and drain regions is $n$-doped with a concentration $N_D = 1.9 \times 10^{17}$ m$^{-2}$ while the channel is left undoped; only the electron branch of the current-voltage characteristics is considered within this doping scheme.

### 2.2.2 Intrinsic Device Simulation

#### Overview

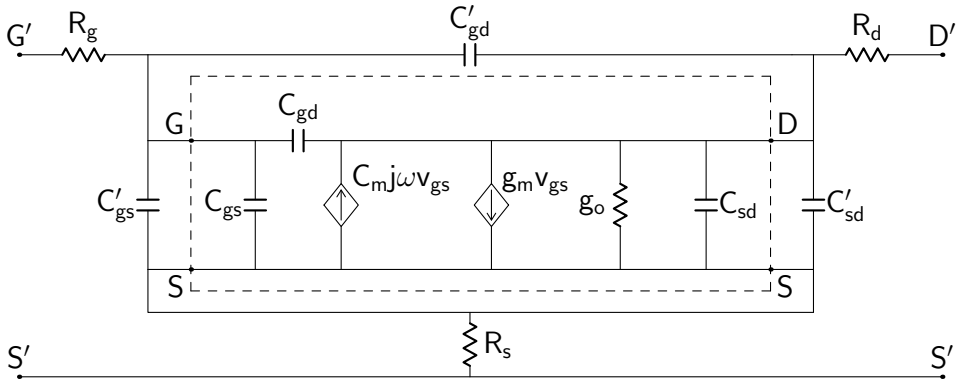
The intrinsic simulation was carried out with our quantum-mechanical device solver applied to the dotted portion of Fig. 2.1. The solver computes the Poisson equation in two dimensions (along $x$ and $z$) self-consistently with the NEGF formalism (along $x$) in order to capture both electrostatic and charge-transport effects. Simulations were carried out under ballistic conditions, which can be justified by the small gate length assumed in this study and by the aim of this work to provide a first-order assessment and understanding of the RF capabilities of GFETs. The self-consistent solver enables the extraction of the intrinsic circuit elements, *i.e.*, those contained within the boxed portion of Fig 2.2(a); the definitions of these elements are given in Fig 2.2(b) [112, Ch. 8].

#### Poisson Solver

In the same vein as the standard analysis of CMOS devices, a two-dimensional computational domain (along $x$ and $z$) for the Poisson equation (discretized with finite differences) is used for simulating GFETs; this assumes that the potential across the graphene sheet perpendicular to the transport direction (along $y$) does not vary, as would be expected with an infinitely wide sheet.

#### NEGF Solver

The NEGF solver utilizes a nearest-neighbor, tight-binding Hamiltonian with a $p_z$-orbital basis [114]. In order to facilitate a numerical solution, Bloch boundary conditions are imposed in the direction transverse to charge transport (along $y$), which results in a series




(a)

$$C_{gs} = -\frac{\partial q_G}{\partial v_S} \qquad C_{gd} = -\frac{\partial q_G}{\partial v_D} \qquad C_{dg} = -\chi\frac{\partial q_I}{\partial v_G}$$

$$C_m = C_{dg} - C_{gd} \qquad C_{sd} = -(1-\chi)\frac{\partial q_I}{\partial v_D}$$

$$g_o = \frac{\partial i_D}{\partial v_D} \qquad g_m = \frac{\partial i_D}{\partial v_G}$$

(b)

Figure 2.2: (a) Equivalent circuit used in this study, with the intrinsic portion boxed. The labels $S$, $D$, and $G$ refer to the source, drain, and gate terminals, respectively, of the intrinsic device, while their primed counterparts $S'$, $D'$, and $G'$ refer to the corresponding extrinsic device terminals. (b) Definition of the intrinsic elements, where the symbols have their usual meanings [112, Ch. 8]. The value of the charge-partitioning factor $\chi$ has a negligible impact on the results of this work; for completeness, we chose $\chi = 1$ based on the short length of our $n^+$ regions [113].

of orthogonal one-dimensional transport modes (along $x$). The orthogonality is ensured by the lack of scattering and the assumption of a constant potential along the width of the sheet. Numerically, the contact self-energies are calculated using the Sancho-Rubio iterative method [115], while the NEGF equations are solved utilizing the recursive Green's function technique [116] under ballistic conditions.

### 2.2.3 Extrinsic Device Simulation

To augment the intrinsic model, parasitic capacitances and contact resistances are added to the intrinsic circuit. The parasitic capacitances are found by simulating an open structure. The open structure consists of the entire device region, including the full metal contacts, but excludes the graphene sheet. The parasitic capacitances are extracted by applying a small voltage to each contact in turn and measuring the charge induced on the other contacts while the potential on the latter is held constant. COMSOL Multiphysics [31] was used to perform this task. For the contact resistances, experimental values from the literature were used. The contact resistances and parasitic capacitances were then added to the boxed portion of Fig. 2.2(a), yielding the overall circuit.

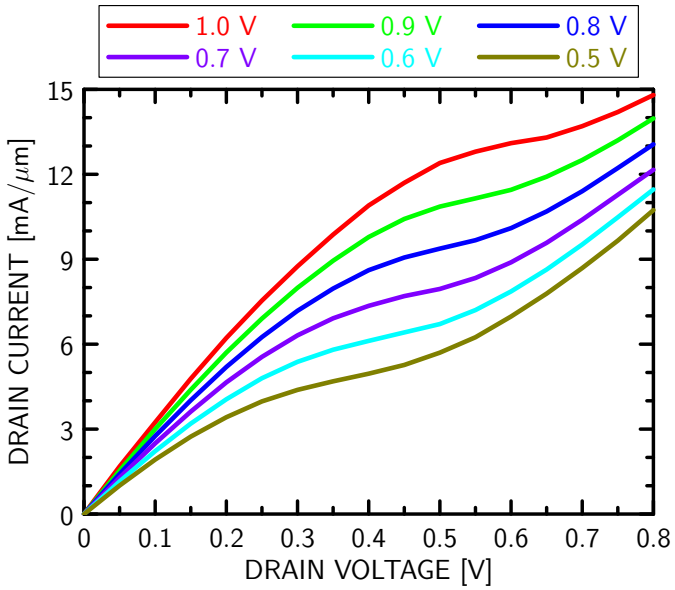
## 2.3 Intrinsic Results

### 2.3.1 Terminal Characteristics

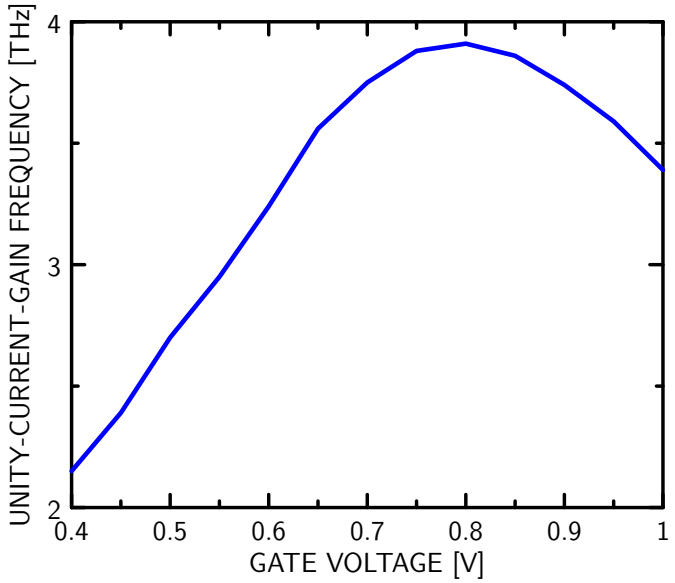
Fig. 2.3 shows the intrinsic terminal characteristics of the GFET; part (a) shows the extracted current-voltage curves and part (b) shows the intrinsic unity-current-gain frequency $f_{\text{T,int}}$ vs. gate voltage $v_G$, found with the drain voltage $v_D$ held at $V_{\text{DD}}/2$ for the maximum possible signal swing at the output, where $V_{\text{DD}} = 1.0$ V is used to correspond to the ITRS specification for the year 2015 [30]. Here, and elsewhere, we take the source as the reference: $v_S \equiv 0$.

The results in Fig. 2.3(a) depict the well-known lack of current saturation at high $v_D$ that occurs in graphene devices and that has been observed in experiments [15]; the lack of saturation arises primarily from the lack of a bandgap and leads to an undesirably high output conductance $g_o$.[1] Fig. 2.3(b) shows the $f_{\text{T,int}}$ rising with $v_G$ to a peak and then falling off. In what follows, we carefully explain the behavior of both $g_o$ and $f_{\text{T,int}}$ in graphene

[1] Saturation in long-channel devices (not considered in this work) will additionally be influenced by velocity saturation through phonon and impurity scattering [117], [118].




(a)




(b)

Figure 2.3: Intrinsic terminal characteristics of the GFET under study, with the source used as the reference ($v_S \equiv 0$). (a) Drain current $i_D$ vs. drain voltage $v_D$ for various values of the gate voltage $v_G$. (b) Intrinsic unity-current-gain frequency $f_{\mathrm{T,int}}$ vs. gate voltage $v_G$, found with $v_D = V_{\mathrm{DD}}/2 = 0.5$ V.

devices with the aid of novel expressions that shed insight into the detailed device physics. For reference, the intrinsic circuit parameter values for the device under study are provided in Table 2.1; the values are quoted at an operating point corresponding to the peak $f_{\text{T,int}}$ in Fig. 2.3(a), *i.e.*, $v_G = 0.8$ V and $v_D = 0.5$ V, where the RF performance can be expected to be optimal.

Table 2.1: Intrinsic Circuit Elements at Peak $f_{\text{T,int}}$

| $C_{\text{gd}}$ **[aF/$\mu$m]** | $C_{\text{gs}}$ **[aF/$\mu$m]** | $C_{\text{sd}}$ **[aF/$\mu$m]** | $C_m$ **[aF/$\mu$m]** | $g_m$ **[mS/$\mu$m]** | $g_o$ **[mS/$\mu$m]** |
|---|---|---|---|---|---|
| 220 | 385 | 0 | 385 | 14.9 | 5.8 |

### 2.3.2 Intrinsic Unity-Current-Gain Frequency

The intrinsic unity-current-gain frequency can be written as the ratio $f_{\text{T,int}} = g_m/(2\pi C_{\text{gg}})$, where $g_m$ is the transconductance and $C_{\text{gg}}$ is the capacitance seen looking into the intrinsic gate, defined as $C_{\text{gg}} = \partial q_G/\partial v_G$ with $v_S$ and $v_D$ held constant and given by $C_{\text{gg}} = C_{\text{gs}} + C_{\text{gd}}$ in terms of the elements in Fig. 2.2. The $g_m$ and $C_{\text{gg}}$ are plotted in Fig. 2.4.

#### Transconductance

A useful relationship for $g_m$ (derived in Appendix A) is

$$\boxed{g_m = G_0 \left(1 - \frac{C_{\text{gg}}}{C_{\text{ox}}}\right) \int_{-\infty}^{\infty} \frac{\partial T(E)}{\partial E} \left[f_1(E) - f_2(E)\right] \, dE} \tag{2.6}$$

where the symbols are as follows: $G_0 = 2q^2/h$ is the quantum of conductance, with $q$ being the magnitude of the electronic charge and $h$ being Planck's constant; $C_{\text{ox}}$ is the gate electrostatic capacitance; $T(E)$ is the total transmission function including all conducting channels; and $f_1(E)$ and $f_2(E)$ are the source and drain Fermi functions, respectively, given by

$$f_{1,2}(E) = \frac{1}{1 + \exp[(E - \mu_{1,2})/k_B T_L]} \tag{2.7}$$

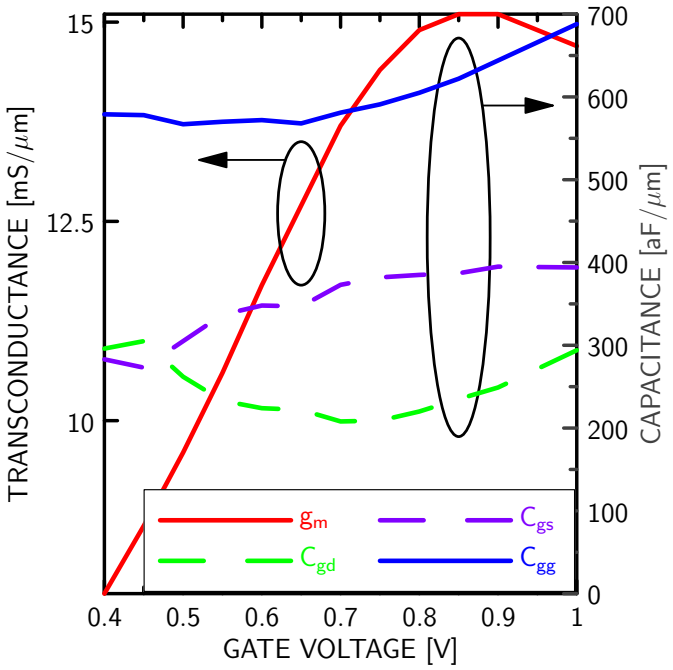



Figure 2.4: Transconductance $g_m$ and gate capacitance $C_{\text{gg}}$ vs. gate voltage $v_G$ for the GFET. The components $C_{\text{gs}}$ and $C_{\text{gd}}$ of $C_{\text{gg}}$ are also shown, where $C_{\text{gg}} = C_{\text{gs}} + C_{\text{gd}}$. The drain voltage $v_D$ is held fixed at $V_{\text{DD}}/2 = 0.5$ V.

with $\mu_1 = \mu - qv_S$ being the source Fermi level, $\mu_2 = \mu - qv_D$ being the drain Fermi level, $\mu$ being the equilibrium Fermi level, $k_B$ being Boltzmann's constant, and $T_L = 300$ K being the lattice temperature.

Since $G_0$ is a constant, (2.1) reveals that two quantities can impact the $g_m$. The first is the capacitance factor $(1 - C_{\text{gg}}/C_{\text{ox}})$, which represents the effectiveness of an incremental gate voltage $\partial v_G$ in yielding an incremental change in the channel potential $\partial E_{\text{ch}}$ [as shown by (A.2) and (A.10) in Appendix A]:

$$\partial E_{\text{ch}} = -q\partial v_G \left(1 - \frac{C_{\text{gg}}}{C_{\text{ox}}}\right) \tag{2.8}$$

where $E_{\text{ch}}$ in a graphene device (having no bandgap) can be taken to be the position of the Dirac point at the midpoint of the channel. The second is the integral, over all energies, of the responsivity in the transmission function [represented by $\partial T(E)/\partial E$] multiplied by

the "difference in agenda" [119, Ch. 1] between the source and drain contacts [represented by $f_1(E) - f_2(E)$]. Overall, for a high $g_m$, we thus not only need the gate to effectively modulate the channel through a favorable capacitance factor $(1 - C_{\text{gg}}/C_{\text{ox}}) \to 1$, but also require a strong responsivity in the transmission function $\partial T(E)/\partial E$ at those energies where a nonzero difference in agenda $f_1(E) - f_2(E)$ exists.

The integral in (2.1) takes a particularly simple form at zero temperature, when the Fermi functions (2.7) reduce to step functions centered around $\mu_1$ and $\mu_2$:

$$\int_{-\infty}^{\infty} \frac{\partial T\left(E\right)}{\partial E} \left[f_1\left(E\right) - f_2\left(E\right)\right] \, dE = T\left(\mu_1\right) - T\left(\mu_2\right) \tag{2.9}$$

which suggests that *the $g_m$ is proportional to the difference in transmission at the source and drain Fermi levels*. While approximate, we can use this result even when $T_L \neq 0$ to qualitatively understand the bias dependence of the $g_m$.

First consider the three parts of Fig. 2.5, which show the situation in a GFET at gate and drain biases sufficient to create appreciable current; for the device under study, this corresponds to $v_G = 0.4$ V and $v_D = V_{\text{DD}}/2 = 0.5$ V. Part (a) shows the spectral function (local density of states) $A(x, E)$ and the Dirac point $E_D(x)$ vs. position $x$, part (b) shows the spectral function $A(x, E)$ at the midpoint of the channel ($x = 19$ nm in Fig. 2.1) vs. energy $E$, and part (c) shows the corresponding transmission function $T(E)$ vs. energy $E$. Focusing on parts (a) and (b), it is evident that the number of states available for transport increases with energy $E$ for $E \geq E_{\text{ch}}$ and is diminished for energies $E_D(0) \leq E \leq E_{\text{ch}}$, where the latter can be attributed to the potential barrier depicted by the shape of $E_D(x)$. In graphene, this yields a transmission $T(E)$ that increases linearly for energies $E \geq E_{\text{ch}}$ and which is curtailed for $E_D(0) \leq E \leq E_{\text{ch}}$, as shown in part (c). It is worth mentioning that the asymmetry in states [and hence $T(E)$] about $E_{\text{ch}}$ is unique to our quantum-mechanical approach; semiclassical top-of-the-barrier models, such as those in [103] and [104], effectively assume a symmetrical distribution of states (and hence transmission) about $E_{\text{ch}}$.

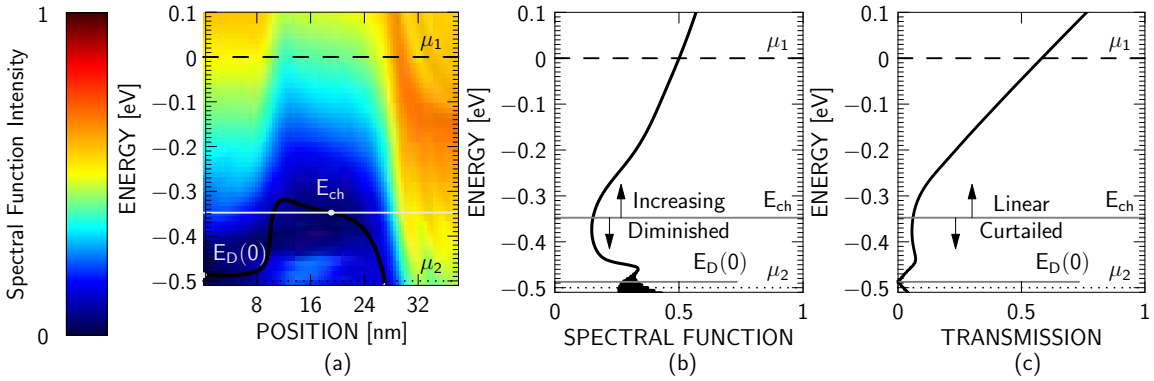



Figure 2.5: Simulation results showing: (a) the spectral function $A(x, E)$ (plotted as an intensity) vs. position $x$ in the transport direction, with a superimposed sketch of the Dirac-point energy $E_D(x)$ vs. $x$; (b) spectral function $A(x, E)$ at the midpoint of the channel ($x = 19$ nm in Fig. 2.1) vs. energy $E$; and (c) the transmission function $T(E)$ vs. $E$. Marked in the plots are the source and drain Fermi levels ($\mu_1$ and $\mu_2$), the channel potential $E_{\text{ch}}$, and the Dirac-point energy $E_D(0)$ at the source. The results are shown for $v_G = 0.4$ V and $v_D = V_{\text{DD}}/2 = 0.5$ V. For simplicity in plotting, the scaling of the spectral intensity in part (a) and the scaling on the spectral and transmission axes in parts (b) and (c) have been normalized to unity; the values shown are hence relative, not the actual values of $A(x, E)$ and $T(E)$. For the spectral function in (a), dark blue indicates a low spectral intensity while orange and red indicate a high spectral intensity.

As the gate voltage is increased, the entire picture in Fig. 2.5 can be visualized as being "pushed down." We have illustrated the situation schematically in the three parts of Fig. 2.6, shown for $v_G = 0.45$, $0.75$, and $0.95$ V, using a linear form for $T(E)$ for $E \geq E_{\text{ch}}$ and $T(E) \approx 0$ for $E_D(0) \leq E \leq E_{\text{ch}}$; we have also sketched the difference $T(\mu_1) - T(\mu_2)$ that impacts the $g_m$ according to (2.9). Initially, $T(\mu_1)$ increases with $v_G$, while $T(\mu_2) \approx 0$; at $v_G = 0.75$ V, the channel potential has been sufficiently pushed down to be aligned with $\mu_2$, and for higher $v_G$, $\mu_2$ moves into the range of energies corresponding to the linearly increasing portion of $T(E)$, such that the difference $T(\mu_1) - T(\mu_2)$ saturates. These observations are consistent with the behavior of $g_m$ in Fig. 2.4, which shows that $g_m$ increases with applied gate voltage and then begins to saturate for $v_G \geq 0.75$ V.

The eventual slight decrease in $g_m$ for $v_G \geq 0.9$ V can be attributed to the capacitance

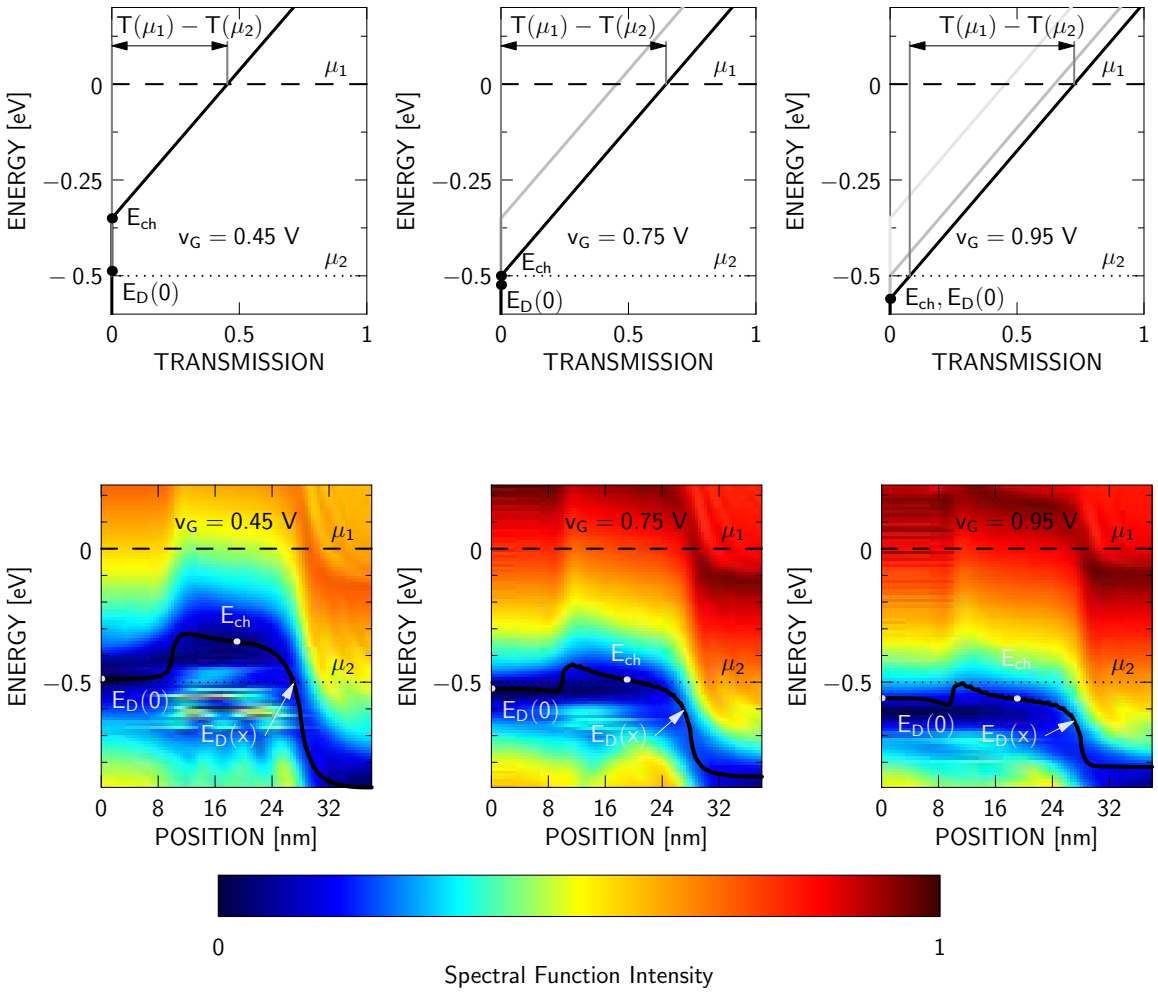



Figure 2.6: Schematic illustration of the transmission function $T(E)$ vs. $E$ and corresponding sketches of the Dirac point $E_D(x)$ vs. $x$, shown for three values of $v_G$, with $v_S \equiv 0$, $v_D = V_{\mathrm{DD}}/2 = 0.5$ V, and the equilibrium Fermi level $\mu \equiv 0$. The scaling on the transmission axes and of the spectral intensity have been normalized to unity; the values shown are hence relative, not the actual values of $T(E)$ and $A(x, E)$. For the spectral intensity, dark blue indicates a low spectral intensity while orange and red indicate a high spectral intensity.

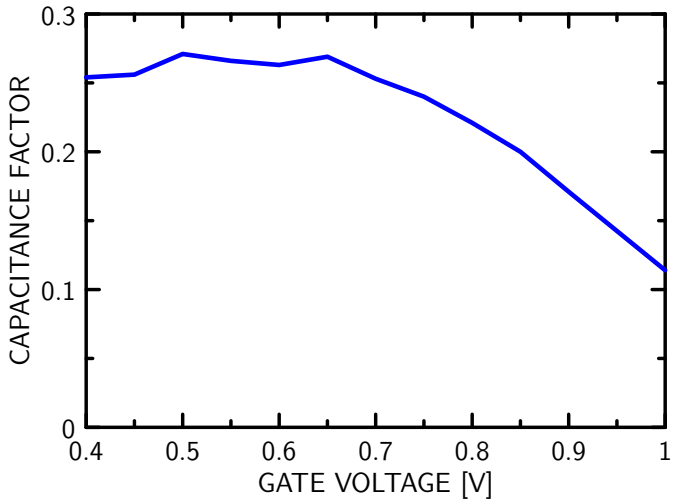



Figure 2.7: Capacitance factor $(1 - C_{\text{gg}}/C_{\text{ox}})$ vs. gate voltage $v_G$ for the GFET. The factor appears in the expression (2.1) for $g_m$.

factor $(1 - C_{\text{gg}}/C_{\text{ox}})$ appearing in (2.1). This factor is plotted in Fig. 2.7; at sufficiently high gate voltages ($v_G \geq 0.75$ V), the factor experiences a noticeable decline, which begins to dominate the behavior of the $g_m$. Since $C_{\text{ox}}$ is a constant (having no dependence on the bias point), the decline is due to a rising $C_{\text{gg}} = C_{\text{gs}} + C_{\text{gd}}$, which occurs because the GFET enters an "ohmic" regime of operation, as we will describe in the next subsection.

Overall, the results in Figs. 2.4–2.7, along with the expressions (2.1) and (2.9), indicate that *the $g_m$ in a graphene device can be expected to increase with gate voltage and eventually saturate (or peak) when $v_G$ is chosen such that the drain Fermi level aligns with the channel potential: $\mu_2 = E_{\text{ch}}$.*

### Gate Capacitance

As shown in Fig. 2.4, the gate-drain capacitance $C_{\text{gd}}$ exhibits a definite minimum at $v_G = 0.75$ V, while the gate-source capacitance $C_{\text{gs}}$ is approximately constant for $v_G \geq 0.75$ V. Much of the rise in the input capacitance $C_{\text{gg}} = C_{\text{gs}} + C_{\text{gd}}$ for $v_G \geq 0.75$ V can thus be attributed to the corresponding rise in $C_{\text{gd}}$.

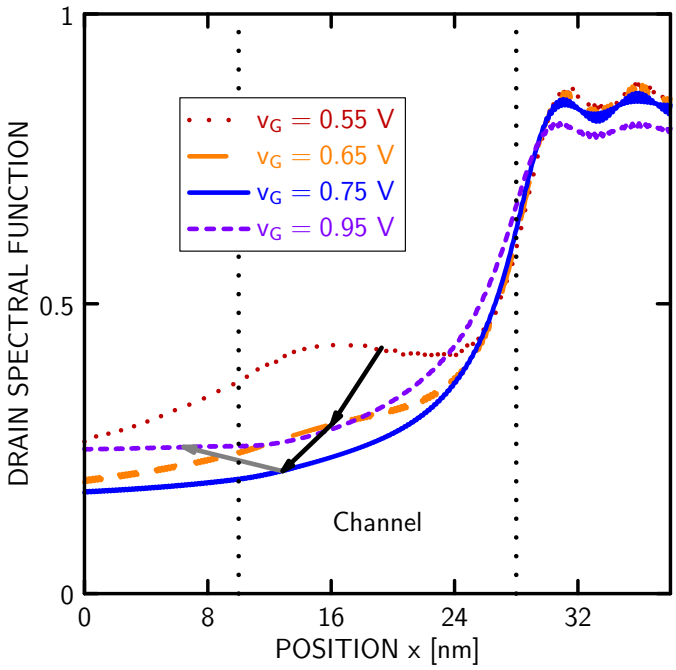



Figure 2.8: Drain spectral function (local density of states that can be filled by the drain) evaluated at the drain Fermi level $\mu_2$ and plotted versus position $x$, *i.e.*, $A_D(x, \mu_2)$ vs. $x$. Curves are shown for several values of the applied gate voltage $v_G$. The black arrows indicate the shift in the spectral function as the gate voltage is increased, until the spectral function reaches its minimum value in the channel at $v_G = 0.75$ V; the gray arrow then indicates the upward shift in the spectral function as the gate voltage is further increased (beyond $v_G = 0.75$ V). The scaling on the spectral axis has been normalized to unity for plotting purposes.

$C_{\rm gd}$ can be written in terms of the physics-based capacitances in Fig. A.11 of Appendix A:

$$C_{\rm gd} = \frac{C_{\rm ox}(C_{\rm de} + C_{\rm dq})}{C_{\rm ox} + C_{\rm se} + C_{\rm sq} + C_{\rm de} + C_{\rm dq}}. \tag{2.10}$$

Its behavior can then be understood by considering the plots of $E_D(x)$ vs. $x$ in Fig. 2.6 along with the results in Fig. 2.8, where the latter shows the drain spectral function (local density of states that can be filled by the drain) evaluated at an energy equal to the drain Fermi level $\mu_2$ and plotted versus position $x$, *i.e.*, $A_D(x, \mu_2)$ vs. $x$. For gate biases below the minimum of the $C_{\rm gd}$ curve in Fig. 2.4, the drain Fermi level in Fig. 2.6 is well below the channel potential $E_{\rm ch}$, and a relatively high density of states in equilibrium with $\mu_2$ is

available at the midpoint of the channel ($x = 19$ nm in Fig. 2.1), as shown, for example, by the curve for $v_G = 0.55$ V in Fig. 2.8. As the gate voltage increases and $E_D(x)$ is pushed down, Fig. 2.6 illustrates that the drain Fermi level $\mu_2$ moves up with respect to $E_{\text{ch}}$ and eventually aligns with it. Correspondingly, in Fig. 2.8, as $v_G$ is varied from $0.55$ V to $0.75$ V, the available density of states at $E = \mu_2$ at the midpoint of the channel falls, reaching a minimum at $v_G = 0.75$ V. Since the drain quantum capacitance $C_{\text{dq}}$ depends directly on the available density of states at the drain Fermi level [119, Ch. 7], it will follow the same trend; $C_{\text{dq}}$ will fall from its value at $v_G = 0.55$ V to a minimum at $v_G = 0.75$ V. Given $\partial C_{\text{gd}}/\partial C_{\text{dq}} > 0$ according to (2.10), the fall in $C_{\text{dq}}$ has the effect of reducing $C_{\text{gd}}$ until $v_G = 0.75$ V, as illustrated in Fig. 2.4.

Further increases in $v_G$ beyond 0.75 V cause $\mu_2$ to be positioned above $E_{\text{ch}}$, as shown, for example, by the results for $v_G = 0.95$ V in Fig. 2.6. The device now enters an "ohmic" region of operation, where both Fermi levels are positioned above the Dirac point $E_D(x)$ for all $x$, and the transport becomes indistinguishable from that in a metallic conductor with a linear potential profile (vs. $x$) and an applied voltage $v = (1/q)(\mu_1 - \mu_2)$; note that by "ohmic" we refer only to the metallic nature of the potential profile, not the "ohmic" or "triode" region of textbook FET operation. As a result, the drain terminal can be expected to gain increased control over the channel potential $E_{\text{ch}}$, which is equivalent to suggesting that the capacitance $C_D = C_{\text{de}} + C_{\text{dq}}$ associated with the drain in Fig. A.11 increases, and hence that $C_{\text{gd}}$ in (2.10) increases, as illustrated in Fig. 2.4.

**Bias Point for Peak $f_{\text{T,int}}$**

Based on the discussion of $g_m$ and $C_{\text{gg}}$, it becomes evident that *the peak $f_{T,int}$ will be achieved when the gate bias is chosen to align the drain Fermi level with the channel potential:*

$$\boxed{\mu_2 = E_{\text{ch}}.} \tag{2.11}$$

This bias point will maximize the transconductance $g_m$ while keeping the gate capacitance $C_{\text{gg}}$ from increasing due to ohmic operation, yielding an optimum $f_{\text{T,int}} = g_m/(2\pi C_{\text{gg}})$. For the device under study, $\mu_2 = E_{\text{ch}}$ is achieved for $v_G = 0.75$ V, which corresponds to the peak in the $f_{\text{T,int}}$ curve of Fig. 2.3(b).

### 2.3.3 Output Conductance

#### Expression

A useful expression for the output conductance can be found by following steps similar to those in Appendix A leading to (2.1) for the transconductance.

The output conductance is defined as

$$g_o = \frac{\partial i_D}{\partial v_D} \tag{2.12}$$

where the derivative is to be evaluated while holding the gate and source voltages ($v_G$ and $v_S$) constant. Differentiating (A.3) for the current while using the product rule and the fact that the source Fermi function $f_1(E)$ in (2.7) has no dependence on $v_D$, we find

$$\frac{\partial i_D}{\partial v_D} = \frac{2q}{h}\int_{-\infty}^{\infty}\left\{\frac{\partial T(E)}{\partial v_D}\left[f_1(E) - f_2(E)\right] - T(E)\frac{\partial f_2(E)}{\partial v_D}\right\} dE. \tag{2.13}$$

This expression suggests the output conductance can be written as the sum of two components:

$$\boxed{g_o \equiv \frac{\partial i_D}{\partial v_D} \equiv g_{\text{ob}} + g_{\text{oq}}} \tag{2.14}$$

where

$$g_{\text{ob}} \equiv \frac{2q}{h}\int_{-\infty}^{\infty}\frac{\partial T(E)}{\partial v_D}\left[f_1(E) - f_2(E)\right] dE \tag{2.15}$$

and

$$\begin{aligned} g_{\text{oq}} &\equiv \frac{2q}{h}\int_{-\infty}^{\infty} -T(E)\frac{\partial f_2(E)}{\partial v_D}\, dE \\ &= \frac{2q^2}{h}\int_{-\infty}^{\infty} T(E)\frac{\partial f_2(E)}{\partial E}\, dE. \end{aligned} \tag{2.16}$$

**Interpretation**

The component $g_{\text{oq}}$ in (2.16) is best understood at zero temperature. The derivative of the Fermi function will become a Dirac-delta function centered at the drain Fermi level $\mu_2$. Performing the integration in (2.16) then reveals

$$\boxed{g_{\text{oq}} = G_0 T(\mu_2)} \tag{2.17}$$

which highlights the interpretation of $g_{\text{oq}}$ as an *output conductance component due to quantum-mechanical transmission around the drain Fermi level*.

The component $g_{\text{ob}}$ in (2.15) represents the effects of *conventional drain-induced barrier lowering* (DIBL), which can be understood with the aid of Fig. A.11. With $C_D \equiv C_{\text{de}} + C_{\text{dq}}$, the incremental channel potential due to the application of an incremental drain voltage $-q\partial v_D$ (with the gate and source voltages held constant) is given by

$$\partial E_{\text{ch}} = -q\partial v_D \frac{C_D}{C_T} = -q\partial v_D \frac{C_{\text{gd}}}{C_{\text{ox}}} \tag{2.18}$$

where $C_T$ is the total capacitance in Fig. A.11, as specified below (A.2) in Appendix A, and where the relation $C_D/C_T = C_{\text{gd}}/C_{\text{ox}}$ follows from (2.10). Using steps similar to those in Appendix A, one then obtains

$$\boxed{g_{\text{ob}} = G_0 \frac{C_{\text{gd}}}{C_{\text{ox}}} \int_{-\infty}^{\infty} \frac{\partial T(E)}{\partial E} \left[ f_1(E) - f_2(E) \right] dE.} \tag{2.19}$$

The interpretation of (2.19) is hence similar to (2.1), with the only difference being in the capacitive factor multiplying the integral; in the present case of (2.19), this factor reflects the direct control of an incremental drain voltage $\partial v_D$ over an incremental channel potential $\partial E_{\text{ch}}$ according to (2.18), and hence the control of $\partial v_D$ over the source-to-drain barrier height and the incremental drain current $\partial i_D$.

### Relation to Traditional MOSFETs

The above results (2.17) and (2.19) can also be interpreted in the context of traditional (silicon) MOSFETs vs. graphene.

In a traditional semiconductor possessing a bandgap, we find that transmission around the drain Fermi level is impossible, *i.e.*, $T(\mu_2) = 0$; this follows from the fact that under normal operating conditions, the drain Fermi level is located at an energy that falls within the bandgap of the energy-band profile of a traditional device channel, such that very little transmission can occur. As a result, for a traditional semiconductor, we find $g_{\text{oq}} = 0$ from (2.17). On the other hand, this result does not necessarily apply to graphene, which possesses no bandgap.

Regarding the component $g_{\text{ob}}$ in (2.19), in conventional transistors with a bandgap, the control of the drain on the channel region (indicated by the factor $C_{\text{gd}}/C_{\text{ox}}$) under normal operating conditions is limited to conventional electrostatic DIBL, *i.e.*, the ratio $C_{\text{gd}}/C_{\text{ox}}$, which was specified earlier in (2.10), is determined only by $C_{\text{de}}$ in the numerator, with $C_{\text{dq}} \to 0$; in the absence of conventional DIBL, we also have $C_{\text{de}} \to 0$, and we hence find $g_{\text{ob}}$ in (2.19) can be made to vanish in a traditional device. On the other hand, this outcome cannot be made to occur in graphene, due to a pronounced $C_{\text{dq}}$ arising from the lack of a bandgap, where the behavior of $C_{\text{dq}}$ was already discussed in conjunction with (2.10) and Fig. 2.8.

### Results

Values for the output conductance $g_o$ and its components $g_{\text{ob}}$ and $g_{\text{oq}}$ [computed from (2.15) and (2.16)] vs. gate voltage $v_G$ are displayed in Fig. 2.9, and they can easily be understood by appealing to the results already discussed.

The component $g_{\text{oq}}$ exhibits a weak minimum at $v_G = 0.75$ V, where the drain Fermi level $\mu_2$ aligns with the channel potential $E_{\text{ch}}$ (Fig. 2.6). At this point, $T(\mu_2)$ is minimized,

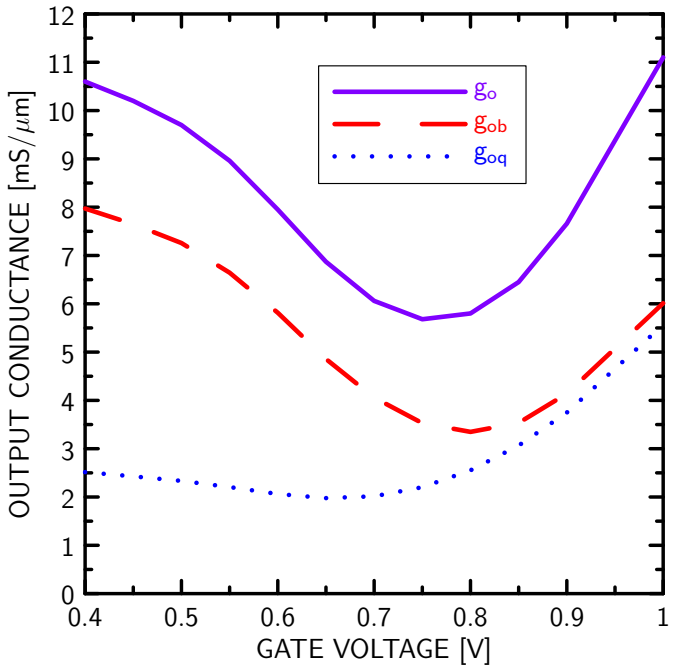



Figure 2.9: Output conductance $g_o$ and its components $g_{\text{ob}}$ and $g_{\text{oq}}$ vs. gate voltage $v_G$ for the GFET. The drain voltage is held at $v_D = V_{\text{DD}}/2 = 0.5$ V.

which has the effect of minimizing $g_{\text{oq}}$ as suggested by (2.17); for gate voltages beyond this point, $\mu_2$ moves into the linear portion of $T(E)$ (Fig. 2.6), causing $g_{\text{oq}}$ to rapidly increase, as illustrated in Fig. 2.9.

The component $g_{\text{ob}}$ exhibits a well-defined minimum at $v_G \approx 0.75$ V. To first order, this corresponds to the behavior of $C_{\text{gd}}$, which dominates the behavior of $g_{\text{ob}}$ through the ratio $C_{\text{gd}}/C_{\text{ox}}$ appearing in (2.19), where $C_{\text{ox}}$ is a constant; as discussed earlier and as illustrated in Fig. 2.4, $C_{\text{gd}}$ will exhibit a minimum at $v_G = 0.75$ V, where $\mu_2 = E_{\text{ch}}$.

Overall, the results in Fig. 2.9 show that both the components $g_{\text{oq}}$ and $g_{\text{ob}}$ are minimized when the biasing is chosen such that $\mu_2 = E_{\text{ch}}$, the same condition identified earlier as yielding peak $f_{\text{T,int}}$. It is worth mentioning that these observations elaborate on those made in [103] and [104]. The approach in [103] is equivalent to assuming $g_o = g_{\text{oq}}$, and the authors point out that the condition $\mu_2 = E_{\text{ch}}$ will ideally yield $g_o = g_{\text{oq}} = 0$ [103, Fig. 2]; a

strong minimum in $g_{\text{oq}}$ is also observed in [103], rather than the weak minimum shown here in Fig. 2.9, which can be attributed to the missing asymmetry in $T(E)$ in [103]. In [104], it is suggested that the lack of a bandgap can cause $C_{\text{dq}}$ and hence $C_{\text{gd}}$ to be appreciable, and that this can impact the high-frequency performance [104, eq. (28)], which is equivalent to considering the impact of $g_{\text{ob}}$. Our approach naturally identifies and clarifies the role of both components.

## 2.4 Extrinsic Results

As mentioned in Section II, COMSOL was used to calculate the parasitic capacitances, with the device width set equal to $1\ \mu$m (for demonstration purposes); values of $C'_{\text{sd}} = 24$ aF, $C'_{\text{gd}} = 40$ aF, and $C'_{\text{gs}} = 40$ aF were obtained for the GFET structure of Fig. 2.1. The source and drain contact resistances were taken to be $R_S = R_D = 50\ \Omega$, near the theoretical minimum for graphene [120, 121]. While these values may be viewed as optimistic, they are consistent with our aim of performing a best-case assessment and should be achievable with improvements in the fabrication process; moreover, we have found that the important outcomes of the results presented here (on the impact of a lack of a bandgap and correspondingly high $g_o$ on the RF metrics) are not affected by the specific values chosen. For the gate resistance, we used a value $R_{\text{g,eff}} = 220/3\ \Omega$, which can be calculated by considering a tungsten gate contact of dimensions $W_g \times L_g \times t_g = 1\,\mu\text{m} \times 18\,\text{nm} \times 60\,\text{nm}$; this material was chosen due to the match in the work function with graphene. These parasitics were used in conjunction with the circuit in Fig. 2.2 to determine the extrinsic figures of merit.

### 2.4.1 RF Metrics

Table 2.2 presents several key RF metrics for the GFET, including the extrinsic unity-current-gain frequency $f_T$, the unity-power-gain frequency $f_{\text{max}}$, the maximum available

gain (MAG) [122], and the maximum stable gain (MSG $= |y_{21}/y_{12}|$, where $y_{21}$ and $y_{12}$ refer to the forward and reverse transadmittances, respectively). The $f_{\max}$ was found by extrapolating Mason's unilateral gain ($U$) [123] to unity at $-20$ dB/decade.

Since the GFET values in Table 2.2 are based on the assumption of ballistic transport, they can be interpreted as indicating that GFETs have ample potential to meet the requirements of the ITRS [30] going forward, and that this potential can be realized despite the lack of a bandgap and the ensuing lack of current saturation [Fig. 2.3(a)], which leads to a poor output conductance $g_o$. We will elaborate further on this point by quantifying the precise impact of $g_o$ on the attainable $f_T$ and $f_{\max}$.

Table 2.2: RF Metrics

| | **Power Supply Voltage $V_{DD}$ [V]** | **Gate Length $L_g$ [nm]** | **Peak $f_T$ [GHz]** | **Peak $f_{max}$ [GHz]** | **MSG/ MAG [dB] at 24 GHz** | **MSG/ MAG [dB] at 60 GHz** | **MSG/ MAG [dB] at 94 GHz** |
|---|---|---|---|---|---|---|---|
| GFET in this work | 1.0 | 18 | 2700 | 3000 | 31.4 | 20.5 | 18.5 |
| RF CMOS (ITRS) [30] | 1.0 | 18 | 490 | 560 | 17.9 | 13.9 | 11.9 |

### 2.4.2 Unity-Current-Gain Frequency

An expression for the extrinsic unity-current-gain frequency that includes the effects of output conductance is [124]

$$f_T \approx \frac{f_{\text{T,int}}}{\alpha_T + [\alpha_T g_o + 2\pi f_{\text{T,int}}(C_{\text{gd}} + C'_{\text{gd}})]\,(R_S + R_D)} \tag{2.20}$$

where $\alpha_T \equiv (C_{\text{gg}} + C'_{\text{gs}} + C'_{\text{gd}})/C_{\text{gg}}$. Fig. 2.10 shows a plot of (2.20) with and without $g_o$, along with results from the circuit of Fig. 2.2, which are used to validate (2.20). As shown,

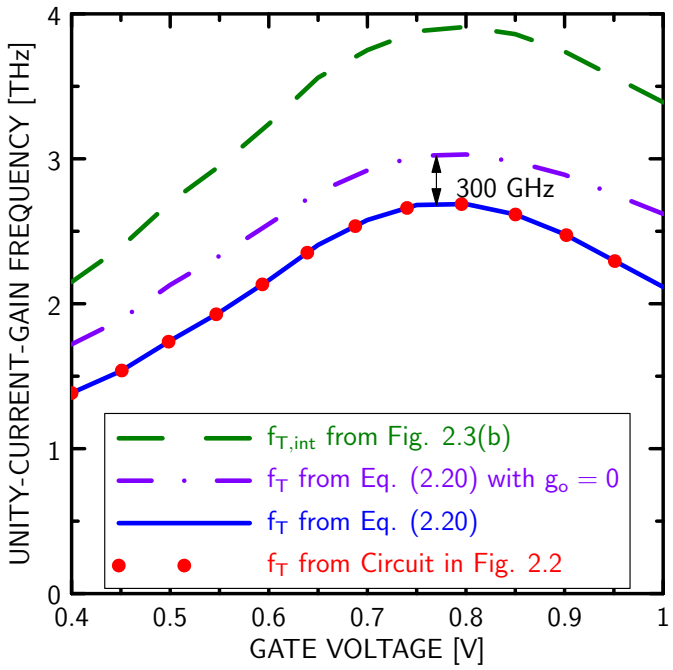



Figure 2.10: Extrinsic unity-current-gain frequency $f_T$ vs. gate voltage $v_G$ as found from (2.20). Values of $f_T$ extracted from the circuit of Fig. 2.2 are also shown to validate (2.20), and values of the *intrinsic* $f_{\text{T,int}}$ reproduced from Fig. 2.3(b) are shown for reference.

the impact of a nonzero $g_o$ in graphene is to reduce the peak $f_T$ by about 300 GHz; the overall impact of the lack of a bandgap is actually greater, since it also leads to a higher $C_{\text{dq}}$ and hence higher $C_{\text{gd}}$ [as discussed in conjunction with (2.10)], increasing the importance of the term involving $R_S$ and $R_D$ in (2.20).

### 2.4.3 Unity-Power-Gain Frequency

An expression for $f_{\text{max}}$ that includes the effect of output conductance is [124]

$$f_{\text{max}} \approx \frac{f_T}{\sqrt{4g_o R_G + 8\pi f_T (C_{\text{gd}} + C'_{\text{gd}})\,[R_G + \alpha_M R_D]}} \tag{2.21}$$

where

$$\alpha_M \equiv \frac{C_{\text{gd}} + C'_{\text{gd}} + C_{\text{sd}} + C'_{\text{sd}}}{C_{\text{gg}} + C'_{\text{gs}} + C'_{\text{gd}}}. \tag{2.22}$$

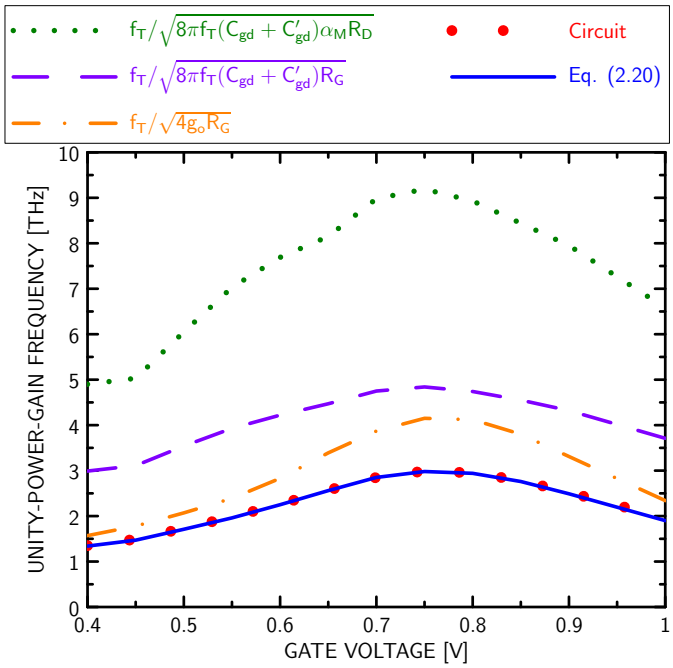



Figure 2.11: Plot of the components of the unity-power-gain frequency $f_{\max}$ according to the expression (2.21) vs. gate voltage $v_G$. Values of $f_{\max}$ obtained from the circuit of Fig. 2.2 are also shown to validate (2.21).

Fig. 2.11 shows a plot of the components on the right side of (2.21), along with results from the circuit of Fig. 2.2. When all three terms in the denominator of (2.21) are included, the agreement with the results from the circuit is nearly perfect, which validates the expression. The impact of the term involving the drain resistance $R_D$ is secondary, with the associated values $f_T/\sqrt{8\pi f_T(C_{\rm gd}+C'_{\rm gd})\alpha_M R_D}$ greatly exceeding the true $f_{\max}$. Retaining only the term involving $R_G$ and $C_{\rm gd}$ yields the classical expression $f_T/\sqrt{8\pi f_T(C_{\rm gd}+C'_{\rm gd})R_G}$ for the $f_{\max}$ of RF transistors [125], [112, Ch. 8]; however, as shown, this overestimates the true peak $f_{\max}$ by close to a factor of two. The reduction is primarily due to the output conductance $g_o$, with the associated values $f_T/\sqrt{4g_o R_G}$ providing the closest estimate to the true $f_{\max}$. These results, which are founded on our fully quantum-mechanical simulations, thus suggest that the lack of a bandgap, and the associated poor output conductance, limits the RF potential of graphene (as measured by peak $f_{\max}$) by approximately a factor

of two. While the data in Table 2.2 show that graphene should nevertheless be competitive, the results in Fig. 2.11 suggest that it is worthwhile to pursue modified forms of graphene exhibiting a bandgap and better output conductance to further improve the high-frequency performance.

## 2.5 Conclusions

The following conclusions can be drawn from this study on the impact of a zero bandgap on the RF potential of GFET transistors:

1. Based on ballistic quantum-mechanical transport in the intrinsic device, the lack of a bandgap causes optimum RF performance to be realized under the bias condition where the drain Fermi level $\mu_2$ aligns with the channel potential $E_{\text{ch}}$, as specified by (2.11).

2. This bias point, which corresponds to $v_G \sim 0.75$ V (where $v_D \equiv V_{\text{DD}}/2 = 0.5$ V) for the chosen device, yields an optimum transconductance $g_m$ while keeping the gate-drain capacitance $C_{\text{gd}}$ and hence the input capacitance $C_{\text{gg}}$ from increasing due to "ohmic" operation, thus yielding an optimum intrinsic $f_{\text{T,int}} = g_m/(2\pi C_{\text{gg}})$ [Figs. 2.4 and 2.3(b)].

3. The same bias point leads to an optimum value for the intrinsic output conductance $g_o$, which can be viewed as being comprised of two parts: a quantum component $g_{\text{oq}}$ and a conventional DIBL component $g_{\text{ob}}$. The relevant equations revealing the associated physics are (2.14), (2.17), and (2.19), and the relevant figure illustrating the behavior of $g_o$ is Fig. 2.9.

4. The relatively poor output conductance limits the extrinsic $f_T$ and $f_{\text{max}}$, a feature which is unique to graphene transistors. With the aid of (2.20) and (2.21), our fully

quantum-mechanical simulations suggest the peak $f_T$ could be increased by 300 GHz and the peak $f_{\max}$ could be doubled (Figs. 2.10 and 2.11) if a bandgap could be introduced to cause $g_o \to 0$ while leaving all other parameters unchanged.

Despite the lack of a bandgap and a pronounced output conductance, our results show that graphene transistors exhibit more than sufficient potential to keep pace with ITRS [30] requirements (Table 2.2). Further studies on the effects of phonon scattering and the effects of introducing a bandgap are warranted to get a more complete description of the RF potential of graphene devices.

# Chapter 3

# Impact of Contact Resistance on the $f_T$ and $f_{\mathbf{max}}$ of Graphene vs. $\mathbf{MoS_2}$ Transistors

## 3.1 Introduction

The high-speed electronic properties of graphene, including a linear band dispersion with high bandstructure velocity [126], record mobility [12], and record current density [127], have all contributed to the intense interest toward its use as a channel material for field-effect transistors (FETs) [16, 78]. At the same time, graphene has no electronic bandgap, which leads to the undesirable outcome that graphene FETs (GFETs) cannot be turned off, and hence that digital circuits cannot be created from graphene, except through modified forms having induced bandgaps, such as ribbons [21], bilayers [19], and antidot lattices [20].

In order to exploit the high-speed properties of graphene, the focus of research on single-layer GFETs[1] has thus leaned towards their use in analog radio-frequency (RF) applications [76]. The measured values of the unity-current-gain (cutoff) frequency ($f_T$) have reached over 400 GHz [83], comparable to the fastest high-electron-mobility transistors

[1] In this chapter, we consider GFETs made only with graphene in its single-layer form; hence, "graphene" always means "single-layer graphene," even when not explicitly stated.

(HEMTs) with similar gate lengths [25]. The observed values of the unity-power-gain frequency ($f_{\max}$) have been somewhat lower, due to the stronger influence of a lack of a bandgap, and hence low output conductance, on power gain vs. current gain [28], but they still hold promise, especially considering the relative immaturity of GFET technology, with a record value of around 70 GHz [82].

Although the mobility and high bandstructure velocity of graphene have been repeatedly suggested [83, 128, 129] as being the main reason for its consideration for electronics, far more important is the ideal electrostatic environment inherent in two-dimensional materials [16]. Two-dimensional materials can be considered the ultimate form of the ultra-thin-body, silicon-on-insulator (UTB-SOI) transistor, a structure that allows for better electrostatic gate control than bulk materials, and hence more efficient downscaling while avoiding short-channel effects. Many two-dimensional materials have also been demonstrated to exhibit a high degree of mechanical strength and flexibility [130, 131, 132]. Such properties naturally lead to an interest not only in incorporating two-dimensional materials in traditional integrated circuit design, but also in the exciting area of flexible electronics [133].

Single-layer molybdenum disulphide (SL $MoS_2$) has been suggested as an alternative two-dimensional material to graphene, mostly because it exhibits a substantial bandgap of 1.8 eV [134], while still demonstrating the inherent electrostatic benefits of a two-dimensional material. On-off current ratios ($I_{\text{on}}/I_{\text{off}}$) of more than $10^7$ have been demonstrated [135], much better than the values of $10^0$-$10^2$ demonstrated for graphene [16]. An additional benefit of SL $MoS_2$ is that the existence of a bandgap may allow for improved RF performance in comparison to graphene transistors, through a reduction in the output conductance. However, to date, the experimentally observed values of $f_T$ and $f_{\max}$ for SL $MoS_2$ transistors have been limited to 6.7 GHz and 5.3 GHz, respectively [71], while multi-layer $MoS_2$ (ML $MoS_2$) transistors have achieved $f_T$ and $f_{\max}$ values of 42 GHz and

50 GHz [70], respectively. It has also been suggested that $MoS_2$ transistors will not be able to operate at high frequencies [136], and that graphene will hence remain the superior choice from this perspective.

A major limitation on the performance of single-layer materials for radio-frequency (RF) applications arises from the high values of contact resistance $\rho_C$ determining the source and drain parasitic resistances. In graphene, the minimum achieved contact resistance has been around 100 $\Omega \cdot \mu\mathrm{m}$, as evidenced by multiple experiments [137, 120, 138]. In SL $MoS_2$, creating high-quality, low-resistance ohmic contacts is a greater problem, due to the large bandgap combined with Fermi-level pinning [56]. Scandium [56], molybdenum [139], and graphene [43] have all been suggested as possibilities for the contact material. However, for each possibility, the contact resistance is above 1 $\mathrm{k}\Omega \cdot \mu\mathrm{m}$ [67], an order of magnitude worse than what has been observed in graphene. Significantly lower (improved) contact resistances have been realized in ML $MoS_2$; chloride-doped devices have reached values below 500 $\Omega \cdot \mu\mathrm{m}$ [140], devices with nickel-etched graphene electrodes have reached values of 200 $\Omega \cdot \mu\mathrm{m}$ [137], and devices using the metallic phase of $MoS_2$ for contacts have reached values of less than 100 $\Omega \cdot \mu\mathrm{m}$ [135].

Given the attractive properties of SL $MoS_2$ for digital applications, an open question is whether or not its analog RF performance could match or even exceed that of graphene. If so, the idea of using SL $MoS_2$ in mixed-signal flexible electronics would become extremely attractive.

Work has already been done in comparing noise performance in the two materials. Currently, graphene has better $1/f$ [141] noise compared to SL $MoS_2$ [142], though an improvement in the $1/f$ noise in SL $MoS_2$ is expected with encapsulation of the channel and optimizations in processing to reduce trap density. The larger contact resistance in SL $MoS_2$ also degrades its $1/f$ noise [142, 143].

While noise is an important consideration, in this work, we focus on comparing the RF

performance of SL $MoS_2$ with that of graphene by examining the achievable $f_T$ and $f_{\max}$, addressing the fundamental question of whether the $f_T$ and $f_{\max}$ of SL $MoS_2$ could meet or even exceed that of graphene, and if so, under exactly what conditions. We begin with a summary of the performance parameters that are determined by transport through the core of the transistor; these are the transconductance $g_m$, internal gate capacitance $C_{\rm gg}$, and output conductance $g_o$. We use this as a basis to examine the overall RF performance, including parasitics, via a comparison of the $f_T$ and $f_{\max}$. First, we demonstrate that SL $MoS_2$ lags graphene in terms of *peak* performance, *i.e.*, the best performance attainable over all bias conditions, as measured by the peak values of $f_T$ and $f_{\max}$. We show that this lag stems largely from the poorer values of $\rho_C$ presently attainable with SL $MoS_2$, and we specify the values of $\rho_C$ that SL $MoS_2$ would need to achieve to match graphene's peak capabilities. Second, we point out that under conditions of constrained bias current, SL $MoS_2$ looks far more competitive. We use the technologically relevant value of $1.65$ mA/$\mu$m [3] and show that graphene loses much of its advantage due to a reduction of its $g_m$ once the current is constrained. With the bias current constrained, we show that SL $MoS_2$ can meet or exceed graphene's performance by achieving contact resistances already attained in ML $MoS_2$. Overall, our work hence specifies exactly how the $f_T$ and $f_{\max}$ of graphene and SL $MoS_2$ compare, with detailed discussion to support the conclusions.

This chapter is organized as follows. Section 3.2 briefly describes our approach, which is based on a quantum-mechanical simulation of a common device structure differing only in the channel material; a quantum-mechanical simulation is essential for small gate lengths as well as for gapless materials. Section 3.2 also discusses the inclusion of all the parasitic resistances and capacitances, which are required for a realistic assessment. Section 3.3 examines the RF parameters determined by transport through the critical part of the common device structure; we consider the $g_m$, $C_{\rm gg}$, and $g_o$. Sections 3.4 and 3.5 consider the *peak* (over all bias conditions) values of $f_T$ and $f_{\max}$, with an emphasis on the impact of $\rho_C$, and

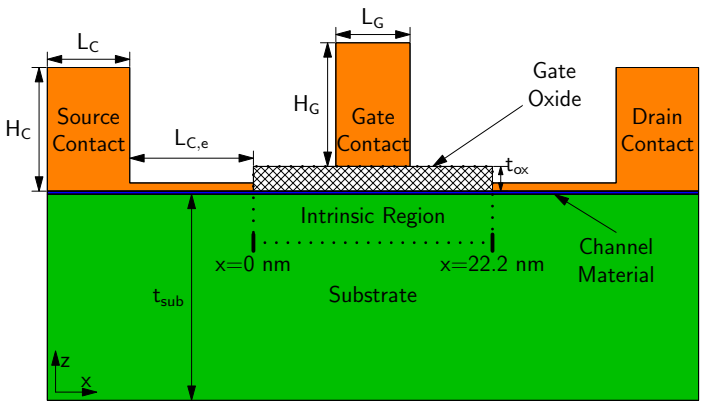



Figure 3.1: Common device structure used in this study. The dimensions are given in Tables 3.1 and 3.2. The dotted lines show a cross-section of the intrinsic portion of the device, defined as the core of the structure excluding parasitics. This core contains the 10.2-nm intrinsic channel along with 6-nm-long portions of the degenerately $n$-doped source and drain reservoirs. The source and drain contact geometries are symmetric with respect to the gate. The positions $x = 0$ and $x = 22.2$ nm, which delimit the intrinsic region, are labeled for later reference.

Section 3.6 reexamines the situation under the constraint of a fixed bias current. Finally, Section 3.7 shows the validity of our approach through a comparison of our simulation results with experimental data available in the literature. The conclusions of our study are summarized in Section 3.8.

## 3.2 Approach

### 3.2.1 Comparison Methodology

In order to make a fair and direct comparison of the RF performance between SL $MoS_2$ and graphene transistors, we simulate the same device structure for both materials, including the dimensions of the metal contacts, the thickness of the gate-oxide layer, and the type and thickness of the substrate; the only difference is the channel material itself. The common structure is shown schematically in Fig. 3.1. Key physical parameters are summarized in Tables 3.1 and 3.2, and they are derived from the ITRS 7-nm node [3]. We assume the channel region is surrounded by degenerately $n$-doped source and drain reservoirs with

Table 3.1: Structure Parameters

| Parameter | Description | Value |
|---|---|---|
| $L_G$ | Physical Gate Length | 12.7 nm |
| $L_{\text{ch}}$ | Effective Channel Length | 10.2 nm |
| $V_{\text{DD}}$ | Power Supply Voltage | 0.78 V |
| $K_{\text{ox}}$ | Gate Dielectric Constant | 15.0 |
| $t_{\text{ox}}$ | Physical Oxide Thickness | 2.46 nm |
| $t_{\text{sub}}$ | Substrate Thickness | 50 nm |
| $K_{\text{sub}}$ | Substrate Dielectric Constant | 3.9 |

an abrupt or step-like doping profile, and that the device is "MOSFET-like," where the source and drain contacts are ohmic and the gate modulates the source-to-channel barrier. These simplifications allow us to comparatively assess the best-case performance of each channel material, consistent with the aim of this study. In this regard, it is worth mentioning that while it is common in experiments to utilize electrostatic doping with a back gate, promising techniques exist to dope graphene and $MoS_2$ [54, 144], and that while it is more common to realize Schottky-barrier transistors in experiments, progress toward "MOSFET-like" devices with ohmic contacts have been demonstrated for both graphene and ML $MoS_2$ [145, 121].

### 3.2.2 Analysis of Transport

#### Overview

The transport is modeled with a quantum-mechanical device simulator that solves the Poisson equation (along $x$ and $z$) self-consistently with the non-equilibrium Green's function (NEGF) formalism [146] (along $x$). The tool simulates electron transport within the dotted region of Fig. 3.1, the critical active region of the transistor, which we call the "intrinsic region," to extract the bias-dependent circuit elements for use in the dashed portion of the small-signal equivalent circuit of Fig. 3.2. For the purposes of this study, the simulations

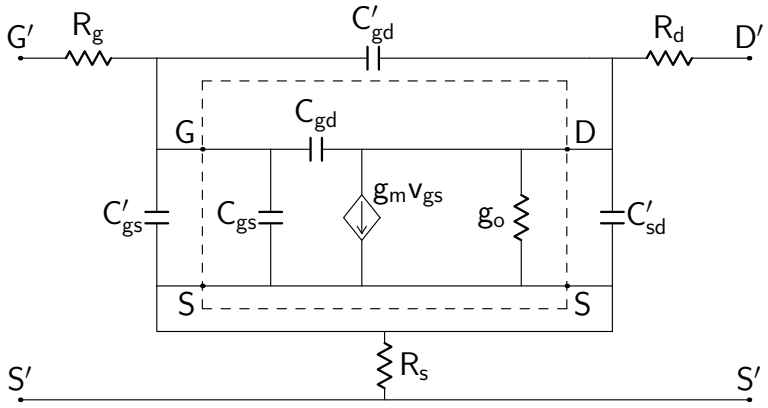



Figure 3.2: Equivalent circuit used in this study, with the intrinsic portion boxed. The labels $S$, $D$, and $G$ refer to the source, drain, and gate terminals, respectively, of the intrinsic device, while their primed counterparts $S'$, $D'$, and $G'$ refer to the corresponding extrinsic device terminals.

were carried out under ballistic conditions for graphene and *with* phonon scattering for SL $MoS_2$. This approach is justified by the effective channel length of 10.2 nm in our structures. Graphene has been shown to exhibit ballistic transport on the micrometer scale [37], while the mean-free path for SL $MoS_2$ is over 14 nm [73] for low-field conditions, but can be as low as 7.5 nm under higher electric fields [36]. Both elastic (transverse and longitudinal acoustic) and inelastic (longitudinal optical, homopolar, and Fröhlich interaction) scattering are modeled in SL $MoS_2$ [73, 74].

**Poisson Solver**

The Poisson equation, discretized with finite differences, is used in the electrostatic simulation of both devices. We assume that the device is wide and that the potential along the width of the channel (along $y$) does not vary, meaning that the simulation does not account for the effects of the edges. A two-dimensional computational domain, in the $x$-$z$ plane, is hence used to capture electrostatic effects in the relevant regions, similar to the standard analysis of CMOS devices.

#### NEGF Solver

For SL $MoS_2$ devices, the NEGF solver utilizes a discretized effective-mass Hamiltonian with an effective mass of $m^* = 0.55m_e$ [72], where $m_e = 9.11 \times 10^{-31}$ kg is the free-electron rest mass. We verified that under all bias conditions, and for energies relevant to transport, the conduction band follows a parabolic dispersion, hence justifying this approach. The NEGF equations are solved in one dimension (along $x$), with the contribution of transverse modes (along $y$) being taken into account by using the Fermi-Dirac integral of order $-1/2$, as in [147]. The contact self-energies are computed analytically because of the simple form of the one-dimensional Hamiltonian [146].

A nearest-neighbor, tight-binding Hamiltonian with a $p_z$-orbital basis is used in the graphene simulation [114]. Bloch boundary conditions are imposed in the transverse direction (along $y$), giving a series of orthogonal one-dimensional transport modes (along $x$). The contact self-energies are computed numerically with the Sancho-Rubio iterative method [115].

In both materials, the NEGF equations are solved using the recursive Green's function technique [116].

### 3.2.3 Inclusion of Parasitics

#### Our Approach

We used parasitic capacitances and resistances, extracted or calculated as described further below, in conjunction with the values of the transport-dependent parameters $g_m$, $g_o$, and $C_{\text{gg}}$, to find the RF figures of merit $f_T$ and $f_{\text{max}}$ for the overall transistor by simulation of the transistor equivalent circuit (Fig. 3.2).

In order to quantify the effects of contact resistance, we extract the extrinsic figures of merit $f_T$ and $f_{\text{max}}$ from the transistor equivalent circuit as a function of realized contact resistance $\rho_C$: $f_T(\rho_C)$ and $f_{\text{max}}(\rho_C)$. This is accomplished by assuming the device width

(into the page) in Fig. 3.1 is $W = 1\,\mu$m, as we have already mentioned, and hence setting $R_s = R_d = R_C$, with $R_C = \rho_C/1\,\mu$m, in the circuit. It is important to note that the use of $W = 1\ \mu$m to extract $f_T(\rho_C)$ and $f_{\max}(\rho_C)$ incurs no loss of generality, since all the parameters in the circuit, from which the figures of merit are obtained, scale with $W$ in such a way so as to leave $f_T(\rho_C)$ and $f_{\max}(\rho_C)$ unaffected by the value of $W$. We explicitly verified this to be the case, but it can also be seen, for example, by inspection of (3.1) and (3.2) further below; all terms in the numerator and denominator can be shown to scale proportionally or inversely with $W$, such that the final result is unaffected. Hence, in what follows, we consider $f_T(\rho_C)$ and $f_{\max}(\rho_C)$ as general measures of the RF performance that could be achieved for realized values of $\rho_C$, with all parasitic capacitances and resistances corresponding to $W = 1\,\mu$m, and we focus on how graphene and SL $MoS_2$ compare as a function of $\rho_C$.

**Capacitances**

The parasitic capacitances $C'_{\text{gd}}$, $C'_{\text{gs}}$, and $C'_{\text{sd}}$ in the circuit of Fig. 3.2 are found by simulating an open structure; the open structure includes the entire device in Fig. 3.1, with the exclusion of the channel material. The capacitances are measured using COMSOL Multiphysics [148] by applying a small voltage to one contact and measuring the induced charge on the other contacts, one at a time. Since we are using identical structures for each channel material, the values for the parasitic capacitances with SL $MoS_2$ and graphene will be the same. In addition to the assumed device width of 1 $\mu$m, a few other parameters needed for the extraction are specified by the ITRS [3] for the 7-nm node, as provided in Table 3.1. Beyond these specified parameters, those remaining are the length and height of the source and drain contacts ($L_C$ and $H_C$), the height of the gate contact ($H_G$), and the length of the metal extension regions ($L_{\text{C,e}}$). Unfortunately, the exact values of these dimensions for the 7-nm node are uncertain. Due to this uncertainty, we have simulated different combina-

Table 3.2: External Structure Parameters

| Parameter | Description | Range [nm] |
|---|---|---|
| $H_G$ | Gate Height | 10-50 |
| $H_C$ | S/D Contact Height | 10-50 |
| $L_C$ | S/D Contact Length | 100-1000 |
| $L_{\text{C,e}}$ | S/D Extension Length | 10-30 |

tions of $H_C$, $H_G$, $L_{\text{C,e}}$, and $L_C$; the range of simulated values can be found in Table 3.2. We found that these figures of merit deviated by no more than five percent about their average values as a function of the capacitances, holding the other parameters fixed and as the capacitances varied over the range of dimensions specified in Table 3.2.[2] Given the small deviation of $\pm 5\%$, there is hence no loss of generality in using the average values over capacitance as representative of the RF performance, and these are therefore the values presented in the following sections.

**Contact Resistance**

The parasitic resistances $R_s$, $R_d$, and $R_g$ of the source, drain, and gate, respectively, are included in the circuit of Fig. 3.2. The considerable impact of these resistances on high-frequency operation motivates us to treat them as key parameters in our study. Appropriate values can be computed by knowing contact resistance and the device geometry.

The values of realized contact resistance $\rho_C$ are typically quoted in the literature in the units of $\Omega \cdot \mu\text{m}$; the corresponding resistance values $R_s$ and $R_d$ determining RF performance would be $\rho_C$ divided by the device width (into the page) of $W = 1$ $\mu$m in Fig. 3.1. This method of calculating $R_s$ and $R_d$ is justified since current crowding is consistently observed in single-layer devices; the current transfers over a characteristic length $L_T$ [149, 150, 151], and contacts longer than $L_T$ exhibit similar contact resistances that depend only on

[2]The capacitances themselves varied as follows: $C'_{\text{sd}}$ varied from 35 to 65 aF/$\mu$m, and $C'_{\text{gs}}$ and $C'_{\text{gd}}$ varied from 99 to 124 aF/$\mu$m.

width [63]. $L_T$ is estimated to be 200–520 nm for graphene [149] and 74–630 nm for SL $MoS_2$ [152, 153]. The results in this chapter hence strictly apply to structures having $L_C \geq L_T$, although this is not a limitation, since $L_C \geq L_T$ would be required to keep the contact resistance low to optimize RF performance.

**Gate Resistance** $R_g$

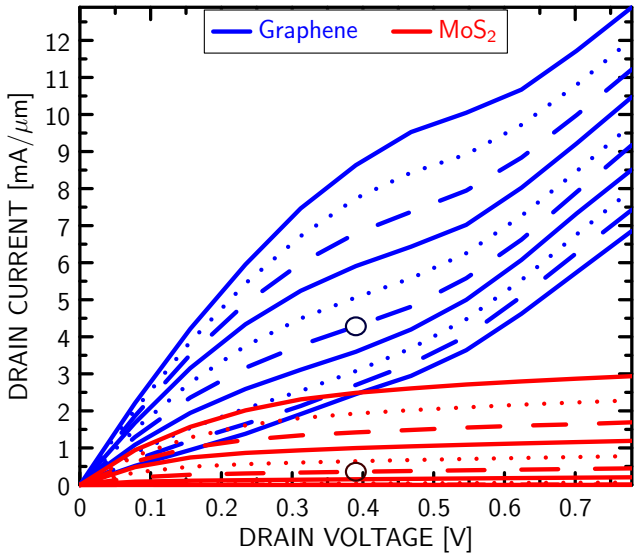
The gate resistance is strongly dependent on the physical layout of the device, and it can be minimized by the use of multiple gate fingers in parallel. In this way, the value of gate resistance can be reduced to the order of a few ohms. Due to the flexibility in achieving desired gate resistance via appropriate layout, we treat the gate resistance as a parameter, with values ranging from 0.1 $\Omega$ to 1 k$\Omega$. We will return to this point in Section 3.5.2.

## 3.3 Summary of Transport-Dependent RF Performance

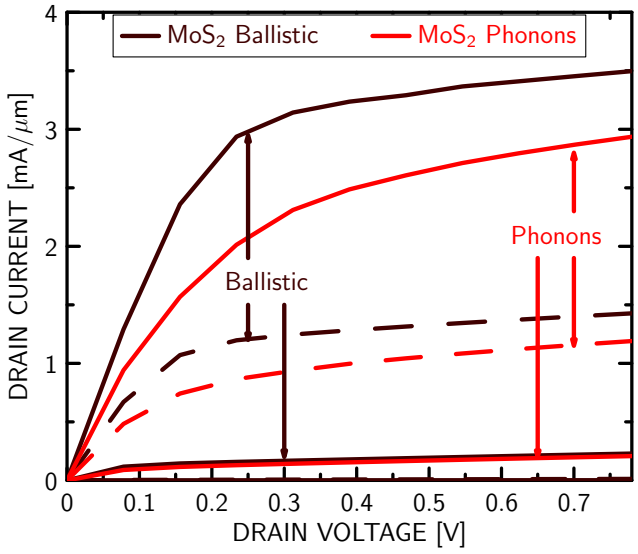
The first step in comparing the overall potential of the two materials is to investigate the RF parameters arising from transport within the critical (intrinsic) operating region of the common device structure, *i.e.*, within the dotted portion of Fig. 3.1. These parameters are the transconductance $g_m$, the internal gate capacitance $C_{\text{gg}} = C_{\text{gs}} + C_{\text{gd}}$, and the output conductance $g_o$, and the corresponding circuit elements are those within the dashed portion of Fig. 3.2. We will keep the discussion in this section very brief; those familiar with the results can skip to Section 3.4.

### 3.3.1 Terminal Characteristics

For reference, we begin with the simulated terminal characteristics of the intrinsic device for the two channel materials, as shown in Fig. 3.3(a). A few features are immediately visible. First, for biasing determined by the same voltages, *e.g.*, $(V_{\text{GS}}, V_{\text{DS}}) = (V_{\text{DD}}/2, V_{\text{DD}}/2)$, where $V_{\text{DD}} = 0.78$ V [3], as circled on the curves, graphene yields much higher current den-




(a)




(b)

Figure 3.3: Summary of terminal characteristics. (a) Current-voltage relationships for graphene and SL $MoS_2$ found from a transport simulation of the dotted portion of Fig. 3.1, shown for gate voltages ranging from $V_{GS} = 0.078$ to $V_{GS} = V_{DD} \equiv 0.78$ V [3] in increments of 0.078 V. The circles on each set of curves indicate the locations of a representative bias point corresponding to applied voltages $V_{GS} = V_{DS} = V_{DD}/2$. (b) The current including phonon scattering vs. ballistic transport for SL $MoS_2$.

sities. Second, the lack of a bandgap in graphene causes the characteristics never to fully saturate, whereas the curves for SL $MoS_2$ do saturate, a fact that is well known, but which we point out for completeness. Finally, Fig. 3.3 (b) illustrates the reduction in current with phonon scattering vs. ideal ballistic transport in SL $MoS_2$.

### 3.3.2 Transconductance and Gate Capacitance

Fig. 3.4(a) shows $g_m$ and $C_{\text{gg}}$ for both materials as a function of $V_{\text{GS}}$, with $V_{\text{DS}}$ held at $V_{\text{DD}}/2$. The $g_m$ is significantly higher in graphene. On the other hand, $C_{\text{gg}}$ is similar in magnitude for the two materials. The similarity in $C_{\text{gg}}$ is a direct outcome of employing identical gate structures for both channel materials in Fig. 3.1, leading to identical gate-oxide capacitance values. For both materials, the gate-oxide capacitance dominates $C_{\text{gg}}$, with the quantum capacitance having only a secondary impact.

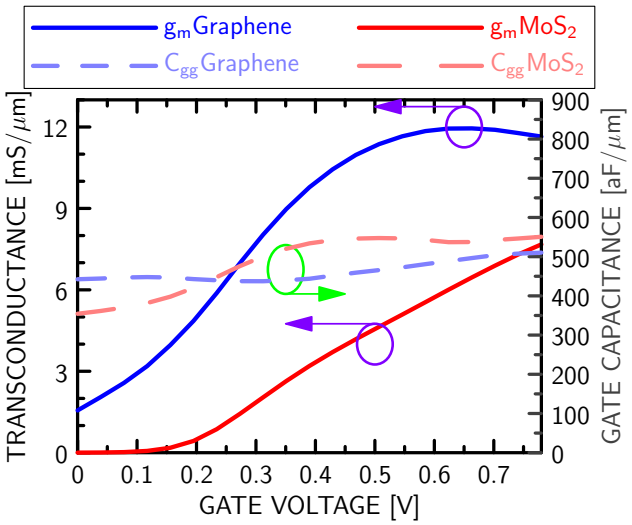
### 3.3.3 Output Conductance

It is well-known that the lack of a bandgap in graphene leads to poor output conductance [28]. The results in Fig. 3.4(b) confirm the expectation, showing that $g_o$ in graphene is substantially worse than in SL $MoS_2$. The inset to the figure shows one immediate impact, which is to severely limit the available voltage gain $A_v = g_m/g_o$ in graphene, despite its higher $g_m$. The poor $g_o$ of graphene has even further ramifications in determining its overall RF performance vs. SL $MoS_2$, once the impacts of parasitics are considered, as we will discuss in Section 3.4.

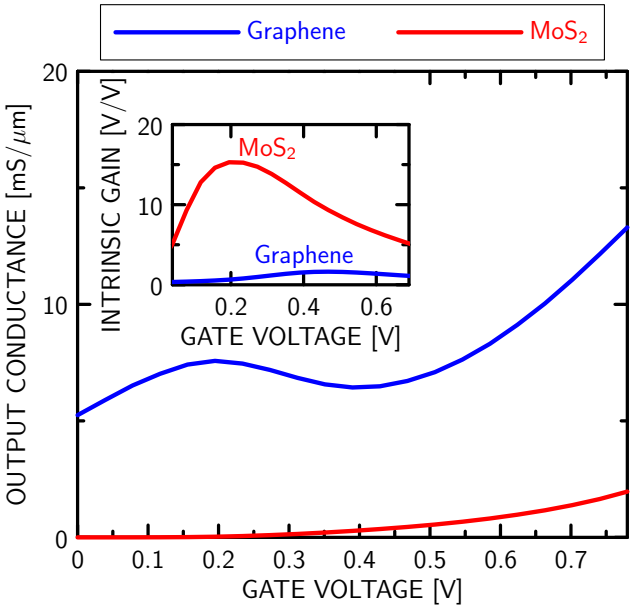
## 3.4 Peak Unity-Current-Gain Frequency $f_T$

### 3.4.1 Definition

The $f_T$ is found by extrapolating the magnitude of the common-source, small-signal current gain to unity. While we found $f_T$ exactly, by simulation of the circuit in Fig. 3.2, a useful




(a)




(b)

Figure 3.4: Summary of transport-dependent RF performance metrics. (a) Transconductance $g_m$ and gate capacitance $C_{\text{gg}}$ vs. gate voltage $V_{\text{GS}}$ for graphene and SL $MoS_2$. The drain voltage is held at $V_{\text{DS}} = V_{\text{DD}}/2$, where $V_{\text{DD}} = 0.78$ V [3]. (b) Output conductance $g_o$ vs. gate voltage $V_{\text{GS}}$ for graphene and SL $MoS_2$. The drain voltage is held at $V_{\text{DS}} = V_{\text{DD}}/2$, where $V_{\text{DD}} = 0.78$ V [3]. The inset to the figure is the available voltage gain $A_v = g_m/g_o$ vs. $V_{\text{GS}}$ for both materials, under the same value of $V_{\text{DS}}$.

approximation is [124]

$$f_T \approx \frac{1}{2\pi} \frac{g_m}{C_{\text{gg,tot}} + \left[g_o C_{\text{gg,tot}} + g_m C_{\text{gd,tot}}\right](R_s + R_d)} \tag{3.1}$$

where $C_{\text{gg,tot}} \equiv C_{\text{gg}} + C'_{\text{gs}} + C'_{\text{gd}}$ is the total gate capacitance and $C_{\text{gd,tot}} \equiv C_{\text{gd}} + C'_{\text{gd}}$ is the total gate-drain capacitance. This expression serves to illustrate how the transport-dependent circuit elements $g_m$, $g_o$, and $C_{\text{gg}}$ discussed in Section 3.3 *interact* with the parasitics to degrade the high-frequency performance of the transistor, and we will refer to it as needed in the remainder of this chapter.

In this section, we will focus on the *peak* value of $f_T$, where "peak" means "absolute maximum" over all gate and drain bias voltages, $0 \leq V_{\text{GS}} \leq V_{\text{DD}}$ and $0 \leq V_{\text{DS}} \leq V_{\text{DD}}$, with $V_{\text{GS}}$ and $V_{\text{DS}}$ referring to the biases used across the internal transistor (within the dotted portion of Fig. 3.1) to determine the internal transistor components (within the dashed lines of Fig. 3.2). Later, in Section 3.6, we will consider the value of $f_T$ under the condition of a fixed bias current.

### 3.4.2 General Behavior vs. $\rho_C$

Fig. 3.5 shows a plot of the peak $f_T(\rho_C)$ vs. the contact resistance $\rho_C$ determining $R_s$ and $R_d$ in the two materials. We have indicated several important pieces of information on the plot.

- Solid curves are used to show the peak $f_T(\rho_C)$ with no simplifications.
- Dotted curves are used to show the value of the peak $f_T(\rho_C)$ when neglecting the effect of the output conductance $g_o$, in order to assess the role of the bandgap in each material.
- Short-dashed vertical lines are used to indicate the best contact resistances realized to date in graphene and SL $MoS_2$ of 100 $\Omega \cdot \mu$m [137] and 1 k$\Omega \cdot \mu$m [67], respectively.

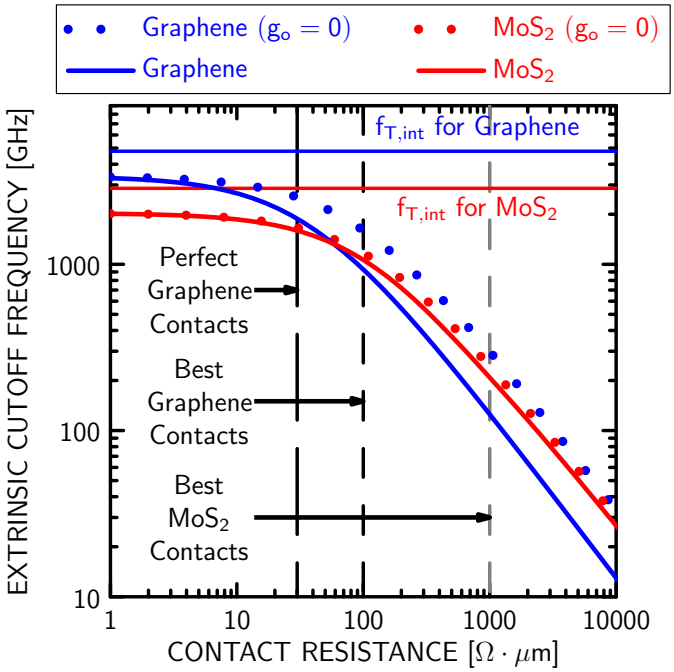



Figure 3.5: Plot of the peak (absolute maximum) unity-current-gain frequency $f_T(\rho_C)$ for SL $MoS_2$ and graphene vs. the contact resistance $\rho_C$ determining the drain and source resistances $R_s$ and $R_d$ (solid curves). The values of peak $f_T(\rho_C)$ are found assuming a device width of 1 $\mu$m, as discussed in the text of Section 3.2.3. The dotted curves show the values when neglecting the effect of the output conductance $g_o$. The best contact resistances achieved to date in the two materials are represented by the short-dashed vertical lines, and the resistance for perfect graphene contacts are indicated by a long-dashed vertical line. The peak intrinsic cutoff frequency $f_{\text{T,int}} = g_m/2\pi C_{\text{gg}}$, *i.e.*, the peak cutoff frequency neglecting all parasitics, is indicated for each device with a horizontal line at the top of the figure.

- A long-dashed vertical line is used to indicate 30 $\Omega \cdot \mu$m, the theoretical minimum contact resistance in graphene [120]. We add that 30 $\Omega \cdot \mu$m represents a lower bound on the contact resistance for both materials, as it is unlikely that contacts to SL $MoS_2$ could ever achieve the same efficiency as contacts to graphene.

- Horizontal lines are used to indicate the peak intrinsic (neglecting all parasitics) cutoff frequency, given by $f_{\text{T,int}} = g_m/2\pi C_{\text{gg}}$, for each material.

Since Fig. 3.5 embeds several pieces of information, it will be most convenient to discuss the various aspects one at a time, and then to gather together the most important

outcomes.

### 3.4.3 Performance Ceiling

The values of the peak intrinsic cutoff frequency $f_{\text{T,int}} = g_m/2\pi C_{\text{gg}}$ indicated by the horizontal lines in Fig. 3.5 can be considered as measures of the "raw speed" of each material, as determined by *transport effects* in the transistor channel, and excluding the detrimental effects of the output conductance $g_o$ and parasitics. From Fig. 3.4(a), since the internal gate capacitance $C_{\text{gg}}$ is similar for both materials, the raw speeds are determined primarily by the peak values of $g_m$. The higher peak $g_m$ in graphene gives it a higher performance ceiling.

### 3.4.4 Behavior for Low and High Contact Resistance

A severe reduction in the peak $f_T(\rho_C)$ with increasing contact resistance $\rho_C$ is observed in Fig. 3.5 for both materials, as shown by the monotonically decreasing (moving to the right) solid curves, highlighting the need to keep $\rho_C$ as low as possible. It is worth noting that achieving zero contact resistance does not mean the $f_T(\rho_C)$ will equal the performance ceiling indicated by the intrinsic limit $f_{\text{T,int}}$; the presence of parasitic capacitances will by themselves cause the peak $f_T(\rho_C)$ to fall short of the intrinsic limit $f_{\text{T,int}}$, even when $\rho_C \to 0$, as illustrated by the behavior of the solid curves on the far left side of Fig. 3.5. We found that the parasitic capacitances $C'_{\text{gs}}$, $C'_{\text{gd}}$, and $C'_{\text{sd}}$ cause a uniform degradation of the curves in Fig. 3.5 for both graphene and SL $MoS_2$ (from where they would otherwise be) by about 30%.

### 3.4.5 Effect of $g_o$

For graphene, a substantial reduction in peak $f_T(\rho_C)$ is observed when accounting for the effect of $g_o$, as evidenced by the large gap between the solid and dotted graphene curves in

Fig. 3.5. For example, at today's best contact resistance of $\rho_C = 100\ \Omega \cdot \mu\mathrm{m}$, the reduction in peak $f_T(\rho_C)$ in graphene due to $g_o$ is around 700 GHz, from 1.6 THz to 900 MHz, representing a degradation of 40%. This $g_o$-driven reduction is more severe than we have previously calculated for longer channel devices [28], suggesting that single-layer GFETs may not scale well to lower technology nodes. The reduction can be viewed as arising from the $g_o(R_s + R_d)$ term in the denominator of (3.1), where $R_s = R_d = \rho_C/1\ \mu$m; only when $\rho_C \to 0$ can the reduction be neglected, as shown by the merging of the solid and dotted graphene curves for low $\rho_C$ in Fig. 3.5.

For SL $MoS_2$, the impact of $g_o$ on peak $f_T(\rho_C)$ is negligible, as evidenced by the strong overlap between the solid and dotted SL $MoS_2$ curves in Fig. 3.5. As might be expected, the large bandgap in SL $MoS_2$ keeps $g_o$ sufficiently low to have a negligible impact, even in the presence of phonon scattering, which we have included for SL $MoS_2$.

### 3.4.6 Comparison with Identical Contact Resistance

The peak $f_T(\rho_C)$ of SL $MoS_2$ is higher than in graphene for any fixed and identical contact resistance greater than $60\ \Omega \cdot \mu\mathrm{m}$, as shown by the relative positions of the solid curves in Fig. 3.5 for $\rho_C > 60\ \Omega \cdot \mu\mathrm{m}$. For contact resistances less than $60\ \Omega \cdot \mu\mathrm{m}$, a *crossover* is observed, and graphene's peak $f_T(\rho_C)$ is higher. The crossover is due to different trends in the behavior of the peak $f_T(\rho_C)$ in the two materials. In graphene, a larger peak $f_T(\rho_C)$ is observed for low $\rho_C$ due to a large $g_m$, followed by a *rapid decline* in the peak $f_T(\rho_C)$ with $\rho_C$ due to a large $g_o$ (interacting with $R_s$ and $R_d$ resulting from $\rho_C$). In SL $MoS_2$, a lower peak $f_T(\rho_C)$ due to a smaller $g_m$ is observed for low $\rho_C$, followed by a *shallower decline* in peak $f_T(\rho_C)$ with $\rho_C$ due to a small value of $g_o$. The crossover value of $60\ \Omega \cdot \mu\mathrm{m}$ is only slightly larger than the theoretical minimum contact resistance of graphene [120], meaning that for *fixed and realizable (above the theoretical minimum)* common values of $\rho_C$ in the two materials, we can say that the peak $f_T(\rho_C)$ in SL $MoS_2$ will typically be higher than,

and at least roughly equal to, that of graphene.

### 3.4.7 Comparison with Present-Day Contact Resistance

The greater performance potential for SL $MoS_2$ at common values of $\rho_C$, indicated by the relative positions of the solid curves in Fig. 3.5 for $\rho_C > 60\,\Omega \cdot \mu\mathrm{m}$, is difficult to realize, because the processing steps are not yet available to make similar quality contacts for both materials in their single-layer forms. As discussed in Section 3.1, contact resistance in single-layer graphene is currently a factor of ten lower than in SL $MoS_2$. Using the best achieved contact resistance to date for each single-layer material, Fig. 3.5 indicates a peak $f_T(\rho_C)$ of 930 GHz for graphene at $\rho_C = 100\ \Omega \cdot \mu\mathrm{m}$ and 210 GHz for SL $MoS_2$ at $\rho_C = 1\ \mathrm{k}\Omega \cdot \mu\mathrm{m}$.

In order for SL $MoS_2$ to achieve graphene's value of 930 GHz, the contact resistance would have to be lowered below $130\ \Omega \cdot \mu\mathrm{m}$. Unfortunately, $130\ \Omega \cdot \mu\mathrm{m}$ is far better than the best achieved to date for SL $MoS_2$ transistors; fortunately, it is also *worse* than the best achieved value of $100\ \Omega \cdot \mu\mathrm{m}$ in ML $MoS_2$, suggesting ML $MoS_2$ as a potential path forward to get the peak performance of $MoS_2$ devices closer to what can presently be achieved with graphene.

### 3.4.8 Possibility of THz $f_T$

The possibility of achieving a peak unity-current-gain frequency of at least 1 THz is an important technological barrier. Even with the large reduction in peak $f_T(\rho_C)$ due to the poor output conductance in graphene, a value of 1 THz is achievable if $\rho_C$ could be made below $90\ \Omega \cdot \mu\mathrm{m}$, which represents an incremental improvement over current graphene contact resistances. On the other hand, for SL $MoS_2$, the contact resistance would need to be made below $100\ \Omega \cdot \mu\mathrm{m}$, a considerably more daunting task, but possible for ML $MoS_2$.

### 3.4.9 Outcomes

Based on the detailed points above, Fig. 3.5 points to the following important outcomes.

- For any *common* value of contact resistance greater than $\rho_C = 60\ \Omega \cdot \mu\mathrm{m}$, SL $MoS_2$ would exhibit a higher peak unity-current-gain frequency, with graphene suffering from the deleterious effects of its poor output conductance.

- However, at present, SL $MoS_2$ suffers from much poorer contact resistances. As a result, the peak performance of graphene remains superior if one compares the performance using the *best* $\rho_C$ values achieved to date. The contact resistance of SL $MoS_2$ would have to be lowered considerably to match graphene.

- For devices corresponding to the 7-nm technology node [3], peak values of $f_T$ of 1 THz or above can be achieved in both materials, but this barrier is more easily reached with graphene, requiring only an incremental improvement in contact resistance from what has been achieved to date.

## 3.5 Peak Unity-Power-Gain Frequency $f_{\mathbf{max}}$

### 3.5.1 Definition

The $f_{\mathrm{max}}$ is calculated by extrapolating Mason's unilateral gain ($U$) [123] to unity. While we found $f_{\mathrm{max}}$ exactly through simulation of the circuit in Fig. 3.2, a useful approximation is [124]

$$f_{\mathrm{max}} \approx \frac{f_T}{\sqrt{\left[4g_o + 8\pi f_T C_{\mathrm{gd,tot}}\right] R_g + \left[\alpha_M 8\pi f_T C_{\mathrm{gd,tot}}\right] R_d}} \tag{3.2}$$

where

$$\alpha_M \equiv \frac{C_{\mathrm{gd,tot}} + C'_{\mathrm{sd}}}{C_{\mathrm{gg,tot}}}. \tag{3.3}$$

A lone factor of $f_T$ is found in the numerator of (3.2), meaning that the two terms in the denominator, one depending on $R_g$ and the other on $R_d = \rho_C/1\ \mu$m, can be conceptualized

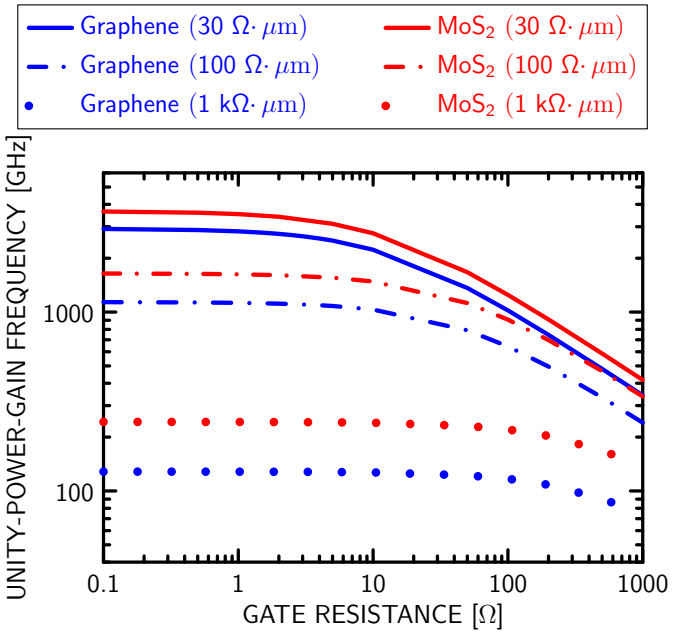



Figure 3.6: Peak (absolute maximum over all bias voltages) unity-power-gain frequency $f_{\max}(R_g)$ vs. gate resistance $R_g$ for graphene and $MoS_2$. Separate curves are shown for values of contact resistance $\rho_C$ equal to $30\ \Omega \cdot \mu\text{m}$, $100\ \Omega \cdot \mu\text{m}$, and $1\ \text{k}\Omega \cdot \mu\text{m}$.

as *modifying* the $f_T$ to arrive at a value of $f_{\max}$. We will refer to this expression as needed in the remainder of this chapter.

In this section, we will consider the peak $f_{\max}$, where "peak" means "absolute maximum" over all gate and drain bias voltages, $0 \leq V_{GS} \leq V_{DD}$ and $0 \leq V_{DS} \leq V_{DD}$. Later, in Section 3.6, we will consider the $f_{\max}$ under the constraint of a fixed bias current.

### 3.5.2 Effect of Gate Resistance

In contrast to the negligible impact the gate resistance $R_g$ has on $f_T$, it is an important quantity when considering $f_{\max}$. Fig. 3.6 shows a plot of peak $f_{\max}$ vs. gate resistance $R_g$, which we denote as $f_{\max}(R_g)$ vs. $R_g$. Results are shown for various assumed values of contact resistance $\rho_C$, where $\rho_C$ determines $R_s$ and $R_d$. Three sets of curves are marked, representing the best contact resistances realized to date in SL $MoS_2$ ($1\ \text{k}\Omega \cdot \mu\text{m}$)

and graphene (100 $\Omega \cdot \mu\mathrm{m}$) and the theoretical minimum contact resistance achievable in graphene (30 $\Omega \cdot \mu\mathrm{m}$).

It is well-known that the gate resistance can be reduced by appropriate layout techniques. Fig. 3.6 shows that as $R_g$ is reduced, $f_{\max}(R_g)$ *saturates* to a maximum value, with the value of $R_g$ needed for the saturation determined by the value of $\rho_C$. Higher values of $\rho_C$ cause the saturation to occur at higher values of $R_g$. Such behavior is expected from (3.2), as reducing $R_g$ in the denominator becomes less important when the term involving $R_d = \rho_C/1\ \mu$m is larger.

Note that for every value of $\rho_C$ used in Fig. 3.6, the corresponding curve can be taken to be saturated for values of $R_g = 1\ \Omega$ or lower. Given that values of gate resistance as low as $R_g = 3\ \Omega$ have already been achieved for 7-$\mu$m-wide graphene devices with two gate fingers [82], and since we are interested in best performance, it is hence convenient for the remainder of this discussion to use $R_g = 1\ \Omega$.

### 3.5.3 General Behavior vs. $\rho_C$

Fig. 3.7 shows a plot of the peak $f_{\max}(\rho_C)$ vs. contact resistance $\rho_C$, found with a gate resistance $R_g = 1\ \Omega$, and where $R_s = R_d = \rho_C/1\ \mu$m. As with Fig. 3.5 discussed earlier, we have included dotted curves to show the values of peak $f_{\max}(\rho_C)$ when neglecting the output conductance $g_o$, short-dashed vertical lines to indicate the best contact resistances realized to date, and a long-dashed vertical line to indicate the theoretical minimum contact resistance achievable in graphene.

As with the peak $f_T(\rho_C)$ in Fig. 3.5, Fig. 3.7 shows a severe reduction of the peak $f_{\max}(\rho_C)$ with increasing contact resistance $\rho_C$, again highlighting the need to keep $\rho_C$ as low as possible.

Fig. 3.7 points to a number of other important features regarding the peak $f_{\max}(\rho_C)$, which we examine individually before summarizing the main outcome.

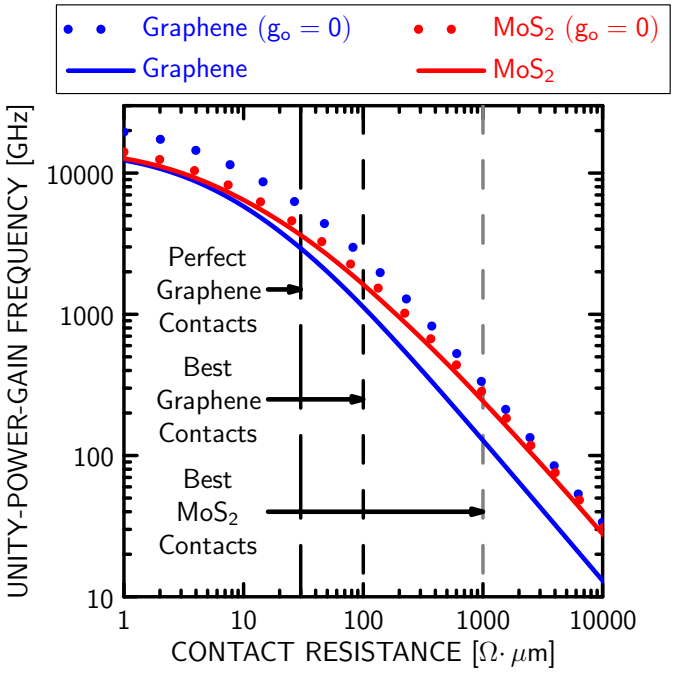



Figure 3.7: Peak unity-power-gain frequency $f_{\max}(\rho_C)$ vs. the contact resistance $\rho_C$ determining the source and drain resistances $R_s$ and $R_d$, with $R_g$ held at $1\,\Omega$, as discussed in the text.

### 3.5.4 Effect of $g_o$

For graphene, the output conductance significantly reduces the peak $f_{\max}(\rho_C)$, as seen by comparing the solid and dotted graphene curves in Fig. 3.7; for example, at $\rho_C = 100\,\Omega \cdot \mu\mathrm{m}$, it drops from 2.6 THz to 1.1 THz. Fig. 3.7 also shows that the effect of $g_o$ on $f_{\max}(\rho_C)$ for graphene cannot be eliminated by minimizing the contact resistance, contrasting what we observed in Fig. 3.5 for the peak $f_T(\rho_C)$; specifically, the graphene curves in Fig. 3.7 with and without $g_o$ do not converge at low values of contact resistance. This behavior can be attributed to the $g_o R_g$ product in the denominator of (3.2), which does not vanish even when $\rho_C \to 0$.

For SL $MoS_2$, the curves in Fig. 3.7 show that the reduction in peak $f_{\max}(\rho_C)$ due to $g_o$ is small; a reduction of around 10% is observed for the range of contact resistances

considered. As expected, the bandgap in SL $MoS_2$ keeps $g_o$ sufficiently small for it to have a minimum impact, even in the presence of phonon scattering, which we have included for SL $MoS_2$.

### 3.5.5 Comparison with Identical Contact Resistance

For all identical values of $\rho_C$, the $f_{\max}(\rho_C)$ in SL $MoS_2$ is higher than in graphene, as shown by the solid curves in Fig. 3.7. It is also worth noting that unlike what we observed with the $f_T(\rho_C)$ in Fig. 3.5, there is no *crossover* of the graphene and SL $MoS_2$ performance curves at sufficiently low values of $\rho_C$. The lack of a crossover can be attributed to the $g_o R_g$ product in the denominator of (3.2), which persists in degrading the peak $f_{\max}(\rho_C)$ of graphene even when $\rho_C \to 0$, due to a pronounced $g_o$.

### 3.5.6 Comparison with Present-Day Contact Resistance

Current technology limits $\rho_C$ to $100\ \Omega \cdot \mu\mathrm{m}$ in graphene and 1 $\mathrm{k}\Omega \cdot \mu\mathrm{m}$ in SL $MoS_2$. With these different values of contact resistance, we find the peak $f_{\max}(\rho_C)$ values to be 1.1 THz for graphene (at $\rho_C$ =100 $\Omega \cdot \mu\mathrm{m}$) and 240 GHz for SL $MoS_2$ (at $\rho_C$=1 $\mathrm{k}\Omega \cdot \mu\mathrm{m}$).

Based on *current* contact technology, SL $MoS_2$ hence cannot match graphene. To reach graphene's value of 1.1 THz, $MoS_2$ would require a contact resistance below 160 $\Omega \cdot \mu\mathrm{m}$, which has only been achieved with ML $MoS_2$.

### 3.5.7 Possibility of THz $f_{\max}$

Finally, both graphene and SL $MoS_2$ should be able to achieve a peak unity-power-gain frequency of 1 THz.

Graphene can achieve $f_{\max}(\rho_C) = 1$ THz operation with a contact resistance around $110\ \Omega \cdot \mu\mathrm{m}$, which has already been achieved. However, reductions in the gate length and optimization in the gate layout will be needed; the current record of 70 GHz [82]

was obtained with a gate length of 100 nm, an order of magnitude larger than the ITRS specifications for the 7-nm node [3] used as guidance for the work in this chapter.

An $f_{\max}$ of 1 THz can be achieved in SL $MoS_2$ with contact resistances of approximately 170 $\Omega \cdot \mu\mathrm{m}$, a value that has been achieved in multi-layer devices.

### 3.5.8 Outcome

The outcome from Fig. 3.7 regarding the peak $f_{\max}(\rho_C)$ largely mirrors what we saw in Section 3.4 for the peak $f_T(\rho_C)$. Supported by the detailed discussion in this section, we can say that at identical contact resistances, SL $MoS_2$ would outperform graphene in terms of the peak $f_{\max}(\rho_C)$, but that $MoS_2$ contact technology simply lags that of graphene, such that with today's values of $\rho_C$, graphene retains the performance edge. Similarly, while THz operation should be possible in both materials, SL $MoS_2$ would require a substantial improvement in its contact resistance.

## 3.6 Comparison with Equal Bias Currents

### 3.6.1 Motivation

Until this point, we have emphasized the comparison of *peak* performance (over all bias conditions) for graphene and SL $MoS_2$. However, the minimization of dc bias current is an important consideration (*e.g.*, to minimize the power drawn from the supply $V_{\mathrm{DD}}$). For the 7-nm technology node, the minimum on current for a transistor is specified to be approximately 1.65 $\mathrm{mA}/\mu\mathrm{m}$ [3]. We will now compare the $f_T$ and $f_{\max}$ under the constraint that the devices each carry this bias current, although our results are independent of the exact value chosen.

We will consider the most important aspects of the $f_T$ and $f_{\max}$ separately, and then state the main outcome.

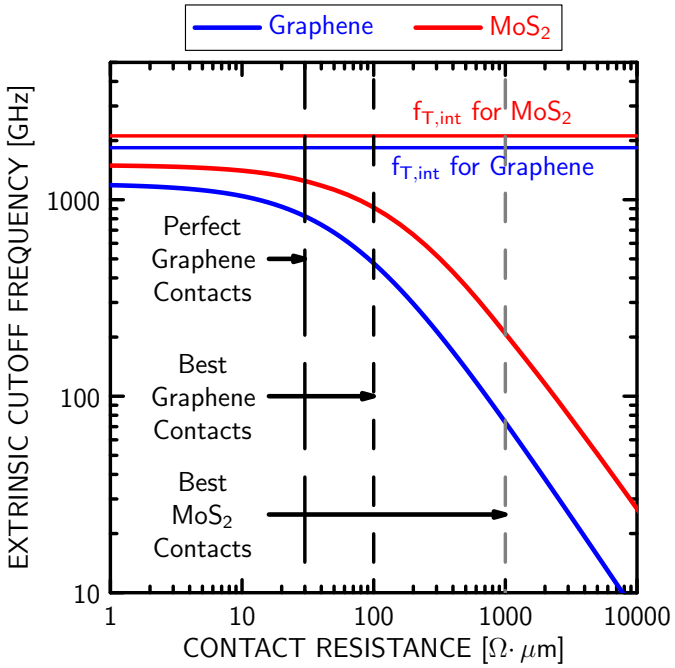



Figure 3.8: Plot of the unity-current-gain frequency $f_T(\rho_C)$ for SL $MoS_2$ and graphene vs. the contact resistance $\rho_C$ determining the source and drain resistances $R_s$ and $R_d$ (solid curves), found under the constraint of a bias current of 1.65 mA/$\mu$m. The values of $f_T(\rho_C)$ are found assuming a device width of 1 $\mu$m, as discussed in the text of Section 3.2.3. The best contact resistances achieved to date for the two materials are represented by the short-dashed vertical lines, and the resistance for perfect graphene contacts are indicated by a long-dashed vertical line. The peak intrinsic cutoff frequency $f_{T,\text{int}} = g_m/2\pi C_{gg}$, *i.e.*, the peak cutoff frequency neglecting all parasitics, is indicated for each device with a horizontal line at the top of the figure.

### 3.6.2 Unity-Current-Gain Frequency $f_T(\rho_C)$

Fig. 3.8 shows a plot of the unity-current-gain frequency $f_T(\rho_C)$ vs. contact resistance $\rho_C$, *under the constraint of equal bias currents, set to 1.65 mA/$\mu$m in both materials.* The following observations can be made and should be contrasted with the results from Fig. 3.5, which showed the *peak* $f_T(\rho_C)$ (over all bias conditions).

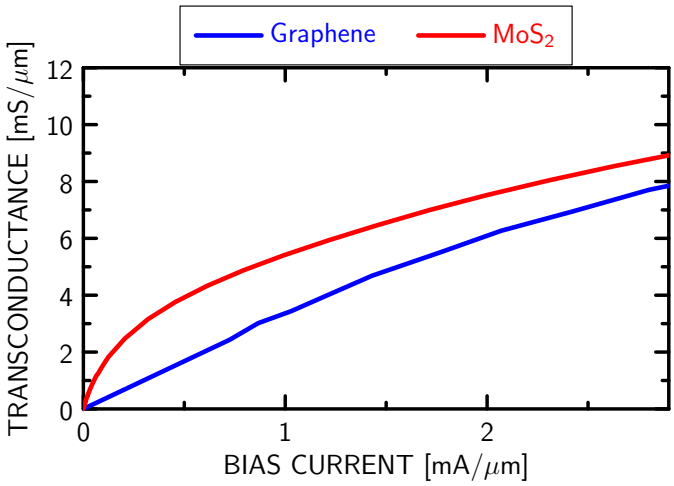



Figure 3.9: Transconductance $g_m$ vs. bias current $I_D$ for graphene and SL $MoS_2$ transistors. The drain and gate voltages were adjusted to provide the largest possible value of $g_m$ at each value of $I_D$.

**Performance Ceiling**

Fig. 3.9 depicts the transconductance $g_m$ vs. the bias current $I_D$. In contrast to Fig. 3.4(a) for equal *voltages*, under the constraint of equal bias currents, the $g_m$ in $MoS_2$ will become larger than that in graphene. While the underlying physical details are outside the scope of the present chapter, this reversal can be attributed to the presence of a bandgap and high density of states in SL $MoS_2$. The higher $g_m$ in $MoS_2$ causes it to achieve a higher value of $f_{\text{T,int}} = g_m/2\pi C_{\text{gg}}$ than graphene. The higher $f_{\text{T,int}}$ is reflected in the horizontal lines in Fig. 3.8, which hence show a reversal in the trend we saw in Fig. 3.5 when considering peak performance over all bias conditions.

**Comparison with Present-Day Contact Resistance**

With a bias current of 1.65 mA/$\mu$m, and for the best achieved contact resistance $\rho_C = 100\ \Omega \cdot \mu\text{m}$ in graphene, the $f_T(\rho_C)$ in graphene drops nearly 50%, from its peak value of 930 GHz in Fig. 3.5 to a current-constrained value of 475 GHz in Fig. 3.8. On the other hand, for SL $MoS_2$, at the best-achieved contact resistance of $\rho_C = 1\ \text{k}\Omega \cdot \mu\text{m}$, the $f_T(\rho_C)$

in Figs. 3.5 and 3.8 are roughly the same at $f_T(\rho_C) = 210$ GHz. The drop in graphene is driven by the large reduction in $g_m$, from a peak of 14.9 mS/$\mu$m to a current-constrained 4.5 mS/$\mu$m, while the invariance in SL $MoS_2$ is due to a much smaller reduction in $g_m$, from a peak of 9 mS/$\mu$m to a current-constrained 6.9 mS/$\mu$m.

These results suggest that, when considering performance under the constraint of equal bias currents, as opposed to peak performance over all possible bias conditions, the gap in performance between graphene and SL $MoS_2$, for present-day contact technology, is not as severe as originally suggested in Section 3.4. In fact, with equal bias currents, a contact resistance of 375 $\Omega \cdot \mu$m realized in SL $MoS_2$ would be sufficient to bridge the gap to the value of unity-current-gain frequency currently possible in graphene.

**THz Operation**

For the bias current considered in this study, graphene cannot achieve an $f_T(\rho_C)$ of 1 THz; in fact, even with perfect graphene contacts, Fig. 3.8 shows that only $f_T(\rho_C) = 800$ GHz can be reached. On the other hand, for SL $MoS_2$, operation at 1 THz can be reached with a contact resistance of 80 $\Omega \cdot \mu$m, which is very nearly achieved with ML $MoS_2$.

**Outlook with Perfect Contacts**

Under equal bias currents, Fig. 3.8 shows that the 800-GHz value of $f_T(\rho_C)$ achievable with perfect graphene contacts can be matched by SL $MoS_2$ with 220 $\Omega \cdot \mu$m contacts.

### 3.6.3 Unity-Power-Gain Frequency $f_{\mathbf{max}}(\rho_C)$

Fig. 3.10 shows a plot of the unity-power-gain frequency $f_{\text{max}}(\rho_C)$ vs. contact resistance $\rho_C$, found with a gate resistance $R_g = 1\ \Omega$, and *with the current constrained* to 1.65 mA/$\mu$m for both materials. The following observations can be made and should be contrasted with the results from Fig. 3.7, which showed the *peak* $f_{\text{max}}(\rho_C)$ (over all bias conditions).

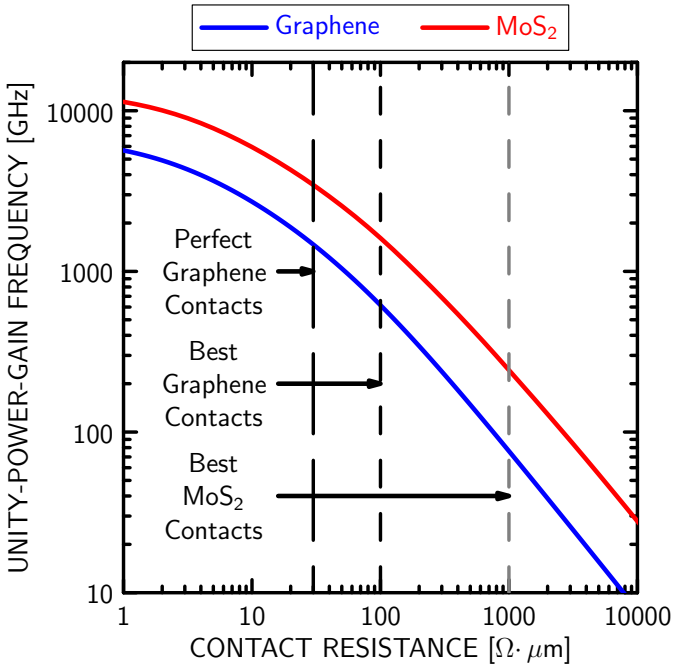



Figure 3.10: Unity-power-gain frequency $f_{\max}(\rho_C)$ vs. the contact resistance $\rho_C$ determining the source and drain contact resistances $R_s$ and $R_d$, with $R_g$ held at $1\,\Omega$, and with the bias current constrained to 1.65 mA/$\mu$m.

### Comparison with Present-Day Contact Resistance

For graphene, at the present-day contact resistance of $\rho_C = 100\,\Omega \cdot \mu\text{m}$, the $f_{\max}(\rho_C)$ is reduced from a peak value of 1.1 THz in Fig. 3.7 to a current-constrained value of 600 GHz in Fig. 3.10. On the other hand, for SL $MoS_2$, at the present-day contact resistance of $\rho_C = 1\,\text{k}\Omega\cdot\mu\text{m}$, the value of 240 GHz from Fig. 3.7 remains nearly unaffected, reappearing in Fig. 3.10. As with the $f_T(\rho_C)$, a contact resistance of 375 $\Omega \cdot \mu\text{m}$ in SL $MoS_2$ should be sufficient to match the 600-GHz value of $f_{\max}(\rho_C)$ possible in graphene.

### THz Operation

With layout optimization to achieve minimum gate resistance, consistent with our assumption that $R_g = 1\,\Omega$, both materials should be able to achieve an $f_{\max}(\rho_C)$ of 1 THz under a constrained bias current, although neither can do so using currently achieved monolayer

contact resistances. In graphene, $\rho_C$ must be reduced to 50 $\Omega \cdot \mu$m (approaching perfect graphene contacts), and in SL $MoS_2$, $\rho_C$ must be reduced to 170 $\Omega \cdot \mu$m (achieved so far only in ML $MoS_2$).

**Outlook with Perfect Contacts**

For graphene devices with perfect contacts ($\rho_C = 30\,\Omega \cdot \mu$m), a drop is observed from the peak $f_{\max}(\rho_C) = 3$ THz in Fig. 3.7 to the current-constrained value of $f_{\max}(\rho_C) = 1.5$ THz in Fig. 3.10. Section 3.5 concluded that the peak value of 3 THz would be impossible to reach using SL $MoS_2$ due to the small contact resistance required; however, the current-constrained $f_{\max}(\rho_C)$ of 1.5 THz in graphene could be reached by achieving $\rho_C = 110\,\Omega \cdot \mu$m in SL $MoS_2$, which has already been done with multi-layer structures.

### 3.6.4 Outcome

The most important outcome from Figs. 3.8 and 3.10 and the detailed discussion above is that $MoS_2$ becomes far more competitive under the condition of equal-current biasing. While graphene still retains its edge if the performance is compared using present-day contact resistances, the gap is substantially reduced, owing largely to the reduction in $g_m$ that occurs in graphene once the current is constrained; SL $MoS_2$ can meet or exceed graphene's current-constrained benchmarks with contact resistances that have already been realized in multi-layer structures, including the possibility of operation at THz frequencies. We have illustrated this outcome using the technologically relevant current value of 1.65 mA/$\mu$m [3].

## 3.7 Comparison with Experiment

While in general there have been many experimental studies of graphene and $MoS_2$ devices, the literature available with measured $f_T$ and $f_{\max}$ is limited. For the purposes of

comparison to experiment, we restrict our attention to the $f_T$, where sufficient experimental data is available to establish trends, and since $f_T$ is far less sensitive to device layout in comparison to $f_{\text{max}}$.

The current experiments on graphene and $MoS_2$ do not show the high values of $f_T$ we discussed in Section 3.4 for a device consistent with the 7-nm node, simply because the size of experimental structures has yet to shrink to the size of leading Si technology. Fig. 3.11 shows a summary of available experimental results of peak $f_T$ vs. $L_G$ for $MoS_2$ and graphene devices; for the purpose of the present comparison, where only trends are of interest, we need not distinguish between experimental values found from single- vs. multi-layer structures. We have superimposed our own single-layer simulation results on this graph.

Consider first the results for graphene. Since the majority of the graphene experimental $f_T$ values have been achieved with a contact resistance on the order of 100 to 200 $\Omega \cdot \mu\text{m}$ [83, 79, 82], we have added our simulated graphene $f_T$ for a 7-nm node device, having a gate length of 12.7 nm, with an assumed contact resistance of 100 $\Omega \cdot \mu\text{m}$. Our simulation result shows good agreement with the trend line found from a linear regression against the graphene data, lending support to our approach and conclusions for graphene.

There is far less data available on the $f_T$ for $MoS_2$, making it difficult to reliably extract a scaling trend. A starting point is a study [70] that included an examination of $f_T$ vs. gate length; this work, in which $\rho_C = 2.5\ \text{k}\Omega \cdot \mu\text{m}$, showed a strong $1/L_G$ scaling behavior for $MoS_2$ devices. The $1/L_G$ scaling behavior can be combined with the best experimental $f_T$ values at a number of gate lengths, extracted from [70, 69, 71], to draw a trend line for $MoS_2$ in Fig. 3.11. The line is anchored at a point specified by an average of the experimental data, and it provides an idea of where the $f_T$ values for $MoS_2$ devices should lie at shorter gate lengths, provided $\rho_C \sim 2.5\ \text{k}\Omega \cdot \mu\text{m}$, the value used in all but one of the experiments; in that one experiment, $\rho_C$ is slightly higher at $3.1\ \text{k}\Omega \cdot \mu\text{m}$, a detail that can be overlooked for

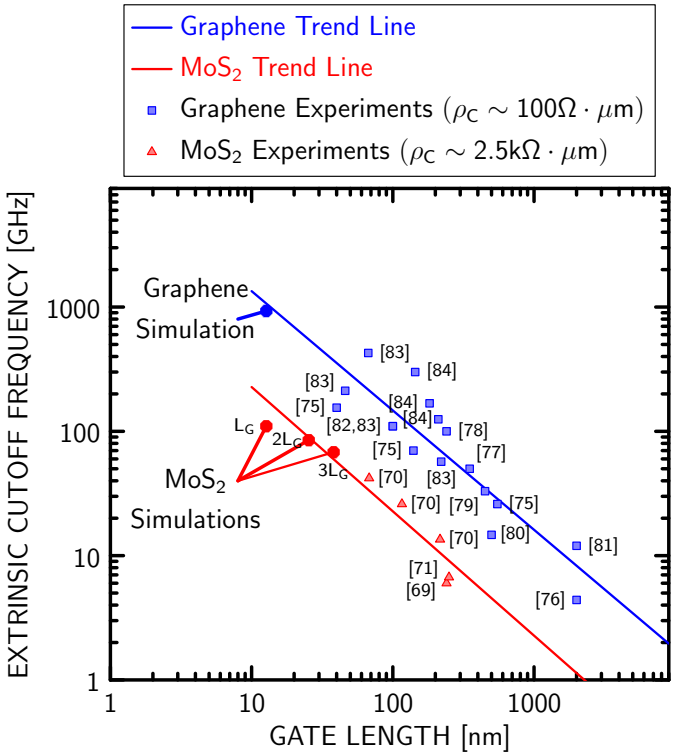



Figure 3.11: Experimental data for peak $f_T$ vs. gate length $L_G$ for $MoS_2$ and graphene devices, with our simulation results superimposed. Experimental data for graphene is from [75, 76, 77, 78, 79, 80, 81, 82, 83, 84], and experimental data for $MoS_2$ is from [70, 69, 71]. The trend line for graphene applies for a contact resistance $\rho_C \sim 100\ \Omega \cdot \mu$m and that for $MoS_2$ applies for $\rho_C \sim 2.5$ k$\Omega \cdot \mu$m, as discussed in the text.

the purpose of our comparison. We have additionally superimposed our simulation data for the $f_T$ of $MoS_2$ devices at shorter gate lengths; in doing so, we chose $\rho_C = 2.5$ k$\Omega \cdot \mu$m to be consistent with the experiments, and in addition to showing the result for $L_G$=12.7 nm, applicable to the 7-nm ITRS node, we have added simulation data for the peak $f_T$ at twice and three times this gate length. The simulation results are consistent with the experimental trend line, lending support to our approach and conclusions for $MoS_2$.

## 3.8 Conclusions

The following conclusions can be drawn from this comparison of the RF potential of graphene and SL $MoS_2$ transistors, using a device structure corresponding to the 7-nm technology node [3], with a focus on the impacts of the transconductance $g_m$ and contact resistance $\rho_C$ in determining the $f_T$ and $f_{\text{max}}$.

1. For equal bias voltages, graphene will always exhibit a higher $g_m$, which leads to a higher value of intrinsic $f_{\text{T,int}}$. For equal bias currents, the trend reverses, and SL $MoS_2$ gains the edge in $g_m$.

2. In terms of peak performance (over all bias conditions), SL $MoS_2$ lags graphene due to the relatively poor quality of SL $MoS_2$ contacts; for example, with current contact technology ($\rho_C = 100\ \Omega \cdot \mu\text{m}$ in graphene and $\rho_C = 1\ \text{k}\Omega \cdot \mu\text{m}$ in SL $MoS_2$), we observe $f_T = 930$ GHz and $f_{\text{max}} = 1.1$ THz in graphene, but only $f_T = 230$ GHz and $f_{\text{max}} = 260$ GHz in SL $MoS_2$. Considerable improvement in SL $MoS_2$ contacts is required for SL $MoS_2$ to bridge the gap, as we detailed in Sections 3.4 and 3.5.

3. In terms of the performance under the constraint of equal bias currents, set to the technologically relevant value of 1.65 mA/$\mu$m dictated by the ITRS [3], SL $MoS_2$ looks far more competitive, and SL $MoS_2$ can meet or exceed graphene's benchmarks by achieving contact resistances exhibited in experimental ML $MoS_2$ structures, as detailed in Section 3.6. SL $MoS_2$ gains ground on graphene when the current is constrained because its $g_m$ remains less sensitive to bias conditions, whereas graphene requires large currents to sustain a large $g_m$.

4. The results are consistent with the trends established by experimental data for present-day devices, supporting the approach and conclusions.

Overall, our work shows that the peak performance edge will likely remain with graphene, due to lagging contact technology with SL $MoS_2$, but that SL $MoS_2$ can meet or exceed graphene in any application that constrains the bias current, provided only that SL $MoS_2$ can achieve contact resistances already realized in multi-layer structures. This result makes SL $MoS_2$ a highly attractive alternative to graphene for any application where the bias current is constrained (*e.g.*, to minimize power consumption), especially given that SL $MoS_2$ can also be used for digital logic, whereas graphene cannot.

# Chapter 4

# Conclusions and Future Work

## 4.1 Summary of Contributions

In this section, we summarize the main contributions from each stage of the work. The work leading to the conclusions listed here is detailed in the previous chapters.

### 4.1.1 Stage I (Chapter 2)

The specific contributions from the first stage, "RF Performance Limits and Operating Physics Arising from the Lack of a Bandgap in Graphene Transistors," which has been completed, are as follows:

1. Based on ballistic quantum-mechanical transport in the intrinsic device, the lack of a bandgap causes optimum RF performance to be realized under the bias condition where the drain Fermi level $\mu_2$ aligns with the channel potential $E_{\text{ch}}$, as specified by (2.11) in Chapter 2.

2. This bias point, which corresponds to $v_G \sim 0.75$ V (where $v_D \equiv V_{\text{DD}}/2 = 0.5$ V) for the chosen device (Fig. 2.1), yields an optimum transconductance $g_m$ while keeping the gate-drain capacitance $C_{\text{gd}}$ and hence the input capacitance $C_{\text{gg}}$ from increasing due to "ohmic" operation, thus yielding an optimum intrinsic $f_T = g_m/(2\pi C_{\text{gg}})$ [Figs. 2.4 and 2.3(b)].

3. The same bias point leads to an optimum value for the intrinsic output conductance $g_o$, which can be viewed as being comprised of two parts: a quantum component $g_{\text{oq}}$ and a conventional DIBL component $g_{\text{ob}}$. The relevant equations revealing the associated physics are (2.14), (2.17), and (2.19), and the relevant figure illustrating the behavior of $g_o$ is Fig. 2.9.

4. The relatively poor output conductance limits the extrinsic $f_T$ and $f_{\text{max}}$, a feature which is unique to graphene transistors. With the aid of (2.20) and (2.21), our fully quantum-mechanical simulations suggest the peak $f_T$ could be increased by 300 GHz and the peak $f_{\text{max}}$ could be doubled (Figs. 2.10 and 2.11) if a bandgap could be introduced to cause $g_o \rightarrow 0$ while leaving all other parameters unchanged.

Collectively, the most important outcome of the work is a deeper understanding of the mechanism which causes the large output conductance in graphene; severe DIBL and direct tunneling contribute equally. The effect of the output conductance lowers the potential operating speed of graphene devices, especially evidenced by the decrease in $f_{\text{max}}$ by a factor of two. A simple model for understanding the physics of nanoscale devices was also developed and utilized.

### 4.1.2 Stage II (Chapter 3)

The specific contributions from the second stage, "Impact of Contact Resistance on the $f_T$ and $f_{\text{max}}$ of Graphene vs. $MoS_2$ Transistors" which has been completed, are as follows:

1. For equal bias voltages, graphene will always exhibit a higher $g_m$, which leads to a higher value of intrinsic unity-current-gain frequency $f_{\text{T,int}}$. For equal bias currents, the trend reverses, and SL $MoS_2$ gains the edge in $g_m$.

2. In terms of peak performance (over all bias conditions), SL $MoS_2$ lags graphene due to the relatively poor quality of SL $MoS_2$ contacts; for example, with current contact

technology ($\rho_C = 100\ \Omega \cdot \mu\text{m}$ in graphene and $\rho_C = 1\ \text{k}\Omega \cdot \mu\text{m}$ in SL $MoS_2$), we observe $f_T = 930$ GHz and $f_{\text{max}} = 1.1$ THz in graphene, but only $f_T = 230$ GHz and $f_{\text{max}} = 260$ GHz in SL $MoS_2$. Considerable improvement in SL $MoS_2$ contacts is required for SL $MoS_2$ to bridge the gap, as we detailed in Sections 3.4 and 3.5.

3. In terms of the performance under the constraint of equal bias currents, set to the technologically relevant value of 1.65 mA/$\mu$m dictated by the ITRS [3], SL $MoS_2$ looks far more competitive, and SL $MoS_2$ can meet or exceed graphene's benchmarks by achieving contact resistances exhibited in experimental ML $MoS_2$ structures, as detailed in Section 3.6. SL $MoS_2$ gains ground on graphene when the current is constrained because its $g_m$ remains less sensitive to bias conditions, whereas graphene requires large currents to sustain a large $g_m$.

4. The results are consistent with the trends established by experimental data for present-day devices, supporting the approach and conclusions.

Collectively, the most important outcome of this work is an assessment of the extent to which the contact resistance and output conductance trade off to limit the RF performance of SL $MoS_2$ and graphene, and to demonstrate that while the poor contact resistance in SL $MoS_2$ results in graphene having superior *peak* performance (over all bias conditions), SL $MoS_2$ could be a superior alternative in low-current applications. The validity of our model was demonstrated by a comparison to experiment.

### 4.1.3 Stage III (Future Work)

The anticipated contribution of the third stage, entitled, "Understanding the RF Scaling Behavior of FinFETs to the End of the Roadmap," has already been outlined in Section 1.3.3. Further details are provided in the following section.

## 4.2 Future Work: Understanding the Behavior of FinFETs to the End of the Roadmap

### 4.2.1 Introduction

In order to improve the overall performance of FETs, the semiconductor industry continues to focus on scaling silicon technology, as described by Moore's Law. However, beyond nodes in the range of 30 nm, scaling planar CMOS technology does not result in the expected increase in performance, as measured through metrics such as speed, power, and cost [154]. Debuting at the 22-nm technology node, FinFETs have addressed concerns of the scalability of silicon, and are now the dominant technology at 14 nm for all major manufacturers [87, 85, 155]. However, future roadblocks exist; for example, Intel's former chief architect, Bob Colwell, has predicted that even with FinFETs, scaling of silicon will not be possible beyond gate lengths of 5-7 nm [156] (corresponding to the 3-nm technology node), and recent announcements have featured silicon germanium (SiGe) as a new channel material for FinFETs at the 10-nm node [89], illustrating that new materials will almost certainly be needed even to keep scaling going until Colwell's forecast limit. Clearly, there are open questions regarding the future of semiconductor technology.

In the first two stages of this work, we investigated the RF performance and device physics of two emerging transistor technologies, graphene and SL $MoS_2$. The methodology and simulation tool, based on the non-equilibrium Green's function (NEGF) approach, can be transferred to other technologies, as evidenced by publications on III-V devices [32] and carbon-nanotubes [33]. Careful attention has been paid to the solver's ability to extract the small-signal equivalent circuit of any device, and it is hence particularly useful for studying the high-frequency characteristics of device structures. It is recommended that future work therefore be focused on applying the tool to other materials and structures of interest to the device research community, starting with FinFETs.

The third stage can be broken into two parts.

First, we have already laid the groundwork and now have a quantum-mechanical simulation tool that is applicable to FinFET device structures. The extended tool (from the first two stages of the Ph.D.) solves the NEGF formalism in three dimensions self-consistently with the Poisson equation in three dimensions for FinFET devices. Options within the solver also exist to solve these equations in two dimensions, an approach that is valid for tall fins, but which can also be used as a first approximation even for short fins to save simulation time. We will soon include the effect of phonon scattering to improve the validity of our modeling approach.

Second, we suggest use of the new solver to study the predicted scaling of the $f_T$ and $f_{\max}$ of FinFETs over the next 10–15 years, down to 5-nm channel lengths, with a particular emphasis on the decreasing importance of phonon scattering that is expected with a reduction of the channel length. This work is in fact already underway, being conducted in conjunction with two of our industrial collaborators, Qualcomm and IBM.

### 4.2.2 Proposed Approach

In this section, we highlight several features of our simulation approach that differ from the two-dimensional materials of the earlier studies.

#### Extended Simulation Structure

Fig. 4.1 shows the basic FinFET structure already simulated. A coupled mode-space (CMS) solution approach [88] is used, by partitioning a device into slices perpendicular to the direction of transport. First, the Schrödinger equation is solved for each slice to obtain a set of wave functions and eigenenergies; the CMS process then combines the slices together to a simplified Hamiltonian consisting of several coupled one-dimensional channels, which can be solved using the NEGF.

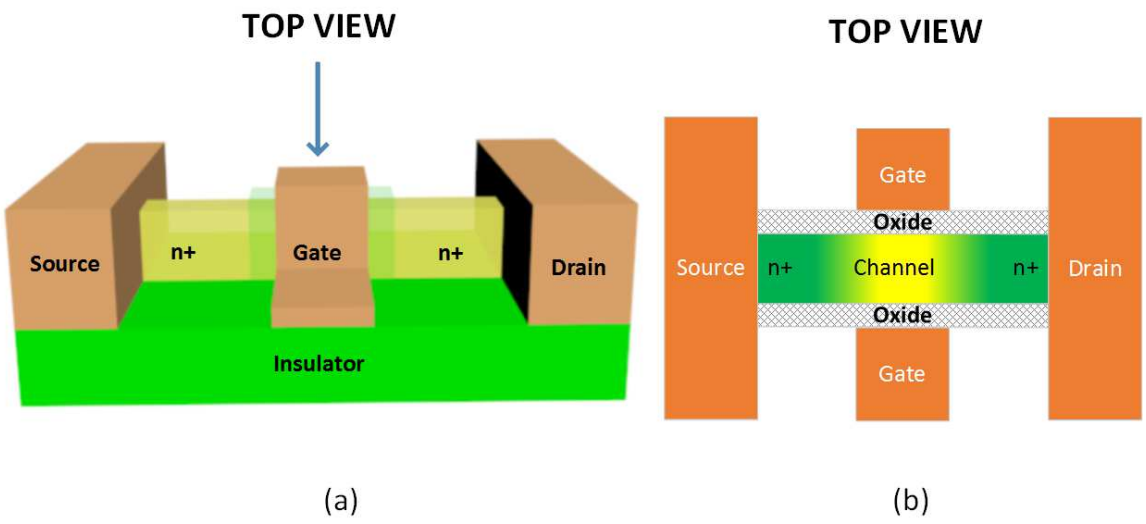



Figure 4.1: The FinFET viewed (a) in three dimensions and (b) from a top view. The simulation domain for the intrinsic device is most easily seen in part (b); it is defined by the oxide, channel, and $n^+$ regions bounded by the orange contact regions.

### Valleys

One vital aspect of studying silicon is the presence of six electronic valleys arising from the more complex crystal structure versus that of two-dimensional materials. The curvature of these valleys changes depending on the direction of electron transport. Transport along the $[100]$ crystal direction will result in three sets of doubly degenerate valleys, while transport along the $[110]$ direction will result in two sets of triply degenerate valleys. All these energy valleys are illustrated schematically in the constant-energy plot of Fig. 4.2.

### Phonon Scattering

Although we have successfully introduced phonon scattering into the simulation of SL $MoS_2$ transistors, more work is needed for FinFETs. It is first necessary to understand the important mechanisms of phonon scattering in Si and SiGe. Once understood, these sources can then be incorporated to finalize the modeling approach for FinFETs.

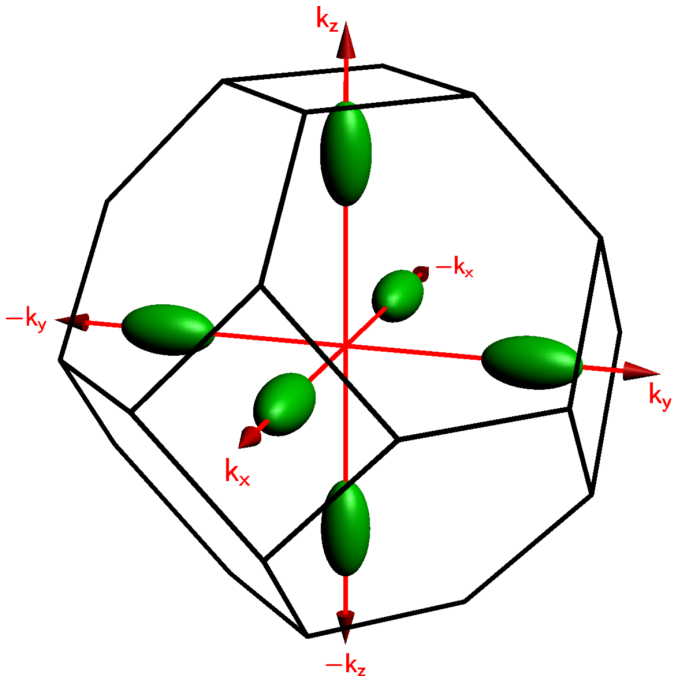



Figure 4.2: The first Brillouin zone of silicon along with the six constant-energy ellipsoids in reciprocal space. Each ellipsoid represents one valley minimum in the electronic structure.

### 4.2.3 Initial Results

#### Charge, Current, and Cutoff Frequency

Figs. 4.3, 4.4, and 4.5 show initial results, illustrating the viability of the approach. For example, Figs. 4.3 and 4.4 illustrate the charge distributions in 22-nm and 5-nm devices, respectively, looking down from above the gate, *i.e.*, from a "top view," as marked in Fig. 4.1(a); in each case, the distributions *without* [part (a)] and *with* [part (b)] appreciable gate voltage are shown. A close examination of the plots reveals that the distribution of the charge varies between the structures once an appreciable gate voltage is present. Fig. 4.5 shows current-voltage characteristics for a 22-nm device, and it illustrates that the characteristics can be different for differently oriented channels.

Fig. 4.6 shows a plot of the peak $f_{T,int}$ vs. technology node, based on specifications from the ITRS [3]. The values for $f_{T,int}$ are high, but the inclusion of scattering, parasitics, and

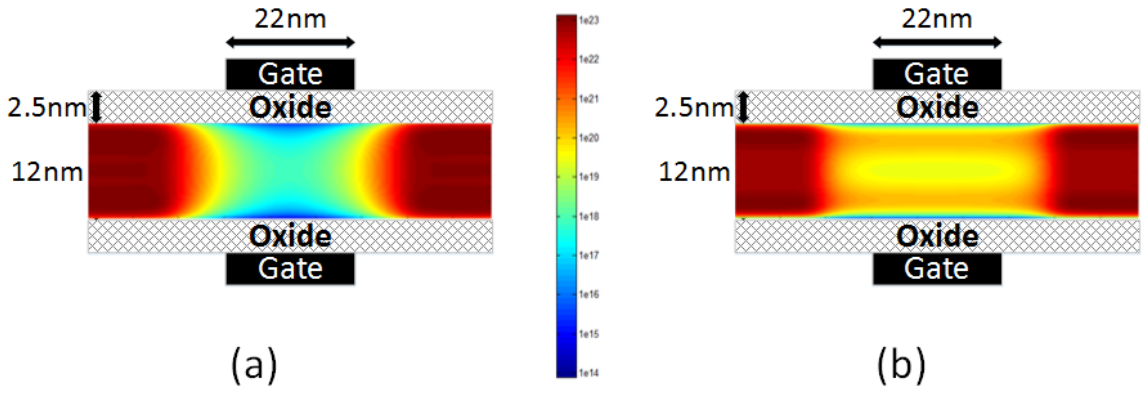



Figure 4.3: Charge distribution in a 22-nm FinFET (a) without and (b) with an appreciable gate voltage. When an appreciable gate voltage is present, the charge density exhibits two peaks, located above and below the center of the channel.

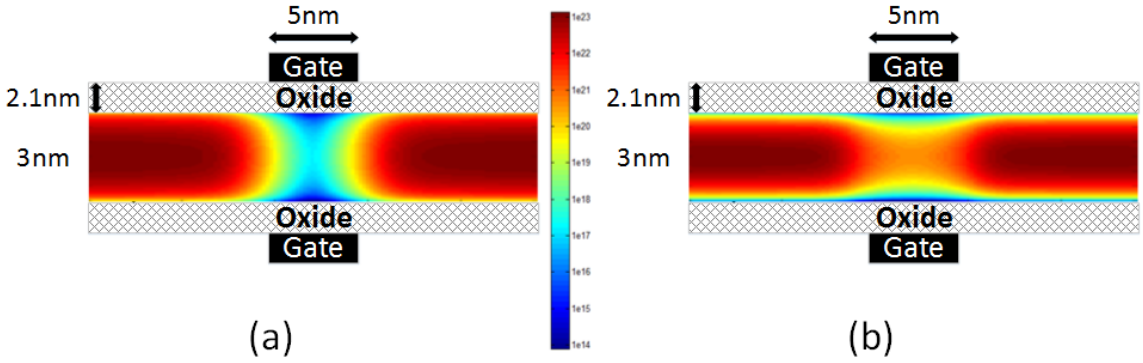



Figure 4.4: Charge distribution in a 5-nm FinFET (a) without and (b) with an appreciable gate voltage. When an appreciable gate voltage is present, the charge density exhibits a single peak, located at the center of the channel.

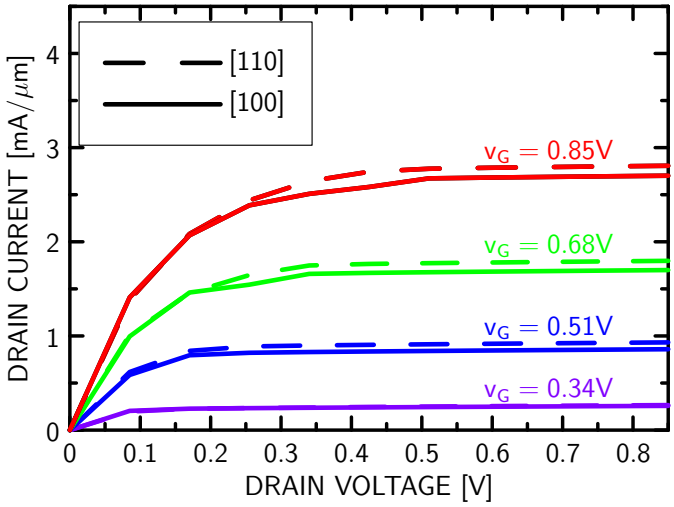



Figure 4.5: Current-voltage characteristics for a 22-nm FinFET along the $[110]$ and $[100]$ crystal directions.

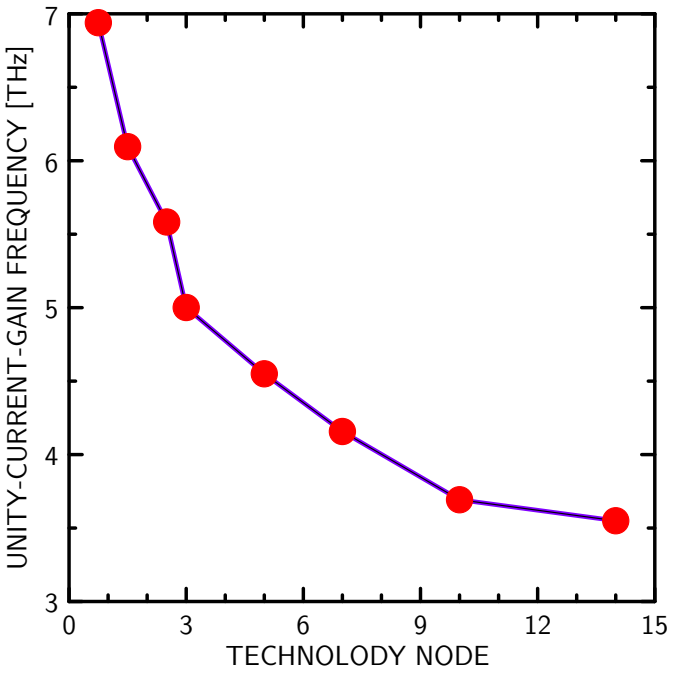



Figure 4.6: Intrinsic unity-current-gain frequency $f_{T,int}$ vs. technology node. Nodes are identified by their ITRS [3] name in nm, *not* by gate length.

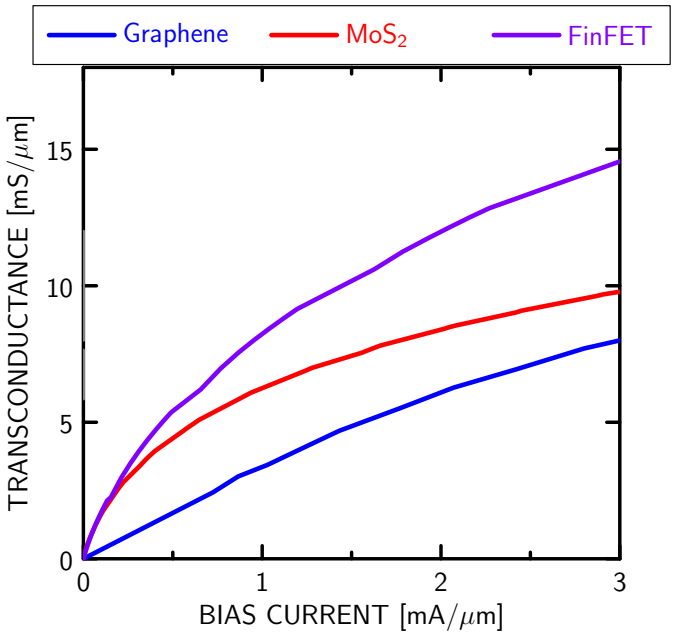



Figure 4.7: Transconductance $g_m$ vs. drain bias current $I_D$ for graphene, SL $MoS_2$, and FinFET transistors. The drain and gate voltages were adjusted to provide the largest possible value of $g_m$ at each value of $I_D$.

calibration to realistic structures will reduce the value from those shown. Further work will also be done to understand the role that quantum confinement within the fin structure has on the scaling behavior.

### Comparison with Graphene and SL $MoS_2$

We have simulated FinFETs from the 7-nm technology node, corresponding to a gate length of 12.7 nm, similar to what we did for graphene and SL $MoS_2$ in Chapter 3. Fig. 4.7 shows the plot of $g_m$ vs. drain current $I_D$ in the spirit of Fig. 3.9, but including FinFETs. Initial results indicate that the $g_m$ of silicon FinFET technology is superior to the two-dimensional materials under the condition of equal bias currents; further work will clarify if such advantages arise due to the silicon bandstructure or due to the physical structure of the FinFET.

### 4.2.4 Work in Progress

Work continues toward the goal of an accurate, predictive model for FinFET technology. Further enhancements, including surface roughness, Coulomb scattering, phonon scattering, and the effects of other channel materials are all underway, as already discussed. Furthermore, we will conduct measurements from actual FinFETs (supplied by IBM) to calibrate our solution to experiment, as we have done with graphene and SL $MoS_2$. After completion of the calibration, we will be able to accurately predict the scaling behavior of FinFETs down to gate lengths of 5 nm.

### 4.2.5 Summary

The new tool for FinFETs is a natural extension of the completed work in stages I and II of this Ph.D. research, and it is already in place and leading to useful collaborations with world-leading firms in electronics, such as our partners at IBM and Qualcomm.

This new tool thus concludes this Ph.D. thesis research, focused on the quantum-mechanical assessment of new materials and device structures for ongoing and future electronics.

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[18] *Table PIDS3a Low Power (LP) Technology Requirements - TCAD* in the process integration, devices, and structures (PIDS) of the International Technology Roadmap for Semiconductors 2013 Edition. [Online]. Available: http://www.itrs.net/Links/2013ITRS/2013Tables/PIDS_2013Tables.xlsx

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# Appendix A

## A.1 Derivation of the Expression for Transconductance

The transconductance is defined as

$$g_m = \frac{\partial i_D}{\partial v_G} \tag{A.1}$$

where the derivative is to be evaluated with the source and drain voltages ($v_S$ and $v_D$) held constant.

To find an expression for the derivative, we first refer to the circuit of Fig. A.11, which can be derived from a general theory of ballistic nanotransistors [157, 158]. The circuit allows a computation of the channel potential $E_{\text{ch}}$ (expressed in the units of electron energy) in terms of the external voltages and physics-based capacitances in the device, where for graphene devices, as mentioned in Section III, the channel potential can be taken to be the position of the Dirac point at the midpoint of the channel. The capacitances in the circuit are the gate electrostatic (oxide) capacitance ($C_{\text{ox}}$), the drain electrostatic and quantum capacitances ($C_{\text{de}}$ and $C_{\text{dq}}$), and the source electrostatic and quantum capacitances ($C_{\text{se}}$ and $C_{\text{sq}}$).

From the circuit of Fig. A.11, we can write the incremental channel potential $\partial E_{\text{ch}}$ that arises from an incremental gate voltage $\partial v_G$ (with $\partial v_S = \partial v_D = 0$), as follows:

$$\partial E_{\text{ch}} = -q\partial v_G \frac{C_{\text{ox}}}{C_T} \tag{A.2}$$

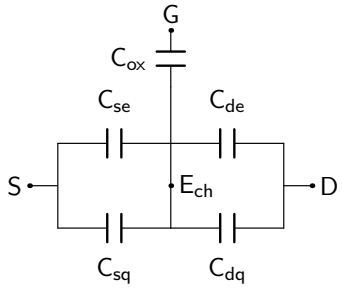


Figure A.11: Equivalent circuit between the external terminals and the channel as derived from a general theory of ballistic nanotransistors [157], [158].

where $C_T = C_{\text{de}} + C_{\text{dq}} + C_{\text{se}} + C_{\text{sq}} + C_{\text{ox}}$ is the algebraic sum of all the capacitances in Fig. A.11 and facilitates a convenient shorthand when expressing the result of the voltage division.

From the NEGF (or Landauer) formalism, the current is [114, p. 321]

$$i_D = \frac{2q}{h} \int_{-\infty}^{\infty} T(E) \left[ f_1(E) - f_2(E) \right] dE. \tag{A.3}$$

Equation (A.3) can be differentiated with respect to the channel potential while holding the source and drain voltages constant; this means that the Fermi functions [specified by (2.7)] will be unaffected by the differentiation, which will therefore impact only the transmission function. Performing the operation, we find

$$\frac{\partial i_D}{\partial E_{\text{ch}}} = \frac{2q}{h} \int_{-\infty}^{\infty} \frac{\partial T(E)}{\partial E_{\text{ch}}} \left[ f_1(E) - f_2(E) \right] dE \tag{A.4}$$

which combined with (A.2) then yields

$$\frac{\partial i_D}{\partial v_G} = -\frac{2q^2}{h} \frac{C_{\text{ox}}}{C_T} \int_{-\infty}^{\infty} \frac{\partial T(E)}{\partial E_{\text{ch}}} \left[ f_1(E) - f_2(E) \right] dE. \tag{A.5}$$

As a first approximation, the *shape* of the transmission function remains fixed under a perturbation, such that an incremental change $\partial E_{\text{ch}}$ in the channel potential simply *shifts* the function: $T(E) \to T(E - \partial E_{\text{ch}})$. The change in the transmission $\partial T(E)$ at an energy $E$ from the shift can then be written as a difference equation:

$$\partial T(E) = T(E - \partial E_{\text{ch}}) - T(E) \tag{A.6}$$

from which

$$\partial T(E) = \frac{\partial T(E)}{\partial E}(-\partial E_{\text{ch}}) \tag{A.7}$$

or

$$\frac{\partial T(E)}{\partial E_{\text{ch}}} = -\frac{\partial T(E)}{\partial E}. \tag{A.8}$$

Substituting the relationship (A.8) into (A.5) then gives

$$g_m = \frac{2q^2}{h}\frac{C_{\text{ox}}}{C_T}\int_{-\infty}^{\infty}\frac{\partial T(E)}{\partial E}\left[f_1\left(E\right) - f_2\left(E\right)\right]\, dE \tag{A.9}$$

which can be recast into the final form (2.1) by recognizing that the circuit of Fig. A.11 implies

$$\frac{C_{\text{ox}}}{C_T} = \left(1 - \frac{C_{\text{gg}}}{C_{\text{ox}}}\right) \tag{A.10}$$

and that $G_0 \equiv 2q^2/h$.