Processing and Switching Mechanisms of Materials for Memory Devices in Flexible Electronics

By

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Abstract

Current trends in Big Data are driving industries towards new innovations for data acquisition and processing. Among these trends is the concept of the *Internet of Things* (typically abbreviated as IOT), which will result in the collection of very large amounts of data from sensors and microelectronic devices integrated in household appliances, wearable electronics for health, vehicles, and manufacturing facilities, among others. Many of these devices and sensors will need to be interfaced directly with living, natural, and other non-rigid surfaces, thus, an enormous field has emerged that falls under the umbrella term of flexible hybrid electronics (FHE). Global standards for FHE currently are being developed and are propelling research support and advances in new materials. The focus of this dissertation will be to investigate the processing of materials used for memory and the mechanism of operation of these materials, which then can be integrated onto flexible substrates.

In the second chapter, metal-assisted chemical etching of Si substrates is used to fabricate freestanding Si pillars via different patterning techniques to create devices with different architectures. Then, a specialty ferroelectric polymer, poly(vinylidenefluoride-co-trifluoroethylene) P(VDF-TrFE), will be interfaced with the silicon structures to explore resistive switching that is driven by polarization of the polymer.

The third chapter demonstrates how to process the commodity polymer, PVDF, which is 10 times less expensive than P(VDF-TrFE), as an alternative to achieving robust memory properties. However, transforming PVDF into ferroelectric phases has proven to be challenging in a manner that is amenable to large-scale commercial applications. Here, it is shown that PVDF can be transformed from the α-phase into the desired ferroelectric β-phase using microsecond pulses of UV irradiation. Under optimal pulse durations, typical characteristics of dipolar and reversible hysteresis loops appear in ferroelectric PVDF, reaching a remnant polarization of 5.4 $\mu C/cm^2$ and a coercive field around 120 MV/m. Potentially, this single-step method can open a wide range of opportunities for high-throughput roll-to-roll annealing of plastic electronics.

Flexible electronic devices assembled upon a platform of liquid gallium and related alloys are of interest due to their mouldability, negligible toxicity, and high conductivity of these materials. In Chapter 4, the eutectic Ga-In alloy (EGaIn) and its surface oxide, gallium oxide, are utilized as electrode and electrolyte materials, respectively. The native oxide is positioned between bulk gallium and degenerately doped p-type silicon to form junctions that show memristive behavior. When cycled between –2.5 and 2.5 V, an abrupt insulator–metal transition is observed that is reversible when the polarity is reversed. The ON/OFF ratio between the high and low resistive states in these junctions can reach values on the order of 10^8, retain the ON and OFF resistive states for up to 10^5 s, and with an endurance exceeding 100 cycles. A nanoscale interface of gallium oxide is the critical feature intrinsic to these devices, through which reversible formation and rupture of Ga filaments occur via electrochemical metallization.

In the last chapter, Chapter 5, follow-up directions of research are provided that are backed with preliminary data. This includes the design of new device architectures for hybrid ferroelectric diodes, light processing of PVDF on plastic substrates, the role of electrodes and the thickness of gallium oxide on resistive switching, and in-situ XPS analysis of resistive switching across gallium oxide/p-type Si interfaces.

Preface

Chapter 1 summarizes the overall picture on the future of memory devices in electronics beyond the trends of miniaturization that is projected in Moore's Law. Diversification of devices towards the area of flexible hybrid electronics will be described. Two material systems are explored, organic polymer PVDF and liquid metal gallium-indium eutectic (EGaIn). Challenges in processing ferroelectric PVDF are described and includes a summary on the recent progress in the field. The mechanisms of resistive switching across oxide-based electrolytes are then discussed and includes prospects of utilizing native oxides in liquid metals towards printable memory cells.

Chapter 2 explores resistive switching across the interface of organic ferroelectric polymers and nanostructured Si. Various device architectures were realized using metal-assisted chemical etching (MACE) and metal dewetting. Control experiments were conducted with the experimental support of Dr. Erik J. Luber (metal dewetting), Brian C. Olsen (MACE process optimization), and Dr. Sayed Youssef Sayed (surface treatment). I also acknowledge the critical and valuable advice provided by Prof. Kamal Asadi on the analysis of these hybrid devices.

In Chapter 3, high through-put processing of low cost and commodity polymer PVDF is explored using high intensity microsecond pulses of white light to realize large area and high through-put manufacturing of the ferroelectric polymer. This project was conducted in collaboration with Prof. Husam Alshareef and Dr. Ji Hoon Park (King Abdullah University of Science and Technology–KAUST) and Dr. Mohd. Adnan Khan, Dr. Ihab Odeh, and Karam Rajab from Saudi Basic Industries (SABIC). Ihab Odeh contributed to the idea of PVDF annealing and Mohd. Adnan Khan, Karam Rajab, and I conducted the experiments. The manuscript was written by myself, and Prof. Jillian M. Buriak contributed to the final manuscript.

In Chapter 4, printable conductive inks comprised of alloys of Ga and their surface oxides were explored as working electrodes and electrolytes, respectively, for redox-based memory devices. This work was conducted in collaboration with Prof.

Marc Tornow and Dr. Maximilian Speckbacher (Technical University of Munich–TUM). Aaron Hryciw and his team from the NanoFab (University of Alberta) helped with the fabrication and characterization of thermally grown SiO_2 films on Si wafers. I designed and performed all other experiments, except for C-AFM, which was conducted by Maximilian Speckbacher. Data analysis was a joint effort by Prof. Jillian M. Buriak, Prof. Marc Tornow, Dr. Maximilian Speckbacher, Dr. Erik J. Luber, Brian Olsen, Dr. Sayed Youssef Sayed, and me. The first draft of the manuscript was written by me and the final version was written with contributions from all coauthors.

In the final Chapter, I will expand on the knowledge gained from Chapters 1–4 to explore new device concepts for memory applications briefly. The idea was done in collaboration with Dr. Maximilian Speckbacher and Dr. Simon Pfaehler from TUM. Approaches to other characterization techniques are suggested to explore the switching mechanisms at the interfaces further.

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Finally, a special thank you goes to my entire family for their love and encouragement and to my one and only wife and mother of my three dear children, Mrs. Oula Almadhoun, for her support and patience throughout this academic journey.

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List of Abbreviations

AFM	Atomic Force Microscopy
ATR-FTIR	Attenuated Total Reflectance – Fourier Transform Infrared
BF	Brightfield
BOE	Buffered oxide etchant
C-AFM	Conductive Atomic Force Microscopy
CBRAM	Conductive Bridge Random Access Memory
C-f	Capacitance-frequency
CMOS	Complementary metal–oxide–semiconductor
C-V	Capacitance-voltage
DCM	Dichloromethane
DI	Deionized
DRAM	Dynamic Random Access Memory
ECM	Electrochemical Metallization
EGaIn	Gallium-indium Eutectic
F8BT	Poly(9,9-dioctylfluorene-alt-benzothiadiazole)
FHE	Flexible Hybrid Electronics
FinFET	Fin Field-Effect Transistor
FTIR	Fourier Transform Infrared Spectrometry
FTJ	Ferroelectric Tunnel Junctions
Galinstan	Gallium-indium-tin eutectic
HRS	High resistive state
IC	Integrated circuit
I_{CC}	Compliance current
IoT	Internet of things
ITO	Indium-tin oxide
ITRS	International Technology Roadmap for Semiconductors
I-V	Current-voltage
J-V	Current density-voltage
LRS	Low resistive state
MACE	Metal-assisted Chemical Etching
MEK	Methyl Ethyl Ketone
MEMS	Microelectromechanical systems
MIM	Metal-insulator-metal
MO	Metal oxide
MOS	Metal-oxide-semiconductor
NP	Nanoparticles
OxRAM	Oxide-based Random Access Memory
P(VDF-TrFE)	Poly(vinylidenefluoride-co-trifluoroethylene)
P3HT	Poly(3-hexylthiophene)
PCBM	[6,6]-phenyl-C_{61}-butyric acid methyl ester
PDMS	Polydimethylsiloxane
PEDOT:PSS	Poly (3,4-ethylenedioxythiophene) polystyrene sulfonate
PEI	Polyetherimide

PEN	Polyethylene naphthalate
PET	Polyethylene terephthalate
PFO	Polydioctylfluorene
ppb	Parts per billion
PVDF	Polyvinylidene difluoride
RAM	Random Access Memory
ReRAM	Resistive Random Access Memory
RF	Radio frequency
RFID	Radio-frequency identification
RMS	Root mean square
ROM	Read-only Memory
RT	Room temperature
SCLC	Space-charge Limited Current
SEM	Scanning Electron Microscopy
SIMS	Secondary Ion Mass Spectrometry
SiNW	Silicon Nanowires
SOI	Silicon on Insulator
SRAM	Static Random-Access Memory
STM	Scanning Tunneling Microscopy
TEM	Transmission Electron Microscopy
Tm	Melting temperature
ToF-SIMS	Time-of-flight Secondary Ion Mass Spectrometry
TUNA	Tunneling Atomic Force Microscopy
UV	Ultraviolet
UV-Vis	Ultraviolet-visible Spectroscopy
VCM	Valence Change Memory
XPS	X-ray Photoelectron Spectroscopy
XRD	X-ray Diffractions

CHAPTER 1: Background

1.1 Introduction

Continuous advancement in the electronics industry has made it possible to create and manufacture more efficient and powerful computer hardware. This is primarily due to the development of complementary metal oxide semiconductor (CMOS) technologies, where advancements in processing techniques allow for the miniaturization of integrated transistors with improved performance and reduced physical volume of electronic chips.[1] Historically, digital computing was demonstrated first in the early 1940s using radio vacuum tubes and mercury glass tubes, which evolved to magnetic-core memory a decade later. Since the 1960s and up until today, the CMOS technology continues to dominate the industry in terms of achieving reliable, low power, and high-speed computation.[2] Today, the main driver for research in CMOS-based electronics is to shrink the size of current transistors to enhance storage density in smaller spaces.[3]

According to Moore's Law, proposed by Gordon Moore in 1965, the number of MOS transistors integrated onto a chip should double every two years.[4,5] Moore's law still holds today but the trajectory for further miniaturization in the future will be constrained by the limited physical properties of metal oxide semiconducting materials. The International Technology Roadmap of Semiconductors (ITRS) addressed the future challenges concerning material scalability and forecast a slow down of Moore's Law. To counter this slow down and ensure a sustained growth in the electronics industry, three strategies have been proposed, as illustrated in **Figure 1.1**:[1]

1. More than Moore (Miniaturization): Increase device integration through continuous shrinking of transistor dimensions. One example is the current advancements in fin field-effect transistor (FinFET) devices. However, and according to Dennard's scaling law,[6,7] quantum effects across oxides that are a few atoms thick is expected to become a hurdle for future development.

2. Beyond CMOS: Using non-conventional materials and technologies for next-generation memory and computing such as the memristor. Other examples include quantum, photonic, and neuromorphic computing.
3. More than Moore (Diversification): Integrating and interfacing various electronic elements that can perform tasks with minimal analog to digital conversion. Examples include sensors for radio-frequency identification (RFID) and micro-electromechanical systems (MEMS). Designing applications for the *Internet of Things*, with a projected market exceeding US$ 10 trillion by 2030, using hybrid and stretchable printed electronics.

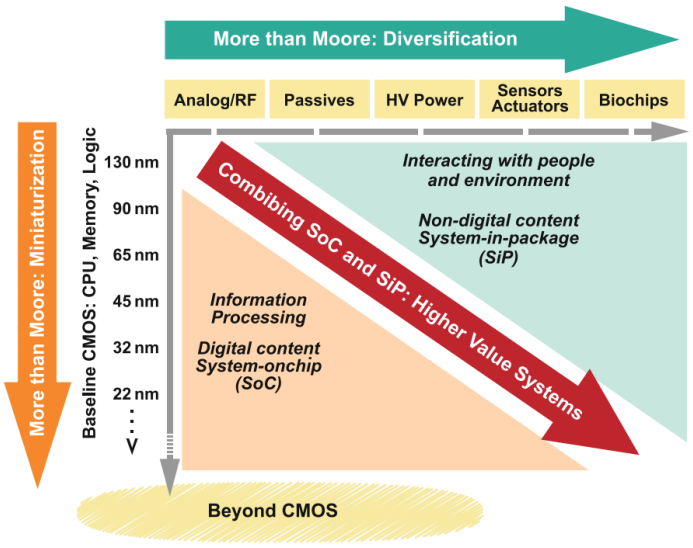

Figure 1.1. Illustration of technology trends (miniaturization, diversification, and beyond Moore) aimed at addressing the slowdown of Moore's law. Reprinted with permission from [1]. Copyright © Springer Science+Business Media, LLC 2011.

1.2 Core Components in Flexible Electronics

The fabrication of functional electronic devices, sensors, and circuits on flexible substrates has gained a lot of traction over the past decade, promising a broad range of applications, where flexibility, scalability, and low cost is important. Although there has been significant progress in the field of flexible and printed electronics, the development of rigid silicon-based integrated circuits over the past 60 years makes them far more efficient, in terms of low power computation and signal processing.

Nonetheless, hybrid electronic systems that can utilize the desired properties of high mechanical flexibility as well as high computational performance are being considered for next-generation electronics.[8] Of great interest is a broad range of applications across healthcare and industry that require interfacing of devices directly onto natural surfaces that are soft, flexible, and rough, such as human skin.[9–12]

A visual example on how multiple electronic components can be integrated onto a flexible substrate is shown in **Figure 1.2**.

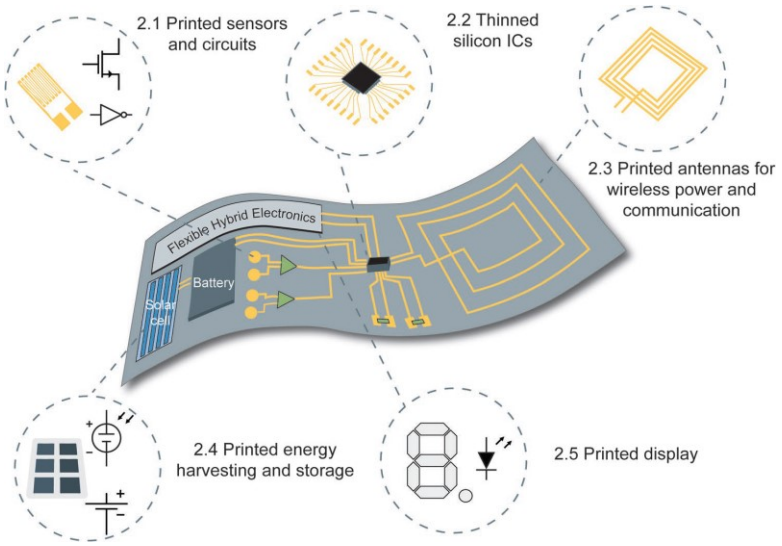

Figure 1.2. Examples of integrating major electronic components directly onto flexible substrates. All components, such as sensors, display, energy harvesting materials, energy storage materials, circuitry, and integrated circuits (IC) are fully printed directly onto a flexible substrate. Reprinted with permission from [8]. Copyright © 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

Flexible components can range from sensors and circuits, energy storage and harvesting devices, antennas, and display.[13] **Figure 1.3** shows a range of conducting, semiconducting, and insulating materials, and their corresponding processing techniques that can be used in such flexible systems. The type of materials is selected depending on the role and function of these devices.

The focus will be on materials used in memory devices, which are typically dielectric materials sandwiched between conducting contacts. Materials that can be processed from solution which are investigated in this thesis are:

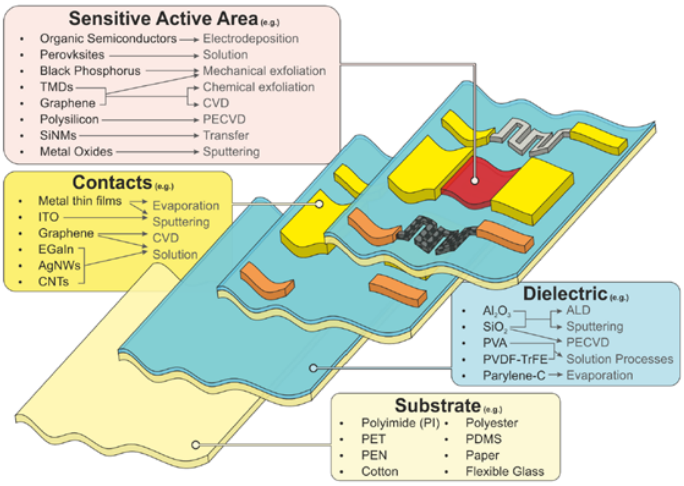

Figure 1.3. Overview of materials and their corresponding processing techniques used in flexible sensors. Reprinted with permission from [13]. Published by MDPI.

1. Polymeric PVDF as a high-k electroactive dielectric: Memory devices using organic materials already have been demonstrated on a market scale. However, high throughput solution processing using low cost PVDF remains a challenge and will be discussed in further details in Chapter 3.
2. Liquid metal EGaIn: The role of a thin metal oxide dielectric on resistive switching is explored. This inorganic dielectric is formed spontaneously on the surface of EGaIn, allowing possible printing of liquid metal/dielectric junctions directly onto flexible substrates. This is discussed in Chapter 4.

1.3 Emerging Memory Technologies for Flexible and Printed Electronics

There is a growing interest towards low-cost and flexible memory devices that can be integrated onto non-conventional substrates, such as fabrics, paper, and plastic packaging materials.[14–19] Today, advancements in Si-based microelectronics already demonstrate exceptionally reliable memory devices based on transistor architectures. However, such technology does not address some of the functionalities demanded for future applications in the field of printed electronics. The prospects of logic and memory technologies emerging in the field of printed electronics is discussed in the following section.

Conventional memory used in today's computers is based on Random-Access Memory (RAM), Read-only Memory (ROM), and flash memory.[20] All these components rely on 3-terminal circuitry: the gate, the source, and the drain. The gate is used to control the flow of charge between the source and drain. Although such devices complicate circuitry and require more chip real estate, charge flow across them remains far more superior than other non-conventional 2-terminal memristor-type devices.

The memristor architecture essentially is composed of an insulator sandwiched between two conductors. The resistance across the insulator will depend on the amount of charge that has passed through it. Most memristors exhibit very similar current-voltage (*I-V)* resistive switching, but their underlying physical switching mechanisms may vary significantly.[21–23] **Figure 1.4** summarizes and compares the different types of non-volatile memory technologies in flexible electronics. The two types of switching phenomena pursued in the thesis, are highlighted in yellow. These are:

1. Resistive: Driven by electrochemical redox reactions; the formation/destruction of conducting filaments switches the memory state of the device.
2. Ferroelectric: Switching is controlled by changes in the polarization states of the ferroelectric material by changes the direction of their dipoles.

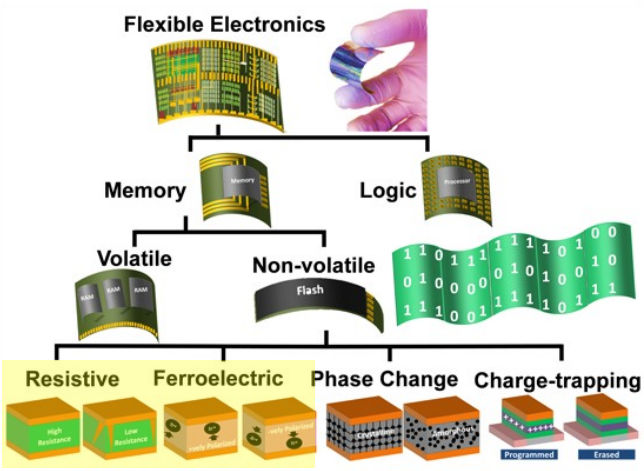

Figure 1.4. Types of memory used in flexible electronics. The two types explored in this thesis are highlighted in the yellow rectangle (Redox-based resistive-type switching and ferroelectric-based switching). Modified and reprinted with permission from [22]. Published by MDPI.

1.4 Organic Ferroelectric-based Memory

1.4.1 Polymer Ferroelectrics

Among the family of organic ferroelectrics, polyvinylidene difluoride (PVDF), with a monomer repeat unit (CH_2–CF_2), shows the strongest ferroelectric behavior, which is characterized by bistable and permanent polarization states that can be reversed under an external electric field. Such electrical behavior makes this polymer a strong candidate for application of data storage and memory devices.[24,25]

The polarization states, which depend on the direction of polar domains (or dipole moments) are indicated by the blue and red arrows in **Figure 1.5a**. Along the polymer chain, the fluorine atoms (green) are oriented in one direction, while the hydrogen atoms (light gray) in the neighboring carbon atom are oriented in the opposite direction. The electric displacement (*D*) or polarization behavior of these polar domains as a function of the electric field (*E*), is shown in **Figure 1.5b**. The polar domains are retained upon the removal of an external electric field, and the direction of these domains can be reversed by applying an electric field of opposite polarity. The rotation of the polymer chain under an electric field is represented in **Figure 1.5c**.

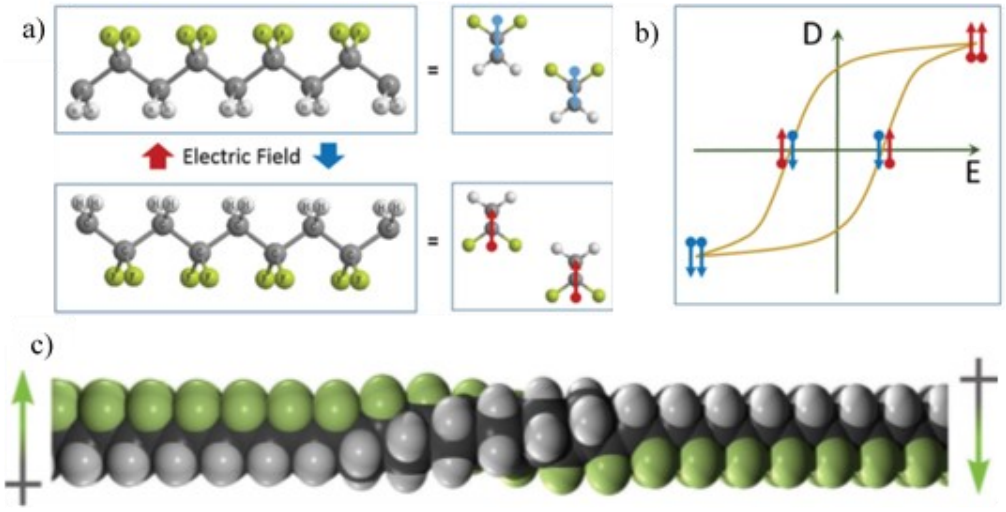

Figure 1.5. a) Chemical structure of PVDF in the β-phase. The red and blue arrows indicate the direction of the polar domains under opposite electric fields. b) Electric displacement (*D*) versus the electric field (*E*) showing typical polarization hysteresis in ferroelectric materials. c) Representation of polymer chain rotation under the influence of opposing electric fields. Reprinted with permission from [24 and 25]. Copyright © 2017 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim and © Elsevier Ltd 2011.

1.4.2 Two-Terminal Ferroelectric Memory Devices

In their simplest form, memory devices based on ferroelectric PVDF or its copolymer poly(vinylidene fluoride-trifluoroethylene), P(VDF-TrFE), are fabricated using a two-terminal capacitor structure and measured using a Sawyer–Tower circuit.[24,26] The capacitor is composed of a thin film of the polymer sandwiched between two conducting electrodes, as shown in the device schematic in **Figure 1.6a**.

Two important parameters that are used to assess the ferroelectric performance of the ferroelectric polymer are the remnant polarization (P_r) and the coercive electric field (E_c), where P_r is electric displacement (or polarization) at zero electric field and E_c is the electric field where the polarization is brought to zero. In principle, a good performing ferroelectric material is characterized by the ability to achieve and retain a high electric displacement (P_r) under minimal switching electric fields (or E_c). The polarization behavior versus the electric field P(VDF-TrFE) is shown in **Figure 1.6b**.[27] This copolymer exhibits an E_c of ~50 MV/m and a P_r of 6–8 μC/cm^2.[28,29]

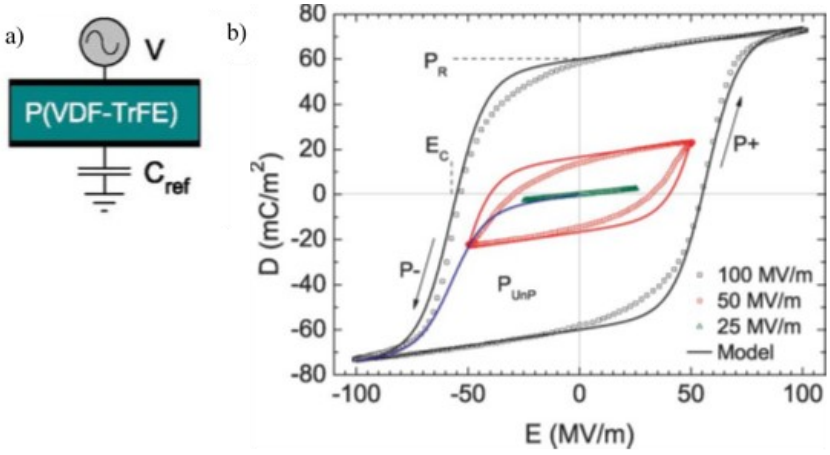

Figure 1.6. a) Device structure for a ferroelectric capacitor made from a film of P(VDF-TrFE) b) A typical polarization hysteresis loop for a P(VDF-TrFE) capacitor. The sweep direction is shown by the arrows on the resultant hysteresis formed upon applying a maximum field of 100 MV/m. Figure modified and reprinted with permission from [27]. Copyright © 2011 Wiley Periodicals, Inc.

In a capacitor structure, the "0" and "1" information depends on the direction of the electric displacement. After polarizing the device in a specific direction, the state of the device is read by applying a switching voltage and recording the transient current response. The polarization state will be lost during this read-out process, and

the device will need to be reset after each read cycle; this is a major disadvantage for integration in efficient electronics.[30,31]

To address the issue concerning destructive read-out in such capacitor structures, an alternative two-terminal device comprised of all-polymer ferroelectric and semiconducting materials has been proposed by Asadi *et al.*[32] The structure and switching mechanism of this diode, fabricated from a blend of P(VDF-TrFE) and P3HT, is shown in **Figure 1.7a**.

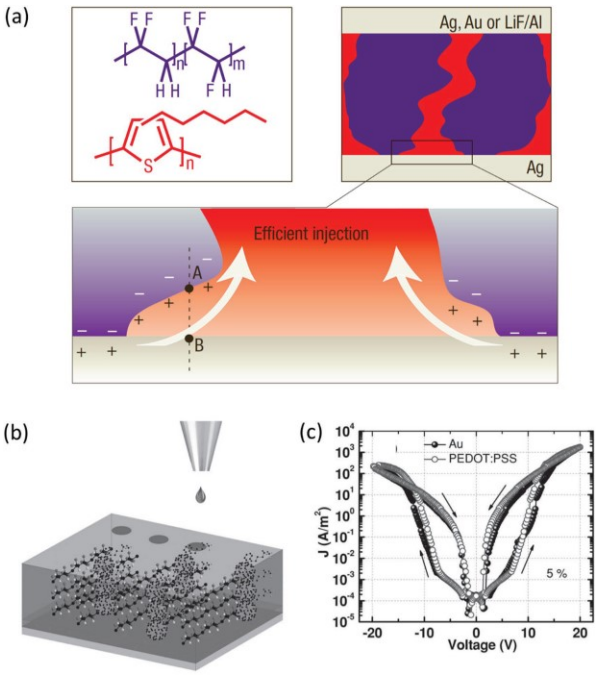

Figure 1.7. a) Chemical structures of the semiconductor P3HT (bottom) and the ferroelectric polymer P(VDF-TrFE) (top). Schematic cross-section of a diode comprised of a blend of the two polymers. Mechanism of switching across the junction by modulation of charge injection at the metal/semiconductor interface b) 3D device representation of a ferroelectric diode made from blends of P(VDF-TrFE) and PCBM. PEDOT:PSS was inkjet printed as the top electrode. c) Current density–voltage (J–V) sweeps of the P(VDF-TrFE)/PCBM devices using Au as a bottom electrode and inkjet printed PEDOT:PSS top electrodes exhibiting resistive switching. Reprinted with permission from [25]. Copyright © 2017 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

In contrast to resistive switching across metal oxides through formation and rupture of conductive filaments, ferroelectric diodes will change their resistance depending on the charge injection at the metal/semiconductor interface. The charge injection will be modulated, depending on the direction of polarization of the ferroelectric, which either will accumulate or deplete charge carriers at the

metal/semiconductor junction. **Figure 1.7b** shows another example of a solution-processed ferroelectric diode fabricated using PCBM as the semiconducting channel.[33] The current density versus voltage behavior for this device is shown in **Figure 1.7c**. Similar to memristors, the state of these devices will depend on the resistance across their terminals. The concept of ferroelectric diodes using hybrid inorganic/organic systems will be explored in more detail in Chapter 2.

1.4.3 Solution-processed Ferroelectric Thin Films of PVDF

As described in the previous section, the polarization behavior of ferroelectric PVDF films, where the direction of polar domains can be switched continuously under an applied electric field, makes this polymer a strong candidate for application of data storage and memory devices. However, PVDF is a semi-crystalline polymer (~50% crystalline), and for it to exhibit favorable ferroelectricity, it needs to be crystallized into specific crystal orientations.[34] Furthermore, to meet the requirements in microelectronics, the polymer needs to form smooth films from solution.[24] These requirements can be optimized by casting the polymer from solution under controlled humidity environments using compatible solvents yielding continuous pin-hole free films. It has also been shown that fabricating capacitors using low molecular weight PVDF (M_w < 400,000) results into films with higher resistivity and improved energy discharge efficiency.[35] On the other hand, films fabricated using high molecular weight PVDF (M_w > 700,000) enhances the capacitance at the expense of lowered resistivity and increased leakage currents. As such, the M_w must be chosen to balance between achieving films with a high dielectric constant and low leakage currents.

Depending on the processing conditions, PVDF can crystallize into four different polymorphs named α, β, γ, and δ with crystal conformations shown in **Figure 1.8**.[36–38]

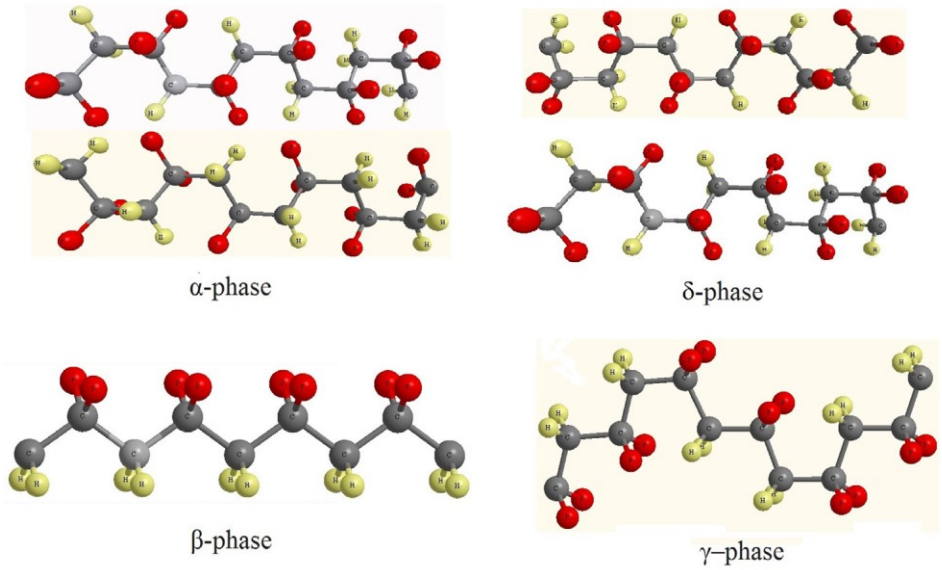

Figure 1.8. Four different crystalline conformations of PVDF. Reprinted with permission from [38]. Copyright © 2017 IOP Publishing Ltd.

Casting films of PVDF from solution or by slow cooling from melt normally leads to crystallization into the most thermodynamically stable and nonpolar α-phase.[34] The less common γ-phase, on the other hand, is difficult to achieve experimentally, as it requires extreme temperature and pressure controls.[40] Various strategies have been implemented to achieve the ferroelectric phases (β- or δ-phases) in PVDF, as summarized in **Figure 1.9**.

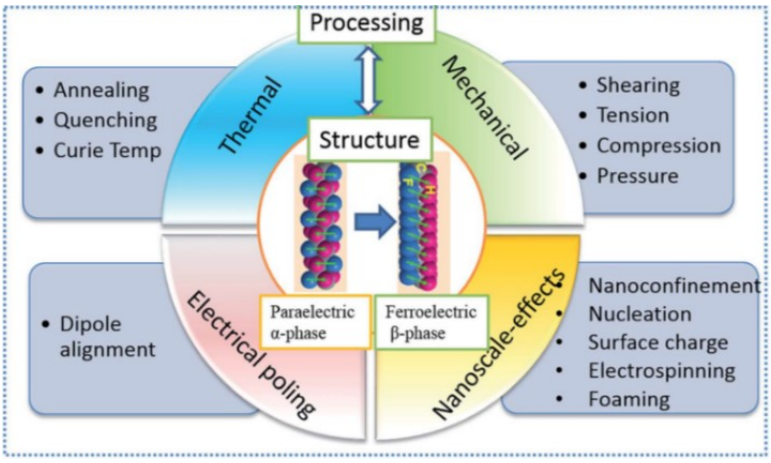

Figure 1.9. Summary of key processing parameters for PVDF-based phases and strategies for achieving required crystalline phases. Additional steps, such as electroforming or mechanical stretching, typically are required to reach the desired ferroelectric phases. Reprinted with permission from [41]. Copyright © The Royal Society of Chemistry 2017.

The polymer typically is subjected to additional processing steps, such as mechanical stretching, electrical poling, controlled thermal annealing, or other nanoscale-effects.[41]

The ferroelectric β-phase in PVDF is the most desired polymorph because it crystallizes in the all-trans (TTTT) conformation, making it possess highly polar domains.[42] These domains can be switched under lower E_c, translating to lower operating voltages, which is an important property required in memory applications.

Other chemical strategies, such as incorporating a specific amount of trifluoroethylene (TrFE, CFH-CF_2) into the homopolymer chain, also have been shown to promote the formation of the ferroelectric β-phase directly from melt, without the need for additional steps, such as electroforming or mechanical stretching.[43,44] However, the low thermal stability (~140 °C) of the remnant polarization for this copolymer limits large-scale integration in industrial application.[45] The commodity polymer PVDF, on the other hand, shows enhanced thermal stability relative to P(VDF-TrFE) but lacks the formation of desirable molecular packing. Nonetheless, efforts to achieve the desired ferroelectric phases in PVDF using controlled processing are being investigated.

Higher grade copolymers or terpolymers of PVDF[46,47] that have large dielectric constant (κ), have other interesting electromechanical properties for alternative applications; these range from pyroelectric and piezoelectric sensors and actuators to high energy density capacitors but are at least 10× more expensive than PVDF (~$10/kg), rendering them less suitable for low cost printed electronics.

In Chapter 3, a scale up approach for α to β phase transformation using photonic annealing, compatible with roll-to-roll process lines, will be discussed in more details to achieving the ferroelectric phases in PVDF thin films.

1.5 Metal Oxide Redox-based Memory

Inorganic metal oxides have been studied widely as potential electrolytes for non-volatile memory devices. Typically, a device is comprised of an insulator, which serves as an electrolyte, sandwiched between two electrodes to form a two-terminal device, as shown in **Figure 1.10a** and **Figure 1.10b**.

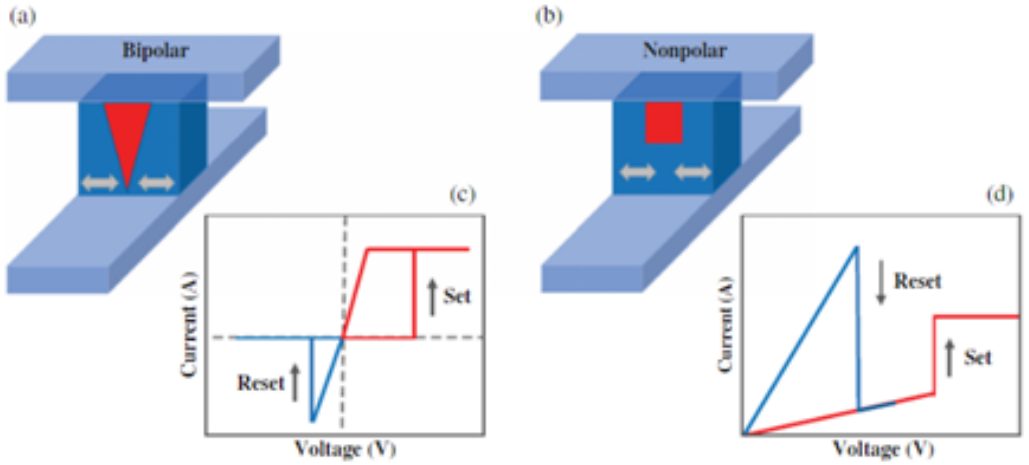

Figure 1.10. Illustration of initial formation of a conductive pathway followed by consecutive set/reset cycles. a) and b) Memristor devices with a metal-insulator-metal (MIM) structure. c) Current–voltage behavior of a memristor exhibiting bipolar switching and d) unipolar switching. Reprinted with permission from [48]. Copyright © 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

Resistive switching is classified into bipolar and unipolar switching, as shown by the current-voltage behavior in **Figure 1.10c** and **Figure 1.10d**, respectively. Switching is characterized by a transition between low resistive ON state (LRS) and high resistive OFF state (HRS). In unipolar switching, the SET and RESET voltages are of the same polarity but of different magnitudes. In bipolar switching, the SET and RESET voltages take place at opposite voltage polarities. A simple illustration for filament formation across the electrolyte is shown in **Figure 1.10a** and **Figure 1.10b**. Upon initial filament formation (also called electroforming), consecutive SET/RESET cycles take place across a thin layer in the insulator.[48]

Changes in the resistance can be due to different effects that take place across the electrolyte and/or by electrostatic/electronic effects across the electrode/electrolyte interfaces. Thus, the underlying physical phenomena that drive these changes in resistance can vary significantly, as summarized in **Figure 1.11**.[49]

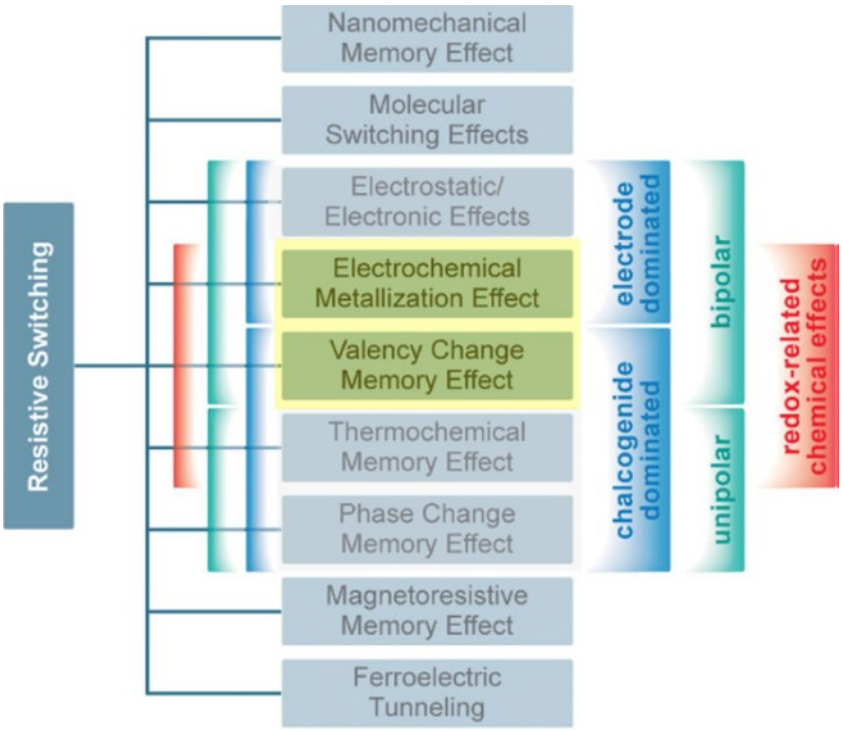

Figure 1.11. Classification of the resistive switching effects that are considered for non-volatile memory applications. This section will cover two types of redox-related chemical switching effects, namely, electrochemical metallization (ECM) and valence change memory (VCM). Reprinted with permission from [49]. Copyright © 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

Complex chemical and thermal processes that drive filament dissolution at the nanoscale are still under discussion.[50] In redox-based resistive switching, the mechanisms that drive resistive switching can be dominated by anionic and/or cationic migration across the electrolyte as well as redox reactions that take place at the electrode/electrolyte interfaces. The focus will be on bipolar resistive switching that is driven by redox-related chemical effects (highlighted in yellow). These switching mechanisms are:

1. Electrochemical Metallization (ECM): Section 1.5.1 describes switching dominated by electromigration of metal cations.
2. Valence Change Memory (VCM): Section 1.5.3 describes resistive switching dominated by electromigration of oxygen anions.

In Chapter 4, resistive switching between liquid metal (EGaIn) and degenerate p-type Si is investigated in detail.

1.5.1 Electrochemical Metallization Memory (ECM)

Resistive switching that is based on electrochemical metallization, sometimes referred to as conductive-bridge RAM (CBRAM), involves the formation and dissolution of metallic filament(s) across the switching layer. These filaments consist of atoms derived from the active electrode material.[51]

The electrochemical processes that drive filament formation are summarized in **Figure 1.12**. When a positive bias is applied to the active electrode (blue spheres), oxidation takes places at the active electrode/electrolyte interface, leading to anodic dissolution of the metal (M), according to the reaction (labeled "A" in **Figure 1.12**):

$$M \rightarrow M^{z+} + z\, e^{-}$$

where M^{z+} is a metal cation formed at the electrode/electrolyte interface. Applying an external electric field drives the migration of these cations (labeled "B" in **Figure 1.12**) across the solid electrolyte (yellow spheres) and towards the negatively charged cathode (gray spheres), where they undergo electrocrystallization[52,53] by cathodic reduction, according to the reaction (labeled "C" in **Figure 1.12**):

$$M^{z+} + z\, e^{-} \rightarrow M$$

The reduced metal then serves as a seed for further nucleation (labeled "D") and growth of metallic filaments (labeled "E"), until it forms a tunnelling gap between the electrolyte and the active electrode (labeled "F").[54–56] At this point, electrons can move across the terminals through percolating metallic filaments.

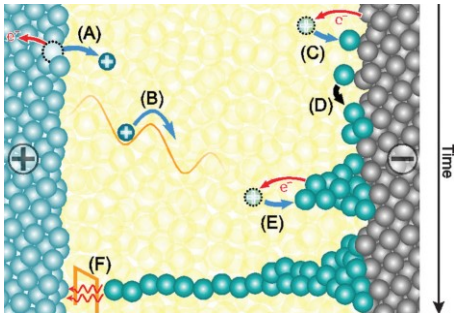

Figure 1.12. Illustration of the electrochemical processes that take place during filament formation. (A) The active electrode undergoes an oxidation reaction for form mobile cations. (B) Migration of cations under the applied electric field. (C) Cations undergo a reduction reaction from electrons injected from the counter electrode. (D) Reduced metal atoms then nucleate and (E) drive further nucleation for filament growth through the electrolyte. (F) Filament extends closer to the active electrode until tunneling of electrons near the interface turns the device to a low resistive state. Reprinted with permission from [56]. Copyright © the PCCP Owner Societies 2013.

The linear current–voltage plot in **Figure 1.13** shows a 2-terminal device exhibiting typical ECM-type bipolar resistive switching. Sweeping the device from A to D shows how changes in resistance, shown in the *I-V* plot, relates to the redox reactions discussed in **Figure 1.11**. In this example, the SiO_x electrolyte is sandwiched between Ag as an active electrode and Pt as an inert electrode. Once a filament is formed (**Figure 1.13D**), the device remains in a low resistance ON state. When a negative voltage is applied, the filament ruptures and returns to a high resistance OFF state (**Figure 1.13E**).[57]

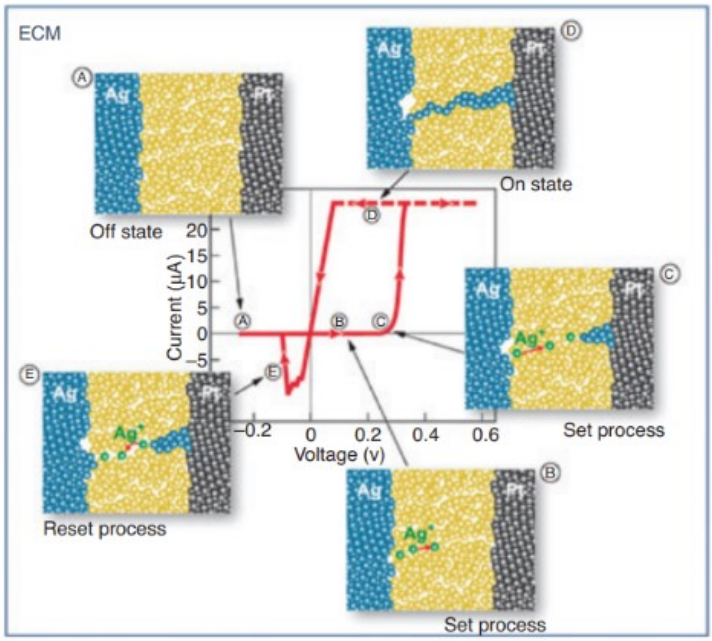

Figure 1.13. Current–voltage plot showing typical bipolar resistive switching in an ECM cell comprised of SiO_x, sandwiched between an active top electrode (Ag) and an inert bottom electrode (Pt). Reprinted with permission from [57]. Copyright © John Wiley & Sons, 2012.

In summary, ECM-type switching is dominated by formation and migration of cationic species to form metallic filaments across the switching electrolyte. The formation and rupture of these filaments is responsible for the observed changes in resistance.

1.5.2 Influence of Electrode Materials on ECM-type Switching

ECM switching is driven by the formation and dissolution of conducting filaments. These filaments are typically comprised of metal atoms from the active electrode.[58] Prior to filament formation, the active electrode serves as an anode that partially oxidizes when a positive voltage is applied to it. Under high electric fields, the cations migrate towards the cathode, where they are reduced to form a nucleus that promotes further filament growth.

To maintain electroneutrality, the system is complemented by electrochemical processes that take place at the counter electrode. For most metal oxides, these counter electrochemical processes involve the reduction of moisture that typically is incorporated in the electrolyte during device fabrication or from the ambient environment.[59] Chemical reduction of water at the counter electrode is favored kinetically over the decomposition of the electrolyte and can, therefore, influence the switching kinetics and even enhance the mobility of the cations.[60]

Silver and copper are the most common active electrodes used for ECM-type switching. Other metals such as titanium[61] and alloys[62,63] also have been used as active electrodes, as they can bypass the need for anodic oxidation at the electrode/electrolyte interface and provide a direct supply of mobile cations needed for switching. Nonetheless, the selection of active electrode materials still is based on empirical data; therefore, their electrochemical properties that drive redox are not well-studied.

For ECM switching, Lubben *et al.* proposed a criterion that relates the thermodynamics of the system to half-cell redox reactions at the active electrode.[58] Generally, their results indicate that the metal of the active electrode should be oxidized easily (without passivating) while the formed cations must be reduced easily. Furthermore, high ionic mobility across the electrolyte that can facilitate fast and low energy switching of thin filaments is necessary. From a thermodynamic approach, these requirements can be satisfied when the metal cations are slightly above or around 0 kJ mol^{-1}. These metals were shown to be Ag, Cu, and Fe, as shown in **Figure 1.14**. As a reference, we also include redox pairs for Ga, which was used as a working electrode for resistive switching in this thesis.

In the next section, the switching mechanism in valence change memory (VCM) will be discussed where switching is dominated by formation of vacancies across the electrolyte.

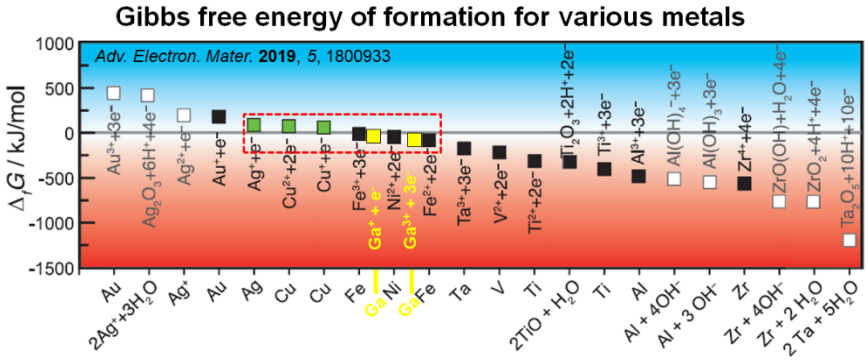

Figure 1.14. Redox pairs of metals with positive Gibbs free energy tend to stay reduced, while metals of pairs with negative energy tend to oxidize but are difficult to be reduced again. The choice of active electrode materials for ECM are fulfilled by metal cations having a Gibbs free energy of formation that is close to 0 kJ mol^{-1} (marked inside the red dashed box), where we have included Ga redox pairs (yellow squares). Figure modified and reprinted with permission from [58]. Copyright © 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

1.5.3 Valence Change Memory (VCM)

Resistive switching in VCM memory, also known as OxRAM, occurs in many metal oxide (MO) systems that exhibit mixed ionic–electronic conduction.[64] **Figure 1.15a** shows an example of VCM switching using an electrolyte sandwiched between inert electrodes.

During the initial electroforming process, driven by voltage and temperature (Joule heating), long range motion of the oxygen vacancies across the MO lead to the formation and growth of a filament or "Plug", composed of highly defective regions.[65] These low resistance defect sites act as mobile donors in the form of oxygen vacancies and/or cation interstitials and exhibit n-type conduction. The "Plug" will grow from "electrode B" and extend until it nears the interface of "electrode A" (Scheme A). At this point, a potential barrier (or "Disc") a few nanometers in thickness is formed, serving as the active switching layer upon further current-voltage cycling. When a negative voltage is applied to "electrode A", oxygen anions drift towards the "Plug", leaving positively charged oxygen vacancies at the "Disc" region (Scheme B). The high concentration of oxygen vacancies then results

in a decrease in the barrier height and width at the "electrode A"/MO interface, turning the device to a low resistance ON state (Scheme C). To reset the device back to the high resistance OFF state, a positive voltage is applied to "electrode A", pushing oxygen vacancies towards the "Plug", oxidizing the "Disc" near the "electrode A"/MO interface, leading to a transition back to the HRS (Scheme D). For illustration, the distribution of oxygen vacancies and the corresponding band-diagrams across the MO and near the "electrode A"/MO interface in the HRS and LRS are shown in **Figure 1.15b** and **Figure 1.15c**, respectively.[66]

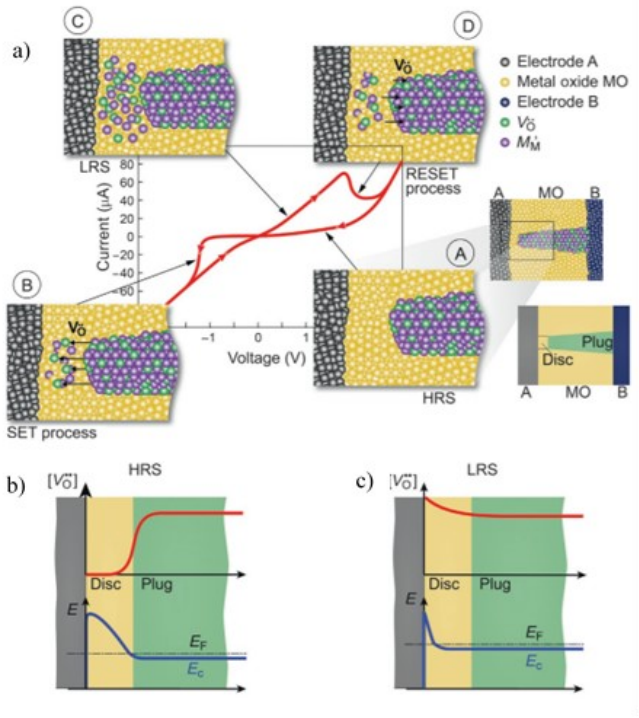

Figure 1.15. a) Current–voltage plot showing typical bipolar resistive switching in a VCM cell comprised of an electrolyte that is sandwiched between two electrodes. Schemes A–D show a filament in the "plug" region extended to electrode A and the corresponding distribution of oxygen vacancies and metal cations in the "disc" region under the influence of an electric field when the device is in (A) the OFF-state (B) during the SET process (C) in the ON-state, and (D) during the RESET process. b) Concentration of oxygen vacancies and corresponding band-diagram when the device is in the HRS OFF-state and in c) LRS ON-state. Modified and reprinted with permission from [65]. Copyright © 2018 Elsevier Inc.

1.5.4 Competition Between VCM and ECM Switching

There are competing mechanisms for filament formation in bipolar resistive switching, dominated by drift of either anions in the VCM mechanism or cations in an ECM mechanism, depending on the relative ion mobility and redox rates.[67,68]

Recent studies using scanning tunneling microscopy (STM) by Wedig *et al.* have provided evidence that host cations in VCM-type metal oxide systems (TaO_x, HfO_x, and TiO_x) on the length scales of ~2 nm can participate in the resistive switching process and form metallic filaments, as shown in **Figure 1.16**.[69]

When an anodic bias voltage was applied to the probing Pt tip, the morphology of the sample surface was unchanged (**Figure 1.16**, Scheme A). However, upon applying a cathodic bias voltage at the tip, there was an abrupt increase in current, reflecting a transition to the low resistive state (**Figure 1.16**, Scheme B). After the pulse elapses at –1 mV (**Figure 1.16**, Scheme C), the conductance is higher than the quantum conductance during the initial atomic point contact in Scheme A. This conductance remains stable for a short period and returns to its initial value; it is explained by the disruption of the metallic filament by reoxidation, even under ultrahigh vacuum conditions (**Figure 1.16**, Scheme D). From these observations, this insulator–metal transition does not point to modifications of oxygen defects within the MO, as described in typical VCM switching, but rather to the formation of a metallic contact described by ECM mechanisms.

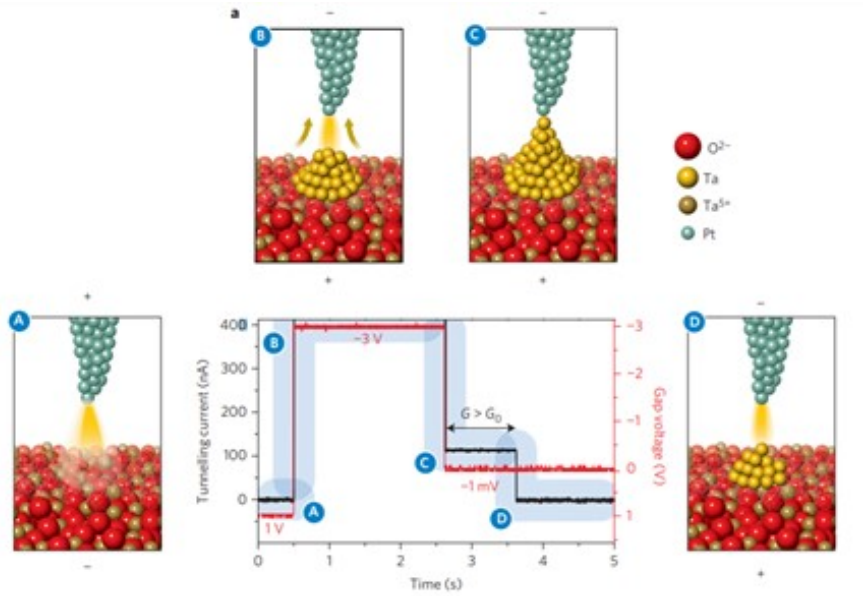

Figure 1.16. Scanning tunneling microscopy conducted on the surface of a 2 nm thin TaO_x film. The schemes from A to D show structural changes that occur on the surface with time by tunneling currents under step-wise alteration of the tip voltage from +1 V → –3 V → –1 mV. Variations in quantum conductance indicate that metallic filaments are formed by migrating Ta^+ ions towards the cathodic tip. Low filament stability is attributed to reoxidation under ambience. Reprinted with permission from [69]. Copyright © 2016 Macmillan Publishers Limited.

As such, distinguishing between VCM and ECM mechanisms becomes increasingly difficult at nanoscale dimensions. Based on these observations, and since the thickness of the passivating GaO_x investigated in this work is also on the order of 1–3 nm, it is postulated that switching is based on the formation of filaments composed of metallic gallium under an ECM switching mechanism. This will be discussed in more details in Chapter 4.

1.6 Liquid Metals in Flexible Electronics

Liquid metals, such as gallium and its alloys (e.g., Ga and In in EGaIn or Ga, In, and Sn in galinstan) are known for their excellent conductivity and flexibility, making them attractive materials in various applications. The behavior of liquid metals is dominated by their surface chemistry, primarily due to high oscillation of electrons near the surface,[70] changing from strongly metallic to van der Waals interactions.[71–73] Thus, their unique surface chemistry has been utilized in many new applications, ranging from catalysis, conductors in flexible electronics, and even as substrates for epitaxial growth of 2D materials.[74–87] Some of these applications are illustrated in **Figure 1.17**. The low toxicity and biocompatibility of these liquid metals make them adaptable in many biomedical applications, such as imaging, drug delivery, and cancer therapy. The rheological properties also have been used for applications in microfluidics.

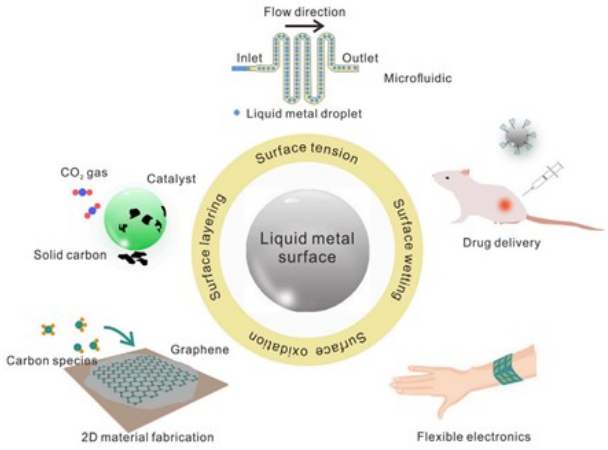

Figure 1.17. Brief overview on surface properties and characteristics of liquid metals and their utilization in a broad range of applications. Reprinted with permission from [73]. Copyright © 2020 Elsevier Inc.

Surface oxidation of liquid metals provide mechanical properties that stabilizes them, allowing the formation of unique shapes. This makes them well-suited for patterning complex shapes in printed electronics.[73] More importantly, Chapter 4 shows how the self-passivating surface oxide plays a critical role in the performance of liquid-based memory devices.

Controlled functionalization, combined with lithographic patterning, also allows for selective coating of the metal and/or metal oxide onto specific sites on the substrate surface.[88,89] Large areas of oxide-capped Si substrates can coat very thin layers of the surface oxide readily.[90]

The rheology of liquid gallium and its alloys enables a simple integration to high-throughput printing, which makes them suitable in flexible electronics. Many well-established fabrication techniques, such as mask lithography,[91–93] freeze-casting,[94] 3D printing,[95,96] laser engraving,[97] and microcontact printing,[98] can be used to pattern liquid metals on the surface of suitable substrates. Simplistic approaches have also been demonstrated to transfer liquid metal onto selected flexible and transparent substrates using a ball-point pen, reaching a modest line resolution of ~650 μm.[99] Applications that require higher line resolutions are possible using alternative methods, such as micro-imprinting, shown in **Figure 1.18**, reaching a line resolution of ~2 μm.[100]

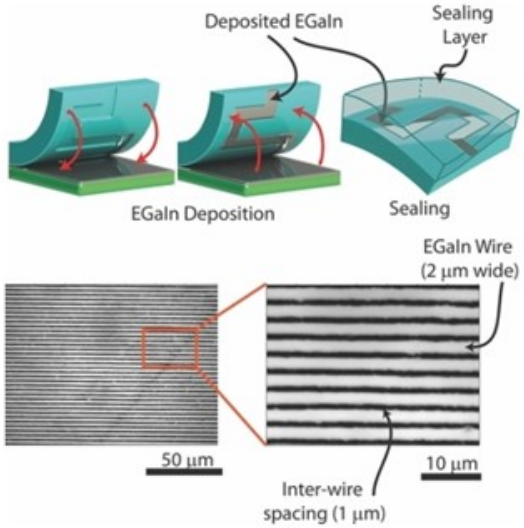

Figure 1.18. Large area PDMS-based imprinting of EGaIn on a flat surface, showing excellent line resolution down to 2 μm width. Figure reprinted with permission from [100]. Copyright © 2014 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

1.6.1 Structure and Properties of Native Gallium Oxide in EGaIn

Depending on the application, the metal core and/or the surface oxide of liquid metals serve as the active material(s). **Figure 1.19** depicts the structure of a liquid metal droplet (black core) passivated by an oxide on its outer surface (blue "shell").[85]

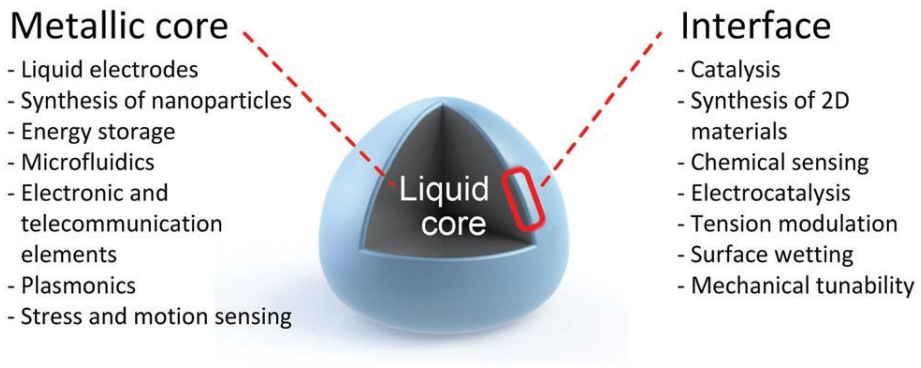

Figure 1.19. Schematic of a liquid metal droplet, showing applications of liquid metals that take advantage of the liquid core or the interfacial region near and at the surface. Reprinted with permission from [86] Copyright © The Royal Society of Chemistry 2018.

Exposing gallium-based liquid metals to air leads to spontaneous and rapid formation of a self-passivating oxide on the surface. These oxides have been studied extensively in various reports.[85,101,102] The oxide layer is found to be amorphous or poorly crystalline and estimated to be between 0.5 and 3 nm in thickness.[76,85,101] Spontaneous formation of the surface oxide can be inhibited only using ultrahigh vacuum systems.

The surface oxide can grow even under low oxygen partial pressures (>ppb) and moderate temperatures by following the well-described Cabrera–Mott oxidation model.[103–105] The formation and growth process proceeds once oxygen atoms are adsorbed to the surface of the metal, until they ionize, migrate, and become incorporated into the oxide layer. This leads to fractal-like growth of the oxide by diffusion-limited aggregation, as shown in the Secondary Ion Mass Spectrometry (SIMS) images in **Figure 1.20**.[106] Figure 1.12a-d show the growth process between 60–2400 sec. In this study, it was found that full oxide coverage takes place after ~7000 sec and is independent of the area of the liquid metal. The bright regions show the oxide layers, where the relative thickness is related to the intensity.

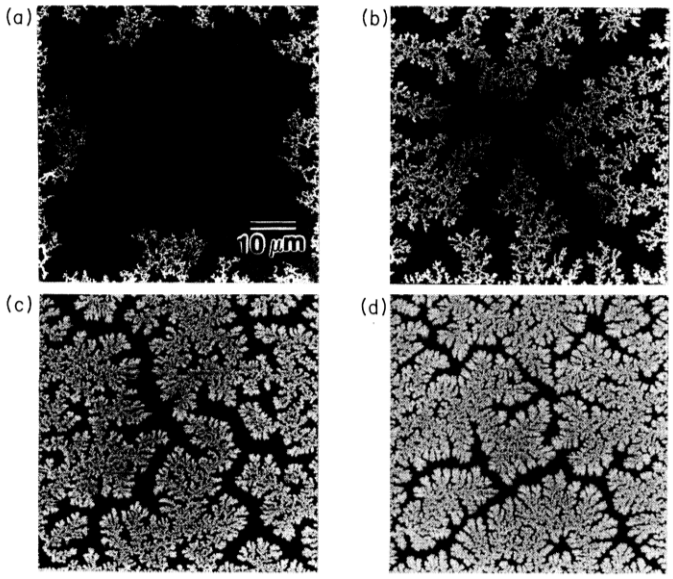

Figure 1.20. Secondary Ion Mass Spectrometry images (60 μm)^2, showing the formation and growth of gallium oxide on the surface of gallium. Reprinted with permission from [106]. Copyright © 1992 The American Physical Society

Although most of the oxide layer formed on the surface of the metal is thin (~0.7 nm), smooth, and conformal, it was found that there are discrepancies in the thickness across the oxide skin near the metal/oxide interface at the microscale.[107] Upon removal of this thin outer oxide layer, threadlike patterns that are 3–4 μm in width were observed using ToF-SIMS analysis, shown in **Figure 1.21**. These oxide patterns resemble the fractal-like patterns observed in **Figure 1.20**, which indicates that the surface oxide is heterogeneous.

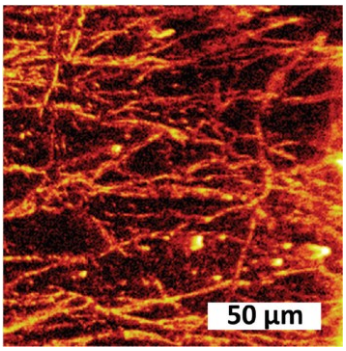

Figure 1.21. ToF-SIMS analysis that shows inhomogeneity in the thickness of the oxide layer after the removal of the thinnest region (~0.7 nm). The brighter threadlike regions (~3–4 μm wide) reflect more counts of $^{71}GaO_2^-$ fragments. EGaIn was frozen to –25 °C during analysis. Reprinted with permission from [107]. Copyright © 2012 American Chemical Society.

The composition of the oxide shell formed on EGaIn has been analyzed using angle-resolved XPS studies.[107,108] These studies show that the type of species that are present across the oxide change with the relative depth, as shown in **Figure 1.22a**. At the oxide/air interface, a thin adventitious layer, with an average thickness of 0.7 nm is present upon exposure to air for ~1 h. This layer is comprised of organic contaminants as well as organic oxygen and hydroxyls. Positioned just below this adventitious layer is Ga_2O_3 (Ga^{3+}), followed by a Ga_2O suboxide interlayer (Ga^{+}), In_2O_3 (In^{3+}), and finally reaching the bulk eutectic metal (Ga^0 and In^0). The formation of a Ga_2O suboxide as an interlayer between Ga_2O_3 and metallic gallium also has been shown using X-ray scattering analysis, shown in **Figure 1.22b**.[101] These analyses were conducted on the surface of the metal by applying very low doses of oxygen to form a monolayer.

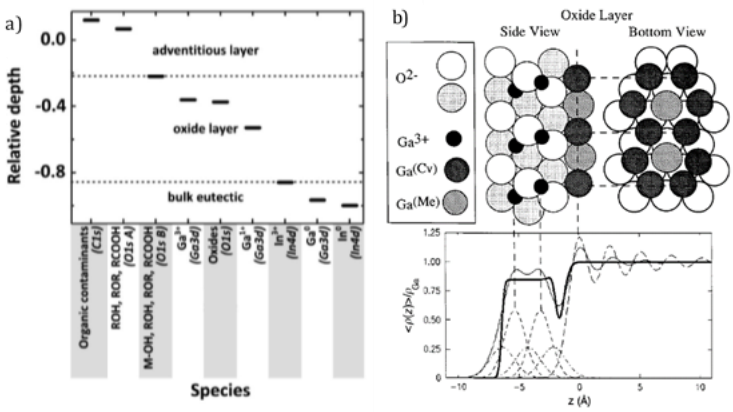

Figure 1.22. a) Heterogeneous composition of the surface oxide in EGaIn revealed via XPS measurements. The relative location of main species between the oxide/air and the oxide/metal interfaces are approximated using angle-resolved XPS. b) XRD data shows the formation of a Ga2O interlayer between metallic Ga and Ga2O3. Reprinted with permission from [101 and 107]. Copyright © 1997 The American Physical Society and Copyright © 2012 American Chemical Society.

1.5 Summary

The processing and switching mechanisms of two materials systems that can be used for printable memory are discussed in this chapter. PVDF can be printed from solution but has challenges associated with achieving the ferroelectric phases. The liquid metal, EGaIn, and its native oxide are also explored as candidate materials for printed memory. The following chapters utilizes the properties of these materials towards the fabrication of memory devices.

CHAPTER 2: Hybrid Ferroelectric Diodes

2.1 Introduction

Advancements in Si-based microelectronics have demonstrated reliable memory devices, based on the three-terminal transistor device architecture.[109] Typically, memory devices in today's computers are characterized by the formation of a voltage-driven hysteresis by charging/discharging of capacitors.[110] However, there are various mechanisms that underpin information storage using different device architectures, and in each case, the physical characteristics of the materials that enable the memory effect can be quite different.[111] Computers operate using three complementary types of data storage that have different functions: 1) Static Random-Access Memory (SRAM), 2) Dynamic Random Access Memory (DRAM), and 3) Magnetic-type hard disks or FLASH memory for long term storage of data.

It is envisioned that future "universal" memory systems will combine the benefits of all the above modes of information storage in computers into a single system. One example is the fabrication of low-power and high storage density resistive random access memory (ReRAM) using simple and scalable crossbar device architectures assembled in 3D.[112–114] Ideally, in such geometries, devices will be scaled down to nanoscale dimensions and will function using 2-terminal contacts, replacing the conventional 3-terminal transistor architecture.

2.2 All-Organic Ferroelectric Diodes

Simple and low-cost fabrication of ferroelectric-based memory, 2-terminal devices, shown in **Figure 2.1a** (capacitor) and **Figure 2.1b** (diode), as opposed to 3-terminal transistors, shown in **Figure 2.1c**, permit simple circuits with the desired crossbar geometries. However, since capacitor structures suffer from cross-talk and destructive read out,[115,116] the target is to fabricate the type of non-volatile ferroelectric memory diodes, shown in **Figure 2.1b** (green rectangle), which can offer the advantage of having a simple 2-terminal device structure that functions like a transistor by changing the resistance across the semiconducting channel. Ferroelectric tunnel junctions (FTJs) comprised of ultrathin layers of ferroelectric materials that change

their intrinsic tunnel resistance, depending on the direction of polarization,[117] is another example of 2-terminal diodes; these will not be discussed in this work.

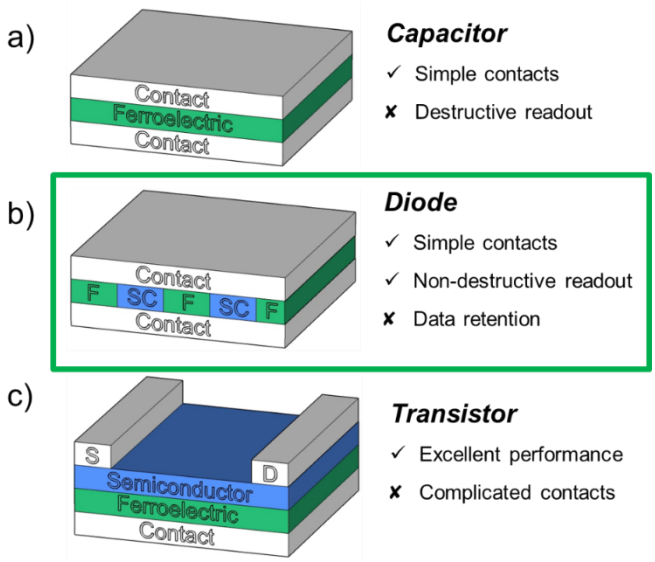

Figure 2.1. Schematic representation of a ferroelectric device, with a) capacitor, b) diode, and c) transistor structures. The objective in this chapter will be to explore 2-terminal diodes using a hybrid system of P(VDF-TrFE) and semiconducting Si. Selected pros and cons are summarized next to each structure.

A cross-sectional device and switching mechanism of the type of ferroelectric diode studied in this chapter is illustrated in **Figure 2.2a** and **Figure 2.2b**. The direction of polarization in the ferroelectric layer (light blue) will depend on the direction of the applied electric field at the electrodes (gray). Consequently, accumulation of electrons or holes at the semiconductor/ferroelectric interface will lead to band bending, which modulates charge injection at the semiconductor/electrode interface. A shift in the barrier height of the semiconductor and the work function of the metal contact will dictate whether the device operates in a high resistive OFF-state (HRS) (injection limited in **Figure 2.2a**) or a low resistive ON-state (LRS) (ohmic-space-charge limited in **Figure 2.2b**).[118]

There are several reports on all-organic ferroelectric memory diodes, based on the organic polyme, P(VDF-TrFE) blended with other organic semiconductors (e.g., P3HT, PCBM, F8BT, PFO).[119–122] **Figure 2.2c** shows a typical current–voltage plot for a device made from a blend of P(VDF-TrFE) and poly(9,9-di-n-octylfluorene-alt-

benzothiadiazole) (F8BT) sandwiched between two Au electrodes.[118] The direction of the arrow in **Figure 2.1c** represents the device being switched from the OFF to the ON state by applying a bias above the coercive voltage (V_c) to induce polarization. Once the domains are polarized, the device remains in the ON state.

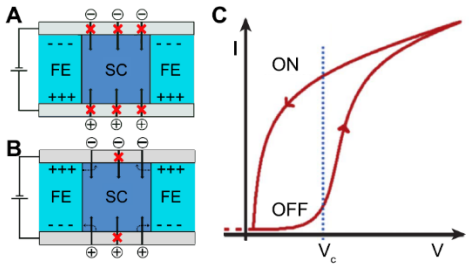

Figure 2.2. Cross-sectional scheme of a ferroelectric diode in the (a) OFF state and (b) ON state. The ferroelectric (FE), semiconductor (SC), and electrode layers are colored in cyan, blue, and gray, respectively. The polarization of the FE bends the bands at the SC interface to create stray fields (dashed arrows), leading to changes in resistance by injecting (black arrows) or blocking (red cross) charge carriers across the SC/metal interface. (c) *I–V* hysteresis behavior for a ferroelectric diode, based on a Au/P(VDFTrFE):F8BT/Au diode. Reprinted with permission from [118]. Copyright © 2017 Elsevier B.V.

Devices with alternating semiconducting and ferroelectric channels are typically fabricated by simple solution casting of these polymer blends (like bulk heterojunction organic photovoltaics) and nanoimprinting, as shown in **Figure 2.3a** and **Figures 2.3b**, respectively.[123–125] The influence of resistive switching on the structure and morphology also was investigated using other patterning approaches, such as polymer self-assembly.[126]

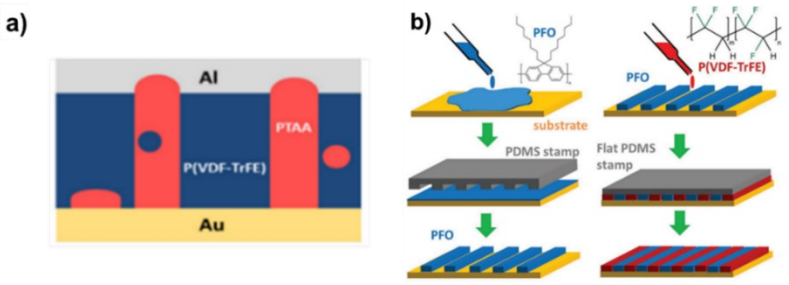

Figure 2.3. Illustration of different approaches to forming ferroelectric diodes that contain channels of semiconducting and ferroelectric materials in the active layer that span the electrodes. a) Direct spinning of polymer blends to form random morphologies. b) Creating channels using nanoimprinting techniques. Figures reprinted with permission from [123] Published by AIP Publishing and [124] Copyright © 2016 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

2.3 Hybrid Ferroelectric Diodes

In contrast to the above all-organic systems, the primary objective in this chapter is the exploration of hybrid inorganic/organic memory diodes based on P(VDF-TrFE) and the semiconductor, silicon. This hybrid system will be composed of a random array of Si nanopillars and P(VDF-TrFE) that mimic the structure of all-polymer ferroelectric diodes, described in the earlier section, and was achieved using the following three-step processing approach:

Step 1. Metal dewetting: First, a lithography-free metal dewetting technique will be used to produce nanopatterns of Ag on the surface p-type Si.

Step 2. Metal-assisted chemical etching (MACE): Next, the dewetted Ag nanopatterns are used as catalysts for metal-assisted chemical etching (MACE) on the Si surface to form Si pillars.

Step 3. Polymer filling: P(VDF-TrFE) is spun from solution to fill the voids created in the Si structure, followed by deposition of top Ag contacts.

Process optimization of the dewetting, MACE, and polymer filling steps are discussed in detail in the following subsections. The optimized parameters chosen to create the final device architecture is illustrated in **Figure 2.4**.

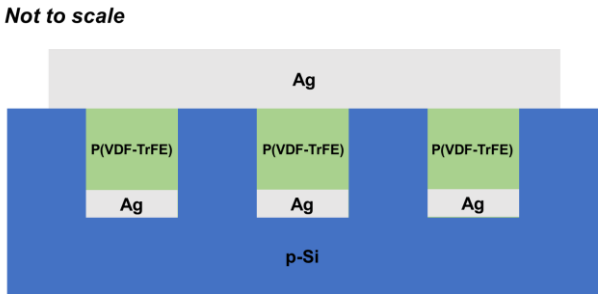

Figure 2.4. 2D cross-section schematic of the final device structure after optimizing the Ag film dewetting conditions, MACE process, polymer filling, and finally the deposition of 60 nm Ag as a top electrode using a shadow mask.

In the first step of this work, a series of control experiments were conducted to understand the origin of *I–V* hysteresis in metal (Ag and EGaIn)/semiconductor (p-type Si) junctions, with and without the addition of the ferroelectric polymer. The chapter is concluded with a discussion and summary on our main findings.

2.3.1 Metal Dewetting: A Lithography-free Patterning Technique

To form arrays of Si nanopatterns, three metal patterning techniques were explored: i) using particle nanolithography to form ordered arrays of Si nanopillars, shown in **Figure 2.5a**, ii) direct etching on Si substrates catalyzed by sputtered metal films of Ag, shown in **Figure 2.5b**, and iii) dewetting thin films of Ag to form random nanostructures of Si, shown in **Figure 2.5c**. Among these three patterning techniques, dewetting using Ag films, shown in **Figure 2.5c**, was adopted for further investigating due to its simplicity and reproducibility. This dewetting process will be discussed in more details in the proceeding sections.

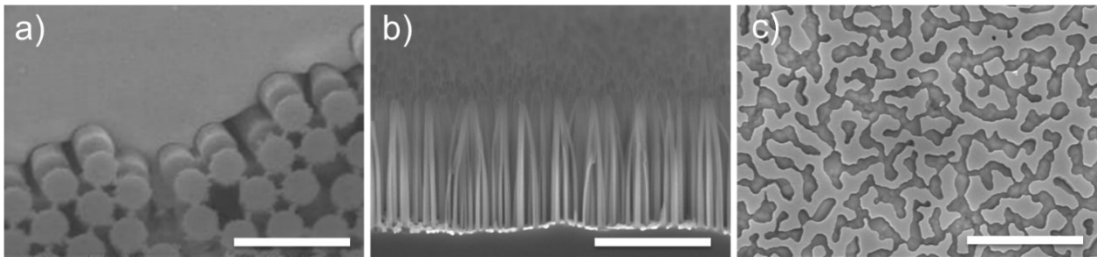

Figure 2.5. SEM images, showing a) top view of partially cylindrical nanopillars formed by MACE after patterning an Au film using particle nanolithography with undissolved spheres on the top surface, b) cross-sectional view of Si nanowires formed by MACE directly on 20 nm of as-sputtered Ag films, and c) top view of random Si nanostructures formed by MACE on dewet films of Ag (~20 nm). All scale bars = 1 μm.

Dewetting of thin metal films on solid substrates has been studied well in the literature.[127–130] Metals are normally metastable in their as-deposited state and can agglomerate spontaneously to form islands, when their mobility becomes sufficiently high under elevated temperatures. In addition to thermally-driven restructuring, several other factors also can influence nucleation and growth phenomena, such as the presence of holes on the surface, contamination, film edges, and grain boundaries.[128]

Dewetting of Ag layers on Si has been shown to form a range of structures and morphologies that depend on the initial thickness of the as-deposited Ag layer. In the following experiments, we examined the dewetting of Ag layers, up to 100 nm, over p-type Si surfaces capped with a native oxide SiO_x using modified annealing conditions described in the literature.[131] Metal dewetting was used to examine the influence of Ag coverage on the rectification behavior and charge transport across the

Ag/p-Si interface and was achieved by heating sputtered Ag films on p-Si at 135 °C inside a vacuum oven for 10 s. Top view SEM images in **Figure 2.6** show the resultant film morphologies for films ranging between 10 and 100 nm following the dewetting process. For films with initial thicknesses of 10–20 nm, isolated Ag nanoparticles (Ag NPs) were formed. The Ag NPs formed after heating the 10 nm- and 20 nm-thick films had a broad size distribution, with the largest particles on the order of 20 nm and 40 nm, respectively. For the 40 nm-thick film, Ag islands were formed, comprised of isolated particles (20–40 nm in diameter) and elongated clusters, with high aspect ratios, reaching a few microns in length (1–5 μm). For the 60 nm-thick films, it appeared that a more interconnected percolating Ag network was formed, a feature that is required for the chemical etching process discussed in later sections. Thicker films of 80–100 nm formed smoother films, with scattered pores and little dewetting. For Ag films with thicknesses >100 nm, dewetting did not change the top surface morphology. The trend of changing morphologies with increasing film thickness (i.e., isolated Ag NPs → percolated Ag → scattered pores over continuous Ag films) is similar to what has been observed in the literature but using relatively thicker initial Ag film layers. These differences are associated with changes in the Ag deposition technique, Si doping and surface treatment, and annealing conditions that resulted in slight variations of the required initial Ag film thicknesses.[130,131]

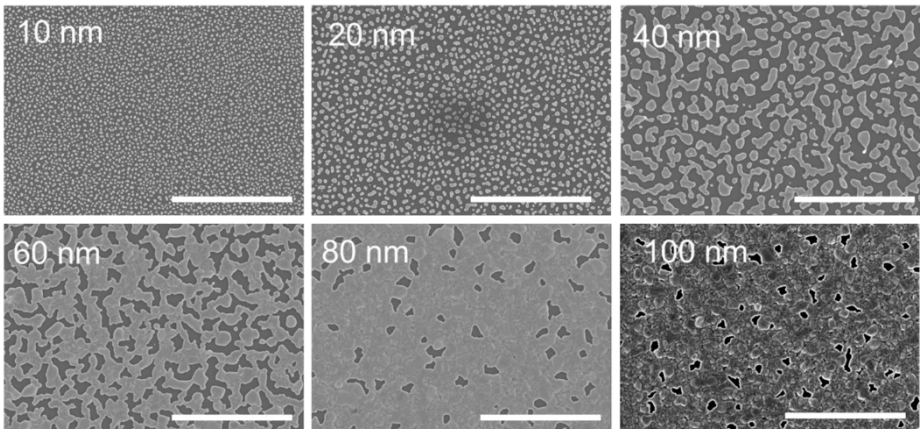

Figure 2.6. Dewetting of Ag films with different initial thicknesses (10–100 nm) at 135 °C for 10 s in vacuum. The morphology of Ag changes from isolated Ag nanoparticles to a percolating network. Pinholes were observed for thicker films, and no dewetting occurred above a thickness of 100 nm. All scale bars = 5 μm.

2.3.2 Understanding Charge Transport over p-type Silicon (p-Si)

Before investigating the proposed inorganic/organic hybrid system, a series of experiments were conducted to help us understand the nature of charge transport across the metal/inorganic semiconductor interface, before and after metal dewetting.

p-type silicon (p-Si) chips were tested electrically by directly probing their surface with InGa eutectic alloy (EGaIn) as a soft metal contact (working electrode). The bottom of the p-Si chip was scratched in the presence of EGaIn using a diamond scribe to ensure an ohmic contact (grounded terminal), as presented in **Figure 2.7a**. The insets in **Figure 2.7b** show 2D schemes of the proposed metal-oxide-semiconductor (MOS) structures, with the surface of p-Si capped with the native SiO_x (2.5 ± 0.5 nm). The formation and presence of a thin native GaO_x layer on the surface of EGaIn is expected, but since we are applying extremely high voltages, its contribution to charge transport will be neglected.[132,133]

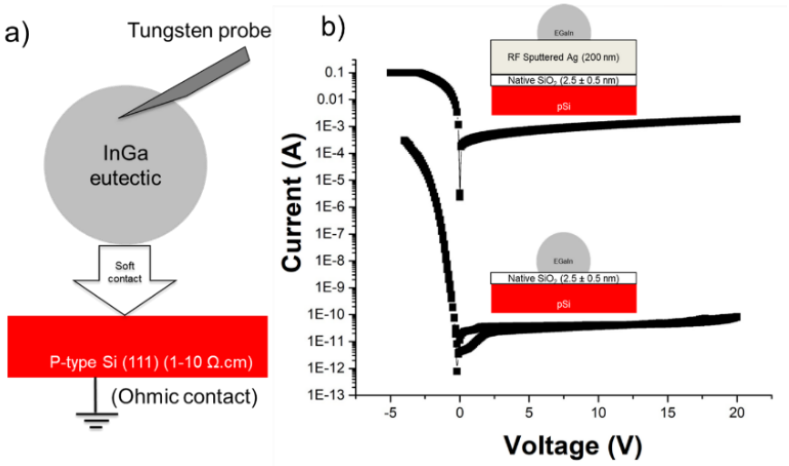

Figure 2.7. a) 2D schematic representation, showing how p-type Si was probed by soft contact with InGa eutectic (EGaIn) and (b) *I–V* behavior of piranha-treated p-Si wafer, with and without a continuous layer of sputtered Ag (initial thickness of 200 nm). Both layers exhibit a rectifying behavior by forming Schottky junctions.

From the *I–V* curve in **Figure 2.7b**, cyclic sweeps (–5 V→ +20 V→ –5 V) of EGaIn/SiO_x/p-Si junctions showed a typical rectifying behavior by forming a Schottky junction at the interfaces, with currents reaching the µA range at –5 V. Similarly, probing EGaIn/Ag/SiO_x/p-Si junctions (p-Si coated with a continuous film of RF sputtered Ag and without any dewetting) also revealed a similar rectifying

behavior but with larger leakage currents under both the forward and reverse biases, showing currents reaching the mA range at –5 V. The formation of a Schottky junction and the resultant rectifying behavior is expected since the work functions of the metals are lower than the Fermi energy for p-type Si ($\Phi_{Ag\ or\ Ga} < \Phi_{p\text{-}Si}$). When *both* terminals were formed by scratched EGaIn, the *I–V* plot shows a transition to ohmic conduction. This change in behavior indicates that the depletion region and the interfacial oxide layer contribute to charge transport and the rectifying behavior across these junctions.

Figure 2.8a shows the band energy for an MOS diode at zero bias for a p-type semiconductor. When a positive bias is applied to the metal in contact with the semiconductor, holes will accumulate at the semiconductor/oxide interface, as shown in **Figure 2.8b**. At this point, charge transport can take place across the interface, and the semiconductor behaves like a metal; this is evidenced by the high currents under forward bias, shown in **Figure 2.7b**. On the other hand, applying a negative bias in **Figure 2.8c** leads to depletion of holes at the semiconductor/oxide interface. In this situation, the current will not flow freely through the depletion region, and lower currents are observed under reverse bias.[134]

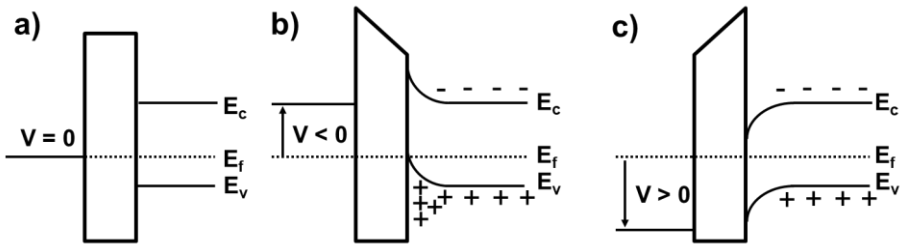

Figure 2.8. MOS band diagram, illustrating the formation of a Schottky junction to explain the rectifying behavior by changes in the distribution of holes (+) and electrons (–) across the semiconductor/oxide interface a) at 0 V, b) when a negative voltage is applied to EGaIn (forward bias) leading to hole accumulation, and c) when a positive voltage is applied to EGaIn (reverse bias), leading to hole depletion at the interface. Adapted from [134].

Using the probing method, described in **Figure 2.7a**, the rectification behavior was examined further after subjecting the above films to the dewetting process, shown in **Figure 2.6**. Given the large variation of Ag coverage at the Ag/p-Si interfaces and the fact that they were probed using a drop of EGaIn (300 ± 100 μm in

diameter), calculating the current density (J) to extract J–V proved to be difficult. Nonetheless, the ultimate purpose of this study is to explore a voltage-induced hysteresis and memory effect. Thus, resistive switching was examined by comparing I–Vs that are representative for each film tested on the same day using the same probing metal (EGaIn) and approximate contact area, and same I–V sweep range and rate). The only variation was the surface morphologies of Ag presented in the series of SEM images in **Figure 2.6**.

Figure 2.9a shows changes in current (arbitrary) under cyclic voltage sweeps between –5 V and +20 V. The 200 nm thick Ag film (yellow trace, continuous and pinhole-free) and Ag-free p-Si surface (dark blue, no Ag film), exhibit a rectifying behavior, with no hysteresis, which substantiates the I–V data in **Figures 2.7b**.

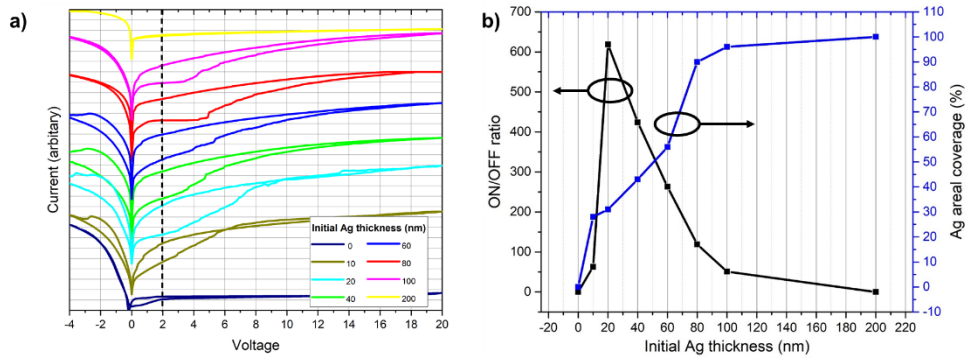

Figure 2.9. a) Transition from a rectifying to hysteretic I–V behavior that was dependent on the initial Ag layer thickness prior to the dewetting process. b) ON/OFF ratio (read at 2 V) derived using the dashed line in the I–Vs in a). Ag areal coverage (%) were extracted using the SEM images shown in Figure 2.6.

In contrast to these devices, the junctions formed over dewetted films exhibited a rectifying behavior, with a visible hysteresis at high positive voltages. At –5 V, junctions initially show a high resistive OFF state and gradually transition to a low resistance ON state under a positive bias, up to +20 V. When the voltage is reversed back to 0 V, these devices remain in the ON state and can be RESET back to the OFF state only when the bias is reversed back to –5 V. **Figure 2.9b** compares the ON/OFF ratio (at 2 V) and Ag surface coverage to the initial Ag film thickness. For a p-Si surface with no Ag layer, there is no hysteresis, which substantiates the rectifying behavior shown for EGaIn/SiO_x/p-Si junctions in **Figure 2.7b**. Upon

inclusion of Ag, an abrupt increase in the ON/OFF ratio, peaking at 600, occurs for films that had an initial thickness of 20 nm. The ON/OFF ratio, however, gradually decreases with increasing Ag surface coverage, until it returns to a rectifying behavior, with no hysteresis for continuous Ag films; this again confirms the data shown for EGaIn/Ag/SiO_x/p-Si junctions in **Figure 2.7b**. These data indicate that the surface coverage of Ag strongly influences the *I–V* hysteresis of these p-Si junctions.

2.3.3 Fabrication and Electrical Characterization of P(VDF-TrFE) Capacitors

To establish a benchmark for polymer processing, thin film capacitors of P(VDF-TrFE) were first fabricated and electrically characterized on Pt-coated Si, as shown in the schematic in **Figure 2.10**.

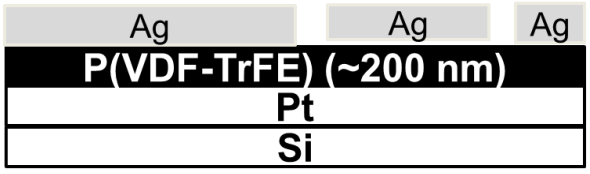

Figure 2.10. Schematic representation of a fabricated ferroelectric capacitor using copolymer P(VDF-TrFE) spun on Pt-coated Si. Circular top contacts of Ag with diameters between 120 and 550 µm were evaporated through a shadow mask to a thickness of 60 nm.

Figures 2.11a-c represent plots from *I–V*, capacitance-frequency (*C–f*), and capacitance-voltage (*C–V*) measurements, respectively. Typically, these electrical characterization techniques are used to characterize the leakage currents and dielectric constant and show the classic butterfly loops in the ferroelectric.[135]

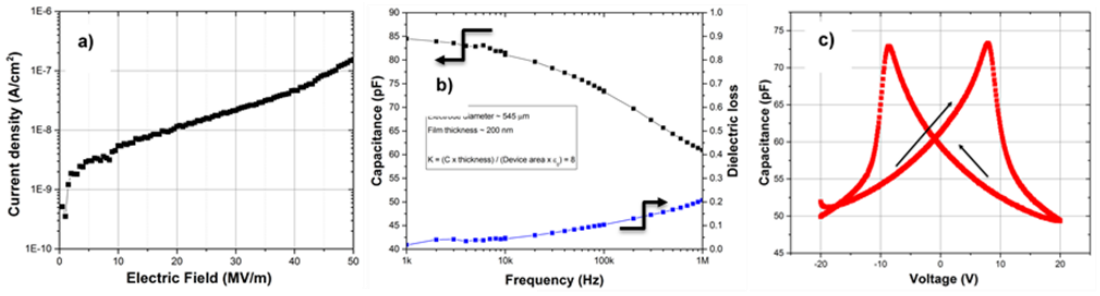

Figure 2.11. a) *I–V* characteristics of P(VDF-TrFE) sandwiched between platinum and silver electrodes after electroforming at 100 MV/m. Polymer film thickness was ~200 nm, b) capacitance–frequency sweep from 1 kHz up to 1 MHz, and c) capacitance–voltage sweep of P(VDF-TrFE). DC: -20 V to 20 V and back. AC signal: 50 mV at 1 MHz.

The thickness of the polymer film was ~200 nm, and the area of the electrode was ~2.3 x 10^{-7} m^2. As shown in **Figure 2.11a**, and after initial poling at 100 MV/m, devices exhibited leakage currents of ~1 x 10^{-7} A/cm^2 at 50 MV/m, which is in line with literature reports using similar electrodes on poled devices.[136]

The relative permittivity (ε_r) is derived from the following relationship:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

where ε_0 is the permittivity of free space [8.854187817 x 10^{-12} $C^2/(N\ m^2)$], ε_r is the relative permittivity of the polymer, A is the area of the device, and d is the thickness pf the polymer layer. From the capacitance measurement in **Figure 2.11b**, ε_r (or dielectric constant, κ) at 1 kHz was calculated to be ~8. Finally, typical ferroelectric switching behavior is observed from the butterfly loop in the capacitance–voltage plot measured at 1 MHz, shown in **Figure 2.11c**. The coercive voltage (V_c), indicated by the peak capacitance in **Figure 2.11c**, occurs around 10 V, translating to a coercive field (E_c) of ~50 MV/m.

Based on these data, processing parameters, such as annealing temperature and time of P(VDF-TrFE) films were fixed to ensure functional and reproducible ferroelectric devices. For the remaining part of this study, the focus will be on fabricating hybrid systems by combining the polymer with Si.

2.3.4 The Role of a Ferroelectric Layer on Current–Voltage Hysteresis

This section describes the addition of a ferroelectric layer of P(VDF-TrFE) over p-type Si surfaces containing dewetted Ag to explore the influence of ferroelectric polarization on charge modulation at the metal/semiconductor. Ag films on p-Si with an initial thickness of 20 nm were selected for further control experiments, as they showed the largest current–voltage hysteresis and ON/OFF ratios. **Figure 2.12a** shows a scheme of the device cross-section. In the SEM image shown in **Figure 2.12b**, some of the polymer was redissolved partially in a methyl ethyl ketone (MEK) solution. The polymer was shown to coat the Si surface and Ag particles conformally, as evidenced by the blurry features in the SEM due to charging effects[137] from the

insulating polymer. In the regions where the polymer was redissolved, the Ag particles were exposed, which improved the sharpness of the image. The AFM topography in **Figure 2.12c** shows that these particles can reach heights of >100 nm, but since the Si base was coated with the polymer, it would be difficult to deduce the maximum height of the particles. Nonetheless, these polymer-coated devices showed low sub-micron surface roughness, which allowed for better data acquisition during C-AFM measurements.

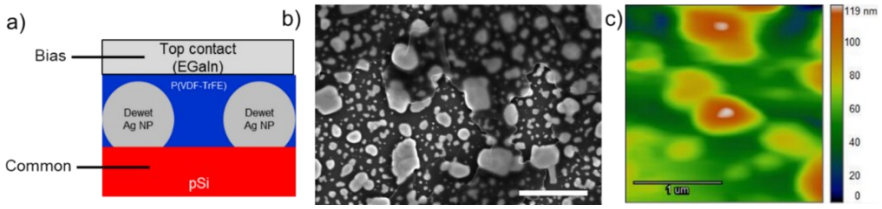

Figure 2.12. a) 2D schematic of devices with dewetted Ag on the surface of p-type Si coated with P(VDF-TrFE) and probed using EGaIn. b) Top view SEM image of the device with partially redissolved polymer. Scale var = 1 µm. c) AFM topography of the device, showing Ag along the elevated regions along the surface (in red).

From the *I–V* plot in **Figure 2.13a**, a large *I–V* hysteresis was observed when a matrix of ferroelectric P(VDF-TrFE) was coated on the surface of Ag/p-Si devices. In **Figure 2.13b**, the retention performance in the ON (SET at 10 V) and OFF (RESET at –5 V) states was examined by stressing each state at 2 V for up to 1000 s. The ON current (~2 µA) slightly increases to 5 µA during the first 50 s, after which it gradually stabilizes back to its initial leakage current. The OFF state current increases continuously from 4 nA and reaches 9 nA after the measured 1000 s. If we extrapolate this behavior over longer periods, it appears that the retention of these devices will diminish over time, and the ON/OFF ratio also would decrease.

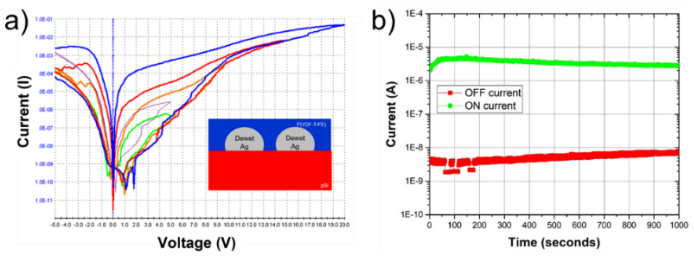

Figure 2.13. a) Enlarged hysteretic loops, showing increasing ON/OFF ratio that is dependent on the magnitude of the final SET voltage. b) Retention characteristics measured up to 1000 s in the OFF and ON states for a device set to a maximum voltage of 10 V.

2.3.5 Conductive Atomic Force Microscopy (C-AFM)

To develop a better understanding on the origin of switching, C-AFM was performed on the surface of devices that showed the largest current–voltage hysteresis. Spatial current variations across the surface of the device were examined by applying a series of scans over time, as indicated by the red arrows in **Figure 2.14**. A platinum tip was used to raster through the entire 2 x 2 μm^2 region during these scans. First, a SET voltage of +10 V was used, followed by a READ voltage of 2 V (**Figure 2.14a, c, and d**). To turn the device back OFF, the region was rescanned at a RESET voltage of –10 V and read again at 2 V (**Figure 2.14b and Figure 2.14d**). The resultant leakage currents took place along the Ag particles and were clearly dependent on the direction of the voltage prior to each READ event.

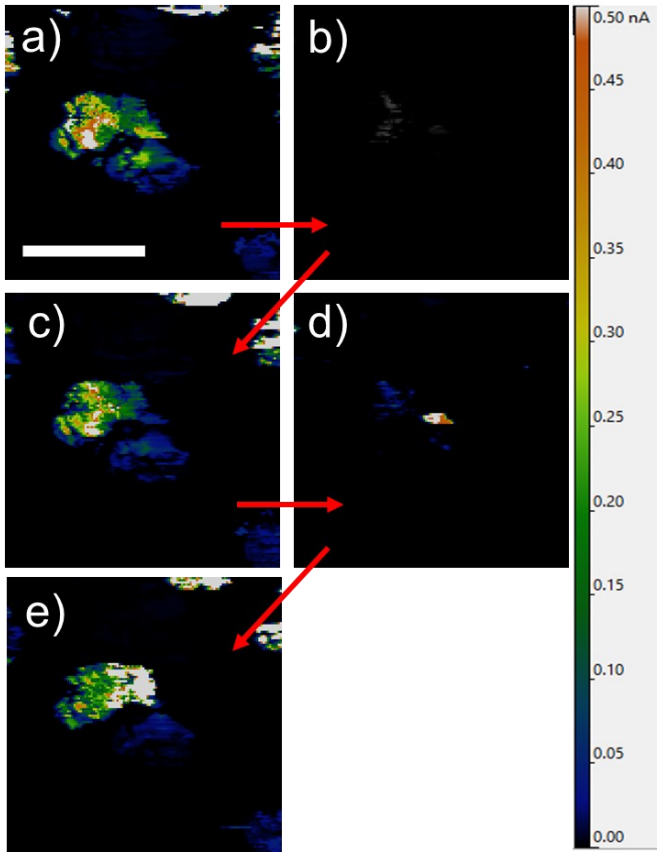

Figure 2.14. Conductive atomic force microscopy on the surface of the device measured in Figure 2.10 probed with a Pt tip. The current profiles in a), c), and e) show the resultant current profiles read at +2 V, after scanning the surface with a tip SET voltage of +10 V. b) and d) show the same surface, also read at +2 V, after being subjected to a RESET voltage of –10 V. The arrows indicate the time series following each SET and RESET event. Scale bar = 1 µm.

2.3.6 Metal-assisted Chemical Etching (MACE): Forming Freestanding Si Nanopillars

In the introduction of this chapter, the concept of fabricating vertically aligned and alternating channels of ferroelectric and semiconducting materials across the two metal contacts to form ferroelectric diodes was described. In such device architectures, illustrated in **Figure 2.1** and **Figure 2.2**, changes in resistance across the semiconducting channel depend on band bending at the metal/semiconductor interface. In this study, Si was chosen as an inorganic semiconductor because the position of the Fermi energy in Si can be tuned, depending on its doping concentration. This allows for a better control over the length of the depletion region and to investigate the role of the ferroelectric material, if any, on band modulation and charge injection across the interfaces. This is achieved by exploring a simple lithography-free approach towards forming vertically aligned Si nanostructures that can ultimately allow for forming our desired device architectures.

Nanostructures derived from silicon, an important material in the current microelectronics industry, have been studied widely as core materials for application in the fields of sensing, optoelectronics[138] as well as energy conversion and storage.[139] Various top-down techniques, such as electrochemical[140] and reactive ion etching,[141] have been employed towards the fabrication of nanostructured Si. One top-down approach, known as metal-assisted chemical etching (MACE), is of particular interest because it has the ability to form a broad range of structures and morphologies such as Si nanowires (SiNWs), porous Si, and Si nanopillars.[139] A scheme of the MACE etching process is shown in **Figure 2.15.**

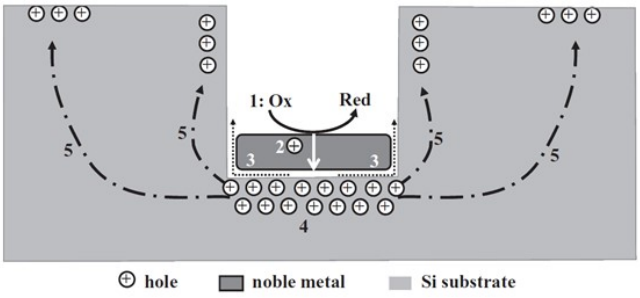

Figure 2.15. Scheme of the different processes that take place during metal-assisted chemical etching. Reprinted with permission from [139]. Copyright © 2011 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

First, a noble metal is deposited to fill the Si surface partially, and the substrate is subjected to an etchant solution made from aqueous hydrofluoric acid (HF) and an oxidizing agent, such as hydrogen peroxide (H_2O_2). Generally, decomposition of hydrogen peroxide is catalyzed at the metal/Si interface (marked **1** in **Figure 2.15**), forms water, and creates holes (marked **2**), which are transferred from the noble metal directly into the Si surface (**Equation 1**):[139]

$$H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+ \quad (1)$$

Enrichment of the Si with holes (marked **3**) then drives its oxidation and, subsequently, reacts with hydrofluoric acid to form hydrogen gas and water-soluble hexafluorosilicic acid (H_2SiF_6) (**Equation 2**):

$$Si + 4h^+ + 6HF \rightarrow SiF_6^{2-} + 6H^+ \quad (2)$$

Since the highest hole concentration is found at the metal/Si interface (marked **4**), the chemical process continues at its highest rate at the interface and leads to anisotropic etching, where the metal sinks into the bulk of the Si substrate. Depending on the doping type and concentration in Si, the generated holes also can diffuse through the outer walls (marked **5**) if the hole consumption at the interface is lower than the hole injection through Si, leading to formation of various morphologies during prolonged side-etching. The etching process leaves an array of patterns that protrude from the surface where Si was not in contact with the metal. MACE has been shown to be applicable across both thin[142] and thick[143] films of the metals.

The etch rate and morphology can be controlled by varying the ratio (ρ) of [HF] and [H_2O_2] in the etchant, where [HF] and [H_2O_2] are the concentrations in moles per liter and $\rho = [HF]/([HF]+[H_2O_2])$.[144] Other parameters, such as the orientation of Si as well as the type and concentration of dopants, also can influence the resultant structure and morphology of the surface. More details regarding the etching mechanisms in MACE can be found in various comprehensive reviews.[139,145]

2.3.7 Optimization of MACE Process and Polymer Coating

Two main parameters that were taken into consideration before testing devices:

1. *The height of the nanostructures:*

The etch time was recorded, and the corresponding pillar height was measured using cross-sectional SEM. Then, the plot of etch depth versus etch time was used to optimize for "ρ", etch rate, and etch time to achieve the desired pillar height. As shown in **Figure 2.16**, dipping the samples in the etchant solution for more than 15 s produced nanostructures with heights >300 nm, which required a thicker polymer layer. Since the polymer has an intrinsically high coercive field (50 MV/m), thicker films will require voltages exceeding 10 V to become polarized. Operating at high voltages is undesired, as it can lead to polymer degradation and dielectric breakdown. Forming pillars below 100 nm was avoided because P(VDF-TrFE) has been shown to exhibit retarded ferroelectric responses at the nanoscale range. To enable consistent and reproducible results, the etch rate and depth was optimized to produce nanostructured patterns with heights between 200–300 nm.

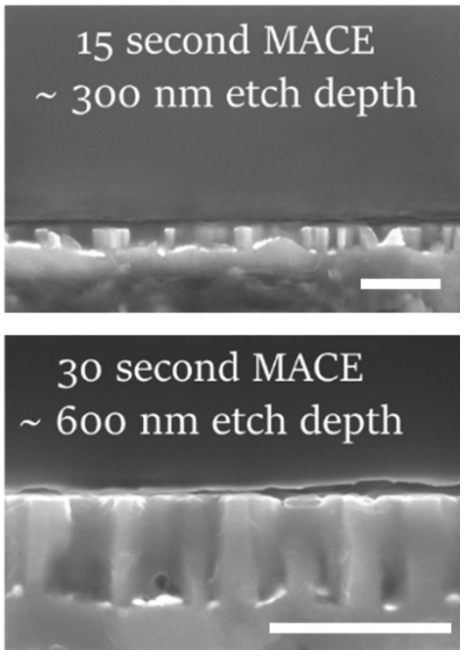

Figure 2.16. Cross-section SEM images, showing time-dependent etch depth of p-Si chips. Initial Ag film thickness, dewetted conditions, and concentration of etchants were fixed.

2. *The thickness of the polymer filling:*

The concentration of the polymer solution and spin speed were chosen carefully to avoid under- or over-filling of the voids. Since the functionality of these ferroelectric diodes depends on the interplay between the semiconductor, ferroelectric, and injecting electrode, this was possibly the biggest challenge in the project, as success requires highly planarized layers of the Si with the polymer. How this issue affected our results will be discussed in more detail in the proceeding section.

2.3.8 Approaches for Conformal Etching

The chips were suspended in the center of a Teflon beaker while stirring the solution. This orientation ensured homogenous etching throughout the surface by improving the diffusion of the agents and by-products across the interfaces of the dewetted samples, as shown in **Figure 2.17**.

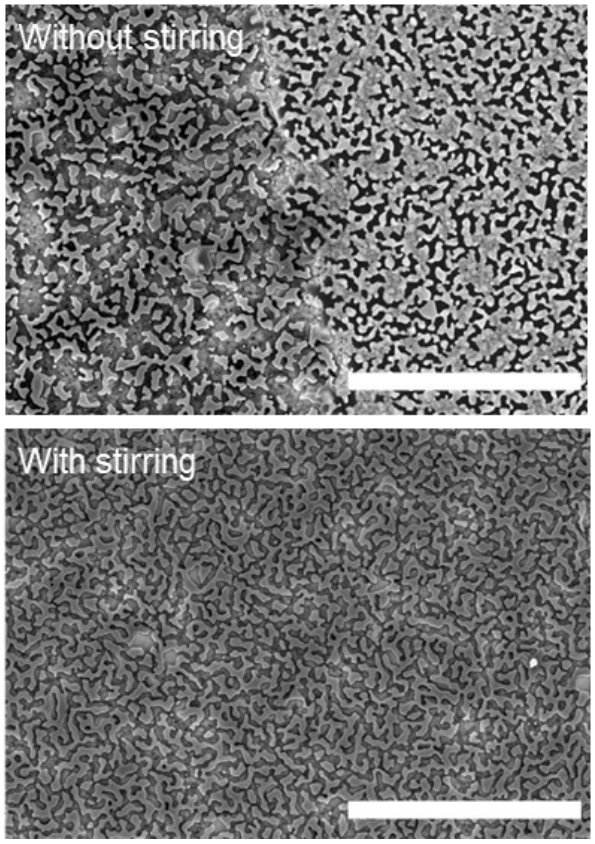

Figure 2.17. Top view SEM images for films that were etched, with and without stirring. Without stirring, some regions remained unetched (shown to the right side of the SEM image). Stirring during the MACE process promoted uniform etching across the surface of the chips.

2.4 Results and Discussion

Based on the conditions identified in the previous sections, the initial Ag thickness and dewetting time were examined such that a percolating network of the metal is formed. All Si wafers were diced into small 1 x 1 cm^2 chips and piranha-cleaned before depositing 20 nm of Ag by RF sputtering (deposition rate ~0.4 Å/s). To dewet the metal films and form the desired percolating structures, the sputtered Ag films were heated over a hotplate at 150 °C for 60 s in air. The structure of the dewetted films of Ag on p-Si are shown in **Figure 2.18a**.

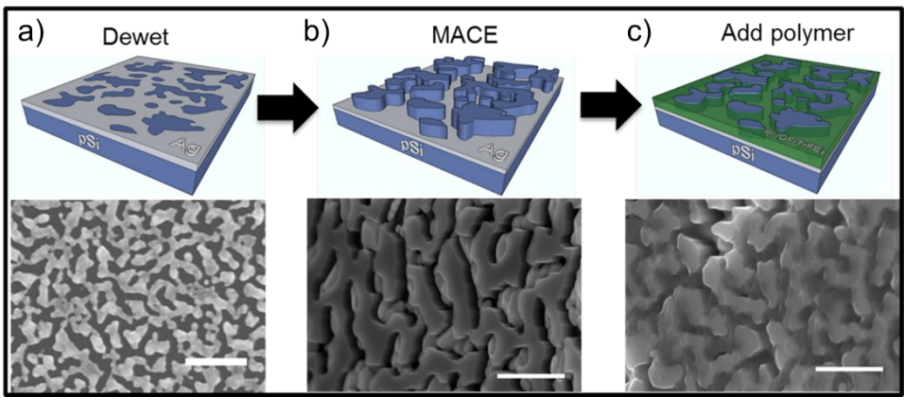

Figure 2.18. 3D schemes, showing the processing steps of hybrid ferroelectric diodes. a) A 20 nm-thick layer of Ag on p-Si was first dewetted, followed by b) MACE, and finally c) filling of voids with a ferroelectric polymer. Directly below each scheme are the corresponding SEM images observed following each process step. All scale bars = 500 nm.

The dewetted films were immersed for 10–15 s into a MACE solution composed of 5.4 M (aq) HF and 0.18 M (aq) H_2O_2, as described in the literature.[146] Preferential etching at the metal/Si interface (indicated by the white arrows) yielded protruding Si structures, with percolating Ag at the base of the chip, as shown in **Figure 2.18b**. Then, the voids were filled by spinning P(VDF-TrFE) from solution at 6000 rpm for 60 s, resulting in the structure shown in **Figure 2.18c.**

After optimizing for the desired structures, memory devices were fabricated successfully, as shown in **Figure 2.19**. From the 3D schematic, we show Ag (in gray) used for the MACE process, which sunk to the base of the Si substrate (in blue), leaving unetched pillars, with random structures protruding through the surface. Then, the polymer (in green) was spun over the Si substrate chips to fill the voids. In the

final step, circular top Ag electrodes (diameters ~300 μm), were RF sputtered through a shadow mask.

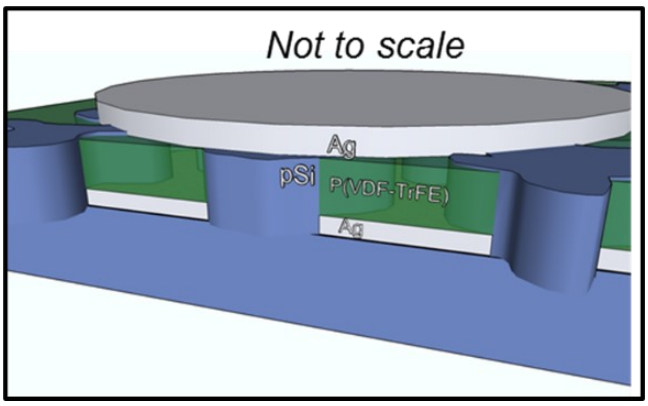

Figure 2.19. 3D cross-section schematic of the final device structure after optimizing the Ag film thickness, dewet conditions, and MACE process, followed by deposition of 60 nm Ag as a top electrode using a shadow mask.

Measurements of *I–V* were the primary technique used to characterize and assess the performance of devices. The bottom contact was grounded and probed by dissolving the polymer and contacting the percolating Ag. The top working electrode was probed using a tungsten needle.

Figure 2.20 shows representative *I–V* behavior upon sweeping the junction from –20 V to +20 V and then back to –20 V. During the initial sweep from –20 V to +20 V (arrows 1 and 2), a rectifying behavior with lower currents under positive voltages was observed. The leakage current along arrow 2 increased, until reaching the compliance current set by the tool (I_{cc} = 10 mA). When the junction was swept back to 0 V (arrow 3), a hysteresis was observed, showing an ON/OFF current ratio reaching over two orders of magnitude (at 2.5 V). When the bias was swept from 0 V back to –20 V (arrow 4), the rectification behavior was reversed, this time showing a blocking behavior at negative voltages. This switching behavior was reversible and stable after at least 10 cyclic sweeps.

This bistable resistive switching behavior mimics the type of switching observed in all-polymer ferroelectric diodes reported in the literature. The origin of the *I–V* hysteresis initially was suspected to be governed by interfacial-type switching, where changes in resistance at the metal/semiconductor interface were mainly due

polarization of the polymer, i.e., dipoles from the polarization state of P(VDF-TrFE) bend the bands at the Ag and p-type Si interface and modulate charge injection. However, care must be taken when interpreting the physical phenomena that drive the changes in resistance because several factors, such as the role of the semiconducting substrate, electrodes, and defects, also can contribute to the mechanism of resistive switching.

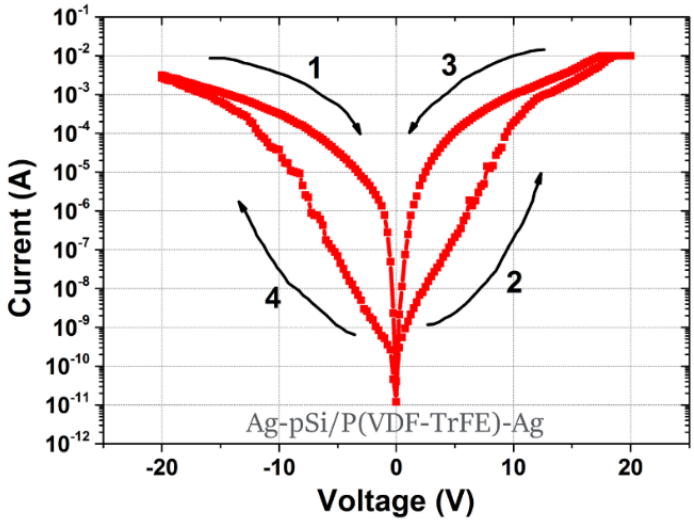

Figure 2.20. a) *I–V* characteristics of P(VDF-TrFE) sandwiched between platinum and silver electrodes. Polymer film thickness is ~200 nm, b) capacitance–frequency sweep from 1 kHz up to 1 MHz, and c) CV sweep of P(VDF-TrFE). DC: ─20 V to 20 V and back. AC signal: 50 mV at 1 MHz.

The data in **Figure 2.7b** shows that Ag/p-Si junctions will form a rectifying Schottky diode. In the hybrid system, the bottom and top Ag contacts were positioned between the polymer and patterned p-Si to form the structure shown in the inside of the dashed red line in **Figure 2.21,** i.e., forming two back-to-back Schottky diodes. Thus, this cannot conclude that the rectification behavior, shown in the *I–V* plot in **Figure 2.20,** is only due to polarization-induced charge blocking and injection at the Ag/p-Si interface.

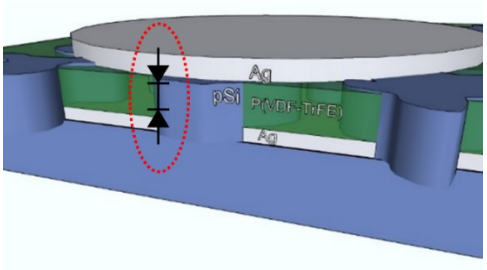

Figure 2.21. Depiction of two back-to-back Schottky diodes formed between the top and bottom Ag contacts.

Silver, with high diffusivity in Si, and was shown to contribute to the observed *I–V* hysteresis in our junctions. In ECM-type memory, Ag is a typical material of choice for active electrodes in nanoionics and readily diffuses through solid oxide electrolytes to form/rupture filaments that lead to changes in resistance. This will be discussed in more detail in Chapter 4 that covers redox-based resistive switching across oxide electrolytes. As such, and with the presence of MOS junctions, decoupling the role of the ferroelectric polymer and doping metals (such as Ga or Ag) on the hysteretic behavior would be incredibly challenging.

Based on the data in **Figure 2.13a**, although the presence of the ferroelectric layer across single Schottky junctions (ohmic ground) has been shown to enhance the *I–V* hysteresis and exhibit large ON/OFF ratios relative to polymer-free junctions, interfacial polarization cannot be assumed to be the only contributor to the observed *I–V* hysteresis. Studies have shown that charge traps in Si due to defects such as dislocations or surface/interfacial states can induce ferroelectric-like hysteresis loops in non-ferroelectric systems.[147] This is especially true for systems involving thin films or nanoscale structures.[148]

2.5 Conclusions

In summary, resistive switching in a hybrid system of ferroelectric polymer P(VDF-TrFE) and p-type Si was explored. A metal-assisted chemical etching technique was used to pattern surfaces on Si and fabricate free standing nanostructures on the surface of Si. The depressed metal used to catalyze the etching process in Si was used as a bottom contact, followed by filling of voids by spinning the ferroelectric polymer from solution. The top contact to the hybrid structures was made using EGaIn and Ag

electrodes. The *I–V* characterization of these devices revealed different modes to resistive switching depending on how these devices were probed:

1. With an ohmic junction to the bottom electrode (scratched with EGaIn) and Schottky junction to the top electrode (Ag or soft contact with EGaIn), typical ECM bipolar switching was observed (i.e., ON or OFF current transitions take place at opposite polarities greater than 0 V). This switching mode can be explained by electrochemical redox processes of the Ag or Ga metals at the oxide and/or Si interface, which will be discussed in more detail in Chapter 4.
2. With Schottky junctions at both the top electrode (Ag or soft contact with EGaIn) and bottom electrode (Ag), the mode of switching changed to reversible diode rectification that was dependent on the direction of the poling voltage. This is explained by the formation of two back-to-back Schottky diodes between the bottom MACE Ag and top sputtered Ag.

2.6 Experimental Section

Fabrication of ferroelectric capacitors:

Device fabrication: The polymer, P(VDF-TrFE) (FC30 70/30% mol), was purchased from Piezotech (www.piezotech.eu). A 3 wt% polymer solution was prepared using methyl ethyl ketone (MEK) as the solvent. Bottom contacts were prepared by sputtering 5 nm of Ti on Si (p-type, (100), 5–10 Ω cm) capped with 100 nm of SiO_2, followed by sputtering of 25 nm of the top Pt layer. Films were spun at 6000 rpm for 60 s under ambient conditions to give film thicknesses of ~200 nm (±20 nm), as measured by an Alpha-step profilometer. Then, the films were baked on a hotplate at 80 °C for 30 min, followed by vacuum annealing at 135 °C for 4 h. Top circular Ag electrodes (diameter ~550 μm and 70 nm in thickness) were evaporated over the samples using a shadow mask for electrical characterization.

Silver dewetting on Si:

Substrate treatment: Si wafers (p-type (boron), <111>, 1–10 Ω.cm p-type) were diced (1 × 1 cm^2) and cleaned in a piranha solution (3:1 H_2SO_4:H_2O_2) for 15 min. (**Caution**! Piranha reacts violently with organics and should not be used without proper safety precautions.)

Metal deposition: Various thicknesses of Ag (10–200 nm), depending on the experiment, were deposited onto treated Si substrates using RF sputtering (deposition rate ~0.2–0.4 Å/s). To dewet the metal films and form the desired thickness-dependent structures, the sputtered Ag films were heated over a hotplate at 150 °C for 60 s in air or 135 °C for 10 s in vacuum, where specified.

Particle lithography using polystyrene (PS) beads: PS beads (diameter ~0.42 μm), purchased from Bangs Laboratories (Lot# 11077), were diluted first to 1% w/v and cetrifuged at 14,000 rpm for 15 min to remove the surfactant. Then, the particles were decanted after centrifugation, and 0.5 mL of DI water were added, followed by vortex mixing and sonication for 10 min. Next, 100 μL of the dispersion were dispensed onto 1 × 1 cm^2 Si chips at 1750 rpm for 60 s (acceleration was set to 600 rpm/s), and the beads were plasma etched in air (450 mTorr at 12 W) for 10 min to reduce the bead diameters by ~50%. After shrinking the beads, 20 nm of Au was evaporated, and the beads were removed using dicholoromethane (DCM). The chips were then ready for the MACE process.

Metal-assisted chemical etching: Si chips loaded with as-sputtered or dewetted Ag (or Au, where particle lithography was used) were suspended onto a 100 mL of a standard solution consisting of 5.4 M (aq) HF and 0.18 M (aq) H_2O_2 at room temperature and with stirring. The concentration ratio of HF and H_2O_2 was fixed, unless specified otherwise for etch rate studies. The etch time was varied depending on the desired etch depth. Two beakers containing DI water were used to dilute the immediately after the etching process.

Electrical characterization:

Current–voltage, capacitance-frequency (1 kHz to 1 MHz, AC signal 50 mV), and capacitance–voltage (at a fixed frequency of 1 MHz and AC signal of 50 mV) measurements were conducted using a Keithley 4200 semiconductor characterization system. C-AFM characterization (Asylum MFP-3D AFM) was conducted under ambient conditions using Pt tips. Unless otherwise specified, the bottom of all chips was scratched with EGaIn and covered with Cu tape to ensure Ohmic contacts to the grounded terminal.

CHAPTER 3[1]: UV‑Induced Ferroelectric Phase Transformation in PVDF Thin Films

3.1 Introduction

A rewritable and non-volatile memory component that can be used to store and retrieve information on demand is an essential component of the suite of printed organic electronics.[149–151] Organic ferroelectrics are promising candidates since they exhibit bistable and switchable remnant polarization and can be processed into thin films from solution.[152] However, high temperature stability and low operating voltages are key challenges that still need to be addressed. In general, high Curie temperature ferroelectrics exhibit more stable remnant polarizations at elevated temperatures. This characteristic gives polyvinylidene fluoride (PVDF) an advantage over its higher cost co-polymer relative, P(VDF-TrFE).[153] Conversely, given the high coercive field intrinsic to PVDF, fabrication of ultra-thin films is essential to achieving low voltage operation of this polymer.[154] These thin films must be dense, smooth, and contain the correct ferroelectric crystalline phases.[155] However, unlike the copolymer P(VDF-TrFE), the processing of PVDF to produce these thin films is problematic. Stringent processing conditions, summarized in section 1.4.3, are necessary to transform the paraelectric α-phase of PVDF to the desirable ferroelectric β, γ, or δ polymorphs.

Several reports have demonstrated robust ferroelectric devices, based on semicrystalline PVDF in the ferroelectric phases, induced either via mechanical stretching,[156–158] electro-forming,[155,159–162] controlled thermal annealing,[163–167] or by including additives.[168–170] Stress-induced α- to β- phase transition in PVDF films by mechanical stretching is applicable only to thick films, rendering it an impractical route for thin films that can operate at low voltages. Likewise, additives such as clays, carbon nanotubes, graphene, or polymers like polymethylmethacrylate are known to

[1] The contents of this chapter have been copied and/or adapted from the following publication: M. N. Almadhoun, M. A. Khan, K. Rajab, J. H. Park, J. M. Buriak, H. N. Alshareef *Adv. Electron Mater.* ***2019****,* 5*,* 1800363.

promote β-phase crystallization; these additives limit, however, the minimum achievable thickness and increase surface roughness of such films due to limited solubility with PVDF. To counter such problems, controlled annealing of PVDF thin films from melts using multi-step heating and cooling can increase the content of the crystalline ferroelectric phases.[168] These processing conditions are time consuming and require annealing temperatures as high as 180 ºC.

More recently, studies by Mengyuan *et al.* successfully demonstrated that ultra-thin PVDF films (down to 10 nm) in the α-phase transforms to the δ polymorph when poled in high electric fields, resulting in the observation of ferroelectric behavior. These films were cast by spinning or doctor blading PVDF from solution under controlled humidity and/or at elevated substrate temperatures.[155,162]

Here, a technique that uses a very short exposure to light (less than a millisecond), resulting in the transformation of the α-phase of PVDF to the ferroelectric β-phase is demonstrated, as depicted in **Figure 3.1**. Compared to the rates and modes of energy transfer found in conventional ovens and rapid photothermal processing, this technique can result in energy transfer in hundreds of microseconds.[171] At such time scales and depending on the optical properties of the absorbing material(s), phase transitions can be induced and quenched before chemical degradation can occur during longer exposures to light, especially in the UV range ($\lambda < 300$ nm).

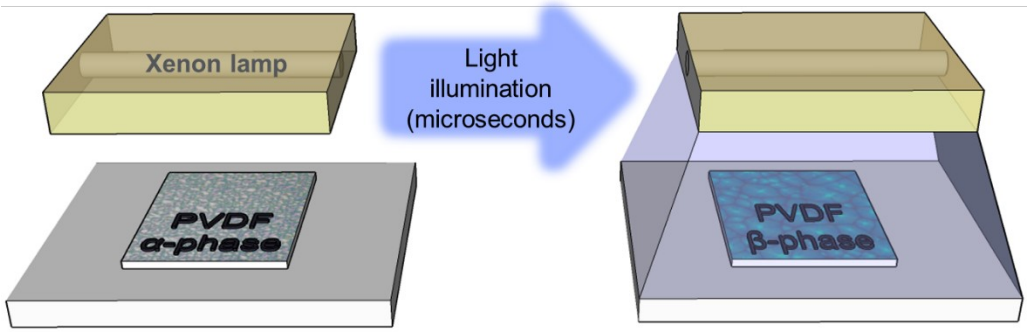

Figure 3.1. Schematic representation of the UV-annealing process of PVDF thin films promoting transformation from paraelectric α- to the ferroelectric β-phase.

3.2 Results and Discussion

Multiple PVDF thin films, ~200 nm in thickness, were spin-coated onto platinum-coated silicon substrates and then exposed to broad spectrum light (λ ~ 200–1200 nm) of different intensities using a xenon lamp source. The duration of the pulses was modulated, holding the distance of the sample from the lamp fixed. The relative energy of the photons striking the surface per unit area was determined using a bolometer. **Figure 3.2a** shows the hysteresis loops of different PVDF films photoannealed at different pulse lengths. Similar to the behavior of the as-spun samples, a pulse length of 200 μs did not induce any observable ferroelectric properties. However, typical characteristics of dipolar and reversible hysteresis loops begin to appear at a pulse length of 250 μs and higher, reaching a maximum P_r of 5.4 μC/cm^2 and a coercive field around 120 MV/m at 350 μs. A further increase of pulse length to 400 μs leads to a drop in the remnant polarization to about 4.5 μC/cm^2. Prolonged pulses of 400 μs and above lead to low device yield, possibly due to polymer degradation and an increase in leakage currents.

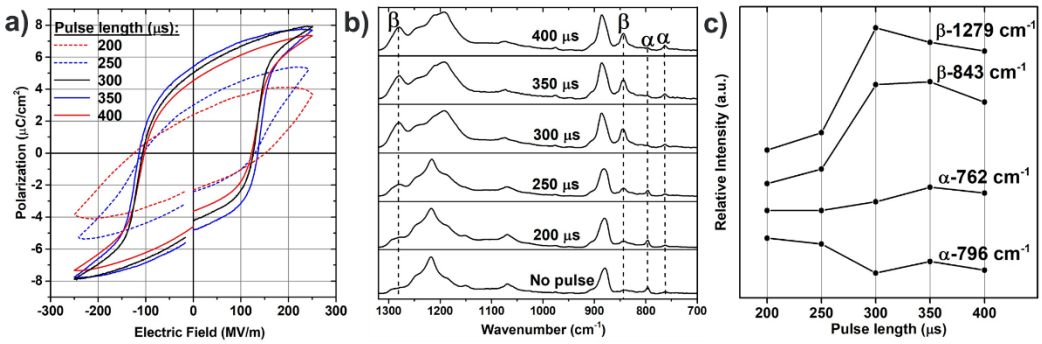

Figure 3.2. a) Ferroelectric hysteresis loops, with maximum remnant polarization obtained at an electric field of 250 MV/m and a frequency of 10 Hz following different pulse lengths. b) Normalized FTIR spectra of thin PVDF films annealed using different photonic pulse lengths. c) Relative change in peak intensities of the α-, β-, and β/γ- phases as a function of pulse length. The maximum content of the ferroelectric phase is reached at a 300 μs photonic pulse.

FTIR was used as a diagnostic tool to determine the phase(s) present in PVDF. **Figure 3.2b** shows the FTIR spectra of PVDF films that have been exposed to different pulse lengths of light. As expected, the peak positions of untreated PVDF films (no light pulse) predominantly appear in the non-ferroelectric α-phase.[172] With pulse lengths above 250 μs, the intensity of the α-phase peak at 1218 cm^{-1} diminishes,

red shifts, and broadens, suggesting a phase change within the PVDF. The feature at 843 cm^{-1}, assigned to CH2 rocking in the ferroelectric β-and/or γ-phases, appears in the PVDF films that are exposed to light. To distinguish between these ferroelectric phases, the peak at 1279 cm^{-1} assigned to TTT CF2 vibrations, also appears under light illumination, confirming the formation of the TTTT conformation characteristic of the β-phase.[173,174] The intensity of these peaks increases with longer pulse lengths, indicating gradual formation of the ferroelectric polymorphs. After normalizing all spectra, we plotted the relative peak intensities that are characteristic of the α- and β-phases, as shown in **Figure 3.2c**. A sharp increase in peak intensities at 843 and 1279 cm^{-1}, associated with the ferroelectric phases, are observed above 250 μs of illumination, accompanied with a sharp rise in the remnant polarization, as shown in **Figure 3.2a**.

It is clear that there is a direct link between the length of the photonic pulse and induction of ferroelectric phases in PVDF. From the UV-Vis spectrum in **Figure 3.3a**, and given that the band gap of PVDF is around 6 eV, the bulk photoabsorption of PVDF takes place in the UV range ($\lambda < 350$ nm).[175] To determine if the UV portion of the spectrum was the main driving force for the observed phase change, wavelengths below 350 nm were excluded through the use of a ceria-doped tube, as shown in **Figure 3.3b**. Since long-pass UV filtering is expected to lower the total delivered photonic energy per unit area, the influence of shot energies on the remnant polarization was determined.

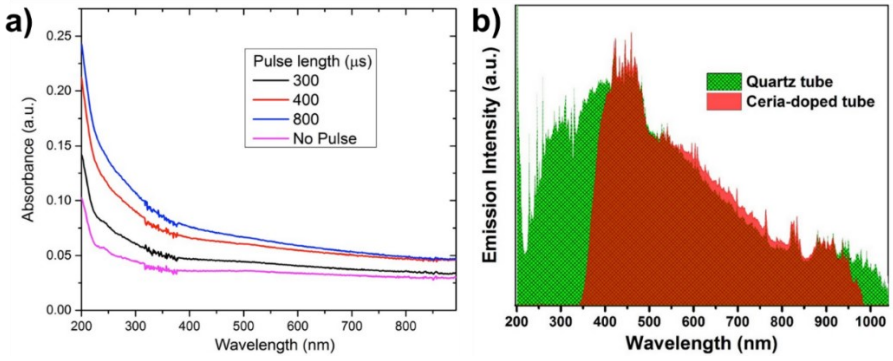

Figure 3.3. a) UV-vis of PVDF films spun on quartz glass after exposure to different pulse durations, showing absorptions in the UV range b) The photoemission spectra from the xenon lamp with UV (quartz tube) and without UV (ceria-doped tube). Photoemissions data reproduced with permission from Novacentrix®.[176]

From **Figure 3.4a**, a pulse length of 300 μs, equivalent to a shot energy of ~5 J/cm^2 with UV light, induced a sharp rise in P_r to ~5 μC/cm^2. However, under UV-filtered pulsed irradiation, there was no sign of ferroelectric switching, even after reaching an equivalent shot energy of ~5 J/cm^2 at a pulse length of 400 μs. **Figure 3.4b** shows that the relative shot energy level changes as a function of pulse length.

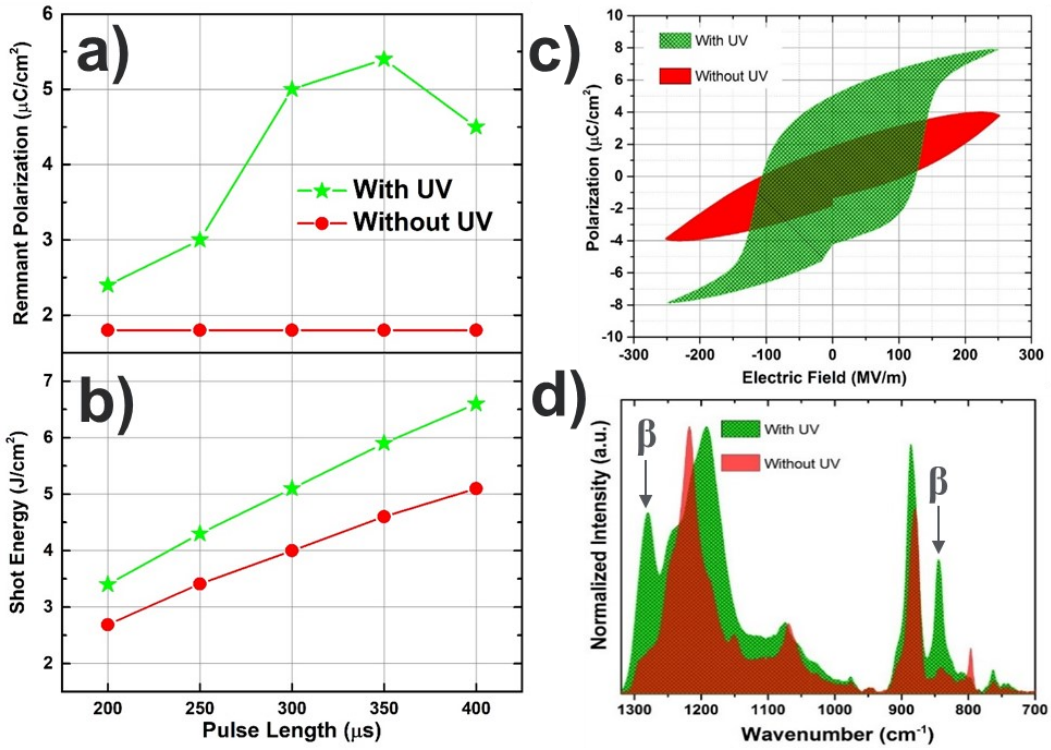

Figure 3.4. a) Changes in the remnant polarization of PVDF as a function of pulse length, with and without UV. b) Relative shot energy for each pulse length, as measured by the bolometer. c) Ferroelectric hysteresis loops of a PVDF film that was exposed initially to a single pulse of 5 J/cm^2 without UV, followed by another pulse of 5 J/cm^2 with sub-350-nm UV light, measured at 250 MV/m at 10 Hz and d) corresponding FTIR spectra of the film before and after inclusion of the UV light.

Figure 3.4c compares the ferroelectric loops of one PVDF film that initially was exposed to a shot energy of ~5 J/cm^2 without UV, followed by another pulse with the inclusion of sub-350-nm UV light. Ferroelectric hysteresis was observed only in the sample after it was exposed to the UV light. FTIR spectra of the film following photonic pulses with and without sub-350-nm UV light, **Figure 3.4d**, clearly reveal how the ferroelectric peaks at 843 and 1279 cm^{-1} are absent when the shorter

wavelengths of UV light are excluded. The FTIR spectra for all samples in which the UV-excluding cerium-doped tube was used were identical to that of untreated PVDF films.

Next, the microstructure of PVDF spherulites upon exposure to a pulsed irradiation of 5 J/cm^2 was examined again, with and without UV contribution. Under polarized light, we observed Maltese cross features around impinged PVDF spherulites for the samples that were not exposed to the sub-350-nm UV light (**Figure 3.5c**, left side). The appearance of the Maltese cross features indicates the presence of optically anisotropic crystallites typical of the α-phase, corroborating the FTIR data in **Figure 3.4d**.[172,177] The Maltese cross features completely disappear in films that were exposed to the sub-350-nm UV light, as shown in **Figure 3.5b**. The absence of these patterns upon UV irradiation indicates that the films have transformed preferentially to the ferroelectric β-phase over other ferroelectric phases.[178,179] **Figure 3.5c** shows a PVDF film that was masked partially from the incident pulse irradiation. As expected, the birefringence disappeared only in the region that was directly exposed to UV light.

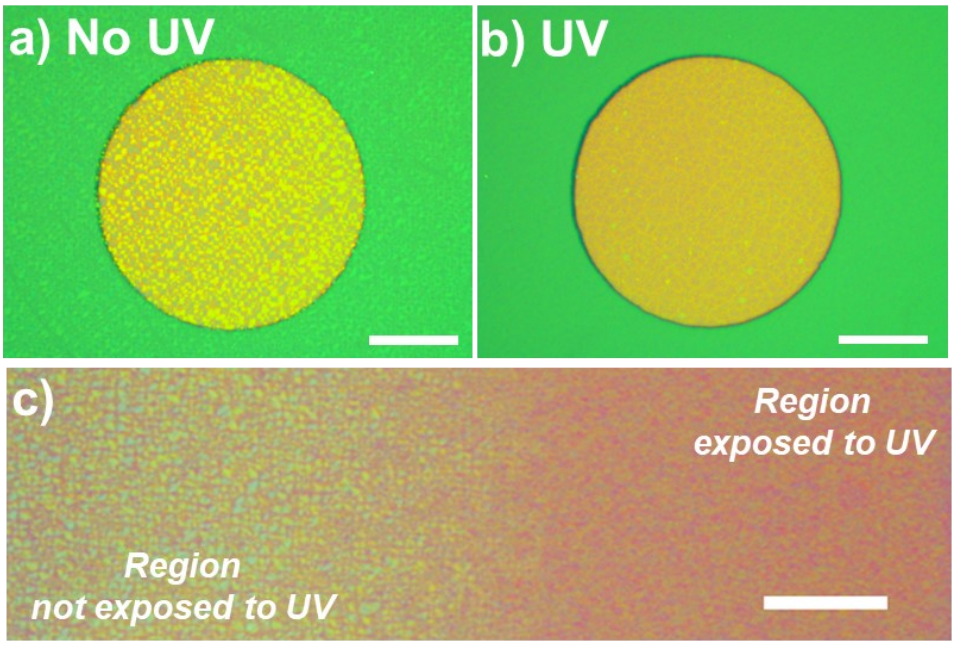

Figure 3.5. Analysis of the PVDF film microstructure: a) Polarized optical micrographs revealing interference patterns around PVDF spherulites. b) Absence of interference patterns upon exposure to UV irradiation. For better contrast, images were taken around the top Au electrodes. c) A partially masked PVDF thin film subjected to a single pulse without filtering UV. The Maltese cross patterns gradually disappear around the regions exposed to UV to the right. All scale bars are 100 μm.

After exposing the same sample to sub-350-nm UV light, it is evident that no further grain growth occurred, as the grain size and film microstructure remained unchanged, as shown by optical microscopy and scanning electron microscopy (SEM) images before and after exposure to the light pulses in **Figure 3.6**.

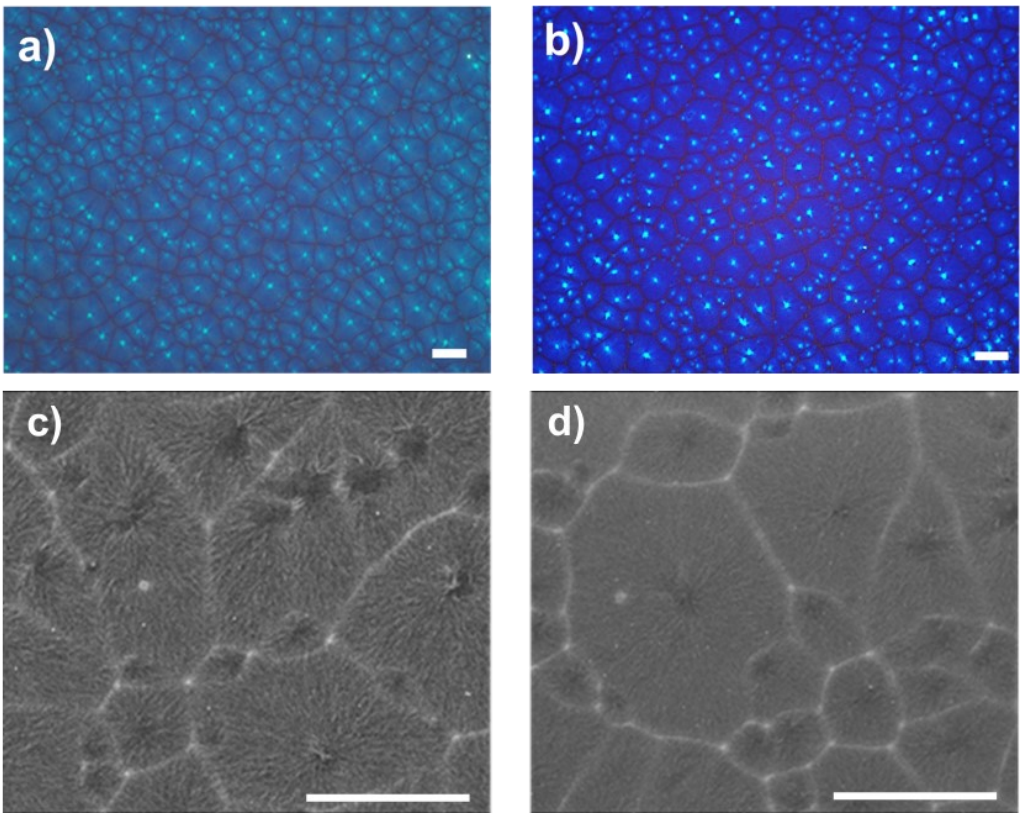

Figure 3.6. Microstructure of PVDF, as viewed under an optical microscope a) before and b) after exposure to sub-350-nm UV light. SEM images of as-spun PVDF c) before and d) after exposure to light. All scale bars are 10 μm.

Finally, we take a closer look at the spherulites using atomic force microscopy (AFM). From **Figure 3.7a**, as-spun PVDF shows typical lamellar sheets that protrude outwards from their nucleation centers until they impinge upon other dendritic lamella from neighboring crystals. Local PVDF lamellae showed a pronounced change in surface roughness after exposure to UV irradiation, shown in **Figure 3.7b**, primarily due to diminished dendrites in the spherulite structure. The roughness, as clearly shown by the 3D topography images and **Figure 3.8**, decreased from a RMS of 15.1 nm to 7.6 nm, indicating topological transformation of the lamella, impacted directly by the incident irradiation on the upper surface of the polymer. Similarly, a

considerable decrease in contrast in the corresponding phase images upon UV exposure, shown in **Figure 3.7c** and **Figure 3.7d**, further suggests reduced variations in local PVDF polymorphs. The transition from dendritic to plain spherulite morphologies reflects local reorientation of PVDF crystals, attributed to the formation of the ferroelectric phases.[180] Microsecond photothermal energy transfer is essential to inducing the ferroelectric phase as well as in reducing the surface roughness of PVDF without causing damaging effects through prolonged exposure to light.

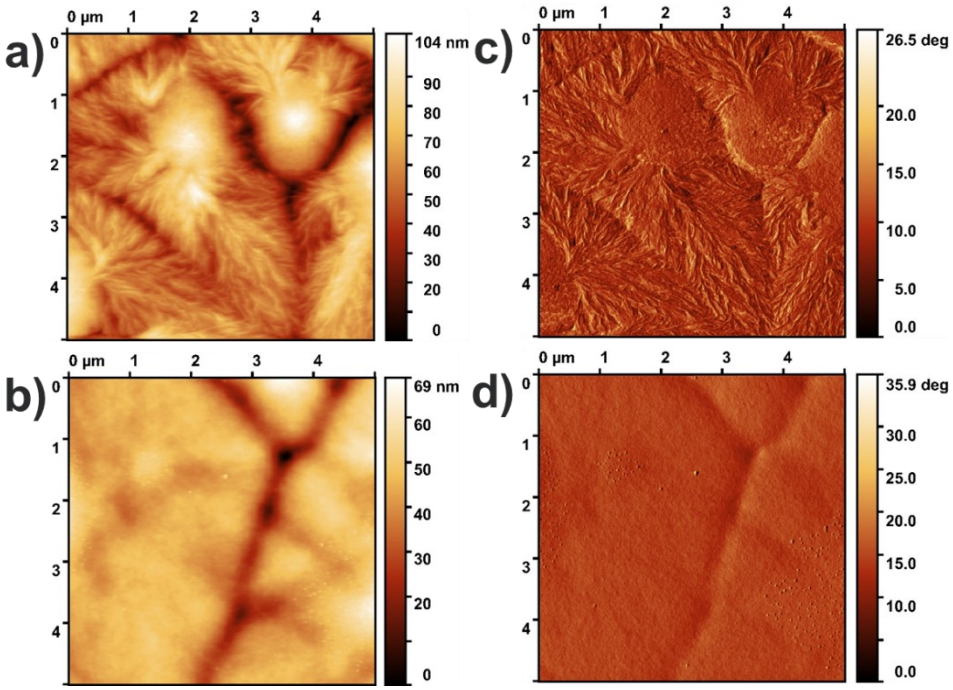

Figure 3.7. AFM a) height and c) phase images of as-spun PVDF thin films. AFM b) height and d) phase images after exposure to UV irradiation.

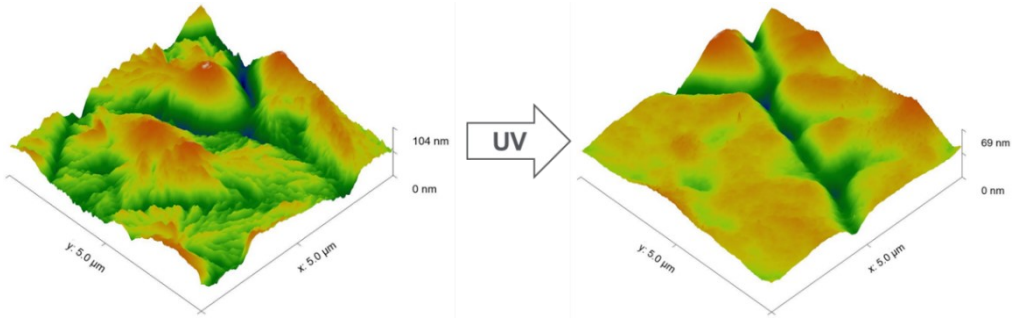

Figure 3.8. 3D AFM topography images from Figure 6, clearly showing spherulites with depressed and smoothened lamella upon UV exposure.

Finally, thermal simulation measurements were conducted to investigate the influence of pulse duration on PVDF phase transformation. In principle, light to heat energy conversion will depend on the optical properties of the materials in the device stack. If we account for the PVDF layer only, as shown in Figure 3.3, the absorption band is highest near the UV region ($\lambda \sim 200$). As such, heat due to thermal relaxation associated with this absorption band, which is related to electronic transitions that originate from unsaturated C=C bonds ($\pi \rightarrow \pi^*$) and C-F bonds ($n \rightarrow \pi^*$) in the polymer.[181] More details of the simulation models used in the software are described elsewhere.[182,183] **Figure 3.9** shows three temperature profiles across different depths as a function of pulse time. A sharp rise in temperature from 25 °C to a maximum of ~390 °C is reached at a pulse length of 400 μs. The highest temperatures, in red, are distributed over the bulk of the uppermost device stack (**Figure 3.9**, inset, not to scale). After absorbing ~6% of the energy, the yellow line shows the approximate temperature experienced at the interface between the silicon substrate and the oxide. The bulk of the silicon substrate absorbs and dissociates most of the remaining heat, with a base temperature shown in green.

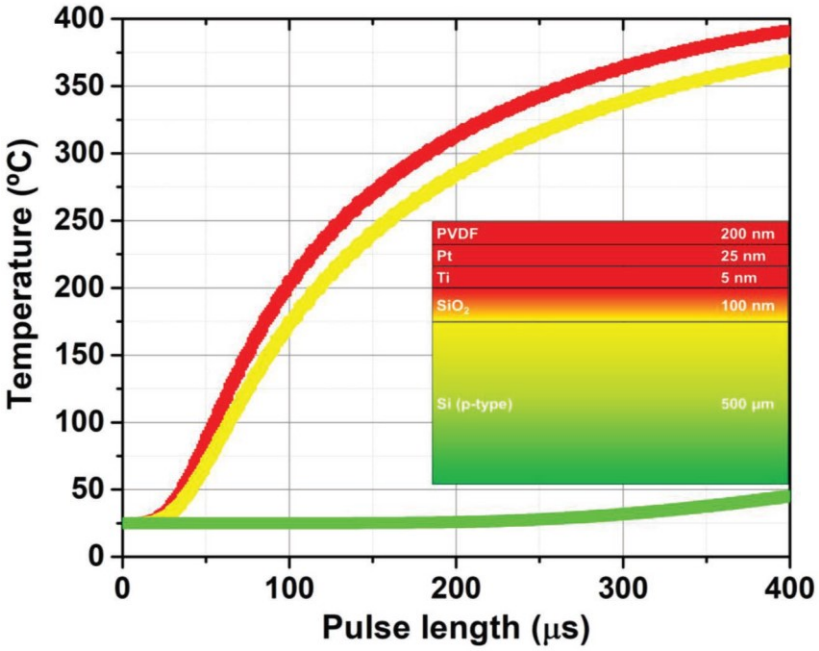

Figure 3.9. Temperature variation as a function of pulse length extracted from thermal simulation. Inset: Device stack, showing distribution of heat with depth.

It is evident from the simulation that thermal quenching in the microsecond regime, reaching temperatures above the melting temperature of PVDF (T_m ~ 170 °C), provides sufficient energy to induce local chain restructuring of PVDF crystallites before the onset of melting and regrowth of the grains. Although similar phase transformations have been demonstrated previously using rapid thermal annealing, defects formed by grain restructuring would be detrimental to film smoothness, which is an important parameter for electronic devices.[167]

3.3 Conclusions

A rapid photonic annealing technique has been developed to induce rapid phase transformation of PVDF films from the non-ferroelectric α-phase to the ferroelectric β-phase, without the need for thermal treatment. Within the thickness range of the films in this study, optimizing the photonic annealing conditions (300–400 μs pulse lengths) resulted in a remnant polarization up to 5.4 μC/cm^2 and a coercive field of around 120 MV/m. The annealing process can be extended to thin films toward a robust polymeric memory operation. Understanding the underlying mechanism of phase transformation by photoabsorption will be the subject of future work.

3.4 Experimental Section

Device fabrication: The polymer, PVDF (average M_w ~534,000), was purchased from Sigma-Aldrich. A 5 wt% polymer solution was prepared using dimethylformamide (DMF) as the solvent. Bottom contacts were prepared by sputtering Pt (25 nm)/Ti (5 nm) on SiO_2 (100 nm)/silicon (p-type, (100), 5–10 Ω cm). All films were spun at 4000 rpm for 60 s under ambient conditions, yielding a film thickness of ~200 nm (±20 nm), as measured by a Dektak profilometer. After exposure to light (described in next section), 60 nm top Au electrodes were evaporated over the samples using a shadow mask for electrical characterization.

Photonic annealing: A PulseForge 1300 photonic curing tool[176] was used to flash the polymer films. For consistency, each sample was placed in the area exposed to uniform radiation and at a fixed distance from the lamp (~3 mm). A quartz glass-covered xenon lamp was used to deliver a single pulse to all samples at 800 V. The

pulse length was varied between 200 and 400 μs, which yielded energy densities of ~2.5–6.5 J/cm^2, as measured by a bolometer. To filter out sub-350-nm UV emission, a ceria-doped tube was used to cover the glass lamp.

Electrical Characterization: Polarization-voltage measurements were conducted using a Premium Precision II Ferroelectric tester (Radiant Technologies) at a fixed frequency of 10 Hz.

Fourier Transform Infrared Spectroscopy (FTIR): Attenuated total reflectance Fourier transform Infrared spectroscopy (ATR-FTIR) spectra of the PVDF films spun on Pt were measured using a Nicolet 6700 (Thermo Scientific).

Polarized Optical Microscopy: All images were obtained on a Nikon Eclipse LV150N in bright-field (BF) illumination mode using a 20x objective (TU Plan Fluor - MUE42200). Analyzer and polarizer sliders were combined to enable simplified polarization microscopy adjusted into the crossed Nicols position.

UV-vis Spectroscopy: Absorption spectra of PVDF films spun on quartz were measured using a PerkinElmer Lambda 750 in transmission mode.

Atomic Force Microscopy (AFM): Surface morphology and roughness images were acquired via tapping mode using an MFP-3D from Asylum Research with a Ti-Pt cantilever (NSC18, MikroMasch).

CHAPTER 4[2]: Bipolar Resistive Switching in Junctions of Gallium Oxide and p-type Silicon

4.1 Introduction

The rapid growth of the field of printed and flexible electronics, based in part upon liquid metals, has led to an interest in devices assembled upon a platform of liquid gallium and related alloys due to the negligible toxicity and high conductivity of these materials.[74–78,80–86,184–186] Interesting and useful electronic behavior of these gallium-based liquid metals derives from their oxide interfaces, which can be harnessed for a diverse array of applications, including catalysis, conductive inks in flexible electronics, and substrates for epitaxial growth of 2D materials.[85,187] This work investigates the use of gallium-based metals as mouldable liquids for printed memory by exploiting gallium oxide in conjunction with silicon.

There is currently a strong drive to elucidate new and non-conventional information storage mechanisms that mimic ionic migration found in neuromorphic systems using memristors.[188–190] Memristive systems are essentially resistors with memory that can store information in the form of multiple resistive states, where each state depends on the intrinsic effects of the switching medium and/or extrinsic effects across the interfaces.[191] Based on nonlinear mathematical models, the concept of the memristor was proposed first by Chua in 1971 as the fourth fundamental circuit component.[192] In 2008, Strukov *et al.* were able to demonstrate empirically a pinched *I–V* hysteresis loop that is characteristic of a memristor using TiO_2-based materials.[193] Since then, there has been an explosion in research on memristive devices using various electrolytes and their combinations,[194,195] including but not limited to small molecules,[196] polymers,[197] and other inorganic oxide systems, such as SiO_x,[198–202] NiO_x,[203] HfO_x,[204–206] CeO_x,[207] ZnO_x,[208–210] ZrO_x,[211–213] and CuO_x.[214]

[2] "The contents of this chapter have been copied and/or adapted from the following publication: Almadhoun, M. N.; Speckbacher, M.; Olsen, B. C.; Luber, E. J.; Sayed, S. Y.; Tornow, M.; Buriak, J. M. Bipolar Resistive Switching in Junctions of Gallium Oxide and P-Type Silicon. *Nano Lett.* ***2021***, 21 (6), 2666–2674.

There are two main switching mechanisms in redox-based memristive systems: i) electrochemical metallization memory (ECM), in which redox reactions are driven by mobile cations to form metallic filaments and ii) valence change memory (VCM), where drifting anions form filaments composed of positively charged oxygen vacancies.[195,215–217] After subsequent switching, these filaments partially reoxidize and form a thin active layer, typically a few nanometers in thickness.[216] Memory devices can operate in ECM, VCM, or both, depending on the choice of electrode and electrolyte materials and cell architecture.[218]

Reversible switching, an essential property for rewritable memory, typically is characterized by reactions that lead to stable formation and dissolution of filaments that span the two electrodes. Stochastic filament formation across thick solid electrolytes has issues with reproducibility and long-term stability that hinder large scale deployment of such devices.[219] One strategy that can be used to mitigate filament formation is to develop nanoscale electrolytes. However, high electric fields across thin films often lead to irreversible damage to oxide electrolytes.[220–222]

Gallium oxide, a wide band gap material (~4.8 eV), with a very large breakdown electric field (~8 MV/cm) and a relatively large dielectric constant (ϵ_r 10–16),[223,224] is considered an attractive candidate in memristive systems because it can sustain high electric fields without undergoing permanent damage.[225–229] Furthermore, it can be tuned sensitively from an intrinsically insulating oxide to a low resistance suboxide, based on subtle variations in composition.[230,231] Studies specific to resistive switching in gallium oxide include bipolar[75,232–243] or unipolar[244,245] switching, depending upon the voltage polarity or magnitude during the set and reset processes.[215,246] The switching mechanism in these devices is influenced by cell architecture as well as the choice of active electrode materials.

In this study, resistive switching across nanoscale thin films of gallium oxide is examined by pairing a native and amorphous GaO_x layer[76,85] between gallium indium eutectic (EGaIn) and degenerately doped p-type Si (p^+-Si). It has been shown from the literature that this gallium oxide layer is composed of a Ga_2O_3 outer layer and an underlying Ga_2O interlayer.[101,247–252] Indium and indium oxide are also both

present and localized between bulk EGaIn and Ga_2O. Since GaO_x comprises the majority species in the oxide, the role of indium and its oxide will not be included in the study. Furthermore, as will be shown later, devices formed using Galinstan and pure gallium exhibit the same characteristics. These junctions exhibit an abrupt insulator-metal transition, with a jump in conductivity reaching up to eight orders of magnitude. The devices return to an insulating state when the polarity is reversed, thus enabling rewritable data storage. Producing these junctions is simple, highly reproducible, and demonstrates how surface oxides formed on liquid gallium can function as active electrolytes and contribute to the phenomenon of resistive switching.

4.2 Results and Discussion

The devices were prepared by dispensing a drop of EGaIn onto a lithographically patterned p^+-Si wafer, as shown by the optical images in **Figure 4.1a** and schematic in **Figure 4.1b**. A cross-section of EGaIn/GaO_x/SiO_x/p^+-Si device architecture formed under ambient conditions is shown in **Figure 4.1b**. EGaIn serves as the top working electrode probed using a tungsten tip or a steel needle connected in series with a 100 Ω resistor to protect the junction from failure.[219] EGaIn (T_m = 15.7 °C) was used as the working electrode to avoid spontaneous solidification of pure gallium (T_m = 29.8 °C) during testing. The thickness of the native oxide formed conformally on the surface of liquid gallium[76,78,85,101,102,185,253] or EGaIn[254–257] has been shown previously to be in the 1–3 nm range, with GaO_x comprising the majority species.[108] Based upon ellipsometry, the thickness of the native SiO_2 formed on the surface of piranha-cleaned p^+-Si was determined to be 2.5 ± 0.5 nm.

From the current–voltage plot in **Figure 4.1c**, junctions initially display an insulating high resistance OFF state when sweeping the device from –2.5 V to 0 V. When a positive voltage is applied, however, these junctions remain OFF until reaching the SET voltage, triggering a sharp transition to a low resistance ON state. At this point, the device retains this ohmic ON state (**Figure 4.2a**), even after sweeping the device back to 0 V. Then, the devices can be RESET back to the OFF state by applying a negative voltage up to –2.5 V, completing one cyclic sweep (–2.5

V → 2.5 V → –2.5 V). No electroforming step was required during the first sweep, and the SET voltage remained the same in the following consecutive cyclic sweeps. This abrupt, reversible, and polarity-dependent switching behavior is a signature of filamentary-type bipolar resistive switching.[195,215] In **Figure 4.1d**, the median resistance in the OFF and ON states and their corresponding ON/OFF ratios are plotted as a function of junction area. The OFF state error bars represent the maximum and minimum values and span two orders of magnitude. We associate this large device-to-device variability in the resistance to partial filling of the patterns by EGaIn, non-conformal microscale contacts along the GaO_x/SiO_x interface at the microscale,[254,258–260] and non-uniformities in oxide thicknesses (GaO_x and SiO_x). Inspection of **Figure 4.1d** reveals that changing the area of the junction has a pronounced effect on the OFF resistance and no influence on the ON resistance. Increasing the area from ~2000 μm^2 to ~30,000 μm^2 changes the OFF resistance by four orders of magnitude, decreasing from ~2 GΩ to ~0.3 MΩ. As such, small area devices (<50 μm^2) can exhibit ON/OFF ratios reaching up to eight orders of magnitude in these heterojunctions.

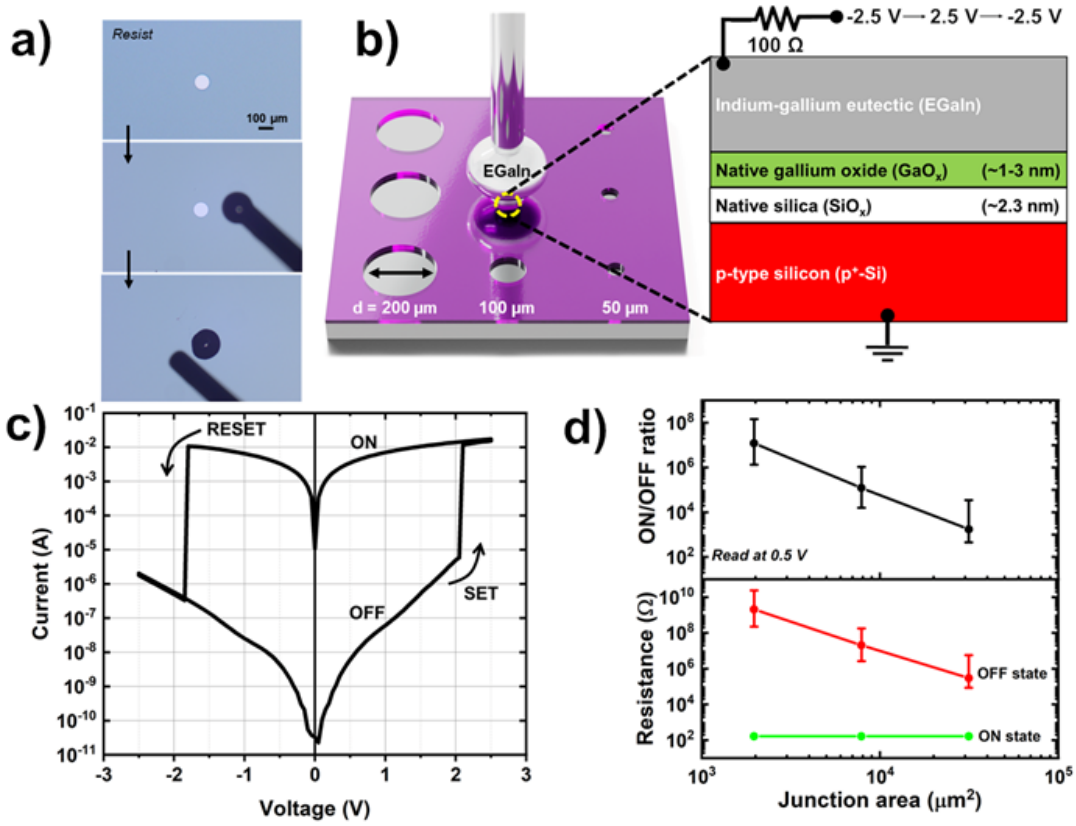

Figure 4.1. a) Optical images, showing the process of dispensing EGaIn from a needle onto the circular opening of patterned silicon, (d = 100 µm). b) Schematic of a degenerately doped p-type silicon (p^+-Si) wafer lithographically patterned to control junction area and the corresponding cross-secstion for a device formed under ambient conditions with a EGaIn/GaO_x/SiO_x/p^+-Si architecture. c) Semilog current–voltage plot of a lithographically defined device (100 μ m diameter) after a single cyclic sweep (–2.5 V → 2.5 V → –2.5 V), showing bipolar resistive switching. d) Median device resistances in the OFF and ON states as a function of junction area and the corresponding ON/OFF ratios. All resistance values were read at 0.5 V. Error bars represent the maximum and minimum resistances measured in the OFF state.

At the SET voltage, charge transport across the junction transitions from a space-charge-limited current (SCLC)[261] in the OFF state to an ohmic conduction in the ON state that is retained even after sweeping the device back to 0 V, as shown from the log–log plot in **Figure 4.2a**. When compared to pure gallium, the presence of indium (24.5 wt%) in EGaIn or indium (21.5 wt%) and tin (10 wt%) in galinstan does not change the switching behavior in these devices, as shown in **Figure 4.2b**.

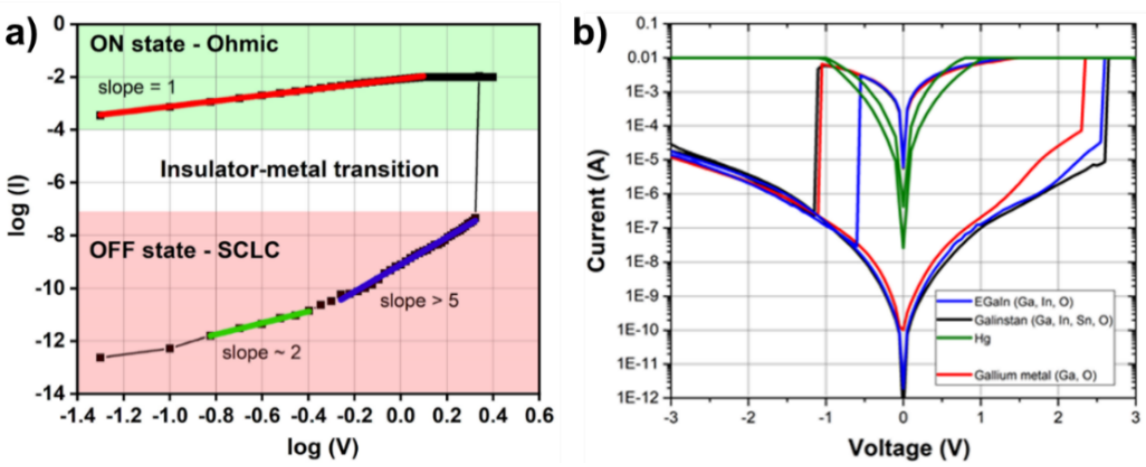

Figure 4.2. a) Log–log current–voltage plots, showing an abrupt insulator–metal transition from trap-controlled space charge limited conduction (SCLC) in the OFF state to ohmic conduction in the ON state. b) Current–voltage behavior of "liquid metal"/SiO_x/sp^+-Si junctions formed using gallium, gallium indium eutectic, galinstan, and mercury.

Compliance-controlled resistance in the ON state is examined in **Figure 4.3a**. The 100 Ω resistor was removed and the compliance current (I_{CC}) was varied instead by the power supply. The linear *I–V* plot in **Figure 4.3a** (inset) displays multilevel ohmic resistances in the ON state for a single junction subjected to multiple cyclic sweeps between –3.0 to +3.0 V. As I_{CC} gets larger, the linear *I–V* slope in the ON state becomes steeper, indicating a gradual decrease in resistance. The ON resistance at 0.5 V as a function of I_{CC} is shown in **Figure 4.3a**. Increasing the compliance current from 2 mA to 20 mA decreases the measured ON resistance from ~325 Ω to 50 Ω (black circles). Subtracting the circuit resistance ($R_{circuit}$) reveals the change in resistance across the wafer and the junction, decreasing from ~75 Ω to 25 Ω. **Figure 4.3b** and **Figure 4.3c** show the state retention and endurance for junctions formed under ambient conditions, respectively. In **Figure 4.3b**, the resistance under a constant bias of 0.5 V in both the ON and OFF states remains stable for at least 105 s, showing an ON/OFF ratio above five orders of magnitude for this particular device.

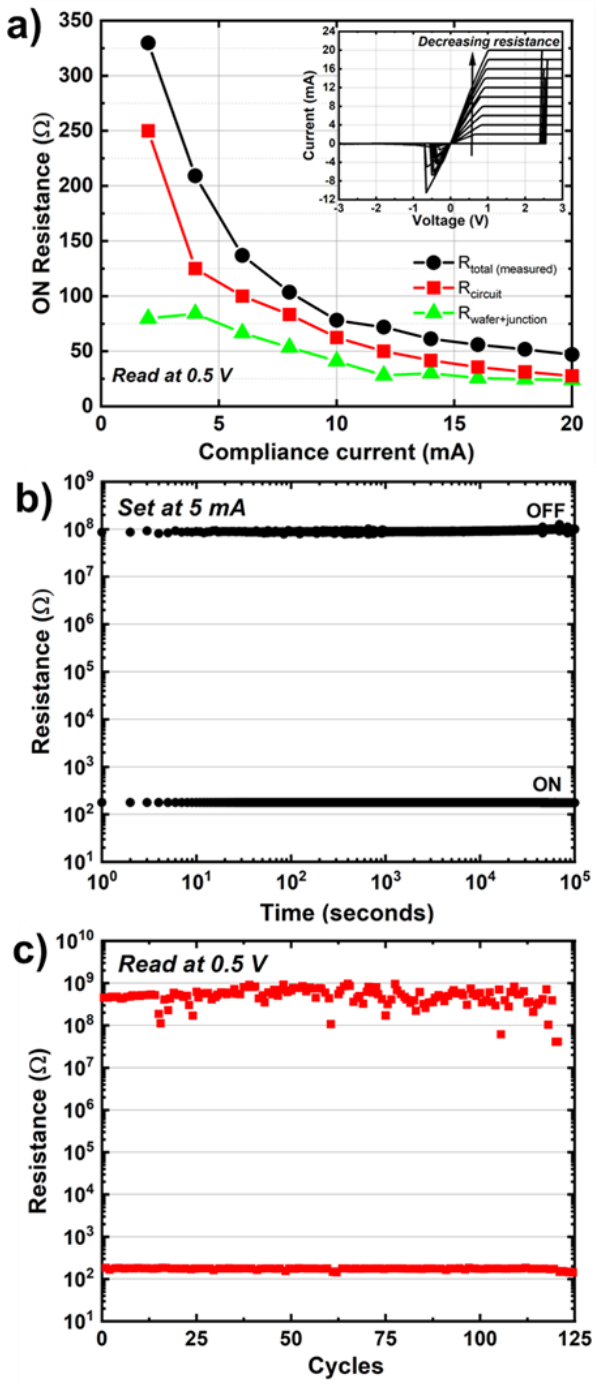

Figure 4.3. Device performance for [EGaIn/GaO_x/SiO_x/p^+-Si] junctions (diameter = 100 μm). a) Dependence of ON state resistance on the limiting current (I_{CC}ß = 2–40 mA). Inset: Linear *I–V* plot, showing multilevel state resistances obtained under different limiting currents. b) Retention time in both the ON and OFF states under a read out voltage of 0.5 V at room temperature. c) ON and OFF resistances read at 0.5 V versus the number of switching cycles between ±3.0 V and I_{CC} = 10 mA.

The retention properties as a function of temperature are examined in more detail in Section 4.2.2. Using typical cyclic *I–V* sweeps (±3.0 V), these junctions

typically survive between 10 to 20 set/reset cycles, with some junctions exhibiting an endurance of up to 125 switching cycles, as shown in **Figure 4.3c**. An endurance of up to 650 cycles also can be reached when the Si surface is probed using relatively thicker GaO_x layers formed by suspending more heavily oxidized EGaIn[260] onto a tungsten probe (more details in Section 4.2.3). The switching characteristics presented in Figures 1 and 2 were measured in air across GaO_x and SiO_x. To assess the role of each oxide on the observed switching qualitatively, the *I–V* characteristics were examined across different junctions through the sequential removal of each oxide layer in the next section.

The resistive switching behavior from representative *I–V* sweeps across Ga/GaO_x/SiO_x/p^+-Si, Ga/GaO_x/p^+-Si, Ga/SiO_x/p^+-Si, and Ga/p^+-Si junctions is shown in **Figure 4.4a–d**, respectively. Junctions with GaO_x were prepared at ambient temperature before being transferred to an argon-filled glovebox. When electrically tested under an inert atmosphere, **Figure 4.4a**, Ga/GaO_x/SiO_x/p^+-Si junctions continued to show reversible switching, which suggests that the switching phenomenon occurs without the involvement of oxygen from the external environment. In **Figure 4.4b**, *I–V* measurements were performed over Si-H_x-terminated p^+-Si. The inset shows the schematic of this device architecture. The absence of the SiO_x layer decreases the total oxide thickness, leading to the observed lowered average SET voltages. The increase in the OFF currents is attributed to high leakage currents across the thin and amorphous GaO_x layer.[259] These junctions exhibit reversible switching, revealing the critical role of GaO_x in enabling nonvolatile switching under high ON currents.

Figure 4.4c (inset) shows the device architecture formed upon contacting oxide-capped p^+-Si using freshly dispensed EGaIn inside the glovebox to avoid spontaneous formation of GaO_x on the surface of EGaIn.[83,262,263] From the *I–V* sweeps in **Figure 4.4c**, these junctions exhibit high OFF resistances due to lower leakage currents across the SiO_x layer, until they undergo dielectric breakdown between 1.5 and 2.0 V.[202] Upon measuring at least 20 devices subjected to high SET currents, all junctions underwent irreversible breakdown, as reversing the polarity did not reset

the device back to an insulating state. However, reversible resistive switching was observed when the junctions were protected using a 2 kΩ resistor (green trace). Finally, in **Figure 4.4d**, permanent ohmic junctions were formed on all Ga/p^+-Si junctions, confirming the central role of the oxides in producing an electrical barrier between metallic Ga and p^+-Si.

These data suggest that the SiO_x layer, with a dielectric constant (ϵ_r) of ~3.9, results in a decrease of the OFF currents,[264] while the GaO_x layer, with a relatively high dielectric constant reaching up to ~15, maintains nonvolatile switching at higher ON currents.[225] Therefore, high ON/OFF ratios reported in this work are enabled by combining the desirable properties from both oxides.

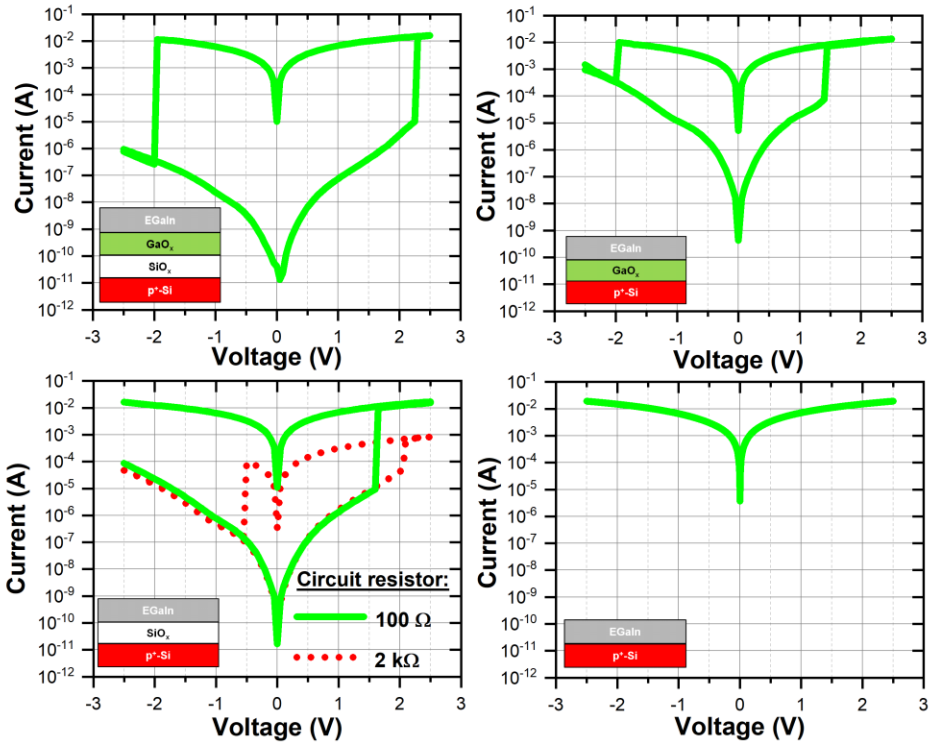

Figure 4.4. Representative current–voltage characteristics after applying cyclic sweeps (–2.5 V → 2.5 V → –2.5 V) to junctions tested inside the glovebox (diameter = 100 μm). a) EGaIn/GaO_x/SiO_x/p^+-Si: junctions prepared outside the glovebox, at ambient temperature, and tested inside the glovebox. b) EGaIn/GaO_x/p^+-Si: junctions prepared outside the glovebox, at ambient temperature, immediately after HF (aq)-treatment, and then transferred and tested inside the glovebox. c) EGaIn/SiO_x/p^+-Si: junctions formed and tested inside an argon-purged glovebox without HF (aq)-treatment. All junctions undergo irreversible breakdown, unless a 2k Ω resistor is added. d) EGaIn/p^+-Si: junctions prepared and tested inside glovebox immediately after HF (aq)-treatment. The insets show device architectures that correspond to the specific treatment conditions and testing environment.

4.2.1 Investigating Switching Mechanisms at the GaO_x/p^+-Si Interface using Conductive Atomic Force Microscopy

Conductive atomic force microscopy (C-AFM) was used to assess the switching dynamics at the GaO_x/p^+-Si interface qualitatively. A smooth GaO_x layer was formed on the surface of solidified Ga using process steps, illustrated in **Figure 4.5a**. **Figure 4.5b** and **Figure 4.5c** show a top SEM image and AFM topography of the resultant film, respectively. A p^+-Si probe tip was then used to scan the surface of the film, as shown in the geometry in **Figure 4.5d**.

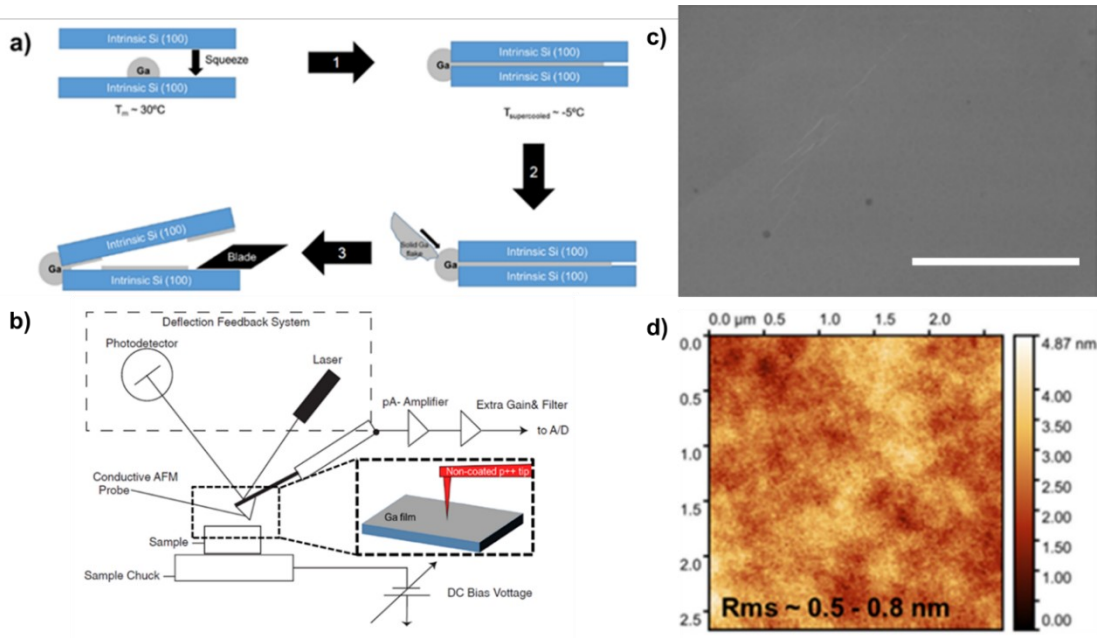

Figure 4.5. C-AFM sample preparation. a) Process steps for fabricating smooth gallium films. b) C-AFM setup and sample geometry. c) SEM image, showing a flat surface, scale bar = 5 µm. d) AFM showing a surface roughness (rms) between 0.5 and 0.8 nm.

Figure 4.6a presents a 2 × 2 μm^2 C-AFM image, showing a surface of GaO_x that was biased at different voltages along profiles 1, 2, and 3. Height maps along these profiles are shown in **Figure 4.6b**. The areas pre-conditioned below VSET (line 1, distance ~0.5–1.5 µm) showed no change in height relative to regions outside the 1 × 1 μm^2 area. However, an elevation in height along line 2, typically 3 ± 0.2 nm in thickness, was observed in areas that were biased above VSET. This result indicates that above a threshold voltage, high electric fields promote migration of Ga^+ towards the p^+-Si tip until a conductive bridge forms between the terminals. When a full

cyclic *I–V* sweep was performed at a fixed spot (marked by the dashed circle), a protrusion reaching a height of 10.7 nm was observed along line 3. *I–V* sweeps at a fixed position, as opposed to conditioning during rapid surface scanning, prolong exposure to high potentials (up to 10 V) and promote continuous upward filament growth, as observed by the protrusion. The full cyclic *I–V* sweep between –5 V and 10 V at the single point is shown in **Figure 4.6c**. The junction exhibits a gradual increase in current, until reaching the compliance current at ~5 V. Reversing the polarity leads to anodic oxidation of Ga at around –2.5 V. Reproducible bipolar switching under the same spot was not possible due to significant morphological changes at high bias voltage.

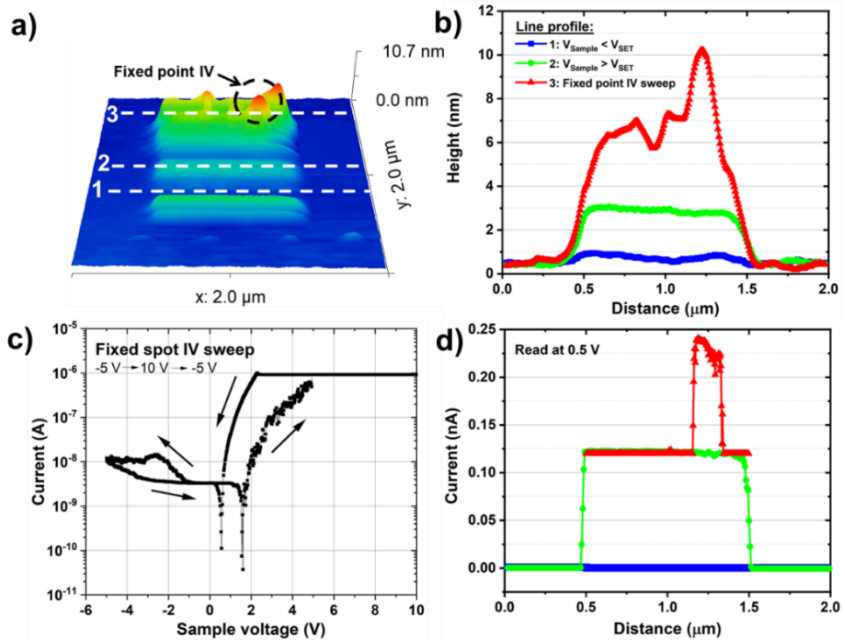

Figure 4.6. C-AFM analysis of native GaO_x films on solid Ga. a) 3D AFM height image recorded after subjecting the surface to different voltage conditions. b) Height profiles along scan lines 1, 2, and 3. c) A single cyclic *I–V* sweep at a fixed point on the surface. d) Corresponding current profiles along the same line profiles shown in b).

Current profiles acquired along the same line scans are shown in **Figure 4.6d**. As shown in line 1, the region preconditioned below VSET showed no detectable current across the entire 2 µm length. Along line 2, the current remained undetectable, until it suddenly plateaued to 0.12 nA over the area that was preconditioned above VSET. In line 3, currents above the preconditioned area increased from 0.12 nA to

0.24 nA within the vicinity of the protrusion due to formation of larger filaments at higher voltages. This C-AFM data suggests that the switching mechanism of these Ga/GaO_x/SiO_x/p^+-Si devices cannot be explained only by a traditional VCM-type mechanism; if these devices were dominated by VCM, large height changes would not be expected, as VCM generally is understood to be based upon the internal migration and redistribution of oxygen ions.[195,215] Conversely, these data point towards an ECM type mechanism, where Ga^+ ions migrate towards the negatively charged electrode, where they are reduced and accumulate to form filaments (these filaments will protrude in the case of C-AFM).[216]

4.2.2 Temperature-dependent Switching Characteristics

Investigating filaments in the ON state resistance:

To understand the nature of these filaments better, the temperature coefficient of resistance was measured for devices in the low-resistance ON state.[265,266] This was achieved by subjecting the junction to a voltage sweep from 0 V to 3 V to SET the device to the low resistive ON state. Then, the device was heated from room temperature (RT~20 °C) up to 90 °C, and the resistance was recorded with time under a constant voltage stress of 0.2 V. The ON state resistance as a function of temperature is shown in **Figure 4.7a**. The thermal coefficient of resistance for EGaIn/GaO_x/SiO_x/p^+-Si devices was determined to be 0.0007 K^{-1}, which is lower than that for metallic indium (0.005 K^{-1}) and agrees well with the value for metallic gallium (0.0004–0.0007 K^{-1}),[267,268] strongly suggesting that the filaments are indeed metallic gallium.

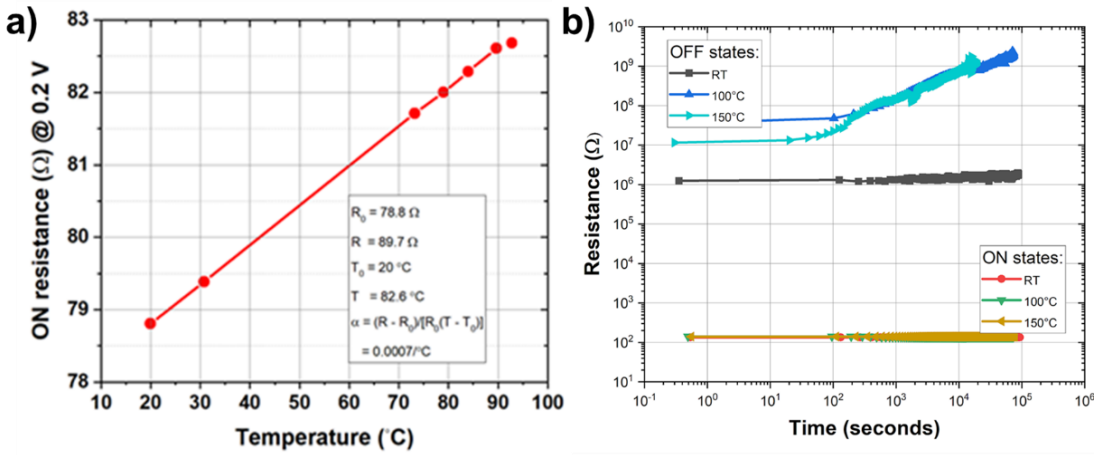

Figure 4.7. a) Temperature-dependent resistance in the ON state measured at 0.2 V and b) Retention behavior for threes devices measured in the ON and OFF states at room temperature (RT), 100 °C, and 150 °C.

State retention behavior at elevated temperatures:

To examine the thermal stability of junctions at elevated temperatures, the retention for three devices (diameter ~100 μm) were tested in the ON and OFF states at 0.5 V at room temperature (RT), 100 °C, and 150 °C for up to ~24 h, as shown in **Figure 4.7b**. Increasing the temperature from RT and up to 150 °C had little effect on the ON state resistances with time. The OFF state resistance at RT remained relatively stable, increasing slowly from 1.3 MΩ to 1.8 MΩ over the tested period of ~24 h. However, a more significant increase in the OFF state is observed with time at 100 °C and 150 °C, changing from the MΩ to the GΩ range within 2 h of exposure to elevated temperatures.

4.2.3 The Impact of Oxide Thickness on Filament Formation and Resistive Switching Characteristics

GaO_x thickness:

In the study discussed in the previous section, the self-passivating GaO_x layer forms spontaneously on the surface of EGaIn. The thickness of the oxide layer ranges between 1–3 nm upon contacting the Si surface in air. The overall oxide thickness will depend on the oxidation rate, which follows the Mott–Cabrera oxidation model.[256]

For a qualitative understanding on how the thickness impacts filament formation (forming voltage, V_{SET}) and resistive switching (retention and endurance), and assuming a constant SiO_x thickness following piranha treatment, device performance of junctions was compared when tested using two different configurations, as illustrated in **Figure 4.8**.

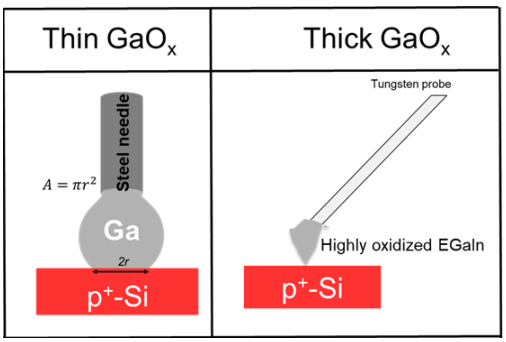

Figure 4.8. Two different methods used to probe the surface of p^+-Si. The thin layers method was used to acquire data described in the previous sections. In this section, however, a relatively thicker oxide is formed using EGaIn suspended off a tungsten probe.

Probing with EGaIn using these different techniques is believed to yield a GaO_x layer with relatively different thicknesses:[260]

1) "Thin" GaO_x layers i.e., fresh EGaIn droplets dispensed from a needle coming into contact with the Si surface within ~1 min of exposure to air. These data have been described in the previous section.

2) "Thick" GaO_x layers i.e., EGaIn that was exposed to air for prolonged periods and suspended onto a tungsten needle. These data are shown in this section.

In **Figure 4.9a** and **Figure 4.9b**, the p^+-Si chips were HF (aq)-treated and probed using EGaIn suspended off a tungsten needle. **Figure 4.9a** shows the *I–V* behavior for a single junction that was subjected to 12 cyclic sweeps. The SET and RESET voltages were 2.3 ± 0.3 V and –1.3 ± 0.3 V, respectively. Probing the same suspended EGaIn onto different areas across the same chip yielded the *I–V* behavior shown in **Figure 4.9b**. The differences in the OFF current are primarily due to large variations in the contact area of EGaIn with the Si surface. Nonetheless, stable bipolar resistive switching was observed in high yields across the entire chip when tested

within 20 min of HF (aq)-treatment, which indicates that reversible resistive switching is dominated by mechanisms across the GaO_x layer.

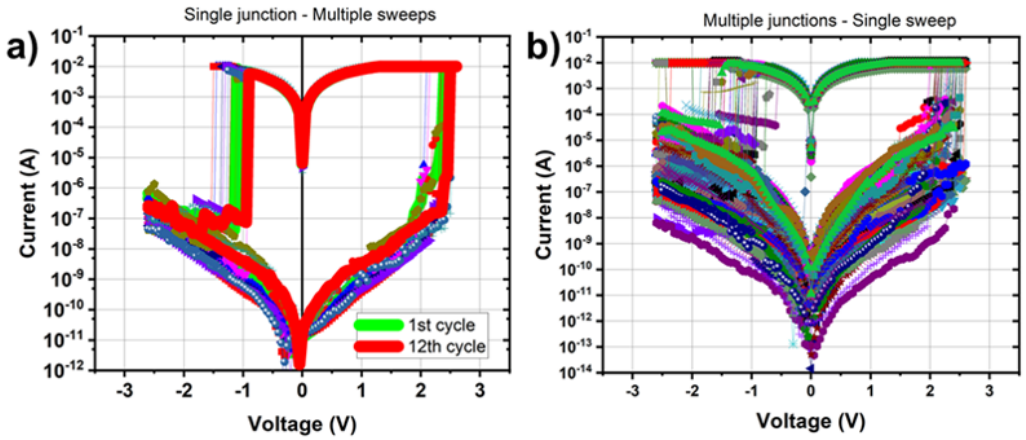

Figure 4.9. *I–V* plots for junctions tested under ambient conditions using highly oxidized EGaIn suspended off a tungsten needle (Figure 4.7, thick). The substrate was treated with piranha solution followed by 4% HF (aq), as described in the experimental. a) A single junction subjected to 12 consecutive cycles. b) Multiple junctions subjected to a single sweep.

The endurance and retention characteristics using the suspended drop is shown in **Figure 4.10a** and **Figure 4.10b**, respectively. In these junctions, the SiO_x layer was not removed and showed endurances of up to 650 cycles. This is greater than an endurance of ~125 cycles achieved using thinner GaO_x layers, described in the previous section. The ON and OFF states also were retained for at least 10k sec. The ON state currents also depended on I_{CC}, as shown in **Figure 4.10c**. In **Figure 4.10d**, we show junctions that were formed outside the glovebox and cycled five times between the ON and OFF states then transferred inside the glovebox. The last resistive state was retained and continued to switch reversibly when cycled at least five additional times inside the glovebox. This indicates that, once an oxide layer is formed, the switching mechanism is internally confined within electrolyte and does not depend on oxygen from the environment.

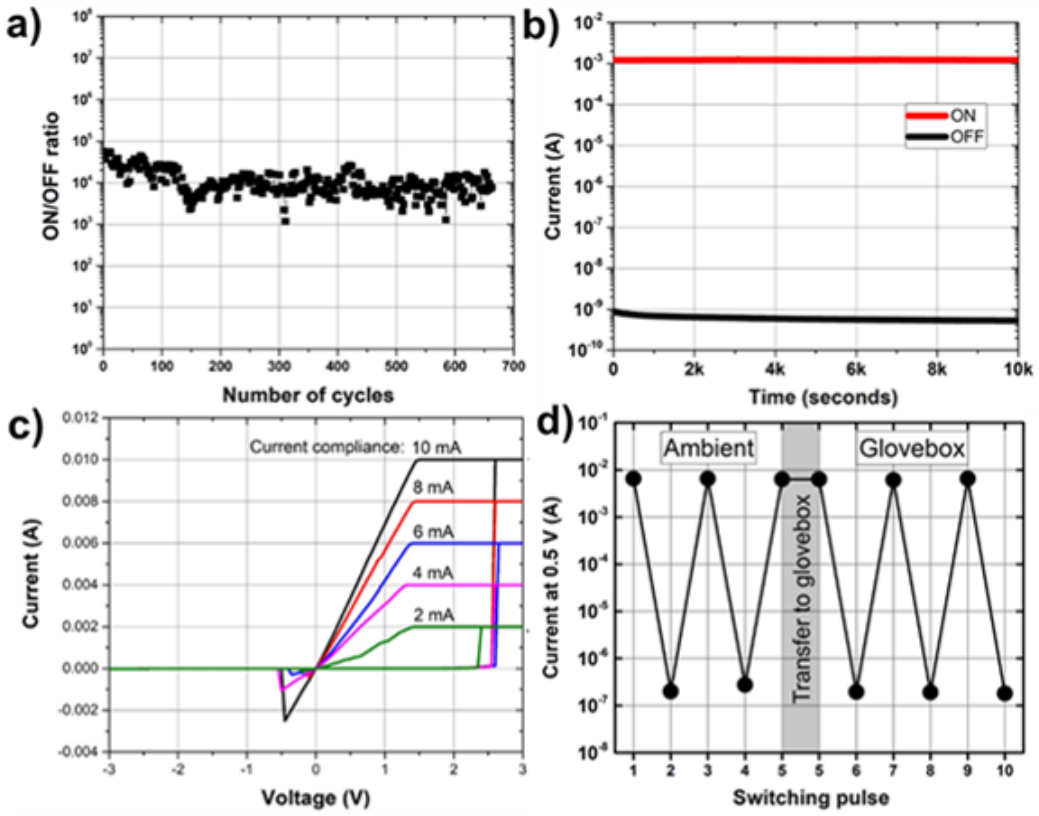

Figure 4.10. Device performance for [Ga/GaO_x/SiO_x/p^+-Si] junctions formed under ambient conditions using EGaIn suspended off a tungsten probe needle. a) ON/OFF current ratios after applying a pulsed cyclic voltage of ±3 V at 1 Hz. b) Data retention properties in both the ON and OFF states under a read out voltage of 0.5 V at room temperature. c) Linear *I–V* plot, showing multilevel state resistances obtained under different compliance currents (I_{CC} = 2–10 mA). d) Switching performance of junction formed under ambient conditions over a pre-patterned p^+-Si wafer (diameter = 100 µm). Device was read at 0.5 V after five consecutive SET (3 V) and RESET (–3 V) switching cycles, then transferred to an argon-filled glove box. The device remained stable for five additional cycles before reaching hard breakdown.

SiO_x thickness:

The effective oxide thickness of the combined GaO_x and SiO_x stacks is 3–6 nm thick. Thus, the role of a single thick SiO_x layer in resistive switching also needs to be considered.[198–202,264] Ga/SiO_x/p^+-Si junctions, with an average oxide thickness of ~5.6 nm (115-point average as measured via spectral reflectance), were prepared and tested inside the glovebox. From the current–voltage plot, shown in **Figure 4.11a**, extremely low leakage currents were measured through the SiO_x layer in the OFF-state that were below the detection limit of the source meter. An abrupt OFF to ON transition was observed between 5.5 and 6 V, in agreement with the dielectric breakdown field of the oxide (~1 V/nm).[269,270] Notably, this OFF to ON transition

was irreversible, even after protecting the junctions with a 1 MΩ resistor. These devices also failed to show any soft breakdown.

When junctions were prepared and tested outside the glovebox, shown in **Figure 4.11b**, the *I–V* characteristics showed a hysteretic *I–V* behavior, with a gradual transition from the OFF to the ON state compared to an abrupt transition for devices presented in this work. Mobile Ga^+ ions are formed *in-situ*, therefore, high electric field strengths are not required to oxidize EGaIn.[218]

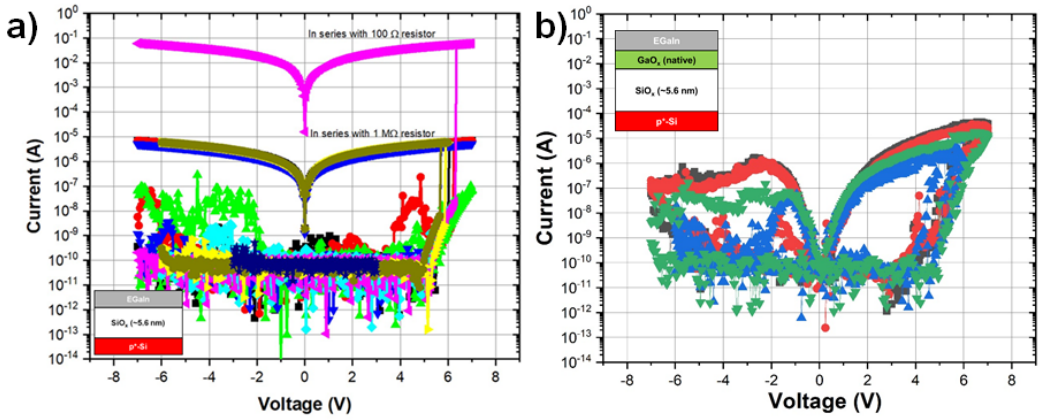

Figure 4.11. a) *I–V* plots for multiple devices (diameter 100 µm) probed inside the glovebox under cyclic sweeps between –6.5 V and +6.5 V. The inset shows the formation of EGaIn/SiO_x/p^+-Si junctions when probing inside the glovebox. b) *I–V* plot for junctions formed outside the glovebox using oxidized EGaIn on the same wafer in a). Inset shows the device architecture for devices formed at ambient temperature.

Based on these observations, it does appear that the presence of the GaO_x plays a central role in soft breakdown and the reversible switching behavior. The presence of the thin native SiO_x has shown to lower the OFF currents and improve the device yield.

4.2.4 Influence of Sweeping Parameters on the Switching Behavior

Sweep rates and step size:

Sweep rates between 0.1and 1 V/s are shown in **Figure 4.12a**, all of which showed reversible switching. The inset shows that the SET voltages are time-dependent and change with the sweep rate, switching at ~2.45 V at a sweep rate of 1.1 V/s and gradually decreasing to 2.3 V at a sweep rate of 0.1 V/s. Resistive switching as a function of voltage step size is examined in **Figure 4.12b**. The sweep delay was fixed

at 0.2 s on the Keithley 4200, and the voltage step size was increased gradually from 0.05 V up to 1 V. Reversible switching persisted to voltage steps up to 0.5 V and did not RESET at a voltage step of 1 V.

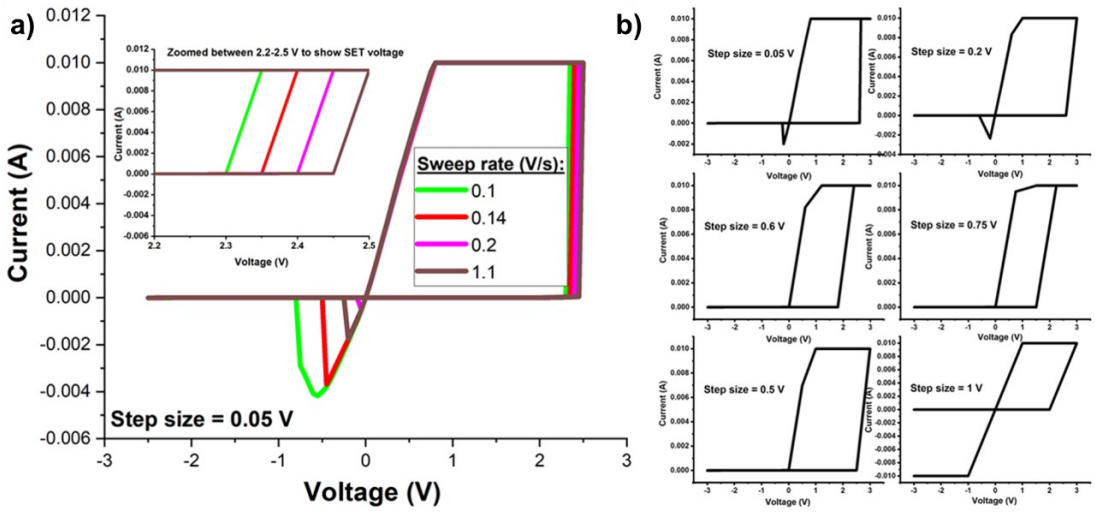

Figure 4.12. a) I–V plots for a single junction subjected to four cycles using different sweep rates. b) Multiple junctions subjected to a single sweep. Cyclic I–V sweeps between –3 V to 3 V for a single junction subjected to increasing voltage step sizes

Threshold voltage switching and compliance currents:

Cyclic sweeps up to 1.8 V and below the switching voltage (~2 V), measured at low sweep rates (≤ 0.05 V/s) were performed. These devices show no hysteresis, as shown by the blue trace in the linear *I–V* plot in **Figure 4.13**. A hysteresis can be observed only above a specific threshold voltage (VSET ~2 V). These hysteretic loops transition from ellipsoidal (I_{CC} ~ µA range) to triangular (I_{CC} ~ mA range), depending on the maximum compliance current during each sweep.

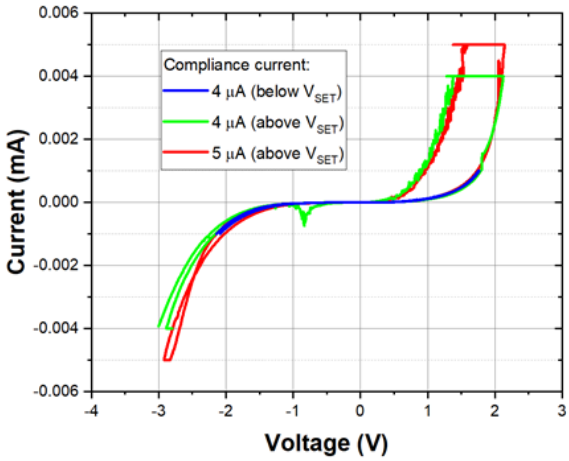

Figure 4.13. Linear *I–V* plot for a single junction subjected to three different cyclic sweeps. Blue: sweeps between ±1.8 V (I_{CC} = 4 µA). Green: sweeps between ±2.2 V (I_{CC} = 4 µA). Red: sweeps between ±2.2 V (I_{CC} = 5 µA).

A study by Aoki et al. examined thick amorphous GaO_x and report a hysteretic *I–V* behavior with a gradual transition between the ON and OFF states.[232] Devices examined in that study use Pt and ITO as ion-blocking electrodes, without the involvement of cation injection at the working electrode/electrolyte interface. Additionally, the gallium oxide layer was deposited using pulsed laser deposition to a thickness of ~90 nm and shows VCM-type switching by mixed ion electron conduction.

The *I–V* sweeps measured for these devices exhibit classical ECM behavior with asymmetric SET/RESET voltages.[216,271–274] Given these *I–V* characteristics and the above C-AFM data indicates that these devices switch via an ECM mechanism, where Ga^+ cations migrate through the gallium oxide and silicon oxide towards the negative terminal due to the intense local electric field. The Ga^+ ions are reduced to metallic Ga clusters (filament or "disc" in this case, given the total oxide thickness is less than a few nm),[275] where the disc can grow from either the p^+-Si cathode or EGaIn anode, depending on the relative ion mobility and redox rates.[276]

An ECM mechanism governing these devices is substantiated further by the data in **Figure 4.3a**, where a gradual decrease in ON resistance is observed when the compliance current is increased. This decrease in ON resistance is characteristic of ECM-type filamentary memory and is associated with the enlargement of metallic

filament(s) under high currents.[246,259,277–280] Area-independent ON resistance reveals that current passes through locally formed metallic filaments, regardless of initial device area. The OFF resistance scales with area Moreover, these devices also exhibit another characteristic of ECM-type memory, where they cannot be switched back to the OFF state above a threshold compliance current (20 mA in this case). The presence of a two-layer oxide structure of GaO_x and SiO_x is believed to be essential to achieving high ON/OFF ratios on the order of 10^8. Dielectric breakdown in gallium oxide can be recovered primarily due to its high polarizability[232] and relatively large dielectric constant (ϵ_r 10–16),[223–225] whereas silicon oxide (ϵ_r ~3.9) lowers the OFF state currents by reducing leakage currents.[264,281]

4.3 Conclusions

Bipolar resistive switching across native oxides within a sandwich architecture of EGaIn and degenerately doped p-type silicon was demonstrated, with ON/OFF ratios on the order of 10^8. Gallium oxide plays the lead role in the phenomenon of reversible switching under high SET currents, while the silicon oxide layer is essential for low OFF currents of devices. Electromigration of Ga^+ ions towards the silicon surface, which are formed at the surface of the oxidized EGaIn, leads to reversible nucleation and growth of Ga filaments across the oxide sandwich and forms the basis of the switching mechanism.

4.4 Experimental Section

Materials

Pure gallium (99.99% purity), EGaIn (75.5% Ga, 24.5% In), and galinstan (68.5% Ga, 21.5% In, 10% Sn) were purchased from Rotometals.com. Silicon wafers (p-type (boron), <100>, resistivity 0.001–0.005 Ω·cm) were purchased from universitywafer.com. Hydrogen peroxide (25–35%) and sulphuric acid were purchased from Avantor Performance Materials. HF (aqueous, 49%, semiconductor grade) was purchased from J. T. Baker. Acetone and isopropyl alcohol were purchased from Fisher. Milli-Q® system was used for deionized water (18.2 MΩ·cm).

Buffered oxide etch was purchased from Transene and was dispensed by the University of Alberta's Centre for Nanofabrication.

Substrate treatments

Piranha treatment. Si wafers were diced into squares (1 × 1 cm^2) and cleaned in a piranha solution (3:1 H_2SO_4:H_2O_2) for 15 min. (Caution! Piranha reacts violently with organics and should not be used without proper safety precautions.)

HF (aq) treatment. The native SiO_x formed on the surface of Si was removed by dipping the Si shards in 4% HF (aq) for 8 min. Then, the shards were rinsed immediately with millipore water and dried with a stream of nitrogen. For experiments carried out in laboratory ambient temperature, outside the argon-filled glovebox, *I–V* testing was conducted and completed within a maximum of 30 min of the treatment with HF (aq). For experiments conducted inside the argon-filled glovebox, the shards were transferred immediately into an argon-purged air-tight enclosure, which was then transferred into the glove box within 5 min of etching. Once the samples were unsealed inside the glovebox, *I–V* testing also was conducted and completed within a maximum of 30 min from HF (aq) treatment. (Caution! Hydrofluoric Acid (HF) is a highly corrosive inorganic acid and should not be used without proper safety precautions.)

Thermal oxidation of SiO_x. The Si wafer was cleaned initially using piranha treatment, and the chemical oxide layer grown during the piranha step was stripped with a 30 s dip in 10:1 buffered oxide etchant (BOE, Transene), followed by a DI water rinse and a cycle in a spin-rinse-dryer. Dry oxidation was performed in an atmospheric pressure quartz tube furnace (Tystar) for 10 min at 850 °C in flowing O_2.

SiO_x thickness measurement. A VASE ellipsometer was used to measure the thickness of the native SiO_x formed on Si wafers following piranha treatment. A Filmetrics optical profiler was used to measure the thickness of thermally grown SiO_x.

Electrical characterization

Device formation. To eliminate possible back-to-back Schottky contacts, the Si shards were scratched on the backside using a diamond scribe and a small amount of gallium-indium eutectic (EGaIn) (75.5% Ga, 24.5% In by weight) and then covered with copper tape. This method ensured that the grounded bottom contact was always ohmic. The junctions and their top contacts were formed by gently dispensing EGaIn from a steel needle (gauge 30G) onto a Si wafer patterned by photolithography using a positive photoresist (HPR-504, thickness ~1.2 μm) to form circles with diameters of 50, 100, and 200 μm. For the *I–V* data in Figure 4.9 and Figure 4.10, EGaIn that was exposed to air for at least one day and suspended onto a tungsten needle for probing the junctions.

Current-voltage measurements. *I–V* curves were acquired using a Keithley 4200-SCS or a Keithley 2400 source meter measured at room temperature or in an argon-purged glovebox. Using a voltage step fixed at 0.05 V, the EGaIn top contact was swept at a rate of 0.5 V/s between –2.5 and 2.5 V and back to complete a one cyclic sweep. For temperature dependent measurements, the chuck on the probe station was heated up to 100 °C. For retention studies, potentiostatic measurements were done using +0.5 V bias, with a sampling frequency of 1 Hz. For endurance testing, a sequence of voltage levels was specified using a voltage list sweep option on the Keithley 4200-SCS (–3 V, 0.5 V, 3 V, 0.5 V), followed by subsequent extraction of ON and OFF resistances from currents measured at 0.5 V after each SET (+3 V) and RESET (–3 V) event, respectively. The sweep delay and hold times were both set to 1 s. Conductive AFM setup used a Nanoscope V Controller with extended TUNA (Tunneling Atomic Force Microscopy) module. p^+ silicon probe tips were purchased from NanoWorld and Arrow EFM.

CHAPTER 5: Thesis Summary and Outlook

5.1 Thesis Summary

The primary objective of this thesis was to develop memristive devices that are within the field of flexible hybrid electronics (FHE) and understand their mechanism of action. In Chapter 1, we provided a brief overview of the field of flexible hybrid electronics (FHE). Chapter 2 outlined a proposal and preliminary results, showing the integration of P(VDF-TrFE) and high surface area p-type silicon in different architectures for hybrid memory. Processing of PVDF using short light pulses was investigated to induce the desired ferroelectric phase in Chapter 3. In Chapter 4, bipolar resistive switching was observed across surface oxides formed between EGaIn (working electrode) and degenerate p-type Si (counter electrode). An ECM switching mechanism is proposed and backed with C-AFM characterization. Although still in the early stages of research, the prospects of using organic ferroelectrics and liquids metals in printed electronics is very promising.

Organic ferroelectric materials that can be cast from solution make them adaptable to scale up processing techniques such as slot dye coating and inkjet printing. Moreover, it has been shown that microsecond UV pulses can transform the polymer to the desired ferroelectric phases making it possible to integrate onto high-throughput roll-to-roll process lines.

The unique surface properties in EGaIn make it useful in a broad range of applications including catalysis and the synthesis of 2D materials. Since EGaIn is a mouldable liquid metal, it can also create conducting channels with complex geometries which can be utilized for applications in flexible electronic and soft robotics. The conducting core as well as the oxide shell formed on the surface of EGaIn can both be simultaneously utilized to fabricate multifunctional heterostructures making them strong candidate materials in future smart devices and sensors. As an example, the concept of forming memory devices by directly printing the active metal and electrolyte in a single step offers the potential for direct integration onto surfaces that require low cost logic and memory.

5.2 Suggestions for Future Research

The following subsections are designed to discuss briefly the preliminary data obtained from follow-up experiments relevant to each chapter in the thesis. These data sets are analyzed briefly and used to suggest research concepts for future work.

5.1.1 Ferroelectric Diodes Using Interdigitated Electrodes

In Chapter 2, we showed examples from the literature that describe different techniques for fabricating ferroelectric diodes. In principle, device architectures will have ferroelectric and semiconducting channels that span two metal contacts. The layers in the diode usually are constructed in a vertical fashion.

Here, a well-established method can be used to form horizontally constructed ferroelectric diodes using interdigitated electrodes, as shown in **Figure 5.1a**.[282] Any type of metal(s) can be selected as the working and counter electrodes and are arranged such that they lie flat on the surface of a highly insulating thermal SiO_2 layer. **Figure 5.1b** shows a gap distance of ~80 nm containing a p-type Si nanocube.

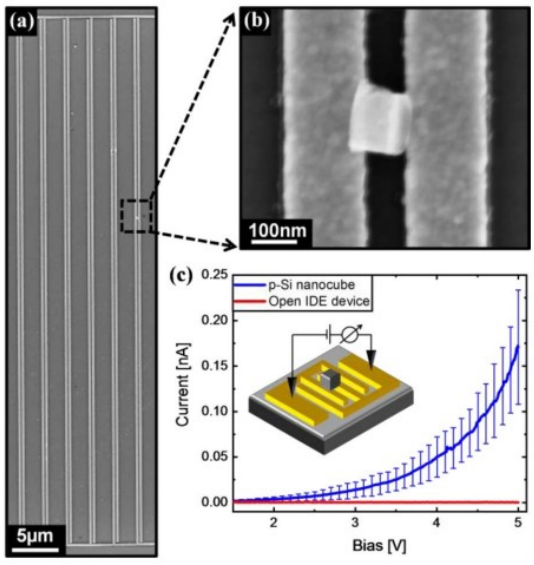

Figure 5.1. a) Top view SEM image, showing an example of interdigitated electrodes patterned using electron beam lithography. b) p-type Si nanocube inserted in the gap between the two electrodes. c) Scheme showing how these devices are probed (inset) and the resultant IV characteristics across the electrodes with and without the presence of the nanocubes. Reprinted with permission from [281]. Copyright © 2018, IEEE.

The gap distance can be modified easily using electron beam lithography. Filling the voids with a planarized layer of P(VDF-TrFE) could produce the desired architectures with the ferroelectric polymer and p-Si channels spanning the electrodes. Furthermore, ion-blocking contacts or inert metals could be chosen judiciously to avoid discrepancies in data due to defect-induced IV hysteresis, as shown in the work in Chapter 2.

As a proof of concept, P(VDF-TrFE) were spun from solution over interdigitated Au electrodes with a gap separation of 100 nm. Devices were subjected to cyclic sweeps between –15 V and +15 V, and the capacitance was measured at a frequency of 1 MHz using an AC signal of 100 mV. The resultant CV plots (2–3 sweeps/device) for three devices revealed butterfly loops that are inherent to ferroelectric polarization, as shown in **Figure 5.2**. Furthermore, the coercive voltage (V_c) was ~5 V. If we assume a coercive field (E_c) of ~50 MV/m (as measured from capacitors in Chapter 2), this will translate to a gap distance of ~100 nm, in good agreement with the chips prepared by our collaborators (Prof. Tornow's group).

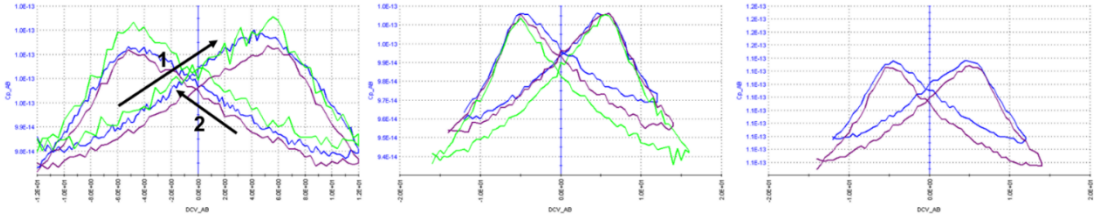

Figure 5.2. Capacitance–voltage measurements at 1 MHz for three devices of P(VDF-TrFE) spun over interdigitated electrodes of Au (100 nm gap).

These data provide direct evidence that the polymer can fill the voids successfully. Thus, the concept of aligning it with p-Si nanocubes between the metal contacts is possible. Forming these diode structures can provide a good platform for controlled device testing to help understand mechanisms of polarization-induced charge transport in ferroelectric diodes.

5.1.2 Light Processing of PVDF over Flexible Transparent Substrates

This section suggests further experiments for the work described in Chapter 3. It was shown that for PVDF films (~200 nm thick) spun over Pt-coated Si substrates, a

maximum P_r of 5.4 μC/cm^2 was reached using a pulse length of 350 μs (translating to a shot energy of ~6 J/cm^2 at 800 V).

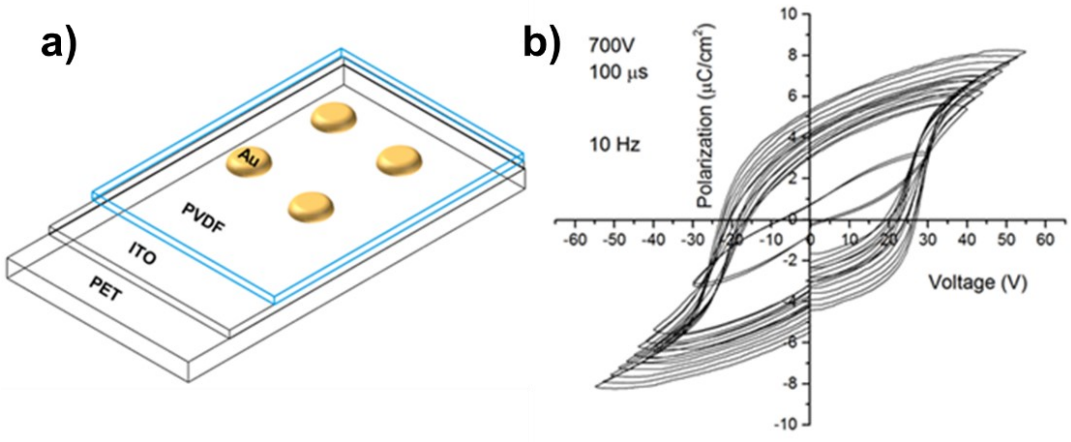

Figure 5.3. a) 3D scheme of PVDF films fabricated onto all-transparent substrates of ITO-coated PET with top Au electrodes. b) Polarization hysteresis behavior for a single device measured at 10 Hz at different voltages.

All-transparent flexible ferroelectric capacitors, excluding the top Au electrodes, were fabricated by spinning PVDF (~200 nm) over ITO-coated PET substrates, as shown in the 3D device scheme in **Figure 5.3a**. Preliminary polarization hysteresis data in **Figure 5.3b** have been shown to exhibit similar P_r values (~5.2 μC/cm^2) using a shorter pulse length of 100 μs and at a lower voltage of 700 V. Variations in thermal dissipation across Si and plastic substrates could be responsible for these differences in optimal shot lengths and energies. Thus, we suggest further controlled experiments using other plastic substrates [e.g., polyethylene terephthalate (PET), polyethylene naphthalate (PEN), or polyetherimide (PEI)] that potentially can require lower energies and shorter pulse lengths to achieve the same ferroelectric properties.

5.1.3 Substrate-dependent Resistive Switching

In Chapter 4, sandwiching the native GaO_x between EGaIn and p-type Si exhibits stable and reproducible bipolar resistive switching. The space charge limited conduction in the high resistance OFF state transitions to an ohmic low resistance ON state at a fixed SET voltage (~2 V), showing impressive ON/OFF ratios.

Recent reports in the literature also have shown resistive switching with EGaIn placed on top of graphene as a counter electrode.[283] Although the GaO_x electrolyte in that work is assumed to be identical to our electrolyte, the switching behavior in these junctions was different from the junctions reported in Chapter 4. To understand the role of p-type Si (p^+-Si) as a counter electrode, we investigated the performance of EGaIn over degenerately doped n-type Si (n^+-Si) substrates. From the *I–V* behavior shown in **Figure 5.4a**, typical reversible bipolar switching over p^+-Si p-type was observed. However, probing EGaIn over n^+-Si showed two major changes in the switching behavior:

1. After applying a SET voltage (~1.5 V in this example), charge conduction in the ON state was space charge limited (SCLC), as shown from the log–log IV plot in **Figure 5.4b**.
2. Reversing the voltage polarity did not reverse the junction back to the OFF state.

This suggests that the stable and reproducible switching that we described in Chapter 4 is specific to charge transport across GaO_x/p^+-Si junctions. It is postulated that when a negative voltage is applied to EGaIn, the rectifying behavior across Ga/n^+-Si junctions (i.e., charge blocking under reverse bias) inhibits a threshold amount of current that is required to drive a push–pull mechanism of oxygen ions to recombine with vacancies and dissolute the formed filament.[284,285] Therefore, and due to the charge blocking effect, GaO_x/n^+-Si junctions will not exhibit reversible filament formation and rupture. However, since the mechanisms that drive filament dissolution are still under discussion and due to the lack of sufficient characterization data, no conclusions can be drawn. In the next section, an *in-situ* XPS characterization technique is suggested that could help shed some light on the chemical changes that drive filament dissolution near GaO_x/p^+-Si interface.

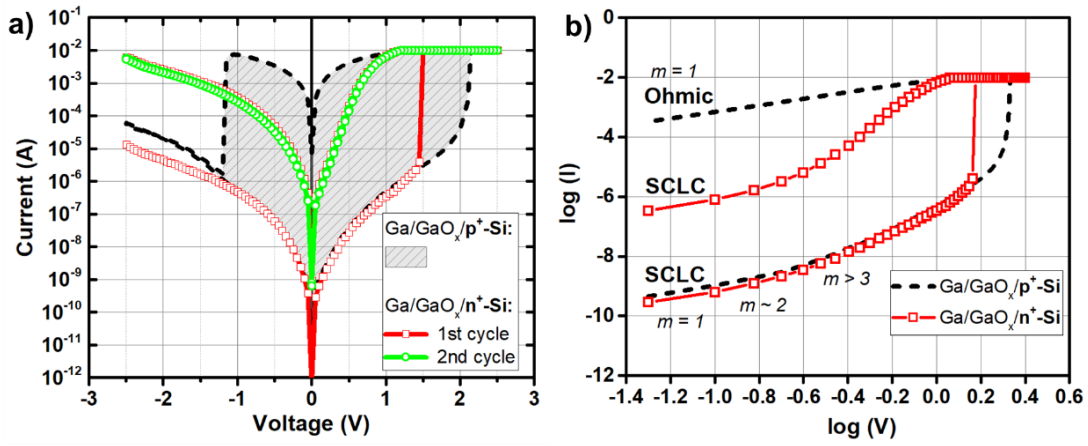

Figure 5.4. a) IV plots for EGaIn junctions formed on degenerate p- and n-type Si. Two sweeps of the same n-type junction show the irreversible nature on these junctions. b) Log–log current–voltage plot, showing the mode of charge transport for p- and n-type Si in the OFF and ON states.

5.1.4 *In-situ* XPS Analysis of Resistive Switching across Gallium Oxide/p-type Si Interfaces

p-doped (degenerate) silicon on insulator (SOI) wafers were acquired through our collaborators in TUM (Prof. Tornow). The top surface of these wafers was probed using EGaIn to form junctions depicted in the scheme in **Figure 5.4a**. The grounded terminal was formed by scratching a side on the top surface with EGaIn to ensure ohmic contact. Forming junctions over a thin layer (110 nm) of p-doped Si showed reproducible bipolar resistive switching, as shown from the cyclic *I–V* sweeps between –3 V and +3 V in **Figure 5.4b**. This behavior replicated the switching behavior discussed in more detail in Chapter 4 which use bulk degenerate p-type Si wafers.

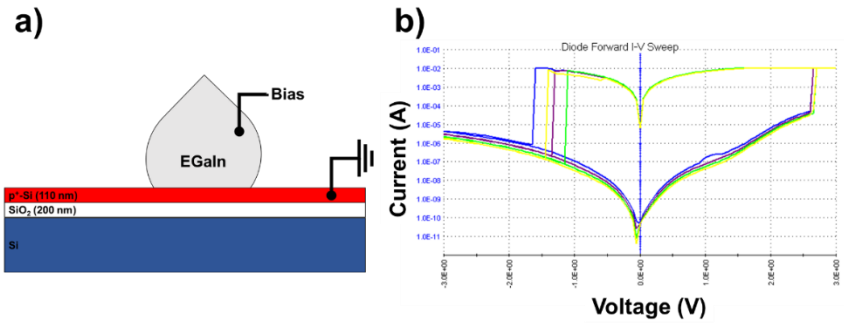

Figure 5.5. a) EGaIn probed on an SOI wafer containing a thin layer of degenerate p-type Si. b) Resultant IV plot for the junctions, showing typical bipolar resistive switching, similar to those described in detail in Chapter 4 using bulk Si wafers.

This indicates that SOI-type device architectures also will exhibit resistive switching. As such, we propose a sample preparation on SOI wafers using a bottom etch technique, typically used for the design of TEM windows,[286] to conduct *in-situ* XPS microprobe experiments and examine filament formation across the EGaIn/Si interface, as shown in the scheme in **Figure 5.6**.

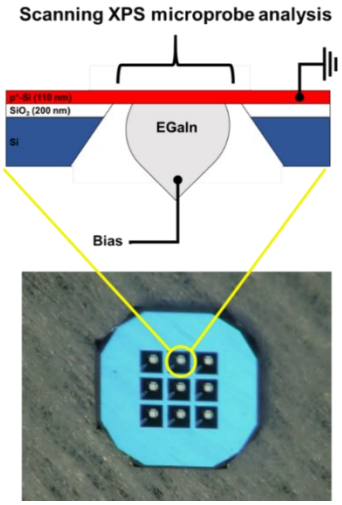

Figure 5.6. Bottom: Optical image, showing standard TEM windows fabricated by Norcada. Reprinted with permission from [282], Copyright © 2019 Norcada. Top: 2D scheme that describes the method for forming junctions through square windows patterned on SOI (can be as large as 500 µm). These devices can be probed, switched, and characterized by XPS simultaneously inside the analysing chamber. The flat surface on the top will be sputtered layer by layer and scanning using an XPS microprobe to locate filament regions.

XPS systems, such as the PHI VersaProbe III Scanning XPS Microprobe,[287] have imaging and mapping capabilities with a spatial resolution of ~10 µm. More importantly, depth profiling over a stage with tunable temperatures (–140 °C and up to 600 °C) can be used[288] by slow sputtering the top Si surface until reaching signals from SiO_x and GaO_x species (the switching interface). This approach potentially can provide crucial information regarding atomic diffusion and changes in the valence states across the switching layer. Continuous scanning across the surface also can identify filament regions within a 10 µm resolution and characterize electronic band structures across these interfaces.

5.1.5 Resistive Switching via Sputtered GaO_x

In Chapter 4, we demonstrated resistive switching across an ultrathin layer of GaO_x formed on the surface of EGaIn. Device stability, yield, and endurance were

improved when degenerate p-type Si was probed with relatively thicker oxide layers of GaO_x. However, since this native oxide is self-passivating, it was difficult to extract accurate thicknesses of the oxide layer when forming junctions. Furthermore, compositional heterogeneities across the amorphous oxide makes it difficult to understand the role of defects on the resistive switching behavior.

To address this limitation in future research, an RF sputtering technique was adopted to deposit layers of gallium oxide with highly controlled thicknesses. The stoichiometry of the oxide also can be controlled by modifying the oxygen pressure during deposition. Another advantage of sputtering the electrolyte is the ability to deposit a working electrode using different metals. Preliminary data obtained using sputtered GaO_x is shared and other deposition techniques to fabricate thin films of gallium oxide over degenerate p-type Si is suggested, such as atomic layer deposition and molecular beam epitaxy.

Thickness-dependent switching:

To examine the film quality of sputtered gallium oxide, we initially deposited a 30 nm layer of the oxide directly onto Si that was prepatterned with a resist. Then, the resist was removed, as shown in **Figure 5.7**.

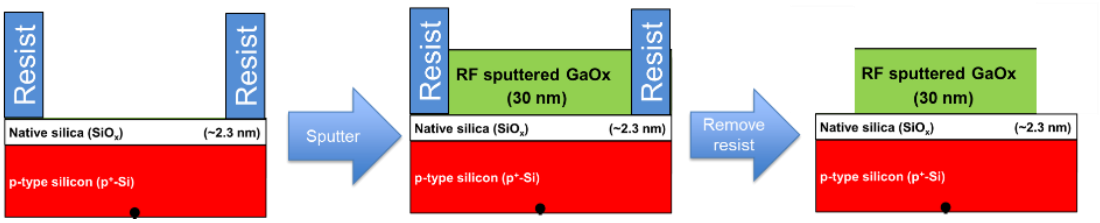

Figure 5.7. Schemes describing the processing steps taken to deposit films of gallium oxide through a lithographically patterned wafer, followed by removal of the resist.

Next, the thickness and surface roughness of the oxide were measured using AFM, revealing an oxide thickness of ~26 ± 2 nm and an rms <0.5 nm, as shown in **Figure 5.8**.

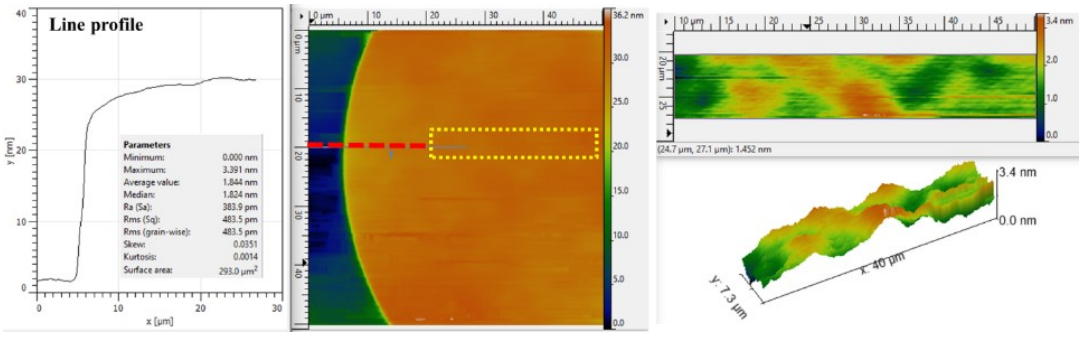

Figure 5.8. AFM measurements on the surface of circular RF sputtered gallium oxide, showing the line profile region (red dashed line) and area taken to measure the surface roughness (yellow dashed rectangle).

The Ga_2O_3 sputter target was highly insulating, and the deposition rate was extremely low (~0.03 Å/s), which can be tuned further to create low roughness films with higher thickness accuracy. The *I–V* characterization on these thick films probed using EGaIn did not show any resistive switching. Other films were sputtered at different thicknesses (3, 6, 9, 12, and 18 nm) with the thinner films (3 and 6 nm) typically undergoing irreversible breakdown, and the thicker films (12 and 18 nm) requiring high forming voltages, after which the devices fail to reversibly switch. The 9 nm films, shown in **Figure 5.9**, exhibited reversible switching and were selected for further studies in the next section. When probed with EGaIn, performing cyclic sweeps between –1 V and +0.5 V showed typical bipolar resistive switching. Unlike EGaIn probed directly onto p^+-Si without any sputtered oxide (described in detail in Chapter 4), these devices required an initial electroforming step at around 10 V. Furthermore, the SET voltages varied between 0.1 and 0.4 V, and the RESET transition behavior was gradual rather than abrupt. However, these data sets remain inconclusive because they showed large device-to-device variations and the experiments were not repeated. Nonetheless, they have been shown to operate at lower voltages (±1 V), which make them worth further exploration.

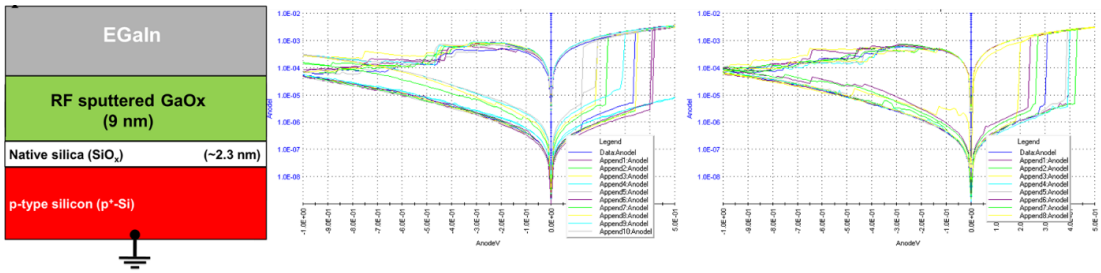

Figure 5.9. 2D device scheme and IV behavior for 2 junctions subjected to multiple sweeps. The switching layer is comprised of RF sputtered GaO_x and was initially electroformed at 10 V.

Role of the working electrode on resistive switching in sputtered GaO_x:

To bypass the use of the liquid EGaIn as the working electrode, other metals were deposited onto the surface of 9 nm of GaO_x films and examined. These working electrodes were chosen to be Ti, Cu, and Ta and were sputtered through a shadow mask to a thickness of 60 nm, then probed using a tungsten needle, as shown in **Figure 5.10**. The diameter of the electrodes was 550 µm and 350 µm. The bottom of Si layer was scratched with EGaIn to ensure ohmic contact to the grounded terminal and was covered with Cu tape.

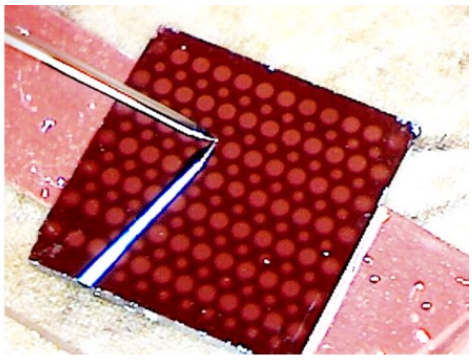

Figure 5.10. Optical image, showing a 1x1 cm^2 chip containing a 9 nm continuous layer of GaO_x and circular top electrodes deposited through a shadow mask. Devices were probed using a tungsten needle. The bottom layer was scratched with EGaIn for ohmic contacts and taped using a copper strip.

Figures 5.11 shows the scheme of the devices fabricated using Cu, Ti, and Ta as top electrodes and their corresponding *I–V* behavior. Like the devices characterized in **Figure 5.9**, an initial electroforming step at higher voltages was required. In **Figure 5.11a**, using Cu as a working electrode showed bipolar switching where the SET voltage slowly decreased after every consecutive cycle, until it stops functioning after

~3–5 cycles (i.e., undergoes irreversible breakdown and remains in the ON state). With Ti in **Figure 5.11b**, all devices failed to show a clear trend in the switching behavior. Interestingly, in **Figure 5.11c**, devices with freshly deposited Ta electrodes exhibited stable bipolar switching that was like junctions probed with EGaIn. However, this switching was not reproducible when remeasured after three days. It is suspected that Ta became highly oxidized during this period, especially since they were not capped with an inert metal, such as Pt. To address this, it is recommended that top metal contacts are deposited at low deposition rates (evaporation techniques are preferrable) and then capped with a Pt layer to protect the working electrode from oxidation in air. Furthermore, to avoid shadowing by partially deposited metal on the edges of the electrode (through small gaps between the sample and the mask), deposition on patterned substrates will produce better defined electrode areas (example shown in **Figure 5.7**).

These data have not been reproduced and require further investigation before drawing conclusions regarding the mechanisms that drive resistive switching across these interfaces.

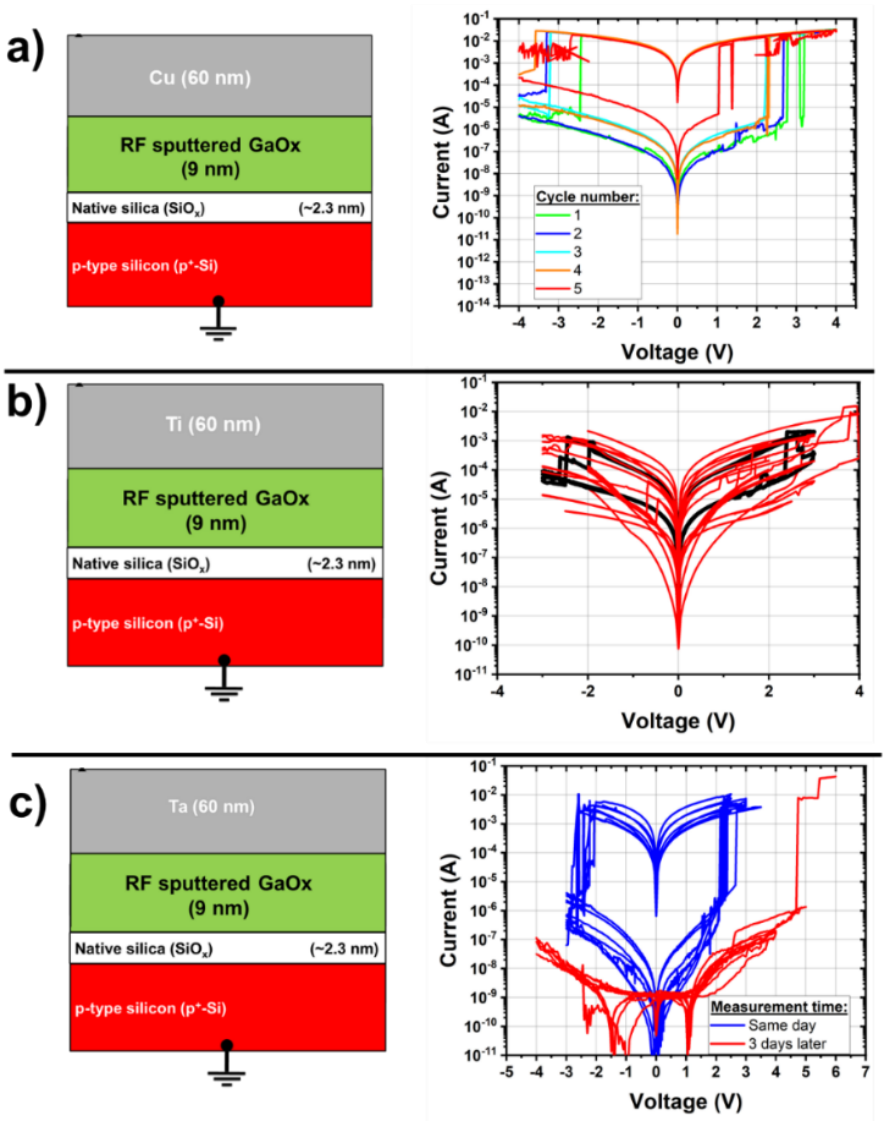

Figure 5.11. 2D device schemes using Cu, Ti, and Ta as top electrodes and their corresponding *I–V* characteristics.

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