Dynamic Carrier Pulse-Positioning for Single-Stage Isolated AC-DC Converter

by

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Abstract

The transportation sector is gaining much more attention towards all-electric modes such as electric vehicles (EV), and more electric aircrafts and ships. EVs lead the transportation sector with luxurious, high performance, and intelligent vehicles. The stored battery energy is the most important factor for the operation of the whole vehicle and therefore, EV battery chargers play an important role in the electric transportation sector. High frequency isolated battery charger converters are much preferred in the industry as they provide electrical isolation and reduce magnetic component size. Phase shifted pulse width modulation is commonly used in transformer isolated converters for high frequency power transfer. Generally, the voltage waveforms are phase shifted no more than 45 degrees for grid connected converter applications. In grid connected applications, the high frequency pulse widths (180° to minimum determined by modulation index) may vary when controlling the grid current. If, for certain duration of the low frequency reference signal, the pulse widths are smaller than the externally-commanded phase shift, the pulses would be completely separated. Under these conditions, unwanted reactive content is generated in the converter increasing the high frequency rms current hence increasing conduction losses. An original concept is proposed to lower the reactive content of the high frequency current by positioning the transformer primary and secondary voltage pulses next to each other whenever the phase shift is larger than the pulse width. The voltage pulses are positioned appropriately in each carrier cycle throughout the entire low frequency reference signal. This concept which is referred to as reference-based pulse position (RPP) allows the

operation of the converter beyond 45 degree limit and up to 90 degrees allowing for more power output. The concept is tested on an isolated single-stage bidirectional three-phase ac-dc converter which conducts both low frequency grid current and high frequency transformer current. The grid side or the primary of the converter generates the high frequency transformer voltage when controlling the grid current. The switches in the secondary side are then controlled in such a way in each carrier cycle as to coordinate with primary voltage waveform to minimize the reactive content of the high frequency current. The power is transferred utilizing the transformer interlimb leakage inductance. The transformer windings are connected so that the 60Hz grid current does not produce flux in the core leaving only the high frequency flux. Therefore, the size of the magnetics can be reduced which favors a compact design. Furthermore, the dc link utilization is maximized by injecting the third harmonic into the sine reference signals which lowers the dc link requirement by 15%.

Preface

A part of the research work presented in the thesis constitute a previously published work by the author Juan Zuniga in IEEE which has the following citation.

- J. Zuniga, M. Takongmo, C. Perera, V. Perera and J. Salmon, "Bidirectional dc-ac Converter Using a High- Frequency Transformer with Multi-Frequency Decoupled Power Control," 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 2021, pp. 1910-1916, doi: 10.1109/ECCE47101.2021.9595026.

I helped Juan Zuniga to execute his experimental tests and was involved in the theoretical analysis of some of his research components at the initial stage.

Further a separate original idea has led to a digest submission to ECCE 2022 conference which forms the contribution of the thesis. The title of the digest paper submitted to the conference is *PWM Cycle Pulse Positioning for a Three Phase Bidirectional Single-Stage Isolated Converter.* The authors of the digest paper are Vishwa Perera (myself), Juan Zuniga, and John Salmon. I was responsible for design and evaluation of the simulation models, deriving analyzes, setting up the experimental system, running tests, data collection, waveform generation from collected data, writing the aforementioned digest. Dr. John Salmon supervised the development of the research and contributed to the creation of pwm concepts. Further, he was the main editor of the digest paper. Juan Zuniga helped me with the analysis of the converter and setting up the experimental test bench and tests. The experimental hardware and laboratory equipment were supplied by Dr. John Salmon.

~To my Mother, Father, Brother, Wife, People, and Myself~

Acknowledgement

Amongst many, whose names I might have forgotten, I would like to express my sincere gratitude to all the beautiful souls whom I met and as a result the person I am today. Among them is my M.Sc. supervisor Professor John Salmon who accepted me to be one of his students. He is an excellent supervisor and gives the students the freedom for progressive research ideas and encourages constructive discussions. I learned to write technical documents clearly and concisely thanks to him. I am so lucky to be a member of his research group. I convey my heartfelt gratitude for all the support he provided me both as a person and an academic supervisor.

My dear parents, I am forever in debt for all your sacrifices that you two laid the foundation for man I have become today. Mother, you were always there when I was a kid and taught me to be honest and concerned about loved ones. Father, you taught me how to work with tools and to take care of things by myself. I am sincerely grateful for the love, care, and protection that you two gave me to the best you knew and could. I am so thankful for my brother Vimukthi who trusted me, loved me, looked up to me and spend time together with me. It means a lot to have a dear brother. Also, I convey my heart-felt gratitude to my beloved wife Vidumini for being in my life. You made a difference in me, and I will carry it further till death do us part.

I want to thank Juan, Chatumal, Marius, Chenhui for making the graduate studies a great experience. Specially I thank Chatumal for his ideas, and support for the research work, and Marius for everything about magnetics I used for my work. I earned not only a M.Sc., but really good friends. Cheers to Juan and Chatumal for being close friends. Furthermore, I would like to thank Albert Terhide for his technical assistance for practical implementation of my experimental setup.

I would like to acknowledge the Natural Sciences and Engineering Research Council of Canada (NSERC) for funding my M.Sc. program. Further, I thank University of Alberta for being a supportive multi-cultural university that helped me to experience the world.

~ Vishwa, April 2022

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LIST OF ABBREVIATIONS

3SSC	Three State Switching Cell
AC	Alternating Current
CI	Coupled Inductor
CM	Common Mode
CMO	Common Mode Offset
DAB	Dual Active Bridge
DC	Direct Current
DM	Differential Mode
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
FPGA	Field Programmable Gate Array
FPS	Fixed Phase Shift
GPI	General Purpose Input
GPO	General Purpose Output
HF	High Frequency
IGBT	Insulated Gate Bipolar-Junction Transistor
LPF	Low Pass Filter
NPC	Neutral Point Clamped
PI	Proportional Integral
PLL	Phase Locked Loop
PLECS	Piecewise Linear Electrical Circuit Simulation
PV	Photo-Voltic
PWM	Pulse Width Modulation
RMS	Root Mean Square
RPP	Reference-based Pulse Position
RT	Real-Time

SPP	Square-wave Pulse Position
SPWM	Sine Pulse Width Modulation
SS	Single Stage
SSC	Single Stage Converter
SVPWM	Space Vector Pulse Width Modulation

Chapter 1

INTRODUCTION

The inspiration behind the chosen converter and pwm methodology is provided. The foundational concept behind the converter is described based on power electronic technology originating in the early 1990's. Concepts relating to the interface of ac and dc grids are given, such as multiport and multifunctional converters. Given the chosen power converter, the selection of an appropriate pwm control technique, amongst three possible methods described, forms the key element of the thesis contribution. Due to the nature of converter operation, the modulation method must be able to dynamically lower the reactive content of the high frequency current, hence the pwm method selected is based on the best switching coordination to lower the reactive content. The nature of what makes a suitable switching pattern control for this converter is highlighted. An introduction to operation, control and analysis of the chosen converter is given.

1.1 THESIS QUESTION

The chosen power converter generates a high frequency pulse-voltage across the transformer primary when controlling the grid current. This voltage waveform is constrained by the low frequency (60Hz) grid current control, and the volt-seconds of the pulses vary throughout the 60Hz period. The secondary inverter needs switch such

that the pulse-voltage produced at the transformer secondary is coordinated with the primary in each carrier cycle to lower the reactive content. The focus is placed on coordinating the secondary to the constrained primary voltage waveform to produce a better switching pattern to lower the high frequency reactive content.

How to best switch the chosen single-stage isolated ac-dc converter such that the transformer primary and secondary voltages are coordinated in each carrier cycle to lower the reactive content of the high frequency current.

A foundational description about the research presented in this thesis is formed by separating the thesis question into two main topics: (a) the converter topology, (b) the pulse width modulation (pwm) methodology. The first topic provides the inspiration behind the selection of the converter topology and the second gives the basis for the selection of the pwm methodology.

1.2 SINGLE STAGE VS TWO STAGE

A converter which processes ac grid power into a controlled dc power in two stages is identified as a two stage converter. In typical two stage converter, the first stage is a diode bridge rectifier which rectifies the ac voltage into dc. This dc voltage is controlled, and grid power factor is corrected by a boost circuitry. The second stage is an isolated high frequency dc-dc conversion stage which outputs a controlled voltage, Fig. 1. 1. Further, the two stages are cascaded, and the power is process in the order ac-dc-dc.

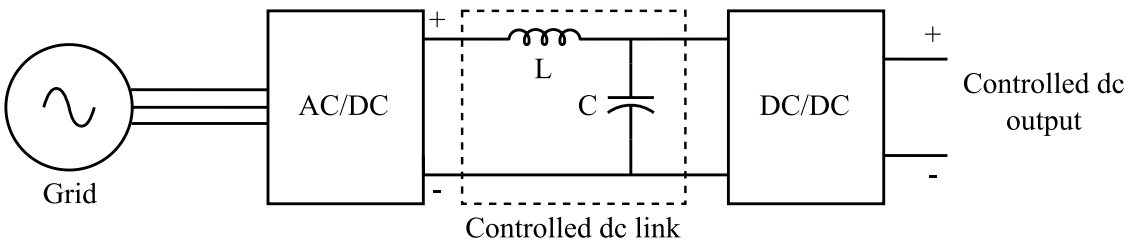

Fig. 1. 1. A generic two stage ac-dc power converter.

However, a single stage converter processes power directly from grid to a controlled dc output. The chosen converter stores energy in the primary dc link capacitor momentarily and passes the stored energy to the secondary at high frequency. The power is processed through parallel circuits instead of series power processing.

1.3 SELECTION OF THE CONVERTER TOPOLOGY

The fundamental inspiration behind the converter is the dual active bridge (DAB) converter topology. A DAB has two actively controlled switching bridges (2 or 3 half bridges) isolated by a high frequency (HF) transformer. The two active bridges are controlled in such a way that voltage of one side lags or leads the other. Due to this voltage phase difference current starts to flow, hence power flow can be controlled. Typical dc-dc DAB circuit diagrams of single and three phase converter topologies are shown in Fig. 1. 2 and Fig. 1. 3. The choice of the DAB topology is based on the following key features.

- The power transfer between primary and secondary happens at the switching frequency.
- The size of the transformer can be vastly reduced due to the high frequency operation.
- Galvanic isolation between primary and secondary due to the high frequency transformer.
- Simple power flow control by phase shifting the secondary carriers.

On a higher level of abstraction, the power flow happens at the swathing frequency. As a result, the magnetic components can be designed to have a lower size and weight. Further, HF transformers provide electrical isolation which is attractive in terms of protection. Power flow control of the DAB is straight forward; phase shift (φ) the

carriers in the secondary with respect to the primary to achieve variable and bidirectional power flow [1],[13].

The three phase DAB consists of a symmetrical three phase transformer [1] where the windings are arranged in Wye-connection, see Fig. 1. 3. Similar to the single-phase DAB, power flow can be achieved by phase shifting the secondary carriers.

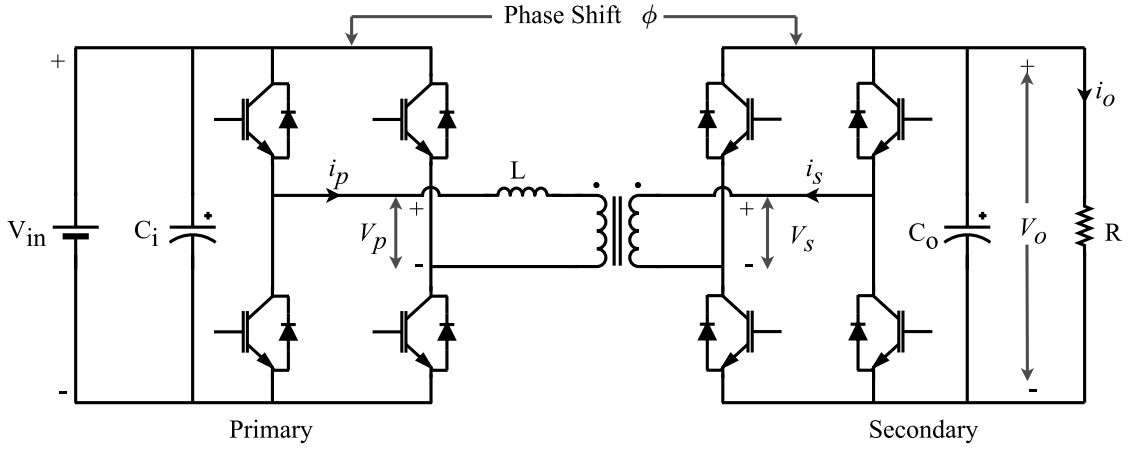

Fig. 1. 2. Single phase dual active bridge converter.

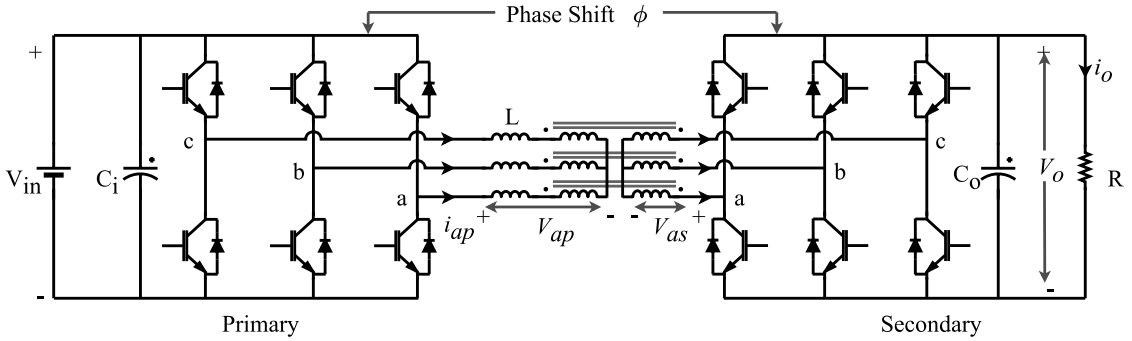

Fig. 1. 3. Three phase dual active bridge converter.

The second basis for converter selection is the grid connected single stage ac-dc power transfer capability. In the present day with the all-electric movement, efficient grid connected ac-dc converters are much preferred for a variety of applications [4]-[6]. Unlike conventional back-to-back ac-dc converters which involves at least 2 stages of power conversion, single stage (SS) ac-dc converters are much preferred. The aim

of the SS converters is to reduce the number of components and reduce the controller complexity.

The third selection basis is the operational capability as a multiport, and multifunctional converter which is highly appreciated in the present day. To simply put, reaping the maximum benefit out of a single converter by having multiple ports and to be used for multiple applications is the goal of the present day.

As the fourth requirement, ways of minimizing the size and weight of the magnetic components are considered. Size and weight of magnetic components play a key role in the physical design of the converters. Lower size and weight help to build compact and lighter power electronic products.

Based on the four selection criteria, ideas were put together to synthesize the converter for the thesis to be a three-phase bidirectional single-stage isolated ac-dc converter as illustrated in Fig. 1. 4.

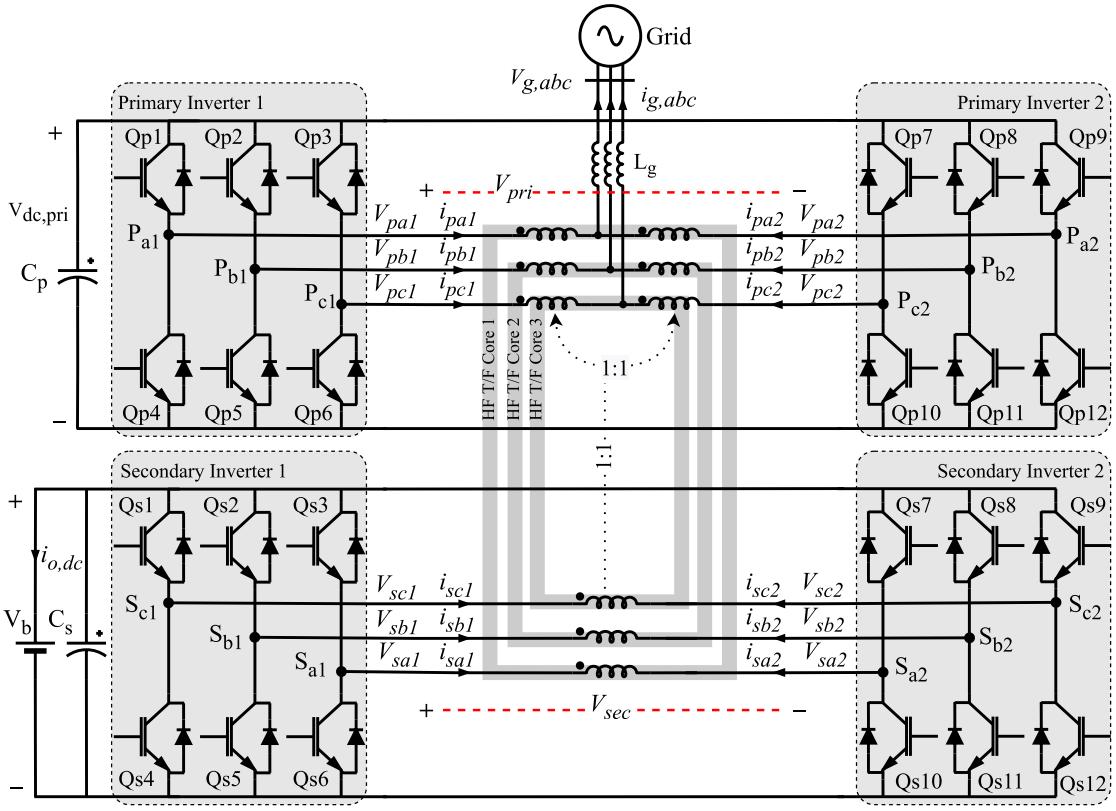

Fig. 1. 4. Selected converter topology – Three phase bidirectional single stage isolated ac-dc converter.

1.4 SELECTION OF THE PWM METHODOLOGY

Three pwm methods are introduced with their waveforms and an overview of the selection requirements is presented. One of the methods described is much similar to the pwm method presented in the literature [2], [3] in operation wise, hence a comparison with the published literature is brought forward. The other two methods are presented for the comparison and the most suited method out of the three is selected for the operation of the converter. The section only presents a high-level view of the three pwm methods and the selected method. For detailed analysis of the three pwm methods refer to the Chapter 3.

The reactive content of the system can be divided into two parts. The first, reactive power absorbed/delivered from/to the grid. The second is the high frequency reactive power between primary and secondary of the converter. The focus of the thesis is to lower the high frequency reactive power. The reactive power at the grid can easily be controlled by the grid current.

Discussion of the first pwm method starts with a brief introduction to the existing method presented in [2], [3]. The primary side of the pwm scheme control the grid current with sinusoidal pulse width modulation (SPWM) and the secondary side operate with a constant level modulation index controlling the secondary dc link voltage. This operation strategy leads to a sinusoidal reference in the primary and a constant level reference signal in the secondary. In order to match the secondary voltage with primary voltage, secondary carriers are subjected to another phase shift other than the main phase shift (φ), refer Fig. 1. 5, Fig. 1. 6 [2]. Changing the main phase shift allows the converter to transfer power between the primary and the secondary. The authors refer to the second phase shift as the secondary phase shift (φ_{sec}) which is used as a mechanism to match the primary and secondary high frequency pulse voltages, and it is implemented based on the primary reference signal variation.

The same primary and secondary voltage patterns can be obtained by feeding the primary reference signal to the secondary and phase shifting the secondary carriers by

the angle φ. This method only requires the secondary carriers to be phase shifted by the main phase shift φ making the control less complicated, Fig. 1. 7. At the steady state operation, there exists a fixed phase shift between the primary and secondary voltages. Thus, the carrier phase shift method, Fig. 1. 7, is termed as fixed phase shift (FPS) throughout the thesis.

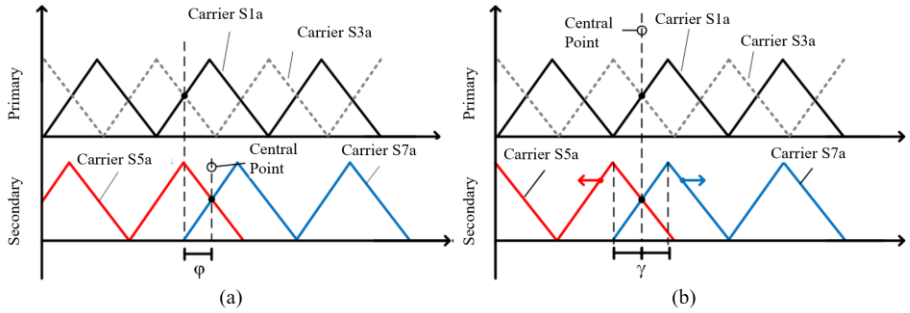

Fig. 1. 5. Carrier phase shift strategy presented in [2]. (a) Main phase shift φ implemented on the secondary carriers, (b) secondary phase shift implemented on the secondary carriers by moving the carriers. Source [2].

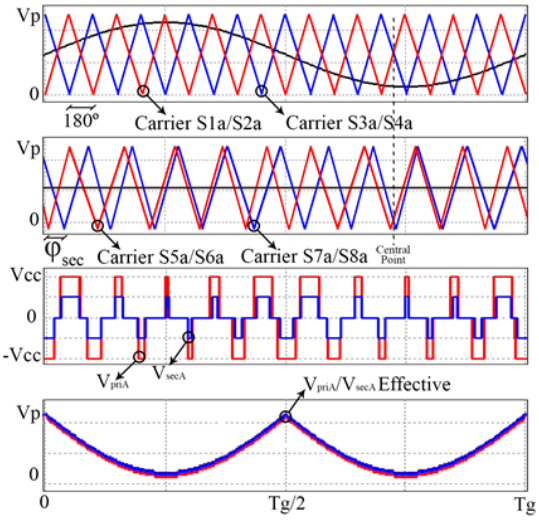

Fig. 1. 6. Illustration of main and secondary phase shift of [2]. A secondary phase shift φ_{sec} is implemented on the secondary carriers in order to align the primary and secondary voltages. Source [2]

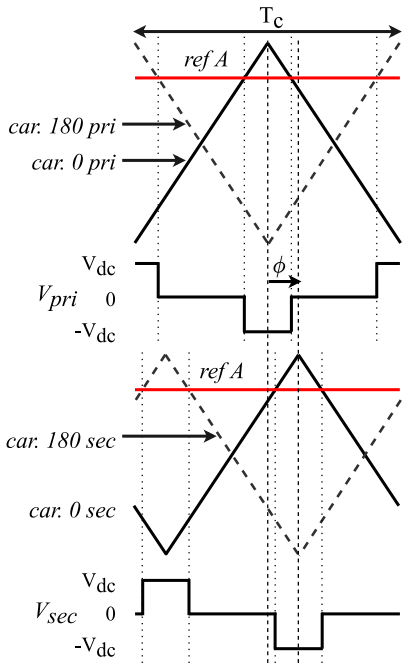

Fig. 1. 7. Phase shifting the secondary carriers only by angle φ to implement the same phase shift in the voltage waveforms.

Before explaining the waveforms of each pwm method, it is first required to introduce the waveforms. The power transfer mechanism of the converter topology, Fig. 1. 4, can be simplified into a transformer model with high frequency pulse voltages at the primary (V_{pri}) and secondary (V_{sec}), Fig. 1. 8. Similar to the DAB circuit, the equivalent series power transfer inductance, L_{lk}, allows a high frequency current, i_{hf}, to flow through the transformer. The waveforms V_{pri}, V_{sec}, i_{hf} are used for the discussion of the three pwm methods.

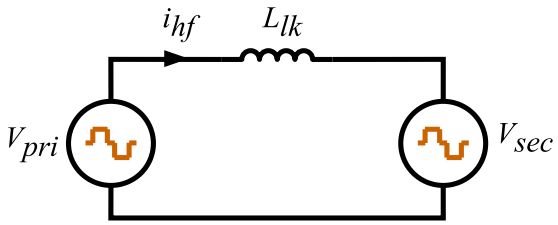

Fig. 1. 8. The power transfer model of the converter topology can be simplified into a transformer equivalent as shown. V_{pri}, V_{sec}: high frequency pulse voltages at the primary and the secondary of the transformer, L_{lk}: equivalent series inductance through which the power is being transferred, i_{hf}: high frequency current.

The FPS pwm method implements a phase shift φ between the primary and the secondary voltage waveforms. The difference in phases allows a high frequency current to flow through the transformer, Fig. 1. 9.

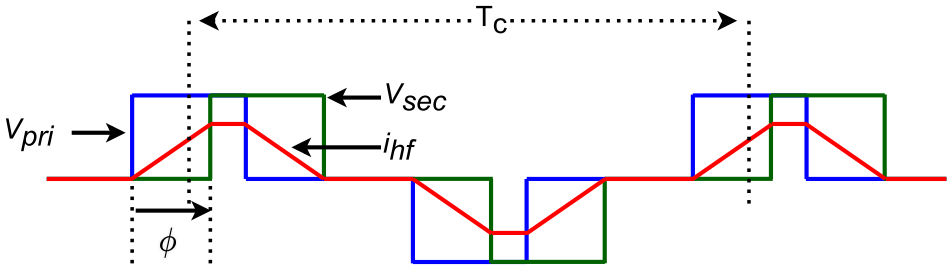

Fig. 1. 9. Characteristic waveforms of the FPS method.

The second pwm method focus on arranging high frequency primary and secondary voltages in a better way such that the methodology allows to reduce the reactive content of the high frequency current. Special strategy is used to position the voltage pulses when the width of the voltage pulses is lower than the phase shift, Fig. 1. 10. Whenever the phase shift is larger than the voltage pulse width, the pwm strategy described is

implemented. As an example, Fig. 1. 10 (a) illustrates an instant where the phase shift φ_1 is greater than the pulse width θ_1. The secondary voltage pulse V_{sec} is completely separated from the primary voltage V_{pri}. The current in the shaded region circulates within system through the capacitors and does not involve in active power transfer. Thus, unwanted reactive content is generated in the system due to phase shifting the voltage pulses beyond their pulse width.

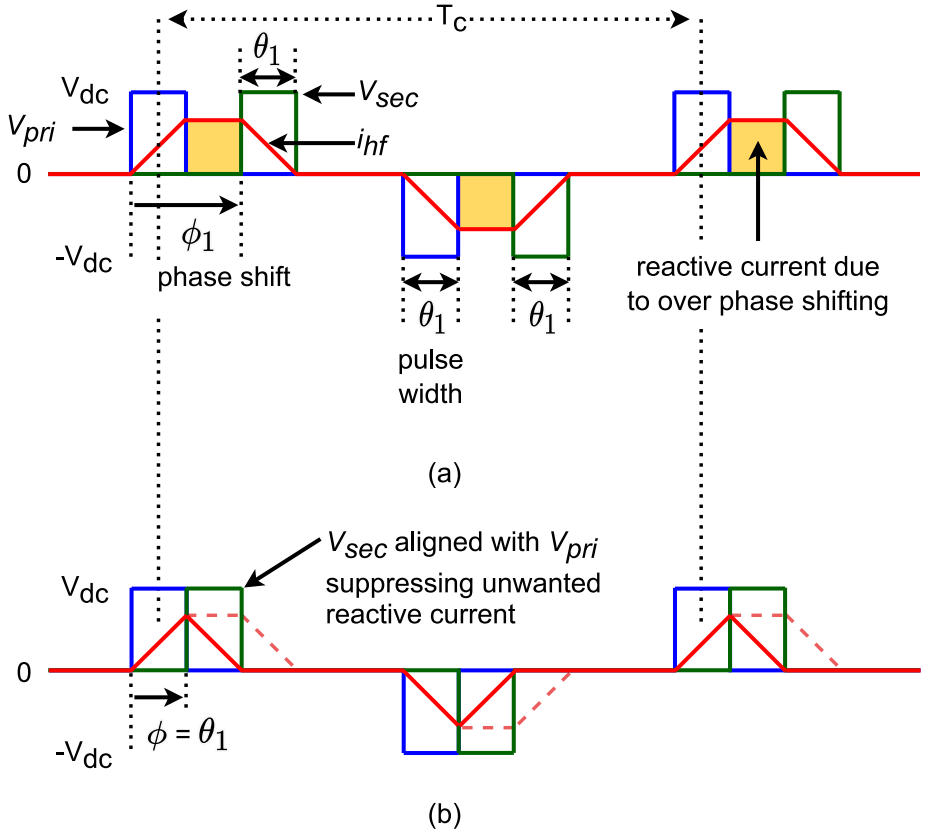

Fig. 1. 10. The concept of pulse alignment when the phase shift is larger than the pulse width.

However, if the secondary voltage pulses are aligned next to the primary voltage pulses without letting the voltage pulses to be separated, the unwanted reactive power otherwise generated can be eliminated. For the secondary voltage pulses to be aligned with the primary, secondary should be phase shifted exactly by the pulse width. Fig. 1. 10 (b) illustrates the secondary being phase shifted by the pulse width θ_1 in order to align with the primary thereby suppressing the unwanted reactive current. The pulse width can easily be evaluated based on the value of the reference signal, (more details

in Chapter 3). Therefore, voltage pulses can be aligned based on the value of the reference signal, hence, this pwm method is termed as reference-based pulse positioning (RPP) method.

The third pwm method can be described as a square wave voltage modulating in the secondary side, which is in turn aligned with the primary three-level voltage waveform as illustrated in Fig. 1. 11. A phase shift can be implemented between the primary and the secondary, however, implementation of the phase shift is not discussed in the thesis. This pwm method is termed as square-wave pulse positioning (SPP) method.

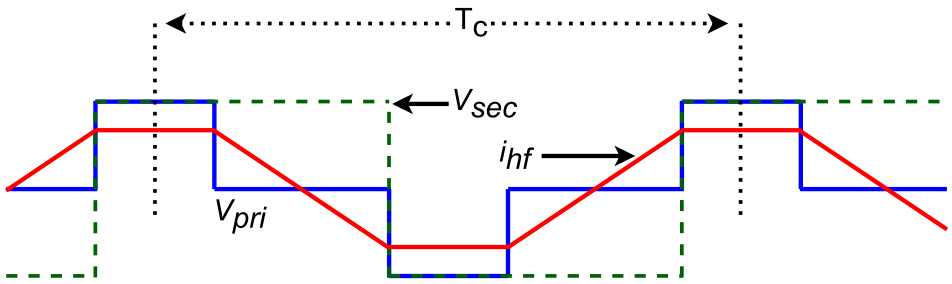

Fig. 1. 11. Concept of square wave pulse positioning.

In summary the three pwm methods that are discussed in the thesis are,

1. Fixed phase shift method (FPS)
2. Reference based pulse position method (RPP)
3. Square-wave pulse position method (SPP)

In order to select a better pwm method, the three pwm methods are analyzed in terms of the rms of the high frequency current and the reactive content of the high frequency current. Based on the analysis of the converter (Chapter 3), the more suited pwm methodology for the operation of the converter with low high frequency rms current and reactive content is the RPP.

1.5 APPLICATIONS OF THE CONVERTER

The converter topology can be viewed as a multifunctional converter which can be used as a multiport power converter having two dc links and a three-phase gird connection, and as an ac-dc converter which can be used in electric vehicle charging. A test case scenario where the converter operates as a battery charger operating at constant current and constant voltage modes of operation is presented in experimental results. The applications of the converter are listed below.

- Electric vehicle battery charger.
- Multi-frequency converter connecting two ac grids.
- Three-port battery charger converter.
- Bidirectional multi-port converter.

1.6 SUMMARY

The background information required for the research work is provided. The selected converter topology is based on the topology and the principle of operation of the DAB circuit. Based on the DAB circuit, the selected topology is made to function as a 3-phase grid connected single stage isolated ac-dc converter. Three pwm methods are considered for the operation of the converter. The secondary modulation must coordinate with the primary to lower the reactive content, thus, the best pwm methodology out of the three is selected for the modulation. The converter can be used as an EV battery charger, a multiport converter, and a multi-frequency ac-ac converter.

Chapter 2

GRID CONNECTED ISOLATED HIGH FREQUENCY CONVERTERS

Key features of a selected group of published converters are presented that relate to high frequency isolated converters. These converters are used to place the converter discussed in the thesis in context. The main relevant types of converter topologies described are: 3-phase and 1-phase DABs; 3-phase and 1-phase multiport converters; 3-phase and 1-phase single-stage ac-dc converters. Common features observed in multiport converters are their use of high frequency transformers, integrated magnetics, and their utilization of a single-stage ac-dc conversion stage. The main types of modulation techniques reported in the literature are sinusoidal, space vector, and variable duty cycle PWM along with phase shift control. The relevance of published work is compared with the thesis research to place the work in context.

Power converters have been an integral part since the technological revolution and more focus is laid on power systems, electric vehicles, more electric air crafts and ships, wind power converters, and solar power converters. The transportation sector is gaining much more attention to the all-electric modes of transportation aligning with global movement towards zero carbon emission goals. Renowned car manufactures like Tesla, BMW, Mercedes, Ford, Porsche, Audi etc. amongst many are advancing constantly for highly efficient, high performance, long distance, smart and intelligent electric

vehicles. Among the myriad of power electronic circuits, battery charging circuits for electric vehicles have gained much attention since energy stored in the battery is if not the most important factor for the operation of the vehicle. Electric vehicle battery charging circuit topologies can mainly be divided into two categories as a) two-stage converter topologies, and b) single-stage converter topologies, both consisting of single and three phase variants. Detailed background review of types of converters in each of the a and b categories and modern trends in electric vehicle charging topologies can be found in the literature [4], [5], [6]. The converters which fall into the category – high frequency isolated converters are highlighted, whose topology and modulation methods have directly comparable characteristics with the work presented in the thesis.

2.1 3-PHASE, 1-PHASE DAB AND DAB BASED CONVERTERS

The three-phase dual active bridge converter forms the basis for the converter topology studied in the thesis, Fig. 1. 3. Though it is a dc-dc converter, the DAB circuit structure can be used to develop the grid connected converter topology. Further, DAB based converter topologies can be found in the literature which have similarities to the thesis topic. The core similarities are the high frequency isolation, single-stage ac-dc power transfer, and phase shifted power flow control. Selected literature is discussed with their merits and relevancy to the thesis.

Detailed study and analysis of the single and three phase DAB circuits for high power applications is first put forward by Rik De Doncker *et. al.* in 1991 [1] and presents both single and three phase versions. A three-phase symmetrical transformer with Y-Y connection is used for the three phase DAB while a single transformer is used for the single-phase DAB providing isolation between the input and the output. The leakage inductance of the transformer is used as the power transfer inductance to achieve power control [1]. The converter discussed in the thesis also uses the interlimb leakage inductance of the transformer, however three separate transformers are being used for the three phases.

The DAB converters were first introduced as dc-dc converters. Both the single and three phase DAB and DAB based converter types have been researched [1],[13],[14],[15]. The H-bridge DAB presented in [1], [13] is much more similar to the single-phase circuit of Fig. 2. 1. The similarity can be observed comparing Fig. 2. 2 and Fig. 2. 3. The power transfer inductance of the thesis converter is the leakage inductance which essentially does the work of series inductance L in Fig. 2. 3. The difference in the circuits of Fig. 2. 1 and that of [1], [13] is that the convert studied in the thesis consists of an additional port which connects to the grid. However, the circuit for primary to secondary power transfer simplifies into a H-bridge DAB for each of the three phases.

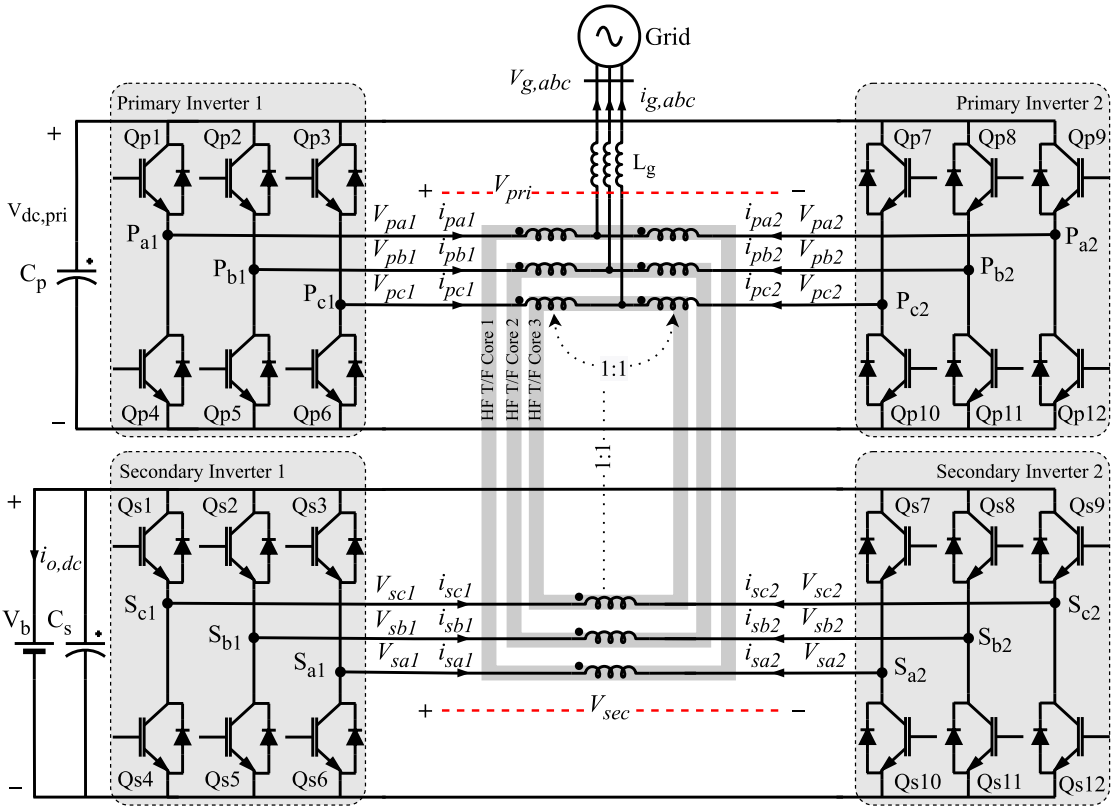

Fig. 2. 1 Converter topology discussed in the thesis. Each phase can be considered as a single-phase DAB (Fig. 2. 3) transferring power between primary and secondary by phase shifting.

The single-stage converters are widely used to process the power conversion in a single step. They bring about the advantages of reduced components, compactness, and improved efficiency over two stage power converters. One main feature of the thesis

converter is the single-stage ac-dc power conversion where, the three-phase ac grid power is converted to dc power and taken out at the other end of the converter. Vast majority of single stage converters use the isolated phase shift power transfer characteristic of DABs. Thus, published DAB concept based single stage converters can be compared with Fig. 2. 1. The closest single-phase single-stage converter configuration to the thesis converter is based up on the interleaved three stage switching cell (3SSC) and DAB concept integrated converters [16],[17]. The switching action of the 3SSC is capable of producing 3 voltage levels ($+V_{dc}$, 0, $-V_{dc}$) in the high frequency transformer primary and secondary. The power transfer is achieved by controlling the phase shift of the secondary voltage waveform relative to the primary. The authors of [16] proposes a three-port converter while[17] proposes a four-port converter which can be used as a single-stage multiport converter. It is unclear about the magnetics used in [16],[17] as the authors does not explicitly mention it, however, it is likely that they have used the transformer leakage inductance. Assuming it is the case, Fig. 2.1 topology and [16],[17] use the transformer leakage inductance for power transfer. Main challenge is the designing of the transformer leakage which is highly dependent on the number of windings, interlimb coupling, winding arrangement and air gap.

Matrix type DABs [18], [19] are another variant of single stage converters. The main advantage of these converters is that the expensive and bulky electrolytic dc link capacitors on the grid side can be removed [18] The single-stage converter presented in [18] have only 16 switches while the converter under consideration in the thesis has 24 switches. However, [18] does not have the multiport capability.

Another DAB based topology is derived from T-type neutral point clamped (NPC) circuit structure, [20], and uses half-bridge interleaving technique along with a coupled inductor (CI) in order to reduce current stresses and weight. A similar circuit configuration can be observed in Fig 2.1 where legs in inverters 1 and 2 are interleaved and interfaced via a coupled inductor.

Totem pole interleaved half bridge based DAB converters also offers the benefit of eliminating bulky electrolytic capacitor form the grid side [21]. Compared with the

single-phase matrix converter based DAB [19], the totem pole DAB converter [21] has 2 additional switches (8 vs 10).

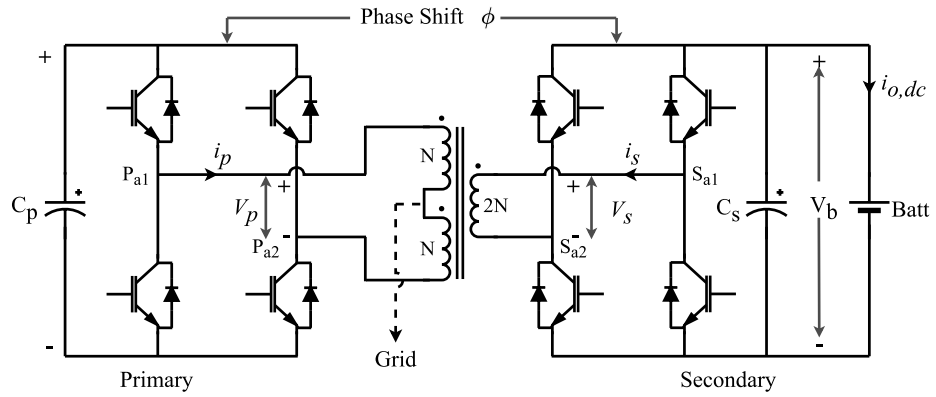

Fig. 2. 2. Single-phase circuit of the converter described in Fig. 2. 1 for the high frequency power transfer. The power transfer inductance can be an externally placed inductor or the interlimb leakage inductance of the high frequency isolation transformer.

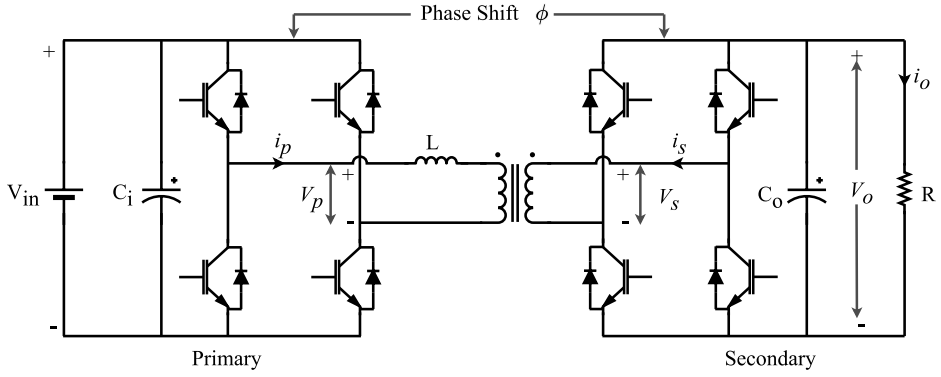

Fig. 2. 3. Phase-shifted dc-dc DAB converter.

2.2 3-PHASE, 1-PHASE MULTIPORT CONVERTERS

The key features of directly comparable multiport converters with the thesis work are presented. Multiport converters offer multiple converters to be integrated and operated in a single power electronic converter system. Increased attention is given to the research on multiport converters in the recent years. It is important to highlight the

key features of the published multiport literature which have comparable features with the thesis work.

A power electronic converter that has multiple power inputs/outputs and is controlled to balance the total power inflow with the total power outflow can be considered as a multiport converter. Multiport converters assist to reduce the number of power processing stages hence, the number of components and thereby power losses. The control of the input/output power balance in a multiport converter can be made much more effective rather than having completely separate controllers for each power stage (however, the control algorithm on the whole can be complex due to the integration of several controllers). Since multiport concept allows the integration of several power processing stages and the control of them, a properly designed single converter can achieve wide range benefits [7], [8], [9], [10]. Mostly renewable energy resources benefit from the multiport converter architecture due to the presence of several power conversion stages.

The converter in Fig. 2. 1 consists of three active power ports: grid, primary dc link, and secondary dc link power ports. The converter also has the capability to extend to another 4^{th} power port at the center tap of the secondary winding. The control of the converter is done so as to balance the power in all the three ports. A capacitor is used for the primary dc link power port of the converter, and it is regulated with respect to the grid voltage. Instead of the capacitor, any controlled voltage port such as a PV system, battery energy storage system, etc. can be connected to extend the usability of the converter. Also, a fourth port can be produced by creating a center tap in the secondary windings, Fig. 2. 4.

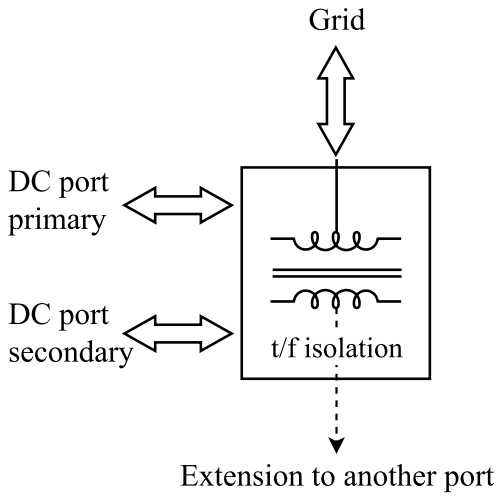

Fig. 2. 4. Multiport capability of the converter discussed.

The three-phase multiport converter topology presented in [2], [11] is very similar to the topology presented in this thesis where both the literature presents the same converter topology with four power ports. The four power ports are created as illustrated in Fig. 2. 4. Furthermore, these literature use external inductors for power transfer instead of the transformer leakage which is used in the thesis converter. The converter controller for both the literature [2], [11] is the same and uses carrier phase shift method. Moreover, the authors implement a second phase shift in order to match the primary and secondary high frequency pwm voltage pulses, refer Fig. 1. 6 and Fig. 1. 7. Such a pulse-matching implementation requires the carriers in the secondary to vary in frequency and it is possible to increase the complexity of the control algorithm. However, variable frequency can also bring about benefits of reducing losses by matching high frequency voltage pulses in specific way as the literature have implemented in [2], [11].

The same converter topology presented in the thesis is first studied for power transfer using a 2kHz sine wave which is controlled by rotating reference frame direct-quadrature (dq) axis power controller [22]. The concept of power transfer is still the phase difference between primary and secondary. However, instead of carrier phase shift, the sinusoidal reference signals are phase shifted by dq-axis controllers. The 2kHz sine wave is modulated on the 60Hz grid modulating signal. Thus, the control strategy

is restricted by the amplitude of the 2kHz signal. Moreover, the size of the magnetics is relatively large as the flux associated with the power transfer occurs at 2kHz as opposed to the switching frequency, 40kHz. In contrast, the same converter topology is operated at the switching frequency of 10kHz in the thesis and the power transfer occurs at the same frequency.

The three-phase three-port converter published in [9] utilizes a full bridge diode rectifier isolated by a delta-wye high frequency transformer. On the other side of the transformer is a three phase bidirectional 2-level voltage source converter interfaced with a three phase grid. The power flow control from inverter to the rectifier is achieved by modulation index control while the grid current is controlled in the dq-axis. The main feature is that the full bridge rectifier side voltage is formed passively through the conduction of the diodes, hence, the control of the converter is very simple. However, the topology in Fig. 2. 1 needs active control of all the switches which requires additional control loops.

A dc-dc converter having a similar circuit to the Fig. 2. 2 is proposed with multiport functionality [14], [15]. A high frequency transformer isolates the primary and secondary while, two inversely coupled inductors are placed in the primary and secondary. The coupled inductors create a high inductance (boost inductance) path when the two ports on primary or secondary operates in the boost mode. The same inductors create a low inductance (leakage or power transfer inductance) path when the converter exchanges power between the primary and secondary. The winding arrangement presented by the work is very useful when interfacing two dc voltage levels in a multiport converter. The single phase circuit of the converter presented in the thesis is the same as in [14], [15] without the two coupled inductors and is able to create high and low inductance paths for current between the inverter legs and the grid current respectively.

2.3 3-PHASE, 1-PHASE SINGLE-STAGE AC-DC CONVERTERS

Single-stage ac-dc converters process power from ac supply to dc output in a single power conversion step. Several single-stage converter topologies are described highlighting the key features compared to the converter under consideration.

Single-stage power processing bring about several benefits to the converter. Given properly designed, the number of active switches can be reduced compared to two stage ac-dc converters. Further, magnetics can be integrated with flux cancelling techniques to lower the size and weight of the converter. In a conventional two stage ac-dc converter the intermediate energy storage dc link, which comprise of a dc inductor and a filter capacitor, may add extra weight and cost given the power rating. Moreover, the dc link voltage needs to be regulated using an active front end converter for a wider output range. However, a single-stage converter can be designed eliminating the large and bulky dc inductor and filter capacitor which results in lower size and overall cost.

The converter in Fig. 2. 1 has already been studied as a single-stage dc-ac converter [22]. The use of bidirectional switches and the dq-axis control easily allows for single-stage ac-dc operation. In contrast to pulse separation operation presented in the thesis, reference signals are phase shifted keeping the carries the same to achieve power exchange. The controller-wise limiting factor for power transfer is the amplitude of the 2kHz sine wave which modulates over the 60Hz grid modulating signal. A tradeoff has to be made between the peak value of the grid side modulating signal and the 2kHz sine wave. The grid modulating signal is linked with the respective dc link voltage hence, the dc link voltage should be sufficiently large for the differential mode power to pass through the 2kHz sine wave.

The closest topologically similar single-stage converter is published in [2], [3] with high frequency isolation and voltage phase shifting. The work uses external inductors for power transfer and carrier phase shift to implement voltage separation between the primary and secondary. In contrast to the carrier phase shift modulation methodology used in [2], [3] the proposed converter uses a reference modification based phase shift

and a fixed zero degree carrier throughout the system. Although the topology uses 24 switches, it can operate as a multiport converter with 4 bidirectional ports. A single phase variant of the same topology is researched in [17] and the publication uses two coupled inductor based high frequency transformers. It is not explicitly mentioned about the power transfer inductance, yet from the diagram it is evident that the transformer leakage is being used for the power transfer. The major distinction between [2], [3] and the thesis work is the way the high frequency voltage pulses are arranged. The thesis focusses on positioning high frequency voltage pulses in such a way that the occurrence of reactive content is minimized in the converter, see Fig. 1. 10

Single-stage ac-dc power transfer can also be achieved by using 3x2 ac-ac matrix converter based DAB circuit topologies [18], [23], [19]. The key feature of using matrix based front end converter is that the large dc link electrolytic capacitor can be removed and replaced with smaller size LC input filters [18], [19]. Only 16 active switches are required for a three phase single-stage ac-dc matrix structure based converter. Another merit is that all the switches can achieve full zero volage switching hence, reduced switching losses. However, these topologies lack multiport connectivity which is an important feature of the converter under consideration.

Another single-stage single-phase converter topology based on T-type NPC is proposed in [20] which constitute a high frequency transformer and a coupled inductor. The coupled inductor helps to generate 3 level voltage at the transformer primary and the power flow across the transformer is achieved through carrier phase shift. The converter presented consists of 12 switches which can be considered to be high compared to a single-phase totem pole single-stage ac-dc converter [21] which has only 10 switches. The converter is realized with 6 carriers which can potentially increase the converter control complexity. Even though single-stage power transfer is achieved, the lack of multiport functionality is highlighted when compared with the proposed converter. However, similarity exists in power transfer by the use of phase shift method.

A totem pole based single-phase single-stage ac-dc converter is presented in [21] with only 10 switches. Key features of the converter include ripple free grid current, electrolytic capacitorless implementation, and full range zero voltage switching [21].

The power transfer is controlled by the phase shift between either side of the high frequency transformer. Also, this single-stage ac-dc converter is not designed with the multiport functionality.

2.4 SUMMARY

A discussion of grid connected isolated high frequency converters is presented which are in direct comparison with the converter under consideration. An alternative current controller for the proposed converter using a 2kHz sine wave modulating on top of the 60Hz grid reference is published [22] with dq-axis power control. In contrast, a power transfer mechanism at the switching frequency is proposed in the thesis. The tradeoff among the amplitudes of 60Hz grid modulating signal and the 2kHz sine wave is the critical factor for power transfer limits in the published work [22]. Directly related work [2], [3], [16], [17] are similar to the topology presented but are not focused on the behavior of the high frequency current. Single-stage ac-dc converters alone consist with T-type NPC, totem pole converters, and matrix based converters. Totem pole and matrix converters are electrolytic capacitorless and hence, their life span is increased. The three phase single stage matrix converter has only 16 switches, but it lacks the multiport capability. The converter under consideration has the multiport functionality, transfers power at the switching frequency, integrated magnetics, three phase grid connectivity, single stage ac-dc conversion, and high frequency isolation. A similar converter topology has been published which uses external inductors for power transfer however, focus is not given to better arrange the high frequency voltage pulses.

Chapter 3

3-Φ BIDIRECTIONAL SINGLE-STAGE ISOLATED AC-DC CONVERTER

A Comprehensive discussion of the converter topology, its operation and performance characteristics are presented. Starting from the DAB, the operating principle, power transfer mechanism and modulation methods closely associated with the converter are discussed. The concept of reference-based pulse position (RPP) is illustrated and discussed which constitute the contribution of the thesis. Furthermore, a brief discussion about the coupled inductor magnetics is provided. Also, mathematical derivations are provided that describes the power flow and currents in the system. Simulated performance curves which demonstrate the converter operation are presented and compared with the other modulation methods. Lastly, control response for transient behavior is presented with simulated waveforms.

3.1 DAB OPERATING PRINCIPLE

To understand the operation of the converter, it is first required to understand the operation of the DAB converter. Therefore, a brief discussion of the basic pwm process is illustrated in this section.

The DAB dc-dc converter consists of two active H-bridges with separate dc links. The two bridges are isolated by a high frequency transformer. Generally, an external inductor is used as the power transfer inductance however, it is also possible to use the leakage inductance of the transformer for the same purpose. The schematic shown, Fig. 3. 1, uses an external inductor for the explanation.

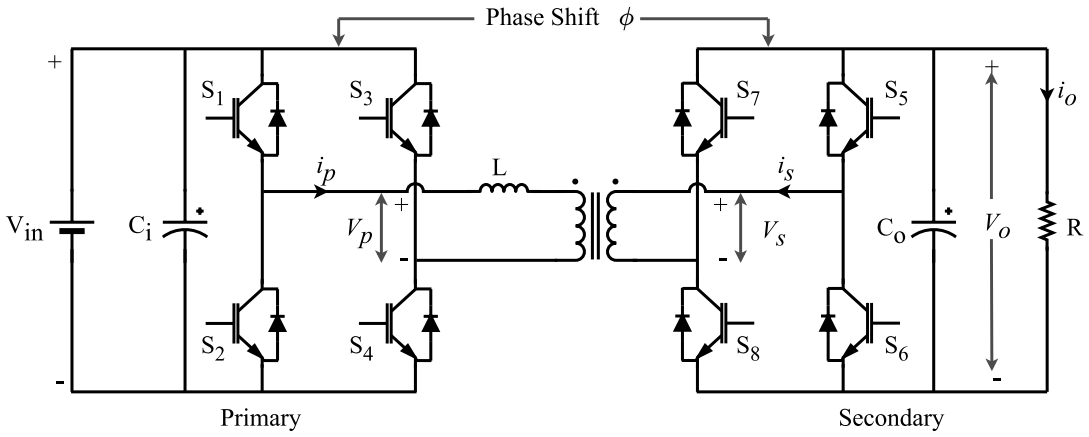

Fig. 3. 1. Circuit schematic of a DAB dc-dc converter.

The switches in a leg operate complementarily, for example S_1 and S_2 operate in complement, and the switches in a bridge turn on diagonally, S_1, S_4 and S_2, S_4. Both the bridges operate in the same way, but the secondary is operated with a phase shift φ. The switching pattern generates a square wave voltage $+V_1$, $-V_1$ across the transformer primary (V_p) and $+V_2$, $-V_2$ across the secondary (V_s), where V_1, V_2 being the primary and secondary dc link voltage values. The switches are modulated with 50% duty resulting in voltage waveforms having the same duty. The phase shift is achieved simply by shifting the secondary carriers with respect to the primary with the required phase shift. The phase shifted voltage waveforms creates a differential volage (V_L) across the inductor L, hence, drive a current i_p through the inductor, Fig. 3. 2.

The principle of operation of the dc-dc DAB converter is the phase shifting of secondary voltage waveform relative to the primary to obtain a bidirectional power flow. A phase shift controller can be designed to control the output voltage V_o by controlling the phase difference. Further, the power transfer occurs at the switching frequency and is non-linearly proportional to the phase shift.

The important takeaway from this section is the pwm operation of a DAB dc-dc converter since the DAB modulation method is compared with thesis research work.

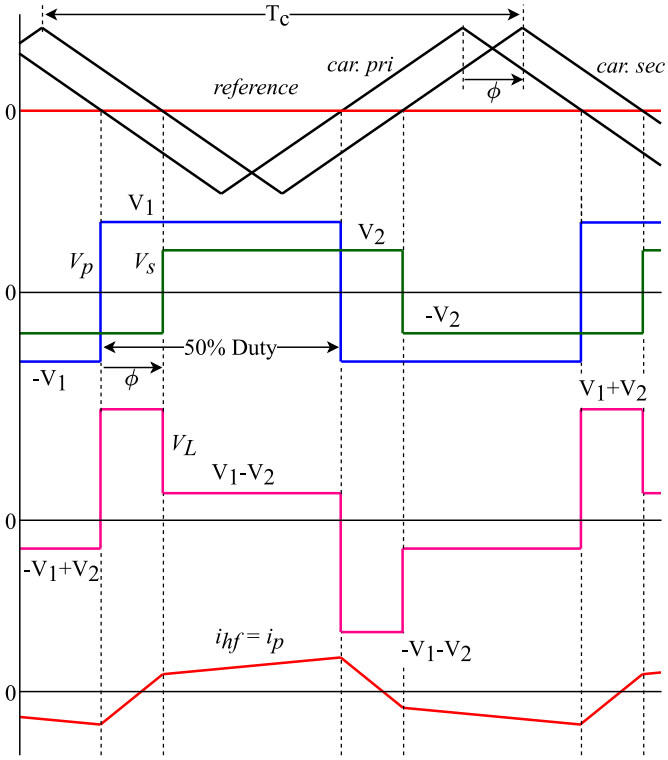

Fig. 3. 2. Switching waveforms of the DAB converter.

3.2 CONVERTER TOPOLOGY

The topology of the single-stage isolated ac-dc converter is described. The circuit, components, and features of the converter are presented.

Two three-phase 2-level voltage source converters (Inverter 1, Inverter 2) are connected in parallel with a shared dc link on either side of the high frequency transformers. An electrolytic capacitor is used for the primary dc link while a filter capacitor is used at the secondary dc link. The primary side connects to a three phase grid and three high frequency transformers are being used for isolation. The secondary side is connected to a battery (V_b) to demonstrate the use case of the converter as a battery charger. The transformer primary windings are connected in such a way to cancel the 60Hz flux produced by the grid current. The flux cancellation is achieved

through the coupled inductor characteristic of flux cancellation by two windings wound in a single core having opposite polarities [12]. IGBTs are used for the active switches hence, bidirectional power flow can be achieved. The primary and secondary windings are wound on the two limbs of the high frequency transformer. Both the primary and secondary have the same number of turns. The grid is connected at the center tap of the primary winding with line filter inductor L_g. As the power transfer inductor, the transformer interlimb inductance is being used allowing for the reduction of the magnetics involved and thereby reducing the size, weight, and cost of the converter. The two parallel converters share the grid current equally thus, the current stresses of the switches are halved. The voltage stresses at the windings are reduced since the voltage waveform is a 3-level waveform which is produced by the interleaved switching legs.

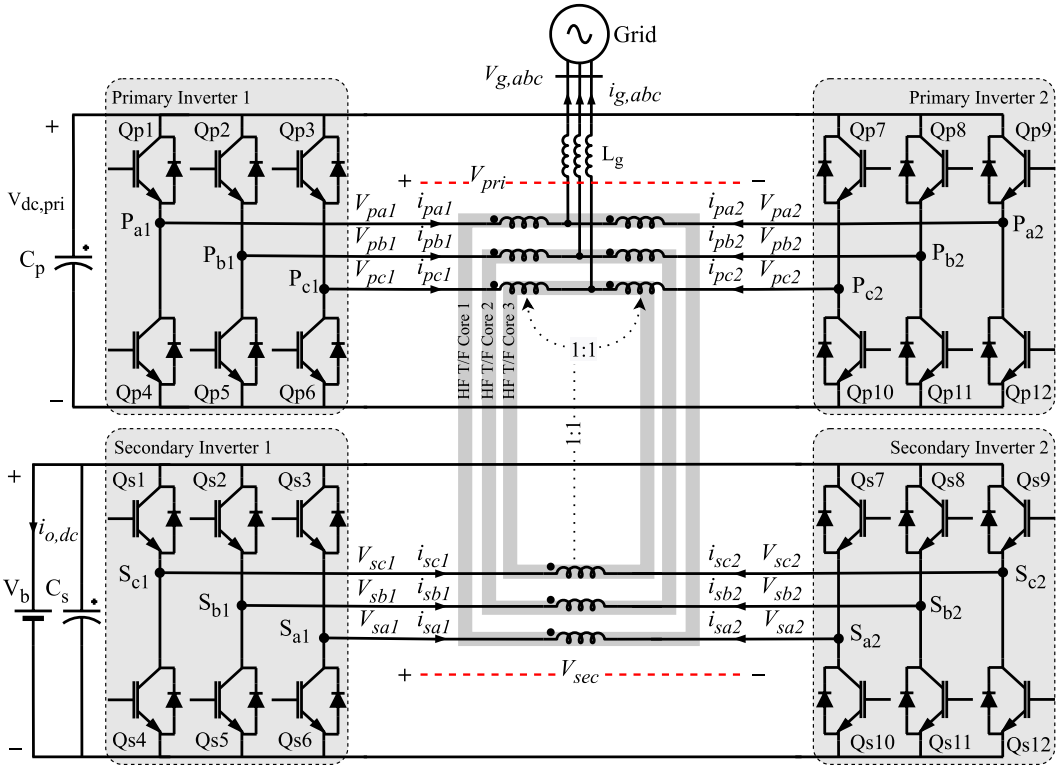

Fig. 3. 3. Schematic of the converter.

The features of the converter include:

- Single-stage ac-dc power transfer
- Bidirectional power flow
- High-frequency galvanic isolation
- Three phase grid connection
- Multiport power converter structure
- Reduced switch voltage and current stresses

3.3 PRINCIPLE OF OPERATION

The section provides details of how the converter operates in general. The basic modulation, operating regions, common mode circuit, differential mode circuit, and primary winding flux cancellation are described.

3.3.1 Basic Modulation

The principle of operation is described considering only the phase A of the circuit due to the symmetric nature of the converter. The analysis of the other two phases follows the analysis of phase A, Fig. 3. 4. The leg group 1 of both primary and secondary is modulated with 0 degree carrier while the leg group 2 is modulated with 180 degree carrier. The two legs in each side function as interleaved inverter legs. Further, both the primary and secondary legs are modulated with the same reference signal. The bottom switch of each leg is gated with the complement signal of the top switch and a dead time is implemented to avoid shoot through.

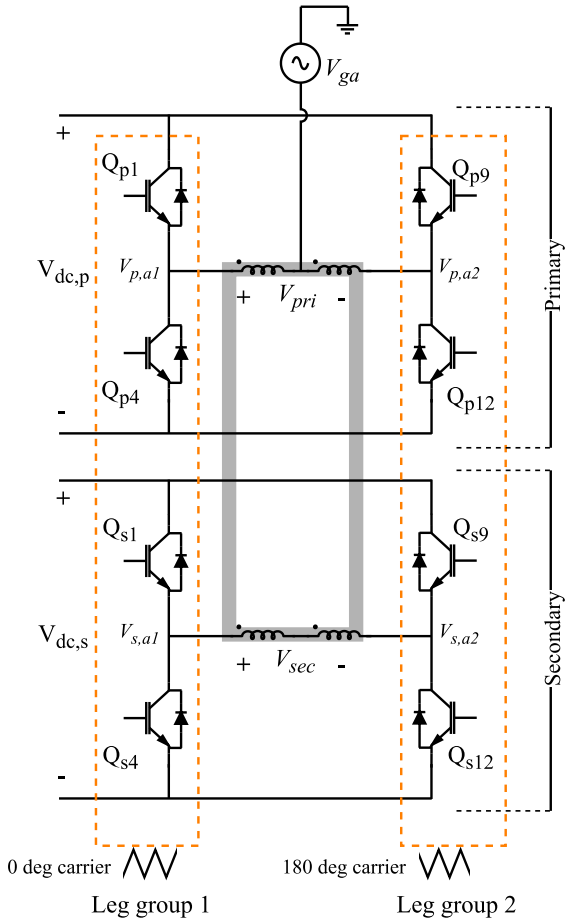

Fig. 3. 4. Phase A equivalent circuit.

The pwm modulation in the primary side can be illustrated with 0/180 degree carriers and the phase A reference ref_a, Fig. 3. 5, and the modulation for the phases B, C follows the same pattern. A three level voltage is generated at the primary of the transformer when the ref_a is compared with the respective carriers. At the secondary side a phase shift is implemented on the V_{sec}. The phase shift can be implemented by shifting the carriers or by modifying the reference signal. The phase shift methods are discussed in the following section, however, to describe the operating principle it is sufficient to consider phase shifted waveforms.

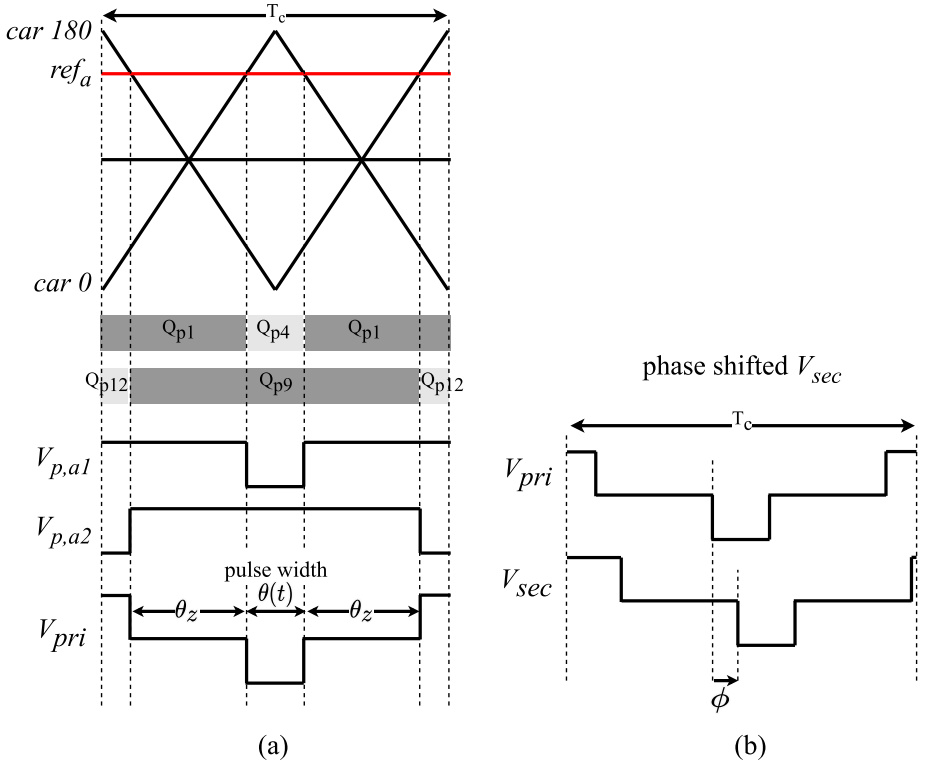

Fig. 3. 5. Switching waveforms and phase shift of primary phase A (a) primary side switching pwm waveforms, (b) phase shift φ implemented on the secondary voltage V_{sec}.

3.3.2 Operating Regions

The reference signal ref_a is a sinusoidal signal that varies its amplitude over time. Thus, the pulse width varies with time since it is directly related to the value of the reference signal at the moment of comparison with the comparator. Considering the pulse width and the phase shift, the whole operation under a low frequency fundamental period can be divided in to three regions, Fig. 3. 6. These three regions are sufficient to study the high frequency current. In the first operating region, the phase shift (φ) is less than the pulse width (θ) and zero voltage duration (θ_z). When the reference signal approaches zero, the phase shift can be larger than θ_z and a differential voltage with levels of V_1+V_2, V_1-V_2, $-(V_1-V_2)$, $-(V_1+V_2)$ can be generated across the inductor. These voltage levels appear in the second region. In the third region, voltage pulses of V_{sec} are completely separated from each other. In this region the high frequency current does

not have a grid or battery induced voltage hence, the current circulates within the converter generating reactive power.

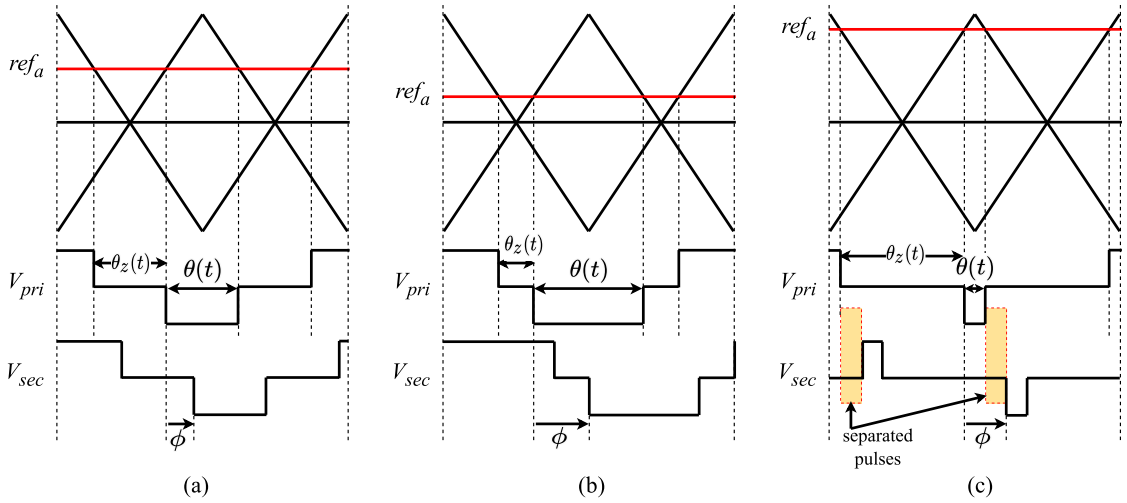

Fig. 3. 6. The three operating regions (a) φ<θ; φ<θ$_z$, (b) φ<θ; φ>θ$_z$, (c) φ>θ. Phase shift in (a) and (b) is less than the pulse width while in (c) phase shift is larger than pulse width.

Phase shifted pwm is the mechanism by which the power is exchanged between transformer primary and secondary. If the phase angle difference of secondary with respect to the primary is negative (leading angle) the power is transferred from primary to the secondary. If the phase difference is positive, the power flow is reversed. The concept can be simply illustrated as in Fig. 3. 7. The active power flows from the higher voltage angle to the lower voltage angle through the impedance X_L, in the figure, the active power flows from source 1 to source 2.

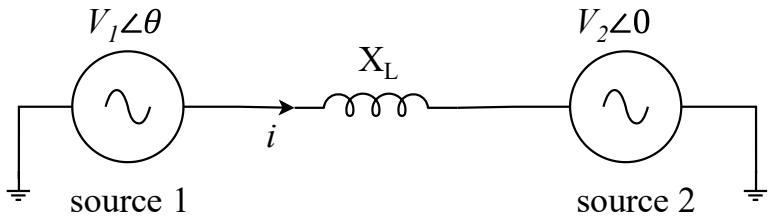

Fig. 3. 7. The active power flows in the direction from higher voltage angle to the lower voltage angle through the impedance X_L.

3.3.3 Common Mode and Differential Mode Circuits

The overall power flow in the converter system can be studied dividing the converter into two circuits as common mode (CM) and differential mode (DM), Fig. 3. 8, Fig. 3. 9. The CM circuit exchange power with the grid and the primary converter. The CM current ($i_{cm} = i_g$) is the sum of inverter output currents (1), and the CM voltage is the average sum of the primary inverter output voltages (2). Only the primary inverters are involved in the CM circuit. The common mode circuit absorb power from the grid and momentarily stores in the primary capacitor. The stored energy is passed on to the secondary side at the proper switching instance establishing a power transfer.

$$i_{cm} = i_g = i_{p1} + i_{p2} \tag{1}$$

$$V_{cm} = \frac{V_{p1} + V_{p2}}{2} \tag{2}$$

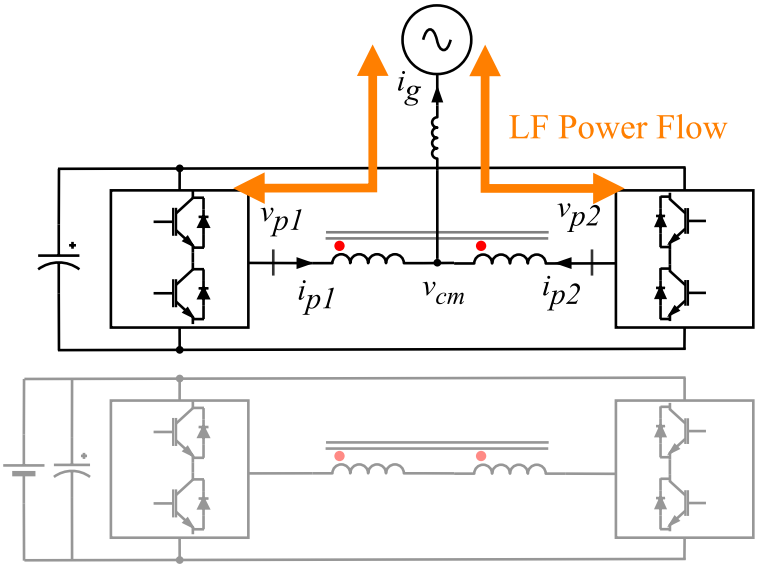

Fig. 3. 8. The common mode circuit of the converter for the phase A. The circuit is the same for phases B, C.

The DM circuit on the other hand exchange power with the primary and secondary via the high frequency transformer. Both primary and secondary inverters are involved but, the grid connection is not involved in the DM circuit. The DM circuit can further be

simplified, Fig. 3. 10, considering its transformer action. Fig. 3. 9 can be redrawn as in Fig. 3. 10 (a) which has simplified the high frequency transformer windings, primary and secondary differential voltage, and the DM current in primary and secondary. Employing the transformer T model, Fig. 3. 10 (b) is arrived. The inductors $L_{lk,p}$, $L_{lk,s}$ represents the primary and secondary leakage inductances. The magnetizing inductance of the transformer is sufficiently large so that it can be neglected, and a simplified transformer model can be derived for the DM circuit, Fig. 3. 10 (c). In the simplified model, the primary and secondary voltages represent high frequency 3-level voltage waveforms represented by different regions in Fig. 3. 6, L_{lk} represents the total leakage and i_{hf} represents the high frequency current. The equations (3)-(6) represents the DM quantities. In the subsequent power transfer analysis of the converter, the simplified transformer model, Fig. 3. 10 (c), is used.

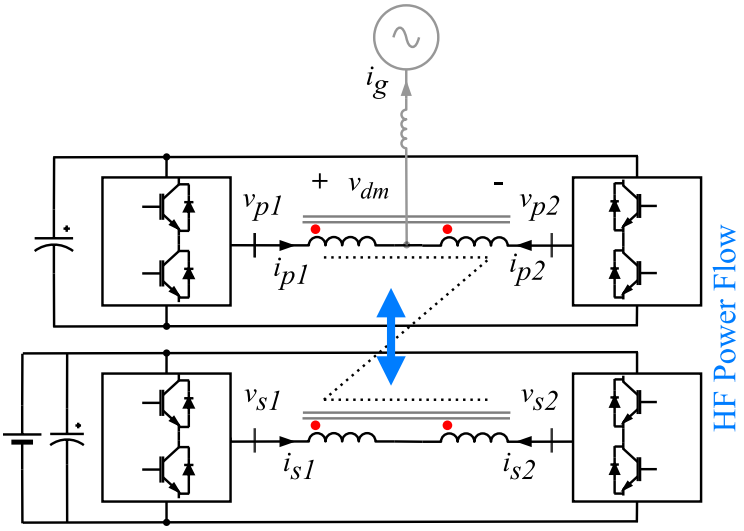

Fig. 3. 9. The differential mode circuit of the converter for the phase A. The circuit is the same for phases B, C.

$$V_{dm,p} = V_{pri} = V_{p1} - V_{p2} \tag{3}$$

$$V_{dm,s} = V_{sec} = V_{s1} - V_{s2} \tag{4}$$

$$i_{dm,p} = \frac{i_{p1} - i_{p2}}{2} \tag{5}$$

$$i_{dm,s} = \frac{i_{s1} - i_{s2}}{2} \tag{6}$$

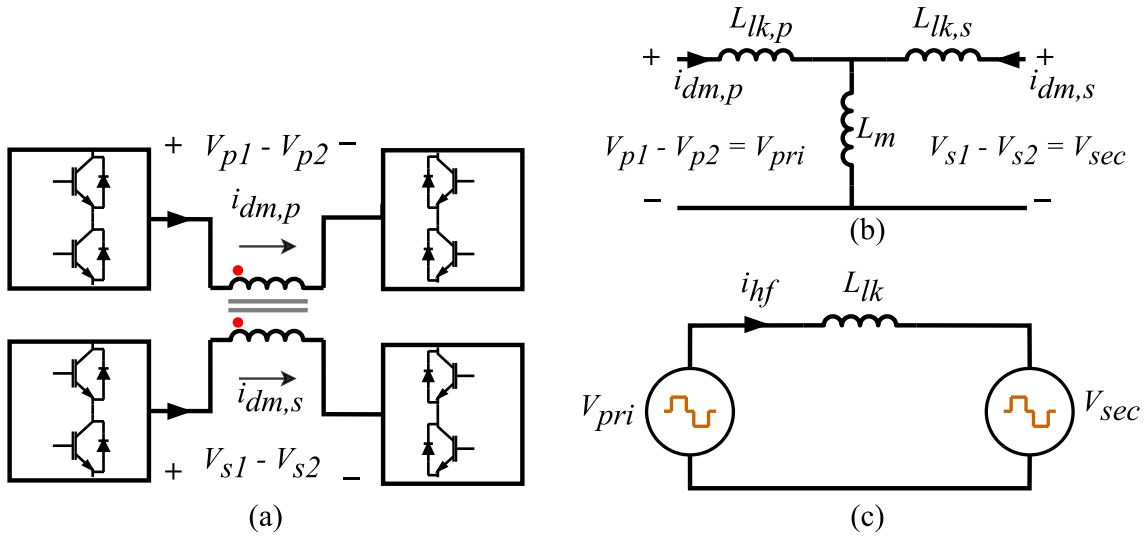

Fig. 3. 10. Simplification of the DM circuit into an equivalent transformer model.

3.3.4 Power Balance

The converter power balance is established with proper control. The primary dc power port consists with a capacitor and its voltage is controlled with the grid current using a voltage controller. On average the power absorbed and delivered by the primary capacitor is zero since its voltage is being controlled to a fixed value. Thus, the power absorbed from the grid is transferred to the secondary less the losses in between. The same is true for the reverse power where the power from the secondary dc port is transferred to the grid while the primary dc link holds zero average power.

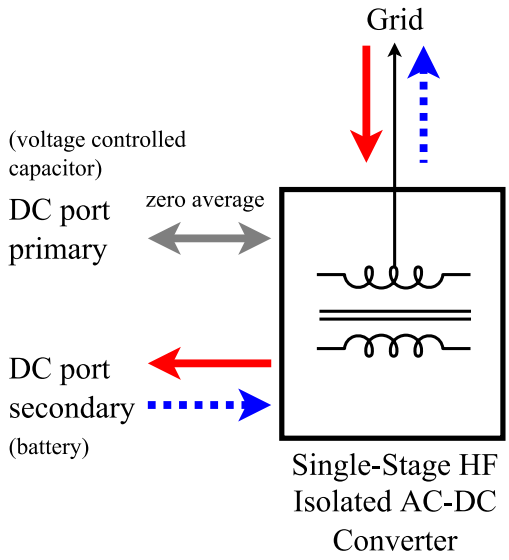

Fig. 3. 11. Power balance of the converter.

3.3.5 Flux Cancellation

The transformer primary windings are arranged in such a way that the 60Hz low frequency flux get cancelled in the core while remaining the high frequency flux. Thus, the transformer can be sized only to handle high frequency flux vastly reducing its size. Solving (1) and (5) the inverter output currents can be defined as (7) and (8).

$$i_{p1} = \frac{i_{cm}}{2} + i_{dm,p} \tag{7}$$

$$i_{p2} = \frac{i_{cm}}{2} - i_{dm,p} \tag{8}$$

Both i_{p1} and i_{p2} have half the CM current. The DM current is added to and subtracted from the inverter output currents. On the P_{a1} winding side, CM flux (φ_{cm}) and DM flux (φ_{dm}) flows in the same direction inside the core based on the winding dot notation. However, on the P_{a2} winding side, the CM and DM flux directions are opposite. The total CM flux in the core get cancelled due to their opposite polarity produced by the half the grid current in i_{p1} and i_{p2}. In contrast, the DM flux flows in the same direction

within the core due to the additive polarity caused by the DM current in the primary windings, Fig. 3. 12.

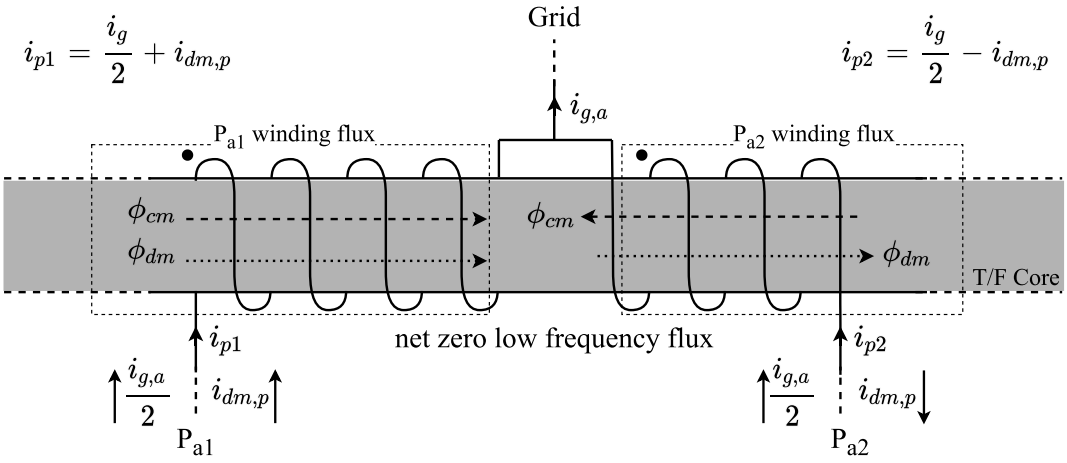

Fig. 3. 12. CM and DM flux inside primary limb of the transformer.

3.3.6 Control Aspects

The primary dc link capacitor voltage is controlled to be the same as the battery voltage in the secondary side and the voltage is controlled through the grid current. When two dc link voltages are equal, the high frequency current is symmetrical and has the lowest rms value. In the case of different voltage levels, transformer turns ration can be adjusted to match the two dc link voltages.

The grid current is controlled with a dq-axis current controller to obtain power factor corrected (unity power factor) current with the grid phase voltages. Further, the primary side voltage and current controllers are decoupled from the secondary side controllers. The secondary consists of the phase shift control algorithm which aligns the secondary high frequency voltage with the primary. Moreover, secondary dc output current, output power, and output voltage are controlled based on the requirement.

3.4 MODULATION METHODS

Different modulation methods that can be used to operate the converter are described. Three main methods are discussed; fixed phase shift (FPS), reference based pulse position (RPP), and square wave pulse position (SPP). A fourth conceptual method, Constant peak current modulation, is presented but it not tested. The modulation method determines the performance of the converter and helps to achieve specific goals desired from the converter.

3.4.1 Fixed Phase Shift (FPS)

The FPS methods, as introduced in Section 1.4, holds the phase shift between the primary and the secondary high frequency voltage waveforms to be a fixed value at the steady stage operation (during the transients the phase shift changes its value and when the steady state is reached the phase shift remains fixed at a certain value with a narrow bandwidth). Published literature mostly use carrier phase shifted pwm in order to achieve the required phase shift. The carrier phase shift can be easily implemented in modern hardware and requires no additional computation. However, one down fall is the phase shift is implemented at the carrier minimum in most hardware present today. For example, the PLECS RT Box, TI DSP, they implement the carrier phase shift at the minimum value of the carrier. In the case of PLECS RT Box, the user (simulation) does not have access to the carrier since the carrier is generated separately with in the Box.

Similar work published in [2], [3] have the same operation as a fixed phase shifted carriers. However, the literature implements a second phase shift in the carriers in order to align the primary and secondary voltages. This second phase shift involves in changing the carrier frequency of the secondary carriers and may increase the complexity of the controller. If the three operating regions, Fig. 3. 6, described in Section 3.3 is maintained as it is throughout the period of the low frequency reference without any modification to the pulse separation between primary and secondary, it is defined as an FPS pwm modulation in the thesis. A typical carrier phase shifted pwm waveforms of primary and secondary voltages are presented in Fig. 3. 13.

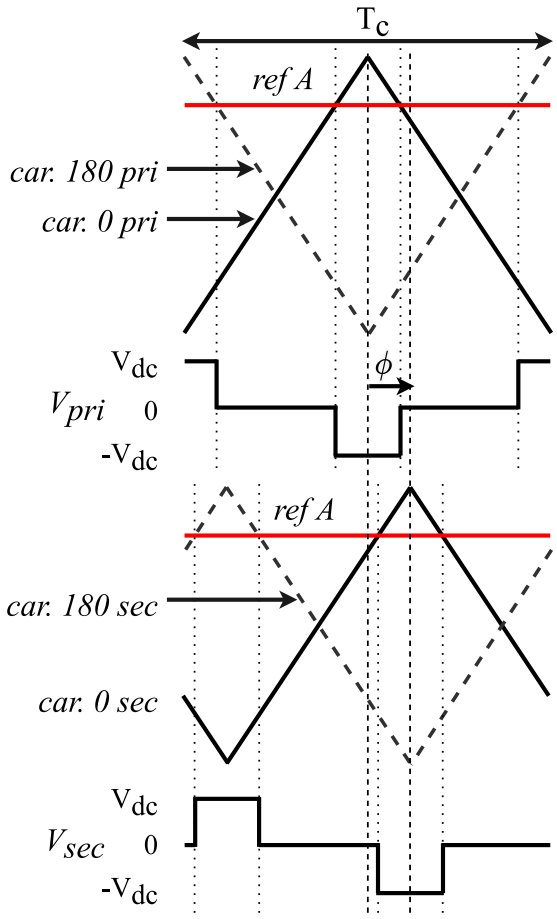

Fig. 3. 13. A typical carrier phase shifted pwm method. both the primary and secondary have the same reference.

3.4.2 Reference-based Pulse Position (RPP)

The simple definition of the RPP method is a pwm method that operates in the regions (a) and (b) of Fig. 3. 6 all the time within a 60Hz low frequency sinusoidal varying reference. This method, which is the contribution of the thesis, eliminates any occurrence of region (c) by means of aligning the shorter voltage pulses next to each other. By aligning the voltage pulses next to each other (eliminating separation between the pulses), the converter can reduce the reactive content of the high frequency current. Further, the rms of the high frequency current can also be reduced. Typically, the pulse separation is limited to 30-40 degrees and the modulation index is limited to 0.8 [3].

However, for reduced dc link voltage, for example using third harmonic added SPWM, the modulation index can reach to 0.9 or above to provide a better utilization of the dc link. When the modulation index is high enough shorter pulses are generated, and if the pulse separation is greater than the pulse width then there is a chance for the occurrence of the region 3 waveforms.

An example illustration of the operation of the RPP method is shown in Fig. 3. 14. The two main variables to consider is the phase shift (φ) and the pulse width (θ). When the pulse widths are larger than the phase shift, the voltage pulses are separated by the corresponding phase shift, Fig. 3. 14 (a). However, if the phase shift is greater than the pulse width, the pulses are separated from each other, Fig. 3. 14 (b). The RPP method brings back the secondary voltage pulse next to the primary by means of dynamically adjusting the pulse separation. The adjusted pulse separation is equal to the pulse width that exists at the instant of making the adjustment, Fig. 3. 14 (c).

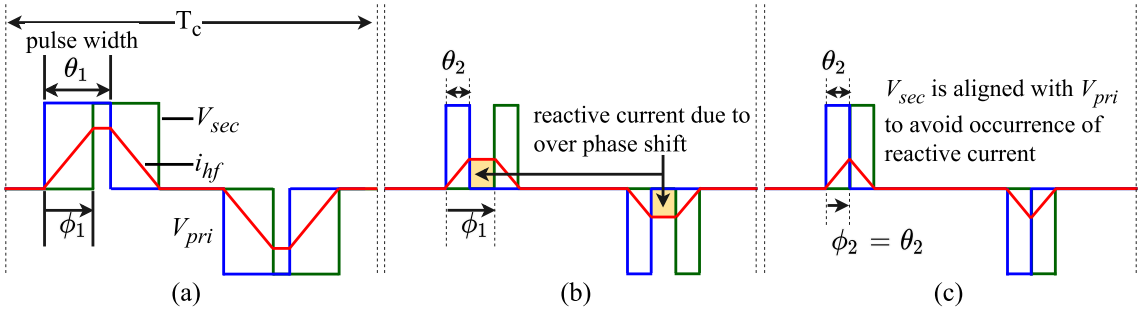

Fig. 3. 14. Concept illustration of the RPP method.

3.4.3 Single Carrier Modulation

The RPP method is implemented with a single carrier (0°) instead of using phase opposite carriers (0°/180° degree). The same pwm operation with dual carriers can be achieved with single carriers by means of,

- Feeding the negative reference to Inverter 2
- Reversing polarity of Inverter 2 pwm output

A single carrier is used to reduce the complexity of the control algorithm and to assist easier operation of dynamic pulse separation. The negative of the time varying reference signal *x(t)* is supplied to the Inverter 2 and its pwm logic is inverted. The end result is exactly the same as using two carrier and one reference.

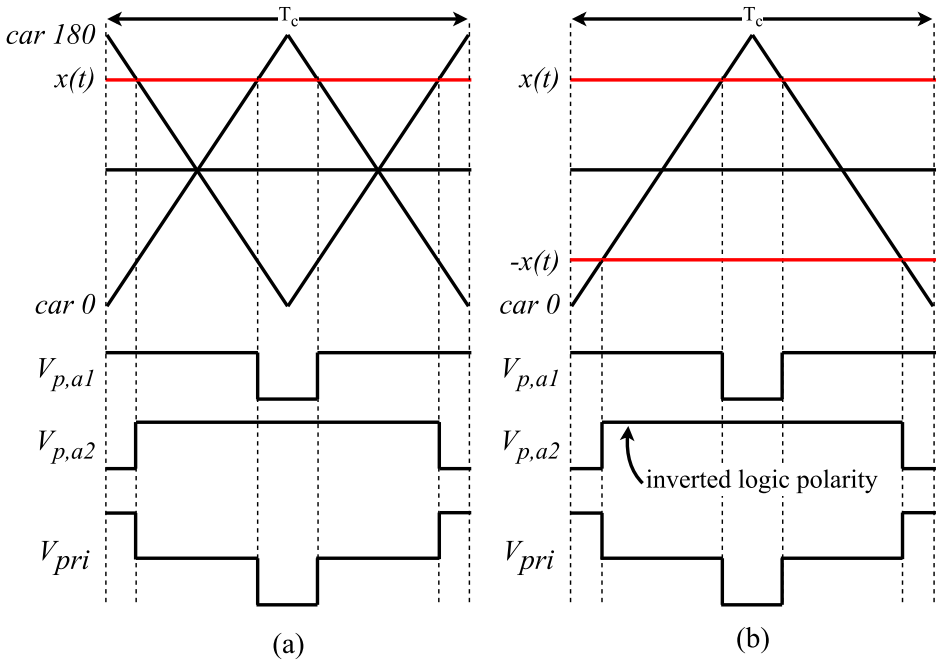

Fig. 3. 15. Single carrier pwm operation. (a) dual carrier operation with 0°/180° carriers, (b) single carrier operation with only 0°. The pwm logic for the negative reference (*-x(t)*) is inverter in the single carrier pwm method.

An expression for the pulse width can be derived based on the carrier and reference in Fig. 3. 16. The triangles CDE and CGH are similar triangles. Applying rule ratio of sides for similar triangles one can derive following expression. Where θ° represents the pulse width in degrees, and *x* represents a third harmonic added sinusoidal waveform with angular frequency $\omega_m = 2\pi f_m$. f_m is the frequency of the grid voltage (60Hz). The carrier waveform has a frequency f_c with period T_c. The m_a represents the modulation index of the fundamental sinusoid.

$$\frac{ED}{HG} = \frac{CD}{CG}$$

$$\frac{\frac{t_1}{2}}{\frac{T_c}{2}} = \frac{1-|x|}{2} \tag{9}$$

$$\frac{t_1}{T_c} = \frac{1-|x|}{2} \tag{10}$$

$$\theta° = \frac{1-|x|}{2} \times 360° = (1-|x|)180° \tag{11}$$

$$x = m_a \sin(\omega_m t) + \frac{m_a}{6} \sin(3\omega_m t) \tag{12}$$

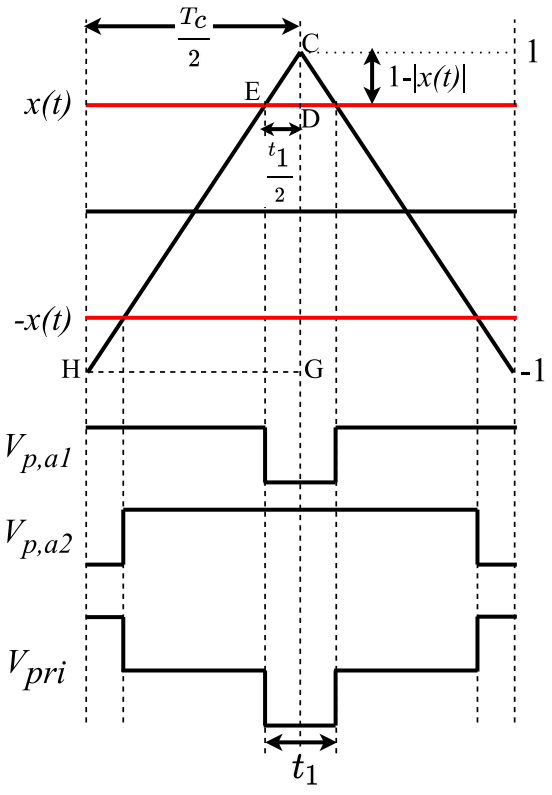

Fig. 3. 16. Pulse width and reference relationship.

The equation (11) reflects that the pulse width of the high frequency voltage waveform changes with the value of the reference signal, Fig. 3. 17. Therefore,

depending on the value of the reference signal at the instant of calculation, the pulse width can take different values. Furthermore, since the reference signal is dependent upon the modulation index of the fundamental sinusoid. The change in pulse width with the fundamental cycle is illustrated in Fig. 3. 17. Highlighted in red is the portion of the pulse widths that need phase shift adjustment for a typical 40 degree phase shift. The pulse width is lower than the phase shift and hence, the waveforms behave in region 3 resulting in unwanted reactive content. Thus, the pulse separation is dynamically re-arranged to position them next to each other within the highlighted portion.

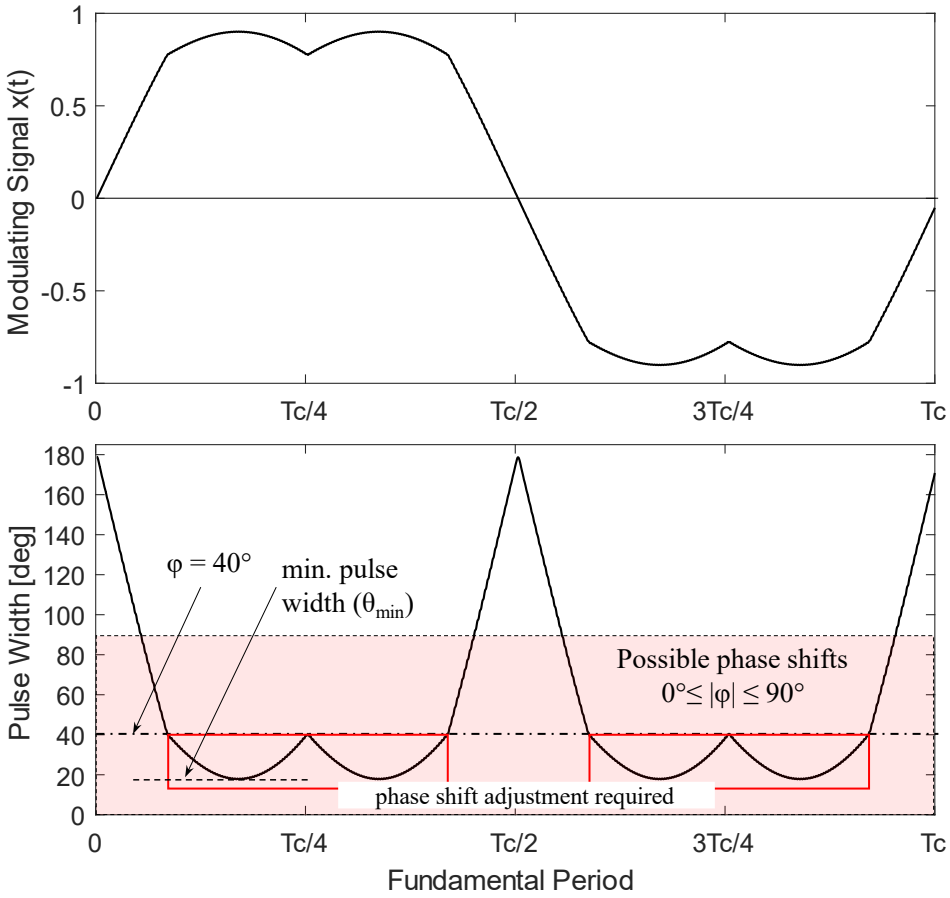

Fig. 3. 17. Change in pulse width with grid fundamental period.

As mentioned earlier, the pulse width varies with the modulation index. The minimum pulse width for a corresponding modulation index can be calculated using (13). Where m_a represents the modulation index of the fundamental component and lies

in the range [0, 1.15]. the minimum pulse width is negatively proportional to the modulation index and vary as shown in Fig. 3. 18. If for example when modulation index is 0.95 the minimum pulse width is 31.3°. And if a pulse separation of 60° is implemented, the portion of the pulse widths which are below the 60° pulse separation are aligned next to each other without letting them separate. For any modulation index, the pulse widths vary from 180° to θ_{min} (as the example shows in Fig. 3. 18).

$$\theta_{min} = \left(1 - \frac{m_a}{1.15}\right) 180° \tag{13}$$

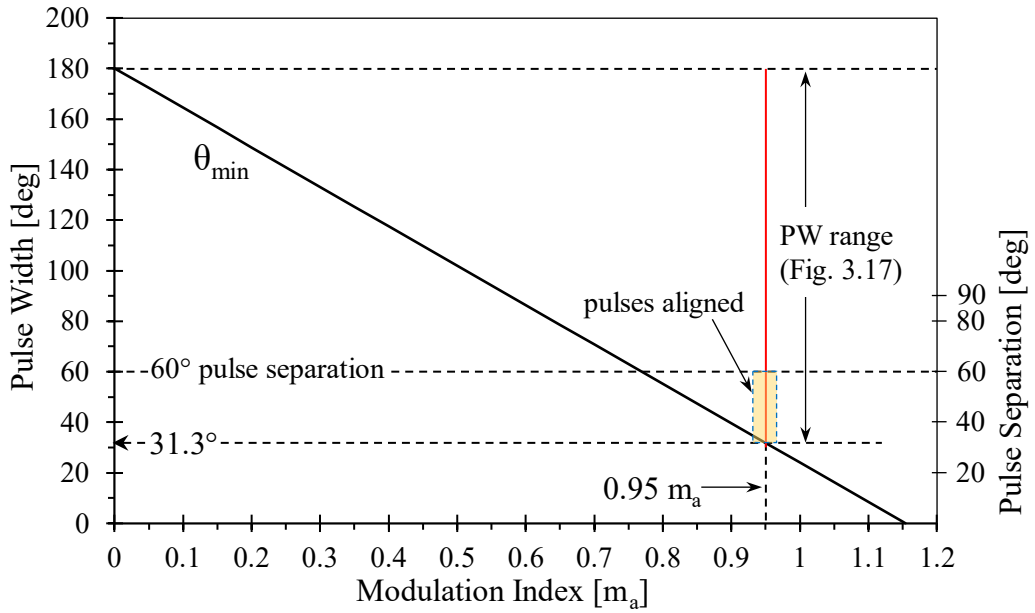

Fig. 3. 18. Pulse width variation with the modulation index.

3.4.4 Implementing Dynamic Pulse Separation

The dynamic pulse position for phase shifts greater than the pulse widths can be achieved in two ways. The first method is to implement the required phase shift in the carriers and the second approach is to modify the reference signal while keeping the carriers unmodified. The thesis work uses the second approach where the required phase shift is achieved by modifying the reference signal. The carrier phase shift can easily be implemented just by phase shifting the carriers where the required phase shift

is determined by an algorithm. The major challenge one faces when implementing the carrier phase shift is the synchronization of the carrier with the commanded phase shift (the PLECS RT box implement carrier phase shift at the minimum of the master carrier hence, the possibility of implementing the actual phase shift in the next carrier cycle. By then the reference signal may have changed to a new value). The phase shift is generated based on the reference signal value; therefore, the dynamic carrier phase shift should be implemented within the same carrier cycle before the reference signal change its value in the next carrier cycle. If the controller is unable to synchronize the phase shift, there can be separations in the voltage pulses. On the other hand, the reference modification method requires to modify the reference twice within the carrier cycle which is synced to the carrier. Thus, the implementation of the phase shift and the pulse width match very well all the time.

3.4.5 Pulse Separation by Reference Modification

The same reference signal *x(t)* is used for both the primary and secondary. The reference signal is sampled at the carrier minimum and maximum. On the primary side, at the carrier minimum a small value (*dx*) is subtracted and at the carrier maximum the same *dx* is added to the original reference. The output of the resulting pwm comparison is a phase lead voltage waveform with φ/2 angle. On the secondary side, the same *dx* is added and subtracted at carrier minimum and maximum respectively. The resulting output is a phase lagged voltage waveform by φ/2 with respect to the original pwm output, Fig. 3. 19. The dashed waveforms represent the waveforms for unmodified reference while the solid waveforms represent those of modified reference. The primary and secondary implements half the phase shift separately in opposite direction (-φ/2, + φ/2). Thus, the total phase shift is the difference between primary and secondary, which is φ, Fig. 3. 20.

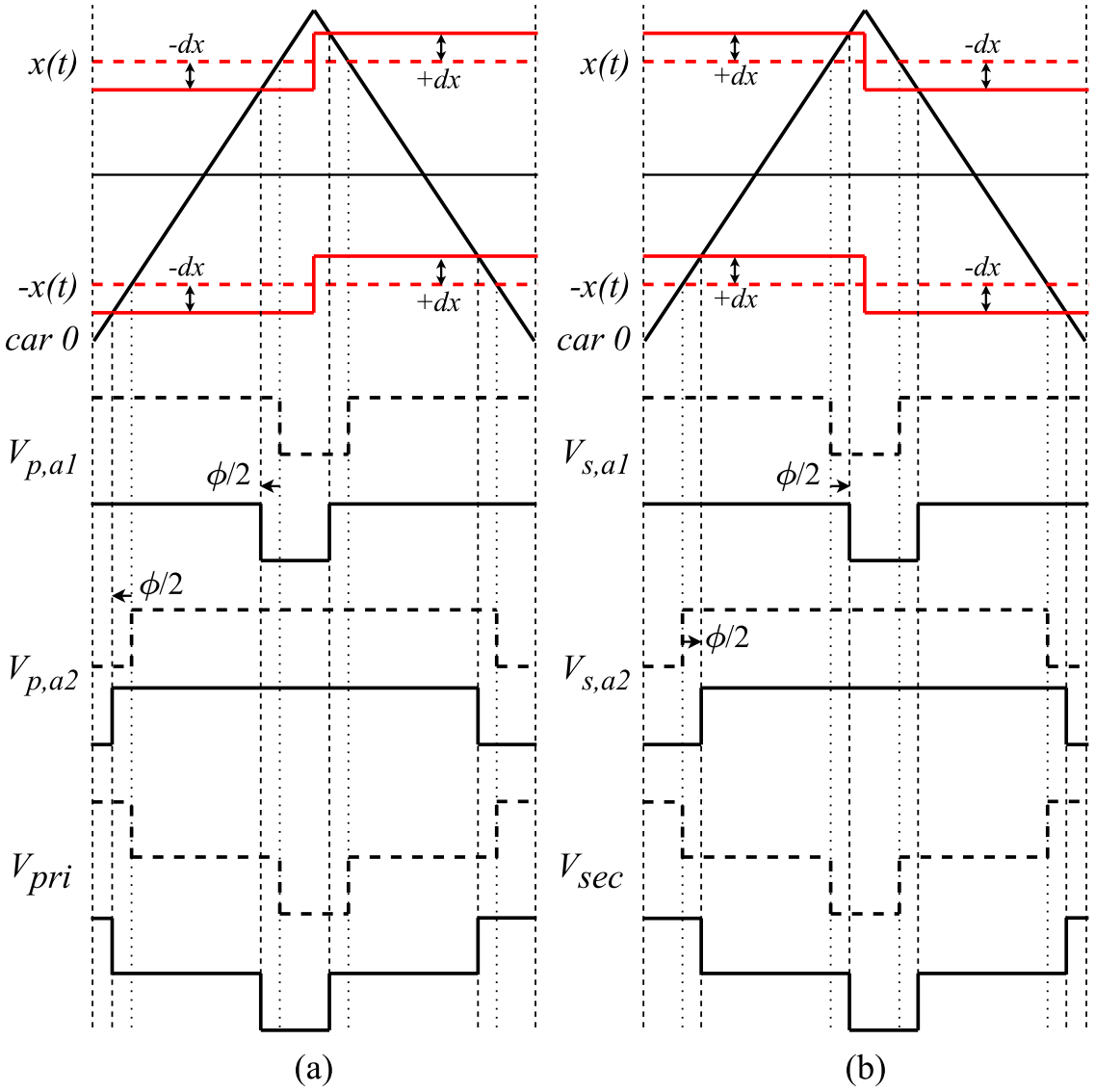

Fig. 3. 19. Pulse separation achieved through reference modification (a) modification for the primary side, (b) modification for the secondary side. The dashed signals represent waveforms of original unmodified reference, whereas the solid signals represent phase shifted waveforms of modified reference.

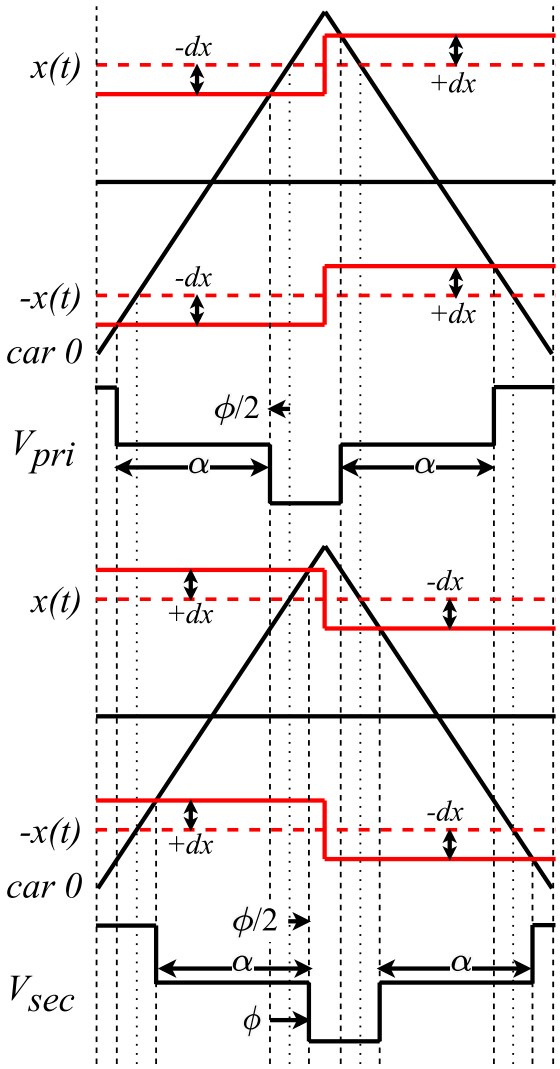

Fig. 3. 20. Total pulse separation is achieved by implementing half the separation on each side in opposite phase angle polarity.

3.4.6 Square-wave Pulse Position (SPP)

SPP method modulates the secondary high frequency voltage as a square wave (+V, -V) with 50% duty. The secondary voltage waveform is aligned with the primary all the time in each carrier cycle. The voltage alignment is achieved through an algorithm based on the primary modulating signal. The pwm operation of the SPP method is illustrated in Fig. 3. 21. The primary modulates with a single carrier as described in the RPP operation section. The secondary produces a 50% duty square wave. The reference

signal of the secondary is a ±1 square wave with the frequency equal to the carrier. The square wave is scaled with the value of the primary reference ($x(t)$) to produce a $\pm lx(t)$ square wave where $|x(t)| = |lx(t)|$. The scaling helps to align the secondary square wave with the primary to produce high frequency current illustrated in Fig. 3. 22.

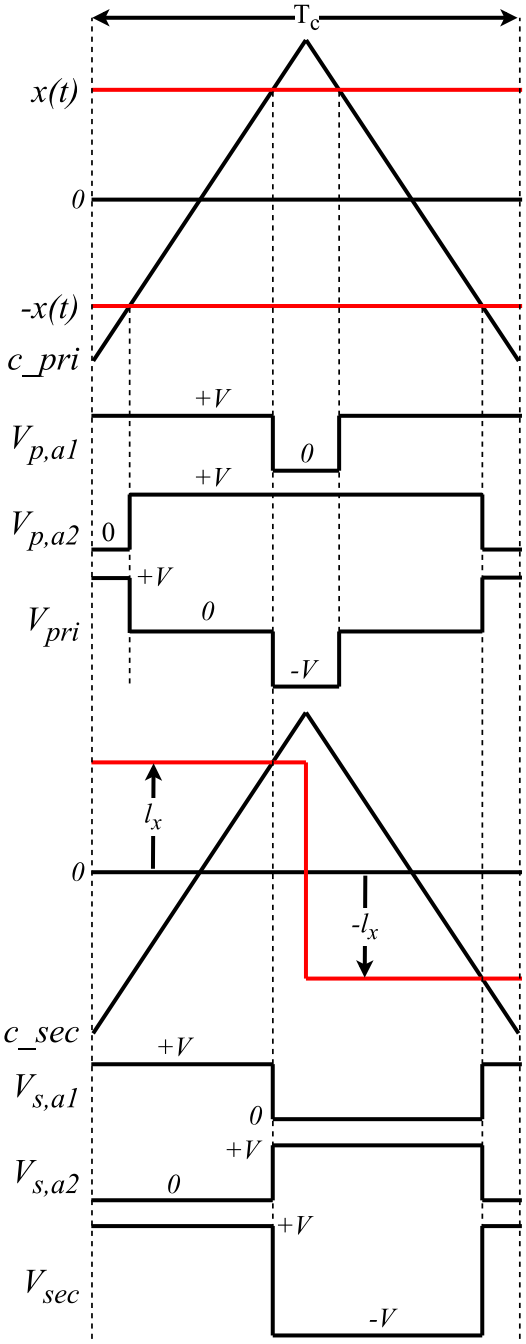

Fig. 3. 21. SPP pwm operation. Secondary reference signal is a square wave with amplitude $l_x = x$ at carrier minimum and maximum.

No phase shift is implemented on the secondary voltage waveform. In this method, maximum power can be extracted from the grid. For the duration of the primary voltage, which is formed through the grid voltage, high frequency current does not change its polarity. If the high frequency current changes its polarity the active power delivered gets lowered. A negative power quantity and a positive power quantity get cancelled, hence circulating reactive power. If the current does not change polarity for the duration of the grid volage, no power is lost and most power can be extracted from the grid.

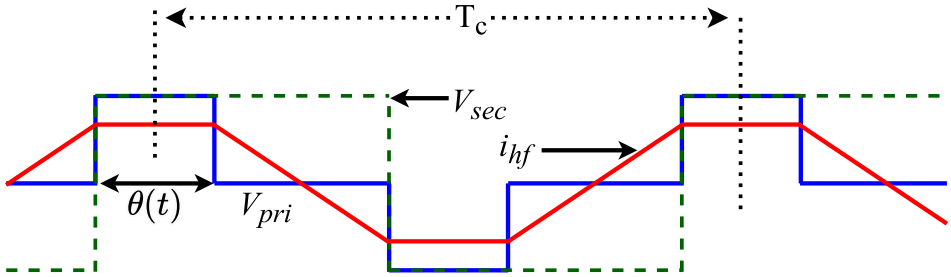

Fig. 3. 22. High frequency pwm waveforms of square-wave pulse position modulation.

3.5 MAGNETICS

Capability of using different winding arrangements, separate, and integrated magnetics are discussed in this section. The power is transferred through an inductor which can be a separate external inductor placed with a transformer or the leakage inductance of a single transformer. In the case of using a single transformer, different winding arrangements can be used to form the leakage inductance.

The first approach is to place the power transfer inductor in series with the transformer. The transformer is designed with tight coupling and with minimum leakage. The externally placed inductor is properly designed for the required power rating and phase shift range, Fig. 3. 23(a). The second approach is integrating the inductance into the transformer by means of the leakage inductance. The leakage inductance that is created as a result of winding placement on the core limbs is the

interlimb leakage inductance, Fig. 3. 23(b). A hardware example for external inductors used with high frequency transformers is shown in Fig. 3. 24.

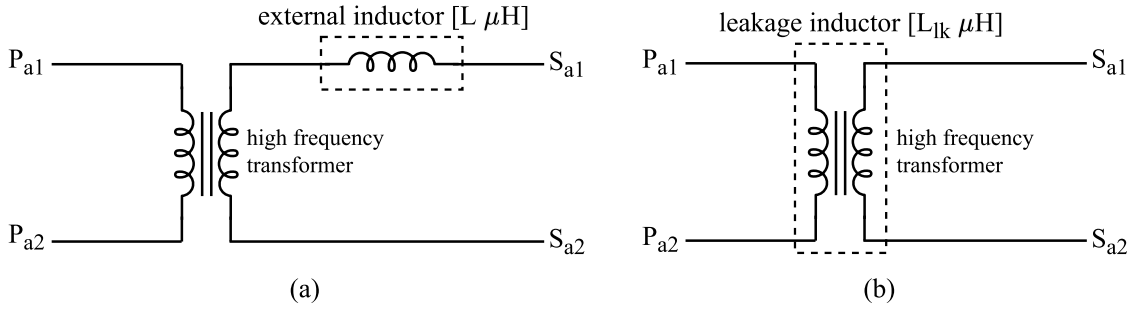

Fig. 3. 23. Power transfer inductance placement (a) as an external series inductor, (b) integrating with the transformer to form an interlimb leakage inductance.

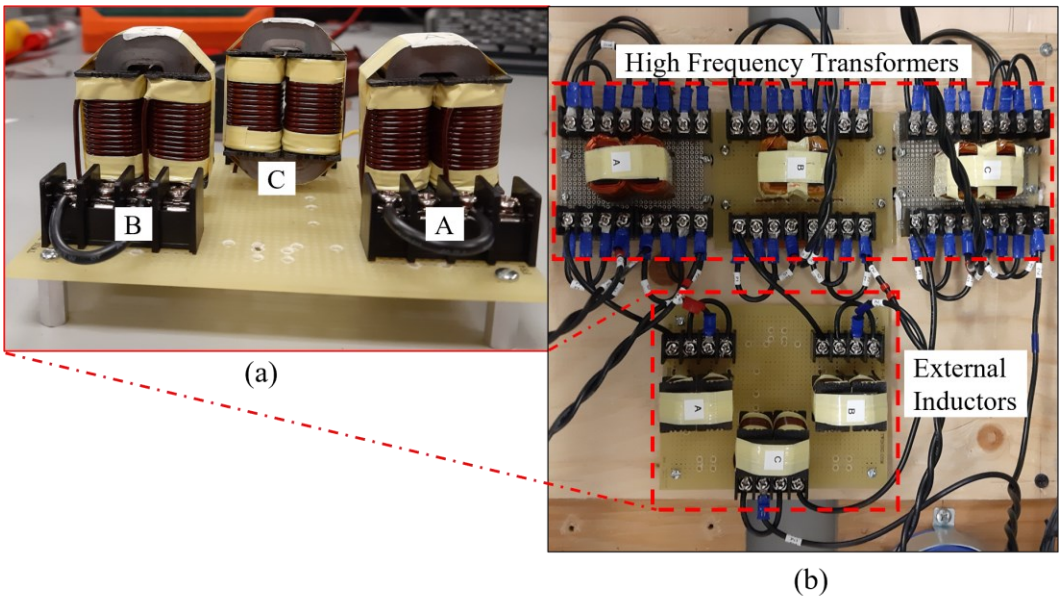

Fig. 3. 24. External inductors used with high frequency transformers. Each inductor is 100uH, 9.4A rms rated.

The second method is to use the interlimb leakage inductance of the transformer itself. To utilize the interlimb inductance the windings can be arranged in different ways which can result in different leakage inductances. For example, the arrangements illustrated in Fig. 3. 25 generates 3 interlimb leakage inductance values for the same core. Arrangement Fig. 3. 25(a) winds primary and secondary on each limb. Thus, the

magnetic coupling between the primary and secondary is very high leading to a very low leakage inductance between the primary and the secondary. Another way to arrange windings on the same limb is Fig. 3. 25(c) where the windings have strong coupling but relatively weaker than arrangement (a) hence, the leakage is relatively larger than (a) but it is still a lower value due to strong coupling. The arrangement Fig. 3. 25(b) places the primary and secondary on separate limbs resulting a low magnetic coupling than the previous two. Thus, the leakage inductance is higher in (b) compared to the other two arrangements.

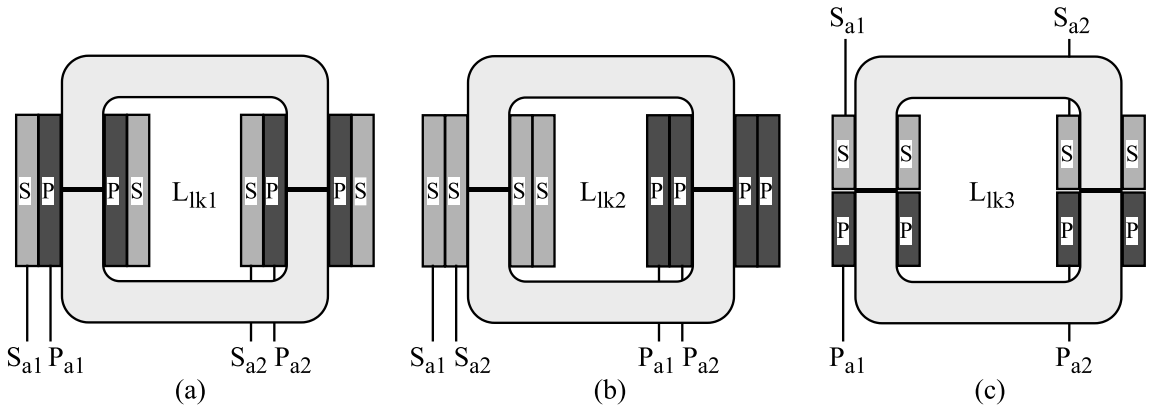

Fig. 3. 25. Different winding arrangements to realize interlimb leakage inductance. The windings 'S', 'P' represents the secondary and primary windings. Here, $L_{lk1} < L_{lk3} < L_{lk2}$.

The four windings in each phase can be defined as individual inductors, Fig. 3. 26. Using this definition, following set of matrix equations can be derived. Where, M_{xy} is the mutual inductance between winding x and y; ρ is the time derivative and $\rho i_1 = di_1/dt$.

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} L_1 & M_{12} & M_{13} & M_{14} \\ M_{21} & L_2 & M_{23} & M_{24} \\ M_{31} & M_{32} & L_3 & M_{34} \\ M_{41} & M_{42} & M_{43} & L_4 \end{bmatrix} \cdot \begin{bmatrix} \varrho i_1 \\ \varrho i_2 \\ \varrho i_3 \\ \varrho i_4 \end{bmatrix} \tag{14}$$

The matrix (14) can be solved to obtain the leakage inductance taking the physical winding configuration into consideration, Fig. 3. 27. The following derivation is done for the winding configuration (b) of Fig. 3. 25 and Fig. 3. 27.

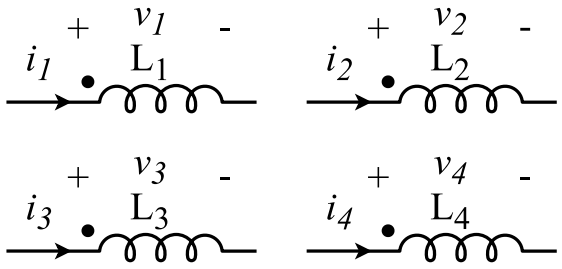

Fig. 3. 26. Notation of current and voltage of each element of the winding matrix.

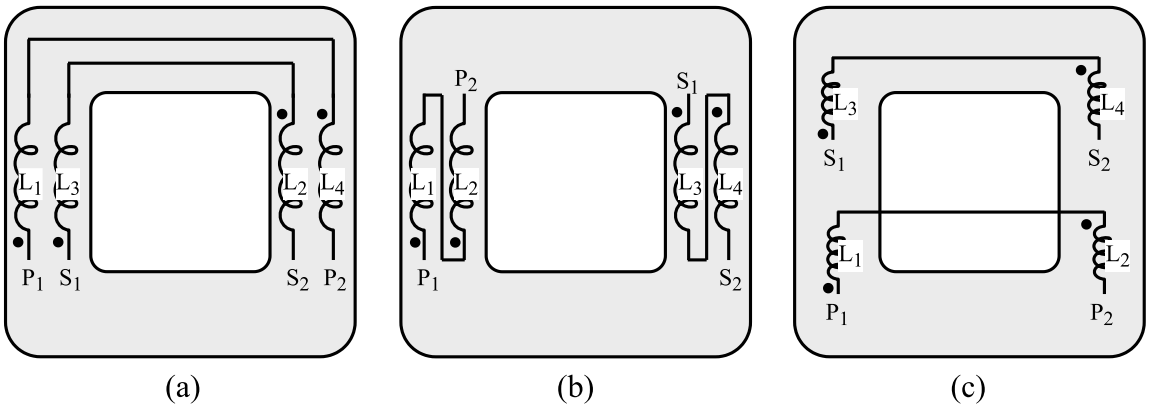

Fig. 3. 27. Physical winding arrangements corresponding to Fig. 3. 25, Fig. 3. 26.

$$v_{p1} - v_{p2} = v_{pri} = v_1 + v_2 \tag{15}$$

$$v_{s1} - v_{s2} = v_{sec} = v_3 + v_4 \tag{16}$$

$$v_{pri} = L_1\rho i_1 + L_2\rho i_2 + M_{12}\rho i_2 + M_{21}\rho i_1 + M_{13}\rho i_3 + M_{23}\rho i_3 + M_{14}\rho i_4 + M_{24}\rho i_4 \tag{17}$$

$$v_{sec} = L_3\rho i_3 + L_4\rho i_4 + M_{34}\rho i_4 + M_{43}\rho i_3 + M_{31}\rho i_1 + M_{41}\rho i_1 + M_{32}\rho i_2 + M_{42}\rho i_2 \tag{18}$$

Based on the winding placement of the arrangement Fig. 3. 27(b), Fig. 3. 28, the coupling between windings on the same limb are taken as k_1L and the coupling between

windings of opposite limbs as k_2L. Further the derivation assumes all the winding inductances are same; $L_1=L_2=L_3=L_4=L$. Thus,

$$v_{pri} = (L + k_1L)(\rho i_1 + \rho i_2) + 2k_2L(\rho i_3 + \rho i_4) \quad (19)$$

$$v_{sec} = (L + k_1L)(\rho i_3 + \rho i_4) + 2k_2L(\rho i_1 + \rho i_2) \quad (20)$$

The currents through each winding can be expressed using the inverter output currents, see Fig. 3. 28.

$$i_1 = i_2 = i_{dm} = \frac{i_{p1} - i_{p2}}{2} \quad (21)$$

$$i_3 = i_4 = i_{hf} = i_{s1} = -i_{s2} \quad (22)$$

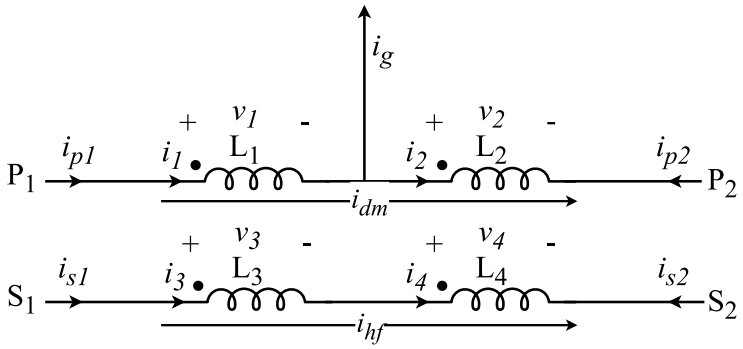

Fig. 3. 28. Winding placement for the arrangement (b).

Thus, the primary and secondary voltage can be simplified as,

$$v_{pri} = 2L(1 + k_1)\rho i_{dm} + 4k_2L\rho i_{hf} \quad (23)$$

$$v_{sec} = 4k_2L\rho i_{dm} + 2L(1 + k_1)\rho i_{hf} \quad (24)$$

Referring to the transformer T model of the converter, Fig. 3. 29, following relations can be derived.

$$v_{pri} = (L_k + L_m)\rho i_{dm} + L_m\rho i_{hf} \quad (25)$$

$$v_{sec} = L_m\rho i_{dm} + (L_k + L_m)\rho i_{hf} \quad (26)$$

Equating impedance variables of (23), (24) with (25), (26) the equivalent leakage L_k and magnetizing inductance L_m can be found.

$$L_k = 2L(1 + k_1 - 2k_2) \tag{27}$$

$$L_m = 4k_2L \tag{28}$$

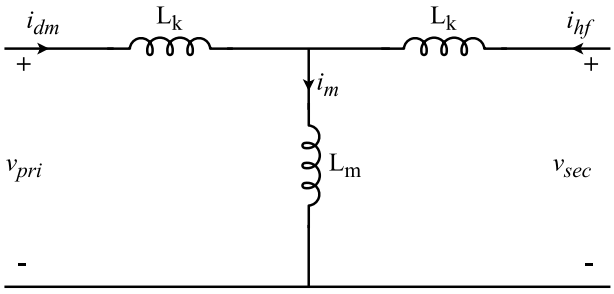

Fig. 3. 29. Transformer T model.

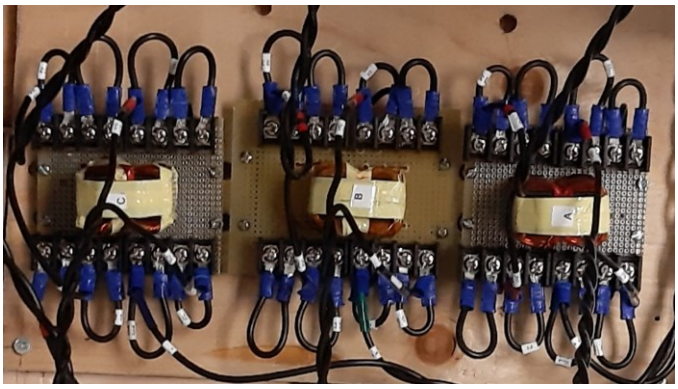

Fig. 3. 30. Integrated leakage inductance wound according to Fig. 3. 25(b)

It can be seen from the derivation that the leakage and magnetizing inductance depend on the coupling between the windings. Thus, the way the windings are arranged create different leakage inductances. Winding arrangements presented in Fig. 3. 27 can be leveraged to obtain desired leakage inductance value. The interlimb leakage inductance values measured for arrangements Fig. 3. 27 (a), (b) for the transformer shown in Fig. 3. 30 are 6uH, and 360uH respectively.

3.6 CONVERTER ANALYSIS

Mathematical analyses of the converter for high frequency active and reactive power, output power, high frequency rms current are presented. Minimization of the high frequency rms current within a fundamental cycle due to reference based modulation is discussed.

3.6.1 Basic Waveforms

The primary and secondary voltages (v_{pri}, v_{sec}) for both the RPP and FPS are three level voltages and can be expressed with Fourier series expansion. The controller is operated in such a way that $v_{pri} = v_{sec} = V$. The angular frequency $\omega_0 = 2\pi f_c$ where f_c is the carrier frequency. The quantity $\alpha = |x(t)|\pi$ is the angle corresponding to the zero voltage interval, see Fig. 3. 20.

$$v_{pri}(t) = \sum_{n=1,3,5,\ldots} \frac{4V}{n\pi} \cos\left(n\frac{\alpha}{2}\right) \sin(n\omega_0 t) \tag{29}$$

$$v_{sec}(t) = \sum_{n=1,3,5,\ldots} \frac{4V}{n\pi} \cos\left(n\frac{\alpha}{2}\right) \sin(n(\omega_0 t - \varphi)) \tag{30}$$

The high frequency current which flows through the leakage inductor can be derived as (31). Further, due to the symmetry of the high frequency current following relation can be observed.

$$i\left(\frac{\pi}{\omega_0}\right) = -i(0) \tag{31}$$

$$i_{hf}(t) = \int \frac{v_{pri}(t) - v_{sec}(t)}{L_k}\, dt \tag{32}$$

Applying the limits of (31) into (32),

$$i_{hf}(t) - i_{hf}(0) = \int_0^t \frac{v_{pri}(t) - v_{sec}(t)}{L_k}\, dt \tag{33}$$

Substituting (29), (30) into (33) and solving for the high frequency current yields (34).

$$i_{hf}(t) = \sum_{n=1,3,5,\ldots} \frac{4}{n^2\pi\omega_0 L_k}\sqrt{A^2 + B^2}\, \sin\left(n\omega_0 t + \arctan\frac{A}{B}\right) \tag{34}$$

$$A = V\cos\left(n\frac{\alpha}{2}\right)[\cos(n\varphi) - 1] \tag{35}$$

$$B = V\cos\left(n\frac{\alpha}{2}\right)\sin(n\varphi) \tag{36}$$

Quantities involving A, B can further be simplified, and simpler expressions can be derived as follows.

$$\arctan\frac{A}{B} = \frac{-n\varphi}{2} \tag{37}$$

$$\sqrt{A^2+B^2} = 2V\cos\left(\frac{n\alpha}{2}\right)\sin\left(\frac{n\varphi}{2}\right) \tag{38}$$

$$i_{hf}(t) = \sum_{n=1,3,5,\ldots} \frac{8V}{n^2\pi\omega_0 L_k}\cos\left(\frac{n\alpha}{2}\right)\sin\left(\frac{n\varphi}{2}\right)\sin\left(n\omega_0 t - \frac{n\varphi}{2}\right) \tag{39}$$

It is evident from (39) that the phase angle of the fundamental component of the high frequency current is $n\varphi/2$ lagging with the fundamental primary voltage v_{pri} and leading with the same angle with fundamental v_{sec}. This relation holds only when the primary and secondary dc link voltages are made to operate the same and the same 3-level voltage modulation pattern is implemented in both the sides. A high frequency voltage and current phasor diagram for the fundamental component can be drawn based on the equations, Fig. 3. 31, where $v_{Lk} = v_{pri} - v_{sec}$ is the voltage across the leakage inductor.

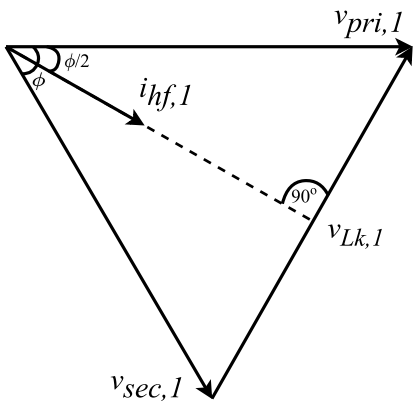

Fig. 3. 31. High frequency voltage current phasor diagram.

3.6.2 High Frequency Active and Reactive Power

The high frequency power can be derived based on the voltage and current seen on the primary side [24], [25]. The average power in a switching cycle is defined as P_n.

$$P_n = \frac{1}{T_c} \int_0^{T_c} v_{pri}(t) i_{hf}(t)\, dt \tag{40}$$

Substituting for v_{pri} and i_{hf} from (29) and (39) into (40) gives,

$$\begin{aligned} P_n = & \frac{1}{T_c} \int_0^{T_c} \sum_{n=1,3,5,\ldots} \frac{4V}{n\pi} \cos\left(n\frac{\alpha}{2}\right) \sin(n\omega_0 t) \times \\ & \sum_{n=1,3,5,\ldots} \frac{8V}{n^2 \pi \omega_0 L_k} \cos\left(\frac{n\alpha}{2}\right) \sin\left(\frac{n\varphi}{2}\right) \sin\left(n\omega_0 t - \frac{n\varphi}{2}\right) \end{aligned} \tag{41}$$

It can be seen the product of v_{pri} and i_{hf} involves the harmonic products of different order and the periodic integral of them over a carrier period. Since the periodic integral of non-equal harmonics is zero, the average power under a carrier cycle becomes only the summation of product of equal harmonics [24], [25]. Thus, P_n can be simplified into (42).

$$P_n = \sum_{n=1,3,5,\ldots} \frac{8V^2}{n^3\pi^2\omega_0 L_k} \cos^2\left(\frac{n\alpha}{2}\right)\sin(n\varphi) \tag{42}$$

The reactive power in the system can be expressed as two components which are the products of same harmonic numbers and different harmonic numbers. The average reactive power in a carrier period Q_n for $n=m$ where n, m are the harmonic numbers can be expressed as (43).

$$Q_{n=1,3,5,\ldots} = \frac{8V^2}{n^3\pi^2\omega_0 L_k}\cos^2\left(\frac{n\alpha}{2}\right)[1-\cos(n\varphi)] \tag{43}$$

The average carrier periodic reactive power Q_{nm} for product of different harmonics where ($n\neq m$) is,

$$Q_{nm} = \frac{16V^2}{mn^2\pi^2\omega_0 L_k}\cos\left(\frac{m\alpha}{2}\right)\cos\left(\frac{n\alpha}{2}\right)\sin\left(\frac{n\varphi}{2}\right) \tag{44}$$

3.6.3 High Frequency Current

The rms of the high frequency current can be derived from (39) considering the amplitude of the sine harmonics.

$$I_{hf,rms} = \frac{4\sqrt{2}\,V}{n^2\pi\omega_0 L_k}\cos\left(\frac{n\alpha}{2}\right)\sin\left(\frac{n\varphi}{2}\right) \tag{45}$$

Further, the rms of the winding currents $I_{w,rms}$ in the primary side results due to the high frequency current i_{hf} and half the grid current $i_g/2$. Thus, the primary winding rms current can be derived.

$$I_{w,rms} = \sqrt{\left(\frac{I_{g,rms}}{2}\right)^2 + I_{hf,rms}^2} \tag{46}$$

The rms of the high frequency current i_{hf}(t) under a carrier cycle vary within the 60Hz grid fundamental period, Fig. 3. 32. The rms current generated by the proposed modulation method, RPP, does lower the rms compared to the FPS method. Further, the rms of the square wave modulation method, SPP, has the highest value observed under the grid fundamental. The measure of the high frequency rms current reflects the amount of reactive content present in the high frequency waveforms. Thus, the SPP method has the highest reactive content under grid fundamental and RPP has the least reactive content among the three methods.

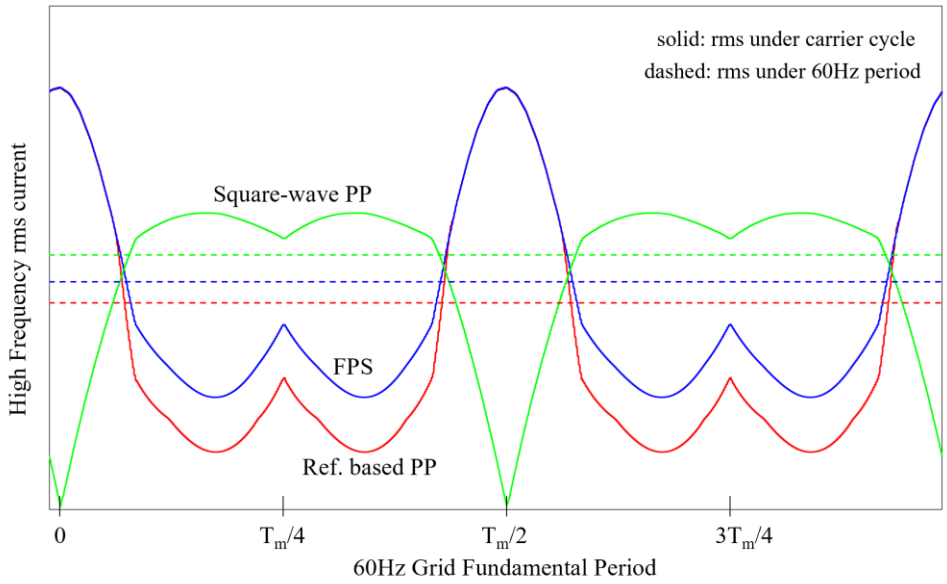

Fig. 3. 32. Simulated variation of rms of the high frequency current under a 60Hz grid fundamental period plotted for a constant power level.

3.7 SIMULATED PERFORMANCE

The comparison of the high frequency rms current and reactive power for the RPP, FPS, and SPP pwm methods reflects that the SPP approach consists of the highest values out of them. Further, the readings of SPP does not change with pulse separation since the SPP method does not control the pulse separation. The RPP method proposed in the thesis produce the lowest rms current and reactive power amongst the three, Fig.

3. 33, Fig. 3. 34, Fig. 3. 35. The power output of the RPP and FPS are almost the same since the volt-seconds for active power transfer remains the same despite pulse alignment, Fig. 3. 36. Since, the square wave pulse position method produces excessive reactive content, it can be disregarded on the basis of reactive content.

The high frequency reactive power against the output power for RPP, FPS, and a single phase DAB reflects that a DAB has lower reactive power amongst the three however, the RPP method is close enough for a DAB given a sufficient dc voltage (m_a~<0.9), Fig. 3. 37.

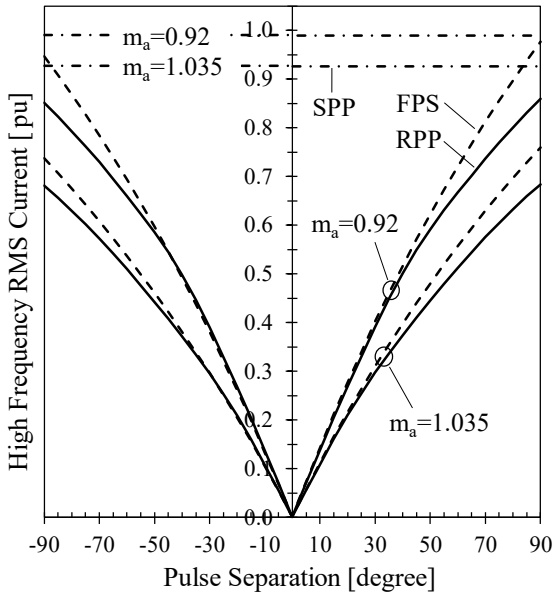

Fig. 3. 33. Simulated high frequency rms current change with pulse separation. Vdc = 329V (1.035m_a), 370V (0.92m_a). Pbase = 4.45kW.

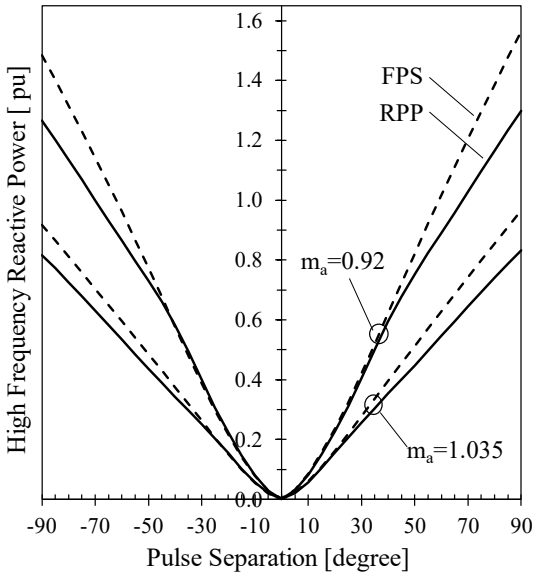

Fig. 3. 34. Simulated high frequency Var variation with pulse separation. Vdc = 329V (1.035m_a), 370V (0.92m_a). Pbase = 4.45kW.

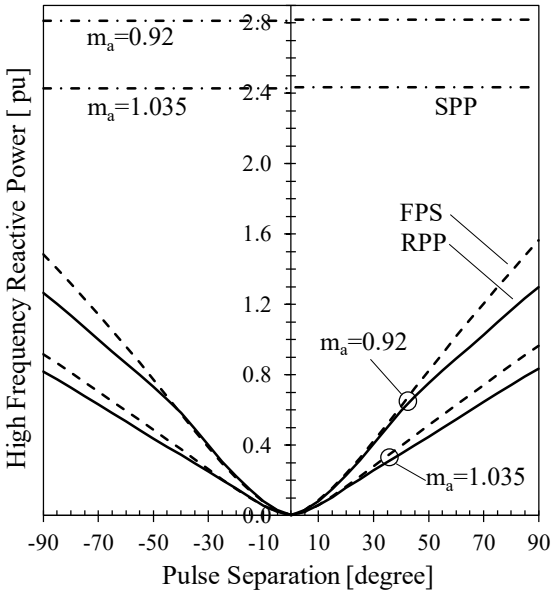

Fig. 3. 35. Simulated high frequency Var change with pulse separation. Vdc = 329V (1.035m_a), 370V (0.92m_a). Pbase = 4.45kW.

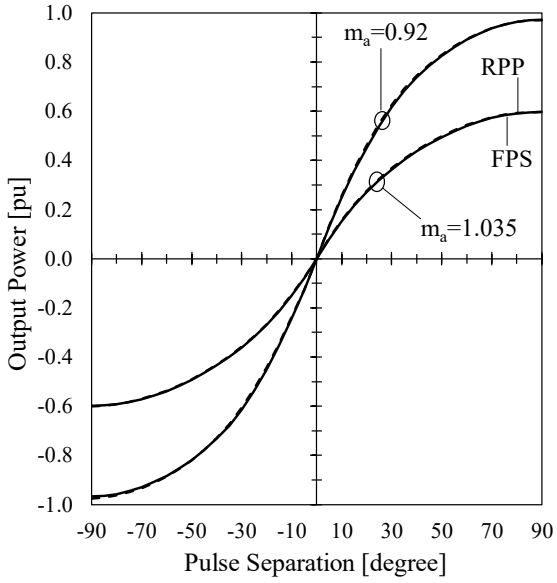

Fig. 3. 36. Simulated output power against pulse separation. Vdc = 329V (1.035m_a), 370V (0.92m_a). Pbase = 4.45kW.

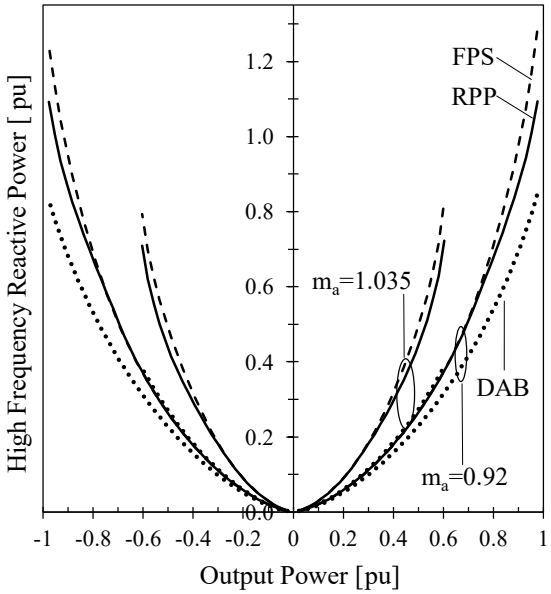

Fig. 3. 37. Simulated high frequency Var plotted against output power. Results per-unitized with 4.3kW.

Performance of high frequency rms current with increasing dc link voltage is proportional to $V \sin\left(\frac{n\varphi}{2}\right)$, see (45), hence, demonstrates slightly curved variation, Fig.

3. 38. The high frequency Var change is proportional to $V^2[1-\cos(n\varphi)]$, see (43), (44), hence a rapid increment can be observed, Fig. 3. 39.

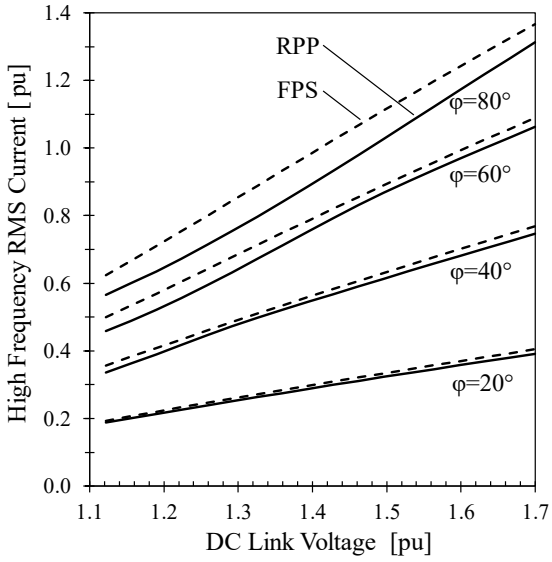

Fig. 3. 38. Simulated high frequency rms current change against dc link voltage. V_{LL} = 208V, Pbase = 5kW, Vbase = 208*√2.

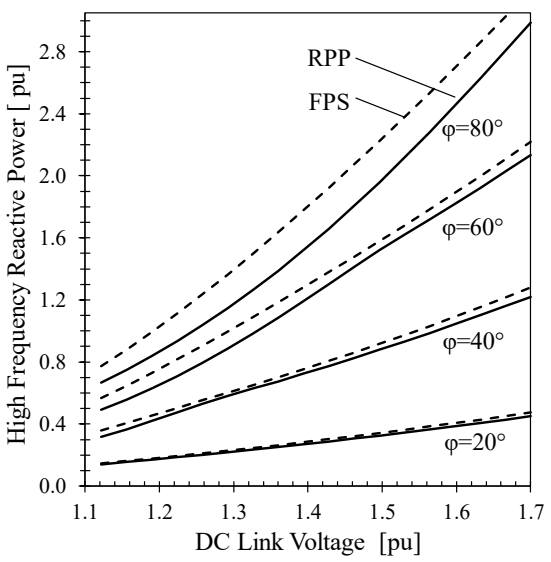

Fig. 3. 39. Simulated high frequency Var change against dc link voltage. VLL = 208V, Pbase = 5kW, Vbase = 208*√2.

The parameter variation with pulse separation, for example 40° behaves such that the high frequency voltage pulses are positioned next to each other when their widths lower than 40°, and phase shifted by 40° when the pulse widths are larger than 40°.

The output power change with respect to the dc link voltage and φ(t) is proportional to $V^2\sin\left(\frac{n\varphi}{2}\right)$ which also continue to rapidly increase with dc link voltage and pulse separation, Fig. 3. 40. The ratio of high frequency reactive power to output power for the single phase DAB remains constant throughout entire dc link voltage range for a given pulse separation (both primary and secondary has the same dc voltage). With increasing pulse separation, the power ratio of FPS tends to be higher than RPP at lower dc link voltages (towards high modulation indices). A trend between RPP and DAB is observed that with increasing voltage the RPP method approaches the DAB behavior, Fig. 3. 41. However, a maximum voltage limit for the RPP method exists to obtain its benefits; the maximum value of the reference signal should be greater than 0.5, see

(46.1), (46.2). Thus, the maxim dc link voltage should be 2pu. The base voltage is taken as 208*√2 = 1pu.

$$x_{max} = \frac{2}{V_{dc}} \frac{1\,pu}{\sqrt{3}}, \quad x_{max} \geq 0.5 \tag{46.1}$$

$$V_{dc} \leq 2\,pu \tag{46.2}$$

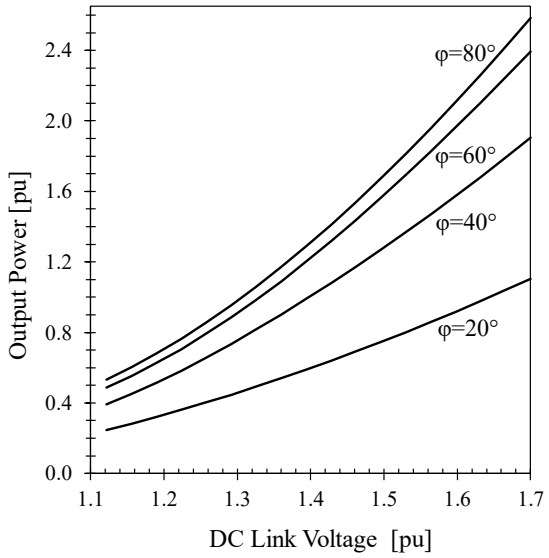

Fig. 3. 40. Simulated output power change with dc link voltage. V_{LL} = 208V, Pbase = 5kW, Vbase = 208*√2.

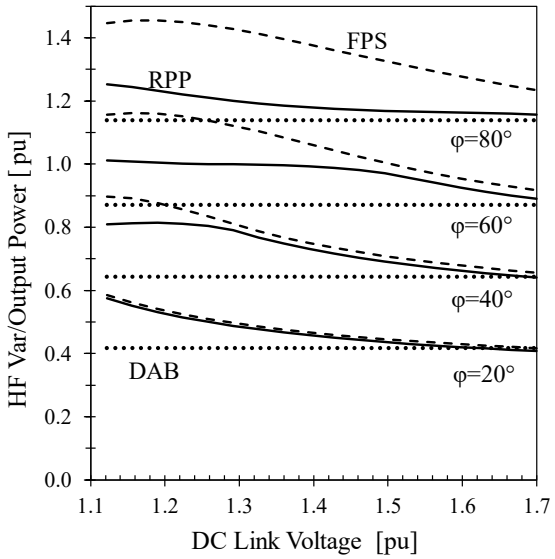

Fig. 3. 41. Simulated HF Var to output power ratio with dc link voltage. V_{LL} = 208V, Pbase = 5kW, Vbase = 208*√2.

A minimum value for dc link voltage can be found by setting 5% for output impedance and another 5% for transient dynamics. Considering V_{LL}*√2 to be 1pu, for maximum modulation index (m_a = 1.15) the dc link requirement is 1pu. Thus, allowing for output impedance and transients, the minimum dc voltage requirement is 1.1pu (1.05m_a). The maximum dc link requirement is 2pu (0.575m_a) to obtain the benefit of the RPP method. A reasonable dc link operating voltage range would be 1.3 – 1.4 pu for larger pulse separations (60° – 90°). The RPP method has a good reduction in high frequency rms current and reactive power compared to the FPS within this range, Fig. 3. 38, Fig. 3. 39. In terms of fundamental modulation index, the voltage range corresponds to 0.89 – 0.83 m_a. operating at the lower end of the dc voltage range can result in distorted waveforms and poor pulse separation controllability during

transients. Operating at excessively large dc voltage puts voltage stresses in the components however, quality waveforms and good transient responses can be obtained.

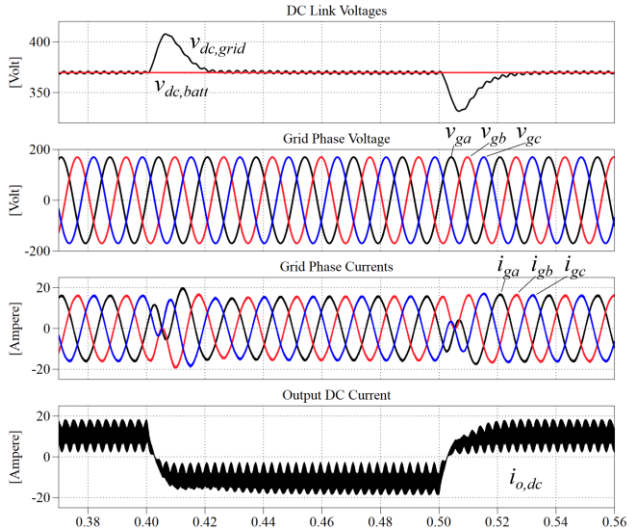

Fig. 3. 42. Power reversal ±4kW. V_{LL} = 208V, Vdc = 370V.

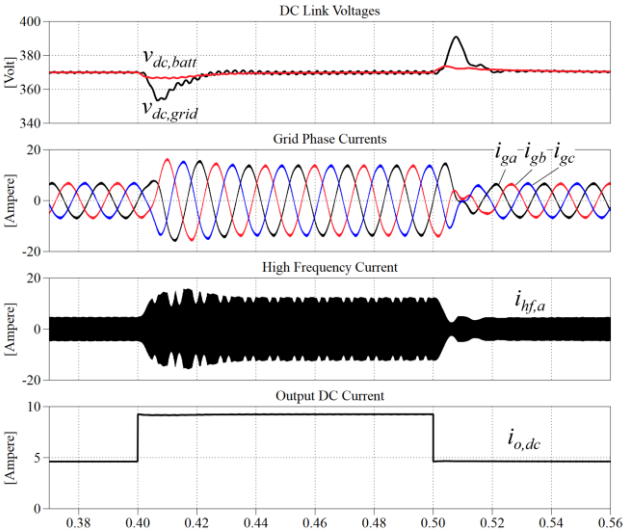

Fig. 3. 44. Load change. 80-40-80 Ω. VLL = 208V, Vdc = 370V.

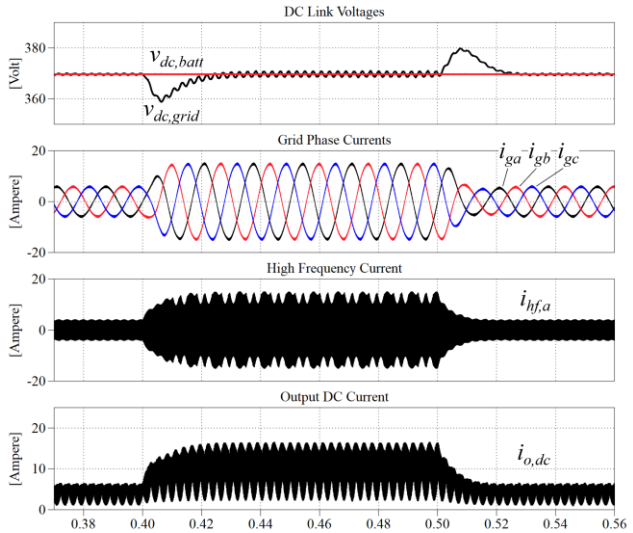

Fig. 3. 43. Output current step change 4-10-4 A. V_{LL} = 208V, Vdc = 370V.

Figures 3.42, 3.43, 3.44 presents the simulated performance of transient changes in output power, output current, and output load. The controller is able to handle transients with good control response reaching the steady state in two fundamental cycles.

3.8 SUMMARY

A detailed description of the converter and its operation, modulation, and performance is provided. Three modulation methods, FPS, RPP, SPP are presented and amongst them, the RPP delivers better performance with lower high frequency rms current and reactive power. A brief discussion of three possible transformer winding arrangements is made for which a range of the interlimb leakage values can be obtained depending on the application. The SPP pwm approach produces the highest rms currents and reactive power hence, it can be dismissed. Both FPS and RPP have the same power output with pulse separation and the RPP gives better results at higher pulse separations. Even though, the converter with RPP modulation has higher reactive power compared to a single-phase phase-shifted DAB, the distinction diminishes with increasing dc link voltage. Allowing 10% for output impedance and transient dynamics, the minimum dc link voltage requirement is 1.1pu, and the maximum dc link voltage is 2pu to obtain the benefits of RPP method. Recommended dc link operating voltage range is 1.3 -1.4 pu where the reduction in high frequency reactive content maximized for the RPP method. The controller performs well for transients and reaches the steady state in two fundamental cycles.

Chapter 4

CONVERTER CONTROL

Details of the control of the converter and the reference modification algorithm are provided. Different sub-controllers involved and tuning of them using bode plots is also provided. A specific case of determining carrier minimum and maximum for the PLECS RT Box 1 is described for the proper operation of the reference modification algorithm in the experimental hardware. Furthermore, control strategy to minimize grid voltage harmonics existing in the laboratory setup is presented.

4.1 GRID CONTROL MODULATION

The grid side reference signals are modulated by a sine wave with its third harmonic added onto it. This modulating signal is achieved by adding a common mode offset (CMO) signal to the three sine modulating signals, Fig. 4. 1. The final outcome of adding the CMO is almost similar to the space vector pwm (SVPWM) which increase the fundamental modulation index to 1.155. The SVPWM can be achieved either by an elaborated process of determining the switch on duration with respect to the reference vector or simply by adding a CMO to all the three reference signals. The CMO signal is found by the following expression.

$$CMO = \frac{-1}{2}[max(A,B,C) + min(A,B,C)] \quad (47)$$

Then the augmented reference signals are,

$$v_{a,aug} = v_{a,ref} + CMO \tag{48}$$

$$v_{b,aug} = v_{b,ref} + CMO \tag{49}$$

$$v_{c,aug} = v_{c,ref} + CMO \tag{50}$$

Where $v_{a,ref}$, $v_{b,ref}$, $v_{c,ref}$ are the sinusoidal control signals which are output from the grid side controller which can be expressed as,

$$v_{a,ref} = m_a \sin(\omega_m t) \tag{51}$$

$$v_{b,ref} = m_a \sin(\omega_m t - 2\pi/3) \tag{52}$$

$$v_{c,ref} = m_a \sin(\omega_m t + 2\pi/3) \tag{53}$$

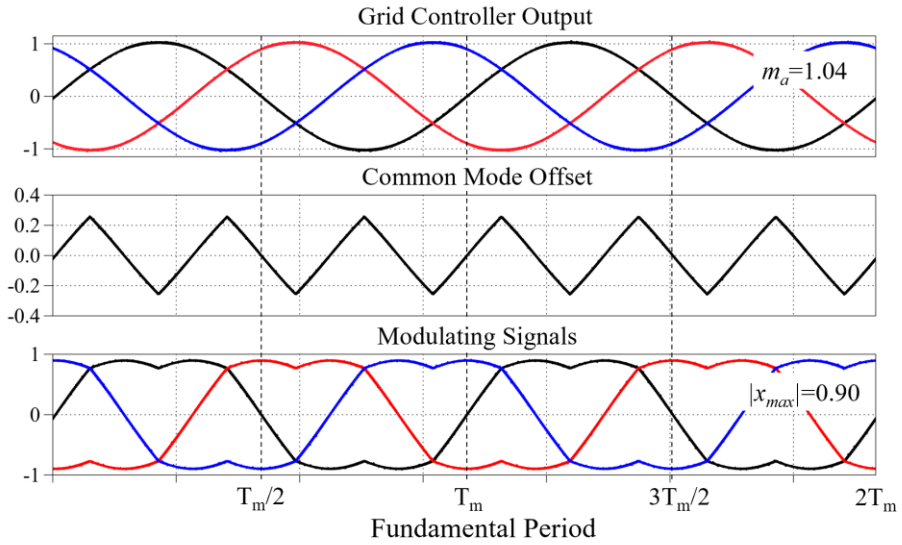

Fig. 4. 1. Space vector modulation by the addition of common mode offset. Fundamental modulation index (m_a) = 1.04. Maximum value of modulating signals with CMO (x_{max}) = 0.9. The peak of the reference signals is decreased by a factor of 1.15 due to SVPWM.

The benefit of using the SVPWM is the improved utilization of the dc link voltage, which means a lower dc link voltage can be used to get the same modulation index with respect to the use of sinusoidal pwm (SPWM) method. With the SVPWM the peak of

the reference signals is reduced by a factor of 1.15 and hence, the fundamental modulation index (m_a) can be increased by a factor of 1.15 [26].

The relation between the fundamental modulation index, dc link voltage and the grid line rms voltage ($V_{LL,rms}$) with the SVPWM can be expressed using the equation (54), where $V_{ph,ph}$ is the peak of the phase voltage. Whereas for the SPWM the relation holds as in (55). The quantity $\frac{\sqrt{3}}{2}m_a$ represents the peak value of the modulating signal. Therefore, for the same grid voltage and the peak modulating signal, the dc link voltage with SVPWM can be reduced approximately by 15% compared with the SPWM.

$$\left(\frac{\sqrt{3}}{2}m_a\right)\frac{V_{dc}}{2} = V_{ph,pk} = \sqrt{\frac{2}{3}}\,V_{LL,rms} \tag{54}$$

$$m_a\frac{V_{dc}}{2} = \sqrt{\frac{2}{3}}\,V_{LL,rms} \tag{55}$$

4.2 REFERENCE MODIFICATION ALGORITHM

The modulation methodology (RPP) for the converter described involves modifying the reference signal to achieve the required dynamic pulse separation. This is achieved by adding or subtracting a *dx* value at the carrier minimum or maximum. An algorithm sums the *dx* depending on the value of the reference signal and the pulse separation command.

The algorithm starts at idle and checks whether the carrier minimum or maximum is reached which are square waves of 1 and 0 values. If the value is 1, then the minimum or the maximum is considered reached. Once the algorithm has decided the carrier limits, the *dx* required to sum with the reference is evaluated based on the commanded pulse separation (ps=φ) and the reference value (*x*). finally, the algorithm switches into one out of two reference modification expressions with respect to the polarity of φ, see Fig. 4. 2. A PLECS C-Script code was developed to implement the algorithm. Refer Appendix A for the complete C-Script code. Fig. 4. 3 illustrates the final modulating

signals output by the algorithm. The smooth curves are the original reference signals coming by the grid current controller.

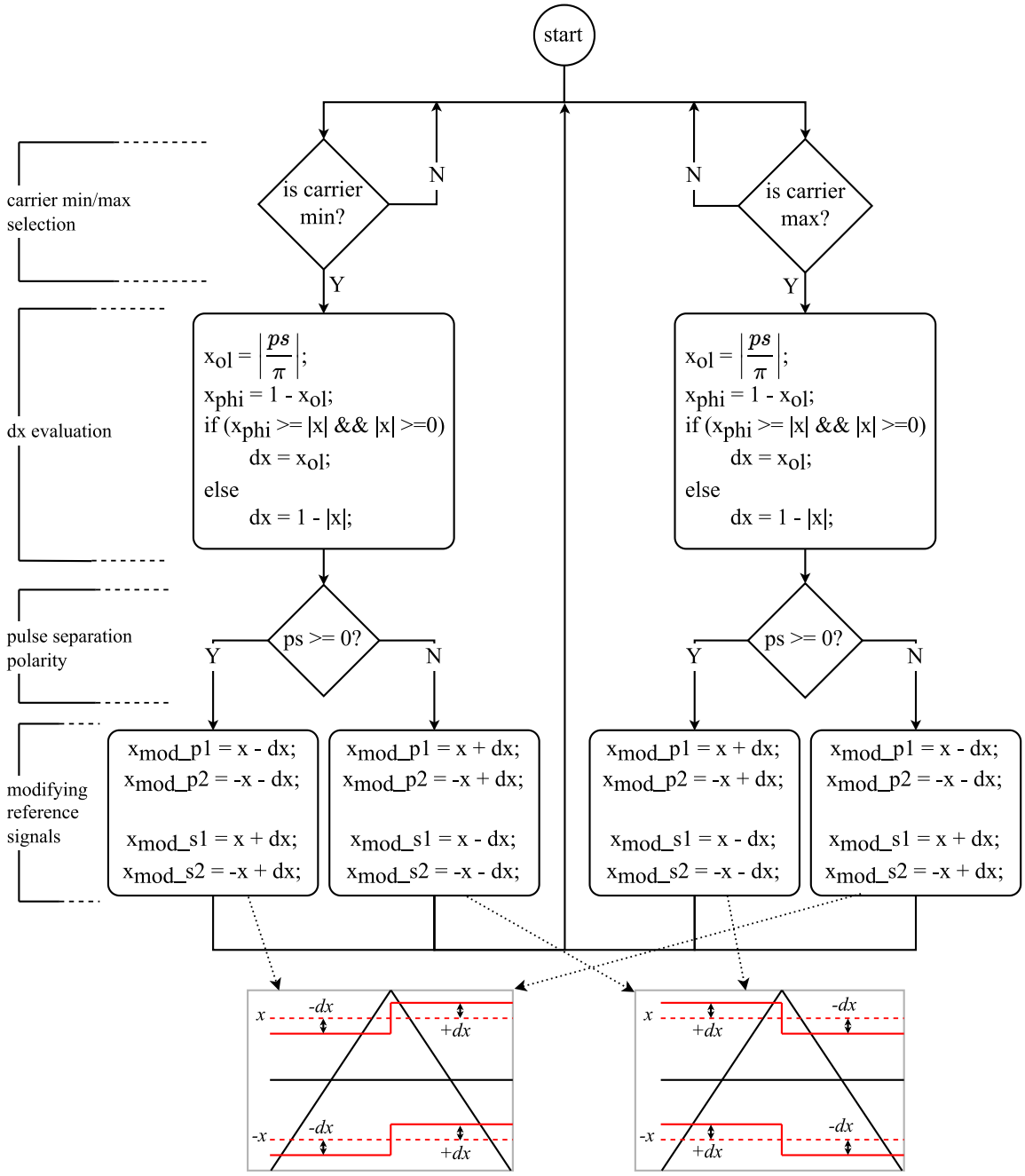

Fig. 4. 2. Reference modification algorithm.

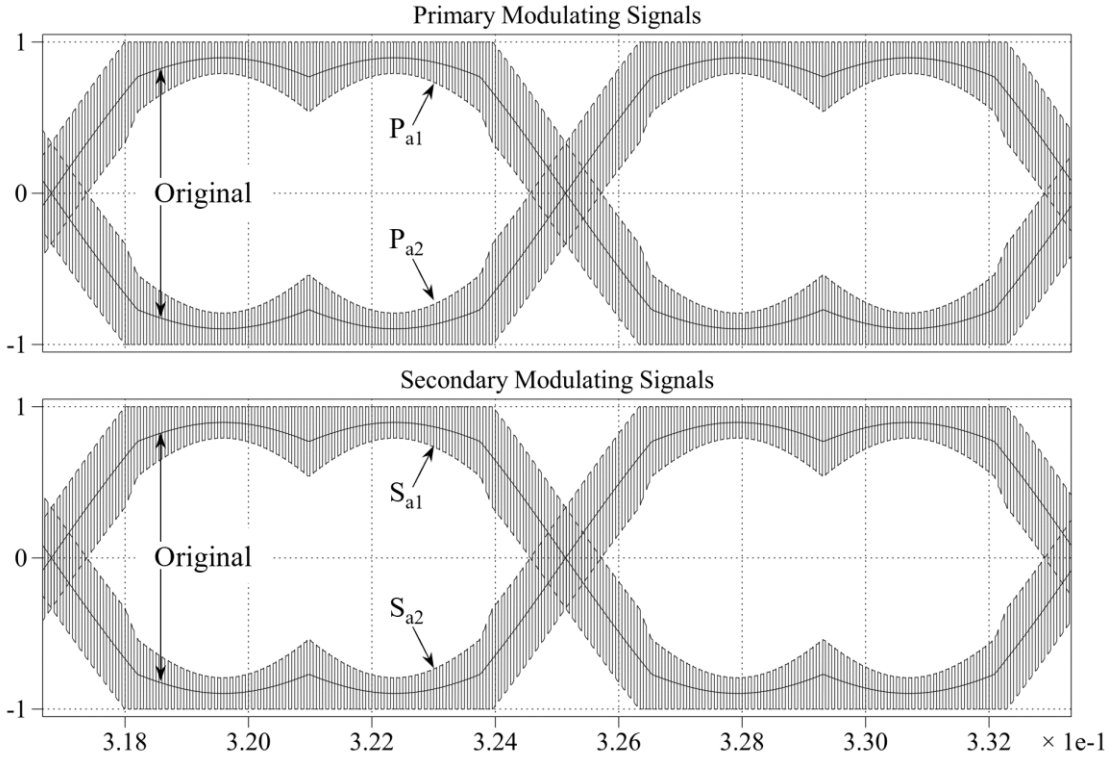

Fig. 4. 3. Final modulating signals generated by the algorithm for the phase A for m_a=0.9. P_{a1}, P_{a2} are the modulating signals for the primary respective inverter legs while S_{a1}, S_{a2} are for the secondary.

4.3 CONVERTER CONTROLLER

The overall converter controller and its sub-controllers are presented. Bode diagrams related to controller tuning are also presented. Furthermore, the derivation of control transfer function is also discussed.

The overall controller, Fig. 4. 4, can be divided into the following sub-control loops.

- Grid dc link voltage controller
- Grid current controller
- Pulse positioning controller

The grid side controller consists of the grid dc link voltage and grid current controllers where the two controllers form outer and inner control loops respectively. The two controllers are cascaded such that the grid dc link is purely controlled by the grid

current. The voltage controller outputs the d-axis current reference for the current controller. The reactive power, exchanged with the grid, is kept at zero by maintaining the q-axis current reference to zero. This reactive power should not be confused with the high frequency reactive power, where the focus of the thesis is to lower the latter.

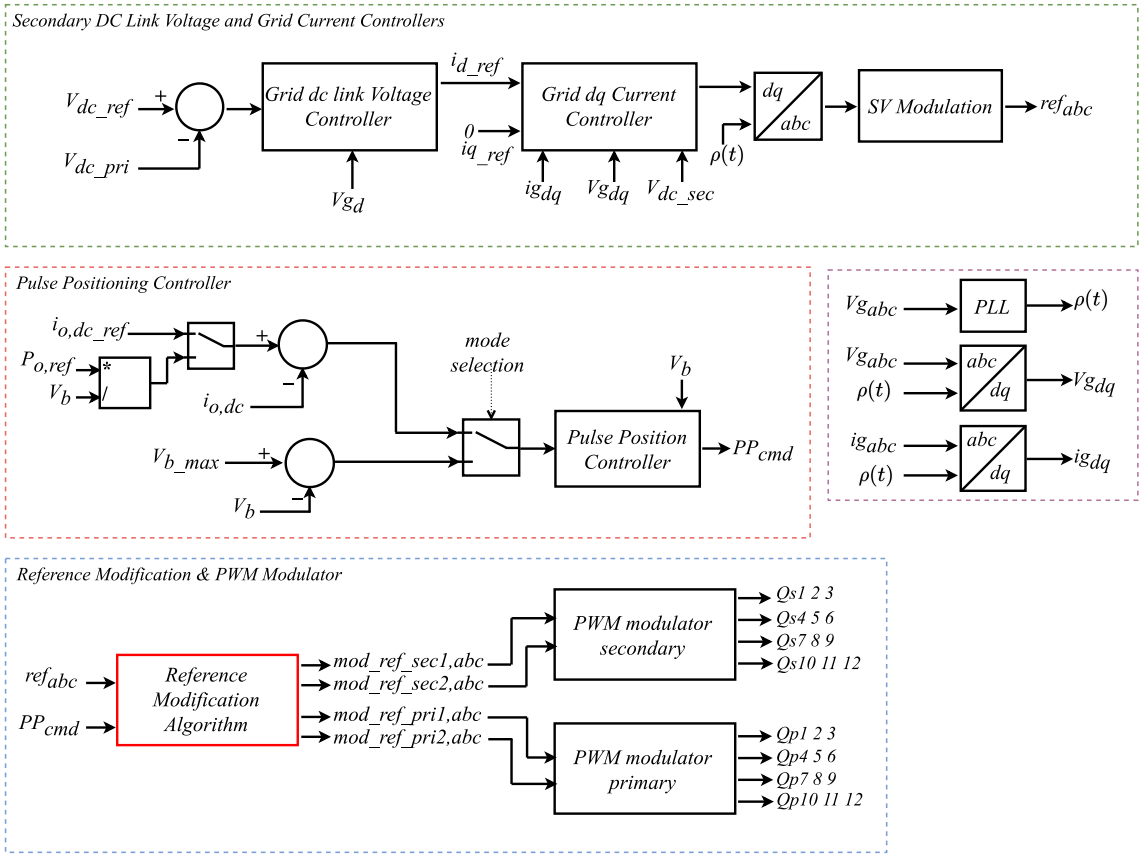

Fig. 4. 4. Overall converter controller

4.3.1 Grid Current Controller

The grid current control is designed in the dq-axis (rotating reference frame) and consists of a L (grid line filter inductor) and R (parasitic resistance) physical output filter. The dynamic equations [27] for the LR output filter can be written in the dq-axis as (56), (57). V_{td}, V_{tq} represents the dq components of the phase voltage at the center tap of the transformer windings at the grid side. m_d, m_q are the dq components of the modulation index and u_d, u_q are the simplified control variables in dq-axes for the

control of the grid current. The current controller in the dq-axis can be visualized from the equations as in Fig. 4. 5.

$$L\frac{di_d}{dt} = L\omega_m i_q - Ri_d + V_{td} - V_{gd} \tag{56}$$

$$L\frac{di_q}{dt} = -L\omega_m i_d - Ri_q + V_{tq} - V_{gq} \tag{57}$$

$$V_{td} = \frac{V_{dc}}{2}m_d \qquad V_{tq} = \frac{V_{dc}}{2}m_q \tag{58}$$

$$m_d = \frac{2}{V_{dc}}\left(u_d - L\omega_m i_q + V_{gd}\right) \tag{59}$$

$$m_q = \frac{2}{V_{dc}}\left(u_q + L\omega_m i_d + V_{gq}\right) \tag{60}$$

$$L\frac{di_d}{dt} = -Ri_d + u_d \tag{61}$$

$$L\frac{di_q}{dt} = -Ri_q + u_q \tag{62}$$

The current controller includes a resonant gain tuned at the 6th harmonic of the grid frequency. The grid connection at the laboratory consists of 5th and 7th order harmonics which causes the grid voltage to be distorted. When the grid voltage is transformed into the dq frame, the above harmonics are transformed into the 6th harmonic [28]. Thus, the reference signals and the grid current contain the 6th harmonic component. To dampen the 6th harmonic a resonant gain tuned at the 6th harmonic frequency is inserted to the current controller, see Fig. 4. 5. The transfer function of the resonant gain Hr(s) is set as in (63) with gain $k_r = 5$, where $a_r = 200$ rad/s the bandwidth of the resonant gain and $\omega_m = 2\pi f_m$ the fundamental grid angular frequency. The bode diagram for the current controller with the resonant gain is obtained as in Fig. 4. 6.

$$Hr(s) = \frac{a_r s}{s^2 + a_r s + (6\omega_m)^2} \tag{63}$$

The current controller bandwidth is set to 1kHz to respond for the 6th harmonic and the integrator bandwidth is set to 1/10 time the controller bandwidth and k_p = 14.0873 V/A, k_i = 8851.3 V/A.

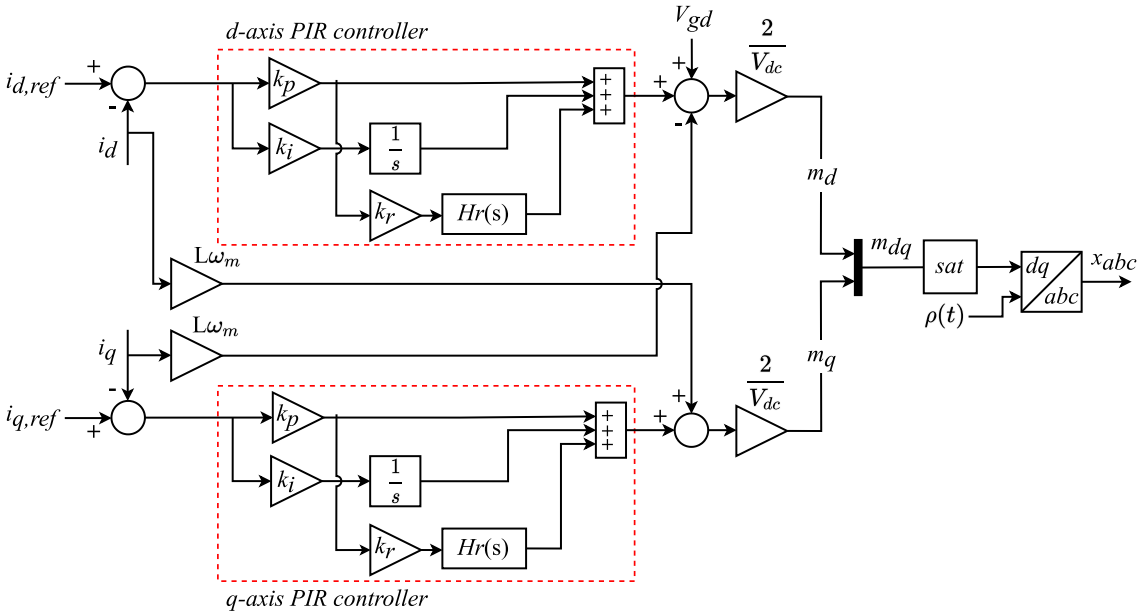

Fig. 4. 5. Schematic of the grid current controller in the dq-axis.

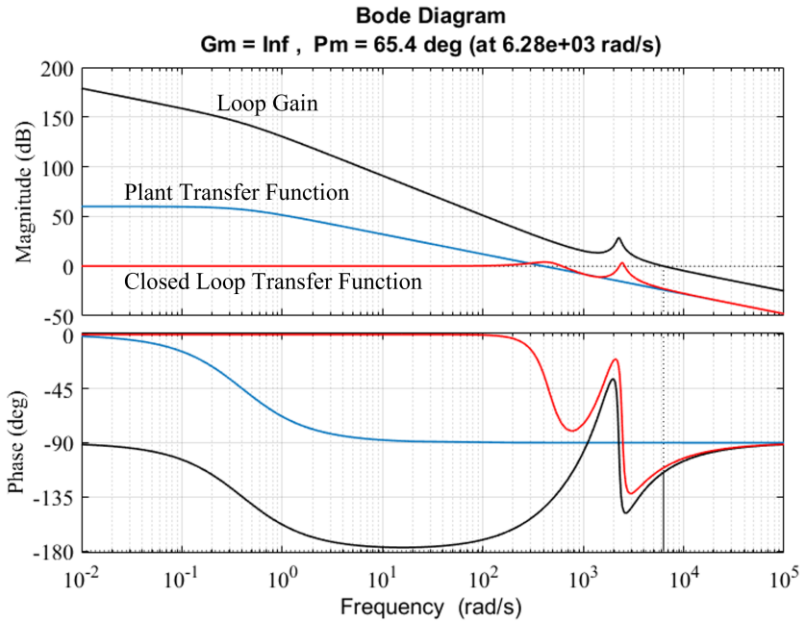

Fig. 4. 6. Bode diagram of the current controller.

4.3.2 Grid dc Link Voltage Controller

The grid capcitor voltage is changed by the capacitor current, which is the dc link current on the grid side. The transfer function for the grid capacitor can be written (64).

$$\frac{V_{dc}(s)}{I_c(s)} = \frac{-1}{C_p s} \tag{64}$$

Since the capacitor voltage is solely controlled by the grid curret, a power balance relation can be derrived for the dc link (65). The votlage controller bandwidth is set to 60Hz with an integrator bandwidth of 24Hz. An integrator back calculation path is added to avoid the voltage controller running into unstability. If the $I_{d,ref}$ run into saturation, the back calculation path provides a negative integrator gain to reverse the integrator slope. Controller gains are k_p=035, k_i=52.7829.

$$P_{dc} = V_{dc} * i_c$$
$$P = \frac{3}{2} V_{gd} * i_d \tag{65}$$

$$i_d = \frac{2V_{dc}}{3V_d} i_c \tag{66}$$

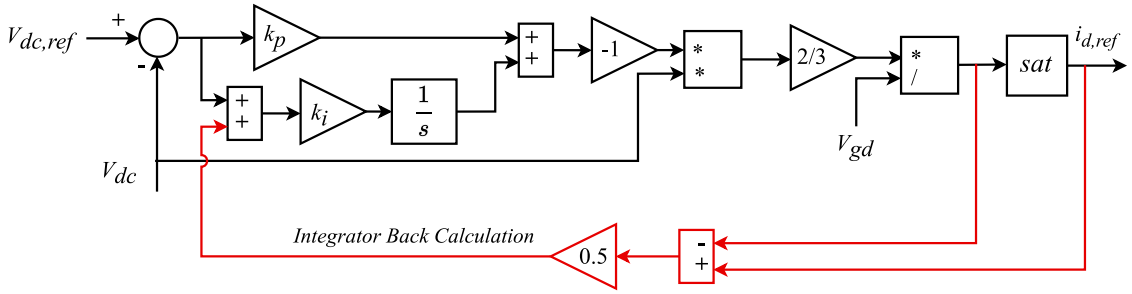

Fig. 4. 7. Control schematic of the grid dc link voltage controller.

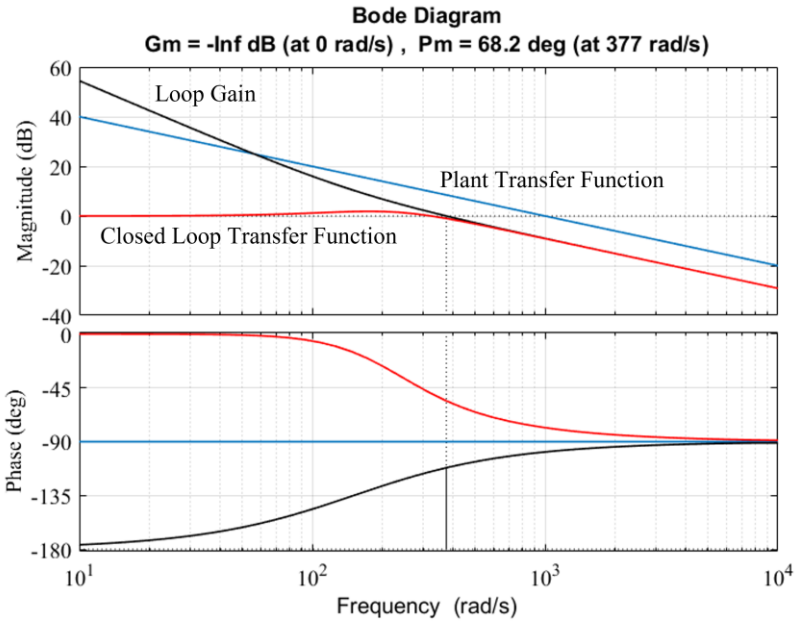

Fig. 4. 8. Bode diagram of the Voltage controller.

4.3.3 Pulse Position Controller

The phase shift controller presents non-linear relation with the output voltage and current parameters. By analyzing the per phase secondary dc link current waveform following non-linear relation (67) with pulse separation can be derived.

$$I_{odc} = \frac{V}{2\pi L_k \omega_0}(2\theta\varphi - \varphi^2) \tag{67}$$

It is clear that the control input for the output current is a squared term of the pulse separation. A trial and error method were used to tune a PI controller for the I_{odc} control to have a reasonable response. It is also possible to derive pulse separation to output voltage transfer function considering the output impedance and the concept of gyrator [29], [30], however, this method is out of the scope of this thesis. A feed forward path derived from (67) is summed with the PI output to deliver fast response to change in I_{odc}. Furthermore, integrator back calculation anti-windup method is implemented to stop the integrator accumulating error.

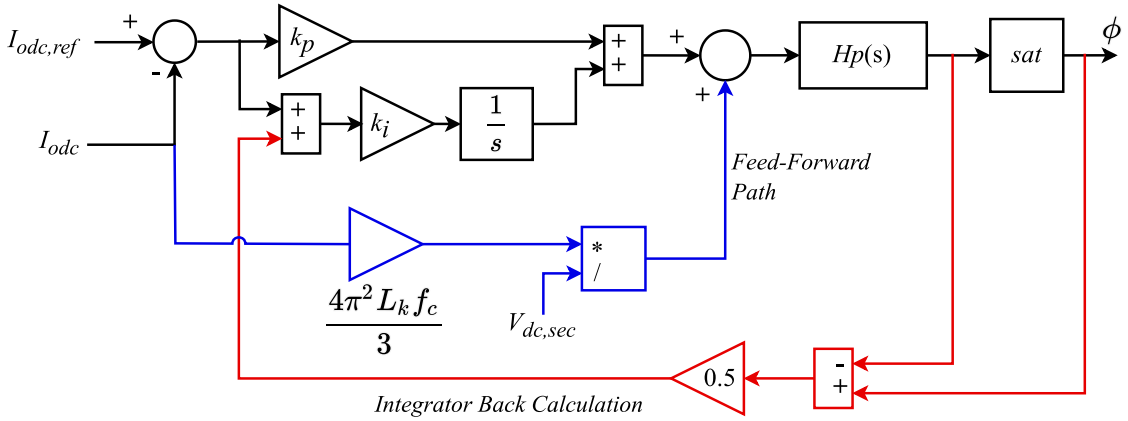

Fig. 4. 9. Control schematic of the pulse separation controller.

4.3.4 Output Control Modes

The pulse separation controller is able to control the output current, voltage, and power with the same controller, Fig. 4. 10. The battery charger operation can work with output current, power, and voltage control modes. If the output is a load, the same controller can work only in the voltage control mode.

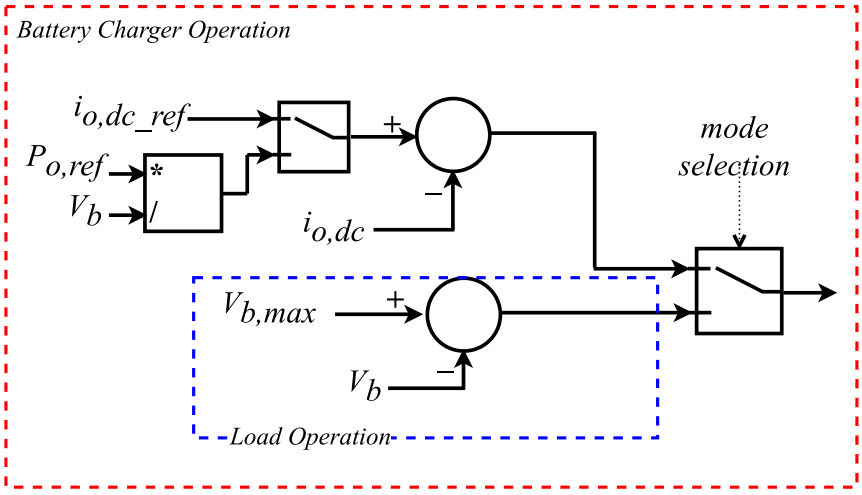

Fig. 4. 10. Output modes of operation.

4.3.5 Grid Harmonic Elimination

The grid connection present in the laboratory setting consist of 5th and 7th order harmonics. When the grid voltage is transformed into the dq frame, these harmonics get transformed into the 6th order [28]. Thus, the current controller produces 6th harmonic component in the grid current. To minimize the harmonic effect, a phase locked loop (PLL) controller was developed [28], Fig. 4. 11. $H_p(s)$ is a second order Butterworth low pass filter, $H_6(s)$ is a notch filter tuned at the 6th harmonic and $K_1(s)$ is the PI compensator.

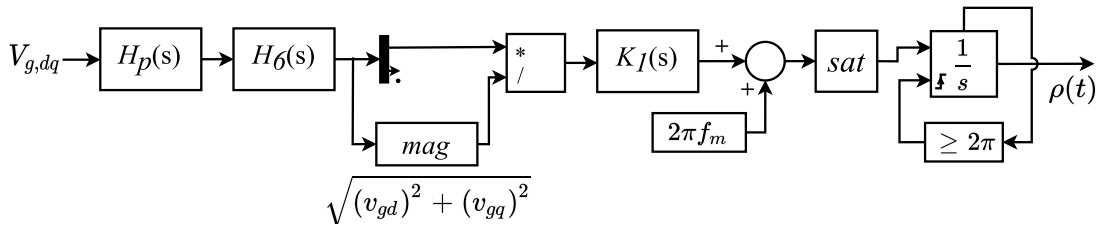

Fig. 4. 11. Schematic of the designed PLL controller.

$$H_p(s) = \frac{\alpha_1^2}{s^2 + \sqrt{2}\,\alpha_1 + \alpha_1^2} \tag{68}$$

$$H_6(s) = \frac{s^2 + (6\omega_1)^2}{s^2 + \alpha_2 s + (6\omega_1)^2} \tag{69}$$

$$K_1(s) = \frac{k_p(1 + \omega_i)}{s} \tag{70}$$

Where, α_1, α_2 are the bandwidths of the LPF and notch filter with values 565, 500 rad/s. The $K_1(s)$ compensator gains are 50, 20 rad/s. The PLL controller along with the current controller resonant gain provides damping for the 6th harmonic present in the grid current.

4.3.6 RT Box Carrier Min/Max Detection

The PLECS RT Box 1 [31] architecture implements the carriers in a FPGA separate to the DSP which executes the control algorithm. By design, the carriers cannot be

accessed through the simulation at the run time. Further, due to two hardware platforms the clock signals cannot be synchronized for discretization time steps other than integer multiples of the carrier period. Hence, a hardware/software method was developed to synchronize carrier min/max with the simulation.

A square wave is generated through the simulation by comparing zero reference with a carrier. The pwm output is then fed to a general purpose output (GPO) port 1 and then it is routed back into the simulation through general purpose input (GPI) port 1, Fig. 4. 12. The acquired synchronization square wave has its rising and falling edges at the half-way the carrier signal. The goal is to phase shift the obtained square wave such that the rising edge coincide with the carrier minimum or maximum. This is done by comparing a phase shifted sine wave with zero to produce the required phase shifted square wave. The phase shifted sine is generated by changing its phase angle. The phase angle consists of two parts; a) periodic phase generated by integrating $2\pi f_c$ and resetting it with every rising edge of the synchronizing square wave and b) base offset required to get correct output, Fig. 4. 13. Resetting the integrator at each rising edge synchronizes the carrier with the simulation (synchronize FPGA with DSP at regular intervals). A discretization offset should be added to eliminate sampling error of the digital signal.

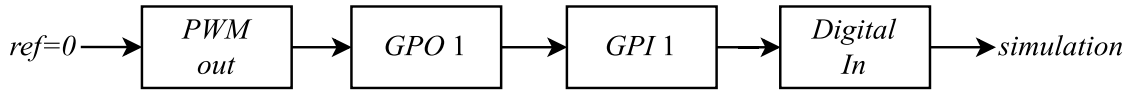

Fig. 4. 12. Routing the synchronizing square wave into the simulation.

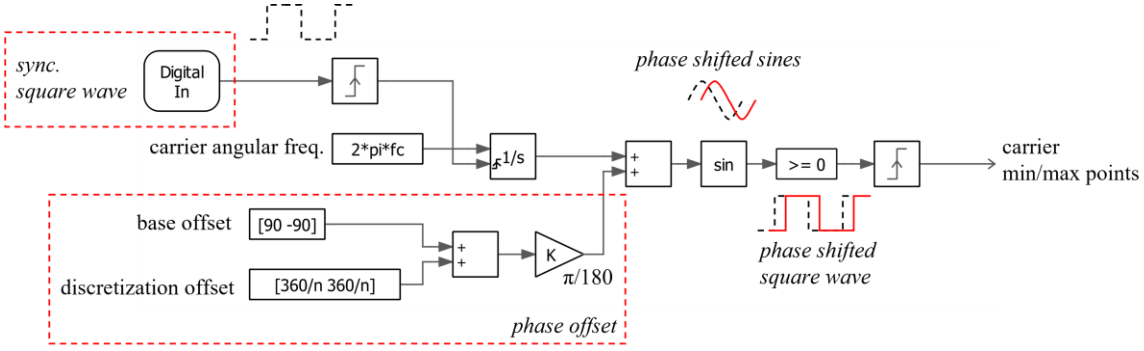

Fig. 4. 13. Synchronizing the simulation with carrier minimum and maximum.

4.4 SUMMARY

Detailed description of the converter control is described. The overall controller is introduced first and its sub-controllers are detailed subsequently. The reference modification algorithm which implements the RPP pwm method is introduced and described with a pseudo-code flow diagram. Additional control methods used to eliminate the grid harmonics is also presented. Lastly, hardware/software combination used to synchronize the carrier minimum and maximum with the simulation is presented which cannot be accessed directly within the PLECS RT Box 1 environment.

Chapter 5

EXPERIMENTAL PERFORMANCE ASSESSMENT

Experimental performance of the converter with the reference-based pulse position (RPP) and fixed phase shift (FPS) methods is compared, and important characteristics are highlighted. Performance curves, oscilloscope captures are presented to support the comparisons. The parameters: rms of the high frequency current, high frequency reactive power, output power, and pulse separation are used for the comparison. Furthermore, converter operational waveforms at different settings are illustrated. Finally, transient responses of the converter for step change in the output current, and output load are presented.

The experimental setup uses PLECS RT Box 1 as the controller. The four three phase two level inverters are interfaced with the high frequency transformers with their connection wires twisted to reduced EMI noise, Fig. 5. 1. To represent the battery operation, a dc source is connected in parallel with a resistor load at the secondary side. The resistance is chosen such that the dc source always supplies current. By disconnecting the dc source, the output behaves as a resistive load. The parameter values used for the experimental analysis are tabulated in Table 5.1. The high frequency reactive power is evaluated using the equations (71) – (73).

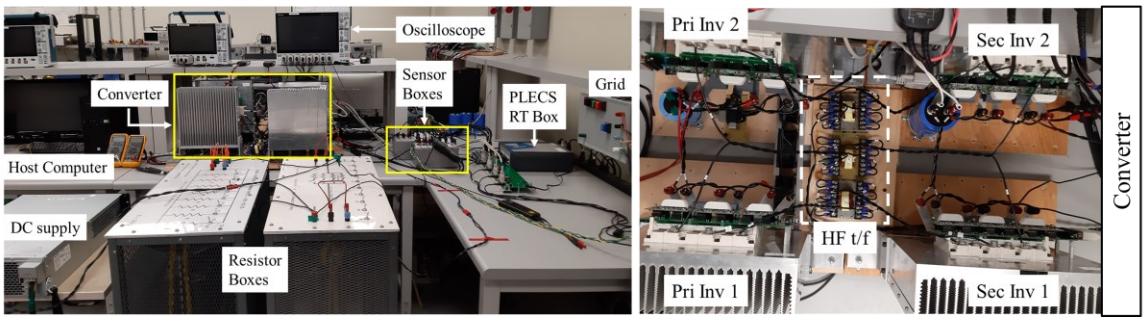

Fig. 5. 1. The experimental setup.

Table 5. 1. System Parameters

Parameter	Value
Switching Frequency (f_c)	10kHz
Fundamental Frequency (f_m)	60Hz
Grid Line Inductance (L_g)	2.5mH
Grid dc Link Capacitance (C_{pri})	1mF
Output dc Link Capacitance (C_{sec})	4mF
Interlimb Leakage Inductance (L_k)	360µH
Transformer Turns Ratio	1:1
Maximum Modulation Index (m_a)	1.035
Nominal Grid Voltage ($V_{g,LL}$)	208V

$$P = 3 * P_{hfA} = i_{hf} * v_{sec} \tag{71}$$

$$S = 3 * v_{sec,rms} * i_{hf,rms} \tag{72}$$

$$Q = \sqrt{S^2 - P^2} \tag{73}$$

5.1 EXPERIMENTAL PERFORMANCE CURVES

The characteristic variation with pulse separation for the RPP and FPS pwm methods follows the same trend pattern as in simulation results. Due to the cycle-by-cycle pulse alignment of the RPP methodology, a reduction in the high frequency rms current and the reactive power can be observed as expected. It is noted that the reduction in the absolute rms and reactive power values are not largely distinctive, however, the concept is proved through experimental results, see Fig. 5. 2,Fig. 5. 3,Fig. 5. 4.

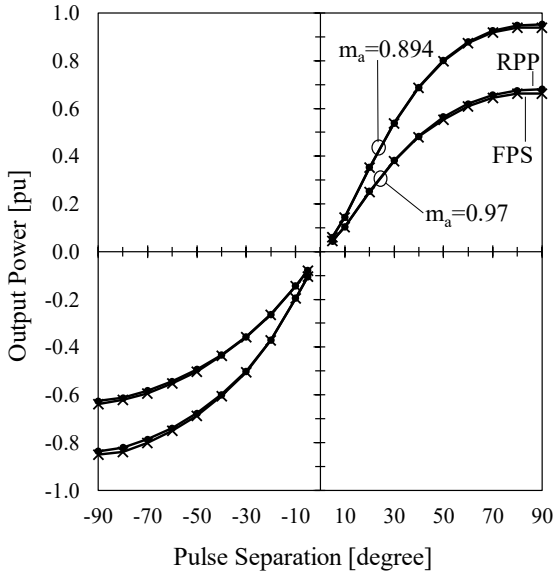

Fig. 5. 2. Experimental output power change against pulse separation. VLL = 104V; Vdc = 175V ($0.97m_a$), 190V ($0.894m_a$); Pbase = 1.3kW.

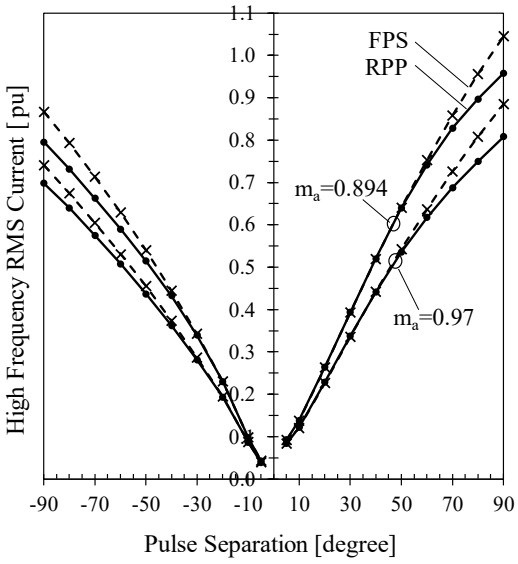

Fig. 5. 3. Experimental high frequency rms current against pulse separation. VLL = 104V; Vdc = 175V ($0.97m_a$), 190V ($0.894m_a$); Pbase = 1.3kW.

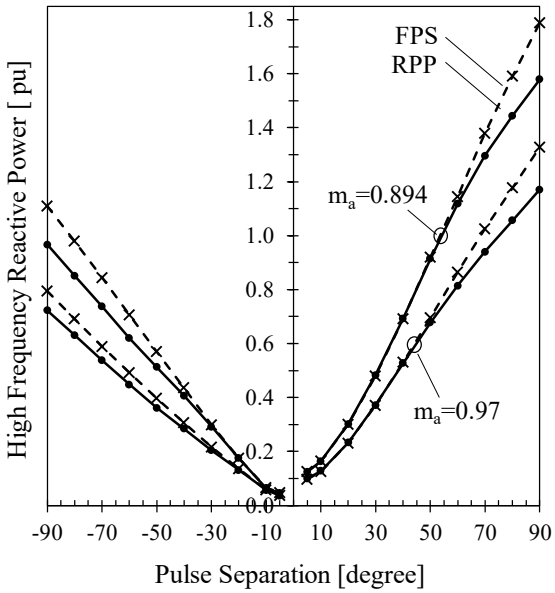

Fig. 5. 4. Experimental high frequency reactive power change with pulse separation. VLL = 104V; Vdc = 175V ($0.97m_a$), 190V ($0.894m_a$); Pbase = 1.3kW.

The high frequency reactive power plotted against the output power reflects the reduction in the reactive content for the same power output. A notable distinction is

observed for higher power outputs which is due to larger pulse separations, see Fig. 5. 5, hence the RPP method has an advantage at higher pulse separations. However, the reactive power of both the methods can surpass 1pu when the output reaches 1pu. Further, the reactive power increases rapidly with the dc link voltage.

The converter was tested for a constant current battery charging application to demonstrate the current control capability. The converter was commanded to output 4.6A while the output voltage being increased from 195V to 250V. At the lower voltage end the pulse separation is made large by the controller to deliver 4.6A and it drops inversely as the voltage reaches the upper end. The high frequency rms followed the φ(t) and the benefit of the RPP method is achieved for separations greater than the minimum pulse width.

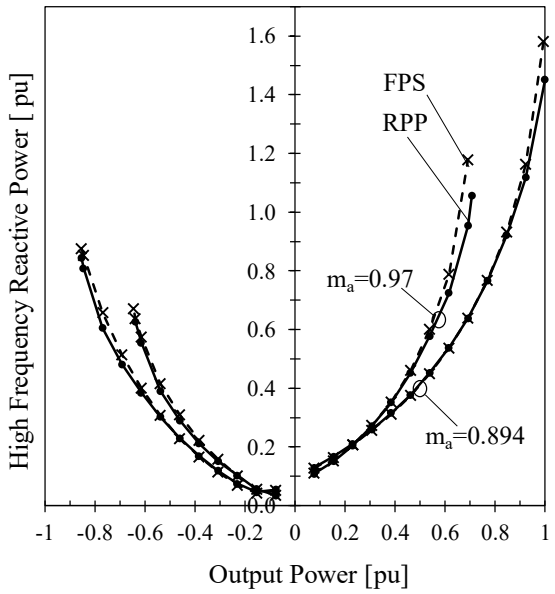

Fig. 5. 5. Experimental high frequency reactive power change with output power. V_{LL} = 104V; Vdc = 175V (0.97m_a), 190V (0.894m_a); Pbase = 1.3kW.

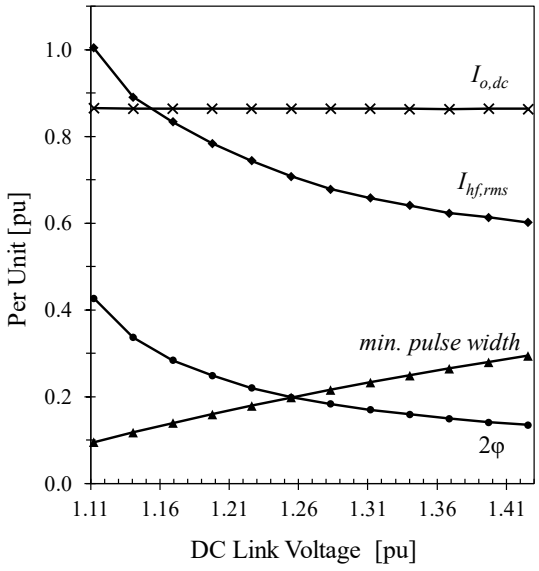

Fig. 5. 6. Experimental illustration of constant current battery charging concept for RPP method. Vbase = 124√2V; Pbase = 1.16kW.

The experimental performance of high frequency rms, reactive power, and output power with the dc link voltage at 50% grid voltage have rapid increments at higher pulse separations. The experiment was conducted only for 1.538 to 1.923 per unit dc link voltage range.

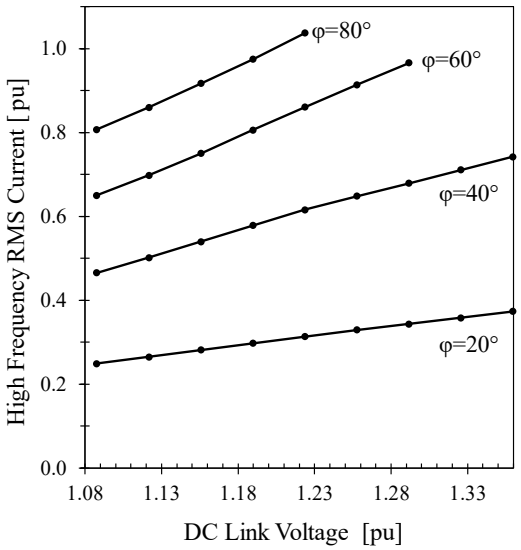

Fig. 5. 7. Experimental high frequency rms current change with dc link voltage.Vbase = 104√2; Pbase = 1kW.

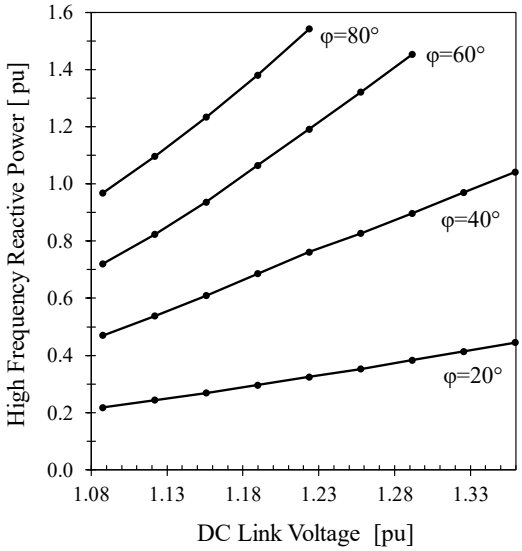

Fig. 5. 8. Experimental high frequency reactive power change with dc link voltage. Vbase = 104√2; Pbase = 1kW.

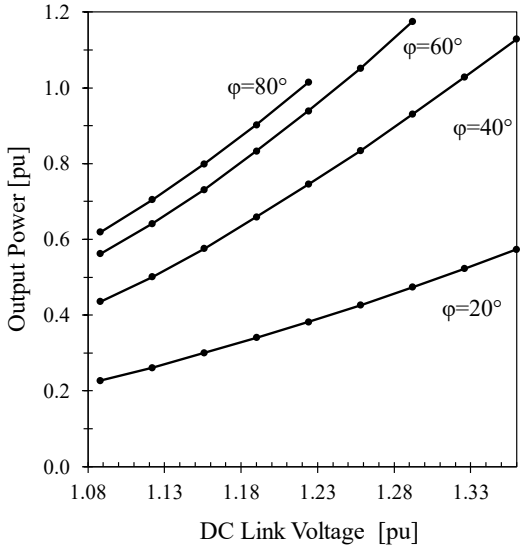

Fig. 5. 9. Experimental output power change with dc link voltage. Vbase = 104√2; Pbase = 1kW.

5.2 OPERATIONAL WAVEFORMS

The experimental high frequency pulse voltage waveforms for the FPS method produce unwanted reactive content when the pulse separation is greater than the pulse

width. On the other hand, the RPP method avoids such occurrences of reactive content by aligning the voltage pulses next to each other, Fig. 5. 10 against Fig. 5. 11. The commanded φ is implemented for pulse widths larger than the φ, Fig. 5. 12, Fig. 5. 13.

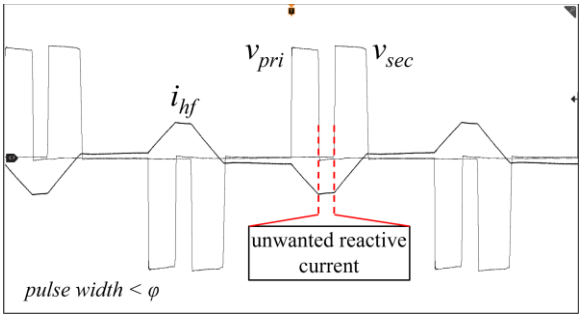

Fig. 5. 10. Experimental FPS operation for pulse width < φ. V_{LL} = 104; Vdc = 180V; φ = 60°.

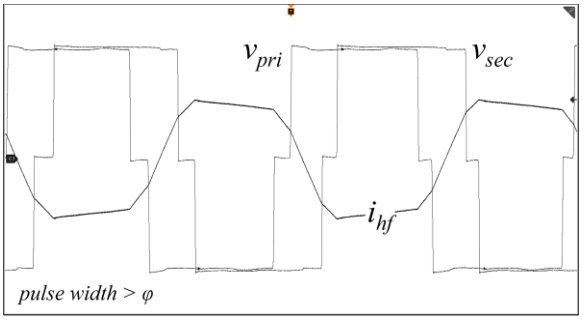

Fig. 5. 12. Experimental FPS operation for pulse width > φ. V_{LL} = 104; Vdc = 180V; φ = 60°.

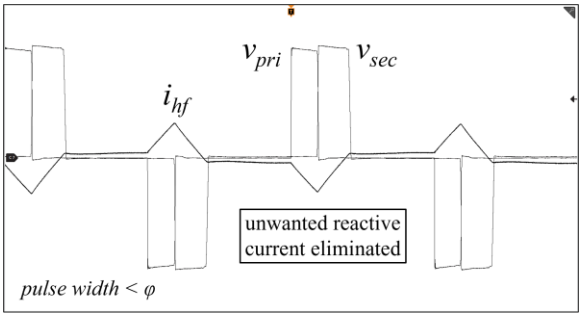

Fig. 5. 11. Experimental RPP operation for pulse width < φ. V_{LL} = 104; Vdc = 180V; φ = 60°.

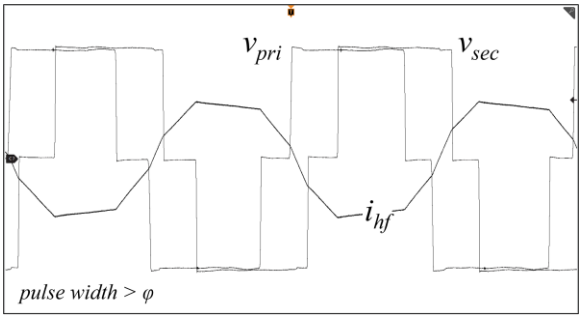

Fig. 5. 13. Experimental RPP operation for pulse width > φ. V_{LL} = 104; Vdc = 180V; φ = 60°.

Scope settings for Fig. 5. 10 – Fig. 5. 13: time 20us/div, voltage 50V/div, current 5A/div.

Fig. 5. 14 to Fig. 5. 17 illustrates the operation of the RPP pwm method for pulse separations 20, 40, 60, and 80 degrees. The change in the high frequency current waveshape can be clearly observed with pulse separation. Where, V_{ga} and $i_{g,abc}$ represents the grid voltage (phase A) and three phase currents, i_{pa1} the primary inverter 1 phase A winding current, i_{hf} the high frequency current, $i_{out,dc}$ the output dc current.

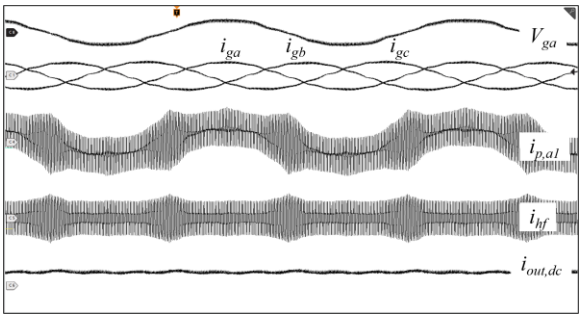

Fig. 5. 14. Experimental 20 degrees. $i_{g,abc}$ 10A/div; i_{pa1}, i_{hf} 5A/div; $i_{out,dc}$ 5A/div; time 4ms/div; Vga 200V/div. V_{LL} = 104V; Vdc = 180V.

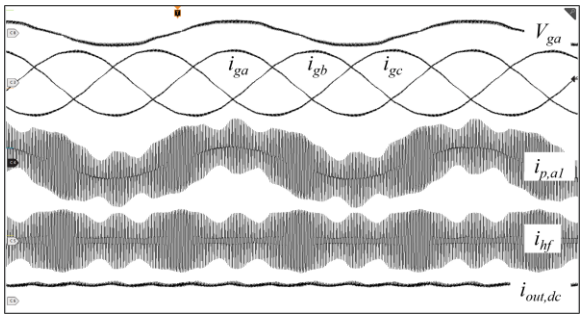

Fig. 5. 16. Experimental 60 degrees. $i_{g,abc}$ 10A/div; i_{pa1}, i_{hf} 10A/div; $i_{out,dc}$ 10A/div; time 4ms/div; Vga 200V/div. V_{LL} = 104V; Vdc = 180V.

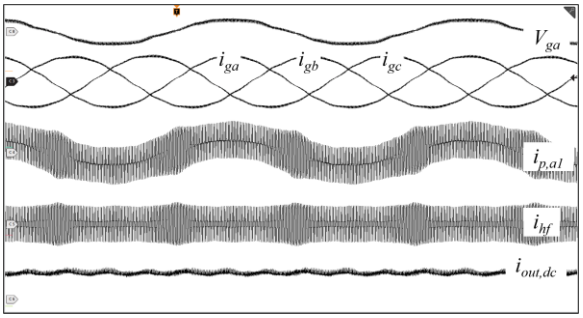

Fig. 5. 15. Experimental 40 degrees. $i_{g,abc}$ 10A/div; i_{pa1}, i_{hf} 10A/div; $i_{out,dc}$ 5A/div; time 4ms/div; Vga 200V/div. V_{LL} = 104V; Vdc = 180V.

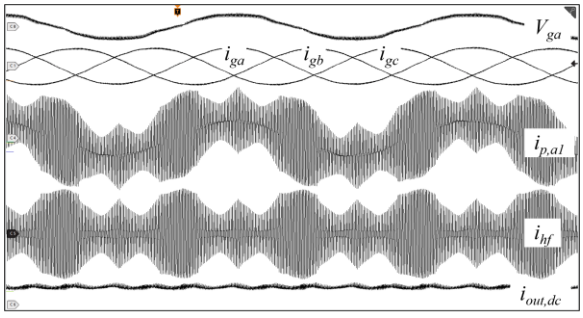

Fig. 5. 17. Experimental 80 degrees. $i_{g,abc}$ 20A/div; i_{pa1}, i_{hf} 10A/div; $i_{out,dc}$ 10A/div; time 4ms/div; Vga 200V/div. V_{LL} = 104V; Vdc = 180V.

5.3 TRANSIENT RESPONSE

Transient response for change in output current settles within 4 fundamental cycles and provides good control response, Fig. 5. 18, Fig. 5. 19. The current command was changed between 2, and 5.8A. Furthermore, a load resistance was added to the output to show transient response for a load change. The controller is able to provide a solid response to load changes, Fig. 5. 20, Fig. 5. 21. Moreover, power reversal of 1.6kW measured at the output is implemented, Fig. 5. 22, Fig. 5. 23. The grid current when battery is supplying power to the grid has harmonics which could be from the inverter dead-time and grid voltage harmonics. Improving the current quality is one of the future works of this converter.

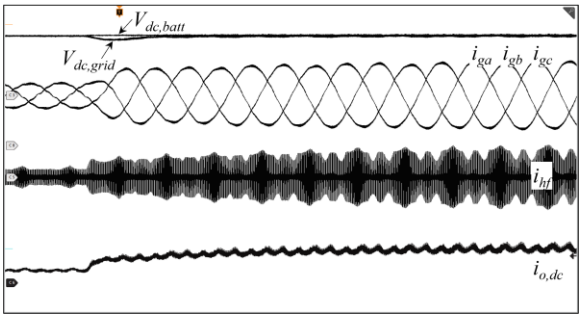

Fig. 5. 18. Experimental transient $i_{out,dc}$ 2A - 5.8A. V_{LL} = 104V; Vdc = 180V. Scope settings: time 10ms/div; $i_{g,abc}$, i_{hf} 10A/div; $i_{out,dc}$ 5A/div; $V_{dc,batt}$, $V_{dc,grid}$ 50V/div.

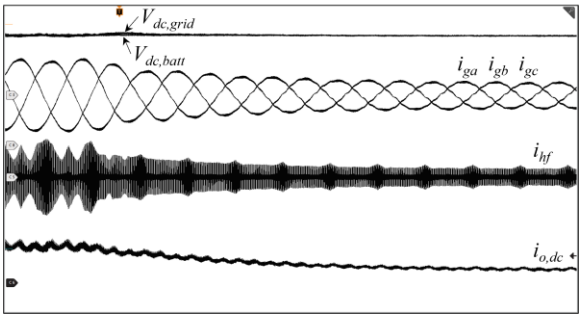

Fig. 5. 19. Transients $i_{out,dc}$ 5.8A - 2A. V_{LL} = 104V; Vdc = 180V. Scope settings: time 10ms/div; $i_{g,abc}$, i_{hf} 10A/div; $i_{out,dc}$ 5A/div; $V_{dc,batt}$, $V_{dc,grid}$ 50V/div.

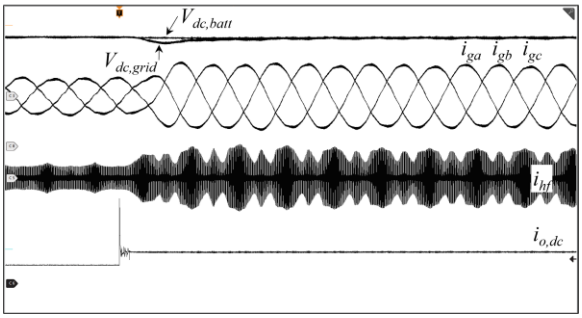

Fig. 5. 20. Experimental transients load change 83 - 40Ω. V_{LL} = 104V; Vdc = 180V. Scope settings: time 10ms/div; $i_{g,abc}$, i_{hf} 10A/div; $i_{out,dc}$ 5A/div; $V_{dc,batt}$, $V_{dc,grid}$ 50V/div.

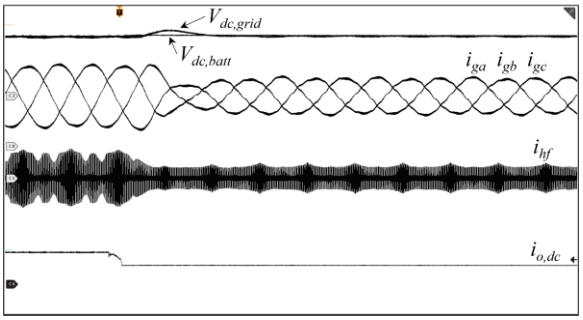

Fig. 5. 21. Experimental transients load change 40 - 83Ω. V_{LL} = 104V; Vdc = 180V. Scope settings: time 10ms/div; $i_{g,abc}$, i_{hf} 10A/div; $i_{out,dc}$ 5A/div; $V_{dc,batt}$, $V_{dc,grid}$ 50V/div.

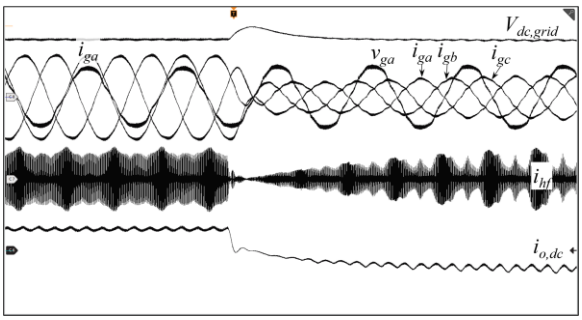

Fig. 5. 22. Experimental power reversal Pout 1.6 to -1.6kW. V_{LL} = 124V; Vdc = 230V. Scope settings: time 10ms/div; $i_{g,abc}$, i_{hf}, $i_{out,dc}$ 10A/div; $V_{dc,grid}$ 50V/div; V_{ga} 100V/div.

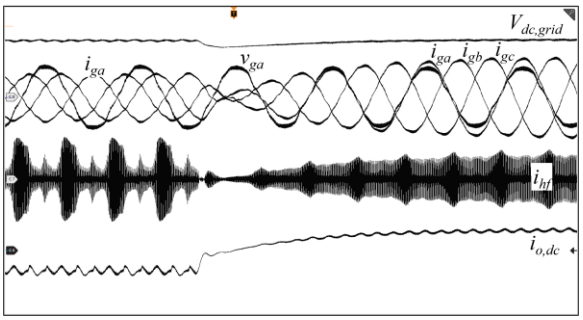

Fig. 5. 23. Experimental power reversal Pout -1.6 to 1.6kW. V_{LL} = 124V; Vdc = 230V. Scope settings: time 10ms/div; $i_{g,abc}$, i_{hf}, $i_{out,dc}$ 10A/div; $V_{dc,grid}$ 50V/div; V_{ga} 100V/div.

5.4 SUMMARY

Key experimental performance curves that compare the reference-based pulse positioning method with the fixed phase shift method are presented. the curves have similar trend as in the simulated performance curves. The experimental results support the analysis and reflect reduction in high frequency rms current and reactive power compared to the FPS approach. A constant current battery charging scenario is experimentally demonstrated by controlling the output current at 4.6A. High frequency voltage and current waveforms at 60° pulse separation show the operation of the pulse alignment algorithm and it is validated. The converter operation is presented through oscilloscope captures at 50% grid, 180V for pulse separations ranging from 20°-80°. Transient responses for power reversal, output current step change, and output load step change demonstrate good control response of the controller.

Chapter 6

CONCLUSION AND FUTURE WORK

A summary of the research work and a brief description of the future developments are provided. Firstly, the research work is summarized, and then future developments are presented.

6.1 SUMMARY OF RESEARCH WORK

Phase shifted pwm is commonly used in DAB and DAB derived isolated converters for high frequency power transfer. The converter under consideration generates a high frequency pulse voltage waveform when controlling the grid current at the primary of the converter. This waveform is constrained by the main pwm which controls the grid current, and the width of these pulses vary throughout the grid fundamental period. The secondary pulse voltage waveform is phase shifted relative to the primary to exchange power. Published works related to the presented single stage converter implements the phase shift (for example 40°) in all the secondary voltage pulses relative to the primary. However, voltage pulses which have lower pulse widths than the phase shift are separated from each other when the phase shift is implemented. An original concept is presented where the secondary inverter is switched to coordinate with the primary, thereby the secondary voltage pulses are positioned in each carrier cycle to lower the reactive content of the high frequency current. If the voltage pulses are separated

beyond their pulse widths a reactive circulating current is generated within the system which increases the high frequency rms current and its reactive content. The proposed a pwm method (RPP) position the secondary voltage pulses next to primary whenever the pulses try to separate each other. This pulse positioning is implemented in each carrier cycle. The proposed control concept allows the converter to be operated at pulse separations beyond 45 degree limit and can reach up to 90 degrees providing a wide control range and a relatively lower sensitivity to change in the control variables. However, the published works only allows 30°-45° phase shifts with 0.8 sine modulation index to avoid pulses being separated. Further, the RPP method modifies the reference signals to achieve the required pulse separation as opposed to conventional carrier phase shift approach. Modifying the reference signals provides more flexibility to achieve a desired output.

The converter is experimentally tested on an isolated single-stage bidirectional three-phase ac-dc converter. The converter processes grid power to the output dc bus through a high frequency transformer which conducts both low frequency grid current and high frequency transformer current. The grid side or the primary generates the high frequency transformer voltage when controlling the grid current. The secondary switches are modulated in such a way to coordinate with the primary voltage waveform to minimize the reactive content.

The main aspects of the research work are the pwm method, control, and the converter topology. Three pwm methods are presented: FPS, RPP, SPP. The operational concept of the FPS method is already published in the literature while the other two are original to the thesis. The square-wave pule position (SPP) method produces the highest reactive content and high frequency rms current thus, within the scope of lowering reactive content the SPP method is dismissed. However, the method can deliver the maximum power output for a given dc link and grid voltage compared to the other two.

The reference-based pulse position (RPP) method is proposed in the thesis which coordinates the high frequency voltage pulses in each carrier cycle as opposed to implementing a fixed phase shift (FPS) throughout the grid fundamental cycle. It should be noted that the phase shift in the FPS is a control variable, and it varies to deliver

variable power output. The term fixed implies that, at the steady state operation the controlled phase shift is a constant value under a 60Hz fundamental period and delivers a specific power value. Both the simulation and experimental results validate the concept of reactive content reduction in the RPP method which is directly comparable to the FPS. The reduction is greater at higher pulse separations. At 90° pulse separation, at $0.97m_a$, and 50% grid an experimental reduction of 8.6% and 11.8% for high frequency rms current and reactive power were observed for the RPP method compared to the FPS method. Further, at $0.894m_a$ reduction of 8.3% and 11.7% were experimentally recorded for the RPP method for the same settings. The output power for both the methods were almost the same with the pulse separation since the volt-seconds for active power remains the same for the two methods. Simulated performance comparison with a single-phase phase-shifted dc-dc DAB reflects that the DAB produces lower reactive power per output power compared to the FPS and RPP. However, the RPP method is close enough to a DAB at higher dc voltages ($\sim 0.7 \leq m_a \leq \sim 0.9$). The FPS method generates the highest reactive out of the three.

The controller is able to control the grid current, primary dc link voltage, output dc current, output voltage, and reference signal. The grid current is controlled in the dq-synchronous reference frame achieving unity power factor at the grid. The grid side capacitor voltage is controlled by the grid current which decouples the primary inverter dynamics from the secondary inverter, which is the main advantage. High frequency current can also be used to control the grid capacitor voltage, however, doing so requires to actively balance the power input with output considering the losses. In contrast the former method does not require a power balancing path and delivers power to the output subjected to the pulse separation. The phase shift controller is able to control the output power, voltage, and current depending on the output circuitry. For a battery mode operation all the three variables can be controlled. Experimentally the output power, and output current control is demonstrated. For load mode operation the output voltage can be controlled which is also demonstrated experimentally. Transient responses are shown for power reversal, step change in output current, and step change

in output load. The converter reaches steady state within 4 fundamental cycles demonstrating good control response.

The converter operates as a single stage converter with 4 three-phase two-level voltage source converters hence, 24 active switches. It is acknowledged that the active device count is relatively high for a single stage ac-dc converter (typically 16 switches for 3x2 matrix converter). However, the converter brings benefits of lowered dc link voltage, reduced magnetics, and multiport functionality. The transformer interlimb leakage inductance is used to transfer the power and the transformer windings are connected in such a way that the 60Hz low frequency flux cancels in the core while remaining high frequency flux. Three different winding arrangements are described which can be used to generate the required leakage inductance based on the application. The converter consists of 3 ports and further it can be expanded to 4 ports. Thus, the benefits the converter bring about favors its application than the higher number of active switches.

6.2 FUTURE DEVELOPMENTS

The following are the selected future developments that can potentially improve the performance of the converter.

1. Low switch-count single stage ac-dc converter

It is acknowledged that the number of switches in the converter, 24, is excessive for a single stage converter. Single stage converter with a switch count in the rage 12 – 16 is preferred. A suitable topology can be explored using 3-limb cores instead of C-cores which would reduce the size of the converter. Further, lower number of switches reduce the switching losses.

2. Using 3-Limb Cores Instead of C-Cores

Using 3-Limb cores can reduce the size and weight of the magnetics of the converter. A sophisticated switching mechanism has to be designed to cancel the low

frequency flux and to provide minimum interference between high frequency flux patterns by the three phases.

3. Design Optimization and Loss Analysis

More detailed analysis can be carried out to optimize the magnetics. A guideline for designing magnetics to achieve specific interlimb leakage inductance can be developed thus, favoring lower size and count in magnetic devices. Further, a loss analysis can be carried out for the selection of appropriate components and to achieve maximum efficiency.

4. Performance Improvement by Introducing Carrier Change

The converter performance can be improved by changing carriers which leads to 5-level high quality pwm line-line inverter output voltage. The current system requires one carrier per each of the two inverter legs (leg 1: 0°, leg 2: 180°) for each phase. An additional set of carriers (90°, 270°) are implemented such that the transition happens from 0° to 90° for leg 1 and 180° to 270° for leg 2. The transition is trigged at the zero crossover of the reference signal. This mechanism lowers the switching harmonics imposed on the grid.

5. Implementing Other Cycle-by-Cycle pwm Control Methods

Two other pwm approaches: peak current control, improved pwm power control, are suggested to provide wide applicability of the converter. The peak current control pwm methodology is designed to maintain the high frequency current at its maximum/or at a controlled value throughout the entire 60Hz grid cycle. The method requires to change secondary voltage pulses so as to maintain the peak current. The latter pwm strategy is designed to deliver maximum possible active power within a carrier cycle and adjust dynamically itself throughout the entire 60Hz cycle.

6. Implementing Control Algorithm in a DSP Environment

The PLECS RT Box 1 does not provide access to the carrier information. Thus, a hardware-software combination was used to implement the RPP method. As a result, there exists a half carrier cycle delay in the controller execution. Furthermore, the

switching frequency is constrained to 10kHz due to the hardware structure of the RT Box. A DSP environment would lower execution delays, allows for high switching frequency operation, and provides more flexibility in carrier level pwm logic handling.

7. Use of Silicon-Carbide (SiC) Devices

The experimental test bench consisted with Silicon IGBT switches with 2us deadtime. The deadtime is excessive and the ratio deadtime to switching frequency increases as the switching frequency increases hence, constrain the maximum frequency. SiC devices with lower deadtime has the potential to decrease the overall size of the magnetics and improve the quality of current waveforms.

8. Four Port Multi-Frequency Control

The control of the converter with 4 ports with two grid connections having two frequencies can be studied. Lowering reactive content in this setting would allow for more efficient multiport functionality.

9. Eliminating the Effect of Grid Harmonics

The laboratory setting has 5^{th} and 7^{th} order harmonics in the grid voltage. Only a software based grid harmonic elimination was discussed in the thesis. Additionally, a properly sized L-C filter can be placed at the grid terminals and the controllers can be tuned to eliminate the effect of the grid harmonics to a larger extent.

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APPENDIX A

PLECS RT BOX 1 C-SCRIPT CODE OF THE REFERENCE MODIFICATION ALGORITHM.

```
static double xa, xb, xc;
double ma;
double xphi, xol;
static double dxa, dxb, dxc; // reference signal
change amount
static double out_s1_a, out_s2_a, out_p1_a,
out_p2_a;
static double out_s1_b, out_s2_b, out_p1_b,
out_p2_b;
static double out_s1_c, out_s2_c, out_p1_c,
out_p2_c;
static double ps; // phase shift in radians

if(InputSignal(0,3) == 1){ // @carrier minimum
// signal sampling and assignment
xa = InputSignal(0,0);
xb = InputSignal(0,1);
xc = InputSignal(0,2);
ps = InputSignal(0,5);
ma = InputSignal(0,6);
/* ################## dx evaluation
###################################
*/
// xmax = ma*K; // maximum of reference signal
xol = fabs(ps/pi);
xphi = 1 - xol; // ref signal value for min pulse
width at PS value.
// Phase A
if((xphi >= fabs(xa))&&(fabs(xa) >= 0)){
dxa = xol;
} else {dxa = 1 - fabs(xa);}
// Phase B
if((xphi >= fabs(xb))&&(fabs(xb) >= 0)){
dxb = xol;
} else {dxb = 1 - fabs(xb);}
// Phase C
if((xphi >= fabs(xc))&&(fabs(xc) >= 0)){
dxc = xol;
} else {dxc = 1 - fabs(xc);}
/* ################## End of dx evaluation
############################### */
/* ############ Reference Modification based
of PS polarity ############## */
if(ps >= 0){
// DTC Phase A @ min point PS >= 0
if(xa >= 0){
out_s1_a = xa - dxa - dx_dt;
out_s2_a = -xa - dxa;
out_p1_a = xa + dxa;
out_p2_a = -xa + dxa;
}else {
out_s1_a = xa - dxa;
out_s2_a = -xa - dxa - dx_dt;
out_p1_a = xa + dxa;
out_p2_a = -xa + dxa;
}


// DTC Phase B @ min point PS >= 0
if(xb >= 0){
out_s1_b = xb - dxb - dx_dt;
out_s2_b = -xb - dxb;
out_p1_b = xb + dxb;
out_p2_b = -xb + dxb;
}else {
out_s1_b = xb - dxb;
out_s2_b = -xb - dxb - dx_dt;
out_p1_b = xb + dxb;
out_p2_b = -xb + dxb;
}
```

```
// DTC Phase C @ min point PS >= 0
if(xc >= 0){
out_s1_c = xc - dxc - dx_dt;
out_s2_c = -xc - dxc;
out_p1_c = xc + dxc;
out_p2_c = -xc + dxc;
}else {
out_s1_c = xc - dxc;
out_s2_c = -xc - dxc - dx_dt;
out_p1_c = xc + dxc;
out_p2_c = -xc + dxc;
}
} else {
// DTC Phase A @ min point PS < 0
if(xa >= 0){
out_s1_a = xa + dxa + dx_dt;
out_s2_a = -xa + dxa - dx_dt;
out_p1_a = xa - dxa;
out_p2_a = -xa - dxa;
}else {
out_s1_a = xa + dxa - dx_dt;
out_s2_a = -xa + dxa + dx_dt;
out_p1_a = xa - dxa;
out_p2_a = -xa - dxa;
}
// DTC Phase B @ min point PS < 0
if(xb >= 0){
out_s1_b = xb + dxb + dx_dt;
out_s2_b = -xb + dxb - dx_dt;
out_p1_b = xb - dxb;
out_p2_b = -xb - dxb;
}else {
out_s1_b = xb + dxb - dx_dt;
out_s2_b = -xb + dxb + dx_dt;
out_p1_b = xb - dxb;
out_p2_b = -xb - dxb;
}
// DTC Phase C @ min point PS < 0
if(xc >= 0){
out_s1_c = xc + dxc + dx_dt;
out_s2_c = -xc + dxc - dx_dt;
out_p1_c = xc - dxc;
out_p2_c = -xc - dxc;
}else {
out_s1_c = xc + dxc - dx_dt;
out_s2_c = -xc + dxc + dx_dt;
out_p1_c = xc - dxc;
out_p2_c = -xc - dxc;
}
}
/* ####### End of Reference Modification
based of PS polarity ############ */

}

if(InputSignal(0,4) == 1){ // @carrier maximum
// signal sampling and assignment
xa = InputSignal(0,0);
xb = InputSignal(0,1);
xc = InputSignal(0,2);
ps = InputSignal(0,5);
ma = InputSignal(0,6);
/* ################## dx evaluation
###################################
*/
// xmax = ma*K; // maximum of reference signal
xol = fabs(ps/pi);
xphi = 1 - xol; // ref signal value for min pulse
width at PS value.
// Phase A
if((xphi >= fabs(xa))&&(fabs(xa) >= 0)){
dxa = xol;
} else {dxa = 1 - fabs(xa);}
// Phase B
if((xphi >= fabs(xb))&&(fabs(xb) >= 0)){
dxb = xol;
} else {dxb = 1 - fabs(xb);}
// Phase C
if((xphi >= fabs(xc))&&(fabs(xc) >= 0)){
dxc = xol;
} else {dxc = 1 - fabs(xc);}
/* ################## End of dx evaluation
############################## */
/* ############ Reference Modification based
of PS polarity ############## */
if (ps >= 0){
// DTC Phase A @ max point PS >= 0
if(xa >= 0){
out_s1_a = xa + dxa;
out_s2_a = -xa + dxa + dx_dt;
out_p1_a = xa - dxa;
out_p2_a = -xa -dxa;
}else {
out_s1_a = xa + dxa + dx_dt;
out_s2_a = -xa + dxa;
out_p1_a = xa - dxa;
out_p2_a = -xa - dxa;
}
```

```
// DTC Phase B @ max point PS >= 0
if(xb >= 0){
out_s1_b = xb + dxb;
out_s2_b = -xb + dxb + dx_dt;
out_p1_b = xb - dxb;
out_p2_b = -xb - dxb;
}else {
out_s1_b = xb + dxb + dx_dt;
out_s2_b = -xb + dxb;
out_p1_b = xb - dxb;
out_p2_b = -xb - dxb;
}
// DTC Phase C @ max point PS >= 0
if(xc >= 0){
out_s1_c = xc + dxc;
out_s2_c = -xc + dxc + dx_dt;
out_p1_c = xc - dxc;
out_p2_c = -xc - dxc;
}else {
out_s1_c = xc + dxc + dx_dt;
out_s2_c = -xc + dxc;
out_p1_c = xc - dxc;
out_p2_c = -xc - dxc;
}
} else {
// DTC Phase A @ max point PS < 0
if(xa >= 0){
out_s1_a = xa - dxa + dx_dt;
out_s2_a = -xa - dxa - dx_dt;
out_p1_a = xa + dxa;
out_p2_a = -xa + dxa;
}else {
out_s1_a = xa - dxa - dx_dt;
out_s2_a = -xa - dxa + dx_dt;
out_p1_a = xa + dxa;
out_p2_a = -xa + dxa;
}
// DTC Phase B @ max point PS < 0
if(xb >= 0){
out_s1_b = xb - dxb + dx_dt;
out_s2_b = -xb - dxb - dx_dt;
out_p1_b = xb + dxb;
out_p2_b = -xb + dxb;
}else {
out_s1_b = xb - dxb - dx_dt;
out_s2_b = -xb - dxb + dx_dt;
out_p1_b = xb + dxb;
out_p2_b = -xb + dxb;
}
// DTC Phase C @ max point PS < 0
if(xc >= 0){
out_s1_c = xc - dxc + dx_dt;
out_s2_c = -xc - dxc - dx_dt;
out_p1_c = xc + dxc;
out_p2_c = -xc + dxc;
}else {
out_s1_c = xc - dxc - dx_dt;
out_s2_c = -xc - dxc + dx_dt;
out_p1_c = xc + dxc;
out_p2_c = -xc + dxc;
}
}
/* ####### End of Reference Modification
based of PS polarity ############ */
}

OutputSignal(0,0) = out_s1_a; // 1
OutputSignal(0,1) = out_s1_b; // 2
OutputSignal(0,2) = out_s1_c; // 3

OutputSignal(0,3) = out_s2_a; // 4
OutputSignal(0,4) = out_s2_b; // 5
OutputSignal(0,5) = out_s2_c; // 6

OutputSignal(0,6) = out_p1_a; // 7
OutputSignal(0,7) = out_p1_b; // 8
OutputSignal(0,8) = out_p1_c; // 9

OutputSignal(0,9) = out_p2_a; // 10
OutputSignal(0,10) = out_p2_b; // 11
OutputSignal(0,11) = out_p2_c; // 12
```