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A MULTIPROCESSOR DESIGN FOR A PHOTODIODE ARRAY DIRECT READER

by

TED MC GOWAN

A THESIS SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND RESEARCH IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

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Date: Sept. 10, 1992

DEDICATION

To

my parents,

my wife Noreen,

and my children Stephen and Nicole.

ABSTRACT

The photodiode array is a linear solid state imaging device. As a spectrochemical detector it allows the simultaneous measurement of spectral information from several resolution elements as opposed to the single resolution element measurements of photomultiplier tubes.

In particular, when a number of short segment photodiode arrays are used to replace photomultiplier tubes in a direct reader, its spectral measurement power is greatly enhanced, allowing it to record simultaneously both analyte spectral line intensity and the background intensity in the immediate vicinity of the line. Access to this information about the background against which the intensity of a spectral line is measured, is a major advantage a photodiode array direct reader has over the more conventional photomultiplier based design. Furthermore, this additional background information is available for several analyte lines in a multielement measurement situation.

A single microprocessor or microcomputer is incapable of supporting several photodiode arrays, all of which require high speed signal conversion and control operations. Furthermore, any successful computer system for a spectrometer based on several photodiode arrays, each of which not only generates

spectra consisting of several data points but several such spectra per analytical measurement, requires highly developed data manipulation capabilities.

The design and construction of a photodiode array signal acquisition and control system based around a network of single board computers is described. The hardware and software developed and the underlying design concept for a networked system of signal acquisition, control, and high-level data processing computers for a photodiode array direct reader is described.

The ability of the system to acquire spectra simultaneously on all channels at integration times as low as 10 milliseconds is demonstrated. This contrasts with a single processor based system which was limited to sequential monitoring of individual photodiode array channels with minimum integration times of 0.1 second.

The performance of the system is shown to be greatly superior to a single computer based design. The reproducibility and quality of the spectra generated show significant improvement. Detection limits compare well with the original photodiode array direct reader system and to photomultiplier based direct readers.

Finally, innovative techniques for the correction of spectral interferences using simulated interference spectra are explored.

ACKNOWLEDGEMENTS.

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CHAPTER 1

INTRODUCTION

1.1 Photomultiplier Tube Based Spectrometers for ICP Spectrometry

The development of reliable and sensitive photomultiplier tubes led to their use in spectrometric instrumentation as far back as 1945 (1). The electronic recording of spectral data offered several advantages over the previous technology which employed photographic plates as detectors. Some of these advantages were superior accuracy, precision and sensitivity, less tedious manual involvement and greatly increased dynamic range (2).

Many types of spectrometers are available to record emissions from spectral sources. Off these, two distinct categories have been developed for determining the concentrations of several elements by the direct measurement of the intensities of their atomic emission spectra. These are:

(i) Sequential spectrometers and
(ii) Simultaneous spectrometers.

Sequential spectrometers used for atomic emission measurements are generally monochromators incorporating an entrance slit, a diffraction grating, an exit slit and a single photomultiplier tube.

Light from the spectral source enters through the entrance slit and is dispersed by the diffraction grating. The diffraction grating can be rotated so that a distinct spectral band incorporating the specific wavelength of an analyte is passed

through the exit slit. The intensity of the emission is measured by the photomultiplier tube.

To accurately measure the emission intensity for an atomic species it is important that the background upon which the emission appears is also measured.

The scanning monochromator can obtain some information about this background by scanning across a narrow wavelength range on either side of the spectral line. Its main disadvantage is that the recording of this background signal is sequential rather than simultaneous i.e., ideally both the analyte signal and the background in its vicinity should be recorded simultaneously. For multielement determinations this type of spectrometer will also have to sequentially record the intensities of spectral emissions for all elements.

Various manufacturers have developed what are termed "slew-scanning" spectrometers employing this sequential approach to multielement atomic emission measurements. These spectrometers allow fast rotation of the grating (slew) from one analyte line to the next and then slowly scan the line profile and background in its vicinity. Similar to other sequential spectrometers, a constant analyte signal is required and these spectrometers are generally unsuitable if used with solid sample introduction devices which generate transient signals.

The photomultiplier tube based direct reader has become the standard simultaneous instrument for multielement quantitative atomic spectroscopy. A well known configuration for this type of spectrometer is shown schematically in Figure 1. This configuration is known as the Paschen - Runge mount and is based on the Rowland circle principle. This uses a concave reflective diffraction grating with a radius of curvature equal to the

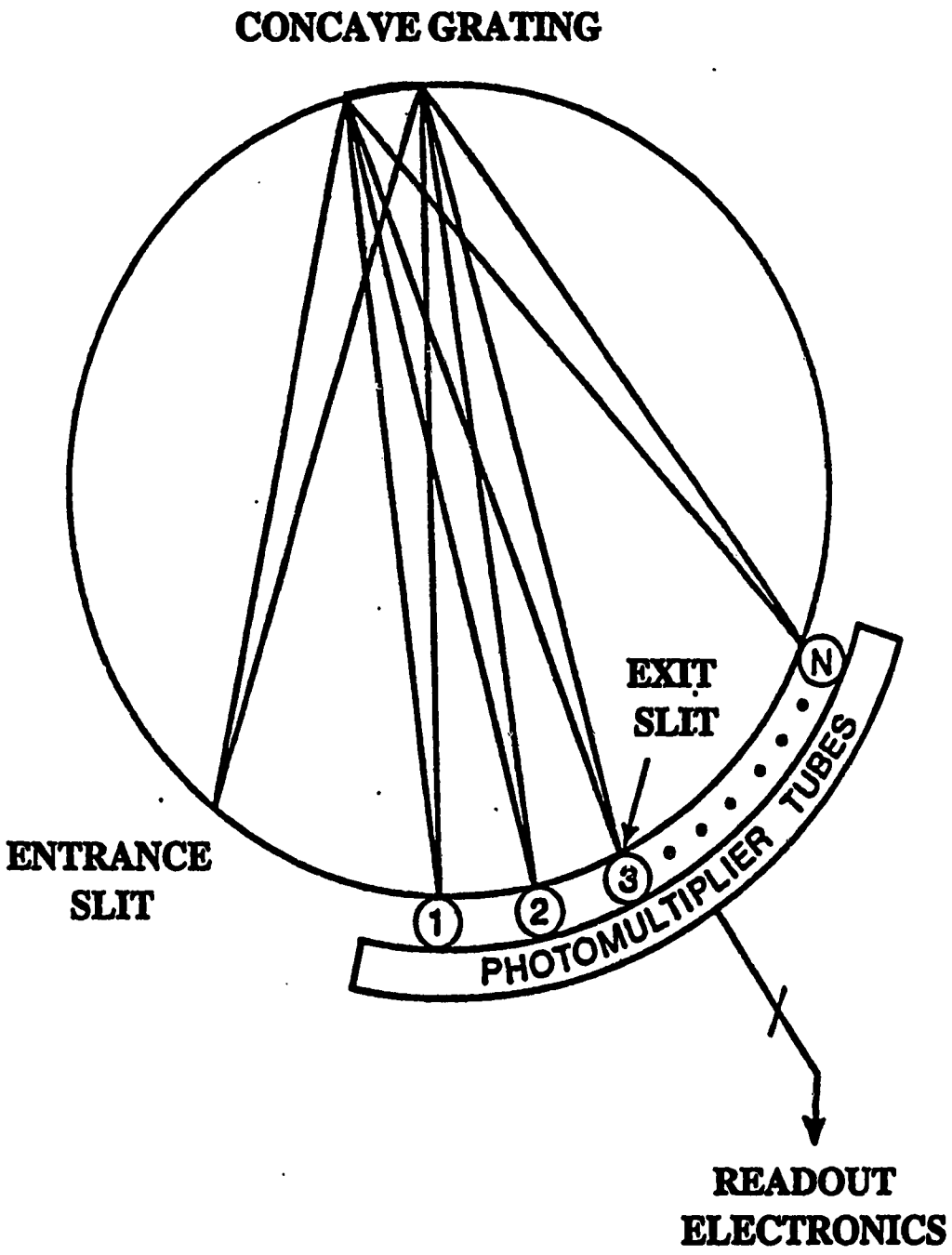


Figure 1. *The photomultiplier tube based direct reader*

diameter of the Rowland circle. Light from a slit on the circumference of the Rowland circle is dispersed and re-focused by the concave grating to images along the circumference of the same circle. Exit slits and secondary optics are used to isolate and transfer specific spectral lines to the individual photomultiplier tubes (PMTs). Each exit slit-PMT combination is frequently referred to as a channel.
This is a simple optical system which has a concave grating as the single optical device within the instrument. The focal circle is therefore free, allowing for the dicretionary positioning of detection devices.

A commercial direct reader having this configuration is the Compact Atomcounter which was manufactured by the Jarall-Ash company prior to 1961. This direct reader had a focal curve opposite the grating of 1.5m. The reciprocal dispersion is give by:

$$\frac{d\lambda}{dl} = \frac{a \cos \beta}{nr}$$

where:

$\frac{d\lambda}{dl}$ = rate of change of light wavelength with change in position around the Rowland circle

a = grating ruling interval
n = spectral order
r = radius of curvature of the grating
β = angle of dispersion of a particular wavelength of light

This is a medium resolution instrument with a typical reciprocal dispersion of approximately 0.55 nm per mm in the first order.

With such a direct reader spectral line intensities can be measured with relative standard deviations of about 1% (3) and a linear dynamic range of about seven orders of magnitude.

Despite the capabilities of the photomultiplier tube based direct reader, it still lacks many of the features desired for an ideal atomic emission measurement system, especially when used with an inductively coupled plasma (ICP) atomic emission source. Chiefly among these are it's lack of versatility and its inability to record the total spectrum or continuous wavelength information. The latter is of great importance when the spectral background in the vicinity of the analyte line is unknown or variable.

The versatility problem arises when it is desirable to observe an alternative spectral line to the one the manufacturer originally designed the instrument to monitor, or, to record intensities of a number of spectral lines which are in very close proximity to each other. The initial task (to add to or alter a channel in the field) is achievable but requires a lot of expertise and perhaps even the assistance of the manufacturer, while the latter is almost impossible to carry out. To select an alternative spectral line requires placing the exit slits, mirrors and wavelength selection filters with great accuracy since the actual entrance slit images are of the order of tens of micrometers in width. For spectral lines occurring very close together the only remedy is to use a system of mirrors, this is both extremely difficult and not always successful. Some manufacturers attempt to increase the versatility of the direct reader by including a scanning monochromator (4) with the system (sometimes called an n+1 channel).

1.1.1 The Background Correction Problem

This lack of versatility makes the direct reader inadequate for many applications, especially as a non-routine general purpose spectrometer. Also difficulties in quantifying background radiation which originates in a spectroscopic system (i.e., either in the source or in the spectrometer) is a major impediment to the computation of accurate analytical measurements. This background radiation is a particular problem in an atomic emission source such as the ICP which produces a wealth of populated higher energy atomic levels and thus numerous spectral lines. The ICP also emits a continuum which tends to complicate measurements for some elements. This excitation of a large number of spectral lines naturally gives rise to situations where two or more lines overlap, leading to spectral interferences.

To achieve an accurate measurement of the intensity of an analyte spectral line in the presence of a variable spectral background, it is necessary to obtain the complete background signal in the vicinity of the line. Obviously, the acquisition of both the spectral line and its background signal simultaneously is an advantage.

In situations where direct spectral overlaps occur, accurate measurements of the spectral intensity of the analyte line can only be made after subtraction of the signal component due to the interferent. This can only be achieved if the interferent itself can be quantified accurately and preferably simultaneously in another measurement channel. This of course means that the the spectral line intensity of the interferent and its background signal are both required. Therefore ideally, in cases of direct spectral overlaps, two measurements of signal plus background (that of analyte and interferent) must be made simultaneously.

Current photomultiplier based direct readers are incapable of making such simultaneous measurements of analyte signal plus background. Therefore the accuracy of corrections in cases of spectral overlaps is poor. A detailed discussion of the sources of various spectral interference is given in Chapter 7 of this thesis.

1.1.2 Current Background Correction Methods used with Photomultiplier Tube Direct Readers.

Current background correction methods for PMT based direct readers can be catogerized as either **on-peak** of **off-peak** methods.

On-peak corrections can be very accurate but require that the interfering concomitant has its own measurement channel on the direct reader. Prior to ordering the instrument, all the matrices to be tested must be specified so that the necessary detection channels are placed in the focal plane or curve.

Before an analysis, the response of each of the channels of the spectrometer to the individual matrix elements is obtained. Interferent calibration curves of apparent concentration of the analyte against the actual concentration of the interfering matrix element are prepared. During analysis, measurements of the interfering matrix elements are made in separate channels and using this data corrections are made to the analyte concentrations. The corrections are determined from the working calibration curve (i.e., of apparent concentration of analyte caused by the interferent in the analyte channels).

On-peak correction is the only way to correct for direct spectral overlaps in PMT-based direct readers. It requires that the positions of all the exit slits be established with respect to the

diffraction grating and the entrance slit. This is achieved by thermostatic control of the instrument.

Off-peak correction methods are used to correct for background radiation in the vicinity of the spectral line. Using these methods the spectral bandpass falling on the exit slit is shifted slightly so that the background on either side of a spectral line is measured by the detector.

To achieve an off-peak measurement two approaches have been taken, both of which involve an effective shifting of the angle at which the incident light meets the diffraction grating. One of these methods involves physically shifting the entrance slit. This requiires a high degree of precision. It has also the disadvantage that it changes the position of the slit with respect to the spectral source. It is well known that the intensity profile of spectral lines emitted from the ICP is position dependent and therefore background measurements may be inaccurate.

The other method for off-peak measurements involves rotating a quartz refractor plate located just behind the entrance slit. The rotation of the refractor plate causes an effective shift in the position of the entrance slit with reference to the grating. This method once again requires a very precise movement to change the angle of rotation. There may also be changes in reflectivity at the plate surface (6) with rotation angle.

Off-peak measurements can correct for continuum radiation and stray light but not for spectral overlaps. It requires a stable source and would therefore not be successful if used with ICP sample introduction systems which generate transient emission signals.

To conclude therefore, continuum, wing (close encounters) and direct spectral interferences can be major problems in ICP emission spectrometry. As a result, simultaneous multiple wavelength monitoring of several spectral lines and of the background in the vicinity of these lines, is often required in order to arrive at an accurate analytical result for the analyte.

The use of photodiode arrays as detector elements in direct reading spectrometers may offer solutions to many of the above problems.

1.2 A Photodiode Array Based Direct Reader

Evans (5) designed a photodiode array direct reader to overcome some of the major disadvantages of PMT based systems.

These disadvantages, as already described included limited versatility and inadequate simultaneous spectral information measurement, especially in the vicinity of the spectral line of the analyte. A photodiode array offers a spatially continuous detector to tackle these problems.
Self scanning linear photodiode arrays (PDAs) have been utilized in many areas where spectrochemical measurements (7-10) are required. These range from astronomy for very low light level measurements (11) to a plethora of laboratory spectrochemical measurement systems.

Detailed discussions on the use of photodiode arrays for atomic spectrochemical measurement are given by both Horlick (12) and McGeorge (13).

Photodiode arrays are fabricated on a silicon chip. The physical length of the array itself is about 1 cm for a 1000 element photodiode array unit. The height of an individual

photodiode element of the array is no greater than 2.5 mm. All the commercial arrays are linear and therefore some problems could be envisaged when attempting to focus all pixels of the array in the curved focal plane of a direct reader. This problem can be alleviated if not elimated by using short 128-element arrays.

The 2.5 mm height of the photodiode is also much less than the image of the entrance slit (1 cm) in the focal plane and as a result not all the light reaching the focal plane of the spectrometer is utilized. It would be possible to resort to some form of secondary optics to condense the beam.

In the photodiode array direct reader developed by Evans and Horlick (5) the original secondary optics used with the photomultipier tube design, including the exit slits on the direct reader focal plane have been removed. These have been replaced by the short 128 element photodiode arrays on a moveable carriage (Figure 2).

The photodiode arrays are positioned on a carriage along the focal plane so that each one detects a window of spectral information. Additionally, the photodiode array is mounted so that each diode is parallel to the entrance slit and therefore samples a unique wavelength range of the dispersed light.

The integration times and readout triggering signals for each array are controlled by a single microcomputer which also stores, processes and displays the acquired spectra.

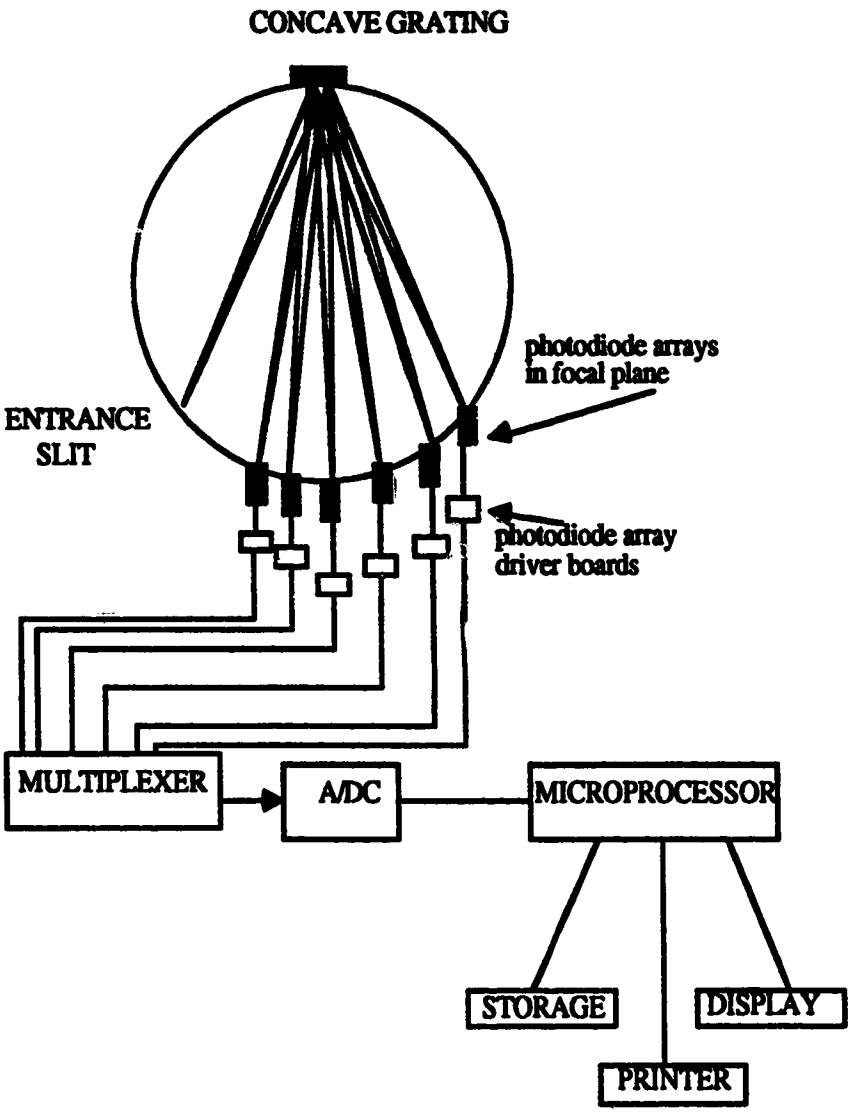


Figure 2 Single processor based multiple photodiode array direct reader

1.3 Advantages and Limitations of the Single - Computer Based Photodiode Array Direct Reader

The successful construction of the initial photodiode array direct reader proved that image sensor technology could be adapted and applied successfully to overcome the unique measurement problems associated with standard PMT based direct readers.

Evaluation of the system indicated that moving the photodiode array window about the focal curve was relatively easy and that choosing a new spectral line was greatly simplified. This removed to some extent the versatility problem associated with direct readers. Spectral backgrounds, measured simultaneously with the analyte signal, indicated that backgrounds from the same array readout could be used to correct for the effect of spectral background features. Signals due to interferent (recorded on other photodiode arrays in the system), when used to correct for direct spectral overlaps proved reasonably successful. For the photomultiplier based direct reader temperature dependent changes in alignment resulted in drifting of the spectral line across the exit slit. This was much less of a problem here since multichannel measurements are taken.

Despite the success of the prototype when applied to relatively simple measurements, it was found to have many major limitations when utilized as a general purpose direct reading spectrometer. Most of these limitations arose from the original design concept utilizing a single microcomputer to perform all the necessary tasks for the entire system. This greatly over extended the available resources of the computer system involved, as indeed it would of any currently commercially available microcomputer system.

A 64K Apple II+ microcomputer was used to handle all the control tasks. These included setting the integration times, sending trigger pulses and capturing data from all six photodiode arrays involved. It also stored, graphically displayed, and processed the spectral data. This burden of tasks on a small microcomputer led to limitations in both flexibility and performance. Also, the use of additional photodiode arrays to expand the system could not be accommodated without total system redesign.

Ideally, the simultaneous readout of all the spectral windows is desired rather than the sequential readout performed by this system. Arising from this sequential array readout, there was a 0.1 second lower limit forced on the possible integration times which could be used. This eliminated the possibility of measuring a number of relatively strong signals (which would require shorter integration times) simultaneously.

Data handling and display facilities were both inadequate and inflexible due to the limited random access memory (RAM) and poor quality graphics. Additionally, the graphical display locked the user into a general data display format for all spectra. No capability for expanding spectra to highlight minor spectral features was available.

Noise problems also arose on readout of arrays leading to a frequent overranging of the signal at the output of the video amplifiers. This prevented signal averaging and often slowed down data processing since each spectrum had to be viewed individually beforehand. This limited confidence in the data acquired and was therefore a serious problem. It is probable that this noise arose from the use of three separate power supplies in the system. The analogue-to-digital converter (ADC) and the pre-amplifiers were powered by a different power supply than the

array driver board. As a result frequent differences in ground potentials were measured.

Besides inadequate grounding, serious problems arose from inadequate shielding of the analogue signals. These were transferred, by both BNC and Ribbon cable from inside the spectrometer to the external Apple II+ based digitization board. The actual ADC itself, which was located on a circuit board inside the Apple II+ was not shielded from transitions occurring nearby.

Several other areas for improvement were noted by the original designer (5), including the need for a better diffraction grating and an improved, more stable array cooling system.

In order to eliminate its major drawbacks and deficiencies, it was evident that the system based on a single microcomputer was inadequate and a totally new system design concept was necessary.

1.4 Alternative System Concept

It has already been demonstrated that a single microcomputer, cannot satisfactorily handle the complex array control and signal acquisition requirements of a multiple photodiode array direct reader. An alternative expandable system, based on a single microprocessor would require the capability of performing parallel analogue-to-digital conversions on several channels simultaneously. This type of system is not available commercially and would virtually be impossible to build from scratch. The ability to store, file and manipulate the large amount of data generated by the multiple PDA direct reader would require an easy to use microcomputer system with powerful graphics and data processing capabilities.

To satisfy all these requirements, an alternative design concept for the system is one that would involve the use of a single computer and digitization system for each array. This subsystem would handle signal pre-treatment, acquisition and control for a single array, and ideally would also perform temporary storage/accumulation of the array signal(s). Additionally, each signal acquisition computer could independently perform signal averaging and take multiple spectra of a transient signal. A number of these single board computers could be networked together, to a "front end" or "host" processor (Figure 3).

The "front-end" processor functions as the user interface for permanent storage, processing, reduction and display of signals.

The acquired data would be transferred digitally, via an RS232C serial interface from the temporary storage on the acquisition computer to the "front-end". Since all analogue signal pre-treatment and conversion would occur inside the grounded light proof box of the spectrometer, a great degree of noise immunity to the RF from the ICP and other external noise sources would be possible. The RS232C standard therefore would be adhered to for communications throughout the networked system. It is probably the most common standard interface supported on computers and it is well understood.

This modular approach would if necessary allow the replacement of the "front-end" or "host" as technology developed, while maintaining the high performance data acquisition component of the system.

The input of parameters such as the integration times for each array by the user, would be accomplished via this "front-end". A file of these parameters could subsequently be

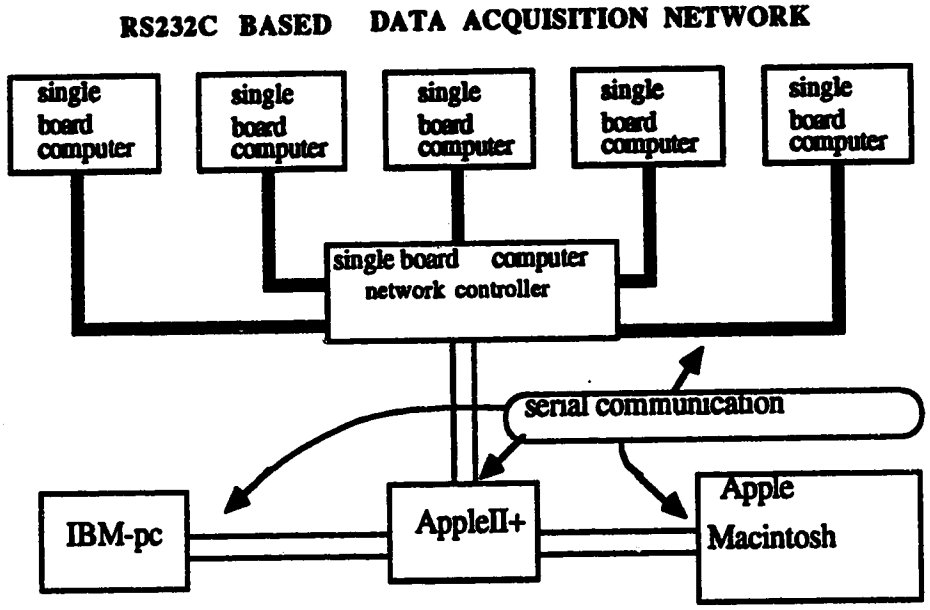


Figure 3 Network concept for multiple photodiode array direct reader.

transmitted over the network to the individual acquisition computers. A controller would serve to control access to the network and trigger all systems for simultaneous spectral acquisition etc.

Data could after acquisition, be transferred serially from the "front-end" to other computer systems if desired, for further processing or to exploit more powerful graphic facilities. The system would also be designed around a single power supply, thus reducing noise from this source (experienced with the previous system).

In summary, what is desired is an ideal single board or "slave" processor to perform all present and projected control and data-acquisition tasks involving the photodiode array, and an ideal "front-end" processor for interaction with the user. A network design incorporating a controller, would facilitate flexible and transparent communication between these two functionally different ends of the system.

The specification required for the single board data acquisition and control computers could therefore be summarized as follows;

1. It should have a large number of Input/Output and control lines.
2. It requires a large amount of onboard RAM (Random Access Memory) for the temporary, sequential storage of several signals.
3. Onboard timers and counters are necessary for the control of integration times.
4. An onboard RS232 communications interface is necessary.
5. An onboard monitor for program development and debugging is required.

6. It should be compact ie. capable of being located together with several other similar systems, inside the dark box of the spectrometer.
7. It should be capable of acquiring and storing data at speeds of 10KHz or greater.
8. It should be relatively inexpensive.

The "front-end" processor would preferably have the following features:

1. Menu or icon-driven
2. User friendly
3. A range of data-processing and graphics software
4. Capable of efficient file handling
5. Permanent data storage facilities
6. Hardcopy and report facilities
7. Software development tools (e.g. cross-assembler) for the development of software for the signal acquisition and control computers.

The goal of this work is to design, build and characterise, such a multiple PDA direct reading spectrometer in the concept of Figure 3, with the above listed features. The hardware and software aspects of the system are presented in Chapters 3, 4 and 5 and a basic evaluation of the resulting system is presented in Chapters 6 and 7. But first, in the next chapter (Chapter 2) the old system is briefly overviewed and summarised.

CHAPTER 2

PRELIMINARY SYSTEM DESCRIPTION

2.1 System Components

The original multiple photodiode array direct reader was designed around a single processor. It was a sophisticated instrument consisting of a number of individual components having varying degrees of complexity. In the development of the new system, some components had to be discarded and replaced, while others were kept intact and incorporated into the new design.

The following components/sub-assemblies which were part of the original design were modified for inclusion in the multiple processor photodiode array direct reader:

- A direct reading spectrometer based on the Rowland circle (Compact Atomcounter).
- The 128 - element photodiode arrays.
- The photodiode array carriages and ribbon cables.
- The modified RC1024S photodiode array driver board.

The following additional hardware sub-systems are necessary as part of the multiple-processor design:

- A single board computer interfaced to each individual photodiode array.
- Separate analog-to-digital converter/track-and-hold amplifiers for each photodiode array/computer system.
- Separate analogue filters and pre-amplifiers for each photodiode array.

- Level conversion circuitry for the serial interface.
- A suitable network which would allow each single board computer access to a common host.
- Hardware for a network controller.
- A suitable computer to act as host.

The choice and subsequent integration of these hardware sub-systems into a functional direct reading spectrometer is described in the next chapter (Chapter 3). Additionally, to have an operational multiple processor photodiode array direct reader, three major software modules are required. These are:

(a) ROM based software in each acquisition computer. For communication with the host, to set integration times, control acquisition of the signal and to both store and accumulate the acquired signal.

(b) ROM based software in the computer which functions as network controller. This software controls triggering and sensing of multiple processor operations while also acting as a data acquisition computer for an attached photodiode array.

(c) Floppy disk based software in the host or "front-end" computer. This software facilitates communication with the user, thereby allowing parameter transmission too, and data retrieval from, the single board computers. Front-end software for performing a variety of other functions such as data transmission to other microcomputers, data reduction and display is also required.

A detailed description of the software and its design for the system is given in Chapter 4.

The following computer systems were used either as part of, or as software development aids for the multiple processor based photodiode array direct reader;

- The John Bell single board computer (John Bell Engineering, Inc. 1014 Center Street, San Carlos, CA 94070)

- The Apple II+ and the Apple Macintosh (Apple Computer, 20525 Mariani Avenue, Cupertino, CA95014)

- The Rockwell AIM65 microcomputer (Rockwell Inc., 3310 Miraloma Ave., P.O. Box 3669, Anaheim, CA92803) was used for EPROM programming.

2.2 The Modified Direct Reading Spectrometer

The direct reader (Jarrell-Ash Company, pre 1961 Compact Atomcounter) and accompanying concave diffraction grating is the same as that originally used by Evans (5).

The original photomultiplier tube detectors, exit slit assemblies and electronics had been discarded. The light proof box had been mounted on a steel frame and the entrance slit is 51.5 cm above the floor making it compatible with spectral sources mounted at this height on rail beds in the laboratory. The configuration of the spectrometer is known as the Paschen-Runge (14) mount and is based on the Rowland Circle principle (15).

The spectrometer uses a concave diffraction grating with a radius of curvature equal to the diameter of the Rowland Circle. The focal length of the grating is 1.5 meters. Images of the

entrance slit are focused as spectral lines along the circumference of the circle.

Photodiode arrays can be placed along the exit focal plane (Figure 2), limited only by the manouverability of the photodiode mounting stands within the spectrometer. The length of circumference of the useful focal plane is about 1 meter. Therefore many locations are available for detection of spectral lines. Whenever it is physically impossible to place two arrays close enough together then spectra can be be accessed in different spectral orders at other positions on the focal plane. This provides an extra degree of flexibility.

The accessible spectral range is from 200 nm to 600 nm in the first order. The instrument has a reciprocal dispersion ranging from 5.65 nm per centimetre directly opposite the grating, to 5.40 nm per centimetre at the maximum accessible angles of dispersion (first order).

2.3 The Reticon RL128 Photodiode Array.

The Reticon "S" Series linear self scanning photodiode arrays have been specially designed for spectroscopic work. They have an aspect ratio of 100:1 (i.e., 2.5 mm high and set on 25 μm spacing). In most previous arrays the photodiode elements were not as high and therefore could not sample as large a portion of the slit image.

Each 128 element array is capable of sensing a spectral window of 1.4 to 1.8 nm (in the first order) depending on whether it was mounted directly opposite the grating or at the maximum angle of dispersion. Although not used in this design, PDA's of 64, 256, 512, 1024, 2048 and 4096 elements are available.

PDA's consist of parallel rows of p-type silicon on a substrate of n-type silicon (Figure 4). Hole electron pairs can be generated by light falling on both the n and p-type silicon. The diodes operate in a charge storage mode i.e. the p-n junctions are reverse biased and therefore act like small capacitors and store charge. To recharge a photodiode to full reverse bias the p-type bars are grounded while the n-type substrate is maintained at a positive potential.

The acquisition of a spectrum using this photodiode array is carried out electronically. Initially a positive start pulse is sent to the shift register on the array. This "high" logic level opens a FET switch which connects the p-type bar to a previously grounded video line thereby recharging the photodiode to full reverse bias. The recharging process takes about 1 μs following which the p-type bars are again isolated from ground. A clock shifts the bit in the shift register therefore addressing the FET switch for the next photodiode and it is recharged in a similar fashion. This process continues until all of the 128 photodiodes are recharged. The freshly charged photodiodes can now be discharged at a rate proportional to the intensity of the light impinging on them. After a period during which discharge is allowed to take place (known commonly as the integration time), the photodiodes are again recharged to full reverse bias in exactly the same fashion as previously described. This time, the amount of discharge which is registered by the video signal line is converted by the analogue circuitry to a voltage which is digitized by the computer system.

These Reticon arrays have additional features including both dummy diodes (16) and separate shift registers for readout of the odd and even photodiodes. The dummy diodes serve to generate a signal on a separate video line, therefore generating the equivalent capacitively coupled switching transients as the active

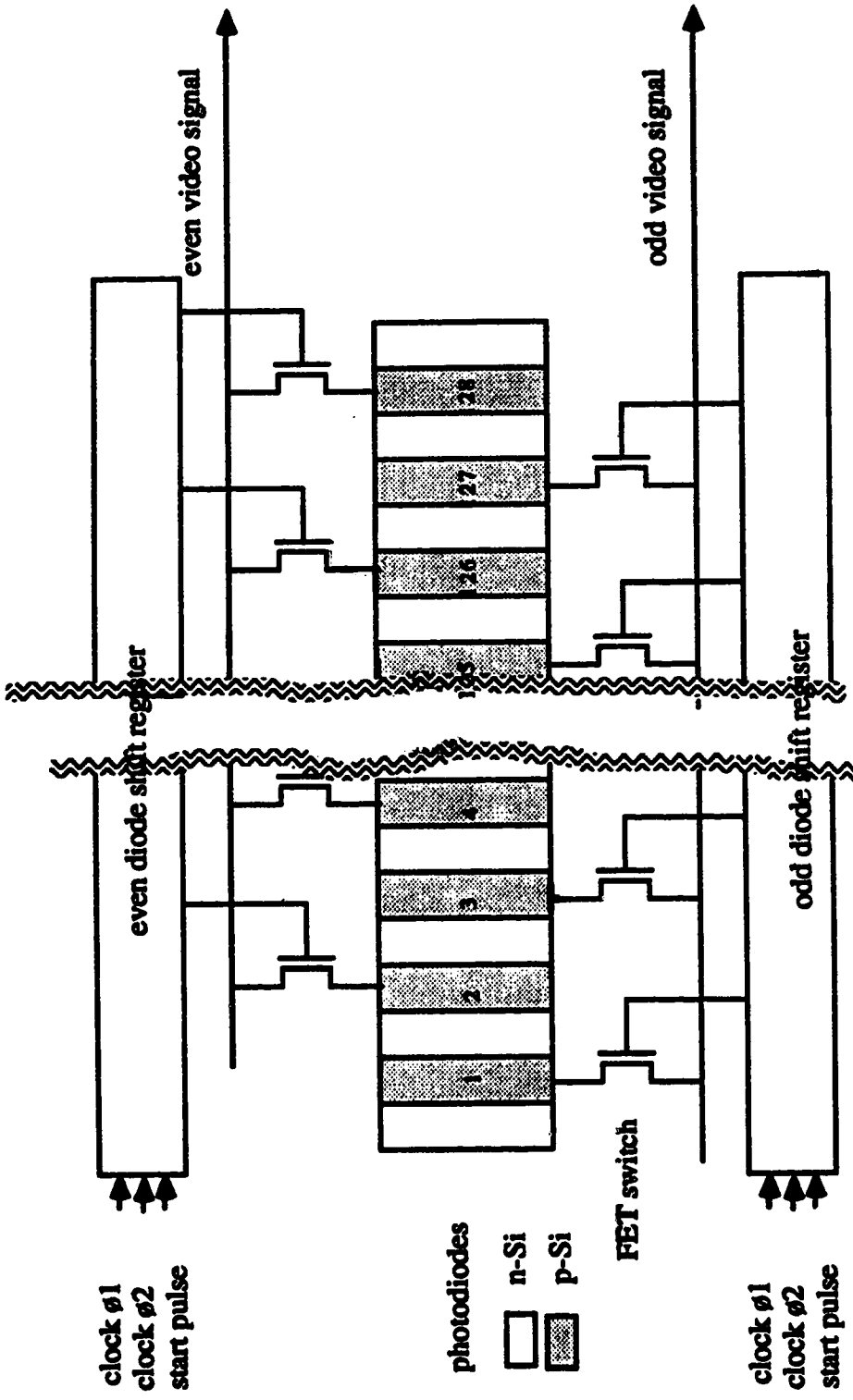


Figure 4 Linear photodiode array design

photodiodes. Differential processing of both dummy and active video signals is used to diminish the effect of these transients.

Separate shift registers and video outputs for odd and even photodiodes, have to be accompanied by separate signal processing circuitry. This often leads to an odd-even pattern which adds to fixed pattern signal generated by other sources. This can be minimized by control potentiometers on the analogue driver board but can be directly subtracted by the computer using a background or "dark current" spectrum.

2.4 The RC1024S Printed Circuit Drive Board.

The RL128 photodiode array was originally received from the manufacturer mounted on the RC1024S printed Circuit Board (24 cm wide by 12 cm high).

This circuit board provides both the complete digital circuitry for clocking and readout of the array in addition to analogue circuitry to process the video signals (Figure 5). An onboard oscillator provides the time base with which the integration time and all the clock signals required for readout of the array are generated. The board performs a number of control functions ranging from regulation of input drive voltages, synchronization of clock signal edges, differential readout of active and dummy photodiodes and the combining of the odd and even video signals to produce a single video output.

Circuitry on this board converts the TTL based signals to the MOS levels required to drive the array shift registers and also provides the DC restorative level against which all the video signals were measured.

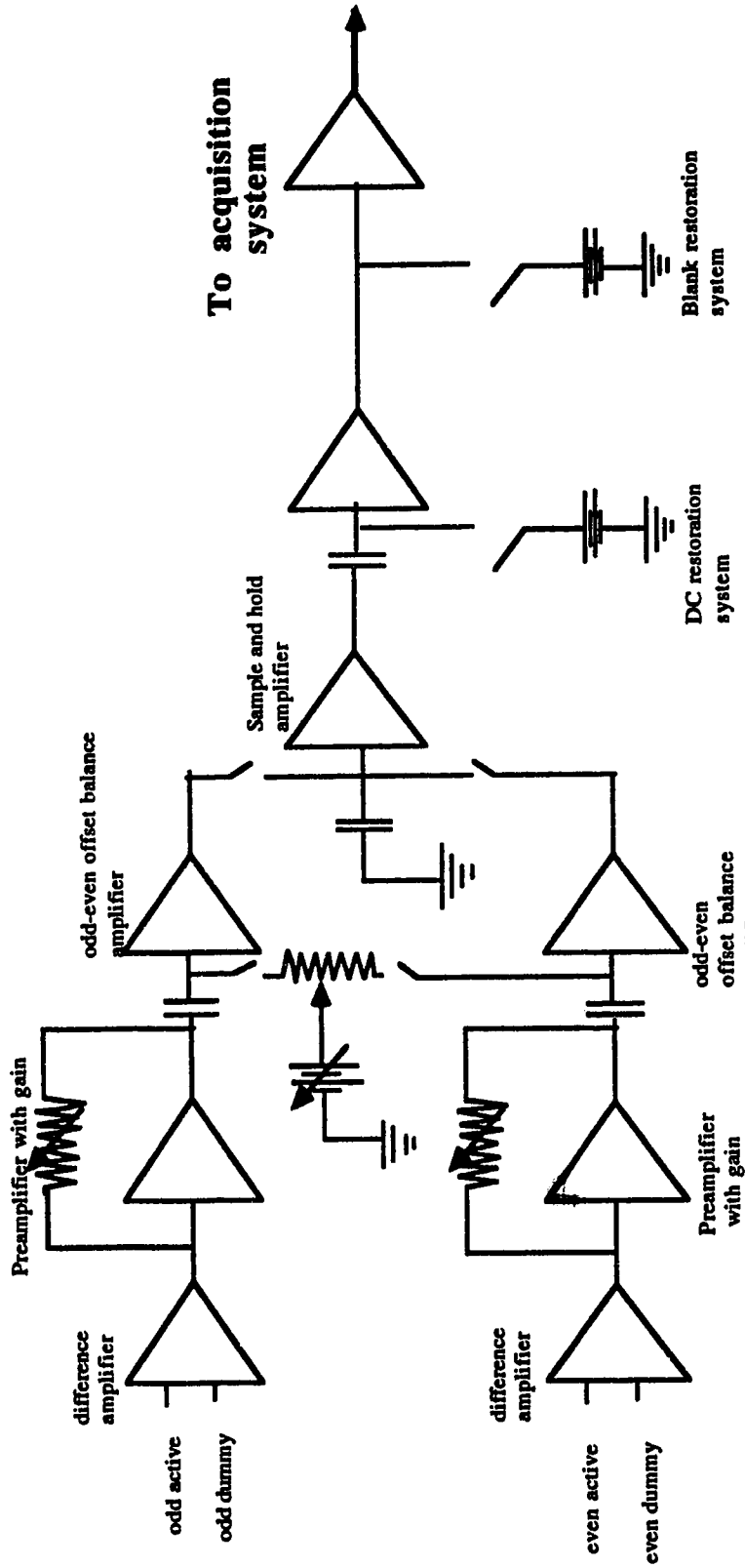


Figure 5 The RC1024S analogue video processing circuitry for the photodiode array

Analogue signal conditioning includes charge to voltage conversion and amplification of the signal to provide a 3 Volt output.

In order to use the photodiode array in the direct reader and extend its versatility, several modifications were made to circuitry on the original RC1024S driver board (5). Some of these modifications were left unchanged and the board was incorporated into the redesigned multiple processor system.

Previous features, left unchanged but integrated into the redesigned spectrometer, are the following:

a) Onboard (RC1024S) semi-automated control over the integration times had been removed and replaced by fully automated microcomputer control.

b) External (computer) generation of a start pulse to initiate readout of the array.

c) The relocated photodiode array. It had been removed from the main driver board for mounting in the focal plane of the spectrometer.

d) The gating circuit designed to gate clocking pulses to the array. In the previous system (5) it was found that fixed pattern background signal saturated the array. This gating circuit reduced this background considerably.

e) The signal connections to the edge connector of the RC1024S board were maintained as described in reference 5.

f) Reduction of the frequency of the onboard oscillator to facilitate signal acquisition and conversion by a microcomputer

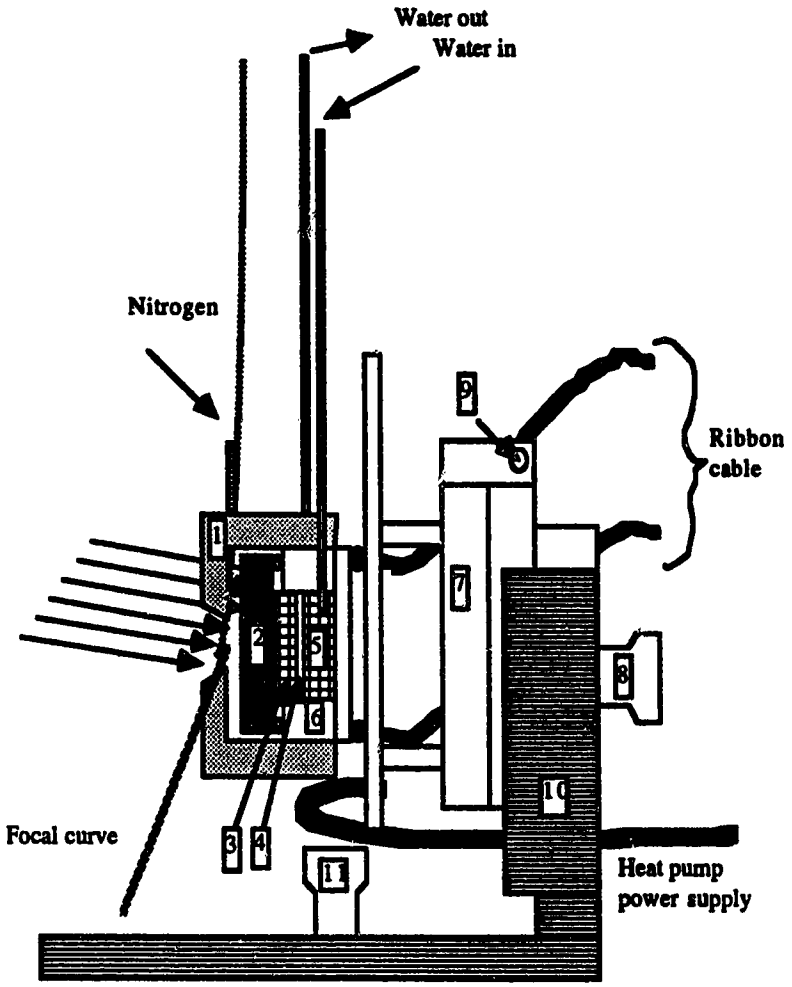
2.5 Photodiode Array Cooling

PDA's require cooling to reduce their integrated dark current. Four Peltier (17) heat pumps are used for this purpose. These are attached to the array and electrically connected in series (5). Each array cooling system draws 2 amps at 6V. Cooling water is used to remove 18.24 Watts or 4.4 calorie/sec of heat from the hot side of the Peltiers. To keep the array temperature fluctuations less than 1°C a water flowrate of at least 5 ml/s is required. To supply this flow to several arrays simultaneously, without creating high back pressure, the water is drawn in parallel from a manifold (5).

2.6 Photodiode Array Mount and Carriage

The photodiode array and cooling system is mounted on a carriage (Figure 6). This carriage clamps to the mounting rack which previously carried the exit slits for the PMT detection system.

Using this carriage and mounting rack the photodiode array has three degrees of freedom on the Rowland circle, all of which are essential for finding and optimizing the spectral signal.
The array can be moved vertically to allow it to be positioned for maximum spectral line intensity and horizontally towards and away from the grating to achieve focus. There is also a rotational adjustment about the axis normal to the Rowland circle. This latter adjustment, is used to align the photodiodes with the images of the entrance slit in the direct reader focal plane.
The array is kept tangential to the Rowland circle by two steel pins which are held in contact with the edge of the mounting rack.



1. Mask to control dry nitrogen
2. Photodiode array
3. Peltier cooled copper plate
4. Peltier cooler.
5. Water cooled copper plate
6. DIP socket
7. Array mount and stand-offs
8. Vertical adjusrment
9. Rotation adjustment
10. Original exit slit mounts
11. Horizontal Focussing adjustment

Figure 6 The photodiode array, its carriage and cooling system as configured in the direct reader

CHAPTER 3

HARDWARE DESIGN

3.1 Interfacing the Photodiode Array to the Single-Board Computer.

The system incorporates a Reticon 128 element photodiode array. The photodiode array was originally mounted on and driven by the RC1O24S driver board. The board was supplied with the array by Reticon (18).

This driver board had been modified (5) to allow the photodiode array to operate a short distance away from the RC1024S board. In this configration he photodiode array is connected to the driver board by a ribbon cable. This allowed the photodiode array to be placed in the focal plane of the spectrometer as is shown schematically in Figure 2.

The new data acquisition system (Figure 3) is based on an appropriate single-board (John Bell 64K) computer functioning as a "slave" intelligent peripheral to the Apple II+ "master" or "front-end" computer. The Apple II+ "front-end" computer functions as the user interface and system controller. The features of the single-board computer are listed in Table 1.

The single-board computer was interfaced to both a high speed successive approximation analogue-to-digital converter and to the Apple II+. This prototype system was used to determine the operating characteristics of a dual processor system (i.e., "front end" microcomputer user interface plus the single-board computer based data acquisition system) for data intensive applications such as, the sequential acquisition of multiple

photodiode array generated spectra and for the acquisition of the spectra of transient signals.

The construction of this prototype was the essential first step in the development of the multiple processor based PDA spectrometer. From the start it was endeavoured to put all PDA operating parameters and its control requirements under software control.

1. AIM 65 bus (Rockwell Corporation).
2. 6502 central processing unit.
3. Two user available 6522 PIAs.
4. 6850 ACIA and an RS232 serial interface.
5. 8K of erasable programmable read only memory.
6. 55K of random access memory.
7. 1K of user address space.

TABLE 1 Features of the John Bell Single-Board Computer.

The detection and data collection systems include the following components:

1. The photodiode array.
2. The photodiode array carriage and its ribbon cable.
3. The photodiode array driver board RC1024S.
4. The supplementary circuits to gate the oscillator, modify the data acquisition control pulses and to convert RS232 signals to RS232C levels.
5. The analogue filter and pre-amplifier.
6. The analogue-to-digital converter complete with track-and-hold amplifier.
7. The single-board, 64K computer.

The removal of the photodiode array from its driver board and the construction of the photodiode array carriage has been previously described (5). In the following sections, the additional interfaces and modifications required to make the dual processor system functional, are described.

3.1.1 Interfacing the Gating Circuit to the Single-Board Computer

In the previous photodiode array direct reader (5), it was found that due to the photodiode array being operated some distance away from the RC1024S driver board, an unusual interfering background signal appeared. The magnitude of this background signal was almost proportional to the number of oscillator periods which made up the integration time. After this conclusion was reached a gating circuit (Figure 7) was designed to stop these pulses reaching the array during the integration time. This gating circuit reduced the background problem significantly.

This gate consists of a dual edge triggered D type flip-flop and a quad NAND gate 7400. The D and S inputs of both flip-flops are held at a high logic level. In this mode, a rising edge at the clock input of either flip-flop causes the respective Q output of that flip-flop to go high. The Q output of the first flip-flop is the gate control. It goes high and opens the gate when the flip-flop is clocked by a rising edge of the start pulse input from the single-board computer. When readout has been completed the overflow pulse from the RC1024S board clocks the second flip-flop sending its Q output high and its complementary Q output low. This Q output clears the first flip-flop which closes the gate and then closes the second flip-flop.

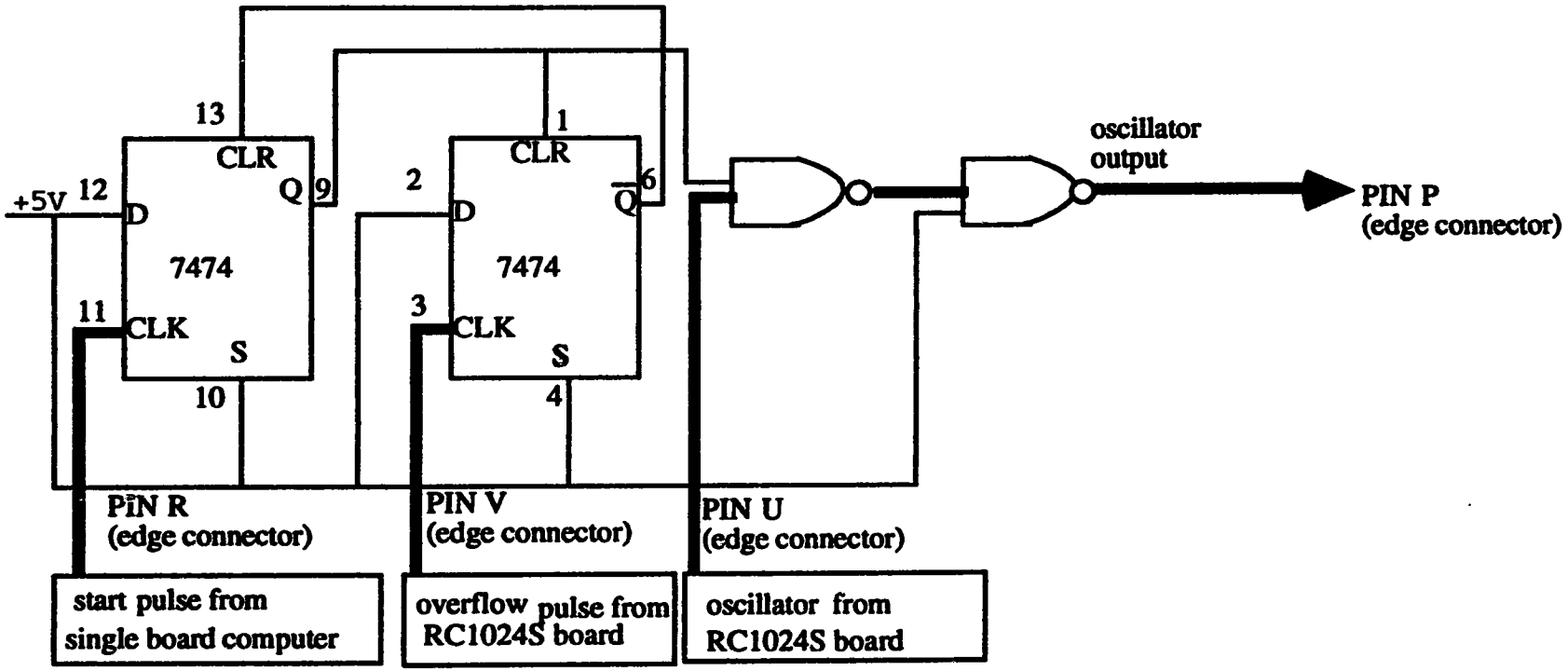


Figure 7 Gating circuit for the RC1024S onboard oscillator.

This gating circuit was integrated with the new data-acquisition system (Figure 8). It was built on a separate circuit board and piggy-backed onto the auxiliary circuit board. The auxiliary circuit board also housed the circuits for the analogue filters and preamplifier, the analogue-to-digital converter, the sample-and-hold amplifier and monostables for the treatment and generation of control signals required for the analogue-to-digital conversion.

This gating technique limits to some extent, the flexibility of the photodiode array acquisition system. This is due to its utilisation of the RC1024S onboard oscillator. This oscillator produces a fixed frequency, independent of the data acquisition and control computer. It was a goal of the present work that the oscillator for the system would be placed under the software control of the single-board computer. This it was hoped would facilitate variable frequency clocking and clock stopping (13) techniques with with the arrays.

A new oscillator gating technique was implemented which eliminated the use of the onboard oscillator and replaced its function with timer T1 of 6522 VIA#2 on the single-board computer. One software programmable mode of operation for the above timer is a free running mode, whereby the 1.22MHz oscillator on the single-board computer is utilized to produce a variety of programmable output frequencies.

The frequency of the new oscillator could be varied, under software control and using parameters transmitted to the single-board computer from the Apple II+ user interface. The software was designed to allow clocking of the array during readout. The oscillations were terminated when the computer sensed that the array had been read out (i.e., when data from 128 diodes has been

digitized). The hardware based oscillator gate for the RC1024S onboard oscillator (Figure 7) now became unneccessary.

Interfacing the new oscillator to the photodiode array system involved connecting the programmable oscillator output on PB7 of the 6522 VIA#2, to the clock input on the RC1024S array driver board. Timer 1 on this VIA generates a square wave, which is output on PB7 and used as the oscillator.

Regretably, although this computer generated oscillator functioned satisfactorily in the dual processor system, the software neccessary for this mode of operation was not adequately debugged when the multiple processor system was finally constructed. Therefore it was decided to delay the introduction of this method of array clocking for the entire system and to rely, temporarily at least, on the hardware gated oscillator, previously described.

Software subroutines which initiate the 6522 based oscillator, thereby providing a 10kHz square wave on PB7 are nevertheless included in the main EPROM program for all data acquisition units. To reactivate this clocking method, it is simply neccessary to call these subroutines from the main program, to reconnect PB7 to pin P of the RC1024S edge connector and to disconnect the gated oscillator which is output from the hardware gate These subroutines can start the oscillator just before data acquisition commences, and stop it after the array has been read out.

It is necessary to provide a start pulse for the photodiode array before readout commences. This serves both to connect the control section of the RC1024S board to the oscillator and to cut off the blank restorative signal (i.e., the signal that is sent out over the video lines when no photodiodes are being read out).

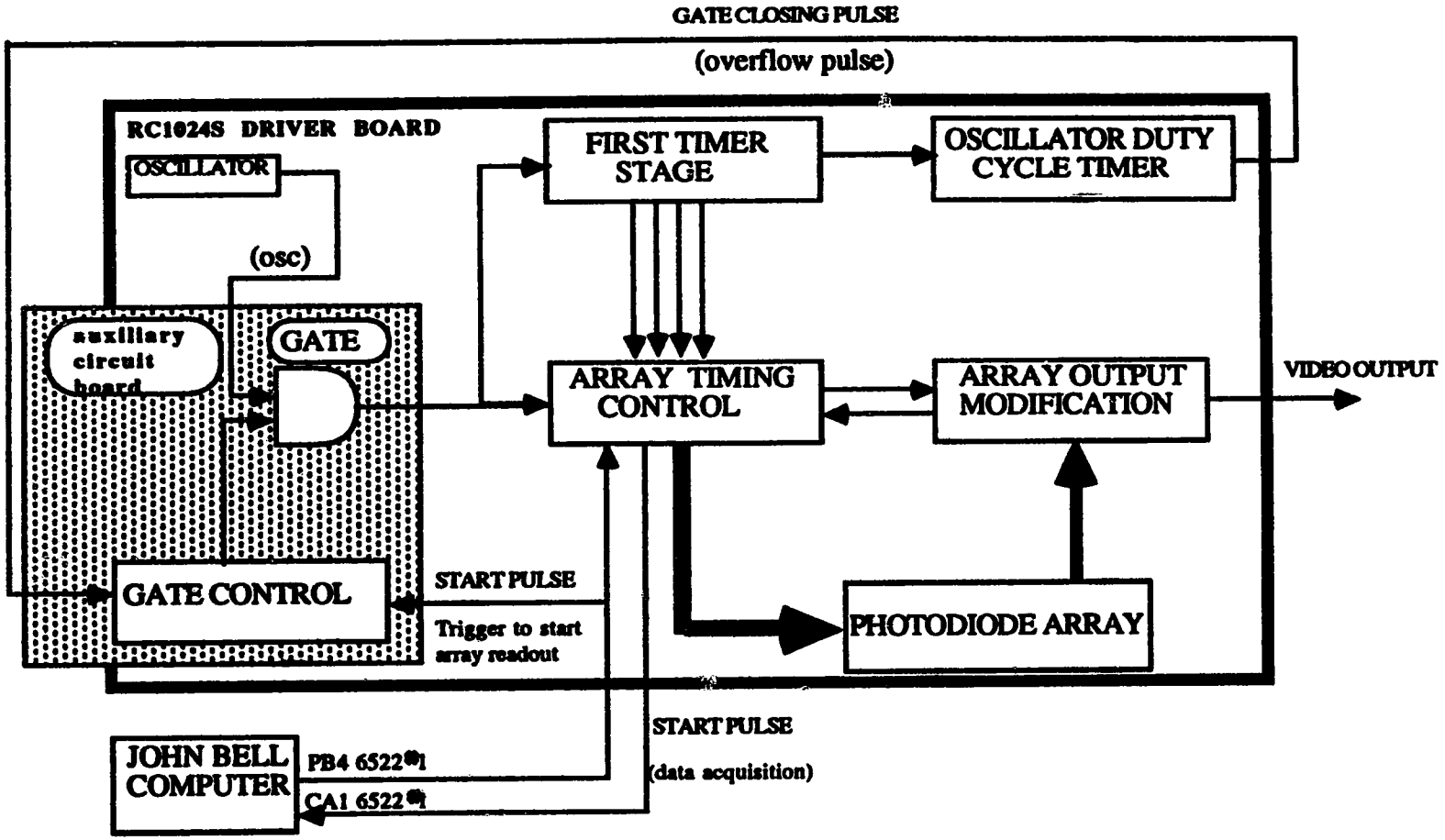


Figure 8 Interface of single board computer to the gating circuit.

After the integration time has elapsed this start pulse is generated through PB4 of 6522 #1. This pulse clocks the output of a 7474 flip flop high on the RC1024S board (Appendix 1). This pulse also connects the gated oscillator to the control system on the RC1024S board (Figure 7). The readout control system of the driver board then generates the sampling and control pulses from this clock. As soon as one of these timing pulses, called ø2 ODD goes low for the first time it clears the onboard 7474 flip-flop sending its output low. This high-to-low transition is used as the trigger for the computer to start data acquisition. On the array driver board this pulse is simultaneously, inverted and converted to MOS logic levels by the MH0026 and acts to trigger readout of the photodiode array. The complementary output of this onboard 7474 flip-flop goes high and clocks a second RC1024S 7474 flip-flop which cuts of the blank restorative signal.

Two sampling pulses are generated before readout of the photodiodes commence but these are ignored by the data acquisition system, since they occur prior to the trigger signal from the RC1024S board.

When the last photodiode is read out, the photodiode array sends out an end of line signal. This is transferred to a shift register on the RC1024S board where it remains until the next even sample pulse is generated. This sample pulse clocks the shift register, thereby clearing the 7474 flip-flop which controls the blank restorative level. This takes a further two sampling pulses implying that 132 sampling pulses must be generated in total to read out the 128 element photodiode array. The signal timing sequences for the start and at the end of readout, are given in Appendices 2 and 3 respectively.

3.1.2 Control Pulses for Data Acquisition.

Due to modifications previously made to the photodiode array driver board, the differential readout of active and dummy photodiodes does not function well. This differential readout attempts to minimize switching transients as photodiodes are coupled in turn onto the video output lines. Therefore it is necessary to delay the data acquisition pulse to allow the signal to be digitized and acquired when these switching spikes have passed. The pre-amplifier and the low - pass filter amplifier tend to dampen the sharp transitions in the analogue signal (e.g., switching spikes). Evans (5) gave an example for a photodiode array sampled at 50kHz or 20 μs per photodiode. Of this 20μs, the switching spike takes up about 7 μs. The present filter/amplifier circuit is similar in design to that described by Evans (5) and therefore exhibits similar features. Allowance for an adjustable delay to be applied to the signal sampling and conversion pulses of greater than 10 μs is designed into the present system.

Separate trains of sampling pulses are generated on the RC1024S circuit board for the odd and even photodiodes. These are logically OR'd together and appear on an edge connector tab (W) on the circuit board. The period of these pulses is dependent on the frequency of the oscillator. These are the pulses which are modified to eliminate switching transients by providing a delayed "hold" signal for the track-and-hold amplifier and a delayed convert pulse for the analogue-to-digital converter (ADC). The delays imposed on these pulses allow the system to perform analogue-to-digital conversions only when the video signal is stable.

The timing circuit (Figure 9) used to modify the sampling pulses and generate the required "hold" and "convert" signals for data conversion consists of three 74121 monostables.

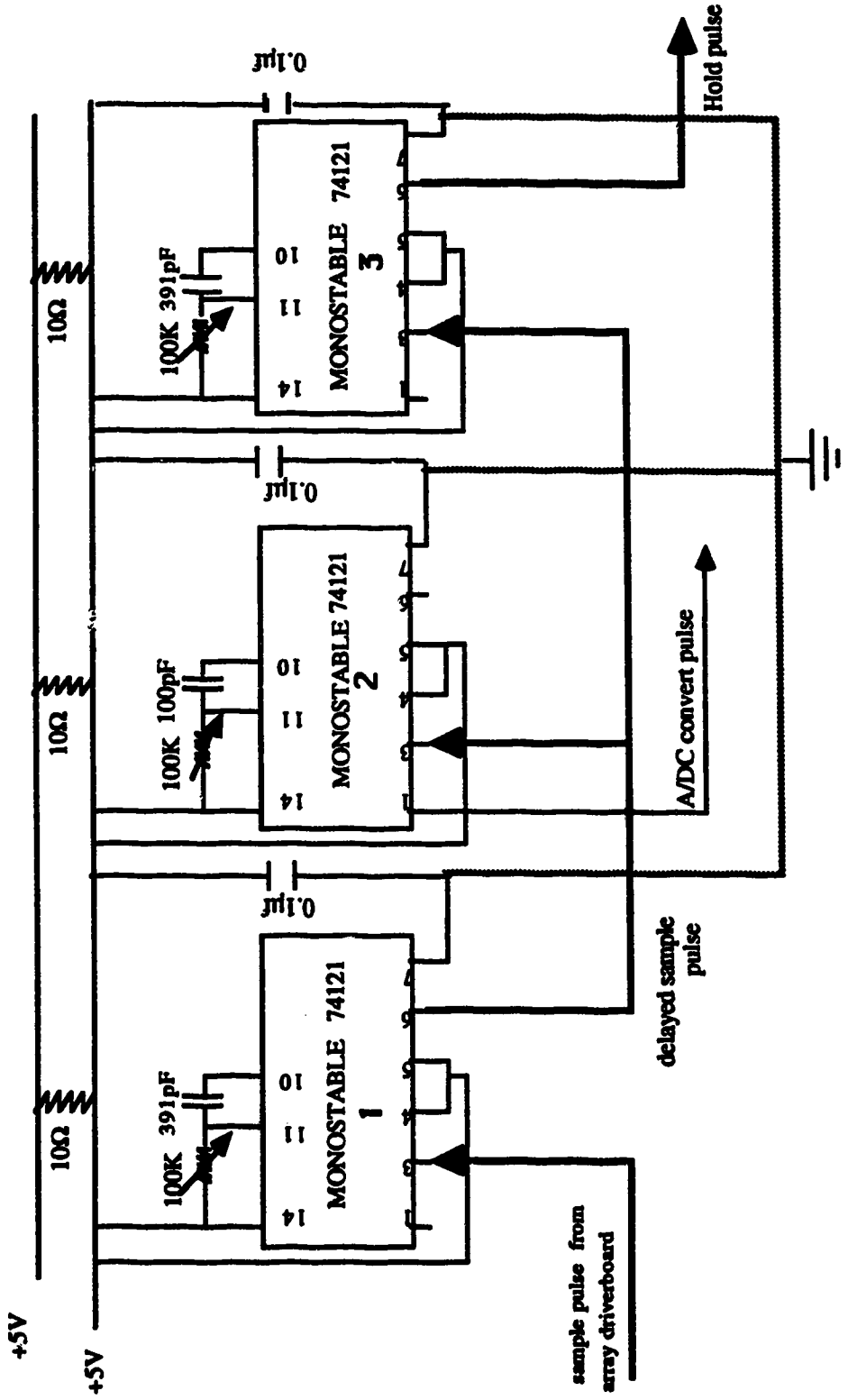


Figure 9 Control pulse modification circuit

On receipt of a negative transition on the sampling pulse originating from the RC1024S board, the output of the delay monostable (#1) goes high, it remains high for a duration determined by the 391 pF capacitor and the timing resistors. The variable resistance used here allows control over the delay time which can be adjusted and optimised.

From this delayed sampling pulse the two additional control signals are generated. These are produced using two additional 74121 monostables. 74121 #3 goes high on the negative transition of the delayed sampling pulse. It is similar to 74121 #1 in that its output pulse width is controlled by a 391pf capacitor and a variable resistance. This positive pulse is used to force the track and hold amplifier from tracking to hold. The width of the pulse is adjustable to greater than 15us using the variable resistance so that data conversion by the ADC (whose completion is indicated by the negative edge of its status line) is complete before the track and hold is returned to tracking by the falling edge of this pulse. Thus the track-and-hold amplifier ensures that during analogue-to-digital conversion, the analogue signal is held constant.

On switching from tracking to hold this amplifier experiences a small uncertainty of about 200 nanoseconds in the time aperture during which the switching occurs and it takes an additional 2μs approximately for the signal to settle. This switching spike must have passed and the signal must be constant before analogue-to-digital conversion commences. Also, triggered by the delayed pulse from monstable #1 is monostable #2 which provides a negative pulse. Its pulse width is varied to generate the delayed conversion trigger for the analogue-to-digital converter.

The complete timing sequence is shown schematically in Figure 10.

3.1.3 The Analogue Filter and Pre-amplifier.

The operational amplifiers used in this design are the LF351's from National Semiconductor Corporation, they are a high slew rate type. The first operational amplifier (Figure 11) acts as a second order low pass filter (40dB fall off per decade) with an adjustable 3dB point in the 5-50KHz range. The design was adapted from the manufacturer's handbook (6). It also acts as a summing amplifier, allowing incoming signals to be offset by ±1 V.

The offset controller is a screw adjustable potentiometer mounted on the auxiliary circuit board. This offset controller allowed the required offset voltages to be adjusted and applied conveniently. The purpose of this filter was to exclude noise from exterior sources, such as from the radio-frequency power supply for the inductively coupled plasma.

The second operational amplifier used in this circuit reinverted the signal which is inverted by the first amplifier. It then amplifies it thereby allowing the photodiode array signals to match the full input range (0-10 V) of the analogue-to-digital converter.

3.1.4 The Track-and-Hold amplifier and Analogue-to-Digital Convertor System.

The track-and-hold amplifier and analogue-to-digital convertor are inter-connected (Figure 12) and put under the control of the timing signals generated by the circuit of Figure 9.

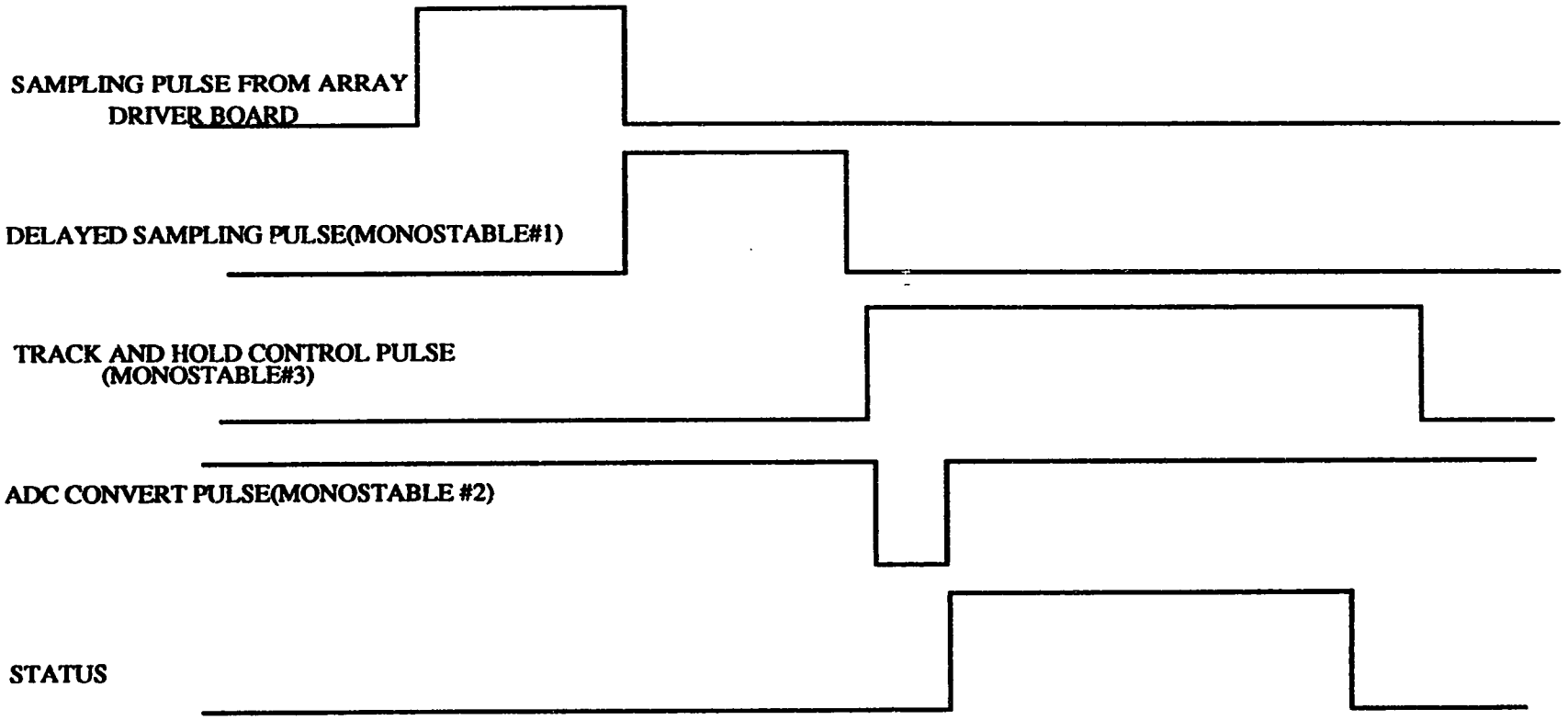


Figure 10 Timing sequence for photodiode array readout

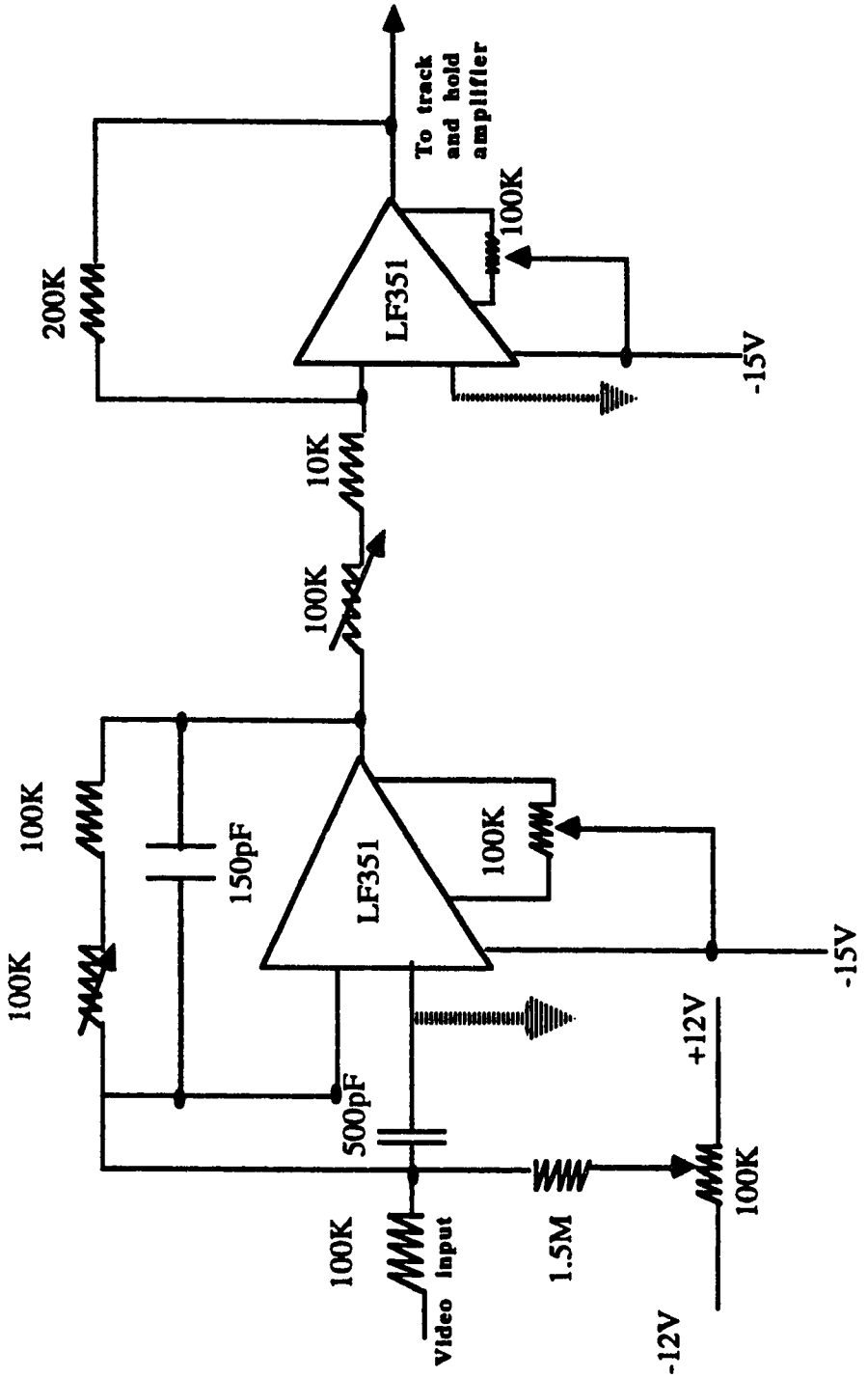


Figure 11 Analogue filter and pre-amplifier circuit

The AD574 is a complete 12 bit, successive approximation analogue-to-digital convertor with reference and clock. This component was connected as outlined in the Analog Devices literature (7). It is capable of doing a complete 12 bit conversion in 12 μs.

During the conversion, the analogue signal was held constant by a the AD582 track-and-hold amplifier (also from Analog Devices). The hold pulse developed by the pulse modification circuit (Figure 9) causes the track-and-hold amplifier to change from signal tracking to hold. It requires about 200 ns to switch the amplifier and another 2.0 microseconds (μs) for the decay of the switching transient. The negative transition of the convert pulse whose width is about 2 μs in duration is generated simultaneously with the "hold" pulse. The switching transients from the "hold" signal is allowed to settle before conversion is initiated by a positive edge of this "convert" pulse.

At the end of the conversion, i.e., when all the required bits are set, the hold signal returns to its low state thereby returning the track-and-hold amplifier to tracking.

The amplified video signal(0-1 V signal at the output from the driver board was amplified to the 0-10 V required for the ADC input range) from the photodiode array was connected between pins 13 and 9 for a 0 to +10V input range of the AD574. The convert pulse, developed from the sample pulses generated on the photodiode array driver board (Figure 10) is fed to the 'convert' control input of the ADC. When the edge of this negative pulse goes high, analogue-to-digital conversion commences, simultaneously the status (STS) output line of the ADC is forced high and remains so, until the conversion is complete. When conversion is complete the status output of the ADC goes low. It is this negative transition which the single-board computer is polls

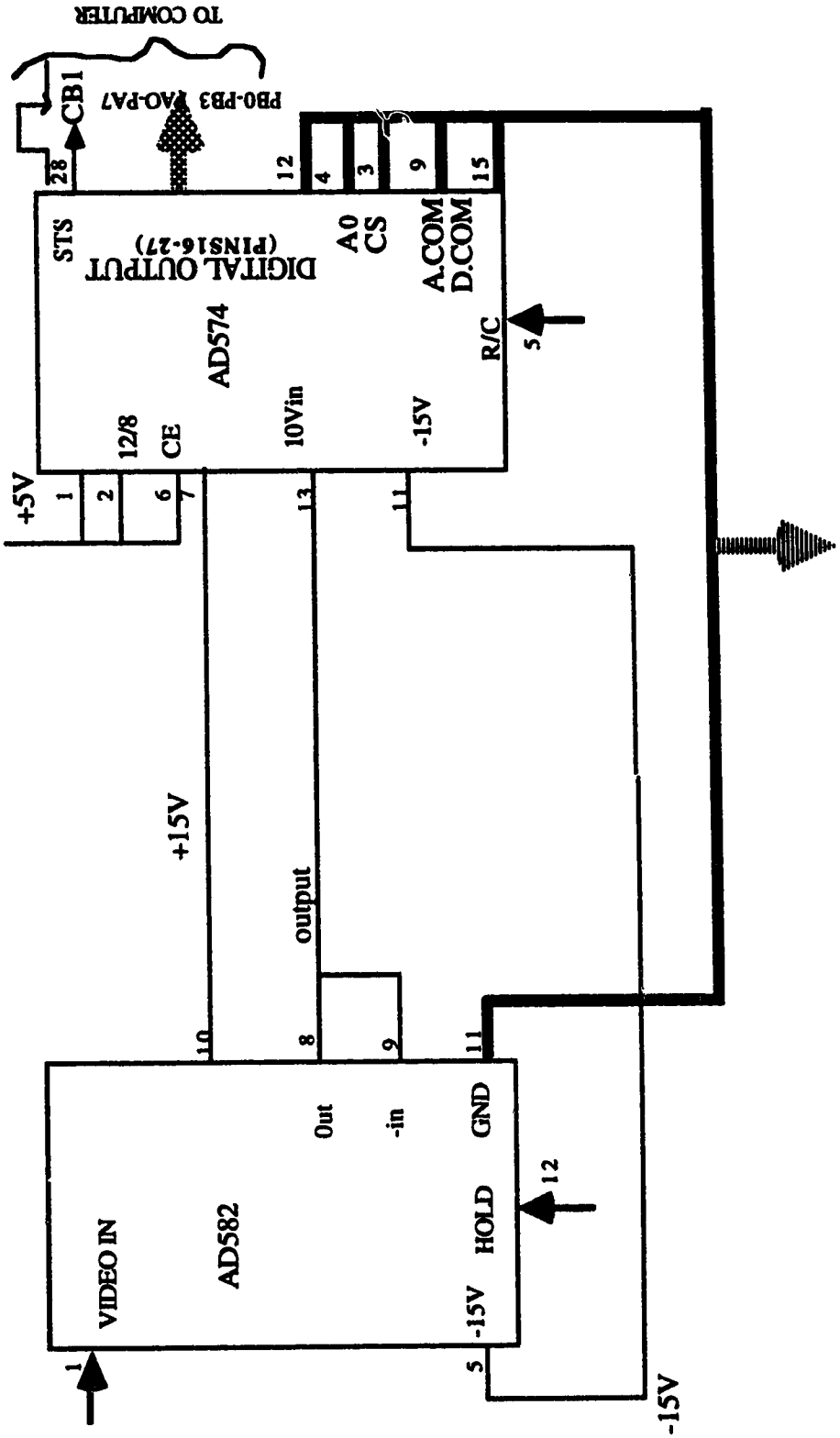


Figure 12 The track-and-hold amplifier and analogue-to-digital converter interface

for as a trigger to acquire into its memory, the digital representation of the photodiode signal, now latched on the digital output lines of the ADC.

Both the AD574 and the AD582 are mounted on an auxiliary circuit board (Figure 13) together with the amplifiers and other additional circuitry required.

3.2 The Apple II+/Single-Board Computer Serial Interface (Dual-processor System)

The asynchronous serial interface between the single-board computer and the Apple II+ (used as the "front-end" processor) is critical to the success of the entire system. It is operated in a standard RS232C mode having both switch and software selectable baud rates.

Software and data transmitted from the Apple II+ disk storage can control the baud rate for the single-board computer from between 110 to 9600 baud. In effect, the Apple II+ disk storage is used by both computers. The RS232C interface connecting them makes this possible.

The EIA-RS232C is a serial data transmission standard for relatively low data transmission rates. The full RS232C standard specifies a 25 pin connector between communications equipment but only the receive, transmit and ground lines are absolutely necessary. All other lines can be made redundant for many applications. This greatly reduces the wiring necessary for functional serial interfaces between systems.

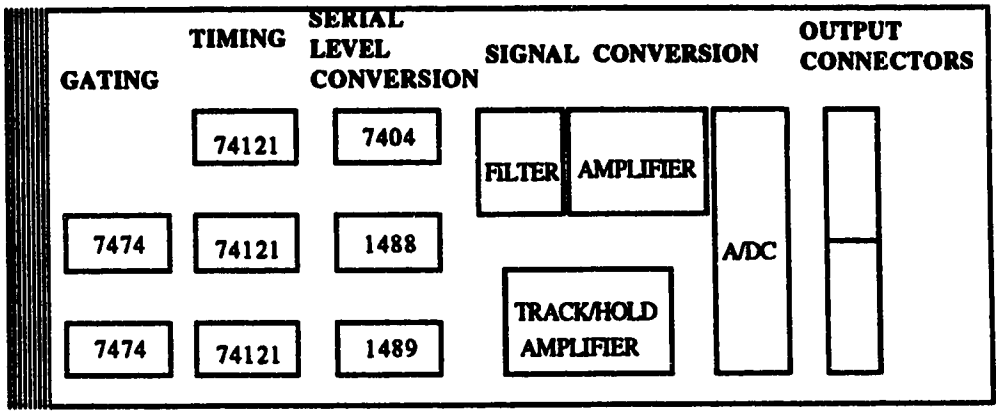


Figure 13 Layout of the auxiliary circuit board

Details of the serial interface between the single-board computer and the Apple II+ are given in Figure 14. The single-board computer has as a resident chip, the 6850 ACIA (Asynshronous Communication Interface Adaptor) which performs parallel to serial conversions and vice versa. It also handles most of the other control functions required of the RS232 interface.

The Super Serial card (Apple Computer Incorporated) for the Apple II+ has a 6551ACIA which implements the RS232C standard for this microcomputer.

Both the 6850 and the 6551 are clocked internally by their respective computer systems. This simplifies greatly the interfacing problem. While the Super Serial card adheres to the ±12V transmission voltages of this standard, the single-board computer itself does not have its digital signals converted to these levels. The MC1488 and 1489 chips (Figure 14) were used to make these voltage levels compatable for data communications between both computers.

In addition to performing voltage level conversion, these chips invert the signals. Reinversion of signals is achieved by incorporating a 7404 inverter into the circuit.

The ACIAs used for this application serves as a good example of how specific hardware can be used successfully to reduce the software overhead in implementing RS232 interfaces. The ACIA handles the primary function of converting a parallel byte of data into a serial byte and visa versa while automatically providing stop, start, and parity bits.

In this system control of parity, the number of stop and start bits and the baud rates is achieved by either programming

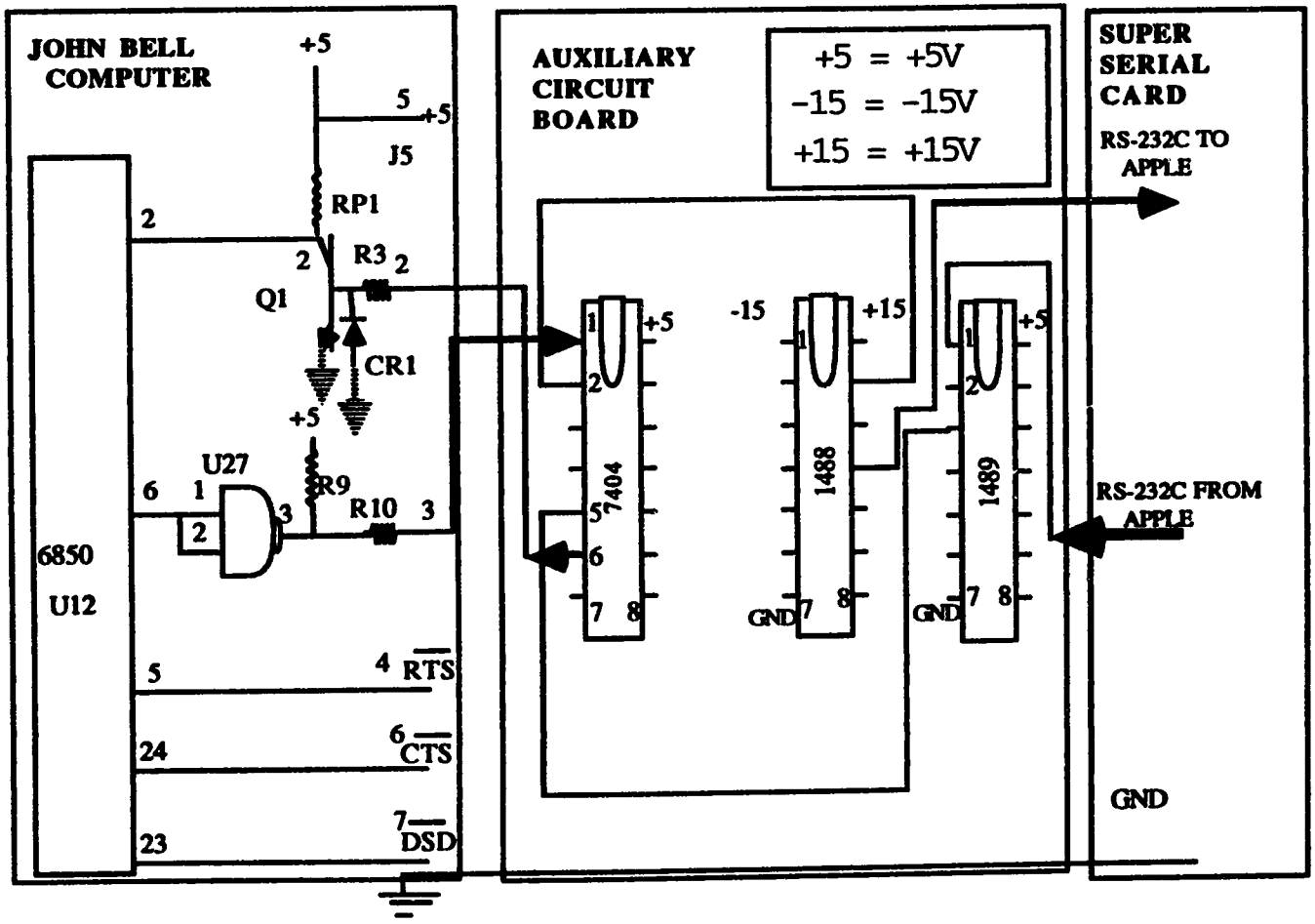


Figure 14 Serial interface between the "front-end" processor and the John Bell single-board computer

the correct registers of the ACIA or via hardware, by the setting of switches mounted on the respective computer or peripheral.

Except for baud rate control, all other serial interface control parameters, for the single-board computer are under software control. Eventually, it was found that operation of this interface under complete software control was the most convenient mode of operation. Therefore the original single-board monitor program was modified to allow software control of its RS232 baud rates, therby making different rates selectable for many applications via the Apple II+ user interface.

3.3 Power Supplies and System Bus.

The system was designed to eliminate some of the more serious problems associated with the previous multiple photodiode array system. One of these problems was that the ADC and the analogue pre-processing circuitry were driven by separate power supplies and were therefore prone to serious noise problems, especially those associated with ground potential differences. In this design, the total system is run from a single power supply.

The complete data acquisition system is placed in a card cage which is constructed from Critchley racking. The system is comprised of three main circuit board units interconnected by a bus (Figure 15). These three circuit board units are:

- The single-board computer.
- The photodiode array driver circuit board RC1024S.
- The auxiliary circuit board.

The system bus consists of edge connectors mounted on each circuit board, inter-connecting the single-board computer with the

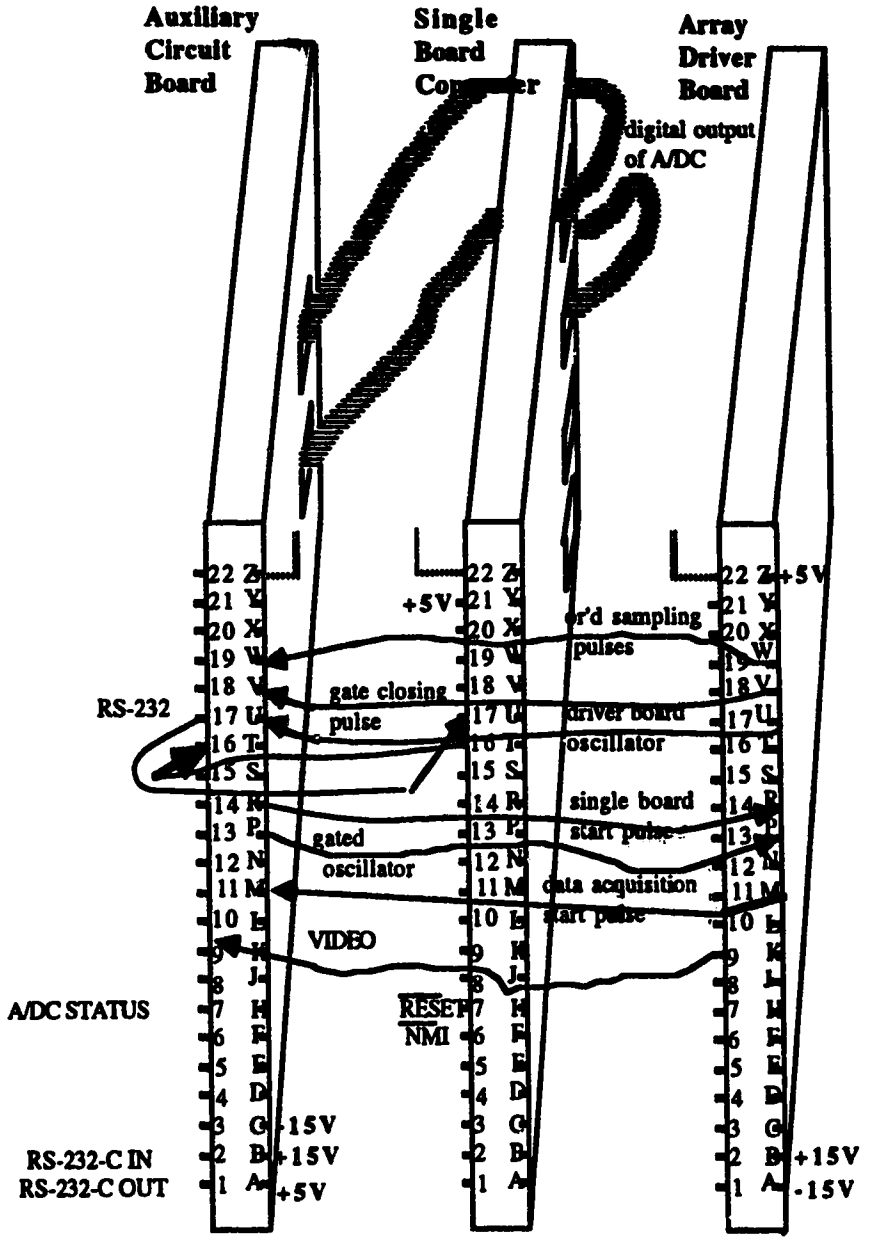


Figure 15 Inter-connecting bus for individual modules of the single-board computer based data acquisition system.

other boards of the system. The auxiliary circuit board (Figure 13), is a general purpose Vector plugboard (3677) with a standard 22/44 pin male connector. This board is designed to accommodate all the additional circuitry, not available on the computer and driver board. The video signal from the array driver board and the signals to and from the oscillator gating circuit on the auxiliary circuit board are transferred over this bus. Additionally, the bus provides for the convenient transfer of start, sampling and RS232 signals between the system modules.

A ribbon cable transfers the digital output from the A/DC to the I/O lines of the single-board computer. Start and trigger pulses, between the data conversion circuits and the single-board computer are also channeled through this cable.

It was essential that the system should be designed around a bus such as this, in order to achieve, simultaneously, compactness and the many localized control and data acquisition functions desired.

Utilization of I/O ports on the John Bell single-board computer is shown schematically in Figure 16. The I/O lines of one 6522VIA are almost completely dedicated to the data acquisition function. The remaining 6522VIA was partially utilized by the original manufacturers monitor program as a means of adjusting the baud rate externally using jumpers. This section of the monitor program was eventually modified and the use of these I/O lines for this purpose was no longer necessary (see Chapter 4 for details of modifications to the monitor program). At a later stage one of these single-board computers utilized these additional I/O lines to provide the necessary control for a network of single-board computer based data acquisition systems (see section 3.5).

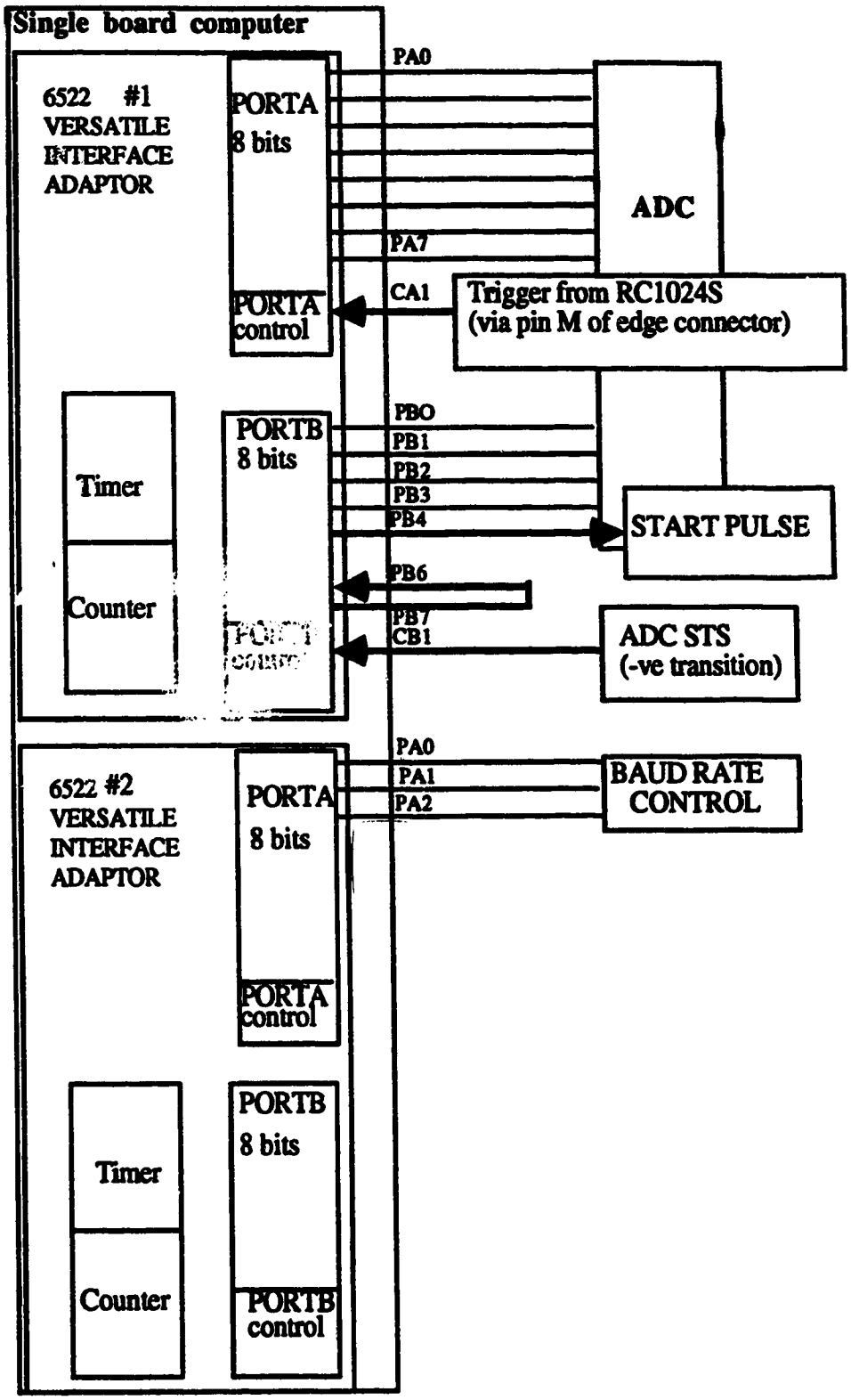


Figure 16 Utilisation of I/O ports on the John Bell single-board computer

3.4 Hardware Features on the Apple II+ "Front-end"

The Apple II+ used in this system served four key functions:

- •Software development
- •User Interface
- •Preliminary data processing
- •Graphical display.

The Apple II+ uses the same microprocessor (6502) as the single-board computer. It is a flexible microcomputer designed to accommodate easy interfacing of peripheral devices. While this microcomputer provides limited built in I/O which is available to the user, it does provide a backplane of slots for easy attachment of such peripherals (Figure 17). The main circuit board has one I/O connector originally designed for attachment of game equipment. This can be used for input and output of steady state logic levels and can act as an interval timer under software control.

3.4.1 16K Memory Expansion Board.

This expands the Apple II+ memory to its maximum of 64K. When loaded with Integer BASIC, it has as part of that language set, a version of assembler language that is useful for writing assembly language programs. This assembler was not utilized during the development of this present system. It was more convenient to hand assemble the short routines required in the development of the operating system for the single-board computers.

3.4.2 The Printer Interface Board.

This is the Grappler+ by Orange Micro and it is interfaced to an Epson MX80FT dot matrix printer. This combination can print

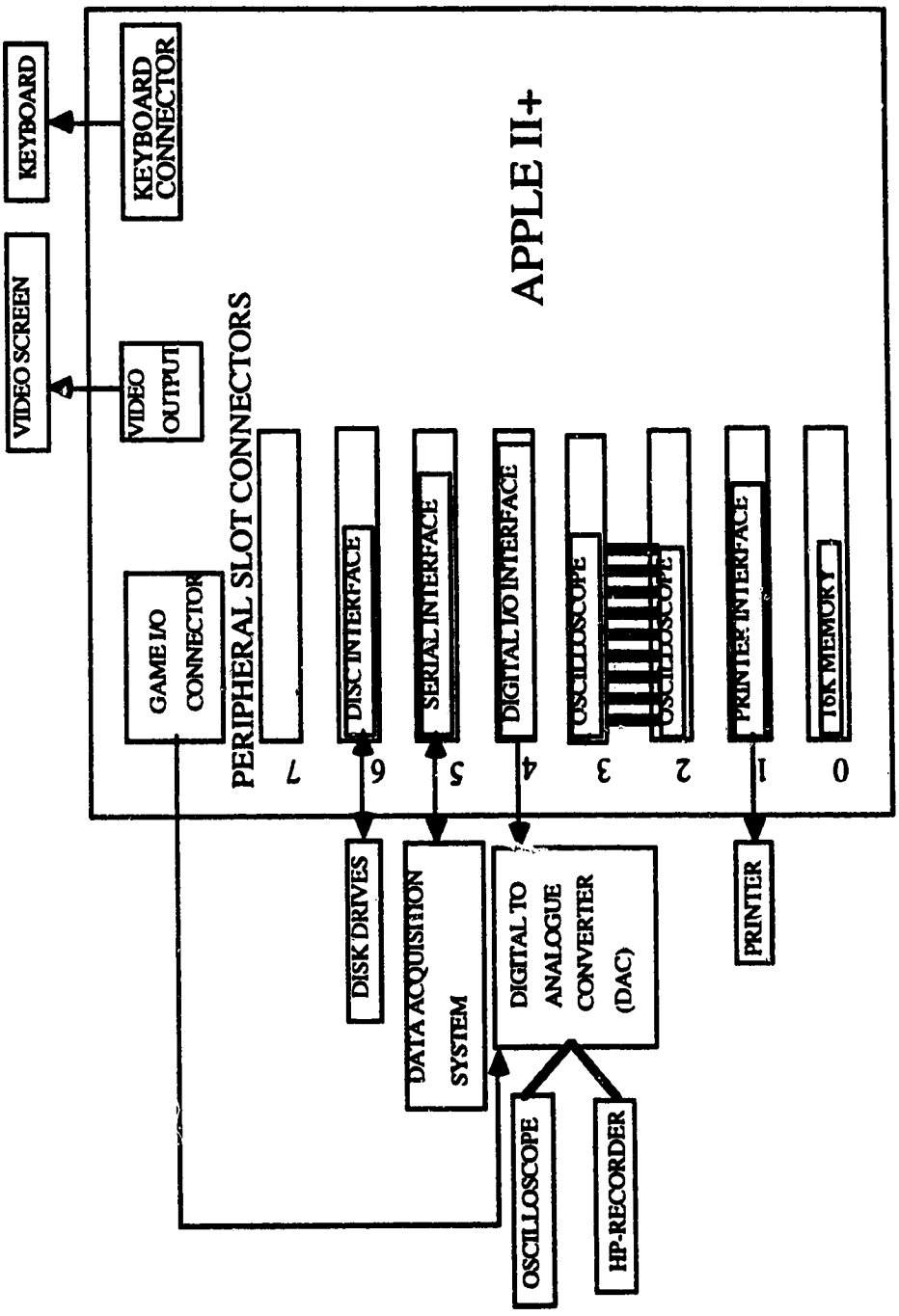


Figure 17 Utilisation of the Apple II+ backplane

out data of up to 80 characters wide and can also produce a printed copy of any high resolution graphics display on the video monitor.

3.4.3 The Input/Output Board.

This is the D109 system from Interactive Structures. It contains two 6522 Versatile Interface Adaptors (VIA), therefore it has four 8 bit parallel I/O ports and 8 control lines. This is interfaced to a digital to analogue converter (5) which allows any data in the system to be displayed on an oscilloscope or graphed by a chart recorder.

3.4.4 The Disk Operating System Controller.

This controls two disc drives that use 51/4 inch diameter floppy discs. Drive No.1 is usually loaded with the "front-end" operating system which generates the user interface. Drive No.2 is used for data storage.

3.4.5 The Serial Cards.

Two Super Serial (Apple Computer Corporation) cards having 6551 ACIAs are used in the system. One controls the RS232C serial interface between the single-board data acquisition and control computers while the other is used to transmit acquired data files to other computers, especially to the Apple Macintosh.

3.4.6 The Digital Oscilloscope.

This is the A-Scope from Northwest Instruments and is used in much the same way as an ordinary oscilloscope for viewing the raw video output from the photodiode array. It was used mainly

during development of the signal conditioning electronics for the system.

3.5 The Networked Multiple Processor Photodiode Array System.

The design and construction of a single-board computer based data acquisition system for a photodiode array has been described above. This computer functions as a "slave " peripheral to a "host" or "front-end" microcomputer For the construction of the multiple processor photodiode array direct reading spectrometer, a total of five of these "intelligent" slaves were constructed as duplicates of the initial prototype.

The following sections contain a description of a network designed to allow all these units to communicate with the "front-end" and to perform spectral acquisition both simultaneously and sequentially at high speeds.

3.5.1 The Computer Network

A network was designed which facilitated control of "front end" communication with a number of these single-board computers which are functioning as independent data acquisition systems. At the data acquisition and control level, it was determined that for communication via the RS232C ports one of the single-board computers was designated as the communications controller for the entire system. It would control access to the communication lines linking the "front-end" and the other single-board processors in the network.

Appropriate control lines were available on the present John Bell single-board computer with which to build this controller. One obvious advantage of this control scheme is that the software

overhead is simplified by the utilization of the extensive user available I/O on this computer.

A "party line" concept involving the "user interface" and all the single-board computers daisy chained simultaneously, to the same communications lines was an alternative concept for network communications. This method was not pursued for a number of reasons. One of these reasons is that it would be difficult develop the necessary software for the single-board computer in order to implement such a network with only limited machine language programming facilities available. A more significant reason is that a closely packed network which incorporates the standard RS232C communications protocol, in addition to supplementary control lines facilitating sychronous operation of the attached processors, would be much more flexible for this aplication.

A "network controller" determines which data acquisition unit on the network the user wishes to communicate with and then automatically make the connection. This involves connecting the serial input and output lines on the appropriate single-board computer to those of the "front-end" processor. Additionally, this controller coordinates the tasks of parameter setting, data collection and data transmission by all processors on the network (See Figure 3)

3.5.2 RS232C Serial Communication.

Manufacturers of computers and data handling equipment are usually careful to directly incorporate an RS232C (EIA specification) serial interface into their designs. This facilitates ease of communication with a variety of devices supporting this standard. Those manufacturers who do not do so, invariably allow

for an expansion of their system, to support such an interface via third party peripherals.

Most laboratory instrument manufacturers are supplying full RS232C interfaces or at least, partial implementation of this standard on their equipment. There has understandably been a lot of interest in the literature concerning serial interfacing of computers to laboratory instrumentation.

Kueml and Griffins (20) reported a microcomputer controlled serial interface between a high performance liquid chromatograph and a diffuse reflectance infra-red fourier transform spectrometer. Ewen and Adams (21) discussed microcomputer interfacing and asynchronous serial communications interfaces to laboratory equipment. Karanassios (22) overviewed the development of the RS-232C and other bus structures for laboratory applications. McClard (23) described a convenient interface between the Apple II+ computer and the Perkin Elmer Lamba Spectrophotometer. Gampp et al (24) described a microprocessor controlled system utilizing serial interfaces for the automatic acquisition of potentiometric data. Finally, Blank and Wakefield (25) reported the role of serial interfacing in their description of a double beam photoacoustic spectrometer for use in the ultraviolet, visible and near-infrared spectral regions.

Interest in the whole area of serial communications was sufficient to warrant the publication of books specifically dealing with its use and implementation (26).

3.5.3 RS232C Standard.

The original use of the RS232 standard is reflected in the implementation shown schematically in Figure 18.

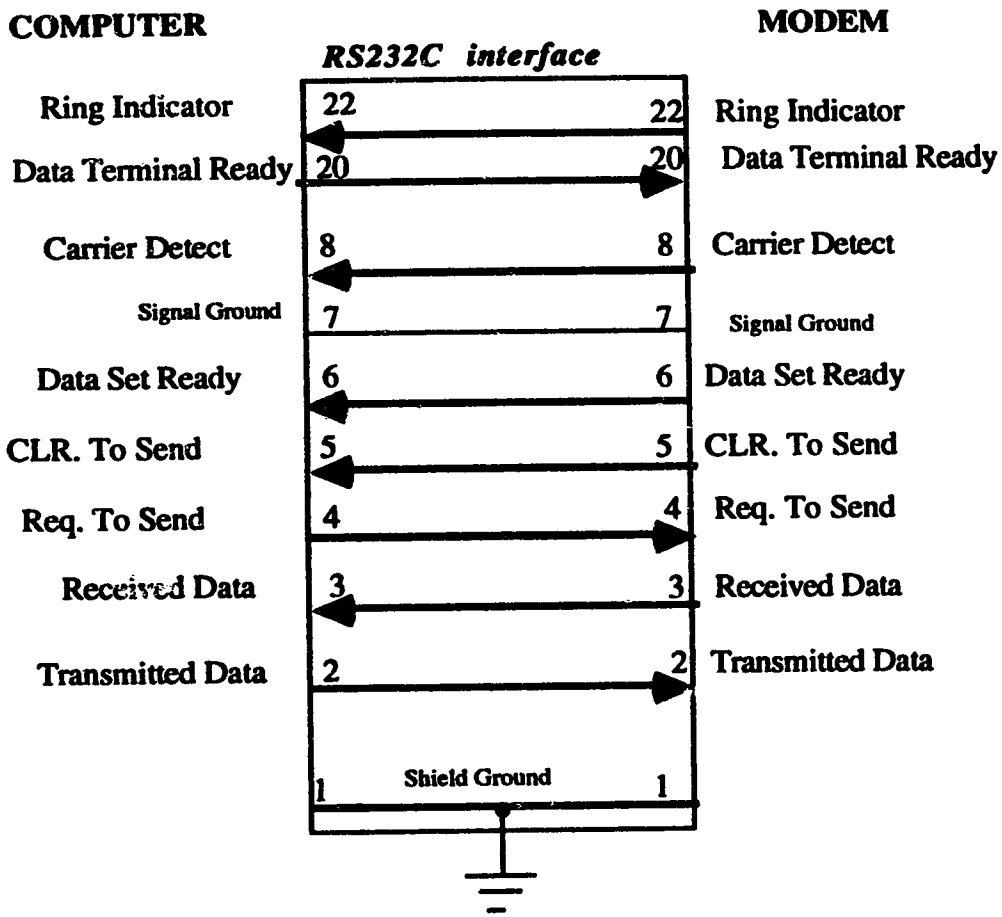


Figure 18 RS232C interface with communication equipment

On the left of the figure is an interface to a computer or terminal connecting to a modem interface on the right of the figure. The RS232C standard was originally developed to foster data communications on public telephone networks as this figure illustrates. At the other end of a communications line, another modem translates the frequency modulated information back to a sequence of high and low voltages which the receiving computer can recognize.

The following is a summary of the characteristics of the interface to which the RS-232 standard:

- *Electrical signal characteristics*

This defines the electrical characteristics of the interchange signals and associated circuitry.

- *Mechanical interface characteristics*

This defines a 25 pin connector between the two inter-connected devices.

- *Functional descriptions of interface circuits*

Here the specific description of the data timing and control circuits for use at this interface is given.

The RS232C standard therefore originally provided a specification for connecting remote devices together using the telephone network as an immediate medium, with interfacing accomplished by the modems. The original standard specifies a 25 pin connector and 21 signals between the computer and the peripheral device, but very rarely do manufacturers of microcomputers adhere rigidly to the standard.

In the mid-60's, during the early phases of the development of time-shared computers, remote access over serial links was done almost exclusively through telephone connections to terminal and computer equipment. In the 1980's with the

proliferation of microcomputers, terminals are usually connected directly to computers through RS232C ports, and do not use the telephone networks or modems except for truly remote connections.

Returning to Figure 18, the two signal grounds defined by the RS232C standard are conspicuous. One ground is a chassis ground and is tied directly to the shields in the systems. This ground connection should be made between two devices only if it is safe to connect the chassis grounds together. The other ground is a signal ground that provides a common reference point for all other signals. This latter connection is mandatory. Since the signal grounds are not necessarily isolated from the chassis ground, RS232C interfaces have an inherent ground loop problem. While the standard is successful over short distances, over longer distances it becomes unreliable and hazardous. The published standard recommends that each device should have a cable length not in excess of 50 feet. For longer cables, the standard strongly recommends that other means of interconnection be used.

The terminal or computer to modem interface has a pair of wires dedicated to the transmit and receive functions. These are compatible signals because transmit is a modem input and a computer/terminal output, the converse applies to receive. RTS (REQUEST TO SEND) and CTS (Clear TO SEND) relate to the characteristics of half duplex telephone lines. Such lines are capable of bi-directional traffic but they can transmit in only one direction at a time. The terminal signals a modem with an RTS when it has a character to transmit, but the character has to be queued, until the modem changes from the receive to the transmit mode; when transmission is possible the CLR TO SEND is returned to the terminal and transmission can begin.

Two Ready signals are included in the RS232C standard DATA SET READY (DSR), signifies that the modem is operational and DATA TERMINAL READY (DTR) is the corresponding signal for computers and terminals. The remaining two signals (CARRIER DETECT and RING INDICATOR) in this figure relate to telephone functions.

The standard incorporates other signals not shown in this figure but these predominantly relate to testing. For connections between computers and terminals that do not use a telephone network, the signals shown in Figure 18 are sufficient for nearly all functions of this interface.

3.5.4 Connecting Computers Directly Using RS232C.

Figure 18 shows how a computer or terminal can be wired to a modem. This method of course is not feasible when it comes to connecting two computers together. The connections in this figure show both the computer and terminal transmitting and receiving on the same pin. There are several ways of avoiding this, one of which is to have a terminal having the same interface as a modem but then these terminals would be incompatible with other modems or telephone networks.

The most common solution is to rearrange the signal paths in the interconnecting wires as is shown schematically in Figure 19. Here the transmitted and received data lines are crossed so the devices can transmit and receive properly. REQUEST TO SEND and CLR. TO SEND no longer serve useful modem like functions. Hence, REQUEST TO SEND is folded back as CLEAR TO SEND, and a transmission request is thereby always granted. The DATA SET READY and DATA TERMINAL READY are crossed in the cable so that each end of the link can detect the presence of a ready condition on the other end. Narrow lines in Figure 19 signify

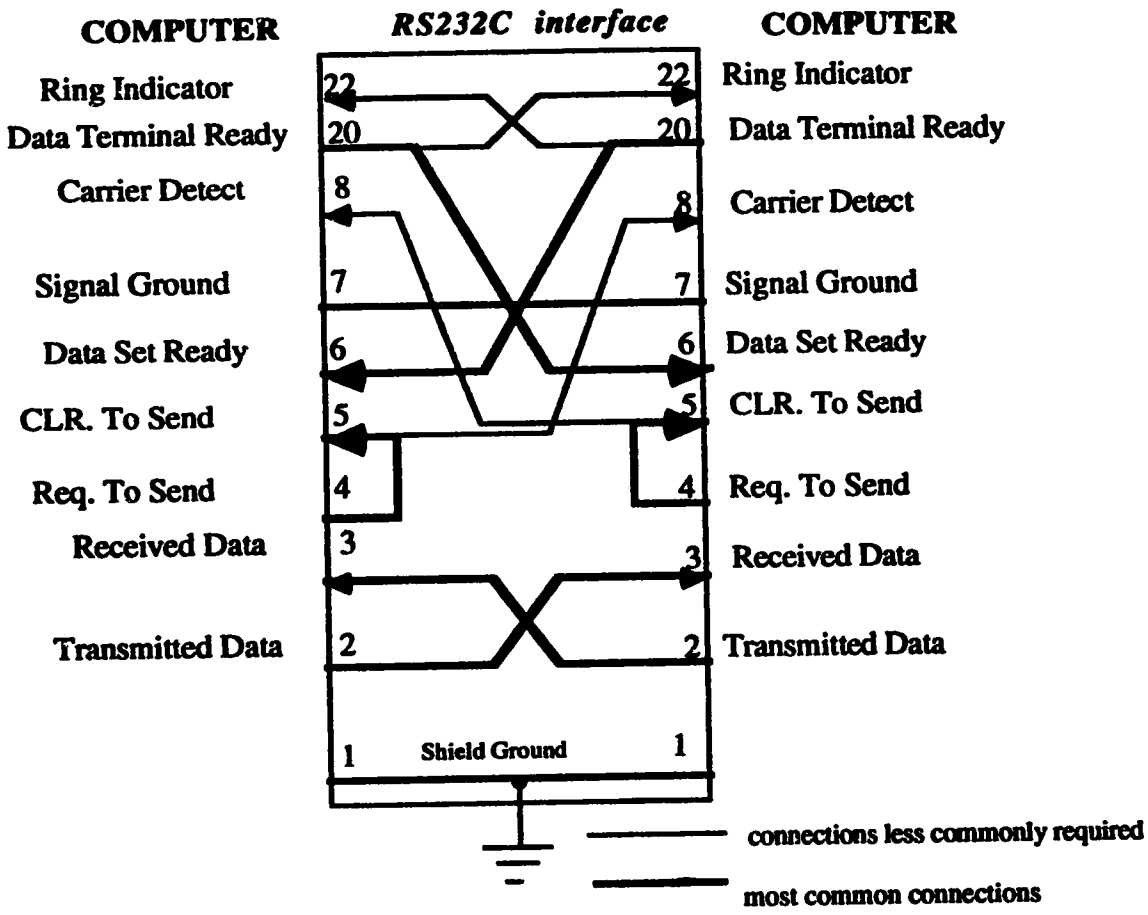


Figure 19 Configuration of RS232C lines to allow two computers to communicate directly without a modem.

connections which are sometimes made but are less common in practice, than the connections represented by solid lines that cross-couple or feedback pairs of signals.

The electrical conventions for RS232C circuits are shown in Figure 20. Voltages are symmetric with respect to ground and are at least 3 V for a logic 0 (Mark) and -3V for a logic 1 (Space). Usually, the voltage levels are powered by ± 12V or ± 15 V supplies so that, the voltage swing between 1 and 0 may be 20 volts or more. Inexpensive translator circuits are available for changing the voltage levels.

The MC1488 transmitter chip accepts TTL input levels and produces RS232C output levels. The actual output voltage is a function of the supply voltages on the 1488 and these are usually ± 15V or ± 12V.

The MC1489 receiver converts RS232C levels to TTL voltages. It uses the standard 5V supply for signal receiving and this is all that is necessary, although an additional small voltage supply can be connected to the receiver to alter the switching threshold. Even though the switching threshold with a 5.0 V supply is above 0.0 Volts and not symmetric with respect to signaling voltages, it is still well within the specification for RS232C voltages. The receiver has about 1V of noise protection, through hysteresis.

The large voltage swing on RS232C signals is required to ensure noise immunity on the communications link. With a common signal ground between transmitter and receiver there is no opportunity for double ended signaling and therefore common mode noise is inherently coupled into the signaling system.

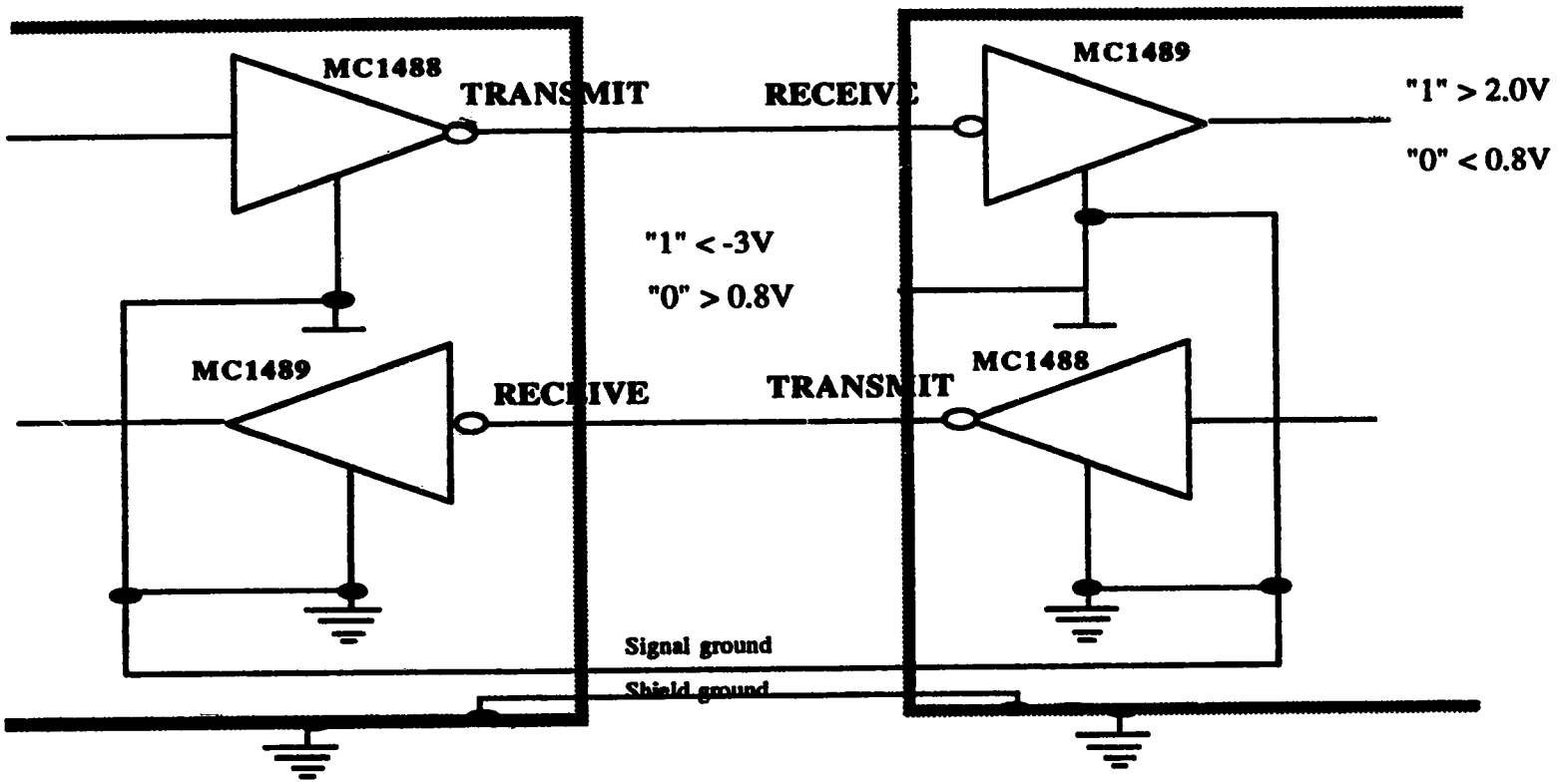


Figure 20 Electrical conventions for RS232C interfaces

TTL voltage levels are too sensitive to noise unless the common mode noise can be eliminated. TTL has approximately 1.2 V range between logic 0 (0.8 V) and logic 1 (2.0 V or greater), so noise voltages of the order of 0.5 V can cause severe problems. Common mode noise can easily climb to a few volts in the presence of radio-frequency sources, electric motors or even typewriters.

The common signal ground is largely responsible for forcing the higher transmission voltages found in the RS232C standard. Even for these voltages, use of the standard only covers transmission rates of up to 20 kHz and useful distances of about 40 meters (the maximum distance at which the signal grounds can be connected safely).

3.6. Networking Single-Board Computers Using a Multiplexer/Demultiplexer Interface Circuit.

The serial output line from the "front-end" processor is demultiplexed using a 74155 decoder/demultiplexer (Figure 21) and connected by the controller to the desired serial input of any "auxiliary" or "slave" processor on the network. The demultiplexer configuration of this chip is as described in the National Semiconductor data book (Logic Data Book, National Semiconductor Corporation). The circuit features dual-in-line 1 to 4 line demultiplexers with individual strobes and common binary address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route input data to the appropriate output. The individual strobes permit activation or inhibition of each of the 4-bit sections as desired. An inverter following the C1 control input permits its use as a 1 to 8 line demultiplexer, without external gating. Input clamping diodes are provided on these circuits to minimize transmission-line effects and to simplify system design.

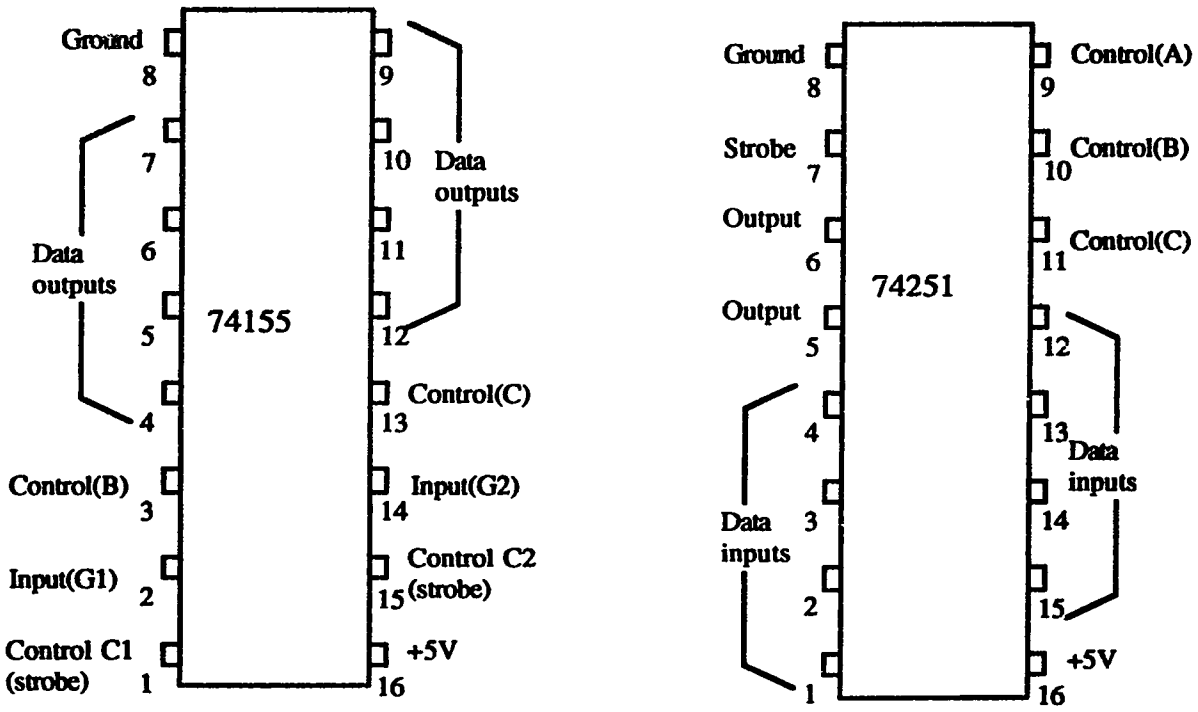


Figure 21 The 74251 multiplexer and the 74155 demultiplexer

In the 1 to 8 line demultiplexer configuration control inputs C1 (pin1) and C2 (Pin 15) are connected together as are the data input pins G1 (Pin 2) and G2 (Pin 14). Serial data from the user interface (following level conversion to TTL voltages) is input via these (G) input lines. The PA0, PA1 and PA2 output lines from the 6522PIA on the John Bell single-board computer are connected respectively to the (C1+C2), 3 and 13 input control pins of the demultiplexer.

The control logic for selection of the particular data acquisition unit to which serial data are output from the "front-end", is shown in Figure 22. From the demultiplexer these serial output data are transferred via the edge connector to the respective serial input of the data acquisition unit or "slave" processor.

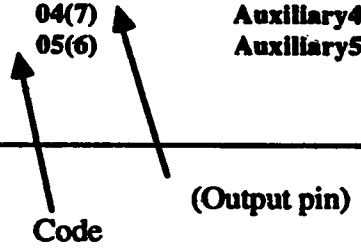
On bootup of the controller the PA0, PA1, and PA2 controlling inputs are held low (this is accomplished by the software in the onboard EPROM). This allows serial data to pass to the controller via pin 9 (Figure 22). Therefore, the controller unit has immediate access to incoming instructions from the "front-end" processor.

A 74251 multiplexer is used to select the desired serial output from the single-board data acquisition system or auxiliary processor for access to the "front-end" processor. This IC is a 16 pin package (Figure 21) with full on chip binary decoding allowing selection of one of the data sources.

This chip also contains a strobe controlled tristate output. The strobe is maintained at a low logic level to enable the chip, whose outputs operate as the standard TTL totem-pole output configuration. One of the outputs provide inverted data (Pin 6). Therefore it is not necessary to invert the signals using a separate 7404 inverter circuit as was neccessary in the case of the dual-processor based data acquisition system configuration.

The same 6522PIA I/O control lines (PAO, PA1 and PA2), as those used for the demultiplexer, are used to control the 74251. This ensures simultaneous connection of both the serial input and output lines of auxiliary and "front-end" processors. The control logic for selection of the particular data acquisition unit to communicate with the "front-end" is shown in Figure 23. From the multiplexer output the serial data from the auxiliaries is transferred on a single wire, via an edge connector, to the "front end".

CONTROL LOGIC				
(PA0/C*)	(PA1/B)	(PA2/A)	Demultiplexer output selected	Unit Selected
0	0	0	00(9)	Controller
0	0	1	01(10)	Auxiliary1
0	1	0	02(11)	Auxiliary2
0	1	1	03(12)	Auxiliary3
1	0	0	04(7)	Auxiliary4
1	0	1	05(6)	Auxiliary5



PA0-PA2 are 6522VIA output control lines

Pins A to C are multiplexer control inputs

C* control input is Pins 1 & 15 connected together.

Figure 22 Logic diagram for channel selection using the 74155 demultiplexer

CONTROL LOGIC			Multiplexer Output Selected	Unit Selected
(PAO/Pin 9)	(PA1/Pin 10)	(PA2/Pin 11)		
0	0	0	00(4)	Controller
0	0	1	01(3)	Auxiliary1
0	1	0	02(2)	Auxiliary2
0	1	1	03(1)	Auxiliary3
1	0	0	04(15)	Auxiliary4
1	0	1	05(14)	Auxiliary5

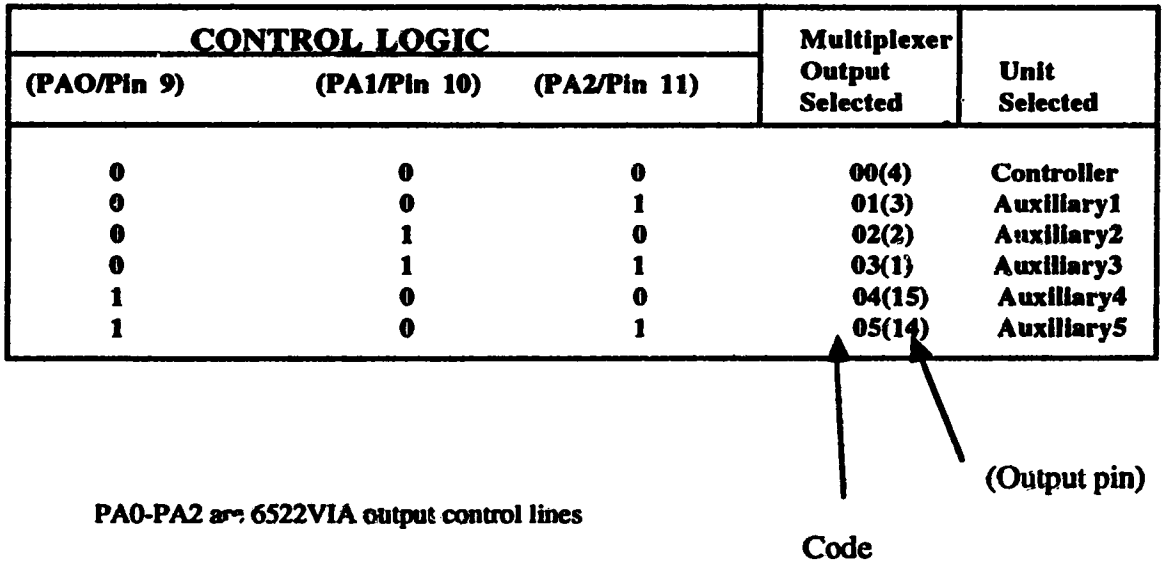


Figure 23 Logic diagriam for channel selection using the 74251 multiplexer

On bootup of the controller the PA0, PA1, and PA2 controlling inputs are held low allowing data on pin 4 to be channeled to the "Front-end". This immediately connects the controller unit itself, for communications with the "front-end" processor.

A schematic diagram of the multiplexer/demultiplexer based network control hardware is given in Figure 24.

3.6.1 Control Signals.

For a flexible networked multiple processor system it was necessary to have a control system which was independent of the relatively slow response times (especially those of inadequate signalling speed) characteristic of serial interfaces. These speed constraints are particularly significant when tasks need to be performed simultaneously by all processors. One of these tasks, is the simultaneous triggering of all processors to acquire data. This simultaneous acquisition of data is neccessary especially when direct sample insertion units are used with the ICP.
These units produce transient signals on several channels simultaneously. Therefore the simultaneous acquisition of data is accomplished by the incorporation of a flexible hardware connection from each individual auxiliary to the controller.

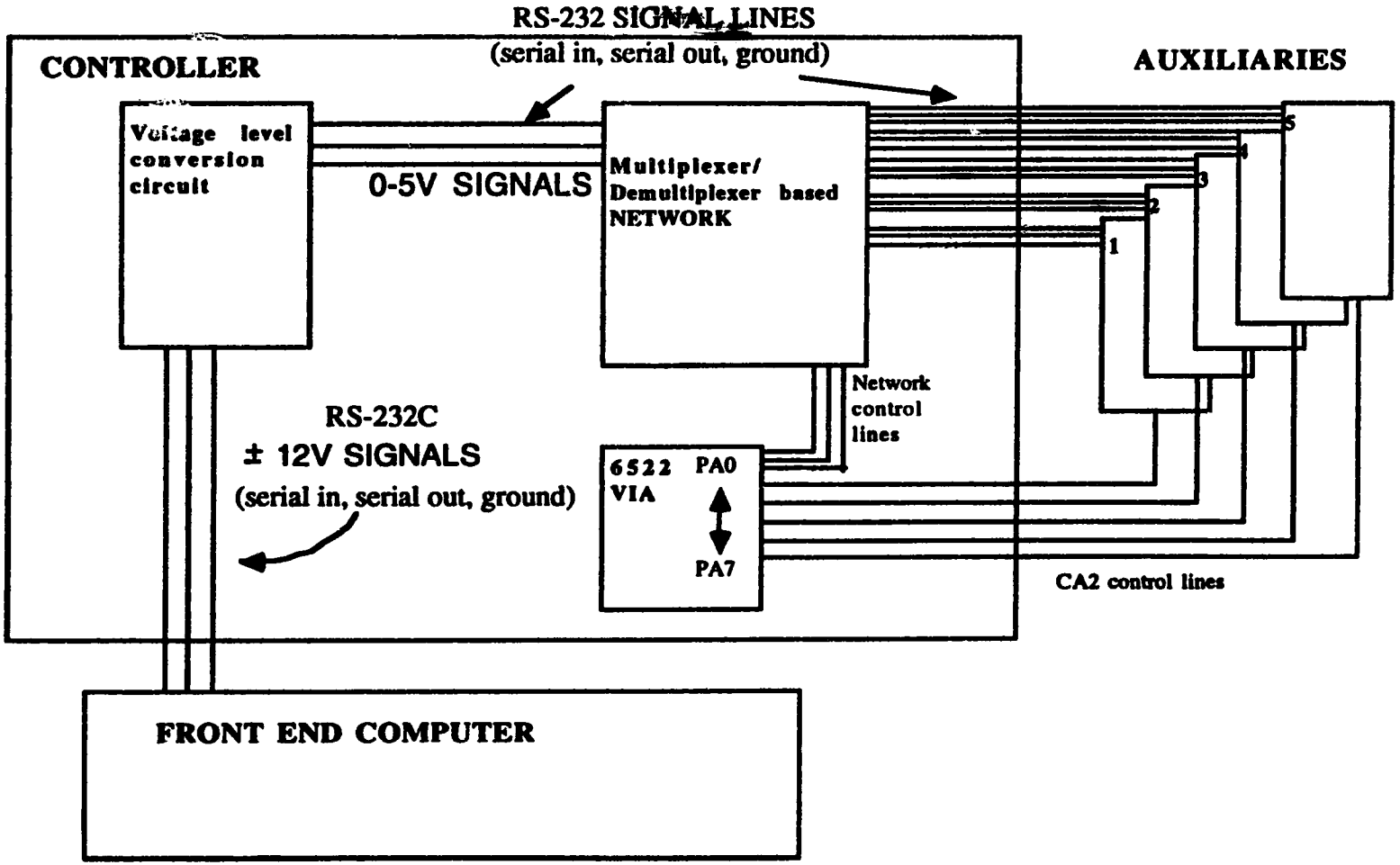


Figure 24 Schematic of network control for serial communication between "front-end" and auxiliary processors

For this purpose a single 6522PIA control line (CA2) from each auxiliary is connected to an I/O line on a 6522 I/O port of the controller (Figure 24). A single byte of data written to this port by the controller, can trigger all auxiliary processors instantaneously.

In the following chapter the software required to operate this networked multiple processor system is discussed in detail.

CHAPTER 4

SOFTWARE DESIGN

4.1 Dual-Processor System

4.1.1 Introduction.

A summary schematic diagram of one channel of the functional multiple PDA direct reading spectrometer as depicted in Figures 2 and 3 is shown in Figure 25. This system consisting of a single data acquisition channel working in coordination with the "front-end" computer is termed the "dual-processor" system. A channel is seen now to consist of the PDA mounting carriage, a PDA driver board, an auxiliary circuit board (Figure 13), and a single-board computer. This channel is connected to the "front-end" computer via a serial interface. These hardware components of the system have been described in the last chapter. While the hardware is important, the design and development of the software to run the system was equally critical to the overall success of the project.

A modular software design strategy was adopted. This facilitated the easy interchange of routines to perform various experiments without changing the core of the operating system. Thus the capability of the system to change to a time study, simultaneous, or fast variable integration time mode etc. was built into the system software.

4.1.2 System Concept

The Apple II+ "front-end" software was designed to be user friendly and menu driven. To facilitate this, programs were written in Applesoft Basic, the particular mode of operation of the

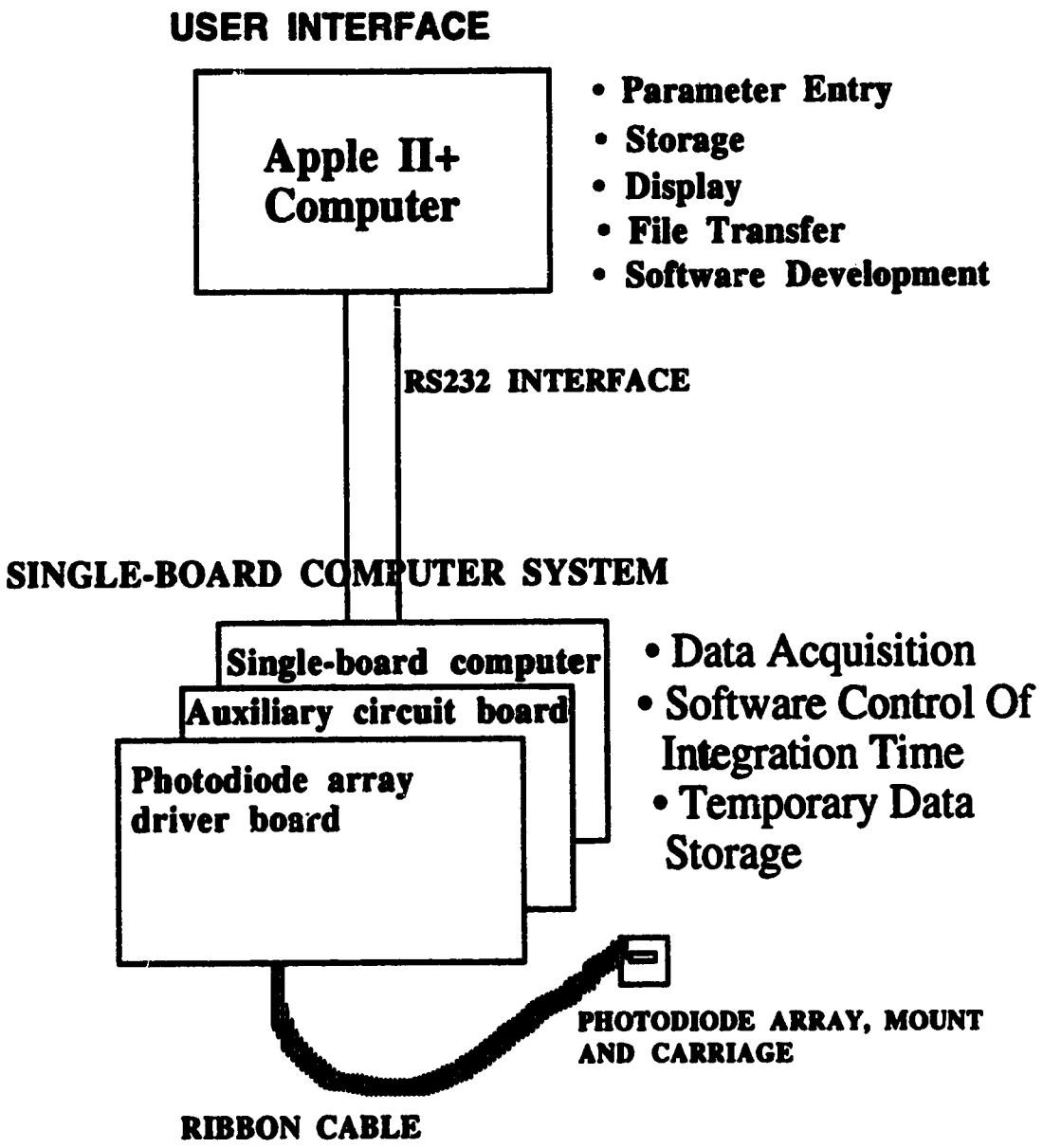


Figure 25 Dual-processor data acquisition system

single-board "slave" could be chosen directly from the menu. On selection of the desired mode of operation, the operator is prompted to enter new operating parameters. Following the entry of these parameters data acquisition proceeds automatically, with control being returned to the user following the transfer of data to the Apple II+ "front-end".

For setting integration times, oscillator frequency and the number of replicates per spectrum, the Apple II+ converts the users requirements into a parameter list. This list is transmitted via a machine language communications program to the single-board "slave".

The Apple II+ communications programs were all written in machine language both to facilitate maximum baud rate and to allow precise control over the serial interface.

All of the programs for the single-board computer, were written in assembly language. These routines were converted to machine code and transmitted to the a reserved RAM area of the single-board computer, whence they were executed via extensive use of indirect subroutine jumps.

To facilitate transmission to the auxiliary of the main single-board operating program, routines were written and made co-resident with the original monitor program in the 2K EPROM of the single-board computer. Many other generally used machine languages routines were also placed in this EPROM and could be called as desired from the main program. This software design strategy, resulted in maximum system flexibility and in the efficient use of the "slave" memory space while at the same time, making software development, modification, testing and implementation much less cumbersome. If this approach was not taken then during debugging, each new program and program

modification would possibly require the burning of an new EPROM or endless manual entry of code

To aid in software debugging it was necessary to operate the Apple II+ functioned both as a terminal and as a functional controller of the single-board "slave" during the data acquisition process. BASIC programs were written for the Apple II+ which when run configured it as a "dumb terminal" or as a controller, thereby facilitating easy conversion to either of these modes of operation.

In order to facilitate various modes of operation by the single-board computer, both the RESET and the NMI hardware interrupts were used. These interrupts when activated, force an indirect jump to the monitor program and to the data communications programs respectively, in the onboard EPROM. Complete software control of this operational mode change, was also implemented. Therefore a control program transmitted to the single-board computer from the "front-end" caused a jump to its on-board monitor while the Apple II+ simultaneously, reverted to the "dumb terminal" mode of operation and visa versa.

4.1.3 Modes of Operation

Depending on the experiment, the software allows the system to operate in the following distinct modes.

1. Continuous readout mode.
2. Single scan mode.
3. Sequential multiple parameter mode.
4. Time study mode.
5. Variable clock frequency and clock stopping mode.
6. Communication control mode.

Since the system is reprogrammable various other application programs for other modes of operation can eventually be developed.

The first mode of operation is useful when the photodiode array is being positioned and focused on a spectral line. The continuous readout of the photodiode array generated spectrum is viewed on an oscilloscope. This oscilloscope is triggered by the data acquisition start pulse from the photodiode array driver board.

The single-scan mode is useful when it is necessary to obtain a rapid indication of the signal with a trial set of parameters. This spectrum, when examined with the available data analysis software can provide for preliminary examination of the signal or facilitate testing of the effectiveness of background subtraction and other data processing software.

The third operational mode, the sequential multiple parameter mode, can digitize and store sequentially six PDA generated spectra. Variable user programmable, integration times and accumulated readouts per spectrum can also be performed. It is possible, to use this mode to examine transient signals occuring over a definite time period. Unlike the following mode, it is not suitable for those applications which would require the taking of more than six spectra of the transient signal.

The fourth mode is a true time study or transient study mode with no replications (i.e., signal averaging) allowed and has equal integration time increments, per spectrum. It is capable of taking 128 successive scans and logging them sequentially as two-byte values. For this mode, the abundant RAM (55K) on the single-board computer is essential, 32K RAM is utilized as buffer space for the acquired data. This data can subsequently be

transmitted to the Apple II+, and stored on disk, or optionally, the data for selected photodiodes can be transmitted and either stored or processed by the Apple II+ software.

With the fifth mode of operation, the clock frequency driving the photodiode array can be changed. This mode would be used for certian research and other specialised applications. For this mode to function, it is neccessary to connect PB7 of the 6522PIA to the present gated oscillator input on the array driver board. The present gated oscillator should be disconnected.

In mode six, the single-board computer is configured as a communications controller, controlling the flow of data between the host and the other data acquisition systems. Simultaneous spectral acquisition by several processors can also be controlled in this mode, while the contoller still maintains its own capability as a spectral acquisition unit. This mode of operation was a first step towards the development of a network controller for a multiple-processor-based photodiode array direct reader

4.1.4 Flowcharts

The following flowcharts, describe the functioning of some of the more important system programs used in the initial dual-processor system which has just been described:

- Single-board operating system program (Figure 26).
- "Front-end" communications program for parameter output and data retrieval (Figure 27)

4.1.5 The John Bell Computer

The John Bell single-board computer, was chosen as the computer with which the controller and auxiliary data acquisition

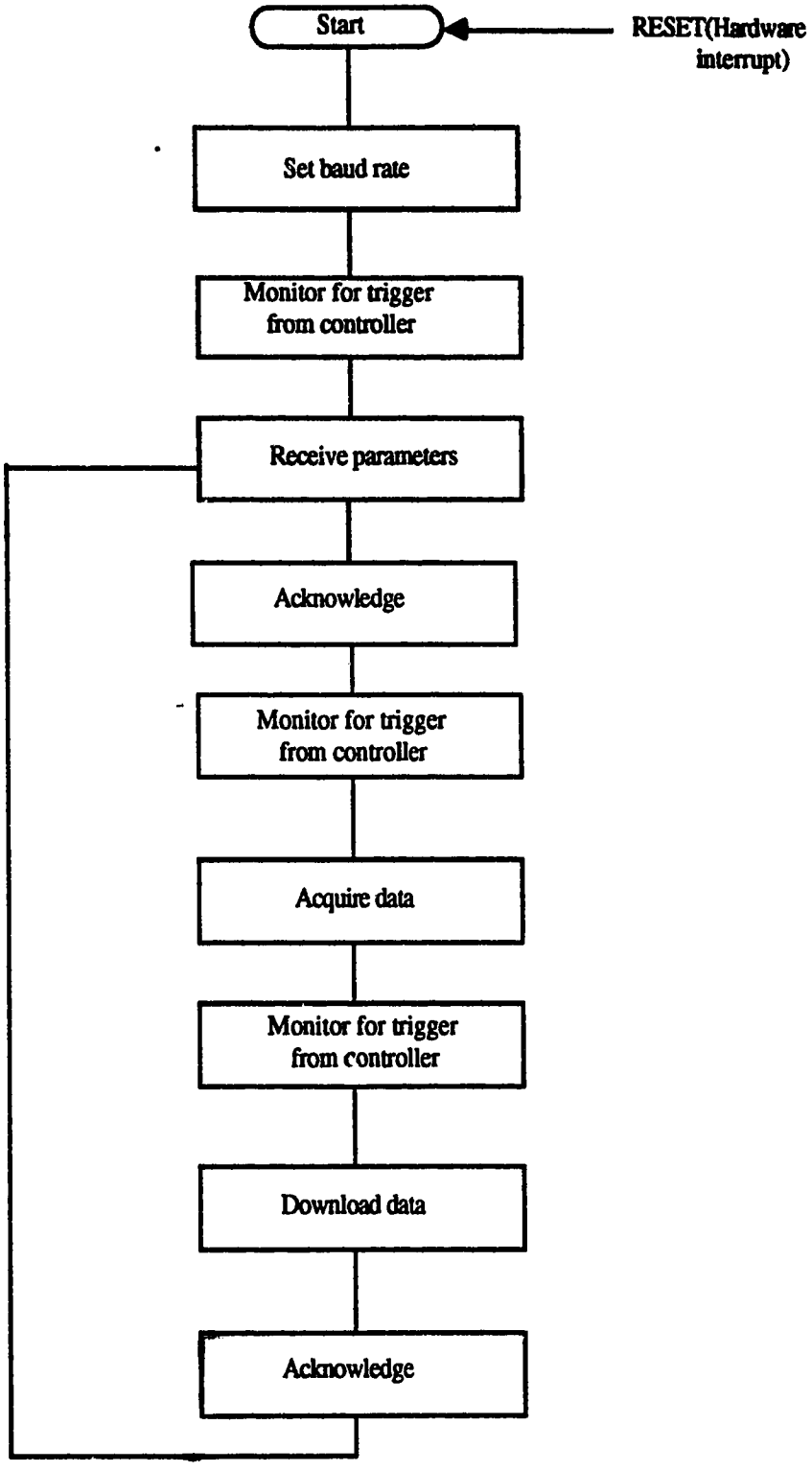


Figure 26 Flowchart of the operating system program for the single-board data acquisition computer

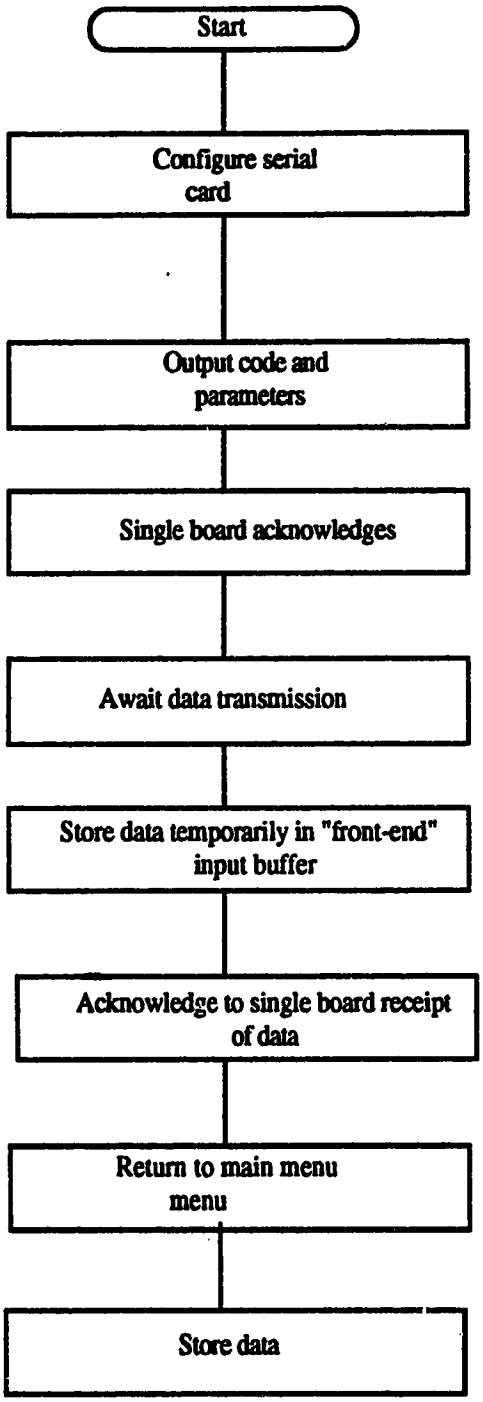


Figure 27 Flowchart of Apple II+ communications program for parameter output and data retrieval

systems were constructed. The important features of this computer were summarised in Table 1. It has 55K of dynamic RAM, a serial RS232 port under the control of a 6850 Asynchronous Communication Interface Adaptor (ACIA), two 6522 Versatile Interface Adaptors (VIA) and 8K of addressable memory space for use by either EPROM or ROM chips. A 2K EPROM based monitor program was supplied by the manufacturer. The major function of this monitor was to facilitate serial communications between the single-board computer and a terminal.

The memory map for the single-board computer is given in Table 2.

MEMORY ADDRESS (HEXADECIMAL)	MEMORY FUNCTION
FROM TO	
FD00 - FFFF	Monitor space(ROM)
E000 - FCFF	ROM space
DFF0 - DFFF	6850 serial Input/Output
DFE0 - DFEF	6522 Input/Output #2
DFD0 - DFDF	6522 Input/Output #1
DC00 - DFCF	User reserved addressable Input/Output space.
0200 - DBFF	Binary storage and machine code memory(RAM)
0100 - 01FF	System stack (RAM)
0000 - 00FF	Zero page (RAM)

TABLE 2. Memory Utilization in the John Bell Computer.

From Tables 1 and 2, major differences between this computer system and the 64K Apple II+ personal computer are apparent. Unlike the Apple II+ which is used as the "front-end" in

this system, most of the memory addresses and a lot of I/O capability is still available to the user. Approximately 7K of EPROM space is available in which user programs can be installed. 55K of RAM space is also available to the user. This constrasts with the 64K Apple II+ where no EPROM space is provided and approximately 8K of free RAM space (when DOS is in memory) is available. The single-board computer is therefore a superior machine for control applications and for rapid data acquisition functions which require a lot of buffer RAM storage space. A version of BASIC (Tiny BASIC) was available for this computer but not utilized since for high speed data acquisition and transmission programs written in assembly language were essential.

The assembly language programs were developed on the Apple II+ and then transmitted as machine code to the RAM of the single-board computer for testing and debugging. Spectra were acquired by running these programs, now resident in the RAM of the single-board computer. These data were subsequently transmitted from the buffer RAM storage locations on the single-board computer to the Apple II+. Eventually, most tested and debugged programs were installed and made coresident with the original monitor on the 2512, 2K EPROM. This EPROM was programmed with the EPROM programming accessory available for the AIM65 computer(27).

A detailed description of the memory map for programs and data stored in the "slave" John Bell computer (used in this dual-processor system) is given in Table 3. The EPROM used in this case, was a 2512, 2K EPROM. The monitor and some additional customised operating system routines are located in this EPROM. With this 2K EPROM in place, only the addresses from $F800 to $FFFF of the 8K memory space ($E000-$FFFF) allocated for EPROM usage is used.

MEMORY ADDRESS (HEXADECIMAL)		MEMORY FUNCTION
FROM	TO	
F800	FCFF	Permament machine language programs (EPROM)
DC00	DBFF	Scratchpad memory (RAM)
9800	DBFF	Unused memory (RAM)
9000	97FF	Relocatable machine language programs transmitted from "front-end" (RAM)
8000	8FFF	Raw acquired data memory(RAM)
7F01	7FFF	Buffer memory for parameters and housekeeping data transmitted from the "front-end" (RAM)
0200	7F00	Unused RAM memory
0100	01FF	System stack (RAM)
0000	00FF	Zero page applications (RAM).

TABLE 3. Allocation of Memory in the Single-board Computer when used in the Dual-processor Mode.

4.1.6 Memory Organization of the Apple II+

The memory map for the overall utilization of the RAM and EPROM memory space in the Apple II+ "front-end" computer, is discussed in section 4.2.3.1 of this thesis.

4.2 Multiple processor system

4.2.1 General Functional Description of the "Front-end" and Data Acquisition Computers

The "front-end" computer developed for the prototype system was the Apple II+. It had the advantage of being readily

available when the project was initiated and had locally available hardware, software and expertise. The available software and hardware was modified to suit the requirements of a "front-end" processor. This reduced the expenditure of both time and funds in the initial start-up phase of the project.

The John Bell computer provided, on a single-board, the ideal integrated set of control components and memory resources necessary for PDA computerization (Chapter 3). It is an excellent unit for handling the special readout control functions of a single photodiode array. This single-board computer is not a widely used product when compared to those computers used in the high volume personal computer market, therefore, it has very few of the capabilities desired of a "front-end" processor.

Front-end processor capabilities should include, user friendliness, data storage and processing capabilities, program development and editing tools and finally, data display and reporting facilities. To access these functions while at the same time, exploiting the ideal characteristics of this John Bell single-board computer for array control, readout and data acquisition it is interfaced to a "front-end" processor. This "front-end" is the Apple II+ microcomputer system.

The Apple II+, being phenomenally successful in the home computer market, attracted a huge number of third party hardware and software developers to meet the growing needs of users. Therefore "front-end" functions can be performed at a reasonable cost. Furthermore, Apple Computers Inc. continue to upgrade the initial versions with larger memories, better accessories and reasonably inexpensive networking products (e.g.AppleTalk Network). The introduction, for the Apple II+ line of computers of new software capabilities eg, window/icon driven software, similar in concept to that utilized on the Apple

Macintosh, ensure the further development of this machine as a more powerful "front-end" processor. This would allow an easy transition to state of the art microcomputer technology with the minimum modifications to the present software.

The Apple II+ is based around a 6502 central processing unit. In this respect, it is similar to the John Bell computer. The common processor, is a feature which simplifies an already difficult multiple processor software design problem.

4.2.2 Software Design Concepts

Proper software design, for both the "front-end" and for the array control and data acquisition processors was essential. Software is required to control the smooth interaction of "front-end" with single-board processors while at the same time providing a friendly user interface, to the operator.

For the John Bell single-board computer systems which lacked on-board software design tools, it was necessary to develop their software on the Apple II+. The developed machine language routines, were stored on the Apple II+ diskette. For debugging purposes, the routines are transmitted to the single-board computers over the serial interface.

For the multiple processor system, additional software was developed, allowing the "front-end" and the John Bell intelligent data acquisition units to communicate with each other over a shared network. An RS232C communications channel from processors on the network to the Apple II+ provided for communication with the "front-end". Control and timing of data acquisition and data transfers was handled by a controller. Therefore, over this serial line application programs, parameters and control characters were transmitted to the peripheral

processors. During data acquisition progress data was transmitted to the Apple II+ "front-end". Following data acquisition, the acquired data were finally transmitted, from the buffer RAM of the single-board computers, to the "front-end" for processing, storage and display.

4.2.3 Description of Apple II+ Software

The Apple computer uses 16 bit addressing and can, as a result, reference any of 65,536 memory locations. A considerable portion of this memory though, is consumed by the operating system and for language interpretation. The memory remaining would not be enough to hold all the necessary programs or to store all the acquired data. To circumvent this inconvenience, maximum use is made of the disc operating system (DOS) in the regular utilization of disc storage. This is facilitated when using the Basic programming language since DOS commands, can be included within a BASIC program.

A menu program written in BASIC, displays a menu on the video monitor and allows the operator to call other BASIC programs from the disk. These secondary programs perform the required task and sometimes call machine language programs and other Basic programs.

For serial communications at baud rates greater than 600 machine language programs are used.

To operate any of the data acquisition units using routines stored on the Apple II+ diskette, machine language routines are initially loaded into the RAM of the Apple II+. From here these routines are transmitted to the auxiliary data acquisition unit using high speed serial communications routines.

Parameters and control data for the auxiliary processors and the controller are initially entered into a scratchpad or buffer area of the Apple II+ memory. A file containing a copy of the scratchpad is stored on diskette. A sorting routine was developed to examine and remove from scratchpad error causing characters (these characters cause errors since they are recognized as control characters by the serial interface). A separate scratchpad table of the error causing addresses is generated. After transmission of all the scratchpad data, to the single-board computer, the temporarily deleted characters are restored using the address table.

Figure 28 outlines the main features of the "front-end" user interface program. A flowchart, describing in detail, the programs which comprise the Apple II+ user interface is given in Appendix 10

4.2.3.1 Organization of Apple II+ Memory Space

The memory map for the Apple II+ when the disk operating system is booted (single-board loaded into memory) is given in Table 4.

Approximately half of the memory addresses are used for specific purposes. Since it was convenient to utilise some of the software developed for the previous system (5), for the purpose of graphical display of the acquired spectra, it was important therefore to maintain the same protected memory locations, for specific programs and data. Machine language programs are protected from being overwritten by Basic programs by using the HIMEM command within a Basic program. "HIMEM: 29439" ($72FF in hexadecimal) at the start of a Basic program limits use by Basic programs of addresses above $72FF. Since $9600 is the lowest address used by DOS it therefore sets the higher limit of

the protected area. Therefore, the addresses between $72FF and $95FF are reserved as a buffer for machine language programs, prior to transmission to the peripheral data acquisition units. Part of this memory area is also used as a buffer for the acquired data, transmitted to the "front-end" by these units.

MEMORY ADDRESS (HEXADECIMAL)		MEMORY FUNCTION
FROM	TO	
D000	FFFF	BASIC language and monitor(ROM)
C000	CFFF	Input/Output reserved memory
9600	BFFF	DOS reserved (RAM)
7300	95FF	Binary storage and machine code program (RAM)
4000	72FF	BASIC programs (RAM)
2000	3FFF	High Resolution graphics page (RAM)
0800	1FFF	BASIC programs (RAM)
0400	07FF	Video screen text memory(RAM)
03F0	03FF	Vector storage (RAM)
0300	03EF	Machine code programs(RAM)
0200	02FF	Keyboard input buffer (RAM)
0100	01FF	System stack (RAM)
0000	00FF	Zero page (RAM)

TABLE 4. Memory Utilization in the Apple II+ Microcomputer

The binary storage and machine language processing space is utilized both during data acquisition and for subsequent data-processing. Therefore, since processing follows data acquisition, the best procedure was to acquire the data initially and to immediately store it on disk. Later, the desired processing could be carried out on the stored data files. Even spectral stripping, was best carried out using background spectra, previously stored on disk. The background spectrum often contained useful

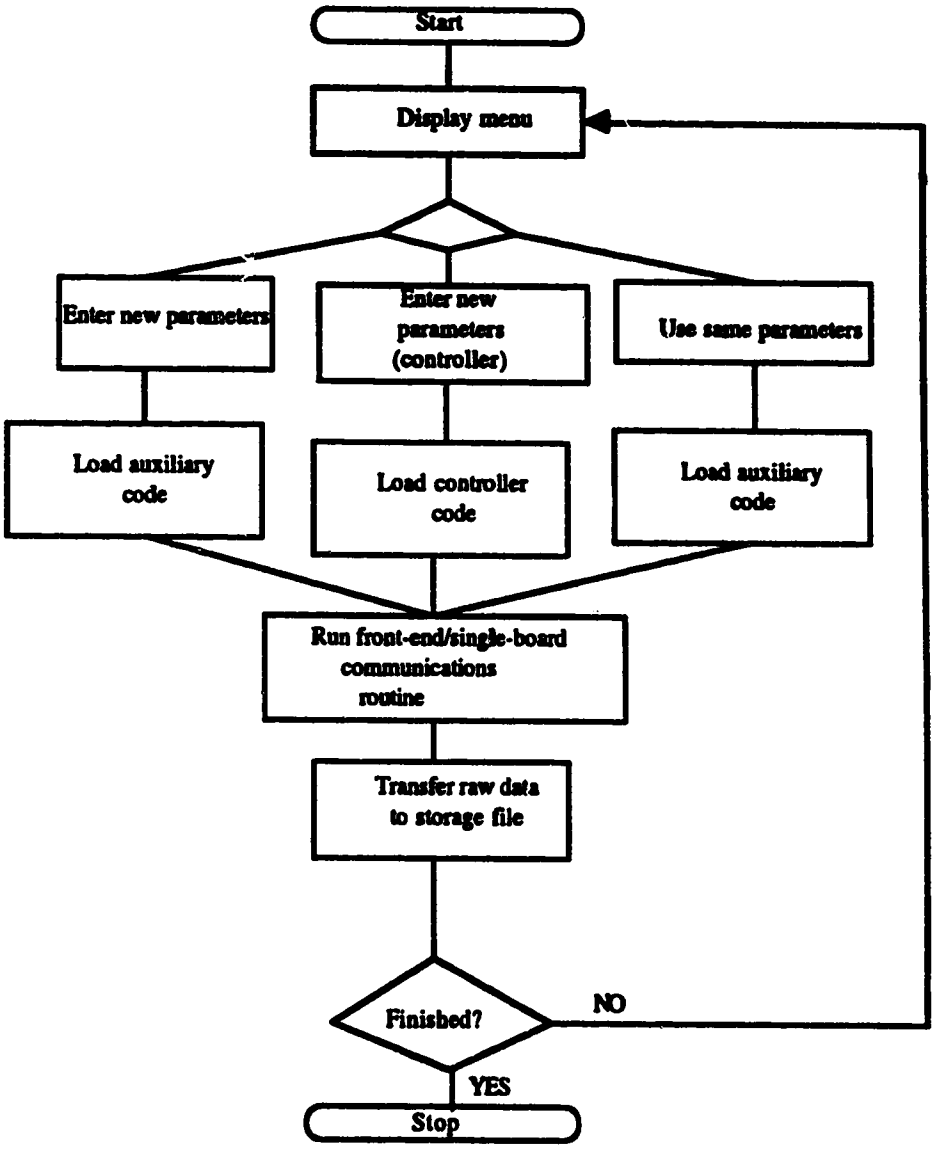


Figure 28 Flowchart for the Apple II+ user interface program

information which could be studied later and therefore required permanent storage. Another advantage was that the immediate processing of data delayed the acquisition process, to the extent that long term fluctuations of the source lead to increased noise. The RAM buffer memory space in the Apple II+ which was used during parameter setting and data transfers from the single-board computer, is subdivided as is shown in Table 5.

MEMORY ADDRESS (HEXADECIMAL)		MEMORY FUNCTION
FROM	TO	
9400	95FF	Buffer space for John Bell programs and data.*
9300	93FF	"Front-end" routines for data transmission
9200	92FF	Buffer space forJohn Bell programs.*
9100	91FF	"Front-end" routines for data retrieval
9000	90FF	John Bell data acquisition routines *
8000	8FFF	Input acquired data buffer.

TABLE 5 Memory Map for Binary Data and Programs for the Apple II+ when used in the Dual-processor Configuration

** Not used when all John Bell programs had been transferred to on-board EPROMS.*

Machine language routines used in the John Bell data acquisition units are loaded from diskette into the memory locations indicated. From here, these routines are transmitted to the single-board "slave" using the data communications routine "Brun" which is called from the main Basic program.

In this way programs for the single-board computers, could be stored on the Apple II+ diskettes and transmitted when required for data acquisition or testing. A short routine in the

EPROM on the John Bell board accepts and stores these programs in RAM and then executes the transmitted program.

This procedure, was found to be the most efficient during program development and testing, since routines did not need to be repeatedly entered into the single-board RAM, by manual methods. If as is to be expected occasionally, some of the RAM based code in the single-board was lost, it was then possible to reload the program from disk storage. When the finalized version of the data acquisition program was ready, it was placed pernamently in EPROM on the single-board computer.

4.2.3.2 Storage and Filing of Data

Data arriving from the single-board data acquisition units is allowed a relatively large buffer area. This could accommodate up to 32, 2-byte readouts of the 128-element photodiode array or 20, 3-byte signal averaged readouts. This large buffer was therefore capable of accepting in a few seconds a relatively large amount of data from the single-board computer. The data transfers occur at a fast baud rate with little liklihood of this data being lost in the process.

Fresh data in this buffer area are finally stored on disk under a file name indicating its origin. This data file is accompanied by a file containing the parameters used. On recall from disk storage, the data can be relocated to other areas of memory for the subtraction of a background spectrum, the calculation of the average spectrum if signal averaging was used and for other forms of spectral processing.

The acquired data can be displayed on the computer monitor, or output to an oscilloscope via a digital-to-analogue convertor. The data can also be transmitted to an Apple

Macintosh computer for further analysis and for report generation. Extensive use was made of this facility.
Since final data processing was more successfully performed on the Macintosh rather than on the Apple II+, the Apple II+ was eventually phased out of this role. Its major function was finally that of a user interface during data acquisition, data storage and transmission.

4.2.3.3 Entering Parameters and Control Data

Operating parameters and control data are called for by Basic programs and then stored in the scratchpad locations using the Basic POKE command. They are then read by a machine language program and output, via the serial port, to the appropriate data acquisition unit.

The control data are examined by the controller to determine which data acquisition unit the "front-end" desires to communicate. Other information, such as indicating to the controller that synchronous data acquisition by all processors is desired is also carried by these control data.

4.3 Software Concepts for Network Control

The rationale behind the IEEE-488 interface and the HP-IB (Hewlett-Packard Interface Bus) is that by coupling interactive data acquisition systems with desk-top computers their measurement power can be enhanced. This was also the overriding goal in the design of the present multiple processor system. Digitization of analogue signals by remote processors can provide more immunity to noise and therefore better data.

Three major objectives must be achieved and combined to develop and configure a less costly, more powerful, multiple-processor measurement system;

- A common interface
- Distributed computing through "smart" data acquisition and control systems with internal microprocessors.
- Powerful "front-end" computing power to provide data processing, data base management, graphics and ease of programming.

Some of the benefits associated with this approach are;

- More consistent results in repeated measurements
- Greater throughput since the system is faster
- More thorough control, because system speed allows more parameters to be controlled and measured in a shorter time
- Greater accuracy because more data can be extracted from the system to allow for error correction on the results.
- "Adaptive" data acquisition since the system can be reconfigured for other measurements by downline transmission of programs from the "front-end"
- Measurement results can be stored temporarally in a memory buffer allowing more rapid sequential spectral acquisitions
- Wide choice of computers for "front-end" to process and manage data and finally
- Synchronous operation allowing all channels to acquire spectra simultaneously

4.3.1 General Description of Network Operation

The complete system consists of a controller, the "front-end" processor, and a number of auxiliary or "slave" processors networked together by a cabling system which provides both serial and parallel data paths (see Chapter 3 for hardware description)

This cable(bus) serves to interconnect all the systems and therefore facilitates both synchronous and sequential communications. The mode of operation of the system is chosen by the user interacting with the "front-end" and is implemented by the controller.

Using the terminology of the IEEE-488 (HBIB) standard, all systems act as TALKER, and LISTENER. Only one system acts as CONTROLLER and is also a TALKER and LISTENER. A TALKER can transmit data or parameters to other devices via the bus and a LISTENER can receive data and parameters from other devices via the bus. Therefore measurement systems LISTEN to receive their parameters and control data and TALK to send their control and progress data (via CA2 control line).

The "front-end" facilitates software development. When a particular measurement application is developed, these programs are placed pernamently in the EPROM memory of the controller and of the auxiliary data acquisition and control systems. The "front-end" then functions in its more usual role as a parameter entry station and acquired data storage and processing device. The controller manages the operation of the system primarily by designating which devices are to send and receive data (or parameters). It also controls specific actions by auxiliary devices e.g. synchronous data acquisition.

A functional outline of network operation, from the point of view of software control, is shown schematically, in Figure 29.

Each photodiode array has the capability of functioning in a completely automonous fashion (synchronous operation, multiple sequential scans, very long integration time scans, etc.), once it triggered by the controller to acquire data. With ample memory (RAM) at each acquisition unit, extensive background and signal information can be acquired.

Multiple sequential spectra at integration times as low as 10ms. can be acquired simultaneously, at each channel. All data can be transmitted to the host or preprocessed (background subtracted and signal averaged) in the data acquisition system. Sometimes, information which may be useful in explaining an observation, can be lost in this preprocessing step, therefore, it is often desirable, to access and store all raw data. For this purpose, adequate memory in the remote system, allows all raw data, including background data, to be stored temporarily and only when spectral acquisition is complete, will data be transmitted to the host.

The controller's role is critical to data acquisition step. It is programmed to trigger spectral acquisition by the auxiliary units, to control the flow of parameters to these auxiliaries, to monitors their progress as they proceed and finally to inform the "front-end" if any system fails to function properly. The controller can also perform data/spectral acquisition itself. It is also important that the controller and the "front-end" can communicate and proceed with usual functions while data acquisition on some channels is still proceeding.

The interconnecting network bus was designed both to simplify the wiring and the software development required while

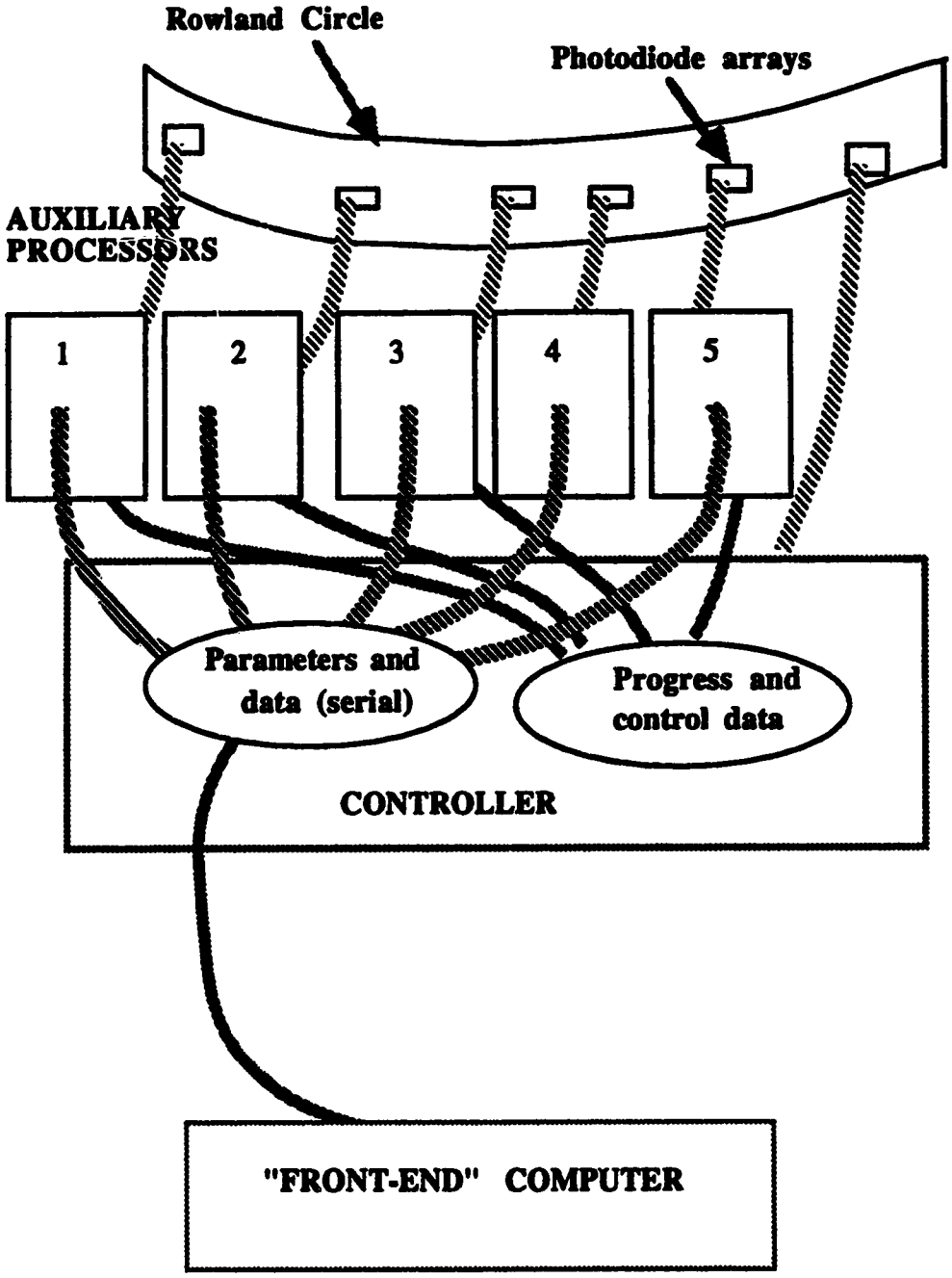


Figure 29 IEEE488 like concept for multiple processor control system

at the same time, achieving the maximum flexibility and control, for various projected applications of the complete system. To achieve this end, a 4 line bus was chosen. Three of the lines service serial data communications, while a single fourth line serves to transfer progress and control data between the controller and the other data acquisition systems. It is this additional connection which gives the system its more powerful control capabilities, since through it, the controller can address all devices simultaneously in few microseconds.

In summary, the signal lines can be grouped into two categories according to their function;

1. RS232 serial communications lines (3 Signal Lines)

2. General interface management and control line (1-signal line).

The serial lines consist of a transmit, receive and a signal ground line. These lines can communicate programs, parameters and data between all processors on the network.

The general interface management line is self explanatory, in that it allows the controller and the controlled auxiliary systems, to perform high speed handshaking control functions. Typical functions include, the signaling to an auxiliary system that data arriving on the serial bus should be intercepted, or that the "front-end" is awaiting the transmission of acquired data. Signals traveling on this line serve also to communicate to the controller that an auxiliary has received or output data. This prompts the controller to reopen its own communications channel to the "front-end" and to await further user instructions

4.4 Overview of Network Software Control

Many of the network features, result from the original design goal of building a flexible but nevertheless standard communications system between processors.

Details of the hardware used to implement the RS232C standard are given in Chapter 4. Level converters (TTL to RS232C and RS232C to TTL) are used in conjunction with the digital multiplexer/demultiplexer combination for network control. These converters ensure that large voltage transitions differentiate the "1" and "0" serial logic levels (therefore, decreasing transmission errors due to noise), carrying data between the external "front-end" and the acquisition units inside the spectrometer. In the more shielded environment, inside the spectrometer casing, TTL levels are used for serial data transmission.

The detailed interactions between the controller (which is also used as a data acquisition unit), auxiliaries and the "front-end" are outlined in the software descriptions given in Appendices 8 and 9.

After triggering spectral acquisition by the auxiliaries the controller will jump to its own spectral acquisition routine and acquire data according to the parameters entered. After acquisition it will immediately transmit its data to the "front-end". All the auxiliaries are acquiring spectra independently, at this time. If one of the auxiliaries is using a particularly long integration time, then it is possible to allow this system to proceed undisturbed. Transmission of raw data from the other systems and the setting of new parameters with the subsequent initiation of an additional data acquisition sequence can proceed during this time.

The CA2 digital input/output control line was chosen to provide handshaking control because it was convenient to operate it in several modes including, pulse output, level output, edge triggered and level triggered input. Therefore it provides a very versatile control line and is suitable for a variety of applications within the network configuration.

4.5 Software/Hardware Integration

To more completely understand the functioning of the network it is necessary to consider in more detail how the hardware and software are integrated in the system.

The chief hardware features are the multiplexer/ demultiplexer combination on the controller unit (Figure 24, Chapter 3). Control of these devices is realized by interfacing their controlling inputs to the PA0 - PA3 lines of 6522#2 of the John Bell single-board computer. Additionally, a CA2 line from each auxiliary data acquisition unit is interfaced to the PA3 - PA7 lines of the same VIA on the controller.

The software for the controller (see Appendix 5) initially configures, the registers of its 6522PIA#2, to open the multiplexer/demultiplexer channels and allow it to communicate serially with the "front-end", at 600 BAUD. It then polls its serial input lines for a code indicating which unit on the network the "front-end" intends to communicate with. This code is a digit from 0 to 6 excluding 1 (which causes an error since it is recognized as a control character by the present "front-end" serial output routine). The code is previously POKEd into the scratchpad location $7F00 of the "front-end", after the user selects the unit from a menu. The code is transmitted from the "front-end" to the controller by the machine language output routine CODE. The

controller uses this code to acquire control data (absolute indexed addressing) stored in its EPROM memory.

Table 6 describes this data (located at addresses starting $F5C1) which is used for control over the network of the auxiliary processor indicated by the code.

HEXADECIMAL ADDRESS	CONTROL DATA (BINARY)	PROCESSOR SELECTED
F5C1	00001001	AUXILIARY 1
F5C2	00010010	AUXILIARY 2
F5C3	00100011	AUXILIARY 3
F5C4	01000100	AUXILIARY 4
F5C5	10000101	AUXILIARY 5

TABLE 6 Data in Controller EPROM Memory Locations used for the Selection and Control of Auxiliary Processors

This data table contains the data required for the following:

- For configuration of the multiplexer/demultiplexer network control lines, using the 6522PIA digital I/O lines
- For configuration of the 6522PIA digital I/O line which is nterfaced to the CA2 control line of the auxiliary data acquisition system.

In this way the controller allows the auxiliary and the "front-end" to communicate, while the CA2 control line provides a trigger for the controller from the auxiliary when needed.

This system reduced the complexity of the software required for communications between the "front-end" and the appropriate unit in the network. Therefore, the task of

substituting a different "front-end" computer at a later stage is made easier.

Having opened communications between an auxiliary and the "front-end", the user can choose to exit the parameter transmission program (Opt 2S) and communicate interactively with the EPROM based monitor program of the auxiliary. In this mode, the Basic communications program "P" is run on the Apple II+ "front-end", making it emulate a "dumb terminal". The modified John Bell monitor program on the auxiliary processor can be activated by pressing the reset switch (grounds the RESET pin on the processor)

Through interactive monitor communications it is possible to run and test the resident routines in the onboard EPROM of the auxiliary or to manually enter assembly coded test routines into its RAM. The monitor supplied with the John Bell single-board computer itself is quite primitive with only memory modify, memory fill, memory dump and run commands available. Nevertheless, even these limited functions were invaluable during system development.

4.6 Software for the Controller

See Appendix 6 for a detailed listing of the controller program and Appendix 8 for a detailed flowchart describing the interaction between the controller with the other processors in this multiple processor system.

4.6.1 Memory Organization

The memory map for the utilization of the RAM and ROM memory space on the controller is given in Table 7.

4.6.2 Developing an Automatic Bootstrap Program for the Controller

The original John Bell monitor was entered on reset by having its reset vector pointing to vectored address $FDOO which is the start of the original monitor program. This has been changed and the changes are now described.

MEMORY ADDRESS (HEXADECIMAL)		MEMORY FUNCTION
FROM	TO	
FCOO	FFFF	Modified John Bell monitor program (EPROM)
F700	FCFF	Unused ROM (except for $F940-50) (EPROM)
F000	F6FF	Controller programs (EPROM)
E000	EFFF	4K of unused ROM (ie not accessed
		by present 4K chip)
DBA0	DBFF	Additional parameter and scratchpad memory buffer(RAM)
8000	DB9F	Raw Data buffer(RAM)
7F00	7FFF	Buffer for controller codes, parameters and other data transmitted from "front-end" (RAM)
0200	7EFF	Additional raw data (RAM)
0100	01FF	System stack (RAM)
0000	00FF	Zero page, used for system pointers and
		Zero page addressing modes (RAM)

TABLE 7. Utilization of RAM and ROM in the Controller.

On hardware reset (by asserting the reset switch) or at power-up the controller is automatically placed in communication with the "front-end" computer. The following software design strategy is used to achieve this.

Using the vectored interrupt capability of the 6502 microprocessor (27,28) the addresses $FFFC and $FFFD are programmed to contain the vectored hexadecimal address $FC00 ($FFFC ($00), $FFFD ($FC)). The initialization program for the controller is located at this address in EPROM. The program configures the PA0-PA3 digital I/O lines of the controlling 6522PIA as outputs, and then asserts a low logic level on these digital output lines. This opens a channel of the 74251 multiplexer (Figure 23). This channel is interfaced to the serial transmit line of the controller's RS232 port and thus, a direct connection for serial transmission of data to the "front-end" serial port is obtained. Simultaneously, the 74255 demultiplexer control lines are forced low, allowing serial data from the "front-end", to be directed via an output channel of the demultiplexer to the serial input of the controller (Figure 22). This channel of the demultiplexer has previously been interfaced to the recieve line of the controller's RS232 port.

4.6.3 Interactive Communication with the Controller

Following the opening of communications channels to the "front-end" (see previous section), the startup routine at $FC00, forces a direct jump to the modified monitor program at $FD00. This monitor program was originally designed to facilitate interactive communication between a terminal and the single-board computer.

The capability of this monitor program is limited to of a few primitive operations, but was nevertheless quite useful during system development. It could display in hexadecimal, the contents of a memory location, run a program provided the hexadecimal starting address of the program was entered, modify the contents of the RAM memory and fill a given memory range

with a desired hexadecimal value. These functions facilitated testing and debugging of the system software.

4.6.4 Modifications to the Original John Bell Monitor

Certain features of this monitor program were modified and customised for use with the present instrument.

The original program utilized hardware control of the baud rates, used for serial communications. For the setting of baud rates the computer used the 16-bit timer and counter on one of the resident 6522 VIAs. These provide the recieve and transmit clocks for the onboard 6850 ACIA chip. Various baud rate were hardware selectable by jumpering the PB0-PB3 digital I/O lines of 6522PIA#2 (Figure 16). For the present instrument this procedure was inflexible and in addition resulted in the loss of 3 digital I/O lines on all acquisition units, including the controller itself. It was nevertheless necessary to have control over baud rate selection in order to facilitate communication speeds consistent with the capabilities of the "front-end" software. This involved interactive communications and rapid data transmission. BASIC for example, can seldom communicate faster than 600 BAUD. This is quite acceptable for interactive communications but is the minimum acceptable data transmission speed when large amounts of raw data must be transmitted to the "front-end".

It was therefore much more desirable to design software selection of the baud rate into the new operating system of the controller. This was accomplished by modifying the original single-board monitor program at memory locations ranging from $FF11 to $FF17 (See Appendix 6 for listing). The code which accessed the data on the PB0-PB2, I/O lines of 6522VIA #2, indicating which baud rate to use was removed. It was replaced

by code which caused the system to operate automatically at 110 baud for interactive communication with the "front-end".

The baud rate can now be changed for faster interactive communications if required, by replacing the code in the EPROM location $FF12 by data given in TABLE 8.

HEXADECIMAL CODES	BAUD RATE SELECTED
00	110
04	300
0C	600
10	1200
14	2400
18	4800
1C	9600

TABLE 8 Hexadecimal Codes used in $FF12 to facilitate Software Control of Baud Rates

4.6.5 Controller Operating System Design

The customised operating system developed for the controller consists of a number of programs functioning as a primary operating system shell. From this shell a library of data acquisition subroutines can be called. The particular data acquisition subroutine used depends on the requirements of the particular experiment.

An operating system was designed which facilitated the modification if desirable, of the system software for operation in various data acquisition modes. Operational modes of interest in the present system are; simultaneous data acquisition from all photodiode arrays including spectral acquisition at very short

integration times, continuous readout of arrays to aid initial focusing and alignment at a spectral region, and the capability to read out and record multiple sequential spectra from each channel for the study of transient signals.

The main program for the controller starts at $F010. This is the sixteenth memory location in the 4K EPROM used. The program initially changes the baud rate to 600. This baud rate rate was the standard rate chosen for the system to communicate data and parameters with the "front-end".

Changing the baud rate is achieved by changing the data in both timer 1 (T1) and timer 2 (T2) registers of 6522#VIA#2. These timers control the frequency at which the receive and transmit clocks on the 6850 ACIA of the single-board computer operate. This faster baud rate is required to hasten the rate at which data are transmitted from the controller to the "front-end". Even faster baud rates, can be achieved but initial experiments indicated that a baud rate of 600 was satisfactory.

4.6.6 Control of Integration Times by the Controller.

The subroutine at $FO9O places the 16-bit number $O780 in scratchpad locations $DBFE ($07) and $DBFF ($80). These scratchpad data are later accessed by the main data acquisition program. This number ($0780) has been calculated to provide initial division of the onboard clock frequency when loaded into the 16-bit timer register of timer 1 (T1) on 6522VIA #1. Therefore, T1 of 6522 #1 acts as a clock divider for the 1.2288 MHz crystal clock on the single-board computer.

The period of the square wave produced is 3.129 milliseconds. This square wave is used as a counter input to a second 16-bit timer/counter on the same 6522PIA.

The number required in the T1 register to yield a square wave of period 3.129 milliseconds, was calculated using the formula:

$$Tp = 2(N+2)Tc$$

where,

N = Number in 16 bit timer register (T1)
Tc = Processor clock period(1/1.22microseconds)
Tp = T1 output period(3.129 milliseconds).

Therefore, N = 1920 (decimal) i.e., $0780 (hexadecimal).

From the integration time entered by the operator, the number of 3.129 millisecond clock periods required to make this time up is computed by the "front-end". This parameter is then transmitted to the controller and stored in scratchpad memory until data acquisition commences. When the data acquisition routine begins this number is transferred to the counter register of timer 2 (T2) of the same 6522 VIA whose T1 is already programmed to output pulses of period equal to 3.129ms.

The oscillator output of T1 appears on PB7. This output is used as an input for T2, via PB6 (Figure 16). T2 which functions as a down counter, flags the processor when the correct integration time has elapsed (represented by the parameter in its register).

The combination of this timer and counter provide 32-bit control of the integration times used in the acquisition of PDA spectra.

4.6.7 Passing Parameters to the Controller

After the controller has initialized the auxiliary processors and sequenced the flow of parameters to them, it must then perform data acquisition synchronously with them. Therefore, it is necessary that the controller has in its memory the correct parameters for spectral acquisition from its attached PDA to commence. These parameters are the signal integration time for the array and the number of replications for signal averaging required (if any) at this integration time.

For sequencing the flow of parameters to the auxiliary processors, the controller must initially identify which of these processors the "front-end" desires to communicate with. The binary equivalents of numbers from 0 through 6 excluding 1, are transmitted as codes to identify the required processor (01 is an ASCII control character and if transmitted causes data immediately following it to be lost when the present Apple II+ communications routine is used). Code "0" is used to indicate the controller itself and codes 2 to 6 identify auxiliaries 1 to 5, respectively.

The routine at $F540 polls the serial port for the code and on receipt of this code places it in a scratchpad memory location ($7F00). If the code is other than zero, this is an indication that the "front-end" desires to communicate with an auxiliary processor. In this case the controller responds by carrying out the following control operations;

1. It alerts the specific auxiliary processor with which the "front-end" desires to communicate.
2. It opens a serial communication channel between the "front-end" and the specified auxiliary.

To assist in performing these functions, the controller uses the transmitted code to access a data table, located at $F5C0-$F5C5 (TABLE 6). The network control lines (PA0-PA2, 6522VIA#2) are configured as active outputs (routine at $F600). The 6522 digital I/O lines (PA3-PA7, 6522VIA#2) interfaced to the CA2 control line of each auxiliary are maintained as inputs (Figure 24).

Using the data from the EPROM based data table (TABLE 6), the appropriate auxiliary is automatically connected to communicate with the "front-end". To trigger the appropriate auxiliary, data from the EPROM based data table are accessed using the code previously transmitted from the "front-end". After a short delay (routine at $F500) which allows the network to stabilize, the auxiliary is activated by a positive edge on its CA2 control line. During triggering, the serial communications channel between the "front-end" and the auxiliary is held open. Following triggering, the controller returns the PA3-PA7 control lines to their input configuration. All other processors are ignored and therefore a single auxiliary processor can be addressed and configured separately by the "front end".

The controller now monitors the CA2 line of the auxiliary for a high logic level which indicates that it has received its parameters. The controller on receipt of this trigger, resumes communication with the "front-end" and monitors for the next code. If the next received is not zero, then the controller repeats the steps described above and allows parameters to be set for the next auxiliary.

If the code transmitted from the "front-end" is zero, then this indicates that the "front-end" has already passed parameters, to all the required auxiliary processors and that it is ready to transmit replication and integration time parameters to the controller itself. The controller now receives these (routine at

$F0E0) parameters and transfers them to its scratchpad memory (three bytes of data are erroneously logged due to network switching, these bytes are discarded). Some housekeeping data are now transferred (routine at $F0F0) to zero page from the scratchpad memory. Corrections are made (subroutine at $F100) if errors occurred in the transmitted scratchpad data. An acknowledgement (subroutine at $F120) is transmitted to the "front-end" indicating that all parameters have been received. Following this, a positive pulse (subroutine at $F570) on the CA2 lines of all processors triggers synchronous data acquisition. The controller now proceeds with its own data acquisition task(subroutine at $F130).

The data acquisition routine used by the controller is similiar to that used in the auxiliary processors.
When data acquisition is complete, the controller outputs an acknowledgement to the "front-end", indicating that it is ready to transmit (subroutine at $F250) its own acquired data.

4.6.8 Control of Data Transmission to the "Front-end".

Following the transmission of its acquired data to the "front-end", the controller proceeds to sequence (subroutine at $F5AO) the flow of data from the auxiliaries.

To facilitate the orderly transmission of data to the "front-end" for processing and pernament storage, a similiar system of codes to that used during system configuration is adopted. This procedure allows the interrogation of each auxiliary independently.

The auxiliary processors await a trigger from the controller before transmitting any data. This is necessary not only because competition between processors for the single serial data link with

the "front-end" would result in certain loss of the data, but more importantly, because the "front-end" has insufficient buffer memory to accept and keep track of all of the data if it arrived in a non-controlled fashion. Therefore data were transmitted from a single processor at a time, and stored under a filename onto diskette.

In fact, it was not necessary to transmit all the data to the "front-end" immediately since it was relatively secure in the RAM memory of the single-board processors. Thus ample time was availabe to complete the transfer and permanent storage of spectra from different processors under identifying filenames.

The controller monitors (subroutine at $F540) the "front-end" for the code indicating the auxiliary processor from which data is to be transmitted. On receipt of the code, the controller uses it to once again to reference the EEPROM based data table (Table 6) for the specific control data for this auxiliary processor. It now opens (subroutine at $F600) the serial communications channel between the auxiliary and the "front-end". It then triggers the auxiliary to commence transmission of its data by applying a positive edge on its CA2 control line.

The controller now monitors (subroutine at $F560) for a high logic level on the CA2 output of the auxiliary as an indication that the auxiliary has completed data transmission. On receiving this trigger the controller resumes communication (subroutine at $F5EO) with the "front-end" and sends an acknowledgement (subroutine at $F290) to indicate that the auxiliary processor has transmitted all its data.

The controller continues sequencing the transfer of data from the auxiliaries until the code "0" is received from the "front-end". This indicates that the controller should return to the start

of its main program in readiness for a completely new multiple-processor data acquisition run.

4.6.9 Access via the Controller to the Monitor in Auxiliary Processors.

Software in both the controller and the auxiliaries allows communication between the monitor of any auxiliary system and the "front-end". This is essential for program testing, debugging or simply for examining interactively memory locations in all processors.

All auxiliary processors on reset, are programmed to monitor the CA2 control line for a positive edge and following this to enter their modified monitor program (See section 4.7.3 for a discussion on these modifications). As already discussed, the controller on hardware reset is connected directly with the "front-end" for interactive communication via its modified John Bell monitor. In this mode the code for the desired auxiliary is entered into sctratchpad memory location $7F00. By running the monitor interchange routine (subroutine at $F640), interactive communication with the modified monitor of the auxiliary processor can be achieved.

The interchange routine initially accesses (subroutine at $F600) data from data Table 6, using as an index the $7F00 based scratchpad code. It then opens the network for communication with the designated auxiliary. the controller then sends a positive edge over the CA2 control line to trigger it into serial communication with the "front-end".

The next function of the controller is to determine when this session of interactive communication with the "front-end" is completed. The digital I/O line of the controller (interfaced to the

CA2 line of the auxiliary) is placed in the input mode. The controller now monitors for a high logic level at this interface indicating that the auxiliary has completed its interactive communication with the "front-end".

The auxiliary processor has a choice of two options in returning control back to the controller;

1. It can return control back to the controller and monitor for another trigger before returning to its monitor program (subroutine at $F600).
2. If the auxiliary has already received parameters and is therefore setup for data acquisition, it may return control to the controller and immediately enter its main program controlling data acquisition (subroutine at $F590).

The auxiliary asserts a low logic on its CA2 control line except when a high logic level is on occasion required to trigger the controller. This avoids erroneous triggering of the controller.

To summarise, a system of control codes are transmitted to the controller indicating to it which actions to taken. Once the controller's main program is started it remains in a loop. Inside this loop, it controls the transmission of parameters and raw data between the "front-end " and all other processors connected on the network.

It can be released from this loop by activating its reset switch. On reset, it is automatically placed inside its modified monitor program for interactive communication with the "front-end" The controller is therefore always under the control of the "front-end".

4.7 Software for the Auxiliary Data Acquisition Unit

See Apppendix 7 for a listing of the program for the auxiliary processor. See Appendix 9 for a detailed flowchart describing the interaction of the auxiliary with the other processors in this multiple processor system.

4.7.1 Memory Organization.

The memory map for the utilization of ROM and RAM in the auxiliary processsor is given in Table 9. The general allocation of memory space is similar to that for the controller, except for the absence of network control software which is not necessary for the auxiliaries.

4.7.2 Development of a Stand-alone PDA Spectral Acquisition Unit.

Similar to the controller the auxiliary data acquisition units utilize the reset vector interrupt capability of the 6502 microprocessor. The $FFFC (data $E0) and $FFFD(data $FC) memory locations, near the top of the EPROM area are modified to contain the starting address of the initialization program (subroutine at $FCEO).

The initialization program asserts a low logic level on the CA2 control line which is interfaced to the controller (Figure 24). It then polls for a positive edge trigger from the controller (subroutine at $F580). The auxiliary therefore remains inactive until the controller triggers it. After triggering by the controller, it asserts a low logic level on the CA2 control line (therefore leaving this line as it was previously) and enters its customised monitor program, which is also located in its onborad EPROM.

Interactive communication can now proceed between the auxiliary and the "front-end", at a baud rate of 110.

MEMORY ADDRESS (HEXADECIMAL) FROM TO	MEMORY FUNCTION
FCE0 - FFFF	Modified John Bell monitor program (EPROM)
F700 - FCFF	Unused EPROM
F000 - F6FF	Program space (EPROM)
E000 - EFFF	4K of unused memory (single-board not accessed by present 4K EPROM chip)
DBA0 - DBFF	Additional parameter and scratchpad memory buffer(RAM)
8000 - DB9F	Raw data buffer(RAM)
7F00 - 7FFF	Buffer for scratchpad data received from the "front-end" (RAM)
0200 - 7FFF	Additional raw data memory(RAM)
0100 - 01FF	System stack (RAM)
0000 - 00FF	Zero page used for; program pointers and zero-page addressing modes.

TABLE 9. Utilization of RAM and ROM in the Auxiliary Processors.

4.7.3 Modifications to the John Bell Monitor used in the Auxiliary.

Three main modifications were made to the original monitor program;

- A new initialization program (subroutine at $FCE0) was entered into the EPROM.

•The reset interrupt vector address was changed from $FDOO of the original monitor to the start of the new initialization program (subroutine at $FCEO).
•The original code at address locations from $FF11-$FF17 was modified to replace hardware selectable baud rates with software selectable rates

The latter modification was previously described in section 4.6.4. It places baud rate selection under software control, thereby allowing the auxiliary to operate automatically at a baud rate of 110 during interactive communication with the "front-end", and at 600 and 9600 baud for data and parameter transfers.

4.7.4 Program Design.

The design procedure adopted in developing the main operating system is in general, similiar to that used for the controller. The software design is modular with major operating programs comprising a series of independent subroutines. All subroutines are called from a main program which sequences the numerous tasks required. These tasks include communication with the controller and the "front-end" in addition to, spectral acquisition with subsequent data transmission.

The data acquisition program appears as a single subroutine called from the main program (operating system). Therefore, the mode of data acquisition can be varied (continuous readout of photodiode array, multiple sequential scans, etc.) by modifying the main program so that it calls an alternative data acquisition subroutine, while the bulk of the main program, remains unchanged.

4.7.5 Main Program.

The main program begins at $F010. It can be called directly from the modified monitor by first running the routine at $F590. This routine triggers the controller into communication with the "front-end". The ACIA on the auxiliary is configured to operate at 600 baud immediately (which is used as a standard communications rate during spectral acquisition). $0780 (decimal 1920) is placed in the T1 timer scratchpad locations of the single-board computer ($DBEE ($07) and $DBFF ($80)). This count, when placed in the appropriate registers serves to reduce the onboard 1.22MHz clock rate to approximately 300Hz for computation of the integration times.

The control of integration times for the auxiliary is carried out in exactly the same way as that for the controller. This has already been described in great detail, in section 4.6.6.

4.7.6 Passing Parameters from the "Front-end" To the Auxiliary Processor.

Before the auxiliary can monitor the serial port for parameters, it initially polls its CA2 control line (subroutine at $F520) for a trigger (a positive edge) from the controller. This line is interfaced to an I/O line of 6522VIA#2 on the controller. Immediately preceeding this trigger the controller opens the communications network for serial communication between the auxiliary processor and the "front-end". The auxiliary now monitors (subroutine at $FOEO) its serial port for integration time, number of replications and other scratchpad data being transmitted from the "front-end".

96 bytes of scratch-pad data are directly transfered from the "front-end". Since three bytes of data are initially received

erroneously, due to switching transients induced on opening the network, the auxiliary is therefore programmed to receive 99 bytes in total, of scratchpad data, the erroneous 3 bytes of which are discarded. The transmission of these three erroneous bytes occurs consistently and reproducably therefore they can easily be removed.

As previously described for the controller, housekeeping data received from the "front-end" is transferred (subroutine at $FOFO) from scratchpad to zero-page locations. If errors are found to exist, corrections are performed (subroutine at $F100) on this scratchpad data. An acknowledgement is transmitted (subroutine at $F120) to the "front-end" indicating that parameters have been received. The controller is then triggered (subroutine at $F530) by a high logic level on the CA2 control line and it takes control of the serial lines from the auxiliary.

The auxiliary, now configured for data acquisition, awaits another positive edge trigger on its CA2 control line, (subroutine at $F540) before proceeding to acquire data (subroutine at $F130) synchronously, with the other auxiliary processors and the controller itself.

Following data acquisition the auxiliary awaits a trigger (subroutine at $F540) from the controllerprior to transmitting its data. Initially it outputs an acknowledgement (subroutine at $F340) to the "front-end" indicating that it is ready to transmit, followed by transmission of data (subroutine at $F250).

Following transmission of data, the auxiliary triggers the controller (subroutine at $F556) and returns to the start of its main program. Here it awaits another trigger from the controller, before monitoring for a new set of parameters for the next experiment.

The ability of its CA2, I/O line, to be programmed in a variety of modes (edge sensitive, level sensitive etc.) and either as an input or an output provides great network control flexibility between the auxiliary and the controller. Since this line is directly connected in parallel to the controller, its response time is in the microsecond range. In the present multiple processor system it lends itself very well to control functions where response time is important i.e., simultaneous triggering of spectral acquisition on all PDA channels This response time would be impossible to achieve over the serial link.

In summary, the auxiliary performs all its functions automatically. Once the main program is started it remains in a parameter receival/data collection/data transmission loop under the control of the controller.

CHAPTER 5

SYSTEM CONFIGURATION AND ALIGNMENT

5.1 Layout of Multiple Processor System

The ICP spectral source and optical systems were mounted on an instrument rail bed constructed by Evans (5) of the type originally developed by Walters (29). The rail bed was aligned in such a way that the source was co-linear with the diffraction grating. The direct reader itself is mounted on a fixed frame so that its entrance slit matches the ICP source mounted on the rail bed.

The detection system comprising of the photodiode array, its mounting carriage, and the triple circuit board assembly comprising the complete data acquisition unit (John Bell single-board computer, RC1024S evaluation board, auxiliary circuit board), enclosed in a rack, is placed inside the dark box of the spectrometer. In the final prototype, five of these detection systems are completely housed within the spectrometer while the components for a sixth are kept to provide spare parts.

The general layout within the spectrometer is shown in Figure 30. All service lines (array cooling water, array ribbon cable, power lines for data acquisition units, etc.) were flexible so that individual units can be moved about with minimum difficulty during alignment.

Dry nitrogen was used to flush the array windows, in order to prevent fogging on the cooled array. This was distributed to all the arrays through a manifold and maintained at about 10cm water head pressure.

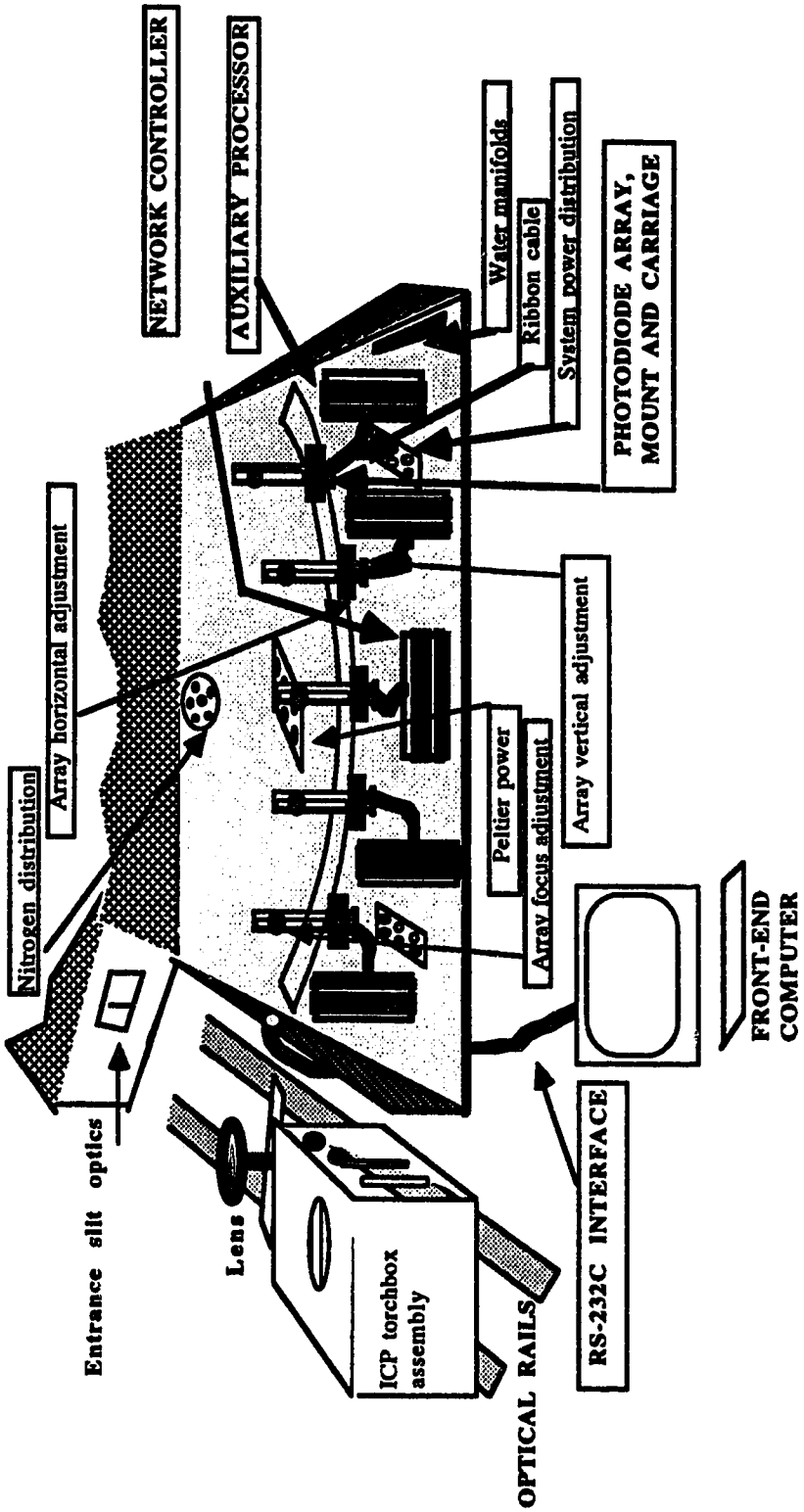


Figure 30 Physical layout of multiple processor photodiode array direct reader

All power is supplied through sets of sockets fitted with keyed plugs to maintain correct polarity

The RF generator for the ICP produces radio-frequency noise and its cooling fans are a source of vibrational noise when kept in the vicinity of the spectrometer. The housing of all the individual data acquisition units within the spectrometer dark-box, linked by a serial interface to the outside for the digital transfer of data to the "front-end", reduced considerably any effect this radiofrequency interference may have had. The 13-ft. long cable connector, between the power supply and the matching network at the plasma head, allowed the power unit and cooling fans to be kept outside the room. This also contributed to reducing the noise problems.

5.2 Locating Spectral Lines.

Light from the entrance slit on the circumference of the Rowland circle is dispersed and focused by the concave grating to images along the circumference of the same circle. This is of course the Rowland circle principle which was described in Chapter 2. In the PMT- based system, the exit slit selected the spectral line of interest for detection. In the PDA spectrometer the photodiode array acts as both exit slit and detector. In effect, it is an array of one hundred and twenty eight, 25 μm wide exit slits and detectors capable of recording simultaneously, photon flux falling on up to a 1.7 nm of a spectral window.

Once the spectral line is located within this window, its peak intensity may drift from one diode to another over the duration of a few hours. Since this drift is directly observable, it can be corrected, in subsequent data processing. This is a major advantage of the windowed (photodiode array) direct reader over discrete detection systems where even a slight drift in the vicinity

of the exit slit presents major realignment problems for the operator.

To locate a spectral line, the 632.8-nm spectral emission of a helium-neon laser was used as a primary reference point on the focal plane. It was set up on the rail-bed and after its intensity was reduced using, neutral density filters, the line position was noted with respect to the scale on the PDA mounting rack. The single-board computer was programmed to send start pulses for continuous readout of the photodiode array at a short integration time while simultaneously, the video signal from the RC1024S driver board was displayed on an oscilloscope. The array carriage was moved until the signal was located, whereupon it was locked in position. The integration time was then increased or decreased, depending on the strength of the signal from the laser. Both vertical and horizontal adjustments were made on the array carriage in order to obtain maximum sensitivity and sufficient focus so as to avoid under-sampling of a spectral line.
Using the position of this array carriage as the primary reference point and the reciprocal dispersion of the spectrometer, it was possible to locate approximate positions for other spectral lines.

The of an spectral line was then located by aspirating a concentrated (usually 1000ppm) solution of the appropriate element. The photodiode array carriage was placed close to the approximate position of the line, calculated using the primary reference point. Using a short integration time, the carriage was adjusted slowly in the vicinity of the spectral line while viewing the array readout signal on the oscilloscope. Once the line was detected and verified to be the sought for signal, the mounting carriage was locked in position and the signal optimized as described earlier.

Hollow cathode lamps when used, were mounted on the rail bed close to entrance slit, for maximum light throughout. It was necessary to use relatively long integration times when optimizing the signal from a hollow cathode lamp. This served to overcome the problem of the low light intensities, generated by some of these lamps.

As one approached the UV or lower wavelength portion of the spectrum it was more difficult to locate lines. This is the result of inappropriate blazing of the grating and the poor UV response of the silicon photodiode.

At times use was made of the BASIC program ARRAYSET (5). This program uses, as a data base, the tables published by Winge, Peterson and Fassel (30). It produces, a list of the useful lines for elements in first, second and third order. The program lists them in spectral order over the range governed by the physical size and shape of the direct reader. The output for each line gives in sequence the order, the spectral position, the element and the symbols indicating whether an ion or an atom line. One drawback is that many lines are not listed in the Winge tables and so are not included in this computerised database.

CHAPTER 6

PERFORMANCE EVALUATION OF THE SYSTEM

6.1 Photodiode Array Noise Characteristics.

6.1.1 Introduction

McGeorge and Salin (31) have discussed the noise characteristics of linear photodiode arrays in relation to their practical use as detectors for ICP-AES. Simpson (32) identified and discussed the various noise sources for the S-series photodiode arrays. It is necessary to characterize the present multiple processor photodiode array system in light of the above studies and the unique configuration of a Rowland Circle based spectrometer.

Simpson described the various noise sources as follows:

1. The photon shot noise of the incident light:
2. The shot noise of the dark current.
3. Pre-amplifier noise.
4. Reset noise of the diodes of the array.

The photodiodes used here have a saturation charge of 14 pC which is equivalent to 87.5 x 10^6 electrons. Therefore when considering noise, the rms noise in electrons will be used throughout. Also, in the following discussion, the photon shot noise will not be considered since it is a characteristic of the radiation source, it will be discussed separately later.

Using the expressions developed by McGeorge and Salin (31) the total dark noise variance on readout of the array is:

$$\sigma_d^2 = \sigma_a^2 + (\sigma_d)_s^2 + \sigma_r^2 \qquad (1)$$

where σ_a is the analytical measurement readout noise, $(\sigma_d)_s$ is the dark current shot noise and σ_r is the detector readout noise which includes both categories 3 and 4 above. σ_a is the uncertainty introduced by the resolution of the final readout device (e.g. digital or analogue display or the analogue-to-digital convertor (ADC)). A 12-bit ADC was used in the present system therefore, the measurements are not readout noise limited (the least significant bit is therefore 0.24 millivolts in a IV signal which is much less than that experimentally observed).

Noise can also be introduced in the form of interference from other sources, such as, radio-frequency noise from the plasma or cross coupling between the video signal output lines and the various clock signal lines to the array. This latter noise source, is quoted in the literature as being of the order of 1% (9) of the full scale range of the photodiode array. This noise, was much greater in magnitude for the previous single processor PDA direct reader (5) due to the array having been removed from the driver board. This problem was removed by the design of a gating circuit (5) which was also incorporated into the present multiple processor system.

Proper shielding, grounding and maintaining the data acquisition units inside the metal dark box of the spectrometer, effectively provided some immunity from radio-frequency and additional sources of noise.

The process of electronically reading out the array introduces noise (32,11). Of this noise, the photodiode reset and thermodynamic noise n_r is given by (32);

$$n_r = 1/q_e(kT(2Cp + 2Cvc))^{1/2} \qquad (2)$$

where k is the Boltzmann constant, T the absolute temperature, Cp the photodiode capacitance, Cvc is video line or clock line capacitance and q_e is the charge on the electron. Simpson quotes a value of 1000 electrons rms for n_r, at 25°C for a 1024 element photodiode array with low noise circuit design.

The noise per readout n_r and the number of readouts m, can be used to calculate the total readout noise contribution σ_r (31) ;

$$\sigma_r^2 = m(n_r)^2 \qquad (3)$$

Therefore, it is expected that the more readouts used to make a measurement the greater will be the relative relative noise. This may account for the observation (33) that signal averaging using several short integration periods for a single measurement leads to a smaller signal-to-noise ratio than a measurement for the same total duration but for a single long integration time.

Finally, two other effects can increase the noise, on photodiode array generated spectra. These are commonly termed, "fixed pattern" and "odd-even pattern" noise and are non-random variations in signal. Both of these, can be removed by subtracting a background spectrum from the analyte spectrum.

The "fixed pattern" noise arises as a result of photodiodes having slightly different sensitivities in their response to dark current and to capacitive coupling of switching transients, onto the video signal on array readout. The "odd-even pattern" observed does not originate in the array itself, but arises because the odd and even photodiode signals of the array are processed by different circuits. The signals are then combined on the RC1024S evaluation board using an on-board sample and hold amplifier before output to the remainder of the data acquisition system.

6.1.2 Experimental

The average background signal and background noise (standard deviations of the background) were plotted as a function of integration time (Figure 31). Note that the vertical of this plot has been expanded and that the 200 millivolts (mV) background is only equivalent to 20% of the saturation charge. Sixteen successive readouts from the array, cooled to -20°C were used for each measurement. Separate measurements were made for both odd and even photodiode populations since the signals are processed by two different circuits.

The background signal increased for both very long and very short integration times while at intermediate integration times i.e from 4 seconds to 64 seconds, it was never greater than 10% of the saturation charge.

The background noise ranges from 0.5-1.0 millivolts (mV) in a 1V signal (the video signal generated at the output of the array driver board ranges from 0-1V) for for relatively short integration times, it remains at about this level down to very short integration times but reaches a maximum of 30mV for the longer integration times used.

6.1.3 Discussion of Results

The dark current leakage decreases the charge on the photodiode capacitance and also produces a shot noise. Dark current shot noise can exceed the readout noise and thus become the major noise source if dark current is not controlled. Vogt et al (11) and Talmi et al (9) have characterized and discussed the control of photodiode array dark current. It is important that dark current be kept as low as possible to maintain the dynamic range

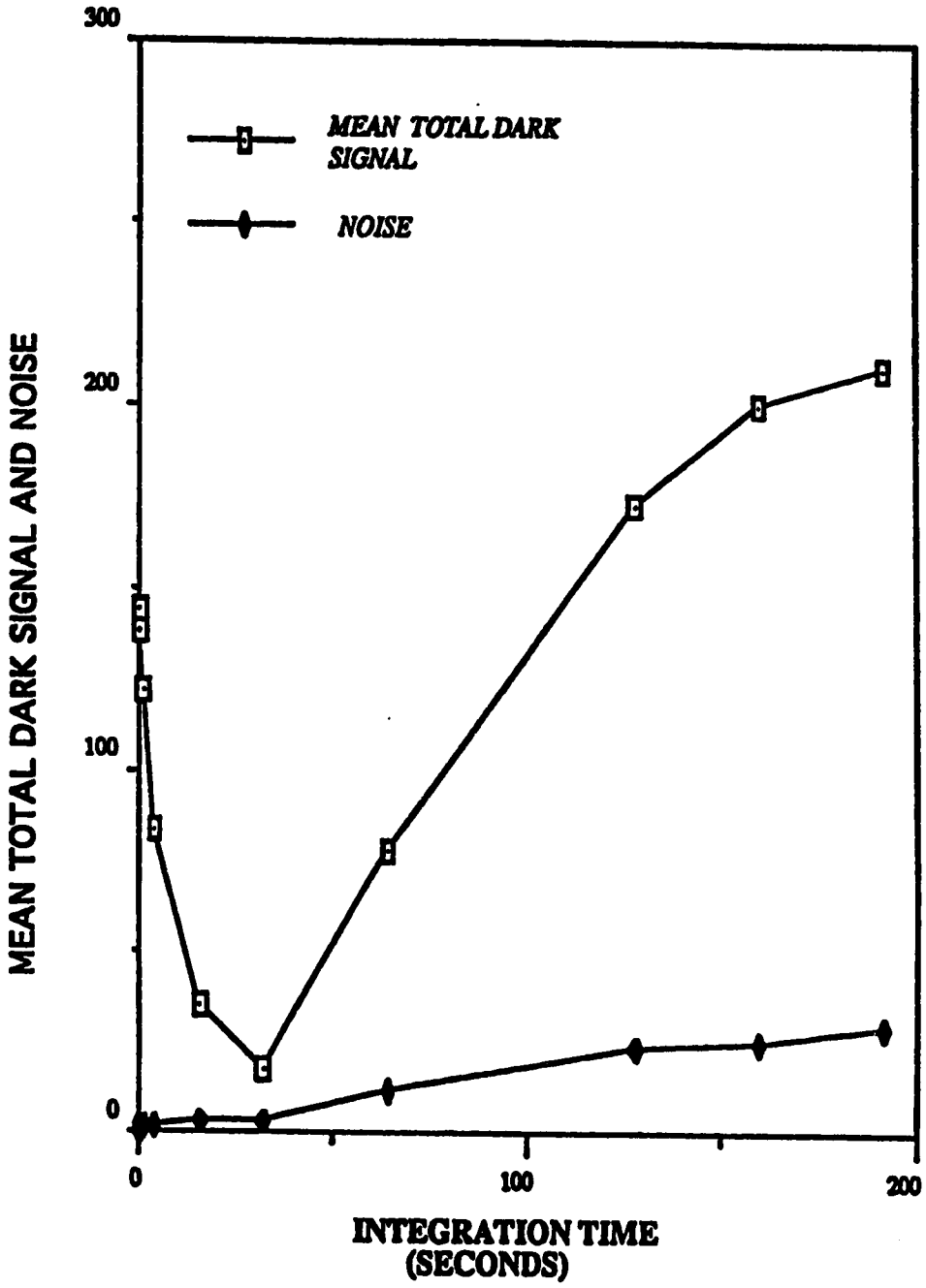


Figure 31. Mean dark signal and noise as a function of integration time

and to reduce the photodiode to photodiode dark current variations. The dark current drops to half its value, for every 6.7°C (9) drop in temperature while at room temperature the photodiode array can saturate in 2-10 seconds. There is an integration time dependence on dark current.

The dark current shot noise n_d (in electrons) is given by (11);

$$n_d = (I_d T_i / q_e)^{1/2} \qquad (4)$$

where Id is the dark current and Ti is the integration time in seconds, qe is the charge on an electron in coulombs.
For a 1- second integration time at -20°C Talmi and Simpson (9) reported n_d as 545 electrons rms.

Taking $545Ti^{1/2}$ electrons as the dark current shot noise and 2000 electrons (31) as the minimum readout noise and assuming the analytical readout noise is insignificant, then at -20°C and a 100 sec. integration time the total noise variance on readout of the photodiode array can be calculated in electrons as:

$$\sigma_d^2 = 0^2 + (545(100)^{1/2})^2 + 2000^2$$

This is equivalent to a total noise of 5805 electrons which when expressed in volts (using 87.5 x 10^6 electrons as the photodiode saturation charge and a 1 Volt output from the array as equivalent to this charge) is approximately 66 microvolts (μV) on a 1 Volt signal (i.e. 5605/87500 x $1x10^6$μV/Volt). This is much less than the experimental noise level in the present system which has about 1 mV rms noise.

The photodiode array temperature can be reduced and controlled using thermoelectric methods (9,10) or liquid nitrogen (11). In the present system, the Peltier coolers succeed in cooling the arrays to approximately -20°C which should be sufficient to reduce the dark current and thus the total dark readout noise, to much less than 1 mV in a 1V signal.

Over a range of integration times less than 16 seconds and greater than 30 seconds, the total dark readout noise is found to be greater than this. Total readout noise is obviously very dependent on the integration time used.

Most of the previous predictions concerning dark current assume that the temperature is held constant during the integration time. This of course, is not true since the Peltier coolers are not absolute coolers but heat transfer pumps transferring the heat from the photodiode array to the cooling water. Therefore, fluctuations in the voltage supply to the coolers or in the flowrate or temperature of the water carrying heat from the coolers can lead to variations in dark current over an integration time period. Evans (5) estimated that a change in temperature of the cooling assembly of 0.029°C over a 100 second integration time could cause a dark current noise of the order of 1mV. This would require that the Peltier coolers have a long term voltage stability of below 0.08% or that the cooling water has a much greater temperature stability than 0.03°C.

Power dissipation within the photodiode array chip during readout, can also lead to the generation of hole-electron pairs and thus increased dark current noise (11). This is more significant at short integration times, especially when the array is read out continually in succession for the purpose of signal averaging. Continual readout of the photodiode array is usually the standard clocking technique for PDA spectrometric systems. For the above

experiment, the array was not read out continually, prior to signal acquisition. Therefore the initial burst of readouts, with the associated heat dissipation could cause an instantaneous jump in dark current. It is possible therefore, that this is the cause of the higher than expected background for the array (cooled and in the dark) for very short integration times.

Vogt et al (11), have reported that for an array cooled to below -130°C that five successive readouts caused an equivalent of 3000 electrons increase in dark current. Furthermore, they note that it takes a further 30 seconds after a quick burst of successive readouts for the array to regain equilibrium. This effect is also observed on readout in a similar way of the present arrays. This increase in dark current at very short integration times is obvious from the data, plotted in Figure 31.

At longer integration times, the standard deviations (noise) again tended to increase. This is possibly due to long term instabilities or drift in the Peltier cooling system, described earlier. An optimized system, designed by McGeorge (13) gave a 1 part in 2000 noise or 0.5mV standard deviation in a 1V signal. This is marginally better than that observed for the present system under similar operating conditions.

Clearly, the electronics and cooling systems require optimization for operation at or near the detection limit. Since the use of longer integration times is essential to compensate the photodiode array detector for its poor sensitivity relative to the PMT, it is critical therefore, to reduce the background noise at the longer integration times. This can be achieved by better control of the cooling system.

It is clear from this analysis, that the photodiode array is capable of operating in a very low noise mode. This can be

achieved by implementing greater control over factors which have been identified as leading to system instability. These include the photodiode array cooling system and the choice of operating parameters including the integration times which are used. These conditions must be implemented in the present system to achieve the theoretically optimum low noise performance

6.1.4 ICP Noise Characteristics.

Much emphasis is placed on the noise characteristics of the detector in a spectroscopic system while the noise performance of the source itself, is often neglected. Fortunately, the ICP noise performance has been evaluated by many authors (31, 33-37).

The ICP source with PMT detection, has been reported to be flicker noise limited at signal levels well above the detection limit (33). Therefore at approximately 100 times above the PMT based detection limit, the standard deviation of the signal increases linearly with the signal intensity. In the same publication, it was reported that there was little or no dependence of signal-to-noise ratios on plasma coolant gas flow rate, that there was an approximately 20% decrease in signal-to-noise ratio on going from 1.5kW power to 2.5 kW power while the signal to background ratios decreased by a factor of 3 to 4 and finally, that the use of an appropriate internal standard leads to a doubling of the signal-to-noise ratio.

Boumans et al (36) reported that at low radiant flux such as encountered for background signals at relatively low wavelengths (<250 nm), photomultiplier shot noise tends to dominate the noise characteristics of the system. The type of nebuliser used also affects the noise characteristics of the system (38).

Salin (33) reported that at of the Zn I 213.8 nm and the Cd I 228.5 nm lines, a 5 ppm solution of Zn and Cd respectively generated signals that were not photodiode readout noise limited. No significant increase in signal-to-noise ratio was achieved by increasing the integration time. It is therefore inferred from this paper, that the transition from being photodiode noise limited to source flicker noise limited depends on the many factors including, the throughput of the spectrometer, the concentration of the solution, the number of array readouts which are averaged per measurement, etc.

6.1.5 Photodiode Array/ICP Detection Systems.

In a detailed theoretical and practical study McGeorge and Salin (31) concluded that photodiode arrays should be capable of performance comparable to that provided by PMT detection systems for wavelengths longer than 230 nm. This conclusion is based on the use of systems with collection efficiencies and integration times similar to those which are presently used in conventional spectrometers. If the wavelengths are less than 230 nm then the ICP-PDA performance will not be as good that for an ICP-PMT system. This is especially true when operating close to the detection limit. Well above the detection limit, the combination of the ICP and the PDA should again compare well with PMT-based systems.

6.1.6 Compromise Conditions for Photodiode Array Spectral Measurements.

Despite the frequent use of photodiode arrays in ICP emission spectrometry and frequent studies of their performance, very little has been said concerning practical compromise conditions for their operation. Furthermore, although photodiode arrays offer good overall characteristics for spectrometry, the

requirement for increasing integration times, to enhance their effectiveness, in weak signal situations (using the ICP) has received little attention.

The shortest possible integration times are of course desirable and analysts would perhaps be a little concerned when integration times of 100 seconds or more are used. A shorter integration time is associated with a faster measurement. In coming to this conclusion, analysts should be aware that the photodiode array is a multichannel device, integrating information on at least the equivalent of 128 channels simultaneously, during this time.

Therefore, when compared to photomultiplier based multichannel systems, a more suitable view would be that the time per resolution element is less than 1 second. Likewise if the 100 second integration time was used for a 1024 element array then we could view this as less than 0.1 second per resolution element.

Another more important question that needs to be addressed concerns the use of longer integration times i.e., can the use of very long integration times lead to an increase in signal-to-noise ratios? This depends on both the characteristics of the photodiode array detector and the source of spectral information i.e. on the limiting noise in the system.

It has been reported that in low- light level experiments, such as in astronomical spectroscopy, the use of very long integration times, sometimes over several hours, leads to better measurements resulting from increased signal-to-noise ratios. For these measurements a photodiode array, cooled to liquid nitrogen temperatures (11) was necessary. This indicates that a properly cooled photodiode array system with low noise electronics, has no inherent signal-to-noise ratio disadvantage when used at long

integration times. This of course assumes high stability of both the electronic components and of the cooling system.

In a study of the effect of various nebulisers on the signal-to-noise ratio characteristics of the ICP source, Belchamber and Horlick (37) found that for both the Meinhard and Cross-flow nebulisers, the ICP signal-to-noise ratios remained constant and sometimes increased as a function of integration time. For the ultrasonic nebuliser there was a marked decrease in signal-to-noise ratios as a function of integration time. The measured signals were well above the detection limit for these experiments. These results indicated that signal-to-noise ratios for some systems depended on nebuliser design and therefore on the desolvation and atomization processes occurring in the plasma. Typical signal-to-noise ratio limits of 100 and 500, for analyte ion lines and argon atom lines (no desolvation occurring) respectively, were also reported.

Considering the above discussion and the experimental results on the noise characteristics of the photodiode array, the following parameters and operating conditions were used when possible in order to extract the best data from an ICP-photodiode array system;

1. Single or double array readouts per measurement, rather than signal averaging using several replicates which would tend to introduce noise

2. Lower ICP power for best signal-to-noise and signal-to-background ratios.

3. Dynamic background (subtracting baseline on same spectrum) and blank background subtraction

6.2. Performance Evaluation using the ICP Source.

To properly evaluate the performance of the instrument it was used in an analytical situation with the ICP source. It was decided to evaluate its performance based on the following criteria, over a major portion of the usable spectral range of the spectrometer. The following performance characteristics of the spectrometer were evaluated:

- •Signal-to-noise ratios (S/N).
- •Detection limits.
- •Linear dynamic range (calibration curves).
- •Background subtraction capabilities.
- •Spectral overlap corrections.
- •Simultaneous multielement analysis using multiple PDAs

In the remainder of this chapter, both the signal-to-noise ratios and the detection limits achieved are discussed. The other performance features mentioned above, are examined in detail in the next chapter.

Separate 1000 ppm stock solutions of calcium, zinc, magnesium, copper and manganese were prepared and diluted close to the expected detection limits, doubly distilled and deionized water was used for all dilutions. The plasma was operated at compromise conditions (see Appendix 11). These chosen elements cover a spectral range from 213 to 403 nm which combined with the scope of the studies carried out, should give a good indication of the performance and possibilities of this spectrometric system. It should be noted that signal-to-noise ratios and detection limits given here provide only indications of the system performance and are by no means the best data achievable with PDA systems. They nevertheless provide

information on this instrument's performance under normal day-to-day working conditions.

Unless otherwise noted the integration time used for spectra displayed in this chapter is 30 seconds

6.2.1 Signal-to-Noise Ratios;

Close to the detection limit, the limiting noise level is due to the inherent noise in the photodiode array detection system (33). This noise is independent of the analyte signal but has a dependence on the integration time used and the number of replicates used for each measurement.

So that this dependence on the integration time is kept constant for all spectral signals measured, a 30-second integration time was used throughout. This is viewed as a compromise integration time. 32 single readouts of the array at 30 seconds integration time each, were recorded and the water background was subtracted from each. The signal-to-noise ratio was calculated from the analyte signal spectrum.

The peak height signal, corresponding to the photodiode which measured the strongest analyte signal for that particular element was used. An intra-spectral baseline height was not subtracted, therefore the signal-to-noise ratios may be lower as a result. Additionally, since the noise measurement was made on the signal itself and not on the background signal, therefore the noise levels obtained are expected to be higher (the latter method is often used in error, for S/N calculations).

Close to the detection limit, photodiode readout noise will be significant. Since signal averaging is not employed for these

measurements, the readout noise will tend to lower the signal-to-noise ratios achieved.

The calcium II line at 393.4 nm (Figure 32) was chosen since it has a very intense emission in the ICP. A signal-to-noise ratio of about 20 for 100 ppb calcium solution was obtained (Table 10). This is quite good considering the total measurement time for 32 readouts is in excess of 15 minutes. A study carried out subsequently, gave a signal-to-noise ratio of double the value achieved here (40) but using a total measurement time of 6 minutes. A shorter measurement time, results in decreased drift and therefore a better signal-to-noise ratio if drift is the limiting source of noise.

The magnesium doublet at 279 and 280 nm (Figure 33), occurs at shorter wavelengths than the calcium signal. The doublet spacing is such that both lines can be measured with a single array. The signal-to-noise ratio measurements were made using similar conditions to those used above for calcium.

The peak height signal-to-noise ratio for a 1 ppm solution of magnesium was 116 (Table 10). The the Mg II 279.55 nm line was used and the results indicate that for some signals, a good signal-to-noise ratio can be achieved at a reasonable integration time. Evans's (5) results for this measurement, could not be directly compared. He found a signal-to-noise ratio of less than 1 for a 10 ppb solution of magnesium. It is worthwhile noting that for a smaller number of readouts i.e., for a shorter total measurement time, that the signal-to-noise ratio achieved was greater. This indicates (as was noted previously for the calcium data) that for a shorter measurement period, less long-term fluctuations or drift in both the signal source and detection system can occur.

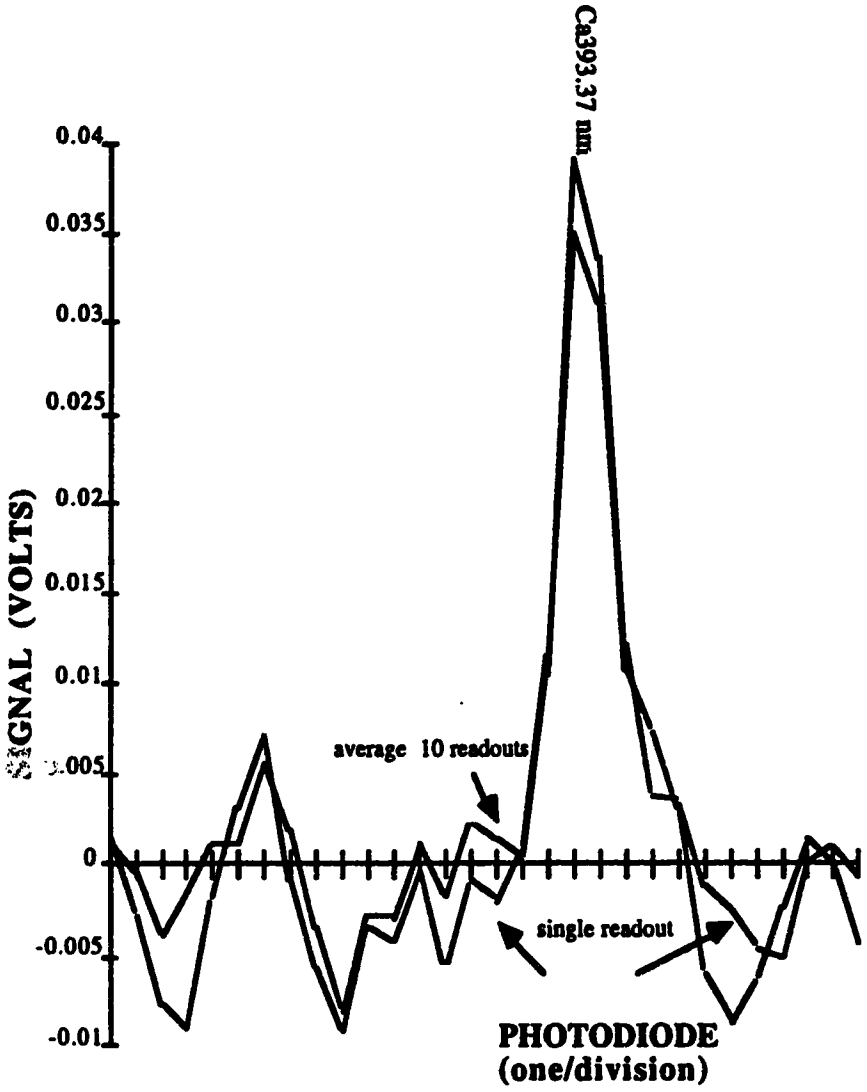


Figure 32 Spectrum of Ca II at 393.4nm, 100ppb solution for both a single and a signal averaged readout, 30-sec. integration time.

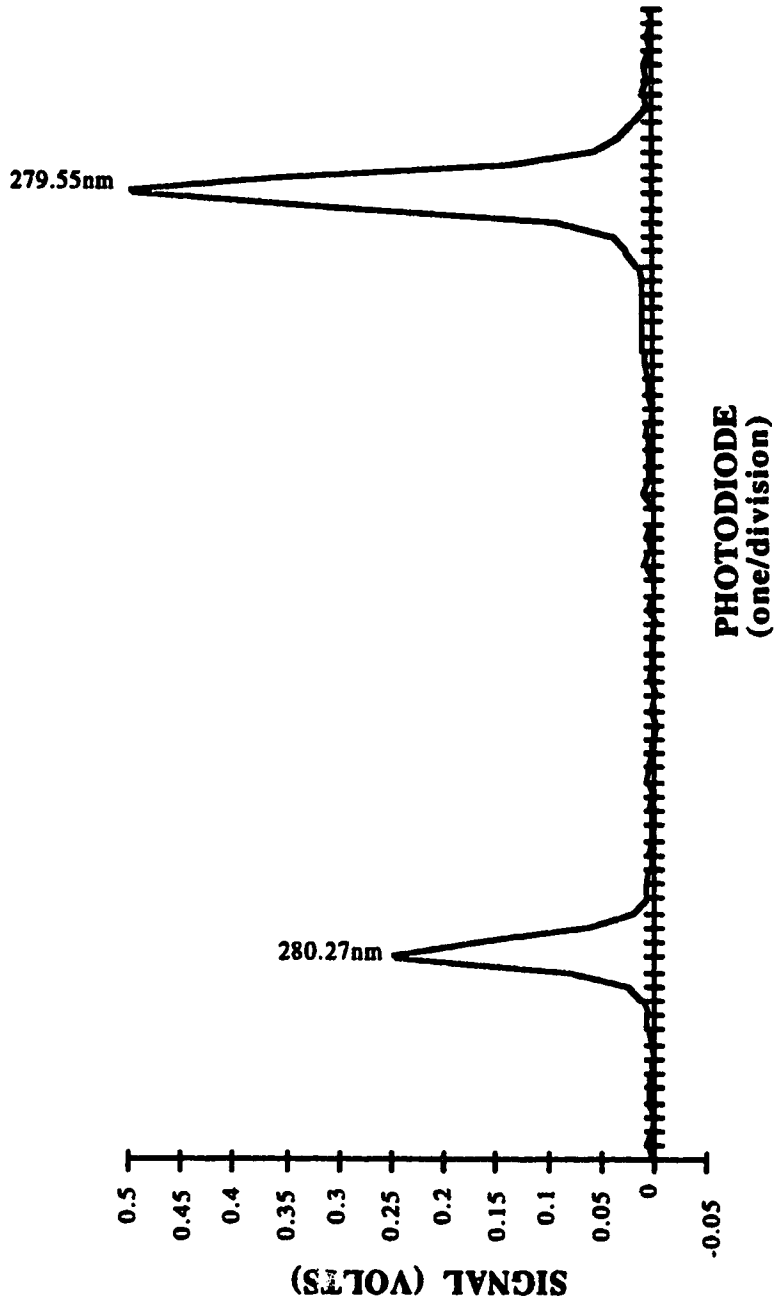


Figure 33 The Magnesium II doublet at 279.55 and 280.27nm, 1ppm solution, 30-sec. integration time.

Averaging six array readouts and calculating a S/N over the same total measurement time, approximately doubled the signal-to-noise ratios.

SELECTED ELEMENT		SIGNAL-TO-NOISE RATIO		
ELEMENT	CONCENT-RATION	WAVE-LENGTH	32 REPLICATES	AVERAGE (6 REPLICATES)
MnI	10 ppm	403.08 nm	18	45
MgII	1 ppm	279.55 nm	116	213
CaII	100 ppb	393.36 nm	22	30
CuI	10 ppm	324.75 nm	90	200
ZnI	10 ppm	213.85 nm	20	45

TABLE 10 Signal-to-Noise Ratios for Selected Elements

Ratioing the background (background signals from several photodiodes on the same array as the signal) by an iterative procedure with the signal, also approximately doubles the signal-to-noise ratio. This is especially obvious for the magnesium data, probably because the signal is relatively strong and the background has possibly, some non-random fluctuations (possibly stray light) which correlate with it. Therefore an internal standard type of effect can be achieved by iterative ratioing of the analyte signal with the background. This type of data processing is only possible due to the simultaneous acquisition of both signal and background on the same photodiode array.

For manganese the triplet at 403.08, 403.31 and 403.45 nm (Figure 34) was chosen because these lines are close enough together to fall on a single array. The baseline resolved triplet illustrates the resolution which can be achieved with this spectrometer. Baseline resolution of lines less than 0.14 nm

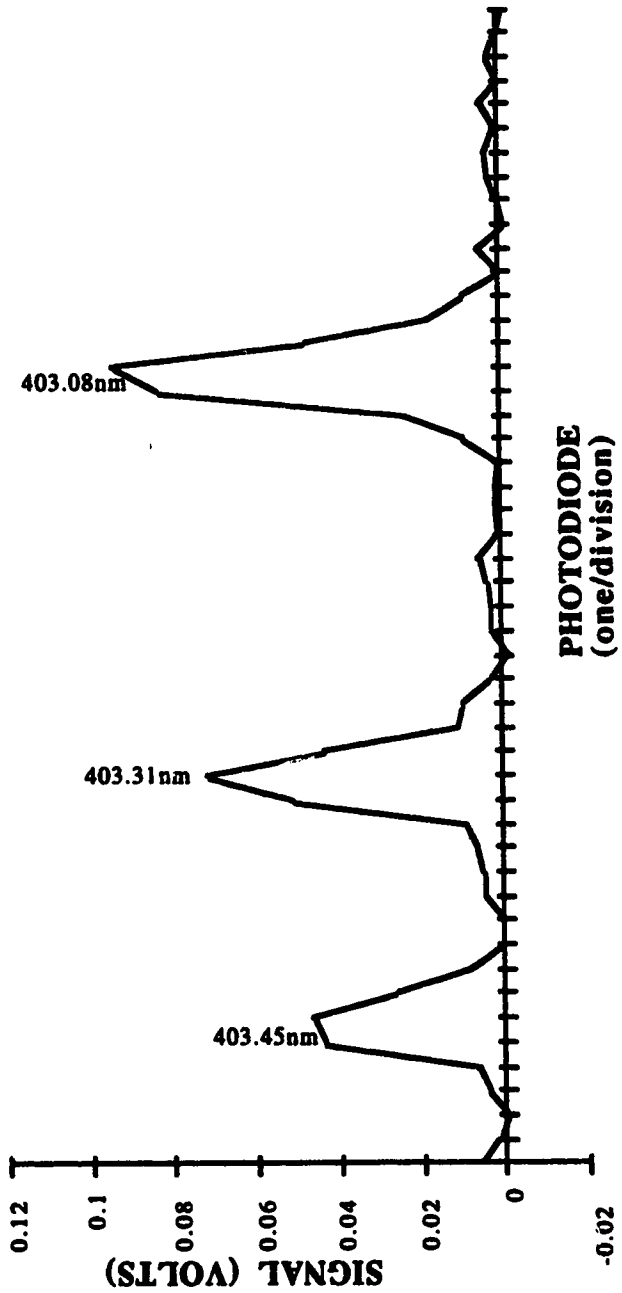


Figure 34 The Manganese triplet at 403.08nm,403.31nm and 403.45nm, 10ppm solution, 30-sec. integration time. (background subtracted spectrum).

apart is easily achievable. The signal-to-noise ratio of 18 for the peak height of the 403.08 nm line is again typical for such low intensity signals, over the approximately 15 minutes which was required to take the data.

The Zn 213.86 nm (Figure 35) spectral emission was chosen since it is a wavelength in the far-UV and is therefore expected to be of relatively low intensity. It was difficult to focus the array for Zn due to this low signal intensity. The signal was acquired in the second order to obtain increased intensity (5) (i.e., Zn 213.86 nm in the first order appears at 427.7 nm in the second order which is closer to the wavelength at which the the grating is blazed)

The signal achieved for 10 ppm Zn solution was better than expected, despite the decreased response of the photodiode array for UV light and the inadequate blazing of the grating used (5).

The diffraction grating of the instrument is blazed for 360 nm. This is because it was originally supplied with DC arc and AC spark spectral sources. The quantum efficiency of the photodiode at 213 nm (9) is about 75% of that at 400 nm. Evans (5) estimated that the grating blaze was the main cause for poor detection limits in the UV. He found a detection limit ratio for Zn:Ca of 154:1 as opposed to the 50:1 found by Salin and Horlick (33). In the present study, a 40:1 detection limit ratio is obtained but for zinc signals measured in the second order.

The Cu 324.75 nm emission (shown in Chapter 7 as Figure 38) yielded a signal-to-noise ratio of 90 for a 10 ppm solution using similar conditions and parameters to those used for the previous elements. This again indicates that good signal-to-noise ratios can be achieved provided the emission is strong enough and if adequate light reaches the detector.

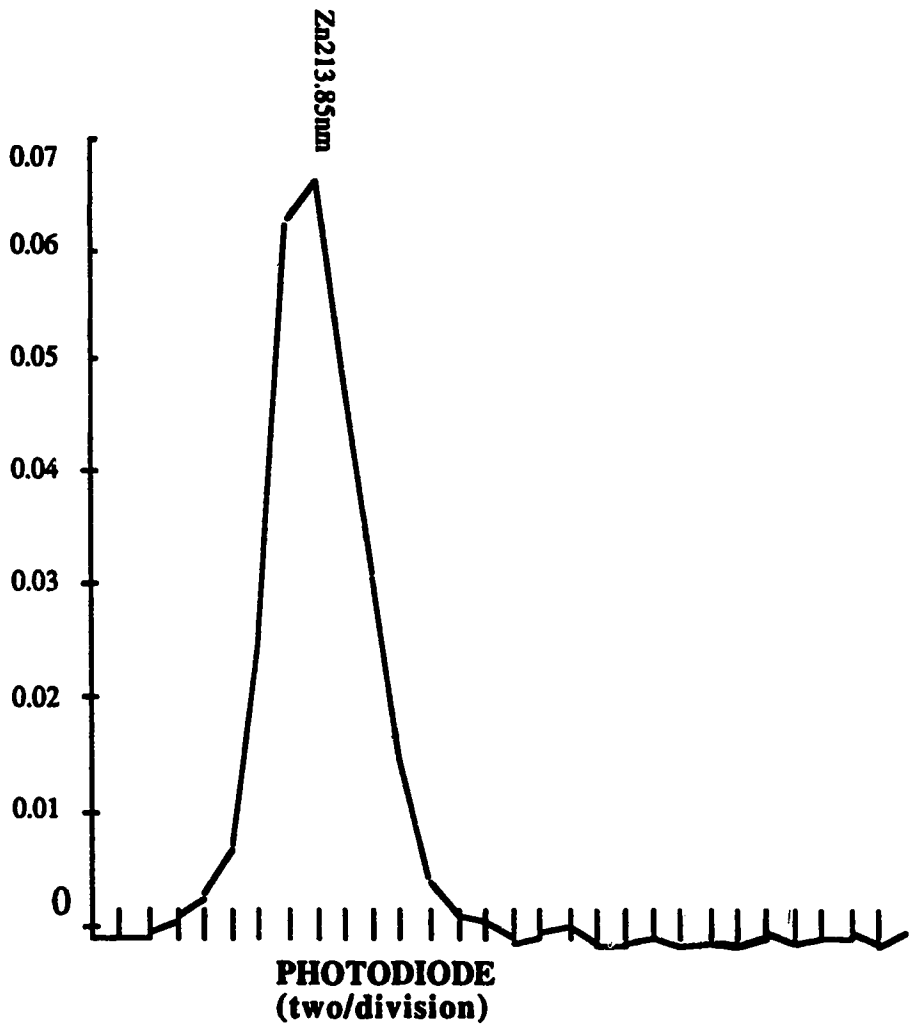


Figure 35 The Zn 213.85nm spectral line, 10ppm solution, 30-sec. integration time. second order spectrum.

6.2.2 Effect of Integration Time and Signal Averaging on Signal-to-Noise Ratios.

The normal procedure for the calculation of signal-to-noise ratios can give a false indication of detection levels in a photodiode array based ICP spectrometer exploiting long integration times. The normal procedure of using 16 to 32 background subtracted replicates of the signal is quite suitable in cases where signal intensities are strong and where integration times can be kept short. The purpose of the large number of replicates is to obtain a better average value of the signal and a more precise measurement of the error (noise). If the system is such that 32 replicates would actually give less precision in either of these measurements, then adhering rigorously to it would be pointless. In the case of the multiple photodiode array spectrometer, long integration times are necessary to offset the twin disadvantages of the photodiode arrays having less sensitivity than photomultiplier tubes and of a Rowland Circle based spectrometer not designed specifically for studies involving the ICP source.

It is also important to note that with this medium resolution spectrometer, the photodiodes do not saturate with ICP background nearly as rapidly as when the more common 0.35 meter Czerny Turner designs are used. The obvious reason for this is that the spectral bandpass, falling on a single photodiode, is much less in higher resolution spectrometers. Using the signal integration time and a similar ICP background as a benchmark, it has been found that the photodiode array based direct reader, is capable of measurements at integration times greater than 100 seconds while, a Czerny Turner based instrument also used in the laboratory causes the array to saturate with ICP background in approximately 10 seconds. Therefore, while 32 separate 10-second integration time measurements can be completed in the

reasonable time of 5.3 minutes, it takes about 16 minutes to perform 32 replicates at a 30-second integration time.

This latter total measurement time, is too long to assume that conditions will remain constant, especially when acquiring low intensity signals. A less biased approach to the calculation of S/N, would be to access instrumental performance over a common measurement time, while during this measurement time taking about 10 replicate measurements.

The data in Table 10, demonstrate that improved signal-to-noise ratios can be achieved using a shorter measurement time. The signal-to-noise ratios for 32 measurements of the signals are given for a 30-second integration time per measurement i.e. a total measurement time of approximately 16 minutes. These are compared to the average signal-to-noise ratio achieved, for a total measurement time of 5.3 minutes.

6.2.3 Detection Limits

The detection limits (Table 11) are calculated by taking as the noise, the standard deviation of 20 background diodes on the same array readout on which the signal itself was recorded. Peak height, was used for signal measurements throughout. The plasma was operated under the same compromise conditions used previously, for the signal-to-noise ratio measurements. An intermediate integration time of 30 seconds was used. The detection limit is taken as that concentration yielding a signal equivalent to twice the standard deviation of the background.

Better detection limits are possible if the system is optimised for each element, but a more realistic analysis of system performance is achieved at the compromise plasma conditions and

operating parameters used. This is the most common approach taken for ICP system evaluation.

SELECTED ELEMENT			DETECTION LIMIT (PPB)
ELEMENT	CONCENT-RATION	WAVE-LENGTH	
MnI	10 ppm	403.08 nm	42
MgII	1 ppm	279.55 nm	2
CaII	100 ppb	393.36 nm	2.5
CuI	10 ppm	324.75 nm	16.6
ZnI	10 ppm	213.85 nm	144

TABLE 11 Detection Limits of Selected Elements

6.2.4 Decreasing Detection Levels using Long Integration Times.

As already mentioned, very little data are available in the ICP literature, on the application of photodiode arrays at integration times longer than about 10-seconds. Success at longer integration times, depends on the long-term noise characteristics of both the ICP source and of the photodiode array detector itself. The latter is related to the stability of the photodiode array cooling system while the former depends on many factors effecting analyte nebulisation, desolvation and excitation in the ICP, in particular, the nebuliser system used.

Using a 10 ppm Mn solution, the 403.08 nm line of the Mn I triplet was used to evaluate the detection limit at various integration times. The results are tabulated in Table 12. The detection limit is taken as the concentration which produces a signal equivalent to twice the standard deviation of the background. This table indicates that by the use of a longer

integration time, a stable signal can still be achieved and that detection limits can be improved.

INTEGRATION TIME	DETECTION LIMIT.
50 Seconds	120 ppb
100 Seconds	70 ppb
150 Seconds	41 ppb

TABLE 12 Detection Limits for Zinc at 213.85 nm as a Function of Integration Times

Better detection limits for Mn at 403.08 nm were achieved using longer integration times and the improvement was almost directly proportional to the increase in integration time. This occurs because the system is readout noise limited for weak signals or close to the detection limit. Readout noise does not increase linearly with integration time but the integrated analyte signal does (Figure 31). Hence, the signal simply accumulates linearly, with integration time and the detection limits improve proportionally. All of the standard deviations for the above detection limit data are calculated for the photodiode having highest analyte signal intensity. Signal averaging, diminishes the effect of readout and dark current shot noise, both of which are random.

In summary, signal-to-noise ratio (S/N) is a basic figure of merit for a system, indicative of the precision. It is equivalent to the reciprocal of the relative standard deviation (rsd) and hence a S/N of 100 is equal to a 1% rsd. Thus with S/Ns ranging from 20 to 200 the measurement precision is ranging from 5% to 0.5%. It is also important to note, as has been observed in these experiments that the time required to evaluate S/Ns can adversely affect the final result. Therefore better S/Ns result when a shorter evaluation time is used.

CHAPTER 7

BACKGROUND AND SPECTRAL INTERFERENCE CORRECTIONS

7.1. Introduction

One of the major disadvantages of the classic PMT-based direct reading spectrometer is the problem of background radiation. Background radiation can arise from the spectroscopic system, introduced in the form of stray light, overlapping orders and detector background or it may be a characteristic of the source itself, e.g., a spectral line overlap or background continuum.

7.2 Instrument Generated Background.

There are three major forms of instrument introduced background in this spectrometric detection system.
These are:

(1) Stray light.
(2) Overlapping orders.
(3) Photodiode array or detector system background noise.

Stray light is any unwanted radiation reaching the detector due to defects in the diffraction grating or in other parts of the instrument. With ruled gratings, the most serious manifestations of stray light are the occurrence of Rowland and Lyman ghosts. Rowland ghosts are secondary images spaced symmetrically about the parent line (39). They are due to imperfections in the lead screw which is used to advance the diamond cutting tip when the master grating is being made on a ruling machine. The spacing of the ghosts is given by (5,53);

$$\lambda' = \lambda\left(1 + \frac{m'}{mn}\right)$$

where λ is the wavelength of the parent line, λ' is the wavelength of the ghost of order m', m is the spectral order of the parent line and n is the number of lines ruled per turn of the ruling engine. For an engine ruling 500 lines for each full turn of the lead screw and a strong signal at 500nm in the first order, ghosts at 1nm intervals from 500nm could be expected.

Several of these ghosts were observed by Evans (5) using this instrument and their intensities relative to the parent lines were quantified. He found parent to ghost intensity ratios of 133. This is extremely poor since manufacturers of ruled gratings often claim parent to ghost intensity ratios of 1000 to 10,000 (39). If a holographic grating was used this problem would be eliminated since these are ghost free.

This interference problem caused by Rowland ghosts, would have to be considered when selecting the best spectral lines for analysis. For example, Evans (5) chose the 394.4 nm line for aluminium analysis in the presence of a matrix high in calcium. This was because the first order ghost of the Ca 396.8 nm line was very close to the more sensitive Al 396.2 nm line.

Lyman ghosts (39) are other secondary images caused by external periodic vibrations during the grating ruling process. These appear as images a large distance away from the spectral line. No Lyman ghosts have been identified, with the present grating but nevertheless, they may be present, but difficult to identify.

Near and far scatter from the surface of the grating and appearing in the region of 5 nm and greater than 5 nm from the parent lines respectively, may also occur. Near scatter is caused by random disturbances of the ruling machine, while far scatter arises from minor imperfections, in the grooves of the gratings. These are also minimized by the use of holographically recorded gratings.

Also contributing to general stray light, is the reflection of undiffracted and diffracted light from the interior surfaces of the light proof box. Entrance slits and the photodiode array window in the exit focal plane can also contribute to this scatter. A finely divided coating of ice forms on the ends of the array cooling bars and may reflect light falling on it. This and other parts of the photodiode assembly, which is in the focal plane of the Rowland circle, may cause light to be reflected and lead to stray light elsewhere, on the focal plane. The data acquisition units and the circuitry inside the light proof box, behind the focal plane, could cause light scatter but this would be less serious than the other sources, since it would be unfocussed. It is possible to eliminate most of this type of scatter by covering the circuitry and data acquisition units with black velvet.

The grating produces multiple orders of spectral lines and this feature can lead to significant interferences, if care is not taken. Wavelength selective filters, are often used to differentiate between the major spectral orders. Higher orders are often useful in solving detector spacing problems. With this spectrometer, wavelengths in the 200 nm region, showed much better detection limits, when viewed in the second order.

An additional background arises when the photodiode array is used as a detector. The photodiode as already mentioned, operates in a charge storage mode. The charge on the photodiode

can be reduced by either light intensity, which is the desired discharge mechanism or by heat, which is undesirable. The photodiode array is cooled to about -20°C to reduce this heat induced discharge. Nevertheless, some discharge by this mechanism is inevitable and therefore contributes, to the overall background signal observed. Since every photodiode has a slightly different sensitivity to heat, the background across the array may be uneven. The unevenness of this background is further enhanced by an "odd-even pattern" which results when the odd and even photodiodes are "processed" by separate sets of analogue circuitry. Another factor contributing to this unevenness of background is non equal cooling across the array (5), this is a feature exhibited by some of the present photodiode array assemblies.

It is fortunate however, that all the background originating on the array itself can be removed by subtraction of a background spectrum, obtained in the dark for the same integration time as the signal spectrum.

7.3 Source Generated Spectral and Background Interferences.

Source generated interferences in the ICP have presented serious problems in multielement analysis. These interferences can arise from the argon support gas, entrained air or concomitants introduced in the sample matrix. Molecular species, the majority of which are CN, NO, NH and OH, exist in the plasma and undergo vibrational and rotational transitions, as well as electronic ones. These transitions may give a fine structure to the spectral background, therefore making background corrections difficult.

If organic compounds are avoided there will be no problem from CN bands. Likewise, if the plasma coolant gas flow rate is

high enough then air entrainment is less and the NO and NH bands do not create serious problems.

Hydroxyl bands arise from the water used as nebulization solution and therefore are not easily eliminated. Over 296 hydroxyl features, some of which are major interferences (41), have been identified in the spectral range from 281.0 nm to 324.5 nm. Argon lines from the plasma gas itself also cause interference (42) and, due to their variable intensities from scan to scan, they may be quite difficult to subtract out completely.
Certain metal ions generate recombination continua by radiative recombination with the high concentration of electrons in the argon plasma. Strong continua are formed by magnesium, calcium and aluminium. These bands alter spectral baselines below 250, 302, and 220 nm, respectively (43).

These source generated spectral interferences can be subdivided into three main categories:

(a) Direct spectral overlaps
(b) Partial overlaps
(c) Continuum

In case (a) the spectral line of another element overlies the analyte line. These wavelengths are too close to resolve even with high resolution instruments.

In case (b) there is partial, or wing overlap by the line of an interfering element. In this situation, unlike case (a), improved resolution of the spectrometer may eliminate or significantly reduce the interference.

In case (c) a background continuum underlies the line. This interfering signal is added to both the background and the analyte signal. Often the continuum may have some fine structure, which

may render incorrect, measurements of background taken at two points on either side of the peak. This is the procedure used by instruments employing off-peak correction methods.

There is a general consensus in the literature that the numerical uncertainty in our knowledge of interference correction factors is a limiting feature in ICP analysis. This is especially true for trace element work on samples having complicated matrices e.g. geological materials (44).

Berman et al (45), in a trace element study on marine sediments, concluded that the main problem for ICP was spectral interference. Mermet and Trassy (46) highlighted the large number of lines excited in the plasma and suggested that spectral interference effects would be increased by the effect of line broadening (due to Doppler and collisional broadening).

Previously, problems with spectral overlaps were compounded due to the incomplete knowledge of spectral lines emitted by the plasma. The MIT tables (47) and the NBS wavelength tables are based on intensities from arc and spark spectral sources and cannot adequately give an indication of the interferences found in the ICP. Some interfering lines of low intensity are not even recorded in these tables. The situation is now greatly improved by the work of several authors (48).

Serious spectral interferences can be avoided by choosing an alternative line. This is possible when the major matrix elements are known but for some elements, the choice of alternative lines is limited and some interference has to be tolerated and corrections made.

When the interference is less than 10% inter-element correction factors are usefully applied. For interferences greater than 10% the errors on the corrections become too great (44).

The importance of considering spectral interference is seen in the line selection available for zinc determinations. Boumans (49) records three lines for zinc having detection limits below 10 ppb, Zn 213.85, Zn 202.55 and Zn 206.20 nm. The Zn 213.85 nm line has a direct spectral interference from copper and nickel. The Zn 202.55 nm line is interfered with by magnesium (a major constituent in many rocks). The Zn 206.20 nm line has close to it, a chromium line at 206.15 nm. Aluminium which generates a recombination continuum from 190-220 nm will interfere with all these lines.

Partial line overlaps are sometimes more serious since small changes in the profile setting of the spectrometer, can have a large effect on the magnitude of the inter-element correction factor that is used. Therefore, day-to-day changes in interelement interferences can occur even with temperature stabilized entrance slits.

Attempts to reduce the inaccuracies in intensity measurements caused by spectral interferences are numerous. Botto (50) attempted to improve the accuracy of correction by working at a constant Cu atom line/Mn ion line intensity ratio in a hope to accurately reproduce plasma conditions. Using a dual channel polychromator and an echelle he succeeded in significantly reducing interference for the determination of As, Be, Cd, Mo, Pb, Se, Tl. An attempt to eliminate spectral interferences altogether was made by Hieftje and Downey (51). This was done by applying selective spectral line modulation to the analyte line. The main limitation of this technique is that it can only be used for atom lines.

7.4 Line Broadening Phenomena and Spectral Corrections

For the photodiode array direct reader with medium resolution, any discussion on the correction of spectral interferences, would be incomplete if proper attention is not given to the resolving power of the instrument.

It is first necessary to examine the ICP source and consider the resolution requirements as dictated by actual line widths and shapes produced.

The width and profile of a line from the ICP source is governed by the well known phenomena (52) listed below:

(1) Natural broadening.
(2) Doppler broadening.
(3) Pressure broadening.
    1. Collisional.
    2. Stark profile.

All the above, can be grouped into two categories, based on the line shapes produced. Types 1 and 3 produce a Lorenzian profile with its resulting broad wings and type 2 produces a Gaussian profile with the only important effect occuring in peak width.

The combination of the Gaussian and Lorenzian profiles are often referred to as the Voigt Profile.

Natural broadening is explained from considerations of Quantum Theory, and application of the Heisenberg Uncertainty Principle. It can be considered from the point of view of the finite lifetime of an energy state, with transitions occuring from states

of short lifetimes, giving broad spectral lines and those from states having long lifetimes, giving narrow spectral lines. Its contribution to the spectral line width is of the order of 1.2 X 10^{-5}Å. So it can be ignored in medium resolution ICP spectrometers.

Doppler broadening leads to half intensity line widths of the order of 0.001 nm to 0.02 nm. It is more serious for lower atomic number elements.

Highly ionized elements in the plasma e.g. the alkalis, Ca and Mg are severely collisionally broadened. Collisional broadening leads to half intensity widths of around 0.03 nm (Ca II 393.366 nm line) but due to its Lorenzian profile, this type of broadening is much more serious on the wings of a line. For Ca II 393.366 nm in the ICP, the wings of the line can spread over 1 nm, from the central maximum.

The wings of the CaII 396.8 nm line interfere with the Al 396.2 nm line (5). This line has wings which spread about 2 nm from the line center, a phenomena which cannot be ignored for aluminium determinations carried out in the presence of calcium.

The plasma environment in which the positively charged ions exist is rich in electrons, therefore, the resulting intense and variable electric fields created perturb the energy levels which are undergoing electronic transitions (52). These outer energy levels, therefore experience, what is commonly termed the linear Stark effect. The linear Stark effect appears as severe Lorenzian type broadening of the spectral line.

When spectral interference is caused by fundamentally broad lines, increased resolving power is of little use and the only

solution lies in spectral stripping or by computerized background removal.

Taking all these source generated effects into account, it is quite obvious that increasing the resolving power of the spectrometer, will help overcome only some of the spectral overlap interference effects generated by the source.

The grating on the present Rowland circle based spectrometer, has 74,000 lines ruled on it, thus giving a theoretical resolvable line interval of from 0.0027 nm at 200 nm, to 0.01013 nm at 760 nm.

A single photodiode samples a 13 μm band of the focal plane fully and provides partial sampling of a 6 μm width on either side of this. Overall, some intensity is sampled over a total width of 25 μm. The spectrometer has a reciprocal dispersion of 0.565 nm/mm directly in front of the grating and 0.540 nm/mm at an angle of dispersion of 17°. Therefore the spectrum is sampled (assuming a sensor width of 25 μm) by the photodiodes at from 0.0135 to 0.0141 nm intervals. For better resolution, the slit width would have to be reduced and the photodiode width made smaller. This would of course, reduce sensitivity, due to the reduced light throughput and decreased sensor area.

7.5 Background and Spectral Interference Correction Methods in Modern ICP Spectrometers.

Current background correction methods used with PMT based direct readers can be categorised as either on-peak or off-peak methods. Slew scanning approaches are also becoming more important.

With on-peak correction an extensive survey must be made of all concomitants in the sample. The response of each of the channels to the concomitants is determined and correction factors applied. The method requires that separate channels are available for each of the concomitants, so that they may be quantified during the analysis. Using a working curve, the enhancement in signal, caused by the concomitant in the test channel, can be removed. It is necessary therefore, to specify the probable concomitant present in analyte samples when purchasing the instrument. The manufacturer then ensures that the necessary analyte and concomitant channels, are included in the focal plane.

Hence this procedure can provide quite accurate results if the sample matrices are well defined and if the entrance slit and all exit slits are stabilised thermostatically, relative to the diffraction grating. Thermostatic control, is necessary to prevent shifting of the line profile and thus loss of alignment. The main disadvantage of the technique is that variable or unknown sample matrices cannot be tolerated and that the system lacks flexibility.

The off-peak method, involves determining the background at both sides of the analyte line. This is accomplished by either physically moving the entrance slit or by using a quartz refractor plate. The quartz refractor plate is placed just behind the entrance slit of the direct reader.

On moving the entrance slit, the typical spectral bandpass of 0.0265 nm falling on a 50 μm wide exit slit would be shifted ±0.034 nm (40) from the spectral line on all direct reader channels and a background measurement taken. The method is subject to error since the same location of the ICP is no longer being viewed (imaged).

The quartz refractor plate accomplishes the same spectral shifting effect, except by an optical method, as that resulting from the physical movement of the entrance slit. It may introduce an added error due to changes in the reflectivity of the plate surface, as the angle is changed.

Both shifting methods are subject to errors due to the high precision in movement required and due to spectral interferences with the analyte line, if present. Since both of these methods require separate measurements of signal intensity, the precision of data is therefore highly susceptible, to instabilities in the ICP source. It is also impossible therefore to use these methods for analysis involving transient signals since these signals, would have an inherent, changing or dynamic background.

With slew scanning spectrometers spectral lines are detected sequentially. The rotation of the grating is fast (slew) between spectral lines and then the profile of the line is scanned slowly.

The technique offers some unique potential and provides flexibility for analyses involving of a variety of matrices. It is nevertheless, a sequential and not a simultaneous technique, and as such, it is dependent on the analyte signal remaining constant. Finally, photodiode array direct readers provide simultaneous measurement across a spectral window, therefore allowing accurate measurement of the complete spectral background. This provides for a variety of unique signal correction approaches which are discussed in the following section of this chapter.

7.6 Background and Spectral Interference Correction Features of a Photodiode Array Direct Reading Spectrometer.

In the focal plane of the direct reader, the photodiode array acquires signals simultaneously on its 128 photodiodes. These 128 photodiodes form a 1.7- nm spectral window. This capability offers distinct advantages over the off-peak and slew scanning approaches for background correction both of which have no simultaneous capability. Compared to on-peak correction methods, the photodiode array provides a sufficient spectral window to allow simultaneous measurement of the background surrounding a spectral line. This eliminates the necessity for extra channels except in situations where direct spectral overlaps occur, in which case, the interfering concomitant must be quantified using an additional PDA channel. In most cases, direct spectral overlaps can be avoided by choosing alternate spectral lines, but even if this is not possible, the present moveable multiple photodiode array windows can be configured to determine the concomitant on a PDA channel other than that of the analyte channel.

This approach therefore, returns some flexibility to the direct reader enabling analysis of a variety of sample matrices which cannot be analyzed accurately, using a direct reader equipped with on-peak background correction capability.

With the photodiode array it is possible to display and examine graphically, both the signal and the background in its vicinity. Interfering spectral features can be identified and taken into consideration when the background correction is applied. All raw data can be stored and the appropriate background correction made later.

It is possible to apply background correction in a variety of different ways using the photodiode array. These are:

(1) *Subtraction of a spectrum taken in the dark (dark spectrum) or the spectrum of a blank solution (blank spectrum) from the analyte spectrum.*

(2) *Blank spectrum subtraction in addition to a dynamic background correction* i.e., subtraction of a blank spectrum accompanied by further corrections to the analyte signal by correction with background signals, generated on the the baseline photodiodes of the analyte spectrum.

(3) *Use a dynamic background correction factor only*, i.e., subtraction of background signals recorded simultaneously with the analyte signal on the baseline photodiodes. This approach is most successful when the background in the vicinity of the spectral line is flat.

(4) *Direct subtraction of spectral interferences.* This is a technique unique to photodiode array direct readers. Two photodiode array windows are used, one optimised for measurement of analyte intensities, while the other is optimized for measurement of intensities of a suitable spectral line of the interferent. The ratio of signals generated by the interferent in both channels is determined. Once this ratio is known, then a single measurement on the channel optimized for measurement of the interfering element is all that is required (during analysis) in order to calculate an entire interference spectrum (simulated interference spectrum) for the analyte channel. This simulated interference spectrum can then be subtracted from the spectrally overlapped analyte spectrum.

With the first method (Method 1), the array background, odd-even pattern and ICP background can theoretically, be totally removed.

Using Method 2, unwanted signal, already detailed for Method 1 above is removed. In addition, stray light introduced by the concomitant should be eliminated and any errors caused by odd-even pattern remaining after the initial background subtraction can be removed. It is usually observed that some odd-even pattern remains after blank spectrum subtraction. This is possibly due to drift or slight non-linearities in the video signal conditioning circuitry at various signal levels. The dynamic subtraction, theoretically should eliminate any of this low frequency flicker (drift) noise adversely affecting direct background subtraction. For dynamic corrections to be applied most successfully, odd and even photodiodes should be treated as separate populations.

Method 3 should yield good results provided a flat background, not affected by concomitants in the analyte matrix, is obtained. It is used without the subtraction of a blank spectrum and therefore, by eliminating a measurement with its associated drift, will increase the precision. This is especially true where long integration times are used. In these circumstances, the combination of low signals and drift render blank spectrum subtraction an imprecise correction technique.

The various features of these methods of spectral correction, are now discussed and examined using data acquired with the multiple processor PDA direct reader.

Signal spectra were acquired for aqueous solutions of 10 ppm zinc, manganese and copper. Background spectra are

generated by the aspiration of a water blank solution. The background spectrum is captured by the same photodiode array window as that which previously recorded the analyte spectrum. The same integration times and ICP operating conditions are used for recording both analyte and blank (background) spectra. The blank spectra are subsequently subtracted from the analyte spectra by the computer. The resulting background subtracted spectra, together with, the original anlyte spectra, are overlayed, on the same graph (Figures 36-38).

The capability of overlaying spectra and displaying them both graphically and in hard-copy is achieved conveniently, using the spreadsheet features of the spectral processing package, integrated into the overall software of the present system.

The ability to display spectra in this way and to expand areas of a spectrum in order to examine more closely spectral features, assists greatly in the examination of spectral information.

For the Zn 213.85-nm line the signals on the relevant number of diodes (30 diodes), in the vicinity of the zinc line were selected and the spectrum displayed. The most intense signals are automatically expanded to full scale (Figure 36). The raw signal spectrum (signal + background) appears very noisy with respect to the wavelength axis. When the background spectrum is subtracted, it is clear that the poor quality raw spectrum, is mainly attributable (since it can be subtracted out) to the odd-even pattern, brought about by the separate processing of odd and even photodiodes, by the photodiode array electronics.

The manganese spectrum (Figure 37), displayed in a manner similar to that for zinc (Figure 36) shows that this photodiode array has a less distinct odd-even pattern. This figure clearly

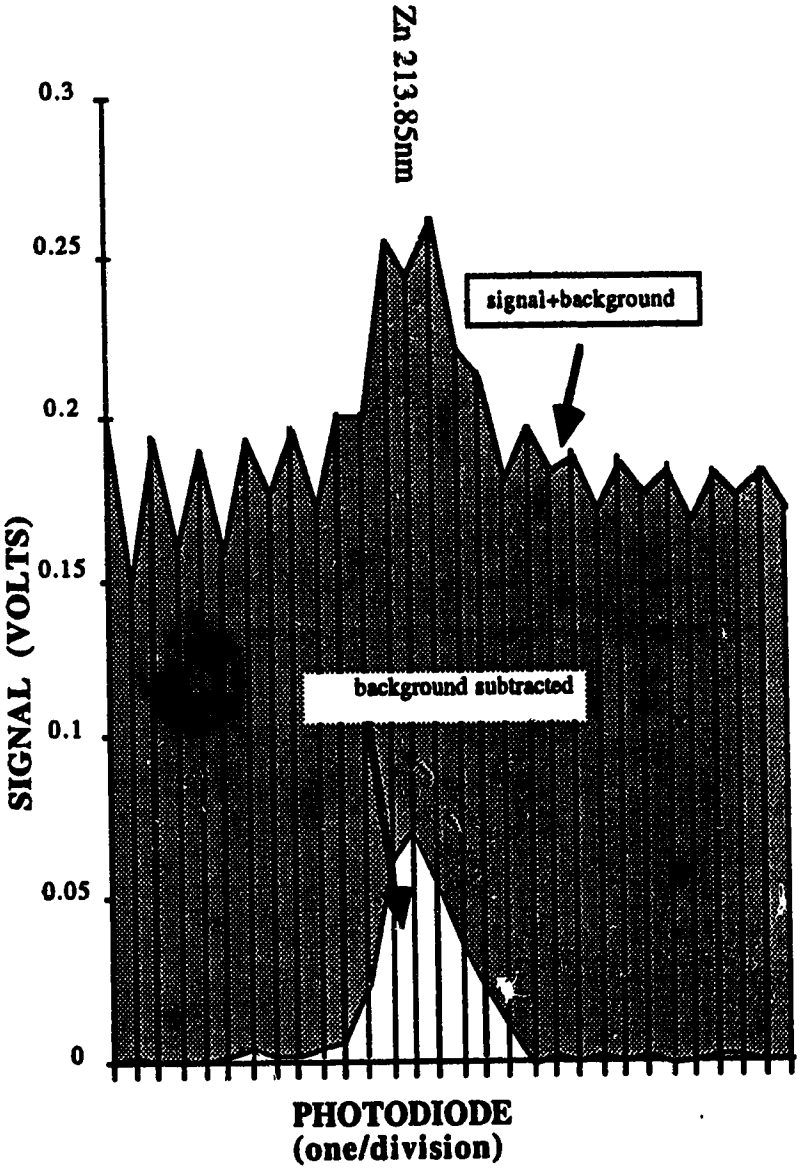


Figure 36 Raw and water background subtracted spectrum of 10ppm Zinc, 30-sec. integration time.

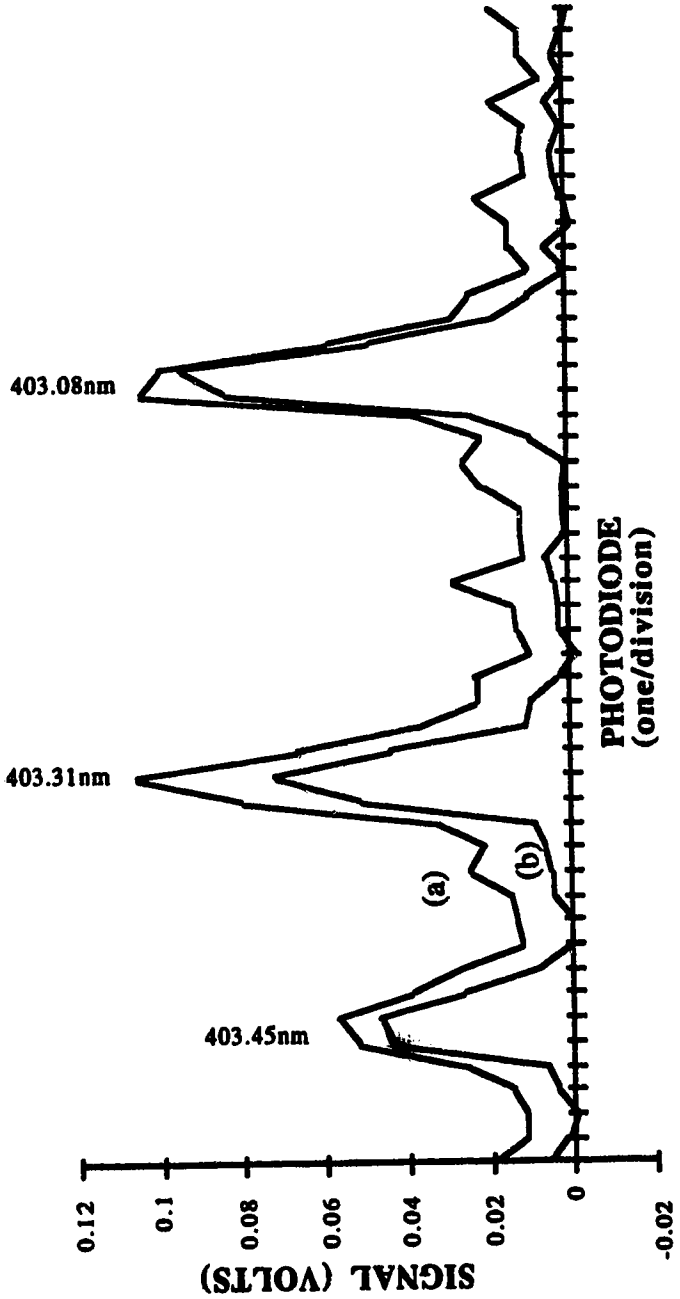


Figure 37 (a) Raw signal spectrum of 10ppm Manganese.
(b) Background subtracted spectrum of 10ppm Manganese,
10-sec. integration time.

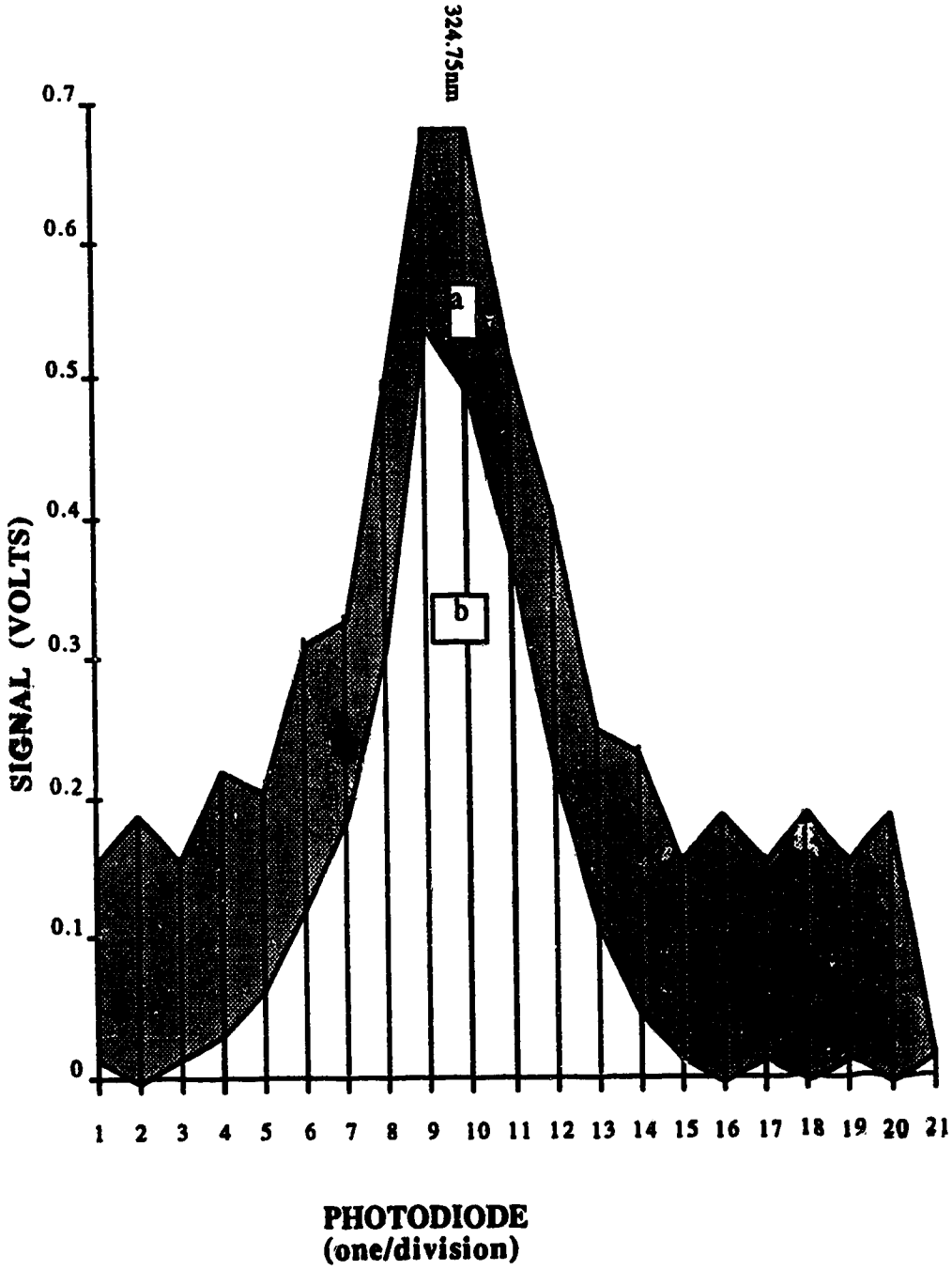


Figure 38 (a) Raw signal spectrum of 10ppm Copper.
(b) Background subtracted spectrum of 10ppm Copper, 10-sec. integration time.

highlights, the removal of a number of unassigned spectral features by the background subtraction technique. These features are probably attributable to water. The copper spectrum (Figure 38) in the vicinity of the 324 nm spectral emission is expanded and displayed. For detailed examination of the copper emission, 20 photodiodes are selected and their signals displayed. This spectrum highlights the serious odd-even pattern which is feature of spectra generated with this photodiode array. This figure also demonstrates that the odd-even pattern is not always totally removed by the subtraction of a background spectrum. This is especially true for arrays with a serious odd-even pattern.

Overall, these three figures (Figures 36-38) indicate that background subtraction can to a great extent, remove any constant background level (i.e., dark current and spectral continuum) as well as the fixed pattern PDA background signal. Total correction of odd-even effects may not be achieved.

The precision achieved when correction methods 2 and 3 are used to remove interferences is compared by measuring the signals generated by aqueous solutions of manganese for various integration times. The Mn 403.06 nm (Figure 37) line was chosen and corrected peak heights measured. The precision obtained for both methods averaged about rsd (relative standard deviation) 1% for integration times less than 30 seconds. For the dynamic correction (refers to corrections made to the signal using baseline data on the analyte spectrum), the average signal of seven baseline photodiodes was used to determine correction factors.

For very long integration times (>30seconds), it was found that the overall precision for the determination of corrected peak heights, was greater, when separate background spectra were not subtracted i.e. when Method 3 or dynamic correction alone was used. Hence the average rsd of 3.1% was achieved using Method 3

for long integration times. The best overall precision obtainable using Method 2 for long integration times was rsd 6.5%.

Therefore there is a tendency to greater imprecision, in measurements involving spectra acquired at longer integration times. This imprecision is probably due to drift. It can also be concluded that a dynamic correction, when applied on its own, yields more precise results. There is also drift during the measurement time for the background spectrum and therefore subtraction of a separately recorded background spectrum results in more imprecision. The success of dynamic correction indicates that the background, for both the analyte signal and baseline photodiodes drifts to the same extent and in the same direction.

One of the most important features of the ICP, as a source of spectrochemical information, is that it is optically thin and as a consequence, it can yield linear calibration curves for concentration vs. signal intensity over several orders of magnitude in concentration. To analytical spectroscopists, the ICP is therefore considered to have a large linear dynamic range. To exploit this feature fully, ICP spectrometers must be capable of measuring signals generated by the ICP source for a wide range of analyte concentrations. The multiple photodiode array direct reader exploits the dynamic range of the ICP by controlling the signal integration time of the photodiodes. Therefore, short integration times are used to acquire intense signals (high concentrations of analyte) while long integration times are used for the weaker signals (low concentrations of analyte).

Manganese was again chosen as the analyte for demonstration of this feature of the instrument. The intensity of the MnI 403.08 nm spectral line was chosen for measurements. Aqueous manganese solutions comprising of 0.1, 1.0, 10, 100, and 1000 ppm manganese were prepared. The integration time was

changed under software control to allow the signal to match the dynamic range of the analog-to-digital converter. Since a range of integration times, some greater than 100 seconds were used the dynamic background correction technique i.e. Method 3 was used for background corrections. It has previously been demonstrated that better precision is achieved if this background correction technique is used.

The average signal on ten baseline photodiodes in close proximity to the Mn 403.08 nm line is used as the background. These baseline photodiodes are also chosen so that they have the same odd-even pattern as the photodiode used to measure the Mn 403.08 nm line. Even though an error probably arises since we do not take into account, the fact that each photodiode has a slightly different sensitivity to dark current noise this still accounts for less imprecision than the process of subtracting separate background spectra for each integration time used.

Using this intra-spectral (dynamic) correction technique, data demonstrating the capability of this photodiode array based system to exploit the excellent dynamic range of the ICP are tabulated (Table 13) and plotted (Figure 39). The calibration curve is found to be remarkably linear with a correlation coefficient approaching unity.

In section 7.3 of this chapter, source generated spectral interferences were highlighted as the most problematic interferences in ICP spectrometry. As outlined previously, these interferences arise as a direct result of the high temperature of the ICP source which excites a large number of atomic energy levels. It presents a significant problem, especially for samples whose matrices contain a large variable concentration of interferent, e.g., geological samples. Many approaches to dealing with the problem have been attempted (see section 7.3) but some

are limited in scope while others are very inaccurate. The most successful of these approaches involve the use of two channels, one of which is used to measure the analyte signal while the other channel quantifies the interferent. Correction factors, based on this measurement of the interferent are then applied to the analyte signals. Many factors render this method either imprecise, inflexible or impractical;

•Imprecise, because there is little or no simultaneous spectral background information accessible at either channel. Slew scanning instruments go some way towards acquiring this information, even though they cannot acquire it simultaneously on each channel.

•The method is inflexible and impractical for most conventional direct readers since the positioning and alignment of channels to quantify the interferent would require the help of the manufacturer. Again, a slew scanning instrument would be less constrained but the lack of simultaneous capability would limit its usefulness, especially when transient signals must be quantified.

CONCENTRATION (ppm)	SIGNAL (Volts)
1000	6.95
100	0.717
10	0.0715
1	0.00715
0.1	0.000716

TABLE 13. Dynamic Range Data for Manganese at 403.08 nm
(Dynamic background correction technique was used to correct for peak heights. Data is normalised to a 10 sec integration time)

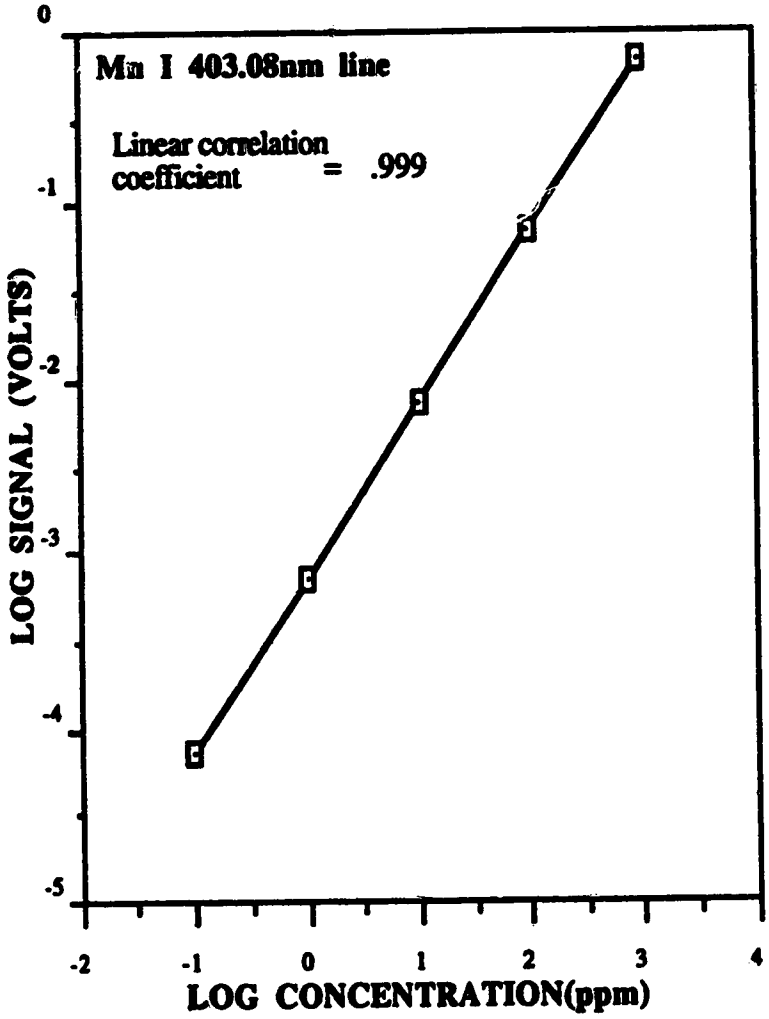


Figure 39 Calibration plot for Manganese demonstrating the dynamic range achievable with the PDA direct reader.

The PDA direct reading spectrometer is flexible by virtue of its moveable detectors which can be positioned as desired, along the Rowland circle. It has the capability of acquiring analyte signal and background on several channels simultaneously.

In the following experiment, this capability of the PDA direct reader will be examined. An attempt will be made to correct for source generated, direct spectral overlaps. Two photodiode arrays are used, one to estimate the intensity of the interfering concomitant, while the other senses and quantifies the spectral line intensity of the analyte and the background in its vicinity. The interference due to the concomitant is estimated and subtracted from the measured analyte signal.

The direct spectral overlap examined here results when traces of zinc are determined in the presence of high concentrations of Copper. The Zinc line at 213.853 nm is overlapped by the copper line at 213.856 nm.

One photodiode array is positioned to measure the copper emission at 324.75 nm (Figure 38). This is a strong copper emission which is essentially free from spectral interference. A second photodiode array is used to measure the 213.85 nm line of zinc in the second order, at 427.71 nm (Figure 40). Figure 40 highlights the presence of intense Argon emissions from the carrier gas at 426.6 and 427.2 nm. Due to their intensity, these emissions tend to saturate the array. Variations in the intensity of these argon lines from scan to scan, render it impossible to completely remove them by subtraction of a blank spectrum. This causes the errors observed in the background subtracted spectra. These errors are especially noticeable for the photodiodes sensing the wings of these emissions (Figure 40), where it is to be

expected that changes in plasma conditions from scan to scan, will cause the greatest emission intensity changes.

It is useful to to keep in mind the portion of the spectral window we are viewing since this can easily be increased or reduced to facilitate examination of spectral information of greatest interest. For Figure 40 the bandpass per photodiode is 0.013 nm, therefore, the spectral window being viewed over the 100 photodiodes selected, is 1.3 nm. In the following discussion, the zinc analyte signal and the effect of copper interference (several of whose minor emissions appear on top of or close to the zinc signal) on this signal is examined. Therefore, the portion of the spectrum to the left of the Ar 427.2 nm line is expanded for closer examination (Figure 41). This expanded spectrum highlights very clearly, the Zn 213.853 nm emission (in the 2nd order) and the direct overlap on the emission by the Cu 213.856 nm (also in the 2nd order) spectral line. Also visible is a weak copper line at 427.51 nm and an even weaker copper line (which is not listed in the literature) at 427.64 nm.

A 10 ppm Zn solution with concentrations of copper as matrix ranging from 0 to 5000 ppm was used to investigate the effect of increasing concomitant (copper) concentration on the zinc signal.

All directly interfering lines and those emissions appearing in close proximity to the Zn213.85 nm emission appear to increase linearly with copper concentration (Figure 41).

Concentration (of interferent) dependent line broadening phenomena cause the wings of spectral lines to broaden onto the baseline of the spectrum. This baseline, if used in peak intensity calculations can lead to curvature in the analytical calibration curves. This additional background phenomena can also be

observed when zinc is determined in the presence of a "variable matrix" of copper. Diodes in the vicinity of the argon 427.2 nm line (diodes 29-35 of Figure 41) which is broadened with increasing copper (matrix) concentration would therefore provide an unsuitable choice for baseline in peak correction calculations. Contributing to the uneven background in the vicinity of the argon 427.2 nm emission, is another direct spectral overlap by a weak copper line with the argon 427.2 nm line. To the left of the liner (photodiodes 1-4 of Figure 41), the background is less effected by changing concomitant concentration and therefore provides a much better choice to use as a baseline. Once again, the the acquisition and presentation of extensive background information in the vicinity of the analyte signal by this PDA direct reader, proves invaluable in choosing the best approach to these difficult spectral correction problems.

It is obvious that the increase in background on these water subtracted spectra, is not caused by general stray light, since changes in intensity of the background, across the spectral window are observable. General stray light would tend to be distributed evenly across the entire spectral window

In these spectra, there is an obvious direct spectral overlap by copper matrix on the zinc analyte signal and variable wing overlaps due to broadening effects. Both interferences must be taken into account when attempting corrections to the zinc signal for spectral overlaps.

In Figure 42 (a 0.27 nm window, close to the zinc 213.85 nm line) the overlapped zinc and copper interference spectra, show clearly the effect of a 5000 ppm Cu matrix, in the vicinity of the spectrum obtained for 10 ppm Zn at the same integration time. The spectra for the zinc and copper solutions were acquired separately and a water blank spectrum was subtracted from each.

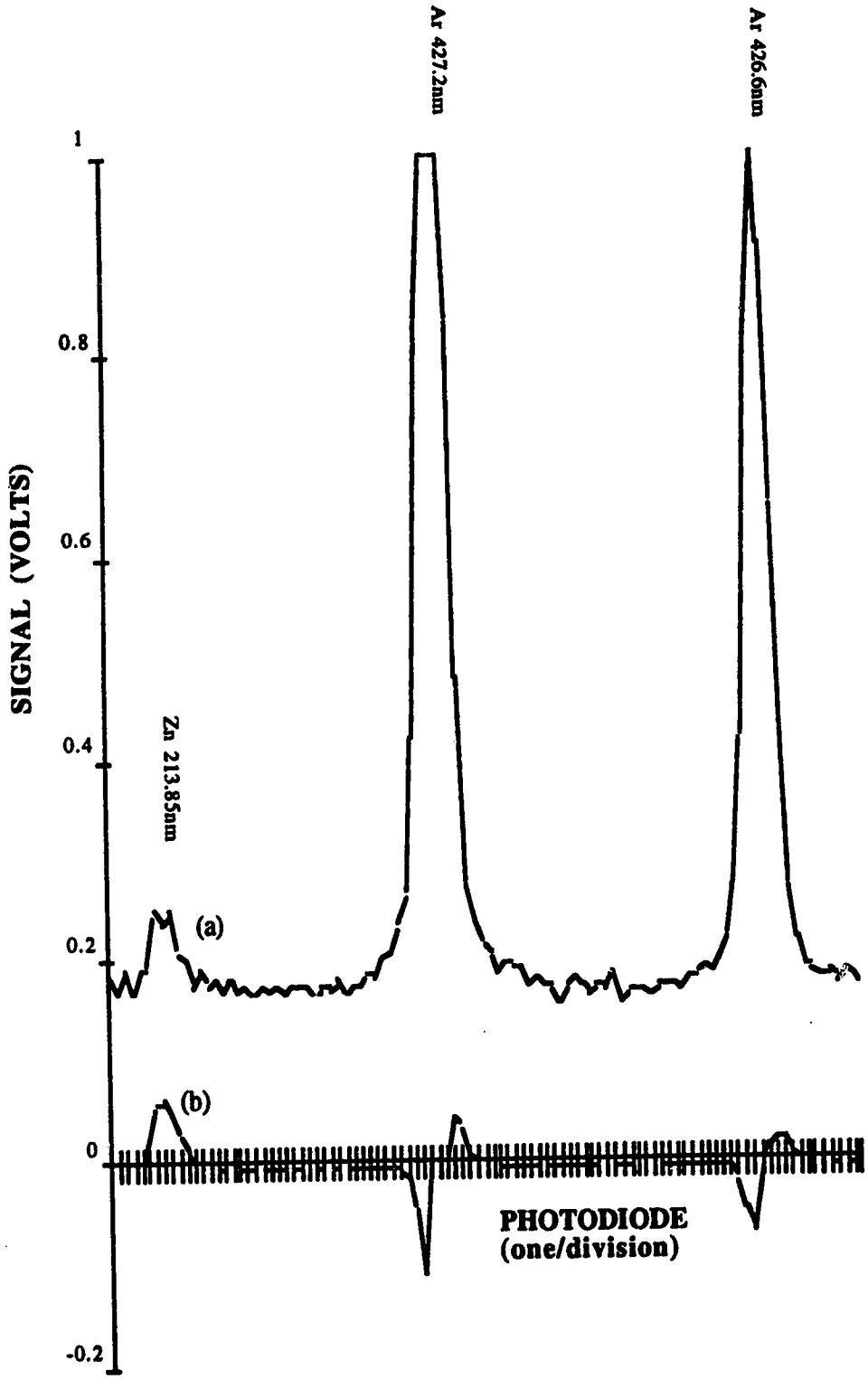


Figure 40 Spectrum of 10ppmZn and the adjacent Argon emissions a) before background subtraction and (b) after the water background is subtracted

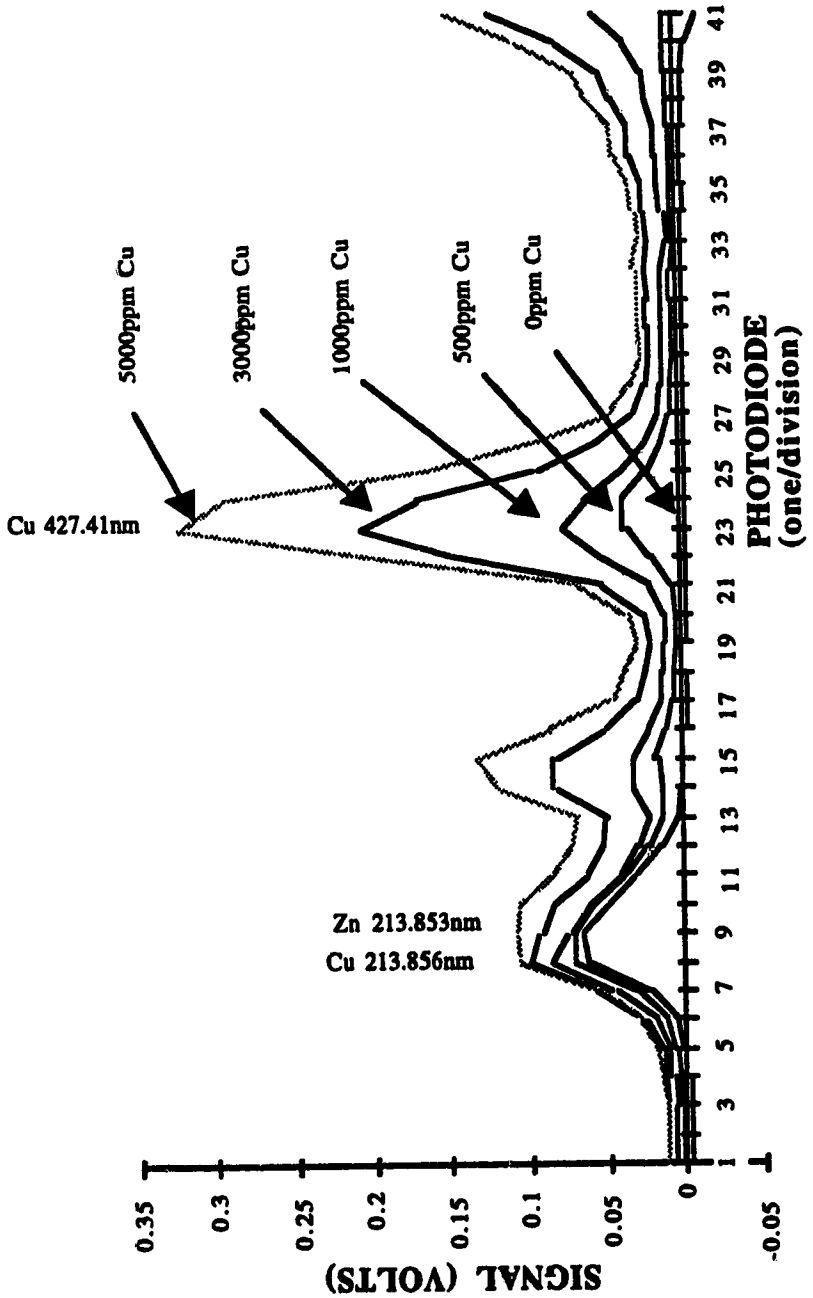


Figure 41 Water background subtracted spectra of 10ppm Zn with variable copper matrix.

The most prominent information given by this figure is the extent of interference due to copper, it is not only directly overlapping the zinc signal but also causes additional interference over the entire spectral window.

In figure 43(a), a 0.53- nm window in the vicinity of the zinc signal is expanded for the examination of overlapped spectra of (a) the 5000 ppm copper interferent, (b) the zinc analyte with 5000 ppm copper interference and (c) the recovered analyte spectrum (i.e. when spectrum (a) is subtracted from spectrum (b)). In figure 43(b), the recovered spectrum (c) is compared with the spectrum produced when only a water blank spectrum is subtracted from a spectrum of a 10 ppm solution of Zn having no added copper interferent. It is obvious that subtraction of the spectrum of the interferent can lead to recovery of the analyte signal. Nevertheless, the recovered spectrum appears more noisy along the wavelength axis. The increased noise results from the effect that very high concentrations of matrix have on plasma stability. Therefore as a result of this noise, it is expected that for high concentrations of matrix interferent, a decrease in the precision of analytical data is expected. This noise will be studied in greater detail in section 7.7 of this chapter.

Clearly, the photodiode array spectral window, combined with powerful graphics software easily facilitates better understanding and examination of these spectral interferences. These interferences are typical of those which pose the greatest problems for conventional direct readers.

It has already been demonstrated that direct subtraction of the spectrum produced by a concomitant, has a unique potential for removing simultaneously direct spectral overlaps, wing overlaps, concomitant introduced stray light and other

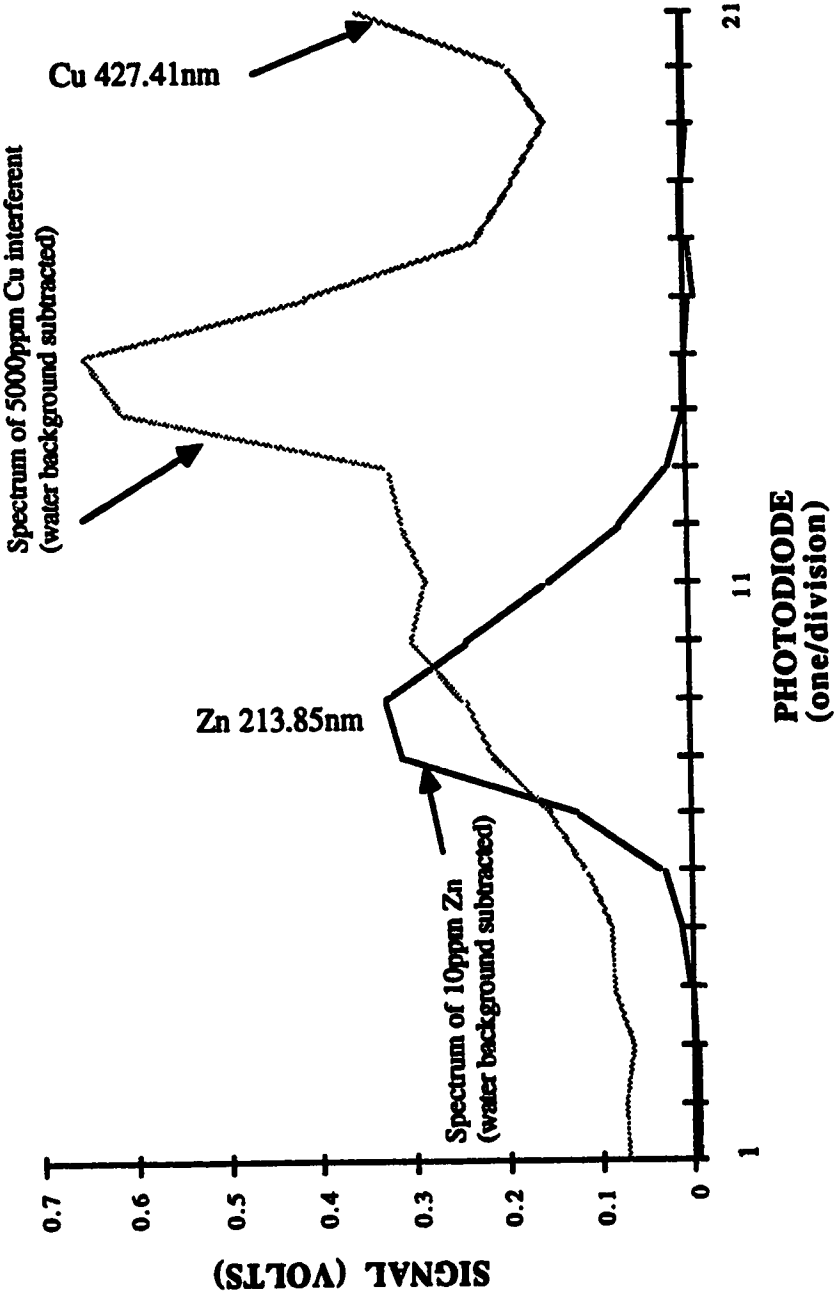


Figure 42 Water background subtracted spectra of 10ppm Zn and 5000ppm Cu in vicinity of Zn 213.85nm spectral emission

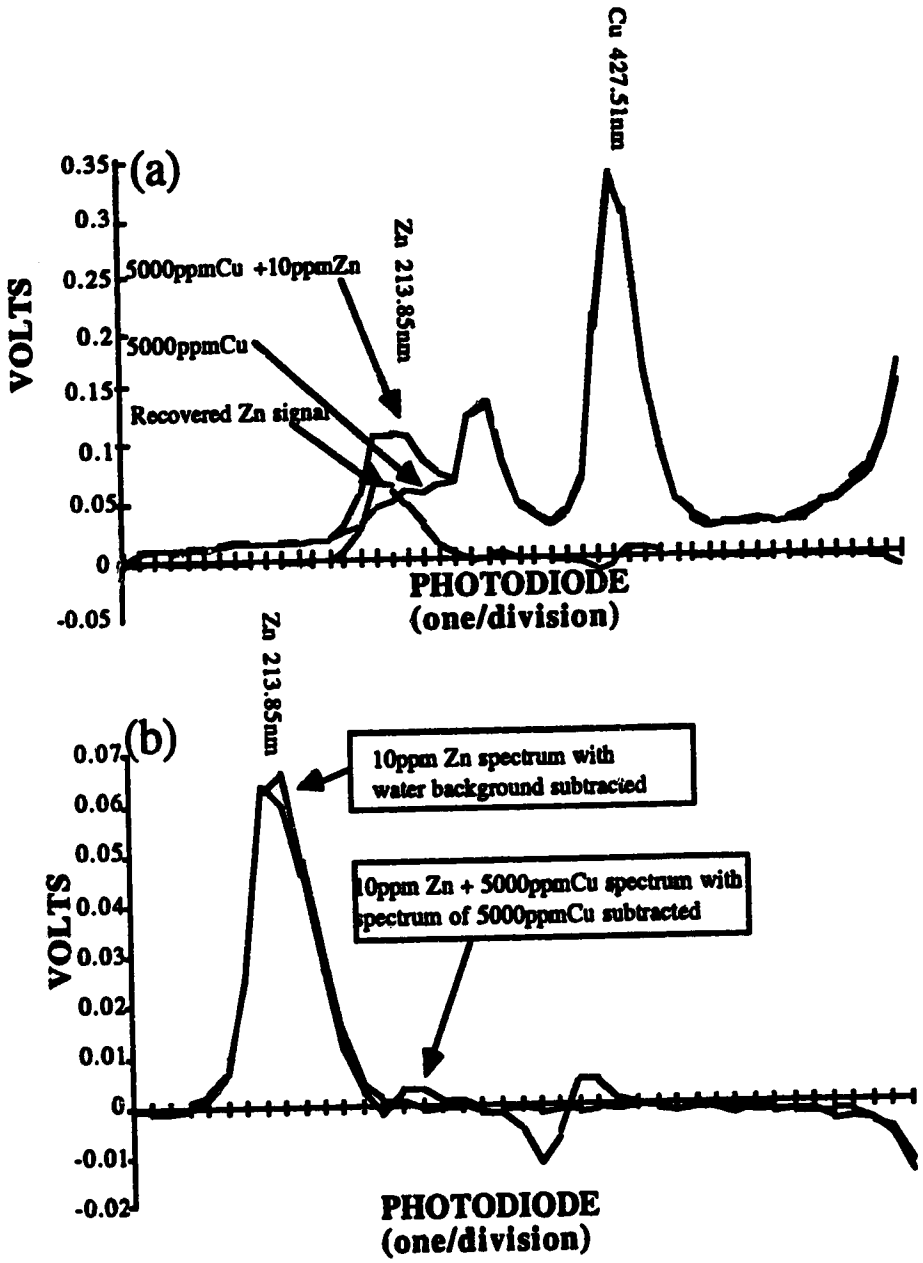


Figure 43 Recovery of Zn signal at 213.85nm by direct subtraction of spectrum of 5000 ppm copper interference

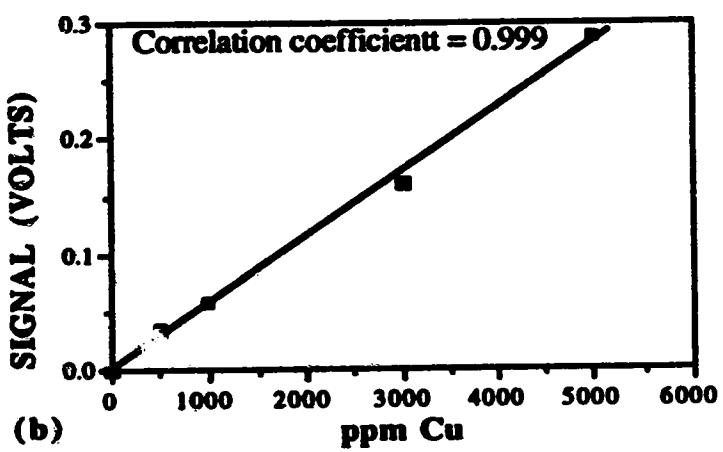
(a) Spectrum of 5000ppm copper interferent, zinc signal plus copper interferent and of recovered signal.

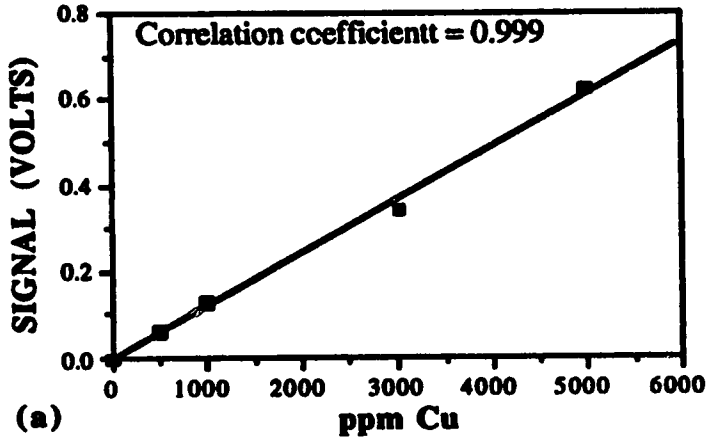
(b) Comparision of recovered spectrum and spectrum of 10ppm zinc

background interferences. In the following experiment two photodiode array channels will be used to measure both interferent and spectrally overlapped analyte signals separately.

Using the information about background given by the photodiode array channels it will be seen that very good corrections for interference effects, including corrections for direct spectral overlaps of the analyte signal can be made. The linearity of the interference effect will be investigated. Additionally, these corrections are applied successfully over a range of interferent concentrations. The precision with which this correction can be applied is also investigated

Copper solutions ranging from 500-5000 ppm copper and each containing 10 ppm zinc are used as calibration standards. The Cu 324.75 nm resonance emission was measured by one photodiode array while the other array is positioned to measure the Zn 213.85 nm emission. This latter array, by coincidence, also happens to measure a minor copper line at 427.51 nm. The copper calibration plots for both the 324.75 nm (Figure 44(a)) and the 427.51 nm (Figure 44(b)) copper lines are linear with correlation coefficients approaching 1. In figure 44(c) the magnitude of the copper interference at the Zn 213.8 nm analyte line is also plotted as function of the concentration of the copper interferent. In this plot the copper interference is presented as the equivalent concentration of zinc required to produce the same increase in intensity. From this plot, it is clear that each 1000 ppm of copper, generates on average, a signal equivalent to 1.8 ppm Zn at the 213.85 nm. It is also noted, that the data for Figure 44(b) shows a lot of scatter and as a result a poor correlation coefficient (0.98) is achieved.





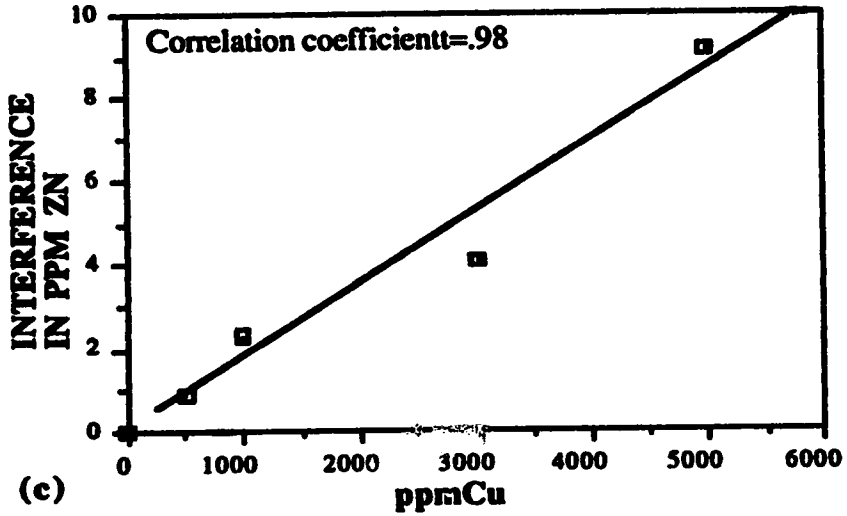


Figure 44 Calibration plots for copper at (a) 324.7nm (b) 427.5 nm and (c) the copper interference at Zn 213.86nm expressed as ppm Zn.

Having determined the relative copper : zinc response at 213.85 nm using standard Cu solutions, these data are used to determine interference correction factors. The correction factor also takes into account background intensities and wing overlaps. The best corrections are those which can totally remove the effect of copper interference at the zinc 213.85 nm line, i.e., to reduce the level of interference to zero (see figure 43).

The effectiveness of corrections based on peak height and peak area are compared in Figure 45. Corrections based on peak area calculations give on average, more accurate corrections than those based on peak height measurements. This is obvious from the graph, which shows that corrections based on peak area are generally more accurate. Correction factors based on peak height tend to over correct for interference. The precision of the corrections is found to be directly related to the concentration of matrix element. Measurements of precision were made at various concentration levels of interferent and range from approximately 2% rsd, for low interferent concentrations to 7% rsd for 5000 ppm copper.

Since the signal intensities at the zinc line are weak, any increase in noise generated by the nebulization and desolvation step will cause a large decrease in precision. A signal-to-noise ratio study also shows a general increase in noise across the spectrum as a function of increasing interferent concentration. These studies are the subject of the next section of this chapter.

Overall, the corrections achieved are reasonably accurate, with the precision mainly limited by noise, generated possibly, at the nebulisation step by the high concentrations of copper matrix.

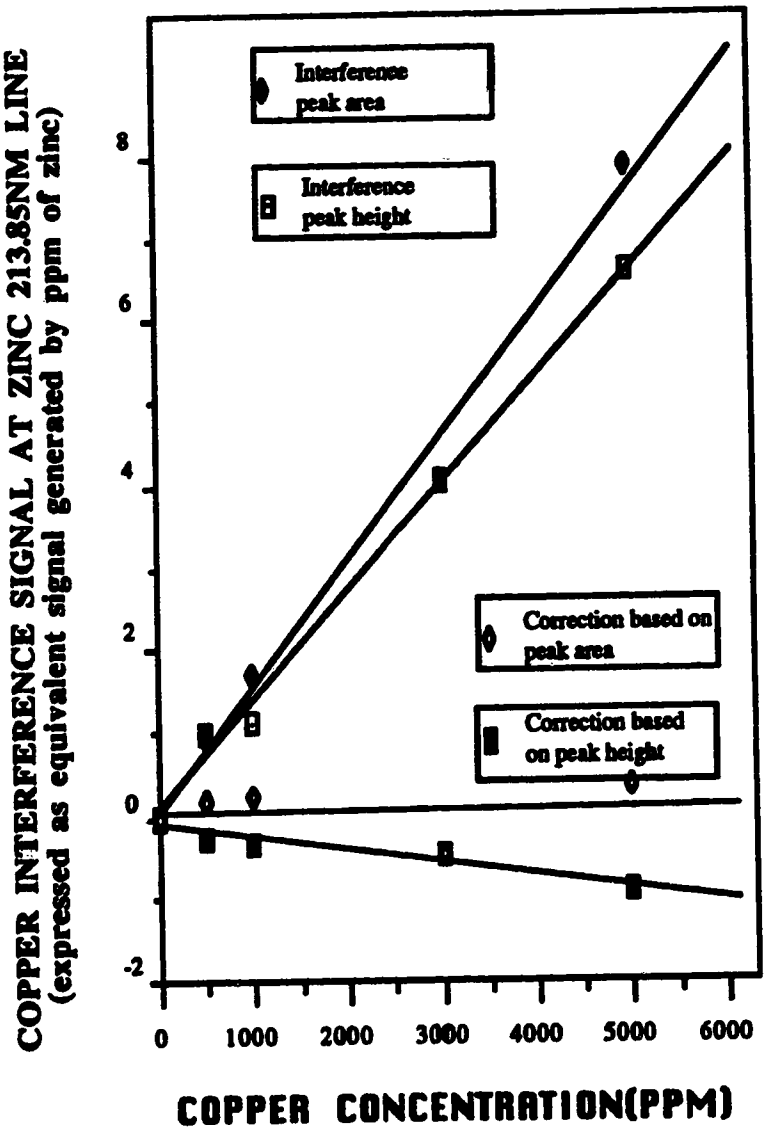


Figure 45 Graphical display of copper spectral interference and corrected signals at Zn 213.85 nm, as a function of copper concentration

Earlier in this section, direct subtraction of the spectrum produced by an interfering element was proposed as a unique method, by which, corrections could be made to analyte spectra exhibiting severe direct spectral overlaps. It was also proposed, that measurements of the interferent, made on a separate channel could be used to generate simulated interference spectra for the analyte channel. A standard spectrum of the interferent in the analyte channel is used in the calculation of these simulated spectra. Finally to correct the raw analyte spectra, these simulated interference spectra could subsequently be subtracted from the raw signal spectra (analyte and interferent signals).

Initially, the ratio of intensities for the interferent in both the zinc and copper channels, was determined using a standard solution of 5000 ppm copper. Measurements were then made of copper interferent concentration with the PDA centered at 324.75 nm copper line. These measurements and the previously determined ratio of signals in each channel, are subsequently used to scale a stored (in the computer memory) standard spectrum of the copper interference, originally acquired from the zinc channel. This resulting scaled (simulated) spectrum is then subtracted from the overlapped (i.e., analyte plus interferent) spectrum in the zinc 213.85 nm spectral window. The following solutions were prepared, aspirated into the ICP and the resulting spectra, generated in both the copper and zinc photodiode array windows was stored.

Solution (a)	10 ppm Zn
Solution (b)	10 ppm Zn + 500 ppm Cu
Solution (c)	10 ppm Zn + 1000 ppm Cu
Solution (d)	10 ppm Zn + 3000 ppm Cu

A water blank spectrum was subtracted from the spectrum of solution (a). Simulated interference spectra were calculated as described previously for solutions (b), (c) and (d). The appropriate simulated spectrum was subtracted from the raw spectrum acquired from the zinc analyte channel for each of the solutions. All corrected spectra are overlayed for each of the above solutions in Figure 46. A 0.53 nm spectral window, in the vicinity of the Zn 213.85 nm line is expanded for detailed graphical examination.

The corrected spectra in the vicinity of the Zn213.85 nm line match almost exactly the profile of the spectrum for the matrix free, water background subtracted spectrum of 10 ppm Zn solution. Some minor copper signals especially at the higher concentrations are not completely removed (Figure 46). Nevertheless, good corrections for the effect of interferent have been achieved using this method. The effectiveness of correction is especially evident when the corrected spectra of Figure 46 are compared with original raw spectra shown in Figure 41

This appears to be a unique and successful method for the correction of all concomitant introduced interferences.

Better control of aerosol and plasma gas flow-rates, together with a better understanding of the causes of increased noise at higher matrix concentration, could eventually lead to a method to increase the precision of the corrections. Spectrometer redesign for greater light throughput would also be an advantage.

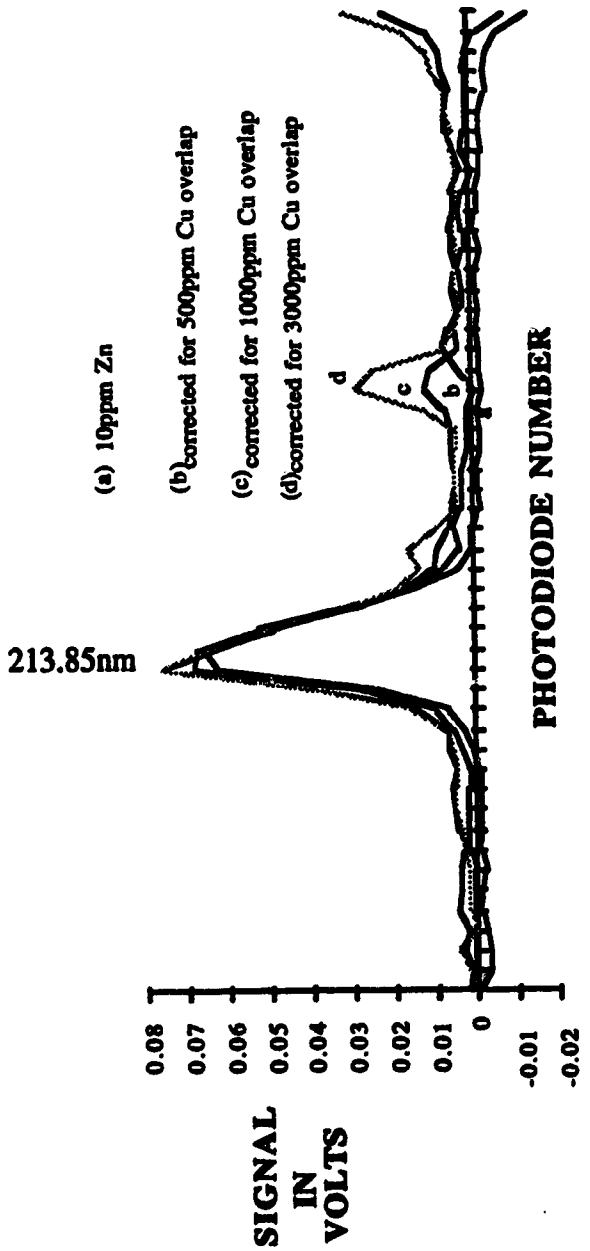


Figure 46 Corrected spectra, following subtraction of simulated spectra of copper interference from raw signal spectra

7.7 Signal-to-Noise Ratio Spectra

A signal-to-noise ratio (S/N) spectrum is a plot of S/N vs wavelength (or photodiode number) across the entire spectrum. It is a useful way of examining the stability of signals as a function of wavelength across a spectrum. Noise is calculated as one standard deviation of the signal acquired by a photodiode for several replicate measurements. The signal used for this calculation, is the average signal obtained for the replicate measurements, on the same photodiode. Therefore S/N is this average signal divided by the standard deviation of the signal. To obtain a S/N spectrum from photodiode array data, the S/N of each photodiode is plotted versus photodiode number (each photodiode represents an incremental change in wavelength of from 0.013 to 0.017 nm in the case of this photodiode array direct reader).

Complete (a) signal (b) S/N and (c) standard deviation spectra from spectra obtained for 10 ppm Mn are shown in Figure 47. The standard deviation spectrum is a plot of the standard deviation of the signal recorded on each photodiode, versus photodiode number, i.e., wavelength increment. When the standard deviation spectrum is displayed alongside both the signal and S/N spectra it is possible to graphically examine the spectra and determine whether low S/Ns are due to low signal (poor sensitivity), high noise (leading to large standard deviations) or a combination of both. For Figure 47, the standard deviations range from 0.5 millivolts to 4.5 millivolts over the 50 diodes comprising the 0.65 nm spectral window. The average standard deviation is approximately 2.5 millivolts.

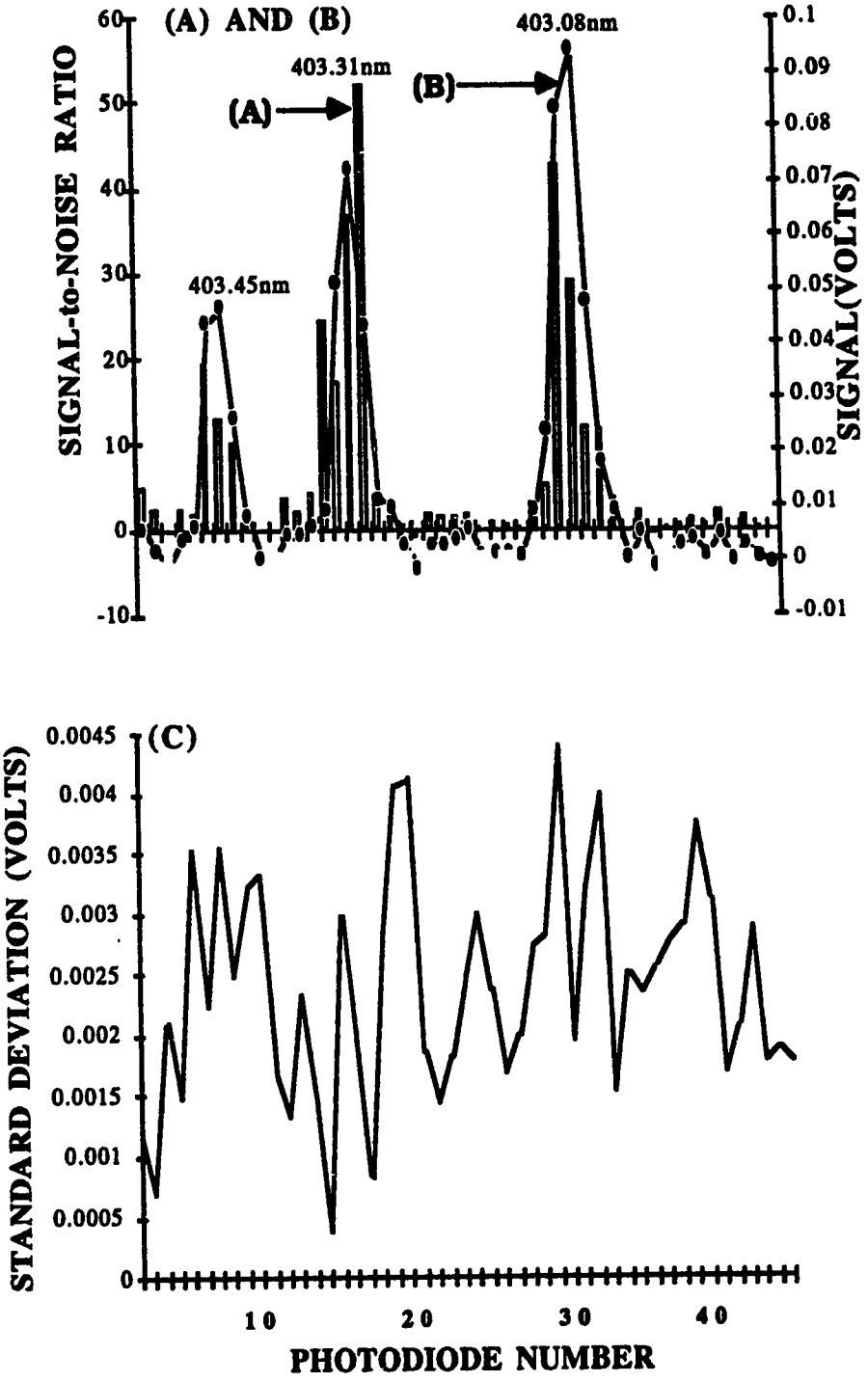


Figure 47 Complete a) signal-to-noise ratio b) signal and c) standard deviation spectra for 10ppm Manganese.

Considering that the dynamic range for the analogue-to-digital converter ranges from 0-1 Volt i.e. 0-1000 millivolts then provided no additional noise is introduced the average theoretical precision achievable on a full scale signal is 2.5/1000 or 2.5 parts per thousand which when expressed as a percentage is is equivalent to 0.25% rsd. Experimentally the present PDA system has yielded rsd's approaching 0.45%.

For the S/N plot of 10 ppm manganese shown in Figure 47, the best S/N achieved was approximately 50. Since S/N is the reciprocal of rsd expressed as a percentage, then a S/N of 50 is equivalent to an rsd of 2%. This is much poorer than that which is theoretically possible. It is obvious therefore, that if the theoretical S/Ns are to be achieved for 10 ppm Mn then as a first approach, the signal must be increased to fill the dynamic range of the detector (e.g. by increasing the integration time). A further decrease in the standard deviation of the signal (noise) is possible but would be quite difficult to achieve since measurements already indicate that we are photodiode readout noise limited. Therefore both S/N and standard deviation spectra provide additional useful information on those problems which limit precision in these measurements and thus provide a basis regarding the appropriate modifications which must be implemented to achieve better data

S/N spectra are also useful in many other studies involving the PDA direct reader. One such study, is that involving the correction of spectral interferences, discussed in some detail, in the previous section. In this case S/N spectra help in explaining the decrease in the precision of these corrections. The specific study involved the correction of the direct spectral overlap caused by copper interferent on the zinc analyte signal. Signal-to-noise ratio spectra in the vicinity the zinc analyte signal, are calculated from spectra obtained for several concentrations of copper

interferent. The overlapped signal-to-noise ratio spectra are displayed (Figure 48) for several concentrations of interferent. The overlapped signal spectra were previously given in Figure 41. The decrease in S/N across the spectrum as a function of the concentration of copper interferent is obvious. Obviously the increasing concentration of matrix interferent is not only increasing the spectral overlap of the analyte signal but is making combined signal more noisy.

To add further emphasis to this conclusion, it is informative to compare the noise in the zinc analyte spectrum with a blank water spectrum subtracted from it, to the recovered analyte spectrum after the copper interference spectrum has been removed by subtraction. Direct subtraction of a spectrum for 5000 ppm copper from the spectrum for a solution containing 5000 ppm copper and 10 ppm zinc is carried out. The resultant spectrum is displayed, together with the water background subtracted spectrum of of 10 ppm zinc alone (Figure 43). It is obvious that a good analyte signal spectrum can be recovered by direct subtraction of the interfering spectrum.

This spectrum however yields very little information concerning the poor precision associated with these corrections. On the other hand overlapped S/N plots for both spectra from Figure 43, indicate graphically once again that high concentrations of concomitant increases the noise and therefore decreases the S/N across the spectrum (Figure 49)

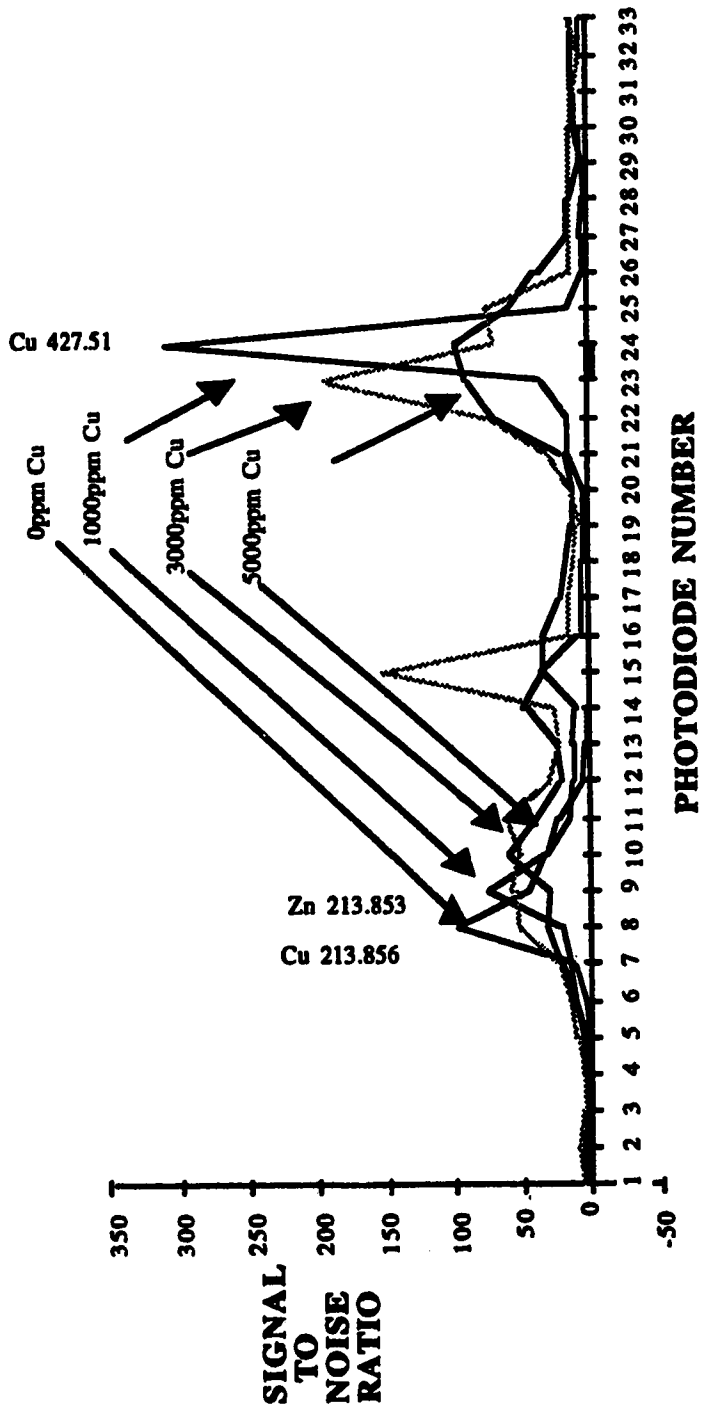


Figure 48 Signal-to-noise ratio spectra for 10ppm Zn having variable concentrations of copper as matrix.

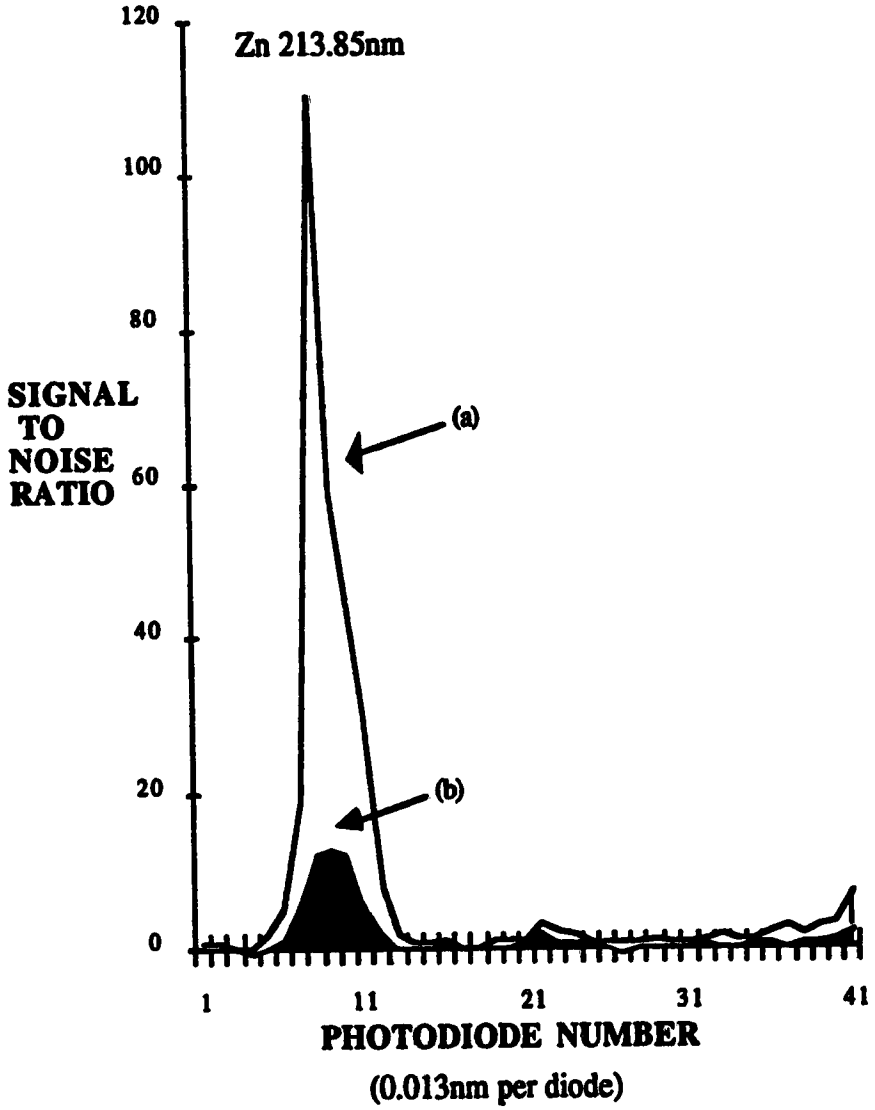


Figure 49 Signal-to-noise ratio spectra for zinc signal with and without added copper interferent

(a) 10ppm zinc having water background subtracted
(b) 10ppm zinc + 5000ppm copper having spectrum of 5000ppm copper subtracted.

7.8 Final System Analysis and Comments

One way to measure the achievements for any project is to evaluate the final system to see if it reaches the goals set at the conceptual stage. Many of these initial goals were set for the purpose of improving on the limitations of a multiple PDA direct reader, designed and evaluated by another researcher (5). But the more important goals for a redesigned PDA direct reader were more ambitious than this. A fundamental change in the entire concept of how a PDA direct reader would be controlled was envisioned.

For a PDA to achieve it's optimum performance it would ideally require a dedicated processor and dedicated fast memory to store the large amounts of data it produced at high speeds. A PDA direct reader requires several such channels together with a method for linking them all together into a useful instrument. Herein lies the real achievement of this work. The other goals set us as a result of identified deficiencies in the previous system (5) were achieved either automatically as a result of this new design or by taking care not to repeat design faults found in this system.

Most of the initial goals set for the redesigned system have been met and overall a more powerful PDA direct reader has been built. The main achievement has been in the design of a functional direct reader based on multiple PDAs, individually controlled by dedicated processors. It has been proven that a multiple processor based PDA direct reader is not only possible but also, by the considered application of present technology such an instrument can be built at a reasonable cost.

A network has been developed for the system, facilitating the linkage of all processors and allowing the control of multiple processor operations at speeds approaching 1-MHz. Some of the

features of this system meet the following goals which were identified in the hindsight evaluation of the previous direct reader. These are:

1) The system uses a single power supply thus eliminating one source of noise identified in the previous system.

2) Localized PDA signal acquisitions by processors has eliminated another major noise source arising when susceptible video signals were carried several meters to analogue conversion systems.

3) The minimum integration time usable for simultaneous signal acquisition from several channels has been reduced from 0.1 second to several milliseconds.

4) Finally, further major improvement over the previous design is the degree of modular development this system allows.

There are two major mutually dependent sections to the system. However both of these sections function independently for most operations, therefore independent modifications to each system is possible. These individual systems are the microcomputer used as the user interface, i.e., the "front end" and the network of PDA signal acquisition and control processors. The PDA acquisition and control systems incorporating the single board computers, can be modified or extended independently of the "front end" computer system. However, it is not envisioned that any further major changes to this data acquisition end of the computer system will be necessary since, the single board computers possess superfluous control and signal acquisition capabilities to meet the needs of present and projected future experiments. Therefore PDA acquisition has become standardized with this processor. Gone is the need to redesign for this signal acquisition functionality while further technology developments

may merit the incorporation of more powerful data crunching machines to be used as a "front end". These "front-end" developments can be incorporated independently of the rest of the system. This is a very important feature of the present design. With the rapid developments occuring in laboratory computing, it is envisioned that the "front end" will be changed to a more powerful data processing and graphics machine. The incorporation of the new "front end" will not require a complete system overhaul but the development of relatively simple software to replace the present communications over the RS232 serial interface to the single board processors. The decision to use the RS232 interface as the communications standard for the system also serves to simplify this type of development.

In the following discussion some ideas on how the electronic control system could be improved, streamlined, and developed are examined.

The system could be further developed in the general area of serial communications between the "front end" processor and the single board computer. Baud rates could be optimized and standardized to facilitate the development of less complicated operating system programs. At present, the controller transmits it's data at 600 baud while the auxiliaries have been optimized to transmit at 9600 baud. Interactive communications between the single board processors and the "front-end" is presently set at a rate of 110 baud.

When more powerful "front end" processors are incorporated into the system, the capability to handle much greater amounts of data will be available. In this situation the software should be modified to allow for transmission of larger blocks of data from the single board processors. At the moment the data acquired from 6 scans of the 128 element PDA is

transferred in one go. This is enough at present to exhaust the memory buffer capacity of the 64K Apple II+.

Further developments in the communications software for the single board processor may be facilited by the use of a version of BASIC available for this computer from it's manufacturer.

In the present system, there is no automatic error checking on serial data transferred between the "front end" and the single board computers. This could be incorporated into any new communications software written for the system. Also some problems leading to erroneous bytes of data being received over the network have been observed, this was prevented from causing serious problems by designing software which discarded the erroneous data. It would be an advantage if the causes of these errors were exactly identified and understood more completely.

Expanding the system to accommodate more PDAs is of course possible. Here there are two approaches which can be taken, both dictated by the eventual number of PDA - processor systems (channels) required. Three channels, bringing the total to eight altogether, could be handled by the present controller. It would simply be necessary to connect the appropriate serial lines of the new systems to the multiplexer/demultiplexer network and to modify the software, to handle the switching of communications with these additional channels when necessary. For the development of larger PDA - processor systems, the best approach would be to develop a new controller/auxiliary subsystem similar in all ways to the present one. This subsystem could have a dedicated or shared serial link with the "front end". Another option would be to design a much larger multiplexer/demultiplexer channel selection system. In this case the same multiplexer/ demultiplexer control lines could be used

to control additional multiplexer/demultiplexers. Eventually, if over twenty channels were required the controller should be dedicated to its controlling tasks and carry out no data acquisition. Data acquisition is also one of its functions in the present system. In this way very large multiple processor systems linked to a single "front end" are possible.

One problematic feature of the electronic system still remaining from the original design is the ribbon cable attaching the array to the RC10245 driver board. Here the clocking signals for the array can interfere with the video output on adjacent wires of the ribbon. This could cause problems if the ribbon was moved and had varying degrees of twists during signal acquisition. This can only be eliminated by using an array/driver board combination designed in a compact package and suitable for positioning in the focal plane of this spectrometer.

Although in this work, the electronics of the system have been greatly improved from the previous design, the mechanical and optical features of the basic instrument have not been changed and as a result the capability of the system as a whole is limited. These limitations have already been examined in detail by Evans (5) and it is only necessary to discuss them here for the sake of completeness. The following is a summary of these deficiencies;

1) Since the systems (spectrometer of source) were not on a single mount the spectrometer was prone to losing alignment over a period of a few hours. This did not pose as serious problem in the present research.

2) External optics for gathering light from the plasma and passing it to the grating could be improved, e.g., by using a collimating light collection lens.

3) The grating was not blazed for the UV wavelengths mainly generated by the ICP and this resulted in quite large first order intensity losses.

4) The grating exhibited severe ghosting which added to the spectral interferences problem, the use of a holographic grating would eliminate this.

5) The dark current variations due to inadequate thermostatic control of the array.

5) The width of the array carriage, equivalent to a 25 nm spectral window in the focal plane can limit access to adjacent emissions. Four solutions indicate that this is not unsurmountable problem. These are; a) use larger arrays, b) use an alternate spectral line for the element, c) use the same wavelength in another spectral order and d) use a system of plane mirrors to reflect the close by emission onto another array.

The construction of the instrument amounted to a major hardware and software development task. As a consequence of this, the time spent on the evaluation of the working instrument was not as long as was ideally desirable. From the limited evaluation carried out, it is evident that the possibilities for the instrument are exciting. The capability of simultaneous spectral acquisition from several PDAs is one of the unique features of this design. The simultaneous recording of both background and analyte signals on several channels offers new approaches to the correction of spectral overlaps. Interferences of this type which pose great problems for conventional PMT direct readers can be tackled with much greater success using this instrument. The simultaneous recording of both background and analyte signals on several channels simultaneously was proven to be of great

benefit. The new correction technique for spectral overlap interferences, involving the generation of simulated interference patterns should be further explored and refined. The basic operation of how to apply the technique was described here, but a wider ranging study, over several plasma operating conditions, has yet to be carried out. This type of study would be worthwhile, especially if, it was also carried out for a variety of commonly occuring spectral overlaps.

Further extensions of the preliminary noise studies are also required. From the data presented here it is obvious that the instrument has potential for studies of ICP noise characteristic. Noise studies carried out across a spectral window, yield much more information than those studies which involve localized measurements at an individual spectral line. These studies should be extended to examine the effects on precision of various nebulizer systems, controlled nebulizer flow systems and for controlled plasma gas flow. The reason for this is that it is highly improbable, that the precision of correction procedures in cases of spectral overlaps, can be improved without more precise control of plasma operating conditions.

Additionally, it is evident from the work described here that matrix loading i.e. interferent concentration can adversely effect the signal - to - noise ratio. The effect of sample matrix on plasma conditions and plasma stability could be further investigated using noise studies similar to those already carried out.

To summarize, this instrument is an evolutionary development in the application of photodiode arrays as detection elements in direct reading spectrometers. A system involving microcomputers and single board computer- PDA units have been linked together in a unique way, resulting in a ICP detection system of great potential. A preliminary evaluation of the system

for a direct reader has been carried out and documented. The instrument has been applied to some difficult ICP measurement problems and found to offer new solutions to these problems. The future potential of the instrument as a probe for the study of fundamental ICP characteristics has also been outlined.

7.9 Conclusion and Update

Since the experimental work for this thesis was completed (late1986) image sensors including photodiode arrays have figured prominently in instrumentation development for ICP-AES.

A spectrometer for atomic emission analysis has been reported that uses nine 1024 - element PDAs. In this design a set of nine arrays replace the photographic plate on a Hilger medium quartz spectrograph(54). Full spectral coverage from 200 to 1000 nm is achieved by staggering the arrays so that 40 diodes of one array overlap the next array. The system is relatively expensive and the hardware required to control the PDAs is extensive.

Another important development regarding PDAs is the recent development by Reticon of a random-access-readout PDA sensor (55). This PDA offers the possibility of selective readout of certain photodiodes while allowing the remaining detectors to continue integration.

A novel PDA spectrometer configuration has been introduced (56) that combines a linear photodiode array detector with an echelle spectrometer. In this system light from a source is first pre-dispersed with the use of a low resolution concave grating polychromator. Desired narrow-wavelength regions are selected with the use of a slotted mask placed in the focal plane of this polychromator. The selected wavelengths transmitted by this mask are then recombined by a concave mirror and a second

grating. This beam of selected wavelengths is directed to an echelle grating and the dispersed radiation is finally focused on a linear photodiode array detector. The spectral characteristics of this instrument have been evaluated (57), and it was reported to have wide wavelengths coverage.

This spectrometer is in effect a user-configurable direct reader since slotted masks can be prepared to select the desired set of wavelengths. This instrument is currently being commercially developed by LECO Corporation. It should be noted that in this configuration (without order sorting) the echelle produces a one-dimensional spectrum.

An instrument combining an echelle spectrometer with a charge injection device (CID) has also been developed (58). In this configuration the echelle spectrometer incorporates a prism for order sorting and as a result a two dimensional spectrum is generated. The CID consists of a two-dimensional array of detector elements. When combined with the two-dimensional echelle spectrum it provides simultaneous multielement detection over a spectral range from170-800 nm. In addition, the large linear dynamic range of the CID and the capability for random access integration (where each detector element can be non-destructively read until the desired signal-to-noise ratio is achieved), provides a detection system of great promise. This system was characterized for the multielement analysis of solutions using a DCP (58,59) and an argon ICP (60).

Simultaneous background measurements allow efficient background correction (59) and spectroscopic interferences can be eliminated by selecting another wavelength (59,60). Detection limits are comparable with conventional detection systems using similar emission sources for most elements(61). A direct reader of this type is commercially available and marketed by the

Thermo Jarrell Ash Corporation under the brand name IRIS CID Plasma.

A commercial direct reader of similar optical design to the CID-echelle system described above but incorporating a segmented two dimensional charge-coupled-device(CCD) as the detector has been developed (62). By using a segmental CCD rather than a complete two dimensional array of CCD detector elements, it seems possible to avoid most of the "blooming" problems originally associated with these devices and simultaneously to greatly reduce the readout noise. This innovation allows the CCD segments of the detector to be independently addressed and the appropriate integration time to be set for each spectral window, thereby avoiding saturation. The performance evaluation (63) of this detector reports that the signal-to-noise ratio is photon shot noise limited. This would indicate that an image sensor device is available for spectral measurements which is not readout noise limited, indeed an exciting development.

In summary, the attempt as described in this thesis to develop a more ideal direct reader has been successful in so far as it has provided a better spectral measurement capability for a classical optical design of a direct reader. The development of independent programmable detector arrays for the focal plane of a direct reading spectrometer has yielded a practical solution for some of the tenacious problems which have plagued these instruments for decades.

The experimental work for this thesis was completed in 1986. The above review of developments since then has highlighted increased activity in the area of improving detection systems for direct reading spectrometers. In particular, the use of image sensors of various types has figured largely in these

developments. Of significance regarding this thesis work is the trend in recent years towards the development of better quality image - sensing devices for spectroscopy, and in particular of devices incorporating independently programmable segments of sensor elements. In effect, the type of image sensor segment desired in the mid-1980s, was then only available by combining individual devices (e.g., 128-element PDAs), it is now being made available as a single two-dimensional device. Obviously the optical configurations of direct readers also required innovation so that these compact detectors could be used. Indeed of great significance is the movement towards a complete redesign of the optical system of the modern direct reader to more fully exploit the capabilities of these novel detection devices. It seems probable that the classical direct reader incorporating photomultiplier tubes as detectors will eventually become obsolete.

Whether PDA, CCDs or CIDs provide the next generation of detection device for direct reading spectrometers, the promise offered by these devices to improve AES measurements is great. Coupled as image sensor-echelle systems these devices appear set to revolutionize AES.

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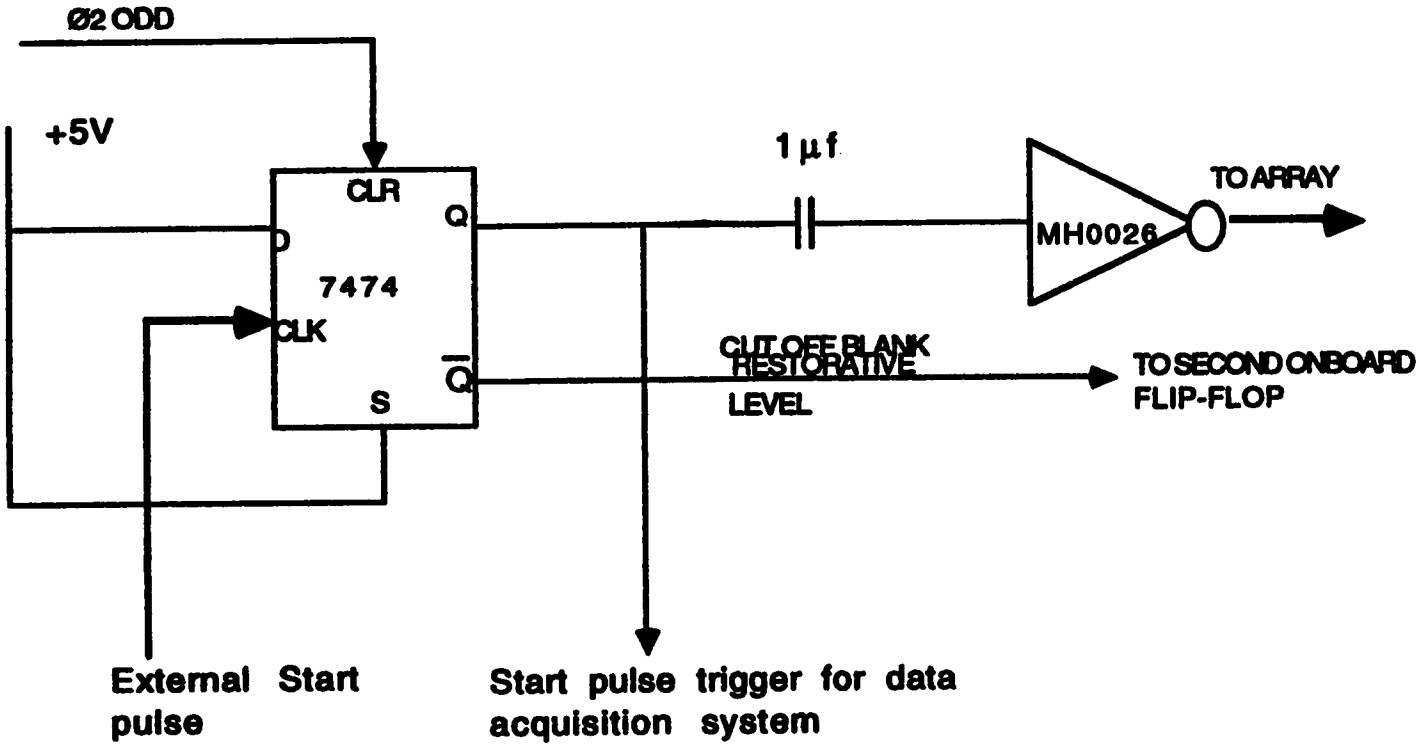
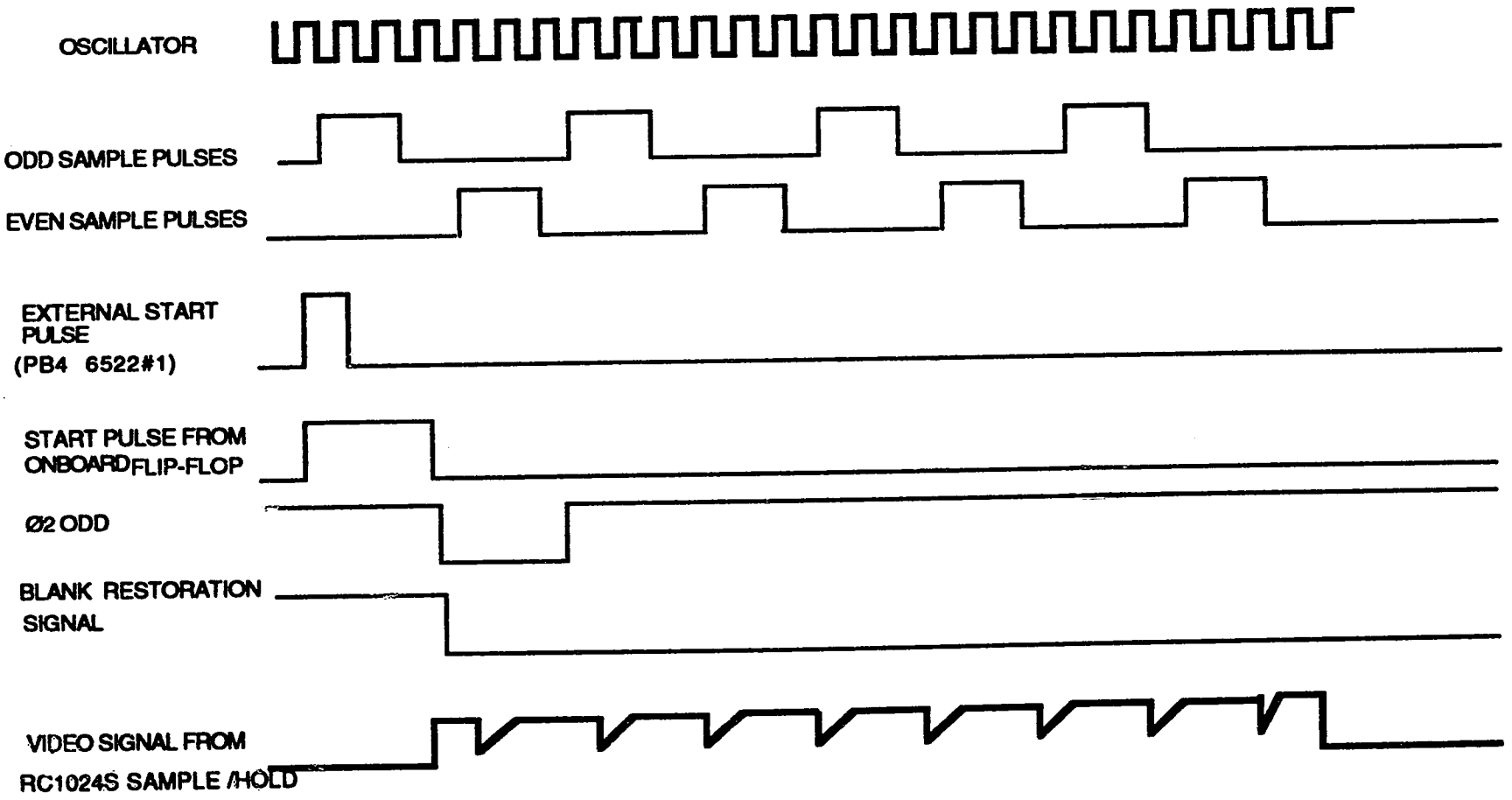
APPENDIX 1

Appendix 1 The Start Pulse Circuit on the RC1024S Photodiode Array Driver Board



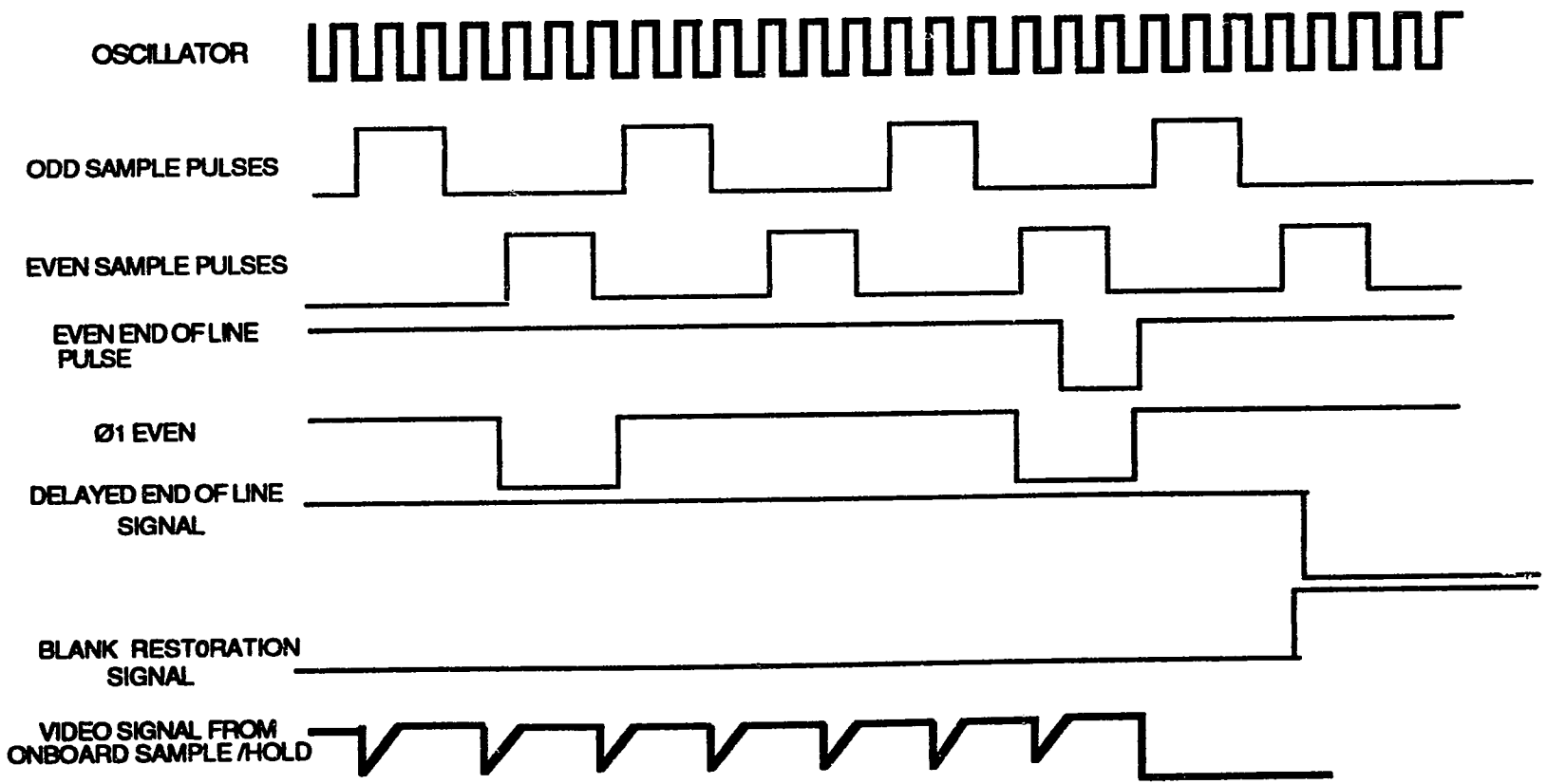
APPENDIX 2

Appendix 2 Timing Sequence for the Start of Photodiode Array Readout



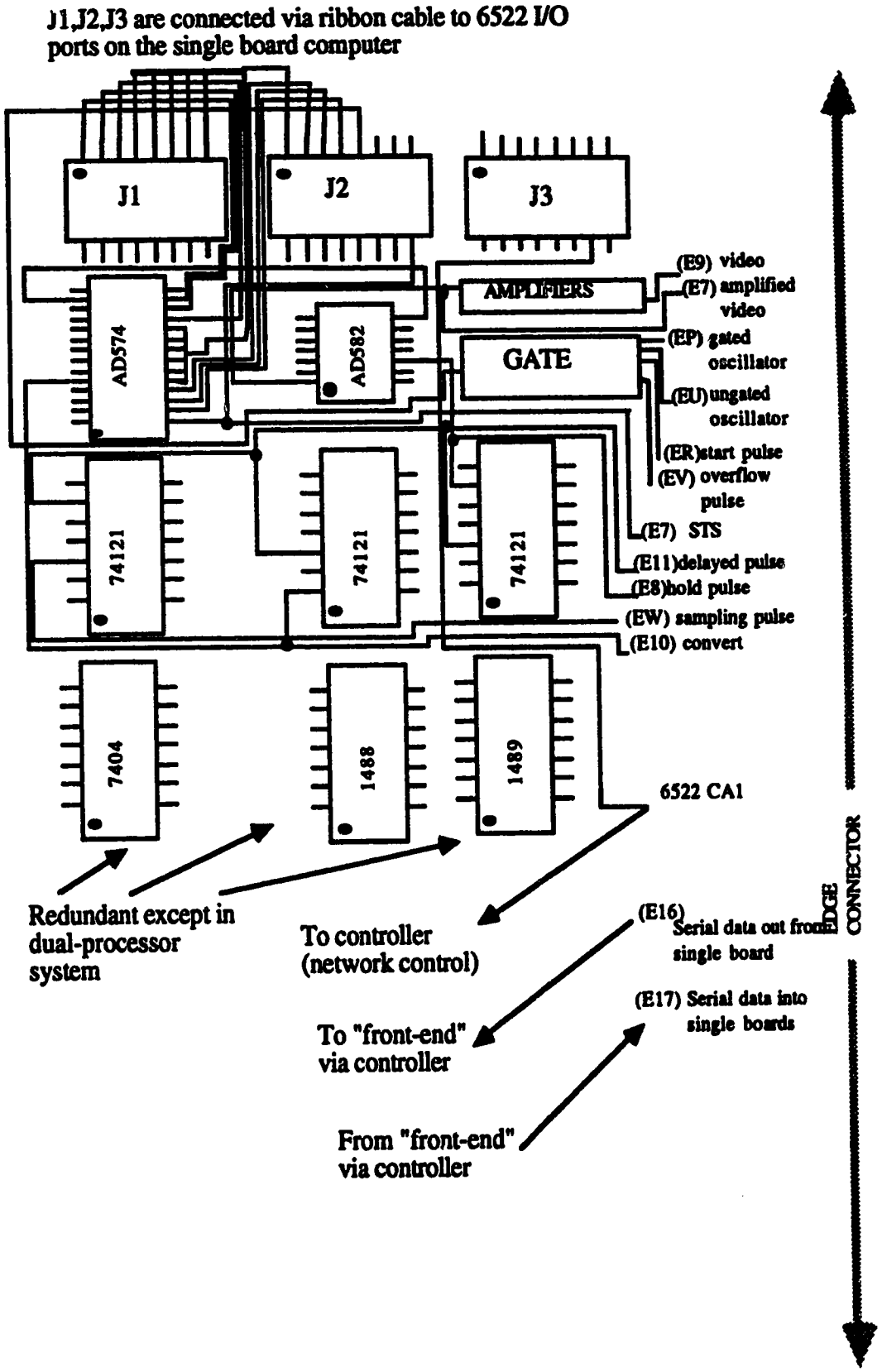
APPENDIX 3

Appendix 3 Timing Sequence for the End of Photodiode Array Readout



APPENDIX 4

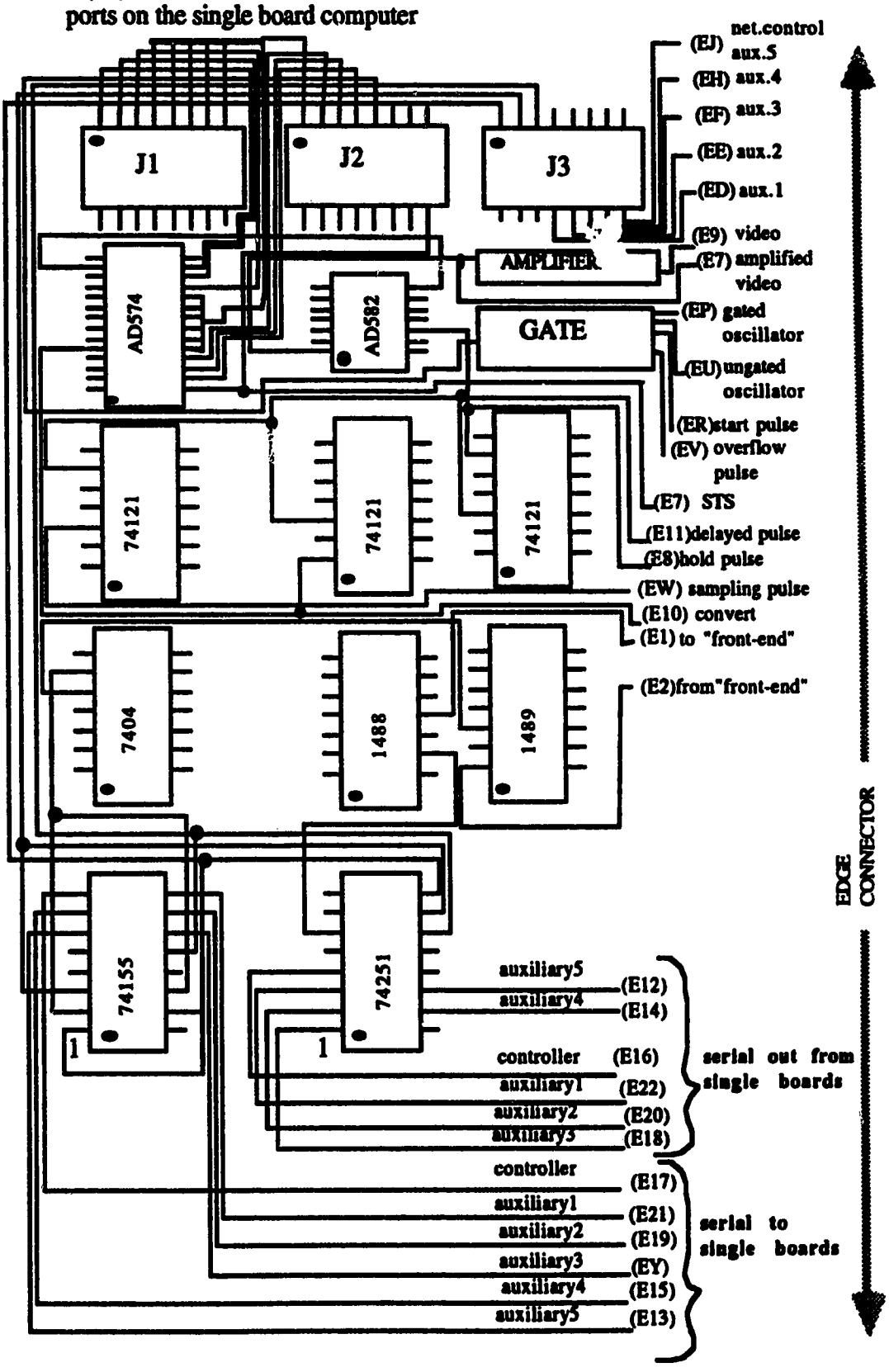
Appendix 4 Detailed Schematic of Custom Designed Circuit Board for the Auxiliary



APPENDIX 5

Appendix 5 Detailed Schematic of Custom Designed Circuit Board for the Controller

J1,J2,J3 are connected via ribbon cable to 6522 I/O ports on the single board computer



APPENDIX 6

APPENDIX 6 Programs for the Controller

```
HEX.      ASSEMBLY      COMMENTS
ADD-      CODE
RESS

F000  LDA  #0C  :Set serial communications at a BAUD RATE of 600
      JSR  FF18
      JMP  F900  :Routine for continuous readout of the photodiode
                 array.

----------MAIN PROGRAM  (ENTERED FROM MONITOR)----------

F010  LDA  #0C  :Communicate at 600 Baud for parameter setting
                and data transfer.
      JSR  FF18
      JSR  F090  :Setup scratchpad for T1 integration time timer.
      JSR  F520  :Controls parameter transmission from front end to all
                processors.
      JSR  F0F0  :Transfer erroneous data to zero page for correction of
                the controller's parameter list.
      JSR  F100  :Makes corrections for transmission errors, uses data in
                zero page.
      JSR  F571  :Send acknowledgement that controller has
                received its parameters and then send a positive
                edge to all auxiliaries to indicate that they should
                commence data acquisition.
      JSR  F130  :Acquire data.from photodiode array
      JSR  F230  :Make baud rate 600 again and indicate to front end
                that data is about to be transmitted.
      JSR  F250  :Transmit data from the 6 photodiode array scans of the
                controller.
      JSR  F5A0  :Control data transfer from auxiliaries and send
                an acknowledgement each time a set of data is
                transmitted.
      JMP  F018 :Return to start and again control parameter transmission
                from  front-end .

----------SETUP OF SCRATCHPAD FOR T1 INTEGRATION TIME TIMER-----

F090  LDA #07  :Placing 0780 in register for Timer T1 generates output
                pulses of period 3.22 milliseconds on PB7
      STA DBFE
      LDA  #80
      STA DBFF
      RTS
```

```
----------Acquire 99 ($63) bytes of parameter data from "front-end"-----
                (The three initial bytes recieved are not parameter data and result
                from switching transients which arise when the serial lines
                     are connected to the front-end by the controller,these
                          bytes are logged but ignored)

F0E0  LDX #63
      JSR F040
      STA 7F00,X
      DEX
      BPL F0E2
      RTS

----------Transfer erroneous address data to zero page----------

F0F0  LDX #20
      LDA 7F00,X
      STA 00,X
      INX
      TXA
      CMP #60       :Check if 96 bytes have been transferred.
      BNE F0F2
      RTS

------Correct the data (locations where errors were detected -------
          before parameter transmission) in zero page for
                01 and $81 errors.

F100  LDX #3E       :Data was downloaded into locations $00-3E of zero page
                     $3E is high byte of first address.
      JSR F2B0      :Generate 01 in accumulator
      STA (00,X)    :01 will be stored at the address stored at the indicated
                     location given in zero page. If no address is present then
                     01 is continually loaded into 0000.
      DEX
      DEX
      TXA           :The X register is decremented twice to point to
                     the next zero page location.
      CMP #1E       :The first 20 addresses were used for "01" errors.
      BNE F102
      LDX #40       :The locations $0040-0060 were reserved for
                     addresses having "$81" code errors.
      JSR F2A0      :This routine generates "81".
      STA (00,X)
      INX
      INX
      TXA
      CMP #60       :When $0060 is reached then finish.
      BNE F110
      RTS
```

```
----------Transmit acknowledgement to "front-end" indicating that parameters
                                    have been recieved

F120   LDX #7F
       JSR F2CO          :Set up serial port for output.
       LDA F3DO,X        :Output ASCII characters from character table
                         stored in ERROM.
       STA DFF1
       DEX
       BPL F122
       RTS

-----Acquire and store the data sequentially from 6 successive-----
                    array readouts.

F130   CLD               :Clear decimal mode
       SE1               :Set the interrupt
       LDX #00           :Place zero in all buffer memory locations
       LDA #00
       STA 8000,X
       STA 8100,X
       STA 8200,X
       STA 8300,X
       STA 8400,X
       STA 8500,X
          STA 8600,X
       STA 8700,X
       STA 8800,X
       DEX
       BNE F136
       LDA #05           :Place number of consecutive scans in zero page
                         location $0080.
       STA 80
       LDA 01            :Place number of replicates in $0081.
       STA 81
       LDA #03           :$7F03 is where low byte of second integration
                         time parameter is. Data in location $0082 will
                         later be used as an index to locate integration time.
       STA 82
       LDA #00           :The base address($8000) for low byte of
                         data is placedin zero page.
       STA 83
       LDA #80
       STA 84
       LDA #00           :The high byte base address is placed in zero page
       STA 85
       LDA #83
       STA 86
```

```
LDA #00          :The carry byte base address is placed in
                 zero page.
STA 87
LDA #86
STA 88
NOP
NOP
NOP
NOP
LDA 7F13         :The number of replications for initial scan is
                 placed in scratchpad $DBFA.
STA DBFA
LDA 7F01         :Low byte integration time parameter is transferred
                 from parameter file to scratchpad.
STA DBFD
LDA 7F02         :High byte integration time parameter is transferred
                 from parameter file to scratchpad.
STA DBFC
LDX DBFA         :Number of replicates is placed in X-register.
LDA #00          :Make CA2 and CB2 control lines -ve edge active.
STA DFDC
JSR F500         :Output a start pulse to clear array.
LDA #E0          :Set T1 as pulse output on PB7 and T2 as counter
                 on PB6.
STA DFDB
LDA DBFF         :Place count ($0780) in T1 allowing the
                 generation of pulses of3.125 milliseconds on PB7.
STA DFD4
LDA DBFE
STA DFD5
LDA DBFD         :Set  integration count in the T2 timer register
                 using data in $DBFD (Low byte) and
                 $DBFE (High byte).
STA DFD8
LDA DBFC
STA DFD9
LDA #20          :On the timing out of T2 proceed to read out the
                 array.
BIT DFDD
BEQ F1B8
JSR F2D0         :Start oscillator for array clocking and send
                 start pulse.
LDA DFD1         :Clear CA1 and CB1.
LDA DFD0
LDA #00          :Make PA and PB lines inputs.
STA DFD2
STA DFD3
LDY #7F          :The y-register is used as the diode counter.
CLC
```

```
      LDA DFDD          :Look for the array readout start pulse on CA1.
      AND #02
      BEQ F1D1
      LDA DFDD          :Poil for sampling pulse on CB1.
      AND #10
      BEQ FID8
      LDA DFD1          :Load the high byte and store.
      ADC (83),Y
      STA (83),Y
      LDA DFDO          :Load the low byte and store but first eliminate the
                        4 bits which are not data.
      AND #OF
      ADC (85),Y
      STA (85),Y
      LDA (87),Y        :Save the carry bit.
      ADC #00
      STA (87),Y
      DEY               :Decrement the diode counter.
      BNE F1A4
      NOP
      NOP
      DEC 80            :Decrement the "number of consecutive scans"
                        counter.
      BM1 F20D
      JSR F4EO          :Stop the computer based oscillator until the
                        next readout.
      JSR F2FO          :Update data storage ponters for the next
                        readout.
      JSR F320          :Use next integration time parameter
      JMP F4FO          :Uppdate scratchpad with the "number of
                        replicates" parameter in preparation for
                        next readout
      RTS

------Set communications speed to 600 Baud. Output----------
      acknowledgement to "front-end" that data is available is about
          to be transmitted

F230  LDA #0C  :Set baud rate to 600
      JSR FF18          :Outputs acknowledgement that data has been
                        acquired and is about to be transmitted.
      RTS
```

```
----------Outputs controller data from 6 successive array----------
                  scans.

F250  LDX #06     :Load x register with the number of scans to be
                  transmitted
      LDA #00     :Set up the data base addresses $8000, $8300
                  and $8600 for indexed indirect access to data
                  through zero page addressing modes.
      STA 83
      STA 85
      STA 87
      LDA #80
      STA 84
      LDA #83
      STA 86
      LDA #86
      STA 88
      LDY #7F     :The Y register is used as the photodiode
                  counter.
      JSR F5CO    :Check if serial port is ready for byte output.
      LDA (83),Y  :Output low byte of data.
      STA DFF1
      JSR F2CO    :Output high byte of data.
      LDA (85),Y
      STA DFF1
      JSR F2CO    :Output carry byte of data.
      LDA (87),Y
      STA DFF1
      DEY         :Decrement the photodiode counter.
      BPL F268
      DEX         :Decrement number of consecutive scans
                  counter.
      BEQ F28C    :If data for all scans is transmitted then
                  finish.
      JSR F2FO    :If data for all scans has not been transmitted then
                  update data storage address.
      JMP F266    :Output data for the next scan.
      RTS

----------Transmit acknowledgement to front end indicating----------
                  that all data has been transmitted.

F290  LDX #7F
      JSR F2CO
      LDA F450,X
      STA DFF1
      DEX
      BPL F292
      RTS
```

```
----------Generate  81  (Hex)--------------------

F2AO  SEC
      LDA  #83
      SBC  #02
      RTS

-------------Generate   01----------------------

F2BO  SEC.
      LDA  #3C
      SBC  #3B
      RTS

-------Reset and poll the serial port to check if it is ready for byte output--------

F2CO  LDA  #11            :Master Reset; 8 Data Bits, 1 Start, 2 Stop Bits.
      STA  DFFO
      LDA  DFFO           :Check if ready for byte output
      AND  #03
      BEQ  F2C5
      RTS

--------Start  oscillator  for  array  clocking  and----------------------
          send a start pulse to the array

F2DO  JSR  F4DO           :Start computer based oscillator for array clocking.
      LDA  #10            :Pulse PB4 high, PB4 of 6522 #1 acts as the start
                          pulse  output.
      STA  DFD2
      LDA  #OO
      STA  DFDO
      LDA  #00
      STA  DFDO
      LDA  #10
      STA  DFDO
      RTS

----------Update  data  storage  addresses  for  the  next  readout--------

F2FO  CLC
      LDA  #80      :The address is incremented by adding $80 to the
                    base addresses stored in zero page.
      ADC   83
      STA   83
      LDA   84
      ADC  #00
      STA   84
```

```
       CLC
       LDA  #80
       ADC   85
       STA   85
       LDA   86
       ADC  #00
       STA   86
       CLC
       LDA  #80
       ADC   87
       STA   87
       LDA   88
       ADC  #00
       STA   88
       RTS

-----Update the integration time scratchpad area for the next----------
                    readout

F320   LDX   82      :Initial data in $0082 ($03) which when used
                     as offset to $7F00 references the low byte
                     of the integration time parameter
       LDA  7F00,X
       STA DBFD      :Low byte relocated to scratchpad
       INX
       LDA  7F00,X
       STA DBFC      High byte relocated to scratchpad
       INX           :Index is incremented and used to update $0082
       STX   82
       RTS

---------Output acknowledgement to front-end that data has been acquired and
                  is about to be transmitted

F340   LDX  #71
       JSR  F2C0     :Check that transmit bit of ACIA is set
       LDA  F350,X   : Transmit ASCII charactor
       STA  DFF1
       DEX
       BPL  F342
       RTS
```

```
----ASCII Character TABLE used for output as acknowledgements to front end-----

F350

 "

 "

F4DF



---------Stops timer which generates alternative oscillator for array on PB7------

F4EO   LDA  #00      :Store zero in low byte register of T1, 6522#2
       STA  DFE4
       LDA  #00      :Store zero in high byte register of T1, 6522#2
       STA  DFE5
       RTS

-------Update the number of replicates for this scan in scratchpad---

F4FO   LDX   81      :Relocate replicate data for next readout parameter, from
                      parameter buffer to scratchpad location $DBFA
       LDA  7F13,X
       STA  DBFA
       INX           :By incrementing X-register it is now ready to be used
                      to access the replication parameter for the
                      next readout
       STA   81
       JMP  F18E

-------Generate a start pulse and trigger array readout-------------------------

F500   LDA  #10      :Make PB4 of 6522#1 an output
       STA  DFD2
       LDA  #00      :Initially set at at zero
       STA  DFDO
       LDA  #00
       STA  DFDO
       LDA  #00
       STA  DFDO
       LDA  #10      :This positive edge activates (triggers) the array
       STA  DFDO
       RTS
```

```
-----Controls parameter transmission from front-end to all processors ------

F520  JSR F540      :Receive code indicating auxiliary from front-end
                    and store it at scratchpad location $7F00
      AND #FF
      BEQ F533      :If code is zero look for controller's parameters
      JSR F600      :Access network control data at ($F5C0-C5) using code
                    recieved.
                    Trigger auxiliary and open the network allowing serial
                    communication between the auxiliary and the front-end.
      JSR F560      :Monitor for trigger (logic "1") from
                    auxiliary
      JSR F5EO      :Open network for controller/front-end serial
                    coommunications.
      JMP F520 :    Monitor front-end for next code.
      JSR FOEO      :Receive controller's integration time and
                    replicate parameters from front-end.
      RTS

--------Look for code indicating a particular auxiliary----------

F540  LDX #04       :Read serial port for code, repeat four times (the first three
                    bytes are ignored and are switching transients on network)
      JSR F940 :
      STA 7F00      :Store code in scratchpad location $7F00.
      DEX
      BPL F742
      RTS


            ***NB. The code is also transmitted four times
            from the front-end. This deals with the occasion when
            no switching transient arises.

--------Control multiplexer/demultiplexer network to connect the serial lines of
      auxiliary to the front-end. This routine exits with PA3-PA7 configured as
      inputs

F550  LDX #07       :Configure bits controlling network (PAO-PA2) as outputs.
      STA DFE3
      LDX 7FOO      :Place code in X-index register as an index to obtain the
                    correct network control data for that auxiliary .
      LDA F5BF,X    :Access data for opening the correct network channel
                    from the data table
      STA DFE1      :The PA3-PA7 VIA I/O lines of the controller
                    are interfaced to
                    the CA2 control lines of the auxiliaries.
                    Since the PA lines are
                    programmed as inputs not outputs on this occasion then
                    any data written to the ports is ignored by the auxiliaries
      RTS
```

```
-----Poll for a '1' at the CA2 - PA control interface for indication that the ----
              auxiliary has finished the present task

F560  LDA  #07
      STA  DFE3
      LDA  DFE1
      AND  #F8
      BEQ  F565
      RTS

-----Send an acknowledgement to the front-end indicating that the controller has
        recieved its parameters, then send a pulse to all CA2 auxiliary inputs as a
        trigger for them to commence data acquisition

F570  JSR  F120      :Send acknowledgement to front-end
      LDA  #FF       :Configure all channels PA lines of
                     6522#2  outputs
      STA  DFE3
      LDA  #00       :Assert logic "O" on all 6522#2 PA I/O lines including the
                     network control lines PA0-PA2 which
                     maintain the serial communications lines
                     with the front-end for the controller open
      STA  DFE1
      LDA  #F8       :Send a "positive edge" trigger (ie. logic "1") to PA3-PA7
                     lines of J3 while keeping the network open for
                     the controller ie.PAO-PA2 at logic"0"
      STA  DFE1
      JSR  F5D0      :Delay a few microseconds (not essential)
      LDA  #00       :The PA3-PA7 lines are configured as logic "0" again
      STA  DFE1
      LDA  #07       :The PA3-PA7 lines are configured as inputs before exiting
                     while the PAO-PA2 lines are maintained as outputs
      STA...DFE3
      RTS

-------Controls sequence of operations neccessary for successful data -------
           transmission to the host. Sends as acknowledgement
            after transmission  of data from an auxiliary

F5AO  JSR  F540      :Look for code from front-end indicating which
                     auxiliary it requires data from
      AND  #FF
      BEQ  F5B9      :If "0" then return to start of control sequence
      NOP
      NOP
      NOP
      JSR  F600      :Send trigger ie. positive edge to auxiliary and
                     open network for auxiliary to communicate with front-end.
      JSR  F560      :Look for logic "1"  as a trigger from auxiliary.
      JSR  F5EO      :Open network for controller.
      JSR  F290      :Send acknowledgement that data has been
```

```
                transmitted by the auxiliary.
      JMP F5AO  :Return and look for the next code.
      RTS.

----------Delay Routine (microseconds)----------

F5DO  LDY #02
      DEY
      BPL F5D2
      RTS

---------Open network for controller/front-end serial coommunications.

F5EO  LDA #07     :Configure network I/O lines PA3-PA7 as inputs
                  and PAO-PA2 outputs
      STA DFE3
      LDA #00     :Configure PA3-PA7 to allow controllers/front-end
                  communication before exiting subroutine.
      STA DFE1
      RTS

-----Open the network for auxiliary/front end serial communications and trigger
                  the auxiliary processor
            ****NB CODE 02 is auxiliary #1,
                 CODE 03 is auxiliary #2
                 CODE 04 is auxiliary #3...etc....

F600  LDA #07     :Make network control lines outputs and the
                  CA2-PA control lines inputs.
      STA DFE3
      LDX 7F00    :Place the code for the auxiliary in the X-register
                  and use it to access data to trigger the auxiliary
                  and control serial communications with the front-end
      LDA F5BF,X
      AND #07     :Keep only the network control data and open the
                  serial communications for the auxiliary
      STA DFE1
      JSR F5DO    :Delay a few microseconds
      LDA F5BF,X  :Access the data for the auxiliary again and this
                  time make the appropriate PA-CA2 line an output
                  without affecting the remaining lines on thkis port.
      ORA #07
      STA DFE3
      LDA F5BF, X :Using this data again output logic "0" to
                  appropriate CA2-PA (to trigger the auxiliary)
                  line while keeping serial communications open for this
                  auxiliary
      AND #07
      STA DFE1
      LDA F5BF,X  :Using this data output a "1" logic level on the
                  CA2 line (this acts as a positive edge trigger for
                  the auxiliary)
```

```
        STA  DFE1
        AND  #07        :Again a logic "0" is output on the CA2 line.
        STA  DFE1
        ORA  #07        :All the CA2-PA lines are configured as inputs
                         on exiting this routine.
        STA  DFE3
        RTS
```

---- This routine triggers an auxiliary (depending on whichever code is in -- scratchpad at $7F00) to monitor its open serial port. The controller now waits for a trigger pulse back from the auxiliary indicating that it has finished communicating with the front-end. On recieving this trigger, the controller reopens serial communications with the front-end and returns to its own monitor program

```
F640    JSR  F600       :Send positive edge to auxiliary
        JSR  F560       :Monitor for trigger ("1") indicating auxiliary is finished
        JMP  FC00       :Open network for controller and return to
                         the monitor program.

-----------------Vectored  Reset  interrupt  routine-----------

FC00    LDA  #07        :Vectored Reset interrupt routine. Opens network
                         for the controller and immdeiately jumps to
                         John Bell monitor program. Communicates with front-end
                         at 110 Baud.
        STA  DFE3
        LDA  #00
        STA  DFE1
        JMP  FD00       :John Bell Monitor.

--------------Manufacturer's  monitor  program-----------------

FD00
  "
  "
FFFF
```

```
----------Modification to manufacturers monitor program to allow------
                  software controlled serial communications with
                     front-end on startup.

FF11  LDA  #00      :Indexing data (00) for 110 Baud serial
                     communications.
      NOP
      NOP
      NOP
      NOP
      NOP
FF18  TAY           :Data in accumulator used to set the required baud rate.
      LDA #DO
      STA DFEB
         etc.


------------------------Vectored   addresses--------------------------

FFFC  00          :Custom vectored RESET subroutine pointing
                   to startup program at address ($FC00)
FFFD  FC          :Vector address($FF00) used by monitor program
FFFE  00
FFFF  FF
```

APPENDIX 7

APPENDIX 7 Programs for the Auxiliary Processors

```
HEX.      ASSEMBLY      COMMENTS
ADD-      CODE
RESS
F000  LDA #0C   :Set serial communications a  a BAUD RATE of 600
      JSR FF18
      JMP F900  :Routine for continuous re  ut of the photodiode
                array.

----------MAIN  PROGRAM----------

F010  LDA #0C   :Communicate at 600 Baud for parameter setting
                and data transfer.
      JSR FF18
      JSR F090  :Setup scratchpad for T1 integration time timer.
F018  JSR F520  :Looks for trigger from controller and then takes new
                parameters from host
      JSR F0F0  Transfer erroneous data to zero page for correction of
                the parameter list.
      JSR F100  :Makes corrections for transmission errors, uses data in
                zero page.
      JSR F530  :Acknowledge parameters received; trigger controller
                to take over communications; wait for trigger before
                data acquisition.
      JSR F130  :Acquire data from photodiode array.
F027  JSR F230  :Look for trigger from controller and set transmission
                rate at 9600 Baud.
      JSR F250  :Transmit data from 6 consecutive readouts.
F02D  JSR F556  :Trigger the controller to resume communication
                over the network.
F030  JMP F650  :Transmit the final two bytes of data
                and then return to start to monitor for new
                parameters.

----------SETUP OF SCRATCHPAD FOR T1 INTEGRATION TIME TIMER--

F090  LDA #07   :Placing 0780 in register for Timer T1 generates output
                pulses of period 3.22 milliseconds on PB7
      STA DBFE
      LDA #80
      STA DBFF
      RTS
```

```
----------Acquire 99 ($63) bytes of parameter data from "front-end"-----
                  (The three initial bytes recieved are not parameter data and result
                  from switching transients which arise when the serial lines
                        are connected to the front-end by the controller,these
                              bytes are logged but ignored)

FOEO  LDX #63
      JSR F940
      STA 7F00,X
      DEX
      BPL FOE2
      RTS

----------Transfer erroneous address data to zero page----------------

FOFO     LDX #20
      LDA 7F00,X
      STA 00,X
      INX
      TXA
      CMP #60  :Check if 96 bytes have been transferred.
      BNE FOF2
      RTS

------Correct the data (locations where errors were detected -------
         before parameter transmission) in zero page for
               01 and $81 errors.

F100  LDX #3E  :Data was downloaded into locations $00-3E of zero page
               $3E is high byte of first address.
      JSR F2BO :Generate 01 in accumulator
      STA (00,X)   :01 will be stored at the address stored at the indicated
               location given in zero page. If no address is present then
               01 is continually loaded into 0000.
      DEX
      DEX
      TXA      :The X register is decremented twice to point to
               the next zero page location.
      CMP #1E  :The first 20 addresses were used for "O1" errors.
      BNE FI02
      LDX #40  :The locations $0040-0060 were reserved for
               addresses having "$81" code errors.
      JSR F2A0 :This routine generates "$81".
      STA (00,X)
      INX
      INX
      TXA
      CMP #60  :When $0060 is reached then finish.
      BNE F110
      RTS
```

```
----------Transmit acknowledgement to "front-end" indicating that parameters
                                    have been recieved

F120   LDX #7F
       JSR F2CO      :Set up serial port for output.
       LDA F3DO,X    :Output ASCII characters from character table stored in ERROM.
       STA DFF1
       DEX
       BPL F122
       RTS

---------Acquire and store data sequentially from 6 successive-----
                              readouts.

F130   CLD           :Clear decimal mode
       SEI           :Set the interrupt
       LDX #00       :Place zero in all buffer memory locations
       LDA #00
       STA 8000,X
       STA 8100,X
       STA 8200,X
       STA 8300,X
       STA 8400,X
       STA 8500,X
       STA 8600,X
       STA 8700,X
       STA 8800,X
       DEX
       BNE F136
       LDA #05       Place number of consecutive scans in zero page
                   location $0080.
       STA 80
       LDA 01      :Place number of replicates in $0081.
       STA 81
       LDA #03       :$7F03 is where low byte of second integration
                   time parameter is.  Data in location $0082 will
                   later be used as an index to locate integration time.
       STA 82
       LDA #00     :The base address($8000) for low byte of data is placed
                   in zero page.
       STA 83
       LDA #80
       STA 84
       LDA #00     :The high byte base address is placed in zero page
       STA 85
       LDA #83
       STA 86
       LDA #00     :The carry byte base address is placed in
                   zero page.
       STA 87
       LDA #86
```

```
STA 88
NOP
NOP
NOP
NOP
LDA 7F13    :The number of replications for initial scan is
         placed in scratchpad $DBFA.
STA DBFA
LDA 7F01    :Low byte integration time parameter is transferred
         from parameter file to scratchpad.
STA DBFD
LDA 7F02    :High byte integration time parameter is transferred
         from parameter file to scratchpad.
STA DBFC
LDX DBFA    :Number of replicates is placed in X-register.
LDA #00  :Make CA2 and CB2 control lines -ve edge active.
STA DFDC
JSR F500 :Output a start pulse to clear array.
LDA #E0  :Set T1 as pulse output on PB7 and T2 as counter
         on PB6.
STA DFD4
LDA #80     :Place count ($0780) in T1 allowing the generation of
         pulse of 3.125 milliseconds on PB7.
STA DFD5
LDA #07
STA DFD5
LDA DBFD    :Set  integration count in the T2 timer register using data in
             $DBFD (Low byte) and $DBFE (High byte).
STA DFD8
LDA DBFC
STA DFD9
LDA #20  :On the timing out of T2 proceed to read out the
         array.
BIT DFDD
BEQ F1B8
JSR F2D0 :Start oscillator for array clocking and send
         start  pulse.
LDA DFD1    :Clear CA1 and CB1.
LDA DFD0
LDA #00  :Make PA and PB lines inputs.
STA DFD2
STA DFD3
LDY #7F  The y-register is used as the diode counter.
CLC
LDA DFDD    :Look for the array readout start pulse on CA1.
AND #02
BEQ F1D1
LDA DFDD    :Poll for sampling pulse on CB1.
AND #10
BEQ FID8
LDA DFD1    :Load the high byte and store.
ADC (83),Y
```

```
      STA  (83),Y
      LDA   DFDO  :Load the low byte and store but first eliminate the
                  4 bits which are not data.
      AND  #OF
      ADC  (85),Y
      STA  (85),Y
      LDA   (87),Y:Save the carry bit.
      ADC  #00
      STA  (87),Y
      DEY         :Decrement the diode counter.
      BNE  F1A4
      NOP
      NOP
      DEC  80     :Decrement the "number of consecutive scans"
                  counter.
      BM1  F20D
      JSR  F4EO       :Stop the computer based oscillator until the next readout.
      JSR  F2FO       :Update data storage ponters for the next
                      readout.
      JSR  F320       :Use next integration time parameter
      JMP  F4FO       :Uppdate scratchpad with the "number of replicates"
                    parameter in preparation for next readout
      RTS

--------Look  for  trigger  from  controller  before  transmitting-------
           data to the  "front -end" at 9600 Baud.

F230  LDA #OC               :Set communications for 600 Baud.
      JSR  FF18:
      JSR  F540             :Look for trigger from controller before
                          transmitting  data.
      JSR  F340             :Set data transmission rate for 9600 Baud.
      RTS

                        --------This routine is not used --------

F23D  LDA  DFED
      AND   #02
      BEQ  F23D
      JSR  F340
      RTS

----Transmit  data  from  six  successive  photodiode  array  scans--------
                          to the "front end" .

F250  LDX  #06      :Load x register with the number of scans to be
                  transmitted
      LDA  #00      :Set up the data base addresses $8000, $8300
                  and $8600 for indexed indirect access to data
                  through zero page addressing modes.
      STA  83
      STA  85
```

```
       STA  87
       LDA  #80
       STA  84
       LDA  #83
       STA  86
       LDA  #86
       STA  88
       LDY  #7F  :The Y register is used as the photodiode
                 counter.
       JSR  F5CO      :Check if serial port is ready for byte output.
       LDA  (83),Y    :Output low byte of data.
       STA  DFF1
       JSR  F2CO      :Output high byte of data.
       LDA  (85),Y
       STA  DFF1
       JSR  F2CO      :Output carry byte of data.
       LDA  (87),Y
       STA  DFF1
       DEY       :Decrement the photodiode counter.
       BPL  F268
       DEX        :Decrement number of consecutive scans
                 counter.
       BEQ  F28C :If data for all scans is transmitted then
                 finish.
       JSR  F2FO If data for all scans has not been transmitted then
                 update data storage address.
       JMP  F266 :Output data for the next scan.
       RTS

----------Transmit acknowledgement to front end indicating----------
                    that all data has been transmitted.

F290   LDX  #7F
       JSR  F2CO
       LDA  F450,X
       STA  DFF1
       DEX
       BPL  F292
       RTS

-------------Generate  81  (Hex)  ----------------------

F2AO      SEC
       LDA  #83
       SBC  #02
       RTS
```

```
-----------Generate   01------------------

F2BO  SEC
      LDA  #3C
      SBC #3B
      RTS

---------Poll serial port to check if it is ready to transmit--------
          the next byte.

F2CO  LDA  DFFO
      AND  #03
      BEQ F2CO
      RTS

------------Start oscillator for array clocking and send----------
                a start pulse to the array.

F2DO  JSR F4DO      :Start computer based oscillator for array clocking.
      LDA  #10      :Pulse PB4 high, PB4 of 6522 #1 acts as the start pulse
                    output.
      STA  DFD2
      LDA  #00
      STA  DFDO
      LDA  #00
      STA  DFDO
      LDA  #10
      STA  DFDO
      RTS

---------------Setup data storage base addresses for next-------------
                              readout.

F2FO CLC
      LDA  #80      :The address is incremented by adding $80 to the
                  base addresses stored in zero page.
      ADC  83
      STA  83
      LDA  84
      ADC  #00
      STA  84
      CLC
      LDA  #80
      ADC  85
      STA  85
      LDA  86
      ADC  #00
      STA  86
      CLC
      LDA  #80
      ADC  87
      STA  87
```

```
       LDA  88
       ADC  #00
       STA  88
       RTS

-----Update the integration time scratchpad area for the next----------
                    readout

F320   LDX   82      :Initial data in $0082 ($03) which when used as offset to
                     $7F00 references the low byte of the integration time
                     parameter
       LDA  7F00,X
       STA DBFD      :Low byte relocated to scratchpad
       INX
       LDA  7F00,X
       STA DBFC      :High byte relocated to scratchpad
       INX           :Index is incremented and used to update $0082
       STX   82
       RTS

--------------Go to subroutine which sets baud rate to 9600----------
                      and serial, port for 8 data bits per byte .

F340   JSR  F630
       RTS

-----------Output indication to front end that photodiode array data has been-
                               acquired.

F345   LDA   F350,X:Transmit ASCII charactor
       STA  DFF1
       DEX
       BPL  F342
       JSR  F630 : Set baud rate at 9600 and serial port to transmit eight
                   data bits per byte
       RTS

----ASCII Character TABLE used for output as acknowledgements to front end

F352
  '
  '
  '
F4DF
```

```
---------Stops timer which generates alternative oscillator for array on PB7-----

F4EO  LDA  #00      :Store zero in low byte register of T1, 6522#2
      STA  DFE4
      LDA  #00      :Store zero in high byte register of T1, 6522#2
      STA  DFE5
      RTS

-------Update the number of replicates for this scan in scratchpad---

F4FO  LDX   81      :Felocate replicate data for next readout parameter, from
                    parameter buffer to scratchpad location $DBFA
      LDA  7F13,X
      STA  DBFA
      INX           :By incrementing X-register it is now ready to be used
                    to access the replication parameter for the
                    next readout
      STA   81
      JMP  F18E

-------Generate a start pulse and trigger array readout-------------------------

F500  LDA  #10      :Make PB4 of 6522#1 an output
      STA  DFD2
      LDA  #00      :Initially set at at zero
      STA  DFDO
      LDA  #00
      STA  DFDO
      LDA  #00
      STA  DFDO
      LDA  #10      :This positive edge activates (triggers) the array
      STA  DFDO
      RTS

---------Monitor for a positive edge on the CA2 line----------------
                acquire new parameters

F52O  JSR  F580     :Assert CA2 Line "O"
      JSR  F540     :Look for a positive edge from controller.
      JSR  F580     :Assert CA2 logic "O" when exiting.
      JSR  FOEO     :Look for new parameters by polling
                    serial port.
      RTS

-------Acknowledge that parameters have been received.-----------
          Trigger the controller to resume communications
          with front end. Await a positive edge on CA2 before starting
        data acquisition.


F530  JSR  F120     :Send acknowledgement that parameters
```

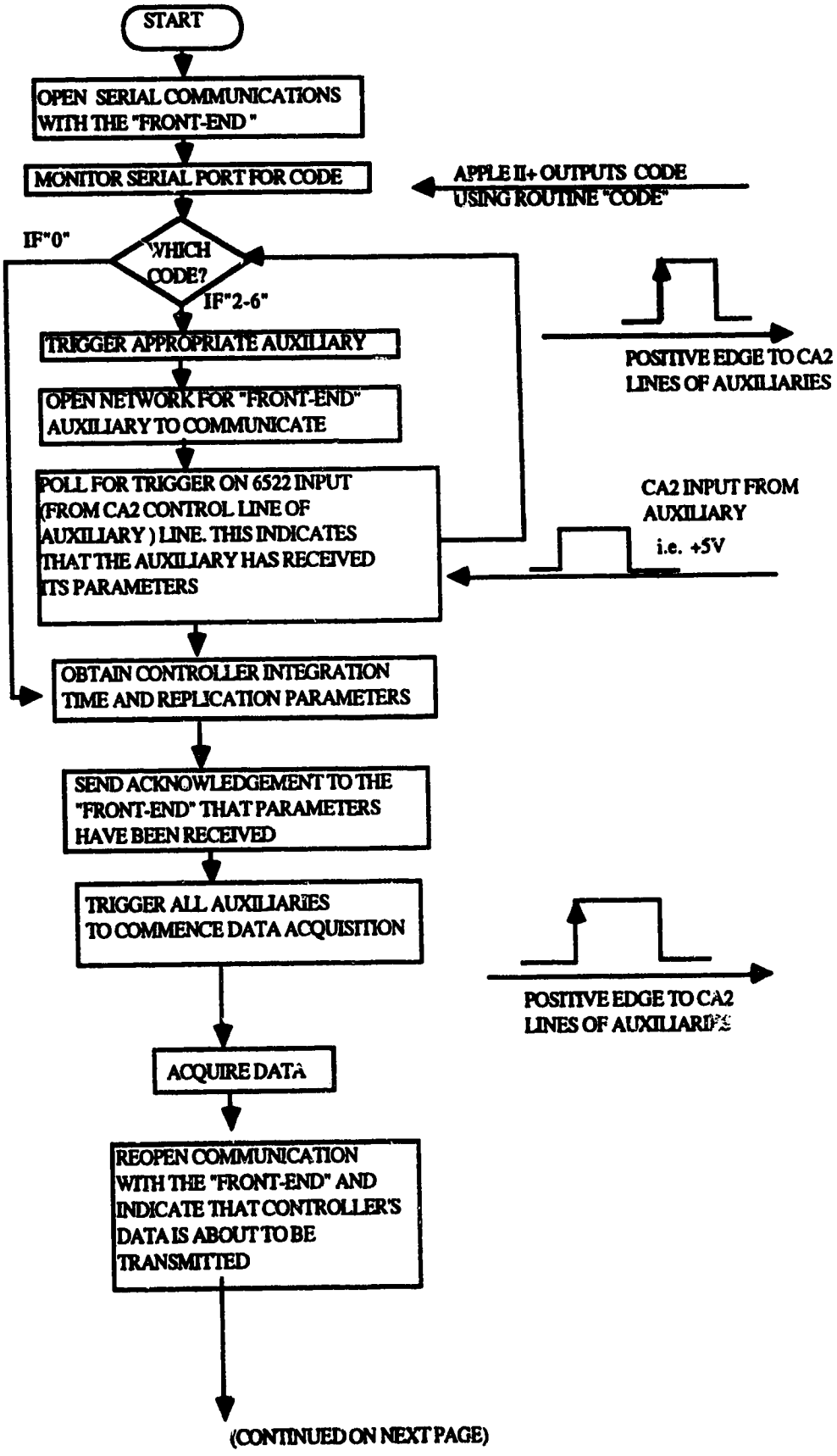
```
                have been received.
      JSR F570  :Make CA2 logic "1" for a few milliseconds.
      JSR F580  :Reassert CA2 to "0" logic level.
      JSR F54O  :Monitor for positive edge on CA2 and reassert
                "O" logic on CA2 when exiting.
      RTS

--------Look for a positive edge (trigger) from controller----------

F540  LDA #04   :Make CA2 positive edge active.
      STA DFEC
      LDA #01   :Clear CA2 interrupt flag.
      STA DFED
      LDA DFED  :Monitor for positive edge on CA2.
      AND #01
      BEQ 074A
      JSR F580  :Make CA2 logic "O" when exiting
      RTS

------------Trigger the controller------------------------------

F556  JSR F570  :Make CA2 logic "1" for a few milliseconds.ie.
                to trigger the controller.
      JSR F580 :  Make CA2 logic "O" before exiting
      RTS

----------Delay routine ----------------------------------------

F560  LDX #02
      DEX
      BPL F562
      RTS

------------------Trigger the controller--------------------

F570  LDA #OD :Make CA2 "1".
      STA DEFC
      JSR F560 :Delay routine ensures that CA2 is kept high for about
               10 us (ample time to activate (trigger) the controller
     RTS

---------------------Make CA2 line "O" logic-----------------

F580  LDA #0C
      STA DFEC
      RTS

---------This routine allows the user to return control to the---------
           controller monitor program while placing the
            auxiliary itself in the main data acquisition routine.

F590  JSR F556 :Trigger the controller
```

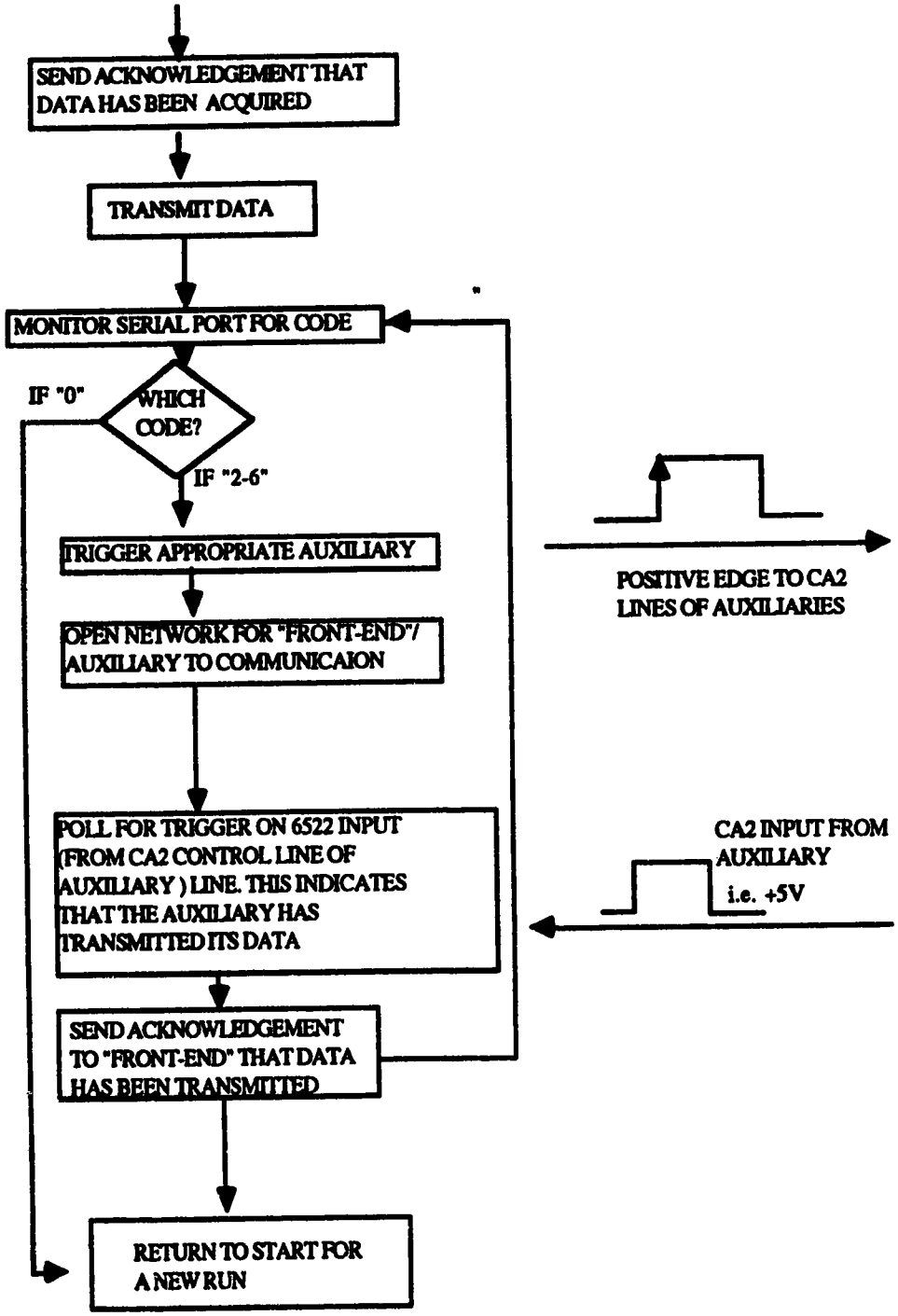
```
        JMP  FOIO :Jump to the main program and monitor for parameters
                  at 600 Baud.

---This routine allows for the rapid interchange between the controller and the
 auxiliary for interactive communication with the front-end.  This is used for
interactive manipulation and viewing of memory locations through the use of the
individual processor monitor program and for debugging

F600    JSR  F556 :Trigger the controller by making the CA2 line positive
                  for a few milliseconds.
        JSR  F540 :Wait for a positive edge from controller.
        JSR  F580 :Communicate through the serial port with the front end.
                  Make CA2 logic "O" again.
        JMP  FDOO:Go to monitor program

------Set data transmission speed to 9600 Baud and 8 data bits per byte

F630    LDA  #IC  :Set transmission rate to 9600 Baud.
        JSR  FF18
        LDA  #11  :Reset register for transmission of 8 bits per bytes.
        STA  DFF0
        RTS

----------Routine previously used to ransmit two bytes of data, now unused

F63D    JSR  FF18
        LDA  8580
        STA  DFF1
        LDA  8880
        STA  DFF1
        JMP  FOIO

------------Retransmit the final two bytes of data ---------

F650    JSR F2C0 :Check if serial port is ready to transmit data.
        LDA  8580     :Output the final low byte again .
        STA  DFF1
        JSR F2C0      :Check if serial port is ready to transmit data.
        LDA  8880     :Output the final high byte again.
        STA  DFF1
        JMP  FOIO     :Return to start and monitor for a new set of parameters.

---------This routine, activted on reset, forces the auxiliary to wait-------
                  for a trigger from the controller before
                   entering its monitor program which allows interactive
                     communication with the front end

 FCE0   JSR  F580 :Make CA2 output an output and logic "O" .
        JSR  F540 :Monitor for trigger from controller ie. a positive
                  edge on CA2 control line.
        JSR  F580 :Reaffirm a low ("O")logic level on CA2.
        JMP  FDOO:Go to the monitor program and communicate with the
```

```
                front end at 110 Baud.

---------Modification to John Bell monitor to allow software control of baud rates

FF11   LDA  #00  :John Bell monitor modified for 110 Baud
                 communication without the use of hardware jumpers.
FF12-FF17  NOP's

-----------------John  Bell  Monitor  Program-----------------

FDOO
  '
  '
  '
FFFB

--------------------------Vectored  Addresses-----------------

FFFC       EO   :Vectored RESET subroutine address ($FCE0)
FFFD       FC

FFFE       OO   :Vectored address($FF00) used by original monitor program
FFFF       FF
```

APPENDIX 8

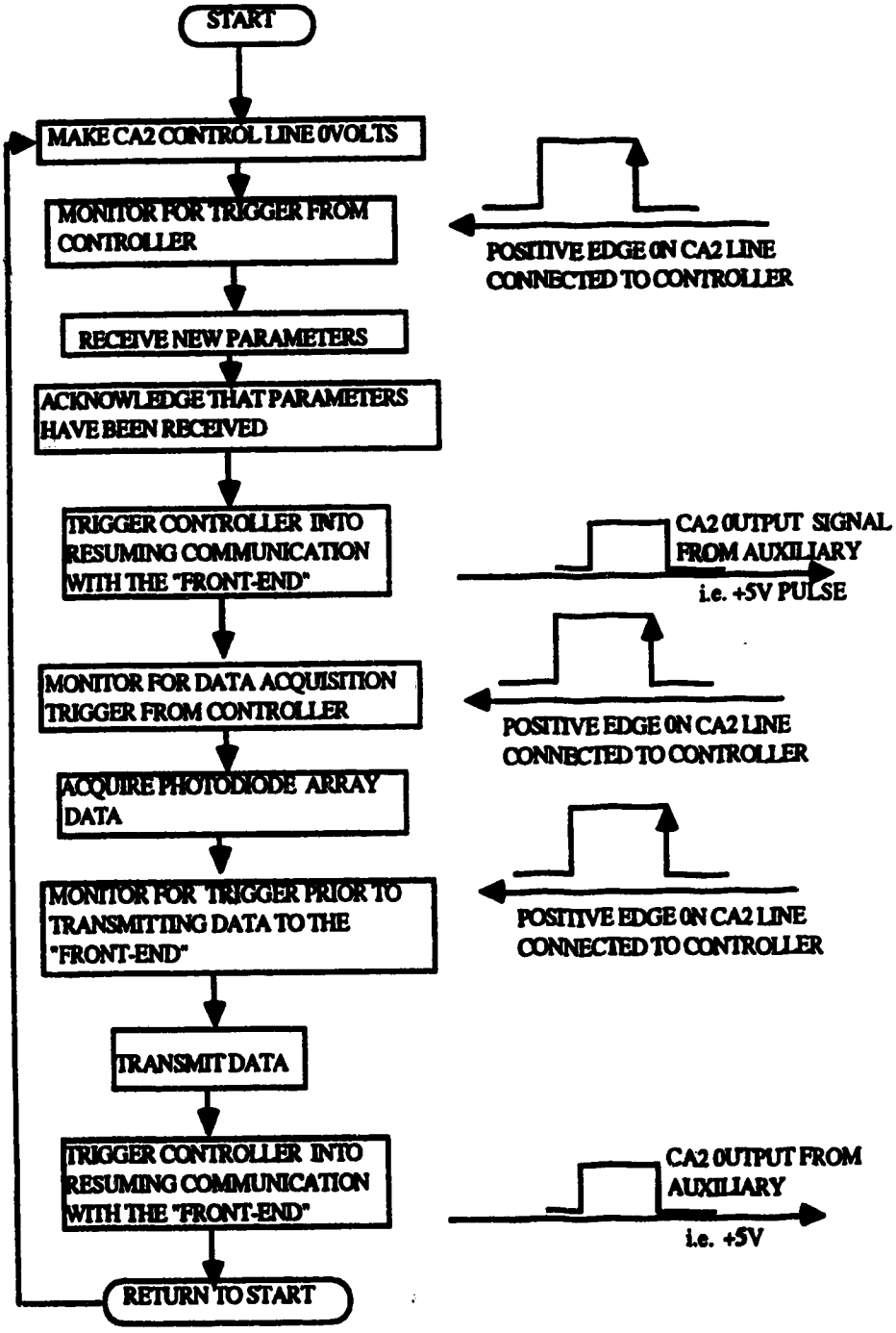
Appendix 8 Flowchart Describing Controller Operating System Program




SEND ACKNOWLEDGEMENT THAT DATA HAS BEEN ACQUIRED
TRANSMIT DATA
MONITOR SERIAL PORT FOR CODE
IF "0"
WHICH CODE?
IF "2-6"
TRIGGER APPROPRIATE AUXILIARY
OPEN NETWORK FOR "FRONT-END"/ AUXILIARY TO COMMUNICAION
POLL FOR TRIGGER ON 6522 INPUT (FROM CA2 CONTROL LINE OF AUXILIARY) LINE. THIS INDICATES THAT THE AUXILIARY HAS TRANSMITTED ITS DATA
SEND ACKNOWLEDGEMENT TO "FRONT-END" THAT DATA HAS BEEN TRANSMITTED
RETURN TO START FOR A NEW RUN
POSITIVE EDGE TO CA2 LINES OF AUXILIARIES
CA2 INPUT FROM AUXILIARY
i.e. +5V

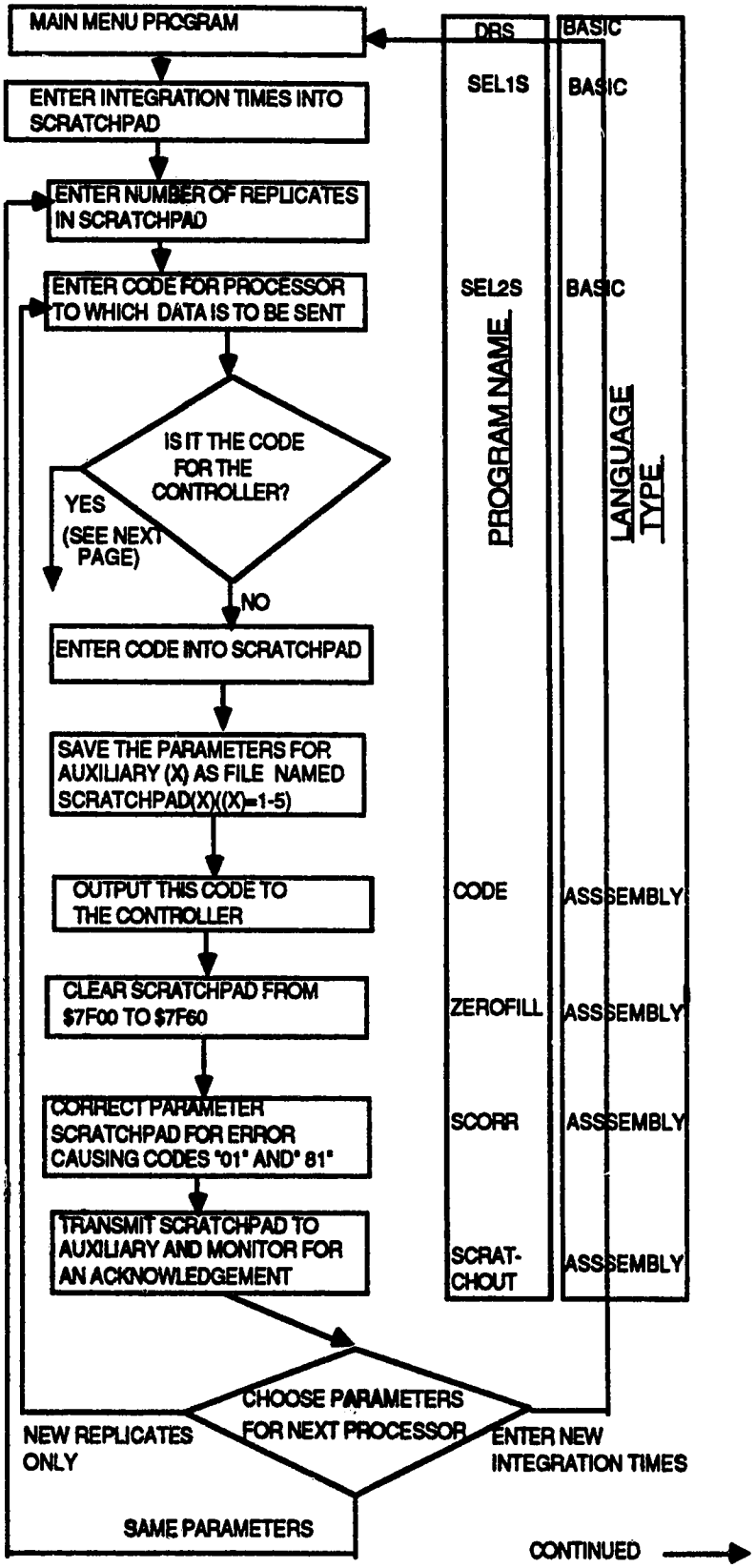
APPENDIX 9

Appendix 9 Flowchart Describing Auxiliary Operating System Program

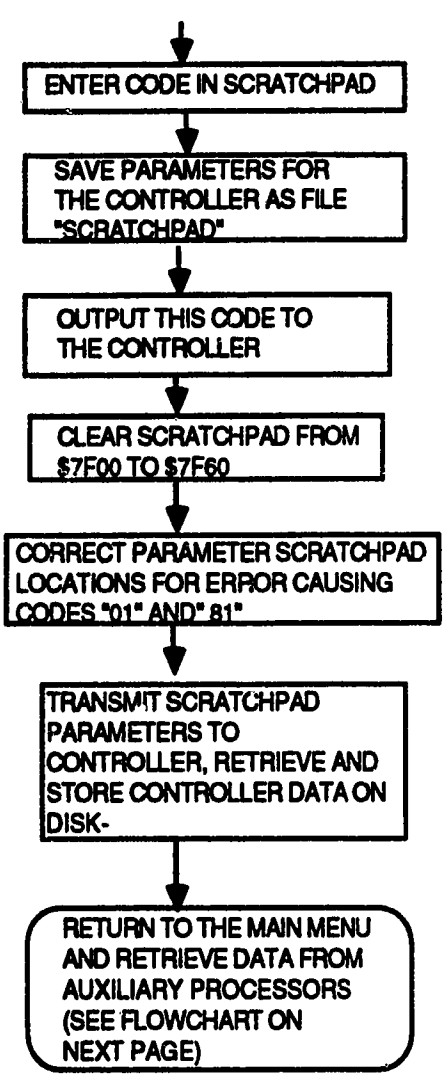


APPENDIX 10

Appendix 10 Flowchart Describing "Front-end" Operating System Program

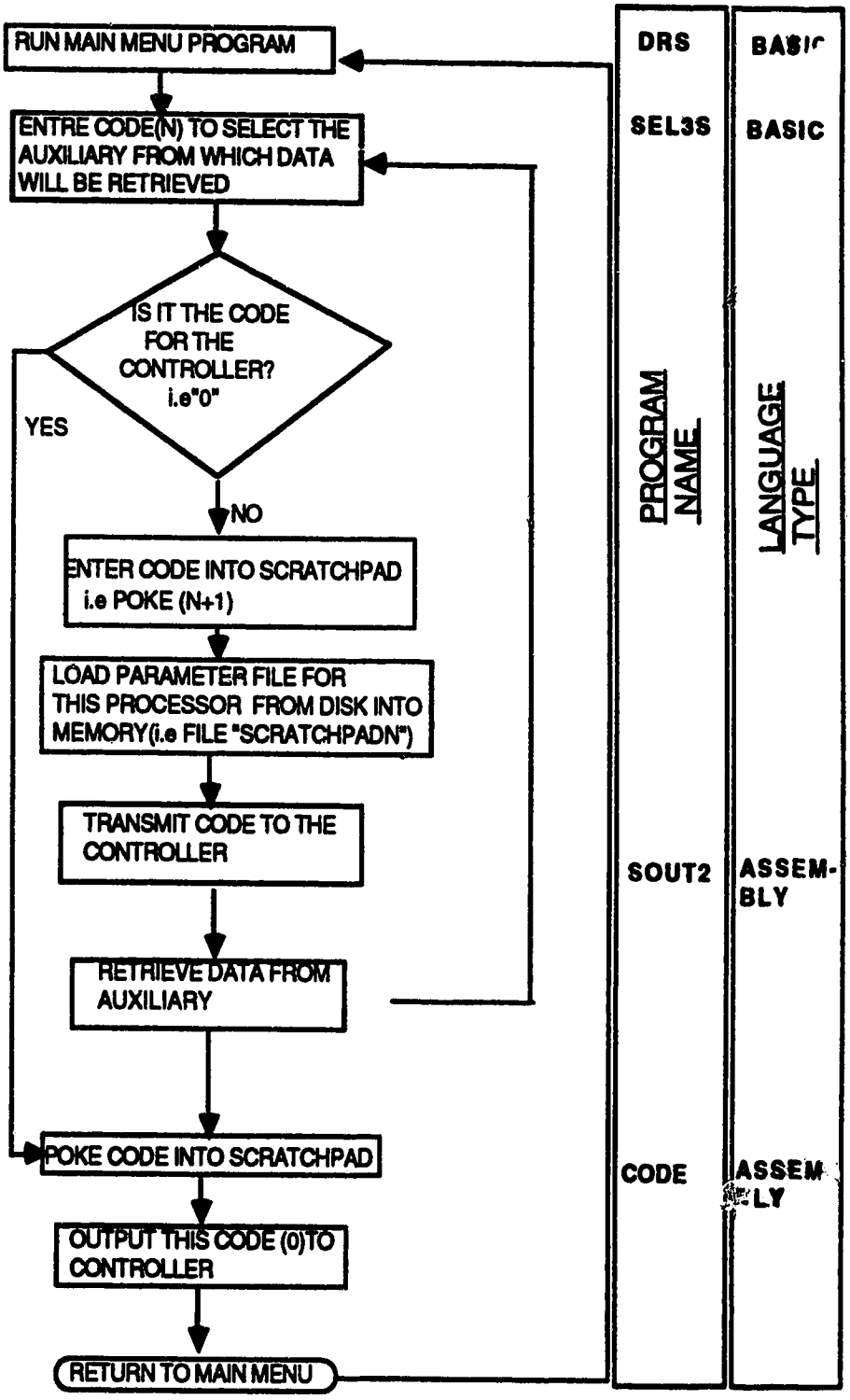


(APPENDIX 10-CONTINUED FROM PREVIOUS PAGE)



PROGRAM NAME	LANGUAGE TYPE
SEL2S	BASIC
CODE	ASSSEMBLY
ZEROFILL	ASSSEMBLY
SCORR	ASSSEMBLY
SOUT	ASSSEMBLY

APPENDIX 10 (CONTINUED-DATA RETRIEVAL FROM AUXILIARIES)



APPENDIX 11

APPENDIX 11 PLASMA OPERATING CONDITIONS

PLASMA TYPE: Plasma-Therm ICP 2500

RF GENERATOR

TYPE: Model HFP 2500F, 2.5 kW RF (27.12 MHz)

SPRAY CHAMBER: Plasma- Therm

NEBULIZER: Glass concentric (Meinhard)

POWERS USED: 1.6 kW except for Chapter 7 where 1.8kW was used

GAS FLOWRATES AND PRESSURES

PLASMA GAS : 13 Liters / minute

NEBULIZER GAS: 0.65 Liters / minute, 20 psi

AUXILIARY GAS: 0.8 Liters / minute