Energy Management Strategy for Supercapacitor in Droop-controlled DC Microgrid Using Virtual Impedance

by

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Abstract

With a proper energy management strategy (EMS), supercapacitor (SC) can be integrated into droop-controlled DC microgrid as an independent supercapacitor energy storage system (SCESS). The resulting microgrid could supply repeatedly quick bursts of electrical power due to load or source transients and improve power quality and lifetime of other distributed generations (DGs) or distributed energy storages.

In this thesis, a novel control strategy for SCESS is proposed. The method uses the virtual impedance loop to add a virtual resistor and a virtual capacitor connected in series between the converter and DC bus, which decouples power flow between SCESS and other DGs while ensuring the plug'n'play feature. The results show that the proposed EMS has a competing dynamic performance with excellent flexibility as compared to existing methods.

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List of Abbreviations

RES	Renewable energy source
SC	Supercapacitor
EMS	Energy management strategy
SCESS	Supercapacitor energy storage system
DG	Distributed generation
ESS	Energy storage system
PV	Photovoltaic
WT	Wind turbine
FC	Fuel cell
SOC	State of charge
PEMFC	Proton exchange membrane fuel cells
BESS	Battery energy storage system
MPP	Maximum power point
LVRT	Low voltage ride-through
NiMH	Nickel-metal hydride
Li-Ion	Lithium-ion
LIB	Li-Ion battery
PHEV	Plug-in hybrid electric vehicles
DoD	Depth of discharge
HPF	High-pass filter
LPF	Low-pass filter
KCL	Kirchhoff's current law
PCC	Point of common coupling
CCM	Continuous conduction mode

Chapter 1

Introduction

Increasing concerns about economic and environmental impacts of traditional fossil fuel based power generation and distribution have redirected researchers to focus on renewable energy sources (RESs). Combined with the concept of microgrid [1], Such RES based system generates clean power with value-added perks [2]. Therefore, integration of RESs to DC microgrids becomes an intriguing topic since many RESs generate DC power in nature.

However, unlike traditional centralized power generation, most RESs (e.g. wind turbines) are intermittent in nature [3]. Other clean energy choices (e.g. fuel cells) have their intrinsic limitations so that they are vulnerable to fast grid dynamics [4]. To solve these problems, supercapacitor (SC) is employed to buffer the imbalance between energy generation and demand [3]-[7]. The research reported in this thesis aims to develop an energy management strategy (EMS) for SC energy storage system (SCESS) which can provide adequate surge current compensation during sudden supply/load changes in a DC microgrid, and can therefore buffer intermittency of RESs and keeps vulnerable RESs or other energy storage elements (e.g. batteries) from supplying burst power.

1.1 Droop-controlled DC Microgrid

A. Renewable Energy and Distributed Generation

Energy scarcity, reliability and related environmental issues are becoming the biggest problems around the world. The renewable and clean energy alternatives (solar power, wind power, fuel cell, etc.) may provide a good solution for that issue to some extent. In the foreseeable future, increasing portions of electrical energy demand will be met through widespread deployment of distributed clean energy resources, namely, distributed generation (DG). Therefore, enormous efforts are

devoted to the research in integration of these clean energy generation alternatives into the mainstream energy generation and distribution systems, driven by both environmental and economic benefits.

Traditional centralized power plants are a crucial part of the electric grid. However, the stability of the system is ensured by redundancy with electromechanically controlled reconfiguration and protection [8]. The use of DG shall help to increase the grid reliability and mitigate the need for urgent generation expansion or grid upgrades. Multiple DG units with disparate dynamics are interfaced to local power distribution system via power converters with various control strategies. These power converters help decouple the dynamics between power generation, transmission and distribution networks, and help maintain power quality and stability within their local areas, which is impossible for conventional centralized power generation system.

B. Concept of Microgrid

Intermittent nature of renewable energy makes the integration of these new technologies into conventional distribution network more difficult as compared to the case of traditional power plants which have a relatively constant energy generation ability. The concept of microgrid arises from integrating those renewable energy generation of small variable nature with energy storage system (ESS) into a controllable subgrid which could autonomously work in both islanding and grid-connected modes [1] [7] [8]-[10]. Therefore, the microgrid concept becomes a widely accepted concept that consists of energy storage and generation in order to increase penetration of RESs while mitigating stresses of the existing power grid. Note that increased penetration of distributed generation in distribution system requires improved power management strategies to ensure grid safety.

Depending on the voltage type of the common bus, microgrids can be classifies as AC and DC microgrids. While a lot of work has been devoted to AC microgrid due to the dominance of AC in electricity distribution system, interests on DC microgrid are growing since many renewable energy applications such as solar panels and

fuel cells generate DC power by nature [7]. From utility grid's point of view, a connected DC microgrid can be controlled as an ideal load or power source. The distributed sources and ability to decouple the microgrid from the utility grid and provide controllability and reliable power quality [8]. The DC microgrid may also become more attractive when critical communications are avoided so that plug'n'play can be easily implemented on every distributed generation units which increases the flexibility of DC microgrid.

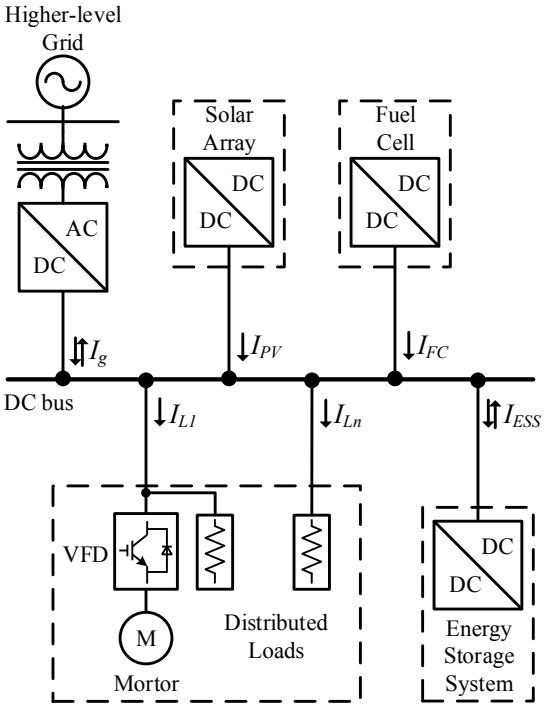


Fig.1.1 Typical configuration of a DC microgrid

Fig.1.1 illustrates the typical configuration of a DC microgrid composed of various DG units and distributed loads with local energy generation and storage. Each DG unit is interfaced with the DC microgrid through a DC/DC converter. The converters are connected to the common DC bus with their corresponding line impedance. A bidirectional DC/AC converter interfaces the DC microgrid with higher-level system such as AC microgrid or distribution system. This interlinking converter provides bidirectional power transmission ability, depending on power generation and demand between both sides. Note that ESS such as batteries is a crucial and indispensable component of DC microgrid, because ESS serves as a

buffer to balance power generation and demand within the microgrid, making microgrid's islanding operation viable.

C. Principals of Droop-controlled DC Microgrid

Unlike the case in grid-connected AC microgrid where power flow balance and voltage regulation are referred to the dominance of AC distribution system, voltage regulation and power flow management in DC microgrid is maintained by the interfacing converters, such as those for PV panels and various ESSs. For reasons such as reduced complexity or improved reliability, droop control implemented by virtual impedance control loop is the primary choice in DC microgrid [11][13]. This control strategy originated from droop control of synchronous generator and is widely used as a reliable method of voltage regulation and power flow management in AC microgrids [12][14][15]. The droop method utilizes DC bus voltage as communication link between DG units so that no additional communication is needed [14]. Plug'n'play feature for each DG is thus realized as long as controller of each DG unit complies with a pre-defined droop control slope. The principal of droop control with virtual impedance loop is briefly reviewed as follows.

In a droop-controlled DC microgrid shown in Fig.1.1, the voltage regulation of the DC bus is performed by cooperation of all DG and ESS units, so that load is shared between them without additional communication lines. This can be achieved by adding voltage-current droop control in outer voltage loop, namely, by adding virtual resistor R_{vn} for the nth DG in autonomous DC microgrid. The output voltage reference V_{refn} for the nth DG is generated by:

$$v_{refn}(t) = V_{ref*} - R_{vn} i_{on}(t) \tag{1.1}$$

where V_{ref*} is nominal voltage of DC bus, i_{on} is output current of the nth DG. The droop characteristics described by (1.1) are also shown in Fig.1.2 as a negative droop sloop.

Suppose the dynamics of inner voltage and current loops are fast enough to track

v_{refn}, the nth DG in a droop-controlled DC microgrid shown in Fig.1.1 can be modeled as a Thevenin equivalent circuit as shown in Fig.1.3.

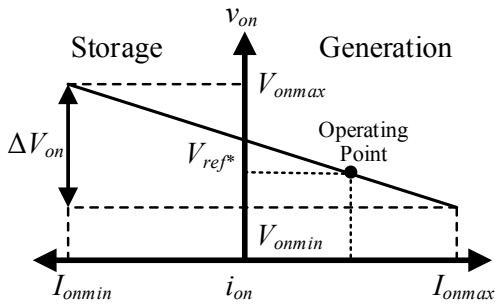


Fig.1.2 V-I droop function

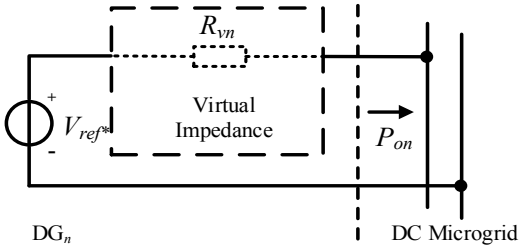


Fig.1.3 Thevenin equivalent circuit of the *n*th converter with virtual impedance loop

Then output power P_{on} of the nth DG can be derived as:

$$P_{on} = V_{bus} i_{on} = V_{bus}\left(V_{ref*} - V_{bus}\right) \times \frac{1}{R_{vn}} \tag{1.2}$$

The load sharing ratio between each DG unit is:

$$P_{o1} R_{v1} = P_{o2} R_{v2} = \cdots \qquad _n \tag{1.3}$$

1.2 Challenges in Operation of RES and ESS

Renewable energy is the energy harvested from natural resources and is able to be continuously replenished. These natural resources are not going to be exhausted and are perpetually renewed, so that energy generated by these resources are renewable and sustainable. Typical renewable energy systems (RES) ready for deployment as a DG unit include solar power or photovoltaic (PV) system, wind power or wind turbine (WT), and fuel cell (FC) systems with renewable fuels (e.g.

hydrogen, ethanol, biodiesel, etc.). Though RES brings about various advantages such as less maintenance cost, less or no waste products like greenhouse gasses or chemical pollutants compared to conventional power plants, challenges such as intermittent power output limit the large-scale application of these renewable sources. Traditionally, researchers utilize ESS to offset constraints in RES [16][17]. However, integration of ESS as an emerging technology has its intrinsic drawbacks and tradeoffs as well. This section provides a brief review on constraints in developments of RES and ESS.

A. Intermittency of solar power and wind power

Generally speaking, power harvested from PV panel and WT is considered as intermittent power generation, since their output power is not continuously available due to factors that are predictable or hard to predict [3][16]-[19].

The intermittency of solar power is contributed by two sources: the predictable source and the unpredictable one. The predictable source is caused by the changing location of the sun itself. PV panels do not produce power during night times. And their power generation of during daytime is closely associated to their relative positions to the sun. The unpredictable source of intermittency is the weather, especially the cloud cover. Though locations of large-scale solar farms are meticulously chosen so that the intermittent sources become much more predictable, conditions for small-scale PV applications as DG units in microgrids may not be that favorable. For instance, factors such as vegetation, surrounding architecture, and the rooftop's inclination angle will all add additional intermittency to PV applications in residential microgrids.

WT generates electrical power from wind's kinetic energy, so that the intermittency of wind power is closely related to the variation of wind speed. It is apparently that wind speed near a single WT is very hard to predict, indicating that the wind power is highly intermittent, as is the case in WT as a DG unit in a small-scale microgrid. On the other hand, for large-scale wind farms sprawling over a vast area, the intermittency of total output power are greatly reduced and more predictable.

Currently, intermittency of RES doesn't impose significant stress on the grid due to low penetration [18]. However, with the fast development of renewable energy, more installations of PV and WT will cause more frequent adjustments for fossil fuel plants to match power demand to power generation, which would add cost and curtail reliability. Moreover, in microgrids where power demand is met by those RES of intermittent nature, mitigating the intermittency becomes essential in order to ensure the safe operation of the microgrid.

To compensate for intermittency of RES, ESS is usually employed to store excess energy for use when needed. For large-scale solar or wind farms, renewable pumped storage and thermal storage are utilized due to economic interests. For RES as DG units in microgrids, battery and SC are the primary choices for the integration of ESS with RES [17]. Note that ESS not only helps mitigate the intermittency of RES so as to increase system's reliability, it also increases energy extracted from renewable sources. Study in [16] shows that a proper EMS for ESS cooperating with RES can allow up to three times the amount of wind energy to be absorbed by a weak grid, compared to conventional grid connection of wind farms.

B. Slow dynamics of FC

FC system is the RES that converters chemical energy from a renewable fuel into electrical power by a chemical reaction. The continuous operation of FC relies on the fuel supply. There are several types of FCs, which are categorized by the type of electrolyte used. Certain type of FC systems such as Proton exchange membrane fuel cells (PEMFC), are able to provide reliable electrical power with zero emissions. The principal diagram of a PEMFC is shown in Fig.1.4.

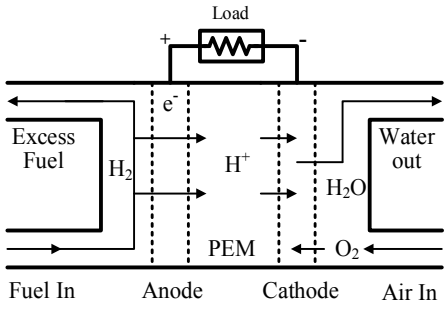


Fig.1.4 Working principal of PEMFC

The drawbacks of FC are originated from its structure and working principle. FC utilizes various expensive and vulnerable membranes (e.g. polymer electrolyte membrane for PEMFC) to conduct controllable chemical reactions. Together with facilities for constant fuel delivery and maintenance of FC's temperature and humidity, the time constant of FC system is much larger compared to switching power converter systems. This leads to troublesome long start-up period and slow dynamic response for FC system. For instance, cold start-up time for a 10 kW PEMFC system is 2.5-5s and transition of operation points takes about 2s [20]. Moreover, physical structure of membranes and electrolytes is not suitable to handle sharp changes in fuel delivery in order to avoid overheating or over air pressure, which would cause membrane degradation and shorten its lifetime as a result [20]-[22]. What's more, even the low-frequency current ripple results in the efficiency reduction of FC stack has detrimental effect on its long-term performance [4].

Therefore, in order to compensate FC's slow dynamic response in order to meet load variations and intermittency of other RES cooperating with FC, ESS with considerable energy and power density is preferable. Battery and SC are the two most widely used in combined FC and ESS systems [20].

C. Challenges associated with BESS in DC microgrid

The ESS is used to feed the grid when load power cannot be met by adjustments of electricity generation of other DGs. In small-scale microgrids such as DC microgrids, battery is commonly used to form a battery energy storage system (BESS).

In order to maintain tight voltage regulation and good power quality, electricity generation must adapt to consumption in any type of grid. However, both of power supply and demand may vary drastically over time, depending on types of DG units and load profile. With a proper EMS, the BESS is able to compensate for intermittency of various RES such as PV and WT mentioned above, by reducing their output variability. The excess energy stored in BESS can be used to support

peak demands in a DC microgrid. What's more, by integrating BESS into microgrids, curtailment of RES will be greatly reduced since BESS extends the time that PV and WT operating near their maximum power point (MPP). Other value-added benefits associated to BESS such as assisting low voltage ride-through (LVRT) are also reported in [2][23].

Currently, battery technologies include two broad categories: nickel-metal hydride (NiMH) and lithium-ion (Li-Ion) [54]. The family of Li-Ion battery (LIB) has higher power & energy density, making it the primary choice for BESS in high-power applications such as microgrids and plug-in hybrid electric vehicles (PHEV) [24] [29].

However, concerns such as lifetime and power density limit the further application of BESS. The lifespan of battery is considered to be short (cycles), as compared to other units in a microgrid. Typical lifetime for different type of LIB are from 300-2000 cycles [25].The lifetime of battery depends on many factors, such as the body temperature, number of peak currents, charge/discharge cycles, etc. Among them, the most significant factor is the number of charge/discharges cycles with depth of discharge (DoD) [26].

During charge/discharge cycles, chemical crystals are formed inside battery cells, which are hard to be re-dissolved back into the electrolyte. The crystals will grow large enough to short individual cells so that the capacity of battery is reduced with increasing internal resistance. Authors of [26]-[28] points out sharp body temperature rise is expected when batteries are supplying repeatedly burst power, resulting a lower efficiency, which would add additional charge/discharge cycles under same circumstances.

Therefore, the best way to extend the lifespan of BESS is by smoothing the output power as well as avoiding deep discharges. Research in [26] also points out that oversizing may help extend the lifetime. However, system's volume and mass are significantly increased.

1.3 Applications of SC with RES and BESS

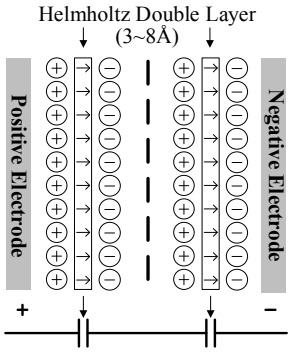


Fig.1.5 Typical construction of a SC

SC is a type of electrochemical capacitor with high capacity. A typical SC module (shown in Fig.1.5) has a capacitance hundreds times higher than electrolytic capacitors, valuing up to 100 F per unit. A SC is able to deliver electrical power much faster than batteries, and has much longer lifespan (charge/discharge cycles). A SC uses the double-layer effect to store electric energy in both electrostatic storage and electrochemical storage. The former store electric charge in Helmholtz double layer, and the latter stores energy fradaically through electrosorption and redox reactions, forming a pseudocapacitor [30].

The drawbacks of SC is its high cost and relatively low energy density as compared to batteries [17][31]. As a result, the SCESS in DC microgrid are employed to supply burst power, instead of replacing existing BESS as a pure energy storage device. As illustrated earlier in this chapter, the ability of supplying burst power without compromising lifespan makes SCESS an ideal ancillary power supply for applications of RES and BESS. Hybridization of SCESS with RES and BESS is becoming an economic way to make RESs more viable [31]. For instance, SCESS helps PV or WT mitigate the variations of output power, and hybridization of SCESS with BESS shields the battery from supplying burst current so that battery's lifespan is extended with enhanced power density [17][31][32].

In order to combine the advantages of SC and RES/BESS, while overcoming drawbacks of them, various hybridization schemes are proposed. The desired operation of hybridization is as follows: the RES/BESS unit should supply a nearly

constant load current, and prevent terminal voltage dips, while the SCESS should match the output power to the load by supplying the dynamics with an average output power of zero. There're three types of hybridization of RES/BESS and SCESS (shown in Fig.1.6), the passive hybridization, which has been widely used, the semi-active hybridization, and the parallel active hybridization [32].

The passive hybrid is the simplest and most common hybridization, studied by many researchers [33]-[35]. In the passive hybridization, the RES/BESS and SC packs are connected in parallel directly to the dc link, as shown in Fig.1.6(a). The main drawback of this topology is low utilization of the energy stored in SC since the small variation in terminal voltage of RES/BESS, especially for LIB. To

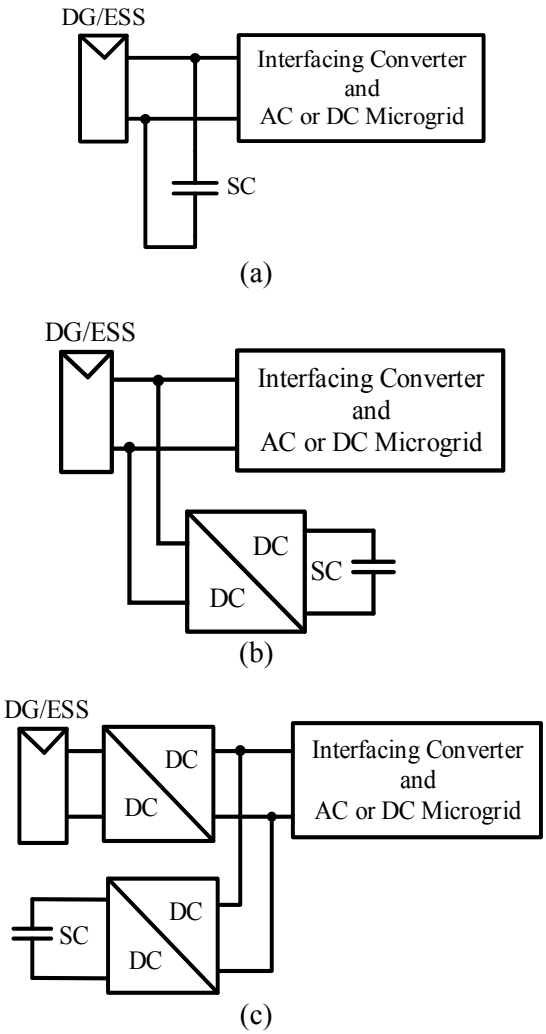


Fig.1.6 Three types of hybridization between RES and ESS. (a) Passive hybridization. (b) Semi-active hybridization (c) Parallel-active hybridization

compensate it, significant oversizing of SC is required, which adds to the overall system cost.

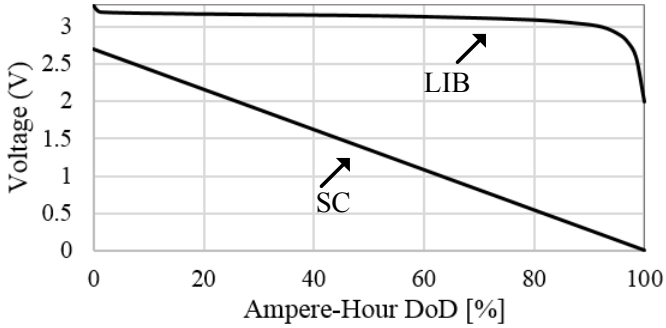


Fig.1.7 Typical discharge curves of LIB and SC cells as a function of AH DoD

Taking the hybridization of LIB and SC as an example, as can be seen on Fig.1.7, the LIB and SC has a significant difference on DoD curve, which means the passive hybridization can only utilize much smaller proportion of energy stored in SC as compared to the LIB. Another drawback is the uncontrollable current sharing between each units, which means the battery/fuel cell cannot avoid supplying surge current [32].

In the second type of hybridization, the semi-active hybridization, SC is connected to RES/BESS through a DC/DC converter, which has a wide range of input voltage in order to overcome the drawback of low utilization as analyzed above [22][37]-.[40] Therefore, the size of SC is able to be estimated and optimized [38]. The topology is shown on Fig.1.6(b). This scheme overcomes the main drawback in passive scheme at the cost of an additional converter. However, current of the RES/BESS such as FC and LIB is still uncontrollable, making it supplying part of surge current in some cases [32].

The parallel-active hybridization solves the known problems in passive and semi-active hybridization schemes. In addition, it allows a nearly constant power flow from the RES/BESS by adding an additional DC/DC converter. The topology is shown in Fig.1.6(c). All DG units become fully controllable and decoupled. Compared to the former two hybridizations, the main disadvantage of this topology is the utilization of two DC/DC converters, one rated at the load average power and another rated according to the dynamic peak power, bringing extra complexity,

control effort, and additional losses into the system [32]. Authors in [36] [41] also point out that an increased voltage operation range will cause an increase in energy loss and will speed up the degradation of SC due to increase in temperature.

The thesis focuses on the last type of hybridization since it decouples the controller and power flow between battery and SC which enables a nearly constant power flow for the battery during transients. Traditionally, SC is usually employed as a dedicated ancillary surge power supply within sensitive BESS or RES of slow dynamics, such as FC, PV and LIB systems [25][42][43]. Therefore, the majority of existing EMS approaches treat SC module as a slave current source integrated with the master converter [3][4][19][20][22][44]-[53]. Most of these methods include distributed sensors and communication lines to measure energy demands in order to provide accurate current reference to the current-controlled VSC interfacing with SC. However, with a proper EMS, SC can be deployed as independent SCESS and serve as universal surge current supply for all other DGs connected to the DC microgrid, by taking advantage of parallel-active hybridization. This may lower cost and complexity of the entire system since the dedicated SC module is no longer needed for each DG unit which is sensitive to high-frequency transients. This idea calls for realizing plug'n'play control of SCESS in a DC microgrid that traditional master-slave control approaches cannot achieve.

Recently, improvements for traditional EMS realizing plug'n'play have been proposed. These EMSs utilize HPF in the voltage loop [5] or SC's SOC [39][40] to achieve plug'n'play feature. However, these approaches have their intrinsic disadvantages, which will be analyzed in Chapter 2.

1.4 Research Objectives and Thesis Layout

As briefly discussed in the previous section, existing approaches have various drawbacks and an effective EMS for SCESS operating in a droop-controlled DC microgrid has not been proposed yet. The thesis's research objective is to fill this

gap and propose a pragmatic, concise and effective EMS for application of SCESS in droop-controlled DC microgrids.

In this work, the proposed EMS utilizes the virtual impedance loop to realize power flow management and plug'n'play feature. To make the dynamics of output current of SC estimable and controllable, the proposed EMS emulates a virtual resistor and a virtual capacitor connected in series to the output of SCESS. Together with the impedance network in the DC microgrid, the behavior of SCESS facing sudden supply or load changes could be model as a resistor-capacitor network (RC network). Then SCESS's surge current compensation effort can be evaluated and dynamically controlled by adjusting the time constant τ of the resulting RC network. Moreover, small-signal analysis suggests damping of system and stability issues are assessed by tuning the virtual resistor. Other control objectives such as SC's SOC regulation and seamless transfer between modes are also designed and modelled in the thesis. A DC microgrid prototype was built to evaluate the performance of the proposed EMS. The constructed prototype is briefly illustrated and simulation & experiment results are presented to validate the effectiveness of the proposed EMS. Comparisons with existing approaches are also carried out.

The thesis layout is listed as follows. In the rest of the thesis, Chapter 2 describes a comprehensive review of existing EMS for SCESS, addressing their features and drawbacks. Chapter 3 and Chapter 4 illustrates technical details of the proposed EMS, with detailed modelling and small-signal analysis, in order to provide design guidelines for the proposed EMS. Chapter 5 presents simulation and experiment results verifying the effectiveness of the proposed EMS. The description of the constructed experimental DC microgrid prototype is also illustrated in this chapter. The conclusions of the research and suggested future work are presented in Chapter 6.

Chapter 2

Review of Existing EMS for SCESS

The desirable EMS for SCESS operating in a droop-controlled DC microgrid should meet the following requirements:

- Mitigating intermittency of RES
- Extending lifespan for ESS
- High overall system efficiency
- The ability to coordinate with other RES and ESS units without physical communication links (Plug'n'play)

Before discussing the proposed EMS in this work, available EMS methods in literature are reviewed in this chapter. Their features and drawbacks when used in a DC microgrid are discussed. Section 2.1 presents the traditional master-slave EMS with extensive communication between DG units. Section 2.2 introduces an HPF-based voltage-controlled EMS, which realizes plug'n'play without physical communication lines. Section 2.3 presents another type of EMS based on SC's SOC to realize plug'n'play. The disadvantages of the three types of EMS are briefly analyzed.

2.1 Traditional Centralized Master-Slave EMS

Traditionally, SC is employed as a dedicated ancillary surge current supplier for coordinating with RES or ESS. As a result, traditional SCESSs are usually controlled with the centralized master-slave EMS. The centralized master-slave EMS utilizes a centralized master controller to send voltage/current references to slave converters. For a DC microgrid composed of n DG units ($DG_1, DG_2 \ldots DG_n$) interfacing with various RES, with SCESS unit and distributed loads, the global control diagram can be expressed as Fig.2.1.

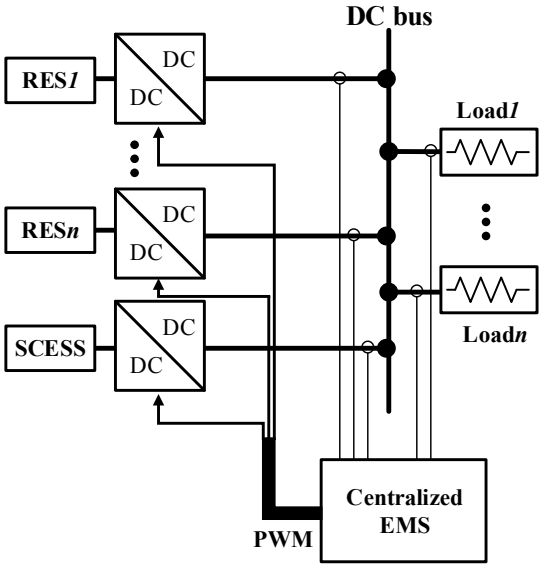


Fig.2.1 Overall control diagram of centralized master-slave EMS

As shown, the centralized controller calculates power generation and demand and allocate steady power demand to DG units while transient or surge power demand to SCESS. Physical communication lines are required to realize this type of EMS and distributed sensors are needed. Theoretically, this type of EMS shall provide excellent power sharing and surge current compensation performance since the master controller has the comprehensive supervision of the DC microgrid. In literature, this EMS is the most popular one for combined FC/SC and ESS/SC systems [3][4][19][20][22][44]-[53]. All these different ideas can be subsumed under two categories depending on the controller of SCESS.

2.1.1 Current-mode Controlled SCESS

An example control diagram of the current-mode controlled EMS for SCESS for DC microgrid is shown in Fig.2.2. As shown, the SCESS is controlled as an ancillary surge current supplier. RES/ESS DG units are coordinated by the centralized controller to regulate the DC bus voltage. The steady-state power sharing management could also be determined by the centralized controller or realized by decentralized droop control on each unit. In this category of EMS, the power generation and load power are accurately measured and filtered by a high-pass filter (HPF), in order to generate accurate current reference for the SCESS.

The SCESS is controlled as a current-mode VSC with the reference generated by HPF [3][19][20][22][44][46][47][49]-[53][55]. The regulation of SC's SOC could be added as an outer voltage loop [22], which is also shown in Fig.2.2.

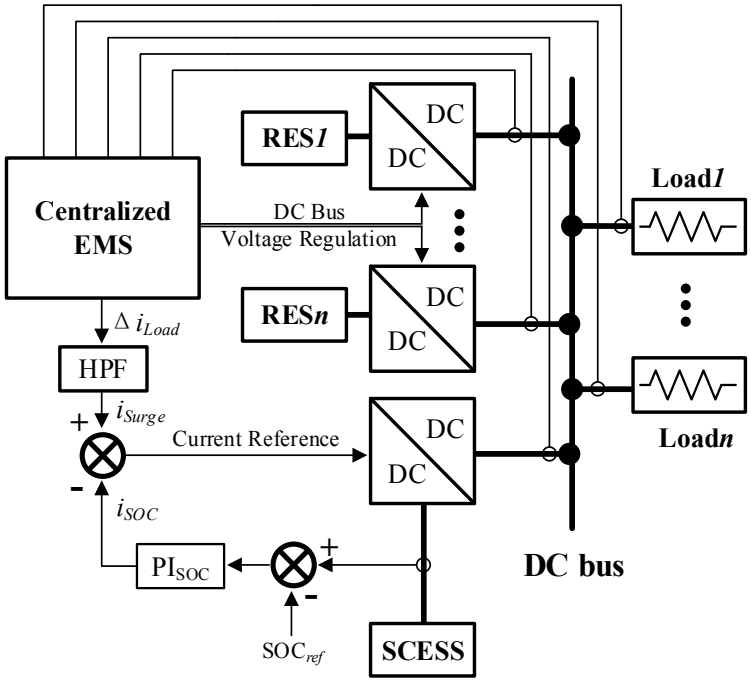


Fig.2.2 Control diagram of centralized master-slave EMS using HPF

Note that the output current of RES is designed to contain only the low-frequency load current, which could be derived as a target function $G_c(s) = i_{RESn}(s)/i_{Load}(s)$. Since only the low-frequency current is expected, $G_c(s)$ is designed to be a first-order low-pass filter (LPF) [22]. Then the HPF designed for SCESS could be designed by combining dynamic models of DG units to meet the target function.

2.1.2 Voltage-mode Controlled SCESS

For voltage-mode controlled SCESS, the SCESS participates DC bus voltage regulation directly. First type of EMS belong to this category is shown in Fig.2.3, as is proposed in [48][56]. Here the DC bus voltage control loop generates output current reference for RES/ESS units and SCESS. The current reference for DG units are filtered by a LPF so that the output current of those units only contain low-frequency variations. The SCESS will supply the rest high-frequency current to maintain the DC bus voltage.

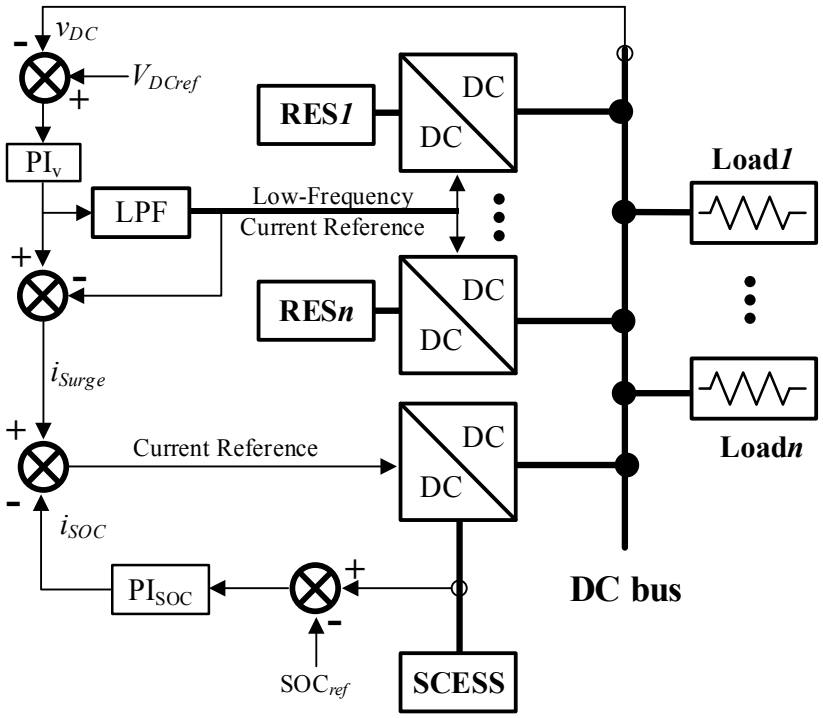


Fig.2.3 Control diagram of centralized master-slave EMS with a master DC bus regulation loop

The other type of EMS in this category is presented in Fig.2.4, as is proposed in [6][25][42][43][45][57][61]. As shown, the EMS relies on SCESS solely to regulate DC bus voltage. RES/ESS units are controlled as current sources to coordinate with SC's SOC. To enhance the dynamic performance of DG units in

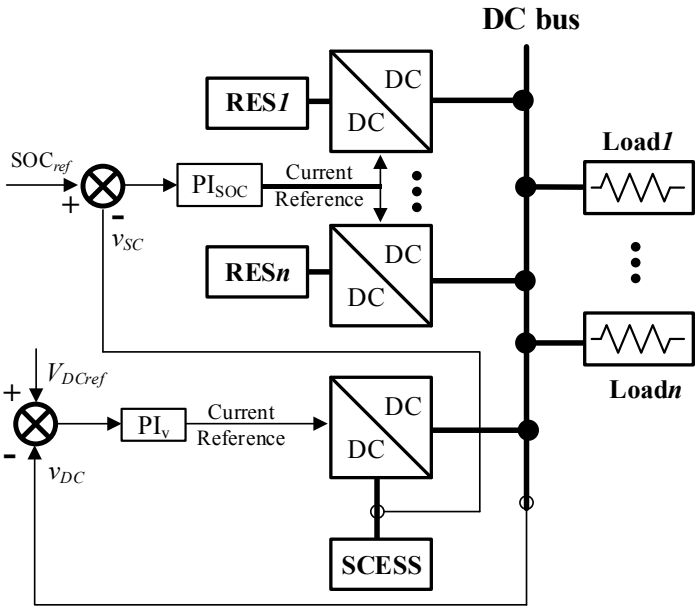


Fig.2.4 Control diagram of centralized master-slave EMS utilizing SC's SOC

DC microgrid, output power of SCESS could be filtered by a LPF and added to current loops of RES/ESS units as a current feed forward [45].
Note that extensive modeling of each DG unit is needed in order to tune the controllers, since reference of a specific DG unit is generated by dynamics of all other DG units connected to the DC microgrid [22]. The controller should be designed robust enough to stabilize the DC microgrid due to intermittency of DG units and load power.

In general, those two categories of traditional centralized master-slave EMS illustrated in this section provide excellent performance of voltage regulation and power sharing due to the centralized controller and communication lines. However, when the DC microgrid grows more complex where loads and DG units are more distributed, the resulting complexity of design of controller and maintenance of physical communication lines make this type of EMS much less favorable.

Therefore, for a DC microgrid with distributed loads and DG units of high intermittency, a decentralized EMS are needed. As stated earlier in this section, traditionally SC is employed as a dedicated surge current supplier in a specific application of RES, like LIB/SC combined storage system. However, given its fast dynamic response and longevity, the SC could be employed as an independent SCESS connected to the DC bus and provide universal surge current compensation for all DG units in the same DC microgrid. This would suggest the decentralized EMS have plug'n'play feature so that DG units could coordinate with each other as well as the SCESS without physical communication lines while maintaining good power sharing performance. The resulting solution will reduce the control complexity and overall cost since dedicated SCESS for each DG unit is no longer needed.

So far, an effective decentralized EMS for SCESS has not been proposed in literature yet. However, existing method could be modified to meet the requirements mentioned above, such as plug'n'play feature. Among them, the voltage-mode controlled EMSs have the potential of realizing plug'n'play. The

following two sections illustrates two types EMS with plug'n'play feature evolved from traditional EMSs presented earlier.

2.2 HPF-based EMS with Plug'n'play

The voltage-controlled EMS with plug'n'play feature is proposed in [5]. This method enables independent operation of SCESS, without physical communication lines, gaining the potential plug'n'play feature.

This improved method originates from the traditional EMS illustrated in the previous section. As can be seen on Fig.2.3, the current references of both SCESS and other DG units are generated by a centralized DC bus voltage regulator. Note that parallel operation of SCESS and RES/ESS DG units are only dependent on the centralized DC bus voltage regulator. As a result, this type of traditional centralized EMS has the potential to realize plug'n'play. Inspired by droop control, which is a decentralized EMS for voltage regulation and power sharing, the control diagram of the improved voltage-controlled EMS with HPF is shown in Fig.2.5.

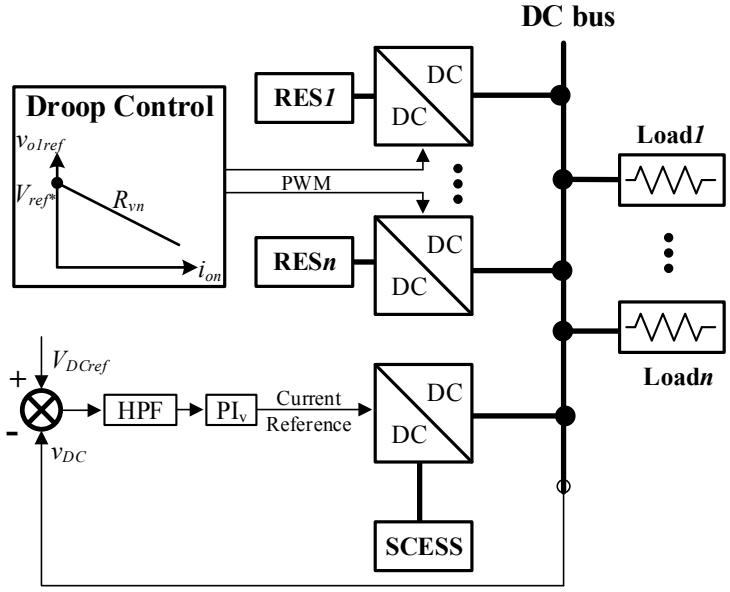


Fig.2.5 Control diagram of Improved voltage-controlled EMS with HPF

As compared to Fig.2.3, the centralized voltage controller is replaced by droop controller with virtual resistance loop. The EMS uses HPF to generate current reference for surge current compensation. To limit the current slope for DG units

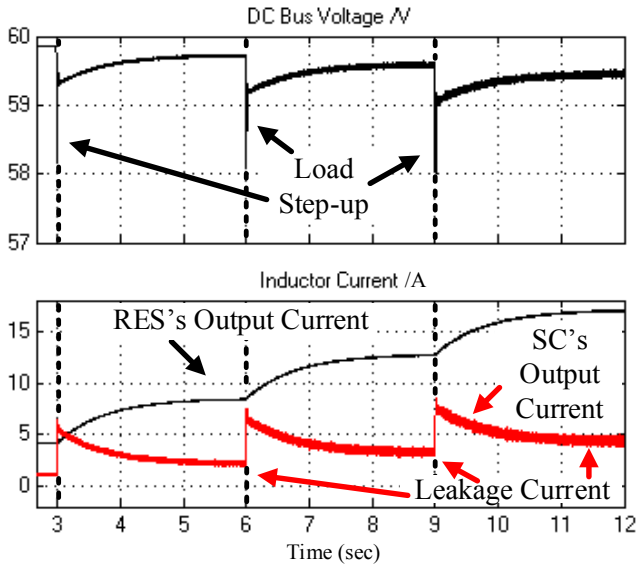


Fig.2.6 Performance and DC leakage current of the HPF-based EMS with plug'n'play

sensitive to surge current (e.g. LIB and FC), LPF is applied to the corresponding controllers. The control of SCESS becomes independent of other DG units. Therefore, this improved EMS is suitable for applications in droop-controlled DC microgrid.

However, the major drawback of this EMS is the DC leakage current during steady state, as simulated in Fig2.6. As shown, the DC output current of SCESS doesn't return to zero after transients induced by load variations. The amplitude of the DC leakage current is not a fixed value and is distinguished by dynamic behavior of the controller during transients. Suppose the HPF is a first-order high-pass filter and the compensator is a PI controller, which could be described as:

$$G_{HPF}(s) = K\frac{s}{\tau s + 1} \tag{2.1}$$

$$G_{PIv}(s) = P_v + \frac{I_v}{s} \tag{2.2}$$

where K and τ are the gain and time constant for HPF, and P_v and I_v is the proportional and integral term of PI compensator.

Then the current reference generated by the voltage loop with a constant non-zero

error signal $e(s) = E_v/s$ can be derived as:

$$i_{ref}(s) = e(s)G_{PI}(s)G_{HPF}(s) = E_v\left(\frac{KP_v - \tau KI_v}{\tau s + 1} + \frac{KI_v}{s}\right) \tag{2.3}$$

Note that in (2.3) the resulted current reference has a non-zero term, indicating a step-up response which has the same sign with the error signal $e(s)$. This means controller's forward path is has a finite gain on DC or low-frequency components associated to parameters of PI compensator and transients, resulting a leakage current in steady state. The leakage current may not be a serious issue when loads are lumped and DG units are controlled by a centralized EMS. However, in a droop-controlled DC microgrid with DG units and distributed loads, the DC bus voltage droops with the load current, as is illustrated in previous chapter. This would deteriorate the condition, making the leakage current unable to be contained effectively through coordinating control with multiple DG units. Though the leakage current could be eliminated by SOC regulation loop eventually, this improved EMS is not considered to be a suitable EMS for DC microgrids with distributed loads. The uncontrolled leakage current widen SC's SOC which contains the performance of surge current compensation and results lower efficiency due to unnecessary charge/discharge cycles.

To eliminate the steady-state leakage current caused by the presence of integral term of PI compensator, the compensator could simply be replaced by a constant gain or the proportional term of the original PI compensator. The resulting control loop is quite similar to the EMS proposed in [59][60]. Then the loop could be tuned by following the approach in [59], as $G_P(s)=P_v$ denotes the DC bus capacitance C_{bus}. Eq. (2.3) could be rewritten as:

$$i_{ref}(s) = e(s)G_P(s)G_{HPF}(s) = sC_{bus} \times \frac{K}{\tau s + 1} \times e(s) \tag{2.4}$$

Note that the term sC_{bus} in Laplace domain indicates the lumped output current of all capacitors connected to the DC bus. The second term in (2.4) illustrates a LPF

of the same bandwidth as the HPF. The simulation results shown in Fig.2.7 confirm that the resulted system eliminates DC leakage current and has competing compensation performance.

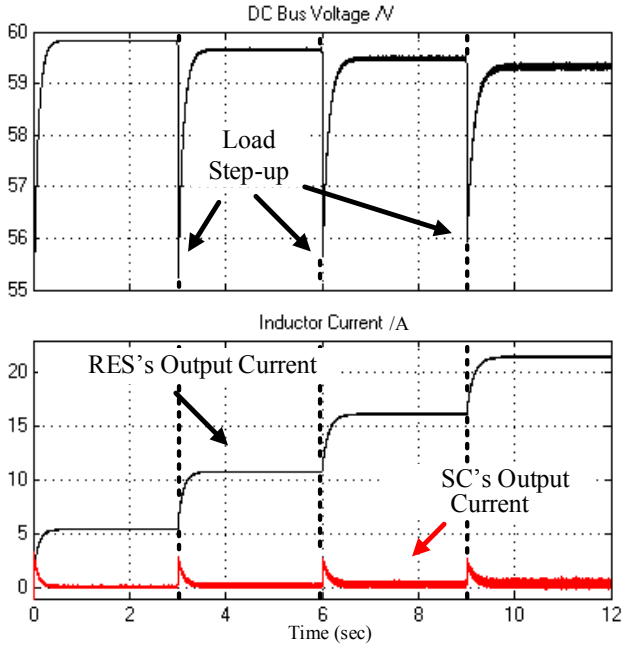


Fig.2.7 Performance of the improved EMS without integral term

However, this method inherits part of disadvantages from the family of centralized master-slave EMS where performance of compensation relies on dynamics of each converter connected to the DC bus. In a DC microgrid, DGs and loads connect and disconnect to the grid from time to time, making the dynamic response and DC capacitance of the DC microgrid change dramatically. This would add stability concerns since the HPF-based methods are in lack of robustness. Therefore, the improved method mentioned above may not be suitable for applications in droop-controlled DC microgrids since its performance is dependent on selection of C_{bus} and τ.

2.3 SOC-based EMS with Plug'n'play

The current reference for the inner current loop shown in Fig.2.2 is generated by the centralized controller in traditional EMS, which is not applicable in droop-controlled DC microgrid. Therefore, in order to realize plug'n'play while circumventing disadvantages induced by HPF as illustrated in the previous section,

the current reference shall be generated by outer voltage/current loops with variables measured locally to the SCESS. Authors in [39][40] proposed a EMS utilizing SC's SOC as the outer voltage loop to realize plug'n'play in a DC microgrid of varying DC bus voltage. The global control diagram is shown in Fig.2.8.

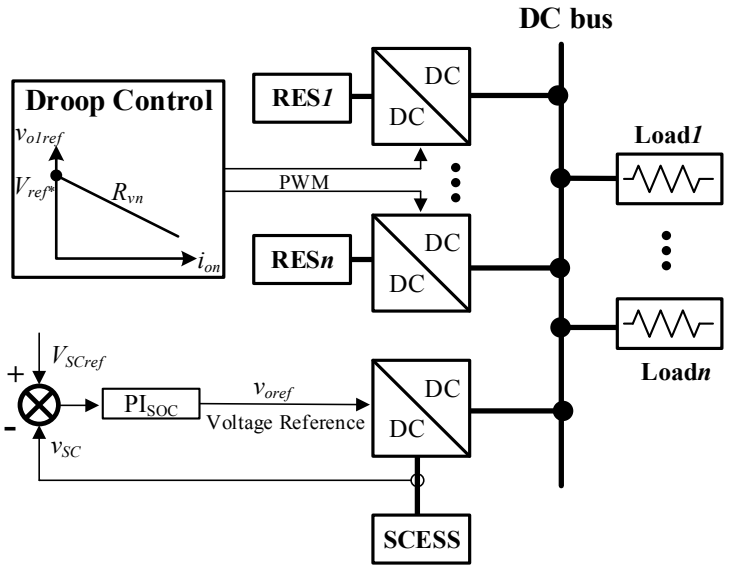


Fig.2.8 Control diagram of EMS employing SC's SOC

As shown, the EMS employing SC's SOC forms a cascaded control loop. The inner voltage/current loops control DC bus voltage (coordinate with other DG units), and SC's output current, respectively. Then the outer closed loop controls SC's SOC while generating voltage reference for inner voltage loop. Those three cascaded loops are regulated by PI controllers, and allow for accurate management of SC current as well as output voltage. During transients caused by load changes, which requires the SCESS compensating the surge power demand, the slow outer SOC regulation loop maintains nearly a constant DC bus voltage v_{oref}. Then the SOC regulation loop regulates SC's SOC back to its nominal value. The DC bus voltage is maintained by all DG units connected to the DC microgrid by droop control. In addition, a feedforward loop could be added to the current loop if the load demand is predictable.

This type of EMS adapts to the conditions in droop controlled DC microgrids. The outer SOC regulation loop enables the SCESS to meet surge power demands,

protecting sensitive RES units from supplying burst power. Plug'n'play is also intrinsically realized, since the output voltage reference v_{oref} is generated by outer SOC regulation loop. Since the outer loop regulates SC's terminal voltage by a PI controller, problems described in previous section like DC leakage current during steady state no longer exists. In general, this EMS is simple and effective for applications of SC in droop-controlled DC microgrids.

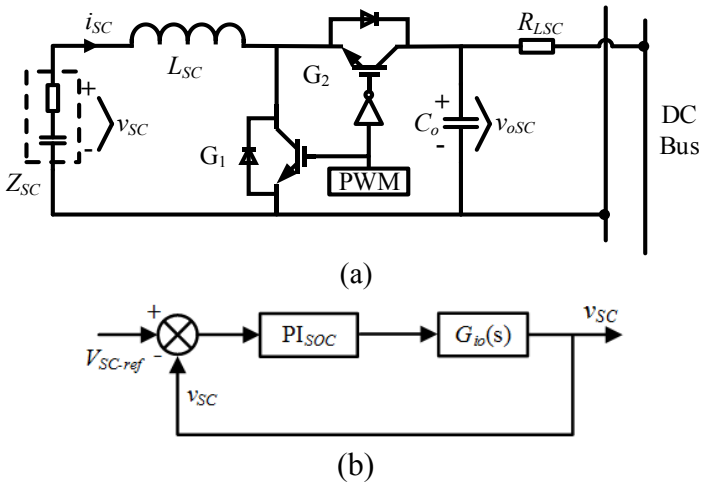


Fig.2.9 (a) Model of a bidirectional boost converter. (b) Control diagram of SOC regulation loop.

However, the slow dynamic response limits the application of this type of EMS. The slow dynamic response of the system comes from the outer SOC regulation loop, as is the model shown in Fig.2.9.

In order to tune the PI controller regulating the outer voltage loop, the output-voltage-to-input-voltage transfer function $G_{io}(s)$ is need. For the typical boost converter adopted by [40], shown in Fig.2.9 (a), the transfer function $G_{io}(s)$ could be derived as (neglecting parasitic impedances):

$$G_{vio}(s) = \frac{-2C_oV_{oSC}s + I_{SC}(1-D) - \frac{V_{oSC}}{R_{LSC}}}{\frac{I_{SC}L_{SC}}{Z_{SC}}s + \frac{V_{SC}}{Z_{SC}} + I_{SC}} \qquad (2.5)$$

where C_o and L_{SC} are output capacitor and boost inductor, I_{SC} is the designed

charging current for SC, V_{SC} is the nominal voltage of SC, V_{oSC} is the nominal output voltage, R_{LSC} is the output impedance and $Z_{SC}=R_{SC}+1/(sC_{SC})$ is SC's equivalent impedance, of which C_{SC} is very large compared to C_o.

The openloop response of the model is very slow since the coefficients of s include C_{SC}, which is $1F$ to more than $100F$ depending on the capacitance of SCESS. The large C_{SC} makes the poles of the system closer to real axis, which means the natural frequency of the system is much smaller, leading to slow dynamic response. Though PI controller is able to regulate the dynamic response to some extent, trade-offs such as gain/phase margins offset that effort since issues like delays in digital control system request more robustness of the control system.

The slow dynamics may cause problems when the leakage current is regulated by this SOC regulation loop. Due to the large inertia introduced by C_{SC}, the resulted system tends to release/absorb much more energy than required during transients. This also requires more redundancy and oversizing of SC when designing the SCESS, adding excessive cost. The redundant energy released/absorbed by SC will needed to be re-balanced with the microgrid eventually. This results lower overall efficiency and may cause unnecessary disturbances to the DC microgrid and raise stability concerns.

Another problem associate with the slow dynamics is that it takes too long for the voltage of SC to return to its nominal value, compromising the effectiveness of surge current compensation. As is shown in the simulation in Fig.2.10, after the surge current compensation stage where output current of SCESS from zero to a positive value due to sudden load step-up, the output current is regulated to become negative and the SCESS enters the rebalancing stage where SC's voltage is regulated back to its nominal value. In order to avoid too much overshoot and oscillation and to stabilize the system, the compensator of SOC regulation is designed well damped, resulting little overshoot, namely, very small charging current. This may result overstress on SCESS when the load changes quickly and frequently, as is the case for PHEV where unpredictable acceleration and braking

requires SCESS to release and absorb energy quickly and repeatedly. Under such circumstances, the SC may not have enough time to be regulated to its nominal terminal voltage before the next transient occurs. The overstress caused by slow dynamic response is also clearly presented in experimental results in [40].

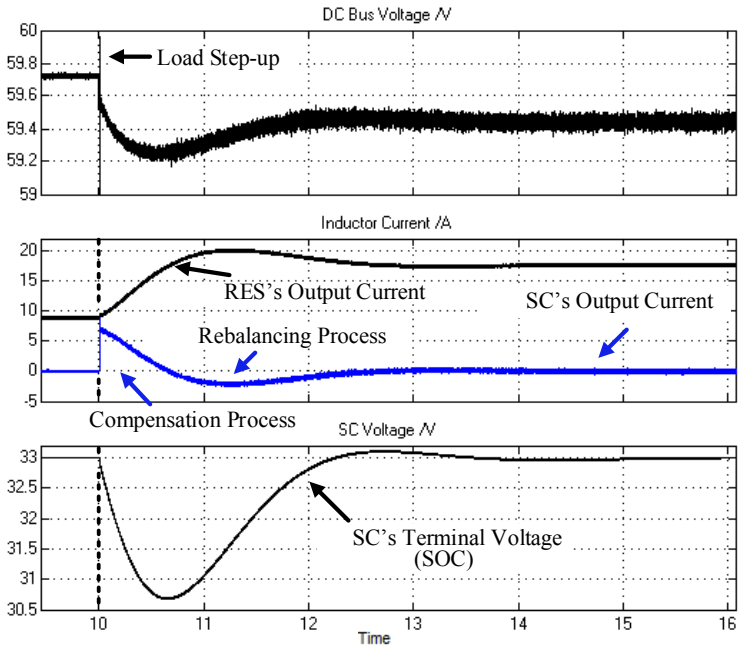


Fig.2.10 Performance of EMS employing SC's SOC

Moreover, to further tune the compensator, detailed models of DC microgrid is required as is illustrated by authors of [39][40]. However, for a droop-controlled DC microgrid where the topology changes frequently and dynamics of DG units change dramatically due to the intermittency of RES and load conditions, the robustness of the controller has to be meet by enlarging the gain/phase margins. This makes it harder for the controller's optimization which might offsets the drawbacks mentioned earlier in this section. In addition, the rigid control loops fails to provide a convenient way for the designer to estimate the amount of energy released/absorbed during transients, hindering the optimization for sizing of SC.

To sum up, this type of EMS merges surge current compensation and SOC regulation into one single loop with reduced degrees of freedom. The simplicity and effectiveness of this type of EMS is realized by making sacrifice for dynamic response and redundancy. Thus, there's a tradeoff between performance and

complexity of EMS design. This EMS provides adequate surge current compensation performance for DG units with slow dynamics and known load variations, especially for fuel cells, but it's not the best option for other applications that have stringent requirements for dynamic response, such as droop-controlled DC microgrid.

2.4 Summary

This chapter reviews state-of-art EMS for SCESS in DC microgrids. Their drawbacks when used in a DC microgrid are discussed. Simulations are carried out to confirm disadvantages of some reviewed methods in this chapter. Note that simulations are performed with the same system configuration and control parameters presented in Chapter 5.

In literature, the most widely adopted EMS is the centralized master-slave EMS that utilizes a centralized controller with distributed sensors and physical communication lines to generate accurate voltage/current reference for SCESS. The dependency on reliable physical communication making it unsuitable for SCESS operates in a DC microgrid where plug'n'play feature is desired.

The improved EMSs with plug'n'play feature evolved from transitional ones can be classified into two categories. The first category includes HPF in the voltage loop so that the current reference of SCESS is generated by outer voltage loop, realizing plug'n'play. This EMS has the drawback of DC leakage current in steady state, making it less favorable. Though this leakage current could be eliminated by various means, the performance of this category of EMS is sensitive to dynamics of the DC microgrid. The other category is based on SC's SOC, where the SOC regulation loop generates references for voltage and current loops, realizing plug'n'play feature. However, dynamic performance of the method is designed to be slow, widening the SC's SOC range during operation and resulting overstress conditions.

Chapter 3

Proposed EMS for SCESS

This chapter presents the proposed EMS for SCESS with plug'n'play operation. The proposed EMS has two working modes: surge current compensation mode and SOC regulation mode. Working modes are managed by a mode switcher, which is designed to realize seamless transitions between working modes. The surge current compensation loop is realized by virtual impedance loop with virtual resistor and virtual capacitor, where the virtual capacitor can control the SC's compensation time constant and dismiss any leakage steady-state current, and virtual resistor can improve the transient damping. The SOC compensation loop uses traditional voltage-mode controller with PI compensator.

3.1 Proposed Multi-loop EMS with Virtual Impedance

As illustrated in the previous chapter, an effective EMS for SCESS in droop-controlled DC microgrid is not yet available in literature. Existing approaches have various problems such as steady state leakage current, and slow dynamic response. The proposed novel EMS in this thesis is inspired by existing approaches with a better tradeoff between performance and complexity.

In a droop-controlled DC microgrid, the voltage regulation is performed by cooperation of all DG units, ESS units and SCESS units, so that the load is shared between units without physical communication lines. The model of the droop-controlled microgrid studied by this thesis is shown in Fig.3.1.

As shown, the prototype of the DC microgrid is composed of RES/ESS, SC with their respective interfacing boost converters, and loads. The converters (DG and SCESS) interface the DC microgrid with small line resistances (R_{L1} and R_{LSC}). The load variations are modeled by a lumped resistor network. The DG is controlled by

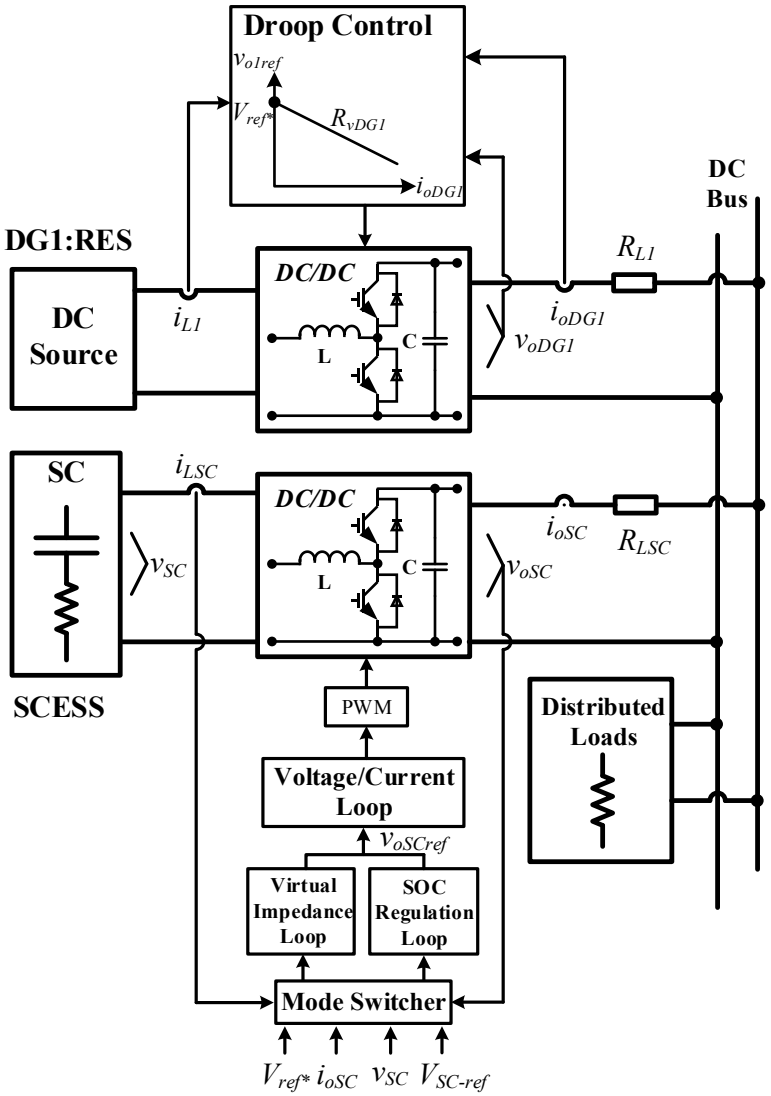


Fig.3.1 Overall control diagram of the droop-controlled DC microgrid studied in this thesis

DC droop controller utilizing virtual impedance loop, while the SCESS is controlled by the proposed EMS.

To circumvent the disadvantages caused by merging surge current compensation and SOC regulation into one single control loop as illustrated in previous chapter, the proposed method disintegrates those two functions and builds two independent control loops for them. A mode switcher is also designed to manage seamless transition between both loops.

3.1.1 Surge Current Compensation Loop

For the DG with canonical voltage-mode double-loop (outer voltage loop and inner current loop) controller, the voltage-current droop control could be realized by adding virtual resistor R_{vDGn} together with output current to form the outer virtual impedance loop. The DG's output voltage reference v_{refDGn} is generated as (time-domain):

$$v_{refDGn}(t) = V_{ref*} - R_{vDGn} i_{oDGn}(t) \tag{3.1}$$

where V_{ref*} is the nominal voltage of DC bus and i_{oDGn} is the output current of nth DG.

The droop method takes the voltage of DC bus as a virtual communication link between each DG unit. Inspired by this principle, the SCESS could be controlled by adding a virtual capacitor C_{vSC} in series with the virtual resistor R_{vSC}. Then the output voltage reference of SCESS v_{refSC} could be derived as:

$$v_{refSC}(t) = V_{ref*} - R_{vSC} i_{oSC}(t) - \frac{1}{C_{vSC}} \int i_{oSC}(t)\, dt \tag{3.2}$$

where i_{oSC} is the output current of SCESS.

Eq. (3.2) adds a virtual capacitor between output converter and line resistance. This way, C_{vSC} is charged and discharged according to power demands implied by DC bus voltage during transients, resulting surge current compensating effort. In steady state, C_{vSC} blocks DC output current so as to ensure zero DC output current of SCESS during steady state which is preferable for the operation of SC. Thus, the dynamic response of the proposed virtual impedance loop mimics a RC network. Fig.3.2 shows the virtual impedance control diagram for the example microgrid of Fig.3.1.

Note that both parameters C_{vSC} and R_{vSC} in the virtual impedance loop are adjustable during operation. The adjustable virtual impedance loop provides great flexibility for various applications. Surge current compensation performance can be adjusted dynamically in order to coordinate with the control of other DG units. To illustrate

the working principle and flexibility of the proposed virtual impedance loop, the studied droop-controlled DC microgrid shown in Fig.3.2 could be further simplified to Fig3.3 by assuming that inner voltage loops for both converters are sufficiently faster than the virtual impedance loop.

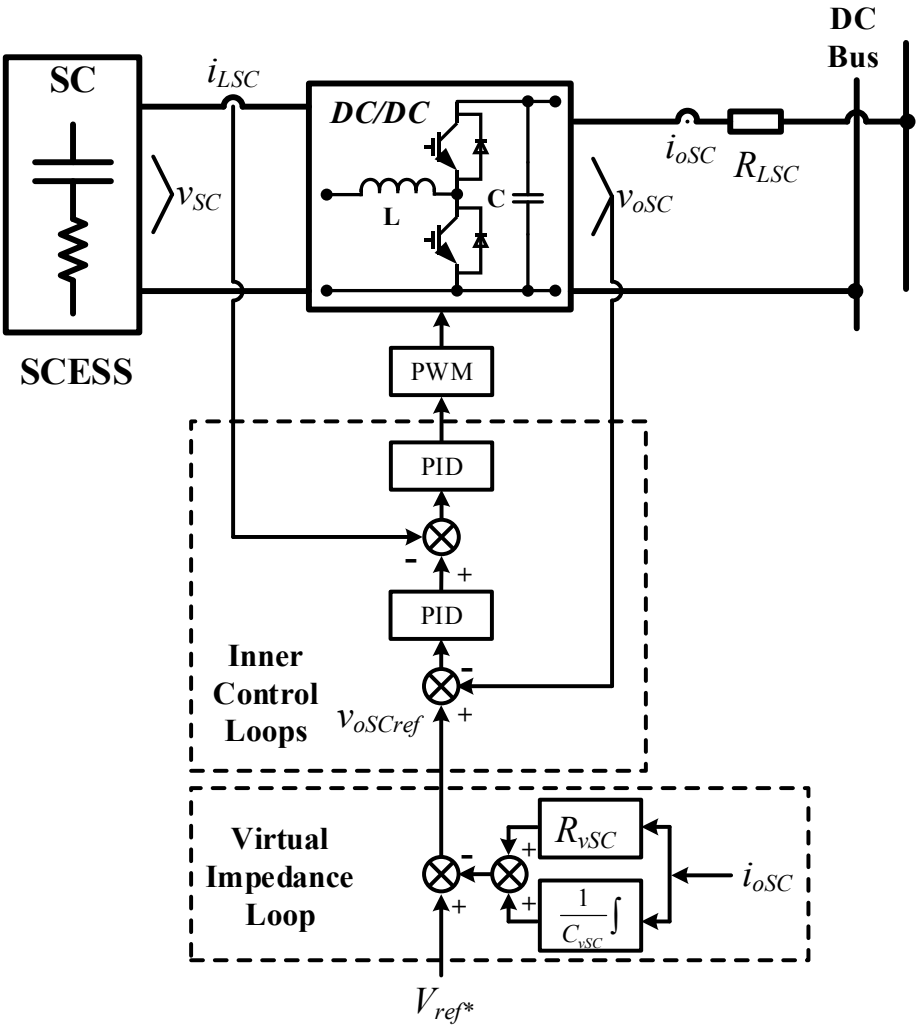


Fig.3.2 Control diagram of the DC microgrid with the proposed virtual impedance loop

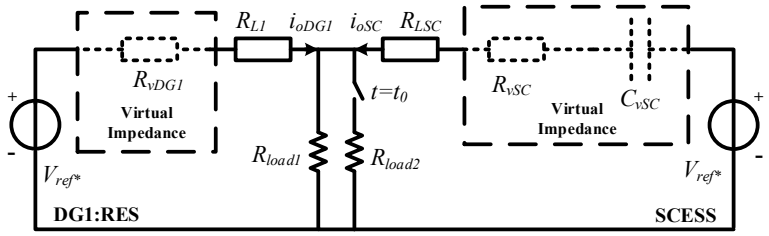


Fig.3.3 Equivalent model of the proposed EMS during load changes, neglecting interactions with inner control loops

Then the surge current i_{oSC} supplied by SCESS during transient caused by sudden load change from R_{load1} to R_{load2} could be solved in Laplace domain by applying Kirchhoff's circuit laws.

Suppose sudden load change happens at $t=0s$, then the output voltage and current of both converters are:

$$V_{oDG1}(s) = \frac{V_{ref}^*}{s} - I_{oDG1}(s) R_{vDG1} \tag{3.3}$$

$$V_{oSC}(s) = \frac{V_{bus0}}{s} - I_{oSC}(s) R_{vSC} - \frac{I_{oSC}(s)}{sC_{SC}} \tag{3.4}$$

$$I_{oDG1}(s) = \frac{V_{oDG1}(s) - V_{bus}(s)}{R_{L1}} = \frac{\frac{V_{ref}^*}{s} - V_{bus}(s)}{R_{vDG1} + R_{L1}} \tag{3.5}$$

$$I_{oSC}(s) = \frac{V_{oSC}(s) - V_{bus}(s)}{R_{LSC}} = \frac{\frac{V_{bus0}}{s} - V_{bus}(s)}{R_{vSC} + R_{LSC} + \frac{1}{sC_{SC}}} \tag{3.6}$$

where V_{bus0} is the steady state DC bus voltage before the load change ($t=0^-$).

The relationship between V_{bus0} and R_{load1} could be derived as:

$$V_{bus0} = \frac{R_{load1}}{R_{vDG1} + R_{L1} + R_{load1}} V_{ref}^* \tag{3.7}$$

Applying Kirchhoff's current law (KCL) at the point of common coupling (PCC):

$$I_{oDG1}(s) + I_{oSC}(s) = \frac{V_{bus}(s)}{R_{load2}} \tag{3.8}$$

Then i_{oSC} could be solved in Laplace domain by combing (3.3)-(3.8), as:

$$I_{oSC}(s) = K\frac{1}{\tau s + 1} \tag{3.9}$$

where,

$$K = \left(\frac{1}{\frac{R_{vDG1} + R_{L1}}{R_{load1}} + 1} - \frac{1}{\frac{R_{vDG1} + R_{L1}}{R_{load2}} + 1} \right) C_{SC} V_{ref*} \tag{3.10}$$

$$\tau = \left(R_{vSC} + R_{LSC} + \frac{1}{\frac{1}{R_{vDG1} + R_{L1}} + \frac{1}{R_{load2}}} \right) C_{SC} \tag{3.11}$$

Eq.(3.9)-(3.11) describe dynamic performance of the proposed virtual impedance loop, which mimics the dynamic behavior of a RC network. As illustrated, the surge current compensation effort could be controlled by adjusting C_{vSC} and R_{vSC}. From (3.10), a larger C_{vSC} yields better compensation effectiveness since more energy is released or absorbed by the virtual capacitor. As illustrated earlier in this section, the time constant τ of RC network could be estimated as (3.11), and the τ could be adjusted by tuning C_{vSC} and R_{vSC}. Therefore, compensation performance can be designed to meet certain requirements by tuning corresponding virtual impedance loops. The designer could also take use of the characteristics mentioned above to decide the optimum capacitance of the SC.

Eq.(3.11) could be further simplified as follows. Suppose line resistances R_{L1}, R_{LSC} and virtual resistors R_{vDG1}, R_{vSC} are generally much smaller than the resistive load R_{load1}, R_{load2}, (3.11) could be further simplified by applying $R_{L1}, R_{vSC} \ll$ $_{load2}$:

$$\tau \approx \left(R_{L1} + R_{vDG1} + R_{LSC} + R_{vSC} \right) C_{vSC} \tag{3.12}$$

For a DC microgrid with n DG units compensated by SCESS, the time constant could be calculated as:

$$\tau = \left(R_{vSC} + R_{LSC} + \frac{1}{\frac{1}{R_{vDG1} + R_{L1}} + \frac{1}{R_{vDG2} + R_{L2}} + \cdots \quad \frac{1}{R_{vDGn} + R_{Ln}} + \frac{1}{R_{load2}}} \right) C_{SC} \quad (3.13)$$

where R_{vDGn}, R_{Ln} are virtual resistor and line resistance for the n^{th} DG unit.

If n is considerably large so that $\left(R_{vDG1} + R_{L1}\right) \| \cdots \| \quad \ll \quad _{LSC}$, then (3.14) could be further simplified as:

$$\tau \approx \left(R_{LSC} + R_{vSC}\right) C_{vSC} \quad (3.14)$$

As a result, one can use (3.12) and (3.14) to estimate time constant of the compensation performance. The compensation effort simulates a typical RC charge/discharge process. Following this idea, after $t=3\tau$, the system could be considered to have been brought back to its steady state (95%) after sudden changes in power demand. Then virtual capacitor C_{vSC} can be determined from the time constant as:

$$3\tau = T_s \quad (3.15)$$

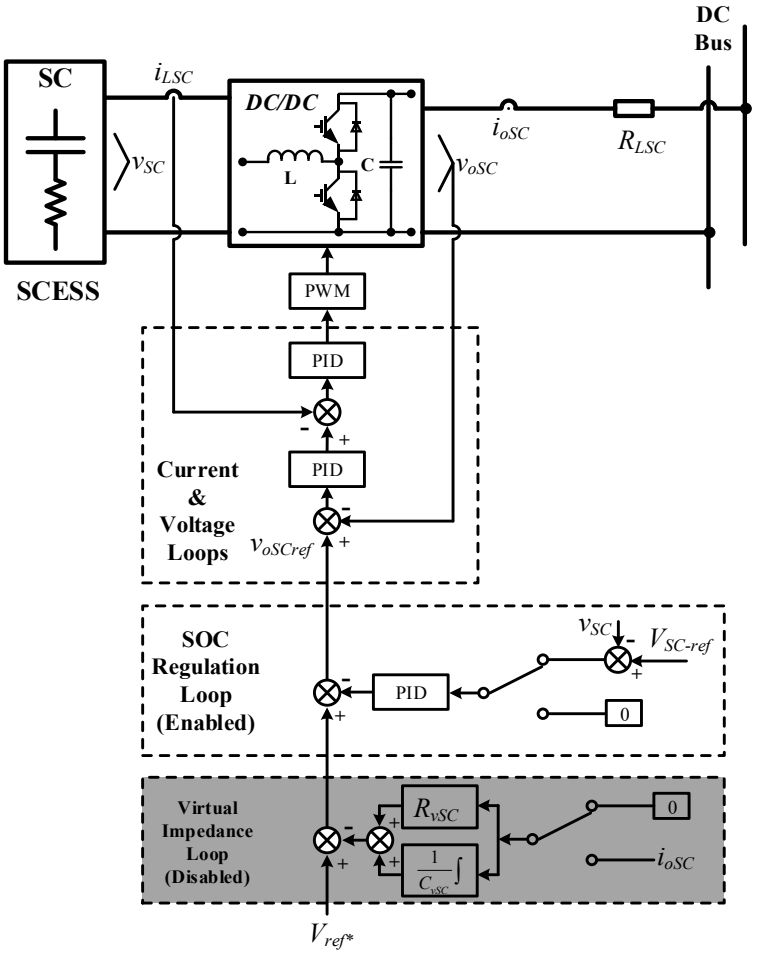
where T_s is the desired settling time for the compensation, which is associated to load profiles and intermittency of specific RES units.

3.1.2 SOC Regulation Loop

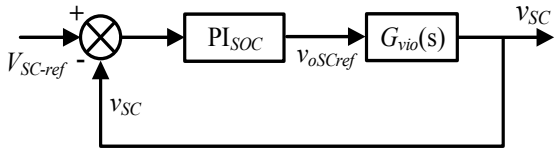
Traditionally, SOC regulation is made to be slow enough so as to mitigate interactions between surge current compensation and SOC regulation. The slow dynamic also comes from inertia introduced by the large capacitance of SC. The advantage of this idea is that both loops are able to operate simultaneously, resulting a concise and efficient design. However, the major drawback is that the dynamic performance of the SOC loop is limited by the surge current compensation loop. Under conditions where load changes quickly and repeatedly (e.g., regenerative braking in electrical vehicles), the slow SOC regulation would in return deteriorate

the performance of compensation, causing overstress conditions. As illustrated in Section 2.3, the EMS merges SOC regulation and surge current compensation into one single loop. This EMS therefore has the same problem mentioned above.

In order to offset the disadvantages mentioned above, the EMS proposed in this thesis separates the surge current compensation loop and SOC regulation loop from each other in order to fully decouple their dynamics, and introduce a concise mode switcher to manage transitions between both modes.



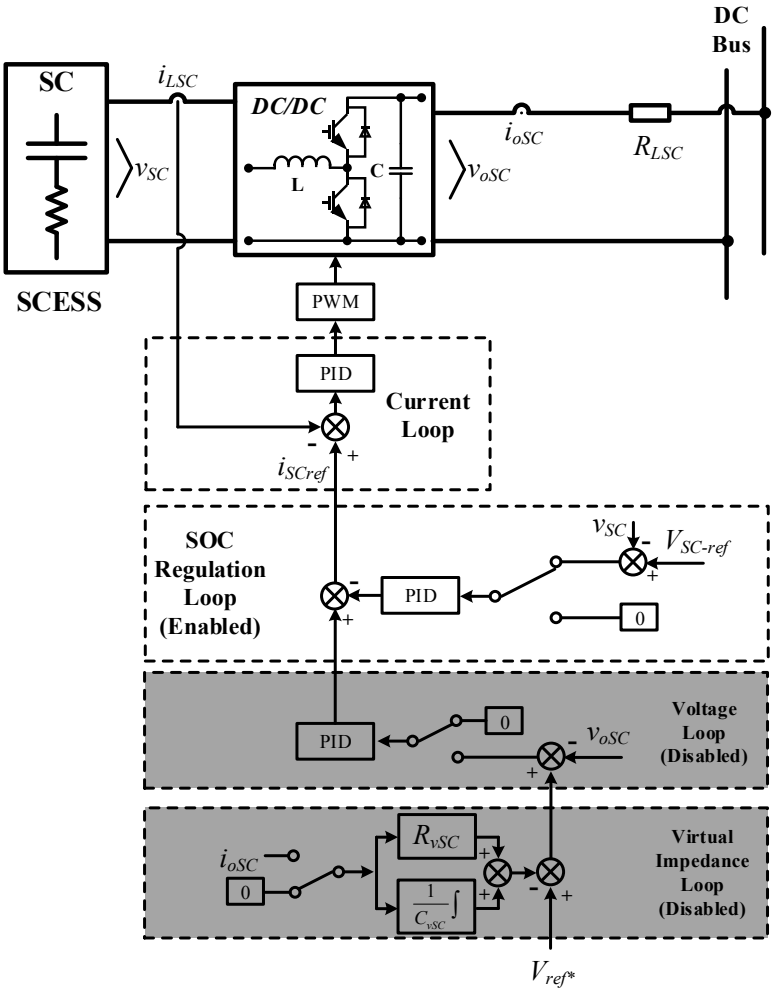
(a)



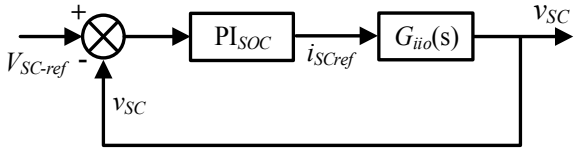
(b)

Fig.3.4 (a) SOC regulation loop generating v_{oSCref} (b) Small-signal model of the resulted system

For SOC regulation, the control loop employed in this study is basically the same to SOC controllers in Section 2.3, where error signal of SC's voltage is compensated by PID controller with a faster dynamic response. The SOC loop could perform reference generation for inner voltage loop or current loop, depending on requirements of dynamic performance and control complexity of the designed system. As for voltage reference generation, the control diagram is shown in Fig.3.4. $G_{vio}(s)$ is the output-voltage-to-input-voltage transfer function.



(a)



(b)

Fig.3.5 (a) SOC regulation loop generating i_{SCref} (b) Small-signal model of the resulted system

Note that SOC regulation loop could also be added to the inner current loop, as is shown in Fig.3.5. $G_{iio}(s)$ is the output-voltage-to-inductor-current transfer function. This method has the potential to provide faster dynamic performance as compared to the method shown in Fig.3.4. However, additional control efforts are needed in order to achieve seamless mode transitions. In this thesis, the method shown in Fig.3.4 is adopted due to its simplicity.

The resulting cascaded multi-loop controller can be tuned sequentially together with inner voltage/current loops, using various methods (e.g. Ziegler–Nichols method) to achieve smooth tracking with fast disturbance rejection. Since the dynamics of SOC regulation loop is not dependent on surge current compensation, the designer could even customize SOC regulation instead of adopting traditional voltage feedback with PI compensator, resulting better dynamic performance. This thesis will only focus on design of traditional voltage controller with PI compensator.

3.1.3 Mode Switcher Design

In order to enable seamless mode transfer between surge current compensation and SOC regulation modes, a mode switcher is required. The basic idea of seamless transfer is to avoid abrupt changes to PWM signal so as to ensure smooth transitions. For the controller in this thesis, abrupt changes are caused by residual value of the integral term of PI controllers. Following the idea described above, mode switchers could be designed. The proposed mode switchers for SOC regulation loops shown in Fig.3.4 and Fig.3.5 are presented in Fig.3.6 and Fig.3.7, respectively.

Theoretically, the error signal of both surge current compensation loop and SOC regulation loop are close to zero in steady state since integral term of PID controller is able to eliminate DC residual steady-state error for either loop. From this point of view, the seamless mode transition from SOC regulation mode to surge current compensation mode could be achieved by substituting error signal e_{SC} of SOC regulation loop by zero while switching zero to i_{oSC} in surge current compensation loop, and vice versa. For method shown in Fig.3.5 where current reference is

generated by SOC regulation loop, the inner voltage loop shall also be suspended and resumed by switching between error signal e_{vo} and zero, as is shown in Fig.3.7.

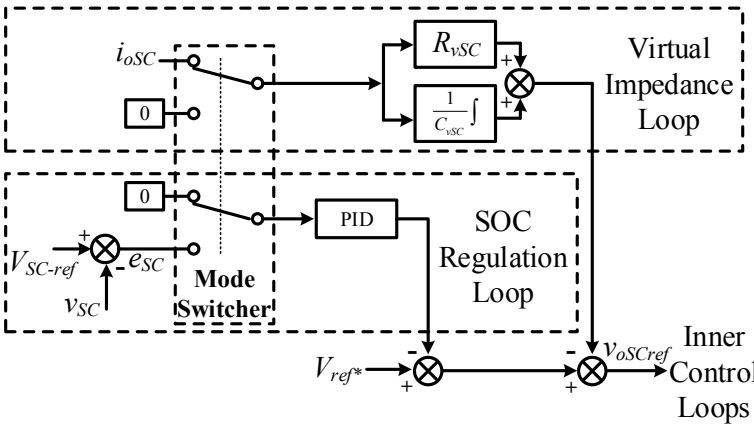


Fig.3.6 Configuration of the mode switcher for SOC regulation loop generating v_{oSCref}

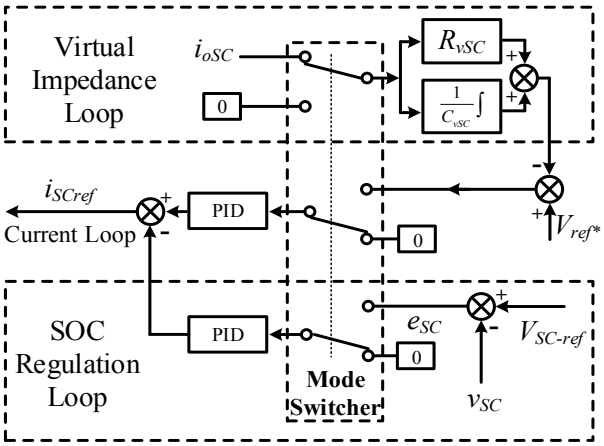


Fig.3.7 Configuration of the mode switcher for SOC regulation loop generating i_{SCref}

The transition between both modes are achieved by switching between error signals and zero to suspend and resume corresponding loops, so as to avoid abrupt changes in reference generation. In this way, by swapping input signal of integral terms between zero and error signal, the output of PI controller or the residual value of the integral term would be hold to its current value when the controller is switched to the other mode and the output voltage and current reference v_{oSCref} & i_{LSCref} will not have abrupt changes as a result.

As for residual value of integral terms, in order to circumvent integral saturation of PI controller in SOC regulation loop, the residual value of the integral term in SOC regulation loop could be added to surge current compensation loop during mode

transitions. Then the integral term in SOC regulation loop could be safely reset when surge current compensation mode is active, preparing for upcoming mode transitions.

3.2 Advantages of the Proposed EMS

Compared to the existing SCESS control strategies, the proposed EMS has the following advantages:

- The surge current compensation is controlled by voltage-mode controller, so that physical communication lines and accurate measurements of power demands between DGs and distributed loads are no longer needed. Thus plug'n'play is realized without compromising power sharing ability and surge current compensation capability in droop-controlled DC microgrid.
- The plug'n'play feature ensures SC's continuous and seam-less operation, making it serve as a universal surge current compensator for all other load-sensitive DGs connected to the droop-controlled DC microgrid. This helps reduce complexity and cost of the system, as dedicated surge current compensators tuned for every load-sensitive DGs are no longer needed.
- The dynamic performances of both surge current compensation loop and SOC regulation loop are decoupled and could be tuned independently. This makes the proposed EMS preferable under conditions where load changes quickly and repeatedly, which requires quicker SOC regulation in order to optimize surge current compensation.
- Control efforts mentioned above are achieved by concise multi-loop controller design, making it easier and more intuitive for PID controller tuning in order to meet certain stability concerns and dynamic performance requirements.

3.3 Summary

In this chapter, a novel EMS for SCESS in droop-controlled DC microgrids is

proposed. The proposed EMS employs virtual impedance loop composed of a virtual resistor R_{vSC} and a virtual capacitor C_{vSC} to provide surge current compensation, which simulates a dynamically adjustable RC network. The independent SOC regulation loop compensated by a PI compensator is also introduced to provide enhanced performance of SOC regulation. These two working modes (surge current compensation mode & SOC regulation mode) are regulated by a mode switcher with concise control structure that is easy to implement in digital control system. The mode switcher allows for seamless transfer between both modes and eliminates unnecessary coupling between.

This novel EMS has several advantages over existing ones described in Chapter 2. The first advantage is that the proposed voltage-controlled EMS realizes plug'n'play feature so that non-compromising power sharing performance between SCESS without physical communication links is realized. Meanwhile, this feature makes SCESS serve as a universal surge current compensator for all other DGs connected to the droop-controlled DC microgrid that are sensitive to abrupt output power variations. This helps reduce complexity and cost of the microgrid, since dedicated surge current compensators tailored for each DG are no longer needed. Furthermore, the mode switcher helps decouple dynamics of both modes, enabling versatile and optimal design for SOC regulation.

Chapter 4

System Modeling and Controller Design

This chapter presents an iterative frequency-shaping method to tune compensators loop-by-loop. First the small-signal models of the bidirectional boost converter is deduced. Then the compensators in current, voltage and SOC regulation loops are tuned loop-by-loop successively. Finally tuning virtual resistor and virtual capacitor of surge current compensation loop is illustrated. Stability issues are also discussed later in this chapter.

4.1 Small-signal Modeling of Bidirectional Boost Converter

In order to investigate dynamic performances and stability of the proposed EMS during compensation process, small-signal analysis can be applied. The bidirectional boost converter is modeled according to its state-space average model.

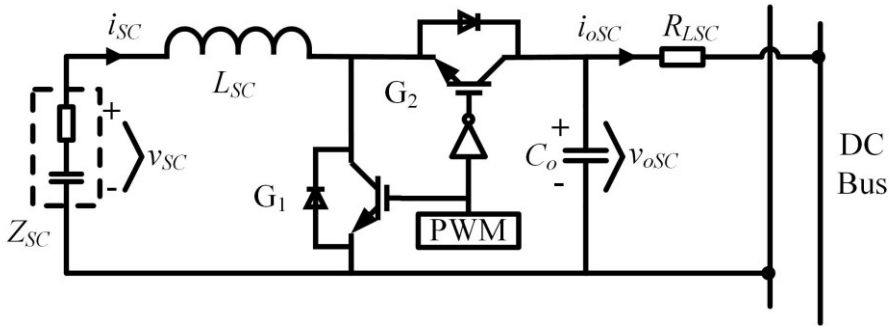


Fig.4.1 Topology of the bidirectional boost converter studied in this thesis

Fig.4.1 shows the bidirectional synchronous boost converter configuration, interfacing SC. The two switches are complementary, ensuring bidirectional power flowing. The converter operates in continuous conduction mode (CCM). The switching-average model can be described as:

$$\overline{\zeta} = \frac{1}{T_s}\int_{t}^{t+T_s} \zeta(t)\,dt \tag{4.1}$$

where T_s is switching cycle, ζ is the designated variable.

By applying voltage-second balance on capacitor and current-second balance on inductor, the following are obtained:

$$C_o \frac{d\bar{v}_{oSC}}{dt} = (1-d)\bar{i}_{SC} - \bar{i}_{oSC} \tag{4.2}$$

$$L_{SC} \frac{d\bar{i}_{SC}}{dt} = \bar{v}_{SC} - (1-d)\bar{v}_{oSC} \tag{4.3}$$

$$\bar{i}_{oSC} = \frac{\bar{v}_{oSC} - \bar{v}_{bus}}{R_{LSC}} \tag{4.4}$$

where L_{SC} is the inductance of boost inductor, C_o is the capacitance of output capacitor, v_{SC} is SC's terminal voltage (converter's input voltage), v_{oSC} is the output voltage, i_{SC} is current of inductor L_{SC} (SC's output current), i_{oSC} is converter's output current, v_{bus} is DC bus voltage, R_{LSC} is output line resistance and d is the duty ratio.

The small-signal models could be extracted by introducing disturbances:

$$\begin{cases} d = D + \hat{d} \\ \bar{v}_{oSC} = V_{oSC} + \hat{v}_{oSC} \\ \bar{v}_{SC} = V_{SC} + \hat{v}_{SC} \\ \bar{i}_{oSC} = I_{oSC} + \hat{i}_{oSC} \\ \bar{i}_{SC} = I_{SC} + \hat{i}_{SC} \\ \bar{v}_{bus} = V_{bus} + \hat{v}_{bus} \end{cases} \tag{4.5}$$

where D, V_{oSC}, V_{SC}, I_{oSC}, $I_{SC,}$ V_{bus} are constants according to the designed operating point of the bidirectional boost converter. In steady state where SCESS's output current is zero, those constants shall follow the relationship shown in (4.2)-(4.4). Thus, by combining (4.2)-(4.5), transfer functions for parameter design of inner voltage & current loop and surge current compensation loop could be derived. The duty-ratio-to-inductor-current transfer function $G_{di}(s)$ and inductor-current-to-output-voltage transfer function $G_{iv}(s)$ are:

$$G_{di}(s)=\frac{\hat{}}{d}\Big|_{\hat{}}=\frac{C_oV_{oSC}s+\frac{V_{oSC}}{R_{LSC}}}{L_{SC}C_os^2+\frac{L_{SC}}{R_{LSC}}s+(1-D)^2} \tag{4.6}$$

$$G_{iv}(s)=\frac{\hat{}}{\hat{}}=\frac{1-D}{C_os+\frac{1}{R_{LSC}}} \tag{4.7}$$

As for design of SOC regulation loop, dynamics of the SC should be taken into account. As is shown in Fig.4.1, applying power balance between input and output of the switching network yields:

$$\bar{v}_{oSC}\left(\bar{i}_{oSC}-sC_o\bar{v}_{oSC}\right)=\bar{v}_2\bar{i}_{SC} \tag{4.8}$$

$$\bar{v}_2=V_{SC}+\left(sL_{SC}+Z_{SC}\right)\hat{} \tag{4.9}$$

Considering SC's dynamics:

$$\bar{i}_{SC}=\frac{\bar{v}_{SC}}{Z_{SC}} \tag{4.10}$$

where Z_{SC} is SC's equivalent impedance.

Then the output-voltage-to-input-voltage transfer function $G_{vio}(s)$ and output-voltage-to-inductor-current $G_{iio}(s)$ are derived by combining (4.4), (4.5), (4.8)-(4.10), as:

$$G_{vio}(s)=\frac{\hat{}}{\hat{}}=\frac{-2C_oV_{oSC}s+I_{SC}(1-D)-\frac{V_{oSC}}{R_{LSC}}}{\frac{I_{SC}L_{SC}}{Z_{SC}}s+\frac{V_{SC}}{Z_{SC}}+I_{SC}} \tag{4.11}$$

$$G_{iio}(s)=\frac{\hat{}}{\hat{}}=\frac{-2C_oV_{oSC}s+\frac{V_{SC}I_{SC}}{V_{oSC}}-\frac{V_{oSC}}{R_{LSC}}}{I_{SC}\left(sL_{SC}+Z_{SC}\right)+V_{SC}} \tag{4.12}$$

where I_{SC} is the designed charging current.

4.2 Design of Inner Current and Voltage Loops

The cascaded voltage and current loops adopted in this thesis are compensated by two PI controllers, as is shown in Fig.4.2. The compensator in current loop utilizes a proportional regulator to provide fast tracking performance of i_{SC} with a large control bandwidth. The voltage loop takes a PI compensator to ensure stability and accurate reference tracking, with a dynamic response at least 5 times slower than the inner current loop to avoid unnecessary coupling.

The parameters of the bidirectional boost converter shown in Fig.4.1 are given as follows. The nominal DC bus voltage V_{bus} is $60V$. Input voltage range is 20-$40V$. Output power range is $\pm 1kW$. The boost inductor L_{SC} is selected as 0.5mH and the filter capacitor C_o is $550\mu F$. The switching frequency f_s is $20kHz$. The line resistance R_{LSC} is $50m\Omega$. A table of the parameters are also provided in Chapter 5.

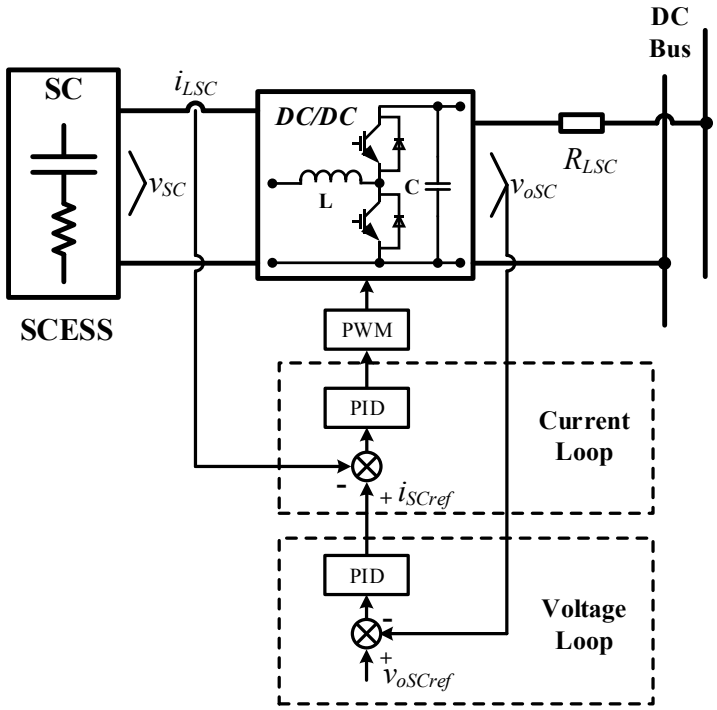


Fig.4.2 Inner voltage/current control loops

A. Design of Current Loop

The control diagram of inner current loop is shown in Fig.3.10. The loop gain is defined as:

$$\ell \qquad {}_{c}K_{PWM}G_{di}(s) \tag{4.13}$$

where K_{PWM} is the converter gain and K_{pc} is the proportional term of the compensator.

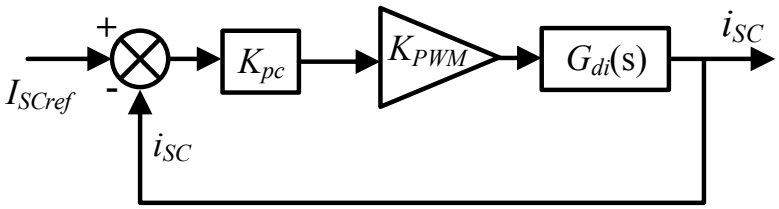


Fig.4.3 Small-signal model of current loop

The cut-off frequency f_{cc} of the current loop shall be no greater than 1/5 of the switching frequency f_s. Here f_{cc} is chosen as f_s/10. Considering K_{PWM}=1, then the proportional regulator K_{pc} is given as:

$$|\ell \qquad {}_{j2\pi f_{cc}} = \left|K_{pc}K_{PWM}G_{di}(j\omega_c)\right|_{\omega_c = j2\pi f_{cc}} = 1 \tag{4.14}$$

Since the designed converter for SCESS is connected to DC bus with a zero output current during steady state, zero-load condition (I_{oSC} = 0, I_{SCref} = 0) is selected for the PI controller design, which is compliant with derivation of (4.7). Here K_{pc} is finally chosen as K_{pc} = 0.08 with ω_c≈10,000 *rad/s*. The openloop frequency

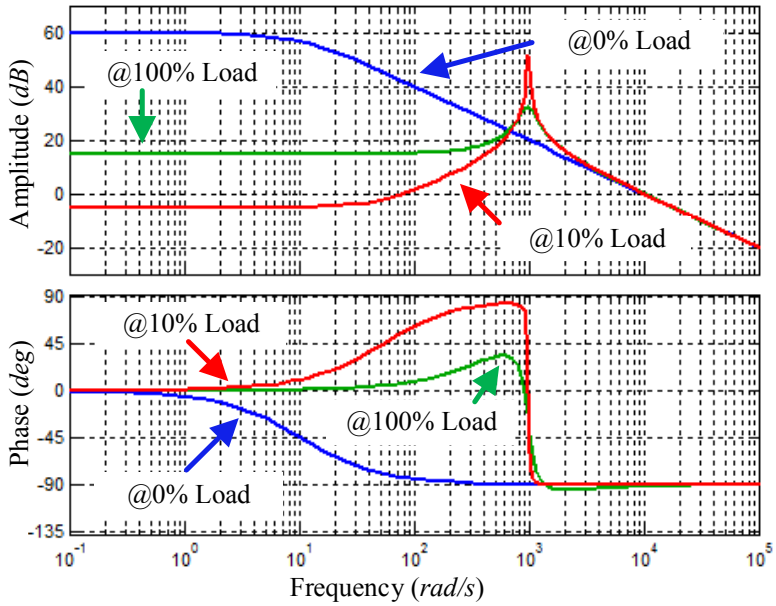


Fig.4.4 Bode diagrams of the inner current loop

response of the designed inner current loop with various load conditions is shown in Fig.4.4. As shown, the system remains stable with considerable phase margin (≈π/2) under all load conditions.

B. Design of Voltage Loop

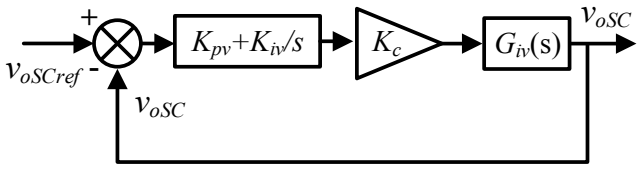


Fig.4.5 Small-signal model of voltage loop

As for the PI compensator of the voltage loop, the cut-off frequency f_{cv} shall be no greater than 1/5 of f_{cc} to mitigate coupling between voltage & current loops. Following this idea, the dynamic response of inner current loop could be considered fast enough to track dynamics of the outer voltage loop, As a result, the inner current loop is replaced by a constant gain K_c when designing the voltage loop, as is shown in Fig.4.5. Since the bandwidth of the voltage loop is much lower than the current loop, the current loop could be simplified to K_c=1 while designing the compensator for voltage loop. Then the loop gain of the voltage loop is defined as:

$$\ell \qquad \left(K_{pv} + \frac{K_{iv}}{s} \right) K_c G_{iv}(s) \tag{4.15}$$

where K_{pv} and K_{iv} are the proportional term and integral term of the PI compensator.

The frequency margin is designed to be no smaller than π/4. Here f_{cv} is chosen as f_{cc} /10. Zero-load condition is selected for design of the voltage loop. Then the PI controller could be designed as:

$$\left|\ell \qquad \right._{=2\pi f_{cv}} = \left| \left(K_{pv} + \frac{K_{iv}}{j\omega_v} \right) K_c G_{iv}(j\omega_v) \right|_{\omega_v = 2\pi f_{cv}} = 1 \tag{4.16}$$

$$\angle \ell \qquad \left._{=2\pi f_{cv}} = \angle \left(K_{pv} + \frac{K_{iv}}{j\omega_v} \right) K_c G_{iv}(j\omega_v) \right|_{\omega_v = 2\pi f_{cv}} \geq -\frac{3}{4}\pi \tag{4.17}$$

The parameters are finally chosen as, K_{pv}=1.24 and K_{iv}=4000 , with $\omega_{cv} \approx 141$ *rad/s*. The openloop frequency response of the designed voltage loop with various load conditions is shown in Fig.4.6. As shown, the system remains stable with considerable phase margin (≈π/2) under all load conditions.

4.3 Design of SOC Regulation Loop

As mentioned in Section 3.1.2, regulation of SC's SOC could be done in various ways, since the mode switcher decouples the dynamic between SOC regulation and surge current compensation. To optimize the performance of SOC regulation, the combination of load profile, intermittent nature of other renewable resources and dynamic response of the DC microgrid should be taken into consideration. In this thesis, the traditional and widely-used voltage control scheme with PI compensator is taken as a brief example of SOC regulation loop design.

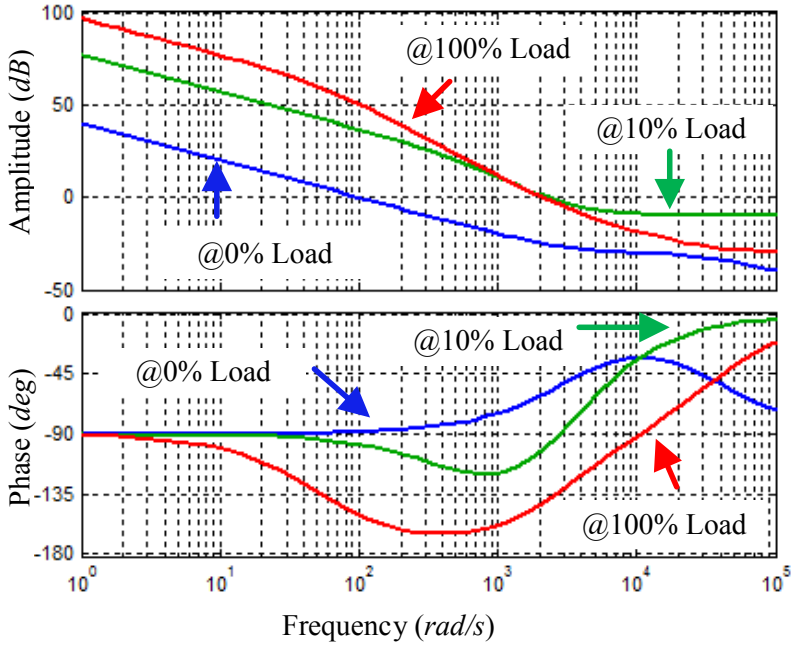


Fig.4.6 Bode diagrams of the voltage loop

When the system operates under SOC regulation mode, depending on reference generation of SOC regulation loop (V_{oSCref} or I_{SCref}), control diagram shown in Fig.3.1 can be simplified to Fig.3.4 and Fig.3.5, by assuming the cut-off frequency of the outer SOC regulation loop f_{SOC} is at least 10 times lower than the inner

voltage loop (f_{cv}) designed in the previous section. Then the designer could choose the parameters of PI compensator by following similar steps shown in previous section to meet desired design requirements such as bandwidth and phase margin.

For SOC regulation loop generating V_{oSCref}, shown in Fig.3.4, the loop gain is defined as:

$$\ell \qquad = \left(K_{pSOC-v} + \frac{K_{iSOC-v}}{s} \right) K_v G_{vio}(s) \tag{4.18}$$

where $K_{pSOC\text{-}v}$ and $K_{iSOC\text{-}v}$ are the proportional term and integral term of the designed PI compensator, and K_v is the converter gain of the inner voltage loop which equals to 1.

The frequency margin is designed to be no smaller than π/3. Considering a proper charging current I_{SC} and cut-off frequency $f_{SOC\text{-}v}$ the PI controller could be designed as:

$$\begin{aligned} &\left| \ell \qquad C-v) \right|_{\omega_{SOC-v}=2\pi f_{SOC-v}} \\ &= \left| \left(K_{pSOC-v} + \frac{K_{iSOC-v}}{j\omega_{SOC-v}} \right) K_v G_{vio}(j\omega_{SOC-v}) \right|_{\omega_{SOC-v}=2\pi f_{SOC-v}} \end{aligned} \tag{4.19}$$

$$\begin{aligned} &\angle \ell \qquad C-v) \Big|_{\omega_{SOC-v}=2\pi f_{SOC-v}} \\ &= \angle \left(K_{pSOC-v} + \frac{K_{iSOC-v}}{j\omega_{SOC-v}} \right) K_v G_{vio}(j\omega_{SOC-v}) \Big|_{\omega_{SOC-v}=2\pi f_{SOC-v}} \geq -\frac{2}{3}\pi \end{aligned} \tag{4.20}$$

For SOC regulation loop generating I_{SCref}, shown in Fig.3.5, the loop gain is defined as:

$$\ell \qquad = \left(K_{pSOC-c} + \frac{K_{iSOC-c}}{s} \right) K_c G_{iio}(s) \tag{4.21}$$

where $K_{pSOC\text{-}c}$ and $K_{iSOC\text{-}c}$ are the proportional term and integral term of the designed PI compensator, and K_c is the converter gain of the inner current loop which equals to 1.

The frequency margin is designed to be no smaller than π/3. Considering a proper charging current I_{SC} and cut-off frequency $f_{SOC\text{-}c}$ the PI controller could be designed as:

$$\begin{aligned} &\left|\ell \qquad _{C-c})\right|_{\omega_{SOC-c}=2\pi f_{SOC-c}} \\ &=\left|\left(K_{pSOC-c}+\frac{K_{iSOC-c}}{j\omega_{SOC-c}}\right)K_c G_{iio}\left(j\omega_{SOC-c}\right)\right|_{\omega_{SOC-c}=2\pi f_{SOC-c}} \end{aligned} \tag{4.22}$$

$$\begin{aligned} &\angle\ell \qquad _{C-c})\big|_{\omega_{SOC-c}=2\pi f_{SOC-c}} \\ &=\angle\left(K_{pSOC-c}+\frac{K_{iSOC-c}}{j\omega_{SOC-c}}\right)K_c G_{iio}\left(j\omega_{SOC-c}\right)\Big|_{\omega_{SOC-c}=2\pi f_{SOC-c}} \geq -\frac{2}{3}\pi \end{aligned} \tag{4.23}$$

4.4 Design of Surge Current Compensation Loop

When the system operates under surge current compensation mode, the control diagram can be simplified to Fig.4.7 with small-signal models derived in Section 4.1.

As illustrated in Section 3.1.1, the virtual capacitor C_{vSC} shall be designed in the first place since it mainly determines the loop's compensation effort as described in (3.10) and (3.11). In order to make the performance of surge current compensation match power demands during sudden changes in load or renewable generation, desired settling time T_s of the DC microgrid is needed. The DC microgrid's settling time here is defined as the time elapsed from a sudden load/demand change to the time at which the DC bus voltage entered and remained

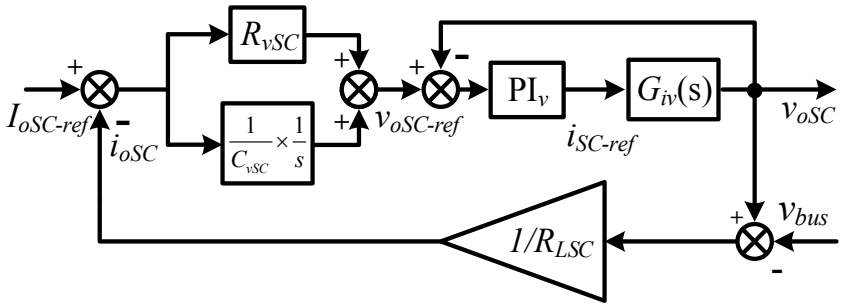


Fig.4.7 Small-signal model of surge current compensation loop

within a specified error, which could be considered as steady state. T_s is designed by taking load profiles, DGs' dynamics and tolerance fraction into consideration.

For the droop-controlled DC microgrid illustrated in this thesis, line resistance R_{L1} and virtual resistor R_{v1} of DG1 is set as 200 mΩ and 100 mΩ, respectively. The settling time T_s is designed as T_s=1s.

As illustrated by (3.9), the compensation effort simulates a typical RC charge/discharge process. Following this idea, after $t=T_s=3\tau$ (95%), the system could be considered to be brought back to its steady state after sudden changes in power demand. For the example system in this thesis consisting of specified numbers of DGs (DG1) and one SCESS, the virtual capacitor C_{vSC} can be determined from (3.12) and solved as:

$$C_{vSC} \approx \frac{1}{3} \times \frac{T_s}{R_{vSC} + R_{LSC} + R_{vDG} + R_{L1}} = 1.04F \tag{4.24}$$

Note that the virtual resistor R_{vSC} has not been designed yet. Here we simply set R_{vSC} as zero in (4.24). As would be illustrated later, R_{vSC} is designed to be as small as possible, resulting little impact on τ.

As for the design of the virtual resistor R_{vSC}, both dynamic performance and stability issues need to be considered. From this point of view, close-loop characteristic equation of the controller shown in Fig.4.7 can be deduced as:

$$s^3 + As^2 + Bs + C = 0 \tag{4.25}$$

where,

$$A = \frac{(1-D)(R_{vSC} + R_{LSC})P_v + 1}{R_{LSC}C_o} \tag{4.26}$$

$$B = \frac{1-D}{R_{LSC}C_oC_{vSC}}\left((R_{vSC} + R_{LSC})C_{vSC}I_v + P_v\right) \tag{4.27}$$

$$C = \frac{1-D}{R_{LSC}C_oC_{vSC}}I_v \tag{4.28}$$

Then dynamic performance of the control system shown in Fig.4.7 can be indicated by eigenvalues of (4.25). Fig.4.8 and Fig.4.9 show root locus of the control system presented in Fig.4.7, indicating the dynamic performance of the proposed EMS with different configurations of virtual impedance. The root locus plots the poles of the close-loop transfer function as a function of the parameter R_{v2} or C_{v2}.

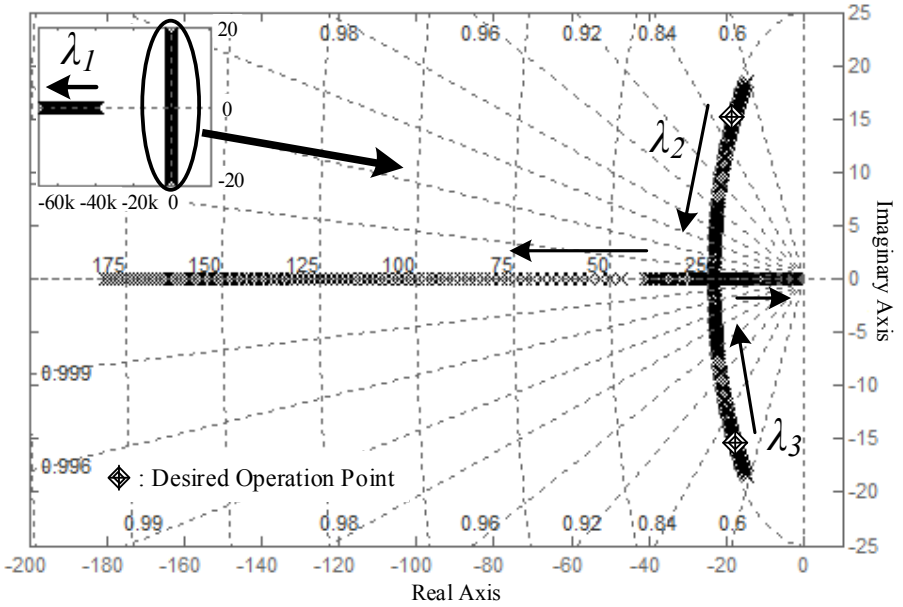


Fig.4.8 Root locus with varying virtual resistor (C_{vSC}=1F) in surge current compensation mode (arrow direction: R_{vSC} changes from 0$m\Omega$ to 500$m\Omega$).

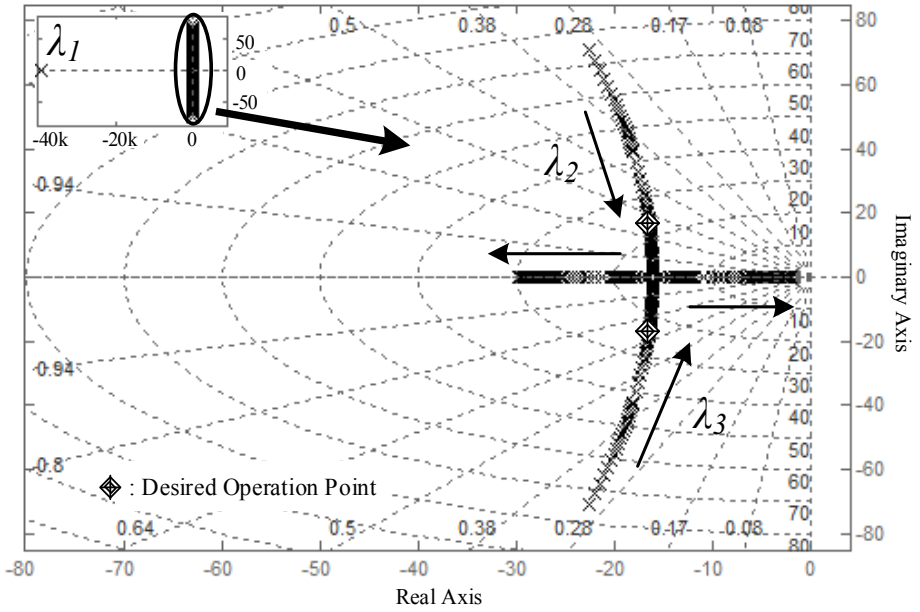


Fig.4.9 Root locus with varying virtual capacitor (R_{vSC}=7$m\Omega$) in surge current compensation mode (arrow direction: C_{vSC} changes from 0.1F to 3F).

As shown, the 3rd-order system has three poles (λ_1, λ_2 & λ_3) on left half *s*-plane. λ_1 is always on real axis, far from the imaginary axis (10 times larger than λ_2 & λ_3). And possible locations of the dominant poles (λ_2, λ_3) can be distinguished by discriminant (Δ) of (4.25), as:

$$\Delta = \left(\frac{AB}{6} - \frac{A^3}{27} - \frac{C}{2} \right)^2 + \left(\frac{B}{3} - \frac{A^2}{9} \right)^3 = \alpha^2 + \beta^3 \tag{4.29}$$

- If $\Delta<0$, then λ_2 & λ_3 are distinct real poles
- If $\Delta=0$, then λ_2 & λ_3 are multiple real poles
- If $\Delta>0$, then λ_2 & λ_3 are two non-real complex conjugate poles

And the dominant poles (λ_2, λ_3) can be solved algebraically, as:

$$\lambda_2, \lambda_3 = \frac{-1 \pm \sqrt{3}i}{2} \sqrt[3]{\alpha + \sqrt{\Delta}} + \frac{-1 \mp}{2} \quad \sqrt[3]{\alpha - \sqrt{\Delta}} - \frac{A}{3} \tag{4.30}$$

Then the system in Fig.4.7 described by cubic function (4.25) can be simplified to a 2nd order system by neglecting λ_1 (10x larger than λ_2 & λ_3), as:

$$s^2 + 2\xi\omega s + \omega^2 = 0 \tag{4.31}$$

where,

$$\omega = \sqrt{\lambda_2 \lambda_3} \tag{4.32}$$

$$\xi = -\frac{\lambda_2 + \lambda_3}{2\sqrt{\lambda_2 \lambda_3}} \tag{4.33}$$

As shown in Fig.4.8 for a specific value of C_{vSC}, the damping ratio (ξ) of the system increases as R_{vSC} increases, and the behavior of the system changes from underdamped ($\Delta>0$, $\xi<1$), to overdamped ($\Delta<0$, $\xi>1$). Fig.4.9 shows similar characteristics as well. For a specific value of R_{vSC}, an increase in C_{vSC} results larger ξ. This provides the designer a useful indicator to tune the dynamics of virtual

impedance loop. For example, one could use (3.13) together with RES & load profiles and DGs' dynamics to determine a suitable T_s or C_{vSC} (as shown in (3.12)-(3.14)), then adopt models derived in this section to tune R_{vSC}.

In this thesis, ξ=0.7 is selected as the design criteria for R_{vSC}, ensuring fast dynamic response while mitigating unnecessary overshoot. Thus, for C_{vSC}=1.04F derived earlier in this section, the corresponding virtual resistor (ξ=0.7) is solved as $R_{vSC} \approx 7m\Omega$ by combining (4.30)-(4.33). Compared to R_{LSC} which is $50m\Omega$, the calculated R_{v2} is only 14% of the former, which shall have an insignificant influence on accuracy of (3.12), as expected earlier. Bode diagrams shown in Fig.4.10 confirms the accuracy of (3.12), as the closed-loop bandwidth of the designed virtual impedance loop (17.8 *rad/s*) is 5x smaller than the inner voltage loop (96.3 *rad/s*) designed in Section 4.2.

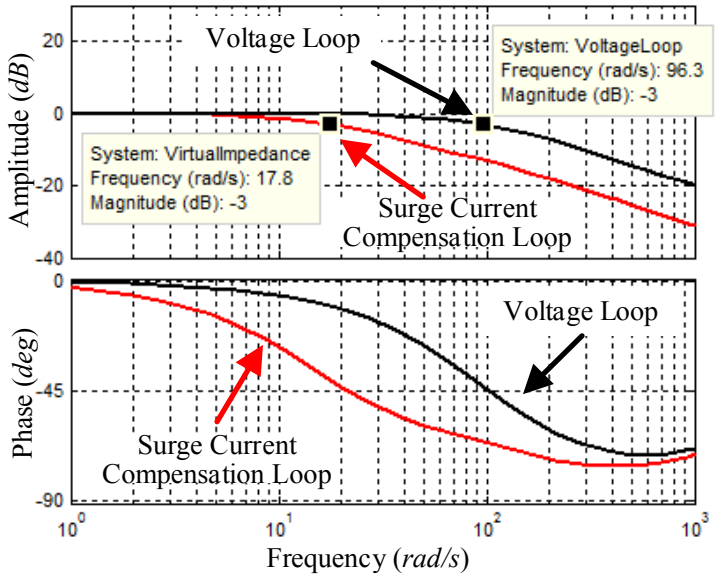


Fig.4.10 Closed-loop bode diagrams of inner voltage loop and surge current compensation loop

Note that the system remains stable as changes of R_{vSC}.or C_{vSC}. are within rational ranges (R_{v2}.changes from 0 to $10R_{L2}$.for specific C_{vSC}, or C_{vSC} changes from 10% to 300% for specific R_{v2}), as is shown in Fig.4.8 & Fig.4.9. This validates that the designed virtual impedance loop provides reliable and satisfying surge current compensation performance with robustness and flexibility, which is able to be deployed in a variety of applications.

4.5 Summary

This chapter presents the iterative frequency-shaping method to design and tune PI controllers and virtual impedances loop-by-loop. These the control efforts are achieved by concise multi-loop controller design, making the tuning process more intuitive to meet specific requirements of dynamic performance and stability margin.

The results show that the proposed EMS provides reliable and satisfying dynamic performance with considerable robustness and flexibility, which is able to be deployed in a variety of applications.

Chapter 5

Simulation and Experiment Verification

In this chapter, simulation and experiment verification of the proposed EMS are presented. The system is simulated in MATLAB/SIMILINK. The experiment is carried out on a platform designed and constructed as part of this thesis work. Key parameters used in simulation and experiment are given. A brief description for the design of experimental platform with intelligent power modules (IPMs) and dSPACE DS1103 PPC controller board is also presented.

5.1 Simulation verification

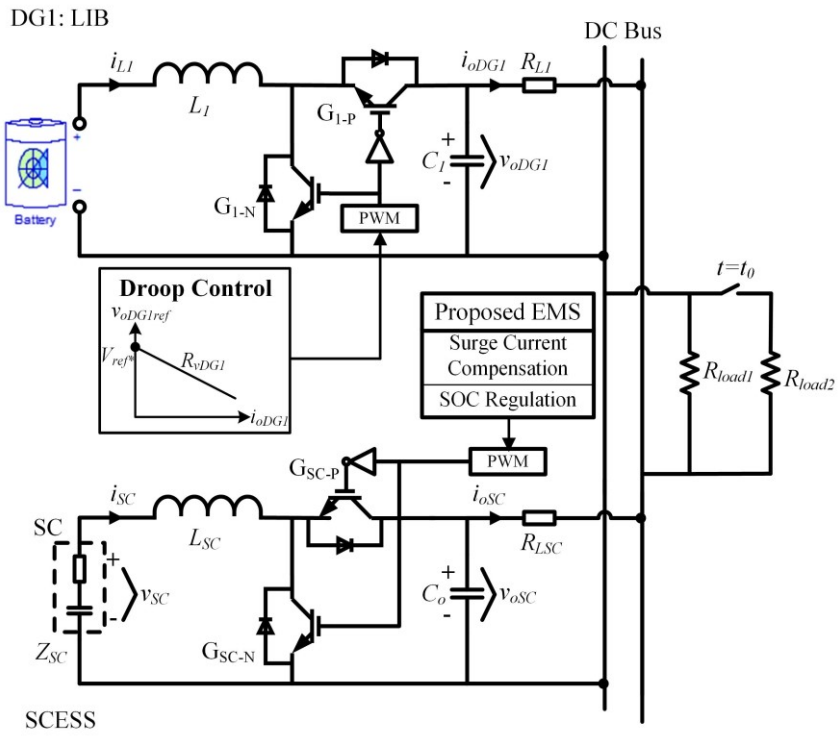


Fig.5.1 Circuit &control configuration used in simulation

In order to investigate the effectiveness of the proposed EMS, a DC microgrid consisting of one DG unit interfacing with a Li-ion battery (DG1), one SCESS and resistive loads has been modeled. The circuit configuration of the system is shown in Fig.5.1. The system was simulated using MATLAB/SIMULINK (8.1.0.604)

with parameters shown in Table.5.1.

As illustrated in Fig.5.1, DG1 and SCESS are powered with the LIB and SC respectively. In steady state, DG1 supplies the resistive loads and helps regulate SC's SOC. During transients (e.g. sudden load changes), SCESS will supply/absorb the burst power so as to achieve smooth transition of DG1's operation point (current of inductor).

Table. 5.1 Circuit and control parameters in the simulation

Symbol	Parameter	Value
f_s	Switching Frequency	$20kHz$
V_{ref*}	DC Bus Voltage Reference	$60V$
L_1, L_{SC}	Boost Inductor	$2.5mH$ (DG1);$0.5mH$ (SCESS)
C_1, C_o	Filter Capacitor	$940\mu F$ (DG1);$500\mu F$ (SCESS)
R_{Load1}, R_{Load2}	Resistive Loads	15Ω, 15Ω
R_{L1}	Line Resistance (DG1)	$200m\Omega$
R_{v1}	Virtual Resistor (DG1)	$100m\Omega$
R_{LSC}	Line Resistance (SCESS)	$50m\Omega$
R_{vSC}	Virtual Resistor (SCESS)	$0\sim250m\Omega$
C_{vSC}	Virtual Capacitor (SCESS)	$0.5F\sim2F$
K_{pc}	Proportional term for Current Loop Compensator (SCESS)	0.08
K_{pv}	Proportional term for Voltage Loop Compensator (SCESS)	1.24
K_{iv}	Integral term for Voltage Loop Compensator (SCESS)	4000

5.1.1 Case Study I: Surge Current Compensation

Fig.5.2 and Fig. 5.3 demonstrate dynamic performance of the proposed EMS facing sudden load changes with different virtual impedance combinations. In both cases (load step-up & step-down), the output current of SC changes quickly to meet abrupt variations of power demand, allowing for smooth transitions of Li-ion battery's output current, which realizes surge current compensation and keeps the Li-ion battery of DG1 from supplying surge power. When the system returns to steady state, output current of SC returns to zero, which is favorable for narrowing SC's SOC range.

Comparisons shown in Fig.5.2 and Fig.5.3 validate conclusions of previous section that SC's dynamics are able to be managed by tuning virtual impedances. Increasing virtual capacitor increases damping ratio and results in better

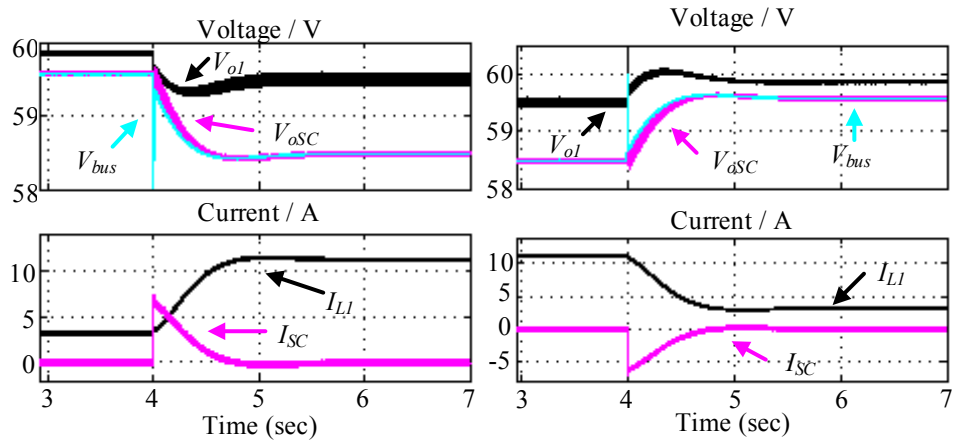


Fig.5.2 Dynamic performance of the proposed EMS during sudden load step-up (left) and step-down (right): C_{vSC}=1.04F, R_{vSC}=7$m\Omega$, ξ=0.70, 3τ=1.0s.

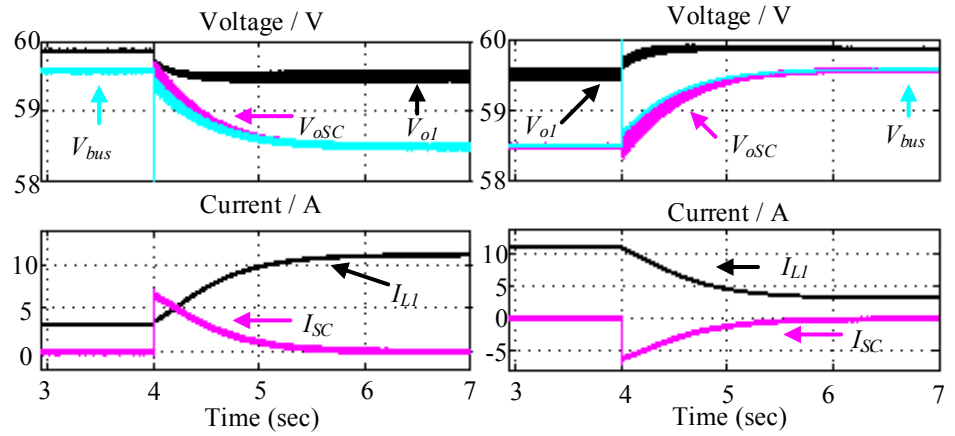


Fig.5.3 Dynamic performance of the proposed EMS during sudden load step-up (left) and step-down (right): C_{vSC}=2.08F, R_{vSC}=0$m\Omega$, ξ=0.87, 3τ=2.0s.

compensation effort, since more energy is released from a larger virtual capacitor. In both Fig.5.2 (C_{vSC}=1.04F, R_{vSC}=7$m\Omega$, ξ=0.70) and Fig.5.3 (C_{vSC}=2.08F, R_{vSC}=0$m\Omega$, ξ=0.87), SCESS's output current returns to zero after t=3τ with negligible overshoot, which meets the design goals derived by (3.12) and (4.33).

5.1.2 Case study II: Damping effect of the virtual resistor

Fig.5.4 and Fig.5.5 demonstrate damping effect provided by the virtual resistor. Significant oscillations are observed in Fig.5.4 during sudden load changes due to a small virtual resistor that results small damping ratio (Fig.5.4: C_{vSC}= 0.5F, R_{vSC}=7mΩ, ξ=0.52).

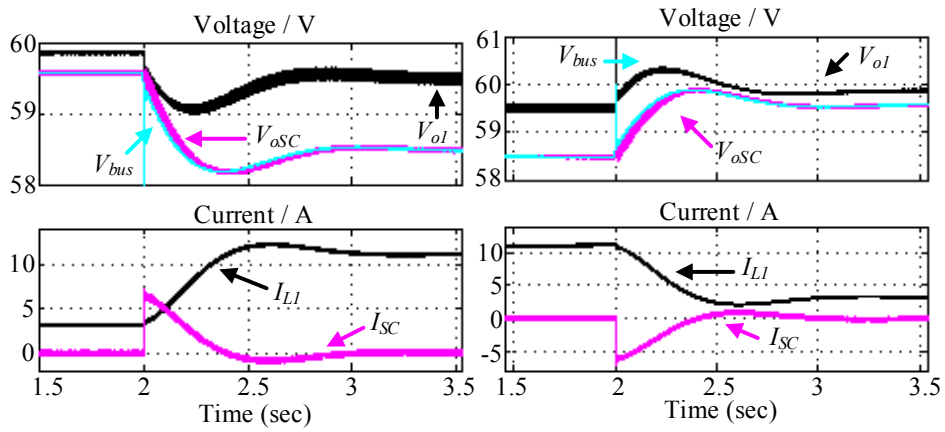


Fig.5.4 Mitigating oscillations during sudden load step-up (left) and step-down (right) by increasing virtual resistor to provide additional damping: C_{vSC}= 0.5F, R_{vSC}=7mΩ, ξ=0.52

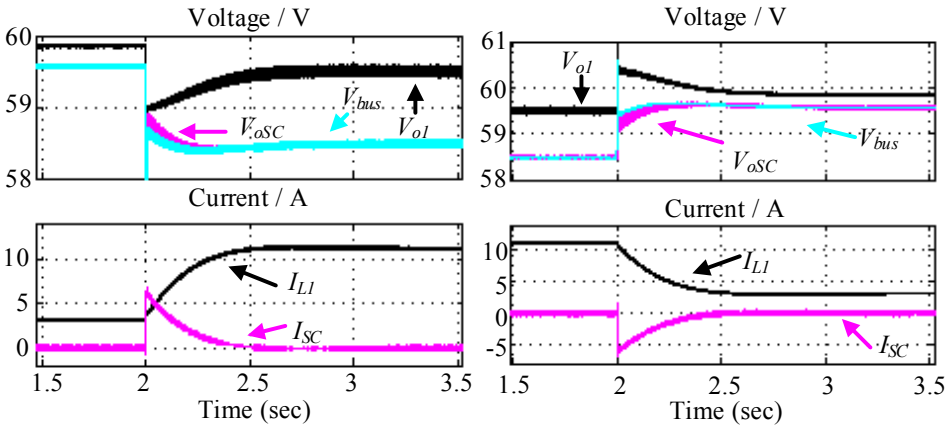


Fig.5.5 Mitigating oscillations during sudden load step-up (left) and step-down (right) by increasing virtual resistor to provide additional damping: C_{vSC}=0.5F, R_{vSC}=220mΩ, ξ=2.1

Comparisons between Fig.5.4 & Fig.5.5 show that larger virtual resistor (R_{vSC} changes from R_{vSC}=7mΩ in Fig.5.4 t220mΩ in Fig.5.5) helps mitigate oscillations by increasing damping ratio. Note that a too large virtual resistor could significantly raise the control bandwidth of the virtual impedance loop so that unnecessary coupling between virtual impedance loop and inner voltage regulation loop may occur. This would affect the accuracy of (3.12), making it hard to estimate the compensation effort. Note that for damping purpose, the virtual resistor is usually not too large, and (4.32) and (4.33) could help the designer to estimate time constant and damping ratio as well. However, for situations where a very large virtual

resistor is desired, a better approach is to increase C_{vSC} and run through the iterative frequency-shaping design process to achieve a smaller R_{vSC} that follows (3.12).

5.2 Experiment verification

5.2.1 Description of Experimental platform

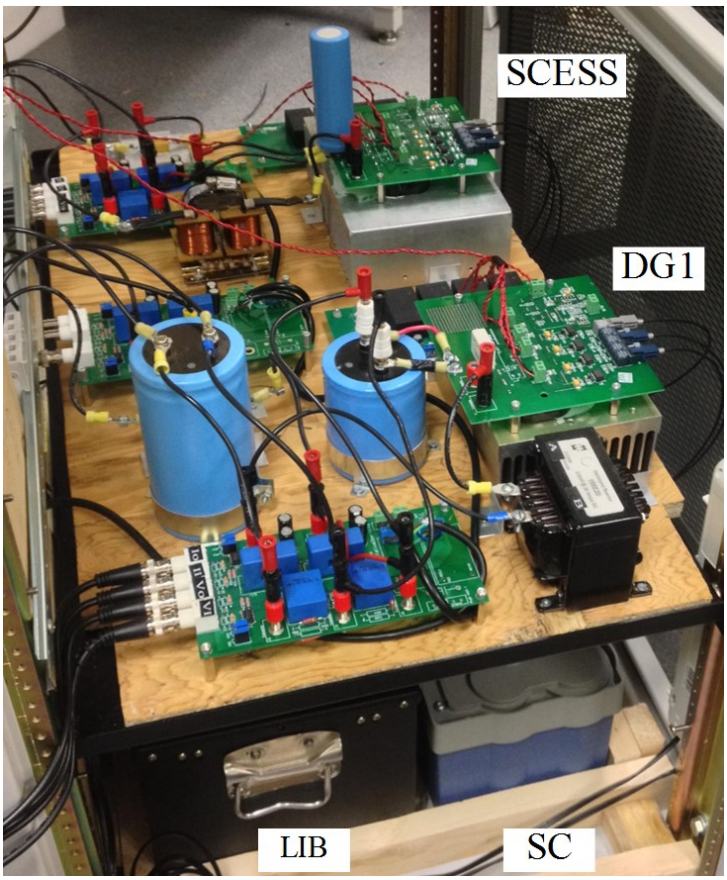


Fig.5.6 Experiment set-up

A prototype of droop-controlled DC microgrid consisting of two 1kW bidirectional DC/DC boost converters with resistive loads were built, to verify the effectiveness of the proposed EMS. A picture of the prototype is shown in Fig.5.6. The system was controlled by dSPACE DS1103 PPC controller board, using system configuration and control parameters shown in Fig.5.7 and Table 5.2.

As shown on Fig.5.7, the dSPACE DS1103 PPC controller board generates PWM signals for both the two bidirectional boost converters using its built-in TMS320F2808 digital signal processor. The PWM signals are first transmitted to a

signal-shaping board which uses analog logic circuits to mitigate noises and shapes the PWM signal for fiber optic links (HFBR-2521/1521).

Table.5.2 Circuit and control parameters in the experiment

Symbol	Parameter	Value
f_s	Switching Frequency	$20kHz$
V_{ref*}	DC Bus Voltage Reference	$60V$
L_1, L_{SC}	Boost Inductor	$2.5mH$ (DG1);$0.5mH$ (SCESS)
C_1, C_o	Filter Capacitor	$940\mu F$ (DG1);$500\mu F$ (SCESS)
R_{Load1}, R_{Load2}	Resistive Loads	15Ω, 15Ω
R_{L1}	Line Resistance (DG1)	$200m\Omega$
R_{v1}	Virtual Resistor (DG1)	$100m\Omega$
R_{LSC}	Line Resistance (SCESS)	$50m\Omega$
R_{vSC}	Virtual Resistor (SCESS)	$0\sim250m\Omega$
C_{vSC}	Virtual Capacitor (SCESS)	$0.5F\sim$2F
K_{pc}	Proportional term for Current Loop Compensator (SCESS)	0.05
K_{ic}	Integral term for Current Loop Compensator (SCESS)	2
K_{pv}	Proportional term for Voltage Loop Compensator (SCESS)	0.9
K_{iv}	Integral term for Voltage Loop Compensator (SCESS)	200

Then the shaped PWM signals are transmitted to IPM controller board of each converter. On the IPM controller board, the isolated PWM signals will be delivered to inputs of IPM, which has its built-in IGBT drivers and protection circuits. The fault signal of IPM controller board is then transmitted through fiber optic links back to the signal-shaping board. The signal-shaping board is able to react to fault signals sent by the controller board or the IPM controller board to provide protections for IPM realized by fast analog logic circuits. The fault signals such as over-voltage warning signal from SC module are also connected to IPM controller board and transmitted back to signal-shaping board.

The IPM controller board drives the two switches of the bidirectional boost converter, and forms DG1 and SCESS together with corresponding RESs (Li-ion battery and SC, respectively) and passive components such as inductors & output capacitors. The snubber circuit for IGBT is composed of a film capacitor that help suppress voltage transients. DG1 and SCESS are connected to common DC bus with resistive loads to form a DC microgrid. Sensor boards with voltage & current

transducers (LV20P & LA55P) perform measurements and send the analog signals back to controller board which has built-in 16-bit A/D converters.

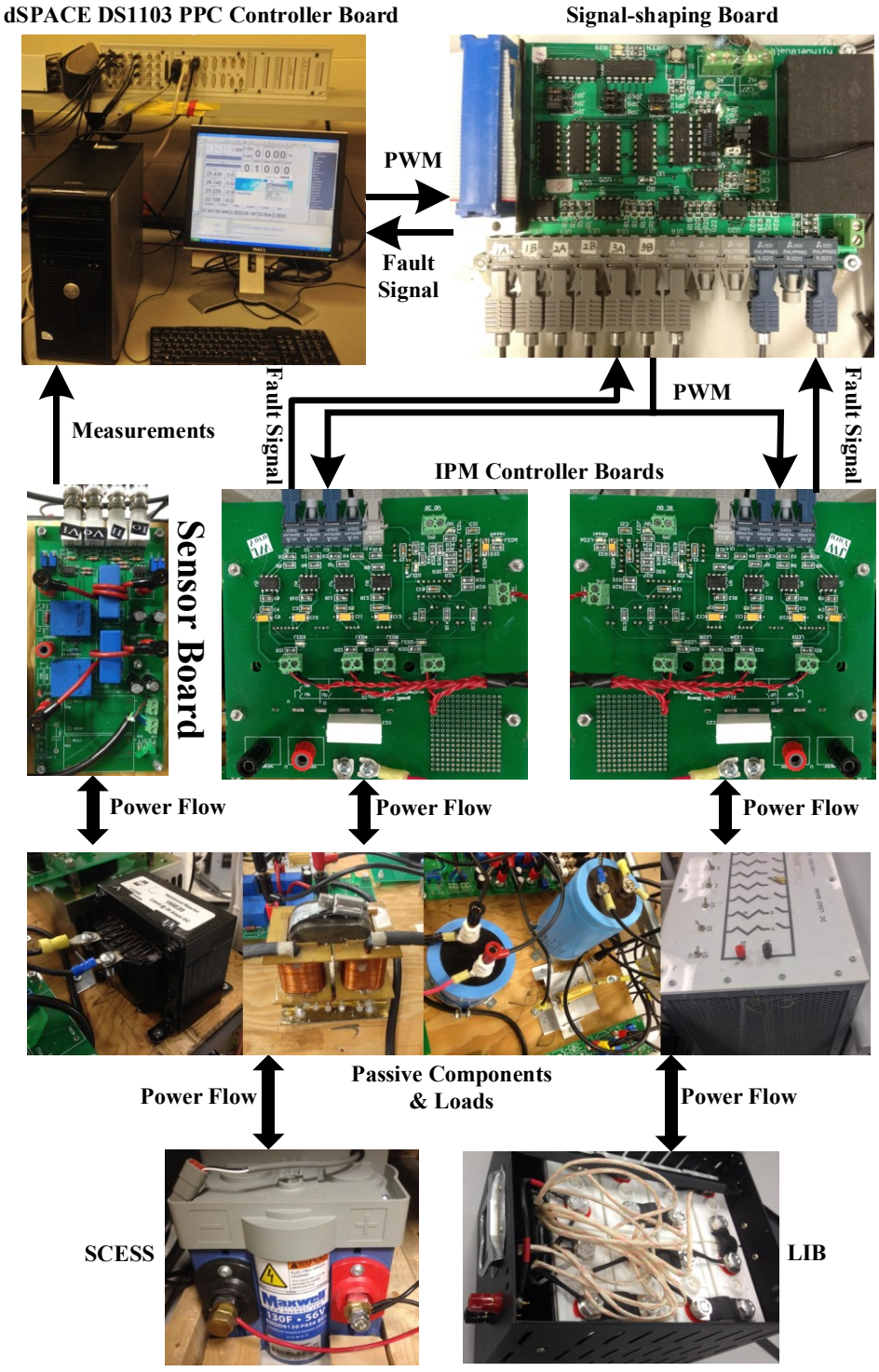


Fig.5.7 System configuration of the experimental platform

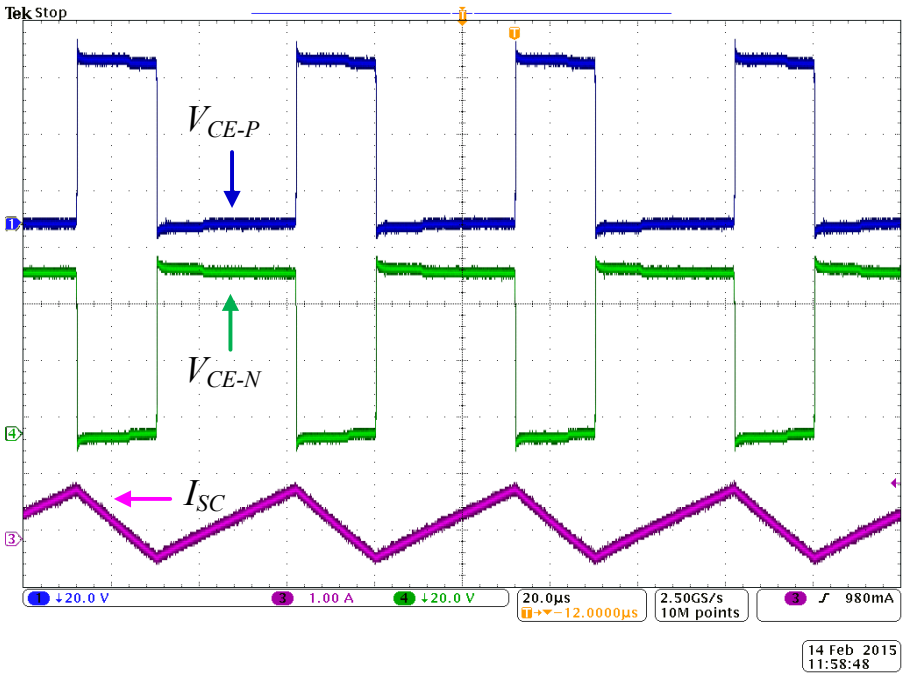


Fig.5.8 Closed-loop switching waveforms of the designed SCESS

The switching waveforms of the designed SCESS module with close-loop voltage/current regulation & virtual impedance loop operating in steady state is shown in Fig.5.8. As shown, the voltage between collector and emitter of IGBTs (V_{CE-P} denotes the upper leg and V_{CE-N} denotes the lower leg) results little spikes during switching actions, indicating the film capacitor is adequate for the snubber design. The results also shown that dead zone ($2\mu s$ for f_s=$20kHz$) has insignificant effect on operation of the designed bidirectional boost converter.

5.2.2 Case Study I: Surge Current Compensation

Fig.5.9 and Fig.5.10 depict the steady-state and transient response of the droop-controlled DG1 (Li-ion battery) and SCESS managed by the proposed EMS with matching parameter configurations of virtual impedance loop shown in Table.5.2. At steady state, DG1 supplies the resistive load and output current of SCESS remains zero. When a sudden load change occurs, SCESS supplies/absorbs burst power when a sudden load change occurs, allowing for smooth changes in the output current of the battery (DG1).

The results show an excellent dynamic response of the proposed EMS. In both

Fig.5.9 (τ=1/3 s, C_{vSC}=1.04F, R_{vSC}=7$m\Omega$, ξ=0.70) and Fig.5.10 (τ=2/3 s, C_{vSC}=2.08F, R_{vSC}=0$m\Omega$, ξ=0.87), SCESS's output current returns to zero after t=3τ with negligible overshoot, which confirms conclusions in Section 4.4 and simulation, that the time constant and damping ratio are able to be tuned by (3.12) & (4.33).

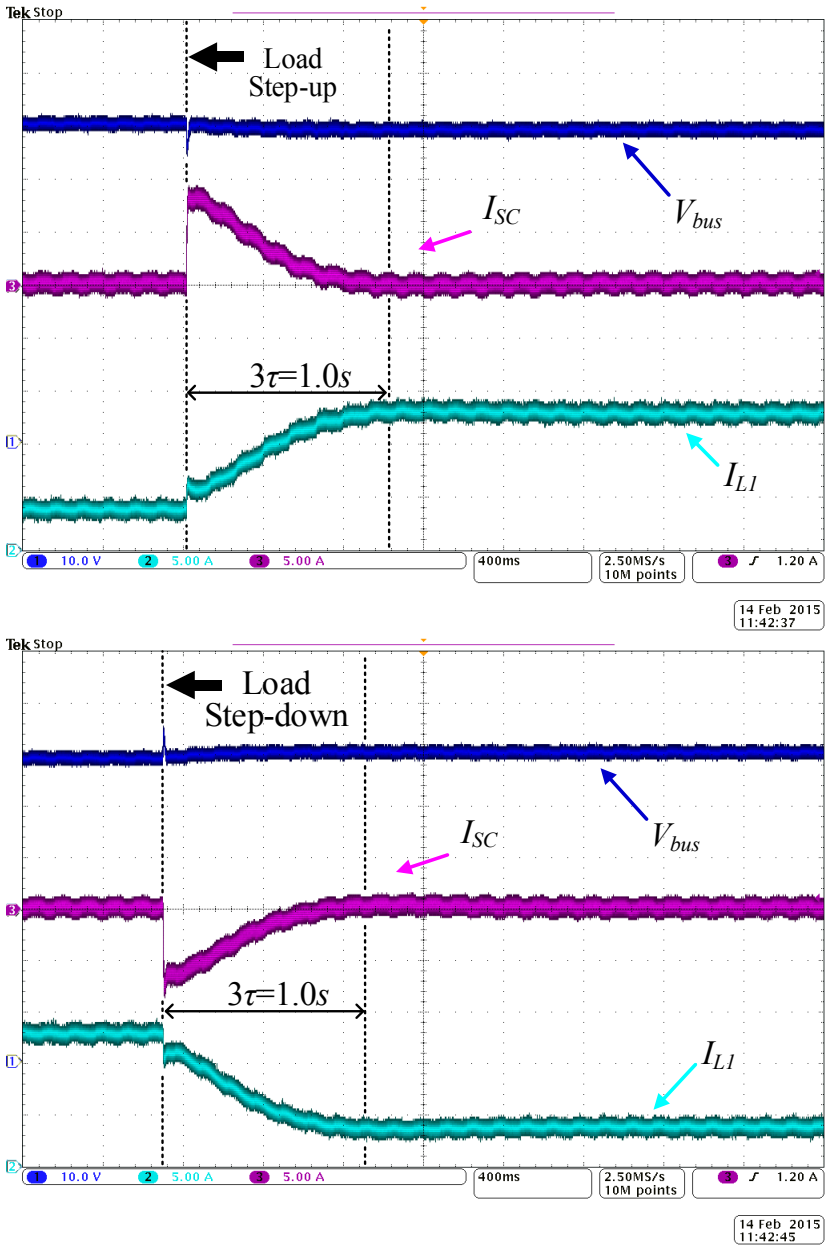


Fig.5.9 Steady-state and dynamic performance of the proposed EMS during sudden load step-up (up) and step-down (down) with different values of virtual resistor R_{vSC} and virtual capacitor C_{vSC} (DC bus voltage V_{bus}: 10 V/div; Inductor currents I_{L1}: 5 A/div, I_{SC}: 5 A/div; Time: 400 ms/div) : C_{vSC}=1.04F, R_{vSC}=7$m\Omega$, ξ=0.70, 3τ=1.0s.

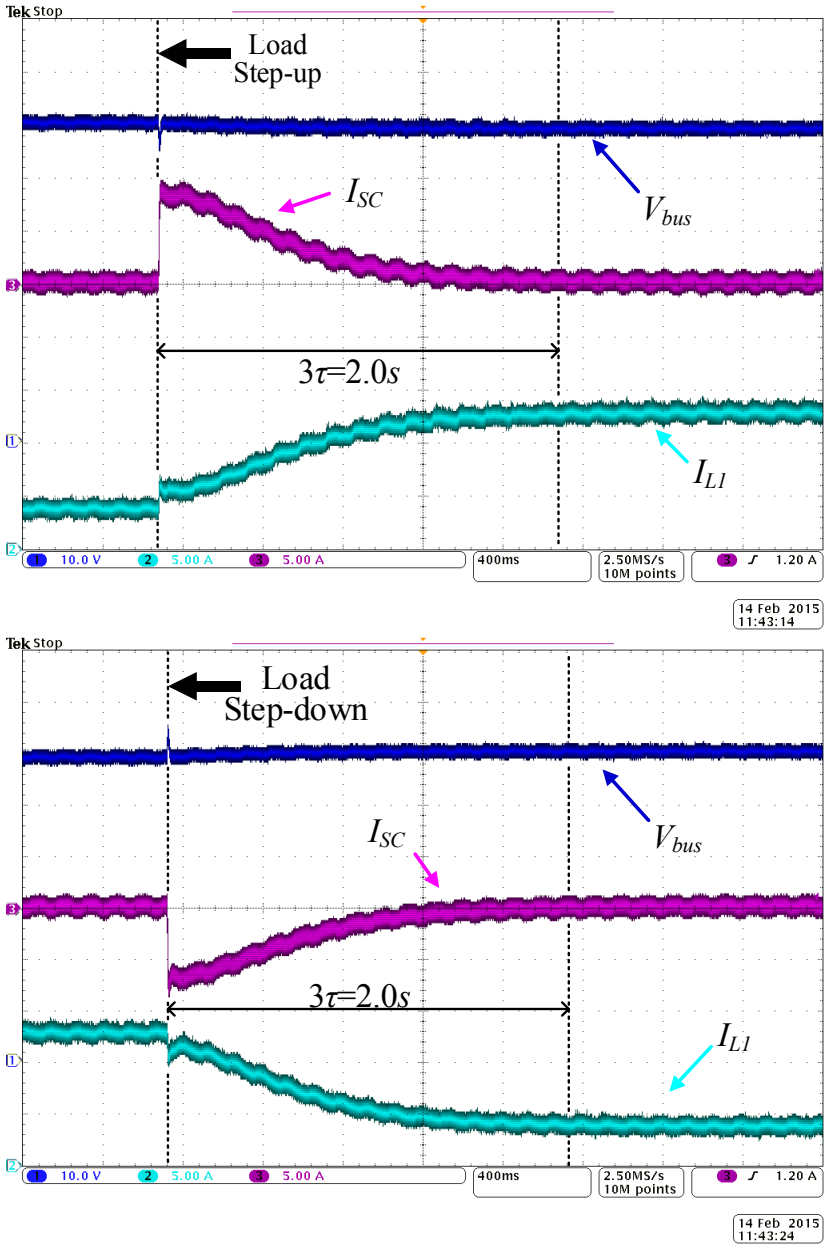
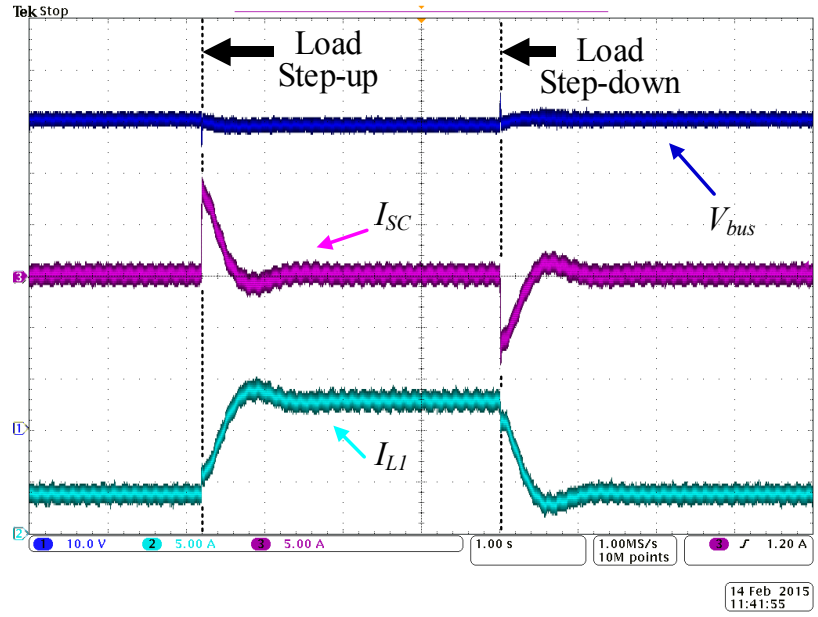


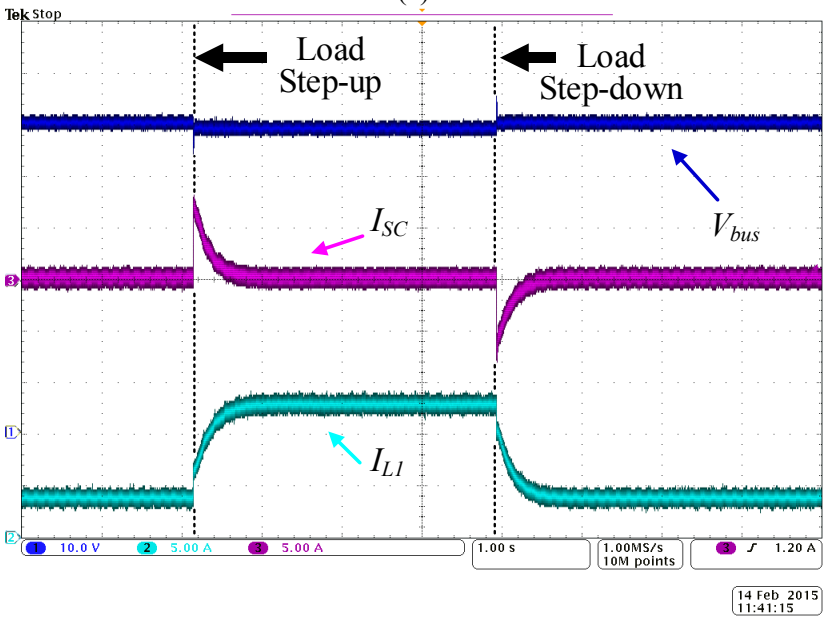
Fig.5.10 Steady-state and dynamic performance of the proposed EMS during sudden load step-up (up) and step-down (down) with different values of virtual resistor R_{vSC} and virtual capacitor C_{vSC} (DC bus voltage V_{bus}: 10 V/div; Inductor currents I_{L1}: 5 A/div, I_{SC}: 5 A/div; Time: 400 ms/div) : C_{vSC}=2.08F, R_{vSC}=0$m\Omega$, ξ=0.87, 3τ=2.0s.

5.2.3 Case study II: Damping effect of the virtual resistor

Fig.5.11 validates the damping effect of the virtual resistance. Oscillations in Fig.5.11 (a) are mitigated by increasing the virtual resistor from (Fig.5.11(a): C_{vSC}= 0.5F, R_{vSC}=7mΩ, ξ=0.52) to (Fig.5.11(b): C_{vSC}=0.5F, R_{vSC}=220mΩ, ξ=2.10), as is shown in Fig.5.11(b).



(a)



(b)

Fig.5.11 Damping effect of the virtual resistor (DC bus voltage V_{bus} : 10 V/div; Inductor currents I_{L1}: 5 A/div, I_{SC}: 5 A/div; Time: 1 s/div). (a) C_{vSC}= 0.5F, R_{vSC}=7mΩ, ξ=0.52 (calculated) (b) C_{vSC}=0.5F, R_{vSC}=220mΩ, ξ=2.10 (calculated)

5.2.4 Case study III: performance of SOC regulation and mode switcher

The performance of mode transitions between surge current compensation mode and SOC regulation mode is shown in Fig.5.12. The result shows that the proposed

EMS decouples the control of SOC regulation and surge current compensation. As is shown in Fig.5.12, SCESS returns to surge current compensation mode from SOC regulation mode with negligible disturbance to the other DG and the DC bus, realizing seamless transfer between both modes.

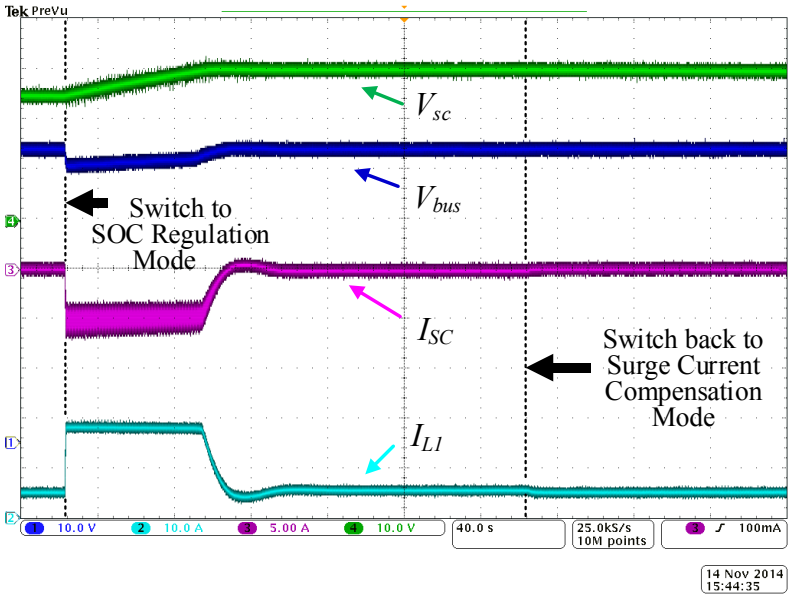


Fig.5.12 Mode Switch between SOC regulation mode and surge current compensation mode (DC bus voltage V_{bus}: 10 V/div; Inductor currents I_{L1}: 5 A/div, I_{SC}: 10 A/div; Time: 40 s/div).

5.3 Summary

This chapter illustrates simulation and experimental results related to the proposed EMS described in Chapter 3 and Chapter 4. Circuit configurations and control parameters used in simulation and experiment are also presented.

The results confirm that the proposed EMS is able to perform surge current compensation without physical communication lines, realizing the plug'n'play feature. The simulation & experimental results also show that the proposed virtual impedance loop could adjust the compensation dynamics by tuning virtual resistor R_{vSC} and a virtual capacitor C_{vSC}, which matches deduction of (3.12) & (4.33). Furthermore, the resulted system is proved to provide satisfying surge current compensation with a wide value range of R_{vSC} and C_{vSC}, which suggests the

proposed EMS provides reliable dynamic performance with considerable robustness and flexibility, which is able to be deployed in a variety of applications.

As for SOC regulation, the experimental results show that performance of the proposed SOC regulation loop together with mode switcher meets the design goal illustrated in Chapter 4 that SC's SOC is regulated to its normal value without unnecessary coupling with inner voltage/current regulation loops and virtual impedance loop. Seamless transfer performed by the mode switcher is also confirmed as effective in the experiment.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

As reviewed in Chapter 1 and Chapter 2, an effective EMS for SCESS in droop-controlled DC microgrids is not available in literature. Several improvements could be added to existing approaches but the resulted systems fail to circumvent their intrinsic disadvantages. Therefore, this thesis proposes a novel EMS for SCESS in droop-controlled DC microgrids. The proposed EMS employs virtual impedance loop composed of a virtual resistor and virtual capacitor to provide surge current compensation, and an independent SOC regulation loop to regulate SC's SOC. These two working modes (compensation mode and SOC regulation mode) are determined by a mode switcher, which provides seamless transfer between two modes.

The control efforts are achieved without acquisitions of accurate power demands provided by distributed sensors and communication lines, so that plug'n'play is realized. In addition, system modeling and stability analysis in Chapter 3 and Chapter 4 confirm that the virtual impedance loop makes the performance of surge current compensation predictable and adjustable. The iterative frequency-shaping method illustrated in Chapter 4 makes the design progress easier and more intuitive for designers to estimate and optimize dynamic performance of the proposed EMS. Furthermore, the dynamic performance of surge current compensation and SOC regulation are decoupled by a mode switcher. This makes the proposed EMS easily adapted to various applications of different specifications on dynamic response, which further extends the flexibility of the proposed EMS.

The simulation & experimental results in Chapter 5 show that the proposed EMS is able to meet power demands during sudden load changes in order to protect sensitive DGs from supplying burst power. Time constant of the designed EMS is

estimable and adjustable, confirming that the dynamic performance of the proposed EMS is controllable and predictable. In addition, the proposed mode switcher is able to achieve seamless transfer between SOC regulation mode and surge current compensation mode, resulting little disturbances to the DC bus during transitions.

6.2 Future work

Based on the research presented in this thesis, several areas where future work is needed are indicated as follows.

Firstly, more work shall be devoted to the sizing of SC in order to provide designers with detailed guidelines when integrating SCESS into existing droop-controlled DC microgrids.

Secondly, the dynamic response of the proposed EMS could be further enhanced, so as to provide even better compensation efforts in order to further mitigate voltage spikes during sudden load/supply changes. For example, current feed-forward could be added to the inner current loop, by adding output current of the filter capacitor C_o, indicated by $C_o \times dV_{oSC}/dt$.

Thirdly, as mentioned in Section 3.1, the both virtual impedances (resistor R_{vSC} /capacitor C_{vSC}) have the potential to be adjusted dynamically instead of fixed to default values, in order to combine the advantages of both type of virtual impedances. As indicated by Chapter 4 and later confirmed in Chapter 5, larger C_{vSC} results better compensation efforts but increases time constant, while larger R_{vSC} provides extra damping effect but may introduce unnecessary coupling between control loops. For example, a more effective surge current compensation might be realized by increasing C_{vSC} while maintaining R_{vSC} to a relatively small value at the beginning of sudden load/supply changes, and reducing C_{vSC} and increasing R_{vSC} later, in order to bring the system back to steady state more quickly. However, stability analysis under such circumstance shall be more complicated as parameters in virtual impedance loop are dynamically changing according to disturbances.

Finally, reliable EMS for parallel operation of multiple SCESS modules in droop-controlled DC microgrid needs further investigation. As the scale of DC microgrid develops, it's entirely possible that a DC microgrid may have several SCESSs that operate simultaneously sharing surge power. Unlike traditional droop method that focuses on steady-state power sharing, the novel EMS focuses on power sharing during sudden load/supply changes. Under such circumstances, a reliable EMS is desired that realizes transient power sharing between SCESS modules in order to narrow their range of SOC while achieves power sharing ability with plug'n'play feature or much less dependency on extensive physical communications compared to traditional centralized master-slave EMS in Chapter 2.

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