Wide Input Voltage Inverter Configurations and Control Systems for Renewable Energy Resources

by

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Abstract

Nowadays, among renewable energy sources, PV systems are highly popular due to their easy installation and affordability. A key component of the PV system is the inverter, which can significantly affect the reliability, efficiency, and power quality of the system. The PV inverters are required to track the maximum power point (MPP) of the panel to maximize the production of the system. To achieve this goal, the inverter must be able to generate the required output waveforms for a wide range of input voltages. Normally, two-stage inverters are used to achieve this goal and produce high-quality output power; however, both stages process the full output power and have a high number of reactive components with high switching stress which can result in lower power density and higher losses of the converter. In this thesis, new topologies are proposed to reduce the required number of passive components for the inverter while allowing it to operate for a wide range of input voltages and maintain the power quality of the output.

The first proposed design features an extended input voltage range using a cascaded full-bridge inverter with a cascaded floating capacitor, leveraging low-frequency operation to generate fundamental output voltage components. It is coupled with low-voltage high-frequency operation to mitigate harmonics. A comprehensive control mechanism is used to regulate the modulation angle of the low-frequency full bridge. Additionally, a synchronous (or DQ) reference frame controller is used to regulate current and enable MPP tracking. To further reduce the blocking voltage of the capacitor-connected full bridge, the second structure replaces the PV-connected full bridge with a T-type inverter, halving the blocking voltage.

The flyback-assisted inverter is also proposed to further extend the inverter's operating input voltage range. This topology integrates cascaded full-bridge inverters

with a flyback converter. This configuration allows the high-frequency full bridge to process a portion of the power based on input voltage. Precise control mechanisms for determining modulation angles and maximum power point tracking (MPP) in PV systems are implemented. Furthermore, the controller deactivates the flyback converter when the photovoltaic (PV) voltage reaches an optimal level for generating the desired output voltage. This reduces switching losses and can further improve converter efficiency.

Furthermore, a cascaded full-bridge converter with a single switching frequency is proposed to accommodate the broad voltage range of the flyback-assisted converter, while minimizing component count, and improving power density. A new control structure for the fast and robust operation of the inverter is proposed. These control mechanisms can independently regulate the power of each full bridge, allowing the converter to operate within a wide range of input voltages.

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Chapter 1

Introduction

Nowadays, the adoption of renewable energies in distributed generation, transportation, and multi-energy systems has become a vital factor in shaping a sustainable future free from fossil fuels. DC-AC inverters, with their significant power transformation capabilities for AC loads or grids, play a critical role in harnessing the potential of solar energy, wind power, and hydrogen, enabling the efficient utilization of these Eco-friendly sources [1].

Among renewable energies, PV systems are highly popular due to their easy installation and affordability. Over the years, grid-connected PV inverter systems have experienced widespread and successful commercialization, facilitating the rapid growth of solar energy generation [3]. Recently, there has been a significant demand for both commercial and residential use, leading to rapid development in single-phase grid-connected voltage source inverters' technology in the last decade [4].

The majority of single-phase PV inverters available in the market utilize a two-stage architecture [5], [6]-[13]. This architecture consists of a DC-DC maximum power

point tracking (MPPT) converter and a voltage source inverter. The rationale behind this approach lies in the fact that the optimal voltage of a PV panel to generate the maximum power sometimes falls below the peak value of the grid voltage [5]. To overcome this limitation, a boost converter is employed to step up the voltage in a DC link, enabling the buck-type voltage source inverter to deliver power to the grid.

In addition, some single-phase inverters have only a one-stage inverter system with a low-frequency transformer, allowing for the attainment of an output peak AC voltage greater than the input DC voltage. This is achieved by combining a full-bridge inverter with a low-frequency step-up transformer [16]. However, the inclusion of a bulky transformer introduces additional challenges, such as increased system volume, higher losses, and elevated overall system cost [17].

Finally, there are single-phase single-stage topologies. These inverters require a buck-boost-type DC-AC behavior that can be operated in a wide input range of voltage. This thesis aims to propose novel wide input range inverter topologies that can provide the desired output voltage without the need for a bulky transformer or multiple passive components [5] and [18]. Moreover, the proposed topology aims to address the challenges associated with previously proposed single-stage power converters.

1.1 Review of Existing Wide Input Voltage Range Inverters

Converters with wide input ranges can be mainly divided into three categories. Firstly, two-stage converters: this type of converter consists of two stages that collaborate to generate the required output voltage [7]. Second is two-mode converters:

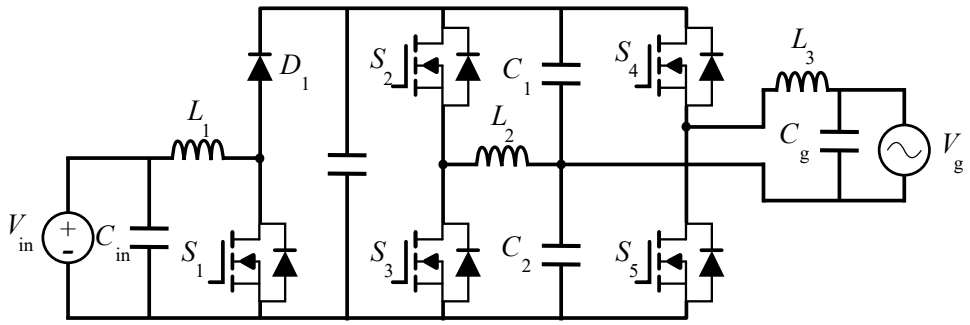
these converters can operate as either two-stage or single-stage converters based on the input voltage [19]. Typically, they function as two-stage converters when the input voltage is low. However, when the input voltage exceeds the peak of the grid voltage, they operate as single-stage power converters. Finally, there are single-stage power converters, where the circuit only includes one component responsible for generating the desired voltage [20].

1.1.1 Two-Stage Wide Input Range Inverters

This type of converter generates output voltage with the assistance of passive components, such as capacitors or inductors, positioned within the configuration as storage elements. These components enable the transfer of generated power from a PV source to the grid. One stage is responsible for transferring power from the PV source to these reactive components, while the second part of the circuit processes this power to generate the required AC output voltage [6]-[13].

Two-stage topology was proposed in [3], where a front-end boost stage is combined with a half-bridge inverter stage, and a buck-boost power decoupling stage, Fig. 1.1. The boost converter in the first stage is responsible for regulating the capacitor voltage at a higher level, enabling a wide range of input voltages and coping with partial shading conditions. The second inverter stage is responsible for decoupling the double grid freq oscillations and generating the output AC voltage; this part of the converter will operate in buck mode.

Using the boost DC/DC converter and buck inverter enables this circuit to operate across a wide range of PV source voltages and track the MPP of the system. Furthermore, the implementation of the power decoupling stage has led to a reduction in the size of the circuit's capacitor and allows for the exclusive use of film capacitors



(a)

Figure 1.1: Half-Bridge Voltage Swing Inverter [3].

in the system's structure. However, it's important to note that all switches in the system operate at high frequencies and high voltages, and the circuit requires a higher number of components, which results in the complexity of the system, increasing the costs, and a lower power density for the overall circuit [4].

The Z-source and quasi-Z-source inverters, as described in references [21] and [22], utilize an impedance network consisting of inductors and capacitors to enable the converters to operate over a wide range of input voltages (Fig. 1.2). The operation of these converters can be categorized into two modes: the active mode, and the shoot-through mode. These converters capitalize on the shoot-through state, a condition where both switches in the inverter are momentarily closed, to facilitate efficient power conversion.

However, there are certain drawbacks associated with these inverters. As they are designed to provide a boosting capability, the voltage and current stress on the components are higher than in a conventional converter system. This can pose challenges when it comes to component selection and overall system reliability [23].

Another drawback of the Z-source and quasi-Z-source inverters is the larger number of components involved in the conduction loop. The impedance network in these

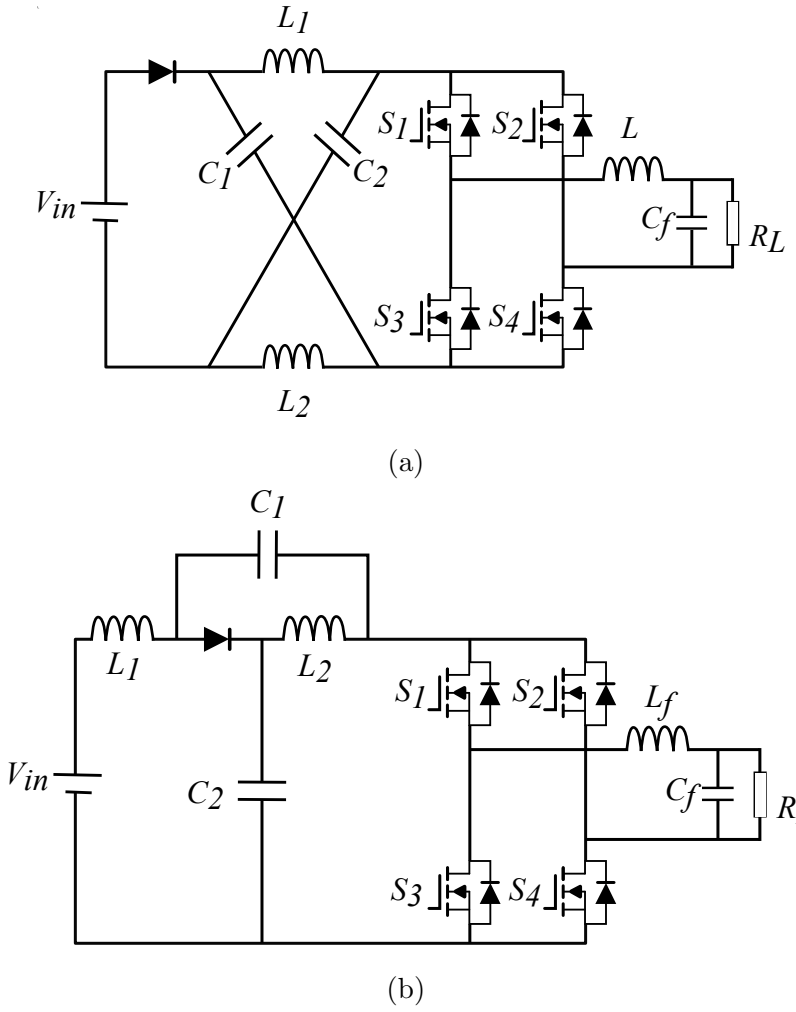


Figure 1.2: (a) Z-source Inverter [21], (b) Quasi-Z-source Inverter [22].

inverters requires additional components, such as inductors and capacitors. While this design choice aims to enhance performance, it simultaneously contributes to increased complexity in the system. Additionally, it adds to the cost and size of the overall setup, [24]-[23].

1.1.2 Two-Mode Wide Input Range Inverters

This group of inverters has two modes of operation, which means it can function as a two-stage inverter for low input voltages and as a single-stage inverter for high voltages. Typically, when the input voltage is low, the converter activates the second stage of the circuit, which is a DC/DC converter used to boost the input voltage, [19]-[25].

As an example of two-mode converters, Fig. 1.3 illustrates the Grid-connected Inverter with an integrated partial DC-DC converter. This inverter combines the Hybrid Energy Routing Inverter Configuration (HERIC) with two additional semiconductor switches, namely S_7 and S_8. The integration of these extra switches allows the circuit to operate in two distinct modes: a three-level mode, single-stage, and a five-level mode, two-stage, [19].

In the three-level mode, when the output voltage from the photovoltaic (PV) array exceeds the peak grid voltage, switch S_7 is turned ON while switch S_8 remains OFF. This configuration enables the circuit to function as a HERIC inverter, utilizing switches S_1 to S_6. During this mode, the DC-DC converter, consisting of switches S_9, inductor L_{dc}, and diode D, remains deactivated. Thus, this setup results in a three-level mode of operation, similar to that of a traditional HERIC inverter [19].

However, if the output voltage from the PV array drops below the peak grid voltage, the DC-DC converter is activated. This activation allows power to be transferred from the PV array to the second DC-link capacitor, C_{dc_2}, in a way that the combined DC-link voltage ($V_{dc_1} + V_{dc_2}$) exceeds the peak grid voltage. This mode of operation enables the inverter to produce a five-level voltage output. The voltage across C_{dc_2}, denoted as V_{dc_2}, is utilized by the inverter only when the instantaneous grid voltage

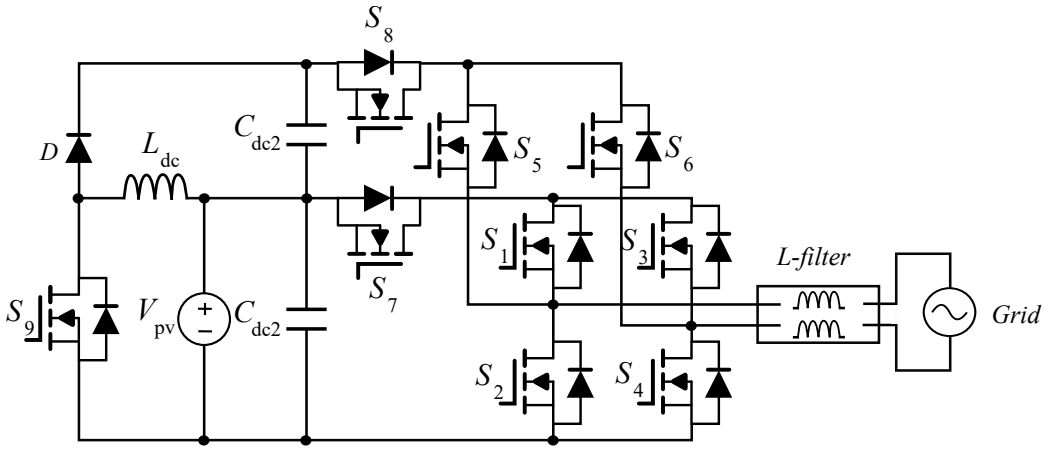


Figure 1.3: Grid-connected inverter with an integrated partial DC-DC converter [19].

is higher than the PV array voltage (V_{dc_1}), as depicted in Fig. 1.4 [19]. Using this configuration enables the converter to operate with PV voltages ranging from $200v$ to $420v$.

During periods when the instantaneous grid voltage is lower than the PV voltage (V_{dc_1}), power is directly sourced from the PV array without involving the DC-DC converter. Consequently, the DC-DC converter only processes a fraction of the total PV power. The majority of the power flows directly from the PV array to the inverter, resulting in higher efficiency even at low PV voltage levels, compared to the use of a cascade configuration involving a DC-DC boost converter and conventional inverters.

However, it should be noted that the inverter utilizes a modulation technique, as shown in Fig. 1.4, which synthesizes the voltage levels. This modulation technique leads to an increase in the rate of change of voltage (dv/dt) across the switches and imposes additional filter requirements. Moreover, operating all the switches at high frequency can result in high switching losses and reduce overall efficiency [26].

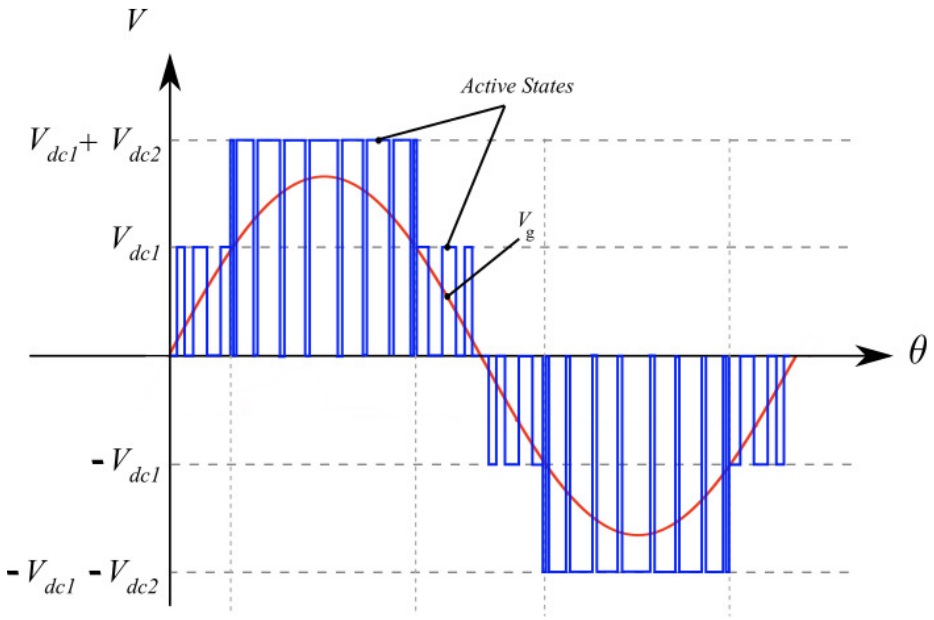


Figure 1.4: Working principle of the grid-connected inverter with an integrated partial DC-DC converter [19].

1.1.3 Single-Stage Wide Input Range Inverters

This type of inverter only employs a single stage to process all the power generated by the PV source and produce the necessary output voltage. These converters do not incorporate any DC/DC converters, and the inverter topology itself is designed to operate across a wide range of input voltages, [27]-[33].

One example of a single-stage inverter is proposed in [34], which is a differential inverter as shown in Fig. 1.5 that can operate across a wide range of input voltages and track the MPP of the PV systems. This converter utilizes a unique approach by deferentially connecting the load across two half-bridge dual-buck structure converters and modulating the output voltages of these converters.

To ensure the generation of the required output voltage, each converter produces

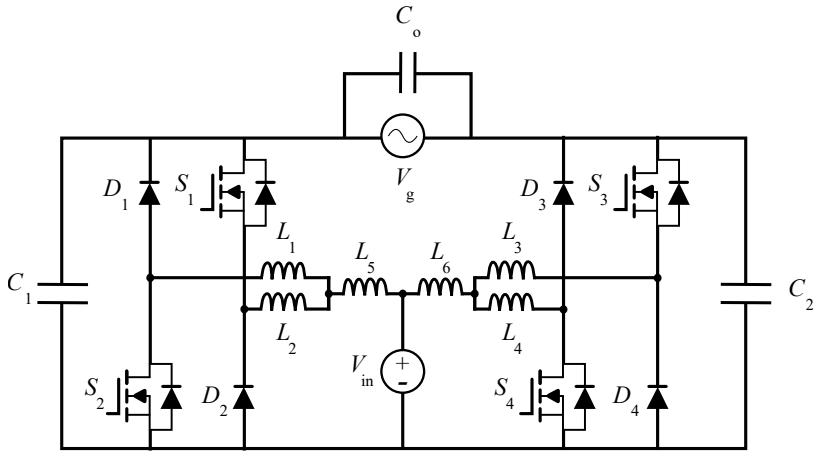


Figure 1.5: Dual-Buck-Structured Single-Stage Buck-Boost Inverters [34].

a DC-biased sine wave output, as depicted in Fig. 1.6. Despite the presence of a DC bias at both ends of the load in relation to the ground, the differential DC voltage across the load effectively remains zero. This modulation technique contributes to maintaining a balanced and stable load operation while achieving the desired output voltage.

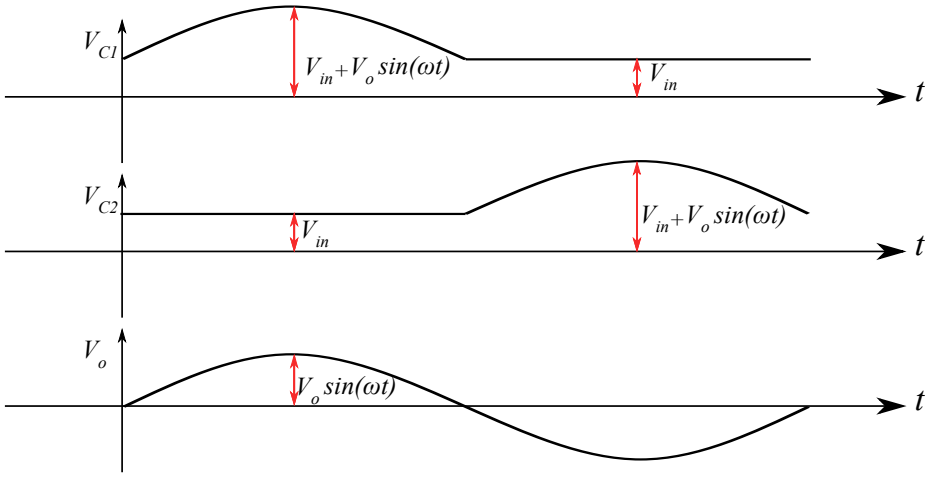


Figure 1.6: Voltage across the capacitors of the differential inverter proposed in [34].

This topology exhibits minimal distortion in output AC waveform due to either no or minimal dead-time requirements in the switching signals. Furthermore, current stress is reduced by half in comparison to other existing differential converters, enhancing the converter's overall reliability [34]. However, this inverter once again necessitates a significant number of passive components, and all switches operate at high frequency and voltage. As a result, the converter becomes bulky and expensive. Additionally, this topology features a larger magnetic volume compared to other alternatives [35] & [36]-[39]. Moreover, the high number of passive components and switches limit the converter's voltage range of operation to $70v$ to $200v$.

Another example of a single-stage converter is the tapped-inductor unfolding buck-boost inverter proposed in [40]. The circuit configuration of this wide input range inverter is shown in Fig. 1.7. This converter can operate in either buck or boost mode to generate the desired output voltage based on the maximum power point (MPP) voltage of the PV system. In buck mode, S_4 is always on, S_3 is always off, and S_1 and S_2 switch at high frequency. In boost mode, S_1 is always on, S_2 is always off, and S_3 and S_4 switch at high frequency. In both scenarios, switches S_5 to S_8 contribute to the unfolding process.

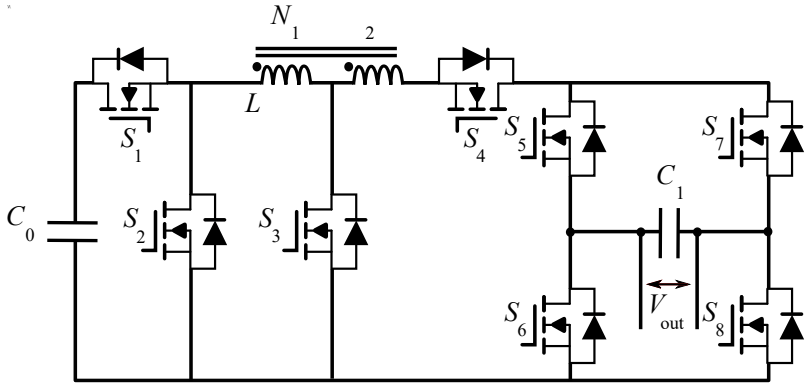


Figure 1.7: Single-Stage Buck-Boost Inverters [40].

The primary advantage of this topology is the reduced size of passive elements, achieved through the implementation of the unfolding stage and the elimination of the dc-link stage. This allows the converter to operate for PV voltage range from $250V$ to $450V$. However, the high number of required switches could outweigh the benefits gained from the reduction in passive component sizes [41], [6].

1.2 Objective

The primary objective of this thesis is to propose an inverter for a PV system that can track the system's maximum power point when the PV voltage changes in a wide range due to temperature or shading effects. Various configurations are being investigated, and control schemes that address the specific requirements of each topology are provided. In summary, the main objectives of this thesis are:

1. To propose a new inverter with a wide input voltage range that can function across various input voltages and interface with the grid. Two novel hybrid cascaded topologies with wide input voltage ranges are proposed to leverage the simplicity of the cascaded structure, allowing for multi-level output voltage and reduced harmonics, while also enabling operation across different PV voltages. The system's controller is implemented in the DQ frame to capitalize on the benefits of well-established three-phase DQ controllers designed for single-phase inverters.

2. To enhance the input voltage range of the inverter, a new two-mode structure is proposed. To expand the range of hybrid cascaded topologies further, a fly-back configuration at a fraction of the output power is incorporated. This allows the processing of a portion of the power when the voltage of the PV drops and

prevents the generation of the output voltage. Additionally, a DQ controller is implemented for this topology, making use of the well-developed three-phase DQ control techniques.

3. To enhance the inverter's performance, a new control method is implemented to achieve a wide range of input voltage with a reduced number of components. A novel control approach is introduced for the cascaded full-bridge converter, enabling independent control of the active power for each full bridge. With this control scheme, the system can operate within an input voltage range as broad as that of a fly-back-assisted inverter, while also reducing the overall component count.

4. To reduce the number of passive components that will be used in a wide input voltage range converter. This thesis proposes four topologies that utilize active filtering and do not require stored energy to generate the desired output voltage. As a result, these topologies lead to a lower number of passive component requirements.

5. To further improve the efficiency by utilizing a converter with low frequency and high voltage switches to generate the fundamental harmonic, and another inverter with high switching freq and low voltage stress to generate the high freq components. This approach can reduce overall system losses and increase efficiency.

1.3 Thesis Outline

Chapter 2 of this thesis will propose two new structures for wide input voltage range inverters. The first one is the full bridge inverter with an auxiliary floating capacitor,

which utilizes two cascaded full bridges. The first full bridge is connected to the PV source and will operate at a low frequency, tasked with generating the fundamental component of the output voltage. On the other hand, the second full bridge will operate at a high frequency and is responsible for mitigating the harmonics produced by the first full bridge. To enhance the efficiency of the second full bridge, the blocking voltage of the switches is limited to around sixty percent of the PV voltage. By employing these low-voltage switches, the efficiency of the lower full bridge can be maintained at a high level. Furthermore, the DQ current controller for this single-phase inverter is employed to regulate the power from the PV source. The second converter proposed in this chapter is the T-type inverter with an auxiliary floating capacitor. In this converter, the T-type topology replaces the full bridge inverter to interface with the PV source. Once again, the T-type inverter will operate at a low switching frequency, tasked with generating the fundamental component of the output voltage. The full bridge connected to the capacitor in this configuration is responsible for canceling out the harmonics. This full bridge also operates at a high frequency, but the blocking voltage of the switches is reduced to around thirty percent, which is half of that used in the first converter. This voltage reduction further improves the efficiency and allows for the use of smaller switches, resulting in an increase in the power density of the converter.

In Chapter 3, a fly-back-assisted wide input range inverter is proposed. This inverter utilizes two cascaded full-bridge inverters and a fly-back converter in its structure. The first full bridge inverter is connected to the PV source, while the second full bridge is connected to a capacitor. The PV source and the capacitor are interconnected through the fly-back converter. This structure enables an extended operating voltage range for the converter, allowing it to operate effectively at lower voltages. This enhancement is primarily attributed to the presence of the fly-back converter, which can handle up to 25% of the output power based on the source volt-

age. Moreover, the fly-back converter will deactivate when the PV voltage reaches a level sufficient for generating the desired output voltage. This feature effectively reduces unnecessary switching losses associated with the fly-back converter. Additionally, a controller is proposed for calculating the modulation angle of the primary full-bridge connected to the PV system. Furthermore, a DQ current controller is implemented to ensure that the converter can accurately track the MPP of the PV system.

To preserve the voltage range of the fly-back-assisted converter while minimizing the component count, Chapter 4 introduces a cascaded full-bridge converter with a single switching frequency. This configuration incorporates two cascaded full bridges operating at a high frequency and utilizes a novel control approach to enable independent power control of each full bridge. This controller structure ensures that the voltage range remains as wide as that of the fly-back-assisted converter. Importantly, the fly back component is eliminated from the topology, resulting in an enhanced power density of the configuration.

Finally, the thesis is concluded in Chapter 5, and suggestions for the future work of this research are presented.

Chapter 2

Hybrid Cascaded Extended Input Voltage Range Inverters

In this chapter, two new grid-connected inverters designed to operate within a wide range of input DC link voltages are introduced. These inverters offer a significant advantage by allowing operation over a broad range of PV voltages, eliminating the need for a separate DC/DC converter to accommodate low output voltages from PV systems. By eliminating the DC/DC converter, a single-stage converter is achieved, resulting in higher power density and efficiency.

Furthermore, the converters presented in this chapter can achieve higher efficiency compared to existing single-stage inverters. This is mainly due to the reduction in the switching frequency of the main converter, which is switched at the grid frequency, resulting in lower switching losses. Additionally, the required blocking voltage of the switches in the second part of the converter is reduced, further reducing switching losses despite the high switching frequency.

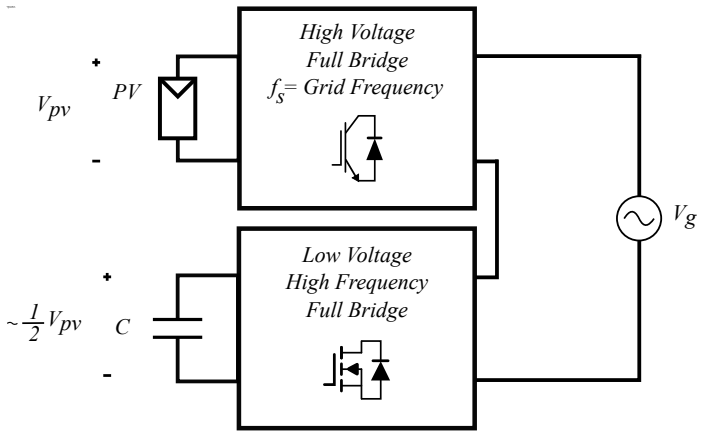


Figure 2.1: Block diagram of the proposed extended input voltage range inverters

Fig. 2.1 provides a visual representation of the block diagram of the inverters proposed in this chapter. As shown, these inverters consist of two essential parts: a low-frequency high-voltage section that connects to the PV system and allows the DC bus voltage to vary, enabling maximum power point (MPP) tracking. The second block is a high-frequency low-voltage section connected to the capacitor, responsible for generating harmonics that cancel out the harmonics produced by the first block. The combination of these two parts enables the inverters to handle varying voltage levels while maintaining optimal performance and efficiency.

By eliminating the need for a separate DC/DC converter, the proposed inverters simplify the overall design, reduce the number of components, enhance system reliability, and lower costs. Furthermore, the reduced switching frequency and blocking voltage of the switches increase the efficiency of the inverter, allowing the system to track the MPP while maintaining high efficiency and eliminating harmonics.

This chapter will discuss the details of each converter's topology and propose appropriate control approaches for each inverter. Additionally, it will discuss the

advantages of each topology in comparison to existing ones in more detail.

2.1 Full Bridge Cascaded Inverter Basic principle of operation

The first converter that will be discussed in this chapter is the full bridge converter cascaded with a high-frequency bridge with a floating input capacitor. The circuit configuration of the proposed extended input voltage range inverter is illustrated in Fig. 2.2. The upper full bridge in this circuit consists of four high-voltage, low-frequency switches that operate at the fundamental frequency. This part of the inverter plays a crucial role in providing the active power generated by the PV system and transferring it to the grid system. To maximize the extracted power from the PV system, this part of the inverter can operate over a wide range of DC link voltages to track the Maximum Power Point (MPP) of the PV system. Additionally, due to the low frequency of these switches, they exhibit minimal losses, contributing to the overall higher efficiency of the inverter while allowing the voltage of the DC bus to swing.

Although using the low-frequency full bridge can considerably improve efficiency, it also produces a significant amount of harmonics at its output that needs to be eliminated. Traditionally, this was achieved by employing an output filter. However, in this inverter, as shown in Fig. 2.2, a second full bridge is connected to the capacitor, which has the task of generating harmonics to cancel out the harmonics generated by the first full bridge.

Since the second full bridge is solely responsible for generating the harmonic voltage, it only generates reactive power and does not need to generate active power.

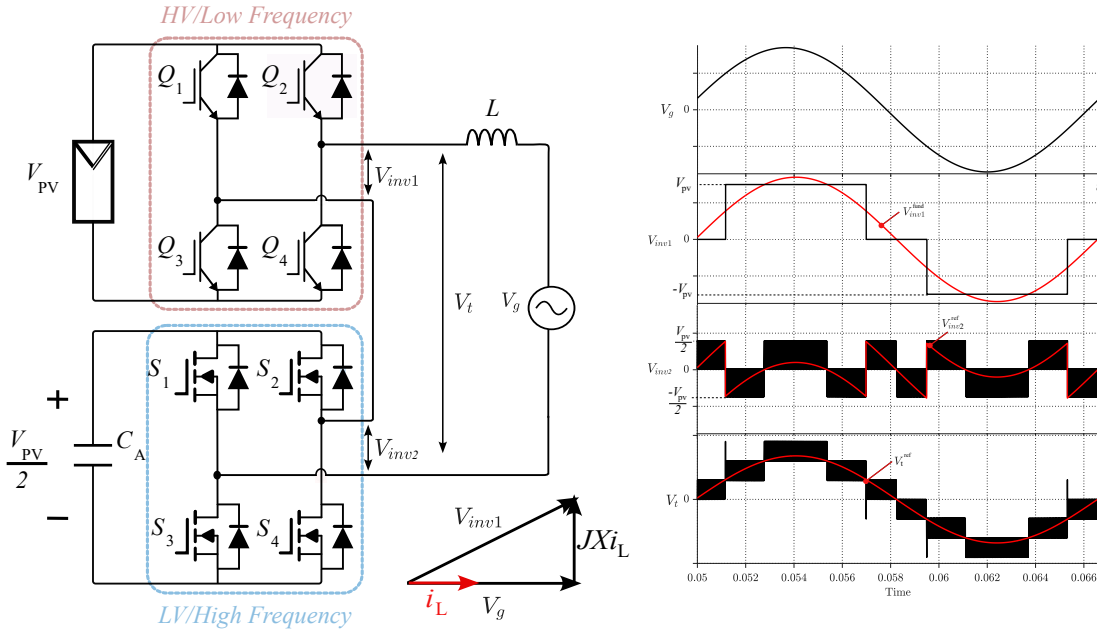


Figure 2.2: Proposed extended input voltage range inverter and important waveform of the converter

Therefore, there is no need to connect the second full bridge to the power source, and the system can operate solely using the capacitor. Unlike the full bridge connected to the PV system, the second full-bridge operates at a high frequency. However, the switches in the second full bridge exhibit relatively low losses despite their higher switching frequency. This is primarily attributed to their connection to a lower voltage level, which is approximately half of the PV system voltage. By operating at this reduced voltage level, the switching losses can be minimized, and the overall efficiency of the inverter is improved.

To achieve optimal performance, the voltage of the capacitor connected to the lower full bridge should be regulated at the reference voltage, which is determined based on the voltage of the PV system. Therefore, the controller of the inverter must calculate the appropriate reference voltage for the capacitor based on the PV system

voltage and ensure that the capacitor voltage is set to the reference value.

Since the first full bridge requires high-voltage, low-switching-frequency switches, four IGBT switches can be used for this converter. On the other hand, since the lower full bridge requires low-voltage, high-frequency switches, four MOSFETs can be used for this full bridge. The utilization of both IGBT and MOSFET switches in the proposed inverter circuit configuration allows for efficient power conversion and transmission. The low-frequency IGBT switches reduce losses during fundamental frequency switching, while the higher-frequency MOSFET switches accommodate rapid switching demands without significantly impacting efficiency. Most importantly, this hybrid configuration capitalizes on the strengths of each switch type, enabling the inverter to operate optimally across a wide input voltage range. Appendix A will provide an in-depth explanation for using the IGBT instead of the MOSFET in the main full bridge.

2.2 Operation and Control of the Proposed Converter

In order for the system to operate effectively, it requires a controller that can generate the appropriate references for each full bridge converter. The controller block diagram of the system is depicted in Fig. 2.3.

This controller comprises Four main components: the α generator, the reference generator for the second full bridge to eliminate the harmonics, the capacitor voltage regulator, and the current controller. The first part is responsible for controlling the modulation angle of the upper full bridge, which enables control over the fundamental voltage. Its primary function is to ensure the desired voltage level generated at the

output of the inverter as described in the phase diagram of Fig. 2.1.

The second part of the controller is tasked with generating the voltage reference for the second full bridge in a manner that eliminates the harmonics generated by the first full bridge. By carefully calculating the appropriate reference voltage, it aims to cancel out any unwanted harmonic components generated by the first full bridge. The details of these controllers will be discussed in the following sections.

Since the second full bridge is not directly connected to the power source, it is necessary to regulate the voltage across the capacitor to a desired value. To achieve this objective, the third part of the controller plays a crucial role in generating slight deviations in the reference for the second full bridge. These deviations help maintain the capacitor voltage at the desired level, ensuring stability and proper operation of the system. The details of each part of the controller will be further discussed in the following sections.

Finally, the last section of the controller has the responsibility of controlling the current of the converter while ensuring that the voltage of the PV will be set at the reference value determined by the MPPT block. The output of this controller will be V_t, which will be the value used to determine α. The details of each part of the controller will be discussed in more detail in the following sections.

2.2.1 Reference Generation for the Full Bridge with Floating Capacitor

Before explaining how to calculate the modulation angle (α) of the main full bridge, it is important to understand the operation and reference generation for the second full bridge. As mentioned previously, the second full-bridge generates harmonics to

cancel out the harmonics produced by the main full bridge. Therefore, the reference voltage for the second full bridge is the difference between the total voltage (V_t) and the voltage of the main inverter:

$$h_{inv2} = V_t - V_{inv1} \tag{2.1}$$

Since the voltage of the first full-bridge is a three-level waveform and the total voltage is sinusoidal, the reference voltage of the second full bridge takes a shape similar to the one shown in Fig. 2.4.

To improve efficiency, the operating voltage of the lower full bridge, which operates at high frequency, should be reduced. The blocking voltage of the lower switches depends on the voltage of the capacitor, which should be higher than the maximum of the reference voltage shown in Fig. 2.4. This is done to avoid over-modulation and the generation of unwanted harmonics. Therefore, based on this information, the α value should be calculated in a way that results in the minimum voltage across the capacitor. This will be discussed in more detail in the following section.

2.2.2 Calculation of Switching Angle

The first full bridge is responsible for generating the fundamental output waveform of the inverter. This full bridge operates at the grid frequency and produces a three-level voltage waveform at its output port, as depicted in Fig. 2.5. The fundamental waveform of this output can be expressed as a function of the switching angle (α). To determine the fundamental component of this waveform, the Fourier series can be written as follows:

$$a_1 = \frac{1}{\pi}\int_0^{2\pi} v_{out_1}\cos(\theta)d\theta \tag{2.2}$$

$$b_1 = \frac{1}{2}\int_0^{2\pi} v_{out_1}\sin(\theta)d\theta \tag{2.3}$$

calculating these equations leads to the determination of the following coefficients:

$$a_1 = 0 \tag{2.4}$$

$$b_1 = \frac{4v_{pv}}{\pi}\cos(\alpha) \tag{2.5}$$

based on these calculations, the equation for the fundamental voltage of the three-level waveform with a switching angle of α is given by:

$$v_1(t) = b_1 \sin(\omega t) = \frac{4v_{pv}}{\pi}\cos(\alpha)\sin(\omega t) \tag{2.6}$$

The optimal switching angle is the one that minimizes the peak of the reference voltage of the second full bridge. By minimizing the peak voltage, the required capacitance can be reduced, resulting in a decrease in the required blocking voltage of the switches. This optimization allows the converter to operate more efficiently.

The waveform of the reference voltage for the second full bridge is depicted in Fig. 2.4. As observed, the peak of this waveform occurs at the switching angle. To minimize this value, the fundamental component of the three-level waveform should have a value of $v_{pv}/2$ at the switching angle:

$$\frac{4v_{pv}}{\pi}\cos(\alpha)\sin(\alpha) = \frac{v_{pv}}{2} \tag{2.7}$$

Solving this equation will result in the following switching angle:

$$\alpha = 25.88 \tag{2.8}$$

Since the fundamental voltage of the converter is generated by the upper full bridge, the peak of this signal must be equal to the peak of the calculated total voltage V_t. The peak of the fundamental voltage of the converter can be expressed as follows:

$$V_{inv1}^{fund} = \frac{4}{\pi}v_{\rho v}\cos(\alpha)\sin(\omega t) \xrightarrow{\omega t=\frac{\pi}{2}} V_{inv1_{peak}}^{fund} = \frac{4}{\pi}v_{\rho v}\cos(\alpha) \tag{2.9}$$

The peak of the fundamental voltage has two parameters: the switching angle and the voltage of the upper full bridge. The optimal value of the switching angle has already been chosen to minimize the blocking voltage of the lower switches, thereby increasing efficiency. Now, the optimal value of the upper full bridge voltage can be determined by equating the peak of the grid voltage and the fundamental voltage as follows:

$$\frac{4}{\pi} v_{\rho v} \cos(\alpha) = V_t \Rightarrow v_{\rho v} = \frac{\pi V_t}{4\cos(\alpha)} \tag{2.10}$$

If the peak of the total voltage is considered 340, the optimal voltage of the upper inverter should be 296. However, the main objective of the inverter is to operate within a wide range of input voltages. To achieve this goal, the voltage of the upper inverter will be allowed to swing around the optimum point. Consequently, an appropriate switching angle can be determined by utilizing (2.13).

To find the range of the voltage swing of the upper full bridge, it should be considered that the blocking voltage of the lower full bridge is desired to be around half of the upper full bridge. This is done to limit the losses. Additionally, the blocking voltage of the switches is equal to the required voltage of the capacitor, which can be calculated using the following equation:

$$V_c = Max\{v_{pv} - f_1(\alpha), f_1(\alpha)\} \tag{2.11}$$

$$V_{inv1}^{fund}(\alpha) = \frac{4v_{pv}}{\pi} \cos(\alpha)\sin(\alpha) \tag{2.12}$$

Equation (2.11) has two parameters, α and v_{pv}, but the switching angle itself is a function of v_{pv}. Using equation (2.10), it can be written as follows:

$$\alpha = \cos^{-1}(\frac{\pi V_t}{4v_{\rho v}}) \tag{2.13}$$

Fig. 2.6 illustrates the relationship between the value of α and v_{pv}. Once α is determined based on v_{pv}, equations (2.11)-(2.13) can be combined, resulting in the ratio

V_c/v_{pv} based on v_{pv}, as depicted in Fig. 2.7.

To ensure high efficiency and minimize the blocking voltage of the lower full bridge switches, the V_c/v_{pv} ratio is maintained at around 64%. Therefore, the lower voltage of v_{pv} should be set to 280. Beyond this value, the blocking voltage of the lower switches would increase dramatically. Conversely, as v_{pv} increases, the V_c/v_{pv} ratio will decrease. However, a limit of 500 is chosen for v_{pv} since, even though the V_c/v_{pv} ratio decreases, the blocking voltage of the lower full bridge needs to remain high enough to support the system's operation at that v_{pv}.

Consequently, this system can operate within the range of 280 to 500 times the value of v_{pv} while maintaining high efficiency. The upper full bridge generates the fundamental voltage using low-frequency switching with high efficiency, while the lower full bridge utilizes low-voltage, high-frequency switches to maintain efficiency.

2.2.3 Current Controller

The primary objective of the current controller is to regulate the current of the converter so that it can set the voltage of the PV source at the desired reference determined by the MPPT, thus enabling it to generate the maximum power. Additionally, the current controller is responsible for controlling the reactive power of the system in a grid-connected setup.

There are two commonly used methods for controlling the reactive power and voltage of the PV source, which in turn enables the control of active power in grid-connected systems. The first method is known as voltage-mode control. This approach involves adjusting the phase angle and amplitude of the converter's AC-side terminal voltage in relation to the grid voltage to regulate the real and reactive power.

By closely matching the amplitude and phase angle of the converter voltage with the grid voltage, independent control of real and reactive power can be achieved. However, voltage-mode control lacks a closed-loop control on the converter line current, which can make the converter susceptible to over-current conditions. Rapid changes in power commands or AC system faults can lead to significant current fluctuations.

To address the limitations of voltage-mode control, the second method, known as current-mode control, is often employed. In current-mode control, a dedicated current-control scheme is used to tightly regulate the converter line current through the converter's AC-side terminal voltage. By adjusting the phase angle and amplitude of the converter line current in relation to the grid voltage, real and reactive power can be controlled effectively. Current-mode control offers several advantages, including protection against over-current conditions, robustness against parameter variations in the converter and AC system, superior dynamic performance, and higher control precision.

Given these advantages, the proposed converter implements control using current-mode control in the dq-frame. However, due to the converter being single-phase, an orthogonal signal generation (OSG) block is necessary to generate the orthogonal component of the grid current in the $\alpha\beta$ frame.

OSG Block

DQ frame current controllers were originally introduced for three-phase systems and later extended to single-phase applications. These controllers utilize the $\alpha\beta$/DQ transformation to convert alternating current variables into equivalent direct current quantities, enabling them to be controlled by PI controllers. The design process for PI controllers is straightforward, and they demonstrate satisfactory performance in

terms of dynamics and steady-state behavior. Furthermore, since the system variables are transformed into DC quantities, the control loop is not influenced by the system frequency. Moreover, this approach allows independent regulation of the voltage of the PV and reactive power through simple adjustments of the D-axis and Q-axis currents, respectively.

In single-phase inverter systems, DQ current control requires the generation of orthogonal signals through an orthogonal signal generation (OSG) block in the $\alpha\beta$ frame. Traditionally, OSG has been implemented using phase shift methods such as Hilbert transform, time delay, all-pass filter, and second-order generalized integrator (SOGI). While these methods generally offer acceptable steady-state performance, the time delay required to achieve a 90° phase shift slows down the system's dynamic response, which can be problematic in smart inverters. Furthermore, frequency drifts can lead to inaccurate phase shifts, resulting in unacceptable errors in active and reactive power control.

To address these issues and achieve a more robust system, this thesis implements an OSG method based on [42]. This OSG approach ensures that the controller remains independent of the system parameters and operating frequency. Additionally, the method is instantaneous, introducing no additional delay or distortion to the control process.

The desired β component is generated by first assuming the grid current as given in equation (2.14). The 90° delayed version of this current, denoted by equation (2.15), can be expressed as follows:

$$i_{g\alpha} = A\sin(\theta + \varphi) \tag{2.14}$$

$$i_{g\beta} = -A\cos(\theta + \varphi) \tag{2.15}$$

here, θ is defined as the integral of ω with respect to time, as shown in equation (2.16). In equations (2.14)-(2.16), ω and θ represent the angular frequency and phase angle of the grid voltage, respectively, while φ denotes the phase angle between the grid voltage and current.

$$\theta = \int_0^t \omega(\tau) d\tau \tag{2.16}$$

The reference values of the D- and Q-axes currents, denoted as I_d^* and I_q^*, respectively, correspond to the α-axis reference current $i_{g\alpha}^*$ given by:

$$i_{g\alpha}^* = B \sin(\psi + \gamma) \tag{2.17}$$

In the above equation, ψ is the angle of the $\alpha\beta/DQ$ transformation, and B and γ are defined as follows:

$$B = \sqrt{I_d^{*2} + I_q^{*2}}, \quad \gamma = \tan^{-1}\left(\frac{I_q^*}{I_d^*}\right) \tag{2.18}$$

The objective is to estimate the actual $i_{g\beta}$. When the phase-locked loop (PLL) operates in a steady state, ψ is equal to θ. Additionally, due to the selection of PI controllers, which eliminate the steady-state error of the current controller, $i_{g\alpha}$ eventually converges to $i_{g\alpha}^*$. Similarly, if the β-axis component of the grid current were to exist, it would also converge to $i_{g\beta}^*$. Therefore, the β-axis component can be estimated based on the reference values of the D- and Q-axes currents. Consequently, the proposed method utilizes the values of I_d^* and I_q^* to generate an estimation of $i_{g\beta}$, denoted as $\hat{i}_{g\beta}$, given by equation (2.19). Fig. 2.8 illustrates the block diagram of this method.

$$\hat{i}_{g\beta} = -B \cos(\psi + \gamma) \tag{2.19}$$

Design of Current Control

The DQ current controller's diagram is depicted in Fig. 2.9. In this controller, the reference value for the D component (i_{dref}) will be generated by a PI controller, with its input being the difference between the reference voltage of the PV system and the measured voltage of the PV system. The reference voltage of the PV system is determined by the Maximum Power Point Tracking (MPPT) algorithm. The primary goal of i_{dref} is to ensure that the voltage of the PV system is set to the desired value and that the PV system generates the maximum power possible.

Furthermore, the reference value for the Q component of the current can be generated based on the desired reactive power values using the following equation:

$$i_{\text{qref}}(t) = -\frac{2}{3V_{sd}} Q_{\text{ref}}(t) \tag{2.20}$$

Moreover, considering a steady-state operating condition and substituting $\omega(t) = \omega_0$, the system equations in the DQ frame can be expressed as follows:

$$L\frac{di_d}{dt} = L\omega_0 i_q - Ri_d + V_{td} - V_{sd} \tag{2.21}$$

$$L\frac{di_q}{dt} = -L\omega_0 i_d - Ri_q + V_{tq} - V_{sq} \tag{2.22}$$

However, the presence of $L\omega_0$ terms in equations (2.21) and (2.22) causes the dynamics of i_d and i_q to be coupled. To decouple their dynamics, m_d and m_q are defined as follows:

$$m_d = \frac{2}{V_{DC}} \left(u_d - L\omega_0 i_q + V_{sd}\right) \tag{2.23}$$

$$m_q = \frac{2}{V_{DC}} \left(u_q + L\omega_0 i_d + V_{sq}\right) \tag{2.24}$$

By substituting m_d and m_q from equations (2.23) and (2.24) into equations (2.21)

and (2.22), the following equations can be obtained:

$$L\frac{di_d}{dt} = -Ri_d + u_d \tag{2.25}$$

$$L\frac{di_q}{dt} = -Ri_q + u_q \tag{2.26}$$

Equations (2.25) and (2.26) describe two decoupled first-order linear systems. Based on these equations, i_d and i_q can be controlled by u_d and u_q, respectively. Using these equations, and since in the current control system, all the control, feed-forward, and feedback signals are DC quantities in the steady state, the current control block diagram can be simplified as shown in Fig. 2.10.

Fig. 2.10 shows that the control plants in both the d- and q-axis current control loops are identical. Hence, the corresponding compensates can also be identical. For the d-axis control loop, $k_d(s)$ can be a simple proportional-integral (PI) compensation to track a DC reference command:

$$k_d(s) = \frac{k_p s + k_i}{s} \tag{2.27}$$

where k_p and k_i are the proportional and integral gains, respectively. Thus, the loop gain becomes:

$$\ell(s) = \left(\frac{k_p}{Ls}\right)\frac{s + \frac{k_i}{k_p}}{s + \frac{R}{L}} \tag{2.28}$$

Since the plant pole at $s = -\frac{R}{L}$ is close to the origin, the magnitude and phase of the loop gain start to drop from a relatively low frequency. Therefore, the compensates zero at $s = -\frac{k_i}{k_p}$ cancels out the plant pole, resulting in the simplified loop gain $\ell(s) = \frac{k_p}{Ls}$. Consequently, the closed-loop transfer function, $\frac{\ell(s)}{1+\ell(s)}$, can be expressed as:

$$\frac{I_d(s)}{I_{\text{dref}}(s)} = G_i(s) = \frac{1}{\tau_i s + 1} \tag{2.29}$$

provided that:

$$k_p = \frac{L}{\tau_i} \tag{2.30}$$

$$k_i = \frac{R}{\tau_i} \tag{2.31}$$

Here, τ_i represents the time constant of the resultant closed-loop system. Equation (2.29) reveals that by selecting k_p and k_i according to equations (2.30) and (2.31), the response of $i_d(t)$ follows a first-order transfer function with a time constant τ_i as a design choice. To achieve a fast current control response, τ_i should be small, yet sufficiently large such that $\frac{1}{\tau_i}$ (the bandwidth of the closed-loop control system) is considerably smaller than the switching frequency of the converter. The same compensate as $k_d(s)$ can also be used for the q-axis compensate ($k_q(s)$).

The output of the current controller, as shown in Fig. 2.9, is V_d and V_q. These values can be transformed into stationary waveforms, and the generated reference is the voltage that the converter is required to produce at the terminals connected to the grid and inductance. This voltage is called the total voltage (V_t) in this thesis and can be calculated using the following equation. In this equation, ω and φ are determined by the PLL connected to the voltage of the grid.

$$V_t = V_d \sin(\omega t + \varphi) + V_q \cos(\omega t + \varphi) \tag{2.32}$$

2.2.4 Capacitor Voltage Regulator

The voltage regulator for the capacitor is a crucial component of the inverter system. Equations (2.11)-(2.13) demonstrate that the capacitor voltage should be adjusted according to the voltage of the upper full bridge. Fig. 2.11 provides a visual representation of how the capacitor voltage should be controlled in relation to the voltage of the upper full bridge.

To achieve this control, an appropriate controller must calculate the reference voltage for the capacitor and regulate it to the desired value. As mentioned earlier, the capacitor voltage should ideally match the maximum of the waveform shown in Fig.2.4. This maximum occurs at the point α. Based on this observation, the reference voltage can be calculated using equation (2.33), and its corresponding block diagram is illustrated in Fig.2.12.

$$V_{cref} = \max\left\{V_{P_v} - V_g \sin\left(\cos^{-1}\left(\frac{\pi v_g}{4v_{pv}}\right)\right), V_g \sin\left(\cos^{-1}\left(\frac{\pi v_g}{4v_{pv}}\right)\right)\right\} \tag{2.33}$$

After determining the reference voltage for the capacitor, the controller must effectively maintain the voltage at this specified value. To regulate the DC link voltage of the full bridge, the controller controls the active power flowing through the full bridge. By injecting active power into the capacitor, its voltage increases, and vice versa, by extracting active power from the capacitor, its voltage decreases.

To control the active power, the lower full bridge must generate the fundamental voltage at its output. For this purpose, a feedback mechanism is necessary. This mechanism compares the actual DC bus voltage with the reference command. Then, a PI controller determines the desired magnitude of the fundamental voltage required to control the active power. To align the generated fundamental voltage of the lower full bridge with the current passing through it, the angle of V_t is determined based on the values V_d and V_q. This angle, along with the angular frequency of the grid, is used to generate a unity cosine waveform. Finally, the output of the PI controller adjusts the magnitude of this unity waveform, as shown in Fig. 2.13.

Ultimately, the generated reference voltage is added to the reference waveform resulting from the harmonic elimination control block. This resultant waveform is then used to modulate the switches of the lower full bridge, as shown in Fig. 2.3.

2.3 Simulation Results of Full Bridge Cascaded Inverter

This section presents the simulation results of the converter, demonstrating its performance and ability to generate the required output voltage across a wide range of input voltages. Additionally, the FFT of the waveform is displayed, demonstrating the low harmonics present in the output voltage and current.

The full bridge inverter cascaded with a high-frequency bridge with floating input capacitor is simulated for two different input voltages of the PV system and results are reported. The first simulation is done for a voltage of 400, which is the nominal voltage of the converter. Fig. 2.14 shows the waveform of the output voltage, current, and voltage of both full bridge outputs, as well as the voltage of the capacitor. As can be seen from the figure, the converter can generate the desired output voltage and current. Fig. 2.15 shows the harmonic content of these waveforms. This harmonic content indicates that the converter generates a low amount of harmonics, despite the low-frequency operation of the PV-connected full bridge. This is mainly due to the active harmonic elimination in this circuit.

Furthermore, the simulation results for an input voltage of 280 are also depicted in Fig. 2.16. This represents the lowest voltage at which the converter can operate. As evident from the figure, the converter was able to generate the desired output waveform and successfully maintained the capacitor voltage at the desired level.

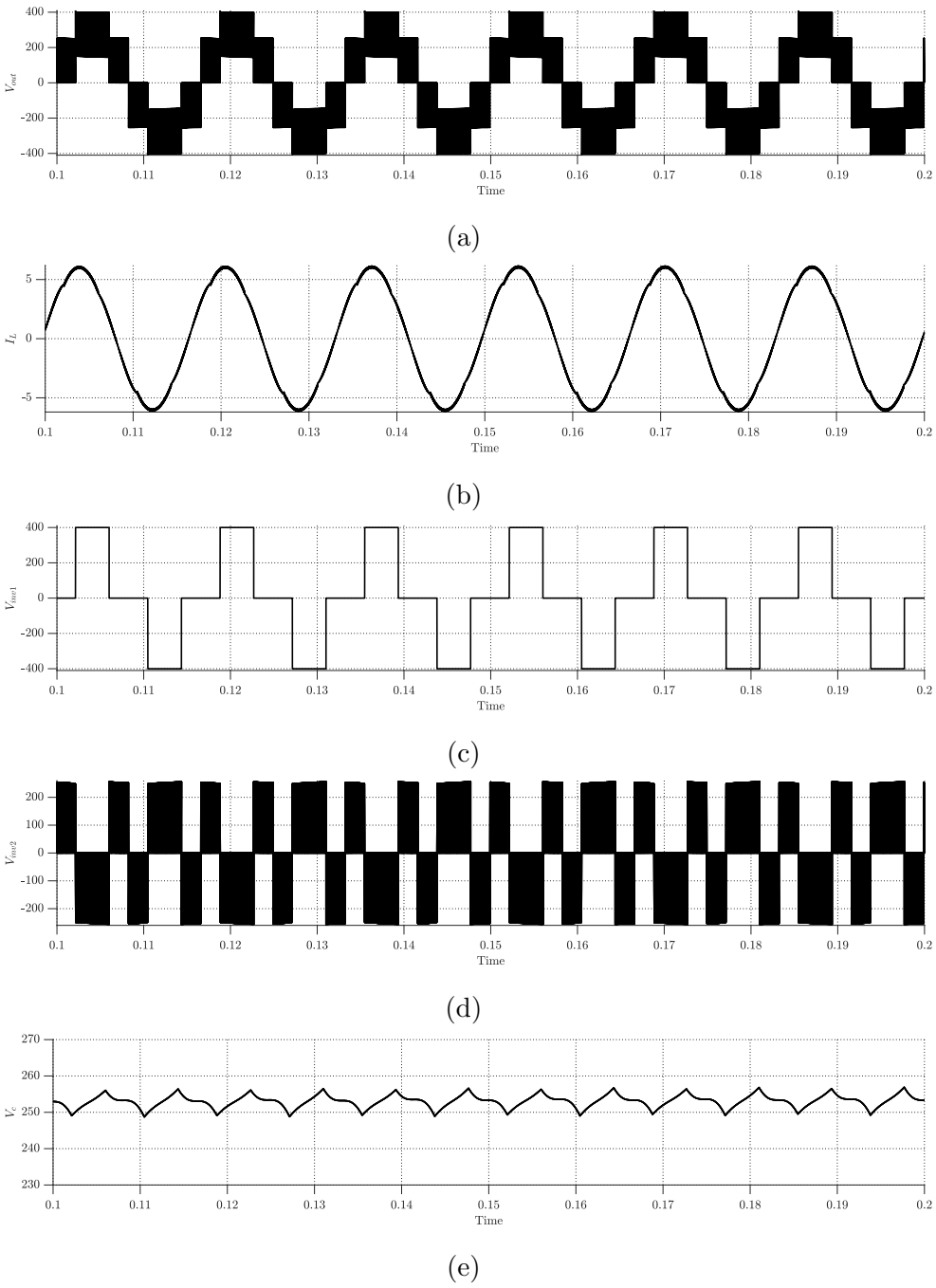


Figure 2.14: Waveform of Full Bridge Inverter Cascaded with a High-Frequency Bridge with Floating Input Capacitor ($V_{pv} = 400$): (a) Output voltage of inverter, (b) Output current, (c) Output voltage of main inverter, (d) Output voltage of capacitor connected inverter, (e) Voltage of capacitor.

Additionally, as illustrated in Fig. 2.17, the converter once again effectively eliminated the harmonics of the main full bridge by utilizing the capacitor-connected full bridge configuration. The circuit parameters for both simulations are identical and are presented in Table 2.1.

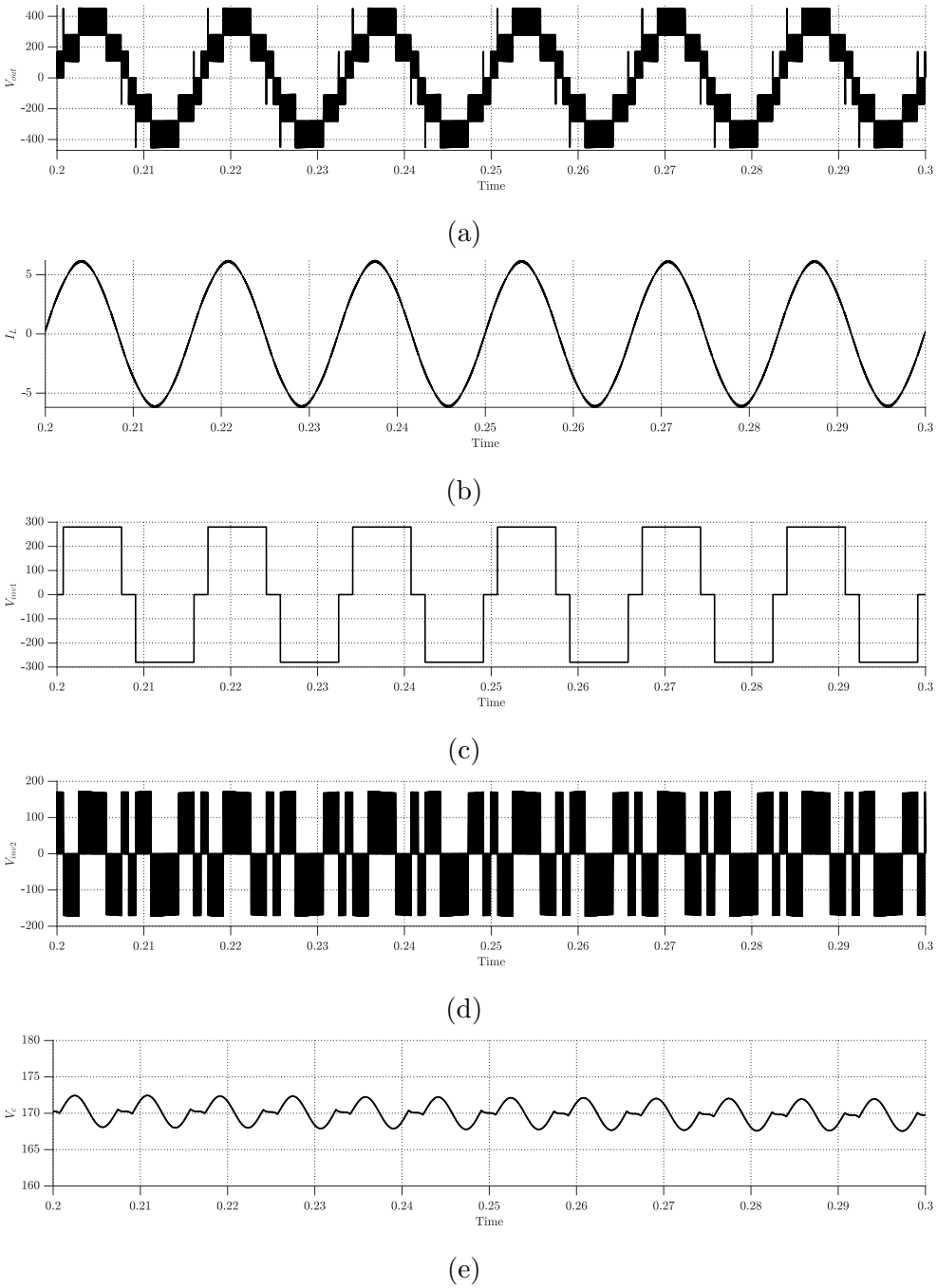
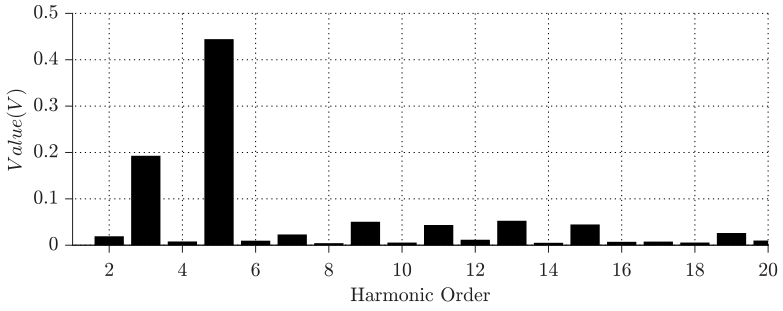


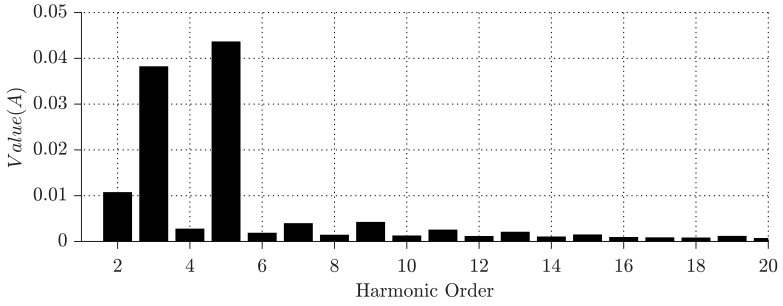
Figure 2.16: Waveform of Full Bridge Inverter Cascaded with a High-Frequency Bridge with Floating Input Capacitor ($V_{pv} = 280$): (a) Output voltage of inverter, (b) Output current, (c) Output voltage of main inverter, (d) Output voltage of capacitor connected inverter, (e) Voltage of capacitor.

Table 2.1: System parameters of the full bridge inverter cascaded with a high-frequency bridge with floating input capacitor.

	Parameter	Value
Input voltage	V_{in}	280-500v
Grid voltage	V_g	240v
Filter inductance	L	5mH
Capacitance	C	1mF
Upper full bridge switching frequency	f_{s1}	60Hz
Lower full bridge switching frequency	f_{s2}	30kHz



(a)



(b)

Figure 2.17: Full bridge inverter cascaded with a high-frequency bridge with floating input capacitor ($V_{pv} = 280$): (a) Harmonic spectrum of the output voltage, (b) Harmonic spectrum of the output current.

These simulation results demonstrate the converter's robust performance across a wide range of input voltages, showcasing its capability in accommodating varying PV system conditions. When tested at its nominal voltage of 400, the converter consistently delivered the desired output voltage and current, while maintaining low harmonic content. Even at the lowest input voltage of 280, the converter continued to exhibit its ability to generate the required waveform and efficiently control the capacitor voltage. These outcomes affirm the effectiveness of the active harmonic elimination technique employed in this circuit design. The consistent performance and harmonic mitigation capabilities of this converter make it a promising choice for PV system applications, offering reliable operation under different voltage conditions.

2.4 T-type Inverter with Cascaded Floating Capacitor

In this section, the T-type converter with a cascaded floating capacitor is explored as the second type of extended input range converter. The circuit configuration of this inverter is depicted in Fig. 2.18. This circuit consists of an upper T-type converter with eight high-voltage, low-frequency switches. The upper T-type converter plays a crucial role in converting the active power generated by the PV system and seamlessly transferring it to the grid system.

However, the low-frequency T-type converter also generates harmonics at its output, which need to be eliminated. Similar to the previous inverter configuration, a full bridge is used to cancel out these harmonics, as shown in Fig. 2.18. This bridge is connected to the capacitor and effectively cancels out the harmonics generated by the T-type converter.

Although the full bridge operates at a high switching frequency, it demonstrates low losses due to its operation at a low voltage level. In this converter, the voltage of the capacitor, which determines the operating voltage of the switches, can be reduced to as low as one-fourth of the PV voltage. This reduction allows for the use of switches with lower blocking voltage and lower $R_{ds_{on}}$, further increasing efficiency. Operating at this reduced voltage effectively minimizes switching losses, resulting in an overall enhancement in inverter efficiency. Furthermore, this converter generates an output waveform with a higher number of voltage levels, which results in a smaller inductor at the output, potentially leading to a more compact design compared to the full bridge.

Regarding switch selection, the T-type configuration requires high-voltage, low-switching-frequency switches, allowing it to utilize eight IGBT switches (Appendix A), while the full bridge calls for low-voltage, high-frequency switches and can make use of four MOSFETs.

2.5 Operation and Control of the T-type Inverter with Cascaded Floating Capacitor

The effective operation of the system relies on the presence of a well-designed controller that can generate the necessary references for both the T-type inverter and the full bridge converter. This controller is similar to the one proposed for the previously discussed topology and is composed of four key components: the α and β generator, the reference generator for the full bridge, the current controller, and the capacitor voltage regulator. Together, these components work harmoniously to ensure the optimal performance of the system.

To begin, the α and β generator within the controller plays a crucial role in controlling the modulation angle of the T-type converter. By precisely manipulating the modulation angle, this component enables control over the fundamental voltage, thus ensuring the desired voltage level at the output. Through its meticulous regulation of the modulation angle, the α and β generator guarantees that the system operates by the predefined total voltage (V_t) requirements.

Moving on to the reference generator for the full bridge, its primary objective is to eradicate any harmonics that may be generated by the T-type converter. This goal is achieved by determining the optimal reference voltage to cancel out any unwanted harmonic components produced by the T-type converter. This step is crucial in maintaining the quality of the output voltage and minimizing the presence of harmonics.

Similar to the previous converter, the current controller is necessary to ensure that the voltage of the PV system is set at the reference value determined by MPPT to extract the maximum available power from the PV source. Moreover, the current controller is required to control the reactive power of the converter. The output of the current controller will be the total voltage (V_t) which is the voltage that the inverter must produce at its output terminals connected to the grid and inductance.

Since the full bridge is not directly connected to the power source, it becomes necessary to employ a capacitor voltage regulator. This component takes on the responsibility of carefully regulating the voltage across the capacitor to a desired level. The capacitor voltage regulator is a vital component in maintaining the overall stability of the system and allowing it to function optimally.

2.5.1 Full Bridge Reference Calculation

The main objective of the full bridge configuration is to generate harmonics that counteract the harmonics produced by the T-type converter. By utilizing the full bridge, the unwanted harmonics can be effectively canceled out. To achieve this cancellation effect, the reference voltage for the full bridge is determined similar to the previous converter, by taking the inverse of the difference between the voltage of the main inverter and the total voltage (V_t).

The voltage produced by the T-type takes on a five-level waveform, while the total voltage follows a sinusoidal waveform. The shape of the reference voltage for the full bridge will be similar to the waveform shown in Fig. 2.19. As discussed in the previously proposed converter, to increase efficiency, it is desirable to use switches with high frequency and low voltage in the full bridge.

The blocking voltage of the lower switches is directly influenced by the voltage across the capacitor. It is essential to ensure that the capacitor voltage remains higher than the maximum value of the reference voltage depicted in Fig. 2.19 to prevent the occurrence of over-modulation and the generation of unwanted harmonics. To achieve the desired minimum voltage across the capacitor, the calculation of the switching angles (α and β) becomes crucial to result in the minimum desired capacitor voltage.

2.5.2 Switching Angle Calculation

The T-type operates at a low frequency and produces a voltage waveform with five levels at its output port, as shown in Fig. 2.20. The fundamental waveform of this output can be described as a function of the switching angles (α and β). To determine

the fundamental component of this waveform, the Fourier series can be used:

$$a_1 = \frac{1}{\pi}\int_0^{2\pi} v_{out_1}\cos(\theta)d\theta \tag{2.34}$$

$$b_1 = \frac{1}{2}\int_0^{2\pi} v_{out_1}\sin(\theta)d\theta \tag{2.35}$$

By evaluating these equations, the following coefficients can be determined:

$$a_1 = 0 \tag{2.36}$$

$$b_1 = \frac{2v_{pu}}{\pi}[\cos(\beta)+\cos(\alpha)] \tag{2.37}$$

Using these calculations, the fundamental voltage of the five-level waveform with a switching angle of α and β can be expressed as:

$$V_{inv1}^{fund} = \frac{2v_{pu}}{\pi}[\cos(\beta)+\cos(\alpha)]\sin(\omega t) \tag{2.38}$$

The α and β should be chosen to result in the minimum required capacitor voltage of the full bridge to increase the efficiency of the converter. Similar to the previous converter and as shown in Fig. 2.19, the peak of this waveform occurs at the switching angles. To minimize this value, the fundamental component of the five-level waveform should have a value of $v_{pv}/4$ at $\omega t = \alpha$ and $3v_{pv}/4$ at $\omega t = \beta$:

$$\frac{2v_{pu}}{\pi}[\cos(\beta)+\cos(\alpha)]\sin(\alpha) = \frac{v_{pu}}{4} \tag{2.39}$$

$$\frac{2v_{pu}}{\pi}[\cos(\beta)+\cos(\alpha)]\sin(\beta) = \frac{3v_{pu}}{4} \tag{2.40}$$

Simplifying these equations will result in the following equations:

$$\sin(\alpha+\beta)-\sin(\alpha-\beta)+\sin(2\beta) = \frac{3\pi}{4} \tag{2.41}$$

$$\sin(\alpha+\beta)+\sin(\alpha-\beta)+\sin(2\alpha) = \frac{\pi}{4} \tag{2.42}$$

Now the two equations and two unknowns can be solved using Matlab, and the resulting switching angles will be as follows:

$$\alpha = 13.44 \tag{2.43}$$

$$\beta = 44.22 \tag{2.44}$$

Assuming that the converter operates at unity power factor, and since the fundamental voltage of the converter is completely generated by the T-type converter, the peak of the fundamental waveform of this five-level waveform should be equal to the peak of the total voltage. Furthermore, in the resulting equation, the optimal values of the switching angles are known. Therefore, using this equation, the optimal value of the voltage of the T-type converter can be found, as shown here:

$$\hat{V}_{inv1}^{fund} = \frac{2v_{pu}}{\pi}[\cos(\beta) + \cos(\alpha)] = V_t \Rightarrow v_{pu} = \frac{\pi V_t}{2[\cos(\beta) + \cos(\alpha)]} \tag{2.45}$$

If the peak of the total voltage is considered 340, the optimal voltage of the upper inverter should be 316.15. However, similar to the previous topology, the voltage of the T-type inverter will be allowed to swing around the optimal point. To control the fundamental voltage, there are two choices: α or β. However, changing β can be a better option since the sine wave has sharper changes around α, which can lead to larger variations in capacitor voltage. To avoid that and simplify the control, α will be considered constant, and β will be adjusted to control the fundamental of the T-type converter.

The range within which the voltage of a T-type converter can swing should be chosen in a way that avoids the requirement of switches with a large voltage blocking capability in the full bridge. Therefore, the voltage of the capacitor connected to the full bridge should be calculated using the following equation:

$$V_c = Max\{\frac{v_{pv}}{2} - f_1(\alpha),\ f_1(\alpha),\ f_1(\beta) - \frac{v_{pv}}{2},\ v_{pv} - f_1(\beta)\} \tag{2.46}$$

$$V_{inv1}^{fund}(\alpha) = \frac{2v_{pu}}{\pi}[\cos(\beta) + \cos(\alpha)]\sin(\alpha) \tag{2.47}$$

$$V_{inv1}^{fund}(\beta) = \frac{2v_{pu}}{\pi}[\cos(\beta) + \cos(\alpha)]\sin(\beta) \tag{2.48}$$

Based on these equations, V_c is a function of three variables: α, β, and v_{pv}. As mentioned earlier, α will be considered constant and equal to 13.44. Additionally, β is a function of v_{pv} and can be calculated using the following equation:

$$\beta = \cos^{-1}\left(\frac{\pi V_t - 1.94522 v_{pu}}{2v_{pu}}\right) \tag{2.49}$$

Fig.2.21 demonstrates the correlation between the variable β and the value v_{pv}. Once β is established from the given v_{pv} value, the ratio V_c/v_{pv} can be derived as shown in Fig.2.22.

As shown in Fig. 2.22, the T-type converter can operate within a voltage range of 300 to 500. However, an improvement has been achieved by maintaining the V_c/v_{pv} ratio at around 34%, which is nearly half of what was previously required in the older topology. This enhancement not only leads to higher converter efficiency but also results in cost savings in terms of the switches used.

2.5.3 Current Controller

This part of the controller closely resembles the current controller used in the full bridge converter with a cascaded floating capacitor, which was previously discussed. Both controllers share the common objective of regulating the converter's current to control the reactive power and set the voltage of the PV source at the desired reference determined by the Maximum Power Point Tracking (MPPT) algorithm. This ensures that the PV system operates at its maximum power generation capacity.

Since the system operates as a single-phase converter, an orthogonal signal gen-

eration (OSG) block is employed to generate the orthogonal component of the grid current in the $\alpha\beta$ frame. The OSG block estimates the β-axis component of the grid current based on the values of I_d^* and I_q^*, as depicted in Fig.2.8. The resulting $\alpha\beta$ currents are then transformed to the DQ frame, and the controller utilizes these values to independently regulate the D and Q currents (Fig.2.9).

The simplified block diagrams of the current controller are illustrated in Fig. 2.10. Based on these diagrams, the coefficients of the PI compensates can be calculated as follows:

$$k_p = \frac{L}{\tau_i} \tag{2.50}$$

$$k_i = \frac{R}{\tau_i} \tag{2.51}$$

Finally, the output of the current controller, V_d and V_q, transforms stationary waveform, representing the voltage that the converter must generate at the terminals connected to the grid and inductance. This voltage, known as the total voltage (V_t), can be calculated using the following equation. In this equation, ω and φ are determined by the phase-locked loop (PLL) connected to the grid voltage.

$$V_t = V_d \sin(\omega t + \varphi) + V_q \cos(\omega t + \varphi) \tag{2.52}$$

2.5.4 Capacitor Voltage Regulator

The equations (2.46)-(2.49) demonstrate that the capacitor's voltage must be modified based on the voltage of the T-type converter. Fig. 2.23 provides a visual representation of how the capacitor voltage should be adapted based on the voltage of the T-type converter.

In a manner akin to the approach described in Section 2.2.4, the regulation of the full bridge voltage is crucial, and its control mechanism can be represented using

the block diagram shown in Fig. 2.13. By comparing the actual DC bus voltage with a reference command, the control unit manages the active power flow through the full bridge, either injecting or extracting power from the capacitor to maintain the desired voltage level. The controller achieves this goal by using a PI controller to adjust the magnitude of the fundamental voltage generated by the full bridge and by using V_t and V_g to align the generated fundamental voltage with the current passing through the full bridge.

2.6 Converters Comparison

Table 2.2 presents a comparison of the introduced full bridge cascaded inverter in this chapter with existing topologies. It is evident that this inverter demands fewer passive components and exhibits a broader input voltage range. Furthermore, unlike the majority of existing topologies, this inverter employs a blend of low-voltage high-frequency switches and high-voltage low-frequency switches to enhance its efficiency.

In addition, table 2.2 provides a comparison of the proposed T-type inverter with a cascaded floating capacitor against existing topologies. This topology, once again, requires a reduced number of passive components and has the capability of an extended operating range for input voltages. Additionally, it utilizes a combination of low-voltage high-frequency switches and high-voltage low-frequency switches to achieve better performance.

Table 2.2: Summary of Various Inverter Topologies

Topology	Input voltage range	Vg	No. of HVHF switches	No. of LVHF switches	No. of HVLF switches	No. of inductors	No. of capacitors
Half-Bridge Voltage Swing Inverter [3] Fig. 1.1	NR	120 / 60 Hz	5	0	1	4	5
The Z-source and quasi-Z-source inverters [21] & [22] Fig. 1.2	NR	NR	5	0	0	3-4	4-5
Two mode inverter [19] Fig. 1.3	220-420	230 / 50 Hz	9	0	1	2	2
Dual-Buck-Structured Buck-Boost Inverters [34] Fig. 1.5	70-200	155 / 60 Hz	4	0	4	6	4
Single-Stage Buck-Boost Inverters [40] Fig. 1.7	250-450	230 / 60 Hz	4	0	4	1 Inductor 1 Transformer	2
Proposed Full Bridge Cascaded Inverter	280-500	240 / 60 Hz	0	4	4	1	2
Proposed T-type Inverter with Cascaded Floating Capacitor	300-500	240 / 60 Hz	0	4	8	1	3

2.7 Simulation Results of T-type Inverter with Cascaded Floating Capacitor

In this section, the simulation results of the T-type inverter with a cascaded floating capacitor are provided to demonstrate the capability of this inverter to generate the required output voltage and current. The simulation investigates outcomes for two distinct input voltages sourced from the photovoltaic (PV) system. Initially, the focus is placed on a voltage level of 400, aligning with the converter's nominal operational voltage. The results are presented in Fig. 2.24, depicting the waveforms

of the output voltage, current, as well as the voltages across both full bridge outputs and the capacitor. These figures showcase the converter's proficiency in effectively generating the desired waveforms. Additionally, the harmonic content of the output current and voltage is depicted in Fig. 2.25, demonstrating the lower full bridge capability in reducing harmonics and generating a clean output waveform.

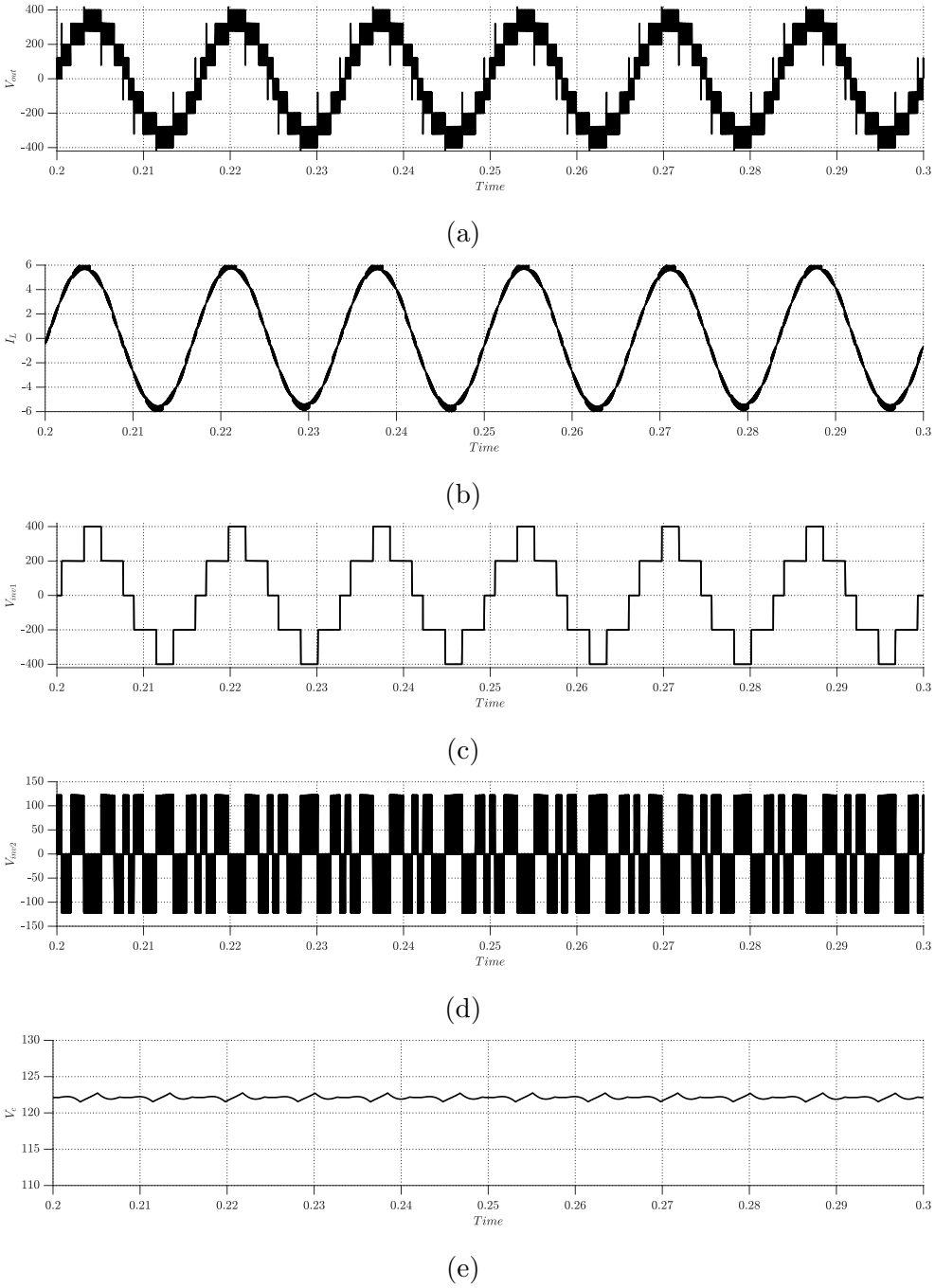


Figure 2.24: Waveforms of T-type inverter with cascaded floating capacitor ($V_{pv} = 400$): (a) Output voltage of inverter, (b) Output current, (c) Output voltage of T-type inverter, (d) Output voltage of full bridge, (e) Voltage of capacitor.

Moreover, Fig. 2.26 portrays the simulation results for a minimum operational threshold of the converter, which is $V_{pv} = 300$. The figures show that the converter accomplished the task of producing the intended output waveform and effectively regulated the capacitor voltage to the desired value. Furthermore, Fig. 2.27 demonstrates the successful harmonic suppression of the T-type converter, achieved once more through the application of the capacitor-linked full bridge setup. The circuit parameters for both simulations remain consistent and can be found in Table 2.3.

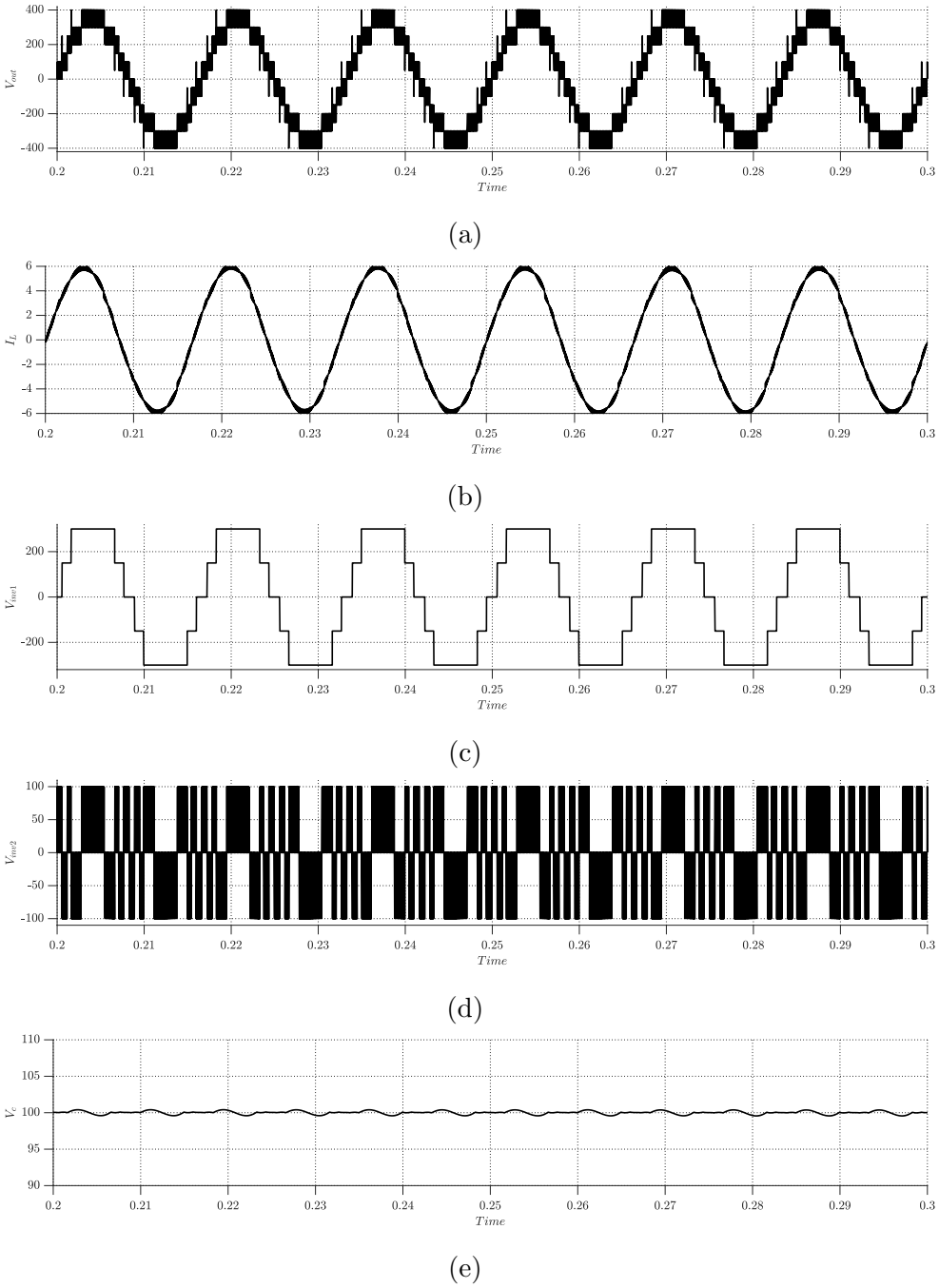
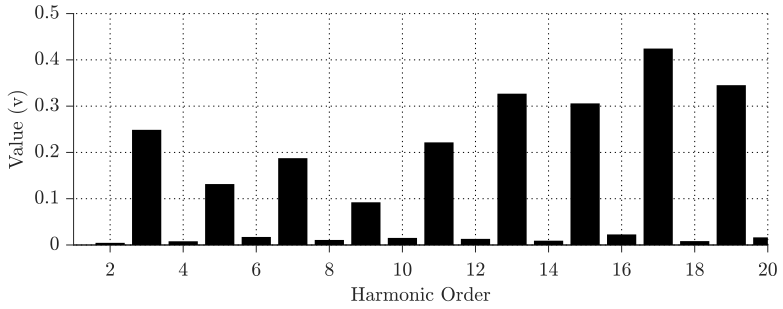


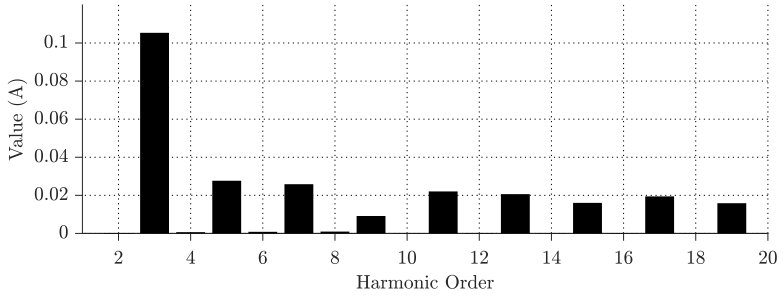
Figure 2.26: Waveforms of T-type inverter with cascaded floating capacitor ($V_{pv} = 300$): (a) Output voltage of inverter, (b) Output current, (c) Output voltage of T-type inverter, (d) Output voltage of full bridge, (e) Voltage of capacitor.

Table 2.3: System parameters of the T-type inverter with cascaded floating capacitor.

	Parameter	Value
Input voltage	V_{in}	300-500v
Grid voltage	V_g	240v
Filter inductance	L	3mH
Capacitance	C	1mF
T-type converter switching frequency	f_{s1}	60/120Hz
full bridge switching frequency	f_{s2}	30kHz



(a)



(b)

Figure 2.27: T-type inverter with cascaded floating capacitor ($V_{pv} = 400$): (a) Harmonic spectrum of the output voltage, (b) Harmonic spectrum of the output current.

The simulation results for the T-type inverter with cascaded floating capacitor reveal its ability to consistently generate the required output voltage and current. The converter effectively minimizes the harmonic content in the output waveform, thanks to the integrated capacitor-linked full bridge configuration. This promising performance makes the converter a promising choice for PV system applications.

2.8 Summery

This chapter introduces two novel inverter designs capable of accommodating an extended input voltage range. The first topology is the full-bridge inverter with a cascaded floating capacitor, utilizing two cascaded full bridges. In this configuration, the PV-connected full-bridge operates at a low switching frequency to produce the required output waveforms. Meanwhile, the second full-bridge operates at a high frequency to effectively mitigate harmonics. However, the blocking voltage of the switches in the lower full bridge is reduced to approximately 60% of the input voltage. This hybrid configuration contributes to enhanced converter efficiency. Simulation results are presented to demonstrate the converter's proficiency in generating the desired voltage and current across various input voltage ranges.

The second proposed converter in this chapter adopts a T-type inverter with a cascaded floating capacitor. In this converter, the T-type topology replaces the full-bridge inverter to interface with the PV source. Once again, the T-type inverter will operate at a low switching frequency, tasked with generating the fundamental component of the output voltage. The full bridge connected to the capacitor in this configuration is responsible for canceling out the harmonics. This full bridge also operates at a high switching frequency; however, the blocking voltage of the switches is reduced to around 30%, which is half of the value utilized in the first converter. Sim-

ulation results once again validate the converter's performance in generating desired output waveforms, with low harmonics achieved through active harmonic filtering via the full bridge configuration.

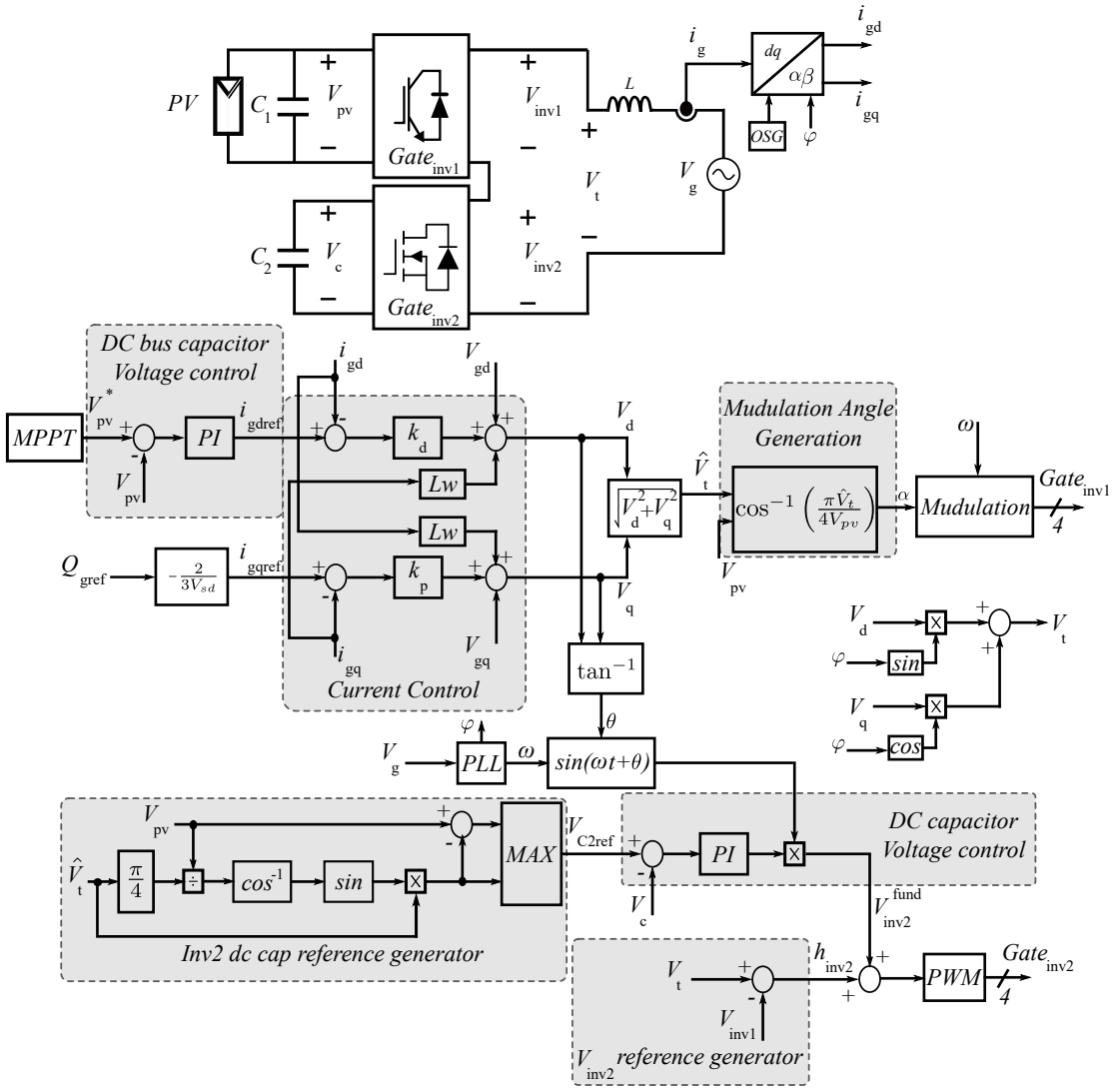


Figure 2.3: Controller block diagram of the full-bridge converter with a cascaded floating capacitor.

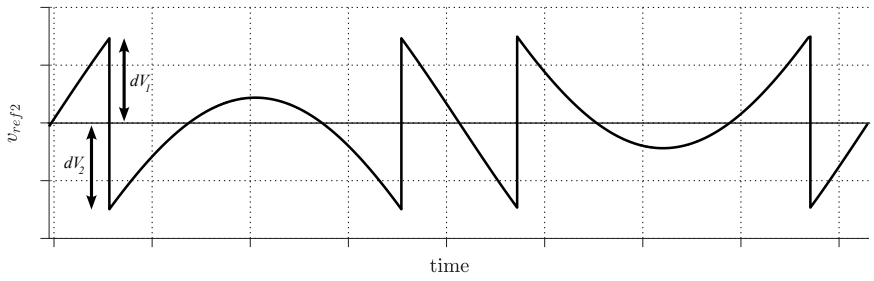


Figure 2.4: Reference voltage of the second full bridge.

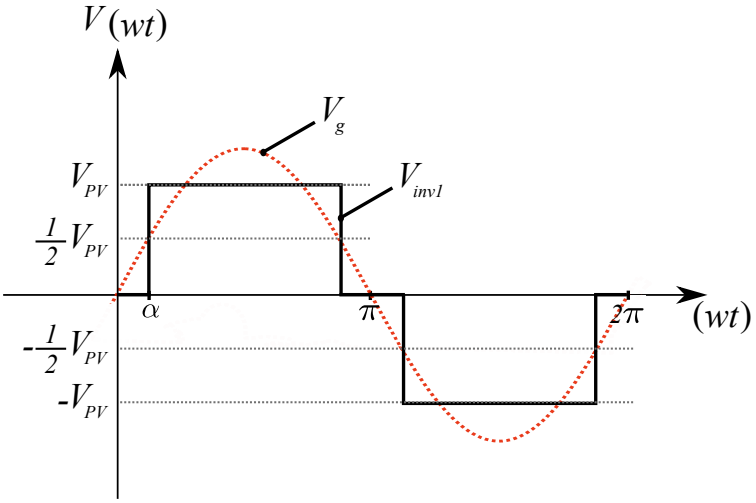


Figure 2.5: Full bridge three-level output waveform.

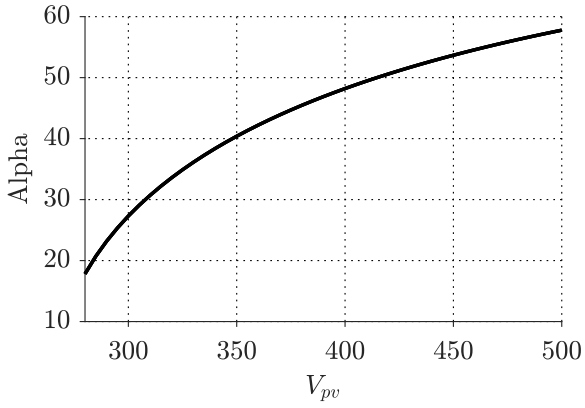


Figure 2.6: Switching angle based on the source voltage.

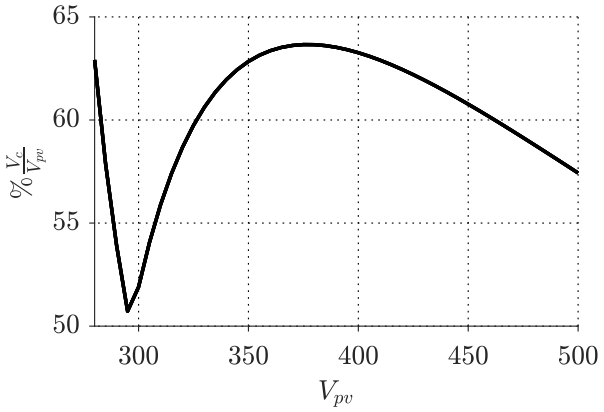


Figure 2.7: The ratio of the capacitor voltage to the source voltage.

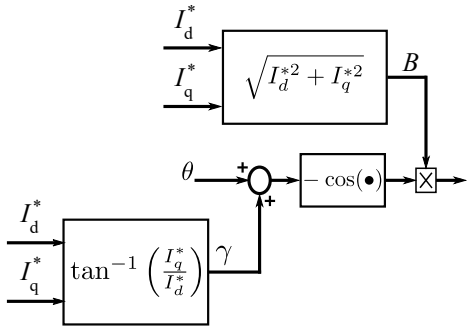


Figure 2.8: OSG block diagram [42].

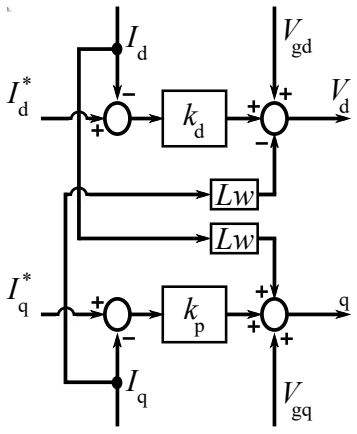


Figure 2.9: DQ current controller

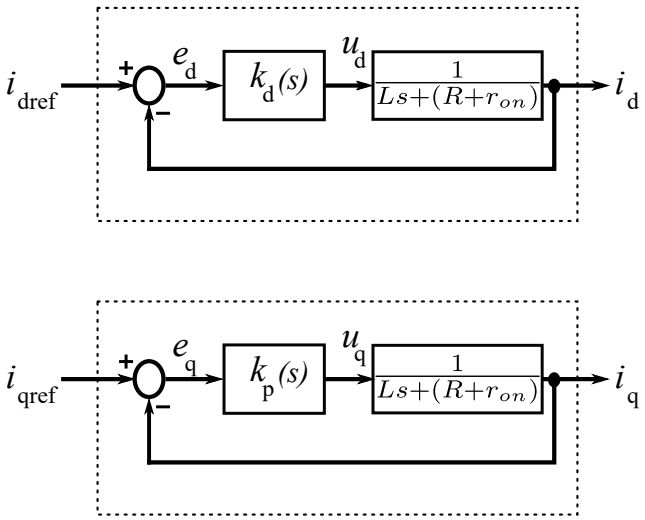


Figure 2.10: Simplified current controller

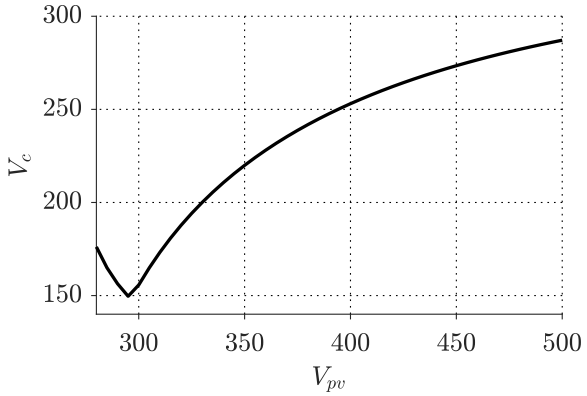


Figure 2.11: Capacitor voltage based on the source voltage.

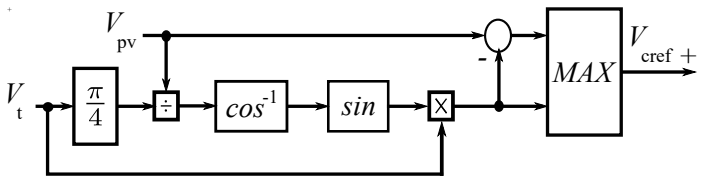


Figure 2.12: Capacitor voltage reference calculator.

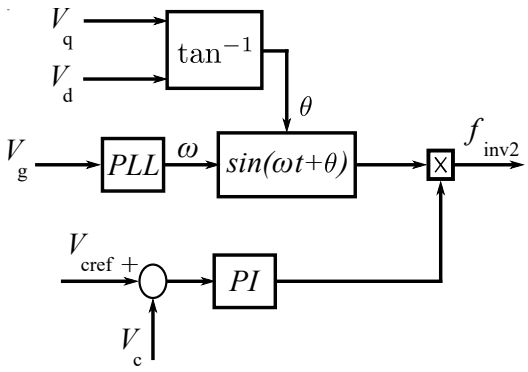


Figure 2.13: Capacitor voltage reference calculator.

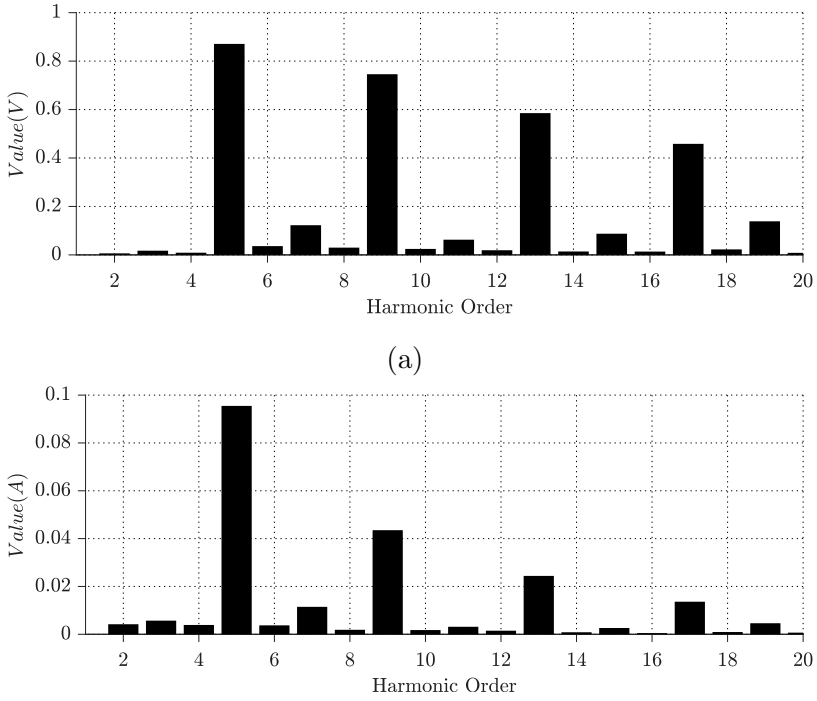


Figure 2.15: Full bridge inverter with a cascaded floating capacitor ($V_{pv} = 400$): (a) Harmonic spectrum of the output voltage, (b) Harmonic spectrum of the output current.

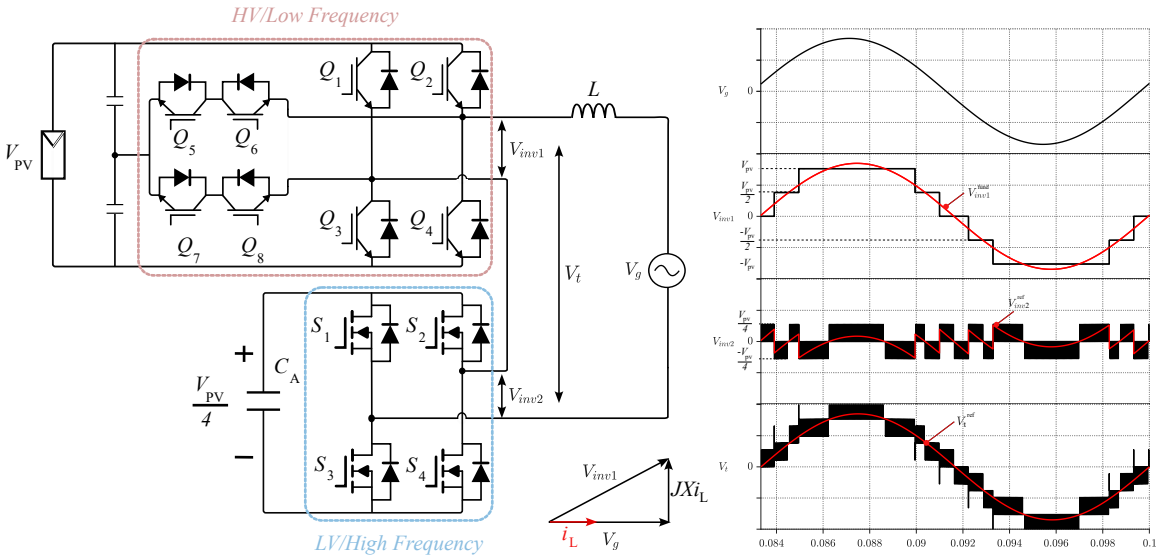


Figure 2.18: T-type inverter with cascaded floating capacitor and important waveform of the converter.

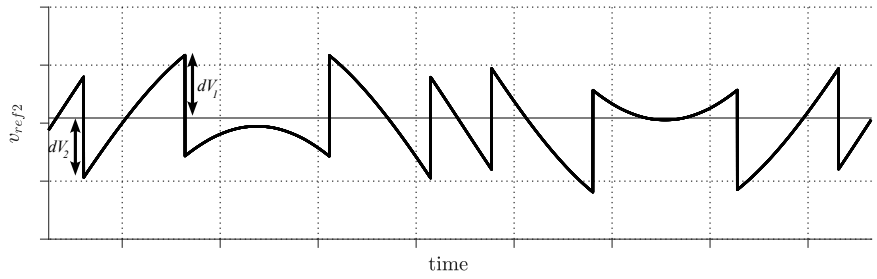


Figure 2.19: Reference voltage of the full bridge.

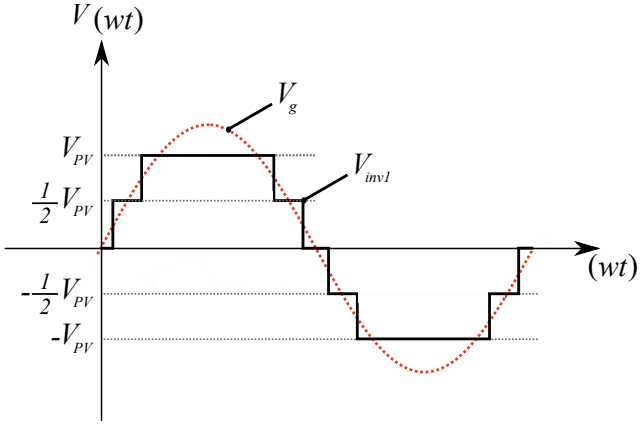


Figure 2.20: Output voltage of T-type converter.

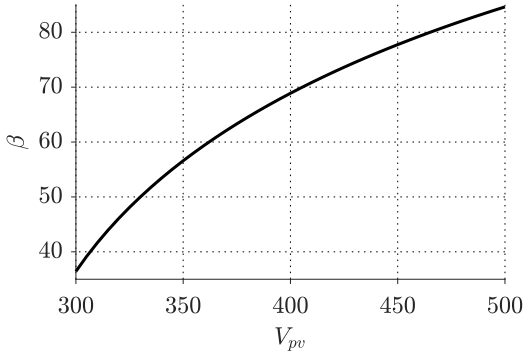


Figure 2.21: β based on the voltage of the T-type converter's source.

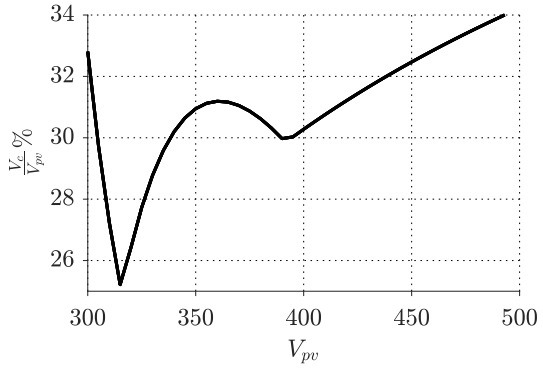


Figure 2.22: The ratio of the capacitor voltage to the voltage of the T-type converter's source.

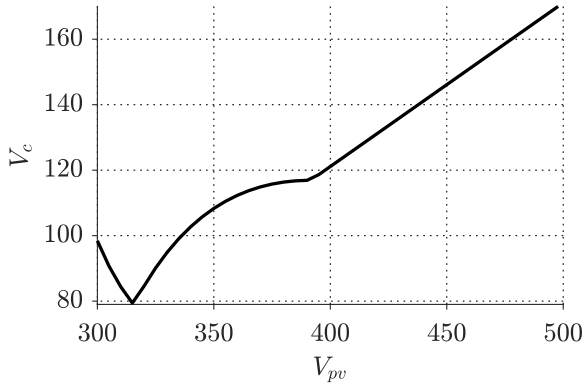


Figure 2.23: Capacitor voltage based on the voltage of the T-type converter's source.

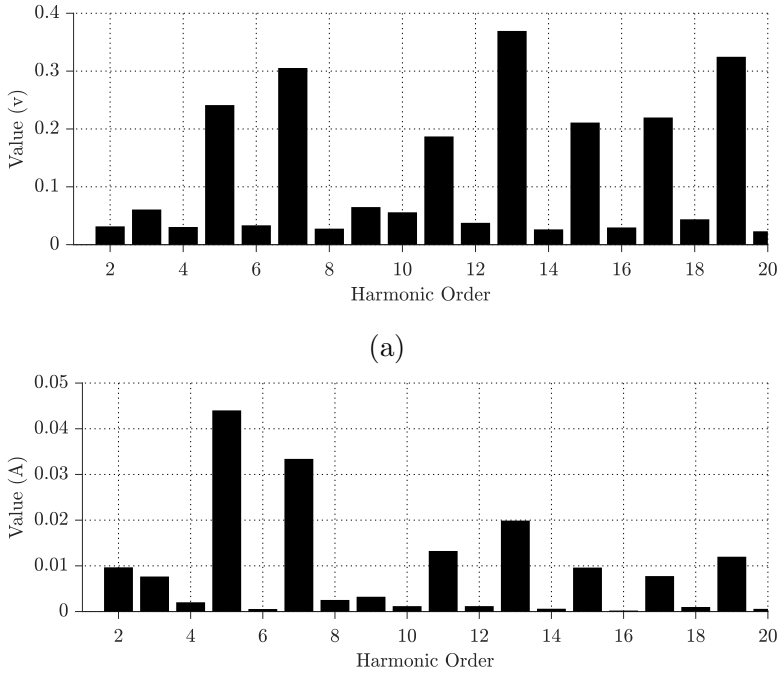


Figure 2.25: T-type inverter with cascaded floating capacitor ($V_{pv} = 400$): (a) Harmonic spectrum of the output voltage, (b) Harmonic spectrum of the output current.

Chapter 3

Flyback-Assisted Wide Input Range Inverter

This chapter presents another topology aimed at achieving an inverter with a wide input range of voltage. In this proposed configuration, an individual PV source solely feeds the system, and a flyback converter is utilized to interconnect the upper and lower full bridges, as illustrated in Fig. 3.1.

Operational efficiency is a crucial aspect of the proposed design. To this end, the high-voltage full-bridge operates at a low switching frequency and handles between 75% to 100% of the total output power, depending on the required voltage of the solar panel to operate at MPP. This ensures that the entire system maintains a high level of efficiency.

On the other hand, the flyback converter and low-voltage full bridge operate at high switching frequencies. However, in this stage, only a maximum of 25% of the power is processed, thereby guaranteeing superior efficiency compared to existing

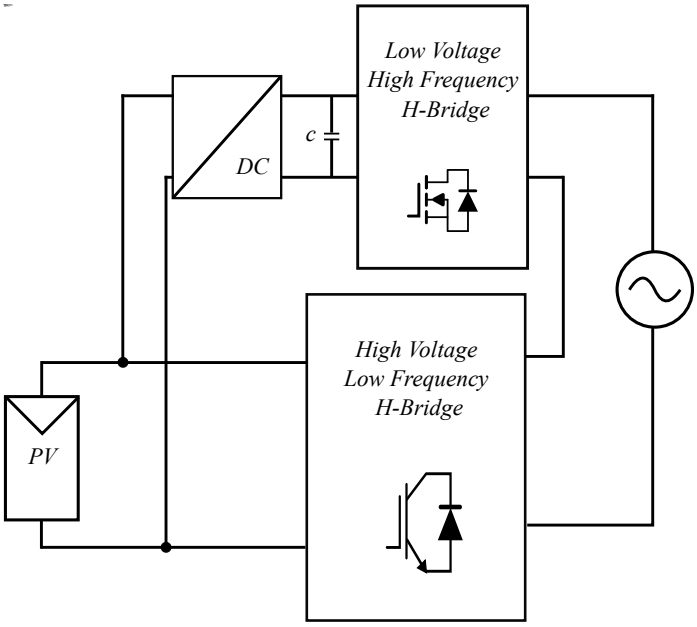


Figure 3.1: Block diagram of the proposed flyback-assisted Wide input range inverter

topologies. Additionally, the flyback converter will be switched out when the voltage of the PV system is high enough to generate the required fundamental voltage alone. This way, the switching loss of the flyback converter will be reduced, and efficiency can be further improved.

In addition, the proposed topology extends the range of achievable voltage compared to the topologies presented in the previous chapter. The flyback converter's ability to process a portion of the power allows for a decrease in the lower voltage limit of the PV (Photovoltaic) system. Additionally, the size of the low-power transformer required for the flyback converter is considerably smaller compared to the high inductance filter required by conventional 2-level inverters. Moreover, the size of the filter required for this topology is also reduced due to the elimination of harmonics by the high-frequency full bridge.

By incorporating these features, the new topology demonstrates promising advantages in terms of efficiency, size, and extended voltage range. The subsequent sections of this chapter will delve into the theoretical framework, detailed design, and performance evaluation of the proposed inverter topology, highlighting its potential applications and benefits in the field of renewable energy systems.

3.1 Circuit Configuration of Flyback-Assisted Wide Input Range Inverter

The single-source inverter proposed in this Chapter comprises two converter stages: the flyback converter and the asymmetric cascaded full bridge inverter. The complete circuit diagram of the inverter is depicted in Fig. 3.2. The operation of each of these parts will be discussed in detail in the following sections.

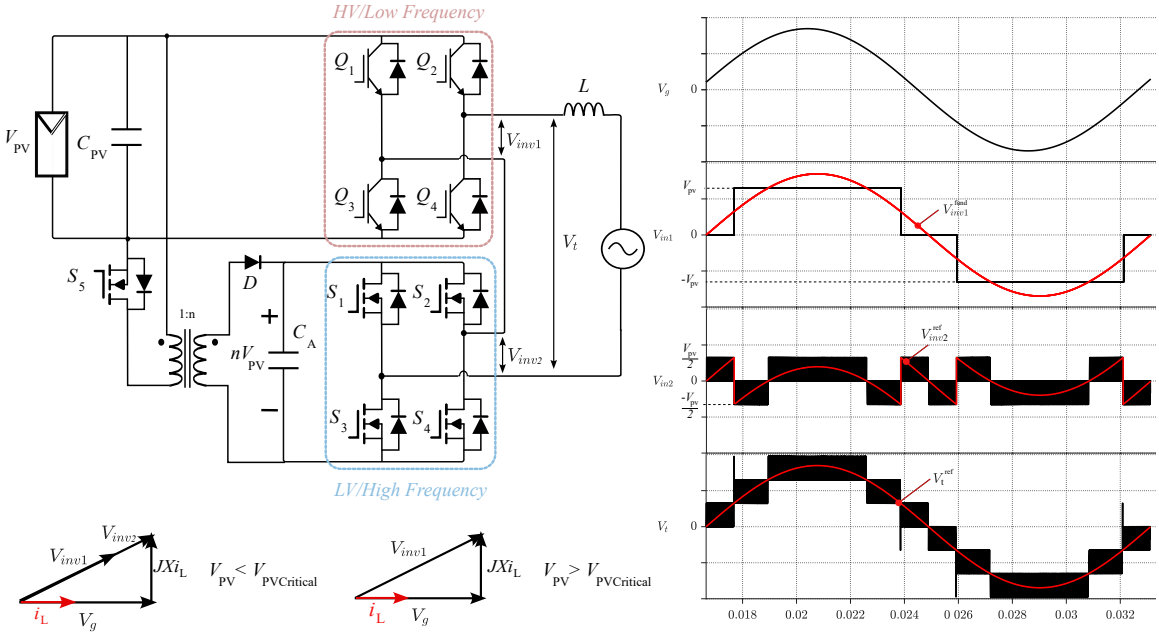


Figure 3.2: Circuit configuration of the proposed flyback-assisted inverter and the important waveforms of the converter

3.1.1 Power Circuit Description and Operation

The cascaded full bridge inverters can be categorized into two groups: symmetric and asymmetric inverters. In conventional symmetric cascaded full bridges, the DC sources have equal voltage levels. In contrast, asymmetric inverters distribute the sources unequally. While symmetric multilevel inverters offer the advantage of a smaller switch voltage stress, asymmetric multilevel inverters can produce a higher number of voltage levels with the same number of full bridge modules. This characteristic results in an output waveform with lower harmonics and enables the reduction in the size of the output converter's filter. In addition, in the proposed inverter the switches with the higher voltage stress operate at the grid freq and thus the unequal voltage stress caused by asymmetrical cascaded multilevel inverter is not an issue. The number of voltage levels obtained with a given N number of H-bridge modules in the case of symmetric multilevel inverters can be expressed as [20]:

$$L = 2N + 1 \tag{3.1}$$

On the other hand, the number of voltage levels for asymmetric multilevel inverters is given by [20]:

$$L = 2^{N+1} - 1 \tag{3.2}$$

Additionally, the lower full bridge, operating at a high frequency, can effectively eliminate the harmonics generated by the upper full bridge due to its low switching frequency. However, in this topology, when the PV voltage drops below a certain value, as illustrated by the phase diagrams in Fig. 3.2, the lower inverter should supply active power. The generation of active power by the lower full bridge can be achieved because another converter is connected to transfer power from the source to the lower full bridge.

It is worth noting that the additional Flyback converter does not need to provide the rated output power. The amount of the fundamental that the lower full bridge is required to generate varies between 25% and 0%, depending on the voltage of the PV source. Therefore, the Flyback converter is only required to be designed at a fraction of the output rated power.

In this topology, the switching devices in both full bridges experience different levels of voltage stress and operate under different frequencies. Ideally, MOSFETs with low conduction resistance $R_{ds_{on}}$ are preferred for the lower full bridge, while the IGBT is better suited for the upper full bridge (Appendix A). The hybrid configuration of IGBT and MOSFET switches capitalizes on the strengths of each type, enabling the inverter to operate optimally across a wide input voltage range.

3.2 Control System Description for the Flyback-Assisted Inverter

The generation of the output voltage with desired characteristics and low harmonics necessitates the utilization of a sophisticated control algorithm capable of producing appropriate references for the modulation block, which can be converted to the switching gates as shown in Fig. 3.3.

The power converter's controller comprises three main parts. The first part of the controller has the responsibility of controlling the current, which is the same as the current controller proposed for the previous converters. This part ensures that the voltage of the PV source is regulated at the desired voltage level determined by the MPPT and also controls the reactive power of the converter.

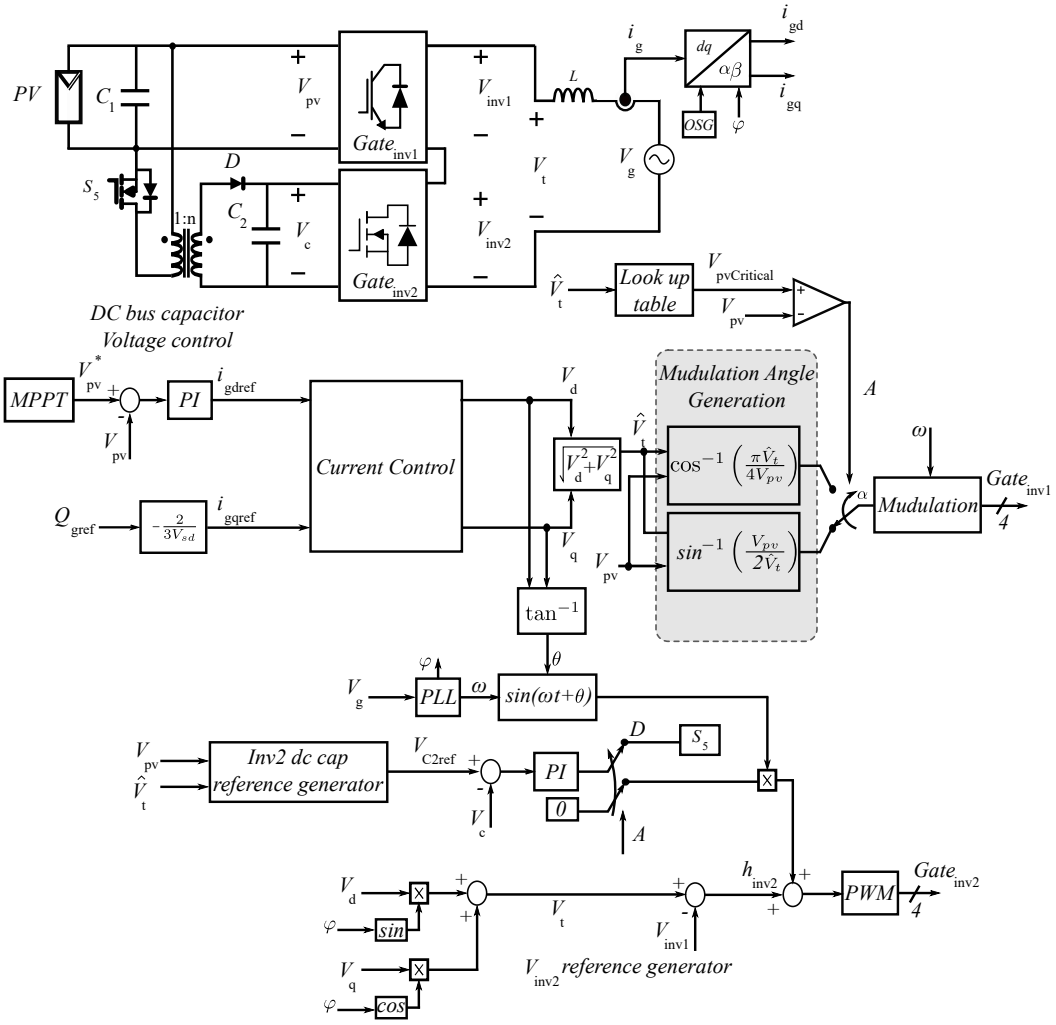


Figure 3.3: Control system of the proposed flyback-assisted inverter

The second control section is responsible for regulating the modulation angle of the main full bridge, such that the maximum possible active power is extracted from the PV and provided by the main full bridge. The third part has the responsibility of overseeing the flyback and lower full bridge. Moreover, this section of the controller is tasked with generating the appropriate reference for the lower full bridge, enabling the cancellation of harmonics from the main full bridge and the generation of a portion of the fundamental voltage of the output waveform based on the voltage of

the source connected to the upper full bridge. As the first part is similar to the previous chapter, the details of the second and third parts of the controller will be discussed in the following sections.

3.2.1 Control of Modulation Angle

In the operation of this inverter, the goal is to process as much power as possible using the full bridge converter connected to the PV source. The flyback and lower full bridge are reserved to generate the fundamental voltage only in case the main full bridge faces a problem. When the PV voltage is high enough, the main full bridge can generate all the fundamental voltage required by the system, the controller will turn off the flyback converter to reduce unnecessary switching losses. This is achieved by using the comparator and lookup table in the control block diagram (Fig. 3.3). The converter functions like a full bridge inverter with an auxiliary floating capacitor, and the modulation angle remains the same as previous chapter, as shown here:

$$\alpha = \cos^{-1}(\frac{\pi \hat{V}_t}{4v_{\rho v}}) \tag{3.3}$$

However, when the main full bridge cannot generate the required fundamental voltage, the flyback is activated, and the previous equation is no longer valid. This occurs when the peak of the fundamental voltage generated by the main full bridge is lower than the peak of the grid voltage, as shown in the phase diagram, Fig. 3.2. The output voltage of the main full-bridge connected to the source exhibits a three-level waveform, and the total fundamental voltage (V_t) required is illustrated in Fig. 3.4. Therefore,

$$\hat{V}_{inv_1}^{fund} = b_1 = \frac{4v_{pv}}{\pi}\cos(\alpha) < \hat{V}_t \tag{3.4}$$

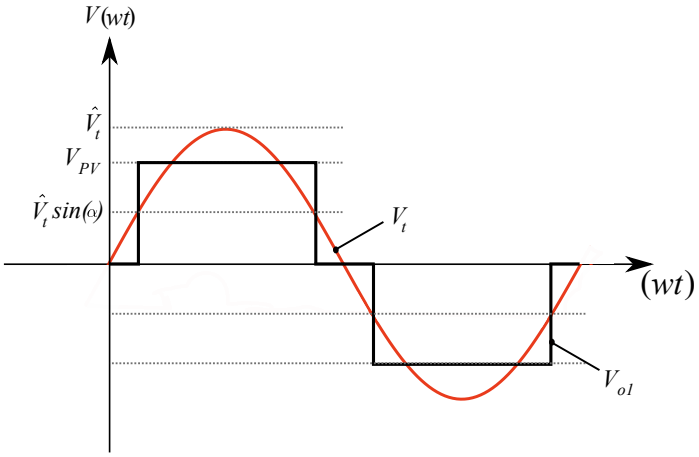


Figure 3.4: Output voltage of PV-connected full bridge and the desired total voltage (V_t).

Since the reference of the second full bridge will be the difference between the total voltage and the generated voltage of the main full bridge, the peak of the fundamental voltage required by the second full bridge can be calculated as follows:

$$\hat{V}_{inv2}^{fund} = \hat{V}_t - \hat{V}_{inv_1}^{fund} = \hat{V}_t - \frac{4v_{pv}}{\pi}\cos(\alpha) \tag{3.5}$$

As it is explained in section 2.2.1, to minimize the lower full bridge inverter bus voltage, in this mode of operation, it is better to find α such that $dV_1 = dV_2$ in Fig. 3.2. Therefore:

$$\hat{V}_t \sin(\alpha) = \frac{v_{pv}}{2} \tag{3.6}$$

For this mode of operation, using (3.6) the modulation angle can be found as follows:

$$\alpha = \sin^{-1}\left(\frac{V_{pv}}{2\hat{V}_t}\right) \tag{3.7}$$

Based on the modulation angle equations (3.3) and (3.7), Fig. 3.5 shows how the value of α changes based on the variation of v_{pv} when $\hat{V}_t$ is equal to 340. This alpha generation block for two modes of operation is implemented as shown in Fig. 3.3.

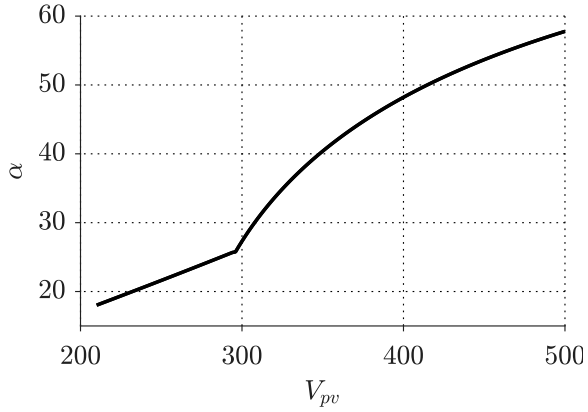


Figure 3.5: Modulation angle based on the voltage of the PV source.

3.2.2 Control of Flyback and Capacitor-Connected Full Bridge

As shown in the control block diagram of Fig.3.3, the lower full bridge should provide the harmonics and fundamental components that the main full bridge could not generate. Therefore, the reference of the lower full bridge can be calculated using the following equation:

$$V_{ref_2}(t) = V_t(t) - V_{inv_1}(t) \tag{3.8}$$

To generate this reference voltage, a control system should be implemented for both the lower full bridge and the flyback converter to accurately modulate them. The details of these controllers will be discussed in more detail in the following sections.

Lower Full Bridge Bus Control

The lower full bridge can generate the reference voltage calculated in (3.8) if the voltage of its capacitor is regulated at a value higher than the peak of its reference. Otherwise, the system will suffer from overmodulation and produce subharmonics in the output. The reference voltage of the capacitor, which is higher than that of

the lower full bridge, can be calculated using the following equation. This equation, unlike the previous ones used for calculating the reference of the capacitor voltage in the previous chapter, has three terms labeled $dV_1 - dV3$ in Fig. 3.6. As shown in this figure, the third term appears since the lower full bridge may process part of the fundamental voltage, which may cause the peak of the reference voltage for the lower full bridge to occur at 90°. Therefore,

$$V_{C_{\text{ref}}} = \text{Max}\left[\widehat{V}_t \sin(\alpha), V_{pv} - \widehat{V}_t \sin(\alpha), \widehat{V}_t - V_{pv}\right] \tag{3.9}$$

As shown in the control block diagram, this equation will be used in this mode by switching the $V_{C_{ref}}$ at the critical points. The PI shown in the diagram will control the duty cycle of the full bridge to make sure the voltage of the capacitor is controlled at its minimum voltage possible.

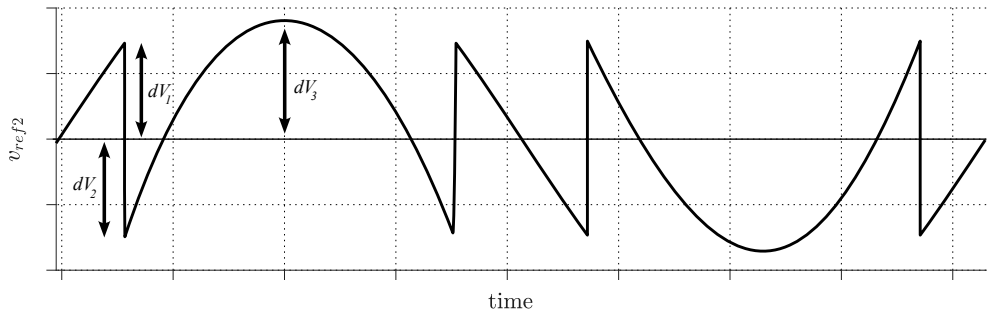


Figure 3.6: Reference of the capacitor connected full bridge.

Using (3.9), the percentage of V_c to V_{pv} for different voltages of the PV source can be plotted as shown in Fig. 3.7. This figure also indicates the critical point where the converter turns off or on the flyback and alters the equation that its controller uses to calculate the modulation angle. As can be observed, by implementing this modulation angle controller, the required voltage of the capacitor is limited to a maximum of 64% of the PV voltage. This allows the lower full bridge to use low-voltage switches, thereby increasing the efficiency of the converter.

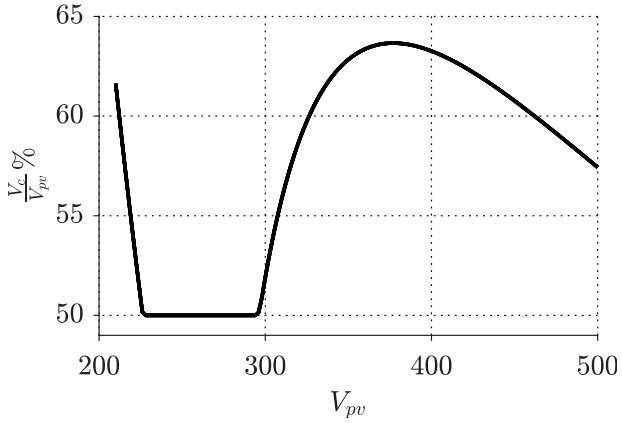


Figure 3.7: Percentage of the capacitor voltage based on the voltage of the PV source.

Flyback Control Mechanism

If the main full bridge can provide the total fundamental required, (3.8) will not have any fundamental component, and the flyback is not required. However, when the main full bridge cannot generate the total fundamental voltage required, the fundamental voltage that the second full-bridge must generate based on v_{pv} can be found by substituting the α from (3.7) into (3.5):

$$\hat{V}_{inv2}^{fund} = \hat{V}_t - \frac{4v_{pn}}{\pi} \cos\left(\sin^{-1}\left(\frac{v_{pv}}{2\hat{V}_t}\right)\right) \tag{3.10}$$

Using this equation, the required percentage of the fundamental voltage that should be generated by the second full-bridge based on the total required fundamental voltage can be found, as shown in Fig. 3.8. As can be seen, after the critical voltage is reached, the percentage will be reduced to zero since the flyback will be turned off by the controller, and no fundamental voltage will be generated by the lower full bridge.

Now, the question is when to switch between these modes of operation. The flyback turns on when the fundamental of the second full bridge in (3.10) becomes

greater than or equal to zero.

$$\hat{V}_{inv2}^{fund} = \hat{V}_t - \frac{4v_{pn}}{\pi}\cos\left(\sin^{-1}\left(\frac{v_{pv}}{2\hat{V}_t}\right)\right) \geq 0 \tag{3.11}$$

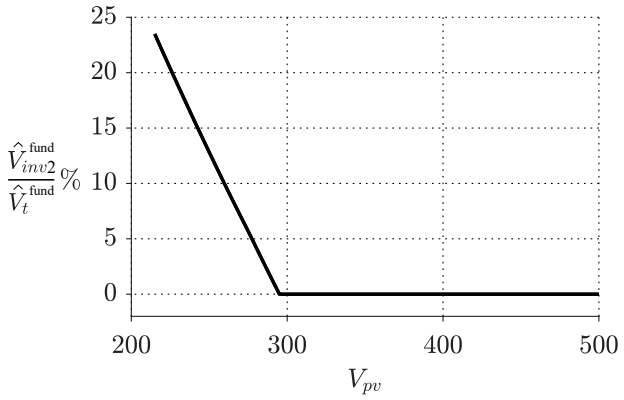


Figure 3.8: Percentage of the generated fundamental voltage based on the voltage of the PV source.

Therefore, to find the value of $V_{pv_{Critical}}$, the following equation must be solved:

$$\left.\begin{aligned} &\hat{V}_t - \frac{4v_{pv}}{\pi}\cos(\alpha) = 0 \\ &\alpha = \sin^{-1}\left(\frac{v_{pv}}{2\hat{V}_t}\right) \end{aligned}\right\} \Rightarrow \hat{V}_t - \frac{4v_{pv}}{\pi}\cos\left(\sin^{-1}\left(\frac{v_{pv}}{2\hat{V}_t}\right)\right) = 0 \tag{3.12}$$

Solving this nonlinear equation in Matlab results in solutions provided in Fig. 3.9. The switching points are used in a look-up table as shown in the control block diagram Fig. 3.3 to generate switching time for V_{pv}.

In summary, this inverter operates in two stages. In the first stage, the flyback is activated, allowing it to process a portion of the fundamental output voltage. Consequently, the inverter can function at lower voltages compared to a full bridge inverter with an auxiliary floating capacitor. During this interval, the flyback converter has the task of controlling the voltage of the capacitor while processing the required active power to enable the lower full bridge to generate the fundamental voltage.

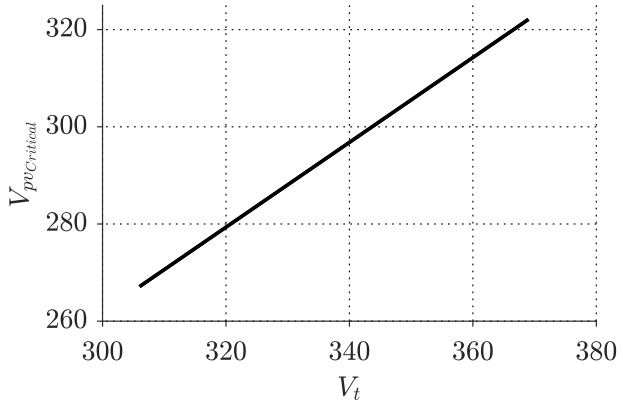


Figure 3.9: Critical voltage ($V_{pv_{Critical}}$) based on the desired output voltage (V_t)

However, in the second stage, the controller deactivates the flyback, causing the system to operate exactly like a full bridge inverter with an auxiliary floating capacitor. During this interval, the same capacitor voltage controller as the one discussed in section 2.2.4 will be used. The reason behind turning off the flyback in the second stage lies in the main full bridge's capability to generate the desired fundamental voltage when the voltage of the source exceeds a critical value denoted as $V_{pv_{Critical}}$. The details of how to calculate $V_{pv_{Critical}}$ will be discussed in the next section. Additionally, turning off the flyback can enhance efficiency and reduce unnecessary switching losses associated with the flyback converter.

3.3 Simulation results

This section presents the simulation results for a flyback-assisted wide input range inverter to demonstrate the performance and capability of this inverter in generating the required output waveforms across a wide voltage range of PV systems. First, the simulation is conducted for 400, which is the nominal voltage of the inverter.

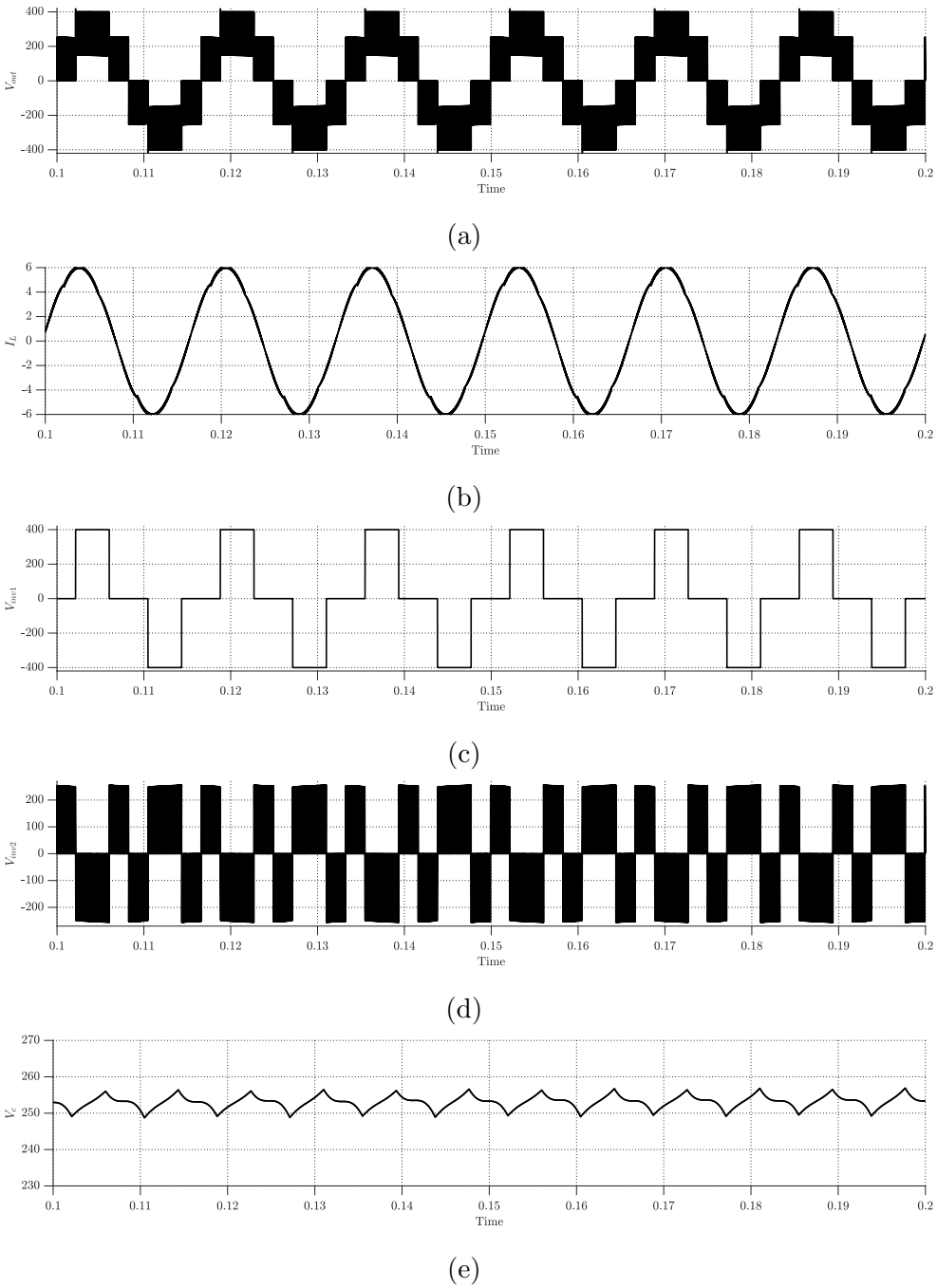


Figure 3.10: Waveforms of the flyback-assisted inverter ($V_{pv} = 400$): (a) Output voltage of the inverter, (b) Output current, (c) Output voltage of PV connected a full bridge, (d) Output voltage of capacitor connected a full bridge, (e) Voltage of capacitor.

Fig. 3.10 depicts the waveforms of the output voltage, current, and voltage of both full bridge outputs, along with the voltage of the capacitor. These figures illustrate that the converter effectively produced the required output voltage and current. The harmonic spectrum of these waveforms is provided in Fig. 3.11 to demonstrate the low harmonic content of the output waveforms and the capability of the lower full bridge to eliminate the harmonics generated by the PV-connected full bridge.

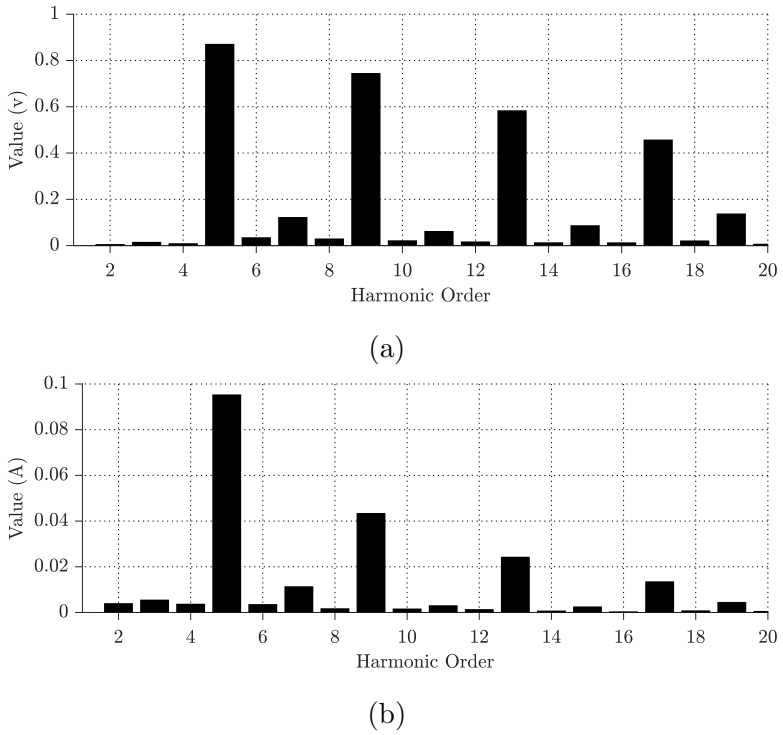


Figure 3.11: flyback-assisted inverter ($V_{pv} = 400$): (a) Harmonic spectrum of the output voltage, (b) Harmonic spectrum of the output current.

Furthermore, the simulation results for the lowest possible voltage of the PV source, which is 210, are reported in Fig. 3.12. As the plots show, the converter can still generate a high-quality waveform at its output despite the drop in the PV voltage. This is primarily due to the assistance of the flyback converter in generating 25% of the required fundamental output voltage through the lower full bridge.

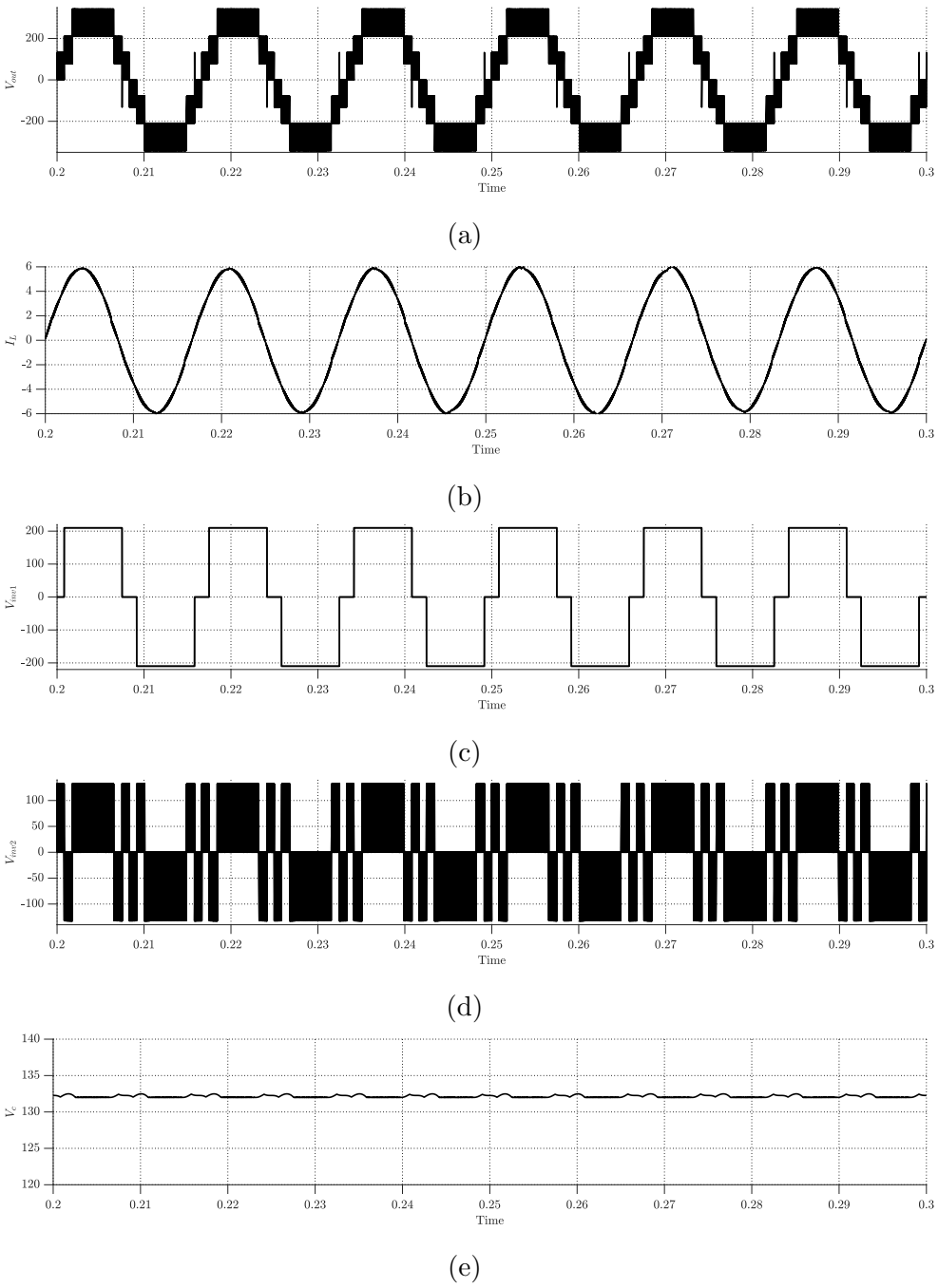


Figure 3.12: Waveforms of the flyback-assisted inverter ($V_{pv} = 210$): (a) Output voltage of the inverter, (b) Output current, (c) Output voltage of PV connected full bridge, (d) Output voltage of capacitor connected full bridge, (e) Voltage of capacitor.

Additionally, as illustrated in Fig. 3.13, the converter effectively eliminates the harmonics of the PV-connected full bridge by utilizing the capacitor-connected full bridge configuration and active filtering. The circuit parameters for both simulations are identical and are presented in Table 3.1.

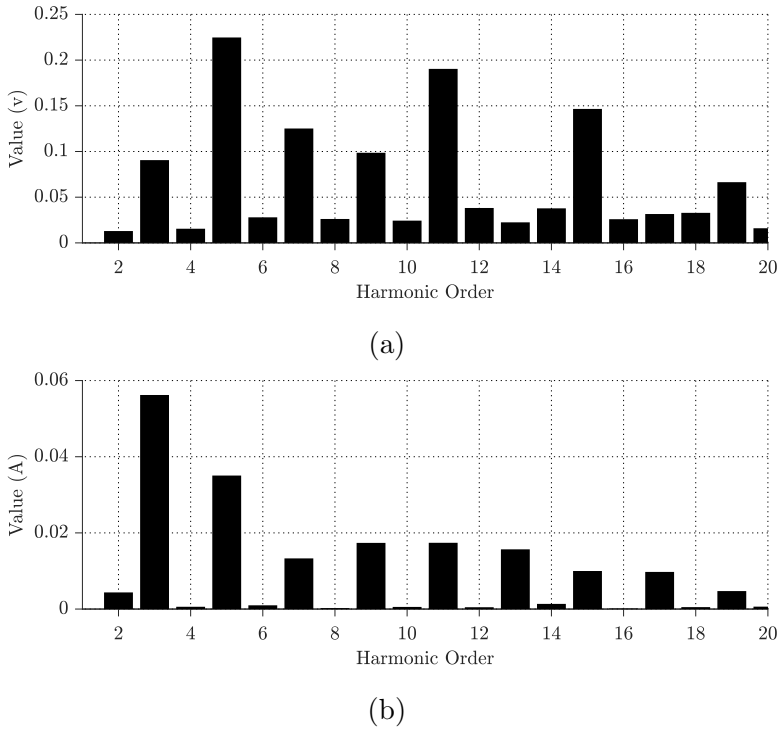


Figure 3.13: Flyback-assisted inverter ($V_{pv} = 210$): (a) Harmonic spectrum of the output voltage, (b) Harmonic spectrum of the output current.

To demonstrate the controller's performance during transient conditions, simulation results are provided for the scenario that the voltage of the PV system drops from $350v$ to $250v$, as shown in Fig. 3.14. The waveforms indicate that when the PV voltage drops, the controller activates the flyback converter, reducing the lower full bridge capacitor voltage to the desired value. Moreover, after the transient has passed, the system can successfully generate the required output voltage with the assistance of the flyback converter.

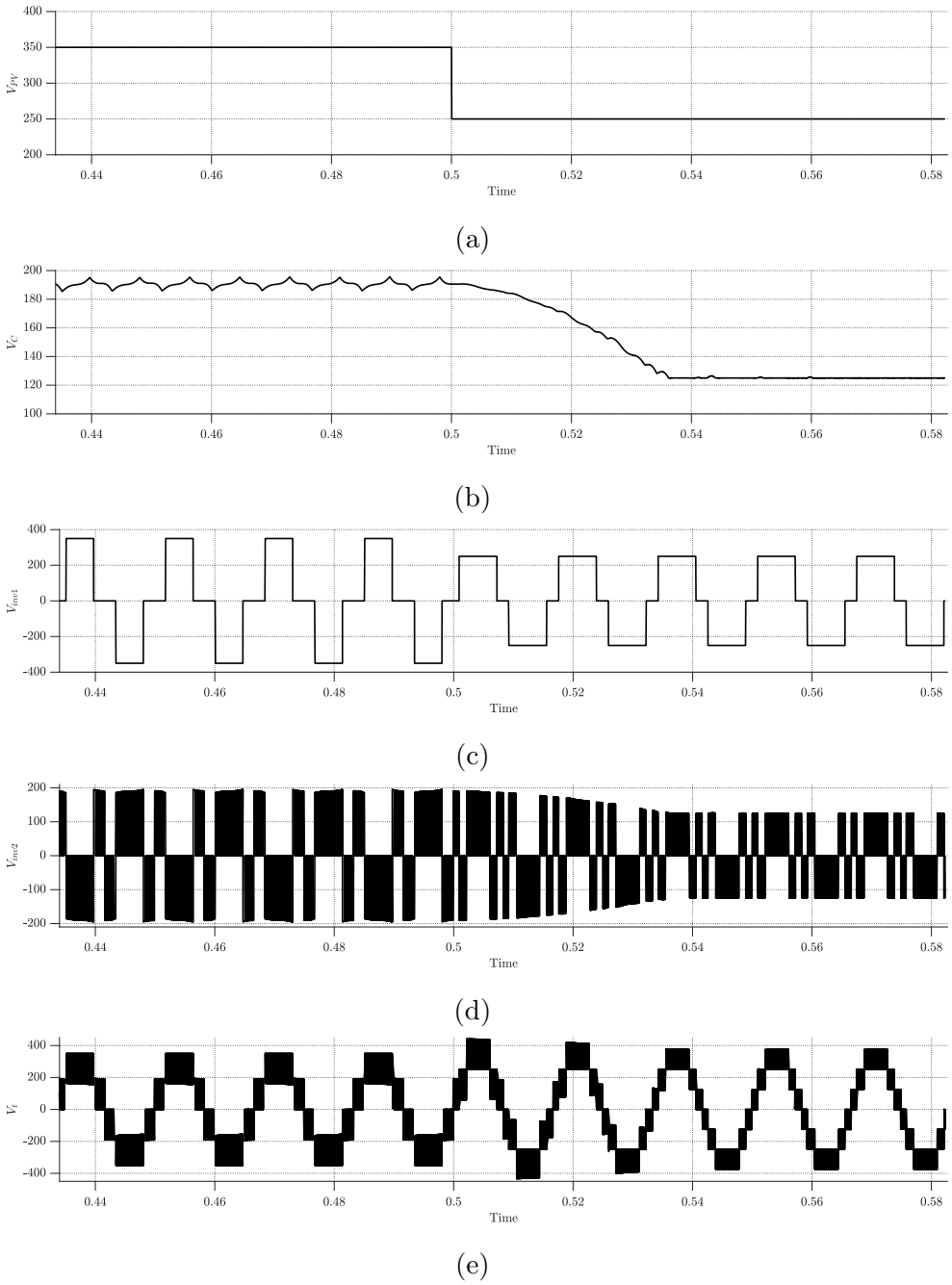


Figure 3.14: Waveforms of the flyback-assisted inverter when the V_{pv} drops from $350v$ to $250v$: (a) Voltage of the PV, (b) Voltage of the lower full bridge capacitor, (c) Output voltage of PV-connected full bridge, (d) Output voltage of capacitor-connected full bridge, (e) Output voltage of the inverter.

Table 3.1: System parameters of the flyback-assisted inverter.

	Parameter	Value
Input voltage	V_{in}	210-500v
Grid voltage	V_g	240v
Filter inductance	L	1mH
Capacitance	C	2mF
Upper full bridge switching frequency	f_{s1}	60Hz
Lower full bridge switching frequency	f_{s2}	60kHz
Flyback Converter switching frequency	f_{sf}	60kHz

Table 3.2: Summary of Various Inverter Topologies

Topology	Input voltage range	Vg	No. of HVHF switches	No. of LVHF switches	No. of HVLF switches	No. of inductors	No. of capacitors
Half-Bridge Voltage Swing Inverter [3] Fig. 1.1	NA	120 / 60 Hz	5	0	1	4	5
The Z-source and quasi-Z-source inverters [21] & [22] Fig. 1.2	NA	NA	5	0	0	3-4	4-5
Two mode inverter [19] Fig. 1.3	220-420	230 / 50 Hz	9	0	1	2	2
Dual-Buck-Structured Buck-Boost Inverters [34] Fig. 1.5	70-200	155 / 60 Hz	4	0	4	6	4
Single-Stage Buck-Boost Inverters [40] Fig. 1.7	250-450	230 / 60 Hz	4	0	4	1 Inductor 1 Transformer	2
Proposed flyback-assisted inverter	210-500	240 / 60 Hz	1	4	5	1 Inductor 1 Transformer	2

A comparison is made between the existing topologies and the proposed flyback-assisted inverter in Table 3.2. It is evident that a reduced count of passive elements is necessitated by this converter, and a broader span of input voltages can be ac-

commodated. Furthermore, unlike the majority of topologies, enhanced efficiency is achieved through the utilization of a blend of low-voltage high-frequency switches and high-voltage low-frequency switches.

3.4 Summery

The flyback-assisted inverter is introduced in this chapter. The new topology is created by incorporating the flyback converter into the configuration of the cascaded full-bridge inverter proposed in the previous chapter. Through this integration, the lower full bridge is empowered to generate a portion of the fundamental voltage essential for expanding the voltage swing range of the PV source. Furthermore, a sophisticated control structure is employed to regulate both the output waveform and the capacitor voltage. Ultimately, the system's performance is validated by presenting simulation results for various input voltages and showcasing the harmonic characteristics of the output waveforms.

Chapter 4

Wide Input Voltage Range Cascaded Full-Bridge Converter with Single Switching Frequency

In section 1.1, various wide input voltage range topologies have been discussed for the purpose of maximum power point tracking (MPPT) of PV modules. However, these topologies are subject to certain limitations. To overcome the challenges encountered by single-stage wide input range inverters, this chapter introduces a novel control strategy applied to a cascaded H-bridge converter.

The proposed topology consists of two H-bridge converters, with one bridge connected to the power source to generate both active and reactive power output, while the other bridge is linked to a capacitor for generating reactive power. Within this configuration, a new control system is implemented, operating in the DQ frame, thereby facilitating precise control of the active and reactive power for each H-bridge. This approach ensures efficient power transfer and enhances the overall performance

of the system.

In addition, the simulation results are provided to demonstrate the system's capability to effectively track the maximum power point of PV modules while successfully addressing the challenges faced by other wide input range inverters. The subsequent sections of this chapter will delve into the detailed circuit configuration and controller design of the proposed cascaded H-bridge converter, elucidating the principles behind the control system in the DQ frame.

4.1 Circuit Configuration

The cascaded multilevel converter topology, as shown in Fig. 4.1, is controlled using a novel approach discussed in this chapter to address the challenges associated with varying input voltages in PV applications. Its main objective is to efficiently track the MPP of the PV system and generate the highest possible power output. The converter achieves this by utilizing two H-bridge converters connected in series, offering enhanced control and flexibility.

In this circuit, having cells with different DC-link voltage lets the converter generate a multilevel output voltage waveform, typically five levels in this case. By providing a high-quality voltage waveform, the converter effectively reduces the presence of harmonics in the output current, thereby minimizing the need for extensive filtering at the output stage. This reduction in harmonics simplifies the design and lowers the cost of the overall system.

The upper H-bridge converter plays a crucial role in the cascaded multilevel converter topology as it serves as the interface between the PV system and the converter, efficiently processing all the active power generated by the PV panels. This section

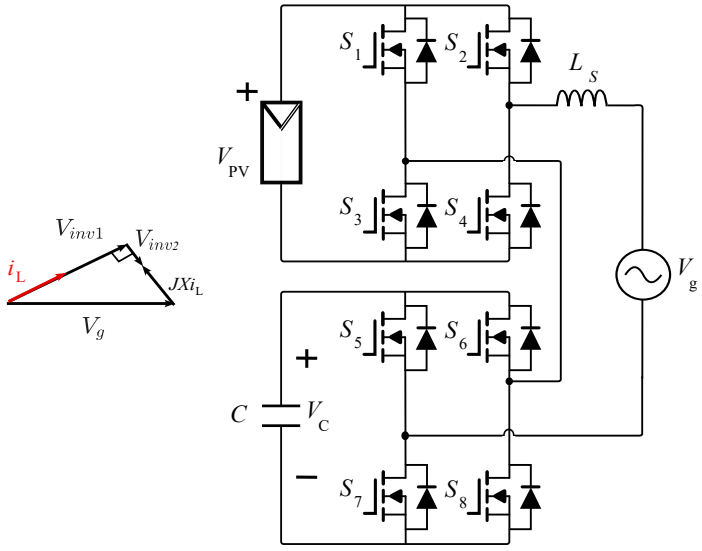


Figure 4.1: Proposed wide input voltage range inverter

of the circuit is responsible for extracting the maximum available power from the PV system by continuously tracking the MPP.

In addition, the lower full bridge converter is connected to a capacitor and produces the required reactive power. This capability allows the voltage of the PV system to swing within a certain range, facilitating the optimal operation of the upper H-bridge converter during MPPT. The voltage across the capacitor is adjusted based on the desired voltage swing of the PV system from its nominal voltage. By incorporating this auxiliary capacitor, the converter effectively expands the operating voltage range of the first inverter, eliminating the need for a separate DC/DC converter to achieve the same result.

For the cascaded multilevel converter to function as intended, a novel control system is necessary. The controller fulfills several crucial objectives. Firstly, it must be capable of precisely controlling the active power of the upper H-bridge converter, enabling it to extract the maximum available power from the PV system under varying

conditions. Secondly, the controller must maintain the voltage of the capacitor in the lower full bridge at a constant reference value, ensuring stable operation of the converter. Additionally, the lower full bridge converter must generate the required reactive power to enable the voltage swing necessary for effective MPPT in the upper H-bridge converter. The detailed analysis and explanation of each component of the control system for the cascaded multilevel converter topology will be discussed in the subsequent sections.

4.2 Control System

The control structure of the system is illustrated in Fig. 4.2. This control structure can be divided into three main sections. The first section is responsible for generating the reference voltage for each full bridge based on the active and reactive power required by the grid. This section ensures that the output voltage of each full bridge is adjusted accordingly to meet the desired power output. By manipulating the reference voltage, the system can control the active and reactive power flow.

The second part of the controller focuses on regulating the voltage of the capacitor in both full bridges. Its primary objective is to maintain a constant voltage of the capacitor at the reference value. This control mechanism ensures that the voltage level remains stable and within the desired range, thereby enhancing the overall performance of the system and allowing the upper full bridge to track the maximum power point (MPP).

Finally, the third part of the controller is responsible for determining the reactive power of each full bridge, as well as the active and reactive power of the grid. This section calculates these parameters based on the desired active power of the full

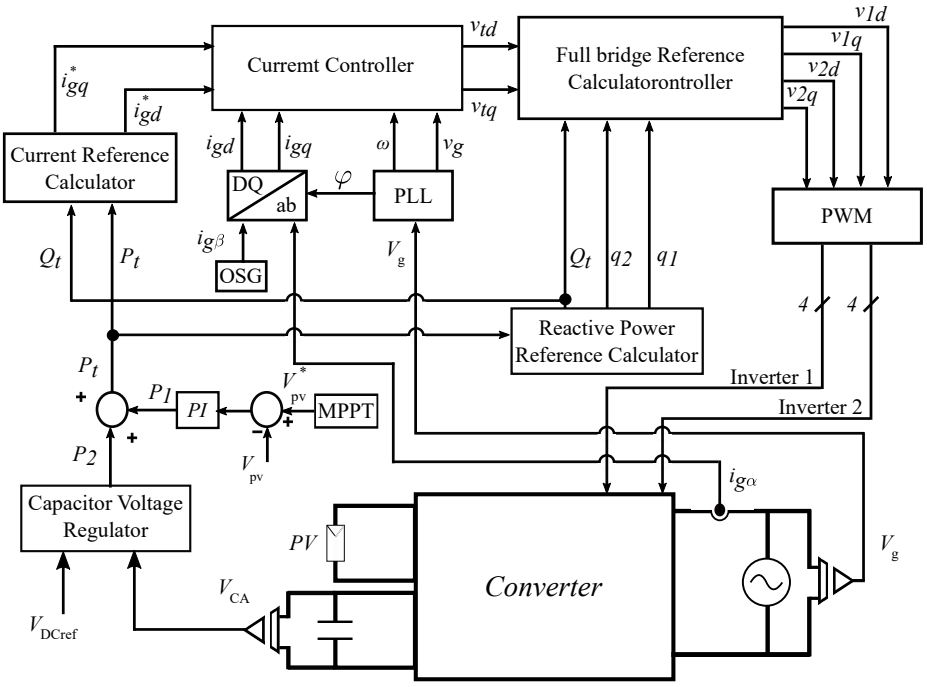


Figure 4.2: Proposed wide input voltage range inverter

bridge connected to the photovoltaic (PV) system. By accurately calculating and monitoring the active and reactive power, this control mechanism allows for efficient power management and coordination between the PV system and the grid.

4.2.1 Real and Reactive Power Controller

The proposed converter is grid-connected, so the frequency of the converter is imposed by the grid. Now, this part of the controller is to generate an appropriate reference for the converter to control the instantaneous real and reactive power that the system exchanges with the grid, that is, $P_S(t)$ and $Q_s(t)$.

There are two primary methods commonly used for controlling $P_S(t)$ and $Q_s(t)$ in grid-connected systems. The first method is known as voltage-mode control. This

approach involves adjusting the phase angle and amplitude of the converter's AC-side terminal voltage in relation to the grid voltage to regulate the real and reactive power. By closely matching the amplitude and phase angle of the converter voltage with the grid voltage, the real and reactive power can be controlled independently. Voltage-mode control is relatively straightforward and requires only a minimal number of control loops. However, it lacks a control loop closed on the converter line current, which can leave the converter susceptible to overcurrent conditions. Consequently, rapid changes in power commands or faults in the AC system can result in significant current fluctuations.

To address the limitations of voltage-mode control, another method, known as current-mode control, is often employed. In current-mode control, a dedicated current-control scheme is utilized to tightly regulate the converter line current through the converter's AC-side terminal voltage. By adjusting the phase angle and amplitude of the converter line current in relation to the grid voltage, the real and reactive power can be controlled. Current-mode control offers several advantages, including protection against overcurrent conditions, robustness against parameter variations in the converter and AC system, superior dynamic performance, and higher control precision.

Considering these advantages, the active and reactive power control for the proposed converter is implemented using current-mode control. The current controller operates in the dq-frame, where the line current components i_d and i_q are controlled to regulate P_s and Q_s. However, since the converter is single-phase, an orthogonal signal generation (OSG) block is necessary to generate the orthogonal component of the grid current in the $\alpha\beta$ frame [42].

In addition to the current controller and OSG block, there is also a need for a block that converts the reference voltage generated by the current controller to the

reference signals for the upper and lower full bridge. This conversion ensures that the converter operates according to the desired power references. In the subsequent section, each of these blocks will be discussed in detail, providing a comprehensive understanding of their functions and operations.

OSG Block

This block is the same as the one that was previously used in the other chapters. The reason for using this block is that the converter is single-phase, and to implement the current controller in the DQ frame, the β-axis component must be created using the OSG block [42]. Similar to what was proposed in section 2.2.3, the β-axis component can be calculated using the following equation:

$$\hat{i}_{g\beta} = -B\cos(\psi + \gamma) \tag{4.1}$$

where ψ is the angle of the $\alpha\beta/DQ$ transformation and:

$$B = \sqrt{I_d^{*2} + I_q^{*2}}, \quad \gamma = \tan^{-1}\left(\frac{I_q^*}{I_d^*}\right) \tag{4.2}$$

Current Control

The current controller currently employed for this converter is the same as the current controllers utilized for the proposed converters in the previous chapter. The diagram of the DQ current controller is depicted in Fig. 2.9. The goal of this converter is to regulate the converter's current to control reactive power and maintain the PV source voltage at the desired reference determined by the MPPT algorithm. This ensures optimal power generation from the PV system.

PI compensators can be used to control the D and Q components of the current separately, as shown in Fig. 2.10. The PI compensator for the D and Q axes will be similar, and their coefficients will be:

$$k_p = \frac{L}{\tau_i} \tag{4.3}$$

$$k_i = \frac{R}{\tau_i} \tag{4.4}$$

Where τ_i represents a time constant of the controller, and a small value should be chosen to achieve a fast current control response. However, it should be sufficiently large so that $\frac{1}{\tau_i}$ (the bandwidth of the closed-loop control system) is considerably smaller than the switching frequency of the converter.

Full Bridge Reference Calculation

As described in the previous section, the reference of the converter is generated using the current controller and OSG block to inject the desired active and reactive power into the grid. However, it's important to note that the output of the current controller is the reference for the entire converter, not for each individual full bridge. This section will discuss how the generated reference voltage by the current controller can be converted into the reference voltage for each full bridge in the DQ (Direct-Quadrature) frame.

Since the two full bridges are connected in series, the same current passes through both of them. Therefore, we can establish the following equation to demonstrate the relationship between the apparent power of each full bridge and the total apparent power:

$$\frac{S_i}{S_t} = \frac{V_i}{V_t} \tag{4.5}$$

This equation can be expressed in the DQ frame as follows:

$$v_{id} + jv_{iq} = \frac{P_i + jQ_i}{P_t + jQ_t}\left(v_{td} + jv_{tq}\right) \tag{4.6}$$

here, P_i and Q_i represent the active and reactive power of the i^{th} full bridge, and P_t and Q_t can be determined using the following equations:

$$P_t = P_1 + P_2 \tag{4.7}$$

$$Q_t = Q_g + Q_L \tag{4.8}$$

here, Q_g and Q_L correspond to the required reactive power for the grid and inductance, respectively.

In Equation (4.6), the values of v_{td} and v_{tq} are the outputs of the current controller block. This equation implies that if the values of the active and reactive power for each full bridge, as well as the reactive power of the grid and inductor, are known, the reference voltage for each full bridge can be calculated. The following section will discuss how these values can be calculated based on the active power of the upper full bridge.

4.2.2 Capacitor Voltage Regulator

As mentioned previously, the lower full bridge plays a crucial role in generating the necessary reactive power to enable the upper full bridge to swing its voltage and track the maximum power point (MPP). In essence, the lower full bridge acts as a STATCOM, and it is essential to control the DC link voltage of this full bridge.

The DC link voltage of the full bridge can be regulated by controlling the active power of the full bridge. By injecting active power into the capacitor, the voltage

of the capacitor increases, and by extracting active power from the capacitor, its voltage decreases. Therefore, to maintain the desired DC bus voltage, a feedback mechanism compares the actual DC bus voltage, denoted as V_{DC}, with a reference command. Based on this comparison, the active power P_2 is adjusted to ensure that the net power exchanged with the DC bus capacitor remains at zero. However, the reactive power Q_2 can be controlled independently. The power balance for the lower full bridge can be formulated as:

$$\left(\frac{C}{2}\right)\frac{dV_{DC}^2}{dt} = P_{loss} - P_2, \tag{4.9}$$

In Equation 4.9, $\frac{dV_{DC}^2}{dt}$ represents the rate of change of V_{DC}^2, P_2 is the control input, and P_{loss} is the disturbance input.

To facilitate control system analysis, the power balance equation can be linearized and simplified. By applying the Laplace transformation to the equation, we can obtain the transfer function $G_v(s) = \frac{\widetilde{V}_{DC}^2(s)}{\widetilde{P}_2(s)}$ as:

$$G_v(s) = \frac{\widetilde{V}_{DC}^2(s)}{\widetilde{P}_2(s)} = -\left(\frac{2}{C}\right)\frac{\tau s + 1}{s}, \tag{4.10}$$

here, $\widetilde{V}_{DC}^2(s)$ and $\widetilde{P}_2(s)$ represent the Laplace transforms of V_{DC}^2 and P_2, respectively. The time constant τ is given by:

$$\tau = \frac{2LP_{2_0}}{3V_{2d}^2}, \tag{4.11}$$

where L is a constant, P_{2_0} is the initial value of P_2, and V_{2d} denotes a specific voltage value.

Fig. 4.3 illustrates a block diagram of the DC bus voltage controller. The controller begins by comparing V_{DC}^2 with the reference value V_{DCref}^2. The resulting error

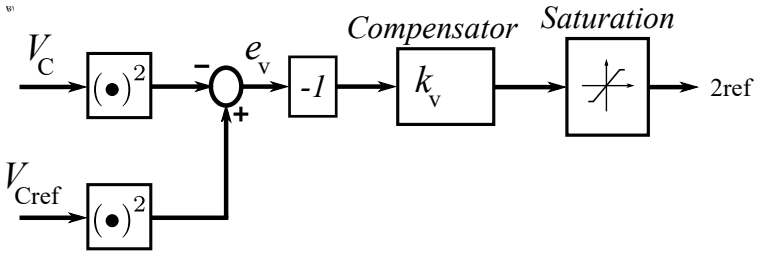


Figure 4.3: DC bus voltage Regulator.

signal is then processed by the compensator $K_v(s)$, which generates the command signal $P_{2_{ref}}$ for the real power controller. The real power controller, in turn, regulates P_2 to the desired value $P_{2_{ref}}$, while independent control over Q_2 is still achievable.

4.2.3 Reactive Power Reference Calculation

This part of the controller is responsible for generating the reference reactive power for each full bridge. These values are determined based on the reference active power for each full bridge. The reference active power for the upper full bridge depends on the PV system and is determined to extract the maximum power from the system. The reference active power for the lower full bridge is determined by the capacitor voltage regulator block to maintain the voltage of the DC link of the full bridge constant at the reference value.

The grid current can be calculated based on the apparent power and voltage of the grid using the following equation:

$$i_g = \frac{P_t + jQ_t}{V_g} \tag{4.12}$$

In this equation, P_t and Q_t represent the total power of the system. Assuming negligible losses in the system, the total active and reactive power can be calculated

using the following equations:

$$P_t = P_1 + P_2 = P_g \tag{4.13}$$

$$Q_t = q_1 + q_2 = Q_g + Q_L \tag{4.14}$$

As mentioned earlier, the active power references of full bridges are determined based on the maximum power point tracking (MPPT) and voltage regulation requirements, so P_t is a known value. Now, Q_t, equivalently q_1 and q_2, need to be determined. The optimal choice of q_1 and q_2 should result in the minimum i_g to minimize losses. Therefore, the goal of this part of the controller is to minimize the grid current. Based on Equation (4.12), since P_t and V_g are constant, Q_t should be minimized.

For each full bridge, the apparent power can be expressed as:

$$|P_i + jQ_i| = |S_i| = |v_i| \cdot |i_i| \tag{4.15}$$

Using this equation, the voltage of each full bridge can be determined based on the apparent power of that full bridge and the voltage and apparent power of the grid:

$$|v_i| = \frac{|S_i|}{|i_i|} = \frac{|S_i|}{\left|\frac{P_t + jQ_t}{v_g}\right|} = \frac{|S_i|}{\left|\frac{S_g}{v_g}\right|} \tag{4.16}$$

Finally, the ratio of the apparent power of each full bridge to the grid is equal to the ratio of the voltage of the full bridge to the grid:

$$\frac{|S_i|}{|S_g|} = \frac{|v_i|}{|v_g|} \tag{4.17}$$

In Equation (4.17), v_i represents the output voltage of the i-th inverter. As known, the output voltage of the full bridge converter is given by:

$$v_i = m_i \times V_{DC} \tag{4.18}$$

where m_i is the reference modulation signal of the full bridge and is between -1 and 1. By substituting Equation (4.17) into Equation (4.18), the following equation is obtained:

$$\frac{|S_i|}{|S_g|} = \frac{|m_i \times V_{DC}|}{|v_g|} = \frac{|m_i| \times |V_{DC}|}{|v_g|} = |m_i| \times \frac{|V_{DC}|}{|v_g|} \tag{4.19}$$

Since the ratio of the DC bus voltage of each converter to the voltage of the grid is constant, if this constant ratio is defined as k_i, and since m_i is between -1 and 1, the ratio of the apparent power should be equal to or less than k_i:

$$\left.\begin{array}{c} \frac{|S_i|}{|S_g|} = |m_i| \times \frac{|V_{DC}|}{|v_g|} \\ \frac{|V_{DC}|}{|v_g|} = k_i \end{array}\right\} \Rightarrow \frac{|S_i|}{|S_g|} \leq k_i \tag{4.20}$$

Using this equation, the maximum reactive power that each full bridge converter can generate or consume can be found as follows:

$$\frac{|S_i|}{|S_g|} \leq k_i \Rightarrow |p_i|^2 + |q_i|^2 \leq (k_i \cdot |S_g|)^2 \tag{4.21}$$

$$|q_i|^2 \leq (k_i \cdot |S_g|)^2 - |p_i|^2 \tag{4.22}$$

$$|q_{i_{\mathrm{Max}}}| = \sqrt{(k_i \cdot |S_g|)^2 - |p_i|^2} \tag{4.23}$$

The total reactive power is equal to the summation of the reactive power of each full bridge, which is equal to the summation of the reactive power of the grid and the inductor, as shown here:

$$\sum_{i=1}^{n} q_i = Q_g + Q_L \tag{4.24}$$

Since the reactive power of each full bridge has a maximum value as mentioned in Equation (4.23), the following equation can be written:

$$|Q_g + Q_L| \leq \sum_{i=1}^{n} \sqrt{(k_i \cdot |S_g|)^2 - |p_i|^2} \tag{4.25}$$

To minimize Q_g, the maximum value of this expression should be minimized. Thus, the value of i_g can be minimized if S_g is found, which minimizes the following value:

$$\sqrt{(k_1 \cdot S_g)^2 - p_1^2} + \sqrt{(k_2 \cdot S_g)^2 - p_2^2} - Q_L \tag{4.26}$$

In conclusion, this part of the controller aims to minimize the grid current by determining the optimal reactive power for each full bridge. This goal can be archived by finding the S_g which minimizes the (4.26). Finally after finding the S_g the value of the q_1 and q_2 can be calculated using the (4.17).

4.3 Simulation results

Simulation results are presented in this section, showcasing the performance and capability of a single switching frequency cascaded full-bridge converter in generating the necessary output waveforms across a broad voltage range of PV systems. In the initial phase, the simulation is executed at the nominal inverter voltage of 400. The waveforms of output voltage, current, the voltage of both full bridge outputs, and capacitor voltage are portrayed in Fig. 4.4. These visual representations indicate the successful generation of the requisite output voltage and current. Fig. 4.5 displays the harmonic spectrum of these waveforms, underscoring the minimal harmonic content of the output waveforms and the converter's proficiency in producing the needed output voltage and current.

Furthermore, simulation outcomes for the minimum attainable voltage (220 V) of the PV source are exhibited in Fig.4.6. As depicted by the diagrams, a high-quality waveform can still be generated at the output by the converter, despite the decline in PV voltage. Fig.4.7 showcases the harmonics of the output waveforms, and once again, the harmonic content using this converter is low, even for the lowest range of PV voltage. The circuit parameters remain uniform for both simulations and are outlined in Table 4.1.

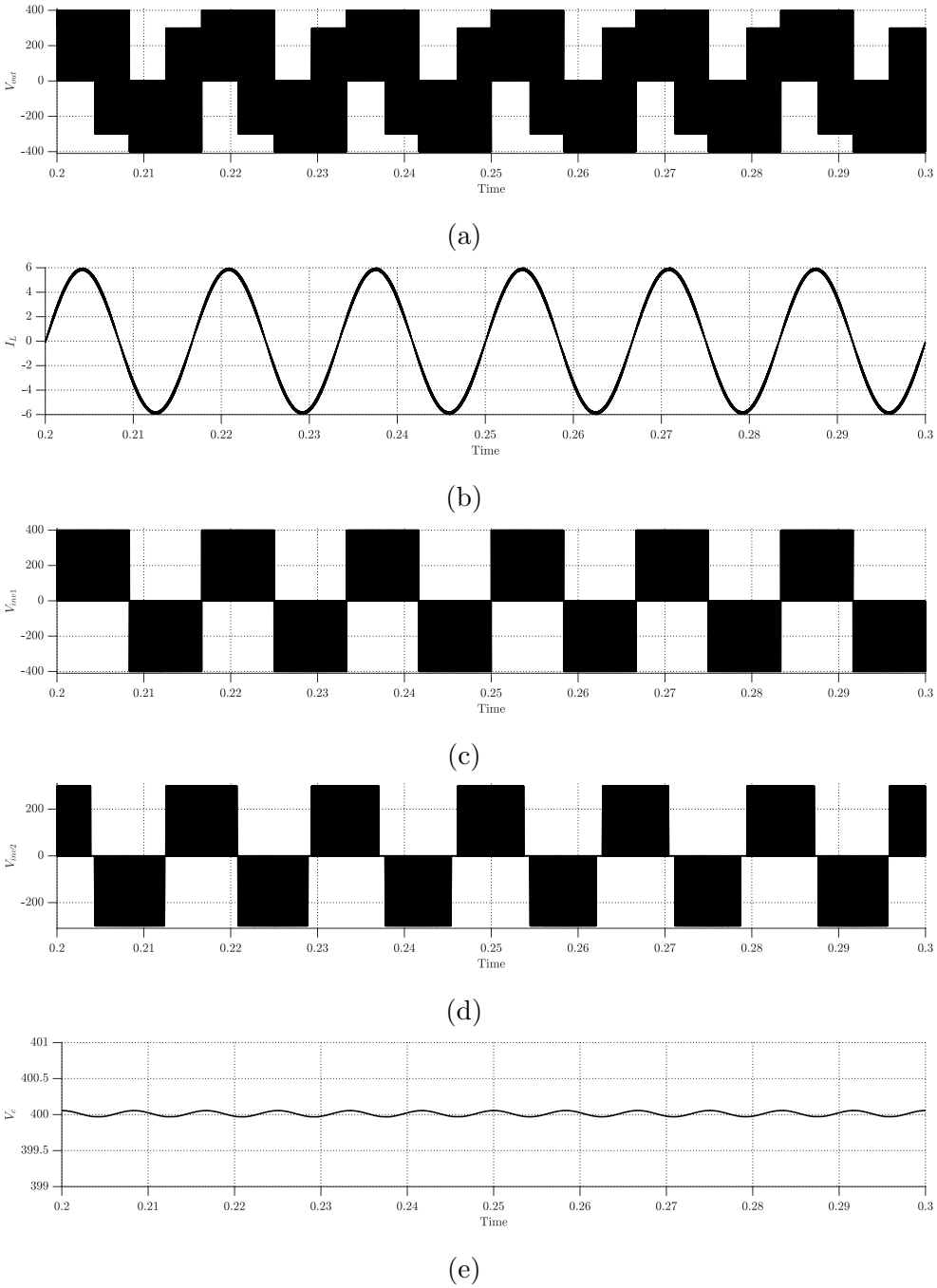
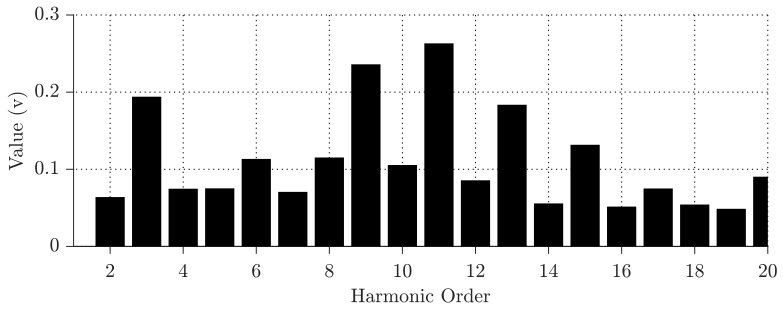
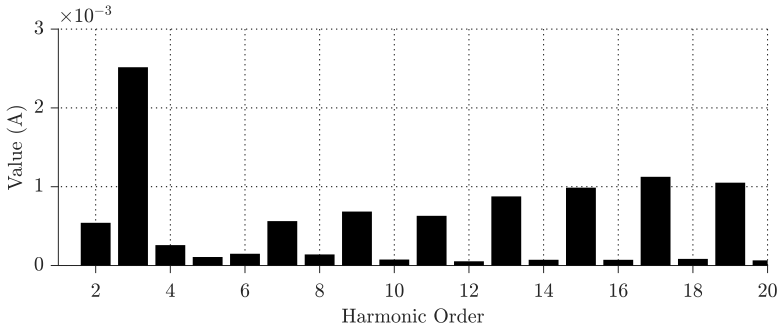


Figure 4.4: Waveforms of cascaded full-bridge converter with single switching frequency ($V_{pv} = 400$): (a) Output voltage of the inverter, (b) Output current, (c) Output voltage of PV connected full bridge, (d) Output voltage of capacitor connected full bridge, (e) Voltage of capacitor.



(a)



(b)

Figure 4.5: Cascaded full-bridge converter with single switching frequency ($V_{pv} = 400$): (a) Harmonic spectrum of the output voltage, (b) Harmonic spectrum of the output current.

Table 4.1: System parameters of the Cascaded full-bridge converter with single switching frequency.

	Parameter	Value
Input voltage	V_{in}	220-500v
Grid voltage	V_g	240v
Filter inductance	L	5mH
Capacitance	C	2.5mF
Switching frequency	f_{s2}	30kHz

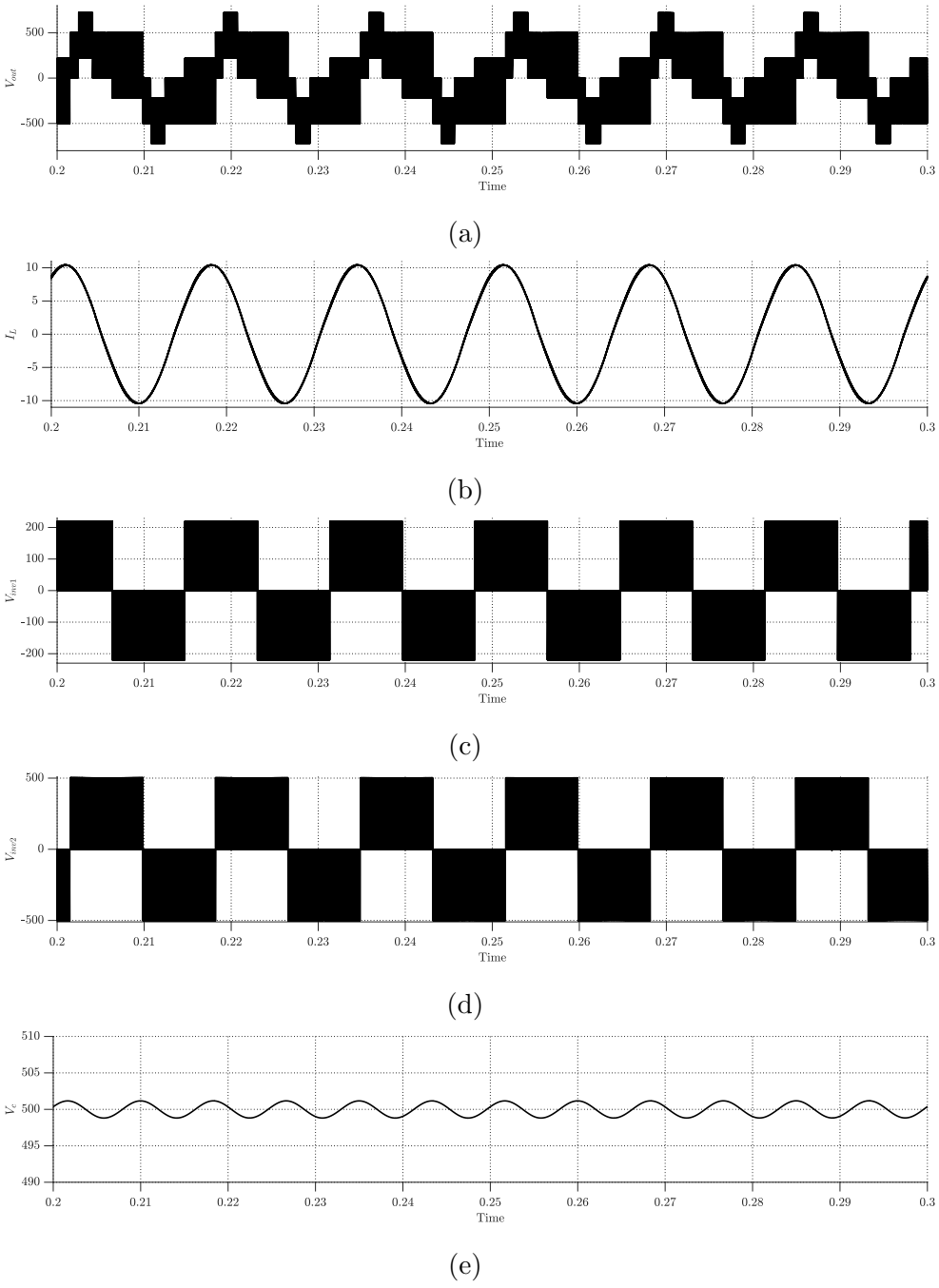
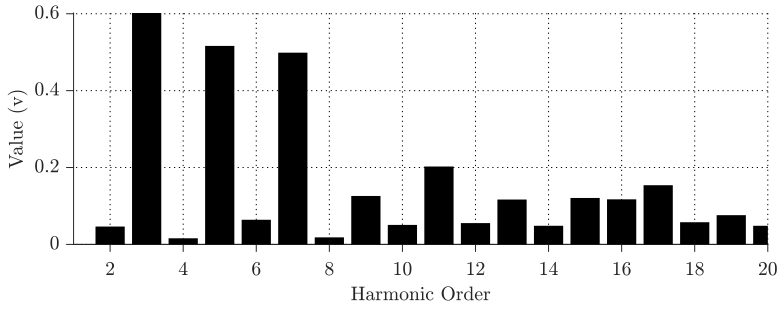
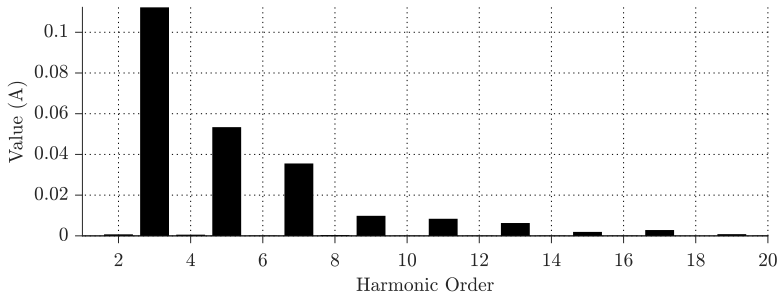


Figure 4.6: Waveforms of cascaded full-bridge converter with single switching frequency ($V_{pv} = 220$): (a) Output voltage of the inverter, (b) Output current, (c) Output voltage of PV connected full bridge, (d) Output voltage of capacitor connected full bridge, (e) Voltage of capacitor.



(a)



(b)

Figure 4.7: Cascaded full-bridge converter with single switching frequency ($V_{pv} = 220$): (a) Harmonic spectrum of the output voltage, (b) Harmonic spectrum of the output current.

A thorough comparison has been conducted between the current topologies and the proposed cascaded full-bridge converter using a single switching frequency, as depicted in Table 4.2. It is evident that this converter necessitates fewer passive components, resulting in a greater power density for the converter. Moreover, this converter demonstrates the ability to handle a wider range of input voltages, thus significantly improving its suitability for implementation in PV systems.

Table 4.2: Summary of Various Inverter Topologies

Topology	Input voltage range	Vg	No. of HVHF switches	No. of LVHF switches	No. of HVLF switches	No. of inductors	No. of capacitors
Half-Bridge Voltage Swing Inverter [3] Fig. 1.1	NA	120 / 60 Hz	5	0	1	4	5
The Z-source and quasi-Z-source inverters [21] & [22] Fig. 1.2	NA	NA	5	0	0	3-4	4-5
Two mode inverter [19] Fig. 1.3	220-420	230 / 50 Hz	9	0	1	2	2
Dual-Buck-Structured Buck-Boost Inverters [34] Fig. 1.5	70-200	155 / 60 Hz	4	0	4	6	4
Single-Stage Buck-Boost Inverters [40] Fig. 1.7	250-450	230 / 60 Hz	4	0	4	1 Inductor 1 Transformer	2
Proposed cascaded full-bridge converter with single switching frequency	220-500	240 / 60 Hz	8	0	0	1	2

4.4 Summery

This chapter proposes a cascaded full-bridge converter with a single switching frequency. It utilizes a new control algorithm to independently regulate the power of each full bridge, aiming to achieve desired output waveforms. This converter is capable of operating across a wide range of input voltages, comparable to the converter introduced in the previous chapter. However, the number of components is reduced to achieve a higher power density. Finally, simulation results are provided for both the nominal voltage of the inverter and the lowest operating voltage of the inverter. These results demonstrate the converter's ability to operate within these voltage ranges and generate the desired waveforms.

Chapter 5

Summary and Future Work

5.1 Summary of Contributions

This thesis proposes four new extended input voltage range inverters for PV systems. These inverters enable the voltage of the PV system to vary to track their Maximum Power Point (MPP). The main contributions of these new topologies and the conclusions of this thesis are summarized below.

(i) Two new hybrid cascaded topologies capable of operating within wide input voltage ranges are proposed in the second chapter. The efficiency of these inverters is improved by operating the PV-connected converter at a low frequency and high voltage, and the capacitor-connected full bridge at a high frequency and low voltage. Additionally, a DQ current controller for this single-phase inverter is implemented, allowing the converter to track the Maximum Power Point (MPP). Finally, the active filtering implemented using the lower full bridge results in output waveforms with low harmonics.

(ii) A Flyback-associated converter is then proposed to further increase the input voltage range of the converter, allowing the PV voltage to swing within a wider range. This goal is achieved by incorporating a flyback converter that enables the lower full bridge to generate 25% of the output fundamental voltage in addition to its task of harmonics removal. The sophisticated DQ current controller is once again employed for this single-phase inverter to enable MPP tracking. Furthermore, the controller calculates the required modulation angle of the PV-connected full bridge to generate the necessary fundamental voltage. Lastly, voltage control of the capacitor connected to the lower full bridge is managed by either the full bridge itself or the flyback, depending on the circuit's conditions.

(iii) In Chapter Four, a cascaded full-bridge converter with a single switching frequency is proposed. This converter is capable of operating across a wide voltage range while utilizing a lower number of components, leading to a higher power density of the topology. To achieve this objective, a new control scheme is implemented, allowing independent power control for each full bridge. With the application of this control scheme, the output waveforms have low harmonics.

(iv) The proposed converters have fewer passive components compared to the existing topologies, primarily due to the active filtering within the system. Furthermore, the converters do not require stored energy to operate across a wide range of input voltages. These factors contribute to a reduction in cost and an increase in power density.

(v) Accurate control of each converter is achieved by utilizing sophisticated control mechanisms for each of them. All the converters are equipped with a current controller in the DQ frame to enable them to track the MPP. Additionally, each converter includes other components, such as the capacitor voltage regulator,

modulation angle calculator, and full bridge reference calculator, which allow it to operate as intended.

5.2 Suggested Future Work

There are several directions that this research can be taken to; some of the most promising ones are suggested as follows:

(i) This thesis introduced new wide-input voltage range inverters for PV systems. For the subsequent stage of research, it is suggested to explore the replacement of capacitors in the topologies with battery storage and conduct a study regarding the connection of the inverter to Islanded Loads.

(ii) All the topologies proposed in this thesis are single-phase inverters. As a logical progression, investigating the extension of these topologies to three-phase systems could be a valuable avenue for future research.

(iii) In the T-type converter, α is considered constant, and β is utilized as a controller to adjust the fundamental output voltage. In the next phase of research, optimization can be conducted to determine the optimal values for each of these parameters, aiming to minimize the required capacitor voltage and further reduce the blocking voltage across the switches in the full bridge.

Bibliography

[1] X. Chen and Z. Zhang, "Two-Mode Controlled Single/Dual-Input DC–AC Inverter With Wide-Range DC Input," IEEE Transactions on Power Electronics, vol. 36, no. 5, pp. 5664–5673, May 2021, doi: 10.1109/TPEL.2020.3027244.

[2] Q. Huang, A. Q. Huang, R. Yu, P. Liu, and W. Yu, "High-Efficiency and High-Density Single-Phase Dual-Mode Cascaded Buck–Boost Multilevel Transformerless PV Inverter With GaN AC Switches," IEEE Transactions on Power Electronics, vol. 34, no. 8, pp. 7474–7488, Aug. 2019, doi: 10.1109/TPEL.2018.2878586.

[3] J. Roy, Y. Xia, and R. Ayyanar, "Half-Bridge Voltage Swing Inverter With Active Power Decoupling for Single-Phase PV Systems Supporting Wide Power Factor Range," IEEE Transactions on Power Electronics, vol. 34, no. 8, pp. 7450–7461, Aug. 2019, doi: 10.1109/TPEL.2018.2877652.

[4] E. Sener, G. Ertasgin, and I. Yazar, "Implementation of a Single-Phase Half-Bridge Grid-Connected PV Inverter," in 2021 5th International Symposium on Multidisciplinary Studies and Innovative Technologies (ISMSIT), Oct. 2021, pp. 510–515. doi: 10.1109/ISMSIT52890.2021.9604581.

[5] C. N. M. Ho and K. K. M. Siu, "Manitoba Inverter—Single-Phase Single-Stage Buck-Boost VSI Topology," IEEE Transactions on Power Electronics, vol. 34, no. 4, pp. 3445–3456, Apr. 2019, doi: 10.1109/TPEL.2018.2855560.

[6] W. Wu, J. Ji, and F. Blaabjerg, "Aalborg Inverter - A New Type of 'Buck in Buck, Boost in Boost' Grid-Tied Inverter," IEEE Transactions on Power Electronics, vol. 30, no. 9, pp. 4784–4793, Sep. 2015, doi: 10.1109/TPEL.2014.2363566.

[7] S. Dhara and V. T. Somasekhar, "An Integrated Semi-Double Stage-Based Multilevel Inverter With Voltage Boosting Scheme for Photovoltaic Systems," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 3, pp. 2326–2339, Sep. 2020, doi: 10.1109/JESTPE.2019.2955729.

[8] Y. P. Siwakoti and F. Blaabjerg, "Common-Ground-Type Transformerless Inverters for Single-Phase Solar Photovoltaic Systems," IEEE Transactions on Industrial Electronics, vol. 65, no. 3, pp. 2100–2111, Mar. 2018, doi: 10.1109/TIE.2017.2740821.

[9] "A new single-stage continuous input current-based high gain boost inverter: Analysis and implementation - Shaw - 2021 - International Journal of Circuit Theory and Applications - Wiley Online Library." https://onlinelibrary-wiley-com.login.ezproxy.library.ualberta.ca/doi/full/10.1002/cta.2931 (accessed Aug. 06, 2023).

[10] J. Roy, Y. Xia, and R. Ayyanar, "Half-Bridge Voltage Swing Inverter With Active Power Decoupling for Single-Phase PV Systems Supporting Wide Power Factor Range," IEEE Transactions on Power Electronics, vol. 34, no. 8, pp. 7450–7461, Aug. 2019, doi: 10.1109/TPEL.2018.2877652.

[11] M. Tofigh Azary, M. Sabahi, E. Babaei, and F. Abbasi Aghdam Meinagh, "Modified Single-Phase Single-Stage Grid-Tied Flying Inductor Inverter With MPPT and Suppressed Leakage Current," IEEE Transactions on Industrial Electronics, vol. 65, no. 1, pp. 221–231, Jan. 2018, doi: 10.1109/TIE.2017.2719610.

[12] Y. Liu et al., "Single-Phase Inverter With Wide Input Voltage and Power Decoupling Capability," IEEE Access, vol. 7, pp. 16870–16879, 2019, doi: 10.1109/ACCESS.2019.2895350.

[13] S. Xu, L. Chang, and R. Shao, "Single-Phase Voltage Source Inverter With Voltage Boosting and Power Decoupling Capabilities," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 3, pp. 2977–2988, Sep. 2020, doi: 10.1109/JESTPE.2019.2936136.

[14] A. Kumar and P. Sensarma, "A Four-Switch Single-Stage Single-Phase Buck–Boost Inverter," IEEE Transactions on Power Electronics, vol. 32, no. 7, pp. 5282–5292, Jul. 2017, doi: 10.1109/TPEL.2016.2605150.

[15] C.-M. Wang, "A novel single-stage series-resonant buck-boost inverter," IEEE Transactions on Industrial Electronics, vol. 52, no. 4, pp. 1099–1108, Aug. 2005, doi: 10.1109/TIE.2005.851642.

[16] F. S. Kang, S. Cho, S. J. Park, C. U. Kim, and T. Ise, "A new control scheme of a cascaded transformer type multilevel PWM inverter for a residential photovoltaic power conditioning system," Solar Energy, vol. 78, no. 6, pp. 727–738, 2005.

[17] A. Anurag, N. Deshmukh, A. Maguluri, and S. Anand, "Integrated DC–DC Converter Based Grid-Connected Transformerless Photovoltaic Inverter With Extended Input Voltage Range," IEEE Transactions on Power Electronics, vol. 33, no. 10, pp. 8322–8330, Oct. 2018, doi: 10.1109/TPEL.2017.2779144.

[18] A. A. Khan and H. Cha, "Dual-Buck-Structured High-Reliability and High-Efficiency Single-Stage Buck–Boost Inverters," IEEE Transactions on Industrial Electronics, vol. 65, no. 4, pp. 3176–3187, Apr. 2018, doi: 10.1109/TIE.2017.2752145.

[19] A. Pourfaraj, M. Monfared, and H. Heydari-doostabad, "Single-Phase Dual-Mode Interleaved Multilevel Inverter for PV Applications," IEEE Transactions on Industrial Electronics, vol. 67, no. 4, pp. 2905–2915, Apr. 2020, doi: 10.1109/TIE.2019.2910041.

[20] A. Ali Khan, S. Ahmad, and U. Ali Khan, "Design of a Non-Isolated Three-Switch Inverter for Renewable Energy Systems, Featuring Simple Circuit, Continuous Output Current, Common Ground and Buck-Boost Operation," in 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Oct. 2020, pp. 1861–1866. doi: 10.1109/ECCE44975.2020.9235793.

[21] J. Anderson and F. Z. Peng, "Four quasi-Z-Source inverters," in 2008 IEEE Power Electronics Specialists Conference, Jun. 2008, pp. 2743–2749. doi: 10.1109/PESC.2008.4592360.

[22] V. Jagan, J. Kotturu, and S. Das, "Enhanced-Boost Quasi-Z-Source Inverters With Two-Switched Impedance Networks," IEEE Transactions on Industrial Electronics, vol. 64, no. 9, pp. 6885–6897, Sep. 2017, doi: 10.1109/TIE.2017.2688964.

[23] Y. Gu, Y. Chen, and B. Zhang, "Enhanced-Boost Quasi-Z-Source Inverter With an Active Switched Z-Network," IEEE Transactions on Industrial Electronics, vol. 65, no. 10, pp. 8372–8381, Oct. 2018, doi: 10.1109/TIE.2017.2786214.

[24] X. Zhu, B. Zhang, and D. Qiu, "A High Boost Active Switched Quasi-Z-Source Inverter With Low Input Current Ripple," IEEE Transactions on Industrial Informatics, vol. 15, no. 9, pp. 5341–5354, Sep. 2019, doi: 10.1109/TII.2019.2899937.

[25] X. Chen and Z. Zhang, "Two-Mode Controlled Single/Dual-Input DC–AC In-

verter With Wide-Range DC Input," IEEE Transactions on Power Electronics, vol. 36, no. 5, pp. 5664–5673, May 2021, doi: 10.1109/TPEL.2020.3027244.

[26] M. N. H. Khan, M. Forouzesh, Y. P. Siwakoti, L. Li, T. Kerekes, and F. Blaabjerg, "Transformerless Inverter Topologies for Single-Phase Photovoltaic Systems: A Comparative Review," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 805–835, Mar. 2020, doi: 10.1109/JESTPE.2019.2908672.

[27] A. A. Khan et al., "Coupled-Inductor Buck–Boost Inverter With Reduced Current Ripple," IEEE Transactions on Power Electronics, vol. 35, no. 8, pp. 7933–7946, Aug. 2020, doi: 10.1109/TPEL.2019.2962668.

[28] M. Chen, C. Yin, and P. C. Loh, "Coupled-Inductor-Based Differential Boost Inverter with Wide Input Voltage Range for Photovoltaic Generation Applications," in IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, Oct. 2019, pp. 4393–4398. doi: 10.1109/IECON.2019.8927507.

[29] A. A. Khan, Y. W. Lu, W. Eberle, L. Wang, U. A. Khan, and H. Cha, "Single-Phase Split-Inductor Differential Boost Inverters," IEEE Transactions on Power Electronics, vol. 35, no. 1, pp. 107–120, Jan. 2020, doi: 10.1109/TPEL.2019.2913750.

[30] U. A. Khan and J.-W. Park, "Full-Bridge Single-Inductor-Based Buck–Boost Inverters," IEEE Transactions on Power Electronics, vol. 36, no. 2, pp. 1909–1920, Feb. 2021, doi: 10.1109/TPEL.2020.3011462.

[31] A. A. Khan, Y. W. Lu, U. A. Khan, L. Wang, W. Eberle, and M. Agamy, "Novel Transformerless Buck–Boost Inverters Without Leakage Current," IEEE Transactions on Industrial Electronics, vol. 67, no. 12, pp. 10442–10454, Dec. 2020, doi: 10.1109/TIE.2019.2962478.

[32] M. Lee, J.-W. Kim, and J.-S. Lai, "Single inductor dual buck-boost inverter based on half-cycle PWM scheme with active clamping devices," IET Power Electronics, vol. 12, no. 5, pp. 1011–1020, 2019, doi: 10.1049/iet-pel.2018.5776.

[33] A. A. Khan et al., "Single-Stage Bidirectional Buck–Boost Inverters Using a Single Inductor and Eliminating the Common-Mode Leakage Current," IEEE Transactions on Power Electronics, vol. 35, no. 2, pp. 1269–1281, Feb. 2020, doi: 10.1109/TPEL.2019.2918349.

[34] A. A. Khan and H. Cha, "Dual-Buck-Structured High-Reliability and High-Efficiency Single-Stage Buck–Boost Inverters," IEEE Transactions on Industrial Electronics, vol. 65, no. 4, pp. 3176–3187, Apr. 2018, doi: 10.1109/TIE.2017.2752145.

[35] O. Husev, O. Matiushkin, C. Roncero-Clemente, F. Blaabjerg, and D. Vinnikov, "Novel Family of Single-Stage Buck–Boost Inverters Based on Unfolding Circuit," IEEE Transactions on Power Electronics, vol. 34, no. 8, pp. 7662–7676, Aug. 2019, doi: 10.1109/TPEL.2018.2879776.

[36] F. Akbar, H. Cha, and D.-T. Do, "CSI7: Novel Three-Phase Current-Source Inverter With Improved Reliability," IEEE Transactions on Power Electronics, vol. 36, no. 8, pp. 9170–9182, Aug. 2021, doi: 10.1109/TPEL.2021.3053132.

[37] A. A. Khan, Y. W. Lu, W. Eberle, L. Wang, U. A. Khan, and H. Cha, "Single-Phase Split-Inductor Differential Boost Inverters," IEEE Transactions on Power Electronics, vol. 35, no. 1, pp. 107–120, Jan. 2020, doi: 10.1109/TPEL.2019.2913750.

[38] Z. Yao, "Review of Dual-Buck-Type Single-Phase Grid-Connected Inverters," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 4, pp. 4533–4545, Aug. 2021, doi: 10.1109/JESTPE.2020.3027770.

[39] A. A. Khan, Y. W. Lu, U. A. Khan, L. Wang, W. Eberle, and M. Agamy, "Novel Transformerless Buck–Boost Inverters Without Leakage Current," IEEE Transactions on Industrial Electronics, vol. 67, no. 12, pp. 10442–10454, Dec. 2020, doi: 10.1109/TIE.2019.2962478.

[40] O. Husev, O. Matiushkin, C. Roncero-Clemente, F. Blaabjerg, and D. Vinnikov, "Novel Family of Single-Stage Buck–Boost Inverters Based on Unfolding Circuit," IEEE Transactions on Power Electronics, vol. 34, no. 8, pp. 7662–7676, Aug. 2019, doi: 10.1109/TPEL.2018.2879776.

[41] U. A. Khan and J.-W. Park, "Full-Bridge Single-Inductor-Based Buck–Boost Inverters," IEEE Transactions on Power Electronics, vol. 36, no. 2, pp. 1909–1920, Feb. 2021, doi: 10.1109/TPEL.2020.3011462.

[42] M. Ebrahimi, S. A. Khajehoddin, and M. Karimi-Ghartemani, "Fast and Robust Single-Phase DQ Current Controller for Smart Inverter Applications," IEEE Transactions on Power Electronics, vol. 31, no. 5, pp. 3968–3976, May 2016, doi: 10.1109/TPEL.2015.2474696

[43] A. A. Khan, Y. W. Lu, W. Eberle, L. Wang, U. A. Khan, and H. Cha, "Single-Phase Split-Inductor Differential Boost Inverters," IEEE Transactions on Power Electronics, vol. 35, no. 1, pp. 107–120, Jan. 2020, doi: 10.1109/TPEL.2019.2913750.

[44] M. S. Manoharan, A. Ahmed, and J.-H. Park, "A Flyback-Assisted Single-Sourced Photovoltaic Power Conditioning System Using an Asymmetric Cascaded Multilevel Inverter," Journal of Power Electronics, vol. 16, no. 6, pp. 2272–2283, Nov. 2016, doi: 10.6113/JPE.2016.16.6.2272.

[45] M. S. Manoharan, A. Ahmed, and J.-H. Park, "A PV Power Conditioning System Using Nonregenerative Single-Sourced Trinary Asymmetric Multilevel

Inverter With Hybrid Control Scheme and Reduced Leakage Current," IEEE Transactions on Power Electronics, vol. 32, no. 10, pp. 7602–7614, Oct. 2017, doi: 10.1109/TPEL.2016.2632864.

[46] A. Ahmed, M. Sundar Manoharan, and J.-H. Park, "An Efficient Single-Sourced Asymmetrical Cascaded Multilevel Inverter With Reduced Leakage Current Suitable for Single-Stage PV Systems," IEEE Transactions on Energy Conversion, vol. 34, no. 1, pp. 211–220, Mar. 2019, doi: 10.1109/TEC.2018.2874076.

[47] M. S. Manoharan, A. Ahmed, and J.-H. Park, "An Improved Model Predictive Controller for 27-Level Asymmetric Cascaded Inverter Applicable in High-Power PV Grid-Connected Systems," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 4, pp. 4395–4405, Dec. 2020, doi: 10.1109/JESTPE.2019.2935536.

[48] M. S. Manoharan, A. Ahmed, and J.-H. Park, "Modeling and Bifurcation Analysis for Photovoltaic Single-Sourced Trinary Inverter With Auxiliary Floating Capacitors Controlled by Finite-Control-Set Model Predictive Control," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 4, pp. 5002–5015, Aug. 2021, doi: 10.1109/JESTPE.2020.3036068.

[49] R. O. Caceres and I. Barbi, "A boost DC-AC converter: analysis, design, and experimentation," IEEE Transactions on Power Electronics, vol. 14, no. 1, pp. 134–141, Jan. 1999, doi: 10.1109/63.737601.

[50] Y. Tang, Y. Bai, J. Kan, and F. Xu, "Improved Dual Boost Inverter With Half Cycle Modulation," IEEE Transactions on Power Electronics, vol. 32, no. 10, pp. 7543–7552, Oct. 2017, doi: 10.1109/TPEL.2016.2592979.

[51] S. Jain and V. Agarwal, "A Single-Stage Grid Connected Inverter Topology for Solar PV Systems With Maximum Power Point Tracking," IEEE Trans-

actions on Power Electronics, vol. 22, no. 5, pp. 1928–1940, Sep. 2007, doi: 10.1109/TPEL.2007.904202.

[52] Y. Liu et al., "Bimodal Transformerless Inverter With Three Switches," IEEE Transactions on Industrial Electronics, vol. 69, no. 9, pp. 8972–8983, Sep. 2022, doi: 10.1109/TIE.2021.3114718.

[53] F. Akbar, H. Cha, S. Lee, and T.-T. Nguyen, "A Single-Phase Transformerless Buck-Boost Inverter for Standalone and Grid-Tied Applications with Reduced Magnetic Volume," in 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia), May 2019, pp. 1071–1077. doi: 10.23919/ICPE2019-ECCEAsia42246.2019.8797203.

Appendix A

Loss and Cost Comparison of IGBT and MOSFET in High Voltage Low Frequency Applications

In this thesis, high voltage low-frequency full bridges and T-type converters are built using IGBTs. Here, it is explained why using IGBTs instead of MOSFETs for these applications can result in reducing losses and the overall construction cost of the converter.

The converters proposed in this thesis will typically be used for small-scale applications in PV systems, approximately around $1kW$. In addition, these converters can operate until the PV voltage equals $500v$. Therefore, in choosing the switches, a blocking voltage of $600v$ is required to provide a 20% safety margin, and since the grid voltage in this application is $240v$, the current rating of the chosen switches should

be around $5A$. Based on these requirements, IGBTs and MOSFETs are selected, and the losses for each one are calculated in the following section.

A.1 Loss Calculation for MOSFET

The switching loss of the MOSFET can be divided into four main parts: conduction loss, crossover loss, gate loss, and output capacitance losses. The conduction loss is due to the resistive behavior of the switch when it is on. Gate loss and output capacitance losses occur due to the discharging of the MOSFET's capacitors in the semiconductor channel during switching. Crossover loss refers to the power dissipation that occurs during the transition period when a MOSFET is switching from the ON state to the OFF state or vice versa. During this transition, both voltage and current are not at their ideal levels, leading to power losses in the form of heat. The equation for calculating the total loss is as follows:

$$P_{loss} = P_{\text{Coss}} + P_{\text{gate}} + P_{\text{cond}} + P_{CO} \tag{A.1}$$

where:

$$P_{\text{Coss}} = \frac{1}{2}\text{C}_{\text{oss}} v_{\text{in}}^2 f_{sw} \tag{A.2}$$

$$P_{\text{gate}} = V_{gs} Q_g f_{sw} \tag{A.3}$$

$$P_{\text{cond}} = R_{\text{DSon}} I_{\text{rms}}^2 \tag{A.4}$$

$$P_{CO} = \frac{1}{2} I_{D(\text{on})} V_{DD} f_{SW} \frac{Q_{GS2} + Q_{GD}}{I_{\text{Driver}(H-L)}} + \frac{1}{2} I_{D(off)} V_{DD} f_{SW} \frac{Q_{GS2} + Q_{GD}}{I_{D\text{river}(L-H)}} \tag{A.5}$$

In (A.5), the value $I_{\text{Driver}(H-L)}$, $I_{D\text{river}(L-H)}$, and Q_{GS2} can be calculated using the following equations:

$$I_{\text{Driver}(L-H)} = \frac{V_{Dr} - (v_{th} + I_0/g)}{R_g} \tag{A.6}$$

$$I_{\text{Driver}(H-L)} = \frac{(V_{th} + I_0 g)}{R_g} \tag{A.7}$$

$$Q_{GS2} \cong 0.5 Q_{GS} \tag{A.8}$$

As mentioned earlier, based on the operating conditions of the converter, there is a need for switches with a blocking voltage of 600V and a current rating of 5A. Therefore, the IPA60R360CFD7 MOSFET is chosen for this application. The parameters of this switch used in the calculation of the switching loss, as per the datasheet, are listed in Table. A.1. Using these parameters, the losses of this MOSFET can be calculated as follows:

$$\begin{aligned} P_{\text{Coss}} &= 8.25 \times 10^{-5} w, \quad P_{\text{gate}} = 8.4 \times 10^{-6} w \\ P_{\text{cond}} &= 3.87 w, \quad P_{CO} = 3.15 \times 10^{-3} w \end{aligned} \tag{A.9}$$

So, the total power loss of this MOSFET is:

$$P_{loss\_MOSFET} = 3.9 w \tag{A.10}$$

Table A.1: Parameters of the IPA60R360CFD7 MOSFET.

Parameter	Q_{GS}	Q_{GD}	V_{th}	g	R_g	C_{oss}	Q_g	R_{DSon}	V_{gs}
Value	4nC	4nC	4V	10	11.6Ω	11pF	14nC	0.48Ω	10V

A.2 Loss Calculation for IGBT

The switching loss of the IGBT can be divided into two main parts: switching loss and conduction loss. Conduction loss occurs when the IGBT is in its on state, leading to resistive behavior that results in power dissipation. This loss is a consequence of

the voltage drop across the IGBT and the current flowing through it, generating heat in the process. On the other hand, switching loss is incurred during the transition between on and off states, primarily due to the time it takes for the device to change states. During this transition, there is a period when both voltage and current are simultaneously high, leading to a brief but significant spike in power dissipation. The following equations show how to calculate these losses:

$$P_{loss} = P_{cond} + P_{sw} \tag{A.11}$$

$$P_{\text{cond}} = V_{ce0} \cdot I_{c,avg} + r_c \cdot I_{c,rms}^2 \tag{A.12}$$

$$P_{sw} = (E_{on,t} + E_{off,t}) \cdot \frac{V_{DC}}{V_{DC,test}} \cdot \frac{I_{\text{peak}}}{I_{I,test}} \cdot f_{sw} \tag{A.13}$$

Once more, considering the operating requirements of the converter, it is necessary to have switches capable of handling a blocking voltage of $600V$ and a current rating of $5A$. Consequently, the IKD03N60RFA IGBT has been selected for this application. The parameters of this switch used in the calculation of the switching loss, as per the datasheet, are listed in Table. A.2. Using these parameters, the losses of this IGBT can be calculated as follows:

$$P_{\text{cond}} = 2.24w, \quad P_{sw} = 9.5 \times 10^{-3}w \tag{A.14}$$

So, the total power loss of this IGBT is:

$$P_{los\_IGBT} = 2.25w \tag{A.15}$$

Table A.2: Parameters of the IKD03N60RFA IGBT.

Parameter	r_c	$E_{on,t}$	$E_{off,t}$	$V_{DC,test}$	$I_{I,test}$
Value	0.28Ω	0.05mJ	0.04mJ	400v	4A

A.3 Comparison

Table. A.3 summarizes the cost and loss for each selected switch. As can be seen from the results, the IGBT has lower losses and costs in comparison to the MOSFET for high voltage operation and low switching frequency. This result establishes the IGBT as the better choice for integration into the proposed converters in this thesis. Its advantageous combination of reduced loss and lower cost makes it an optimal selection to achieve the project's objectives.

Table A.3: Comparison of IGBT and MOSFET for high voltage operation and low switching frequency.

	P_{Loss}	$Cost$
MOSFET (IPA60R360CFD7)	3.9w	\$4.05
IGBT (IKD03N60RFA)	2.25w	\$1.6