Analysis, Design and Implementation of Efficient High Frequency Power Converters for PV Applications using Generalized Steady-state Modeling

by

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Abstract

Efficiency and power density of Power Electronics converters has been constantly increased for decades and is projected to further improve. As an example, the efficiency for converters used in telecommunication and PV applications has increased from around 90% in 1990s to about 98% in recent years which has also contributed to the increase of converter power density. Efficiency and power density improvements can be achieved by proper design of power converters. However, existing approaches for converter design are mainly based on inaccurate or numerical analysis methods which fail to render a systematic and optimal design tool. Generally, design of a power converter includes suitable topology adoption, circuit parameters selection, component selection, etc., which are imposed by the Steady-state model of the converter. Steady-state models of power converters that provide accurate closed-form expressions for converter waveforms are extremely valuable for converter design. An obstacle in the development of such models is the inherent non-linearity of switching power converters. This thesis presents a systematic procedure to model a broad class of power converters using ordinary differential equations (ODEs) with periodic and discontinuous inputs, and provides an approach to determine closed-form expressions for their steady-state waveforms. The presented Laplace Based Steady-state Modeling (LBSM), serves as an effective analysis and design tool for power converters. The value of LBSM is demonstrated by using it to obtain closed-form expressions for the steady-state waveforms of different types of converters. In particular, two commonly used topologies for PV micro-inverters the series resonant converter and the phase-shift converter are analyzed and compared using LBSM and their optimum operating conditions and applications are discussed. The converter waveforms, soft switching ranges and other characteristics obtained using LBSM are also validated through simulations and experiments.

A specific category of power converters are the PV converters which require improved system level energy yield in addition to converter level efficiency and power density. The system level energy yield considerations imposes the use of PV Module Integrated Converters (MIC) with high efficiency around their unity conversion ratio. Partial Power Processing (PPP) concept is a potential solution for MICs as it improve the efficiency around the unity conversion ratio however, partial power converters inherently have limited Maximum Power Point Tracking (MPPT) range. In this thesis, the challenge

of limited MPPT range for partial power converters has been overcome by utilizing a proposed topology and Pulse Density Modulation (PDM) technique which modulates converter's mode of operation. The converter operation is toggled among three highly efficient conversion modes called as Pass-through, Bypass and Process modes. The proposed topology achieves high efficiencies for Pass-through and Bypass modes by limiting the switching actions while it gets high efficiencies even under Process mode with appropriate utilization of converter parasitic elements to achieve soft-switching.

The proposed MIC is analyzed using the LBSM technique to optimize the converter design. As the proposed MIC uses center tapped transformer, a new model for the center tapped transformer is proposed in this thesis which simplifies the analysis of the converter and provides better insight into different parasitic effects of the transformer. Leveraging the LBSM and based on the single cycle analysis of the converter, an equivalent circuit is proposed for the MIC which contains both high and low frequency effects of the PDM control. The LBSM is then used to obtain accurate and closed form equations for the converter waveforms and design parameters which are then used to propose a new PDM approach. A 1 MHz prototype converter for a 220 W sample PV module has been developed and experimentally tested. The soft-switching operation, PDM regulation of the output and efficiency improvements have been validated experimentally. It has been shown that the proposed converter can reach 99.6% to 96% efficiency for the power mismatches in the PV module ranging from 0 to 50% of the maximum module power generation capability, respectively. The efficiency drop is shown to be linear with power mismatch level without any abrupt reductions that is commonly observed in conventional PV module integrated converters.

Dedicated To The Great Saviour of the World ...

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Chapter 1

Introduction

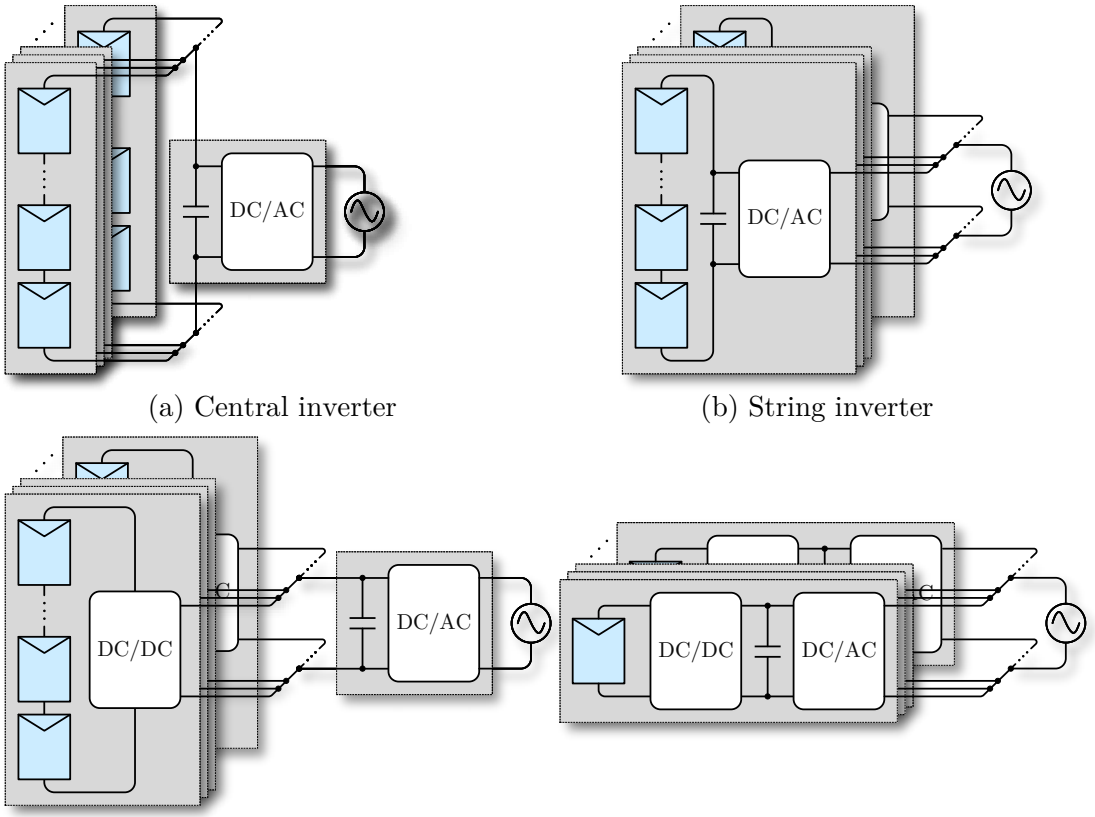
Photovoltaic (PV) solar energy is one of the promising renewable energy resources for which the solar energy is directly converted to electricity [1]. PV modules generate dc voltage in the range of several tens of volts and require both voltage elevation and dc-ac conversion before they can be connected to the ac utility grid.

Furthermore, the power generation of a PV module is dependent on the electrical characteristic of its load and maximum power which is called maximum power point (MPP) is obtained for one specific load characteristic. The MPP of PV modules changes with temperature and irradiation changes, thus maximum power point tracking (MPPT) should be applied on PV modules to extract the maximum energy.

In a PV system, power converters are employed to perform the dc-ac conversion and MPPT. The voltage elevation can be obtained either through the series connection of the PV modules or by means of power converters. Various PV system configurations are presented in the literature based on the series connection of the PV modules or voltage elevation through the power converters [2].

1.1 Background

Figure 1.1 shows some of the most common PV system configurations. In the basic PV system configuration, shown in Fig. 1.1(a), multiple PV modules are connected in series to build up a string with a high dc voltage that is suitable for the dc-ac converter.



(a) Central inverter (b) String inverter

(c) Two-stage (multi-string) inverter (d) Microinverter

Fig. 1.1: Most common PV system configurations in the literature.

Then, parallel combination of some of these high dc voltage strings is connected to a central inverter to perform the dc-ac conversion. This configuration has the lowest power processed by the conversion stage, however, has poor energy capture performance. As a result of series connection, all PV modules in each string have equal currents. However, due to the power mismatch each module may have a different maximum power point (MPP) and consequently a different MPP current. Therefore, in the presence of power mismatch, some of the modules will operate away from their MPP in this configuration resulting in the reduction of captured energy. Power mismatch between modules is the difference between their MPPs which is caused by multiple factors including nonuniform shading, soiling, aging, temperature gradients, etc. In the central inverter configuration, the loss of extractable power may be caused by the power mismatch between different PV strings as well. Depending on the extent of power mismatch in a PV system, up to 30% of the annual extractable energy can be lost in string/central inverter configurations [3]. To overcome the string level power mismatch other configurations are also presented as shown in Fig. 1.1(b) and 1.1(c). In the configuration shown in Fig. 1.1(b), each string is connected to a string inverter to perform the dc-ac conversion separately and in the

configuration shown in Fig. 1.1(c) which is called multistring or two-stage PV system configuration, the strings are equipped with dc-dc converters and multiple strings are then paralleled to increase the power level while only one dc-ac stage is used [2]. Despite its usefulness in addressing string level power mismatches using the string level dc-dc converters or per string dc/ac inversion, these configurations are not able to address the module level power mismatches.

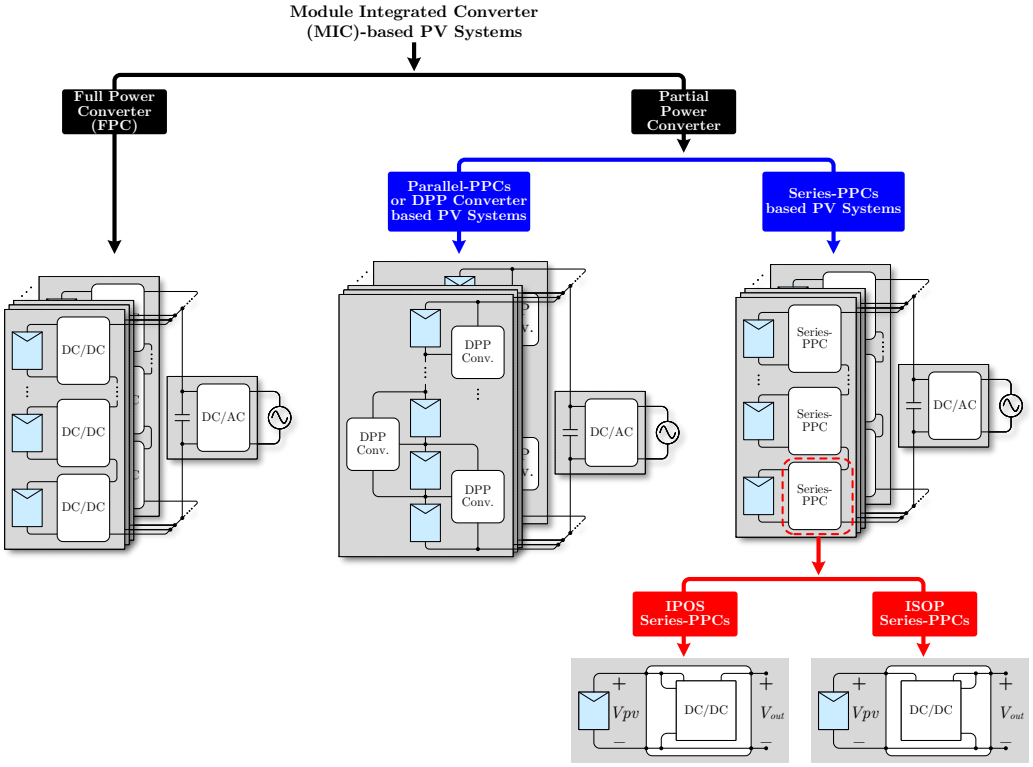


Fig. 1.2: PV systems with different dc-dc Module Integrated Converters (MICs).

There is also another configuration for which the voltage elevation is obtained by means of power electronic converters. This category includes paralleled PV modules equipped with the high step-up dc-dc converters and microinverters which is shown in Fig. 1.1(d). This configuration can overcome the module level power mismatch however it requires a dc-dc converter with a high voltage conversion ratio which is normally obtained using high-frequency transformer. Furthermore, these converters are exposed to wide input voltage range as a result of PV MPP voltage variations at different operating conditions. Therefore, high-frequency and wide input range dc-dc converters must be designed in this configuration of PV systems.

For the configurations with series stack of PV modules the energy loss due to power mismatch can be prevented by equipping each PV module with a dc-dc converter as shown in Fig. 1.2. These dc-dc converters are known as dc-dc module integrated converters (MICs) [4]. MICs perform maximum power point tracking (MPPT) for each PV module and increase the system energy capture. However, as the components used in MICs are not ideal, some energy is dissipated in MICs. The energy loss of MICs is added to the PV system losses and compromises part of the energy capture gain obtained using the module level MPPT. Thus, to justify the inclusion of the MICs from the energy capture point of view, it is crucially important to improve the efficiency of the MICs.

1.2 Challenges

Design of PV converters to meet the requirements imposed by PV system configurations is a challenge that has not been fully addressed in the literature. For the PV system configurations which employ series stack of PV modules, the efficiency of the MICs is a key factor to determine the energy capture improvement offered by them. Efficiency of the MICs in turn depends on their topology and design. Most of the existing literature adopt conventional PWM dc-dc topologies for MIC implementation which suffer from low efficiency. More efficient topologies can be obtained using soft-switching high frequency topologies. However, the application of these topologies for MICs is not investigated in the literature. Also, there is no general and systematic tool in the literature that can be leveraged to improve the efficiency of the MICs by accurate analysis and design optimization. In the PV system configurations that use power converters for voltage elevation e.g., Fig. 1.1(d), wide range soft-switching is required for the high-frequency dc-dc converters. The main obstacle to achieve wide range soft-switching operation for these converters is the lack of general and systematic tools for high-frequency and high-efficiency converter design and analysis.

Steady-state models of power converters that can accurately predict converter voltage and current waveforms are extremely valuable for converter analysis and design, as they enable determination of component voltage and current stresses, identification of soft-switching opportunities, loss estimation, component selection, and topology comparisons. The most valuable modeling techniques are those that provide accurate closed-form expressions for converter waveforms, as they also enable rapid design optimization

[5, 6]. The main obstacle in determining accurate closed-form steady-state waveforms for switching power converters is the presence of switches that introduce nonlinearity into the circuit. The switching action of the switches can be mathematically modeled by discontinuous functions in the governing differential equation of the power converter. However, the presence of the discontinuous functions makes solving the converter's differential equation for a closed-form solution a serious challenge.

1.3 Literature Review

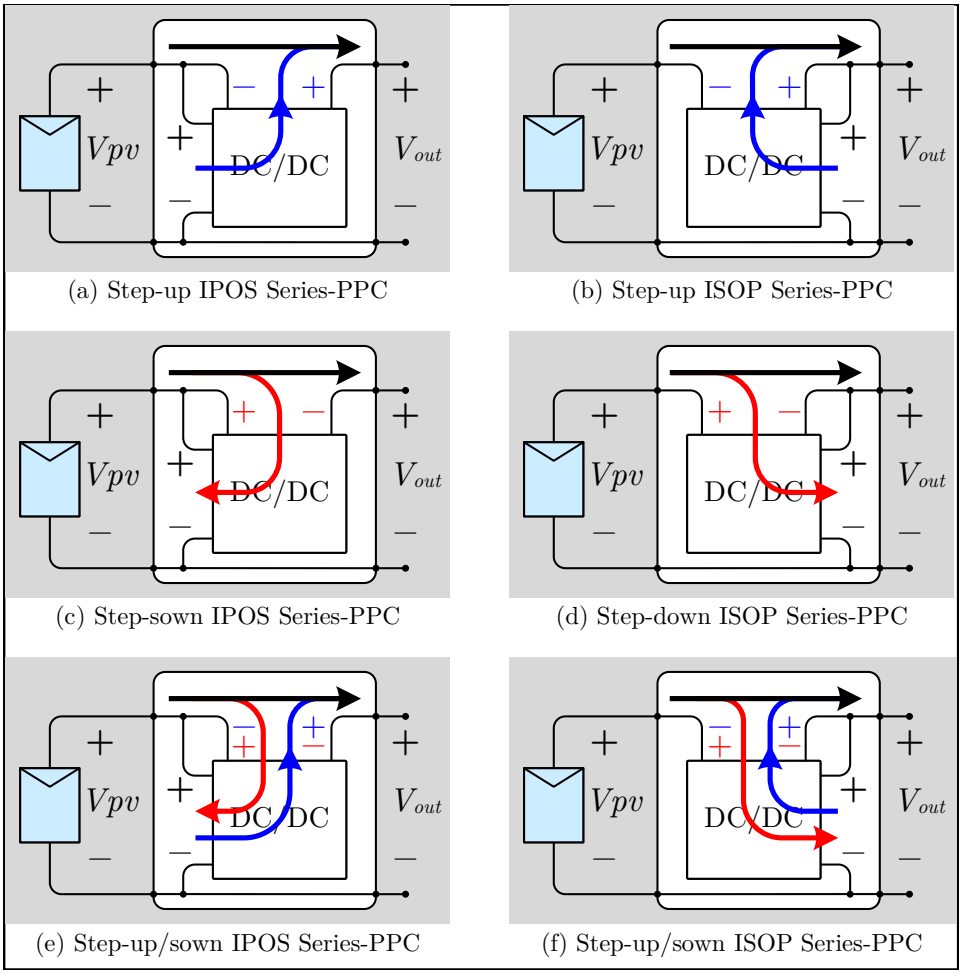
MICs can be categorized into three groups, full power converter, parallel partial power converter (Parallel-PPC) and series partial power converter (Series-PPC). Fig. 1.2 shows different PV system configurations with these MICs. Traditionally, full power converters are employed as the dc-dc MICs. In the configuration equipped with full power converters, all the module generated power is processed by the converter. Hence, if the efficiency of the full power MICs is not high, they insert significant power losses to the system [7]. To address this issue, partial power converters (PPCs) are presented in the literature to process part of the energy flown from their module to the output.

In PPCs, only a part of energy is processed by the converter, hence they can offer improved efficiency compared to FPCs. As it is shown in Fig. 1.2, PPCs comprise of two subcategories of parallel-PPC and series-PPC [4]. The parallel-PPCs are connected in parallel with the PV modules and perform MPPT by shuffling currents among them. Parallel-PPCs are widely referred to as Differential Power Processing (DPP) converters in the literature and are implemented using various configurations and topologies [8]. Fig. 1.2, shows a typical PV system equipped with DPP converters. DPP converters improve the system efficiency by processing only a part of the nominal power and can have smaller rated power than their PV modules [9]. However, there are disadvantages for the DPP converters that have limited their commercial application. Due to the shuffling of currents among converters, the total power processed by converters in some of DPP configurations increases significantly with the increase of the number of modules in a string which diminishes the merits of partial power processing [10] [11]. DPP configurations normally require an extra high-current DC wiring between modules or between modules and the dc bus which increases the cost and adversely affects the reliability and

efficiency. In most DPP configurations, every string only has one MPP voltage and paralleling strings without extra converter may result in string level power mismatch and reduction of captured energy. Furthermore, as DPP converters are connected in parallel with the PV modules they normally operate with rated PV voltage and low current for which power converters exhibit low efficiency due to the load-independent but voltage related losses [12].

To address the issues of DPP converters, series-PPC are presented in the literature. In series-PPCs, a controlled voltage is added in series with the PV voltage to perform MPPT as it is shown in Fig. 1.2 [13]. The series-PPC processes only part of the PV module's power and as such preserves all the merits of DPP without having its disadvantages. Despite the application of series-PPCs in some of the PV systems, the efficiency and MPPT range improvement obtained by employing the series-PPCs in module level in the form of dc-dc MICs is not fully addressed in the literature [14]. In general, there are two factors that affect the efficiency of series-PPCs for an application: topology of the converter and configuration of the series-PPC [15]. Various topologies have been used for the series-PPCs in different levels of the PV systems. Flyback converter is one of the common topologies that has been utilized in series-PPCs due to its galvanic isolation and relatively simple structure [16, 17]. However, the conventional flyback converter suffers from high switching loss and high input current ripple which deteriorate the converter efficiency. Another common topology for PV applications is the phase-shifted full bridge converter which operates under soft-switching condition and provides better efficiencies compared to the conventional flyback converter [18, 19]. To preserve the soft switching operation of the full bridge converter over the voltage conversion range, the converter must have a large magnetizing current which increases the conduction losses and hence reduces the converter efficiency, specifically at full load condition. Alternatively, the magnetizing current can be designed to be low, but the soft switching range is reduced and as a result the soft-switching operation is lost under light load condition resulting in light-load efficiency reduction. The LLC resonant converter has also been used in the series-PPCs in PV applications [20]. The LLC converter can provide the large voltage conversion ratios which is suitable for the microinverter dc-dc stage. It also offers a wide soft-switching range without a significant efficiency penalty at full load operation. However, the LLC converter is not capable of providing zero voltage conversion ratio which is required in some operating point of series-PPC MICs. The zero-voltage conversion

ratio is required when the series-PPC is not supposed to process any power, where its converter inserts zero volts in series with the PV and the PV is directly connected to the string. There are also some current-fed topologies in the literature that have been used as the full power PV converters but not as a series-PPC [21, 22]. These topologies are suitable candidates for the series partial power processing MICs since they can provide both zero voltage conversion ratio and soft switching operation. Despite the effectiveness of these methods in obtaining soft switching for the current-fed push-pull topology, the proposed operation has limited voltage regulation capability and the switch capacitors are not considered in the analysis.



(a) Step-up IPOS Series-PPC

(b) Step-up ISOP Series-PPC

(c) Step-sown IPOS Series-PPC

(d) Step-down ISOP Series-PPC

(e) Step-up/sown IPOS Series-PPC

(f) Step-up/sown ISOP Series-PPC

Fig. 1.3: Different configurations of the series-PPCs.

Configuration of the series-PPCs is another factor that affects their efficiency but has not been specifically investigated for the dc-dc MIC application. According to series partial power processing concept, two power flow paths are provided between the input and the output. One of these paths is created by an isolated dc-dc converter and the other one is a direct connection with a unity efficiency [16]. Depending on the arrangement of the

PV and the output terminals, there are two valid configurations for the series-PPCs, input parallel output series (IPOS) and input series output parallel (ISOP) as shown in Fig. 1.2. Depending on the polarity of the inserted series voltage, each of these series-PPC configurations can have either step-up or step-down or step-up/down operation as it is shown in Fig. 1.3 [14]. Various combinations of configuration and voltage conversion operation of the series-PPCs can be adopted to improve the converter efficiency for the PV applications. In this thesis, each combination of the configuration and the operation of series-PPCs will be referred to as one category of series-PPC. Majority of the presented series-PPCs for the PV application in the literature utilize the step-up IPOS series-PPC shown in Fig. 1.3(a). In [20], a step-up IPOS series-PPC is used as the dc-dc stage of the PV system configuration shown in Fig. 1.1(d) to boost the PV module voltage. However, as the required voltage gain in this system is high, it is hard to provide large voltage conversion ratios while keeping the partial power processing merits. In [13, 18], step-up IPOS series-PPCs and step-up/down IPOS series-PPCs are used as the dc-dc stage of the PV modules string in the two-stage multistring PV systems shown in Fig. 1.1(c) to reduce the component stress and increase the efficiency which are the main concerns in such high-power applications. Generally step-up/down IPOS series-PPCs operate with smaller voltage conversion ratio range compared to step-up IPOS series-PPCs, and as the processed power is related to the voltage conversion ratio range, the step-up/down IPOS series-PPCs process less power [19]. Therefore, step-up/down IPOS series-PPCs are more suitable for string level dc-dc converters of multistring PV systems. The step-up/down IPOS series-PPCs, however, require extra switches to tolerate the bipolar voltage at their output terminal which reduces their efficiency and adds to the converter complexity.

To enable the capability of increasing the number of modules per string and reduce the balance of system (BOS) costs, the total cost of PV systems excluding the PV modules, step-down series-PPCs can be used [11, 23]. To date, only step-down ISOP series-PPC solutions are studied in the literature, as they process less power compared to the step-down IPOS series-PPCs. However, it can be proven that the step-down ISOP series-PPCs are not necessarily more efficient than step-down IPOS series-PPCs. The efficiency of a series-PPC can be obtained form the following equation:

$$\eta_{tot} = 1 - (1 - \eta_c)(P_c/P_{tot}), \tag{1.1}$$

where P_c is the input power of the converter, P_{tot} is the total power generated by PV, η_c is the dc-dc converter efficiency and η_{tot} is the total input to output efficiency. In the literature, when comparing the IPOS and ISOP configurations, the effect of η_c on the total efficiency has been overlooked and it is concluded that if P_c is lower then η_{tot} would be higher. However, in series-PPCs the efficiency is affected by the component stresses and the transformer turns ratio. Therefore, component level realization of the series-PPCs that affects the efficiency needs to be considered for any comparison among the configurations. Then, the component level realization of the adopted topology and configuration must be analyzed to improve the design and obtain higher converter efficiencies. In order to improve the converter design and efficiency their steady-state models needs to be obtained and analyzed.

Various methods have been developed to determine the steady-state switched waveforms of power converters, including a variety of numerical and analytical techniques [24, 25]. The simplest numerical technique relies on computing the converter's state variables by integrating its state equations in small time-steps, starting with zero initial conditions, across multiple switching periods until the values of the state variables reach periodic steady-state [26]. This approach is widely used and can be implemented using commercial circuit simulators, but is computationally inefficient [25]. More efficient numerical techniques have also been developed that determine the initial values of the state variables under steady-state operation before solving for the converter waveforms across only one switching period. These include iterative search techniques [27, 28], a non-iterative augmented state-vector based technique which is limited to converters with known subinterval durations [29], and a hybrid approach which combines the augmented state-vector technique with a binary search to make it broadly applicable [30]. However, unlike closed-form solutions, numerical approaches do not provide insights into the dependence of converter waveforms on its parameters, and are computationally less efficient during converter optimization.

A number of analytical modeling techniques have also been developed to determine steady-state waveforms. A popular analytical approach to converter modeling, applicable to both steady-state and transient operation, is state-space averaging, in which an averaged circuit model and averaged state-space equations of the converter are developed by averaging its switching action over a switching period [31]. While extremely valuable for studying averaged converter dynamics of PWM converters operating in

continuous conduction mode (CCM) and the design of their controllers, such averaged models cannot predict waveform dynamics within a switching period and cannot be directly used to determine switched waveforms [32]. Approximate closed-form expressions for switched waveforms of PWM converters operating in CCM can be found by superimposing the ripple in the state variables, determined under small ripple approximation, onto their steady-state average values [31]. This approach does not work well for converters with large ripple, such as PWM converters operating in discontinuous conduction mode (DCM), soft-switching converters, and resonant converters. More sophisticated averaging techniques that attempt to capture the waveform dynamics within a switching period by incorporating switching frequency and higher order harmonics, in addition to the dc component, have also been developed [33–36]. The use of large number of harmonics to achieve high degree of accuracy makes these techniques cumbersome and does not yield closed-form expressions. The simplest of these approaches, widely used in the modeling of resonant converters, uses only the fundamental component of the switching waveform and is referred to as fundamental harmonic analysis (FHA) or sinusoidal analysis [37]. While this approach yields closed-form expressions, the results are accurate only for resonant converters with high loaded quality factor resonant tanks. Additional steady-state modeling approaches include analytically solving the differential equations associated with each switching interval of the converter and equating the state variable waveforms at the beginning and end of the switching period [38, 39]. A related approach is state plane analysis, in which state variable waveforms are mapped to geometric figures comprising segments of circles, lines or ellipses [40, 41]. State plane analysis becomes extremely tedious for converters with more than two state variables, and both of the above time domain approaches require finding all the switching intervals of the converter and the initial values of the state variables, which is not straightforward. Another time domain steady-state modeling approach is step-superposition analysis, in which step responses to switch-network imposed steps are summed up by leveraging geometric series analysis to determine closed-form expressions for converter waveforms [42]. However, this approach has only been successfully demonstrated for converters in which the switch networks can be replaced by independent sources.

1.4 Proposed Method

In this thesis, the various voltage conversion ratio operations of a series-PPC are thoroughly analyzed for the module integrated dc-dc converters. Two common methods for MPPT of the PV modules using the fixed and variable dc bus voltage have also been considered. It has been shown that step-down series-PPCs are beneficial for both constant voltage and variable voltage dc bus PV systems and a step-down series-PPC is proposed for the dc-dc MIC of PV systems. A soft-switching and high-frequency topology which has a simple structure and can provide zero voltage conversion ratio is adopted to realize the MIC. The gating signals of the converter are changed to achieve soft switching operation. This topology and operation are then used to compare the step-down IPOS with the step-down ISOP category. It has been shown that for the selected topology, the IPOS step-down category provides better total efficiency for the dc-dc MIC. Thus, the MIC is realized using the IPOS configuration. Using the Pulse Density Modulation (PDM), the voltage regulation of the topology is improved in this thesis. Adopting PDM control helps to preserve the soft switching for the entire voltage conversion range without any full load efficiency penalty. Furthermore, the effects of switch output capacitors which were not previously studied, have been investigated in this thesis. It is shown that switch capacitors resonate with the leakage inductance when the switch is turned off and cause voltage spikes and oscillations on switches, which reduces the efficiency specifically in high frequency applications. Two clamp didoes are employed to effectively suppress the voltage spikes, and to restore the energy of the leakage inductance once the switch capacitors are charged to the desired voltage. Furthermore, another operation mode is added to the regular converter operating modes which utilizes the clamp diodes only. Utilizing this mode of operation gives an extra degree of freedom to extend the voltage conversion ratio range to cover the whole zero to one voltage conversion ratio range. Therefore, the proposed converter can perform MPPT for the full power generation range of the PV module from zero to the rated power without any efficiency penalty at the converter normal operating range or any extra components. In addition to the proposed MIC a generalized and systematic tool is also presented in this thesis that significantly improves the existing methods and can be leveraged to analyze and design PV converters including the proposed MIC. Recently a new approach to determine accurate closed-form steady-state solutions of ordinary differential equations (ODEs) with periodic and discontinuous input, referred to as Laplace

Based Theorem (LBT), has been introduced [43], and used to analyze a series resonant converter [44]. However, this approach can only be applied to a limited set of power converters, referred to here as edge switch-network converters, where the switching action of the converter's switches does not reconfigure the interconnection between its energy storage elements. This thesis presents a generalized technique, referred to as Laplace Based Steady-state Modeling (LBSM), which leverages LBT and introduces a systematic modeling procedure to model a broad class of power converters using ODEs with periodic and discontinuous inputs, including edge switch-network converters as well as interior switch-network converters, in which the switching action reconfigures the interconnection between its energy storage elements. Furthermore, the LBSM application to state-space representation of the converters is presented which can facilitate the high order converter analysis.

1.5 Objectives

The objectives of this thesis can be outlined as below:

1. Develop a Laplace based steady-state modeling (LBSM) technique which is applicable to both interior and edge switched network converters.
2. Extend the LBSM technique to state-space representation of the converters.
3. Demonstrate the effectiveness of LBSM, by determining closed-form steady-state waveforms for a number of power converters, including the buck converter, the boost converter, the series resonant converter, and the phase-shift converter.
4. Leverage the LBSM to develop ZVS and loss models for commonly used converters in high step-up PV converters i.e., SRC and PSC and compare them.
5. Investigate various PV system configurations to find the best MIC performance requirements.
6. Propose a suitable topology and configuration for the series-PPC used as PV MIC.
7. Improve the control of the proposed MIC to extend its MPPT range and efficiency.
8. Develop steady-state model for the proposed MIC using LBSM and use this model to further improve converter design.

Chapter 2

Laplace Based Steady-state Modeling (LBSM)

In this chapter, Laplace Based Steady-state Modeling (LBSM) technique is presented as a general tool for converter analysis and design which will be used to analyze and design PV converters in specific. To demonstrate the effectiveness of LBSM, the LBSM is used to determine closed-form steady-state waveforms for a number of power converters, including the buck converter, the boost converter, the series resonant converter, and the phase-shift converter. LBSM is also leveraged to determine the zero voltage switching (ZVS) conditions for the series resonant converter and the phase-shift converter and compare these converters in terms of efficiency. It is shown that in applications where the variation in input voltage is less than a factor of two, the series resonant converter has superior performance; while in applications where the variation in input voltage is larger, the phase-shift converter has superior performance.

This chapter first presents the Laplace Based Theorem (LBT) and describes the procedure to finding the steady-state response of ODEs with inputs that are periodic discontinuous functions. A rigorous proof of the LBT which uses formal mathematical notations is presented. The Laplace Based Steady-state Modeling (LBSM) technique is described for edge and interior switch-network converters. To demonstrate the effectiveness of this technique for edge and interior switch-network converters, closed-form steady-state models for the buck converter and the boost converter are also developed using LBSM. Extension of the LBSM to state space representation of the converters is

given. An example application of the LBSM to converters with AC sources is also presented. The LBSM technique is utilized to analyze and design a phase-shift controlled series resonant converter and a phase shift converter and these two converters are also compared. The accurate ZVS model and loss model of these converters are obtained using LBSM technique which facilitates their comparison. LBSM is also compared to other existing methods in the literature to better illustrate the competencies offered by the LBSM. The predicted results for the series resonant converter and the phase shift converter are experimentally validated.

2.1 Steady-State Solution of ODEs Using Laplace Based Theorem

A power converter can be mathematically modeled by its governing differential equation(s) in which its switching actions are represented by periodic discontinuous functions. The mathematical model can be a single differential equation (typically of high order), or multiple first-order differential equations in the form of state-space representation. Here, the single differential equation approach is used for simplicity, and the state-space approach is presented in Section 2.4. Determining an accurate closed-form expression for the steady-state response of the converter is not straight-forward, as with arbitrary initial conditions the converter's response will typically go through a transient before reaching steady state, as shown in Fig. 2.1. During the transient, the state variables of the converter (i.e., its capacitor voltages and inductor currents) have different values at the beginning and end of a switching period. On the other hand, in steady-state operation, the state variables have the same values at the beginning and end of the switching period and the waveform repeats itself. Therefore, the converter's steady-state waveform can be determined by solving its differential equation over one switching period provided the initial values of the state variable and its time derivatives under steady-state operation are known. These initial values can be determined using Laplace Based Theorem (LBT), which is introduced next.

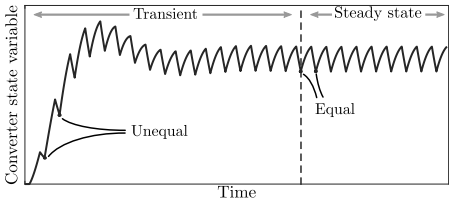


Fig. 2.1: Response of a power converter with an arbitrary initial condition, showing its state variable going through a transient before reaching steady state.

2.1.1 Laplace Based Theorem (LBT)

Laplace Based Theorem (LBT) provides a method to determine the initial values for the steady-state solution of a constant-coefficient non-homogeneous ordinary differential equation with periodic and discontinuous input. Consider a system with the constant-coefficient non-homogeneous ordinary differential equation:

$$a_n \frac{d^n x}{dt^n} + a_{n-1} \frac{d^{n-1} x}{dt^{n-1}} + \cdots + a_0 x(t) = f(t), \qquad (t > 0), \tag{2.1}$$

where x is the state variable, t is time, a_k's ($0 \leq k \leq n$ and $a_n \neq 0$) are constant coefficients (which in general can be complex), and the input f is a periodic function with period T that is integrable over $[0, \mathrm{T})$. The input f can be a linear combination of a piecewise smooth function with finite number of discontinuities and a finite number of Dirac functions on $[0, \mathrm{T})$. Taking the Laplace transform of (2.1) gives:

$$P(s)X(s) + Q(s) = F(s), \tag{2.2}$$

where $P(s) = \sum_{k=1}^{n} a_k s^k$ is the differential equation's characteristic polynomial of order n, $X(s)$ is the Laplace transform of $x(t)$, $F(s) = \left(\int_0^{\mathrm{T}} f(t) e^{-st} dt\right) / \left(1 - e^{-s\mathrm{T}}\right)$ is the Laplace transform of the periodic input function $f(t)$, and $Q(s)$ is a polynomial of degree at most $n-1$ formed using the initial values of the system and given by:

$$\begin{aligned} Q(s) &= -x(0)a_n s^{n-1} - (x(0)a_{n-1} + x'(0)a_n)s^{n-2} - \ldots = \\ &\begin{bmatrix} -x(0) \\ -x'(0) \\ \vdots \\ -x^{(n-1)}(0) \end{bmatrix}^T \begin{bmatrix} a_n & a_{n-1} & \cdots & a_2 & a_1 \\ 0 & a_n & & & a_2 \\ 0 & 0 & \ddots & & \vdots \\ \vdots & \vdots & & a_n & a_{n-1} \\ 0 & 0 & \cdots & 0 & a_n \end{bmatrix} \begin{bmatrix} s^{n-1} \\ s^{n-2} \\ \vdots \\ s \\ 1 \end{bmatrix}, \end{aligned} \tag{2.3}$$

where $x(0), x'(0), \cdots, x^{(n-1)}(0)$ are the n unknown initial values of the state variable x and its time derivatives.

Assuming that $P(s)$ has n distinct roots $s_1, \cdots, s_n$ that do not intersect with the poles of $F(s)$, LBT states that the system has a periodic solution if and only if:

$$\Big[Q(s_1), Q(s_2), \cdots, Q(s_n)\Big] = \Big[F(s_1), F(s_2), \cdots, F(s_n)\Big] \tag{2.4}$$

2.1.2 Proof of LBT

This subsection provides a rigorous proof of the Laplace Based Theorem (LBT) using formal mathematical notations. The proof of LBT relies on the properties of periodic functions and two other theorems, which are described and proved first.

2.1.2.1 Periodic Functions

Let f be a function on $(0, \infty)$ for which there is a constant $\sigma_0 \in R$ such that $\int_0^\infty e^{-\sigma_0 t}|f(t)|\,dt < \infty$.

In particular, f can be piecewise smooth, consist of an infinite sequence of Dirac functions, or be a linear combination of both, as in these situations the condition is fulfilled. Then, the Laplace transform of f is defined by:

$$F(s) = (\mathcal{L}f)(s) := \int_0^\infty e^{-st} f(t)\,dt, \tag{2.5}$$

on the half plane $\Re s > \sigma_0$ and represents an analytic function there. Under certain conditions, F extends to a larger domain as a meromorphic function. One such possibility relates to periodic functions as described below.

Let f be integrable over $[0, \mathrm{T})$, where $\mathrm{T} > 0$, and extend f periodically over $[0, \infty)$. We denote the family of all such functions by $\mathcal{P}_T$. As a common prototype, f can be the linear combination of a piecewise smooth function and a finite number of Dirac functions on $[0, \mathrm{T})$. Using (2.5) and a geometric series argument, it is easy to see that the Laplace transform of f is given by [45]:

$$F(s) = \frac{1}{1 - e^{-s\mathrm{T}}} \int_{[0,\mathrm{T})} e^{-st} f(t)\,dt. \tag{2.6}$$

It is important to note that the integral is not written as $\int_0^{\mathrm{T}}$ because if there is a Dirac function anchored at point $t = 0$, then by periodicity it appears again at $t = \mathrm{T}$. However, it must be counted only once in (2.6). To avoid such a potential problem, in the following whenever $\int_a^b$ is used it is meant $\int_{[a,b)}$.

The function F is initially defined in the right half plane $\Re s > 0$, i.e., $\sigma_0 = 0$. This condition is imposed to guarantee the convergence of the geometric series which creates the factor $1/(1 - e^{-s\mathrm{T}})$. But, using the formula (2.6), it can be extended to a meromorphic function on the whole complex plane $\mathbb{C}$ with simple poles on the imaginary axis: $p_n = i\frac{2n\pi}{\mathrm{T}}$, $n \in \mathbb{Z}$, the set of all integers. In particular, if there is no factor of the form s^n, $n \geq 1$, in the denominator, the origin is always a simple pole of F. This necessary condition plays a vital role in the "only if" part of the Laplace Based Theorem. This result is stated as a lemma for further reference (see [45, 46]).

Lemma 2.1. *Let F be the Laplace transform of the function f. Assume that F has either multiple poles, or poles which are not on the imaginary axis. Then f is not periodic.*

If F is given by (2.6), P and Q are polynomials, and we consider the combination $G := \frac{F-Q}{P}$, then $g = \mathcal{L}^{-1}(G)$ is not necessarily periodic over $(0, \infty)$. Almost all the time, there are exponential terms which are created due to the zeros of P. However, based on the above discussion, a necessary and sufficient condition is found which ensures the periodicity of g. The condition also reveals that the periodicity is a very rare situation.

2.1.2.2 The Quotient Operator

Assume that function $F(s)$ is analytic in a neighborhood of the point a. Then the quotient operator Q_a is defined by

$$(Q_a F)(s) := \frac{F(s) - F(a)}{s - a}, \qquad (s \neq a). \tag{2.7}$$

At the point $s = a$, in order to obtain an analytic function $Q_a F$, there is no choice but to define

$$(Q_a F)(a) = F'(a). \tag{2.8}$$

The function Q_aF is meromorphic on the same domain that F is defined. This operator is usually used to eliminate the zeros of F. Note that if $F(a) = 0$, then Q_aF is obtained by removing the factor $s - a$ from F. If this process is repeated a finite number of times (the order of the zero), then Q_a^nF is zero free at $s = a$ (see [47]). The following result is an essential observation about periodic functions. In technical language, it says that $\mathcal{P}_T$ is invariant under the operation $\mathcal{L}^{-1}(Q_aF)$.

Theorem 1. *Let $f \in \mathcal{P}_T$, and let $a \in \mathbb{C} \setminus \{j\frac{2n\pi}{T} : n \in \mathbb{Z}\}$. Then $\mathcal{L}^{-1}(Q_aF) \in \mathcal{P}_T$.*

Using elementary properties of Laplace transform [48], it is seen that

$$\mathcal{L}^{-1}(Q_aF)(t) = -F(a)e^{at} + e^{at}\int_0^t e^{-a\tau}f(\tau)\,d\tau, \qquad (t > 0), \tag{2.9}$$

where $F(a)$ is given by (2.6) (and, in fact, not by (2.5) if $\Re a \leq 0$). Then, for all $t > 0$,

$$\begin{aligned}
& \mathcal{L}^{-1}(Q_aF)(t+\mathrm{T}) = -F(a)e^{a(t+\mathrm{T})} + e^{a(t+\mathrm{T})}\textstyle\int_0^{t+\mathrm{T}} e^{-a\tau}f(\tau)\,d\tau \\
= \;& -F(a)e^{a(t+\mathrm{T})} + e^{a(t+\mathrm{T})}\left(\textstyle\int_0^{\mathrm{T}} + \int_{\mathrm{T}}^{t+\mathrm{T}}\right)e^{-a\tau}f(\tau)\,d\tau \\
= \;& -F(a)e^{a(t+\mathrm{T})} + e^{a(t+\mathrm{T})}\left(\textstyle\int_0^{\mathrm{T}} e^{-a\tau}f(\tau)\,d\tau + \int_0^t e^{-a(\tau+\mathrm{T})}f(\tau+T)\,d\tau\right) \\
= \;& -F(a)e^{a(t+\mathrm{T})} + e^{a(t+\mathrm{T})}(1-e^{-a\mathrm{T}})F(a) + e^{a(t+\mathrm{T})}e^{-a\mathrm{T}}\textstyle\int_0^t e^{-a\tau}f(\tau)\,d\tau \\
= \;& -F(a)e^{at} + e^{at}\textstyle\int_0^t e^{-a\tau}f(\tau)\,d\tau = \mathcal{L}^{-1}(Q_aF)(t)
\end{aligned}$$

In other words, $\mathcal{L}^{-1}(Q_aF)$ is periodic on $(0, \infty)$ with period T.

Theorem 1 can be extended to include the poles $a = j\frac{2n\pi}{\mathrm{T}}$. In this case, we may first define Q_a by $(Q_aF)(s) = (s-a)F(s)$ and then, with some modifications, the above proof still works.

2.1.2.3 The Quotient Expansion

The classical Partial Fraction Expansion Theorem represents a rational function $f = Q/P$, where Q and P are polynomials, as a linear combination of simpler fractions $1/(s-p)^m$ where p is a root of P and m is at most the order of this root. For our application, we need a special expansion which resembles the partial fraction expansion, but it has a different methodology.

Theorem 2. *Let P be a monic polynomial of degree n with distinct roots $s_1, \ldots, s_n$. Let F be a holomorphic function in a domain which contains the roots of P. Let Q be the unique polynomial of degree at most $n-1$ such that*

$$Q(s_k) = F(s_k), \qquad (1 \leq k \leq n). \tag{2.10}$$

Then there are constants $c_1, \ldots, c_n \in \mathbb{C}$ such that

$$\frac{F(s) - Q(s)}{P(s)} = \sum_{k=1}^{n} c_k \frac{F(s) - F(s_k)}{s - s_k}. \tag{2.11}$$

Consider Lagrange interpolating polynomials

$$L_k(s) := \prod_{\substack{l=1 \\ l \neq k}}^{n} \frac{s - s_l}{s_k - s_l}, \qquad (1 \leq k \leq n). \tag{2.12}$$

Then the polynomial Q is uniquely given by the formula

$$Q(s) = \sum_{k=1}^{n} F(s_k)\, L_k(s). \tag{2.13}$$

Appealing again to the uniqueness of representation by Lagrange polynomials, we also have the well-known identity [49]

$$\sum_{k=1}^{n} L_k(s) \equiv 1. \tag{2.14}$$

Therefore,

$$\begin{aligned} \tfrac{F(s)-Q(s)}{P(s)} &= \tfrac{1}{P(s)} \left(F(s) \textstyle\sum_{k=1}^{n} L_k(s) - \sum_{k=1}^{n} F(s_k)\, L_k(s) \right) \\ &= \textstyle\sum_{k=1}^{n} \tfrac{(F(s)-F(s_k))\, L_k(s)}{P(s)} \\ &= \textstyle\sum_{k=1}^{n} \tfrac{F(s)-F(s_k)}{(s-s_k) \prod_{\substack{l=1 \\ l \neq k}}^{n} (s_k - s_l)} = \sum_{k=1}^{n} c_k \tfrac{F(s)-F(s_k)}{s-s_k}, \end{aligned}$$

where

$$c_k = \left(\prod_{\substack{l=1 \\ l \neq k}}^{n} (s_k - s_l) \right)^{-1}, \qquad (1 \leq k \leq n). \tag{2.15}$$

As a byproduct of this proof, it is interesting to see that the constants c_j do not depend

on F. They are uniquely determined by the zeros of P via (2.15) (recall that P is monic; otherwise there is a multiplicative constant that should be considered).

2.1.2.4 Linear Systems

Consider the initial value problem

$$a_n \frac{d^n x}{dt^n} + a_{n-1} \frac{d^{n-1} x}{dt^{n-1}} + \cdots + a_0 x(t) = f(t), (t > 0), \tag{2.16}$$

where a_k's are complex numbers, $a_n \neq 0$, and $f \in \mathcal{P}_T$. Upon taking the Laplace transform of (2.16), we obtain

$$P(s)X(s) + Q(s) = F(s), \tag{2.17}$$

where P is the characteristic polynomial with order n and Q is a polynomial of degree at most $n-1$ formed with the initial values of the system. Therefore, solving for X, we easily see that

$$X(s) = \frac{F(s) - Q(s)}{P(s)}. \tag{2.18}$$

Assume that P has n distinct zeros which can be every where in the complex plane except at the poles of F, i.e., at $p_n = j\frac{2n\pi}{\mathrm{T}}$, $n \in \mathbb{Z}$, and let a be a zero of P. If $F(a) - Q(a) \neq 0$, then X has a pole at a and, by Lemma 1, we immediately conclude that x is not a periodic function. This simple observation shows that a necessary condition for having a periodic response is that $F(a) - Q(a) = 0$ at all zeros of P. However, it is not trivial at all that this condition is also sufficient. To add the obscurity, note that P and Q are polynomials while F has the factor $1 - e^{-s\mathrm{T}}$. It is not clear why the assumption $F(a) - Q(a) = 0$, for all zeros a, essentially forces this factor to pop out for the whole combination, e.g., as in (2.6), and thus the inverse Laplace transform would give us a periodic function. Some deep observations from operator theory are needed to characterize the situation under which the system gets an input from $\mathcal{P}_T$ and provides an output precisely in the same space.

Theorem 2.2. *Let $f \in \mathcal{P}_T$. Assume that the characteristic polynomial of the linear system* (2.16) *has n distinct roots $s_1, \cdots, s_n$ with*

$$s_k \in \mathbb{C} \setminus \{j\frac{2n\pi}{\mathrm{T}} : n \in \mathbb{Z}\}, \qquad (1 \leq k \leq n). \tag{2.19}$$

Then the system has a periodic solution (i.e., $x(t) \in \mathcal{P}_T$) if and only if

$$F(s_k) = Q(s_k), \qquad (1 \le k \le n). \tag{2.20}$$

Moreover, the above conditions are fulfilled for a unique choice of initial values.

Proof. We already observed that F is meromorphic with poles on the imaginary axis. The assumption (2.19) ensures that F is analytic at the zeros of P. Thus, according to Theorem 2, there are constants $c_1, \ldots, c_n \in \mathbb{C}$ (see (2.15)) such that

$$X(s) = \frac{F(s) - Q(s)}{P(s)} = \sum_{k=1}^{n} c_j \frac{F(s) - F(s_k)}{s - s_k}. \tag{2.21}$$

Using the quotient operator Q_a, we may rewrite the above formula as

$$X(s) = \sum_{k=1}^{n} c_k (Q_{s_k} F)(s). \tag{2.22}$$

Therefore,

$$x(t) = \sum_{k=1}^{n} c_k \, \mathcal{L}^{-1}(Q_{s_k} F)(t), \tag{2.23}$$

and Theorem 1 ensures that each function $\mathcal{L}^{-1}(Q_{s_k} F)$ is periodic over $(0, \infty)$ with period T. □

2.1.3 ODE Steady-State Solution Using LBT

LBT can be leveraged to determine the initial values of the state variable under steady-state operation. Simply substituting (2.3) into (2.4) results in the n linear equations given by (2.24), which can be used to find the n unknown initial values for the steady-state solution:

$$\begin{bmatrix} -x(0) \\ -x'(0) \\ \vdots \\ -x^{(n-1)}(0) \end{bmatrix}^T \begin{bmatrix} a_n & a_{n-1} & \cdots & a_2 & a_1 \\ 0 & a_n & & & a_2 \\ 0 & 0 & \ddots & & \vdots \\ \vdots & \vdots & & a_n & a_{n-1} \\ 0 & 0 & \cdots & 0 & a_n \end{bmatrix} \begin{bmatrix} s_1^{n-1} & s_2^{n-1} & \cdots & s_n^{n-1} \\ s_1^{n-2} & s_2^{n-2} & \cdots & s_n^{n-2} \\ \vdots & \vdots & & \vdots \\ 1 & 1 & \cdots & 1 \end{bmatrix} = \begin{bmatrix} F(s_1) \\ F(s_2) \\ \vdots \\ F(s_n) \end{bmatrix}^T \tag{2.24}$$

Since the s_k's are distinct, the matrix $\left[s_k^{n-l}\right]_{1\leq k,l\leq n}$ is invertible. Also, since $a_n \neq 0$, the upper triangular matrix is invertible. Hence, the equation given by (2.24) always has a unique solution for $x(0), \cdots, x^{(n-1)}(0)$. Therefore, the following procedure is proposed to determine the closed-form steady-state solution of a constant coefficient non-homogeneous ODE having the form of (2.1):

S1) Determine $F(s) = \mathcal{L}\{f(t)\}$, where $f(t)$ is periodic with period T and can be discontinuous.

S2) Determine $s_1, s_2, \cdots, s_n$, the roots of the characteristic polynomial $P(s) = \sum_{k=1}^{n} a_k s^k$.

S3) Formulate the set of n linear equations in accordance with (2.24), and solve (2.24) to determine the n steady-state initial values $x(0), \ldots, x^{(n-1)}(0)$.

S4) Using the n initial steady-state values of the state variable and its time derivatives, solve (2.1) to find the steady-state solution for $x(t)$ across one switching period.

To understand the limitations of the proposed approach note that since LBT is based on a constant coefficient differential equation, it cannot be applied to power converters that contain nonlinear elements other than switches, such as saturable inductors and nonlinear capacitors. Also since there are no algebraic closed-form solutions for the roots of a general polynomial equation of degree five or higher, algebraic closed-form expressions for the waveforms of converters with more than four state variables are not guaranteed. However, closed-form expressions that include non-algebraic operations may exist for some of these cases. Other than these limitations, the proposed approach can be used for a broad class of power converters. The requirement that the roots of $P(s)$ have to be distinct from one another and different from the poles of $F(s)$ is rarely not met in real power converters. For example, if a root of $P(s)$ is at the same location as a pole of $F(s)$ then the converter will have an undamped oscillatory response, which is undesirable and will be intentionally avoided in a practical design. Also if $P(s)$ has non-distinct roots, this will occur for a specific loading condition. For this rare case, converter waveforms can be obtained using a slightly different loading condition in the very close vicinity of the original loading without introducing much error in a practical design. It should also be noted that although LBT holds even when the ODE's constant coefficients (a_k's) are complex numbers, these coefficients will be real for a power converter comprising only switches and Linear Time Invariant (LTI) elements.

2.2 Laplace Based Steady-state Modeling (LBSM)

LBT provides an approach to determine closed-form expressions for the steady-state solution of ODEs with periodic and discontinuous input. However, to utilize LBT to find a converter's steady-state waveforms, the converter must be modeled as a constant-coefficient ODE having the form of (2.1). Therefore, the Laplace Based Steady-state Modeling (LBSM) approach introduced here has two high-level steps. In the first step, a constant coefficient ODE is derived that models the steady-state switched behavior of the converter. In the second step, the procedure described in Section 2.1.3 is applied to the converter's ODE to determine its steady-state waveforms.

Switching power converters comprise linear elements (capacitors, inductors, and transformers), also referred to as energy storage elements, and switches. Converters interface with sources and loads at their input and output ports. Depending on their topology, converters can be categorized into one of two classes: (a) edge switch-network converters, or (b) interior switch-network converters. If the switching action of the converter's switches does not reconfigure the interconnection between its energy storage elements, the converter is called an edge switch-network converter. This will typically only be possible when the switches are connected to the input and/or output ports of the converter. Examples of edge switch-network converters include buck converter, voltage source inverter, and series resonant converter (if the dynamics of its output filter are negligible). If the switching action of the converter's switches reconfigures the interconnection between its energy storage elements, the converter is called an interior switch-network converter. Examples of interior switch-network converters include boost converter, buck-boost converter, Cuk converter, SEPIC converter, Zeta converter, four-switch buck-boost converter, Watkins-Johnson converter, flyback converter, and any of the edge switch-network converters with an input filter whose dynamics cannot be ignored. Different procedures are needed to model edge and interior switch-network converters in the form of constant-coefficient ODEs.

2.2.1 Edge Switch-Network Converters

In edge switch-network converters, the voltage across, or the current through, each switch can be determined solely from the values of the actual or equivalent sources connected at the input and/or output ports of the converter. Hence, individual switches, or more

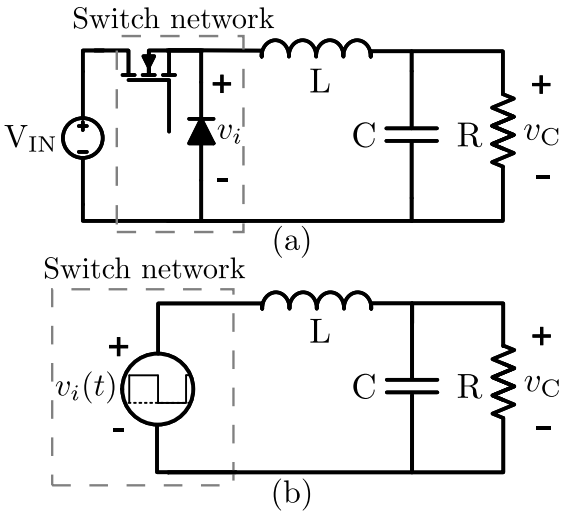


Fig. 2.2: Buck converter: (a) topology, and (b) switched-mode equivalent circuit model.

commonly switch networks, can be replaced by time varying independent voltage or current sources, simplifying the derivation of its ODE. To model an edge switch-network converter in the form of an ODE, the following procedure is proposed:

M1) Create an equivalent circuit model for the converter by replacing switch networks and/or individual switches with periodic discontinuous independent voltage or current sources that model the ports of the switch networks and/or the switches.

M2) Determine the converter's governing differential equation from the equivalent circuit model in terms of one of its state variables. This equation will be a constant coefficient ODE of the form of (2.1).

As an example, consider the buck converter shown in Fig. 2.2(a). This converter can be separated into two cascaded networks: a switch network and an energy storage network. The switch network comprises two switches (a MOSFET and a diode) and is connected to the input voltage source at the input port of the converter. The energy storage network comprises an inductor and a capacitor and is connected to a load resistor at the output port of the converter, forming a linear time-invariant (LTI) network. Following step (M1) and assuming that the converter is operating in continuous conduction mode (CCM), the voltage across the diode is either V_{IN} (when MOSFET is on) or zero (when MOSFET is off). Hence, the buck converter can be modeled using the equivalent circuit shown in Fig. 2.2(b). Following step (M2), Fig. 2.2(b) can be used to easily determine the following constant coefficient ODE for the buck converter operating in CCM:

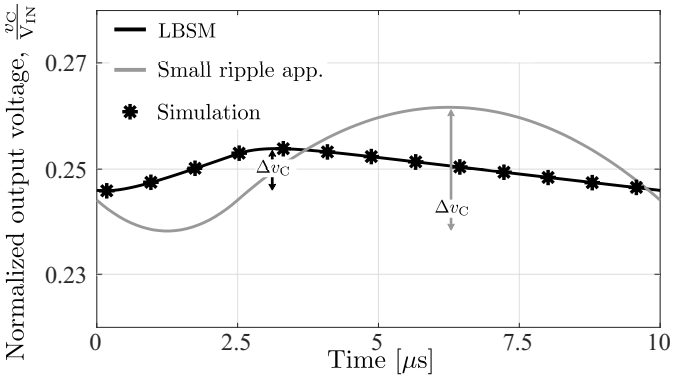


Fig. 2.3: Comparison of normalized output voltage waveform obtained using LBSM, numerical simulation, and small ripple approximation for a buck converter with following parameter values: L = 20 μH, C = 5 μF, R = 0.1 Ω, $D = 0.25$ and $f_s = 100$ kHz. Here, $\Delta v_C/V_C$ is 3.2% and 9.4% for the LBSM and small ripple approximation waveforms, respectively.

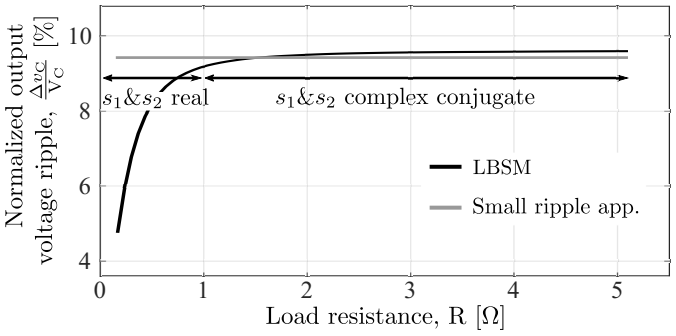


Fig. 2.4: Comparison of normalized peak-to-peak output voltage ripple $\frac{\Delta v_C}{V_C}$ as a function of load resistance obtained using LBSM and small ripple approximation for the example buck converter of Fig. 2.3.

$$\mathrm{LC}\frac{d^2 v_\mathrm{C}}{dt^2} + \frac{\mathrm{L}}{\mathrm{R}}\frac{dv_\mathrm{C}}{dt} + v_\mathrm{C}(t) = v_i(t), \tag{2.26}$$

where $v_i(t) = q(t)\mathrm{V_{IN}}$, and $q(t)$ is a switching function which equals 1 when the MOSFET (i.e., active switch) is on and 0 when the MOSFET is off.

The steady-state solution for this ODE can be found using the four steps given in Section 2.1.3. Following step (S1), the Laplace transform of the input function is:

$$F(s) = \mathcal{L}\{v_i(t)\} = \mathrm{V_{IN}}\frac{1 - e^{-sD\mathrm{T_s}}}{s\left(1 - e^{-s\mathrm{T_s}}\right)}, \tag{2.27}$$

where $\mathrm{T_s}$ is the switching period and D is the duty cycle of the converter. Next, following step (S2), the characteristic polynomial has the following roots:

$$s_{1,2} = \frac{1}{2\mathrm{RC}}\left(-1 \pm \sqrt{1 - 4\frac{\mathrm{R^2C}}{\mathrm{L}}}\right) \equiv s_r \pm s_m \tag{2.28}$$

Following step (S3), and formulating $Q(s_k) = F(s_k)$ for $k = 1, 2$ in the form of (2.24), results in the following set of linear equations:

$$\begin{bmatrix} -v_{\mathrm{C}}(0) & -v'_{\mathrm{C}}(0) \end{bmatrix} \begin{bmatrix} \mathrm{LC} & \frac{\mathrm{L}}{\mathrm{R}} \\ 0 & \mathrm{LC} \end{bmatrix} \begin{bmatrix} s_1 & s_2 \\ 1 & 1 \end{bmatrix} = \begin{bmatrix} F(s_1) & F(s_2) \end{bmatrix}, \tag{2.29}$$

which can be solved for the initial conditions $v_{\mathrm{C}}(0)$ and $v'_{\mathrm{C}}(0)$ to obtain:

$$v_{\mathrm{C}}(0) = \tfrac{F(s_1)-F(s_2)}{\mathrm{LC}(s_2-s_1)}, \quad v'_{\mathrm{C}}(0) = \tfrac{s_1F(s_1)-s_2F(s_2)}{\mathrm{LC}(s_2-s_1)}. \tag{2.30}$$

Finally, following step (S4), and solving (2.26) across one switching period using the above initial conditions, yields the following output voltage:

$$v_{\mathrm{C}}(t) = \begin{cases} e^{s_r t}\left(A\cosh(s_m t) + \frac{B}{s_m}\sinh(s_m t)\right) + \mathrm{V_{IN}} & 0 < t \le D\mathrm{T_s} \\ e^{s_r t}\left(A'\cosh(s_m t) + \frac{B'}{s_m}\sinh(s_m t)\right) & D\mathrm{T_s} < t \le \mathrm{T_s} \end{cases} \tag{2.31}$$

where:

$$A = v_{\mathrm{C}}(0) - \mathrm{V_{IN}}$$

$$B = v'_{\mathrm{C}}(0) - s_r(v_{\mathrm{C}}(0) - \mathrm{V_{IN}})$$

$$A' = A + \mathrm{V_{IN}}e^{-s_r D\mathrm{T_s}}\left(\cosh(s_m D\mathrm{T_s}) + \frac{s_r}{s_m}\sinh(s_m D\mathrm{T_s})\right)$$

$$B' = B - \mathrm{V_{IN}}e^{-s_r D\mathrm{T_s}}\left(s_r\cosh(s_m D\mathrm{T_s}) + s_m\sinh(s_m D\mathrm{T_s})\right)$$

To validate the accuracy of the closed-form expression for the output voltage waveform given by (2.31), it is compared with a simulated steady-state waveform generated using PSIM in Fig. 2.3 for an example buck converter design. The LBSM and PSIM simulation results are identical, since they both accurately solve the same differential equation – the simulation software solves the differential equation numerically from period to period until it reaches steady-state, while LBSM solves it analytically across only one period. Figure 2.3 also plots the output voltage waveform of the buck converter obtained using small ripple approximation. The output voltage waveform, and the associated voltage ripple, predicted by small ripple approximation is quite different from the actual one predicted by numerical simulation and LBSM. Hence, the waveform obtained using LBSM can be used to analyze and design the buck converter more accurately than small ripple approximation. The values of normalized peak-to-peak output voltage ripple as

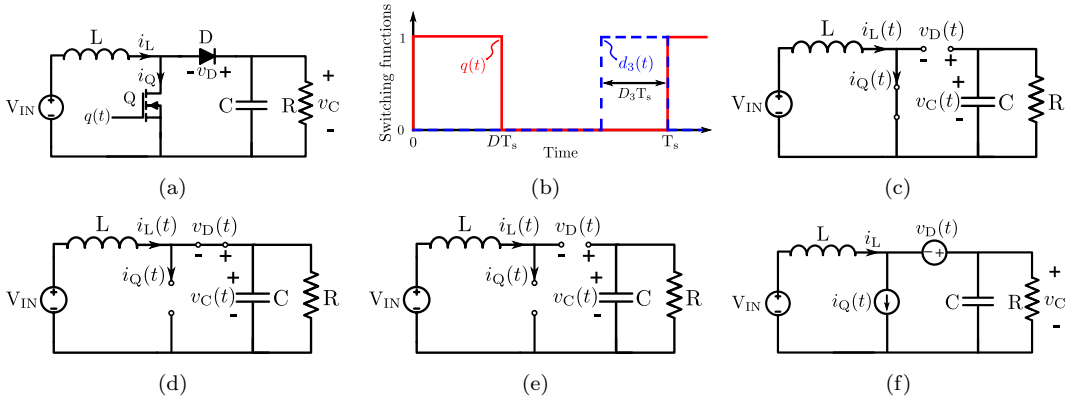


Fig. 2.5: Boost converter: (a) topology, (b) switching function q(t) which serves as the control signal for the active switch, along with a switching function $d_3(t)$ used to model the third subinterval under DCM operation, (c) equivalent circuit during first subinterval $q(t) = 1$ and $d_3(t) = 0$, (d) equivalent circuit during second subinterval $q(t) = 0$ and $d_3(t) = 0$, (e) equivalent circuit during third subinterval if under DCM operation $q(t) = 0$ and $d_3(t) = 1$, and (f) switched-mode equivalent circuit model.

predicted by LBSM and small ripple approximation are compared for a range of load resistances in Fig. 2.4. It is interesting to note that the output voltage ripple predicted by small ripple approximation is independent of load resistance (and equal to 9.4% in this example), while it depends on the load resistance according to LBSM. For small values of load resistance (where s_1 and s_2 in (2.28) are real), the output voltage ripple is substantially smaller than what is predicted by small ripple approximation. This makes sense as the output filter of the buck converter is highly damped under these conditions. Therefore, if the buck converter does not have to be operated under light loading, the LBSM based design could prevent output capacitor over-design and result in improved power density of the converter.

In the above example, the buck converter is assumed to be operating in CCM, so the duration of each subinterval is known from the active switch's control signal. In cases where subinterval durations cannot be simply determined from switch control signals (e.g., buck converter operating in DCM), the subinterval durations will need to be included in LBSM as additional unknown variables, and their values determined by imposing appropriate constraints on the resulting waveform expressions. For example, in the case of a buck converter operating in DCM, the time at which the inductor current becomes zero can be defined as an unknown variable before applying LBSM. After the inductor current waveform has been determined using LBSM, its expression can be set equal to zero and solved for the unknown zero crossing time. The obtained equation is

non-linear, but can be solved numerically.

2.2.2 Interior Switch-Network Converters

In interior switch-network converters, where switching action reconfigures the interconnection between the converter's energy storage elements, the voltage across and the current through at least some switches depends on both the energy storage elements and the actual/equivalent sources connected at the input/output ports of the converter. These interior switches (or switch networks) cannot simply be replaced by independent voltage or current sources with values determined solely from the actual/equivalent sources connected at the input/output ports. Hence, the approach presented to model edge switch-network converters will not work for this class of converters. Instead, an additional initial step (M0) must be introduced, and the remaining steps appropriately modified, to enable interior switch-network converters to be modeled in the form of an ODE, as given below:

M0) Determine analytical expressions for either the current through or the voltage across each interior switch of the converter across all subintervals under steady-state operation using the following procedure: for each subinterval of the converter, starting with the first subinterval, solve the linear circuit for that subinterval to determine analytical expressions for the currents through the switches which are closed during the first subinterval, and for the voltages across the switches which are open during the first subinterval, in terms of the known circuit parameters, any unknown subinterval durations, and one state variable of the converter with an unknown initial value at the start of the first subinterval.

M1) Create an equivalent circuit model for the converter by replacing the interior switches whose currents were determined in step (M0) by periodic discontinuous independent current sources with values given by the above determined analytical expressions, and the switches whose voltages were determined in step (M0) by periodic discontinuous independent voltage sources with values given by the above determined analytical expressions. Any non-interior switches, or switch networks, can still be replaced by independent voltage or current sources with values determined solely from the actual/equivalent sources connected at the input/output ports.

M2) Determine the converter's governing differential equation from the equivalent circuit model in terms of the state variable selected in step (M0). This will be a constant-coefficient non-homogeneous ODE of the form of (2.1).

As an example, consider the boost converter shown in Fig. 2.5(a). Unlike the buck converter, switching action reconfigures the interconnection between its inductor and capacitor (i.e., its energy storage elements). Therefore, to model the boost converter in the form of (2.1) the procedure outlined for the interior switch-network converter has to be followed. Following step (M0), and assuming that the converter is operating in CCM with its active switch controlled by the switching function $q(t)$ shown in Fig. 2.5(b), the boost converter reduces to one of the two linear equivalent circuits shown in Fig. 2.5(c) and Fig. 2.5(d) in its two subintervals. Hence, the voltage across the diode D is given by $v_{\mathrm{D}}(t) = q(t)v_{\mathrm{C}}(t)$ and the current through the transistor Q is given by $i_{\mathrm{Q}}(t) = q(t)i_{\mathrm{L}}(t)$. Furthermore, the equivalent circuit of Fig. 2.5(c) can be solved to determine $v_{\mathrm{C}}(t)$ and $i_{\mathrm{L}}(t)$ for the subinterval corresponding to $q(t) = 1$:

$$v_{\mathrm{C}}(t) = v_{\mathrm{C}}(0)e^{-\frac{t}{\mathrm{RC}}}, \tag{2.32}$$

$$i_{\mathrm{L}}(t) = \frac{\mathrm{V_{IN}}}{\mathrm{L}}t + \mathrm{C}v'_{\mathrm{C}}(0) + \frac{v_{\mathrm{C}}(0)}{\mathrm{R}}, \tag{2.33}$$

resulting in:

$$v_{\mathrm{D}}(t) = q(t)\left(v_{\mathrm{C}}(0)e^{-\frac{t}{\mathrm{RC}}}\right), \tag{2.34}$$

$$i_{\mathrm{Q}}(t) = q(t)\left(\tfrac{\mathrm{V_{IN}}}{\mathrm{L}}t + \mathrm{C}v'_{\mathrm{C}}(0) + \tfrac{v_{\mathrm{C}}(0)}{\mathrm{R}}\right). \tag{2.35}$$

Following step (M1), the boost converter can now be modeled by the circuit shown in Fig. 2.5(f), where the values of the independent voltage and current source are given by (2.34) and (2.35), respectively. Finally, following step (M2), the steady-state behavior of the boost converter can be described by the following constant coefficient ODE which is of the form of (2.1):

$$\mathrm{LC}\frac{d^2v_{\mathrm{C}}}{dt^2} + \frac{\mathrm{L}}{\mathrm{R}}\frac{dv_C}{dt} + v_{\mathrm{C}}(t) = \mathrm{V_{IN}} + v_{\mathrm{D}}(t) - \mathrm{L}\frac{di_{\mathrm{Q}}(t)}{dt} = f(t) \tag{2.36}$$

Here, the periodic and discontinuous input of the ODE $f(t)$ $\left(= \mathrm{V_{IN}} + v_{\mathrm{D}}(t) - \mathrm{L}\frac{di_{\mathrm{Q}}(t)}{dt}\right)$ is given by:

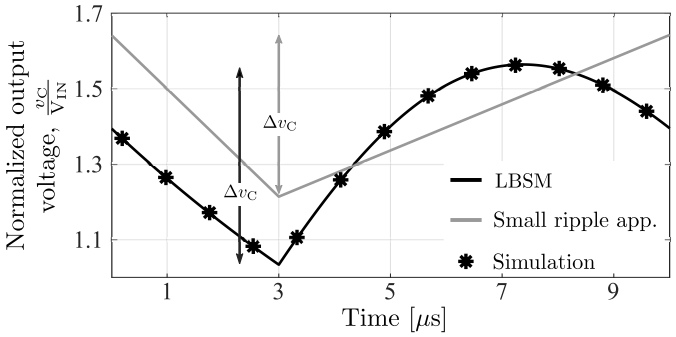


Fig. 2.6: Comparison of normalized output voltage waveform obtained using LBSM, numerical simulation, and small ripple approximation for a boost converter with the following parameter values: $\mathrm{L} = 1\,\mu\mathrm{H}$, $\mathrm{C} = 10\,\mu\mathrm{F}$, $\mathrm{R} = 1\,\Omega$, $D = 0.3$ and $f_s = 100\,\mathrm{kHz}$. Here, $\Delta v_\mathrm{C}/\mathrm{V_C}$ is 39% and 30% for the LBSM and small ripple approximation waveforms, respectively.

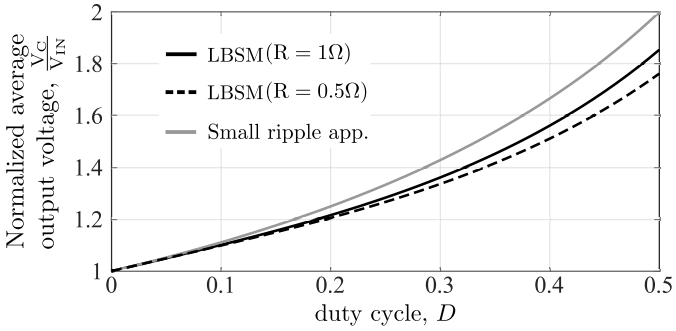


Fig. 2.7: Comparison of normalized average output voltage $\mathrm{V_C}/\mathrm{V_{IN}}$ (i.e., voltage gain) as function of duty cycle obtained using LBSM and small ripple approximation for the example boost converter of Fig. 2.6.

$$f(t) = \begin{cases} v_\mathrm{C}(0)e^{-\frac{t}{\mathrm{RC}}} - \left(\mathrm{LC}v'_\mathrm{C}(0) + \frac{\mathrm{L}}{\mathrm{R}}v_\mathrm{C}(0)\right)\delta(t) & 0 \le t < D\mathrm{T_s} \\ \mathrm{V_{IN}} + \left(\mathrm{LC}v'_\mathrm{C}(0) + \frac{\mathrm{L}}{\mathrm{R}}v_\mathrm{C}(0) + \mathrm{V_{IN}}D\mathrm{T_s}\right)\delta(t - D\mathrm{T_s}) & D\mathrm{T_s} \le t < T \end{cases} \tag{2.37}$$

In (2.37), $\delta(t)$ is an impulse function that appears due to the differentiation of the discontinuous function $q(t)$.

Now, the procedure given in Section 2.1.3 can be used to find the steady-state solution of (2.36). Following step (S1), $F(s)$ (the Laplace transform of $f(t)$) is obtained from (2.37). Following step (S2), the roots of the characteristic polynomial associated with (2.36) are given by:

$$s_{1,2} = \frac{1}{2\mathrm{RC}}\left(-1 \pm \sqrt{1 - 4\frac{\mathrm{R^2C}}{\mathrm{L}}}\right) \equiv s_r \pm s_m. \tag{2.38}$$

Next, following step (S3), and formulating $Q(s_k) = F(s_k)$ for $k = 1, 2$ in the form of

(2.24) and solving it for the initial conditions gives the following steady-state initial conditions:

$$\begin{aligned} v_{\mathrm{C}}(0) &= \tfrac{B(s_1)C(s_2)-C(s_1)B(s_2)}{A(s_2)B(s_1)-B(s_2)A(s_1)}, \\ v'_{\mathrm{C}}(0) &= \tfrac{C(s_1)A(s_2)-A(s_1)C(s_2)}{A(s_2)B(s_1)-B(s_2)A(s_1)}, \end{aligned} \tag{2.39}$$

where $A(s) = \frac{\mathrm{L}}{\mathrm{R}}\left(1-e^{-sD\mathrm{T_s}}\right) + \frac{1-e^{-s\mathrm{T_s}}}{s} - \frac{1-e^{-\left(s+\frac{1}{\mathrm{RC}}\right)D\mathrm{T_s}}}{s+\frac{1}{\mathrm{RC}}}$, $B(s) = \mathrm{LC}\left(e^{-s\mathrm{T_s}} - e^{-sD\mathrm{T_s}}\right)$ and $C(s) = \frac{\mathrm{V_{IN}}}{s}\left(e^{-sD\mathrm{T_s}} - e^{-s\mathrm{T_s}}\right) + \mathrm{V_{IN}}D\mathrm{T_s}e^{-sD\mathrm{T_s}}$. Finally, following step (S4), and solving (2.36) across one switching period using the obtained initial conditions, yields the following output voltage:

$$v_{\mathrm{C}}(t) = \begin{cases} v_{\mathrm{C}}(0)e^{-\frac{t}{\mathrm{RC}}} & 0 \le t < D\mathrm{T_s} \\ \mathrm{V_{IN}} + e^{s_r(t-D\mathrm{T_s})}\Big[k_1\cosh\left(s_m(t-D\mathrm{T_s})\right) + & \\ \qquad \frac{k_2}{s_m}\sinh\left(s_m(t-D\mathrm{T_s})\right)\Big], & D\mathrm{T_s} \le t < T_s \end{cases} \tag{2.40}$$

where

$$k_1 = \left(v_{\mathrm{C}}(0)e^{-D\mathrm{T_s}/\mathrm{RC}} - \mathrm{V_{IN}}\right)$$

$$k_2 = \frac{\mathrm{V_{IN}}D\mathrm{T_s}}{\mathrm{LC}} + \frac{v_{\mathrm{C}}(0)}{\mathrm{RC}} + v'_{\mathrm{C}}(0) + s_r\left(\mathrm{V_{IN}} + v_{\mathrm{C}}(0)e^{-D\mathrm{T_s}/\mathrm{RC}}\right)$$

As expected $v_{\mathrm{C}}(t)$ has a first order response for $0 \le t < D\mathrm{T_s}$ as the inductor and capacitor are disconnected during the first subinterval. To validate the accuracy of the closed-form expression for the output voltage waveform given by (2.40), it is compared with a simulated steady-state waveform generated using PSIM in Fig. 2.6 for an example boost converter design. The LBSM and PSIM results are identical. Figure 2.6 also plots the output voltage waveform of the boost converter obtained using small ripple approximation. The output voltage waveform, and the associated voltage ripple, predicted by small ripple approximation is quite different from the actual one predicted by numerical simulation and LBSM. Hence, the waveform obtained using LBSM can be used to analyze and design the boost converter more accurately than small ripple approximation.

The values of normalized average output voltage (i.e., voltage gain) as predicted by LBSM and small ripple approximation are compared for a range of duty cycle in Fig. 2.7. It is interesting to note that small ripple approximation overestimates the voltage gain.

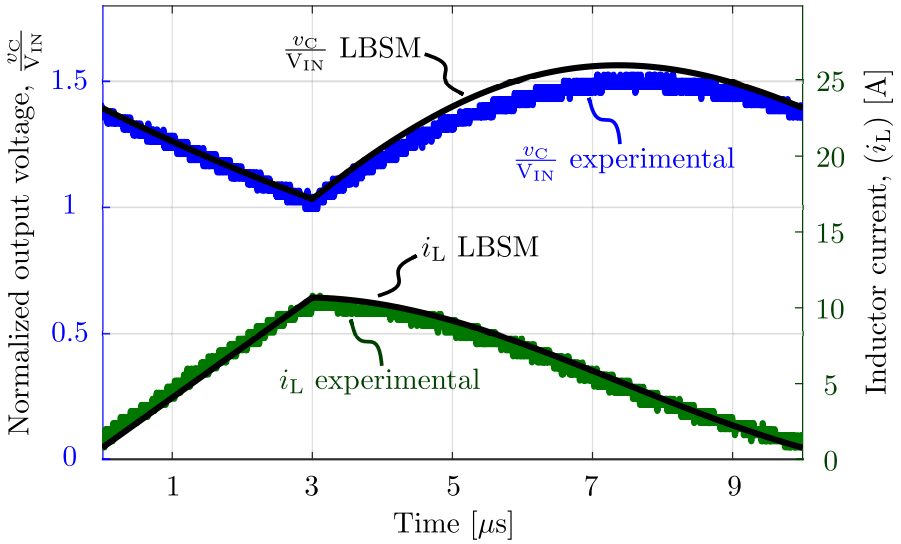


Fig. 2.8: Comparison of normalized output voltage (v_C/V_{IN}) and inductor current (i_L) waveforms obtained using LBSM and experimental measurement for a boost converter operating in continuous conduction mode (CCM) with following parameter values: $V_{IN} = 3.3$ V, L = 1 μH, C = 10 μF, R = 1 Ω, $D = 0.3$ and $f_s = 100$ kHz.

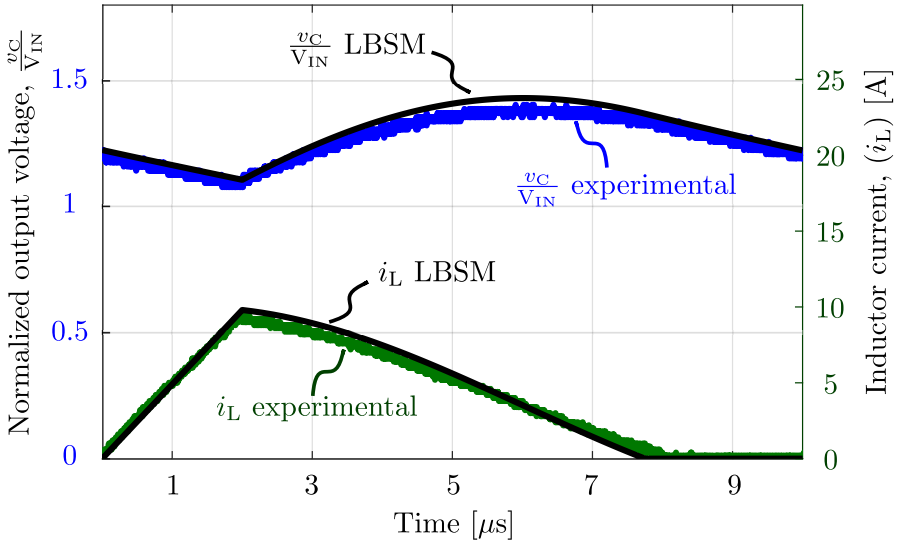


Fig. 2.9: Comparison of normalized output voltage (v_C/V_{IN}) and inductor current (i_L) waveforms obtained using LBSM and experimental measurement for a boost converter operating in discontinuous conduction mode (DCM) with following parameter values: $V_{IN} = 5$ V, L = 1 μH, C = 10 μF, R = 2 Ω, $D = 0.2$ and $f_s = 100$ kHz.

Furthermore, small ripple approximation does not predict the dependence of voltage gain on load resistance. In reality, the voltage gain decreases with increased loading and this decrease is more pronounced at larger duty cycles, as can be seen from Fig. 2.7.

To experimentally validate the waveforms predicted by LBSM for the boost converter operating in CCM, a boost converter is built using the Texas Instruments LMG5200EVM-02 GaN power stage evaluation board. The parameter values for this prototyped boost converter are: $\mathrm{V_{IN}} = 3.3$ V, L = 1 μH, C = 10 μF, R = 1 Ω, $D = 0.3$ and $f_\mathrm{s} = 100$ kHz. The experimentally measured output voltage and inductor current waveforms for the boost converter operating in CCM are compared with the LBSM predicted waveforms in Fig. 2.8. There is a good match in the shape of the LBSM and the experimental waveforms. The slight discrepancy between these waveforms is due to the losses in the experimental prototype, which have not been accounted for in the theoretical analysis.

LBSM can also model the boost converter under DCM operation. Under this operating mode, the boost converter of Fig. 2.5(a) has three subintervals, the first two of which are identical to the subintervals under CCM operation. To model the third subinterval, a new switching function $d_3(t)$ is introduced, as shown in Fig. 2.5(b). The duration of this third subinterval ($D_3\mathrm{T_s}$) is not known a priori, and will have to be determined by LBSM. Again following the modeling procedure for interior switch-network converters, starting with step (M0), the boost converter under DCM operation reduces to one of the three linear equivalent circuits shown in Fig. 2.5(c), Fig. 2.5(d), and Fig. 2.5(e) in its three subintervals. Hence, the voltage across the diode D is given by $v_\mathrm{D}(t) = q(t)\, v_\mathrm{C}(t) + d_3(t)\,(v_\mathrm{C}(t) - \mathrm{V_{IN}})$ and the current through the transistor Q is given by $i_\mathrm{Q}(t) = q(t)\, i_\mathrm{L}(t)$. Furthermore, the equivalent circuits of Fig. 2.5(c) and Fig. 2.5(e) can be solved to determine $v_\mathrm{C}(t)$ and $i_\mathrm{L}(t)$ during the first ($q(t) = 1$ and $d_3(t) = 0$) and the third ($q(t) = 0$ and $d_3(t) = 1$) subintervals:

$$v_\mathrm{C}(t) = \begin{cases} v_\mathrm{C}(0)e^{-\frac{t}{\mathrm{RC}}} & \text{if} \quad q(t) = 1 \text{ and } d_3(t) = 0, \\ v_\mathrm{C}(0)e^{-\frac{t-\mathrm{T_s}}{\mathrm{RC}}} & \text{if} \quad q(t) = 0 \text{ and } d_3(t) = 1, \end{cases} \tag{2.41}$$

$$i_\mathrm{L}(t) = \begin{cases} \frac{\mathrm{V_{IN}}}{\mathrm{L}}t & \text{if} \quad q(t) = 1 \text{ and } d_3(t) = 0, \\ 0 & \text{if} \quad q(t) = 0 \text{ and } d_3(t) = 1, \end{cases} \tag{2.42}$$

resulting in:

$$v_{\mathrm{D}}(t) = q(t)\left(v_{\mathrm{C}}(0)\, e^{-\frac{t}{\mathrm{RC}}}\right) + d_3(t)\left(v_{\mathrm{C}}(0)\, e^{-\frac{t-\mathrm{T_s}}{\mathrm{RC}}} - \mathrm{V_{IN}}\right), \tag{2.43}$$

$$i_{\mathrm{Q}}(t) = q(t)\,\frac{\mathrm{V_{IN}}}{\mathrm{L}}t. \tag{2.44}$$

Following step (M1), the boost converter in DCM can also be modeled by the circuit shown in Fig. 2.5(f), but with the values of the independent voltage and current source given by (2.43) and (2.44), respectively. Finally, following step (M2), the steady-state behavior of the boost converter is again described by (2.36), however, with input $f(t)$ $\left(= \mathrm{V_{IN}} + v_{\mathrm{D}}(t) - \mathrm{L}\frac{di_{\mathrm{Q}}(t)}{dt}\right)$ given by:

$$f(t) = \begin{cases} v_{\mathrm{C}}(0)\, e^{-\frac{t}{\mathrm{RC}}} & 0 \le t < D\mathrm{T_s} \\ \mathrm{V_{IN}} + \mathrm{V_{IN}} D\mathrm{T_s}\delta(t - D\mathrm{T_s}) & D\mathrm{T_s} \le t < (1-D_3)\,\mathrm{T_s} \\ v_{\mathrm{C}}(0)\, e^{-\frac{t-\mathrm{T_s}}{\mathrm{RC}}} & (1-D_3)\,\mathrm{T_s} \le t < \mathrm{T_s} \end{cases} \tag{2.45}$$

In the first step (S1) towards finding the steady-state solution of the ODE modeling the boost converter in DCM, $F(s)$ is obtained from (2.45). In the second step (S2), the roots of the characteristic polynomial come out to be the same as those for the boost converter in CCM as given by (2.38). In step (S3), by formulating $Q(s_k) = F(s_k)$ for $k = 1, 2$ and solving it for the initial conditions gives:

$$v_{\mathrm{C}}(0) = \frac{B(s_1)C(s_2) - C(s_1)B(s_2)}{A(s_2)B(s_1) - B(s_2)A(s_1)}, v'_{\mathrm{C}}(0) = \frac{C(s_1)A(s_2) - A(s_1)C(s_2)}{A(s_2)B(s_1) - B(s_2)A(s_1)}, \tag{2.46}$$

where:

$$A(s) = \frac{1 - e^{-s\mathrm{T_s}}}{s} - \left(e^{\left(s+\frac{1}{\mathrm{RC}}\right)(1-D_3)\mathrm{T_s}}\right) / \left(s + \frac{1}{\mathrm{RC}}\right)$$

$$B(s) = \mathrm{LC}\left(e^{-s\mathrm{T_s}} - 1\right)$$

$$C(s) = \frac{\mathrm{V_{IN}}}{s}\left(e^{-s\mathrm{DT_s}} - e^{-s(1-D_3\mathrm{T_s})}\right) + \mathrm{V_{IN}} D\mathrm{T_s} e^{-s\mathrm{DT_s}}$$

Note that both $v_{\mathrm{C}}(0)$ and $v'_{\mathrm{C}}(0)$ are in terms of D_3 which is unknown. However, under DCM operation, the steady state initial conditions $v_{\mathrm{C}}(0)$ and $v'_{\mathrm{C}}(0)$ are not independent

of each other and are related by:

$$\mathrm{C}v'_{\mathrm{C}}(0) = -v_{\mathrm{C}}(0)/\mathrm{R}, \tag{2.47}$$

as in the third subinterval the capacitor current is equal to the negative of the load current, and the end of the third subinterval coincides with the start of the first subinterval (i.e., this current relationship holds at $t = 0$). Substituting (2.46) into (2.47), yields the following equation for D_3:

$$\begin{aligned} &-\mathrm{u}_1(s_1)\, e^{s_1(1-D_3)} \quad &&+\mathrm{u}_1(s_2)\, e^{s_2(1-D_3)} \\ &-\mathrm{u}_2(s_1)\, e^{-s_1(1-D_3)} \quad &&+\mathrm{u}_2(s_2)\, e^{-s_2(1-D_3)} = \mathrm{u}_3(s_1, s_2), \end{aligned} \tag{2.48}$$

where u_1, u_2, and u_3 are given at the bottom of the page. As (2.48) is a transcendental equation it does not have a closed form solution; however, it can be solved numerically for D_3. Once D_3 is computed, it can be substituted into (2.46) to determine the steady-state initial conditions for the boost converter in DCM. Finally, following step (S4), and solving (2.36) across one switching period using the obtained initial conditions, yields the following output voltage:

$$\mathrm{u}_1(s) = \frac{2e^{\left(-\mathrm{T_s}\left(sD-\left(s+\frac{1}{\mathrm{RC}}\right)\right)\right)}(sD\mathrm{T_s}+1)}{s(e^{s\mathrm{T_s}}-1)(e^{-s\mathrm{T_s}}-1)},$$

$$\mathrm{u}_2(s) = \left(2\mathrm{LC}\left(s+\tfrac{1}{\mathrm{RC}}\right)+\frac{2\left(e^{\left(s+\frac{1}{\mathrm{RC}}\right)\mathrm{T_s}}+e^{sD\mathrm{T_s}}-1\right)}{s\left(e^{\left(s+\frac{1}{\mathrm{RC}}\right)\mathrm{T_s}}-1\right)}\right)\Big/\left(s\left(e^{-s\mathrm{T_s}}-1\right)\right),$$

$$\begin{aligned} &\mathrm{u}_3(s_1, s_2) = \\ &-\left(\mathrm{LC}(s_1 - s_2) + \frac{e^{-s_2\mathrm{T_s}}+e^{s_1 D\mathrm{T_s}}-1}{s_1\left(e^{-s_1\mathrm{T_s}}-1\right)} - \frac{e^{-s_1\mathrm{T_s}}+e^{s_2 D\mathrm{T_s}}-1}{s_2\left(e^{-s_2\mathrm{T_s}}-1\right)}\right) \times \\ &\left(\frac{D\mathrm{T_s}e^{-s_1 D\mathrm{T_s}}}{e^{-s_1\mathrm{T_s}}-1} + \frac{D\mathrm{T_s}e^{-s_2 D\mathrm{T_s}}}{e^{-s_2\mathrm{T_s}}-1} + \frac{e^{-s_1 D\mathrm{T_s}}}{s_1\left(e^{-s_1\mathrm{T_s}}-1\right)} + \frac{e^{-s_2 D\mathrm{T_s}}}{s_2\left(e^{-s_2\mathrm{T_s}}-1\right)}\right) \\ &+\left(\mathrm{LC}(s_1 + s_2) - \frac{e^{-s_2\mathrm{T_s}}+e^{s_1 D\mathrm{T_s}}-1}{s_1\left(e^{-s_1\mathrm{T_s}}-1\right)} - \frac{e^{-s_1\mathrm{T_s}}+e^{s_2 D\mathrm{T_s}}-1}{s_2\left(e^{-s_2\mathrm{T_s}}-1\right)}\right) \times \\ &\left(\frac{D\mathrm{T_s}e^{-s_1 D\mathrm{T_s}}}{e^{-s_1\mathrm{T_s}}-1} - \frac{D\mathrm{T_s}e^{-s_2 D\mathrm{T_s}}}{e^{-s_2\mathrm{T_s}}-1} + \frac{e^{-s_1 D\mathrm{T_s}}}{s_1\left(e^{-s_1\mathrm{T_s}}-1\right)} - \frac{e^{-s_2 D\mathrm{T_s}}}{s_2\left(e^{-s_2\mathrm{T_s}}-1\right)}\right) \\ &+\frac{2e^{\frac{\mathrm{T_s}}{\mathrm{RC}}}}{(s_2)^2\left(e^{-s_2\mathrm{T_s}}-1\right)\left(e^{-s_1\mathrm{T_s}}-1\right)} - \frac{2e^{\frac{\mathrm{T_s}}{\mathrm{RC}}}}{(s_1)^2\left(e^{-s_2\mathrm{T_s}}-1\right)\left(e^{-s_1\mathrm{T_s}}-1\right)}. \end{aligned}$$

$$v_{\mathrm{C}}(t) = \begin{cases} v_{\mathrm{C}}(0)\, e^{-\frac{t}{\mathrm{RC}}} & 0 \le t < D\mathrm{T_s} \\ \mathrm{V_{IN}} + e^{s_r(t-D\mathrm{T_s})}\left[k_1 \cosh\left(s_m(t-D\mathrm{T_s})\right) + \right. & \\ \qquad \left. \dfrac{k_2}{s_m} \sinh\left(s_m(t-D\mathrm{T_s})\right)\right] & D\mathrm{T_s} \le t < D_3'\mathrm{T_s} \\ v_{\mathrm{C}}(0)\, e^{-\frac{t-\mathrm{T_s}}{\mathrm{RC}}} & D_3'\mathrm{T_s} \le t < \mathrm{T_s} \end{cases} \tag{2.49}$$

where $k_1 = \left(v_{\mathrm{C}}(0)\, e^{-D\mathrm{T_s}/\mathrm{RC}} - \mathrm{V_{IN}}\right)$, $k_2 = \frac{\mathrm{V_{IN}} D\mathrm{T_s}}{\mathrm{LC}} + s_r\left(\mathrm{V_{IN}} + v_{\mathrm{C}}(0)\, e^{-D\mathrm{T_s}/\mathrm{RC}}\right)$, and $D_3' = 1 - D_3$. The inductor current under DCM operation can also be obtained using (2.42) in first and third subintervals and (2.49) in the second subinterval. The LBSM predicted output voltage and inductor current waveforms for a boost converter operating under DCM are compared with experimental results in Fig. 2.9, which shows a good match between the LBSM predicted and experimental waveforms.

In addition to dc-dc converters, LBSM can also be used to accurately predict the waveforms of dc-ac and ac-dc converters. This is because LBSM can predict waveform dynamics within a switching period irrespective of whether the external (output or input) voltages are constant (as in dc-dc converters) or time varying (as in dc-ac and ac-dc converters). When the external voltages are time varying, the periodicity used in LBSM must be selected so as to capture the periodicity of its steady-state waveforms. In the case when the output (or input) ac voltage of the dc-ac (or ac-dc) converter has the same periodicity as the converter's switching period (such as in resonant inverters and line-commutated rectifiers), then the steady-state waveforms of the converter will be periodic with a period equal to its switching period; and in this case the periodicity used in LBSM is simply the switching period. On the other hand, if the output (or input) ac voltage of the dc-ac (or ac-dc) converter varies more slowly than its switching period (such as in line-interfaced high-frequency inverters and power factor correction rectifiers), then, assuming an integer relationship between the switching and the external ac frequency, the steady-state waveforms of the converter will be periodic with a period equal to the period of the external ac voltage; and in this case the periodicity used in LBSM is the period of the external ac voltage. In this later case, LBSM will involve a relatively large number of subintervals, and the state-space formulation of LBSM (as given in Section 2.4) will be easier to utilize. The application of LBSM to an example of each type of dc-ac converter is demonstrated in next section.

2.3 Application of LBSM to DC-AC and AC-DC Converters

This section demonstrates the application of LBSM to two dc-ac converters, one of which is bidirectional and can also be considered as an ac-dc converter. As an example of a dc-ac converter in which its steady-state waveforms are periodic with a period equal to its switching period, consider the series resonant inverter shown in Fig. 2.10(a), which is commonly used for induction heating applications. An ODE for this converter can be derived using steps (M1) and (M2) of LBSM for edge-switch network converters:

$$\mathrm{LC}\frac{d^2 v_\mathrm{C}}{dt^2} + \mathrm{RC}\frac{dv_\mathrm{C}}{dt} + v_\mathrm{C}(t) = v_i(t), \tag{2.50}$$

where $v_i\,(t)$ is the rectangular switch node waveform. This ODE is similar to (2.26), but with different roots for its characteristic polynomial:

$$s_{1,2} = \tfrac{R}{2\mathrm{L}}\left(-1 \pm \sqrt{1 - 4\tfrac{\mathrm{L}}{\mathrm{R}^2\mathrm{C}}}\right) \equiv s_r \pm s_m. \tag{2.51}$$

Following steps (S1) through (S4) for (2.50), the steady-state capacitor voltage is identical to the expression given by (2.31) except with the values of s_r and s_m replaced by those given in (2.51). The inductor current can be obtained by differentiating (2.31). The LBSM predicted capacitor voltage and inductor current waveforms for an example series resonant inverter are compared with PSIM simulations in Fig. 2.10(b) and Fig. 2.10(c), which show a good match between the LBSM predicted and the simulated waveforms.

As an example of a dc-ac converter in which its steady-state waveforms are periodic with a period equal to the period of a more slowly varying external ac voltage, consider the bidirectional line-interfaced high-frequency dc-ac converter shown in Fig. 2.11(a). Here, the line voltage is represented by a sinusoidal ac voltage source $v_g\,(t)\ (= \mathrm{V}_g \sin(2\pi f_g t - \phi_g))$ with amplitude V_g, frequency f_g, and phase ϕ_g. The switching frequency of the converter is f_s, and the converter uses a unipolar sinusoidal PWM signal $m\,(t)\ (= m_a \sin(2\pi f_g t))$ with an amplitude modulation ratio m_a $(0 \leq m_a \leq 1)$ and a frequency modulation ratio $m_f\left(= \frac{f_s}{f_g}\right)$. The PWM is implemented digitally with $m\,(t)$ discretized in time at a frequency of $2f_s$. An ODE for this converter can be derived using steps (M1) and (M2) of LBSM for edge-switch network converters:

$$\mathrm{L}\frac{di_{\mathrm{L}}}{dt} = v_i\left(t\right) - v_g\left(t\right) \equiv f\left(t\right), \tag{2.52}$$

where $v_i\left(t\right)$ is the rectangular waveform generated by the full-bridge. Assuming that the period of $v_g\left(t\right)$ is an integer multiple of the switching period (i.e., the frequency modulation ratio m_f is an integer), the input $f(t)$ will be periodic with frequency f_g. To determine the converter's steady-state waveforms from this ODE, first $F\left(s\right) = \mathcal{L}\{v_i\left(t\right) - v_g\left(t\right)\}$ is determined following (S1); next following (S2), the root of the characteristic polynomial $P\left(s\right)$ $(= Ls)$ is found to be $s = 0$; then formulating $Q(s = 0) = F\left(s = 0\right)$ following (S3) and solving it gives the steady-state initial condition for the inductor current:

$$i_{\mathrm{L}}\left(0\right) = \frac{\mathrm{V}_g}{\omega_g \mathrm{L}}\cos\left(\phi_g\right) - \frac{\mathrm{m_a V_{IN}}}{\omega_g \mathrm{L}}\frac{\pi}{2m_f}\sum_{n=0}^{m_f-1}\sin\left(n\frac{\pi}{m_f}\right), \tag{2.53}$$

where $\omega_g = 2\pi f_g$. Finally, solving (2.52) across one line-period (i.e., $1/f_g$) results in:

$$\begin{aligned} i_{\mathrm{L}}\left(t\right) \quad &= i_{\mathrm{L}}\left(0\right) + \tfrac{\mathrm{V_g}}{\omega_g \mathrm{L}}\cos\left(\phi_g\right) - \tfrac{\mathrm{V_g}}{\omega_g \mathrm{L}}\cos\left(\omega_g t - \phi_g\right) \\ &+ \tfrac{\mathrm{V_{IN}}}{\mathrm{L}}\textstyle\sum_{n=0}^{m_f-1} r\left(t - t_{\min}\right) - r\left(t - t_{\max}\right), \end{aligned} \tag{2.54}$$

where

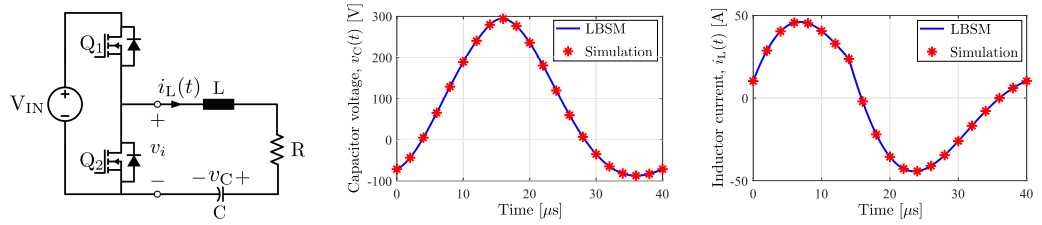
$$t_{\min} = \frac{1}{2f_s}\left(n + 0.5 - 0.5m_a\sin\left(n\frac{\pi}{m_f}\right)\right)$$

$$t_{\max} = \frac{1}{2f_s}\left(n + 0.5 + 0.5m_a\sin\left(n\frac{\pi}{m_f}\right)\right)$$

, and $r\left(t - t_0\right)$ is a ramp function starting at t_0 as defined below:

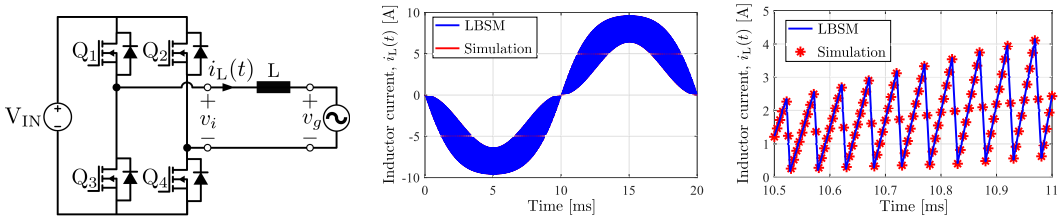
$$r\left(t - t_0\right) = \begin{cases} t - t_0 & t \geq t_0, \\ 0 & t < t_0. \end{cases} \tag{2.55}$$

The LBSM predicted inductor current waveform for an example bidirectional line-interfaced high-frequency dc-ac converter is compared with PSIM simulation across a full line-cycle in Fig. 2.11(b) and across five switching cycles in Fig. 2.11(c). As can be seen there is an excellent match between the LBSM predicted and the simulated waveforms.



(a) (b) (c)

Fig. 2.10: Series resonant inverter: (a) topology, and comparison of its (b) capacitor voltage (v_{C}) and (c) inductor current (i_{L}) waveforms, obtained using LBSM and PSIM simulation with the following parameter values: $\mathrm{V_{IN}} = 230$ V, L $= 25$ μH, C $= 1.44$ μF, R $= 3$ Ω, $f_s = 25$ kHz, and $D = 0.35$.



(a) (b) (c)

Fig. 2.11: Bidirectional line-interfaced high-frequency dc-ac converter: (a) topology, and comparison of its inductor current (i_{L}) waveforms across (b) a full line-cycle and (c) five switching cycles, obtained using LBSM and PSIM simulation with the following parameter values: $f_s = 10$ kHz, $f_g = 50$ Hz, $m_a = 0.8$, $\mathrm{V_{IN}} = 400$ V, $\mathrm{V}_g = 320$ V, and $\phi_g = 0$.

2.4 LBSM Under State-Space Representation

The LBSM has been successfully demonstrated for the single differential equation representation of converters. However, this representation of LBSM can lead to cumbersome mathematical operations in case of higher order converters and converters with complicated inputs. In these cases the state-space representation of the converter can facilitate the application of computational methods to simplify the LBSM calculation. This section describes the Laplace Based Steady-state Modeling (LBSM) technique under the state-space representation of a power converter. The first step of this technique is to model the converter in the following state-space form:

$$\frac{d\boldsymbol{x}}{dt} = \boldsymbol{A}\boldsymbol{x}(t) + \boldsymbol{g}(t), \tag{2.56}$$

where $\boldsymbol{x}(t)$ is the state vector (i.e., a vector of state variables), $\boldsymbol{A}$ is a constant matrix, and $\boldsymbol{g}(t)$ is a periodic and discontinuous vector. The procedure for obtaining this state-space representation depends on whether the power converter is an edge-switch network or an interior-switch network converter.

Edge-switch network converters can be modeled in the form of (2.56) by first deriving the state-space representation of the converter for each of its subintervals in the following form:

$$\frac{d\boldsymbol{x}}{dt} = \boldsymbol{A_i}\boldsymbol{x}(t) + \boldsymbol{B_i}\boldsymbol{u}(t) \quad 1 \leq i \leq m, \tag{2.57}$$

where $\boldsymbol{A_i}$ and $\boldsymbol{B_i}$ are constant matrices dependent on the topology of the converter, $\boldsymbol{u}(t)$ is a vector obtained from the actual or equivalent sources connected at the input and output ports of the converter, and m is the total number of subintervals. The time evolution of the state vector across all its subintervals can now be expressed as:

$$\frac{d\boldsymbol{x}}{dt} = \sum_{i=1}^{m} q_i(t)\boldsymbol{A_i}\boldsymbol{x}(t) + \sum_{i=1}^{m} q_i(t)\boldsymbol{B_i}\boldsymbol{u}(t), \tag{2.58}$$

where $q_i(t)$ is a periodic and discontinuous switching function that equals 1 during the $i-$th subinterval and 0 during all other subintervals, and satisfies $\sum_{i=1}^{m} q_i(t) = 1$. In edge switch-network converters, since switching action does not reconfigure the interconnection between its energy storage elements, all $\boldsymbol{A_i}$ matrices are equal, i.e., $\boldsymbol{A_1} = \boldsymbol{A_2} = \cdots = \boldsymbol{A_m} \equiv \boldsymbol{A_0}$. However, since switching action does reconfigure the connection to the sources at the ports, the $\boldsymbol{B_i}$ matrices are not equal in all subintervals. Hence, the converters state-space representation can be simplified to:

$$\frac{d\boldsymbol{x}}{dt} = \boldsymbol{A_0}\boldsymbol{x}(t) + \sum_{i=1}^{m} q_i(t)\boldsymbol{B_i}\boldsymbol{u}(t). \tag{2.59}$$

This has the desired form of (2.56), where $\boldsymbol{A} = \boldsymbol{A_0}$ and $\boldsymbol{g}(t) = \sum_{i=1}^{m} q_i(t)\boldsymbol{B_i}\boldsymbol{u}(t)$.

To model interior switch-network converters in the form of (2.56) an extra initial step must be included. This step determines an analytical expression for the state vector $\boldsymbol{x}(t)$ in terms of its unknown steady-state initial value $\boldsymbol{X_0}$ using the following equation by starting with the first subinterval [29]:

$$\boldsymbol{x}(t) = \left(\boldsymbol{X_{i-1}} e^{\boldsymbol{A_i}(t-t_{i-1})} + \int_{t_{i-1}}^{t} e^{\boldsymbol{A_i}\tau}\boldsymbol{B_i}\boldsymbol{u}(t-\tau)d\tau \right), \; t_{i-1} \leq t \leq t_i \tag{2.60}$$

where $\boldsymbol{X_{i-1}}$ is the value of the state vector at the beginning of the i-th subinterval (which for $i \geq 2$ is known from the previous subinterval), t_{i-1} is the total time elapsed until the beginning of the i-th subinterval, $\boldsymbol{A_i}$ and $\boldsymbol{B_i}$ are converter matrices for the i-th subinterval as defined in (2.57). Next, the state-space representation of the converter for each of its subintervals in the same form as (2.57) must be derived and used to express the time evolution of the state vector across all subintervals in the same form as (2.58). In interior switch-network converters, since switching action reconfigures the interconnection between its energy storage elements, the $\boldsymbol{A_i}$ matrices are not equal in all subintervals. Also the $\boldsymbol{B_i}$ matrices are not equal. Rewriting $\sum_{i=1}^{m} q_i(t) = 1$ as $q_m(t) = 1 - \sum_{i=1}^{m-1} q_i(t)$, the converters state-space representation can be expressed as:

$$\frac{d\boldsymbol{x}}{dt} = \boldsymbol{A_m}\boldsymbol{x}(t) + \sum_{i=1}^{m-1} q_i(t)\left(\boldsymbol{A_i} - \boldsymbol{A_m}\right)\boldsymbol{x}(t) + \sum_{i=1}^{m} q_i(t)\boldsymbol{B_i}\boldsymbol{u}(t). \tag{2.61}$$

Utilizing (2.60) to eliminate $\boldsymbol{x}(t)$ from the second right-hand-side term of (2.61), and defining $\boldsymbol{\Psi}(t)$ as:

$$\boldsymbol{\Psi}(t) \equiv \sum_{i=1}^{m-1} q_i(t)\left(\boldsymbol{A_i} - \boldsymbol{A_m}\right)\left(\boldsymbol{X_{i-1}}e^{\boldsymbol{A_i}(t-t_{i-1})} + \int_{t_{i-1}}^{t} e^{\boldsymbol{A_i}\tau}\boldsymbol{B_i}\boldsymbol{u}(t-\tau)d\tau\right), \tag{2.62}$$

transforms the converters state-space representation to:

$$\frac{d\boldsymbol{x}}{dt} = \boldsymbol{A_m}\boldsymbol{x}(t) + \boldsymbol{\Psi}(t) + \sum_{i=1}^{m} q_i(t)\boldsymbol{B_i}\boldsymbol{u}(t). \tag{2.63}$$

This has the desired form of (2.56), where $\boldsymbol{A} = \boldsymbol{A_m}$ and $\boldsymbol{g}(t) = \boldsymbol{\Psi}(t) + \sum_{i=1}^{m} q_i(t)\boldsymbol{B_i}\boldsymbol{u}(t)$. It is interesting to note that edge switch-network converters are a special case of interior switch-network converters, as (2.63) reduces to (2.59) when all $\boldsymbol{A_i}$ matrices are the same (and defined equal to $\boldsymbol{A_0}$).

Once the power converter has been modeled in the form of (2.56), steps similar to those described in Section II-A can be used to derive an equation analogous to (2.24):

$$\boldsymbol{X_0} = -\left[\boldsymbol{I} - e^{-\boldsymbol{A}\mathrm{T}}\right]^{-1}\int_{0}^{\mathrm{T}} e^{-\boldsymbol{A}t}\boldsymbol{g}(t)dt, \tag{2.64}$$

where the initial value of the state vector under steady-state operation $\boldsymbol{X_0}$ is analogous to $[x(0), x'(0), \ldots, x^{(n-1)}(0)]$ in (2.24). In the case of edge-switch network converters, $\boldsymbol{X_0}$ can be determined explicitly from (2.64) since all the terms on the right-hand-side

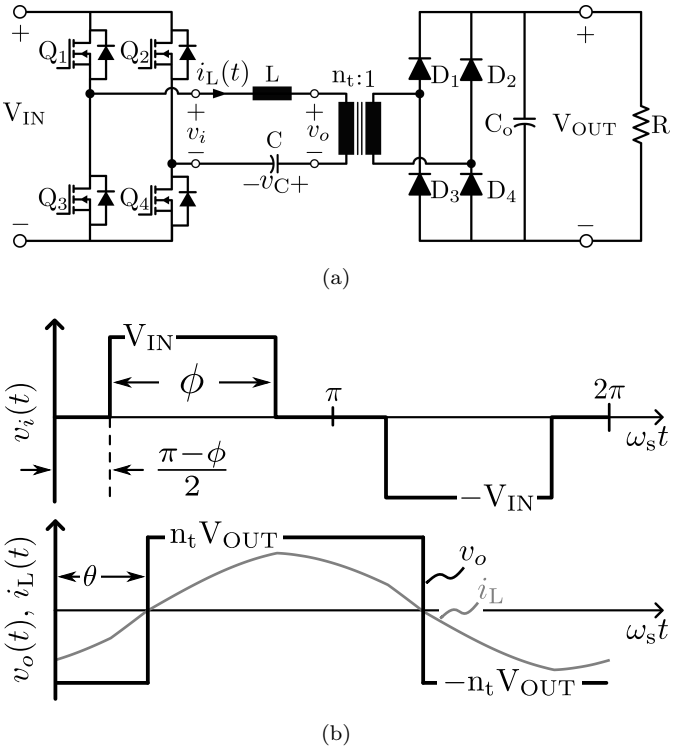


Fig. 2.12: Series Resonant Converter (SRC): (a) topology, and (b) typical waveforms under phase-shift control while maintaining Zero Voltage Switching (ZVS).

of the equation are known. In the case of interior-switch network converters, $\boldsymbol{g}(t)$ is a function of $\boldsymbol{X_0}$ making (2.64) an implicit equation in $\boldsymbol{X_0}$. However, (2.64) is still linear and can be used to solve for $\boldsymbol{X_0}$. Once $\boldsymbol{X_0}$ is known, (2.56) can be solved to find the steady-state solution for $\boldsymbol{x}(t)$ across one switching period.

2.5 Analysis and Design of Series Resonant Converter and Phase-Shift Converter using LBSM

In addition to hard-switching PWM converters, the LBSM technique can also be leveraged for the analysis and design of isolated soft-switching converters. Because of its accuracy LBSM captures the intra-cycle dynamics of such converters, which allows a detailed study of their soft-switching range and performance. Two isolated soft-switching converters, the phase-shift controlled Series Resonant Converter (SRC) and the Phase-Shift Converter (PSC), are investigated in this section.

2.5.1 Phase-Shift Controlled Series Resonant Converter

Figure 2.12(a) shows the topology of the Series Resonant Converter (SRC) and its typical waveforms when operating under phase-shift control while maintaining Zero Voltage Switching (ZVS). An ODE for this converter can be derived using steps (M1) and (M2) of LBSM for edge-switch network converters:

$$\mathrm{LC}\frac{d^2v_\mathrm{C}}{dt^2} + v_\mathrm{C} = v_i(t) - v_o(t), \tag{2.65}$$

where $v_i(t)$ and $v_o(t)$ are as shown in Fig. 2.12(b). In Fig. 2.12(b) the waveform for $v_o(t)$ assumes a large output capacitor $\mathrm{C_o}$, so that the output voltage can be considered constant and an equivalent voltage source connected at the converter's output port can replace the load resistor. Using steps (S1)-(S4) of Section 2.1.3, and under the condition that ZVS is maintained (i.e., $\frac{\pi-\phi}{2} < \theta$), the steady-state solution for (2.65) is:

$$v_\mathrm{C}(t) = \begin{cases} e_1(t) + e_3(t) & 0 \le \omega_s t < \frac{\pi-\phi}{2} \\ e_2(t) + e_3(t) & \frac{\pi-\phi}{2} \le \omega_s t < \theta \\ e_2(t) + e_4(t) & \theta \le \omega_s t < \frac{\pi+\phi}{2} \\ -e_1(t - \frac{\pi}{F\omega_r}) + e_4(t) & \frac{\pi+\phi}{2} \le \omega_s t < \pi, \end{cases} \tag{2.66}$$

where

$$e_1(t) = -\mathrm{V_{IN}}\frac{\sin\left(\frac{\phi}{2F}\right)}{\cos\left(\frac{\pi}{2F}\right)}\sin(\omega_r t)$$

$$e_2(t) = -\mathrm{V_{IN}}\frac{\sin\left(\frac{\phi}{2F}\right)}{\cos\left(\frac{\pi}{2F}\right)}\sin(\omega_r t) + \mathrm{V_{IN}}\left(1 - \cos(\omega_r t - \frac{\pi-\phi}{2F})\right)$$

$$e_3(t) = \mathrm{MV_{IN}}\left[1 + \tan\left(\frac{\pi}{2F}\right)\sin\left(\omega_r t - \frac{\theta}{F}\right) - \cos\left(\omega_r t - \frac{\theta}{F}\right)\right]$$

$$e_4(t) = \mathrm{MV_{IN}}\left[-1 + \tan\left(\frac{\pi}{2F}\right)\sin\left(\omega_r t - \frac{\theta}{F}\right) + \cos\left(\omega_r t - \frac{\theta}{F}\right)\right]$$

Here, $\mathrm{M} = \frac{\mathrm{n_t V_{OUT}}}{\mathrm{V_{IN}}}$ is converter voltage gain without the transformer, $0 \le \phi \le \pi$ is the phase-shift between the two half-bridges of the inverter, $\omega_r = 1/\sqrt{\mathrm{LC}}$ is the radial resonant frequency, ω_s is the radial switching frequency and $F = \omega_s/\omega_r$ is the normalized switching frequency of the converter. An expression for the inductor current i_L can be determined from (2.66) as it is equal to the capacitor current. The two unknowns in

(2.66), voltage gain M and current phase lag angle θ, can be determined by imposing capacitor charge balance and setting i_{L} to zero at $\omega_s t = \theta$:

$$\mathrm{M} = \left(\frac{2F}{\pi Q}\right) \frac{AB\sqrt{A^2+B^2-1}-B^2}{A^2+B^2}, \tag{2.67}$$

$$\theta = \frac{\pi}{2} - F\sin^{-1}\left(\frac{A\sqrt{A^2+B^2-1}-B}{A^2+B^2}\right), \tag{2.68}$$

where

$$A = \sin\left(\frac{\phi}{2F}\right)\tan\left(\frac{\pi}{2F}\right) + \cos\left(\frac{\phi}{2F}\right)$$

$$B = \frac{\left(\pi Q\cos\left(\frac{\pi-\phi}{2F}\right)\right)}{\left(2F\sin\left(\frac{\pi}{2F}\right)\right)}$$

, $Q = {}^{\mathrm{Z}_0}/_{(\mathrm{n_t}^2\mathrm{R})}$ is the loaded quality factor, and $\mathrm{Z}_0 = \sqrt{L/C}$ is the characteristic impedance. By equating θ as given by (2.68) to $\frac{\pi-\phi}{2F}$, the phase-shift associated with the ZVS boundary of the converter ϕ_{ZVS} can be obtained:

$$\phi_{\mathrm{ZVS}} = \pi - 2F\cos^{-1}\left(\left(1+\left(\frac{\pi Q}{2F}\cot\frac{\pi}{2F}\right)^2\right)^{-\frac{1}{2}}\right). \tag{2.69}$$

To evaluate the benefits of the accurate waveforms determined using LBSM, consider an example 100-W constant output power SRC with a constant output voltage $\mathrm{V_{OUT}} = 40\,\mathrm{V}$, in which variations in input voltage from $\mathrm{V_{IN,min}} = 100\,\mathrm{V}$ to $\mathrm{V_{IN,max}} = 330\,\mathrm{V}$ are compensated for using phase-shift control. Assuming the SRC is required to always operate under ZVS, and regulation is done by decreasing the phase-shift from π to ϕ_{ZVS}, the ratio of the SRC voltage gain at π phase-shift to its voltage gain at ϕ_{ZVS} is given by:

$$\frac{\mathrm{M}\left(\phi=\pi\right)}{\mathrm{M}\left(\phi=\phi_{\mathrm{ZVS}}\right)} = \frac{\mathrm{V_{IN,max}}}{\mathrm{V_{IN,min}}}. \tag{2.70}$$

Substituting (2.67) and (2.69) into (2.70) and simplifying gives:

$$\frac{\tan(\gamma)\sqrt{\tan^2(\gamma)+\left(\gamma Q\csc(\gamma)\right)^2}-\gamma Q}{\tan^2(\gamma)-\gamma Q} = \frac{\mathrm{V_{IN,max}}}{\mathrm{V_{IN,min}}}, \tag{2.71}$$

TABLE 2.1: Simulation results for LBSM and FHA based designed SRC with converter operating conditions as: input voltage (V_{IN}) of 100 V, output voltage (V_{OUT}) of 40 V, inverter phase shift ϕ of 180°, and output power of 100 W.

Design method	F	Q	$M(\phi = \pi)$	$I_{L,rms}$ [A]	$0.5LI_{L,pk}{}^2$ [μJ]	$0.5CV_{C,pk}{}^2$ [μJ]
FHA	1.4	3.5	0.303	3.9	1247	519
LBSM	1.4	2.5	0.408	2.9	835	365

where $\gamma = \frac{\pi}{2F}$. Equation (2.71) can be used to determine the appropriate loaded quality factor Q when the normalized switching frequency F is known. Typically, phase-shift control is activated when the effectiveness of frequency control diminishes [50]. Assuming that in our example phase-shift control becomes active at $F = 1.4$, the appropriate value of $Q = 2.5$. Using (2.67), the voltage gain of the converter when $\phi = \pi$ is $M = 0.408$. As the converter has maximum voltage gain at $\phi = \pi$, it uses this phase-shift when the input voltage is at its minimum. Hence, the transformer turns ratio can be computed using $n_t = \frac{M(\phi=\pi)V_{IN,min}}{V_{OUT}}$ and its value is 1.02. Assuming $F = 1.4$ corresponds to 100 kHz switching frequency, the resonant tank component values can be computed using the defining expressions for F and Q, and their values are given by $L = 89\,\mu H$ and $C = 55\,nF$.

The conventional method for designing a phase-shift controlled SRC relies upon Fundamental Harmonic Analysis (FHA), which yields the following design equation:

$$\frac{M(\phi = \pi)}{M(\phi = \phi_{ZVS})} = \frac{\sqrt{64/\pi^4 + (Q(F - 1/F))^2}}{8/\pi^2} = \frac{V_{IN,max}}{V_{IN,min}}, \tag{2.72}$$

which is analogous to LBSM's (2.71). For $F = 1.4$, the FHA based design gives $Q = 3.5$, $M = 0.303$, $n_t = 0.75$, $L = 70\,\mu H$ and $C = 71\,nF$. The FHA and LBSM based designs are compared in Table 2.1. The inductor RMS current and the peak energy stored in the inductor and the capacitor are determined through simulations for both converters. Since the LBSM based design provides a higher voltage gain M, and a correspondingly higher transformer turns ratio, it imposes lower current and voltage stresses on the resonant tank elements compared to the FHA based design. This substantial benefit due to the higher voltage gain is not negated by the LBSM based designs lower tank Q value and potentially increased losses due to higher order harmonics, as any higher order harmonics in the tank current also contribute to real power transfer (further lowering inductor

RMS current) and generally assist in achieving ZVS. In fact, the lower tank Q enables the use of a smaller inductance value inductor (hence, lower effective series resistance given an inductor quality factor), which combined with the lower RMS inductor current results in substantially lower losses. In the considered example, the 26% lower inductor RMS current of the LBSM based design would result in 45% reduction in primary side conduction losses. Furthermore, the 32% lower peak stored energy in the resonant tank would enable the tank elements of the LBSM based design to be substantially smaller in size.

2.5.2 Phase-Shift Converter

Topologically, the Phase-Shift Converter (PSC) with capacitive filter is identical to the SRC except that it does not have the resonant capacitor (see Fig. 2.12(a)). Mathematically, the PSC can be derived from the SRC by taking the limit $\mathrm{C} \to \infty$, which would effectively short circuit the resonant capacitor. Therefore, the expression for the current waveform of the PSC can be derived simply by making the resonant capacitor infinitely large in the expression for the current waveform of the SRC. Making the resonant capacitor $\mathrm{C} \to \infty$ results in $Q \to 0$ and $F \to \infty$. Therefore, the voltage gain and the current phase lag angle under ZVS operation, and the ZVS boundary (ϕ_{ZVS}) for the PSC can be obtained from (2.67), (2.68) and (2.69) under the limit $Q \to 0$ and $F \to \infty$:

$$\mathrm{M} = \frac{1}{\pi}\left(\sqrt{\phi(2\pi-\phi)+(2Q_{\mathrm{L}})^2}-2Q_{\mathrm{L}}\right), \tag{2.73}$$

$$\theta = \frac{\pi}{2}\left(1-\mathrm{M}\right), \tag{2.74}$$

$$\phi_{\mathrm{ZVS}} = \pi - 2Q_{\mathrm{L}}, \tag{2.75}$$

where $Q_{\mathrm{L}} = \frac{\omega_s \mathrm{L}}{\mathrm{n_t}^2 \mathrm{R}}$ is the loaded quality factor of the inductor. At the ZVS boundary, i.e., $\phi = \phi_{\mathrm{ZVS}}$, the expression for M simplifies to:

$$\mathrm{M} = 1 - \frac{2}{\pi}Q_{\mathrm{L}} = \frac{\phi_{\mathrm{ZVS}}}{\pi}. \tag{2.76}$$

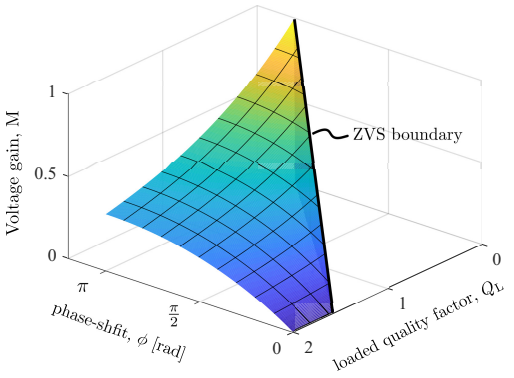


Fig. 2.13: Voltage gain M as a function of phase-shift ϕ and loaded quality factor of the inductor Q_{L} in the ZVS region of the phase-shift converter (PSC).

A plot of voltage gain M as a function of phase-shift ϕ and the loaded quality factor of the inductor Q_{L}, as given by (2.73), for the ZVS region of the PSC is shown in Fig. 2.13.

To compare the PSC with the SRC, the PSC is also designed for the same example specifications, i.e., $\mathrm{V_{IN,min}} = 100\,\mathrm{V}$, $\mathrm{V_{IN,max}} = 330\,\mathrm{V}$, $\mathrm{V_{OUT}} = 40\,\mathrm{V}$, $P = 100\,\mathrm{W}$ and $f_s = 100\,\mathrm{kHz}$. Assuming the PSC is also required to operate under ZVS, and regulation is also done by decreasing the phase-shift from π to ϕ_{ZVS}, the ratio of the PSC voltage gain at π phase-shift to its voltage gain at ϕ_{ZVS} is given by:

$$\frac{\mathrm{M}\left(\phi=\pi\right)}{\mathrm{M}\left(\phi=\phi_{\mathrm{ZVS}}\right)} = \frac{\sqrt{1+\left(\frac{2}{\pi}Q_{\mathrm{L}}\right)^2}-\frac{2}{\pi}Q_{\mathrm{L}}}{1-\frac{2}{\pi}Q_{\mathrm{L}}} = \frac{\mathrm{V_{IN,max}}}{\mathrm{V_{IN,min}}}, \tag{2.77}$$

which is analogous to the SRC's (2.71). For the given specifications, (2.77) gives the required loaded inductor quality factor $Q_{\mathrm{L}} = 1.35$. From (2.73), at $\phi = \pi$, the voltage gain of the converter M is 0.46. Similar to the SRC, the PSC has maximum voltage gain at $\phi = \pi$, which it uses at minimum input voltage. Hence, its transformer turns ratio $\mathrm{n_t} = \frac{\mathrm{M}(\phi=\pi)\mathrm{V_{IN,min}}}{\mathrm{V_{OUT}}} = 1.15$. Given the PSC is also operating at 100 kHz switching frequency, its inductor value can be computed using the defining expression for Q_{L}, and is $\mathrm{L} = 45.5\,\mu\mathrm{H}$. The key parameter and component values for the PSC are compared with those for the SRC, designed for the same example specifications, in Table 2.2. As can be seen from Table 2.2, for this example with an input voltage range of 3.3 to 1, the PSC provides a larger voltage gain relative to the SRC at a given phase-shift and, therefore, gets to use a higher value of $\mathrm{n_t}$. Since both converters have the same fixed output current, the PSC with its higher $\mathrm{n_t}$ has a lower primary-side current irrespective of phase-shift. With near-identical inverter switching losses due to ZVS and

TABLE 2.2: Parameter and component values for the SRC and the PSC in the considered example.

Converter	Tank parameters	$M(\phi = \pi)$	n_t	Tank components
SRC	$F = 1.4$, $Q = 2.5$	0.408	1.02	$L = 89.1\,\mu H$, $C = 55.7\,nF$
PSC	$Q_L = 1.35$	0.46	1.15	$L = 45.5\,\mu H$

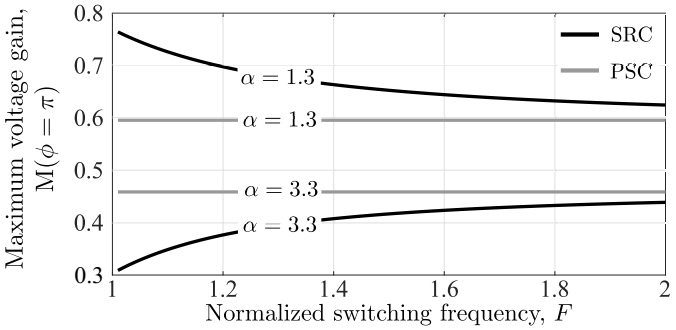


Fig. 2.14: Maximum voltage gain for the SRC and the PSC as a function of normalized switching frequency for maximum-to-minimum input voltage ratio $\alpha = 1.3$ and $\alpha = 3.3$

identical transformer core and secondary-side losses in both converters, the PSC with the lower primary-side currents is expected to be more efficient due to lower primary-side conduction losses and lower inductor core losses. The PSC is also expected to be smaller as it has fewer and smaller tank components.

The comparison between the PSC and the SRC can also be generalized for an arbitrary input voltage range of α to 1, where $\alpha \equiv V_{IN,max}/V_{IN,min}$ is the maximum-to-minimum input voltage ratio. For the PSC, using (2.77), Q_L can be expressed in terms of α as:

$$\frac{2}{\pi}Q_L = \frac{\alpha(\alpha-1) - \sqrt{2\alpha(\alpha-1)}}{\alpha(\alpha-2)}. \tag{2.78}$$

Substituting this expression for Q_L and $\phi = \pi$ into (2.73) gives an expression for the maximum voltage gain of the PSC in terms of α:

$$M_{PSC}(\phi = \pi) = \frac{-\alpha + \sqrt{2\alpha(\alpha-1)}}{\alpha - 2}. \tag{2.79}$$

For the SRC, using (2.67), (2.71) and $\phi = \pi$, an analogous expression for the maximum voltage gain is obtained in terms of α:

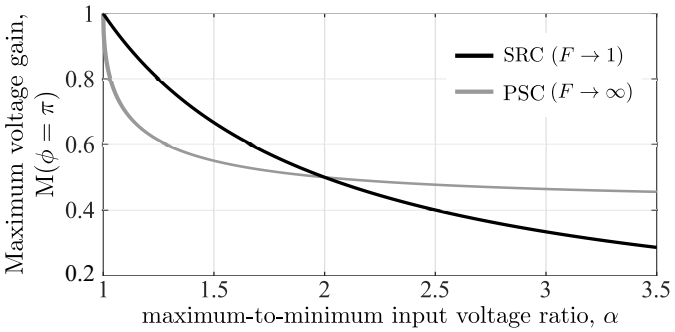


Fig. 2.15: Maximum voltage gain for the SRC ($F \to 1$) and the PSC ($F \to \infty$) as a function of maximum-to-minimum input voltage ratio.

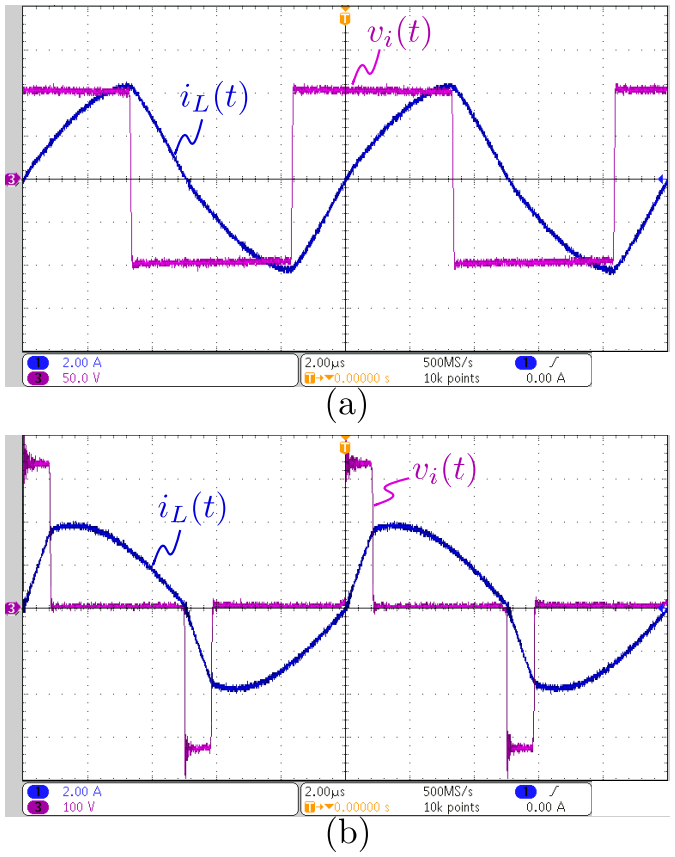


Fig. 2.16: Inverter output voltage $v_i(t)$ and inductor current $i_L(t)$ of the prototyped Series Resonant Converter (SRC) operating with (a) input voltage $V_{IN} = 100\,V$ and (b) input voltage $V_{IN} = 330\,V$.

$$M_{SRC}(\phi = \pi) = \frac{\alpha\left(\tan^2(\gamma) + (2-\alpha)\right) - (2-\alpha)\sqrt{(\alpha-1)\left(2\alpha + \tan^2(\gamma)(1+\alpha)\right)}}{\alpha^2\tan^2(\gamma) + (2-\alpha)^2}. \tag{2.80}$$

Since the SRC and the PSC are operating under ZVS and have identical output currents, any difference in their efficiency will arise from differences in their primary-side

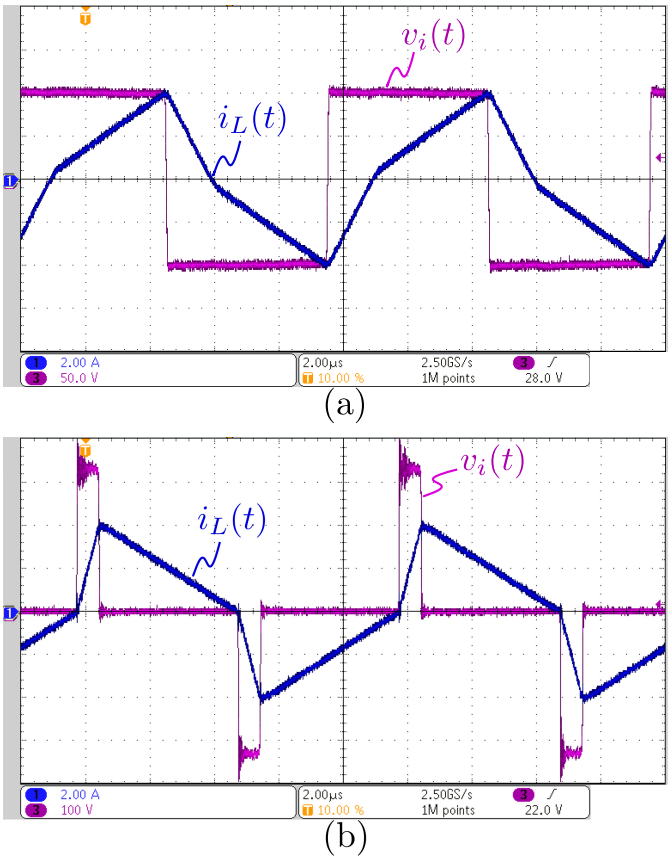


Fig. 2.17: Inverter output voltage $v_i(t)$ and inductor current $i_{\mathrm{L}}(t)$ of the prototyped Phase-Shift Converter (PSC) operating with (a) input voltage $\mathrm{V_{IN}} = 100\,\mathrm{V}$ and (b) input voltage $\mathrm{V_{IN}} = 330\,\mathrm{V}$.

currents. Hence, the most important characteristic of their designs is maximum voltage gain $\mathrm{M}(\phi = \pi)$ which determines the primary-side currents and consequently conduction losses and tank sizes. The maximum voltage gain for the PSC depends solely on α, while for the SRC it depends on both α and the normalized switching frequency F, as can be seen from (2.79) and (2.80), respectively. A plot of maximum voltage gain $\mathrm{M}(\phi = \pi)$ for the SRC and the PSC, as a function of F, for two different values of α (1.3 and 3.3) is shown in Fig. 2.14. As can be seen from Fig. 2.14, either the SRC or the PSC has the higher maximum volage gain independent of F and depending solely on the value of α. If α is small (e.g., $\alpha = 1.3$), the SRC has a larger voltage gain and is the superior design. However, if α is large (e.g., $\alpha = 3.3$), the PSC provides a larger voltage gain and is superior. Another aspect to note from Fig. 2.14 is that the maximum voltage gain of the SRC is a monotonic function of F and as $F \to \infty$ the SRC essentially becomes the PSC. Therefore, a convenient way to determine which converter is superior is to evaluate the maximum voltage gain of the SRC at $F \to 1$ (pure resonance) and at $F \to \infty$ (PSC). If the SRC's maximum voltage gain at $F \to 1$ is larger than its maximum voltage gain

at $F \to \infty$, then the SRC is superior, otherwise the PSC is superior. The maximum voltage gain of the SRC under these two limiting values of F is:

$$\lim_{F\to 1} \mathrm{M_{SRC}}(\phi = \pi) = 1/\alpha \tag{2.81}$$

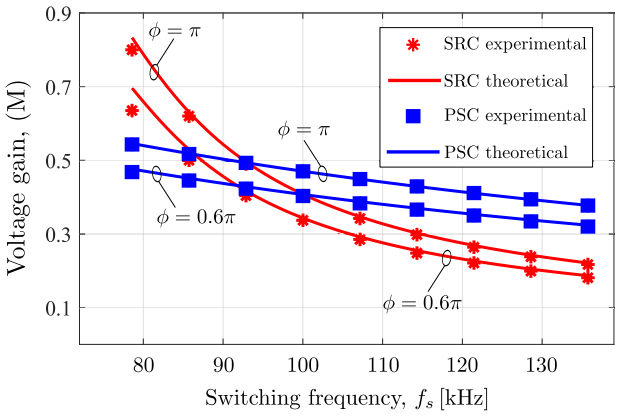
$$\lim_{F\to \infty} \mathrm{M_{SRC}}(\phi = \pi) = \frac{-\alpha + \sqrt{2\alpha(\alpha-1)}}{\alpha - 2} \tag{2.82}$$

The maximum voltage gains of the SRC under the two limiting values of F, as given by (2.81) and (2.82), are plotted in Fig. 2.15 as functions of α. As can be seen from Fig. 2.15, the two gains are equal when $\alpha = 2$. If the maximum-to-minimum input voltage ratio $\alpha < 2$, then the SRC provides the higher maximum voltage gain and is superior, and if $\alpha > 2$ then the PSC provides the higher maximum voltage gain and is superior.

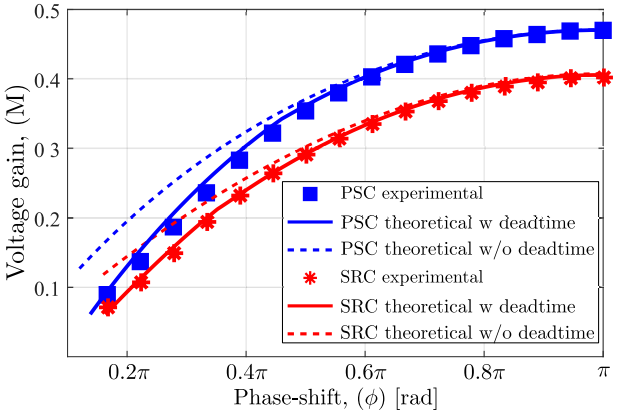
2.6 Experimental Verification of SRC and PSC

To validate the accuracy of the LBSM based designs, and to compare the performance of the SRC and the PSC, the two converter designs given in Table 2.2 are built and tested. The details of the hardware are shown in Table 2.3. The converter is controlled using a Texas Instruments TMS320F28335 DSP microcontroller which generates the gating signals for each half-bridge with a dead time of 0.4 μs and all experimental results are reported for an output power of 100 W. The experimentally measured operating waveforms for the SRC and the PSC are shown in Fig. 2.16 and Fig. 2.17, respectively, for two different values of input voltage (100 V and 330 V). From Fig. 2.16(b) and Fig. 2.17(b) it can be seen that the inductor current in both converters is zero at the instant when the leading leg switches, and both converters operate on the ZVS boundary, when the input voltage is 330 V. This validates the accuracy of the LBSM based design equations as far as predicting ZVS boundary is concerned, since both converters were designed using (2.70) and (2.77) to have a ZVS boundary at an input voltage of 330 V.

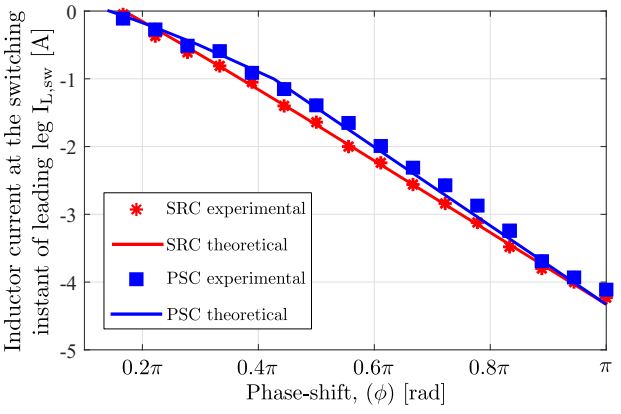
The voltage gain M of the SRC and the PSC (discounting for their transformers' turns ratios) is also experimentally measured and compared with theoretically predicted values of M across a range of switching frequencies and for two different values of phase-shift, as shown in Fig. 2.18(a). Here, the theoretically computed values of M are calculated using (2.67) and (2.73) for the SRC and the PSC, respectively. As can be seen from



(a)



(b)



(c)

Fig. 2.18: Theoretically calculated (using LBSM) and experimentally measured for the SRC and the PSC: (a) voltage gain as a function of switching frequency for two different values of inverter phase-shift, (b) voltage gain as a function of phase-shift when operating at 100 kHz switching frequency and (c) inductor current at the instant when leading leg switches ($I_{L,sw}$) as a function of inverter phase-shift when operating at 100 kHz.

Fig. 2.18(a) there is an excellent match between experiment and theory, validating the accuracy of the LBSM based equations for voltage gain.

TABLE 2.3: Components used in the Prototyped Series Resonant Converter (SRC) and Phase Shift Converter (PSC)

Components	SRC	PSC
Q_1, Q_2, Q_3, and Q_4	FCB070N65S3 650-V/44-A MOSFET	FCB070N65S3 650-V/44-A MOSFET
D_1, D_2, D_3, and D_4	V3P6L 60-V/3-A Schottky diode	V3P6L 60-V/3-A Schottky diode
C	55.7-nF 630-V polypropylene film cap.	N/A
L	89.1 μH 32 turns of 140-strand AWG-38 Litz wire ETD 34/17/11 TDK N87 1.36-mm airgap	45.5 μH 32 turns of 140-strand AWG-38 Litz wire ETD 34/17/11 TDK N87 2.7-mm airgap
Transformer	1.02:1 turns ratio primary: 13 turns of 100-strand AWG-38 secondary: 13 turns of 100-strand AWG-38 E 32/16/9 TDK N87	1.15:1 turns ratio primary: 15 turns of 100-strand AWG-38 secondary: 13 turns of 100-strand AWG-38 E 32/16/9 TDK N87

The prototyped SRC and PSC are also operated under phase-shift control while operating at a fixed switching frequency. Figure 2.18(b) shows the experimentally measured voltage gain M of the two converters as a function of phase-shift while operating at 100 kHz. As expected the PSC provides a larger voltage gain than the SRC across the entire range of phase-shift. The theoretically calculated values of M for the SRC and the PSC, computed using (2.67) and (2.73), respectively, are also shown using the dotted lines in Fig. 2.18(b). As can be seen, there is an excellent match between the experimentally measured and the theoretically predicted values of M for large values of phase-shift. For phase-shifts below about 0.4π for SRC and 0.44π for PSC there is a small deviation between the theoretically calculated and the experimentally measured voltage gains. This deviation at low phase-shifts arises from decreased volt-seconds applied by the inverter during the dead time. The presence of dead time and non-negligible output capacitance of the inverter transistors, that were ignored in the theoretical analysis, results in a reduction of volt-seconds applied by the inverter due to the extra time needed to charge/discharge these capacitances. A ZVS model is developed for the SRC and PSC using the analysis of the effective volt-seconds applied by the inverter in the

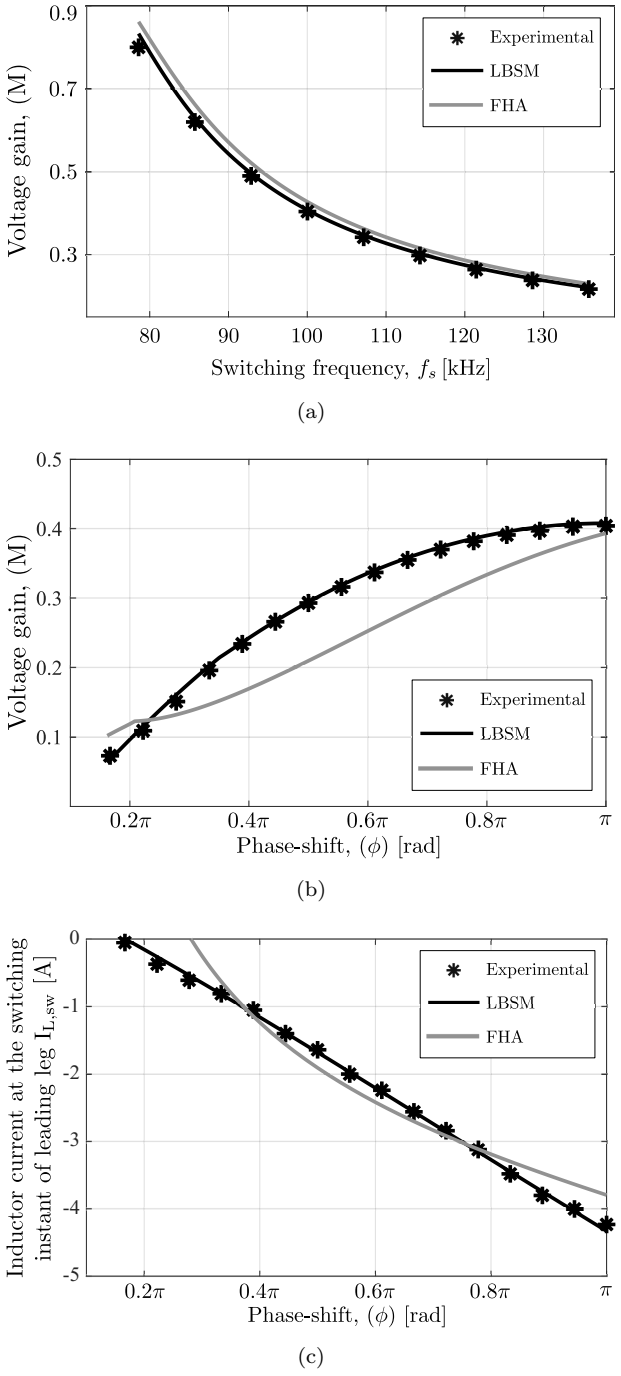


Fig. 2.19: Theoretically calculated using LBSM and FHA and experimentally measured for the SRC: (a) voltage gain as a function of switching frequency with an inverter phase-shift of 180°, (b) voltage gain as a function of inverter phase-shift when operating at 100 kHz switching frequency, and (c) inductor current at the instant when leading leg switches ($I_{L,sw}$) as a function of inverter phase-shift when operating at 100 kHz.

following section. This model can be used to obtain the full and partial ZVS ranges for the mentioned converters.

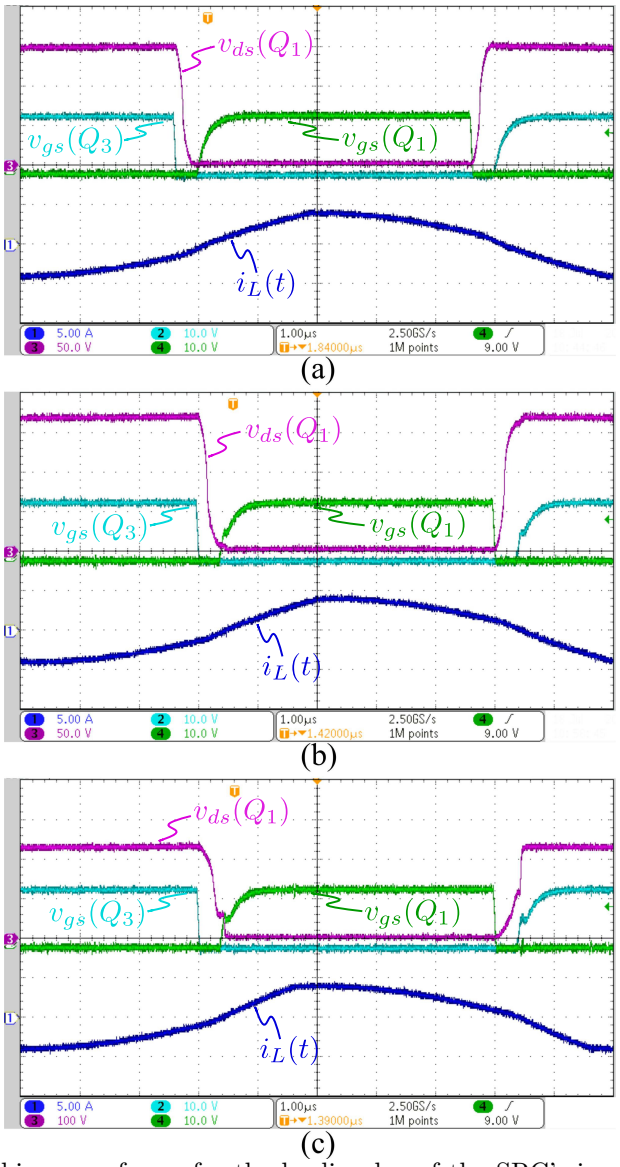


Fig. 2.20: Switching waveforms for the leading leg of the SRC's inverter (Q_1 and Q_3 of Fig. 2.12(a)) including Q_1's gate-source voltage $v_{gs}(Q_1)$, Q_3's gate-source voltage $v_{gs}(Q_3)$, Q_1's drain-source voltage $v_{ds}(Q_1)$ and inductor current $i_L(t)$ under different operating conditions: (a) full ZVS with $V_{IN} = 150\,V$, (b) boundary between full ZVS and partial ZVS with $V_{IN} = 175\,V$, and (c) partial ZVS with $V_{IN} = 225\,V$.

2.7 Effective Phase-Shift for SRC and PSC to Account for Inverter Dead Time

For both the series resonant converter (SRC) and the phase shift converter (PSC) assuming full or partial ZVS, during the dead time of a half-bridge, the dominant resonance is between the converter's inductor L and the output capacitors (C_{oss}) of that half-bridge's two transistors (which act as if in parallel). Any other capacitors of the converter (e.g., the tank capacitor C in the case of the SRC) have little impact on this resonance as they

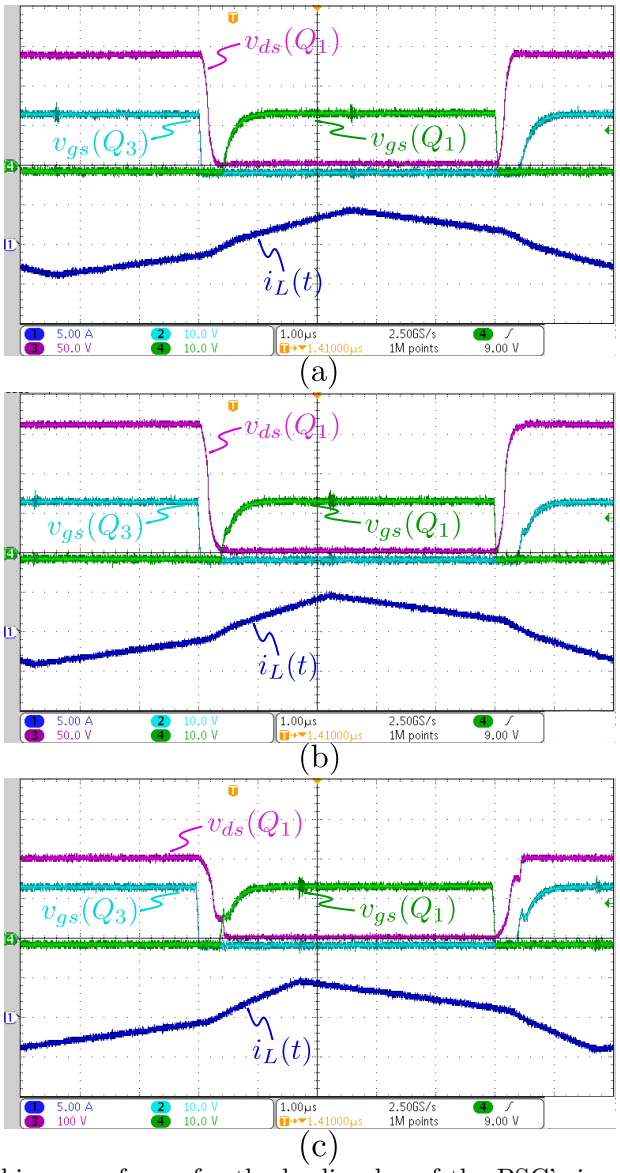


Fig. 2.21: Switching waveforms for the leading leg of the PSC's inverter (Q_1 and Q_3 of Fig. 2.12(a)) including Q_1's gate-source voltage $v_{gs}(Q_1)$, Q_3's gate-source voltage $v_{gs}(Q_3)$, Q_1's drain-source voltage $v_{ds}(Q_1)$ and inductor current $i_L(t)$ under different operating conditions: (a) full ZVS with $V_{IN} = 140\,V$, (b) boundary between full ZVS and partial ZVS with $V_{IN} = 165\,V$, and (c) partial ZVS with $V_{IN} = 205\,V$.

are much larger than, and appear in series with, $2C_{oss}$. This resonance continues until the transistor output capacitors are charged/discharged to $V_{IN}/0\,V$ and the anti-parallel diodes clamp their voltages, or the inductor current changes direction. This resonance occurs during the dead times of both the leading and the lagging half-bridges, and results in a change in the volt-seconds applied by the inverter in a half switching period. However, the impact on inverter volt-seconds due to the dead time of the lagging half-bridge is much smaller than that of the leading half-bridge, as the lagging half-bridge switches at a much higher current resulting in a much smaller inverter output voltage transition

time. Hence, the impact of the dead time of the lagging half-bridge is neglected in this analysis. Considering the radial half time period $0 \leq \omega_s t < \pi$, the instantaneous output voltage of the inverter v_i during the dead time of the leading half-bridge is given by:

$$v_i = \mathrm{Z_{oss}} \mathrm{I_{L,sw}} \sin\left(\omega_{\mathrm{oss}} t - \frac{\omega_{\mathrm{oss}}}{\omega_{\mathrm{s}}} \frac{\pi - \phi}{2}\right), \tag{2.83}$$

where $\omega_{\mathrm{oss}} \left(\equiv \frac{1}{\sqrt{2\mathrm{LC_{oss}}}}\right)$ and $\mathrm{Z_{oss}} \left(\equiv \sqrt{\frac{\mathrm{L}}{2\mathrm{C_{oss}}}}\right)$ are the resonant frequency and the characteristic impedance of the tank formed by L and $2\mathrm{C_{oss}}$, respectively, $\frac{\pi-\phi}{2}$ is the radial time when the leading half-bridge starts to switch, and $\mathrm{I_{L,sw}}$ is the inductor current at the instant $\frac{\pi-\phi}{2}$. The value of $\mathrm{I_{L,sw}}$ used here is determined using LBSM without considering dead times as a reasonably good approximation. The time it takes for the inverter output voltage to reach $\mathrm{V_{IN}}$, Δt, can be determined from (2.83) if $\mathrm{Z_{oss}} \mathrm{I_{L,sw}}$ is greater than or equal to $\mathrm{V_{IN}}$, otherwise, the time taken is the full dead time t_{d} at which point the transistor output capacitors are hard charged; hence, Δt is given by:

$$\Delta t = \begin{cases} \frac{1}{\omega_{\mathrm{oss}}} \sin^{-1}\left(\frac{\mathrm{V_{IN}}}{\mathrm{Z_{oss}} \mathrm{I_{L,sw}}}\right) & \text{if} \quad \mathrm{Z_{oss}} \mathrm{I_{L,sw}} \geq \mathrm{V_{IN}} \\ t_{\mathrm{d}} & \text{if} \quad \mathrm{Z_{oss}} \mathrm{I_{L,sw}} < \mathrm{V_{IN}}, \end{cases} \tag{2.84}$$

The average value of the inverter output voltage during the dead time is given by:

$$\begin{aligned} \mathrm{V_{i,d}} &= \frac{1}{t_{\mathrm{d}}} \left(\int_0^{\Delta t} \mathrm{Z_{oss}} \mathrm{I_{L,sw}} \sin\left(\omega_{\mathrm{oss}} t\right) dt + \int_{\Delta t}^{t_{\mathrm{d}}} \mathrm{V_{IN}} dt \right) \\ &= \frac{1}{t_{\mathrm{d}}} \left(\frac{\mathrm{Z_{oss}} \mathrm{I_{L,sw}}}{\omega_{\mathrm{oss}}} \left(1 - \cos\left(\omega_{\mathrm{oss}} \Delta t\right)\right) + \mathrm{V_{IN}} \left(t_{\mathrm{d}} - \Delta t\right) \right). \end{aligned} \tag{2.85}$$

The dead time eats into the duration ϕ when the inverter output voltage is $\mathrm{V_{IN}}$. Hence, an effective phase shift ϕ_{eff} can be defined for a dead-time-free inverter such that the volt-seconds delivered by it are equal to the actual volt-seconds delivered by the inverter with a dead time:

$$\phi_{\mathrm{eff}} \mathrm{V_{IN}} = \left(\phi - \omega_{\mathrm{s}} t_{\mathrm{d}}\right) \mathrm{V_{IN}} + \omega_{\mathrm{s}} t_{\mathrm{d}} \mathrm{V_{i,d}}. \tag{2.86}$$

Substituting for $\mathrm{V_{i,d}}$ from (2.85) into (2.86) and solving for ϕ_{eff} gives:

$$\phi_{\mathrm{eff}} = \phi - \omega_{\mathrm{s}} \left(\Delta t - \frac{\mathrm{Z_{oss}} \mathrm{I_{L,sw}}}{\omega_{\mathrm{oss}} \mathrm{V_{IN}}} \left(1 - \cos\left(\omega_{\mathrm{oss}} \Delta t\right)\right) \right), \tag{2.87}$$

Since the SRC and the PSC operate symmetrically across a half time period, (2.87) is also the expression for effective phase shift during the second half time period ($\pi \leq \omega_{\mathrm{s}} t < 2\pi$).

This effective phase shift ϕ_{eff} can be used to determine the converter waveforms, including the inductor current and voltage gain using the already developed expressions for

these in terms of phase shift ϕ based on an edge switch network model for the converter in which the dead times were not included. The theoretically calculated voltage gain with the dead time effect included by means of ϕ_{eff} is plotted as solid lines and compared with experimental data and the theoretical calculation without the dead time effect included in Fig. 2.18(b). As can be seen, there is an excellent match between theory and experiment when the dead time is included.

The theoretical calculation of voltage gain utilizing (2.87) and (2.84) relies on $\mathrm{I_{L,sw}}$. An accurate value of $\mathrm{I_{L,sw}}$ can be determined from the LBSM derived waveforms. Figure 2.18(c) shows the theoretically calculated values of $\mathrm{I_{L,sw}}$ for the SRC and the PSC as a function of phase-shift when operating at 100 kHz switching frequency. The experimentally measured values of $\mathrm{I_{L,sw}}$ are also shown in Fig. 2.18(c), and match the LBSM predicted values very well. Since the SRC can also be modeled using FHA, it is instructive to compare the predictions of the LBSM and the FHA based models for the SRC with experimental results. This comparison is shown in Fig. 2.19. Clearly, the LBSM based model provides a closer match to experiments. A comparison of LBSM with other analytical modeling techniques applicable to resonant converters is provided in the following subsection.

2.8 Comparison of LBSM with Existing Analytical Modeling Techniques

This appendix compares LBSM with existing analytical techniques for modeling the steady-state waveforms of resonant converters, as summarized in Table 2.4. The fundamental harmonic analysis (FHA) technique is the least complex, but also the least accurate; it is especially inaccurate for converters with low loaded quality factor resonant tanks and does not model DCM operation. Extensions of FHA, such as in [51, 52], have also been developed in which the rectifier is modeled using a complex impedance instead of a resistance as in FHA. These approaches increase the modeling accuracy to some extent but at the cost of increased modeling complexity and are still unable to model DCM operation. Techniques that incorporate higher order harmonics, such as the generalized averaging method (GAM) [33] and other similar techniques [53], also improve the modeling accuracy to a level limited by the number of harmonics that can

TABLE 2.4: Comparison of LBSM with existing analytical methods for modeling steady-state waveforms of resonant converters.

Method	Closed-form	Accuracy	DCM	$\phi \neq \pi$	High-order topologies	Complexity
FHA	Yes	Medium	No	Yes	Yes	Low
FHA Extensions	Yes	Low	No	Yes	Yes	Medium
GAM	No	Medium	Yes	Yes	Yes	High
SPA	Yes	High	No	No	No	High
Cyclic Averaging	Yes	Medium	No	No	Yes	High
LBSM	Yes	High	Yes	Yes	Yes	High

be practically included. However, these techniques have high complexity and do not yield closed-form expressions for converter waveforms. The state plane analysis (SPA) technique, while accurate, is not practical for converters with more than two state variables, and in the case of the series resonant converter (SRC), SPA yields closed-form expressions only if the inverter output voltage waveform is a symmetrical square wave ($\phi = \pi$). Another analytical approach, cyclic averaging [54], uses augmented averaging matrices to determine steady-state waveforms, but requires knowledge of subinterval duration, which is determined by first applying FHA, limiting its accuracy. As can be seen from Table 2.4, LBSM brings a unique ability to accurately model a broad class of resonant converters without being any more complex than the existing techniques. The LBSM derived waveforms can also be used to determine the boundary between full and partial ZVS for both the SRC and the PSC. Full ZVS is lost and partial ZVS starts when the absolute value of the inductor current at the instant when the leading leg switches ($I_{L,sw}$) is not large enough to fully charge/discharge the transistor output capacitances (C_{oss}) to V_{IN}/0 V during the dead time. As can be seen from Fig. 2.18(c), the absolute value of $I_{L,sw}$ decreases with decreasing phase shift. Using the LBSM calculated values for $I_{L,sw}$ and the output capacitance data for the leading leg transistors, the phase-shifts below which full ZVS is lost and partial ZVS begins is 0.4π and 0.44π for the SRC and the PSC, respectively. These phase-shifts correspond to full ZVS being lost when input voltage exceeds 175 V and 165 V for the SRC and the PSC, respectively. These threshold voltages defining the boundary between full and partial ZVS are also validated through experiment as shown in Fig. 2.20 and Fig. 2.21. Figures 2.20 and 2.21 show the switching

waveforms for the leading legs of the SRC and the PSC, respectively, when operating at input voltages below, equal to and above these threshold voltages. As can be seen from Fig. 2.20(b) and Fig. 2.21(b), the drain-source voltage of the top transistor of the inverter's leading leg barely makes it smoothly all the way to zero and all the way back up to the input voltage when the input voltage is equal to the threshold voltage for the SRC and the PSC, respectively, indicating the boundary between full and partial ZVS.

2.9 Loss Models for the SRC and the PSC

This appendix provides the loss models used to predict the efficiency of the series resonant converter (SRC) and the phase shift converter (PSC). Efficiency is calculated using $\eta = \frac{P_{OUT}}{P_{OUT}+P_{LOSS}}$, where P_{OUT} is the output power of the converter, and P_{LOSS} is the total loss in the converter, comprising conduction losses, transistor switching losses and magnetic core losses. Conduction losses are calculated using:

$$P_{COND} = I_{RMS}^2 (2R_{ON} + R_L + R_T) + 2V_F \frac{P_{OUT}}{V_{OUT}}, \tag{2.88}$$

where I_{RMS} is the RMS value of the inductor current determined from the LBSM derived inductor current waveform, R_{ON} is the on-resistance of the transistors, R_L is the ac winding resistance of the inductor, R_T is the total ac winding resistance of the transformer reflected to its primary side, V_F is the forward voltage of the diodes, and V_{OUT} is the output voltage of the converter. Transistor switching losses are assumed to be zero when the converter achieves full ZVS. Under partial ZVS of the inverters leading leg, switching losses are calculated by accounting for capacitive discharge loss and overlap loss for that leg:

$$P_{SW} = C_{oss,eq} {V_{RM}}^2 f_s + t_{ON} V_{RM} I_{L,d} f_s, \tag{2.89}$$

where $C_{oss,eq}$ is the energy equivalent output capacitance of the transistor, V_{RM} is the switch-node voltage that remains to be discharged/charged determined using the approach described in 2.7 f_s is the switching frequency, t_{ON} is the transistor turn-on time,

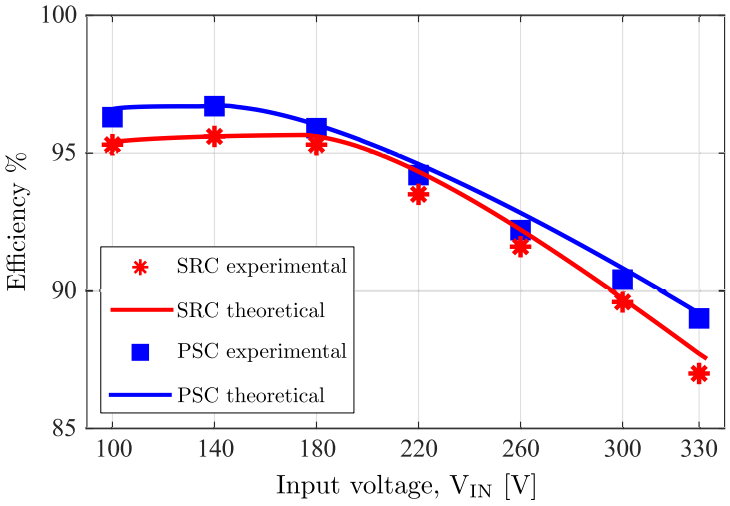


Fig. 2.22: Experimentally measured and theoretically calculated efficiencies for the SRC and the PSC as a function of input voltage.

and $I_{L,d}$ is the inductor current at the end of dead time determined from the LBSM derived inductor current waveform. Magnetic core losses are calculated using Steinmetz's equation:

$$P_{CORE} = C_m f_s^{\alpha} \left(\left(\frac{\lambda_L}{2A_{e,L}N_L} \right)^{\beta} V_{e,L} + \left(\frac{\lambda_T}{2A_{e,T}N_T} \right)^{\beta} V_{e,T} \right), \tag{2.90}$$

where C_m, α and β are core material related constants, $\lambda_T \left(= \frac{V_{OUT}}{2f_s} \right)$ is the flux-linkage applied across the transformer's secondary winding, $\lambda_L \, (= L\Delta I_{L,pp})$ is the flux-linkage applied across inductor L with peak-to-peak current $\Delta I_{L,pp}$, $A_{e,L}$ (and $A_{e,T}$) and $V_{e,L}$ (and $V_{e,T}$) are the equivalent cross section area and core volume, respectively, for the inductor (and the transformer), N_L is the number of turns in the inductor winding, and N_T is the number turns in the secondary winding of the transformer. The transistor, diode and magnetic core parameters used in (2.88)-(2.90) are obtained from manufacturer datasheets, and the remaining parameters are from the information in Table 2.3.

Figure 2.22 shows the measured efficiency of the prototyped SRC and the prototyped PSC for input voltages ranging from 100 V to 330 V while delivering 100 W of output power at an output voltage of 40 V. The theoretically predicted efficiencies for the two converters, determined using the presented loss model, are also shown in Fig. 2.22. As can be seen there is a good match between theory and experiment, and the PSC has a higher efficiency than the SRC across the full input voltage range. Given that the two converters are designed for a maximum-to-minimum input voltage ratio greater than 2,

this result is expected based on the analysis presented using LBSM in Section IV. The higher efficiency of the PSC compared to the SRC is also expected since the prototyped PSC provides a larger voltage gain than the SRC across the entire phase-shift range (see Fig. 2.18(b)), resulting in lower primary-side conduction losses and inductor core losses in the PSC. Beyond the threshold input voltages where full ZVS is lost (175 V for SRC and 165 V for PSC), the efficiency of both converters decreases with increasing input voltage due to increased switching losses. However, the PSC maintains its efficiency advantage over the SRC even at the highest input voltage.

Chapter 3

High Efficiency and Full MPPT Range Partial Power PV Module Integrated Converter

In this chapter, an efficient PV MIC topology is proposed based on the partial power operation. First, application requirements for the PV MICs are elaborated considering different PV system configurations. Based on these requirements, a new high frequency and soft-switching topology is proposed to achieve high efficiency. The proposed topology also adopts partial power processing to further improve the efficiency. Furthermore, the operation of the proposed MIC extends the MPPT range to the full PV MPP range without any efficiency penalty at the partial power range.

3.1 DC-DC Module Integrated Converters

In this section, categorization of the dc-dc MICs and their operation in PV systems are discussed. In essence, dc-dc MICs are adopted for the series stack of PV modules to address the energy capture loss that occurs due to the module level power mismatch. In the PV system configuration shown in Fig. 1.1(b), PV modules are not equipped with dc-dc MICs individually. Hence, to perform the MPPT for the string in the face of temperature and irradiance variations, the dc voltage of the inverter (V_{bus}) should be swept in a predetermined range. In this configuration, if one module generates lower

power compared to the rest of the modules, it would impose the current through the rest of the modules to be reduced which significantly reduces the total power generation. Alternatively, modules can be equipped with bypass diodes so that the weak modules are bypassed under mismatch condition. However, as no power is absorbed form the bypassed modules, a significant portion of the power will be lost. Furthermore, there are some local MPP points in the presence of bypass diodes that may cause the inverter MPPT to fall in these local MPPs and fail to track the global MPP.

3.1.1 Categories of MICs

To improve the energy capture in the presence of module level power mismatches, dc-dc MICs are employed. Based on the voltage conversion ratio of the dc-dc MICs, they can be categorized into three groups of step-down, step-up, and step-up/down MICs. When step-down MICs are used, the output voltage of each MIC is always lower than its PV module voltage and consequently the output current is higher. In this case, all MICs have the same output current as the string current. Therefore, in a PV system equipped with step-down MICs, the string current must be greater than or equal to the maximum MPP current of all the modules, $I_{MPP,max}$, to allow all MICs perform MPPT:

$$I_{str,sd} \geq Max\{I_{MPP,i}\} \qquad 1 \leq i \leq N, \tag{3.1}$$

where $I_{str,sd}$ is the string current in a PV system equipped with step-down MICs, $I_{MPP,i}$ is the maximum MPP current of i-th module and N is the total number of modules in the string. Similarly, when step-up MICs are used in the PV system, the output voltage of each MIC is always higher than or equal to its PV module voltage. Hence, the string current must be lower than or equal to minimum I_{MPP} of all the modules to allow all MICs perform MPPT:

$$I_{str,su} \leq Min\{I_{MPP,i}\} \qquad 1 \leq i \leq N. \tag{3.2}$$

where $I_{str,su}$ is the string current in a PV system equipped with step-up MICs. It is important to note that although the converters can perform MPPT for the whole current range shown in (3.1) and (3.2), selecting the boundary values of the currents result in the lowest current and voltage stress on the converter. If the PV system is equipped with

step-up/down MICs, it can ideally perform MPPT with any amount of string current. However, the best stress at converter output is obtained for:

$$Min\{I_{MPP,i}\} \leq I_{str,sud} \leq Max\{I_{MPP,i}\} \qquad 1 \leq i \leq N. \tag{3.3}$$

Where $I_{str,sud}$ is the string current in a PV system equipped with step-up/down MICs.

3.1.2 MICs in Different PV System Configurations

Generally, there are two categories of PV inverters that can be employed within PV systems equipped with dc-dc MICs: the constant voltage and variable voltage inverters. In the constant voltage inverters, the bus voltage of the inverter is constant while in the other category the dc bus voltage is variable to be able to perform MPPT by sweeping the dc bus voltage in a predefined range. DC-DC MICs normally offer their maximum efficiency when operating with the unity voltage conversion ratio and the efficiency drop occurs when the voltage conversion ratio deviates from unity [23]. The efficiency drops sharply when the MIC leaves the pass-through mode and starts to switch semiconductors. The pass-through mode is a mode of operation in which the MIC connects the PV module to the output directly and the MIC semiconductors are not switched. For example, in the conventional buck converter when duty cycle D is equal to 1, the converter is in the pass-through mode. Similarly, the pass-through mode occurs in the convention boost converter when D is equal to 0.

3.1.2.1 PV Systems with Constant DC Bus Voltage

In the PV systems equipped with constant voltage inverters, the number of modules per string, determines how close the MIC operating points are to the unity conversion ratio. The benchmark number can be defined as the number of models that makes all the MICs to operate with the unity voltage conversion ratio in a PV system with no power mismatch between the modules. The benchmark number, N_b, can be obtained from the following equation.

$$N_b = \frac{V_{bus,c}}{V_{MPP}}. \tag{3.4}$$

Where, $V_{bus,c}$ is the bus voltage of a constant voltage inverter. N_b can be compared to the maximum and minimum number of modules that are required for each category

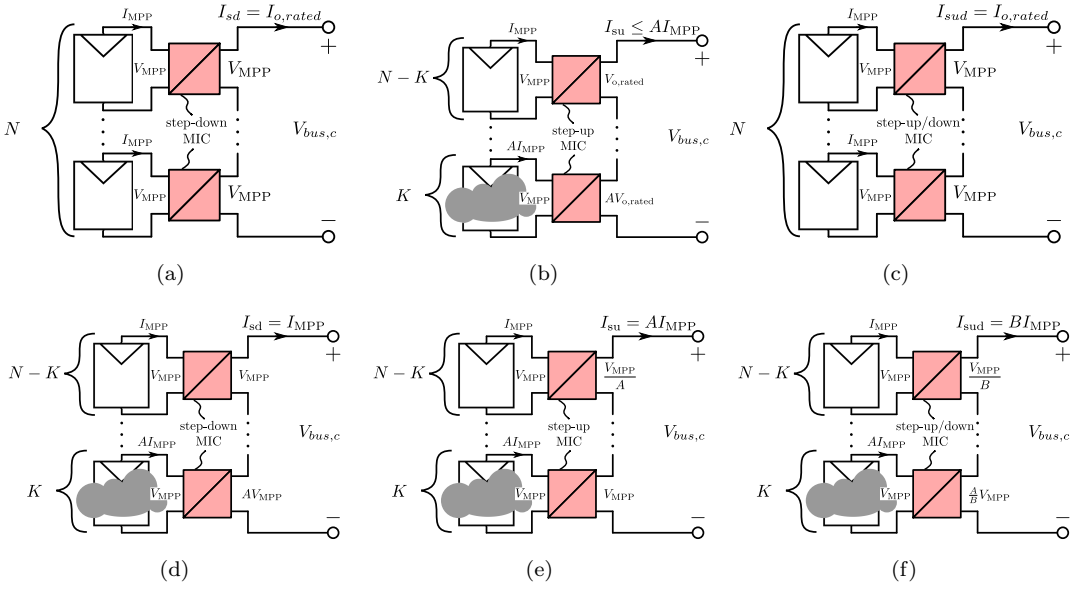


Fig. 3.1: Operation of PV system equipped with (a) and (d) step-down, (b) and (e) step-up, (c) and (f) step-up/down dc-dc MIC under design worst-case scenarios of constant dc bus inverter (V_{MPP} and I_{MPP} are the MPP voltage and current of the modules under standard condition and $V_{bus,c}$ is the constant dc bus voltage).

of dc-dc MICs in presence of power mismatch. Maximum and minimum number of modules can be obtained using the maximum tolerable stress of the converters and using the mismatch scenarios that can occur in PV systems. However, the required number of modules per string, N, may be different from N_b when different categories of MICs are employed especially in the presence of power mismatch. N is affected by the maximum tolerable stress of converters and the mismatch scenarios that can occur in PV systems. To consider the effects of MIC type on their performance under power mismatch condition, a general and simplified mismatch scenario is considered. It is assumed that N modules are used in a string, K modules generate lower power and $1 \leq K \leq N$. The power generation ratio of the lower power generating modules, A, can be obtained from the following equation.

$$A = \frac{P_{MPP,low}}{P_{MPP,rated}}, \tag{3.5}$$

where $P_{MPP,low}$ is the MPP power of modules with lower power generation and $P_{MPP,rated}$ is the rated MPP power of modules. It should be mentioned that $0 < A < 1$.

When the dc bus voltage is constant, by increasing N, the string current which is equal to the MICs output current increases. In PV systems equipped with step-down MICs,

Fig. 3.1(a), the current of the string might exceed the rated output current of the converter $I_{O,rated}$ for large number of modules operating at their rated power. Hence, in these PV systems, the maximum number of modules is limited by the rated output current of the converter and can be calculated form the following equation.

$$N_{sd,max} = \frac{V_{bus,c}}{V_{MPP} I_{MPP}} I_{O,rated} \tag{3.6}$$

where $N_{sd,max}$, is the maximum number of modules in a system with step-down MICs.

Figure 3.1(d) shows a step-down MIC-based PV system under the power mismatch scenario condition. The string current is set to be equal to I_{MPP} which allows MPPT according to (3.1). The voltage on the dc bus can be obtained for this case as,

$$V_{bus,c} = ((N - K) + KA)\, V_{MPP}, \tag{3.7}$$

In this case, if low number of modules are used, the dc bus voltage will fall below $V_{bus,c}$ in the presence of power mismatch as step-down MICs reduce their output voltage to respond the power mismatch. The number of modules per string in a step-down MIC-based system, N_{sd} , can be obtained using (3.7) as,

$$N_{sd,min} \geq \frac{V_{bus,c}}{V_{MPP}} + (1 - A)K, \tag{3.8}$$

According to (3.8), the worst case occurs when $(1 - A)K$ is maximized. By considering A_L as the lowest power generation ratio, and K_L as the greatest number of low-power generating modules, $N_{sd,min}$ can be obtained as:

$$N_{sd,min} = \frac{V_{bus,c}}{V_{MPP}} + (1 - A_L)K_L, \tag{3.9}$$

In order for a PV system to be able to operate with step-down MICs:

$$N_{sd,max} \geq N_{sd,min} \tag{3.10}$$

As it can be seen from (3.6) and (3.9), $N_{sd,min}$ is determined by the PV system parameters only, while the maximum string size depends on the MICs rated output current. Accordingly, the minimum string size is imposed by PV system parameters, then the output current of the converter is selected to have the maximum string size satisfy (3.10).

The more modules in each string, the more deviation from unity conversion ratio and the higher current rated MICs. The best PV system performance and MIC current rating is obtained when $N_{sd,max} = N_{sd,min}$, which results in:

$$I_{o,rated} = I_{MPP}\left(1 + \frac{(1 - A_L)K_L V_{MPP}}{V_{bus,c}}\right) \tag{3.11}$$

Then the lowest stress for the output of the step-down MICs in the constant dc bus voltage inverter systems is:

$$VA_{rated,step-down} = \left(1 + \frac{(1 - A_L)K_L V_{MPP}}{V_{bus,c}}\right) V_{MPP} I_{MPP} \tag{3.12}$$

The same logic can be followed to obtain the string size limitations when using step-up MICs in PV systems equipped with the constant voltage inverter. As the dc bus voltage is constant, by reducing the number of modules per string, the output voltage of the MICs should increase. Thus, for step-up MIC based PV systems, the rated output voltage of the converter $V_{O,rated}$ might be exceeded if low number of modules are used, specially in the presence of power mismatch. Figure 3.1(b) shows the simplified mismatch scenario if the voltage on the converter output has reached the rated output voltage $V_{O,rated}$. Then the dc bus voltage can be obtained as:

$$V_{bus,c} = \left(N + (1 - A)K\right) V_{o,rated}, \tag{3.13}$$

Using (3.13), the minimum number of modules per string that assures converter output voltage is lower than $V_{O,rated}$ under mismatch case is obtained as:

$$N_{su,min} \geq \frac{V_{bus,c}}{V_{O,rated}} + (1 - A)K \tag{3.14}$$

As (3.14) determines the minimum limit, the worst case occurs when right hand side of the equation has greatest value, thus worst case occurs for lowest A value (A_L) and greatest K value ($K = K_L$). Substituting $A = A_L$ and $K = K_L$ in (3.14), minimum number of modules per string is:

$$N_{su,min} = \frac{V_{bus,c}}{V_{O,rated}} + (1 - A_L)K_L, \tag{3.15}$$

Figure 3.1(f) shows the power mismatch scenario with step-up MICs operating with the

largest string current which allows MPPT according to (3.2). The voltage on dc bus is obtained for this case as:

$$V_{bus,c} = \left(\left(\frac{N-K}{A} \right) + K \right) V_{MPP}, \tag{3.16}$$

If large number of modules are used with step-up MICs, the dc bus voltage can exceed $V_{bus,c}$ in presence of power mismatch as step-up MICs increase the output voltage to respond to power mismatch. The number of modules per string can be obtained using (3.16) as:

$$N_{su} = \frac{V_{bus,c}}{V_{MPP}} A + (1-A)K, \tag{3.17}$$

As (3.17) determines the maximum limit, the worst case occurs when right hand side of the equation has lowest value, thus worst case occurs for lowest A value (A_L) and lowest K value ($K = 1$). Substituting $A = A_L$ and $K = 1$ in (3.17), maximum number of modules per string is:

$$N_{su,max} = \frac{V_{bus,c}}{V_{MPP}} A_L + (1-A_L), \tag{3.18}$$

According to (3.15) and (3.18), maximum string size is determined based on PV system parameters only, while the minimum string size depends on converter rated voltage as well. The maximum string size must be first determined using (3.18), then the rated voltage of the converter can be set in a way that following inequality is satisfied:

$$N_{su,max} \geq N_{su,min} \tag{3.19}$$

Selecting smaller minimum string sizes in (3.19) results in higher voltage stress on the converter output. The lowest voltage stress for the converter is obtained when $N_{su,max} = N_{su,min}$:

$$V_{O,rated} = \frac{V_{bus,c}}{V_{bus,c} A_L - V_{MPP}(1-A_L)(K_L - 1)} V_{MPP} \tag{3.20}$$

The current rating of the step-up MICs is lower than I_{MPP} as the maximum number of the modules is less than benchmark string size N_b. The largest current stress of the step-up MICs occurs when there is no mismatch and maximum number of modules are used:

$$N_{su,max} V_{MPP} I_{MPP} = V_{bus,c} I_{su} \tag{3.21}$$

Replacing (3.18) in (3.21) gives the string current which is equal to output current as follows:

$$I_{su} = \left(\frac{A_L + (1 - A_L)V_{MPP}}{V_{bus,c}} \right) I_{MPP} \tag{3.22}$$

Then the lowest stress for the output of the step-up MICs in the constant dc bus voltage inverter systems is:

$$VA_{rated,step-up} = \left(1 + \frac{K_L(1 - A_L)}{A_L \frac{V_{bus,c}}{V_{MPP}} - (1 - A_L)(K_L - 1)} \right) V_{MPP} I_{MPP} \tag{3.23}$$

The other category of dc-dc MICs that can be employed for constant voltage inverter PV systems is the step-up/down MICs. As step-up/down MICs combine both the step-up and step-down operation they can be used with maximum number of modules as shown in (3.6) and minimum number of modules as shown in (3.15), provided that its output current and voltage ratings are $I_{O,rated}$ and $V_{O,rated}$, respectively. This operation imposes significant stress on the output of MICs and makes MICs operate with non-unity conversion ratio even under no mismatch condition. Alternatively, the number of modules per string can be selected equal to benchmark string size N_b so that MICs operate with close to unity conversion ratio. For $N_{sud} = N_b$, the maximum current stress occurs when there is no mismatch and $I_{str,sud} = I_{MPP}$, which is shown in Fig. 3.1(c). Also, the other operating point that is important for the converter stress is mismatch condition shown in Fig. 3.1(f), where $I_{str,sud} = BI_{MPP}$. The dc bus voltage for this case is:

$$V_{bus,c} = \left(\left(\frac{N - K}{B} \right) + K \frac{A}{B} \right) V_{MPP}, \tag{3.24}$$

Ideally, B can have any arbitrary value however to keep the current stress less than I_{MPP} and to make MICs operate with voltage conversion ratios closer to unity it is chosen as $B < 1$. Furthermore, choosing smaller B values can increase the output voltage stress which is V_{MPP}/B according to Fig. 3.1(f). Using (3.24), the value of B for mismatch condition is derived as:

$$B = \frac{V_{MPP}}{V_{bus,c}} \left(N_b - K(1 - A) \right) = 1 - \frac{V_{MPP}}{V_{bus,c}} K(1 - A) \tag{3.25}$$

The minimum value of B that causes the largest voltage stress at MIC output is obtained for $K = K_L$ and $A = A_L$:

$$B_{Min} = 1 - \frac{V_{MPP}}{V_{bus,c}} K_L(1 - A_L) \tag{3.26}$$

Then the step-up/down MICs output stress becomes:

$$VA_{rated,sud} = \left(1 + \frac{\frac{V_{MPP}}{V_{bus,c}} K_L(1 - A_L)}{1 - \frac{V_{MPP}}{V_{bus,c}} K_L(1 - A_L)}\right) V_{MPP} I_{MPP} \tag{3.27}$$

3.1.2.2 PV Systems with Variable DC Bus Voltage

There is also another category of inverters for PV systems which sweeps the dc voltage in a range to perform MPPT. The dc bus voltage can be changed for a variable voltage inverter to meet two constraints. First, MICs of PV modules operate with unity conversion ratio when there is no mismatch. Second, MICs can perform MPPT under mismatch condition. Minimizing the inverter dc voltage range that is required to satisfy the above constraints is another important factor for this type of inverters. The dc bus voltage variations obtained using modules equipped with bypass diodes can be used as the benchmark dc bus voltage range. For PV systems equipped with bypass diodes, the dc bus voltage can exceed $V_{bus,max}$ when there is no mismatch resulting in:

$$V_{bus,max} = NV_{MPP} \tag{3.28}$$

The low power generating modules are bypassed when there is mismatch in a PV system equipped with bypass diodes and dc bus voltage may fall below $V_{bus,min}$. Considering the simplified mismatch case discussed earlier, the minimum dc bus voltage would become:

$$V_{bus,min} = (N - K_L)V_{MPP} \tag{3.29}$$

The benchmark dc bus voltage ratio (VR_b) which shows the ratio of maximum to minimum dc voltage required for a PV system equipped with bypass diodes is:

$$VR_b = \frac{V_{bus,max}}{V_{bus,min}} = \frac{N}{N - K_L}. \tag{3.30}$$

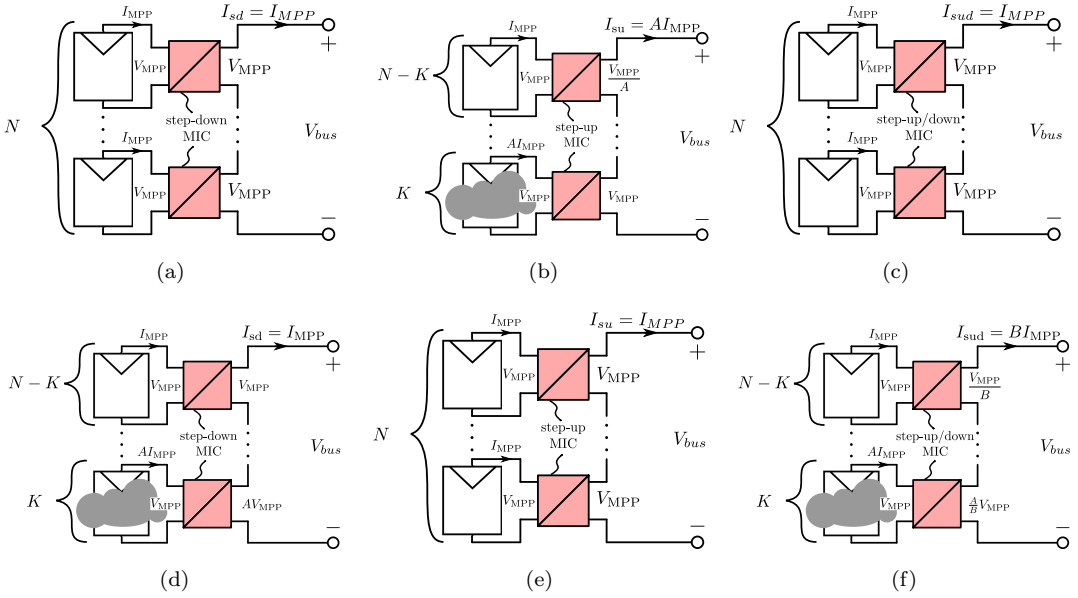


Fig. 3.2: Operation of PV system equipped with (a) and (d) step-down, (b) and (e) step-up, (c) and (f) step-up/down dc-dc MIC under design worst-case scenarios of variable dc bus inverter (V_{MPP} and I_{MPP} are the MPP voltage and current of the modules under standard condition and V_{bus} is the variable dc bus voltage).

Maximum dc bus voltage for step-down MICs occurs under no mismatch condition with $I_{str,sd} = I_{MPP}$ as it is shown in Fig. 3.2(a):

$$V_{bus,sd,max} = NV_{MPP} \tag{3.31}$$

When PV system operates under mismatch condition as shown in Fig. 3.2(d), the dc bus voltage reaches its minimum value $V_{dc,min}$. For step-down MICs, $I_{str} = I_{MPP}$ allows all MICs perform MPPT while it minimizes the current stress at output of converter and provides the largest possible $V_{bus,min}$. As Fig.3.1(d) and Fig. 3.2(d) show the same operation of step-down MICs, equation (3.7) can be used to determine the minimum dc bus voltage for step-down MICs. Using (3.7), the minimum dc bus voltage for step-down MICs is obtained as:

$$V_{bus,sd,min} = (N - K_L + K_L A_L)V_{MPP} \tag{3.32}$$

The output stress for step-down MICs is $V_{MPP}I_{MPP}$ [VA], and dc bus voltage ratio for step-down MIC (VR_{sd}) is:

$$VR_{sd} = \frac{V_{bus,max}}{V_{bus,min}} = \frac{N}{N - K_L + K_L A_L}. \tag{3.33}$$

For step-up MICs, $I_{str,sd} = AI_{MPP}$ allows all the MICs perform MPPT while it keeps the output voltage stress at the minimum possible i.e., V_{MPP}/A. When there is a mismatch as shown in Fig. 3.2(b), the dc bus voltage increases for step-up MICs. As Fig.3.1(b) and Fig. 3.2(b) show the same operation of step-up MICs, equation (3.16) can be used to determine the maximum dc bus voltage for step-up MICs. The maximum dc bus voltage can be obtained using (3.16) as:

$$V_{bus,su,max} = \left(\frac{N-K}{A} + K\right) V_{MPP} = \left(\frac{N}{A} - K\left(\frac{1-A}{A}\right)\right) V_{MPP} \tag{3.34}$$

It is important to note that (3.34) determines the actual voltage of dc bus and does not impose any limit, thus maximum voltage occurs when right hand side of the equation has greatest value which is obtained for lowest A value (A_L) and lowest K value ($K = 1$):

$$V_{bus,su,max} = \left(\frac{N-1+A_L}{A_L}\right) V_{MPP} \tag{3.35}$$

It is important to note that to perform MPPT when $K = 1$, all step-up MICs operate in voltage elevation mode except one of them which results in maximum dc bus voltage. When there is no mismatch in the system, all MICs operate with unity conversion ratio as shown in Fig. 3.2(e) and dc bus voltage is reduced to its minimum as obtained below:

$$V_{bus,su,min} = NV_{MPP} \tag{3.36}$$

The output stress for step-up MICs is $(V_{MPP}I_{MPP})/A_L$ [VA], and dc bus voltage ratio for step-up MICs (VR_{su}) is:

$$VR_{su} = \frac{V_{bus,max}}{V_{bus,min}} = \frac{N-1+A_L}{A_L N}. \tag{3.37}$$

If step-up/down MICs are used with variable dc bus voltage inverters, the maximum dc voltage occurs under no mismatch condition with $I_{str,sud} = I_{MPP}$ as it is shown in Fig. 3.2(c). As Fig. 3.2(a) and Fig. 3.2(c) show the same operation of MIC, the maximum dc bus voltage is still imposed by (3.31) for step-up/down MICs. The minimum dc voltage is also determined using the mismatch scenario shown in Fig. 3.2(f). To improve the dc voltage range, the minimum dc voltage can be increased compared to (3.32) using B values smaller than unity. However, using B values smaller than unity makes all the MICs operate with non-unity conversion ratios in case of power mismatch. Also, the

voltage stress at the output of converter would be increased to V_{MPP}/B. The output stress for step-up/down MICs is $V_{MPP}I_{MPP}/B$ [VA], and dc bus voltage ratio for step-up/down MICs (VR_{sud}) is:

$$VR_{sud} = \frac{V_{bus,max}}{V_{bus,min}} = B\frac{N}{N - K_L + K_L A_L}. \tag{3.38}$$

3.1.3 Comparison of Different MIC Categories

The obtained constraints for MICs in constant voltage and variable voltage dc bus configurations can be used to compare their operation. It is important to note that some of the above constraints for MICs are imposed by the power mismatch case with K=1 which is common in PV systems. However, the rest of the constraints are imposed by worst-case module level power mismatch with the greatest number of low power generating modules K_L. The worst-case module level power mismatch can be caused by different factors depending on the PV system type. For example, in residential PV systems nonuniform shading causes the worst-case power mismatch, while in PV farms normally nonuniform shading is not present and dust accumulation, aging, manufacturing tolerances, etc. can cause the power mismatch. Therefore, the obtained equations are used to compare the operation of MICs with various K_L and A_L values. For constant dc bus voltage configuration, the following parameters are calculated for various K_L and A_L values to compare the three categories of dc-dc MICs: string size, normal voltage conversion ratio which is obtained under no mismatch operation, and converter voltage/current stresses. For a given dc bus voltage $V_{bus,c}$ and rated MPP voltage of modules V_{MPP}, each category of dc-dc MICs is expected to have a different string size. To have equal level of mismatch for various categories of MICs it is assumed that:

$$K_L = \alpha N, \tag{3.39}$$

,where N is the string size obtained for each dc-dc MIC category and $0 < \alpha < 1$ shows the ratio of the number of modules that are exposed to mismatch under worst-case scenario to the total number of modules required to create PV system with a specific rated power. In fact, (3.39) assures that the PV system is exposed to the same per unit mismatch regardless of the dc-dc MIC category used for its PV modules. To better illustrate the comparison results string size is normalized with respect to benchmark string size N_b,

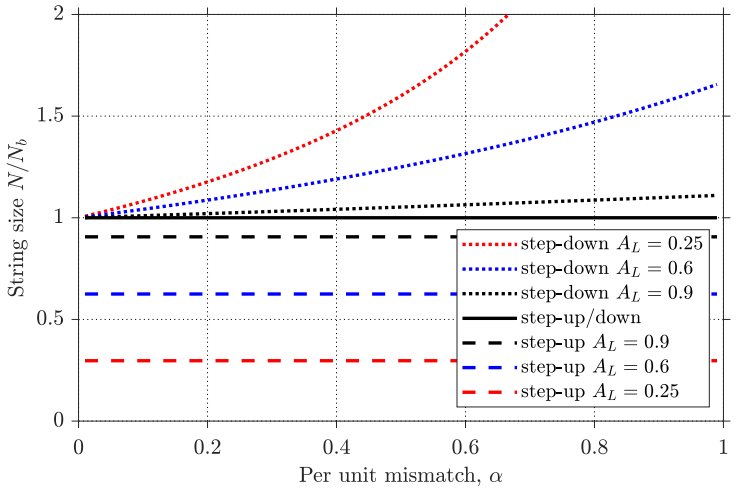


Fig. 3.3: Normalized string size of dc-dc MICs versus per unit worst-case mismatch for different values of A_L.

and total output stress is normalized with respect to $V_{MPP}I_{MPP}$. Replacing (3.39) in (3.9) and (3.18) and normalizing them with respect to N_b results in:

$$\frac{N_{sd,min}}{N_b} = \frac{1}{1-(1-A_L)}, \tag{3.40}$$

$$\frac{N_{su,max}}{N_b} = A_L + \frac{(1-A_L)}{N_b}, \tag{3.41}$$

As discussed earlier, the minimum converter stress for step-down and step-up MICs are obtained for a string size as given in above equations so they have been selected as the string size for step-down and step-up MICs. Also, the step-up/down MIC string size N_b when normalized to benchmark string size N_b results in:

$$\frac{N_{sd,min}}{N_b} = 1 \tag{3.42}$$

It can be observed from (3.40)-(3.42) that all string sizes except the step-up string size are independent of N_b. For a given set of $V_{bus,c}$ and V_{MPP}, the benchmark string size and accordingly step-up string size can also be calculated. Figure 3.3 shows the string size of various categories of the dc-dc MICs versus per unit worst-case mismatch for different values of A_L, assuming that $N_b = 16$. As can be seen the string size for step-down MICs is larger than benchmark string size and it increases as increases or A_L decreases. Step-up MICs string size is smaller than benchmark string size and it is reduced as A_L is reduced while it is independent of α. The normal voltage conversion ratio which

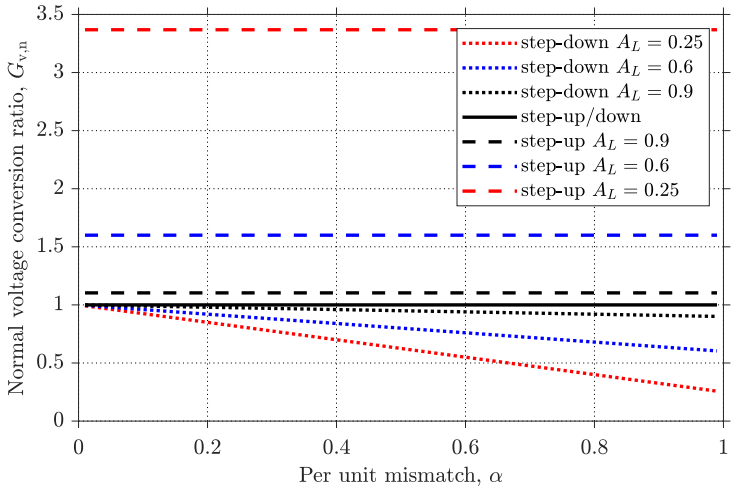


Fig. 3.4: Normal voltage conversion ratio of dc-dc MICs ($G_{v,n}$) versus per unit worst-case mismatch α for different values of A_L.

is obtained when there is no mismatch in the PV system is derived by inversing the normalized string size since the normal voltage conversion ratio is the required voltage gain for MICs to keep the dc bus voltage constant despite the deviations of the string size from N_b. Figure 3.4 shows the normalized voltage conversion ratio for various dc-dc MIC categories. As can be seen the step-up MIC voltage conversion ratio deviates significantly from unity conversion ratio as A_L is decreased. The step-down MICs voltage conversion ratio drops linearly by the increase of and slope of this drop is larger for small values of A_L.

To find the total stress applied to MICs for different worst-case mismatch parameters, equations (3.39) to (3.42) are replaced in (3.12), (3.23) and (3.27). It has been revealed that under the mismatch worst-case scenario defined by (3.39) and using the string sizes as shown in (3.40) - (3.42), all three categories of MICs will result in the same total stress which is derived as follows:

$$\frac{VA_{rated}}{V_{MPP}I_{MPP}} = \frac{1}{1-\alpha(1-A_L)} \tag{3.43}$$

Figure 3.5 shows the total stress of the converter output which is derived as (3.43) versus per unit worst-case mismatch of PV system for different values of A_L. The total stress is the same for all MIC categories and it is increased with the increase of and decrease of A_L.

Now that all the categories of dc-dc MICs are analyzed for constant voltage dc bus

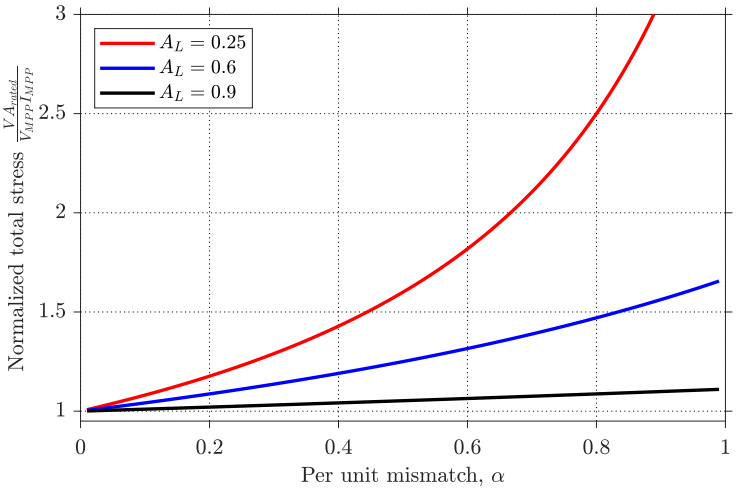


Fig. 3.5: Normalized total output stress of dc-dc MICs $((VA_{rated})/(V_{MPP}I_{MPP}))$ versus per unit worst-case mismatch α for different values of A_L.

configuration they can be compared. The total stress of the different categories of MICs is the same, and the most important factor in the comparison is the string size and normal voltage conversion ratio. Step-up MICs have smallest string size among all dc-dc MICs and operate with normal voltage conversion ratios that are significantly deviated from unity, and as such they are not suitable for constant dc bus configuration. Step-down MICs allow the greatest number of panels per string and can save some BOS costs by using a smaller number of strings. However, their voltage conversion ratio deviates from unity as the string size is increased. The step-up/down MICs cannot offer the string length increment however they operate with unity conversion ratio when there is no mismatch and as such, they can improve the overall efficiency of the PV system. There are also two points about step-up/down MIC realization in component level that must be considered when this MIC is compared to step-down MIC. First, the efficiency of a step-up/down converter in general is less than a step-down converter with the same components stress in both full power realization and partial power realization. In full power realization either two-switch or four-switch topologies are adopted. Two-switch topology suffers from high inductor current problem and non-optimal efficiency at unity conversion ratio as the unity conversion ratio is obtained at d=0.5 which requires periodic switching of the converter rather than a pass-through operation. Four-switch step-up/down topology uses two extra switches; thus, it has increased cost and losses compared to two-switch step-down topology. In partial power realization, bipolar output voltage is required for which at least two extra switches must be added to the topology.

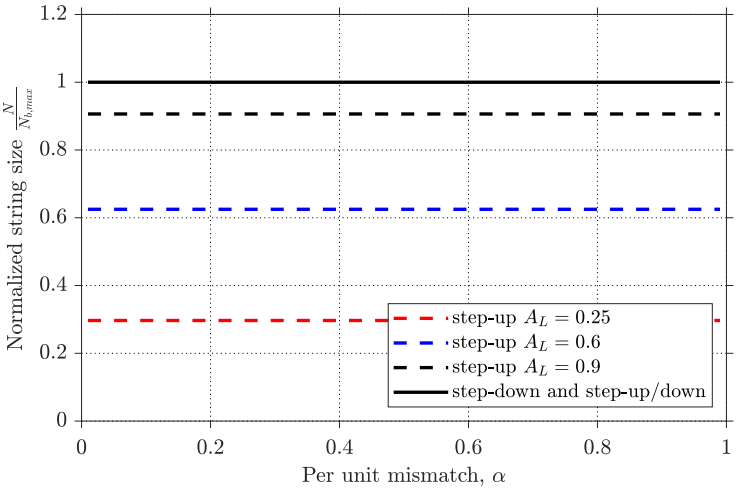


Fig. 3.6: Normalized string size for different dc-dc MIC categories under variable voltage dc bus configuration versus per unit mismatch α for different values of A_L.

The extra switches increase the cost and losses in the converter. Second, the inductor of step-up/down topology is placed in between its switching devices while the inductor of the step-down topology in full power realization is placed at the output side which allows optimization of the inductive filter. Inductor of the step-down MICs can be removed from converters and be replaced with a single, and more efficient inductor at the connection point of the string to the dc bus. Also, the output inductance required for the step-down MICs can be reduced significantly by operating them in interleaved mode. The inductive filter optimization in partial power realization of step-down converters will be discussed in section IV. In conclusion, both step-down and step-up/down MICs have advantages for PV systems with constant dc bus voltage and depending on application requirements and priorities one can select between these two categories. For variable dc bus voltage configuration, the following parameters are calculated for various K_L and A_L values to compare the three categories of dc-dc MICs: string size, different voltage conversion ratios of PV system MICs under the mismatch operation, and converter voltage/current stresses. Solar inverters normally have a maximum input voltage which can be used to obtain the maximum string size for each category of dc-dc MICs. For a given maximum dc bus voltage $V_{dc,max,rated}$ and rated MPP voltage of modules V_{MPP}, the maximum benchmark string size can be obtained as:

$$N_{b,max} = \frac{V_{bus,max,rated}}{V_{MPP}} \tag{3.44}$$

To have equal level of mismatch for various categories of MICs, the worst-case mismatch

is again assumed to be as described by (3.39). Using (3.31) and (3.35), the normalized string size for different dc-dc MICs is obtained as:

$$\frac{N_{step-down}}{N_{b,max}} = \frac{N_{step-up/down}}{N_{b,max}} = 1 \tag{3.45}$$

$$\frac{N_{step-up}}{N_{b,max}} = A_L + \frac{1 - A_L}{N_{b,max}} \tag{3.46}$$

As can be seen, the normalized string size for step-up MICs is a function of $N_{b,max}$ and it can be obtained for any given $N_{b,max}$. Assuming $N_{b,max} = 24$, Fig. 3.6 shows the normalized string size for the different dc-dc MIC categories under variable voltage dc bus configuration versus per unit mismatch for various A_L values.

As can be seen the string size in variable dc bus voltage configuration is not dependent on the per unit power mismatch under worst-case scenario. Step-up MICs result in small string sizes specially for low A_L values, which means this category of MICs requires larger number of strings for a given power level of the PV system and it increases BOS costs. The string length is designed to assure that dc-dc MICs operate with unity conversion ratio when there is no mismatch in the PV system which is only obtained with the aid of inverter MPPT. When there is a power mismatch in PV system the inverter MPPT helps to operate converters with close to unity conversion ratio. However, when there is power mismatch in PV system, to perform MPPT each of the low power generating modules and the rated power generating modules will require different voltage conversion ratios which will be shown by $G_{v,LP}$ and $G_{v,RP}$, respectively. These voltage conversion ratios are obtained according to Fig. 3.2 as follows:

$$G_{v,RP}(step - down) = 1 \tag{3.47}$$

$$G_{v,LP}(step - down) = A_L \tag{3.48}$$

$$G_{v,RP}(step - up) = \frac{1}{A_L} \tag{3.49}$$

$$G_{v,LP}(step - up) = 1 \tag{3.50}$$

$$G_{v,RP}(step - up/down) = \frac{1}{B} \tag{3.51}$$

$$G_{v,LP}(step - up/down) = \frac{A_L}{B} \tag{3.52}$$

As can be seen the conversion ratios are independent of per unit worst-case mismatch α. The step-up/down MIC conversion ratios are a function of B, and here only $A_L <$

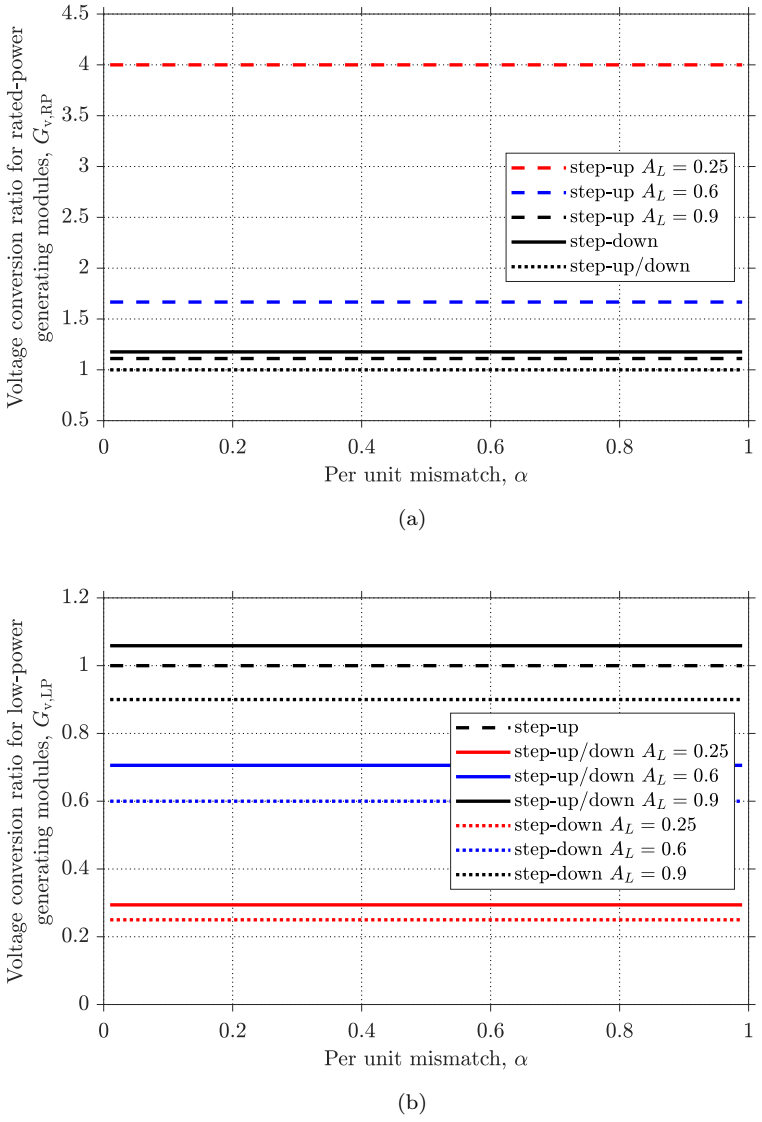


Fig. 3.7: The voltage conversion ratio of the (a) rated power and (b) lower power generating modules for different categories of dc-dc MICs and assuming $B = 0.85$ for step-up/down MICs.

$B < 1$ is considered as the voltage conversion ratios obtained for this range are close to unity. Figure 3.7 shows the voltage conversion ratio of the rated power and lower power generating modules for different categories of dc-dc MICs and assuming $B = 0.85$ for step-up/down MICs. Further discussion is given in coming sections about selection of B value. As can be seen, step-down MICs provide unity conversion ratio for rated power generating modules under mismatch scenario. The step-up/down and step-up MICs provide larger than unity conversion ratio for rated power generating modules and the conversion ratio deviation from unity in step-up MICs increases with the decrease of A_L. Step-up MICs provide unity conversion ratio for low power generating modules

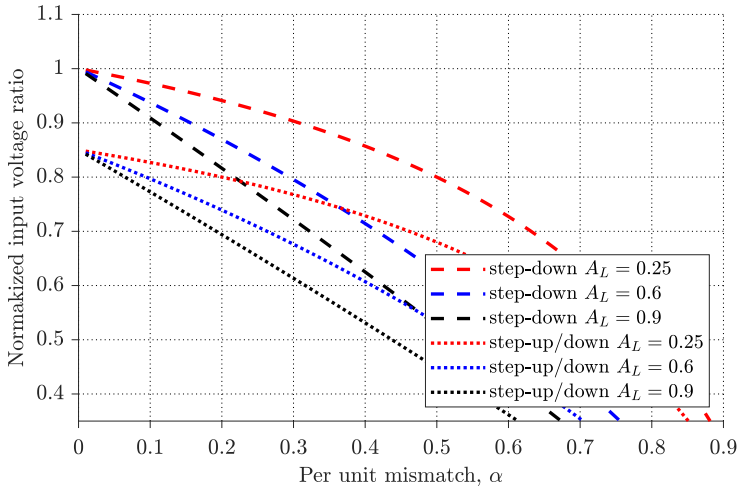


Fig. 3.8: Normalized input voltage ratio for different dc-dc MIC categories under variable voltage dc bus configuration versus per unit mismatch α for different values of A_L.

under mismatch scenario. Step-up/down and step-down MICs provide non-unity voltage conversion ratios and their deviation from unity is increased with the decrease of A_L. The step-up/down MIC provides lower deviation from unity compared to step-down, however the difference in their conversion ratios become insignificant for low values of A_L. The other important factor for variable dc voltage inverters is the input voltage ratio that is obtained using each category of dc-dc MICs. The input voltage ratio of different dc-dc MIC categories can be normalized by dividing them to the benchmark input voltage ratio given in (3.30). Benchmark voltage ratio shows the input voltage ratio for a PV system equipped with bypass diodes. Replacing (3.39) in (3.33), (3.37) and (**??**) and normalizing them with respect to (3.30) gives:

$$VR^{norm}_{step-down} = \frac{1-\alpha}{1-\alpha(1-A_L)} \tag{3.53}$$

$$VR^{norm}_{step-up} = \frac{N_{b,max}}{(1-\alpha)\left(A_L N_{b,max} + (1-A_L)\right)} \tag{3.54}$$

$$VR^{norm}_{step-up/down} = B\frac{1-\alpha}{1-\alpha(1-A_L)} \tag{3.55}$$

Figure 3.8 shows the normalized input voltage ratio for different categories of dc-dc MICs. Now that all the categories of dc-dc MICs are analyzed for variable voltage dc bus configuration they can be compared. The step-down and step-up/down MICs provide the longest string size and best BOS costs, while step-up MICs have significantly smaller string size if the low values of A_L are considered. Normally, if the shading causes

mismatch A_L is small as most of the generated power is blocked under shading. Step-down and step-up/down MICs can operate with lower input voltage ratios compared to benchmark input voltage ratio however the step-up MICs require significantly wider input voltage range. When there is a mismatch in PV system, only the step-down MICs allow the rated power generating modules to operate with unity voltage conversion ratio. Therefore, it can be concluded that only for step-down MICs the rated power generating modules always operate with unity conversion ratio regardless of power mismatch. Since these modules always operate with unity conversion ratio with and without power mismatch, they can be directly connected to the string without any power converter, which significantly improves the cost and power efficiency. This feature is useful for those PV applications where the shaded panels are known as a priori. Furthermore, the step-down MICs has a total output stress equal to $V_{MPP}I_{MPP}$ while step-up/down MICs have total output stress equal to $1/BV_{MPP}I_{MPP}$. In Fig. -8, B value adopted for step-up/down MIC is $B = 0.85$ while it can have any value. If $B = 1$ then step-up/down MIC will be the same as step-down MIC. Reducing B value from 1 makes the input voltage ratio smaller however it causes more deviation from unity for voltage conversion ratio of rated power generating modules and increases the voltage rating of the converter. Selecting B values larger than unity increases the current stress on the MIC and still has the problem of non-unity conversion ratio for all modules under mismatch condition. According to above discussion, the best configuration for variable dc bus voltage configurations is the step-down MICs which gives the ability of adding MICs as much as needed along with its other merits.

The PV system inverter type from the dc bus voltage perspective affects the suitable dc-dc MIC category selection. The main advantage of inverters with constant voltage is that their efficiency can be optimized as they have constant input voltage, while the variable voltage inverters need to cover a range of voltages which may reduce their efficiency. However, there are several aspects that must be considered when comparing these two types of inverters for PV systems. First, in constant dc voltage inverter systems only the dc-dc MICs perform the MPPT and as such they must fulfill an extensive range of power conversion requirements which adversely affects their efficiency and overall system efficiency. The MPP characteristics of PV modules in general are affected by temperature and irradiance and they both might be nonuniform depending on the application. The nonuniform irradiance which is also known as power mismatch among PV modules is

more common and has been discussed above for constant voltage inverters. As it is shown, the dc-dc MICs may experience increased ratings compared to their PV modules or may operate away from their unity conversion ratio if they are used to perform MPPT on their own without the aid of inverter. The uniform irradiance and temperature changes also affect the MPP characteristics. The uniform irradiance variation does not change the MPP voltage a lot and only reduces all the MPP currents of the PV modules. Thus, the MICs will simply operate with the same conversion ratios but with a reduced power which does not affect their efficiency a lot. Uniform temperature variation, that occurs in daily and yearly cycles, changes the MPP voltage of the PV modules. To keep the dc bus voltage constant in spite these MPP voltage changes all the PV modules must be equipped with dc-dc MICs and these MICs will be forced to operate at non-unity conversion ratios for all temperatures except a single temperature. Considering the adverse effects that keeping the dc bus voltage has on the ratings, operating point conversion ratio and consequently efficiency of the MICs, the inverter efficiency gain obtained from employing constant dc bus voltage can be compromised depending on the application. However, if the variable dc bus voltage is employed, the inverter itself responds to uniform temperature variations by changing the dc bus voltage. Therefore, dc-dc MICs will operate at their unity conversion ratio and optimal efficiency in the face of temperature variations. In this case, there is no need to employ dc-dc MICs for PV modules that will never experience shading or extreme power mismatch. Normally the extreme power mismatches occur due to the shading. As the shading is normally caused by objects that have a known position such as chimney, trees, etc., the modules which undergo the nonuniform shading can be determined as a priori. Then, then only those modules that are expected to be shaded can be equipped with dc-dc MICs which saves significant cost and power processing in the system. As discussed earlier, the only dc-dc MIC category that keeps this feature under nonuniform irradiance variations or power mismatch is the step-down MICs. Furthermore, step-down dc-dc MICs employed with variable dc bus voltage inverters have the lowest total output stress which is not increased in presence of mismatch. Also, employing the step-down dc-dc MICs rather than bypass diodes reduces the voltage variation range that is required to perform MPPT in presence of nonuniform irradiance. This can help to further improve the efficiency of the PV inverter. The second factor that must be considered when comparing the constant dc bus inverters with variable dc bus inverters is that the new PV inverters have improved topologies and achieve better efficiency over wide input voltage variations

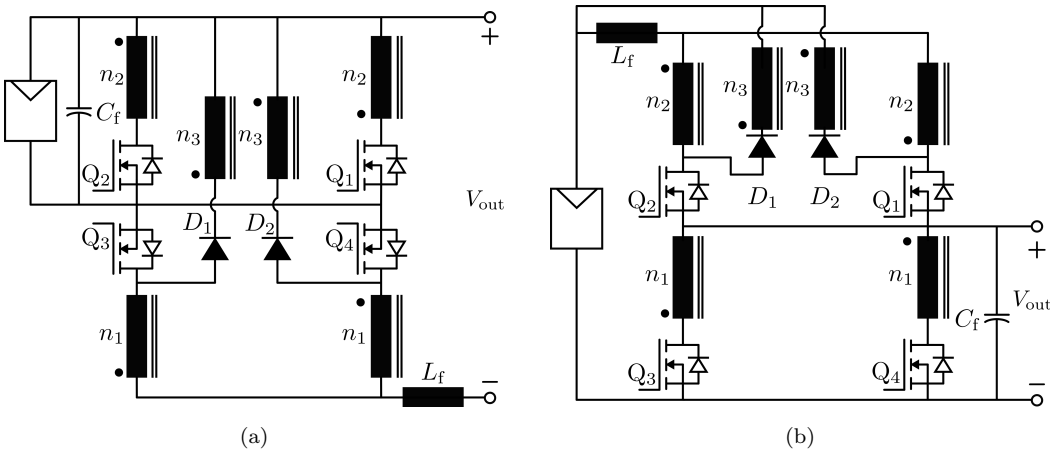


Fig. 3.9: The proposed soft-switching high-frequency topology for step-down MICs implemented using (a) IPOS and (b) ISOP configuration.

compared to the conventional PV inverters [55]. The third factor is the availability and vast deployment of the variable voltage inverters in the current market and existing PV systems. Variable dc voltage PV inverters are the conventional MPPT method for PV systems that are not exposed to heavy power mismatch or the PV systems that were installed before the development of MIC concept, and they have a large portion of the existing market. Thus, the more feasible approach to improve the efficiency of these PV systems is to employ dc-dc MICs which are designed for variable dc bus voltage inverters rather than totally changing the inverter. According to the above discussion, the step-down dc-dc MIC is adopted in this report to be designed in component level. To improve the efficiency of these MICs partial power processing concept is used which will be further discussed in the next sections.

3.2 Soft-Switching High-Frequency MIC Topology

In this section, a soft-switching high frequency topology is proposed for the step-down PV MIC. The proposed topology adopts series partial power processing to further improve the efficiency, thus can be implemented using both IPOS and ISOP configuration. Figure 3.9 shows the proposed topology for the MIC implemented using IPOS and ISOP configurations. Operation of the proposed topology is described using IPOS implementation and its ISOP operation can be described using a similar approach to the IPOS case. The general realization of the PV MIC would be as shown in Fig. 3.9(a), however

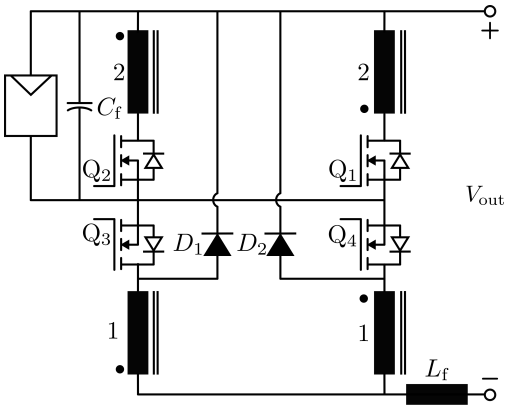


Fig. 3.10: Realization of the proposed MIC with $n_3 = 2 - n_2$, and $n_2 = 2$ to simplify the magnetic components.

some simplifications are still possible. The inductor L_f can be removed from converters and be replaced by a larger single inductor on the inverter dc bus. The turns ratio used for the transformer are as $n_2 = N_2/N_1$ and $n_3 = N_3/N_1$ which can be designed based on the converter operating mode requirements. For a specifc operating mode, diodes D_1 and D_2 are used to clamp the voltages across the switches Q_3 and Q_4. For this operating mode, n_3 must be selected as $N_3 = 2N_1 - N_2$ to be able to clamp the OFF state voltages of Q_3 and Q_4 to the PV voltage. If $n_2 = 2$ for this operation, then n_3 becomes zero and two windings can be saved in realization. Therefore, using these turn ratios, MIC realization is simplified as shown in Fig. 3.10. It is important to note that all the switches are on the same ground and there is no need for power isolation for gate driving of the proposed converter. Furthermore, the inductor can be integrated with the transformer to reduce the size and cost and improve the efficiency. Normally, series partial power converters are controlled using the duty cycle and/or frequency control which is not efficient for the entire load/voltage range. However, Due to the specific structure of the proposed topology, instead of conventional controls, it can be controlled by toggling the converter operating mode among the three feasible states. Duration of the converter operation in each of these operating modes can then be used to control the voltage gain and hence perform MPPT. It is shown that using this time allocating partial power processing technique the MPPT range is extended to the full MPPT range of a PV module without any efficiency penalty at the nominal range.

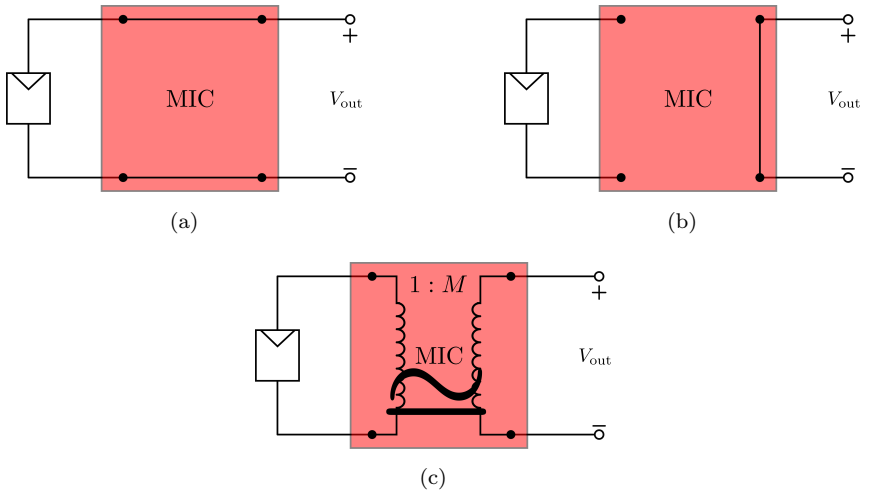


Fig. 3.11: The (a) pass-through, (b) bypass and (c) process modes of operation for the proposed soft-switching high-frequency topology.

3.2.1 Different Modes of MIC Operation

The three modes of operation for the proposed topology are shown in Fig. 3.11 in the MIC's high-level representation. The pass-through mode simply connects the PV module to the output as if there is no conversion at all. The conversion ratio of the pass-through mode is 1. The bypass mode bypasses the output terminal while leaving the PV module open-circuit, thus results in a conversion ratio of 0. MIC in the process mode acts as a DC transformer with constant conversion ratio $0 < M < 1$. Therefore, any conversion ratio between M and 1 can be obtained by proper allocation of the time to pass-through and process modes while conversion ratios between 0 and M are obtained by time allocation between bypass and process modes. Converter operation in each of these modes is described as follows:

3.2.1.1 Pass-through Mode

Figure 3.12 shows the converter circuit in Pass-through mode. In this mode, switches Q_1 and Q_2 are turned-off and switches Q_3 and Q_4 are turned-on causing clamp diodes D_1 and D_2 to be reverse-biased. In this mode, the capacitive filter is discharged by $-(I_{str} - I_{PV})$ current whereas, the inductive filter is charged by $V_{PV} - V_{out}$ voltage. If the converter stays in this mode for an adequately long time, filters let $I_{str} = I_{PV}$ and $V_{out} = V_{PV}$, thus MIC voltage gain becomes 1.

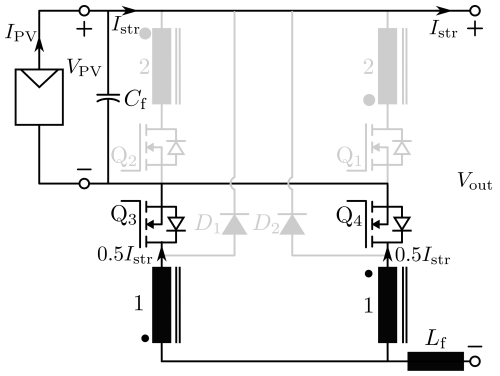


Fig. 3.12: MIC equivalent circuit for Pass-through mode operation.

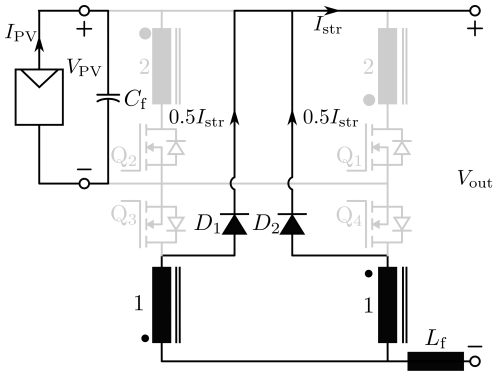


Fig. 3.13: MIC equivalent circuit for Bypass mode operation.

3.2.1.2 Bypass Mode

In Bypass mode, all switches (Q_1, Q_2, Q_3, and Q_4) are turned-off and clamp diodes D_1 and D_2 are forced to conduct the string current I_{str} . MIC equivalent circuit for Bypass mode is shown in Fig. 3.13. In this mode, the capacitive filter is charged by the PV current I_{PV} whereas, the inductive filter is discharged by $-V_{out}$ voltage across it. The converter terminals act as short-circuit if the converter stays in this mode for a long time and the voltage gain becomes zero.

3.2.1.3 Process Mode

In this mode, switches are turned ON and OFF periodically in every switching cycle to process the power using the high frequency transformer. The leakage inductance of the transformer and switch output capacitance are used in this mode to obtain soft-switching operation for the converter. Furthermore, the diodes D_1 and D_2 which are normally used for bypass mode realization are used as clamp diodes in Process mode

operation. Using a specific switching scheme, energy stored in the switch capacitances is restored by the clamp diodes.

The switching scheme of the converter, its components voltage and current waveforms, and switching intervals during each switching period in this mode are shown in Fig. 3.14. The waveforms are obtained for the following assumptions. Capacitor C_f is large enough to keep the voltage constant during the switching cycle. Transformer magnetizing inductance is large enough to be ignored. Total transformer leakage inductance reflected to the string side is denoted by L_{lkg} which is shown on both of the string side windings with an inductance value of $0.5L_{lkg}$. Gate pulses for Q_3 and Q_4 are phase shifted by 180^o and have duty cycles $D > 0.5$ to avoid disruption of inductive filter's current. Gate pulses for Q_1 and Q_2 have 50% duty cycle with a deadtime inserted at the rising edge. Gate pulses for Q_1 and Q_2 are phase shifted by $(D - 0.5) \times 180^o$ with respect to Q_4 and Q_3, respectively. The MOSFETs are modeled as an ideal switch with a parallel capacitor representing the output capacitance. Diodes are modeled as ideal diodes in series with a forward voltage drop. Based on the assumptions, there are 12 switching intervals from which 6 switching intervals $M7$ to $M12$ are the complement of $M1$ to $M6$. Converter operation in each of the switching intervals $M1$ to $M6$ is described below:

***M*1 ($t_0 < t \leq t_1$), see Fig. 3.15(a):** This switching interval begins right after the dead time between Q_1 and Q_2. At the end of the dead time, voltage across Q_2's output capacitance, i.e. C_{oss2}, has reached zero and the anti-parallel diode of Q_2 conducts the current through top left winding. Also, switch Q_3 was conducting prior to this interval, thus the string current, I_{str} , was passing through Q_3 mainly. A small portion of I_{str} was passing through the clamp diode D_2 because of turning off the switch Q_4 . This interval begins with the turn ON of Q_2 which turns on with zero voltage switching (ZVS). When Q_2 is on, V_{PV} is applied on the top left winding resulting in a reflected voltage equal to $0.5V_{PV}$ on each of the bottom side windings. The major part of I_{str} passes through the switch Q_3 and bottom left winding in this interval which loads the high-frequency transformer with a power of $0.5V_{PV}I_{str}$, i.e. half of the rated power of PV. Also, the small portion of I_{str} which passes through the clamp diode D_2 discharges the leakage inductance L_{lkg} using the loop composed of PV, Q_3, leakage inductance, bottom side windings and the clamp diode D_2 . Current of D_2 decays over the time due to the voltage drop of the diode and reaches to zero during the interval M1 ($t_0 < t \leq t_1$). In this interval, switches Q_1 and Q_4 are turned OFF and tolerate $2V_{PV}$ and V_{PV} voltage

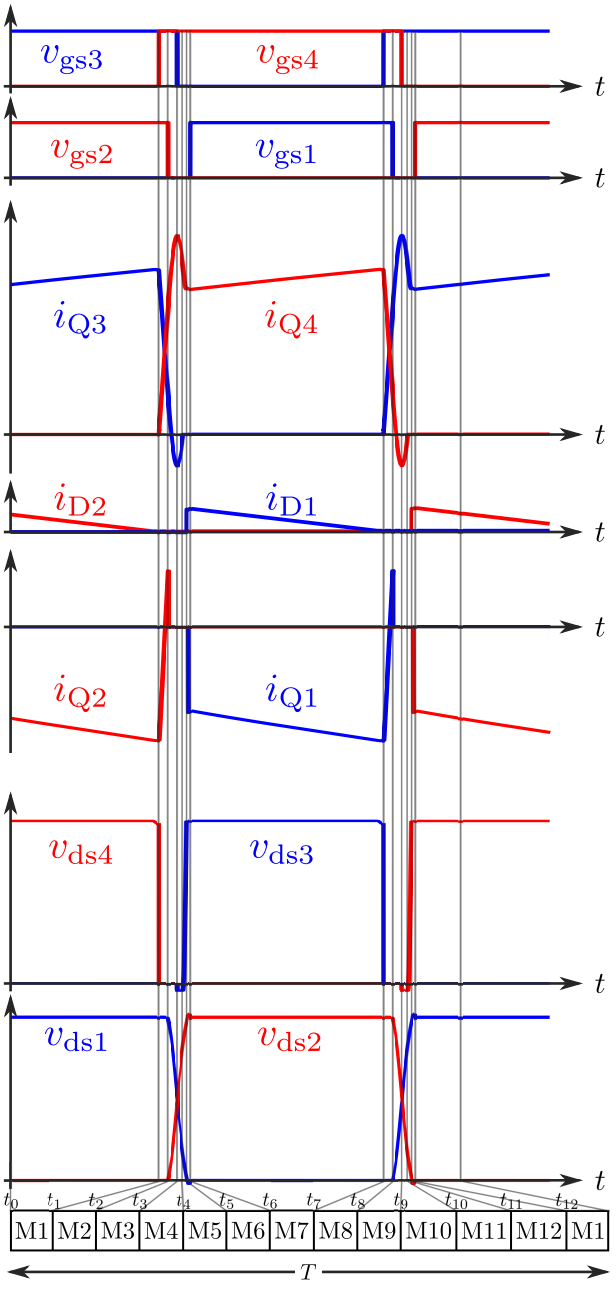


Fig. 3.14: MIC switching schemes, intervals and waveforms for the Processing mode.

stresses, respectively. The capacitive filter is charged by $I_{PV} - 0.5I_{str}$ current whereas, the inductive filter is discharged by $-(V_{out} - 0.5V_{PV})$ voltage. This interval ends at t_1 when the switch Q_4 turns ON and I_str starts to commutate to Q_4.

***M2* ($t_1 < t \leq t_2$), see Fig. 3.15(b):** Switch Q_4 turns ON at the beginning of this interval and the overlap of the Q_3 and Q_4 is started to ensure that the inductive filter L_f current is not disrupted. Furthermore, switch Q_2 is ON and applies $+V_{PV}$ on the top left winding of the transformer. The reflected voltage to the combination of bottom

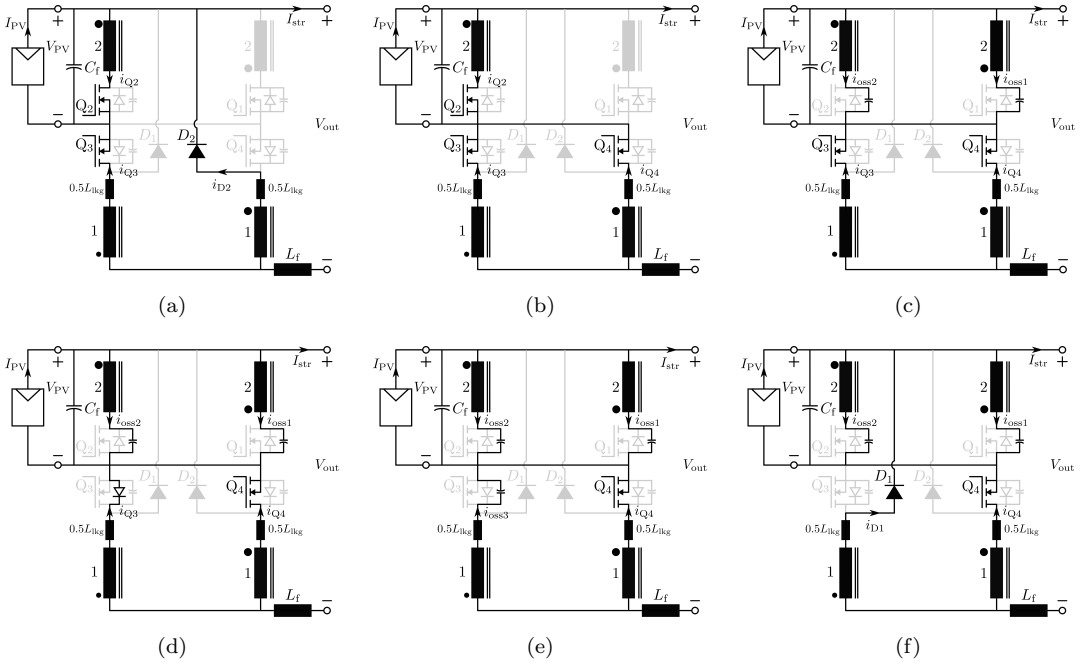


Fig. 3.15: MIC equivalent circuit during switching intervals (a)$M1$, (b)$M2$, (c)$M3$, (d)$M4$, (e)$M5$ and (f)$M6$ of the Process mode.

side windings of transformer is $+V_{PV}$ that is applied on the leakage inductance as the switches Q_3 and Q_4 are ON and create a short circuit path for these windings. The voltage applied on the leakage inductance decreases the Q_3 current and increases the Q_4 current, thus it shifts the current from Q_3 to Q_4 with a slope determined by the value of leakage inductance. As can be seen, Q_4 turns ON with zero current switching (ZCS) and leakage inductance acts as a snubber for it to further reduce the switching losses. To balance the MMF within the core $i_{Q2} = 0.5\,(i_{Q4} - i_{Q3})$. Thus, when half of the overlap time is elapsed, Q_3 current equals the Q_4 current and the Q_2 current becomes zero. This is the end of $M2$ interval when Q_2 turns OFF with ZCS.

***M3* ($t_2 < t \leq t_3$), see Fig. 3.15(c):** Switch Q_2 turns OFF at the beginning of this interval and the dead-time between Q_1 and Q_2 is started. Switch output capacitance (C_{oss}) for Q_1 and Q_2 start to resonate with the leakage inductance which discharges C_{oss1} and charges C_{oss2}. Until C_{oss1} is not discharged to 0 or equivalently C_{oss2} is not charged to V_{PV} , the resonance mode continues and causes the Q_3 current to become negative and Q_4 current to slightly go beyond I_{str}. This interval ends at t_3 when Q_3 turns off with a negative current, thus its current diverts to the body diode and it turns OFF with zero voltage switching (ZVS).

***M*4 ($t_3 < t \leq t_4$), see Fig. 3.15(d):** In this interval, the leakage inductance current passes through Q_2 and the body diode of Q_3. The resonance between output capacitances of Q_1 and Q_2 continues in this interval. As C_{oss1} is charged towards $+2V_{PV}$ and C_{oss2} is discharged towards zero, Q_3 current rises to zero and Q_4 current falls to I_{str}. This relatively short interval ends at t_4 when the current of the body diode of Q_3 becomes zero.

***M*5 ($t_4 < t \leq t_5$), see Fig.3.15(e):** In this interval, the body diode of Q_3 is turned off and its output capacitance C_{oss3} along with C_{oss1} and C_{oss2} form a resonant circuit with leakage inductance. As C_{oss3} charges towards V_{PV} , the leakage inductance current reaches its peak value in the resonance cycle. In order to avoid voltage ringing on Q_3, which deteriorates the converter efficiency and may cause converter failure due to voltage spikes, the clamp diode D_1 is added to clamp the Q_3 voltage to V_{PV} and recover the energy stored in the leakage inductance. This interval ends when the Q_3 voltage reaches V_{PV} and clamp diode D_1 turns ON.

***M*6 ($t_5 < t \leq t_6$), see Fig. 3.15(f):** Clamp diode D_1 starts conducting at the beginning of this interval and the leakage inductance current flows to the capacitive filter through D_1. As C_{oss2} is not yet discharged to zero and C_{oss1} is not fully charged to $+2V_{PV}$ the voltage across the PV side winding (combined top side windings) is less than $+2V_{PV}$. Thus, reflected voltage on the string side (bottom side windings) is less than $+V_{PV}$ while the capacitive filter voltage is $+V_{PV}$. Then the difference of these two values is applied to the leakage inductance along with the voltage drop of diode D_1 . This voltage drop decreases the current though the leakage inductance and diode. This interval ends at t_6 when the C_{oss2} is discharged to zero and Q_2 turns ON with the zero voltage switching (ZVS).

The intervals $M7$ to $M12$ are complements of the intervals $M1$ to $M6$ and the converter operation in these intervals is like the above description.

According to principle of operation discussed above, converter switches always turn ON and OFF with soft switching in Process mode which results in higher efficiency and allows higher power densities. The converter operation here is described for $n_2 = 2$ and $n_3 = 0$ while the other turns ratio are feasible. The only requirement on the turns ratio with the clamping capabiltiy described here is $n_3 = 2 - n_2$, and any N_1,N_2, and N_3 that satisfies this constraint can be used.

The operation of the ISOP counterpart of the MIC is similar to the IPOS configuration that has been discussed here while the voltage and current stress of the switches might be different as a result of swapping the ports of the MIC from PV side to string side in ISOP configuration.

3.2.2 PV MPPT Using the Pulse Density Modulation

The control method optimizes the PV power generation and performs MPPT by regulating the output voltage V_{out}. MIC sets the V_{out} between zero and V_{PV} to respond to the changes in PV power generation. If the converter operates in Bypass mode for a long time the output voltage V_{out} becomes zero and the PV power generation is zero. If the converter operates in Pass-through mode for a long time, the output voltage V_{out} becomes equal to the PV voltage V_{PV} and the PV power generation becomes $I_{str}V_{PV}$. Assuming that $n_2 = n$, if the converter operates in Process mode for a long time $V_{out} = V_{PV}(1-\frac{1}{n})$ (i.e., voltage gain is $1-\frac{1}{n}$), and PV power generation is $I_{str}V_{PV}(1-\frac{1}{n})$. For any PV power generation between zero and $I_{str}V_{PV}(1-\frac{1}{n})$, the controller sets the duration of the converters operation in each of the Process mode and Bypass modes using pulse density modulation (PDM). If the duration of Process mode to the total duration of PDM cycle is denoted by D_{pdm}, then:

$$V_{out} = D_{pdm}(1-\frac{1}{n})V_{PV}. \tag{3.56}$$

Similarly, for any PV power generation between $I_{str}V_{PV}(1-\frac{1}{n})$ and $I_{str}V_{PV}$, the controller sets the duration of the converter's operation in each of the Pass-through and Process modes using PDM. If the duration of Process mode to the total duration of PDM cycle is denoted by D_{pdm}, then:

$$V_{out} = (1 - D_{pdm}/n)\, V_{PV}. \tag{3.57}$$

In fact, using the proposed PV MIC, the converter only processes the power difference between $I_{str}V_{PV}$ and the current power generation of the PV panel.

3.2.3 Selection of Partial Power Processing Configuration

In this section, the two common configurations of partial power processing IPOS and ISOP are compared for the step-down PV dc-dc MIC application. The input voltage of the dc-dc MIC is PV voltage which is fairly constant if MPPT is performed on PV modules. The output current is also determined by the maximum power generation of all modules in the string which is determined by the uniform temperature and irradiance that the PV system in total is exposed to. The output current is changed in a range of zero to nominal MPP current of the PV modules and worst case from the MIC power processing point of view is nominal PV MPP current. Thus, the MICs can be compared assuming a given input voltage and output current while the output voltage and input current are subject to change based on power mismatch applied on the PV module. Below are the input and output voltage/current of the dc-dc MIC:

$$V_{i,MIC} = V_{MPP}, \tag{3.58}$$

$$V_{o,MIC} = \Delta V_{MPP}, \tag{3.59}$$

$$I_{o,MIC} = I_{MPP}, \tag{3.60}$$

$$I_{i,MIC} = \Delta I_{MPP} \tag{3.61}$$

, where V_{MPP} and I_{MPP} are the rated MPP voltage and current respectively and $\Delta_{min} < \Delta \leq 1$ shows the relative power generation of the PV module. The two partial power configurations possible for dc-dc MIC implementation are shown in Fig. 1.2. According to Fig. 1.2 if the converters are considered as ideal power transfer blocks the actual converter of ISOP configuration which is in charge of processed portion of transferred power would have input and output voltage/currents as:

$$V_{i,con}^{ISOP} = (1-\Delta)V_{MPP}, \tag{3.62}$$

$$V_{o,con}^{ISOP} = \Delta V_{MPP}, \tag{3.63}$$

$$I_{i,con}^{ISOP} = \Delta I_{MPP}, \tag{3.64}$$

$$I_{o,con}^{ISOP} = (1-\Delta)I_{MPP} \tag{3.65}$$

Using the same assumptions input and output voltage/currents of the actual converter which is in charge of processed portion of transferred power are obtained for IPOS as:

$$V_{i,con}^{IPOS} = V_{MPP}, \tag{3.66}$$

$$V_{o,con}^{IPOS} = -(1-\Delta)V_{MPP}, \tag{3.67}$$

$$I_{i,con}^{IPOS} = -(1-\Delta)I_{MPP}, \tag{3.68}$$

$$I_{o,con}^{IPOS} = I_{MPP} \tag{3.69}$$

According to (3.62) and (3.66) if the converters are considered as ideal power transfer blocks the ISOP configuration would be deemed appropriate for MIC application at lower Δ values. However, the converters are not ideal power transfer blocks, and many factors determine the suitability of one converter for the application. In this section, the efficiency of the converter which itself is dependent on the component stresses and the component level implementation of the converter are discussed and it is shown that the IPOS converter may result in better efficiencies for the adopted topology and PDM control. According to (3.62) and (3.66), the output voltage of IPOS and input voltage of ISOP becomes zero for $\Delta = 1$. Also, according to the principal of operation described above, the adopted topology and PDM control can only provide a zero voltage on the terminal connected to the inductive filter. Therefore, the component level implementation of the IPOS and ISOP would be as shown in Fig. 3.9. According to Fig. 3.9 the inductive filter for IPOS realization is on the string side and it can be either totally eliminated and replaced by one larger and efficient inductor at the string connection point to the inverter or can be significantly reduced by interleaving the PDM signals for the different MICs in the panel. However, for the ISOP configuration the inductive filter is on the PV side and it cannot be removed or shrank in size. This gives a significant efficiency advantage for the IPOS which is not evident when converters are considered as ideal power transfer blocks. Other than this important advantage the transformer turns ratio and component stresses that are obtained for converter realization in IPOS and ISOP configurations would play a vital role in the efficiency comparison of them. Below the various losses obtained for two realizations of Fig. 3.9 are compared. The transformer ratio is obtained assuming the PDM operation of the MICs using Pass-trough and Process modes only covers the voltage conversion ratios needed for $\Delta_{min} < \Delta \leq 1$. The Bypass and Processing modes PDM operation would cover the $\Delta \leq \Delta_{min}$ which

statistically occurs less frequently in the PV operation time. Using (3.62) and (3.66) and considering the fact that the input and output of the realized converter in case of the IPOS configuration is swapped the required voltage conversion ratios for the actual converter of the partial power MIC configurations are:

$$G_v^{ISOP} = \frac{\Delta}{1-\Delta} \tag{3.70}$$

$$G_v^{IPOS} = \frac{1}{1-\Delta} \tag{3.71}$$

According to (3.57), and considering the inductive filter side as input of the the actual converter and PV side as its output, the actual converter voltage gain is obtained as:

$$G_v = \frac{V_{PV}}{V_{PV} - V_{out}} = \frac{n}{D_{pdm}}. \tag{3.72}$$

Now, (3.72) can be used to calculate n for the range of Δ variations. For $\Delta = 1$, both converters use $D_pdm = 0$ while for $\Delta = \Delta_{min}$, $D_{pdm} = 1$ is used and the transformer turns ratio for each converter is imposed as:

$$n_{ISOP} = \frac{\Delta_{min}}{1-\Delta_{min}} \tag{3.73}$$

$$n_{IPOS} = \frac{1}{1-\Delta_{min}} \tag{3.74}$$

According to (3.73), IPOS converter would always have a larger transformer ratio and as it is shown later in the paper, this results in better component stress on the switches and transformer that improves the efficiency compared to the ISOP configuration. Using the obtained transformer ratios, the switch voltages are derived as below:

$$V_{Q1,2}^{ISOP} = 2\frac{1-\Delta_{min}}{\Delta_{min}} V_{MPP} \tag{3.75}$$

$$V_{Q1,2}^{IPOS} = (1-\Delta_{min}) V_{MPP} \tag{3.76}$$

According to (3.75), the switch voltage stress for ISOP is $1/\Delta_{min}$ times larger than IPOS switch voltage stress. This results in extra conduction and switching loss in the ISOP converter. $R_{ds(on)}$ increases with the square of the voltage stress of the switch and thus a huge conduction loss difference is expected in switches Q_1 and Q_2. Furthermore, as switches Q_1 and Q_2 have ZCS which does not eliminate the capacitive switching losses the ISOP is expected to have a larger switching loss due to larger switch voltage stress.

The voltage stress on the switches Q_3 and Q_4 are as follows:

$$V_{Q3,4}^{ISOP} = \Delta V_{MPP} \tag{3.77}$$

$$V_{Q3,4}^{IPOS} = V_{MPP} \tag{3.78}$$

As the rating of switches are obtained for worst case scenario the voltage rating of switches Q_3 and Q_4 would be the same for both IPOS and ISOP i.e., V_{MPP} leading to same $R_{ds(on)}$. The ISOP converter would have less voltage stress on switches Q_3 and Q_4 for low values of Δ, however as these switches have ZVS turn on the switching loss of the converters will be negligible and same for both ISOP and IPOS. The transformer losses are composed of two parts: core and copper loss. As the voltage stress on the inductive filter side which is to be realized with 1 turn is larger for the ISOP converter it has larger core loss. However, the copper loss of the ISOP converter is Δ^2 of the IPOS converter and it gets smaller for lower values of Δ. It is important to note that the core loss is related to the exponent of voltage, normally third power of voltage for most ferrite cores, and it causes larger difference in core loss of IPOS and ISOP. Furthermore, as MIC application is normally considered as high power-density application the transformer has larger core losses than copper losses and changes in core loss are more pronounced. It can be concluded that the IPOS configuration offers better efficiency in the component level than ISOP configuration if they both are implemented using the proposed converter for PV application. The reason for this superior efficiency is the elimination of inductor using system level integration techniques and effects of transformer turns ratio and component stress on the converter loss.

3.3 Design and Experimental Verification of the Proposed MIC

In this section, the component selection for the IPOS step-down MIC is done for a sample PV application. It is important to note that the MIC component ratings and the conversion ratio of the Process mode are imposed by the transformer turns ratio. As discussed in Process mode section $n_3 = 2 - n_2$ is imposed by converter operation and transformer turns ratio is determined by selection of $n_2 = N_2/N_1$. As N_2/N_1 approaches to $1:1$ converter rating approaches the PV panel maximum power P_{PV}. However, for

N_2/N_1 equal to $n:1$, the converter power rating becomes P_{PV}/n. Increasing n, the converter power rating decreases while the power deviation that can be compensated using Process mode also decreases to $I_{str}V_{PV}/n$. The reduction of the power rating results in higher efficiency, power density, and lower cost for the PV MIC. However, it is important to note that Process mode is the most efficient operating mode of the MIC and selecting larger transformer turns ratio may reduce the energy capture of the PV system. Therefore, turns ratio is selected based on the statistical probability of the power mismatch on PV modules of a PV system. It is assumed for a PV system exposed to uneven shading that 50% power mismatch statistically covers the majority of the PV system operating points. Therefore, $n_2 = 2$ can be chosen to both save two windings in MIC realization and cover the statistically important operating points of a PV system. Assuming a PV module open circuit voltage of 50 V, the maximum voltage on the Q_3 and Q_4 would be 100 V and assuming a power level of 200 W, the transformer can be designed to withstand the core and conduction losses using natural convection according to the design process given in [56]. Using these assumptions, A PV MIC is built with components details as given in Table 3.1.

TABLE 3.1: Components and part numbers used in the prototyped high frequency and efficient partial power PV MIC

Components	Part Number and description
Switches Q_1, Q_2, Q_3 and Q_4	GS61008T, 100V Enhancement Mode GaN Transistor, $R_{ds(ON)} = 7m\Omega$
Diodes D_1 and D_2	CDBB5100-HF, Schottky Diode 100V & 5A
Magnetic Core	E32/6/20/R-3F4 + PLT32/20/3.2/R-3F4
Capacitive filter C_f	16 × GRM188R61H225ME11D, 2.2μF 50V

3.3.1 Experimental Verification

In this section, the proposed operation of the converter is experimentally verified using the prototyped MIC. The prototype MIC is built using the components listed in Table 3.1 and its picture is shown in Fig. 3.16. The ZVS operation of the switches Q_1 and Q_2 is experimentally verified according to Fig. 3.17. In this figure, the gate source voltage and drain source voltage of the switch Q_1 are shown. It can be seen that the drain source voltage of the switch reaches zero before the gate source voltage crosses the threshold

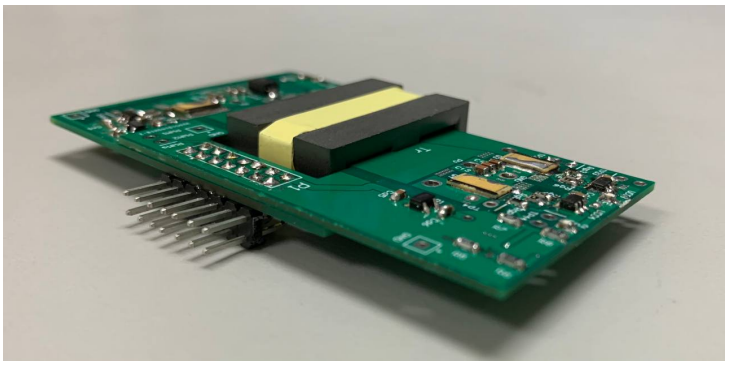


Fig. 3.16: Picture of the prototyped PV MIC for experimental verification.

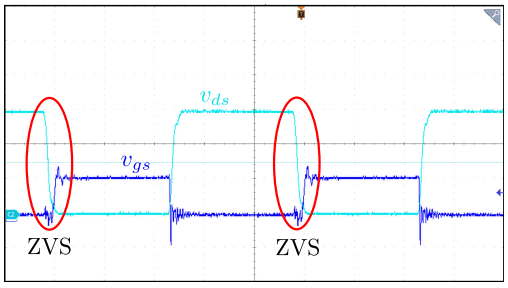


Fig. 3.17: ZVS switching waveforms of the Q_1 (v_{gs} blue with $5V/div$ and v_{ds} cyan with $20V/div$).

voltage and allows the switch Q_1 to turn on with ZVS. The same scenario occurs for switch Q_2 and it operates with ZVS as well. As discussed earlier, switches Q_3 and Q_4 turn ON with ZCS and turn OFF with ZVS. Figure 3.18 shows the the switching waveforms for switch Q_3 and verifies its soft-switching operation. As can be seen, the gate source voltage of the switch has reached below the threshold voltage before the drain source voltage rise, therefore ZVS turn OFF is achieved for these switches. Also, at turn ON, there is no Miller plateau which indicates that there is not significant amount of current in the MOSFET channel when turning it ON and this confirms the ZCS turn ON for the switches Q_3 and Q_4. It is important to note that due to the high frequency operation switch currents cannot be directly measured.

As discussed earlier, PDM method is used for the MIC to perform the MPPT. The PDM has been implemented through a 32 pulse train system, where the PDM duty cycle can be defined as:

$$D_{pdm} = \frac{N_{pdm}}{32}, \qquad N_{pdm} \in \{0, 1, 2, \cdots, 32\}. \tag{3.79}$$

Switching waveforms of the switches $Q_1$and Q_3 and input current ripple are shown for $N_{pdm} = 20$ and $N_{pdm} = 12$ in Fig. 3.19 and Fig. 3.20, respectively. As can be seen the

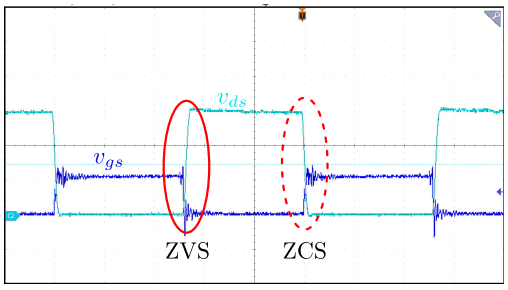
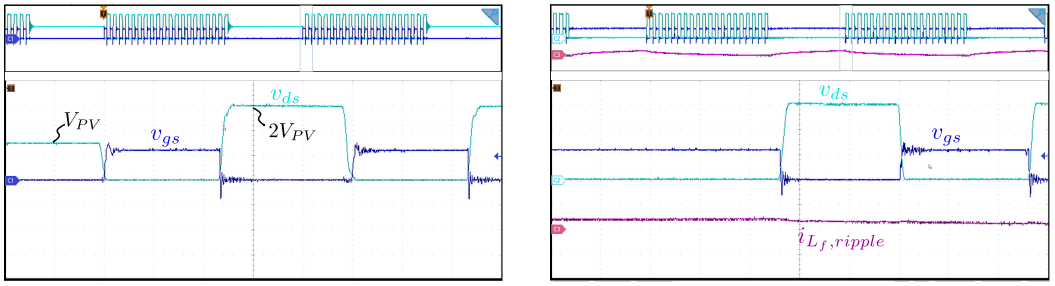
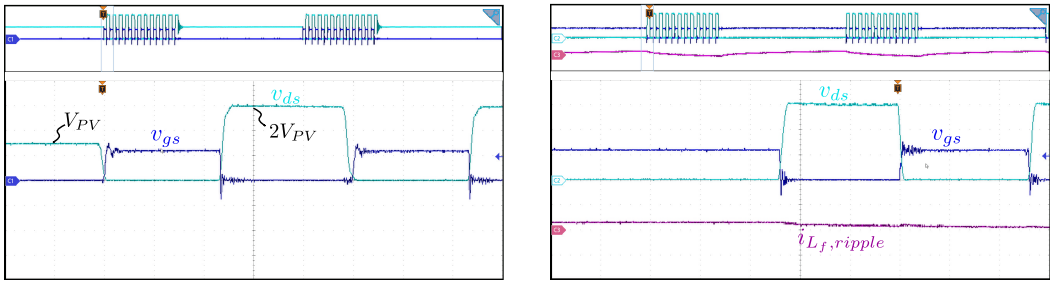


Fig. 3.18: ZCS turn ON and ZVS turn OFF switching waveforms of the Q_3 (v_{gs} blue with $5V/div$ and v_{ds} cyan with $10V/div$).



(a) (b)

Fig. 3.19: (a) Q_1 switching waveforms and (b) Q_3 switching waveforms and input current ripple when operating with $N_{pdm} = 20$.



(a) (b)

Fig. 3.20: (a) Q_1 switching waveforms and (b) Q_3 switching waveforms and input current ripple when operating with $N_{pdm} = 12$.

soft-switching operation of the switches is preserved under PDM operation and input current ripple is negligible. Also, it can be seen that the voltage across Q_1 drops to V_{PV} when both Q_1 and Q_2 are OFF while it is switched between zero and $2V_{PV}$ during the process mode. As amplitude of the positive voltage across Q_1 does not change during the PDM cycle it can be concluded that the voltage ripple is negligible.

MIC efficiency for various power mismatch levels is also measured for the prototyped setup. In this test, PV rated power generation is assumed to be 220 W. To measure

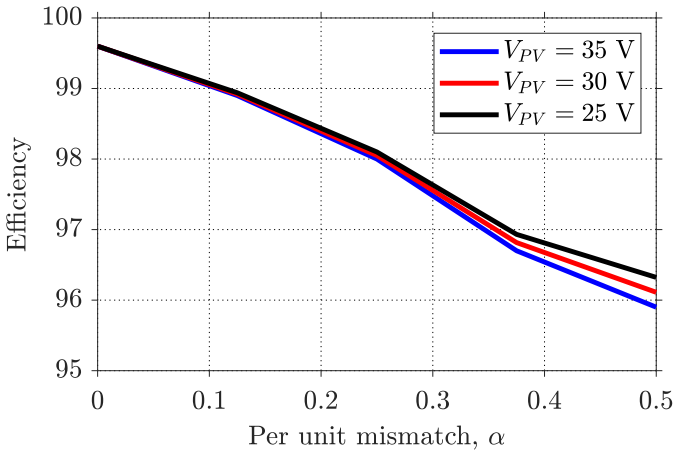


Fig. 3.21: Efficiency of the proposed MIC versus per unit power mismatch on the PV module for various PV module voltages.

the efficiency the string current is maintained at the rated current and per unit power mismatch has been swept between 0 and 50%. The test has been repeated for three PV voltage levels of 25 V, 30 V, and 35 V, and the results are shown in Fig. 3.21. As can be seen, the efficiency is greater than or equal to 96% for all operating conditions and the slope of efficiency reduction with power mismatch is consistent for the whole range. The above observation can be more appreciated if it is compared to the regular PWM dc-dc MICs where efficiencies are normally below 95% and there is a huge step in efficiency when MIC is operated slightly away from zero power mismatch.

Chapter 4

Analysis and design optimization of PV Module Integrated Converter

In this chapter, the proposed PV MIC has been analyzed and its design equations are obtained and optimized. First, a novel model of center-tapped transformer is proposed which takes into account all the parasitic inductance of the conventional model however renders smaller number of inductance in the model. Second, LBSM is used to obtain a steady state model for the converter that has both high frequency effects and PDM effects. The obtained model is analyzed using LBSM to obtain converter waveforms and its design equations in closed form which are then used to obtain optimal operating conditions for the MIC.

4.1 New Model for Center-tapped Transformer

Magnetic components can be presented in different ways among which mathematical and physical circuit representations are two sides of the spectrum. The mathematical representation ensures that every and each coupling between windings of a magnetic structure are considered however it may not have direct physical equivalent inductances in the real world. On the other hand, the physical circuit representation gives physical

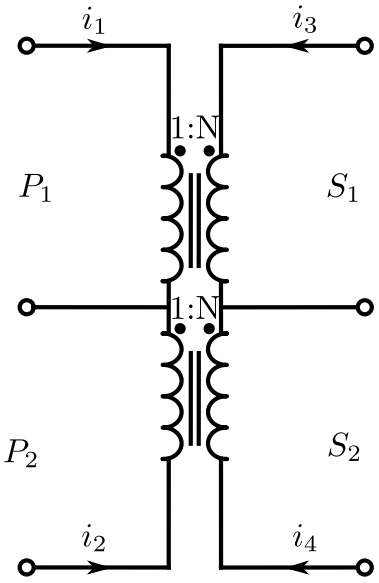


Fig. 4.1: Center-tapped transformer commonly used in power converters.

insight about different couplings of the magnetic component in terms of real world inductance values. For example the T-model of a two winding transformer fully represents all the couplings in the magnetic component and also represents the model by means of physically meaningful inductances. Though, the physical circuit representation is not always attainable for the magnetic components specially with the increased number of windings.

According to mathematical representation, a magnetic component with m winding can be presented using a m by m matrix. As this matrix is symmetrical with respect to its diagonal, the number of independent parameters that is necessary and sufficient for mathematical representation can be obtained as:

$$\text{Necessary and sufficient number of parameters} = \frac{m(m+1)}{2}. \tag{4.1}$$

4.1.1 Extended Cantilever Model of 4 winding Transformer

A common magnetic component that is used in power converters is a center-tapped transformer which is shown in Fig. 4.1. As can be seen, this transformer has 4 windings and according to (4.1) 10 parameters are required to fully model this transformer. Conventionally, extended cantilever models are used for the multi-winding transformer

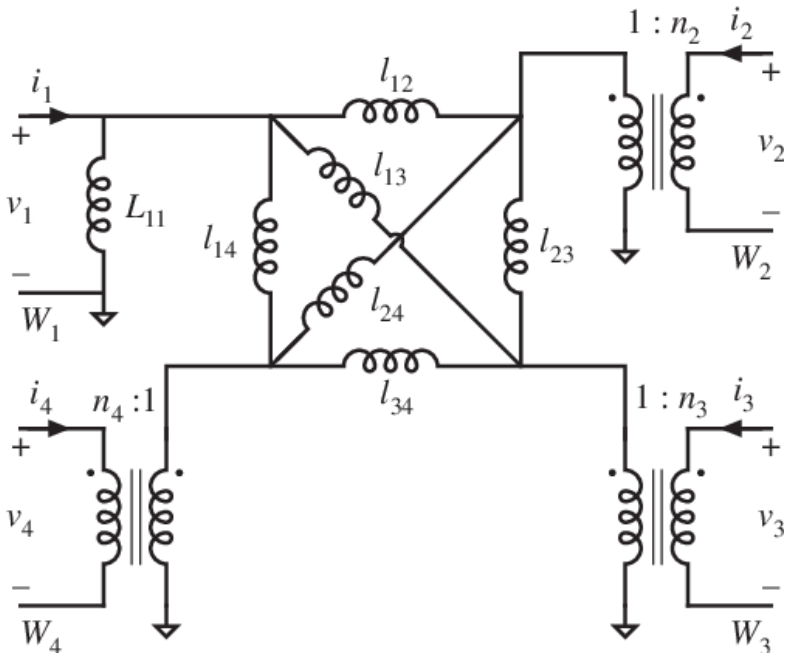


Fig. 4.2: Extended cantilever model of a 4 winding transformer [57].

presentation, where the 10 parameters are as shown in the Fig. 4.2. As can be seen, the parameters are some non-physical turns ratio and inductances.

4.1.2 Proposed Model for a Center-tapped 4 winding Transformer

The extended cantilever model of the 4 winding transformer presented above can be used to model the center-tapped transformer shown in Fig. 4.1. However, it is beneficial to derive the model of the transformer in a format that gives more physical insight compared to the conventional extended cantilever representation. Also, assuming that the center-tapped transformer has symmetrical magnetic implementation, it does not have 4 fully independent ports like a general 4 winding transformer, thus the center-tapped transformer model can be simplified. According to Fig. 4.1, the number of turns is equal for P_1 and P_2 and same number of turns is used for S_1 and S_2. Assume that these windings are also physically symmetrical in the magnetic implementation of the transformer which most likely would be the case for a properly designed planar transformer. This renders a few constraints compared to a general 4 winding transformer which in turn simplifies the model and reduces number of independent parameters. For example by exciting windings under the condition that no current goes through the midpoints (junction between P_1 and P_2 or between S_1 and S_2) two constraints can be formed:

$$\text{If } \{i_1 = -i_2 \,\&\, v_3 = -v_4\}, \text{ then } i_3 = -i_4. \tag{4.2}$$

$$\text{If } \{i_3 = -i_4 \,\&\, v_1 = -v_2\}, \text{ then } i_1 = -i_2. \tag{4.3}$$

Now, consider the case where the current going through midpoints equally distributes between the two windings which results in following two constraints:

$$\text{If } \{i_1 = i_2 \,\&\, v_3 = v_4\}, \text{ then } i_3 = i_4. \tag{4.4}$$

$$\text{If } \{i_3 = i_4 \,\&\, v_1 = v_2\}, \text{ then } i_1 = i_2. \tag{4.5}$$

The above constraints are not necessarily holding true for a general 4 winding transformer model shown in Fig. 4.2 and these four equations reduce the number of necessary and sufficient parameters for a center-tapped 4 winding transformer into 6 parameters.

According to above discussion a 6 parameter model is proposed for the center-tapped 4-winding transformer. The proposed model is shown in Fig. 4.3 which satisfies all the constraints given for center-tapped 4 winding transformer. As it can be seen from constraints, the behavior of the center-tapped transformer can be better understood if the port currents/voltages are considered to be composed of two separate portions of differential and common mode. The new proposed model utilizes the above constraints and describes the transformer model using two circuits in parallel. One circuit shows the differential mode and the other circuit represents the common mode. Now, each of the differential and common mode circuits can be represented by 3 parameters only which is equal to number of necessary and sufficient parameters for a two winding transformer. As the T-model of the two winding transformer provides the most physical insight into circuit elements, the T-model equivalent of transformer is used to represent the differential and common mode circuits. The differential and common mode voltage

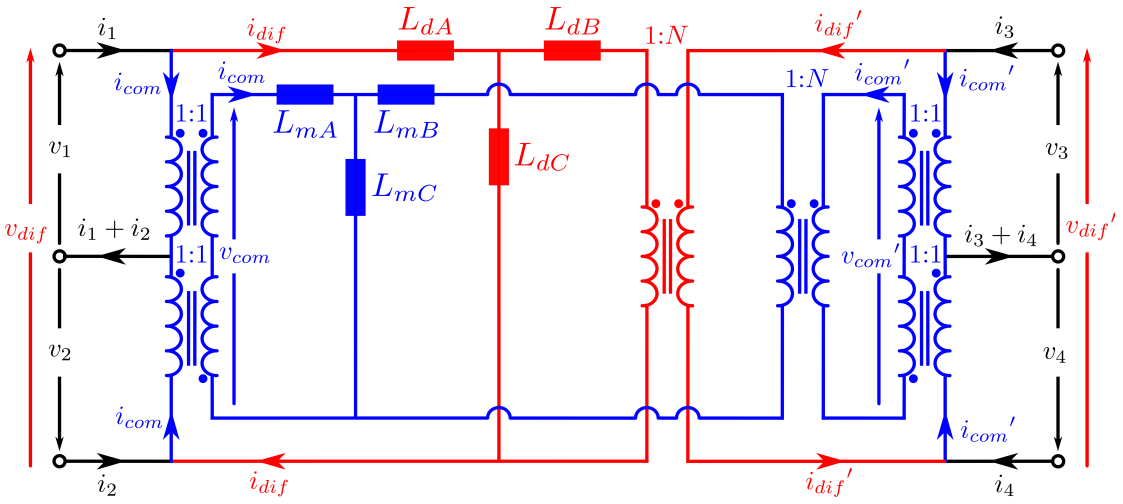


Fig. 4.3: The proposed model for the 4-winding center-tapped transformer based on equivalent differential mode and common mode circuits.

and current of the proposed model are related to winding voltages and currents as below:

$$i_{dif} = \frac{i_1 - i_2}{2}, \tag{4.6}$$

$$i_{com} = \frac{i_1 + i_2}{2}, \tag{4.7}$$

$$i'_{dif} = \frac{i_3 - i_4}{2}, \tag{4.8}$$

$$i'_{com} = \frac{i_3 + i_4}{2}. \tag{4.9}$$

$$v_{dif} = v_1 - v_2, \tag{4.10}$$

$$v_{com} = v_1 + v_2, \tag{4.11}$$

$$v'_{dif} = v_3 - v_4, \tag{4.12}$$

$$v'_{com} = v_3 + v_4. \tag{4.13}$$

4.1.3 Analysis of Parasitic Inductances of the MIC using New Transformer Model

Now, the proposed transformer model can be used to analyze the behavior of the Module Integrated Converter (MIC) proposed in last chapter. In specific, using the transformer model the leakage inductance between different windings can be found. For example

assume that only one of the windings is excited and the rest are open circuit:

$$v_3 = v_s, i_1 = i_2 = i_4 = 0. \tag{4.14}$$

According to the proposed model:

$$i'_{dif} = i'_{com} = \frac{i_3}{2} \tag{4.15}$$

$$i_{dif} = i_{com} = 0 \tag{4.16}$$

Where, i'_{dif} and i'_{com} are the differential and common mode currents on the secondary which are caused by the secondary excitation.

$$i'_{dif} = \frac{v'_{dif}}{N^2(L_{dB} + L_{dC})} \tag{4.17}$$

$$i'_{com} = \frac{v'_{com}}{N^2(L_{mB} + L_{mC})}. \tag{4.18}$$

Using (4.17) and (4.15) results in:

$$\frac{v'_{dif}}{L_{dB} + L_{dC}} = \frac{v'_{com}}{L_{mB} + L_{mC}}. \tag{4.19}$$

Now, using (4.10), the winding voltages can be obtained as:

$$v_3 = \frac{v'_{dif} + v'_{com}}{2} = \left(1 + \frac{L_{dB} + L_{dC}}{L_{mB} + L_{mC}}\right) \frac{v'_{com}}{2}, \tag{4.20}$$

$$v_4 = \frac{v'_{com} - v'_{dif}}{2} = \left(1 - \frac{L_{dB} + L_{dC}}{L_{mB} + L_{mC}}\right) \frac{v'_{com}}{2}. \tag{4.21}$$

which results in:

$$\frac{v_4}{v_3} = \frac{(L_{mB} + L_{mC}) - (L_{dB} + L_{dC})}{(L_{mB} + L_{mC}) + (L_{dB} + L_{dC})}. \tag{4.22}$$

$$\left|\frac{v_4}{v_3}\right| = \frac{(L_{dB} + L_{dC}) - (L_{mB} + L_{mC})}{(L_{mB} + L_{mC}) + (L_{dB} + L_{dC})}. \tag{4.23}$$

Therefore, if winding 3 and 4 of the magnetic structure is considered only, the leakage inductance between them and their magnetizing inductance can be denoted by $L_{lkg} = 2(L_{mB} + L_{mC})$ and $L_{mag} = (L_{dB} + L_{dC}) - (L_{mB} + L_{mC})$, respectively.

The primary side leakage inductances with respect to secondary side can also be obtained using similar approach. The voltage across the differential and common mode circuits

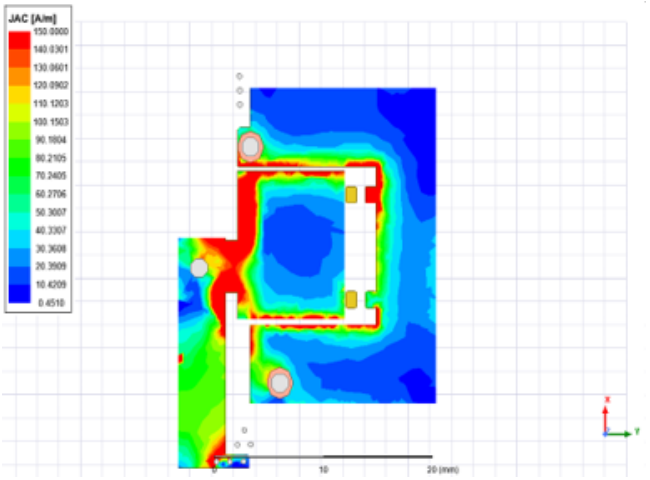


Fig. 4.4: Simulation of the stray inductance caused by PCB connections between secondary windings in Ansys Maxwell.

in primary side are as:

$$v_{dif} = \frac{L_{dC}}{L_{dC} + L_{dB}} \frac{v'_{dif}}{N}, \tag{4.24}$$

$$v_{com} = \frac{L_{mC}}{L_{mC} + L_{mB}} \frac{v'_{com}}{N}, \tag{4.25}$$

Now, leveraging (4.19) the winding voltages can be obtained as:

$$v_1 = \frac{v_{dif} + v_{com}}{2} = \left(\frac{L_{mC} + L_{dC}}{L_{mC} + L_{mB}}\right) \frac{v'_{com}}{2N}, \tag{4.26}$$

$$v_2 = \frac{v_{com} - v_{dif}}{2} = \left(\frac{L_{mC} - L_{dC}}{L_{mC} + L_{mB}}\right) \frac{v'_{com}}{2N}, \tag{4.27}$$

which results in:

$$\frac{v_1}{v_3} = \frac{1}{N} \frac{L_{mC} + L_{dC}}{(L_{mB} + L_{mC}) + (L_{dB} + L_{dC})}, \tag{4.28}$$

$$\frac{v_2}{v_3} = \frac{1}{N} \frac{L_{mC} - L_{dC}}{(L_{mB} + L_{mC}) + (L_{dB} + L_{dC})}. \tag{4.29}$$

According to the above discussion, useful insights can be provided into MIC design. The leakage inductance between secondary windings is a crucial parameter in the MIC operation. As discussed in the previous chapter, during MIC operation in Process mode the secondary side FETs switch under ZVS. During ZVS transition both secondary side FETs are OFF and the charges transfer from the C_{oss} of one FET to another through the secondary windings of the transformer. If the transformer is ideal the common mode voltage during the ZVS transition would be constant and C_{oss} capacitors will be charged up to the dc value that is externally applied to the midpoint of the secondary windings.

However, if the actual magnetic model is considered, the common mode voltage of the transformer will contain a resonant osculation between the C_{oss} and secondary leakage inductance, i.e., $2(L_{mB} + L_{mC})$. This resonance oscillation causes a voltage ringing across secondary FETs which reduces the converter efficiency and may also lead to over-voltage on the FETs and permanent damage to the converter. The insight that new model provides in this regard is that, as shown in $L_{lkg} = 2(L_{mB} + L_{mC})$, the leakage inductance between the windings of the secondary is just a function of common mode circuit parameters. In fact, if the common mode only is excited in the secondary side and the primary side of the common mode circuit is left open circuit the inductance seen is the leakage inductance. This test can be easily designed and carried out in Finite Element Analysis tools to optimize the amount of leakage inductance and consequently the ringing voltage across secondary FETs. For the MIC design at 1 MHz the above test is carried out in Ansys Maxwell software with the full model of the planar transformer and PCB connections. The results show that not only the winding structure of the planar transformer is vital to reduce the leakage inductance but also the stray inductance caused due to PCB connection between windings heavily affects the overall leakage inductance of secondary side. Figure 4.4 shows the simulations from Maxwell for the stray inductance effect on the leakage inductance. As can be seen larger path for the common mode current can lead to larger loop size and increased stray inductance. Therefore, in the PCB design the component placement are optimized to make the stray inductance as small as possible. Also, based on simulations it has been observed that if the layers used to implement the high side and low side secondary windings are interleaved the lowest leakage inductance is obtained. So the PCB layers used for the secondary winding are arranged as S_1, S_2, S_1, S_2 from top layer to bottom layer.

4.1.4 Analysis of Process Mode using Proposed Transformer Model

In general the transformer model given in Fig. 4.3 is a 6th order system which in combination with the power converter system can increase the order of power converter system into a degree that no physical insight can be provided into the analyzed results. As can be seen from differential circuit of the proposed model, L_{dC} is the magnetization inductance of the transformer which is considerably larger than the leakage inductances L_{dA} and L_{dB}. Furthermore, the common mode inductances as shown earlier are normally minimized using interleaving and stray inductance reduction so that the values of

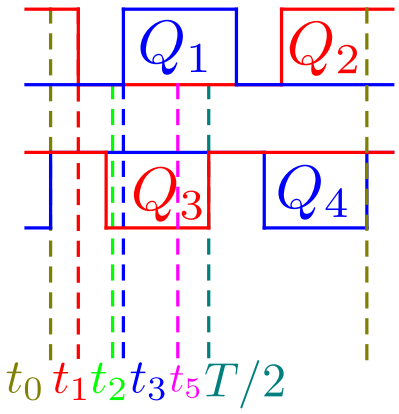


Fig. 4.5: Different intervals of the MIC in Process mode within a half-cycle.

L_{mA}, L_{mB} and L_{mC} are also relatively small compared to L_{dC}. Therefore, it is assumed that $L_{dC} = \infty$ which simplifies the differential circuit into a single leakage inductance $L_{lkg} = L_{dA} + L_{dB}$. Also, according to (4.22), if $L_{dC} = \infty$, then $v_4/v_3 = -1$ which leads to $v'_{com} = 0$ regardless of excitation on the transformer. Due to the symmetry the same relationship can be found between v_1 and v_2 which leads to $v_{com} = 0$ regardless of excitation on the transformer. Therefore, if $L_{dC} = \infty$ then the common mode portion of the model will be always short circuit. It is important to note that having zero Volts on the terminals of common mode circuit does not imply that common mode current is also zero, but it implies that common mode current can take any value. Also, both the differential and common mode current/voltage contribute to the winding currents/voltages of the transformer.

Now, the proposed model with the above assumptions is utilized to derive the MIC waveforms during Process mode. Due to the half-wave symmetry of inputs, only half switching cycle of the converter operation is sufficient to obtain the waveforms. These assumptions are made to make the analysis simpler: 1. In Transformer model $L_{dC} = \infty$, 2. MOSFETs are ideal switches in parallel with C_{oss} 3. MOSFET body diodes are ideal diodes 4. External diodes are ideal diodes in series with a forward voltage drop. From the converter analysis perspective some of the intervals discussed in previous chapter for Process mode can be combined together and the resultant half cycle will be divided into 5 separate intervals. These 5 intervals are shown in Fig. 4.5 and conducting devices in each interval are given in Table 4.1. The converter circuit and its equivalent model using proposed transformer model is shown in the section allocated to that interval's description.

TABLE 4.1: Conducting devices during the intervals of process mode.

Switching interval	PV side	String side	Clamping diodes
$S_0 : t_0 < t < t_1$	Q_2	Q_3 & Q_4	none
$S_1 : t_1 < t < t_2$	none	Q_3 & Q_4	none
$S_2 : t_2 < t < t_3$	none	Q_4	none
$S_3 : t_3 < t < t_4$	Q_1	Q_4	none
$S_4 : t_4 < t < t_5$	Q_1	Q_4	D_1
$S_5 : t_5 < t < T/2$	Q_1	Q_4	none

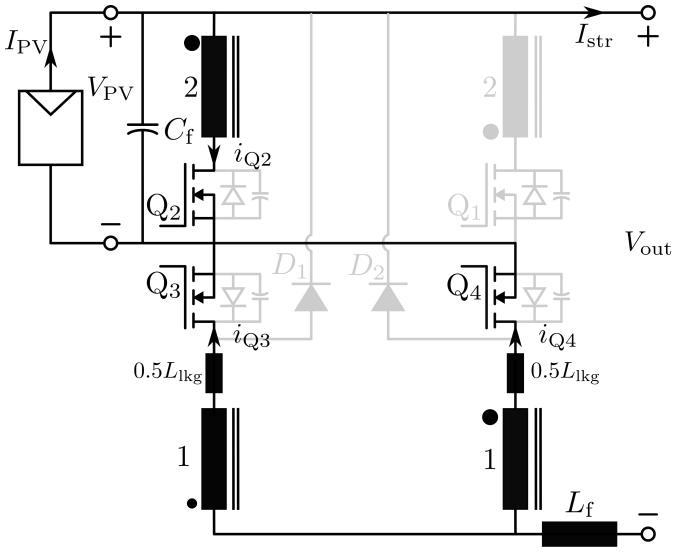


Fig. 4.6: MIC equivalent circuit during switching interval $S_0 : t_0 < t < t_1$ of the Process mode.

According to the new transformer model and assuming $L_{dC} = \infty$ the common mode portion of the transformer model will be short circuit all the time. The differential portion of the circuit however is loaded by the parallel combination of common mode circuit and external differential circuit that is composed at the differential ports of the transformer at each switching interval. Using the MIC circuit in each interval and utilizing the transformer model, converter operation in Process mode is analyzed in the following sections.

Interval S_0 $(t_0 < t < t_1)$**:** This interval begins with the turn ON of Q_4 and prior to this interval only Q_2 and Q_3 were conducting leading to the initial conditions of this

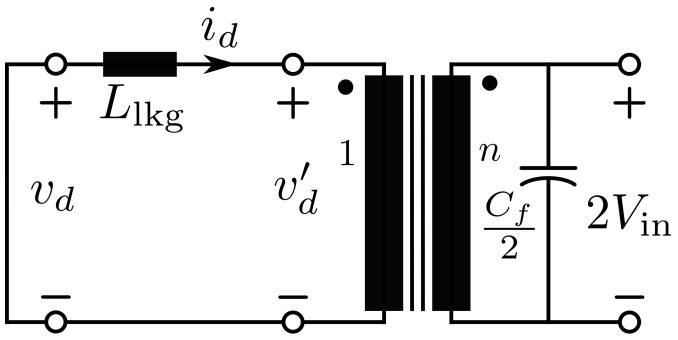


Fig. 4.7: Transformer model loaded with MIC circuit during switching interval S_0 $(t_0 < t < t_1)$ of the Process mode.

interval as below:

$$i_{Q1} = 0, \tag{4.30}$$

$$i_{Q2} = -0.5I_{str}, \tag{4.31}$$

$$i_{Q3} = I_{str}, \tag{4.32}$$

$$i_{Q4} = 0. \tag{4.33}$$

Converter circuit in this interval is shown in the Fig, 4.6 and its equivalent differential mode circuit with transformer model is shown in Fig. 4.7. Since both Q_3 and Q_4 are conducting in this interval, the primary side of the differential circuit is short circuit and thus is not affected by any further loading from common mode circuit. As Q_2 is on in PV side of the transformer PV side winding is directly connected to the capacitive filter. It is important to note that the differential mode voltage is the voltage across both of the PV side windings which is two times the capacitive filter voltage. According, to above circuit the converter waveforms in this interval can be obtained as below:

$$v_d = 0 \tag{4.34}$$

$$\text{Assuming } n = 2, \text{ then } v'_d = V_{\text{in}} \tag{4.35}$$

$$i_d = \frac{i_{Q3} - i_{Q4}}{2} \tag{4.36}$$

$$i_d(t_0) = 0.5I_{\text{str}} \tag{4.37}$$

$$i_d = 0.5I_{\text{str}} - \frac{V_{\text{in}}}{L}(t - t_0) \tag{4.38}$$

$$t_1 = t_0 + \frac{D - 0.5}{2}T \tag{4.39}$$

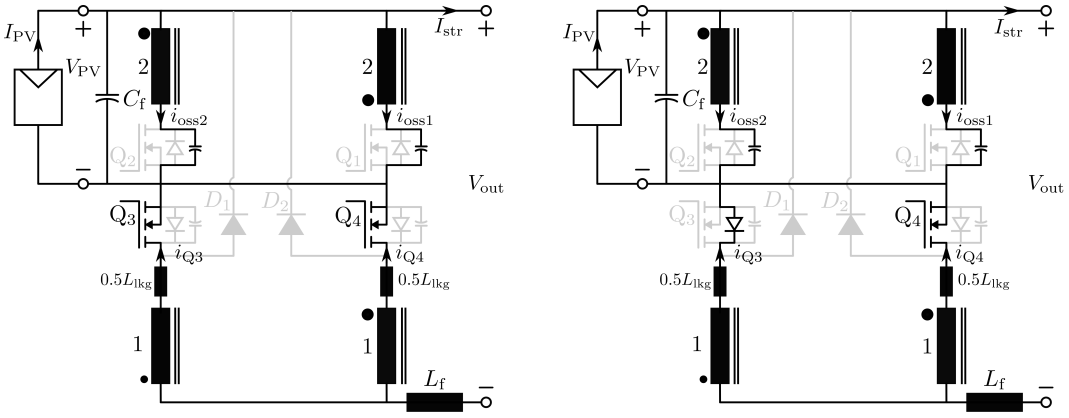


Fig. 4.8: MIC equivalent circuits during switching interval S_1 ($t_1 < t < t_2$) of the Process mode.

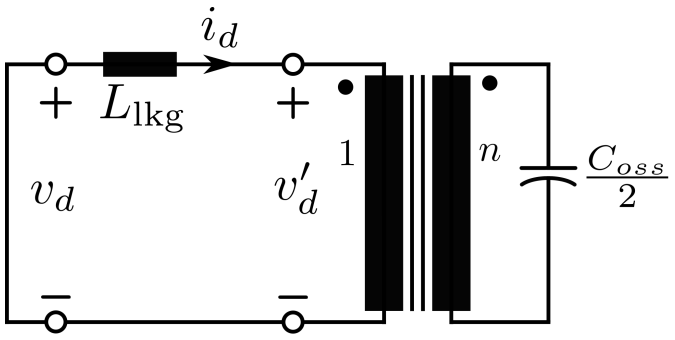


Fig. 4.9: Transformer model loaded with MIC circuit during switching interval S_1 ($t_1 < t < t_2$) of the Process mode.

$$I_1 = i_d(t = t_1) = 0.5I_{\text{str}} - \frac{V_{\text{in}}}{L}\frac{D - 0.5}{2}T \tag{4.40}$$

Interval S_1 ($t_1 < t < t_2$): At the beginning of this interval PV side switch (Q_2) stops conducting, thus only the switch capacitances (C_{oss}) appear on the PV side. From differential circuit point of view the capacitors are in series with each other and they are also in series with the differential circuit inductance thus form a resonant circuit. On the string side, both of the FETs are ON until the overlap time between them is elapsed. After overlap time, the gate signal of the Q_3 is disabled however, the body diode of Q_3 keeps conducting the resonant current until the current hits zero cross at the end of this interval ($t = t_2$). The converter circuit and its differential mode using the transformer model is shown in Fig. 4.8 and Fig. 4.9, respectively. According to above circuit, the converter waveforms in this interval can be obtained as below:

$$v_d = 0 \tag{4.41}$$

$$v'_d = C' \left(\frac{dv'_d}{dt} \right) \tag{4.42}$$

$$C' = \frac{n^2 C_{oss}}{2} \tag{4.43}$$

$$\text{Assuming } n = 2, \text{ then } C' = 2C_{oss} \tag{4.44}$$

$$v'_d(t_1) = V_{in} \tag{4.45}$$

$$i_d(t_1) = I_1 \tag{4.46}$$

$$v'_d = -V_{m,1} \sin\left(\omega_1(t - t_1) + \tan^{-1}\left(\frac{V_{in}}{Z_1 I_1}\right)\right) \tag{4.47}$$

$$i_d = -I_{m,1} \cos\left(\omega_1(t - t_1) + \tan^{-1}\left(\frac{V_{in}}{Z_1 I_1}\right)\right) \tag{4.48}$$

$$V_{m,1} = \sqrt{(Z_1 I_1)^2 + V_{in}^2} \tag{4.49}$$

$$I_{m,1} = \sqrt{\left(\frac{V_{in}}{Z_1}\right)^2 + I_1^2} \tag{4.50}$$

$$\omega_1 = \frac{1}{\sqrt{LC_1}}, \quad Z_1 = \sqrt{\frac{L}{C_1}} \tag{4.51}$$

$$C_1 = C' \tag{4.52}$$

$$t_2 = t_1 + \left(\cos^{-1}\left(\frac{0.5 I_{str}}{I_{m,1}}\right) - \tan^{-1}\left(\frac{V_{in}}{Z_1 I_1}\right)\right) / \omega_1 \tag{4.53}$$

$$V_2 = -V_{m,1} \sin\left(\omega_1(t_2 - t_1) + \tan^{-1}\left(\frac{V_{in}}{Z_1 I_1}\right)\right) \tag{4.54}$$

$$I_2 = -I_{m,1} \cos\left(\omega_1(t_2 - t_1) + \tan^{-1}\left(\frac{V_{in}}{Z_1 I_1}\right)\right) \tag{4.55}$$

Interval S_2 ($t_2 < t < t_3$): This interval begins at switch Q_2's current zero cross point where the body diode stops conducting. Therefore, C_{oss} of Q_2 appears across the differential circuit and this in turn allows for the loading effects from common mode circuit. The common mode circuit is still short circuit and its current is equal to half of the current going through the transformer mid point:

$$i_{com} = \frac{i_{Q3} + i_{Q4}}{2} = 0.5 I_{str}. \tag{4.56}$$

According to the proposed model of the transformer, the common mode circuit is in parallel with the differential mode circuit, thus a constant current source representing the common mode is added in parallel to differential circuit model of the MIC in this interval. This interval has two possible end points: First the PV side FET's C_{oss} is

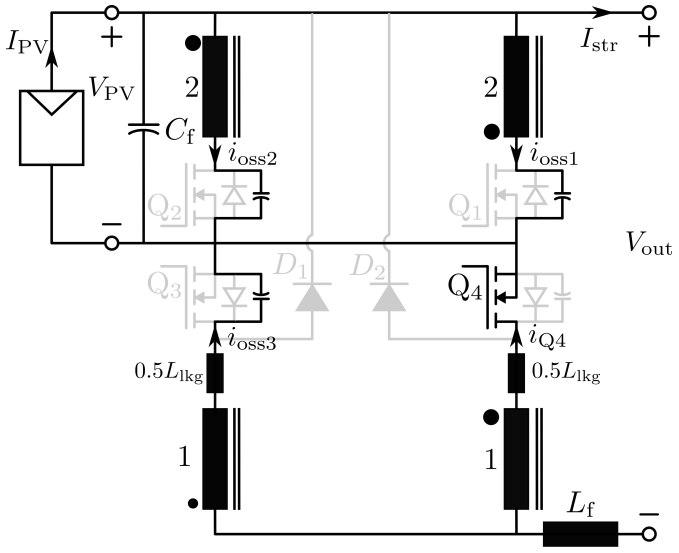


Fig. 4.10: MIC equivalent circuit during switching interval S_2 : $t_2 < t < t_3$ of the Process mode.

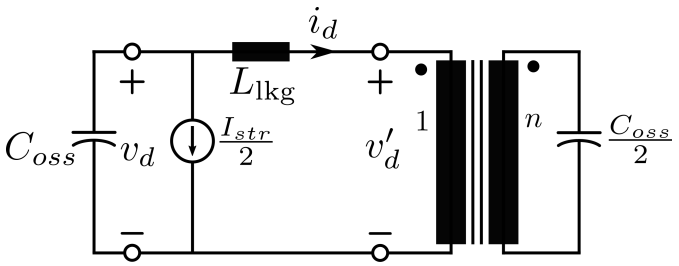


Fig. 4.11: Transformer model loaded with MIC circuit during switching interval S_2 ($t_2 < t < t_3$) of the Process mode.

charged/discharged sufficiently so that the body diode of the FET starts conducting. Second, the C_{oss} of Q_3 in string side is charged up to input voltage level so that the clamp diode D_1 starts conducting. Usually, the first case occurs in high frequency low voltage applications because of the relatively small ratio of L_{lkg} to C_{oss}. The converter circuit and its differential mode using the transformer model is shown in Fig. 4.10 and Fig. 4.11, respectively. According to above circuit, the converter waveforms in this interval can be obtained as below:

$$v_d = C\frac{dv_d}{dt} \tag{4.57}$$

$$v'_d = C'\frac{dv'_d}{dt} \tag{4.58}$$

$$v_d(t_2) = 0 \tag{4.59}$$

$$v'_d(t_2) = V_2 \tag{4.60}$$

$$i_d(t_2) = I_2 \tag{4.61}$$

$$v_d = v_{d-ZSR} + v_{d-ZIR} \tag{4.62}$$

$$v'_d = v'_{d-ZSR} + v'_{d-ZIR} \tag{4.63}$$

$$i_d = i_{d-ZSR} + i_{d-ZIR} \tag{4.64}$$

$$v_{d-ZSR} = -\frac{0.5I_{str}}{C+C'}\left(\omega_2(t-t_2) + \frac{C'}{C}\sin(\omega_2(t-t_2))\right)/\omega_2 \tag{4.65}$$

$$v'_{d-ZSR} = -\frac{0.5I_{str}}{C+C'}\left(\omega_2(t-t_2) - \sin(\omega_2(t-t_2))\right)/\omega_2 \tag{4.66}$$

$$i_{d-ZSR} = -\frac{C'}{C+C'}\frac{0.5I_{str}}{1-\cos(\omega_2(t-t_2))} \tag{4.67}$$

$$v_{d-ZIR} = -\frac{C'}{C+C'}(v_{ZIR} - V_2) \tag{4.68}$$

$$v'_{d-ZIR} = \frac{C}{C+C'}(v_{ZIR} - V_2) + \frac{C'}{C+C'}V_2 = \frac{C}{C+C'}v_{ZIR} - \frac{C'}{C+C'}V_2 \tag{4.69}$$

$$v_{ZIR} = -V_{m,2}\sin(\omega_2(t-t_2) + \tan^{-1}\left(\frac{V_2}{Z_2I_2}\right)) \tag{4.70}$$

$$i_{d-ZIR} = -I_{m,2}\cos(\omega_1(t-t_2) + \tan^{-1}\left(\frac{V_2}{Z_2I_2}\right)) \tag{4.71}$$

$$V_{m,2} = \sqrt{(Z_2I_2)^2 + V_2^2} \tag{4.72}$$

$$I_{m,2} = \sqrt{\left(\frac{V_2}{Z_2}\right)^2 + I_2^2} \tag{4.73}$$

$$\omega_2 = \frac{1}{\sqrt{LC_2}}, \quad Z_2 = \sqrt{\frac{L}{C_2}} \tag{4.74}$$

$$C_2 = \frac{CC'}{C+C'} \tag{4.75}$$

$$C = C_{oss} \tag{4.76}$$

$$C' = 2C_{oss} \tag{4.77}$$

To obtain the end point of the interval following equation should be solved numerically to find t_3.

$$v'_d(t_3) = -V_{in} \tag{4.78}$$

Having t_3 obtained the states of converter at the end of this interval are as below:

$$v'(t_3) = -V_{in} \tag{4.79}$$

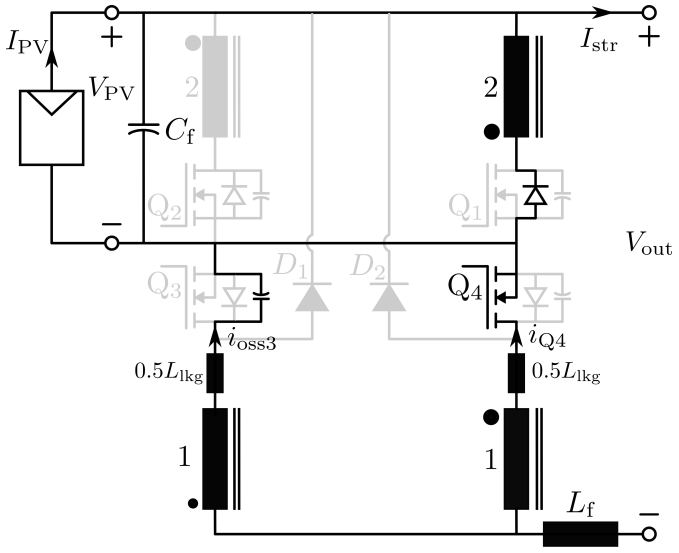


Fig. 4.12: MIC equivalent circuit during switching interval S_3 : $t_3 < t < t_4$ of the Process mode.

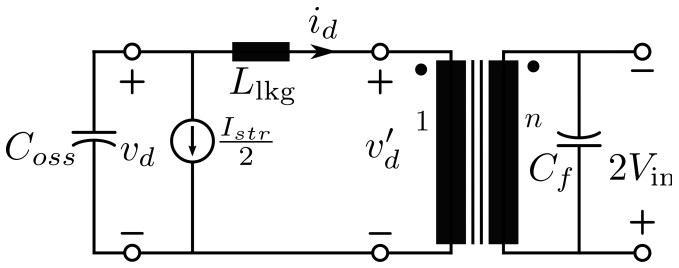


Fig. 4.13: Transformer model loaded with MIC circuit during switching interval S_3 ($t_3 < t < t_4$) of the Process mode.

$$i_d(t_3) = I_3 \tag{4.80}$$

$$v_d(t_3) = V_3 \tag{4.81}$$

Interval S_3 **(**$t_3 < t < t_4$**):** At the beginning of this interval, body diode of the Q_1 starts conducting and directly connects the input voltage to the PV side winding. In the string side, the C_{oss} of Q_3 is still across the differential circuit with its associated loading from common mode circuit. This interval ends at t_4 when the voltage across C_{oss} of Q_3 reaches V_{in}.The converter circuit and its differential mode using the transformer model is shown in Fig. 4.12 and Fig. 4.13, respectively. According to above circuit, the converter waveforms in this interval can be obtained as below:

$$v_d = C\frac{dv_d}{dt} \tag{4.82}$$

$$v'_d = -V_{in} \tag{4.83}$$

$$v_d(t_2) = V_3 \tag{4.84}$$

$$i_d(t_2) = I_3 \tag{4.85}$$

$$v_d = v_{d-ZSR1} + v_{d-ZSR2} + v_{d-ZIR} \tag{4.86}$$

$$i_d = i_{d-ZSR1} + i_{d-ZSR2} + i_{d-ZIR} \tag{4.87}$$

$$v_{d-ZIR} = V_{m,3}\sin(\omega_3(t-t_3) - \tan^{-1}\left(\frac{V_3}{Z_3 I_3}\right)) \tag{4.88}$$

$$i_{d-ZIR} = -I_{m,3}\cos(\omega_3(t-t_3) - \tan^{-1}\left(\frac{V_3}{Z_3 I_3}\right)) \tag{4.89}$$

$$V_{m,3} = \sqrt{(Z_3 I_3)^2 + V_3^2} \tag{4.90}$$

$$I_{m,3} = \sqrt{\left(\frac{V_3}{Z_3}\right)^2 + I_3^2} \tag{4.91}$$

$$v_{d-ZSR1} = -\frac{Z_3 I_{str}}{2}\sin(\omega_3(t-t_3)) \tag{4.92}$$

$$i_{d-ZSR1} = -\frac{I_{str}}{2}(1-\cos(\omega_3(t-t_3))) \tag{4.93}$$

$$v_{d-ZSR2} = -V_{in}(1-\cos(\omega_3(t-t_3))) \tag{4.94}$$

$$i_{d-ZSR2} = \frac{V_{in}}{Z_3}\sin(\omega_3(t-t_3)) \tag{4.95}$$

$$\omega_3 = \frac{1}{\sqrt{LC_3}}, \quad Z_3 = \sqrt{\frac{L}{C_3}} \tag{4.96}$$

$$C_3 = C = C_{oss} \tag{4.97}$$

To find the end point of the interval t_4, the following equation should be solved numerically.

$$v_d(t_4) = -V_{in} \tag{4.98}$$

Interval S_4 ($t_4 < t < t_5$): At the beginning this interval, the voltage across Q_3 reaches the input voltage V_{in} and causes clamp diode D_1 to start conducting. The forward voltage drop of the clamp diode V_f reduces the current originally commuted into diode during the interval. The PV side winding is connected to input voltage during this interval either through Q_1 or its body diode. This interval ends at t_5 where the current through the clamp diode reaches 0. The converter circuit and its differential mode using the transformer model is shown in Fig. 4.14 and Fig. 4.15, respectively. According to

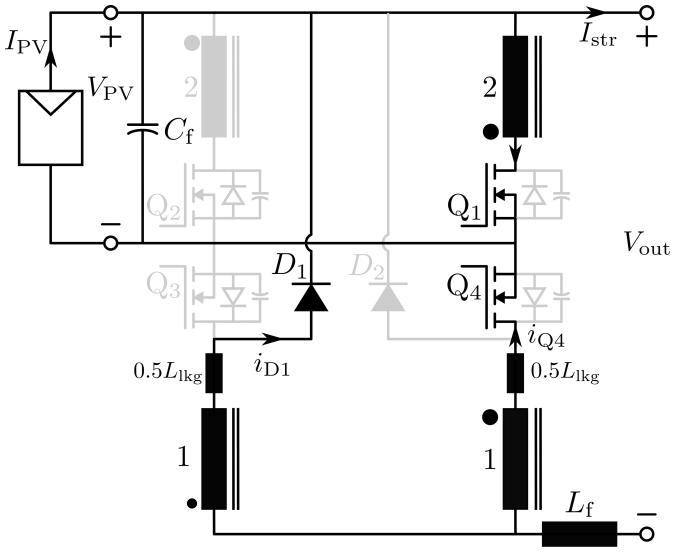


Fig. 4.14: MIC equivalent circuit during switching interval S_4 : $t_4 < t < t_5$ of the Process mode.

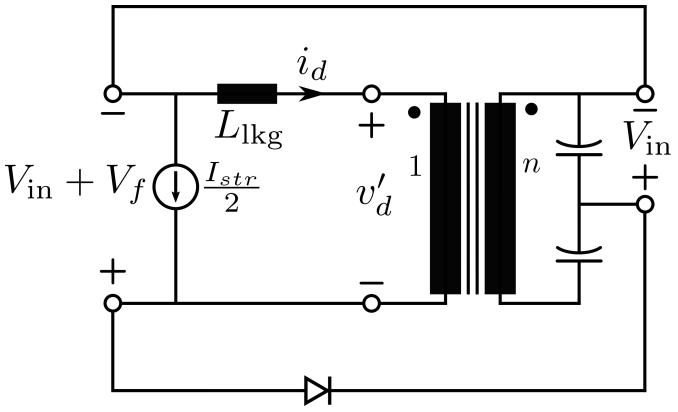


Fig. 4.15: Transformer model loaded with MIC circuit during switching interval S_4 ($t_4 < t < t_5$) of the Process mode.

above circuit, the converter waveforms in this interval can be obtained as below:

$$i_{D1}(t_4) = \frac{I_{str}}{2} + i_d(t_4) \tag{4.99}$$

$$i_d = i_d(t_4) - \frac{V_f}{L}(t - t_4) \tag{4.100}$$

$$i_{D1} = i_{D1}(t_4) - \frac{V_f}{L}(t - t_4) \tag{4.101}$$

$$t_5 : i_{D1}(t_5) = 0 \tag{4.102}$$

$$t_5 = t_4 + \frac{L}{V_f} i_{D1}(t_4) \tag{4.103}$$

Interval S_5 ($t_5 < t < T/2$): In this interval, the clamp diode current has reached zero

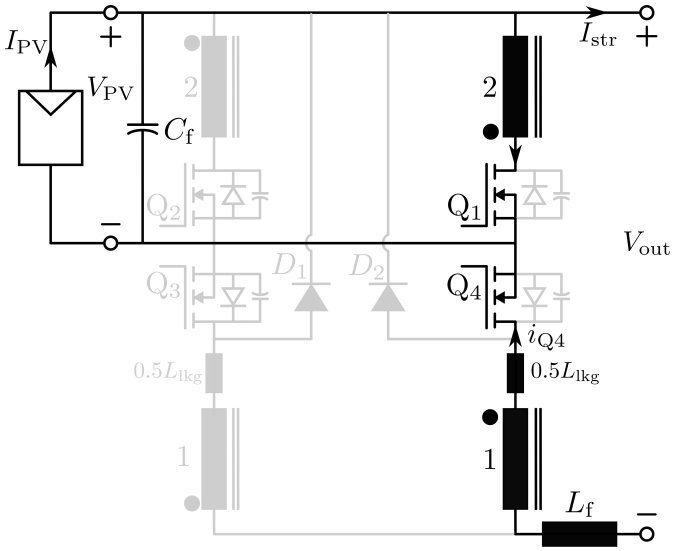


Fig. 4.16: MIC equivalent circuit during switching interval $S_5 : t_5 < t < T/2$ of the Process mode.

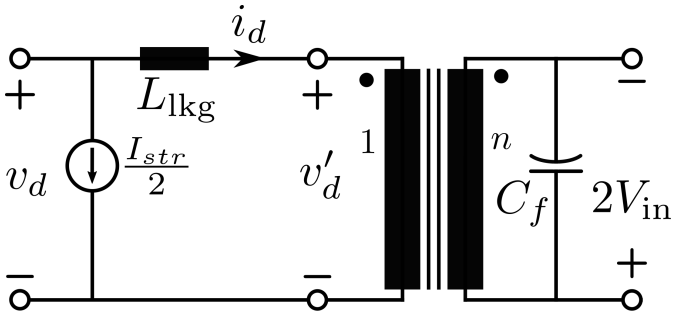


Fig. 4.17: Transformer model loaded with MIC circuit during switching interval S_5 $(t_5 < t < T/2)$ of the Process mode.

and the only conducting devices are Q_1 and Q_4 which have constant currents during the entire interval. The converter circuit and its differential mode using the transformer model is shown in Fig. 4.16 and Fig. 4.17, respectively. As can be seen from differential circuit $i_d = -0.5I_{str}$. Also as $i_{com} = 0.5I_{str}$, equations (4.6) are used to obtain switch currents as:

$$i_{Q1} = 0.5I_{str}, \tag{4.104}$$

$$i_{Q2} = 0, \tag{4.105}$$

$$i_{Q3} = 0, \tag{4.106}$$

$$i_{Q4} = I_{str}. \tag{4.107}$$

As can be seen, the above equations exactly match the actual converter circuit in Fig. 4.16 which verifies the proposed transformer model. The currents obtained at the

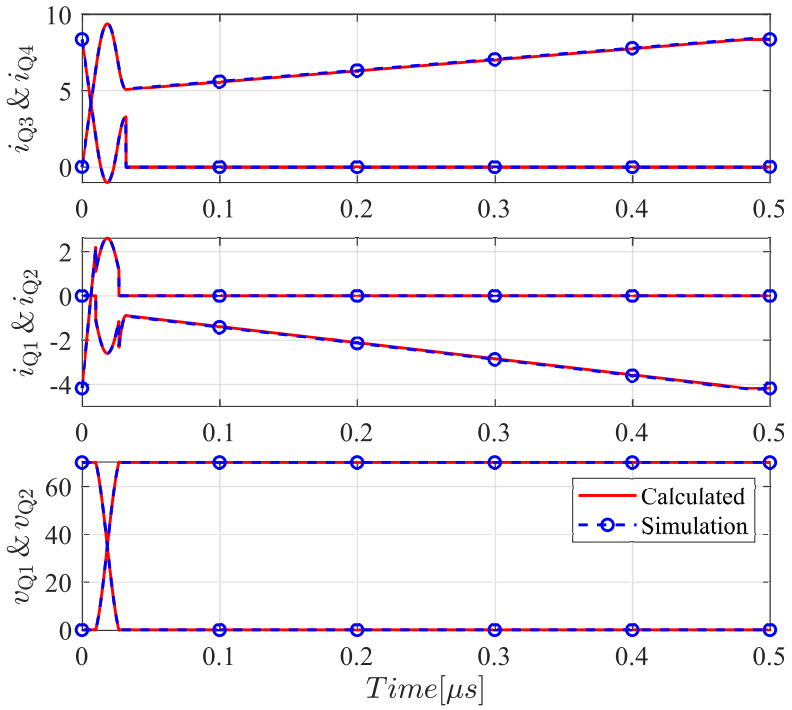


Fig. 4.18: The calculated switch voltage and current waveforms of the MIC versus simulated waveforms.

end of interval S_5 are complement of the initial conditions that are considered for the S_0 which verifies the analysis using the fact that waveforms are half-wave symmetrical.

Now that the equations of converter waveforms are obtained using the new transformer model, the results can be verified by comparing the equations to simulation results. Consider an MIC with the following parameters which are derived according to experimental setup:

$$I_{str} = 8.4[\text{A}], \tag{4.108}$$

$$V_{in} = 35[\text{V}], \tag{4.109}$$

$$V_f = 0.4[\text{V}], \tag{4.110}$$

$$L_{lkg} = 55[n\text{H}], \tag{4.111}$$

$$C_{oss} = 0.5[n\text{F}], \tag{4.112}$$

$$D = 0.52, \tag{4.113}$$

$$T = 1[\mu\text{s}]. \tag{4.114}$$

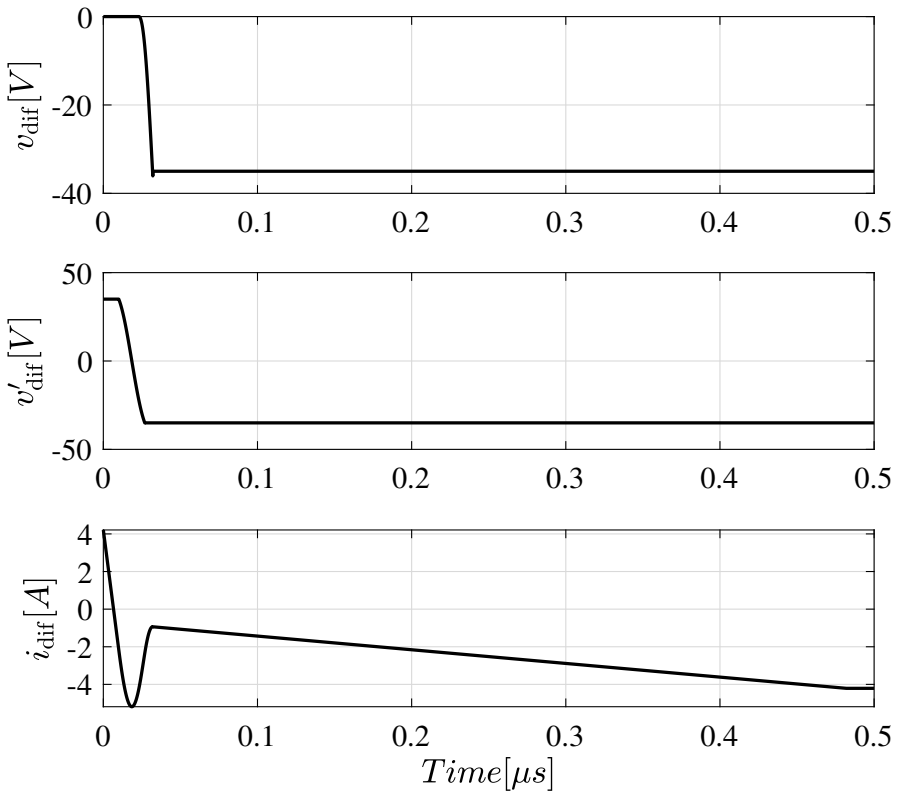


Fig. 4.19: The calculated waveforms of the MIC differential mode equivalent circuit during the Process mode.

Voltage and current waveforms can be obtained for all of the switches in the MIC using the analysis given above. The same circuit parameters are used to simulate the converter in PSIM software and the results are compared to calculated waveforms in Fig. 4.18. As can be seen the calculated waveforms exactly match the simulated waveforms which verifies the proposed transformer model and analysis.

Now, to provide more insight into the analysis of the MIC, the differential circuit results are discussed more. The calculated waveforms for differential mode quantities are given in Fig. 4.19. Considering the string side of the transformer the differential and common quantities translate into switch voltage and current source representing the MIC string side:

$$v_{dif} = v_{Q4} - v_{Q3} \tag{4.115}$$

$$v_{com} = 2v_{cs} + v_{Q3} + v_{Q4} \tag{4.116}$$

, where v_{cs} shows the voltage appearing across the current source representing the string

side common mode circuit. It is important to note that the constant current source used to show the common mode current is representing the series combination of inductive filter and any voltage source or load connected between the inductive filter and the ground of FETs. According to MIC circuit diagram V_{out} and V_{PV} are connected between inductive filter and ground, which results in:

$$< v_{cs} >=< V_{L_f} > +V_{out} - V_{PV}. \tag{4.117}$$

Since at steady state the average inductive filter voltage is zero ($< V_{L_f} >= 0$) the above equation is further simplified:

$$< v_{cs} >= V_{out} - V_{PV}. \tag{4.118}$$

According to the $L_{dC} = \infty$ assumption, common mode ports are always short circuit which simplifies (4.116) into:

$$2v_{cs} = -(v_{Q3} + v_{Q4}) \tag{4.119}$$

For half cycle of MIC operation in Process mode either Q_3 or Q_4 is off which further simplifies the above equation. For the half cycle considered in the MIC analysis given earlier in this chapter $v_{Q4} = 0$ which leads to:

$$2v_{cs} = -v_{Q3} \tag{4.120}$$

Also, using (4.115) $v_{Q4} = 0$ results in:

$$v_{dif} = -v_{Q3} \tag{4.121}$$

and eventually:

$$v_{cs} = \frac{1}{2}v_{dif}. \tag{4.122}$$

Combining the equation obtained from MIC circuit diagram i.e., (4.118) with the equation obtained from the transformer model i.e., (4.122) the following equation is derived:

$$V_{out} - V_{PV} = \frac{1}{2}v_{dif}. \tag{4.123}$$

This results in the following equation for the MIC voltage conversion ratio:

$$\frac{V_{out}}{V_{PV}} = 1 + \frac{1}{2}\frac{< v_{dif} >}{V_{PV}} = 1 - \frac{1}{2}\frac{| < v_{dif} > |}{V_{PV}}. \tag{4.124}$$

For the experimental setup parameters given earlier the voltage conversion ratio becomes:

$$\frac{V_{out}}{V_{PV}} = 0.529 \tag{4.125}$$

The same procedure can be applied to the currents going through the capacitive filter to obtain the current conversion ratio:

$$\frac{I_{PV}}{I_{str}} = 0.529 \tag{4.126}$$

4.1.5 General Equivalent Model of the MIC

Now that the conversion ratios are known for Process mode, an accurate model of the MIC for all of its operating modes i.e., Pass through, Process and Bypass modes can be obtained. In order to draw a general model for the MIC two observations from MIC operation in Process mode are used:

- According to the Fig. 4.19, in the process mode, the differential voltage has a pulse-width shape if the resonance cycles are considered small compared to the whole switching cycle. This pulse width is modulating the PV voltage by a duty cycle approximately equal to 2 times the complement of switch Q_3 and/or Q_4 duty cycle during the Process mode:

$$d_{Proc} \approx 2\left(1 - d_{Q3,4}\right). \tag{4.127}$$

- The MIC operation in Pass-through mode where Q_3 and Q_4 are always ON can be modeled by $d_{Proc} = 0$. MIC operation in Bypass mode where Q_3 and Q_4 are always OFF can be modeled by $d_{Proc} = 2$.

Using above two observations an accurate model of the MIC can be obtained in form of a Pulse-Width Modulating (PWM) converter. The model would only contain the L_f and C_f as the energy storing elements while the effects of the parasitic elements such as C_{oss}

of FETs and inductances of the transformer are abstracted into the d_{Proc}. According to first observation the resonance elements of Process mode along with the duty cycle of Q_3 and/or Q_4 can be modeled as d_{Proc}. The resonance caused by the C_{oss} of FETs and inductances of the transformer will change the d_{Proc} from what (4.127) predicts by a small value. For example as discussed earlier for the parameter set obtained from experimental setup the voltage conversion ratio is obtained as 0.529 while the Q_3 and/or Q_4 duty cycle was $< d_{Q3,4} >= 0.52$. In this example a difference of $< \Delta d >= 0.009$ can be used to compensate for the effects of high frequency parasitic elements:

$$d_{Proc} = 2\left(1 - d_{Q3,4} - \Delta d\right). \tag{4.128}$$

Given a parameter set for the MIC, the equations obtained for high frequency waveforms of the Process mode can be used to obtain the Δd and insert it to (4.128) to find d_{Proc}. Therefore, the MIC model in Process mode would be PWM converter composed of L_f and C_f with the high frequency modulating signal $d_{Proc}(t)$ which switches with double the Process mode's frequency and duty cycle of $< d_{Proc} >$. The general MIC model would include another lower frequency modulation which modulates the total duty cycle d_{tot} with the Pulse Density Modulation (PDM) duty cycle ($d_{PDM}(t)$).

$$d_{tot}(t) = \begin{cases} d_{Proc}(t) & \text{if} \quad d_{PDM} = 1, \\ 0 & \text{if} \quad d_{PDM} = 0, \\ 2 & \text{if} \quad d_{PDM} = -1, \end{cases} \tag{4.129}$$

where the operation of MIC in Process mode, Pass-through mode and Bypass mode are shown for values of the d_{PDM} equal to 1, 0 and -1 respectively. Now (4.124) is utilized to obtain the waveforms that appear across/through the switches of the equivalent PWM converter of the MIC model. According to (4.124), the voltage conversion ratio of converter in Process mode is proportional to the complement of $\frac{1}{2}\frac{|<v_{dif}>|}{V_{PV}}$ term. The ratio 1/2 in this equation is caused by the transformer turns ratio, therefore for any transformer turns ratio this term can be used to model transformer turns ratio effects. The fact that conversion ratio is related to the complement of differential voltage to PV voltage is caused by the application of partial power processing in the converter. This behavior and transformer turns ratio effect can be modeled by using the $1 - \frac{1}{2}d_{tot}$ as the duty ratio of the equivalent PWM converter instead of using d_{tot} as the converter duty cycle.

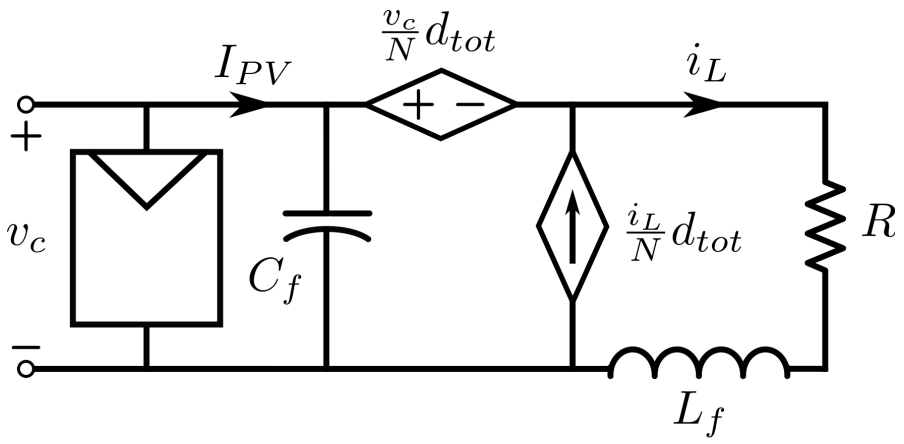


Fig. 4.20: The equivalent PWM converter modeling the behavior of MIC during every mode of operation i.e., Process, Pass-through and Bypass modes.

Figure 4.20 shows the proposed general model of the MIC according to above discussion. In this model the conversion ratio caused by Partial Power Processing, duty cycle of converter in Process mode, and transformer turns ratio are all modeled as a PWM converter.

4.2 Analysis and Design of MIC using State Space LBSM

Now that the general model of the MIC is obtained the LBSM can be leveraged to obtain the closed-form equations for converter waveforms. As the equivalent converter shown in Fig. 4.20 is a second order system and interior switched network, the most efficient approach to analyze it is through the State Space representation of LBSM.

4.2.1 Extending State Space LBSM to interior switched network converters

According to state space representation of the LBSM if the system state space representation is as follows:

$$\frac{d\boldsymbol{x}}{dt} = \boldsymbol{A}\boldsymbol{x}(t) + \boldsymbol{g}(t), \tag{4.130}$$

Then the steady state initial conditions are obtained as:

$$\boldsymbol{X_0} = -\left[\boldsymbol{I} - e^{-\boldsymbol{A}\mathrm{T}}\right]^{-1} \int_0^{\mathrm{T}} e^{-\boldsymbol{A}t}\boldsymbol{g}(t)dt, \tag{4.131}$$

In the above equation, $\boldsymbol{g}(t)$ is the periodic discontinuous vector that consists of external inputs only for the case of edge switched network converters while $\boldsymbol{g}(t)$ for the interior switched network converters is as below:

$$\boldsymbol{g}(t) = \boldsymbol{\Psi}(t) + \sum_{i=1}^{m} q_i(t)\boldsymbol{B_i}\boldsymbol{u}(t) \tag{4.132}$$

where $\boldsymbol{\Psi}(t)$ reflects the interior states appearing as the discontinuous and periodic input to the system in interior switched network converters:

$$\boldsymbol{\Psi}(t) \equiv \sum_{i=1}^{m-1} \left(\boldsymbol{A_i} - \boldsymbol{A_m}\right)\left(q_i(t)\boldsymbol{x}(t)\right). \tag{4.133}$$

In the above equation, $\boldsymbol{A_i}$ and $\boldsymbol{B_i}$ are the state matrix and input matrix of the converter equivalent circuit during its $i-$th switching interval. Also, the total number of switching intervals are denoted by m in the above equation.

Substituting for $\boldsymbol{g}(t)$ from (4.132) into (4.131) results in an implicit equation in terms of $\boldsymbol{X_0}$ which needs further mathematical manipulation before it can be used to compute $\boldsymbol{X_0}$.

$$\boldsymbol{X_0} = -\left[\boldsymbol{I} - e^{-\boldsymbol{A}\mathrm{T}}\right]^{-1}\int_0^{\mathrm{T}} e^{-\boldsymbol{A}t}\boldsymbol{\Psi}(t)dt - \left[\boldsymbol{I} - e^{-\boldsymbol{A}\mathrm{T}}\right]^{-1}\int_0^{\mathrm{T}} e^{-\boldsymbol{A}t}\sum_{i=1}^{m} q_i(t)\boldsymbol{B_i}\boldsymbol{u}(t)dt \tag{4.134}$$

4.2.2 Explicit Solution for X_0

The second term of (4.134) is independent of $\boldsymbol{X_0}$, while the first term of (4.134) is a function of $\boldsymbol{X_0}$ and is derived as follows:

$$\int_0^{\mathrm{T}} e^{-\boldsymbol{A}t}\boldsymbol{\Psi}(t)dt = \int_0^{\mathrm{T}} e^{-\boldsymbol{A}t}\sum_{i=1}^{m-1}\left(\boldsymbol{A_i} - \boldsymbol{A_m}\right)\left(q_i(t)\boldsymbol{x}(t)\right) =$$

$$\int_0^{\mathrm{T}} e^{-\boldsymbol{A}t}\left(\sum_{i=1}^{m-1} q_i(t)\left(\boldsymbol{A_i} - \boldsymbol{A_m}\right)\left(\boldsymbol{X_{i-1}}e^{\boldsymbol{A_i}(t-t_{i-1})} + \int_{t_{i-1}}^{t} e^{\boldsymbol{A_i}\tau}\boldsymbol{B_i}\boldsymbol{u}(t-\tau)d\tau\right)\right)dt, \tag{4.135}$$

where $\boldsymbol{X_{i-1}}$ is the initial value of the states in the beginning of $i-$th switching interval. In order to simplify (4.135), the augmented matrix concept is utilized as below. Consider

the augmented matrices $\hat{\boldsymbol{x}}$ and $\hat{\boldsymbol{A}}_{\boldsymbol{i}}$ as below:

$$\hat{\boldsymbol{x}} = \begin{bmatrix} \boldsymbol{x} \\ 1 \end{bmatrix} \tag{4.136}$$

$$\hat{\boldsymbol{A}}_{\boldsymbol{i}} = \begin{bmatrix} \boldsymbol{A_i} & \boldsymbol{B_i u} \\ \boldsymbol{0} & 0 \end{bmatrix} \tag{4.137}$$

Using the defined augmented matrices, the state equation of the system in its switching intervals simplifies into:

$$q_i(t)\boldsymbol{x} = q_i(t) \begin{bmatrix} \boldsymbol{I} & \boldsymbol{0} \end{bmatrix} e^{\hat{\boldsymbol{A}}_{\boldsymbol{i}}(t-t_{i-1})} \hat{\boldsymbol{X}}_{\boldsymbol{i-1}}, \tag{4.138}$$

where $\boldsymbol{I}$ is unity matrix and $\hat{\boldsymbol{X}}_{\boldsymbol{i-1}}$ is obtained as:

$$\hat{\boldsymbol{X}}_{\boldsymbol{i-1}} = \prod_{k=1}^{i-1} e^{\hat{\boldsymbol{A}}_{\boldsymbol{k}}(t_k - t_{k-1})} \hat{\boldsymbol{X}}_{\boldsymbol{0}} \tag{4.139}$$

Substituting (4.138) and 4.139 into (4.135) results in:

$$\int_0^{\mathrm{T}} e^{-\boldsymbol{A}t} \boldsymbol{\Psi}(t) dt = \int_0^{\mathrm{T}} e^{-\boldsymbol{A}t} \sum_{i=1}^{m-1} q_i(t) \left(\boldsymbol{A_i} - \boldsymbol{A_m}\right) \begin{bmatrix} \boldsymbol{I} & \boldsymbol{0} \end{bmatrix} e^{\hat{\boldsymbol{A}}_{\boldsymbol{i}}(t-t_{i-1})} \prod_{k=1}^{i-1} e^{\hat{\boldsymbol{A}}_{\boldsymbol{k}}(t_k - t_{k-1})} \hat{\boldsymbol{X}}_{\boldsymbol{0}} dt \tag{4.140}$$

Further simplifications result in:

$$\int_0^{\mathrm{T}} e^{-\boldsymbol{A}t} \boldsymbol{\Psi}(t) dt = \sum_{i=1}^{m-1} \left(\int_{t_{i-1}}^{t_i} e^{-\boldsymbol{A}t} \left(\boldsymbol{A_i} - \boldsymbol{A_m}\right) \begin{bmatrix} \boldsymbol{I} & \boldsymbol{0} \end{bmatrix} e^{\hat{\boldsymbol{A}}_{\boldsymbol{i}}(t-t_{i-1})} dt \prod_{k=1}^{i-1} e^{\hat{\boldsymbol{A}}_{\boldsymbol{k}}(t_k - t_{k-1})} \right) \hat{\boldsymbol{X}}_{\boldsymbol{0}} \tag{4.141}$$

To make notation more traceable $\boldsymbol{M}$ is defined as in below:

$$\boldsymbol{M} = \sum_{i=1}^{m-1} \left(\int_{t_{i-1}}^{t_i} e^{-\boldsymbol{A}t} \left(\boldsymbol{A_i} - \boldsymbol{A_m}\right) \begin{bmatrix} \boldsymbol{I} & \boldsymbol{0} \end{bmatrix} e^{\hat{\boldsymbol{A}}_{\boldsymbol{i}}(t-t_{i-1})} dt \prod_{k=1}^{i-1} e^{\hat{\boldsymbol{A}}_{\boldsymbol{k}}(t_k - t_{k-1})} \right). \tag{4.142}$$

Therefore (4.135) is simplified as:

$$\int_0^{\mathrm{T}} e^{-\boldsymbol{A}t} \boldsymbol{\Psi}(t) dt = \boldsymbol{M} \hat{\boldsymbol{X}}_{\boldsymbol{0}} \tag{4.143}$$

Substituting (4.143) into (4.134) results in:

$$\boldsymbol{X_0} = -\left[\boldsymbol{I} - e^{-\boldsymbol{A}\mathrm{T}}\right]^{-1}\left(\boldsymbol{M}\hat{\boldsymbol{X}}_{\boldsymbol{0}} + \int_0^{\mathrm{T}} e^{-\boldsymbol{A}t}\sum_{i=1}^{m} q_i(t)\boldsymbol{B_i}\boldsymbol{u}(t)dt\right) \tag{4.144}$$

Further simplifying the above equation using:

$$\hat{\boldsymbol{X}}_{\boldsymbol{0}} = \begin{bmatrix}\boldsymbol{I}\\ \boldsymbol{0}\end{bmatrix}\boldsymbol{X_0} + \begin{bmatrix}\boldsymbol{0}\\ 1\end{bmatrix}, \tag{4.145}$$

results in:

$$\boldsymbol{X_0} = -\left[\boldsymbol{I} - e^{-\boldsymbol{A}\mathrm{T}}\right]^{-1}\left(\boldsymbol{M}\begin{bmatrix}\boldsymbol{I}\\ \boldsymbol{0}\end{bmatrix}\boldsymbol{X_0} + \boldsymbol{M}\begin{bmatrix}\boldsymbol{0}\\ 1\end{bmatrix} + \int_0^{\mathrm{T}} e^{-\boldsymbol{A}t}\sum_{i=1}^{m} q_i(t)\boldsymbol{B_i}\boldsymbol{u}(t)dt\right) \tag{4.146}$$

Combining the terms containing $\boldsymbol{X_0}$ in both sides of equation results in:

$$\left(\boldsymbol{I} + \left[\boldsymbol{I} - e^{-\boldsymbol{A}\mathrm{T}}\right]^{-1}\boldsymbol{M}\begin{bmatrix}\boldsymbol{I}\\ \boldsymbol{0}\end{bmatrix}\right)\boldsymbol{X_0} = -\left[\boldsymbol{I} - e^{-\boldsymbol{A}\mathrm{T}}\right]^{-1}\left(\boldsymbol{M}\begin{bmatrix}\boldsymbol{0}\\ 1\end{bmatrix} + \int_0^{\mathrm{T}} e^{-\boldsymbol{A}t}\sum_{i=1}^{m} q_i(t)\boldsymbol{B_i}\boldsymbol{u}(t)dt\right) \tag{4.147}$$

Therefore, the explicit solution for $\boldsymbol{X_0}$ is obtained as below:

$$\boldsymbol{X_0} = -\left(\boldsymbol{I} + \left[\boldsymbol{I} - e^{-\boldsymbol{A}\mathrm{T}}\right]^{-1}\boldsymbol{M}\begin{bmatrix}\boldsymbol{I}\\ \boldsymbol{0}\end{bmatrix}\right)^{-1}\left[\boldsymbol{I} - e^{-\boldsymbol{A}\mathrm{T}}\right]^{-1}\left(\boldsymbol{M}\begin{bmatrix}\boldsymbol{0}\\ 1\end{bmatrix} + \int_0^{\mathrm{T}} e^{-\boldsymbol{A}t}\sum_{i=1}^{m} q_i(t)\boldsymbol{B_i}\boldsymbol{u}(t)dt\right) \tag{4.148}$$

As can be seen from (4.148), the initial conditions for an interior switched network converter can be explicitly obtained using the state and input matrices of the converter at its different switching intervals.

4.3 LBSM Analysis of MIC Equivalent Converter

Now that the initial condition equations for a general interior switched network converter is obtained in state space the MIC equivalent PWM converter can be analyzed using LBSM. As the most probable and efficient operation of the MIC is for voltage conversion ratios of 0.5 to 1 where the MIC operates through PDM of Process and Pass-through modes, only this range is shown for the analysis. The range of conversions between 0 and 0.5 can be obtained using the same procedure shown here.

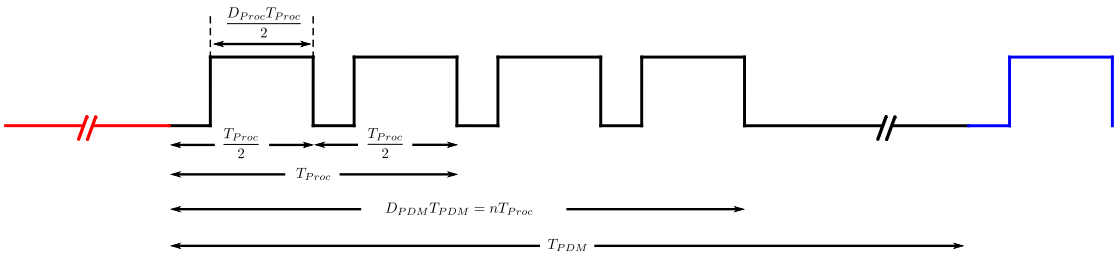


Fig. 4.21: Duty cycle of the equivalent PWM converter of MIC, $d_{tot}(t)$ for the operation of converter with n cycles in Process mode and the rest of the cycles in Pass-through mode.

According to (4.129), the converter operation with only Pass-through and Process modes can be described by having the d_{tot} as a PWM signal changing between 1 and 0 as shown in Fig. 4.21. In Fig. 4.21 it is assumed that MIC operates in Process mode for n cycles of the Process mode and operates in the pass-through mode for rest of the cycles of PDM.

4.3.1 Derivation of State Space LBSM of MIC

According to equivalent PWM converter model of the MIC shown in Fig. 4.20 and d_{tot} given in Fig. 4.21 the state space model of the MIC can be derived. If there are n cycles of operation in Process mode there will be a total of $2n + 1$ switching intervals for the converter. As d_{tot} only has two states of 0 and 1 and according to the converter model only two sets of $\boldsymbol{A}$ and $\boldsymbol{B}$ matrices is sufficient to describe the converter model in all of its switching intervals. These matrices can be derived according to converter model as follows. If $d_{tot}(t) = 0$ then the converter model is:

$$\dot{\boldsymbol{x}} = \boldsymbol{A_1 x} + \boldsymbol{Bu}, \tag{4.149}$$

where:

$$\boldsymbol{x} = \begin{bmatrix} v_c \\ i_L \end{bmatrix}, \tag{4.150}$$

$$\boldsymbol{A_1} = \begin{bmatrix} -\frac{1}{RC} & -\frac{1}{C} \\ \frac{1}{L} & 0 \end{bmatrix}, \tag{4.151}$$

$$\boldsymbol{Bu} = \begin{bmatrix} \frac{I_{PV}}{C} \\ 0 \end{bmatrix}. \tag{4.152}$$

If $d_{tot}(t) = 1$ then the converter model is:

$$\dot{\boldsymbol{x}} = \boldsymbol{A_2 x} + \boldsymbol{B u}, \tag{4.153}$$

where:

$$\boldsymbol{A_2} = \begin{bmatrix} -\frac{1}{RC} & -\frac{1}{C}\left(1-\frac{1}{N}\right) \\ \frac{1}{L}\left(1-\frac{1}{N}\right) & 0 \end{bmatrix}. \tag{4.154}$$

Now, the converter model across all switching intervals can be written using the above equations. The state matrix of odd intervals are the same and the state matrix of the even switching intervals are the same. Also, it is important to note that in LBSM the last switching interval is taken as reference for system state matrix and the state matrix of the other intervals are subtracted from last sate matrix. The state equation of the converter across all of its switching intervals is:

$$\dot{\boldsymbol{x}} = \boldsymbol{A_1 x} + (\boldsymbol{A_2} - \boldsymbol{A_1}) \sum_{i=1}^{n} q_{2i}(t) \boldsymbol{x} + \boldsymbol{B u}, \tag{4.155}$$

Therefore, the steady state initial condition for the MIC can be obtained using (4.148) as:

$$\boldsymbol{X_0} = -\left(\boldsymbol{I} + \left[\boldsymbol{I} - e^{-\boldsymbol{A_1}\mathrm{T}}\right]^{-1} \boldsymbol{M} \begin{bmatrix} \boldsymbol{I} \\ \boldsymbol{0} \end{bmatrix} \right)^{-1} \left[\boldsymbol{I} - e^{-\boldsymbol{A_1}\mathrm{T}}\right]^{-1} \left(\boldsymbol{M} \begin{bmatrix} \boldsymbol{0} \\ 1 \end{bmatrix} + \int_0^{\mathrm{T}} e^{-\boldsymbol{A_1} t} dt \boldsymbol{B u} \right) \tag{4.156}$$

where $\boldsymbol{M}$ is:

$$\boldsymbol{M} = \sum_{i=1}^{n} \left(\int_{t_{2i-1}}^{t_{2i}} e^{-\boldsymbol{A_1} t} \left(\boldsymbol{A_2} - \boldsymbol{A_1}\right) \begin{bmatrix} \boldsymbol{I} & \boldsymbol{0} \end{bmatrix} e^{\hat{\boldsymbol{A}}_{\boldsymbol{2}}(t - t_{2i-1})} dt \prod_{k=1}^{i-1} e^{\hat{\boldsymbol{A}}_{\boldsymbol{k}}(t_k - t_{k-1})} \right). \tag{4.157}$$

In the above equation t_i is the time at which the i-th interval ends and is found according to Fig. 4.21 as:

$$t_i = \begin{cases} \left(1 - D_{Proc} + \frac{i-1}{2}\right) T_{Proc} & \text{if } i \text{ is odd} \\ \frac{i}{2} T_{Proc} & \text{if } i \text{ is even} \end{cases} \tag{4.158}$$

Now that the closed-form equations for the states of the MIC i.e., capacitive filter voltage and inductive filter current are derived, they can be leveraged to provide some insight into MIC design. First, the obtained equations iare used to find the worst case scenario for the ripple on the filters. For this purpose a constant filter parameters are

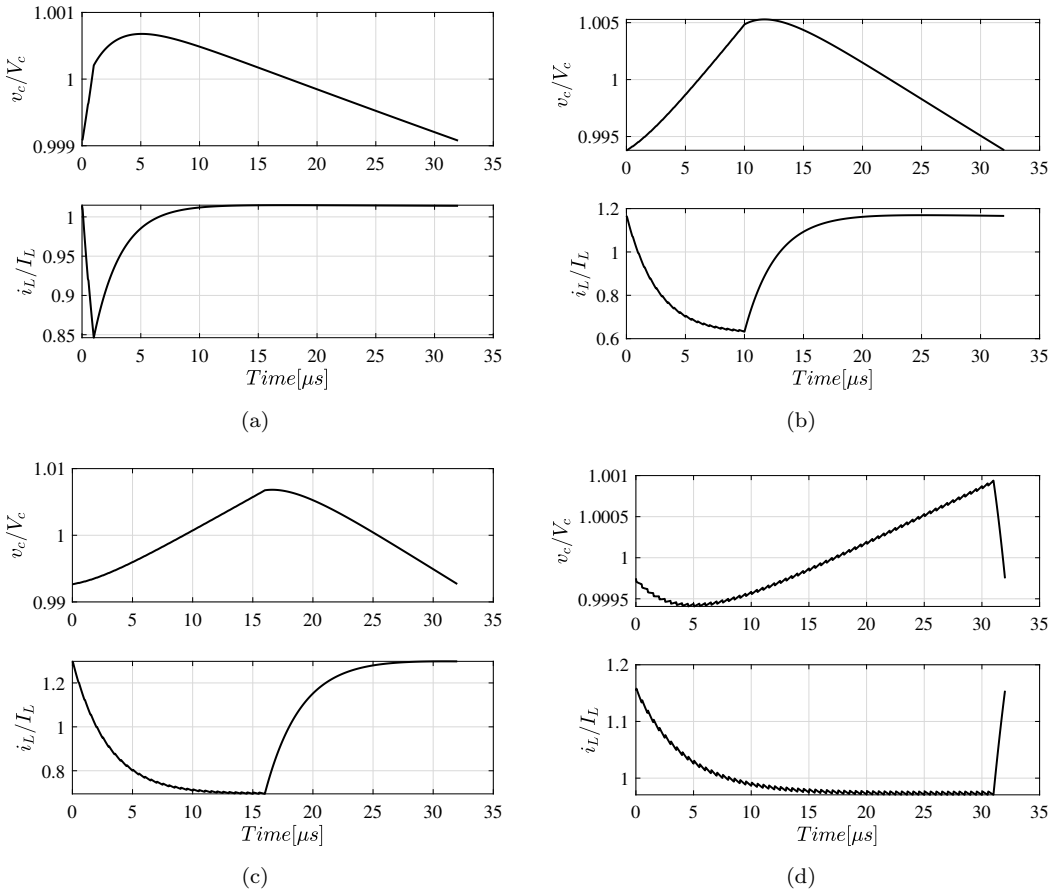


Fig. 4.22: Normalized capacitive filter voltage and inductive filter current with (a) $n = 1$ (b) $n = 10$ (c) $n = 16$ and (d) $n = 31$ obtained using LBSM.

considered as $L_f = 10\mu H$, and $C_f = 100\mu F$ and the waveforms are obtained for different duty cycles of PDM. To show PDM duty cycle n is used here which shows number of cycles in PDM out of every 32 full switching cycles.

4.3.2 Application of LBSM Equations in MIC Design

Fig. 4.22 shows the normalized capacitor voltage and inductor current with respect to time in one PDM cycle for different values of n. As can be seen, the trend of the ripples states that ripples get smaller as the PDM duty cycle approaches 0 or 1 and it gets to maximum value somewhere in between. This observation is crucially important for optimizing the converter design as the worst case ripple is not occurring at lowest or highest PDM duty cycle. Conventional PDM which is used with duty cycle or frequency controlled converters has the worst case ripple for either minimum or maximum PDM duty cycle therefore the PDM frequency is increased to keep the ripple in acceptable

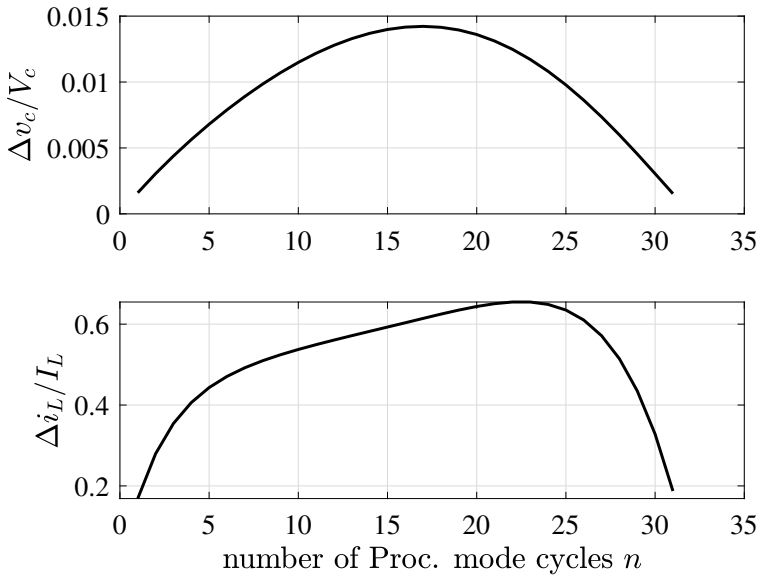


Fig. 4.23: normalized voltage and current ripples of the MIC filter for $L_f = 10\mu H$ and $C_f = 100\mu F$ and PDM cycle of 32 pulses.

range. Increasing the PDM frequency reduces the granularity of the PDM duty cycle and causes reduced MPPT efficiency. For example if a PDM cycle of 32 pulses is used PDM duty cycle can be set with about 3% accuracy while if instead of 16 pulses is used then the PDM duty cycle can only be controlled with about 6% steps. However, based on the observation made using the LBSM results it is known that the minimum or maximum PDM duty cycle are not restricting the ripple level in the MIC. This fact is closely related to the application of PPP along with PDM control which eliminates the bottle neck of the PDM operation. Therefore MIC ripple peaks at some point with PDM duty cycle close to 0.5. Thus, the pulses of the PDM can be interleaved to reduce the amount of ripple on filters and consequently allow for less filter usage or improved granularity in PDM duty cycle. For example Fig. 4.23 shows the voltage and current filter normalized ripple for the discussed MIC filter values and PDM cycle of 32 pulses. As can be seen the maximum ripple occurs at about $n = 24$. In such case, rather than using 24 consecutive pulses out of 32 one can use 3 pulses out of every 4 pulses to get the same PDM duty ratio while reducing the maximum converter ripple. In this case the 1 pulse out of 32 will still give the low amount of ripple as shown in Fig. 4.23 while it still provides a 3% long PDM duty cycle. Therefore according to insight provided by LBSM the PDM duty cycle can be further modulated at middle values to reduce the converter worst case scenario ripples and reduce the filter size accordingly. As another insight given by the LBSM the effect of each filter parameters on the ripples of the MIC can

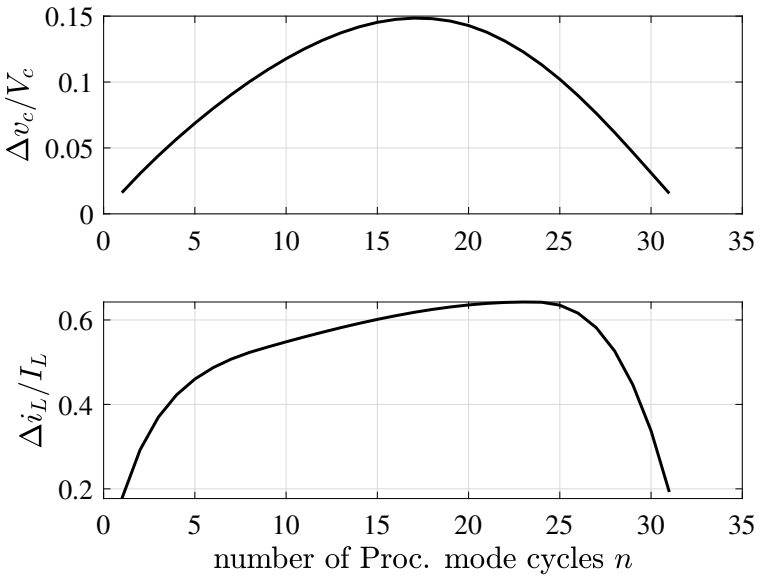


Fig. 4.24: normalized voltage and current ripples of the MIC filter for $L_f = 10\mu H$ and $C_f = 10\mu F$ and PDM cycle of 32 pulses.

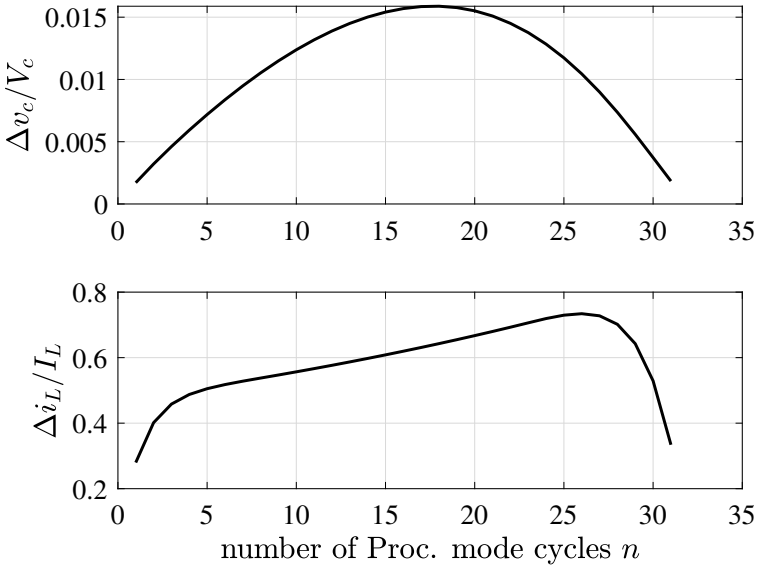


Fig. 4.25: normalized voltage and current ripples of the MIC filter for $L_f = 5\mu H$ and $C_f = 100\mu F$ and PDM cycle of 32 pulses.

be studied. Figure. 4.24 shows the ripples obtained for the MIC with $L_f = 10\mu H$ and $C_f = 10\mu F$ which has the same inductive filter as the MIC shown in Fig. 4.23 but has a capacitive filter that is an order of magnitude smaller than the previous MIC. As can be seen the inductive filter ripple is almost same as Fig. 4.23 while the voltage ripple has increased. The other example can be obtained by comparing the ripples of these two MICs to the MIC with $L_f = 5\mu H$ and $C_f = 100\mu F$ as shown in Fig. 4.25. This example shows that the current ripples are increased compared to Fig. 4.23 while voltage ripples has stayed the same. According to these observations it can be concluded that changing

the value of each filter only affects the ripple of its own and does not affect the other filter's ripple. This insight proves that there is not much coupling between inductive and capacitive filters in converter operation and each can be designed independently.

4.3.3 summary

In this chapter a new model is proposed for center tapped transformer which simplifies the MIC analysis and gives more insight about the effects of different parasitic elements of the MIC transformer. The LBSM analysis of the MIC is performed by proposing a general equivalent PWM converter for the MIC and by means of extending the LBSM application to state space representation of interior switched network converters. Using the LBSM results it is shown that MIC filter design can be improved if the PDM duty cycle of the MIC is further modulated at around half duty cycle. Also, it has been observed that each filter of MIC only affects its own ripple and is independent of the other filter.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

In this research, various PV system configurations have been studied to exhibit the analysis and design requirements for dc-dc PV converters. It has been revealed that an accurate and general modeling tool is required for the steady-state analysis and design of PV converters. A new approach to steady-state modeling, referred to as Laplace Based Steady-state Modeling (LBSM), has been developed and demonstrated to be an effective tool for the analysis and design of a broad class of power converters. In LBSM the converter is first modeled using an equivalent circuit in which the switches are replaced by independent voltage or current sources whose periodic and discontinuous values may depend on the initial values of the converter's state variables during steady-state operation. The initial values of the state variables under steady-state operation are determined using the Laplace Based Theorem (LBT). The constant-coefficient non-homogeneous ordinary differential equation (ODE) associated with the equivalent circuit is then solved for one switching period to determine closed-form expressions for the converters steady-state waveforms.

The value of LBSM is demonstrated by applying it to a number of different power converters, including the buck converter, the phase-shift controlled series resonant converter, and the phase-shift converter, which are classified as edge switch-network converters, and the boost converter operating in either CCM or DCM, which is classified as an interior switch-network converter. The LBSM derived waveforms are experimentally validated

for boost converters operating in CCM and DCM. To the author's knowledge, LBSM is the first systematic modeling approach that can provide accurate closed-form expressions for the steady-state switched waveforms of interior switch-network converters. The technique developed to model interior switch-network converters is also applicable to edge switch-network converters, although it has steps that are not needed for edge switch-network converters. Therefore, a shorter modeling technique applicable only to edge switch-network converters is also provided. The limitations of LBSM are also identified, and ways to overcome some of these limitations are described. For example, for the modeling of converters operating in DCM, LBSM generally requires a numerical solution.

LBSM also reveals interesting facets of different converters. For example, LBSM discloses the dependence of voltage gain on load resistance for a lossless boost converter operating in CCM, which is not predicted by small ripple approximation. The LBSM derived closed-form analytical expressions for the phase-shift controlled SRC and the PSC are also used to design and compare these converters which are commonly used in PV micro-inverter configuration. By comparing their ZVS boundaries, the preferred operating ranges for the SRC and the PSC are determined. It is discovered that if the required maximum-to-minimum converter input voltage ratio is less than two, then the SRC has better performance, otherwise the PSC is superior. The converter voltage gains, ZVS ranges, and efficiencies for the SRC and the PSC predicted by LBSM are validated using experimental prototypes.

According to PV system configuration studies, it has been also concluded that the PV systems equipped with dc-dc MICs offer best energy capture in the presence of power mismatch. Different dc-dc MIC categories are studied in this research considering both constant and variable dc bus voltage PV systems. It has been shown that for most of the applications, step-down MICs offer better performance such as larger string size, less processed power and component stress, lower number of MIC required in system level, etc. A highly efficient and high frequency step-down PV MIC is proposed based on series-PPC. The two configurations of the series-PPC are compared for the component level realization of the MIC and it has been concluded that ISOP configuration may offer better efficiency.

In this research, a new topology is developed for the MIC that renders soft-switching

and offers high frequency operation and high efficiency. Rather than conventional duty cycle or frequency control for soft-switching converters a special PDM control method is adopted to perform MPPT using the proposed MIC. This PDM method regulates the MIC conversion ratio by time modulation of the converter operation in three modes of operation which are called Pass-through, Bypass and Process modes. Using the proposed PDM technique, MIC efficiency drop with conversion ratio reduction can be kept linear unlike the conventional PV MICs where a huge drop is observed around unity conversion ratio. Furthermore, the efficient operating modes of Pass-through and Process are used for high power and statistically most probable range of the PV power generation, while full MPPT range is obtained using Bypass mode. Due to independence of these three modes, the MIC can be optimized for any PV power generation range that is statistically valuable while it is still able to cover the full MPPT range. A prototype MIC is build and tested to experimentally validate the soft-switching operation, PDM and conversion ratio regulation and efficiency improvements.

Also, this thesis introduces a novel model for a center-tapped transformer, which simplifies the analysis of the (MIC) and provides a deeper understanding of the impact of different parasitic elements on the MIC transformer. The analysis of the MIC is conducted through the proposed general equivalent Pulse Width Modulation (PWM) converter that has been developed using deductive observations on the MIC analysis results. By extending the application of the LBSM to the interior switched network converters' state space representation an explicit solution is provided for this class of converters in state space. MIC analysis using LBSM is given in this thesis where the results obtained from LBSM demonstrate that the design of the MIC filter can be enhanced by further modulating the Pulse Density Modulation (PDM) duty cycle around half duty cycle. Additionally, it is observed that each filter of the MIC only affects its own ripple and operates independently of the other filters.

5.2 Future Works

According to the discussions presented in this thesis, this work can be further elaborated in many directions. Below is a short-list of some important directions that can be taken.

1. Consider leveraging the state space LBSM developed for the fast simulation of converters in steady state.
2. Consider adding a higher layer on top of LBSM to analyze all mathematically possible topology variants of existing converter and find the optimum variant.
3. Consider magnetic integration of the MIC inductor and transformer.
4. Consider application of the stack of MICs as a DC source for current sourced inverters.

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