High Power Long Lifetime LED Drivers

by

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Abstract

This thesis addresses the design and implementation of durable LED driver for street lighting application. LED based street lighting products are now available in various power ratings, light intensity, and color temperature [1]. Higher efficiency, light quality and Color Rendering Index (CRI), reliability, and reduced maintenance cost are the main reasons that make solid state lighting superior than its counterparts such as High Pressure Sodium, Low Pressure Sodium, Incandescent, and metal halide lighting.

Design of LED drivers involves many technical and practical issues. Harsh operating temperature, power density, and power quality have always been practical issues regarding the design of LED drivers. For single phase applications, double frequency power oscillations can create problems for LEDs. Using electrolytic capacitor is known to address power oscillation issues which sacrifices the durability of LED drivers. Power Factor (PF) and Total Harmonic Distortion (THD) are measurements determining the quality of the power transferred in an electrical system. Providing high power factor and lower harmonic distortion is also another challenge when using non-linear loads such as LEDs and gate driver circuits that include rectifiers, and active switching devices.

In this thesis a new circuit configuration and control structure is proposed to design a durable, compact LED driver for street lighting application which tackles all the aforementioned challenges. The proposed multi-stage topology employs a boost power converter as the power factor correction and a series resonant converter as the power conversion stage. Exploiting faster dynamic of second stage controller to decouple the input oscillating power from the DC output power made it possible to alleviate the need for a large capacitance on DC link and facilitated the use of film capacitors in which wasn't primarily the best choice due to film capacitors' large packages for higher capacitance values. Utilization of film capacitors made the lifespan of the LED driver match the LED lifespan. Generalized peak current control is employed on PFC stage to achieve power factor correction and constant frequency, making it easier to design the output filter, and reducing THD and electromagnetic interference. Second stage of the proposed LED driver consists of a soft-switching high frequency series resonant converter to control the output current which also provides a high power density and electrical isolation. Moreover, comprehensive design of magnetic devices is performed and simulation and experimental results are presented to verify the effectiveness of the design.

Dedicated to Reza, Behrad, and Sheida . . .

Acknowledgements

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Abbreviations

CCM	**C**ontinuous **C**onduction **M**ode
CRI	**C**olor **R**endering **I**ndex
DCM	**D**iscontinuous **C**onduction **M**ode
EMI	**E**lectro**M**agnetic **I**nterference
FB	**F**ull **B**ridge
GPCC	**G**eneralized **P**eak **C**urrent **C**ontrol
HPS	**H**igh **P**ressure **S**odium
IP	**I**ngress **P**rotection
LBT	**L**aplace **B**ased **T**heorem
LED	**L**ight **E**mitting **D**iode
ODE	**O**rdinary **D**ifferential **E**quation
PC	**P**ower **C**onversion
PFC	**P**ower **F**actor **C**orrection
SRC	**S**eries **R**esonant **C**onverter
SSL	**S**olid **S**tate **L**ighting
THD	**T**otal **H**armoic **D**itortion
VF	**V**alley **F**ill
ZVS	**Z**ero **V**oltage **S**witching

Symbols

ω_s	angular switching frequency	rads^{-1}
ω_r	angular resonant frequency	rads^{-1}
f_s	switching frequency	Hz
F	normalized switching frequency	(-)
n_t	transformer primary to secondary turns ratio	(-)
d	duty cycle	(-)
M	voltage gain	(-)

Chapter 1

Introduction

The ever-increasing demand for longer lifetime, higher efficiency, and better luminous quality, rendered the emergence of new technologies to light the world.

Among various technologies within the lighting industry, solid state lighting (SSL) has drawn attention in recent decades. It commonly refers to all applications which use light emitting diodes (LEDs) as a means to generate light. Not only LEDs generate light output with drastically higher efficiency and more than 50 times longer lifetime compared to traditional incandescent light bulbs [6], they also provide very interesting features like controllability over spectral composition and light temperature [7] that formerly were not feasible using incandescent or florescent lamps. Also efficient emission of light output in different parts of electromagnetic spectrum allows LEDs to be used in ultraviolet sanitation and infrared-night vision applications.

LED drivers play a vital role in solid state lighting, as the majority of the aforementioned features can only be achieved through LED drivers and related control systems. Not only do LED drivers allow for the full utilization of durability, efficiency, reliability and safety of solid state lighting, but also they expand the applications of SSL from exit signs, flash lights and indicators to a vast majority of applications like imaging and biotechnology, human health, transportation, communications, agriculture, display technology and general lighting [7]

This thesis focuses on high power long lifetime LED drivers used for street lighting applications. Contrary to the low (or high) pressure sodium counterpart that is widely

used for street lighting applications, LEDs feature lots of advantages that are stated below.

- Color Rendering Index (CRI):

  CRI is a measurement describing the light's ability to reveal the actual color of the surroundings. LEDs generally introduce the CRI of about $65 - 95\%$ which gives pedestrians and drivers the ability to observe the actual color of the objects. While CRI usually falls below 25% for low pressure sodium lamps that illuminate the environment with a yellow monochromatic light [8].

- Directionality:

  LEDs emit light in 180 degrees, directing light to a targeted area is essentially a more efficient use of the output light rather than the traditional light bulbs that emit light in 360 degrees and need a fixture to direct the output light [8].

- Lifespan:

  As mentioned before, LEDs feature longer lifetime than any other source of light. For the street lighting applications, the typical lifespan of LEDs is between 25000 to 200000 hours while this amount for HPS or LPS lamps is around 24000 and 18000 hours respectively [8].

Providing wider range of color temperature, ease of dimming, lower maintenance cost, and having virtually no warm-up time to reach to the maximum brightness are another advantages that are provided by LEDs [8].

However, it's worth noticing that the double frequency power oscillations and unsolicited subharmonics are the major issues that can adversely affect the LED driver's cost of maintenance, size, life span, and also the quality of LED's output light. Therefore, the design of LED driver should efficiently address these issues.

In this chapter, a brief description of LED driver specifications is provided and topologies for different parts of SSL systems are reviewed. Shortcoming associated to different topologies and control schemes are described, and subsequently a topology and control approach to address the mentioned problems are introduced.

1.1 LED Driver Specifications

Designing LED drivers for street lighting applications must be carefully done regarding the standards and specifications imposed by industry and also certain characteristics that facilitate the optimum performance of the SSL system. In this section, the most important requirements are reviewed.

1.1.1 Power Quality

Industry guidelines and standards [9] impose limits on the output of LED drivers power quality. As opposed to other forms of lighting, SSL usually utilizes active switching components and also non-linear loads for illumination. Sinked current from the grid as a result, may not satisfy the Power factor and THD requirements.

Minimum acceptable power factors for domestic and commercial applications according to the U.S Department of Energy (DOE) are 0.7 and 0.9 respectively. In addition, there are certain requirements for power factor and total harmonic distortion (THD) for all lighting products above 75W specified by IEC 1000-3-2 (class C) standard [10]. There has been numerous approaches for enhancing LED driver's output power quality in terms of THD and PF that has been reviewed in chapter 2.

1.1.2 Power Decoupling

In single phase systems, the instantaneous output power oscillates at twice the grid frequency. This oscillation in output power, if transferred to the LEDs, would substantially reduce the lifetime and adversely affect the quality of output light.

Since LEDs are essentially DC loads, the oscillating power should be handled by certain control schemes or circuits. Traditionally, using electrolytic capacitors would be a common approach to alleviate the problem due to the large capacitance they offer in small packages. But these capacitors are not as durable as LEDs and would add to the maintenance costs and reducing the durability of LED driver. Hence, eliminating the electrolytic capacitor in power decoupling methods, would automatically match the lifespan of LEDs and LED drivers.

A review on existing power decoupling methods and approaches to eliminate electrolytic capacitors has been provided in chapter 3.

1.1.3 Current Sharing

Applications such as street lighting, automotive lighting, and TV backlights require multiple LEDs. Driving a large amount of LEDs can be viable through a large lengthy string or parallel strings. While former approach substantially lessens the reliability of LED lighting system, the latter provides more reliability at the expense of current regulation requirements for each LED string.

Similar to diodes, LED's V-I characteristic curve implies a drastic change in LEDs current with a small variation in its forward voltage. Hence, lack of precision in current sharing between parallel strings can be translated into an uneven luminous flux in the output and in severe cases, the failure of some strings due to excessive over current.

Different approaches for current sharing has been proposed in many literatures. Appendix A provides a brief review of existing approaches.

1.1.4 Other LED Driver Specifications

Depending upon the application, various requirements and specifications should be considered while designing an LED driver. Providing dimming range and variant output current and voltage levels, galvanic isolation, mechanical dimensions and IP rating, input voltage and frequency ranges, maximum output current ripple, maximum power, startup time, and protections are the most important specifications.

1.2 SSL Systems Configurations

Apart from the lighting fixture and physical requirements that solely depend on the certain application, SSL systems usually include LED strings and LED driver. In this section, a brief description on different configurations of LEDs and LED drivers are provided.

1.2.1 LED Connections

Individual applications require a certain amount of light intensity and patterns. Based on different requirements, LED configurations can vary. Connection between LEDs can be of series, parallel, or matrix type.

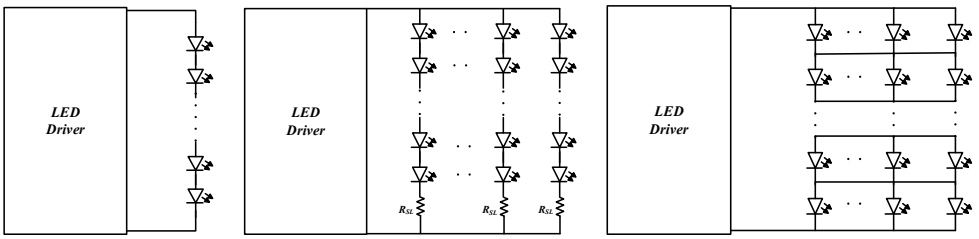


FIGURE 1.1: LED configurations;
(a) Series, (b) Parallel, and (c) Matrix connection

Fig 1.1 (a) shows LEDs in series configuration. This connection is suitable for applications with lower amount of light ouput density and will provide a uniform light and ease of current control. However, in higher power applications, connecting a large amount of LEDs together results in excessive string voltage and in case of failure in any individual LEDs the whole string stops functioning.

Connecting strings in parallel has been depicted in fig 1.1 (b). As opposed to the series connection, this approach provides more fault tolerance and less output voltage for the LED driver, but introduces current sharing issues. Shunt resistors in the picture would facilitate the current sharing between branches but at the expense of a lower efficiency.

Arranging LEDs in series-parallel or matrix form is shown in fig 1.1 (c). Short circuit in any LEDs would disable all the other LEDs in the same row. But open circuit wouldn't affect the overall performance of the whole matrix. Fault tolerance has been improved in this connection type, but complicated current control and PCB design makes this configuration less favorable than parallel connection in high voltage applications.

1.2.2 LED Driver topologies

Key factors determining LED driver's topology are certain requirements associated with the application LED driver is being designed for. In that sense, topologies can vary depending on the below requirements:

- Source type: DC-fed, or AC-fed topologies
- Power Processing from input to output: Entirely or partially
- Number of outputs: Single, or multiple
- Switching type: Soft switching, or hard switching
- Dimming: Non-dimmable, linear dimming, or PWM (burst mode) dimming
- Power decoupling: Incorporating a mass energy storage, or not
- PFC type: Active, passive, or no PFC (for AC-fed LED drivers)
- Isolation: Isolated, or non-isolated

Regardless of the converter topologies employed to meet any of the above requirements, in a broader picture, LED drivers can be divided into two major category of Single and multiple stage groups. Fig. 1.2 shows AC-fed LED drivers with rectified input voltage. As it is shown in the Fig. 1.2, power factor correction is a necessary part of AC-fed LED drivers since they have to comply with PF standards imposed by industry.

1.2.2.1 Single Stage Topologies

As shown in Fig. 1.2 (a), a single stage LED driver is the interface between input and LED string which is also referred to as Power factor correction (PFC) stage. The allowed level of harmonic currents generated by electric load is limited and regulated [9]. Normally a bulk capacitor energy storage often of electrolytic type is used in parallel with the LED string or sometimes with an inductor in series with the LEDs to reduce the ac power oscillations on the LEDs. Compared to multiple-stage counterparts, single stage topologies benefit from a lower component count. But achieving desired characteristics in power factor, THD, dimming range and output current ripple are challenging due to

fewer degrees of freedom in design. Single-stage topologies are often preferred when the variation range of one parameter such as the input voltage is narrow. A brief detail about different topologies of single stage PFCs is provided in chapter 2

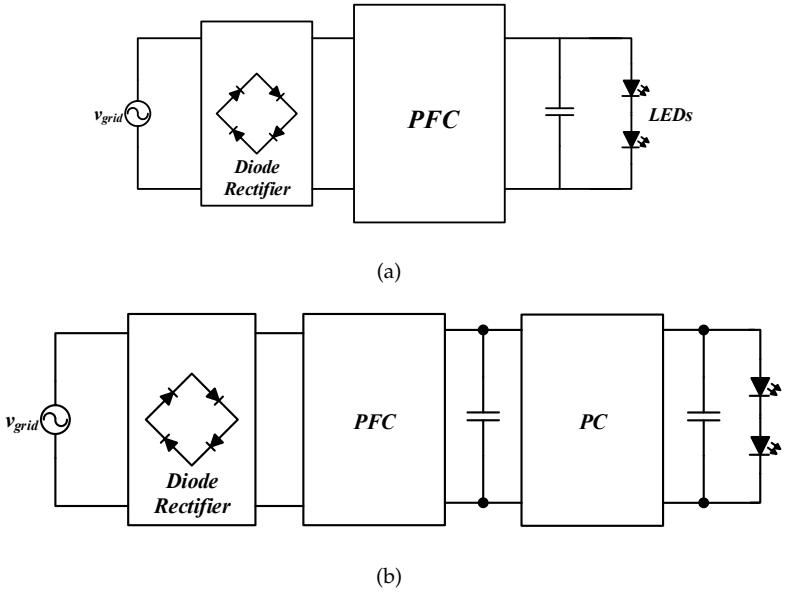


FIGURE 1.2: LED driver topologies;
(a) Single stage concept, (b) multiple-stage concept

1.2.2.2 Multiple Stage Topologies

Fig. 1.2 (b) shows the concept of multiple stage LED drivers. Single stage approach usually fails to fully comply with requirements on the power factor, THD, life span, efficiency and output current ripple. Multiple stage approaches on the other hand, can introduce more design flexibility in achieving the aforementioned performance factors.

Multiple cascaded converters forming an LED driver shown in Fig. 1.2 (b) have the sequential power flow. Reprocessing of power is an issue in multiple stage topologies that can adversely affect the efficiency. It can be either rectified with non-cascaded topologies (refer to Fig. 3.3) or with employing soft-switching. Usually the problem of handling the excess power or reprocessing power is aligned with the use of large storage energy required in the design of LED driver. Hence, different types of multiple stage topologies that facilitate reduced power processing are also used to eliminate electrolytic capacitor in the design. Chapter 3 details approaches using a variety of multiple stage topologies for power decoupling between LED driver stages.

1.3 Description of The Proposed Structure

As it has been mentioned, unsolicited harmonics and double frequency are the main issues regarding the SSL. In this thesis, LED driver topology and control scheme are proposed to rectify the aforementioned issues. Fig. 1.3 shows the proposed power circuit block diagram of our LED driver. Using the proposed power decoupling method that is explained in Chapter 3, ensures that power pulsations are drawn from the grid but a constant power is delivered to the output. v_{BUS} on the DC link of our LED driver has constant DC voltage plus an ac voltage fluctuating at twice the grid frequency. By employing phase shifted pulse width modulation in the second stage as discussed in chapter 4, the impact of pulsating current from LED driver input is minimized in the power injected to the LED strings.

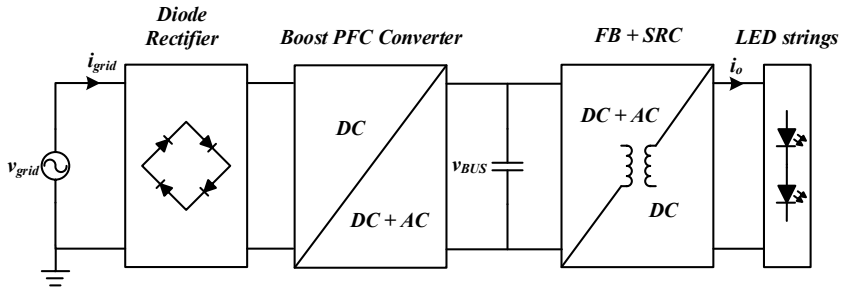


FIGURE 1.3: Power circuit block diagram of the proposed LED driver

As it has been mentioned before, as opposed to other capacitor technologies, electrolytic capacitors provide a large capacitance in small packages. Allowing large voltage swing of 25% on DC link alleviates the need for a large capacitance. In addition, controlling the average bus voltage and optimizing the value of DC link capacitor made it viable to remove electrolytic capacitor in the DC link and substitute it with a 50 μF film capacitor. Eliminating the electrolytic capacitor in turn, rectifies the mismatch between the life span of LEDs and LED drivers, boosts the reliability of the LED driver and reduces the maintenance cost.

1.4 Thesis Objective

The main objective of this thesis is to design and implement an LED driver with high efficiency and long lifetime that complies with North American codes and standards.

To achieve this goal, a multiple stage structure and new control methods are proposed. Briefly, the thesis objectives are:

1. To extend the Generalized Peak Current Control (GPCC) introduced in [11] to PFCs and SSL applications to achieve a fixed frequency in PFC converter, eliminating the unsolicited harmonics.

2. To design the Series Resonant Converter (SRC) using the Laplace based theorem (LBT) introduced in [12] to provide Zero Voltage Switching (ZVS) and delivering a constant power to the output in the allowed range of input voltage.

3. To optimally design the magnetic elements used in resonant converter and PFC output filter, minimizing the size and the resistive and eddy current losses; and

4. To verify the system design and analysis using simulations and experimental results

1.5 Thesis Outline

In chapter 2 a brief description of power conditioning and its importance in SSL is provided. It's followed by a categorization of power factor correction topologies and control schemes. Furthermore, the advantages and shortcomings associated with each topology and control scheme are reviewed.

A high frequency active PFC of boost topology is used to provide power factor correction, which has the following desired specifications: low THD, higher efficiency and reliability along with lower size, cost, and temperature susceptibility, wide range of allowable input voltage, tight current control and fast dynamic. Further through the chapter, an introduction to Generalized Peak Current Control (GPCC) is provided, the principle of operation is explained and the extension of this concept in PFC current control is detailed.

Chapter 3 reviews the power decoupling and Electrolytic capacitor-less LED drivers. As decoupling power with electrolytic capacitor significantly reduces the lifetime of LED driver, a variety of power decoupling approaches for eliminating electrolytic capacitors are reviewed and advantages and disadvantages of each approach is explained.

Furthermore, implementation of the proposed power decoupling approach is detailed and verified with experimental and simulation results.

Chapter 4 starts with providing a brief introduction to soft switching and phase shifted PWM. Further through this chapter, the series resonant converter is explained and the different modes of operation is detailed. Then a series resonant converter steady state analysis and design is presented by explaining the Laplace Based Theorem introduced in [12], followed by description of SRC waveforms and equations, linearizing the equations and applying LBT to obtain the variables describing the SRC. Calculation of design parameters are presented and simulations are provided to prove the ZVS operation is achieved throughout the operation.

Chapter 5 presents a detailed design of magnetic components. The chapter starts with an overview and the categorization of magnetic design, followed by a systematic approach to go through the design steps for saturated and non-saturated thermally limited designs. The design of resonant converter inductor and transformer is done following the non-saturated design steps. Then the design of boost inductor which falls into the category of saturated thermally limited design is done. The choice of design category is optional and it can be verified through the design steps.

Chapter 6 summarizes the contributions of the thesis and proposes other possibilities for future work.

and Finally, in Appendix, current imbalance in LED strings as an issue for SSL applications is explained. A categorization based on the practiced approaches is done and different passive and active current sharing schemes are explained. The proposed current sharing scheme is of passive type and based on charge-balance property of capacitor. The concept is to balance out the voltage difference with a DC blocking capacitor so that regardless of the different forward voltage of LEDs, the same voltage would be applied to each string in a cycle. Different modes of operation is presented and simulation results are provided to verify the analysis.

Chapter 2

Power Factor Correction

2.1 Introduction

Fig. 2.1 shows the topology of the proposed two stage LED driver formed by cascading power factor correction (PFC) and a power conversion (PC) stages. This chapter first justifies the necessity of power factor correction stage in modern LED drivers and then provides brief review of common approaches to achieve PFC. And finally, the proposed approach for PFC control is described.

2.1.1 Power conditioning: An introduction

Power factor is a measuring tool that ensures the power grid feeds the consumers with maximum efficiency. Poor utilization of the distribution system and increase in operating cost for consumers can be aftermath of using electrical or electronic devices with low power factor.

Over the past decade, the ever-growing use of electronic devices introduced new challenges for the power suppliers in the sense of efficiency and quality of the delivered power. Electrical lighting takes a big share of up to 17.5% of the whole electricity consumed in the world [10]. Having considered this large amount of energy consumption gradually tilting towards the Solid State Lighting technologies, the negative effect of the LED-Based lighting on power factor becomes more and more concerning for the utilities.

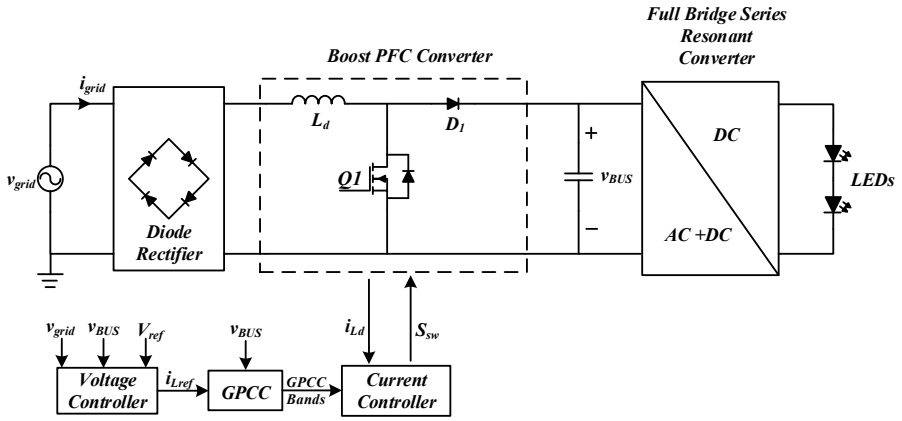


FIGURE 2.1: Boost power factor correction in Two stage LED drive

The disruption of power quality-sensitive services and the adverse effect of power electronics devices on power factor led to the introduction of $EN61000-3-2$ standard that limits the amount of allowed harmonics injected to the power grid and also maintains the power factor within an acceptable level. To comply with the aforementioned standard, all the loads that consume more than $75W$ should utilize power factor correction circuitry that ensures the limited allowed harmonics and the sufficient power factor of more than 90% [10].

2.2 Power Factor Correction Approaches

There are several approaches to maintain the power factor and THD within the allowable range to increase the capacity of power system and also to decrease the consumer's utility bill [13]. A common approach is to shape the input current waveform for the whole electronic device, to ideally be seen as a resistive load from utility's point of view.

Reviewing several approaches that have been developed for power factor correction (PFC), a categorization on PFC topologies and control schemes has been conducted and results presented in Fig. 2.2. According to Fig. 2.2, PFC circuits can be divided into two main category of active and passive PFCs. A brief description of these main categories along with different power factor correction approaches corresponding to each category will be detailed and the pros and cons associated with each approach will be scrutinized.

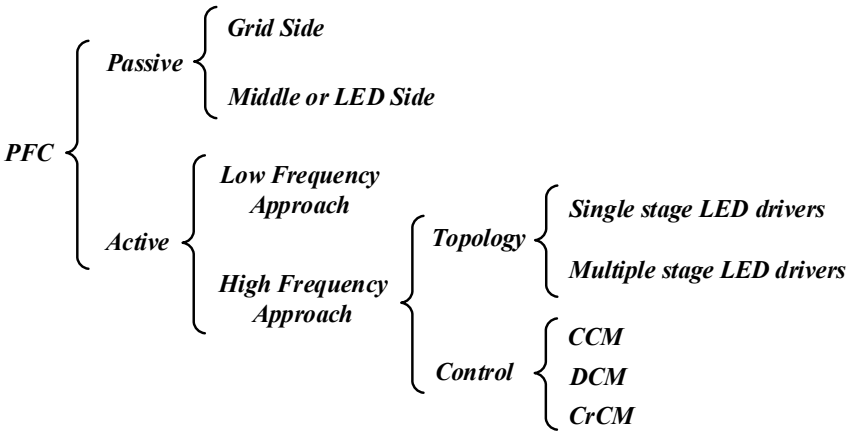


FIGURE 2.2: A category on PFC topologies and control

2.2.1 Passive Approaches

2.2.1.1 Passive grid side PFC

1. AC side inductor: As shown in the Fig. 2.3, PFC consists of a rectifier with AC side inductor. Placing an inductor in series between power grid input voltage and diode bridge rectifier would make a low pass filter (LPF). The LPF would filter out the high frequency harmonics and current spikes. According to [14], the highest PF achievable by this method is only 76% and yet the approach needs a bulky inductor.

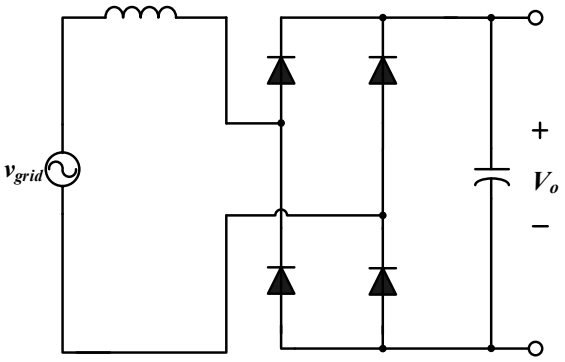


FIGURE 2.3: Rectifier with AC side inductor

2. AC side resonant structures: Fig. 2.4(a) and 2.4(b) show series resonant bandpass and parallel resonant bandstop filter respectively. Band pass series resonant network is placed at the AC side of rectifying bridge and can be tuned at the line frequency. Band stop parallel resonant network can also be tuned to attenuate third harmonics. Although the study in [15] shows promising PF range of more

than 91%, the need for bulky resonant elements and susceptibility to changes of the element values is a big shortcoming associated with this approach.

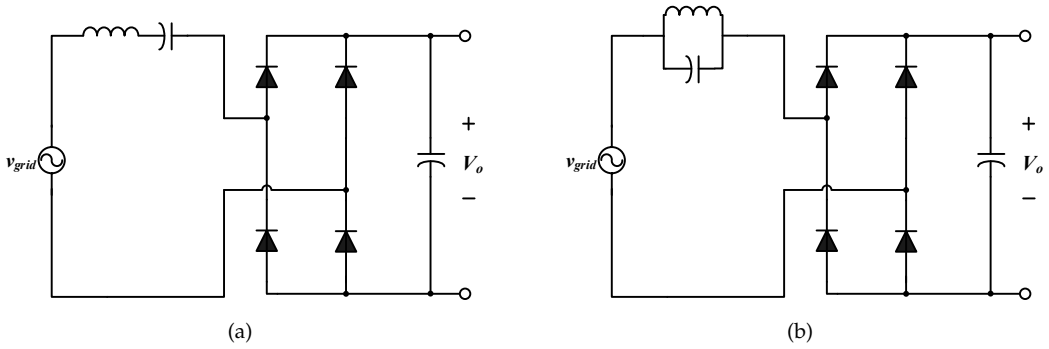


FIGURE 2.4: Rectifier with resonant structure PFC
(a) Series resonant bandpass filter PFC, (b) Parallel resonant band-stop filter PFC

2.2.1.2 Passive middle and LED side PFC

1. Rectifier with DC side inductor: Fig. 2.5 shows the rectifier with DC side inductor. The steady state performance of this topology is somewhat identical to the AC-inductor power factor correction approach. The same 76% is reported in [15] to be the highest achievable PF with this approach.

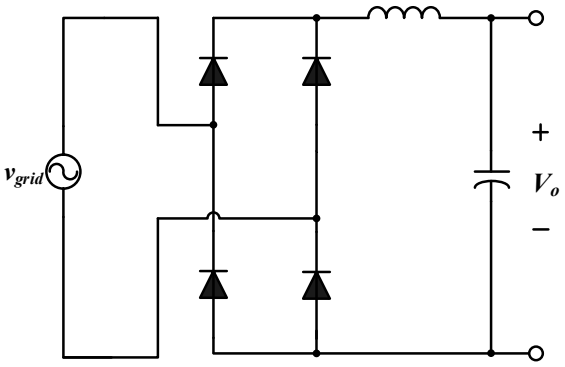


FIGURE 2.5: Rectifier with DC side inductor

2. Inductor-Capacitor-Diode (LCD) PFC Circuit: LCD PFC topology is shown in Fig. 2.6. This approach benefits from using only small values for the reactive components. Although alleged capability of utilizing elements with smaller size is the superiority of this approach, the limited surface area of the small electrolytic capacitors will make them prone to failure under heavy current ripples [16].

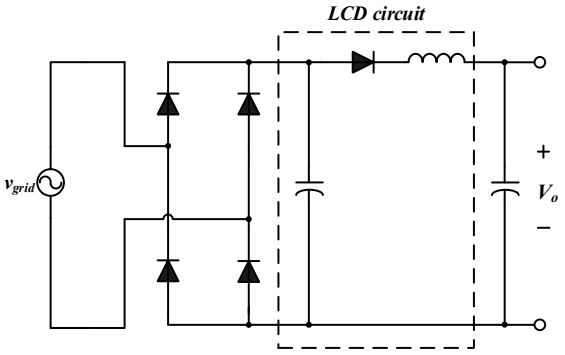


FIGURE 2.6: LCD PFC

3. Valley-Fill circuits:

   This form of rectification would be useful for the low power applications that allow a high amount of ripple voltage on the output of the PFC. As much of a limitation factor those criteria may seem to be, allowing large fluctuations of the voltage to be compensated in the second stage is a widely practiced approach to eliminate electrolytic capacitors in the design of LED drivers.

   As shown in the Fig. 2.7, in the beginning of a cycle, current goes through diagonal diodes of the diode rectifier and middle diode of VF circuit to charge two capacitors in valley-fill circuit to approximately half of the peak line voltage for each capacitor. When the line voltage starts to fall below the peak value, output voltage follows the input voltage until it reaches the half value of peak line voltage. At this point, two capacitors starts to discharge into output via diodes in VF circuit legs to prevent the output voltage to fall below half of the peak line voltage. Inrush current, high crest factor, and low THD is the main disadvantage of this approach.

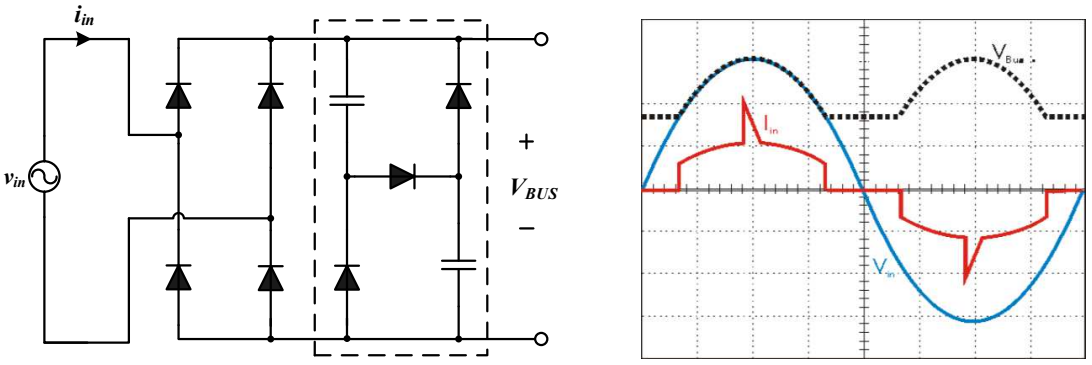


FIGURE 2.7: Valley-fill PFC topology and V-I waveforms[2]

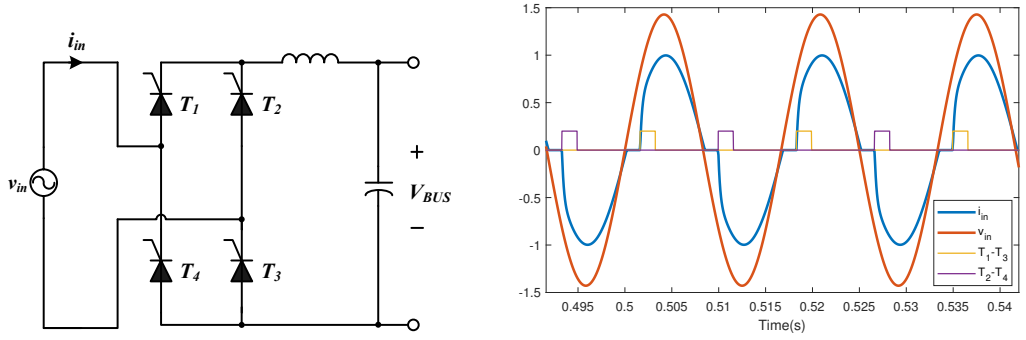
In light of the above, several aspects would make passive power factor correction an attractive proposition. Ease of implementation, simplicity of the design and absence of unsolicited power loss associated with switching actions are the most important ones. Yet, lots of disadvantages such as excessive size of the filter components, cost of reactive materials, lack of efficiency, universal input voltage operation issues, and lack of controllability shifts the focus point toward the active approaches.

2.2.2 Active Approaches

Active PFC approaches use switching actions to shape the input current. From the topology standpoint, active PFCs can come in one and two stage category while from the control perspective, active PFCs can be devided into Low frequency and high frequency approaches.

2.2.2.1 Low Frequency Active Approaches

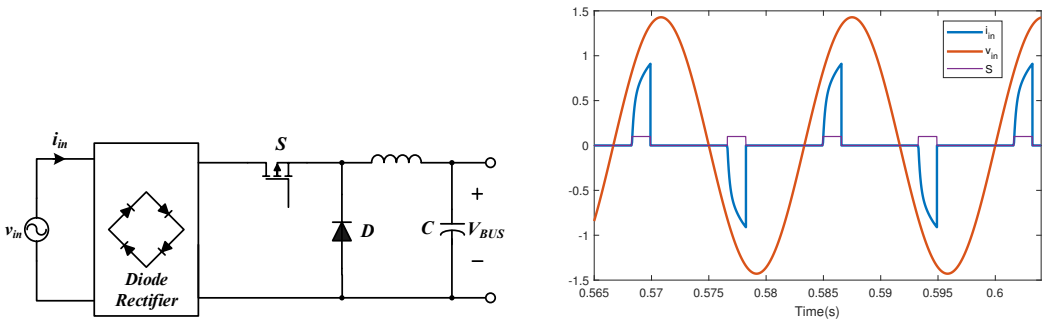
Low frequency active approaches have been reported in many literatures. In [17], authors proposed an active power factor correction approach similar to the passive DC side inductor PFC topology as shown in Fig. 2.5. Yet, diodes in bridge rectifier has been replaced with thyristors. Controllable output voltage and reliability have been achieved but the technique suffers from bulky reactive components and slow dynamic response for the output voltage regulation [15].



(a) (b)

FIGURE 2.8: Low frequency active PFC
(a) Thyristor rectifier with DC side inductor and Phase control, (b) firing angle α

Fig. 2.9 shows another attempt with achieving power factor correction though a buck converter operating in low frequency. The harmonic content of the line current is large and the required inductance is bulky, yet with higher switching frequency, current harmonics can be reduced [15].



(a) (b)

FIGURE 2.9: Low frequency active PFC
(a) Buck converter, (b) control signal indicating one commutation in each half cycle

Low switching frequency will allow for the control of output voltage to certain extent. EMI noise and switching losses that are associated with high frequency switching are also absent [15]. These make the low frequency approaches desirable. However, this approach is not suitable for the applications with tight output control. As the slow dynamic of the voltage regulation doesn't allow for the fast response. The need for bulky reactive elements is another issue introduced by such approaches.

2.2.2.2 High Frequency Active Approaches

High frequency approaches are based on performing the switching action within a cycle with substantially higher rate than the main grid's frequency. These PFC approaches would introduce fast dynamic response to changes in the output voltage, enhancing the circuit with tighter and more accurate control and also reduce the magnetic elements size.

From the topology standpoint, the main distinction comes with single stage and multiple stage categories.

1. PFC in Single stage LED drivers: As shown in Fig. 2.10(a), single stage topologies integrate PFC and power converter (PC) in one stage. It is characterized by lower component count. But at the same time, designing LED driver for high quality of performance doing several tasks like achieving high power factor, low THD, tight output current control, and possibly dimming feature would need more degrees of freedom that single stage topologies would offer.

   Sharing the active switches and commutation network between two separate stages is widely practiced to make integrated topologies. The concept of integrated topologies are shown in Fig. 2.10(b). Lower component count is the advantage of integrated approach. But, usually the voltage stress on the shared switch increases in these topologies and the approach suffers from relatively lower efficiency. Fig. 2.10 (c) shows a single-stage driver based on the integration of a bcuk-boost PFC and flyback. Utilizing the Q_1 switch for both circuit made the two stage circuit turn into one integrated stage.

2. PFC in Multi-stage LED drivers: Multi-stage LED drivers have been developed to overcome the lack of design freedom in single stage LED drivers. Complying with THD, current ripple, and power factor standards as well as longer lifetime and efficiency can all be done with more design flexibility with multistage LED drivers. As a result, the focus has been shifted to design PFC stages tuned to perform optimally achieving some of the aforementioned objectives, and the power conversion stage on the other hand, to perform other tasks with more design freedom.

   As shown in Fig. 3.3, multistage topologies can come in independent cascade or non-cascaded structures. Non-cascaded topologies feature more power processing efficiency as the major part of the power delivered to the output is only processed once. This feature in turn, facilitates the use of non-electrolytic type capacitors which will be detailed further chapter 3.

Various topologies providing active and passive Power Factor Correction have been reviewed. Within next sections of this chapter, control methods corresponding to high frequency approaches are reviewed and the choice of PFC topology and control method is justified.

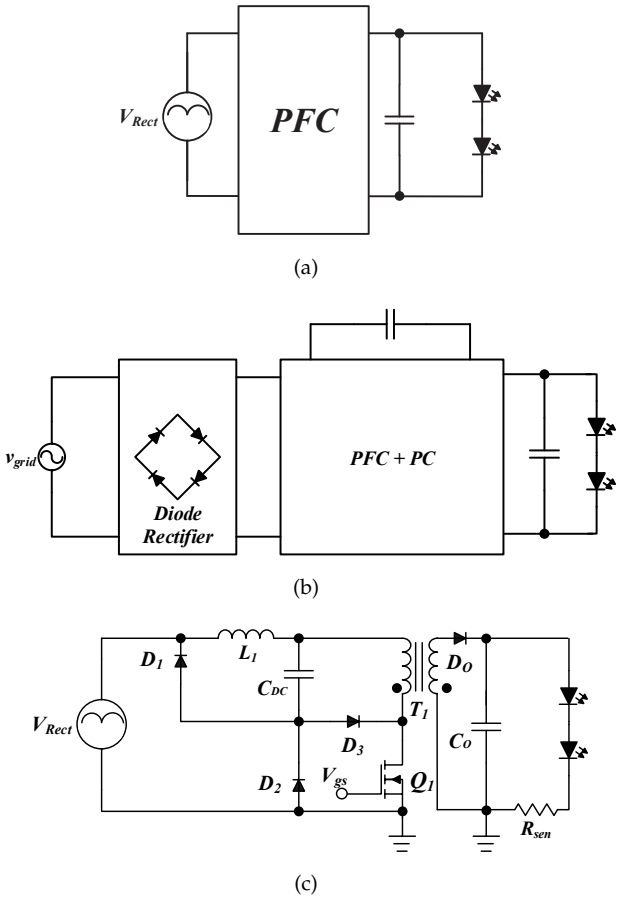


FIGURE 2.10: Single stage PFC topologies;
(a) Single stage PFC concept, (b) integrated-stage PFC concept, (c) integrated boost-flyback PFC schematic

2.2.3 High frequency Approach Control modes

2.2.3.1 CCM control

Continues conduction mode (CCM) is one of the most popular approaches to control high frequency active power factor correction stage. Having the low input current ripple that eases the output filter design and lowers the stress on semiconductor switches can be one of the most important advantages coming with this approach. However, CCM approach doesn't allow for simple soft switching action of the power switches and it requires a comparably large inductance value. This approach is depicted in Fig. 2.11(a).

2.2.3.2 DCM control

Sometimes the limited amount of power required by the load necessitates the inductor current to fall to zero during a portion of switching cycle. Discontinues Conduction Mode control shown in Fig. 2.11(b) offers more stability and reduces the inductance value in comparison with CCM approach. Facilitating fixed frequency switching operation in DCM control can also reduce EMI noises. As opposed to CCM approach that cannot provide any means of soft switching, DCM design can also provide ZCS at turn ON switching instances.

2.2.3.3 CrCM control

Fig. 2.11(c) depicts the critical conduction current control mode. Critical Conduction Mode (CrCM) keeps the controlled current between continues and discontinues conduction. The general idea for implementation of Critical Conduction Mode control is, for the ideal sinusoidal waveform at any given time, to keep the value of average current exactly half of the peak current value.

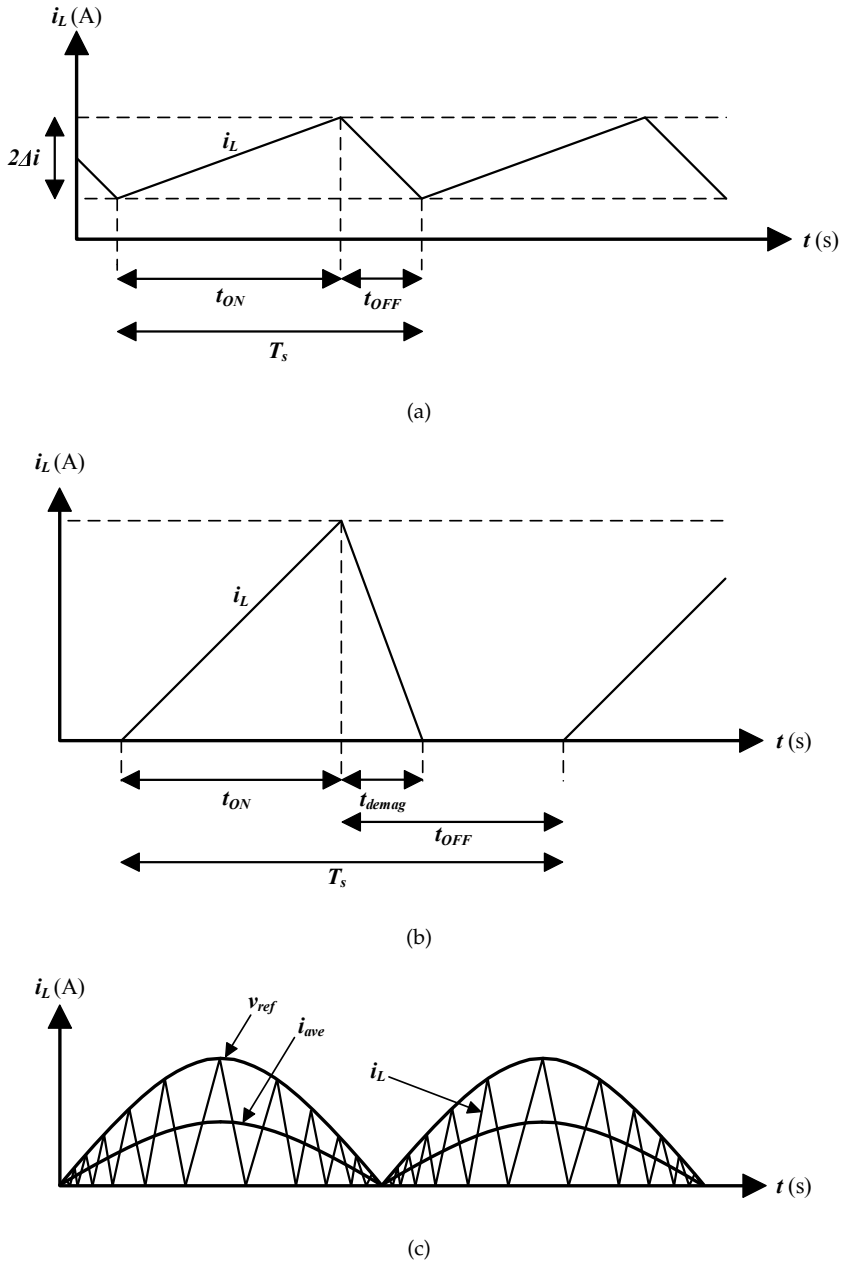


FIGURE 2.11: Current control methods;
(a) CCM, (b) DCM , (c) CrCM

In this mode of operation, the inductor currents ramps up until it reaches the reference signal Band. Then the switch will turn off and the inductor current will decrease until it touches the zero value. Although this type of current control is popular for lighting applications, it suffers from the variable switching frequency which will increase the THD and also makes it harder to design filters to mitigate the harmonics. The switching frequency is the lowest at the peak inductor current and it will reach the highest rate at the zero crossing of the inductor current.

2.3 Choosing PFC Topology

Various topologies to achieve PFC along with main current control schemes have been reviewed and their advantage and disadvantage have been scrutinized. As a result, a choice of PFC stage topology and control has been made and presented below;
Active category has been chosen over the passive type to provide:

- Lower injection of current harmonics into the grid due to the quasi-sinusoidal current waveform
- higher efficiency and reliability along with lower size, cost, and temperature susceptibility
- wide range of allowable input voltage, tight current control and fast dynamic

High frequency multi-stage topology has been chosen over the single stage to provide:

- Design flexibility to optimally achieve higher PF, Lower THD, and reduced EMI noises.
- Allowing for elimination of Electrolytic capacitor and matching lifespan of LED and LED driver

In the next few chapters we justify the choice for PFC topology and control approach.

2.3.1 LED driver PFC topology

Fig. 2.1 shows a boost converter that has been chosen in this thesis to perform power factor correction in our LED driver topology. The boost topology is the most commonly used structure for the PFC stage. As opposed to Buck converter that has crossover distortions because of limitation in the operating voltage (Input voltage must be larger than the output), the boost converter can operate throughout the line cycle. In addition, the discontinuity of the input current along with significant high frequency distortions that is introduced with Buck and Buck-boost converters, is absent in the boost topology.

Considering the ease of design and the above favorite qualities, boost converter has been chosen for the PFC stage.

2.3.2 LED driver PFC control

Main approaches for current control have been reviewed. Researchers in [11] introduced a novel Generalized Peak Current Control (GPCC) technique for DC-AC Converters that can implement all the aforementioned control methods (CCM - DCM - CrCM). GPCC utilizes current bands of a special shape to maintain the fixed switching frequency while the current is controlled within the bands. In this thesis we extend the method in [11] for PFC circuits. As it will be further detailed through the section, at the zero crossing area of reference signal, when CrCM and CCM suffer from variable (Higher) frequency, the control mode goes to DCM. And further on, towards the peak point of the reference signal in the half cycle, the mode can change to CCM or CrCM with regard to the shape of GPCC constructed band.

Remainder of the chapter is dedicated to describe the extension of GPCC for PFC control approach. Further through, the implementation of GPCC on boost PFC and the design procedure is detailed.

2.4 PFC Using the Proposed GPCC Control

Figure 2.12 depicts the control block diagram based on GPCC strategy to achieve power factor correction and inductor current control. Multiple closed loops consisting of an inner current and an outer voltage control are utilized to achieve the aforementioned objectives.

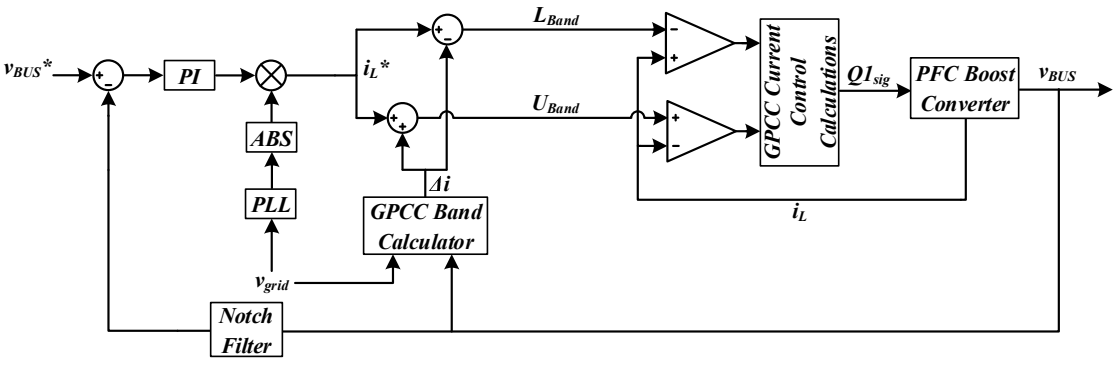


FIGURE 2.12: PFC control diagram

The control mechanism is simple and straightforward. The idea is to employ the general peak current control (GPCC) method to switch the boost converter in a way, that instead of a constant output voltage, input current is shaped into a sinusoidal waveform in phase with input voltage while the switching frequency is kept constant. For this matter, the DC link voltage on the boost converter's output is measured and used to generate the GPCC band in real time (The process in which GPCC bands is created and used to control the inductor current will be described further in this chapter).

Reference current for the boost inductor, i_L^*, is generated using the grid voltage. Grid voltage is synthesized into its phase and magnitude. Then it gets scaled into a desired measure and multiplied by the PI controller error. This way, the reference current for boost inductor is constructed in phase with input voltage to control the DC link voltage and perform power factor correction.

The constructed GPCC band, Δi, then will be added to and deducted from the reference current, i_L^*, to generated the upper and lower bands. These bands will be compared to the inductor actual voltage, i_L, and the switching signals would be generated.

2.4.0.1 GPCC: Overview

Introducing an upper and lower band to control the current within a desired limit has been widely used through Hysteresis control scheme. Hysteresis approach facilitates current control with bands in which current is tightly controlled within, independent of any sort of external disturbances and/or DC biases in the input voltage. Adding this feature with a good large signal response and stability that comes with it, hysteresis current control comes across as an interesting scheme. However, one noticeable disadvantage is the vast range of undesirable very high frequency harmonics that are created by imposing the switching frequency to vary over a fundamental cycle while keeping the current within the bands. The intrusive harmonics that are introduced using this scheme, would make it hard for the designer to optimally design ac and EMI filters.

To rectify the unsolicited harmonic issue, modified peak current control schemes are introduced to generate the output at fixed switching frequency. In this control scheme, unlike the hysteresis approach, only one band is compared to the minimum or maximum of the current to generate switching signal. A clock signal will complement the

switching command in each switching cycle. Although a fixed switching frequency is obtained this way, features like zero tracking error and inherent current limiting are lost [11] and high peak current are generated (at least twice the average).

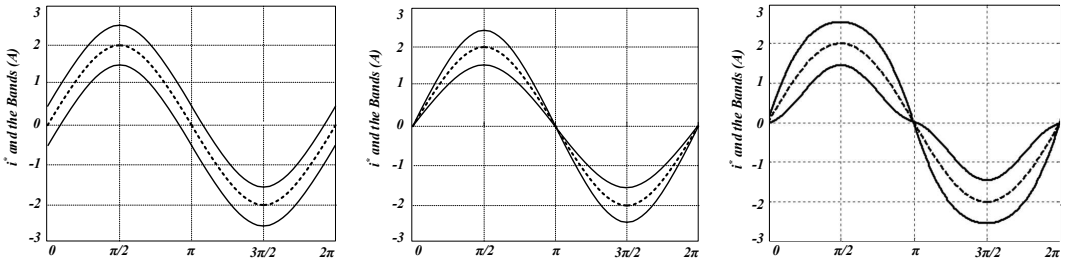
Enumerating all different aspects of hysteresis and peak current control schemes, it is worth noticing that none of these approaches would provide a meaningful systematic modulation for the controlled waveform and hence, harmonics spectrum and converter's performance is not as predictable as when PWM schemes are utilized [11].

The Fixed-Switching GPCC is in fact a peak current control scheme which mimics the behavior of PWM techniques through adapting bands of special forms. Current is tightly controlled within the constructed bands. Bands are specifically calculated to have the same shape of PWM driven converter's current envelopes. Hence, elimination of electromagnetic interference and unwanted harmonics through achieving fixed switching frequency will be obtained.

2.4.0.2 GPCC: Principle of Operation

In this project, Generalized Peak Current Control (GPCC) scheme is extended to control the PFC stage current. This approach will feature all the advantages of peak current controllers such as simplicity, fast transient, good real-time control and dynamic response. In addition, zero steady state error and disturbance rejection which are the highlight of hysteresis schemes are obtained. GPCC approach also serves as a bridge, providing a meaningful link to the known PWM techniques which in turn, can be conducive to enhance the peak current control and hysteresis control with all the advancements and features that are attributed to various PWM approaches.

The principle of operation for fixed switching generalized peak current control is to utilize some bands in which the current will be controlled within. The shape of the bands are constructed to achieve fixed switching frequency while utilizing the bands to mimic pwm behavior. Using the traditional fixed band and sine bands widely practiced in hysteresis techniques would lead to generating a wide spectrum of unwanted harmonics.



(a) (b) (c)

FIGURE 2.13: Comparison between GPCC bands and conventional methods
(a) Conventional Fixed Bands, (b) Conventional Sine Bands, (c) GPCC Bands

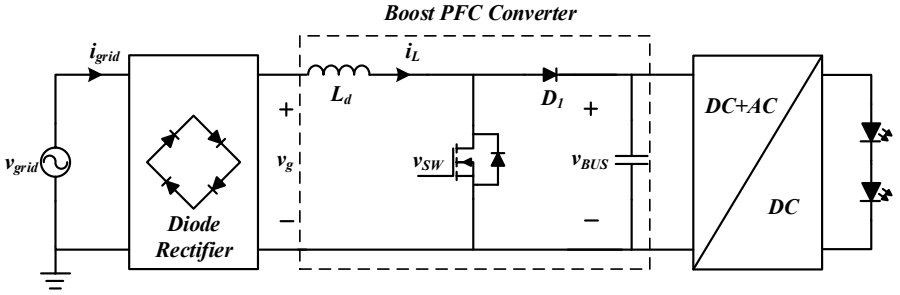


FIGURE 2.14: Step up PFC converter

For the boost converter shown in the Fig. 2.14, we assume a PWM sinusoidal control is used to shape the input current. Boost PFC's output voltage v_{BUS} , inductor current i_L and modulation index m for pwm switching are shown in the Fig. 2.15.

In order to calculate the desired bands, we need some information about the *on* time of and *off* time intervals during a switching cycle. To determine the switching *on* time, the average output voltage of the converter is calculated during one period T_s and denoted by $\overline{v_{SW}}$, and is calculated as follows:

$$\overline{v_{SW}} = \frac{1}{T_s} \int_{t\text{-}T_s}^{t} v_{SW}(\tau)\, d(\tau) \tag{2.1}$$

For the calculation of t_{on}, only the current ripples are taken into account and other parameters are assumed to be constant. This is due to the fact that the effective switching frequency $\frac{1}{T}$, is much higher than the fundamental frequency.

The average output voltage $\overline{v_{SW}}$, and consequently the switching *on* time, t_{on}, can be determined as below:

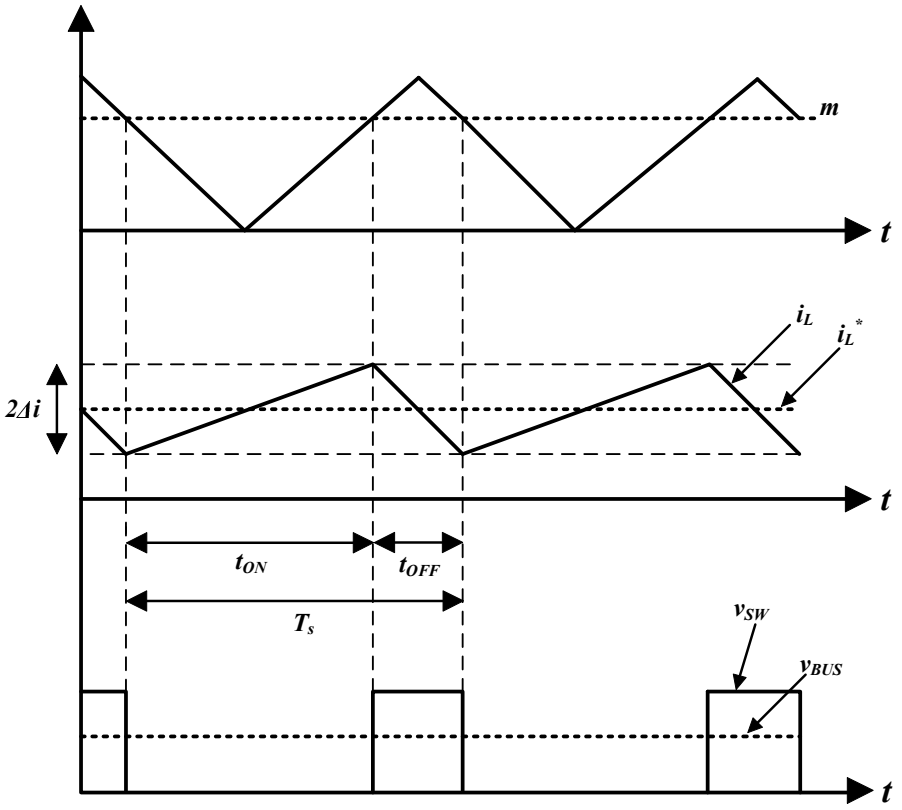


FIGURE 2.15: Step up PFC converter: carrier signal, inductor current and output voltage

$$\overline{v_{SW}} = \frac{1}{T}\left((v_{SW}^{on})t_{on} + (v_{SW}^{off})(T - t_{on})\right) \tag{2.2}$$

$$t_{on} = T\frac{\overline{v_{SW}} - v_{SW}^{off}}{v_{SW}^{on} - v_{SW}^{off}} = T\frac{v_{SW}^{off} - \overline{v_{SW}}}{v_{SW}^{off}} = mT \tag{2.3}$$

According to volt-second rule, The average voltage $\overline{v_L}$ on inductor during a switching period is zero. Therefore, switching *on* time, t_{on}, can be determined as below:

$$\overline{v_L} = \frac{1}{T}\left((v_g)t_{on} + (v_g - v_{BUS})(T - t_{on})\right) \tag{2.4}$$

$$t_{on} = T\frac{v_{BUS} - v_g}{v_{BUS}} = dT \tag{2.5}$$

Symbols

Voltage across the filter inductor is $v = L\frac{\Delta i}{\Delta t}$. Considering the inductor current waveform during t_{on} on Fig. 2.15, the current band will be calculated as below:

$$2\Delta i = \frac{1}{L} v_g t_{on} \tag{2.6}$$

Substituting the parameters from equation 2.5 into the above equation, current bands are calculated as follows:

$$\Delta i = \frac{T}{2L} \frac{(v_g)(v_{BUS} - v_g)}{v_{BUS}} \tag{2.7}$$

$$UpperBand = i^* + \Delta i$$

$$LowerBand = i^* - \Delta i$$

Calculated Δi is used to form the upper and lower bands in which the current is controlled within. The bands are used by a peak current controller and the shape of the bands are similar to the current envelope obtained from the PWM driven converter. Hence, it facilitates achieving the fixed switching frequency.

The circuit diagram of the PFC stage of LED driver is depicted in Fig. 2.14. Assuming the only switch in the PFC stage is controlled by a bipolar PWM scheme, waveforms are depicted in the Fig. 2.15.

The derived equation 2.7 is in fact the peak current envelope when a bipolar PWM scheme is applied to the converter's switch. Hence, utilizing the equation for obtaining the bands and controlling the inductor current within the bands will result in achieving fixed frequency.

Fig. 2.16 shows a random half cycle of the inductor reference current with the constructed upper and lower band. As it can be construed from the figure, at the both end of the half cycle where zero crossing instances of reference current happens, DCM control mode is applied with flexible off time for the switch to keep the frequency constant. The mechanism for changing the control modes is detailed in another section.

The DCM control changes to CCM for the remainder of the half cycle. As a result, Switching frequency over a fundamental cycle remains fixed and compared it to the traditional sinusoidal or fixed bands, the EMI noises and unwanted frequency generation is prevented by a considerable extent.

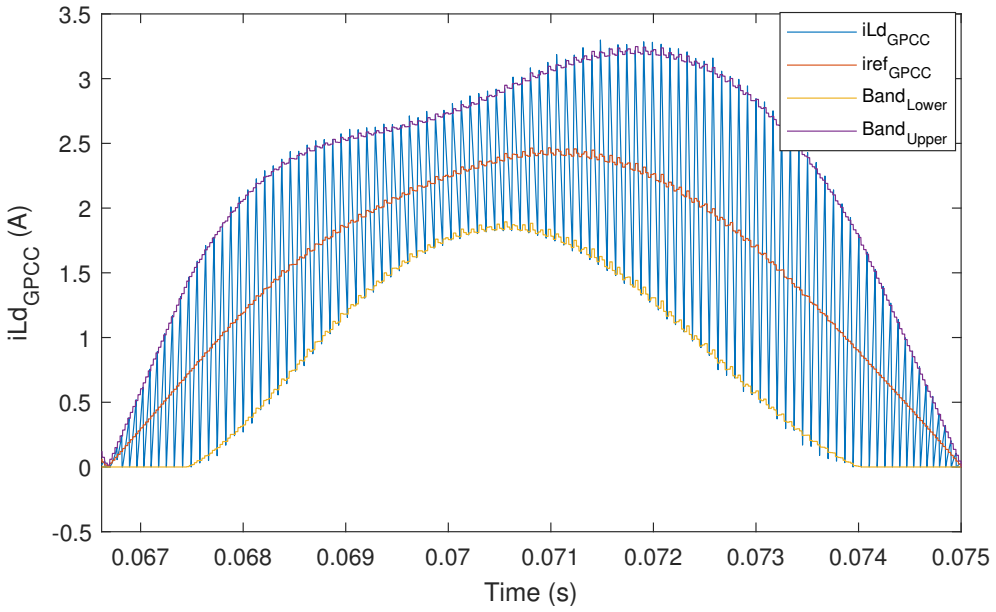


FIGURE 2.16: PFC inductor current based on GPCC control method

2.4.1 DCM Mode for Unidirectional Converters

As it was mentioned, one advantage of using GPCC control is the adaptive bands that are shaped in a way to keep the frequency constant throughout a cycle. For this matter, upper and lower bands are constructed when the Δi calculated from the equation 2.7 is added to and deducted from reference current signal respectively.

According to equation 2.7, the lower band may have a negative value in sections of the half cycle. Having a negative value for the lower band necessitates the use of a bidirectional converter to allow the negative values of the current. However, when the converter is unidirectional, current cannot be negative.

A possible solution would be to equate the lower band to zero when it has a negative value. In this case, the value for the upper band has to change accordingly to keep the average current unchanged. However, the deviation from the original value of the band would lead to a deviation in switching frequency. Because the switching turn on instance would happen when inductor's current meets the newly "held to zero" band instead of the original negative band. As a result, to keep the frequency constant, there must be a delay time when performing the switching action in order to mimic the time it takes for a "hypothetically negative current" to meet the band of negative value.

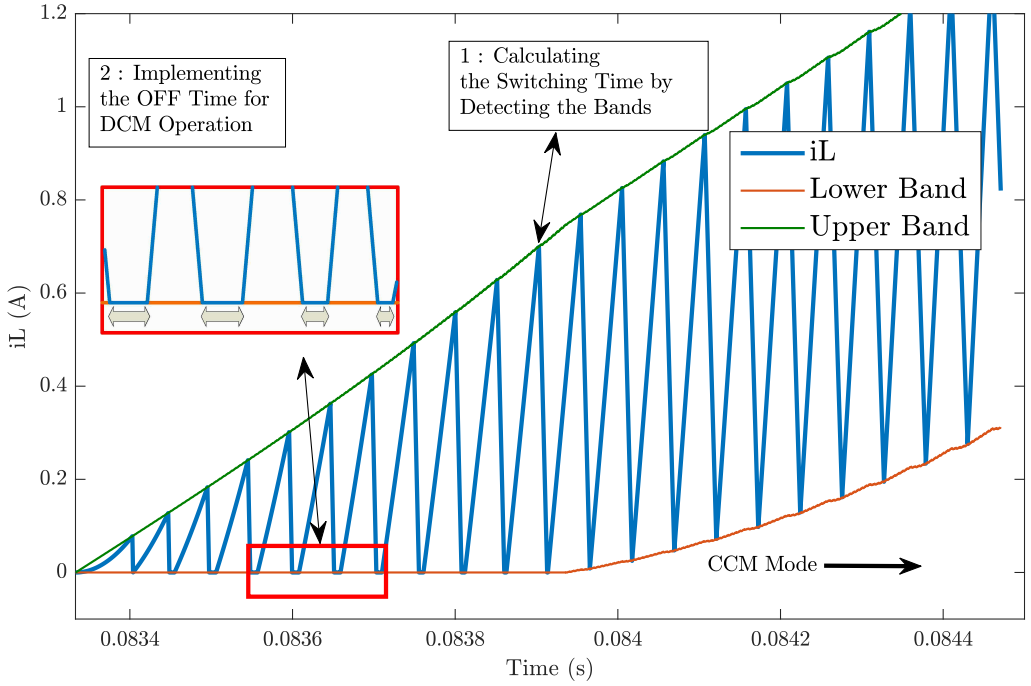


FIGURE 2.17: Band Detection and DCM OFF Time Calculation

Holding the inductor current on zero value for a calculated amount of time would transition the converter's mode of operation into DCM. Logic circuit in Fig. 2.18 has been designed to detect the DCM conditions and to hold the current value in order for keeping the frequency constant.

Fig. 2.17 shows the different modes of GPCC operation. As it can be seen, from the beginning of a half cycle, converter operates in DCM mode. This is mainly due to the fact that switching instance shouldn't happen instantly after the inductor current meets the "held to zero" lower band and there should be a delay to facilitate achieving constant frequency. Taking a closer look at the generated delay, it is clear that the time delay in which the inductor current is held at zero is variable. In Fig. 2.18, the part where is marked as section "A" detects the switching instances by comparing the value for inductor current with lower and upper bands. Section "B" on the other hand, detects the DCM conditions and applies the amount of time delay to maintain the fixed switching frequency accordingly.

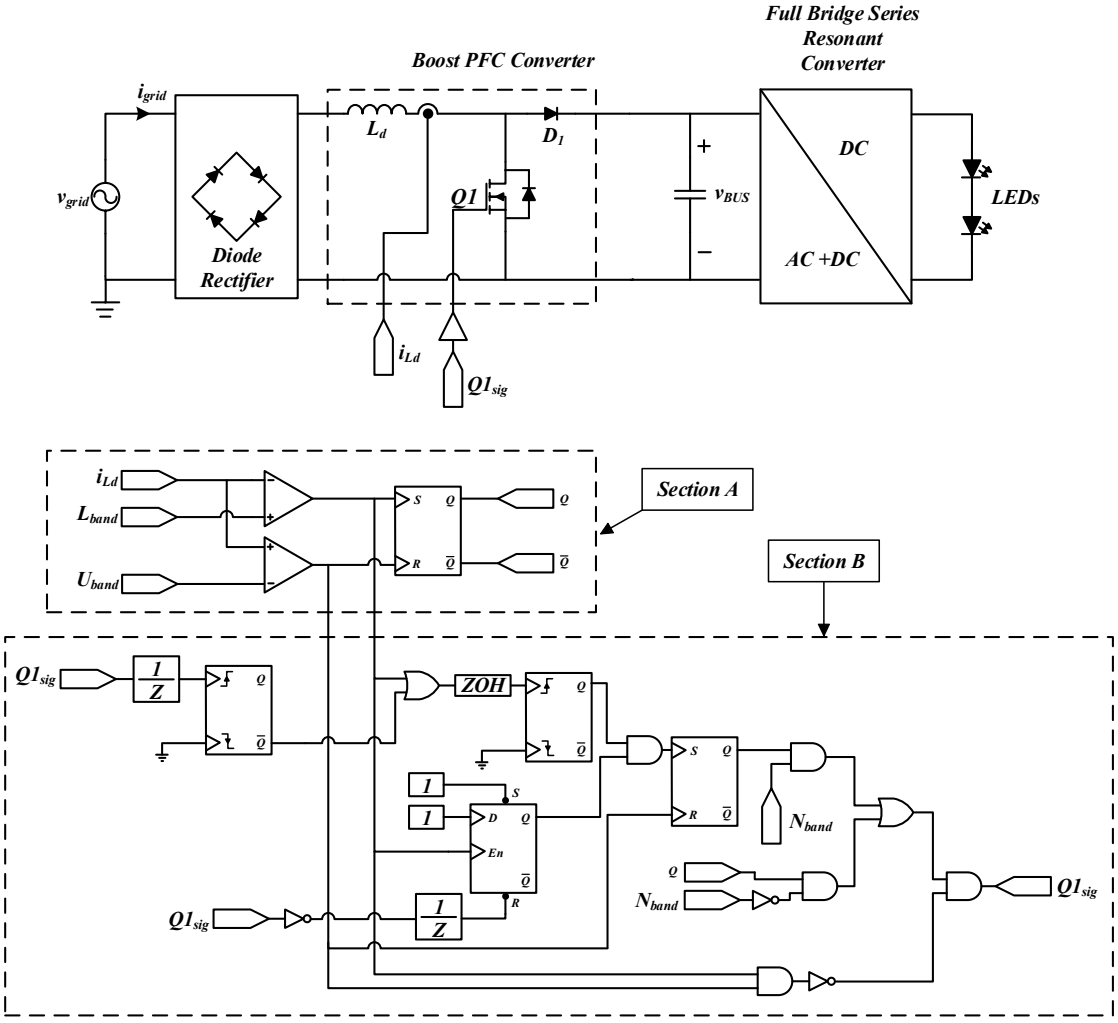


FIGURE 2.18: GPCC logic circuit

2.5 Simulation and Experimental Results

As shown in the Fig. 2.16, switching frequency is fixed throughout the cycle. For unidirectional PFC topologies that cannot facilitate the flow of current in both directions (and hence, the inductor current cannot fall below zero), a delay time in switching is implemented to keep the frequency constant. Fig. 2.17 shows the implemented switching time delay.

As shown in equation 2.7, the shape of the constructed bands are dependent to the value of inductor, L. Therefore, having a larger inductance will make the Δi smaller and the bands tighter. On the contrary, a smaller inductance is expected to make the bands wider. Fig. 2.19 shows the different GPCC bands corresponding to the relevant boost inductor value. Experimental results of GPCC approach for PFC stage have been

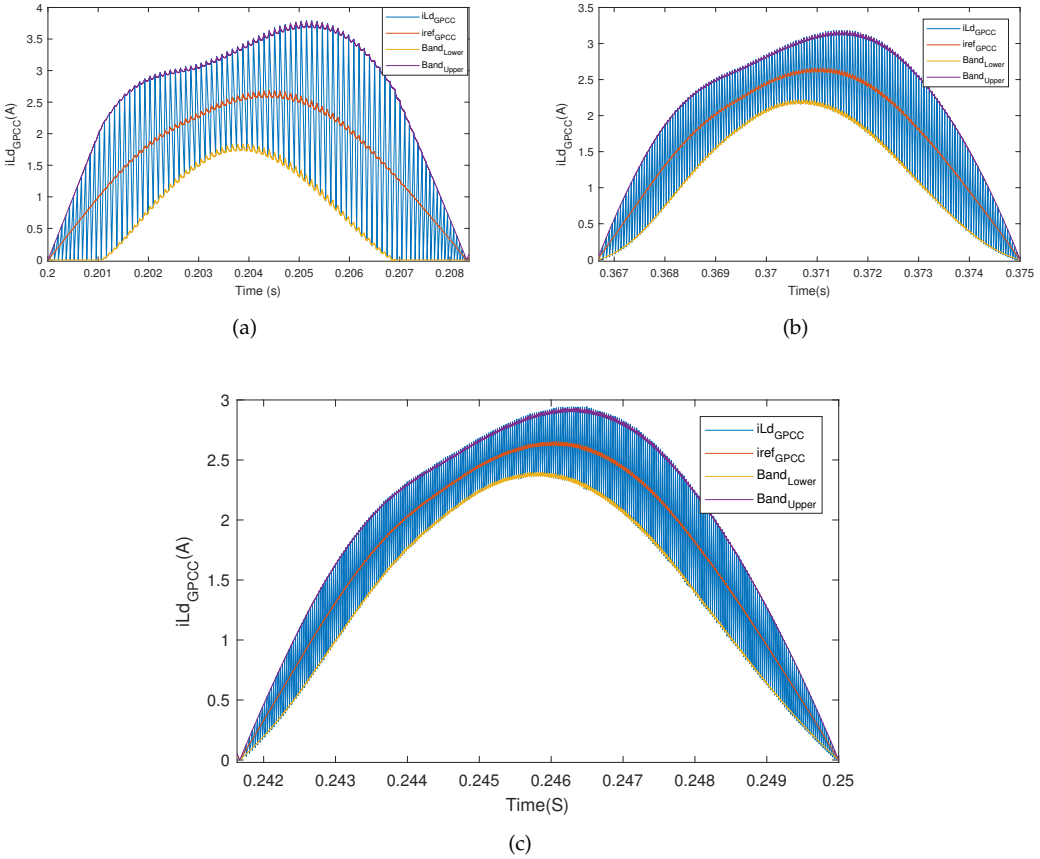
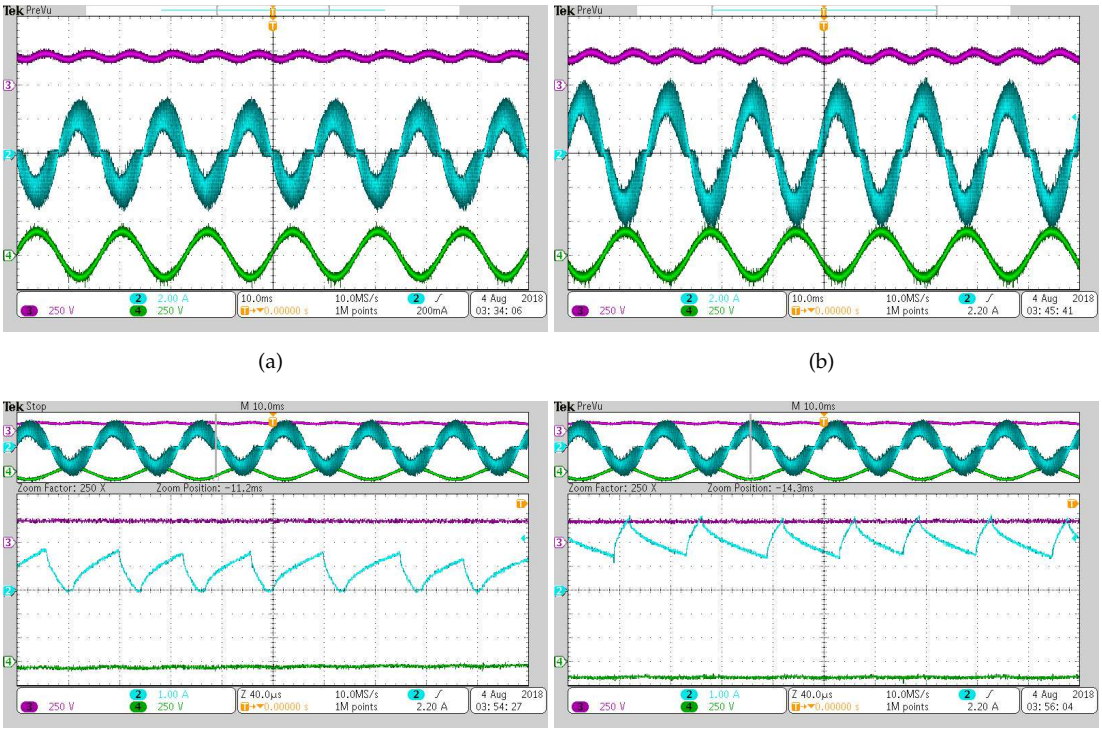


FIGURE 2.19: GPCC constructed Bands corresponding to (a) $i_{Ld} = 1\ mH$, (b) $i_{Ld} = 2\ mH$, (c) $i_{Ld} = 3\ mH$

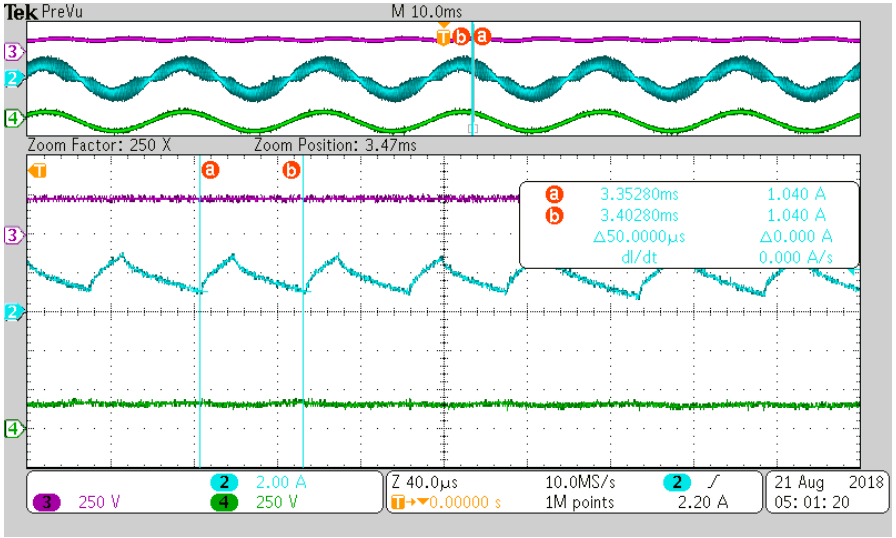
shown in Fig. 2.20. As shown in Fig. 2.20(a) the input current and voltage are in phase (current probe was reversely connected!) and the peak current is 2 A, Fig. 2.20(b) shows the same in-phase voltage and current with 3 A peak current. A closer look into operation of boost converter under DCM and CCM mode is provided in Fig. 2.20(c) and Fig. 2.20(d), respectively. As it's shown in current waveform in Fig. 2.20(c) (channel 2), a delay time is implemented to hold the current to zero for a portion of switching cycle. Switching period in DCM and CCM conditions is measured to demonstrate achieving a fixed frequency. As shown in Fig. 2.21(a) and (b), switching frequency is fixed on 20 kHz for both modes. A dynamic test is also carried on in which the reference current jumps from 2 A to 3 A during the operation. Fig. 2.21(c) shows that after the change in reference current value, GPCC bands are constructed and current is controlled within the bands immediately to follow the new value for reference current.



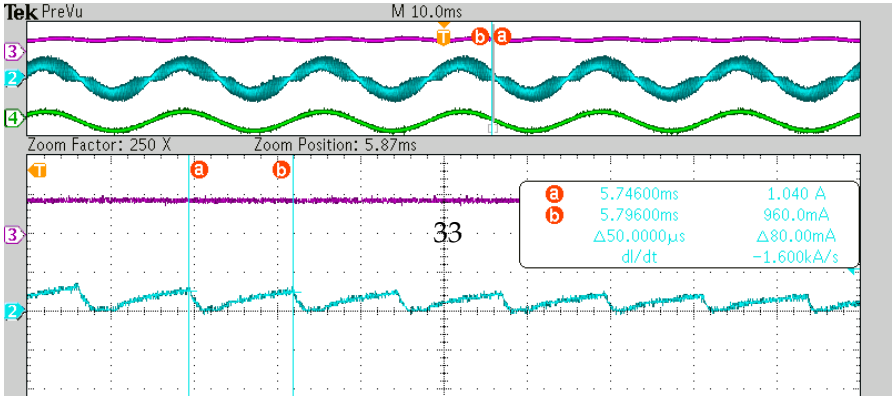
(a) (b)

(c) (d)

FIGURE 2.20: GPCC controlled Power Factor Correction Stage waveforms are output voltage, input current, and input voltage:
(a) GPCC PFC with 2 *A* peak current, (b) GPCC PFC with 3 *A* peak current, (c) DCM operation close-up, (d) CCM operation close-up (c)



(a)



2.6 Summary

This chapter first gives a brief description about power conditioning and how LED based lighting can cause power quality issues for utilities. Subsequently, the corresponding standards and regulations imposed by industry to improve power quality has been introduced. Further through the chapter, active and passive topologies providing PFC have been reviewed and control schemes within high frequency active methods have been described. After a brief analysis of advantage and disadvantages of each approach, the choice for power factor correction stage has been made.

Having a high susceptibility to temperature, large size, high THD, and low efficiency shifts the focus toward the active PFC approaches and within active PFC topologies, a high frequency boost power converter is used for power factor correction which introduces wide range of allowable input voltage and zero crossover distortion (as opposed to buck and buck-boost topologies).

Current control scheme that is implemented in this thesis, is an extended version of Generalized Peak Current Control (GPCC) that is first introduced in [11]. Principle of operation is explained and the equations for constructing the GPCC bands are obtained.

Chapter 3

Power Decoupling and Electrolytic Capacitorless LED Drivers

3.1 Introduction

As current and voltage in PFCs are tuned to be in phase, according to equation 3.1, instantaneous input power in the input of single phase systems like PFCs contains double frequency oscillations. The problem comes into the picture with AC-fed LED drivers. As LEDs are essentially constant voltage loads [18] and are commonly driven by DC current, it's safe to say that they are DC loads by nature. So it is important to decouple the oscillating input power from the constant injected power to the LEDs.

$$p(t) = i(t)v(t) = I_m \sin(\omega t) V_m \sin(\omega t) = I_m V_m \sin^2(\omega t) = \frac{I_m V_m}{2}(1 - \cos(2\omega t)) \quad (3.1)$$

Electrolytic capacitors are continually used to decouple the energy difference between DC Load and AC mains in AC fed LED drivers. As opposed to the film capacitors which come in small packages only for small capacitance values, having a reasonable price and a fairly compact packages for large capacitance values make electrolytic capacitors a good option at the first glance. However, when it comes to benefit from the long lifetime of LEDs, which is in fact one of the main reasons to use LEDs in the first place, electrolytic capacitors are considered a bottleneck.

General idea is to make LED driver, as durable as LEDs. Utilization of electrolytic capacitors is known to be an unreliable approach as it substantially reduces the durability of LED driver, making a distinctive difference between the lifespan of LEDs and LED driver.

Amongst all the factors contributing in aging of electrolytic capacitors, temperature and voltage derating are the most effective one. Yet the effect of voltage derating on deterioration of electrolytic capacitors' lifespan is far less than that of the temperature. Internal heating which usually happens as the voltage ripples are applied to these capacitors can cause the evaporation of liquid electrolyte and drastically accelerate the aging process [19], hence, reducing the reliability and durability of LED driver. Different approaches have been developed to eliminate the use of electrolytic capacitors. Further through this chapter, notable approaches are reviewed. Then, the implementation of electrolytic capacitorless approach for this LED driver is detailed.

3.2 Electrolytic Capacitorless approaches

3.2.1 Pulsating Driving Current

Fig. 3.1(a) shows the input AC and output DC power. The difference between the input and output power has been highlighted and that is handled with the use of capacitor in LED drivers. Looking at the figure, one way to decrease this energy difference between input and output power seems to be utilizing the LED driver in a way to decrease the highlighted area shown in Fig. 3.1(a). Using DC biased sinusoidal or square wave pulsating current in the output to drive LEDs instead of DC current seemed to be the case in some researches. This way, the capacitance required to handle the power difference between input and output can decrease. Yet, the important question that comes into the picture is the effect of using non-DC driving current on life expectancy and luminous efficacy of LEDs. Studies done by researchers in [20] shows that LEDs lifetime doesn't decrease if driving current has the peak-to-average ratio of under 1.6. But usually this ratio is limited to 1.35 ensuring the safety compliance with LED manufacturing company data sheets.

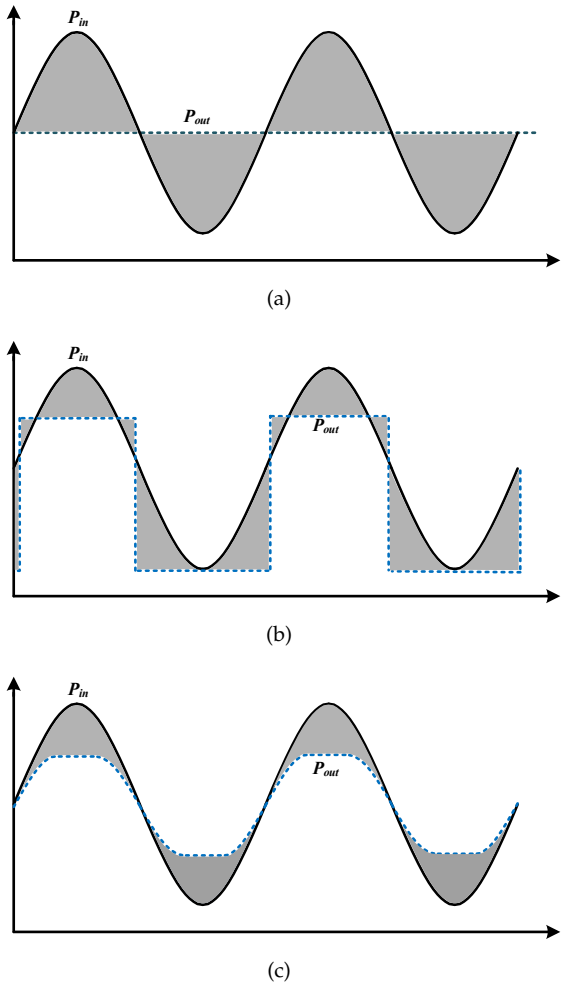


FIGURE 3.1: Output power utilizing different driving currents;
(a) Sinusoidal waveform: input power vs output power with constant dc driving current, (b) output power with square wave driving current, (c) output power with dc biased harmonic combined driving current

To design an electrolytic capacitor-less LED driver, authors in [21] proposed different driving currents. The idea is to minimize the difference between input and output power by utilizing different driving currents with the same average value. Hence, three case scenarios have been developed and studied. Fig. 3.1 shows the output power for a constant driving current, a dc biased sinusoidal driving current combined with second and forth harmonics $(1 - 0.44\cos(2\omega t) - 0.11\cos(4\omega t))$, and a square-wave driving current at low level equaling zero.

It has been concluded that the required storage capacitance needed to handle the input and output power difference is reduced to 55.8% of it's original value when using harmonic injected sinusoidal driving current with the form of $(1 - 0.44\cos(2\omega t) -$

$0.11\cos(4\omega t))$. Coefficients are calculated after determining the relationship between harmonics combined sinusoidal driving current and the storage capacitance. And the coefficient values are calculated to keep the peak to average ratio under 1.35. Also, given the same voltage across the DC link bus, the storage capacitance can be reduced to 52.7% of the original value if the square-wave driving current is used.

3.2.2 Allowing Higher Current Ripples at PFC

Allowing higher current ripples on the output of Power factor correction stage has also been investigated in the literature to facilitate employment of film capacitors [22]. The idea is to control the second converter to compensate for the allowed low frequency current ripples from the first converter. In [22], the input current reference hasn't been constructed by sensing the input voltage and the PF is set to 0.9 instead of unity power factor, the required energy storage is hence, reduced by 34%. Second stage is controlling the LED current, allowing 30% double frequency on LEDs current.

3.2.3 Reduced power processing approaches

3.2.3.1 Cascaded Topologies

By reducing the amount of power that is processed in each stage, the need for electrolytic capacitor has been eliminated in [22]. Fig. 3.2 (a) shows a two stage cascaded topology where the position of LED strings and the storage capacitor is substituted. The second stage is a bidirectional converter operating as buck or boost. when the input power is more than the requires value for LEDs, the excess power goes through the buck converter to the storage capacitor when the input power is less than the required value of power set for LEDs, the power goes through the reverse direction from the storage capacitor to the LED strings through the boost configuration. This way, the only part of the power that is processed twice, is the highlighted area and a smaller film capacitor can be utilized.

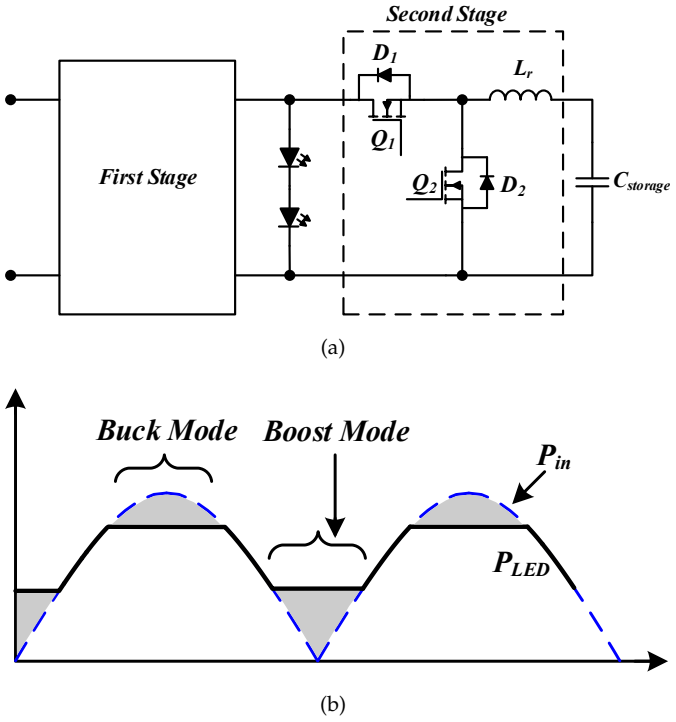


FIGURE 3.2: Reduced power processing approach with cascaded topology

3.2.3.2 Non-Cascaded Topologies

Non-cascaded structures have been introduced to eliminate the electrolytic capacitors while maintaining high efficiency by avoiding redundant power processing.

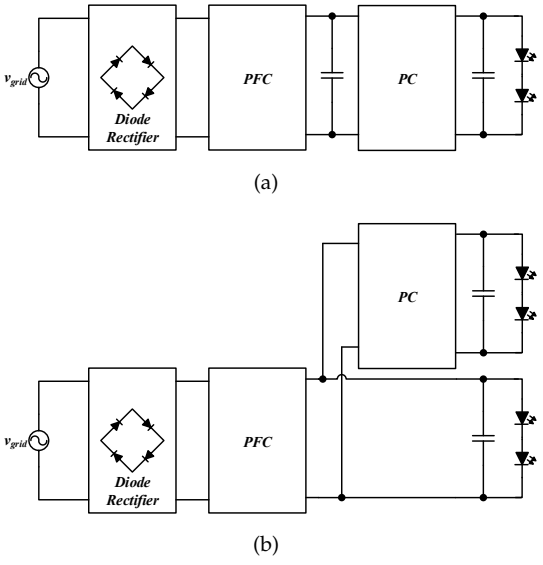


FIGURE 3.3: Multi-stage LED Driver Topologies;
(a) Independent cascade structure, (b) Optimized cascade structure (RRPP)

Fig. 3.3 shows different structures of multi-stage LED drivers. In Fig. 3.3(b) an optimized cascade topology has been introduced by [23]. The topology will follow the reduced redundant power processing (RRPP) scheme by providing partial processing of power by each converter. Therefore, resulting in a better efficiency while eliminating the use of electrolytic capacitor in the process. While PFC converter processes the major part of the input power and allows high voltage ripple on the bus to utilize film capacitor, the dc-dc converter will control the current flowing through the LEDs and operates in the opposite phase of the bus voltage to cancel out the low frequency ripples.

3.2.4 Magnetic Storage

Some methods use magnetic energy storage instead of electrolytic capacitor, and they can enhance LED driver with more robustness, lower maintenance requirement and more versatility in terms of operating temperature [24]. Fig. 3.4 shows the schematic of an offline LED driver. The main parts of the LED driver, as shown in the picture, are the input and output inductors, diode rectifier and valley-fill circuit. The input inductor helps with the reduction of the output power sensitivity to the input voltage fluctuations. Valley-fill circuit has been also employed to mitigate the voltage ripple at the output so that the size of output inductor can be reduced.

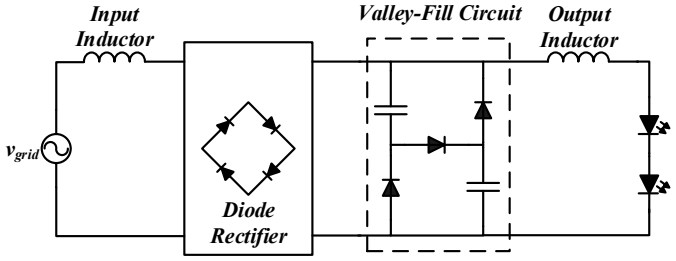


FIGURE 3.4: LED driver with inductive energy storage

3.2.5 Load Modularization

Another approach that has been investigated to address the reliability issues of electrolytic capacitors is load modularization [25]. Load modularization suggests splitting the load into different modules and operating each module with individual phase shifted signal. Fig. 3.5 can describe the approach in a simple way. As shown in the Fig.

3.5 (c), connection and disconnection of different load modules are performed through phase shifted approach so that the whole Load power consumption waveform resembles the input power. This way, the need for electrolytic capacitor is alleviated.

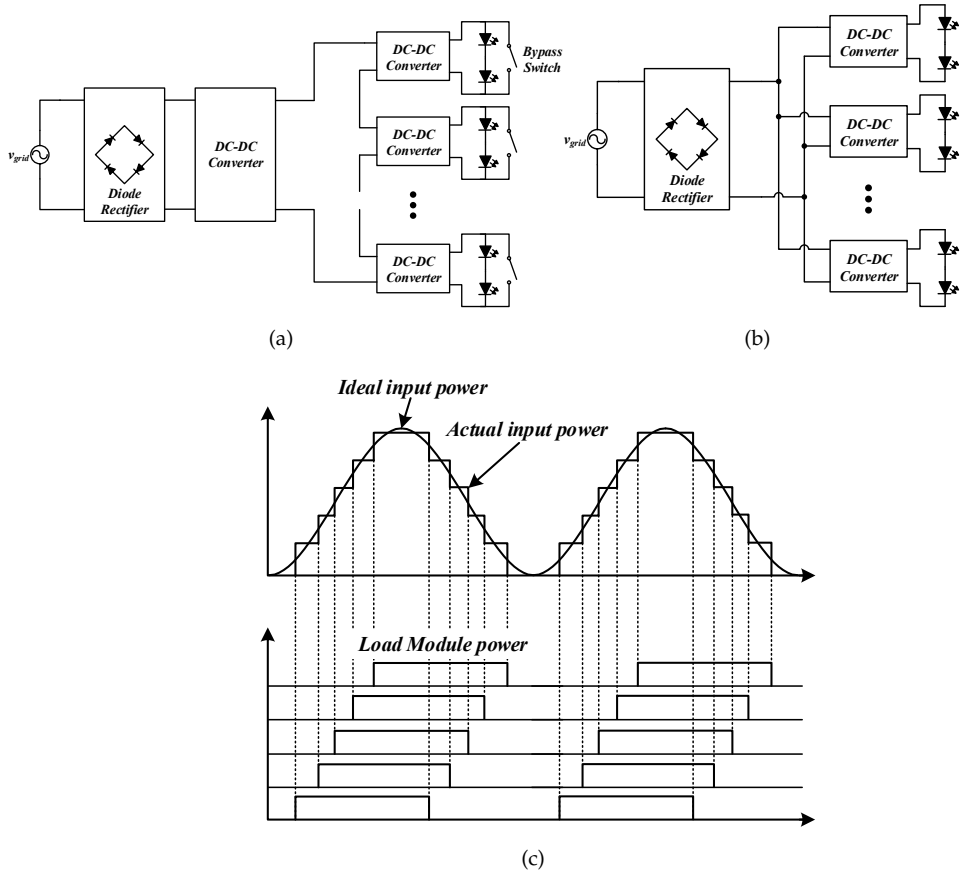


FIGURE 3.5: Load Modularization; (a) Series module connections, (b) Parallel module connection, (c) Input and load output power

3.2.6 Harmonic injection

One way to reduce the size of the output capacitor is to adulterate the HBLED driving current with harmonics to reduce the peak to average ratio of the LED driving current. The unity power factor has the peak to average current ratio of 2 which can cause unreliability while purely DC driving current of LEDs are claimed in [26] to result in overdriving-operating above the specified rated voltage or forward current-in which will shorten LEDs lifetime. Injecting third and fifth harmonic has been practiced in [26] to reduce the peak to average ratio of LED current to 1.34 while maintaining the power

factor over 0.9 to comply with standards such as ENERGY STAR [27]. This solution still suffers from a high THD and a relatively lower power factor.

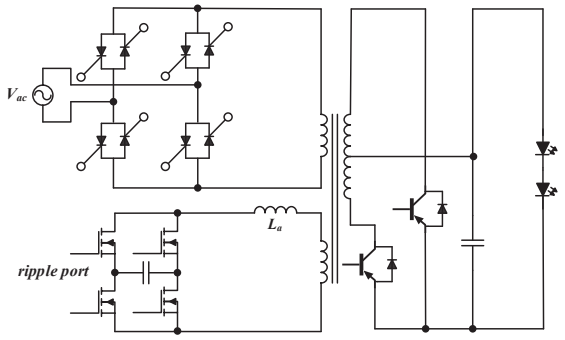


FIGURE 3.6: Isolated energy storage concept

3.2.7 Auxiliary Circuits

From using simple valley-fill circuits to relatively more complicated dedicated converters, using auxiliary circuits as a means to reduce the capacitor size has been introduced in many literatures.

Decoupling capacitor ripple from power ripples has been investigated to alleviate the need for bulky electrolytic capacitors. Authors in [28] introduced a three port concept which isolates the energy storage capacitor from input and output. By processing the instantaneous state of power, the dedicated converters either store the excess energy when the power is more than the DC output power,or feed the LED strings when the energy is below the preset DC reference. In another word, absorbing the ac component of LED driving current and leaving the dc current for LED strings. Although the concept is proposed for DC-AC applications such as photo-voltaic systems, the same concept is applicable to AC fed LED drivers with the reverse power flow. Fig. 3.6 shows the three port concept for LED lighting applications. The fact that there is a ripple port dedicated to process the capacitor ripple from the power ripple gives the designer the freedom to choose the capacitor voltage independently. Hence, utilizing film capacitors.

Fig. 3.7 shows a sepic-derived PFC stage utilizing a valley-fill circuit. The use of valley-fill circuit in this topology reduces the voltage stress on the output capacitor to half the

amount under the same power factor condition. That means the required amount of energy $\frac{1}{2}CV^2$ stored in the capacitor is a reduced by 25%, which facilitates the use of film capacitors. However, introducing twice the amount of film capacitors and numerous diodes are the disadvantage of this approach.

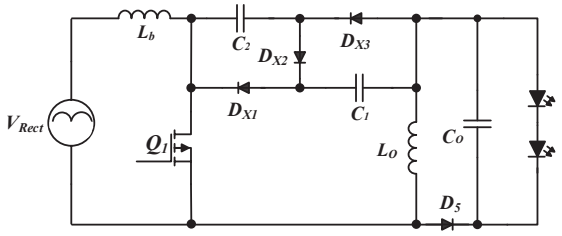


FIGURE 3.7: Sepic-derived PFC stage based on valley fill circuit.

Dedicated converters has also been studied to reduce the size of capacitors, such as [29] and [30] bidirectional converters in series and parallel to the LED load that are shown in Fig. 3.8. By storing the excess energy on the peak of the AC power applied to the LEDs and releasing it on the valley of the fluctuating power, the dedicated converter absorbs the AC component and leaves the DC part of the power for the LED string.

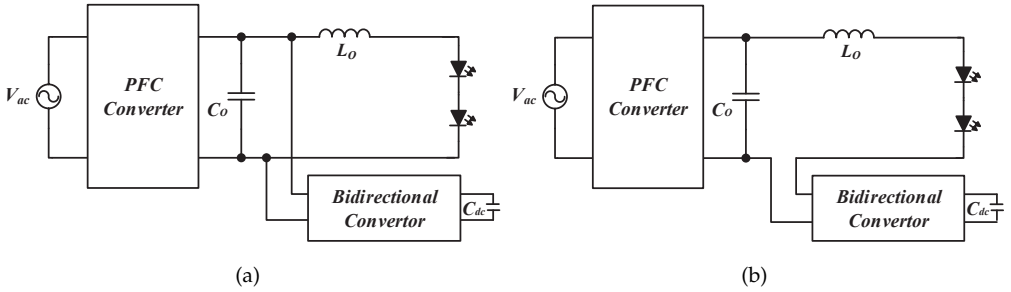


FIGURE 3.8: Electrolytic capacitor elimination using bidirectional converter in (a) parallel or (b) series connection with LEDs

3.3 Implementation of power decoupling approach

In this project we use a power decoupling approach that does not need high voltage on the bus or any additional auxiliary circuit. The method is inspired from PV micro-inverter proposed in [31]. In this method, we allow the bus voltage to oscillate at double frequency and using control methods, we remove the side effects of this double frequency oscillation from input current and LED output current. The block diagram

for power decoupling approach is shown in Fig. 3.9. Two sets of controller block diagrams are shown on each side of DC link. The mechanism in which allows decoupling of input and output power is the difference in the speed of controllers. While PFC controller allows double frequency voltage on DC link capacitor, series resonant converter controls the LED string current in a much faster dynamic to deliver DC power to the output.

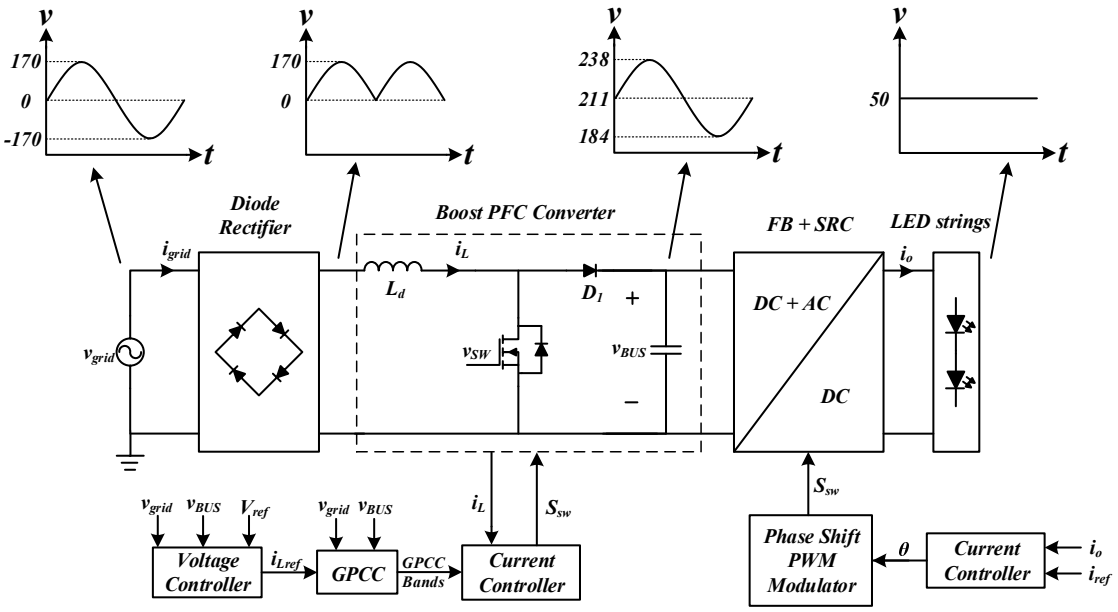


FIGURE 3.9: PFC + SRC control block diagram and Voltage levels

PFC Voltage controller constructs the reference current for boost inductor while controlling the DC link voltage, v_{BUS}. The generated reference current, i_{Lref}, in addition to the DC link and grid voltages, is used to construct GPCC Bands. Inductor current, i_L, is controlled within the bands to achieve a constant frequency. By changing the phase shift between the switches in full bridge series resonant converter, the amount of power delivered to the output changes corresponding to the peaks and valley of the DC link voltage to keep the output current constant.

Allowing higher current ripple on the output of PFC stage by 25% peak to peak oscillation will facilitate the use of smaller capacitor of Film technology. The resonant converter in the second stage of the LED driver is designed to work in a wide range of input voltage (DC link voltage) from $v_{BUS}^{Min} = 184\ V$ to $v_{BUS}^{Max} = 238\ V$ to provide a constant output voltage and attenuate the LED string current fluctuations to a great extent while achieving ZVS.

3.3.1 Capacitor Design

Design of the output bus is critical to have a tolerable large voltage swing on the DC link. A peak to peak voltage swing of 25% has been allowed for that matter, since allowing a higher voltage swing will reduce the bus voltage lower than the grid voltage and that makes the boost converter to malfunction.

As the maximum amount of voltage oscillation has been set, the output capacitor can be calculated using the power balance formula.

$$P_{in} = \frac{\widehat{V_{in}}.\widehat{I_{in}}}{2}.\cos(2\omega t) = P_{out}.\cos(2\omega t)$$

$$\frac{\Delta W}{2} = P_{out}\int_0^{\frac{T}{8}} \cos(2\omega\tau)d\tau = \frac{P_{out}}{2\omega}$$

$$\begin{cases} \Delta W = \frac{P_{out}}{\omega} \\ \\ W_C = \frac{1}{2}CV^2 \end{cases} \Rightarrow \Delta W = \frac{P_{out}}{\omega} = \frac{1}{2}C(V_{out,max}^2 - V_{out,min}^2) \Rightarrow$$

$$\frac{1}{2}C\left(\left(V_{out} + \frac{\Delta V_{out}}{2}\right)^2 - \left(V_{out} - \frac{\Delta V_{out}}{2}\right)^2\right) = CV_{out}\Delta V_{out}$$

$$\Delta V_{out} = \frac{P_{out}}{\omega C V_{out}} \Rightarrow C = \frac{P_{out}}{\omega V_{out}\Delta V_{out}}$$

Setting the PFC output voltage on 211 V , allowing for 25 percent voltage oscillation, and the grid voltage frequency of 60Hz, the DC link capacitor value is calculated to be 0.24 $\frac{\mu F}{Watt}$. For a 200 W design, 48μF is calculated and 50 μF is used in experimental setup.

3.4 Simulation and Experimental Results

According to Fig. 3.10(a), when the DC link voltage is at peak of its value, phase shift between switches Q_1 and Q_2 of full bridge converter (shown in Fig. 4.1 of chapter 4) makes the output voltage of full bridge converter dwell on zero for a portion of switching cycle to reduce the transferred power to the output. On the other hand, the aforementioned phase shift decreases to zero on the valley of the DC link voltage

as shown in Fig. 3.10(b),to maximize the power flow from the input to the output. Therefore, the power for each LED channel is kept constant.

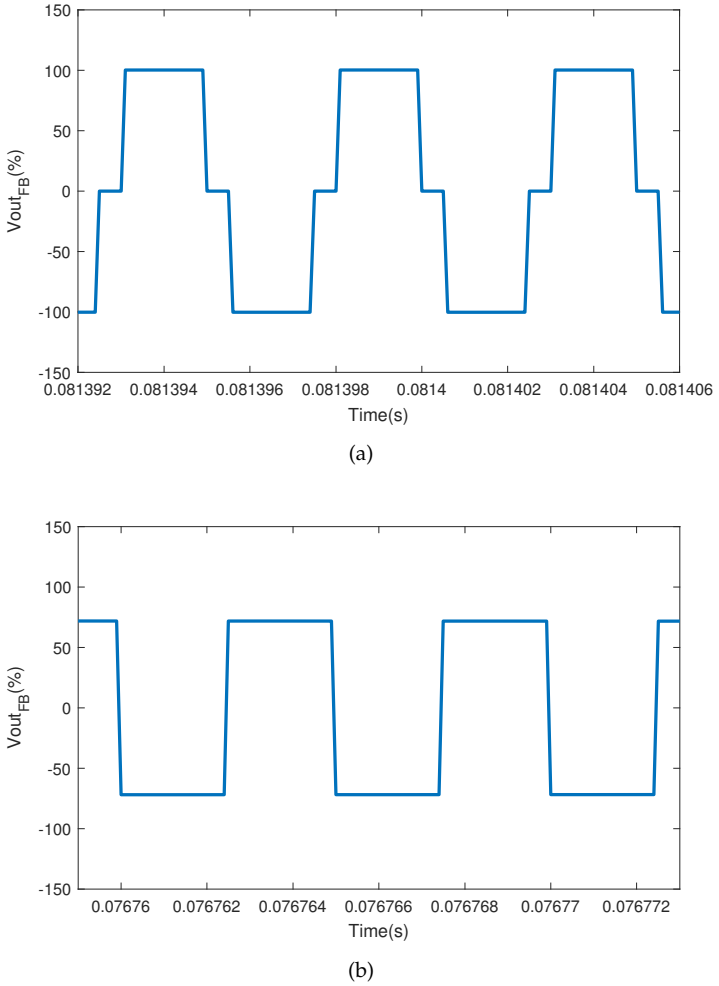


FIGURE 3.10: Output voltage of the full bridge converter: (a) on the peak of DC link voltage , (b) on the valley of DC link voltage

Fig. 3.11 shows the instantaneous input power that consists of DC component and an alternating component that oscillates with twice the line frequency. Employing a second converter of faster dynamic allowed us to achieve constant output power in 4 LED strings while removing electrolytic capacitor from the DC link.

Fig. 3.12 shows the DC link voltage and the LED string current on the output of LED driver. As shown in the figure, 54 volts voltage swing is allowed on DC link to facilitate the use of film capacitor while maintaining the average LED current on 1 A and the peak-to-average ratio of LED string current less than 1.25 to comply with safety standards according to the LED manufacturer data sheets.

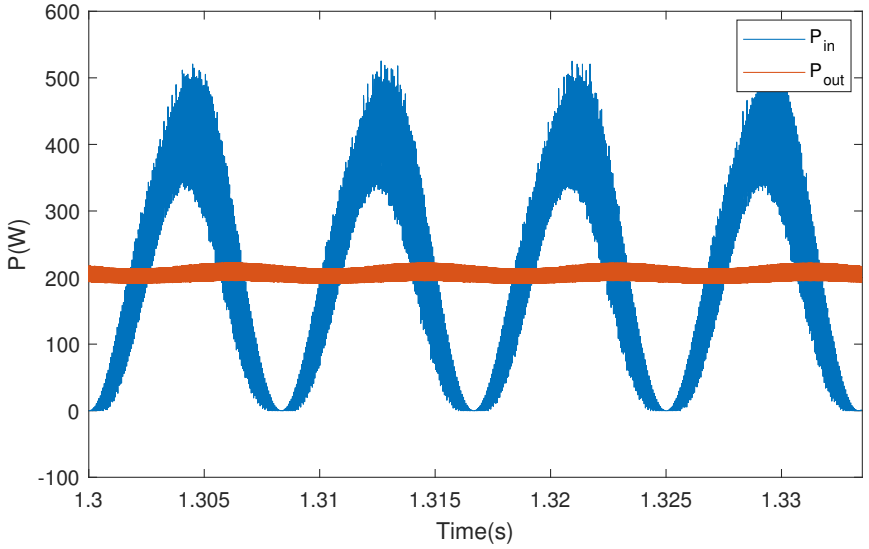


FIGURE 3.11: Power decoupling in LED driver : Input alternating power vs output power of 4 LED channels

3.5 Summary

This chapter first explains why power oscillation is generated in single phase systems. Then the existing methods to decouple output power from the input is reviewed. Power decoupling in solid state lighting not only increases the quality of output light, but also facilitates the use of smaller film capacitors instead of bulky electrolytic capacitors. This will in turn, extend the lifetime of LED driver, matching it with the life span of LEDs. Using auxiliary circuits, injecting harmonics, magnetic storage elements, load modularization, improvement in power processing stages through modified topologies and other means of eliminating electrolytic capacitors are surveyed and subsequently, a power decoupling approach is presented to deliver DC power to LEDs while extracting AC power from the grid.

The proposed approach for decoupling power is inspired from [31] which was used for PV applications and hence, a difference in power flow direction. The approach for decoupling power is to allow a high percentage of voltage fluctuation on DC link capacitor shown in Fig. 3.9. As shown in the Fig. 3.9, two controllers are implemented in our proposed LED driver. While the boost converter (PFC) controller controls the current by keeping the average voltage of the DC link constant and allowing a high DC

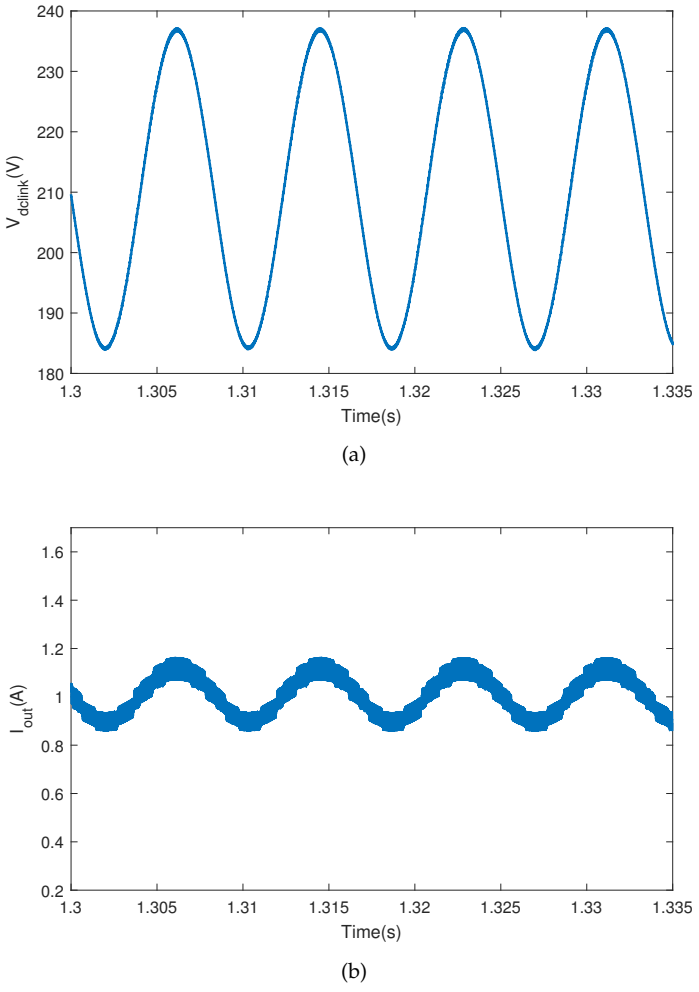


FIGURE 3.12: Power Decoupling in LED driver: (a) DC link voltage, (b) LED string current

link voltage swing, SRC controller is operating in a much faster speed and controls the output current by generating phase shift corresponding to the DC link fluctuations.

Chapter 4

Series Resonant Converter

4.1 Introduction

Fig. 4.1 shows the complete circuit diagram of the proposed LED driver topology. The figure puts emphasis on the second stage by showing the detailed schematics. In order for electrolytic capacitor elimination, a large variation in output voltage of the first stage has been allowed. The regulation of voltage and transferring the energy in an efficient manner is on second stage to be performed. In order to achieve high efficiency while transferring the energy, soft switching has been practiced with a series resonant converter. For better understanding of the principle of operation and the means to achieve current and voltage regulation while maintaining high efficiency, a brief introductory to the soft switching concept has been provided; followed by a detailed explanation of proposed series resonant converter (SRC) topology, modes of operation, steady state analysis, and design considerations.

4.1.1 Soft switching

To simply explain the concept of soft switching, one should consider the case where the switch is in series with an inductor. The current goes through an inductor and it leads to the storage of energy that equals to $\frac{1}{2}Li^2(t)$. According to conservation of energy, this energy remains constant and hence, the turning off action of the switch in series with the inductor, makes no room for this energy to flow and dissipate in the circuit and that results in destruction of the switch.

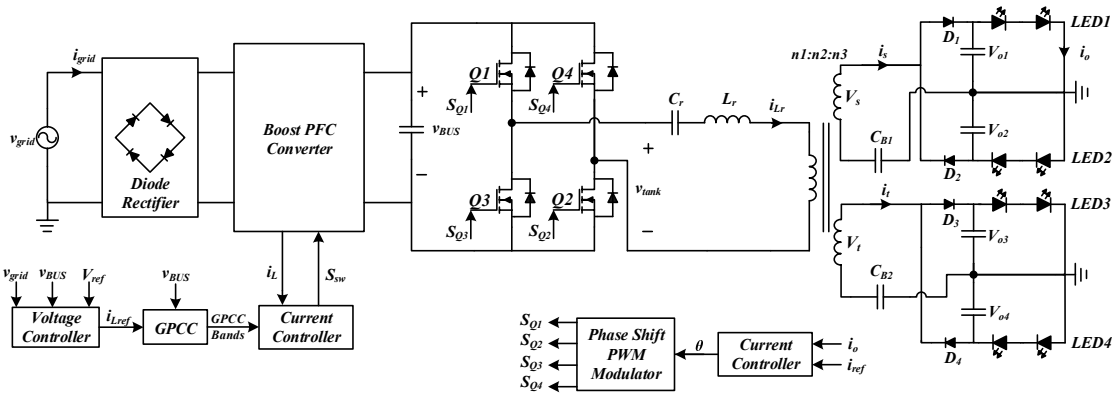


FIGURE 4.1: Series Resonant Converter topology

Commutating diode has been the answer to this issue as it will provide a path for the inductor current to keep flowing in the circuit without interruption. Yet, it turns out the transition between turning off the switch and letting the commutating diode to take on the current doesn't happen instantaneously. For the commutation to happen and for the diode to be forward biased, the voltage starts to build up across the switch before the current starts exiting it.

Switch transition in which produces a non zero $V * I$ will dissipate energy. This dissipation of power, as small as it may appear within one switching cycle, can happen thousands of time per second depending upon the operating switching frequency and lowers the efficiency to a considerable extent. That is where the significance of soft switching comes into the picture. Using a suitable resonant converter topology that can operate in the allowed line and load variation and reduces switching losses would be the answer to this issue.

Within the dead time of the switch, a negative current would facilitate the free-wheeling diode of the MOSFET to turn on before the turn ON and deplete the drain-source capacitor of the MOSFET, C_{ds}, so that the turn ON would happen with zero voltage. This current path through the free-wheeling diode wouldn't be formed with a positive current of $i_{tank}(t)$, because of the unidirectional behavior of free-wheeling diode. The energy inside the C_{ds} would be dissipated inside the switch and hard switching action will occur. The C_{ds} will delay the voltage rise of v_{ds} during turn OFF and it will provide near zero turn off losses of the MOSFET if designed properly.

4.1.2 Phase shifted PWM

To understand SRC analysis in subsequent chapters, a brief explanation of Phase shifted PWM approach is provided. As shown in Fig. 4.2, there is a phase shift equal to ϕ between switches in two legs of full bridge rectifier. If $\phi = 0^\circ$ then the generated voltages is also equal to zero. It means that the switching pattern for Q_1 is the same as Q_3 and the $v_{tank}(t)$ is always equal to zero. If $\phi = 180^\circ$ then $v_{tank}(t)$ would be shaped like a square wave. Increasing ϕ between 0° to 180° corresponds with changing the duty cycle d in the Fig. 4.12 from 0 to 50%. This is how phase shifted PWM is used to control the magnitude of the first harmonic of the generated voltage in the output of full bridge rectifier.

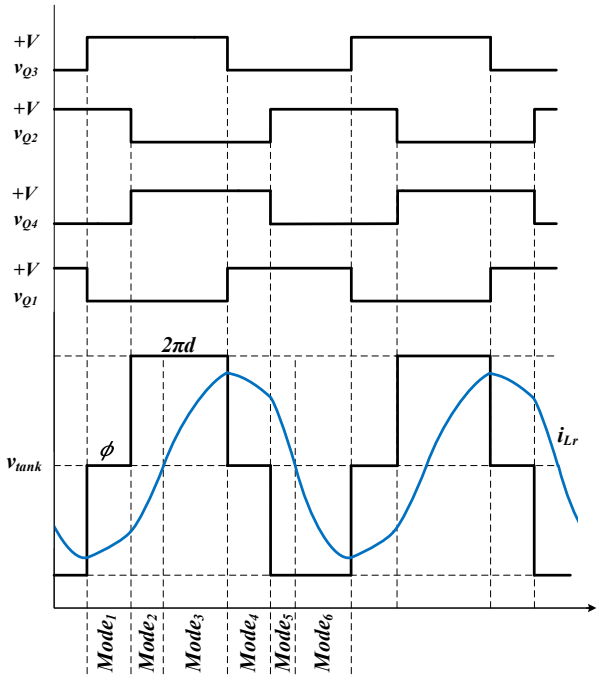


FIGURE 4.2: Phase shift Switching Pattern, resonant Tank Input Voltage, Current, and SRC Modes of Operation

4.2 Series Resonant Converter (SRC) Topology

Fig. 4.1 shows the circuit diagram of the phase shift constant frequency series resonant converter. A full bridge consisting four switches Q_1 to Q_4, a series resonant tank made

by capacitor C_r and inductor L_r, and a transformer are integrated with a passive current sharing structure with two blocking capacitors $CB1$, $CB2$ connected to four LED channels.

For eliminating the electrolytic capacitor, a relatively big voltage swing is allowed on the output of boost converter, v_{BUS}. Hence, the input voltage of the series resonant converter consists of DC and AC parts.

SRC controls the output current of the LED_1 referred as i_o as a Master channel. Precise current control in all the Slave channels is achieved automatically. The principle of operation is discussed in the subsequent section.

4.3 Series Resonant Converter Principle of Operation

The voltage applied to the tank in the output of full bridge structure, v_{tank}, is not of variable frequency. The waveform is of fixed frequency and for a portion of the cycle it is clamped at zero. The LED current is controlled and the phase shift theta, θ, is constructed in degrees at the PI controller output and turns into switching signals via "Phase Shift PWM Modulator". The amount of phase shift that is constructed will be applied to the switches in Full bridge legs. Switches Q_1 and Q_3 and similarly Q_2 and Q_4 operate in a complementary fashion. And the phase lag is applied to the diagonal switches as it can be shown from the Fig. 4.2. The phase lag modulates the amount of time the input voltage is applied to the resonant tank and the LED strings' currents are controlled in this way.

The four active switches turn on achieving ZVS and turn off while the current goes to zero at a voltage close to zero.

4.3.1 Mode I

As shown in Fig. 4.3, switches Q_1 and Q_4 are conducting. Hence, the input voltage of the series resonant converter is disconnected. As indicated in Fig. 4.2, Q_2 has a phase shift regarding to Q_1 with the amount of θ which renders the span of time in which resonant tank is disconnected from the DC link voltage v_{BUS} and therefore v_{tank} is clamped at zero.

Fig. 4.4 shows that in turning ON instance of Q_1, current initially goes though the freewheeling diode instead of switch and that gives the gate-source capacitor of the switch, C_{gs}, time to deplete and switching turn ON to happen in a zero voltage.

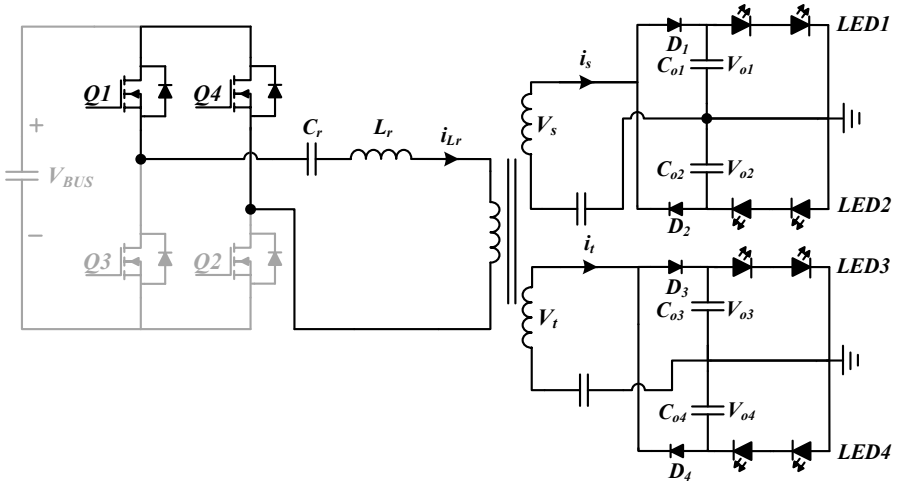


FIGURE 4.3: Mode 1 of resonant converter operation

In the ideal form where there is no resistance like DCR or ESR (DC resistance in series with the inductor and equivalent series resistance in series with capacitor for the real representation of the component) in the circuit, the source has to be only connected to provide the energy for the resonant tank in the beginning and since no energy is dissipated, the current would go back and forth between the resonant components indefinitely. In the case where there is dissipative load, the need for an energy source remains throughout the operation for compensating the energy delivered to the load. Yet the fact remains, that with a partial disconnection of the source, the already depleted inductor in the resonant tank will be charged by the current that is going back and forth between the resonant components. As it's shown in the Fig. 4.2, the current i_{Lr} that goes back and forth between resonant components is negative, charging the inductor with a comparatively slower rate within the cycle.

Diodes D_2 and D_4 are conducting, charging the Capacitors C_{o2} and C_{o4}. Simultaneously, the already-charged capacitors C_{o1} and C_{o3} feed the LED_1 and LED_3 strings.

4.3.2 Mode II

Fig. 4.2 shows the voltages across switches and the input voltage of resonant tank in a few switching cycles. Hence, the double frequency oscillation of v_{BUS} that is neglected

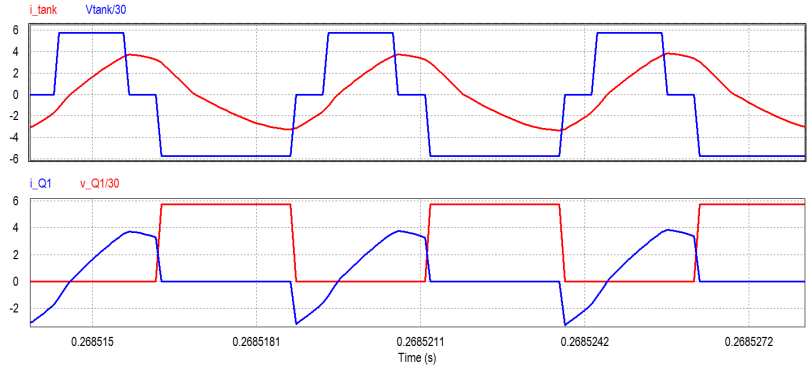


FIGURE 4.4: Zero voltage switching in switch Q_1

and waveforms assumed to have constant envelops. In the second mode, Q_1 and Q_2 are conducting. As shown in the Fig. 4.5, ZVS has been achieved in turning ON of Q_2. Current i_{Lr} is still negative but charging the inductor L_r in a faster pace since the voltage source is now connected. There hasn't been any changes for the direction of the i_{Lr}, therefore, the same diodes Diodes D_2 and D_4 are ON and the operation of the passive current balancing circuit remains the same.

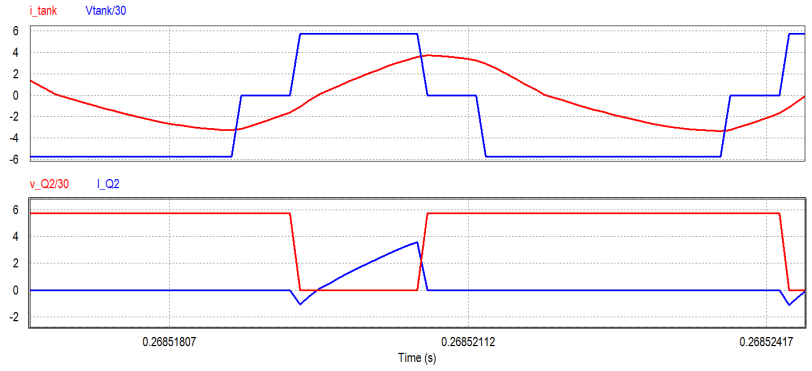


FIGURE 4.5: Zero voltage switching in switch Q_2

4.3.3 Mode III

This mode is characterized by the same conducting switches as the previous mode in the resonant converter side. Yet the current flow direction of i_{Lr} and subsequently the direction of the currents i_s and i_t on the secondary and tertiary side of the transformers is reversed. As the "built up" energy in the resonant inductor is now to be depleted.

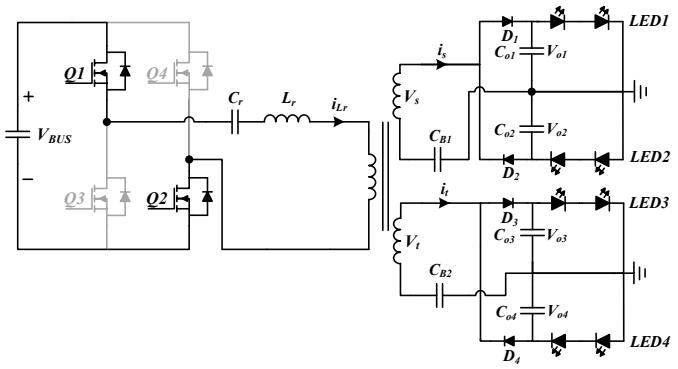


FIGURE 4.6: Mode 2 and 3 of resonant converter operation

Diodes D_1 and D_3 are conducting and the current is going through LED_1 and LED_3 charging the C_{o1} and C_{o3}.

4.3.4 Mode IV

Mode IV is depicted in the Fig. 4.8. This mode is the same as the first one in the sense that the voltage source is disconnected from the resonant tank. Switches Q_2 and Q_3 are conducting. As shown in Fig. 4.7, Q_3 turns ON in ZVS condition. The difference of this mode from the first mode is the current flow that is now positive and the current goes through LED_1 and LED_3 via diodes D_1 and D_3.

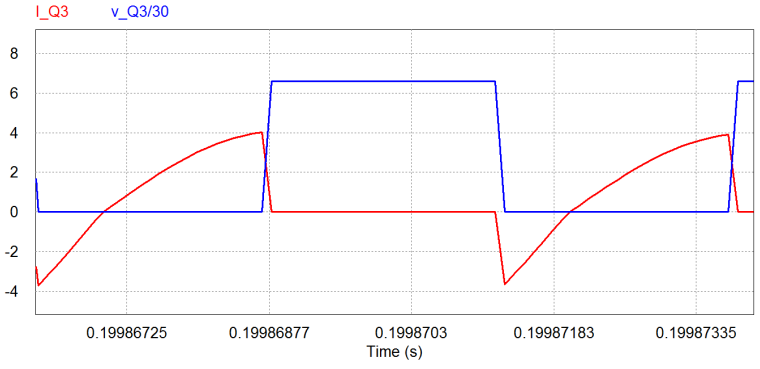


FIGURE 4.7: Zero voltage switching in switch Q_3

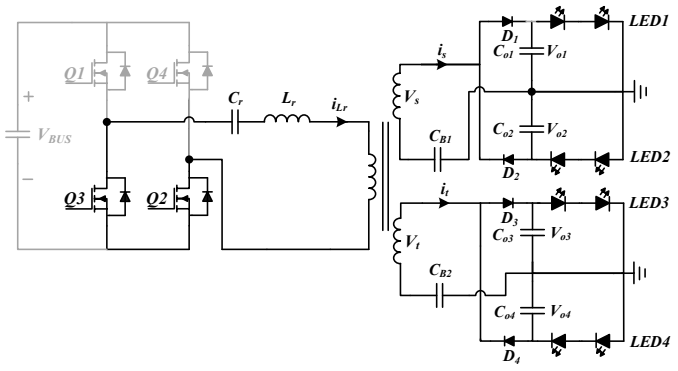


FIGURE 4.8: Mode 4 of resonant converter operation

4.3.5 Mode V

Fig. 4.10 shows the fifth mode of SRC operation. As shown in Fig. 4.9, switch Q_4 starts to conduct under ZVS condition. Along with Q_3 conducting, they present a negative voltage in the resonant tank input. As it can be inferred from the sign of i_{Lr} in the Fig. 4.2, the operation of the passive current balancing circuit is the same because of no change in current direction. The voltage across the inductor is negative and the positive direction of current through it suggests that the inductor is storing the energy in this part of the cycle.

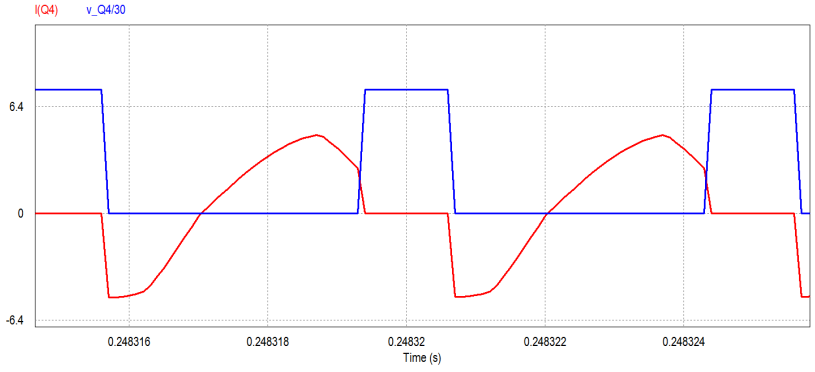


FIGURE 4.9: Zero voltage switching in switch Q_4

4.3.6 Mode VI

The same switches as the previous mode are conducting as negative voltage appears at the input of resonant tank. The direction of the current changes and now the inductor

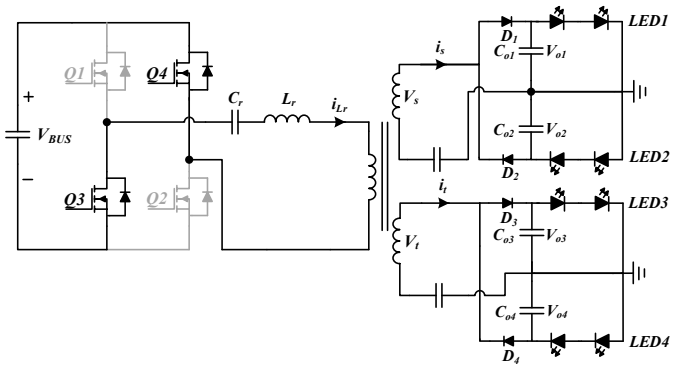


FIGURE 4.10: Mode 5 and 6 of resonant converter operation

is depleting its energy in a fast rate. The negative i_{Lr} in Fig. 4.2 suggests conduction of diodes D_2 and D_4 again and current would go through the LED_2 and LED_4. The output capacitors C_{o1} and C_{o3} are discharging the current into LED_1 and LED_3, respectively.

4.4 Series Resonant Converter Steady-State Analysis and Design

Researchers in [12] developed a Laplace based theorem (LBT) to provide an accurate and parametric design tool for dc-dc converters. LBT compensates for inaccuracies incorporated within conventional average or numerical methods used for design and analysis of dc-dc converters. In order to derive the design parameters and equations for the resonant converter used in this LED driver, LBT is employed on variable duty cycle full bridge SRC. In this section, a brief description of LBT is provided. Following through, the steps for design and analysis of LED driver's SRC is reviewed upon.

4.4.1 Laplace Based Theorem (LBT)

The solution of every ODE can be synthesized into zero state and zero input responses. While the former is caused by the input function, the latter shows system's response to solely initial conditions. Both of these responses can have transient and steady state parts. LBT approach used in [12] would determine the initial conditions at the beginning of each cycle to compensate the transient response to the input function. Hence, a purely periodic system response would be achieved.

4.4.1.1 Laplace Based Theorem

Assuming an n-th order ODE with the form of $P(D)x(t) = f(t)$ where:
$D = \frac{d}{dt}$ is the Differentiation operator.
$P(.)$ is a characteristic polynomial with the below representations:

$$P(D) = \sum_{k=0}^{n} a_k D^k$$

The characteristic polynomial has n roots which can be denoted by s_j. $f(t)$ is an input periodic function with the period of T that has a finite number of discontinuities that is applied to the system. $x(t)$ is the ODE response.

- Taking a Laplace transform of the ODE will result in

$$P(s)X(s) - G(s) = F(s)$$

  where:
  $P(s)$ is the characteristic polynomial in Laplace domain. Variable s is the representation of differentiation operator in Laplace domain. $F(s)$ is the Laplace transform of the input function:

$$F(s) = \frac{\int_0^T f(t)e^{-st}dt}{1 - e^{-sT}}$$

  $G(s)$ is a function of initial conditions of $x(t)$:

$$G(s) = (x_0 a_n)s^{n-1} + (x_0 a_{n-1} + x_1 a_n)s^{n-2} + ... = \sum_{k=0}^{n-1} b_k s^k$$

$$x(0) = x_0, x^{(1)}(0) = x_1, ..., x^{(n-1)}(0) = x_{n-1}$$

- With solving n equations of $G(s_j) = -F(s_j) \quad j = 1, 2, ..., n$, the n initial conditions of $x_0, x_1, ..., x_{n-1}$ can be achieved so that the system response $x(t)$ can be purely periodic in steady state without any transients.

One application would be the presence of discontinuous switching input functions. With the help of LBT, by finding these initial conditions, the changes caused by discontinuous switching functions are accurately predicted at steady state conditions [32].

4.4.2 Analysis of the LED driver series resonant converter

A systematic approach to explain the analysis and design procedure of SRC is presented according to the following list:

- Description of the SRC topology, generic waveforms and ODE governing the system behavior.
- Scrutinizing the details on the conditions for achieving ZVS.
- Introducing main set of variables describing an SRC.
- Linearizing the ODE by introducing intermediate variables.
- Applying LBT to the linearized ODE to obtain SRC's accurate equations in terms of intermediate variables.
- Finding the intermediate variables as a function of main variables.

4.4.2.1 Topology, waveforms, and ODE

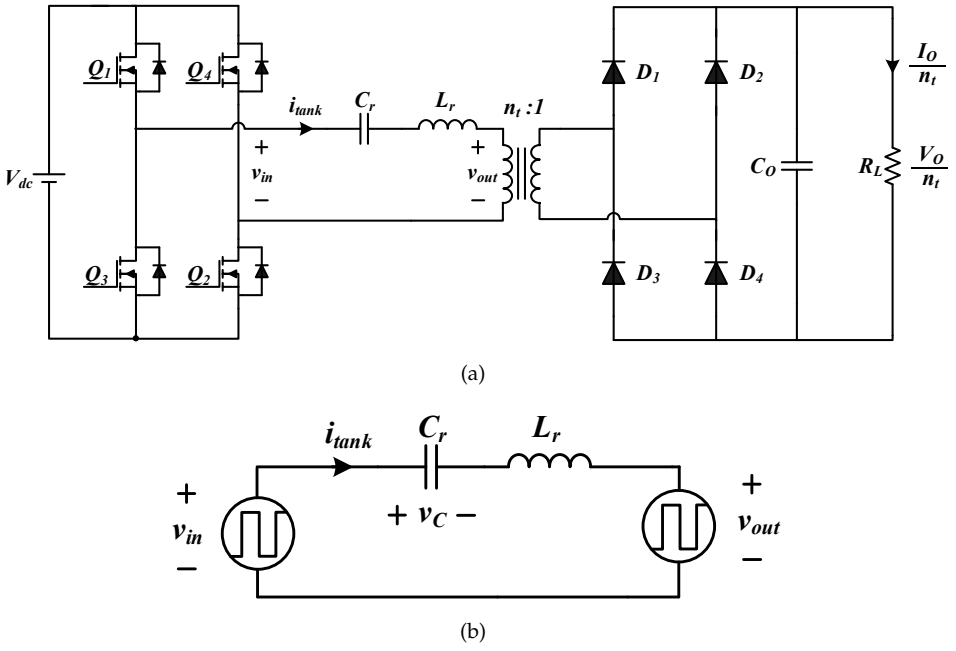


FIGURE 4.11: Series resonant converter: (a) Circuit Schematic, (b) simplified circuit

Fig. 4.11 shows the detailed and simplified schematic of series resonant converter. Controller is based on phase shift PWM or variable duty cycle approach where d is the duty ratio varying between 0 to 50% and $d' = 0.5 - d$.

Assuming simplified version of SRC in Fig. 4.11 (b) to work in CCM mode, the differential equation modeling the behavior of the system is as follows:

$$L\frac{di(t)}{dt} = v_{in}(t) - v_c(t) - v_{out}(t) \tag{4.1}$$

where the output voltage of resonant tank, $v_{out}(t)$, has the square wave form and is equal to:

$$v_{out}(t) = V_o \,\mathrm{sgn}(i_{tank}(t))$$

The use of $sgn()$ function is due to the presence of diode bridge rectifier on the output. Considering the output capacitor C_O large enough, the load voltage can have a constant value of $\frac{V_O}{n_t}$. Depending on the direction of I_O, one can infer that value of the resonant tank output voltage v_{out} is V_O when D_1 and D_4 are conducting and $-V_O$ when current goes through D_2 and D_3.

A closer look into the input and output voltage of the resonant tank ,$v_{in}(t)$ and $v_{out}(t)$ presented in Fig. 4.12, shows the resonant tank input voltage, $v_{in}(t)$, that has three levels of V_{in}, 0, and $-V_{in}$. The output voltage of resonant tank,$v_{out}(t)$, is in phase with its current, $i_{tank}(t)$ and can have the values of V_O and $-V_O$ depending on the direction of the current.

4.4.2.2 ZVS conditions

As it has previously been explained in section 4.1.1, ZVS can be achieved on switching turn on action with the full bridge converter, provided that the resonant converter operates above resonant frequency. This will in turn, make the impedance of resonant inductor dominating the impedance of resonant capacitor. Therefore, the whole resonant tank acts as an inductor. Taking another glance at Fig. 4.12 certifies this assumption by showing a phase lag between $i_{tank}(t)$ and $v_{in}(t)$. As shown in the figure, if we set a starting point for the input voltage (marked with the point 0), current would have a phase lag of θ.

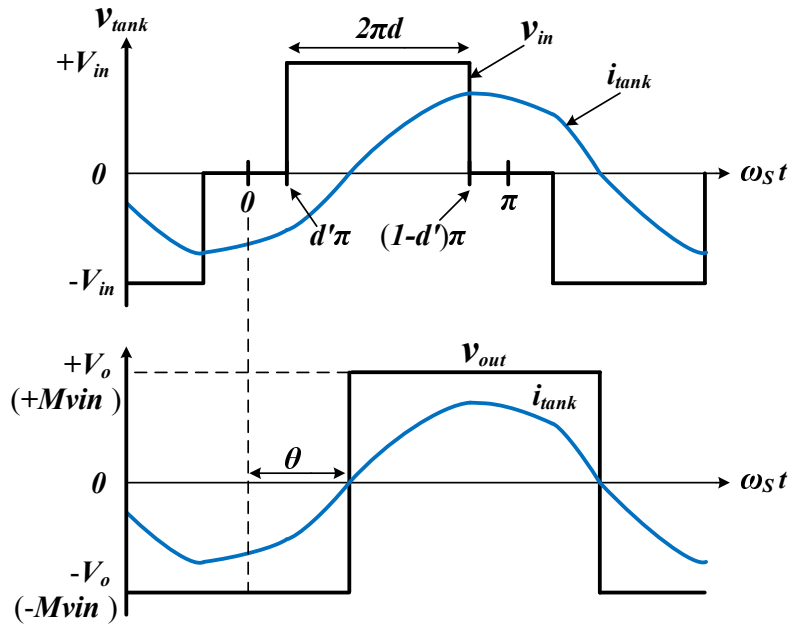


FIGURE 4.12: Typical waveforms of series resonant converter

Having set the starting point for the input voltage, switching action occurs on the $d'\pi$ instant. ZVS is ensured when the value for the $i_{tank}(t)$ is negative at this moment. The condition in which ensures the current $i_{tank}(t)$ to be negative at the switching instant, is for θ to be greater than $d'\pi$.

$$\theta > d'\pi \tag{4.2}$$

4.4.2.3 Introducing main variables

Fig. 4.12 suggests ZVS would be achieved with no great challenge when operating with large duty cycles (larger phase shift ϕ between full bridge legs). But when delivering smaller amount of power to the resonant tank and working with smaller duty cycles, the value for $d'\pi$ increases and it might exceed the value of θ, resulting in losing ZVS.

To assure the first condition of ZVS in equation 4.2 is met, the knowledge about waveforms and characteristics of SRC is necessary. A better insight into the converter characteristics can be provided by introducing main variables of F, Q, and d.

$$F = \frac{f_s}{f_r} = \frac{\omega_s}{\omega_r} > 1 \tag{4.3}$$

$$Q = \frac{Z_0}{n_t^2 R_L} \tag{4.4}$$

where:
$d = \frac{t_{on}}{T}$ is the switching duty cycle. F is the normalized frequency. $f_s = \frac{\omega_s}{2\pi}$ and $\omega_r = \frac{1}{\sqrt{L_r C_r}}$ are switching and resonant frequency, respectively. The value for F should be greater than 1 to assure the inductive behavior of resonant tank and Hence, ZVS operation. $Z_0 = \sqrt{\frac{L_r}{C_r}}$ is characteristic impedance of resonant tank. Q is load quality factor. It's the ratio between the characteristic impedance of resonant tank and the equivalent load resistance referred to the primary side of the transformer that is $n_t^2 R_L$.

The knowledge about three main variables of F, Q, and d is sufficient to obtain all the characteristics of an SRC and describe it's behavior.

4.4.2.4 Linearizing ODE, applying LBT and finding M and θ in terms of main variables

Substituting the $i = C_r \frac{dv_{c_r}(t)}{dt}$ into equation 4.1 will result in the below ODE:

$$L_r C_r \ddot{v_c}(t) + v_{c_r}(t) = v_{in}(t) - V_o \operatorname{sgn}(i_{tank}(t)) \tag{4.5}$$

As mentioned earlier, equation 4.5 is non linear because of the discontinuous input and output voltage. A conventional approach to linearize output voltage and sgn function, is to model the output diode rectifier with a resistance ,$R_{ac} = \frac{\pi^2 R_L}{8}$ (as the output voltage and current are in phase, refer to Fig. 4.12)

For the input voltage with the form presented in 4.12, the common linearization approach is to model it with the first harmonic of its Fourier series as the second order resonant circuit will reduce other harmonics. The problem that arises with this way of linearization in variable duty cycle control is that with the change of duty cycle, the other harmonics grow to a point that they cannot be neglected.

Intermediate variables θ and M are defined to address the non-linearity of the equation 4.5. θ is the current phase lag with respect to the voltage $v_{in}(t)$ and $M = \frac{v_{out}}{v_{in}}$ is the converter voltage gain. LBT approach introduced in [12] can be applied to the linearized

ODE to obtain the exact *ODE* response in terms of θ and M. According to [12], the voltage gain M and current phase lag θ are calculated as follows:

$$M = \begin{cases} \left(\frac{2F}{\pi Q}\right) \frac{AB\sqrt{A^2+B^2-1}-B^2}{A^2+B^2} & \text{if } d'\pi < \theta \\ \left(\frac{2F}{\pi Q}\right) \frac{\sin\left(\frac{\pi d}{F}\right)}{\sqrt{\left(\frac{2F}{\pi Q}\sin\left(\frac{\pi}{2F}\right)\right)^2+\cos^2\left(\frac{\pi}{2F}\right)}} & \text{if } d'\pi \geq \theta \end{cases} \tag{4.6}$$

$$A = \sin\left(\frac{\pi d}{F}\right)\tan\left(\frac{\pi}{2F}\right)+\cos\left(\frac{\pi d}{F}\right), \qquad B = \frac{\pi Q \cos\left(\frac{\pi d'}{F}\right)}{2F\sin\left(\frac{\pi}{2F}\right)}$$

$$\theta = \begin{cases} \frac{\pi}{2} - F\sin^{-1}\left(\frac{A\sqrt{A^2+B^2-1}-B}{A^2+B^2}\right) & \text{if } d'\pi < \theta \\ F\cos^{-1}\left(\left(1+\left(\frac{\pi Q}{2F}\cot\frac{\pi}{2F}\right)^2\right)^{-\frac{1}{2}}\right) & \text{if } d'\pi \geq \theta \end{cases} \tag{4.7}$$

By substituting θ with $d'\pi$ in equation 4.7 the critical duty cycle value d_{ZVS} is obtained. For any d between the critical value, d_{ZVS}, and the maximum value, 50%, ZVS operation is guaranteed.

$$d_{ZVS} = 0.5 - \frac{F}{\pi}\cos^{-1}\left(\left(1+\left(\frac{\pi Q}{2F}\cot\frac{\pi}{2F}\right)^2\right)^{-\frac{1}{2}}\right) \tag{4.8}$$

4.4.3 Design of the LED driver series resonant converter

The critical duty cycle, d_{ZVS}, is defined in the previous section. For every $d > d_{ZVS}$, the condition 4.2 is met and ZVS operation is guaranteed. And if $d \leq d_{ZVS}$, then $\theta > d'\pi$ and ZVS is lost. So in order to design an SRC, first step is to calculate main variables F and Q based on design parameters. Secondly, the critical duty cycle can be obtained using 4.8. And the θ, M, and each d can be calculated using the aforementioned equations.

Looking back at the Fig. 4.1, Input voltage of SRC, v_{BUS}, fluctuates between a minimum and maximum value. The goal is to design SRC in a way to maintain a perfect correlation between minimum-maximum input voltage and minimum allowable-maximum duty cycle to ensure delivery of a constant power to the load while operating under ZVS conditions.

From the analysis done in the previous section, $d = 50\%$ corresponds to maximum voltage gain as the duty cycle decreases, the voltage gain drops. The minimum duty cycle allowable to maintain ZVS operation is $d = d_{ZVS}$ which corresponds to minimum (allowable) voltage gain.

$$\frac{M(d = 50\%)}{M(d = d_{ZVS})} = \frac{v_{BUS}^{Max}}{v_{BUS}^{Min}} \tag{4.9}$$

$$v_{BUS}^{Min} = 184\ V \qquad\qquad v_{BUS}^{Max} = 238\ V$$

4.4.3.1 Calculating Main Variables

As mentioned earlier, values for minimum and maximum DC link voltage, v_{BUS}^{Min} and v_{BUS}^{Max}, are known according to the design of Power Factor Correction stage. The value for the power output for LEDs and the LED string voltage, $V_{dc,out}$, is also known.

According to [12], the voltage across resonant capacitor is :

$$v_{C_r} = \frac{\pi Q}{2F} M v_{BUS} = \frac{\pi Q}{2F} n_t V_{dc,out} \tag{4.10}$$

As the value of Q increases, a larger voltage stress would be applied to the resonant capacitor. Hence, for designing resonant tank with smaller capacitor, the value for F (and subsequently the switching frequency) is set to be high and Q should be of a low value. In [32], the below set of nonlinear equations is introduced to calculate the values of F and Q.

$$\begin{cases} \dfrac{\pi Q}{2F} M(d = 50\%) v_{BUS}^{Min} = 120V \\ \\ \dfrac{M(d = 50\%)}{M(d = d_{ZVS})} = \dfrac{v_{BUS}^{Max}}{v_{BUS}^{Min}} \end{cases} \tag{4.11}$$

Value of $120V$ has been selected as maximum voltage stress across the resonant capacitor. Choosing 1.594 for F, the value for Q has been solved to be $\approx$ 1.315 through numerical method of solving non-linear equation 4.11.

4.4.3.2 Transformer Turns Ratio

Having the value of main variables F and Q obtained, transformer turn ratio can be calculated from equation 4.10. We have :

$$n_t = v_{C_r} \frac{2F}{\pi Q V_{dc,out}} = 1.85$$

4.4.3.3 Characteristic Impedance of Resonant Tank

For a $50V$ LED string voltage and $200W$ output power, R_L can be calculated:

$$R_L = \left(\frac{50^2}{200}\right) = 12.5\ \Omega$$

According to equation 4.4, the value for characteristic impedance of resonant tank can be calculated as follows:

$$Z_0 = R_L Q n_t^2 = 56.2573$$

4.4.3.4 Calculating design parameters

Selecting switching frequency to be $200kHz$, resonant frequency can be obtained:

$$f_r = \frac{f_s}{F} = \frac{200\ kHz}{1.594} \approx 125.47\ kHz$$

$$\omega_r = 2\pi f_r \approx 788354\ \frac{rad}{sec}$$

$$L_r C_r = \left(\frac{1}{\omega_r}\right)^2$$

The values for L_r and C_r can be selected from the available products as below:

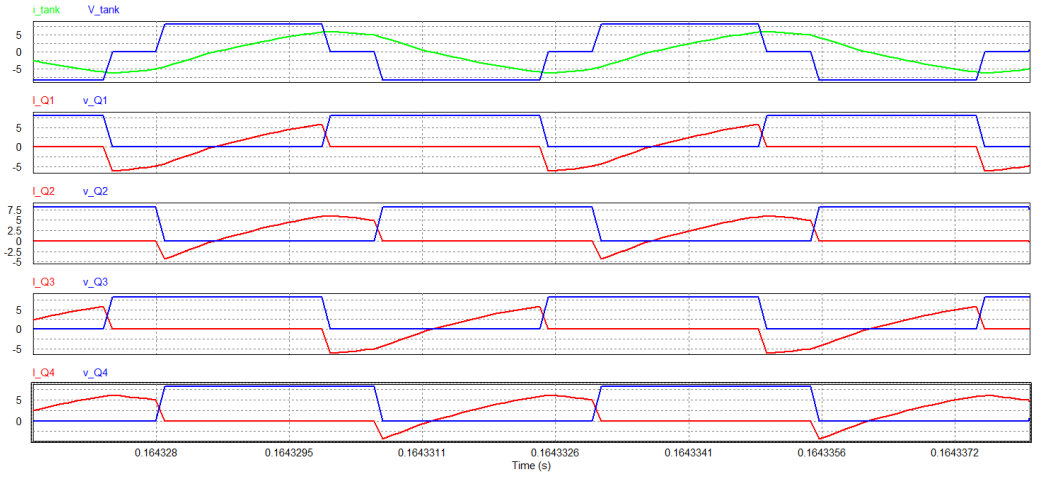
$$L_r = 69.9\ \mu H \qquad\qquad C_r = 23\ nF$$

4.5 Simulation Results

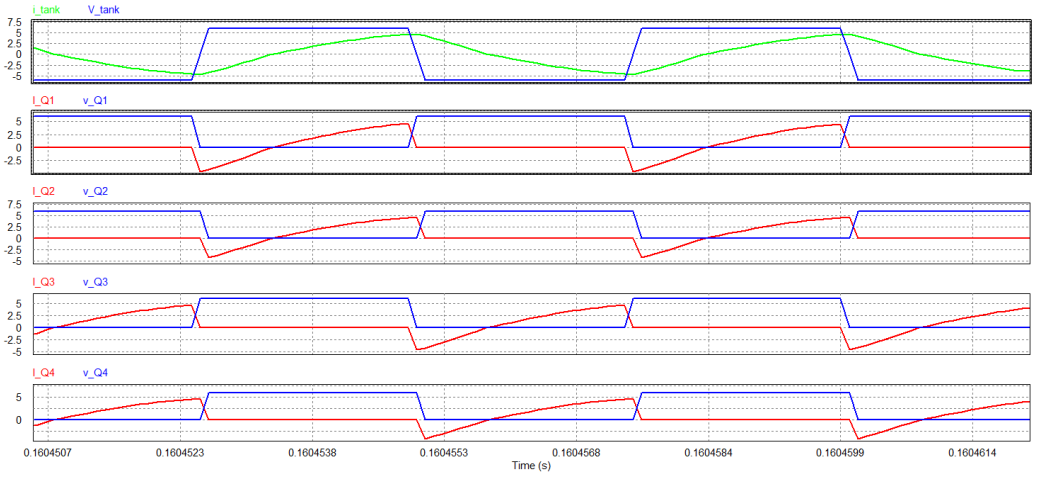
Fig. 4.13 shows the switching voltage and currents of SRC during all modes of operation. As it's shown in the Fig. 4.13(a) at peak of SRC's input voltage, the phase shift between switches Q_1 and Q_2 makes the H-Bridge output voltage to dwell on zero for a portion of the cycle. Zero voltage switching turn ON is achieved in every mode during the operation. As shown in Fig. 4.13(b), the output voltage of H-Bridge is similar to bipolar PWM switching method and has two levels due to implementation of zero phase shift to facilitate maximum power flow form DC link to output. V-I waveforms of the switches in this figure demonstrates achieving ZVS turn ON in all modes of operation.

4.6 Summary

In this chapter a series resonant converter (SRC) topology is used which enhances the proposed LED driver with isolation, high efficiency due to soft-switching, and high power density. Phase shifted PWM is used to control the current in LED strings corresponding to the variation in input voltage of SRC. This chapter presents a brief introduction about the SRC topology, soft switching actions and phase shifted PWM switching method. Further through the chapter, SRC principle of operation is presented by describing all the operation modes. Steady state analysis and design is presented, and Laplace Based Theorem (LBT) is used as a systematic tool to obtain design parameters for the series resonant converter.



(a)



(b)

FIGURE 4.13: ZVS in SRC switches throughout the operation modes:
(a) During the peak of DC link voltage, (b) During the valley of the DC link voltage

Chapter 5

Magnetic Design

5.1 Overview

When it comes to the design of a magnetic component like an inductor or a transformer, the electrical characteristics is not the only focus point. Analyzing the magnetic fields associated with these components may come off as important as designing the electrical characteristics that is observed in the terminals of the device.

The importance of magnetic design for power electronics components yet becomes more visible when the high frequency application introduces a high amount of eddy current losses which cannot be seen through electrical modeling. Also when the packaging and size of the magnetic component is of much importance, magnetic design can aid to obtain an optimal size for the component.

The category choice for magnetic design always falls into one of the three groups of saturated thermally limited, non-saturated thermally limited, and signal quality limited designs. The choice of design category is empirical, and made by measuring the input design parameters like RMS and peak value of the current, insulation requirement, and peak to peak flux [33].

For the Proposed LED driver in the project, three magnetic components consisting of a transformer and a resonance inductor for series resonant converter, and a filter inductor for boost PFC have been designed.

5.2 Non-saturated thermally limited design

Having peak flux lower than the ferrite saturation limit puts the resonant magnetic components in the unsaturated category.

The flow chart in Fig. 5.1 shows the procedure for designing a component under non-saturated thermally limited category.

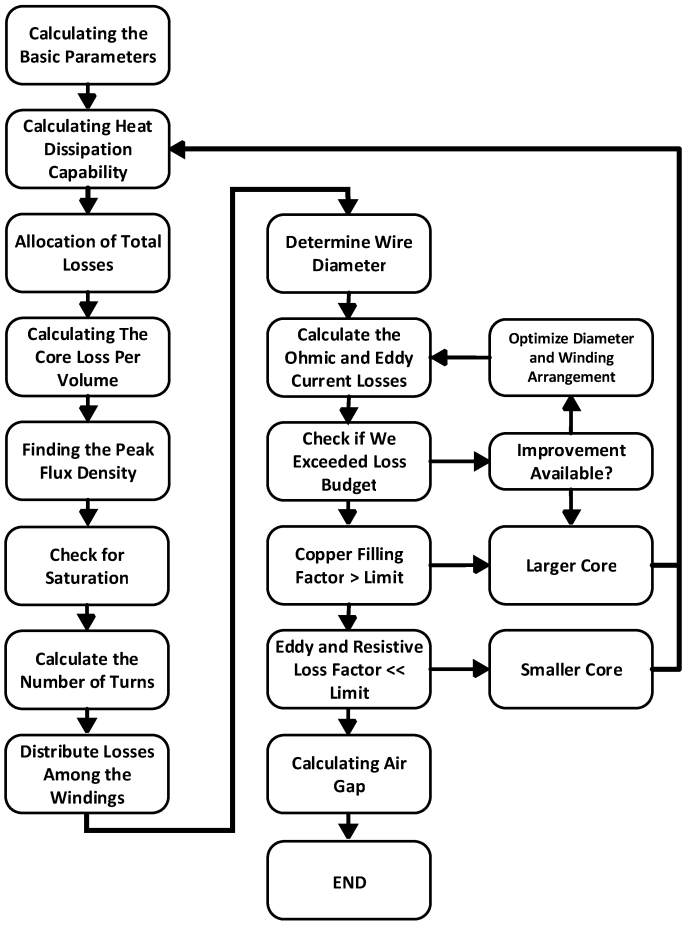


FIGURE 5.1: Magnetic Design Flow Chart for Non-Saturated Components

Fig. 5.1 depicts the design steps for non-saturated components with respect to thermal limitations. Since the AC fluctuations are rather small and the peak flux doesn't exceed the saturation limit for ferrite material in our resonant inductor and transformer, the deign falls into the Non-Saturated thermally limited group. However, the design category choice is practical and if the measurements and calculations in further steps wouldn't be consistent with the design category choice, the other category options can be applied.

Design steps are the same for both transformer and inductor. However, a slight difference comes in calculation of number of turns and also determining the air gap. As it is shown in the flow chart, the design procedure starts with calculation of some parameters like RMS and Peak value of the winding currents and peak to peak flux linkage. Which in turn, would lead to the understanding of the limitations for the design.

After the input parameters are calculated, thermal design of the component takes place. Thermal design gives an insight of the size of the core that can be used. Calculation of the number of turns, current losses, wire sizes, and also optimizing the size of the component can be achieved further through the design steps.

5.2.1 Core Shape and Material

First step of designing a magnetic device is to determine the shape and material of the core corresponding to the application that magnetics are designed for. Choosing the right magnetic material is of high importance since the amount of the flux that goes through the magnetic component in the presence of magnetic field, can drastically change with the type of material that is selected for the component.

Soft ferrites are a commonly used in power conversion applications because their magnetization can easily be reversed without dissipating lots of energy and hence, having a low hysteresis loss. Among ferrite materials, 3F3 material have been used because of higher permeability and low losses in high frequencies.

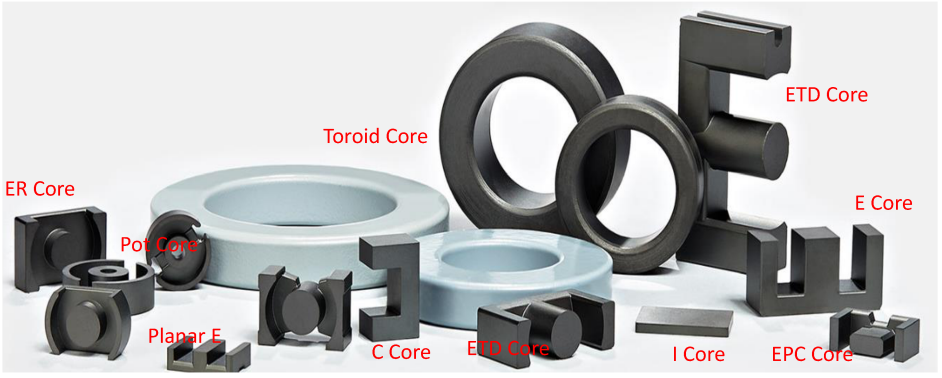


FIGURE 5.2: Ferrite Core Shapes; image courtesy of Magnetic.inc

Different applications impose certain requirements for the core geometry, material and heat dissipation capabilities. The table 5.1 shows different characteristics associated

TABLE 5.1: Ferrite Core Shape Characteristics; courtesy of Magnetic.inc

	Toroid	**E**	**ETD**	**ER,Planar**	**Pot Core**	**RM Pot Core**
Core Cost	Very Low	Low	Medium	Medium	High	High
Bobbin Cost	None	Low	Medium	None	Low	Low
Winding Cost	High	Low	Low	Low	Low	Low
Winding Flexibility	Fair	Excellent	Excellent	Poor	Good	Excellent
Assebly Difficulty	Simple	Simple	Simple	Medium	Simple	Medium
Mounting Flexibility	Poor	Fair	Fair	Poor	Good	Good
Heat Dissipation	Good	Good	Good	Excellent	Poor	Excellent

with each core shape.

As it has been shown in the table 5.1, good heat dissipation, low winding cost and excellent winding flexibility are characteristics of E and ETD type cores. Hence, these cores have been chosen for the LED driver prototype. E and ETD shape cores are widely used in power electronics applications as using the air gap in the center leg can also minimize the fringing effects and reduce EMI

5.2.2 Core Size

For the design of resonant transformer, after determining the core shape in the first step, core size should be estimated. For this matter, the equation 5.1 is used to assess and compare the ability of core sizes of a certain shape to meet the volt-ampere rating of the component.

$$S_{tot} = \sum V_{i,rms} I_{i,rms} = A a_{ch}^{\lambda} \Rightarrow a_{ch} = \left(\frac{S_{tot}}{A}\right)^{\frac{1}{\lambda}} \tag{5.1}$$

where

S_{tot} is the volt-ampere rating of the component
a_{ch} is largest dimension of the component in m

Symbols

A is a coefficient for ferrite, Usually in the range of $(5-25)*10^3$ (if a_{ch} is in $[m]$)
λ is an exponent, characterizing the material and the shape of the core, $\lambda = 3$

$$\begin{cases} V_{in,rms} = 95.64\ V \\ I_{in,rms} = 2.4515[A] \\ V_{out1,rms} = V_{out2,rms} = 51\ V \\ I_{out1,rms} = I_{out2,rms} = 2.26\ A \end{cases} \xrightarrow{A=20*10^3} \begin{cases} S_{tot} = 464.85\ VA \\ a_{ch} = 28.5\ mm \end{cases} \tag{5.2}$$

As the largest dimension for the core has been calculated 2.88 cm, the EE 32/16/9 ferrite core has been chosen with the below characteristics:
$l_e = 74\ mm$, $A_e = 83\ mm^2$, $V_e = 6140\ mm^3$
where
l_e is the effective magnetic path length in mm
A_e is the effective magnetic cross section in mm^2
V_e is the effective magnetic volume in mm^3

Applications with higher frequencies have the higher value for ferrite coefficient $A = (20-25)*10^6$, and applications with lower frequencies $(20-30\ kHz)$ have the lower value of A. Also eddy current effect and insulation requirements necessitate decrease in chosen value for A.

5.2.3 Heat Dissipation and Allocation of Losses

Designing a magnetic component for any certain power electronic application requires calculating the operating temperature. Any negligence of the temperature rise and ambient temperature might result in an inviable design. Yet, temperature sensitivity for individual applications may vary. Hence, intricate thermal modeling of convection and heat radiation is not needed in every design and simplified model would suffice.

For the purpose of determining the heat dissipation capability of a component, an approximate approach is to neglect all the (small) horizontal surfaces and to just take into account the largest horizontal surface and the height of the component. The heat dissipation capability of the component then will be calculated with the equation 5.3.

$$P_h = k_A * a * h \tag{5.3}$$

Where

P_h is the allowable loss budget that will guarantee the temperature rise under 50°C in W

a is the largest horizontal dimension of the core in m

h is the height of the core in m

k_A is coefficient for ferrite power dissipation rate and falls within the range of $1500 - 2500 \ \frac{W}{m^2}$

Although the value of $1500 - 2500 \ \frac{W}{m^2}$ can be used for most of the applications for ferrite materials, it's suggested to use the value of $k_A = 1500 - 2500 \ \frac{W}{m^2}$ for the applications with ambient temperature of 60°C or more.

$$P_h = 2500 * 0.032 * 0.032 = 2.56 \ W$$

The above calculation indicates that for the chosen $EE32/16/9$ core, there is a total of 2.56 W allowable loss budget that will guarantee less than 50°C of temperature rise. This total loss would be distributed between copper and core. Two largest dimensions of the chosen $EE32/16/9$ core are 0.032 m and the value for k_A has been chosen $2500 \ \frac{W}{m^2}$. $k_A = 2500 \ \frac{W}{m^2}$ would allow for temperature rise of 50°C for ferrite transformers.

5.2.4 Optimal Core/Copper Loss Ratio

In the design of magnetic components, there is a trade-off between core losses and copper losses. Hence, the focus point of the design will determine that the greater portion of loss budget should be allocated to either maximum flux density/core losses or eddy and ohmic losses of the windings.

In general, the optimal maximum efficiency which results in a minimum power loss has been shown to be obtained when copper loss and core losses have the same share in loss budget.

$$P_{h,fe} = P_{h,cu} = \frac{P_h}{2} \tag{5.4}$$

Where

$P_{h,fe}$ is the allowed core loss in W

$P_{h,cu}$ is the allowed copper loss in W

$$P_{h,fe} = P_{h,cu} = \frac{P_h}{2} = 1.28\ W$$

5.2.5 Core Loss Per Volume

Given the data collected from the chosen core data sheet, the volume of the core is known. To find peak flux density for a core of a certain material, one should refer to the coherence between peak flux density and core loss per volume which is often presented in core data sheets. Core loss per volume, $P_{fe,sp}$, for ferrite cores is calculated as follows:

$$P_{fe,sp} = \frac{P_{h,fe}}{1000 * V_e}\ \frac{mW}{cm^3} \tag{5.5}$$

$$P_{fe,sp} = \frac{P_{h,fe}}{1000 * V_e}\ \frac{mW}{cm^3} = \frac{1.28}{6140 * 10^{-9} * 1000} = 208.469\ \frac{mW}{cm^3}$$

5.2.6 Peak Flux Density

Peak flux density can be obtained from the graphs in data sheets with regard to a set of characteristics like core loss per volume, temperature, and operating frequency. As these factors are known at this step of the design. Peak flux density can be calculated as follows.

$$P_{fe,sp} = k_{fe} * f^{\alpha} * B^{\beta} \tag{5.6}$$

Fig. 5.3 depicts the Steinmetz equation $P_{fe,sp} = k_{fe} * f^{\alpha} * B^{\beta}$, where

k_{fe} is the core loss coefficient

α is the frequency exponent

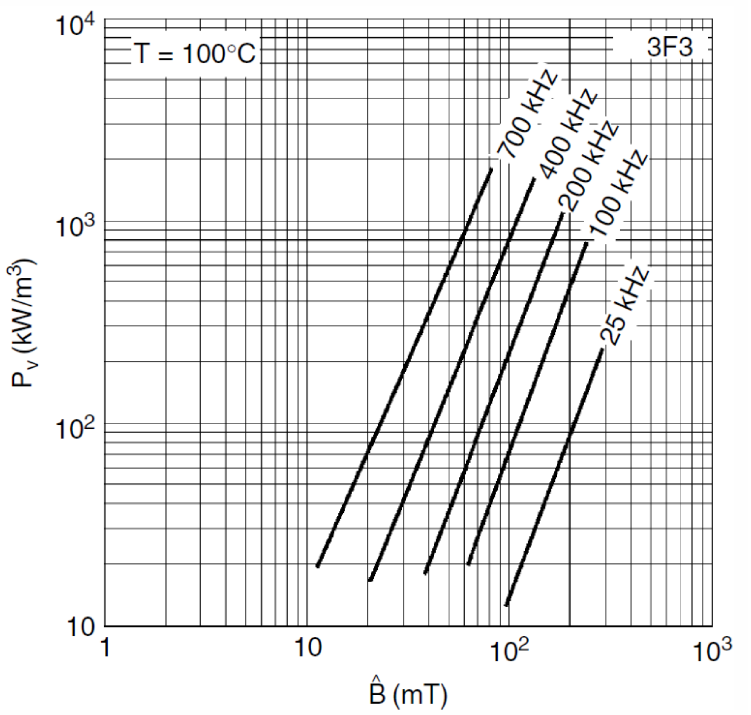


FIGURE 5.3: Core loss per volume as a function of Peak flux density for 3F3 ferrite material @100°C and operating frequency as the changing parameter [33]

B is the peak to peak value of the flux density

f is the operating frequency

The core loss per volume exponent, β, can be calculated by doing a logarithmic interpolation.

$$\beta = \frac{\log \frac{P_{f_{e,sp,2}}}{P_{f_{e,sp,1}}}}{\log \frac{B_2}{B_1}} \tag{5.7}$$

Using two points on the graph according to $200kHz$ operating frequency, The value for peak flux density can be calculated as follows:

@ 100°, 200 kHz, and 0.04 T the core losses are 10 $\frac{W}{m^3}$: First point

@ 100°, 200 kHz, and 0.0975 T the core losses are 200 $\frac{W}{m^3}$: Second Point

$$\beta = \frac{\log \frac{200}{10}}{\log \frac{0.0975}{0.04}} = 3.3623 \tag{5.8}$$

Since the value of the core loss per volume is known, the Peak flux density for 3F3 material according to the chosen points on the Fig. 5.3 can be calculated with the equation:

$$B_{pg} = B_1 * \left(\frac{P_{f_{e,sp}}}{P_{f_{e,sp,1}}}\right)^{\left(\frac{1}{\beta}\right)} \tag{5.9}$$

$$B_{pg} = 0.04 * \left(\frac{208.469}{10}\right)^{\left(\frac{1}{3.3623}\right)} = 0.0987\ T$$

As it has already been mentioned earlier at the beginning of the chapter, design procedure is developed for non-saturated thermally limited applications. It's necessary to check if the obtained peak flux density will exceed the saturation limit for the certain core material that is being used.

In [4], saturation level for a series of frequently used core materials at $100°C$ have been enumerated as follows:
As for energy conversion purposes, most ferrite have the saturation limit of $0.35\ T$. Saturation level for laminated iron cores is typically ranged between $(1.5 - 1.7)\ T$, and for soft magnetic materials, such as noncrystalline iron, saturation happens at about $(1.2 - 1.5)\ T$.

The peak to peak value for flux density is $B_{pp} = 2 * 0.0987 = 0.1974\ T$. This value is smaller than $0.350\ T$ which confirms the non-saturated operation.

5.2.7 Number of Turns

Calculating the number of turns has a slightly different approach for inductors and transformers design in which both approaches will be covered in this section. Some applications require a certain turn ratio that needs to be followed when designing the number of turns. As for the case of series resonant converter, achieving soft switching cannot be done unless a certain designed turn ratio between primary and secondary/ tertiary windings would be followed.

5.2.7.1 Transformer Calculation

In order to calculate the number of turns in a magnetic component, the flux that runs through the component should be calculated. To determine the flux linkage in a transformer, voltage waveform from the terminals of the device has to be monitored. When the v-t graph is obtained, the area under the voltage waveform in a half cycle will determines the peak to peak value for flux linkage.

$$\int_{t_1}^{t_2} v(t)d\tau = \psi_{pp} = V_1^* \frac{T}{2} \tag{5.10}$$

$*V_1$ is the voltage of the primary winding.

Another variable to be calculated is peak to peak flux, the cross section of the core and the peak to peak flux density are known. The peak to peak flux can be calculated as follows:

$$\phi_{pp} = B_{pp} * A_e = 2 * B_{pg} * A_e \tag{5.11}$$

Having the peak flux linkage and and peak to peak flux known, the number of turns for primary windings can be calculated. Number of turns for other windings can be determined through utilizing turn ratios.

$$N_1 = \frac{\psi_{pp}}{\phi_{pp}}, ..., N_i = N_1 \frac{V_i}{V_1}$$

5.2.7.2 Inductor Calculation

The peak to peak value of the current going through the inductor is to be used for determining the flux linkage.

$$\psi_{pp} = L * I_{pp} \tag{5.12}$$

The calculation of peak to peak flux and number of turns are the same as the transformation design approach.

$$\phi_{pp} = B_{pp} * A_e = 2 * B_{pg} * A_e$$

$$N = \frac{\psi_{pp}}{\phi_{pp}}$$

The Series Resonant Converter (SRC) transformer has a turn ratio of 1.85 : 1 : 1 for achieving the ZVS. Fig. 5.4 shows the voltage waveform of the primary windings of the resonant transformer that has been obtained using PSIM software, calculation of the area under the voltage waveform in a half cycle determines the flux linkage value.

$$\psi_{pp} = \int_{T}^{\frac{3T}{2}} v(t)d\tau = 2.22 * 10^{-4}$$

$$\phi_{pp} = B_{pp} * A_e = 8.3 * 10^{-5} * 0.1974 = 1.6386 * 10^{-5}$$

$$N_1 = \frac{\psi_{pp}}{\phi_{pp}} \approx 13.55$$

The chosen number of turns for primary winding, $N_{1,p}$, is 13. Secondary and tertiary number of turns can be determined by the turn ratio and chosen value of $N_{2,p} = N_{3,p} = 7$.

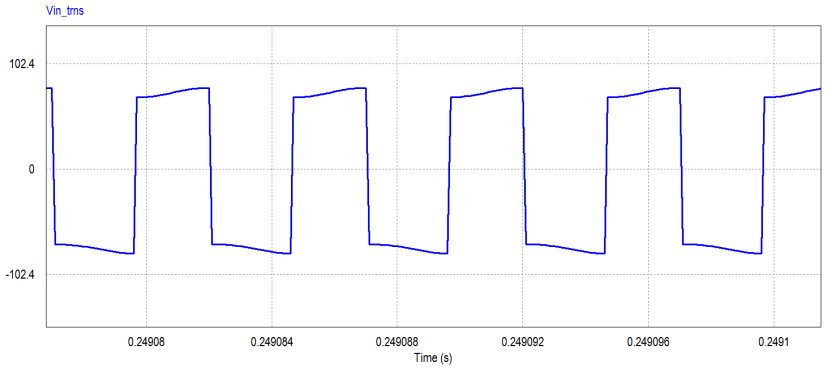


FIGURE 5.4: Primary winding voltage of resonant transformer

It's worth noticing that the previous calculations for the peak flux density should undergo a change. Since the previously calculated peak flux density led to a number of turns that was calculated, the chosen number of turns would have different peak flux density associated with it. consequently, the value for core loss will be changed as the peak flux density changes.

$$\begin{cases} B_{new} = B * \dfrac{N_1}{N_{1,p}} \\ P_{f_{e,sp}} = 10 * (\dfrac{B_{new}}{0.04})^{\beta} \end{cases} \Rightarrow P_{h,fe} = P_{f_{e,sp}} * V_e * 1000 = 1.4707\ W \qquad (5.13)$$

The previously calculated budget for core loss was 1.28 W but the practical design with introducing slightly different number of turns, set the core loss to 1.4707 W

5.2.8 Distribution of Winding Losses

The wire diameter for each winding is subjected to the power that the winding should withstand. In the equation 5.14 , a coefficient corresponding to the volt-ampere applied to each winding is calculated. Further on, through the equation 5.15, the wire diameter for each winding is calculated.

$$\alpha_n = \frac{N_n * I_n}{N_1 * I_1 + N_2 * I_2 + ... + N_n * I_n + ...} \tag{5.14}$$

These coefficients will be used to distribute the total volt-amperes among the windings

$$P_{cu,i} = \alpha_i * P_{h,cu}$$

Where

$P_{cu,i}$ is the allocated loss for the i_{th} winding
α_i is the loss distribution coefficient corresponding to the i_{th} winding
$P_{h,cu}$ is the total allocated loss budget for the copper

5.2.9 Wire Diameters

Having the allowed copper loss for each winding determined, wire diameters for each winding can be calculated using equation 5.15.

$$\begin{cases} P_{cu,i} = R_{ohm,i} * I_{rms,i}^2 \\ \\ R_{ohm,i} = \frac{\rho l_{Ti} N_i}{\frac{\pi d_i^2}{4}} \end{cases} \Rightarrow d_i \geq \frac{2}{\pi} I_{rms,i} \sqrt{\frac{\rho l_{Ti} N_i}{P_{cu,i}}} \tag{5.15}$$

Where

Symbols

$R_{ohm,i}$ is the DC resistance of the i_{th} winding

$I_{rms,i}$ is the RMS current of the i_{th} winding

ρ is the electrical resistivity of the copper wire

$P_{cu,i}$ is the total copper loss budget found in equation 5.4

l_{Ti} is the mean-length-per-turn of the i_{th} winding (indicated in bobbin data sheet).

Note that the used l_{Ti} is for fully wounded bobbin and hence, the calculated $P_{cu,i}$ is designed with an accepted approximation.

Calculations for the 3 winding transformer are as follows:

$$\alpha_1 = \frac{N_{1,P} * I_{in,rms}}{N_{1,P} * I_{in,rms} + N_{2,P} * I_{out1,rms} + N_{3,P} * I_{out2,rms}} = 0.5018$$

$$\alpha_2 = \alpha_3 = 0.2491$$

$$P_{cu,1} = \alpha_1 * P_{h,cu} = 0.6232\ W$$

$$P_{cu,2} = P_{cu,3} = 0.3188\ W$$

having the allowed copper losses, $P_{cu,i}$, determined and distributed over the corresponding windings, the wire diameter d_i can be determined.

$$d_1 = \frac{2}{\pi} I_{in,rms} \sqrt{\frac{\rho l_{T1} N_{1,p}}{P_{cu,1}}} = 0.4789\ mm$$

$$d_2 = d_3 = 0.4598\ mm$$

Practical value for wire diameters, $d_{i,p}$, is slightly higher than the calculated value. Usually the common approach is to choose the next available diameter (the bigger diameter value) when the wires are to be chosen from the American Wire Gauge (AWG) chart. Choosing a slightly larger value for diameter will help reducing the ohmic losses as the DC loss of a copper wire is reversely related to the wire thickness. Yet, extra care must be taken since the larger value for diameter will also allow for larger eddy current losses in which will be further detailed in the section 5.2.12.

In the design of transformers, the calculated wire diameters may not be enough to fill a whole bobbin winding width. A good practice is to enlarge the diameters until a full layer is filled (considering the insulation and required creepage distance between

primary and secondary windings). However, although increasing the thickness of the copper wire for the sake of filling the entire bobbin winding width will improve the DC loss status, but it can increase the eddy current losses to an impractical level. In this case the optimum solution would be to either use the wires as a bundles (parallel wires) or to use Litz wire. The design consideration regarding the use of Litz wire will be further described.

In case of using bundled wires in parallel, the same flux should flow through each wire equally. Twisting the bundle of wires would be the solution and it has been already employed in Litz wires.

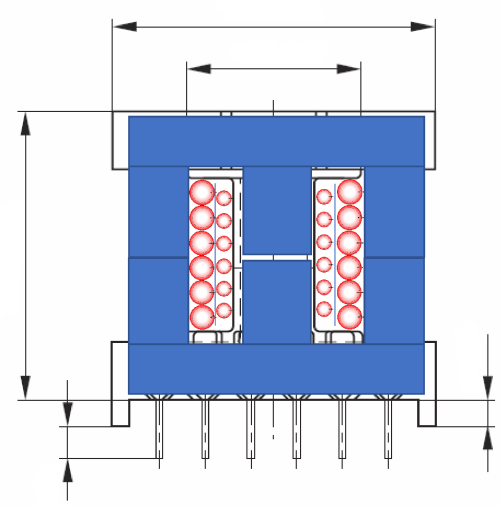


FIGURE 5.5: Bobbin, Core, and Wires Structure

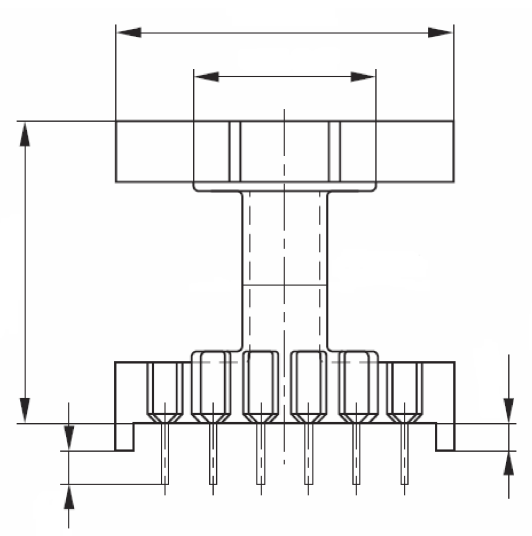


FIGURE 5.6: Bobbin Structure

The graphical winding height and the minimum winding width are shown in the Fig. 5.6

Information related to the window area for the chosen core and bobbin are as follows.
Winding Height = 6 mm Minimum Winding Width = 19 mm
According to the determined number of turns, the largest diameter that can fit the winding width can be calculated.

Number of turns (Primary—Secondary—Tertiary) = 13 : 7 : 7

$$\frac{19}{13} = 1.4615mm \longrightarrow primary \xrightarrow{AWG16} d_{1,p} = 1.29mm$$

$$\frac{19}{7} = 2.7143mm \longrightarrow Secondary|Tertiary \xrightarrow{AWG11} d_{2,p} = d_{3,p} = 2.3048mm$$

The calculated wire diameters in the previous step, $d_1 = 0.4789mm$ and $d_2 = d_3 = 0.4598mm$ are considerably smaller than the ones designed here and although the ohmic losses will be improved in this design, the question would arise regarding the effects of increasing the cross section area on the losses introduced by magnetic fields.

5.2.10 Litz Wire, Skin and Proximity Effect

5.2.10.1 Skin Effect

The DC resistance of a conductor is inversely dependent to its cross section area. Meaning that the thicker the conductor is, the smaller the DC losses will be. Yet the mechanism of the current flow through the conductor, supposedly copper wire, is different for AC currents of higher frequencies. The resistance also depends on the frequency and a concept called skin depth, δ, is introduced for AC currents. Fig. 5.7 shows that in the presence of higher frequencies, the current tends to flow near the surface of the wire and the wire's interior area doesn't carry much current. Hence, skin depth, δ, is relatively small compared to the wire's thickness. Using this smaller area to flow the current would increase the resistance of the wire.

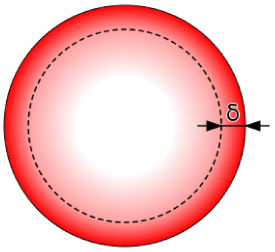


FIGURE 5.7: Skin Effect in conductors

5.2.10.2 Proximity Effect

Alternative current will result in a changing magnetic field around the wire carrying the current. The magnetic field itself, will distort the distribution of the current in wires that are in it's proximity.

According to the Fig. 5.8, the mechanism of inducing the eddy current in the adjacent wire is as follows:

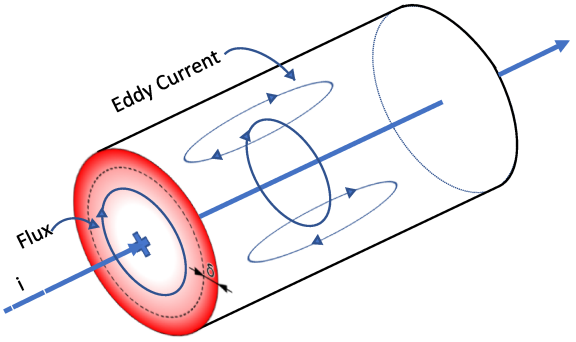


FIGURE 5.8: Eddy current in conductors

Magnetic field would create an eddy current loop in the adjacent wire. The eddy current is flowing length-wise and the loop is shaped in the way that the induced current in the adjacent wire will go through the same direction in the side that is facing away from the original wire and it would go through the opposite direction on the side that is closer to the original wire. Hence, the proximity effect results in a state where the magnetic field associated with two adjacent wire will cause the current to be concentrated in the furthest distance (In case the currents are in the same direction in two conductors) or for the currents to be concentrated in the closest distance (when the currents flow in the opposite direction in two adjacent wires).

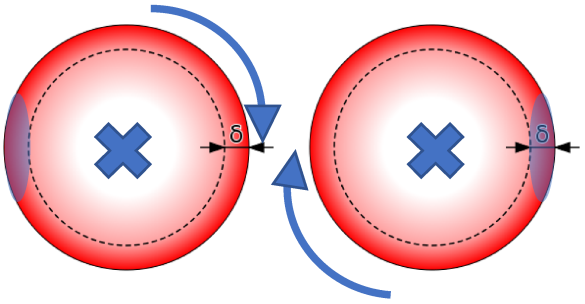


FIGURE 5.9: Proximity Effect: Concentration areas shown in blue highlight

Fig. 5.9 shows that for AC currents at higher frequencies, not only skin effect will reduce the penetration depth (δ), causing current not to utilize the full cross section area of the wire, but also proximity effect will concentrate the current on a smaller section of the allowed depth (highlighted in blue). The overall used area of the wire's cross section will be limited to a very small portion in higher frequencies that causes eddy current losses to easily exceed even tens of times more than DC losses.

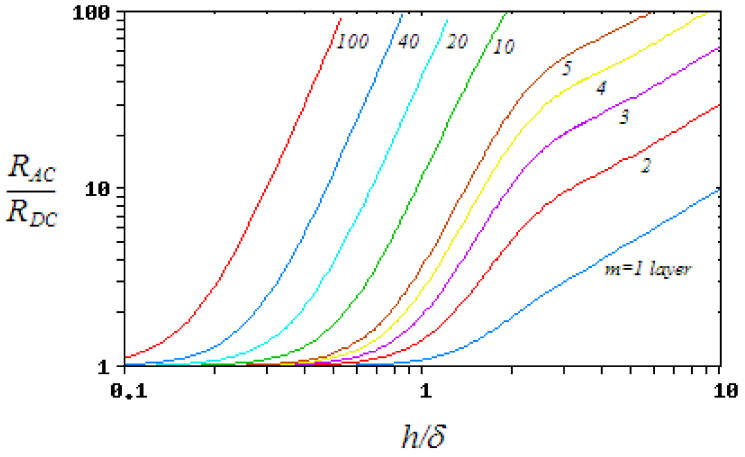


FIGURE 5.10: $\frac{R_{AC}}{R_{DC}}$ ratio for different number of layers and frequencies
h is the wire diameter and δ is the penetration depth
image courtesy of wikipedia.com

The above statement approves the fact that in the presence of time variant magnetic fields associated with the high frequency AC currents, using larger diameters for the conductor or configuring the conductors in more layers doesn't necessarily improve the overall amount of losses.

Fig. 5.10 shows the $\frac{R_{AC}}{R_{DC}}$ ratio for different number of layers and different frequencies (as penetration depth decreases with the increase in frequency). The figures have been elicited from Dowell's method for obtaining the $\frac{R_{AC}}{R_{DC}}$ ratio. The method is one dimensional and does not feature the best accuracy. Yet it can show that the increase in number of layers can dramatically increase the eddy current losses in conductors.

5.2.10.3 Litz Wire

The following formula calculates the penetration depth.

$$\delta = \sqrt{\frac{2\rho_{cu}}{\omega\mu}} \tag{5.16}$$

where

$\omega = 2\pi f$ is the frequency of the applied magnetic field

μ is the permeability of the conductive material

ρ_{cu} is the electrical resistivity of the material (Copper) at $100°C$

Penetration depth goes smaller with higher frequencies and the skin and proximity effect would cause eddy current losses, Litz wires are introduced to address the issue. The underlying concept for the special structure of these wires is to reduce the diameter smaller than the skin depth. Hence, the whole cross section area of the wire can be utilized. For this matter, Litz wires are manufactured as a bundle of strands. Each strand has a diameter smaller than penetration depth and is insulated from the other strands. All the strands are twisted and bundled together to form a wire.

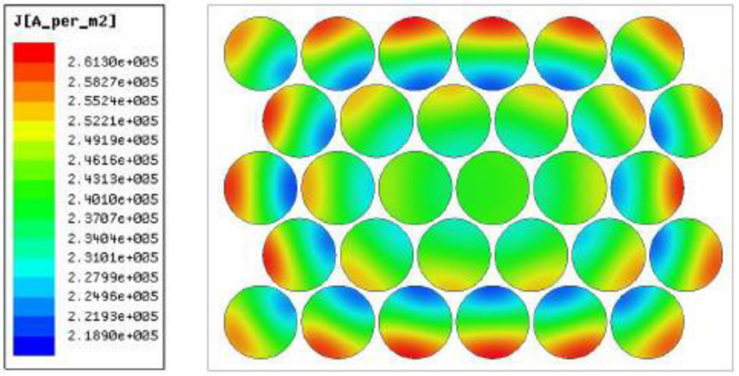


FIGURE 5.11: Combined skin and proximity effect on Litz wire [3]

Researchers in [3] have assessed the current density distribution with sinusoidal excitation $I_{rms} = 1A$ at $16kHz$ for a Litz wire with $30 * 0.5mm$ strands. Fig. 5.11 Depicts the result of the simulation. Current density through the cross section area of the Litz wire shows a very promising increase in the current density in the center of the wire. Yet if the individual strands were not insulated and would be short circuited, the whole bundle of wires would act as a single large wire. Carrying insignificant amount of current at the center. The operating frequency plays a crucial part in the choice of Litz wire construction and also wire gauge.

Table 5.2 shows that as the operating frequency rises, penetration depth would grow smaller and subsequently, the litz wire strands have to be chosen from a smaller diameter options. The table also shows insignificant change in the $\frac{R_{AC}}{R_{DC}}$ ratio as the operating frequency increases.

TABLE 5.2: $\frac{R_{AC}}{R_{DC}}$ for single strand in Litz Wire

Frequency	Wire Guage	$\frac{R_{AC}}{R_{DC}}$
$60Hz - 1kHz$	AWG 28	1.0000
$1kHz - 10kHz$	AWG 30	1.0000
$10Hz - 20kHz$	AWG 33	1.0000
$20Hz - 50kHz$	AWG 36	1.0000
$50Hz - 100kHz$	AWG 38	1.0000
$100Hz - 200kHz$	AWG 40	1.0000
$200Hz - 350kHz$	AWG 42	1.0000
$350Hz - 850kHz$	AWG 44	1.0003

Selection of Litz wire for the LED driver transformer design is as follows:

Considering the operating frequency of $200kHz$,The wire gauge for each strand in Litz wire should selected from AWG 38 or larger. Having AWG 38 selected as the wire diameter for each strand, the next step is to check the manufacturers data sheet to see how many strands should be bundled together to form the desired outer layer diameter (Also considering the wrapping and insulations for the outer layer).

$$\frac{19}{13} = 1.46\ mm \longrightarrow d_{Primary}$$

$$\frac{19}{7} = 2.71\ mm \longrightarrow d_{Secondary|Tertiary}$$

Taking the window area and winding height ($6\ mm$) into consideration, diameters of above scales are large and will exceed the window area limitation. Wrapping and insulations for the desired outer layer of the Litz wire would also limit the available winding space. The number of strands in Litz wires are chosen in the way that the outer layer of each Litz wire is large enough to fill the winding length and also to optimally use the whole window area

Litz wire diameters are chosen as follows:

Primary Windings: 100 strands of $AWG38$ wires - Single layer silk wrapping

$$d_{1,p,single} = 0.101\ mm \longrightarrow d_{Strand}$$

$$d_{1,p,outer} = 1.516\ mm \longrightarrow d_{Bundle}$$

Winding Width = $16.676\ mm \longrightarrow Utilized\ Length$

Secondary — Tertiary Windings: 140 strands of $AWG38$ wires - Single layer silk wrapping

$$d_{2,3,p,single} = 0.101\ mm \longrightarrow d_{Strand}$$

$$d_{2,3,p,outer} = 1.69\ mm \longrightarrow d_{Bundle}$$

Winding Width = $11.83\ mm \longrightarrow$ *Utilized Length*

5.2.11 Determining The Copper Loss

Copper loss can be determined as a summation of ohmic and eddy current losses. While determining the eddy current losses requires complicated calculation compared to DC losses, a quick determination of DC losses will give an insight to the designer on whether the chosen diameters of the wires are sufficiently large or not.

5.2.11.1 Ohmic Losses

Ohmic loss $P_{cu,ohm}$ for all the windings is inversely proportional to the cross section area of the wire.

Ohmic losses for a Litz wire can be calculated as follows:

$$R_{ohm,i} = \frac{1.5\rho l_{Ti} N_i}{\frac{\pi d_{i,p,single}^2 P}{4}} \tag{5.17}$$

Where:

P is the number of strands in a Litz wire

l_{Ti} is the mean-length-per-turn of the i_{th} winding (indicated in bobbin datasheet)

N_i is the number of turns for the the i_{th} winding

$d_{i,p,single}$ is the diameter of an individual strand (i_{th} strand)

P is the number of strands in the Litz wire

In the special case of using Litz wire, the calculation is multiplied by 1.05 because of the 5% increase of the wire actual length due to twisting of the bundle.

$$R_{ohm,1} = 1.05 * \frac{23 * 10^{-9} * 56 * 10^{-3} * 12}{\frac{\pi * (0.10123 * 10^{-3})^2 * 105}{4}} = 0.0252\Omega$$

$$R_{ohm,2} = R_{ohm,3} = 0.0097\Omega$$

$$P_{ohm,1} = R_{ohm,1} I_{in,rms}^2 = 0.1517W$$

$$P_{ohm,2} = P_{ohm,3} = 0.0496W$$

5.2.12 Eddy Current Losses

Soft switching approaches used in the resonant converters facilitate the operation of circuits in high frequencies. As a result, design of magnetic components are subjected to much more influence by eddy current losses associated with time variant magnetic fields, rather than DC losses.

5.2.13 Calculation methodology

A classic method for calculating the eddy current losses is developed by Deowell. The method can approximate the $\frac{R_{AC}}{R_{DC}}$ as shown in the Fig. 5.10. Dowell's approach is one dimensional and assumes the wire in the transformer windings to have rectangular cross section. The common approach for using Dowell's method is to assume circular wire like the rectangular one with the same cross section area.

Yet the Dowell's approach introduces lots of shortcomings as it loses accuracy for the designs with low filling factor (distance between the wires in a row or column). Transition between round to square conductors causes errors and also the presence of air gaps and its effect on the magnetic fields hasn't been addressed [4].

The approach for calculating the eddy current losses is called wide frequency approach [4] in which, will address all the shortcomings of Dowell's method and provides more accurate result based on considering all the transverse (eddy current-based) and local(main current-based) magnetic fields. The approach also takes the winding structure and core shape into account. Hence, understanding the factors contributing to the calculation is necessary.

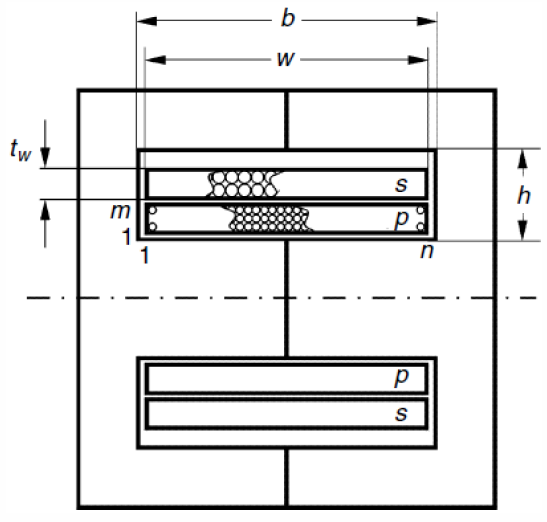


FIGURE 5.12: Magnetic Component Structure [4]

Fig. 5.12 will provide a graphic presentation of the factors and variables used in the calculations and shows the details of winding area parameters.
where

P and S are primary and secondary windings
t_w is winding thickness
w is minimum winding width
m is number of layers for each winding
n is number of turns in a layer
d_{wg} is distance of windings from the center leg
h is window area height
b is window area length

In case of using P parallel wires in the same layer:
$n_E = n * P$ is equivalent number of wires in a layer
$m_E = m$ is equivalent number of layers

In case of using Litz wire with P strands in each wire:
The exact number of layers or individual wires in a layer cannot be counted. Therefore, the equivalent distribution of strands in both directions will result in:
$n_E = n\sqrt{P}$ is equivalent number of wires in a layer
$m_E = m\sqrt{P}$ is equivalent number of layers

After defining the parameters related to winding area, the equations in which will characterize magnetic fields and calculate eddy current losses can be presented.

$$\lambda = \frac{dm_E}{w}$$

$$\eta = \frac{dn_E}{w}$$

Wires inside the winding area of the bobbin need insulation, and in most practical arrangements, they are placed with a certain amount of space between them. Spaced conductors would make vertical fields along side with the typically calculated horizontal fields.

The copper filling factor in a row that a layer of wires is laid down, is denoted as η. Also λ is filling factor perpendicular to the layer. Filling factors are introduced to take vertical fields into account and provide more accurate assessment of eddy current losses.

$$\kappa = \frac{dwg + \frac{t_w}{3}}{\frac{w}{K}}$$

$$k_F = \frac{3.5(0.5 - \kappa)^2 + 0.69}{\kappa}$$

Field symmetry factor K is introduced to account for different winding patterns (Half layer, interleaved) and shape of the core into calculation of eddy current losses. Fig. 5.13 depicts different core shapes and winding structures and their corresponding field symmetry factor.

The field over the winding cross section area increases almost linearly from zero to its maximum value but as for the inductors with air gap in the center leg, the field pattern is not the same near the air gap area. Field Factor k_F accounts for the field pattern near the air gap, and κ is another parameter which reflects the relative distance between the winding and the air gap.

$$\zeta(f) = \frac{d}{\delta(f)}$$

$$\chi(f) = \frac{1}{1 + \frac{1.5}{\zeta(f)}}$$

$$F_i = \eta^2$$

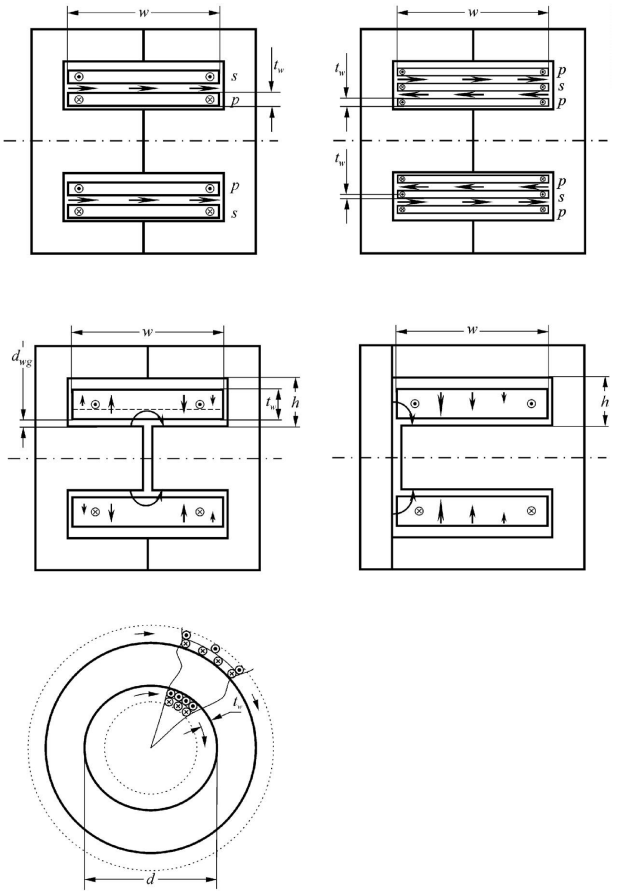


FIGURE 5.13: Magnetic Component Shape and field directions [4]
Up left: Normal Transformer: $K = 1$ for both windings
Up right: Secondary winding is sandwiched in an interleaved winding structure: $K = 1$ for secondary winding
Middle left : Center gaped inductor: $K = 2$ Middle right: EI core inductor: $K = 1$
Lower: Tororid Structure: $K = 1$

$$G_T = \zeta^6 + 2.7\zeta^5 - 1.3\zeta^4 - 17\zeta^3 + 85\zeta^2 - 43\zeta$$

$$G_A = \zeta^6 + 6.1\zeta^5 + 32\zeta^4 + 13\zeta^3 + 90\zeta^2 + 110\zeta$$

$$F_T = \frac{1}{\sqrt{1 + \frac{G_T(\zeta)}{1024}\left(1 + \frac{\pi^2}{12}F_i(\lambda,\eta)\chi^2(\zeta) - (1 - \frac{\pi^2}{12})(\lambda^{10} + \eta^{10})\chi^{10}(\zeta)^4\right)}}$$

$$F_A = \frac{1}{\sqrt{(1 + 1.3537\eta^4)^{-2} + \frac{G_A(\zeta)}{36864}\left(1 - \frac{\pi}{12}(\eta^{2.5} + 0.3\lambda^{10})\right)^4}}$$

$$K_{C,tr} = \frac{1}{16}\zeta^4(f)\left(\eta^2(\frac{m_E^2 - \frac{1}{4}}{3})\frac{\pi^2}{4}F_T k_F + \frac{1}{48}F_A\right)$$

The calculated eddy current losses using this approach will result in almost three times larger amount than the ohmic losses for the designed transformer, $P_{eddy} = 0.7804W$.

Symbols

Further information regarding the introduced parameters are found in [4], chapter 5.

5.2.14 Wire Optimization

Checking the total copper loss, we have:

$$P_{eddy} + P_{Ohmic} \leq P_{h,cu}$$

$$\begin{cases} P_{eddy} = 0.7804W \\ P_{Ohmic} = 0.2508W \quad \Rightarrow K_{eddy} = \dfrac{P_{eddy}}{P_{Ohmic}} = 3.11 \\ P_{h,cu} = 1.280W \end{cases} \tag{5.18}$$

Transformers:
For the instances where $K_{eddy} < 0.5$, a small increase in wire diameters (With respect to the available space in Winding area) would reduce ohmic losses without having a significant impact on the eddy current losses.

Also, as it has been already practice in this design, increasing the wire diameter to fill the entire layer can be another optimizing effort (Extra care must be taken as increasing the wire diameter can reduce the ohmic losses but it will increase the eddy current losses as well. So a compromise to achieve a smaller overall loss should be made)

Using interleaved winding structures can also be conductive to reduce the eddy current losses. The best case is to interleave the secondary thick wire (Typically two or more times larger than the penetration depth) with two layers of primary windings with smaller diameter.

Using Litz wire or parallel wires has also been helpful for decreasing the eddy current losses. Using P_i parallel wires can diminish the the diameter of wires with $\sqrt{P_i}$ factor and hence, reducing the eddy current losses.

Inductors:

In addition to the above improvement approaches, keeping the distance between windings and air gap can also improve the field factor, k_F. and decrease the chance of overheating the wires in the proximity of air gap.

5.2.15 Core Optimization

At this step, the winding area is checked through the equation 5.19 for the capacity to fit all the windings within itself.

$$\sum_{i=1}^{n} P_i N_i \frac{\pi d_{i,p}^2}{4} \leq k_{cu} W_a \tag{5.19}$$

Where:

k_{cu} is the copper filling factor

W_a is the winding area

$$k_{cu} = \frac{\pi * 13 * 100 * (0.101)^2}{4} + \frac{\pi * 7 * 2 * 140 * (0.101)^2}{4} = 26.12\ mm^2$$

The copper filling factor, k_{cu}, for round conductors is usually considered 0.4 and for Litz wires usually between $0.25 - 0.3$. If the window area couldn't fit all the windings, a larger core with higher power dissipation capability will be considered. Choosing a better material with lower losses or higher saturation level is a good way to make the core size choice.
Also if the calculated filling factor was very small, $k_{cu} \ll 0.4$, (So the window area is not fully utilized and filled) and the ratio of eddy current to ohmic losses were too small, $K_{eddy} \ll 0.5$, then a choice of smaller core size is advised.

It's worth noticing that choosing a smaller core size would already result in a larger number of turns for the windings. Choosing a larger wire diameter to compensate for that will in turn, increase the eddy current losses. So in practice, the choice of smaller core size should be considered if both criteria (relatively low eddy current losses and not fully utilized window area) happen at the same time.

5.2.16 Non-Saturated Thermally limited Design of Inductor

Resonant inductor in the series resonant converter also falls into the category of non-saturated design. Design steps are similar to the aforementioned transformer design. The only additional step is to calculate the air gap in the center leg which will be presented below.

- $$\begin{cases} V_{in,rms} = 226\ V \\ I_{in,rms} = 2.47\ A \end{cases} \xrightarrow{A=20*10^3} \begin{cases} S_{tot} = 558.22\ VA \\ a_{ch} = 30.3\ mm \end{cases} \tag{5.20}$$

  ETD 34/17/11 is chosen

  $l_e = 78.6\ mm$, $A_e = 97.1\ mm^2$, $V_e = 7630\ mm^3$

  Bobbin info:

  Winding width $= 20.9\ mm$, Winding height $= 6\ mm$, MLT $= 60.5\ mm$

- $$\begin{cases} P_h = 2500 * 0.034 * 0.034 = 2.89\ W \\ P_{h,fe} = P_{h,cu} = \dfrac{P_h}{2} = 1.445\ W \end{cases} \Rightarrow \begin{cases} P_{f_{e,sp}} = 189.384\ \dfrac{mW}{cm^3} \end{cases} \tag{5.21}$$

- $$\begin{cases} \beta = 3.3623 \\ B_{pg} = 0.0959\ T \end{cases} \Rightarrow \begin{cases} B_{pp} = 2 * 0.0959 = 0.1918\ T \end{cases} \tag{5.22}$$

- $$\begin{cases} \psi_{pp} = 5.25 * 10^{-4} \\ \phi_{pp} = 1.8630 * 10^{-5} \end{cases} \Rightarrow N = 28.18 \tag{5.23}$$

  Chosen value for N = 28

  $$\begin{cases} B_{new} = 0.0965\ T \\ P_{f_{e,sp}} = 193.5225\ \dfrac{mW}{cm^3} \end{cases} \Rightarrow P_{fe} = 1.4766\ W$$

- $$\begin{cases} \alpha = 1 \\ P_{cu} = 1.445\ W \end{cases} \Rightarrow d = 4.5395 * 10^{-4}\ mm \tag{5.24}$$

  Frequency $= 200\ kHz \Rightarrow \delta = 1.7067 * 10^{-4}\ m$

  Wire info:

140 strands of $AWG38$ wires - one layer silk wrapping

$d_{1,p,single} = 0.101\ mm \longrightarrow d_{Strand}$

$d_{1,p,outer} = 1.69\ mm \longrightarrow d_{Bundle}$

Winding Width = 20.28 mm $\longrightarrow$Utilized Length

- $m = 3,\ n_E = 110.4335,\ m_E = 35.4965,\ \eta = 0.5337,\ \lambda = 0.5975,\ K = 2,\ dwg = 0.5\ mm,\ tw = 5.1\ mm,\ \kappa = 0.2096,\ \zeta = 0.5918,\ \chi = 0.2829,\ G_T = 51.7689,\ G_A = 103.7159,\ F_T = 0.9738,\ F_A = 1.1083,\ K_{Fx} = 2.6818\ ,\ K_{Fy} = 2.0325,\ K_{Cin} = 0.3560$

- $P_{cu} = 0.3017$

- Calculating air gap:

$$\sum l_g = \frac{\mu_\circ * A_e * N^2}{L} - \frac{l_e}{\mu_c} = 1.3\ mm \tag{5.25}$$

In the above calculation, the air gap is determined for both fluxes that circulate between side legs and go through center leg. So the air gap should be divided by two: $l_g = 0.65\ mm$

5.3 Saturated Design

In application with low frequency where the DC component of the current is high such as grid frequency filters and DC chokes, the design category should be of saturation limited one. The boost inductor in PFC stage falls into the category of saturated-thermally limited design.

Design approach for magnetic components with the core saturation is similar to the non-saturated ones but with some differences in the primary steps of the design. Fig. 5.14 shows the design steps for saturated-thermally limited magnetic design. .

5.3.1 Calculating the peak to peak flux density

The design procedure starts with finding the peak flux density, B_{pp}. A value for saturation flux, B_{sat}, should be defined according to the core material and temperature. Peak

to peak value for flux density will be then determined as below:

$$B_{pp} = B_{sat} \frac{\Delta i_{L,pp}}{i_{L,DC} + \Delta i_{L,peak}} \tag{5.26}$$

The value for B_{sat} in power conversion with ferrite cores is usually set to 0.35 T. In the design of the boost inductor, the value for $\Delta i_{L,pp}$, $i_{L,peak}$, and other parameters can be achieved from the simulation waveforms with PSIM software.

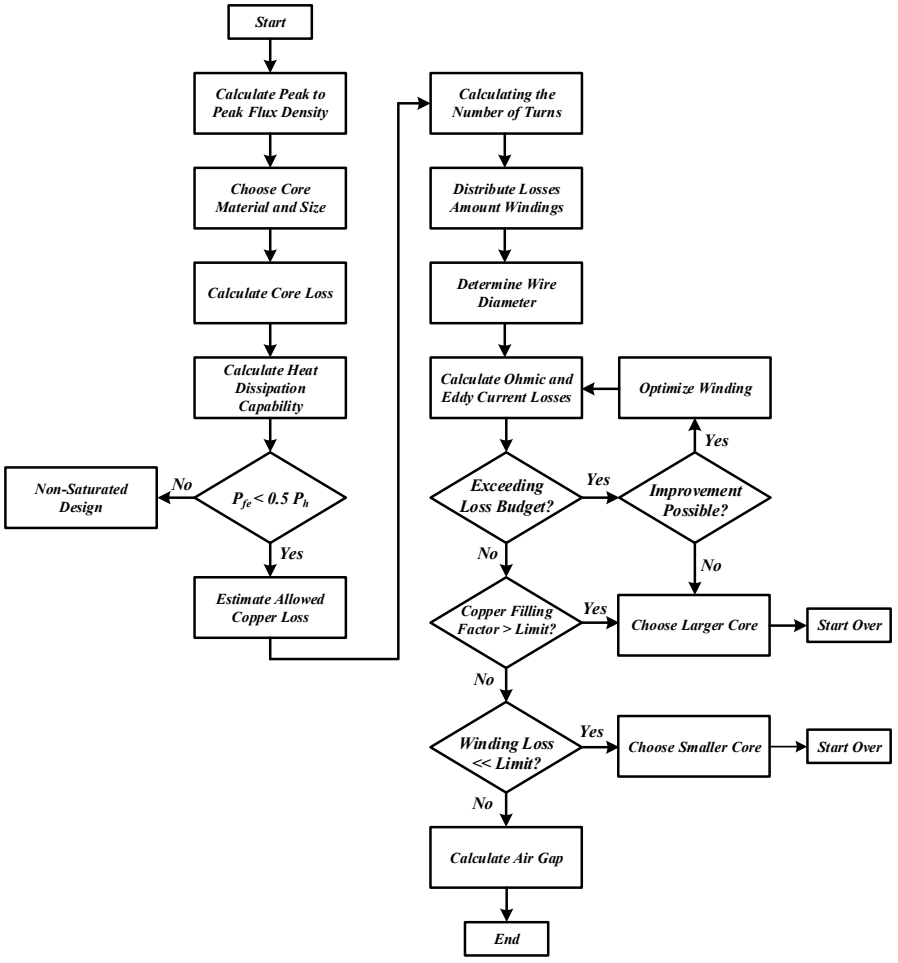


FIGURE 5.14: Flow chart for magnetic design with saturation limit

- Boost inductor design:

$$\begin{cases} V_{L,rms} = 91.7\ V \\ I_{L,rms} = 1.7346\ A \\ f = 20\ kHz \\ \Delta i_{L,pp} = 1.43\ A \\ i_{L,pp} = 3.258\ A \end{cases} \xrightarrow{A=10*10^3} B_{pp} = B_{sat} \frac{\Delta i_{L,pp}}{i_{L,peak}} = 0.1536\ T \tag{5.27}$$

5.3.2 Choosing core material and size

Similar to the step for non-saturated magnetic designs, core size can be determined following a scale law based on natural convection air[33].

$$S_{tot} = \sum_{\text{All Windings}} V_{rms} I_{rms} = A\, a_{ch}^{\gamma}\, f\, \frac{B_{pp}}{2} \Rightarrow a_{ch} = \left(\frac{S_{tot}}{A\, f\, \frac{B_{pp}}{2}} \right)^{\frac{1}{\gamma}} \tag{5.28}$$

where

A is a coefficient for ferrite (in saturated designs) in the range of $(5-15)*10^{-3}$ when a_{ch} is in m.

a_{ch} is largest dimension of the component in m

λ is an exponent, characterizing the material and the shape of the core, $\lambda = 3.5$ for saturated design

f is the operating frequency in Hz

B_{pp} is the peak to peak flux density in T

- ETD 39/20/13 has been chosen

$$\begin{cases} S_{tot} = 159.0628\ VA \\ a_{ch} = 37.6\ mm \end{cases} \Rightarrow \begin{cases} V_e = 11500 * 10^{-9}\ m^3 \\ l_e = 92.2 * 10^{-3}\ m \\ A_e = 125 * 10^{-6}\ m^2 \\ WA = 1.74 * 10^{-4}\ m^2 \quad \text{Window Area} \end{cases} \tag{5.29}$$

Bobbin info:

$MLT = 69\ mm$, Winding Width $= 25.7\ mm$, Winding Height $= 7\ mm$

5.3.3 Calculating core loss

The value for core loss per volume can be found in graphical data provided by the manufacturing companies. Datasheets usually provide graphs showing the core loss per volume as a function of peak flux, temperature and operating frequency. For $N87$ material, the value for core loss per volume is presented below:

- $$\begin{cases} \text{Core material: N87} \quad \text{Ferrite} \\ f = 20\ kHz \\ B_{peak} \approx 76.8\ mT \end{cases} \Rightarrow \begin{cases} P_{f,sp} = 9\ \dfrac{kW}{m^3} \\ P_{fe} = 0.1035\ W \end{cases} \tag{5.30}$$

5.3.4 Calculating heat dissipation capability

The procedure is similar to the non-saturated magnetic design. After determining the allowable amount of loss budget, the expectation is that the core loss would constitute a small portion of the whole loss budget. If the calculated results were not consistent with that rule, the choice of design can be changed to non-saturated one.

$$P_h = k_A * a * h \tag{5.31}$$

- $$P_h = k_A * a * h = 2500 * 40 * 10^{-3} * 40 * 10^{-3} = 4\ W$$

Checking the $\dfrac{P_{fe}}{P_h}$ ratio:

- $$\frac{P_{fe}}{P_h} = \frac{0.046}{4} \ll 0.5 \rightarrow \text{confirming the saturated design}$$

5.3.5 Estimating the allowed copper loss

The component heat dissipation capability and core loss has been calulated in previous steps. In the case of non-saturated magnetic design, the optimum allocation of core and copper loss would be resulted if they have the same share of the total component allowable loss budget. According to [33], this ratio for saturated designs is different and follows the below equation:

$$P_{h,cu} = \frac{2}{3}P_h - \frac{1}{3}P_{fe} \tag{5.32}$$

The value calculated above, shows the estimated copper loss. Calculations for the boost inductor design is as follows:

- $$P_{h,cu} = \frac{2}{3}P_h - \frac{1}{3}P_{fe} \ = 2.65133\ W$$

Next design steps are similar to the non-saturated category and are aimed to calculate the number of turns, wire diameters and copper ohmic and eddy losses. The results for the design is presented below.

5.3.6 Boost inductor design example

- $$\begin{cases} L = 2\ mH \\ \psi_{pp} = 28.6 * 10^{-4} \\ \phi_{pp} = 1.9203 * 10^{-5} \end{cases} \Rightarrow N = 148.9371 \tag{5.33}$$

  Chosen value for N = 149

- $$\begin{cases} \alpha = 1 \\ P_{cu} = 2.65133\ W \end{cases} \Rightarrow d = 5.8453 * 10^{-4}\ mm \tag{5.34}$$

  Frequency $= 20\ kHz \Rightarrow \delta = 0.461\ mm$

  Wire info:

  20 strands of $AWG34$ wires - Single layer nylon wrapping

  $d_{1,p,single} = 0.160\ mm \longrightarrow d_{Strand}$

  $d_{1,p,outer} = 1.016\ mm \longrightarrow d_{Bundle}$

- $m = 6$, $n_E = 98.3870$, $m_E = 26.8328$, $\eta = 0.6125$, $\lambda = 0.6133$, $K = 2$, $dwg = 0.9\ mm$, $tw = 6.1\ mm$, $\kappa = 0.2282$, $\zeta = 0.2964$, $\chi = 0.1650$, $G_T = 19.7713$, $G_A = 41.1194$, $F_T = 0.992$, $F_A = 1.1899$, $K_{Fx} = 2.4224$, $K_{Fy} = 1.7472$, $K_{Cin} = 0.4573$

- $P_{cu} = 2.3164\ W$

- Calculating air gap:

$$\sum l_g = \frac{\mu_\circ * A_e * N^2}{L} - \frac{l_e}{\mu_c} = 1.7\ mm = 2l_g \rightarrow \ l_g = 0.85\ mm \tag{5.35}$$

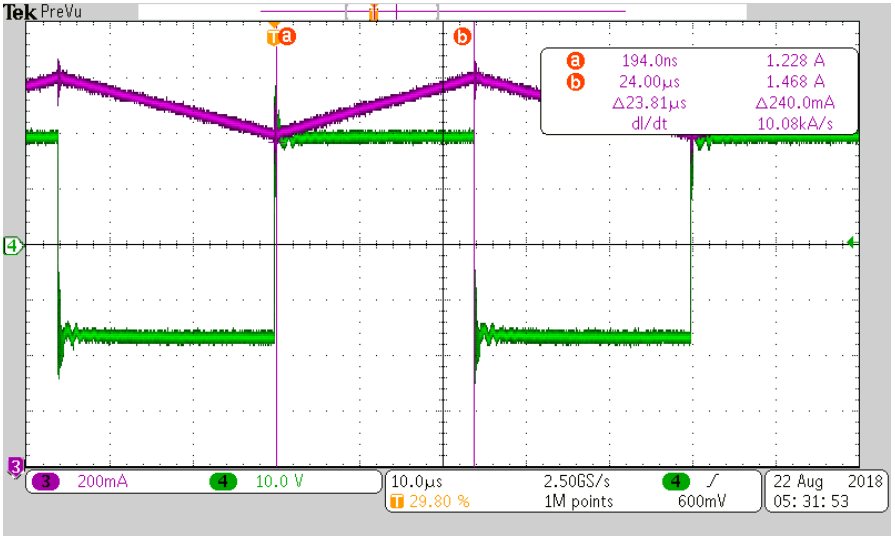
TABLE 5.3: Core size, Winding dimensions, and design specifications for magnetic components

Design Case	Core Size (mm)	Wire Design	Wire Diameter (mm) $d_{1strand} - d_{outer}$	P_{fe} (W)	P_{cu} (W)
Boost Inductor	$ETD\ 39/20/13$	20 strands $*$ $AWG34$	$0.160 - 1.016$	0.1035	2.3164
Resonant Inductor	$ETD\ 34/17/11$	140 strands $*$ $AWG38$	$0.101 - 1.69$	1.4766	0.3017
Resonant Transformer	$EE\ 32/16/9$	P : 100 strands $*$ $AWG38$ S : 140 strands $*$ $AWG38$ T : 140 strands $*$ $AWG38$	$0.101 - 1.516$ $0.101 - 1.69$ $0.101 - 1.69$	1.47	1.031

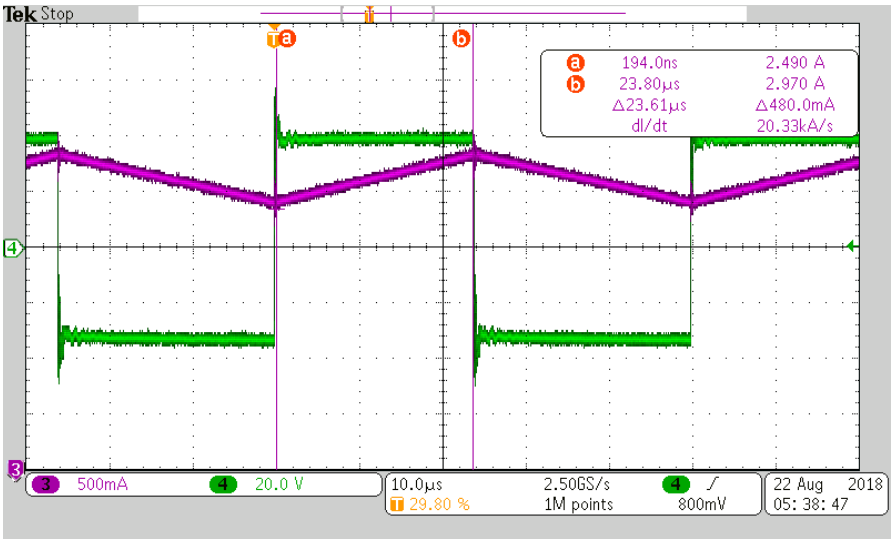
5.4 Summary

This chapter presents a systematic way to design magnetic elements. Boost filter, resonant inductor, and transformer have been designed following flowcharts 5.1 and 5.14.

Design specification of magnetic elements are provided in table 5.3. As shown, litz wire is used to mitigate the adverse effects of eddy current on copper losses. Fig. 5.15 shows the test results for boost inductor. As shown in the figure, the test takes place under 20 kHz and different current peaks of 1.5 A and 3 A and 2 mH value for inductance is obtained.



(a)



(b)

FIGURE 5.15: Voltage and current of boost inductor under 20 kHz frequency: (a) under $iL_{peak} = 1.5\ A$, (b) $iL_{peak} = 3\ A$

Chapter 6

Summary and Future Work

6.1 Summary of Contributions

In this thesis, analysis and design of an LED driver for street lighting applications have been conducted, simulation verification has been carried out, and experimental verification for GPCC based PFC stage has been presented. The objective for this LED driver is to achieve a fixed frequency in PFC stage, eliminate electrolytic capacitor, and achieve soft switching operation of the second stage while controlling the output current and decoupling the input and output power. The main contributions and conclusions in the thesis are summarized below:

- A comprehensive survey on variety of LED driver topologies and control schemes have been conducted.
- A two stage LED driver topology is proposed by cascading a boost PFC converter with a series resonant converter. Series resonant converter offers a compact, efficient, and isolated topology with the capability of switching at high frequencies to provide faster dynamic and to facilitate the power decoupling as well as achieving ZVS.
- Generalized peak current control scheme has been extended from PV inverters to PFC and has been used reduce THD and EMI by keeping the switching frequency constant.

- To eliminate electrolytic capacitor, a power decoupling method inspired from [31] has been implemented that allows large voltage swings on DC link and exploits the faster dynamic of resonant power converter's controller to decouple the output power from the input power.
- Design of magnetic elements have been categorized into two major groups of saturated thermally limited and non-saturated thermally limited and based on the approach introduced in [33], boost inductor, resonant inductor and also resonant transformer have been designed. Boost inductor has been implemented and tested.

6.2 Suggested Future Work

Below, a few directions that this research could go as the next stage of the study are mentioned:

- real-time change in the output luminous intensity of LEDs is referred as dimming. The proposed LED driver has multiple output channels. Using LEDs of red, green, and blue color in different output channels and incorporating dimming feature to control the amount of light intensity provided by each channel can generate a variety of light spectrum in the output. It can be suitable for horticulture applications where different light spectrum can affect the growth performance of plants.
- The LBT method [12] used to design the series resonant converter in this project, is a general tool that can be used to analyze and design high order resonant converters such as LLC and LCC resonant converters as well. The next stage of this study could be to employ LBT for exact parametric analysis and design of LLC or LCC converters in LED driver applications.

Appendix A

Current Sharing

A.1 Introduction

Due to the forward voltage of LEDs, forming the strings with many LEDs connected in series would result in a very large overall voltage of the string, making it impractical for the applications that require high luminous output. Forming multiple parallel connected LED string consisting of several LED units or modules would be a good choice.

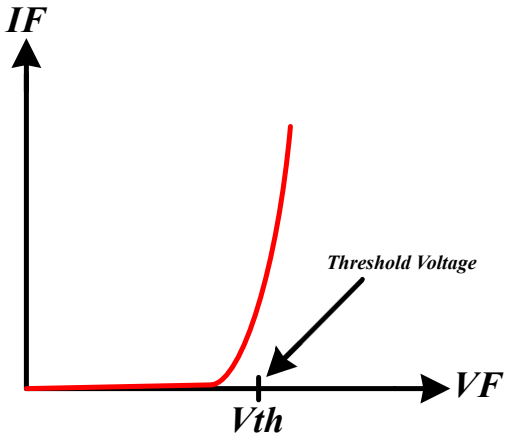


FIGURE A.1: V-I characteristic curve of LED

Fig. A.1 shows the VI characteristics for an LED. As it can be seen from the figure, any increase or decrease in forward voltage of the LED after the threshold voltage, results in a drastic change in driving current that goes through the LED or a string of LEDs connected together. This concern comes into the picture when an application with high

luminous output requires utilization of parallel LED strings. As there is no guarantee that LEDs with the same V-I ratings manufactured in a same company would have the exact same forward voltage. Hence, the current flowing through parallel strings can be significantly different. This will cause uneven light intensity and overdriving some LED strings which will deteriorate their lifetime and efficiency.

Different approaches for tackling the current sharing problem has been briefly reviewed and the operating principles of the chosen approach has been described further through this chapter.

A.2 Current Sharing: Passive and Active Approaches

Stabilizing and balancing the current can be achieved through passive and active methods. Resistors, capacitors, inductors and transformers are used in passive approach characterized by low cost and simple circuit configuration while active approach is based on operating the active components in linear or switching mode to control the current. Relatively higher precision acquired with the active approach usually comes with the expense of higher circuit complexity and cost.

A.2.1 Active Approach

Active devices used for balancing the current between Parallel LED strings can be controlled through linear or switch-mode approaches.

Linear current control method usually has a poor efficiency due to the high amount of power loss in the switch shown in A.2 (a). This is in turn, because of the voltage difference between the LED strings and the bus voltage, V_{Bus}. This issue not only reduces the overall efficiency, but also limits the use of LED driver to only low power applications [34]. Adaptive output voltage control for the V_{Bus} to reduce the voltage difference and hence, power dissipation in linear regulator has been proposed in some articles [35]. However, the overall efficiency is still poor compared to other current sharing approaches.

Using switch-mode dedicated converters for balancing the current is to resemble a separate DC source for each string. A form of using switch-mode converters to regulate the

current for each string is depicted in Fig. A.2 (b). DC-DC converters (usually buck or boost) are commonly used in switch-mode current regulator to control the current for each string. Although having higher efficiency compared to the linear regulator, it suffers from high component count, higher cost and relatively higher circuit complexity.

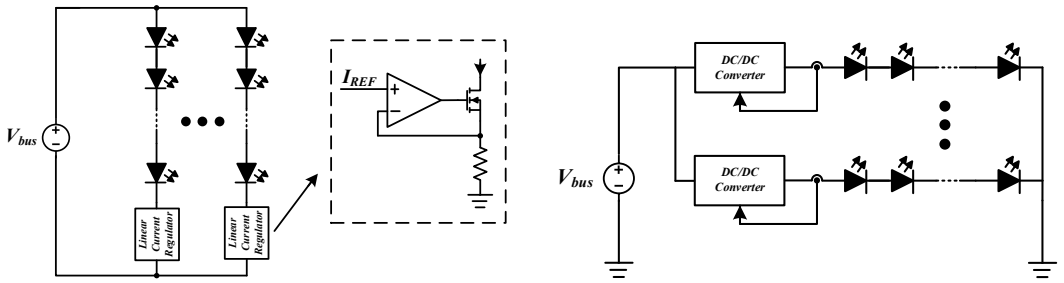


FIGURE A.2: Active current sharing approaches: (a) Linear and (b) Switch-mode

A.2.2 Passive Approach

Passive approach of achieving current balance is proposed due to it's simplicity and low cost. Resistors, inductors, Capacitors, and transformers are utilized in this category to provide current balancing enhancement to the parallel LED strings.

A.2.2.1 Resistive Schemes

Resistive approach is the most simplistic way to provide current balance. The underlying property for current sharing in resistive approaches is current division of the different impedances in each individual current path (inductive and capacitive approaches use the same concept as well, as it will be mentioned further).

Fig. A.3 shows the resistive approach as a means to prove current sharing. To better reduce the current imbalance between different legs, the resistance of the series resistors should be large so that the voltage across the resistor in each leg would be significantly larger than the voltage difference of LED strings. However, Unnecessary loss of energy is one big shortcoming of this approach, making it impractical for high power applications.

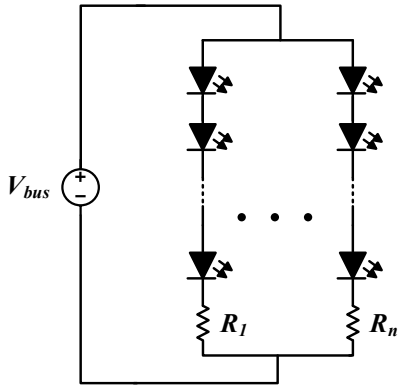


FIGURE A.3: current division method for resistive current sharing

Lossless approaches include using capacitors, coupled inductors, and transformers. They can be used to replace the dissipative ballast resistor to reduce the resistive loss when the LED strings are driven by ac source.

A.2.2.2 Capacitive Schemes

Current balance through utilization of capacitor can be achieved by either charge (amp-second) balance or current division based on different impedances on current paths. The latter is to determine each string's current by the impedance of the capacitor in the string. Provided that the capacitor impedance is much higher than that of the LED string and the tolerance of the capacitor impedance is small enough to prevent the current difference between strings[36]. However, the utilization rate of LEDs will be relatively poor, and the Luminous efficacy of the LEDs may be affected by the pulsating current [37].

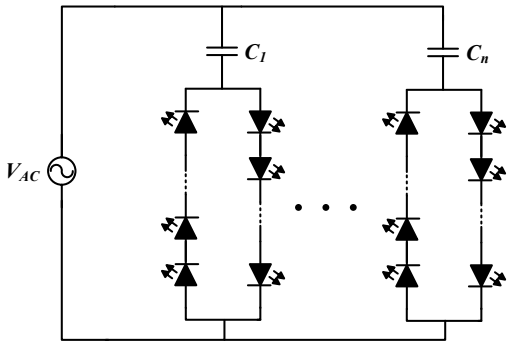


FIGURE A.4: current division method for capacitive current sharing

Another common approach to obtain the current balance between different channels is to utilize charge balancing property of the capacitor. However, many of the proposed topologies are limited to even outputs [36]. Fig. A.4 shows capacitive current balancing through current division approach. This scheme is identical with the aforementioned use of resistors in each branch as the voltage across the capacitor in each leg should be higher than the LED strings' voltage difference to better reduce the current deviation. Yet, the power loss of this approach is significantly lower than that of resistive scheme. For better utilizing the LEDs in both negative and positive half cycle, an anti-parallel LED string is connected in each leg.

Fig. A.5 (a) and (b) show the utilization of charge balance property of capacitors for current sharing. V_{AC1} in the circuit in Fig. A.5 (a) is secondary winding of a transformer and the whole circuit is a module, so if the higher intensity of light, and therefore more output LED strings, is needed then the whole module should be multiplied. In each half cycle, C_{B1} would balance out the voltage difference between LED strings and therefore the current wouldn't deviate [38]. More detailed analysis of the operation principle in this scheme will be provided further through this chapter. Current balancing capacitors can also be shared between branches. Fig. A.5 (b) shows the topology introduced in [39].

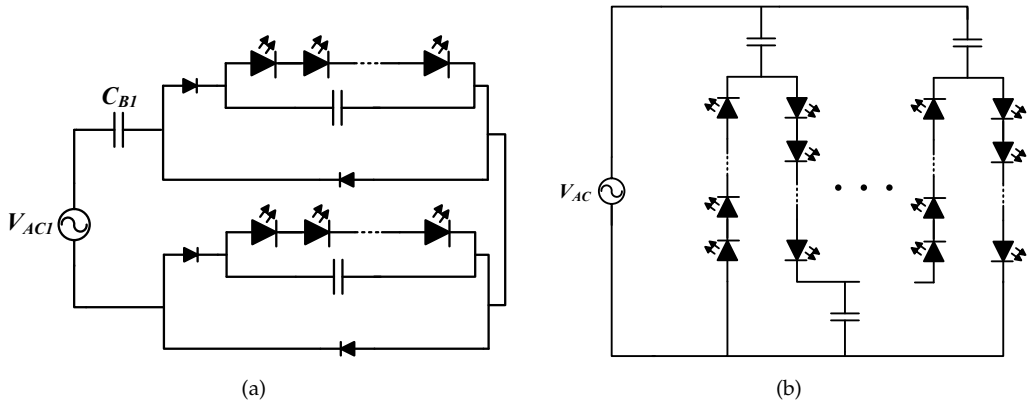


FIGURE A.5: Capacitor charge balancing method for current sharing: (a) two-string structure and (b) multiple-strings structure

A.2.2.3 Inductive Schemes

Inductive scheme for balancing currents has also been practiced in many articles [5]. The gist of this approach is to utilize volt-second balance property of inductors to control the current. However, this approach is not favorable when it comes to applications with high power density and small packaging size.

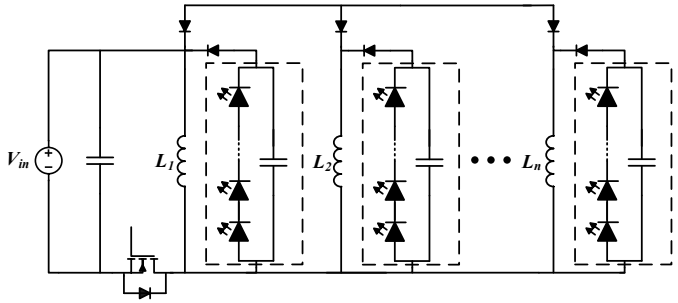


FIGURE A.6: Buck-Boost topology using inductor current sharing in [5]

The use of transformers for current balancing has been practiced in many articles. The concept underlying the principle of operation is the same as inductors. As current balancing takes place as a result of volt-second balance property of the transformers. Some of the most commonly used Transformer structures are presented below.

A.2.2.4 Series Connected and Multiple-output Structure

In this structure, the primary windings of different transformers are connected in series which in turn, causes all the secondary windings to have the same current.[34] Multiple output structure allows to drive LED strings with the same current that is a fraction of the primary current.

A.2.2.5 Huffman-tree Structure

First transformer in this structure carries the highest current. Transformers in cascaded levels have lower but same value of current[40]. As it can be seen in the Fig. A.8, this structure also necessitates the use of even LED string number.

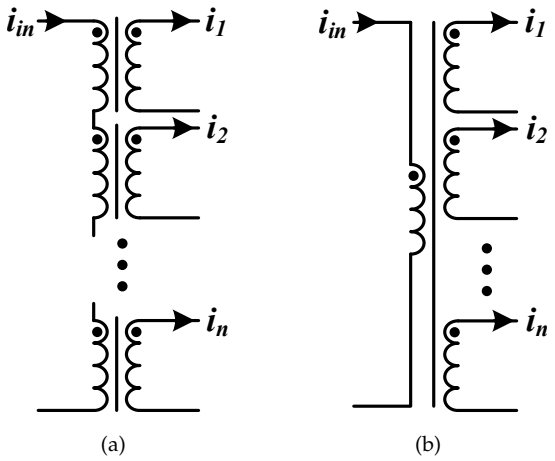


FIGURE A.7: Current sharing approaches with transformer: (a) Series connected transformers and (b) Multiple output transformer

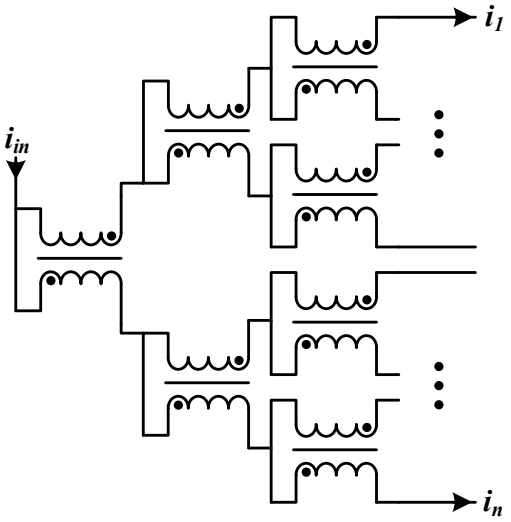


FIGURE A.8: Huffman-Tree structure

A.2.2.6 Daisy-chain and Open-chain Structures

The same current in different outputs in daisy-chain and open-chain transformers are constructed by winding coupling different transformers' windings together[41][42]. As shown in Fig. A.9, daisy chain structure connects the primary winding of the first transformer to the secondary winding of the last transformer. Hence, the number of transformers in this structure is increased by one. But the adverse effects of magnetizing currents on current balancing performance is greatly reduced [43].

After briefly reviewing passive and active approaches for current sharing, it can be

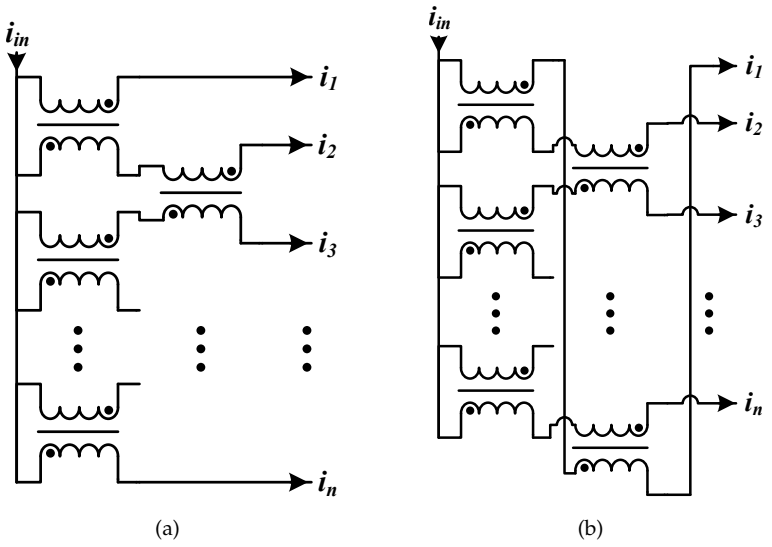


FIGURE A.9: (a) Open-Chain Transformer and (b) Daisy-Chain Transformer

inferred that for applications with lower cost and design complexity, the passive approach is more suitable. Charge balancing current sharing method has been selected for implementation in the experimental setup.

- **Cost-effectiveness and design complexity:** Capacitive approach has the benefit of cost-effectiveness over the active methods. Also, current balancing procedure is done without the need for any active switch and complex control circuit that makes this approach favorable.

- **Less dependency on the capacitor tolerance:** As it has been mentioned, the use of capacitors for current balancing can either be via current division approach, or charge balance approach. While current division approach solely depends on the capacitor and string voltage tolerance, the charge balancing method with blocking capacitors works in a way to provide the average voltage difference of the LED strings and hence, less affected by variations of voltage and capacitor tolerance.

- **Compact size:** Although using inductors and transformers for current sharing enhances the circuit with high thermal capabilities and longer lifetime, the large reactive component sizes might become an issue. Using film capacitors rectifies the mismatch between LED and LED driver lifetime and also has a more compact volume rather than different variations of inductor and transformer topologies.

A.3 Proposed Topology and Principle of Operation

As it has been mentioned earlier through this chapter, one approach to provide current sharing between parallel LED strings is to use charge balancing characteristics of a capacitor. The concept is to balance out the voltage difference with a DC blocking capacitor so that regardless of the different forward voltage of LEDs, the same voltage would be applied to each string in a cycle. Fig. A.10 shows a simple rectifying circuit

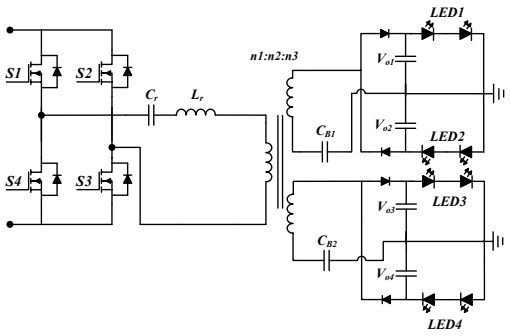


FIGURE A.10: Current sharing circuit topology

that has been used to achieve current sharing. Transformer is used to provide isolation between LED strings and Resonant converter. A DC blocking capacitor is placed in series with the secondary and tertiary winding of the transformer, forming four separate outputs.

The current sharing in this circuit is achieved through charge balancing of capacitors CB_1 and CB_2 to balance out the voltage difference between V_{o1} and V_{o2} and also between V_{o3} and V_{o4}. The average voltage across the blocking capacitor in a switching cycle is referred as V_{CB}.

As it's shown in Fig. A.11 the current going through the resonant tank in the primary side of the transformer is continuous. Hence, the output current on the secondary and tertiary side is continues. The operating principle of the circuit is demonstrated by describing the two modes that are formed in positive and negative half cycles of i_s

A.3.0.1 Mode 1

In this Mode, diode D_1 is conducting. The current i_s will charge the capacitor C_{o1}. The current in LED_2 is provided by the already-charged C_{o2} since D_2 is blocking the current.

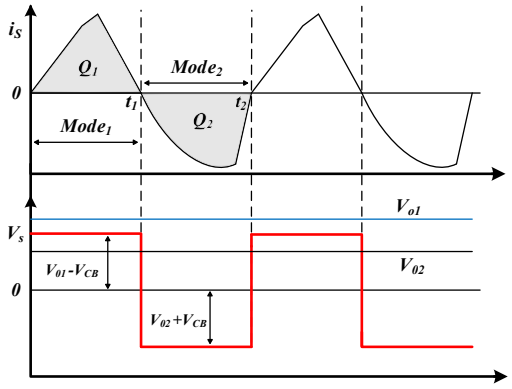


FIGURE A.11: Current and voltages on the secondary side of transformer

Diodes are assumed to be ideal. Simplified circuit is shown in Fig. A.12(a). The voltage across DC blocking capacitor C_{B1} has a DC and a ripple part. In our analysis of the circuit the DC part of the voltage is represented with a DC voltage source and the ripple is kept on the capacitor C_{B1}.

A.3.0.2 Mode 2

Between t_1 and t_2, diode D_2 starts to conduct and diode D_1 blocks the current. Hence, C_{o1} feeds LED_1 and C_{o2} starts to charge. A more simplified model of this mode is presented in Fig. A.12(b)

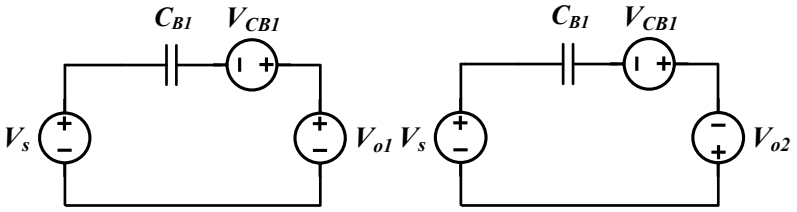


FIGURE A.12: Simplified circuit in Mode 1 and Mode 2 of current sharing

The charge balance property of the blocking capacitor would state that the amount of charge in C_{B1} during both positive and negative interval of secondary winding current i_s (Mode 1 and Mode 2) is equal and can be calculated as:

$$Q_1 = \int_{t_0}^{t_1} i_{s,p}(t)dt \tag{A.1}$$

$$Q_2 = \int_{t_1}^{t_2} i_{s,n}(t)dt \tag{A.2}$$

Where $i_{s,p}$ and $i_{s,n}$ are secondary winding's current in positive and negative half cycle.

Using C_{o1} and C_{o2}, we assume the current ripples are fairly filtered out and LED strings sink the DC current. The amount of average current going through LED_1 and LED_2 is the same, and equal to the average amount of above calculated charge per each switching period. Therefore we have:

$$I_{o1} = \frac{Q_1}{T_s} \tag{A.3}$$

$$I_{o2} = I_{o1} = \frac{Q_2}{T_s} \tag{A.4}$$

The average voltage on blocking capacitor, V_{CB}, can be calculated by volt-second balance property. According to Fig. A.12 for simplified model of the circuit in Mode 1 and Mode 2 we have:

$$\begin{cases} (V_{o2} + V_{CB})(t_2 - t_1) = (V_{o1} - V_{CB})(t_1 - t_0) \\ \\ (t_2 - t_1) = (t_1 - t_0) = \dfrac{T_s}{2} \end{cases} \Rightarrow V_{CB} = \frac{V_{o1} - V_{o2}}{2} \tag{A.5}$$

Since duty cycle is set on 50%, the above equation is simplified. The voltage across the LED strings can sometimes be different. Whether it has been caused by different forward voltage of LEDs or different tolerances on LEDs internal resistance, the need for balancing out this voltage difference for parallel LED strings is inevitable to deliver even luminous output. As it can be inferred from the equation A.5, the average amount of difference between parallel strings can be adjusted by placing a DC blocking capacitor in the circuit.

Bibliography

[1] LED Pole Light 150 Watt 5700K Black AM. https://www.ledmyplace.ca/products/led-pole-light-150watt-5700k-black,.

[2] MAD Costa, Ricardo N do Prado, Alexandre Campos, and Alysson R Seidel. An analysis about valley fill filters applied to electronic ballasts. In *Industrial Electronics Society, 2003. IECON'03. The 29th Annual Conference of the IEEE*, volume 1, pages 509–514. IEEE, 2003.

[3] Oliver Winter, Christian Kral, and Erich Schmidt. Design and loss assessment of air cored axial flux permanent magnet machines, 05 2013.

[4] Vencislav Cekov Valchev and Alex Van den Bossche. *Inductors and transformers for power electronics*. CRC press, 2005.

[5] Werner Thomas and Johannes Pforr. A novel low-cost current-sharing method for automotive led-lighting systems. In *Power Electronics and Applications, 2009. EPE'09. 13th European Conference on*, pages 1–10. IEEE, 2009.

[6] Why Solid-State Lighting? http://http://www.lrc.rpi.edu/programs/solidstate/SSLWhat.asp. Accessed: 2018-05-16.

[7] E Fred Schubert, Jong Kyu Kim, Hong Luo, and JQ Xi. Solid-state lightinga benevolent technology. *Reports on Progress in Physics*, 69(12):3069, 2006.

[8] Lighting Comparison: LED vs High Pressure Sodium (HPS) and Low Pressure Sodium (LPS). http://www.stouchlighting.com/blog/led-vs-hps-lps-high-and-low-pressure-sodium,. Accessed: 2018-07-18.

[9] IEC Standard. Electromagnetic compatibility (emc) part 3-2: Limits-limits for harmonic current emissions (equipment input current under 16 a per phase). Technical report, EN 61000-3-2, 1995.

[10] Non-Linear Load Power Factor Correction. `http://www.radio-electronics.com/info/power-management/power-factor-correction-pfc/nonlinear-load-pfc.php`. Accessed: 2018-05-01.

[11] Mohammad Ebrahimi and S Ali Khajehoddin. Fixed switching frequency generalized peak current control (gpcc) of dc–ac converters. *IEEE Transactions on Power Electronics*, 32(8):6605–6616, 2017.

[12] Mohammad Daryaei, Mohammad Ebrahimi, and S Ali Khajehoddin. Accurate parametric steady state analysis and design tool for dc-dc power converters. In *Applied Power Electronics Conference and Exposition (APEC), 2016 IEEE*, pages 2579–2586. IEEE, 2016.

[13] Wanfeng Zhang, Guang Feng, Yan-Fei Liu, and Bin Wu. A digital power factor correction (pfc) control strategy optimized for dsp. *IEEE Transactions on Power Electronics*, 19(6):1474–1485, 2004.

[14] HZ Azazi, EE El-Kholy, SA Mahmoud, and SS Shokralla. Review of passive and active circuits for power factor correction in single phase, low power ac-dc converters. In *Proceedings of the 14th International Middle East Power Systems Conference (MEPCON'10)*, pages 217–224, 2010.

[15] HZ Azazi, EE El-Kholy, SA Mahmoud, and SS Shokralla. Review of passive and active circuits for power factor correction in single phase, low power ac-dc converters. In *Proceedings of the 14th International Middle East Power Systems Conference (MEPCON'10)*, pages 217–224, 2010.

[16] Passive Power Factor Correction. `http://sound.whsites.net/lamps/pfc-passive.html`. Accessed: 2018-05-01.

[17] Arthur W Kelley and WF Yadusky. Phase-controlled rectifier line-current harmonics and power factor as a function of firing angle and output filter inductance. In *Applied Power Electronics Conference and Exposition, 1990. APEC'90, Conference Proceedings 1990., Fifth Annual*, pages 588–597. IEEE, 1990.

[18] Pedro Santos Almeida, Douglas Camponogara, Marco Dalla Costa, Henrique Braga, and J Marcos Alonso. Matching led and driver life spans: A review of different techniques. *IEEE Industrial Electronics Magazine*, 9(2):36–47, 2015.

[19] Cornell Dubilier. Aluminum electrolytic capacitor application guide. *Accessed 6th Sept*, 2011.

[20] Simone Buso, Giorgio Spiazzi, Matteo Meneghini, and Gaudenzio Meneghesso. Performance degradation of high-brightness light emitting diodes under dc and pulsed bias. *IEEE Transactions on Device and Materials Reliability*, 8(2):312–322, 2008.

[21] Fanghua Zhang, Jianjun Ni, and Yijie Yu. High power factor ac–dc led driver with film capacitors. *IEEE Transactions on Power Electronics*, 28(10):4831–4840, 2013.

[22] Qingcong Hu and Regan Zane. Minimizing required energy storage in off-line led drivers based on series-input converter modules. *IEEE Transactions on Power Electronics*, 26(10):2887–2895, 2011.

[23] Douglas Camponogara, Guilherme F Ferreira, Alexandre Campos, Marco A Dalla Costa, and Jorge Garcia. Offline led driver for street lighting with an optimized cascade structure. *IEEE Transactions on Industry Applications*, 49(6):2437–2443, 2013.

[24] SY Hui, Si Nan Li, Xue Hui Tao, Wu Chen, and WM Ng. A novel passive offline led driver with long lifetime. *IEEE Transactions on Power Electronics*, 25(10):2665–2672, 2010.

[25] Pablo Zumel, Cristina Fernandez, Marina Sanz, Antonio Lazaro, and Andrés Barrado. Hbled driving strategy with reduced storage capacitor based on load modularization. In *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE*, pages 728–734. IEEE, 2011.

[26] Beibei Wang, Xinbo Ruan, Kai Yao, and Ming Xu. A method of reducing the peak-to-average ratio of led current for electrolytic capacitor-less ac–dc drivers. *IEEE Transactions on Power Electronics*, 25(3):592–601, 2010.

[27] US DOE. Energy star® program requirements for solid state lighting luminaires. 2008.

[28] Philip T Krein and Robert S Balog. Cost-effective hundred-year life for single-phase inverters and rectifiers in solar and led lighting applications based on minimum capacitance requirements and a ripple power port. In *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, pages 620–625. IEEE, 2009.

[29] Qingcong Hu and Regan Zane. Minimizing required energy storage in off-line led drivers based on series-input converter modules. *IEEE Transactions on Power Electronics*, 26(10):2887–2895, 2011.

[30] Jiexiu He, Xinbo Ruan, and Li Zhang. Adaptive voltage control for bidirectional converter in flicker-free electrolytic capacitor-less ac–dc led driver. *IEEE Transactions on Industrial Electronics*, 64(1):320–324, 2017.

[31] Sayed Ali Khajehoddin. *Resonant micro-inverters for single-phase grid-connected photovoltaic systems*. PhD thesis, 2010.

[32] Mohammad Daryaei. Analysis and design approach for converters with large signal variations, msc thesis, 2016.

[33] Vencislav Cekov Valchev and Alex Van den Bossche. *Inductors and transformers for power electronics*. CRC press, 2005.

[34] Junming Zhang, Lianghui Xu, Xinke Wu, and Zhaoming Qian. A precise passive current balancing method for multioutput led drivers. *IEEE Transactions on Power Electronics*, 26(8):2149–2159, 2011.

[35] Yuequan Hu and Milan M Jovanovic. Led driver with self-adaptive drive voltage. *IEEE Transactions on Power Electronics*, 23(6):3116–3125, 2008.

[36] Sungjin Choi and Taehoon Kim. Symmetric current-balancing circuit for led backlight with dimming. *IEEE Transactions on Industrial Electronics*, 59(4):1698–1707, 2012.

[37] SM Baddela et al. Parallel connected leds operated at high frequency to improve current sharing; industry applications conference 2004. In *39th IAS Annual Meeting*, pages 1677–1681.

[38] Xinke Wu, Junming Zhang, and Zhaoming Qian. A simple two-channel led driver with automatic precise current sharing. *IEEE transactions on industrial electronics*, 58(10):4783–4788, 2011.

[39] Chen Zhao, Xiaogao Xie, and Shirong Liu. Multioutput led drivers with precise passive current balancing. *IEEE Transactions on Power Electronics*, 28(3):1438–1448, 2013.

[40] KI Hwu and Sheng-Chien Chou. A simple current-balancing converter for led lighting. In *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, pages 587–590. IEEE, 2009.

[41] Junming Zhang, Jianfeng Wang, and Xinke Wu. A capacitor-isolated led driver with inherent current balance capability. *IEEE transactions on industrial electronics*, 59(4):1708–1716, 2012.

[42] Ruihong Zhang and Henry Shu-Hung Chung. Use of daisy-chained transformers for current-balancing multiple led strings. *IEEE Transactions on Power Electronics*, 29(3):1418–1433, 2014.

[43] Ruihong Zhang and Henry Shu-Hung Chung. Paralleled led strings: An overview of current-balancing techniques. *IEEE Industrial Electronics Magazine*, 9(2):17–23, 2015.