Faster-Than-Real-Time Hardware Emulation of Extensive Contingencies for Dynamic Security Analysis of Large-Scale Integrated AC/DC Grid

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***Abstract*—The rapid expansion of modern power systems has brought a tremendous computational challenge to dynamic security analysis (DSA) tools which consequently need to process extensive contingencies. In this work, hardware emulation is investigated to accelerate the DSA solution of a large-scale AC/DC system deployed on the field-programmable gate arrays (FPGAs) faster-than-real-time (FTRT) execution. Electromagnetic transient (EMT) modeling of the DC grid is conducted since the fast converter dynamics require a small time-step for accuracy; in contrast, the transient stability (TS) simulation is applicable to the AC grid which tolerates a much larger step size. To coordinate the 2 different types of simulation, an interface based on dynamic voltage injection is proposed to integrate the AC and DC grids, in addition to maintaining a low hardware latency. An emulation platform consisting of multiple FPGA boards is established so that with a proper allocation it has a sufficient capacity to accommodate the system under study which has 6 ACTIVSg 500-bus systems interconnected by a 6-terminal DC grid. The efficacy of the proposed FTRT hardware emulation platform is demonstrated by 2 case studies with more than 5500 contingencies analyzed in total, where an FTRT ratio of more than 208 is achieved for the hybrid AC/DC grid, while it is over 277 times for a single 500-bus system. Furthermore, the FTRT dynamic emulation results, including the security indices, are validated by the simulation tool DSATools/TSAT®.**

***Index Terms*—AC/DC grid, dynamic security analysis, faster than real time, field-programmable gate arrays (FPGAs), parallel processing, power system security, power system stability, real-time systems, synchronous generator.**

I. Introduction

Dynamic security analysis (DSA) is necessary in assessing the ability of a power system to withstand cascading failures or contingencies in a specified time span to ensure that the power grid is at a secure operating point. In the last few decades, power transmission networks have been expanding significantly including the integration of high voltage direct current (HVDC) systems, making the modeling, simulation, protection, and control of the network significantly more complex. The increasing scale of a power system also demands that more contingency scenarios be taken into consideration during DSA. To mitigate the adverse impacts of a variety of disturbances on the actual power system, online DSA is widely utilized to continuously monitor the grid and take remedial actions [1], [2].

This work is supported by the Natural Sciences and Engineering Research Council of Canada (NSERC).

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The contingency screening type is a major factor that influences the speed of DSA. A typical contingency analysis applies the power flow calculation or state estimation, which only provides a single-state security index for contingency ranking [2], [3]. Due to the relatively low computational burden, the power-flow based contingency analysis methods are widely utilized in high-speed DSA [4]-[6]. However, more stringent criteria have been proposed by the North American Electric Reliability Corporation (NERC) [7], which brings many challenges for conducting fast contingency analysis. Since it is computational onerous to evaluate all the contingencies at a time, a subset is usually selected for analysis in traditional contingency screening methods such as the performance index contingency ranking [8]. However, when a larger subset is required for the contingency analysis of a large-scale grid, it is difficult to achieve real-time execution. Meanwhile, the power-flow based contingency ranking methods fall short of provision of subsequent dynamic process after a disturbance, and are hence excluded for predictive control in an energy control center. Therefore, the transient stability (TS) simulation is adopted for DSA purpose. It enables the representation of the dynamic characteristics of all power system components in time-domain, which is a direct and precise method attributing to the utilization of detailed dynamic models [9]-[11].

The processing hardware is another aspect that limits the performance of DSA tools, which nowadays are usually supported by high-performance CPUs or multiprocessors for efficient simulation or even real-time execution [12]-[14]. Although presently CPU-based commercial DSA simulators are prevalent in stability analysis, the massive scale of the target power system, as well as the huge number of contingencies to be analyzed, always poses a significant challenge to the simulation efficiency. The utilization of the multiprocessors or supercomputers is a straightforward solution for real-time DSA due to the sufficient hardware resources and high processing frequency [15]. However, as many as 24,000 CPU cores may be needed to realize a near real-time simulation of a real power grid containing 3,000 generators [14], which is inconvenient and expensive for commercial use. Although parallel algorithms are utilized for accelerating transient stability simulation [16]-[21], the execution time will still increase along with the dimension of the admittance matrix [22], [23].

In this work, a multi-FPGA-based DSA platform is proposed to provide fast and accurate contingency screening data for a large-scale AC/DC grid by faster-than-real-time (FTRT) emulation. Compared with currently available commercial

real-time (RT) simulation tools, the FPGA-based platform has the following advantages. The most straightforward difference between an FTRT emulation platform and RT simulators is the computation speed. RT simulation implies that the hardware must solve the model equations within an interval of the time-step. On the other hand, FTRT is stricter in terms of hardware latency, and the platform runs at least several times faster than a RT simulator. FTRT emulation can meet all the requirements of RT simulation, while the RT simulation tools are unable to reach FTRT due to their scalability and computational speed limits. Secondly, the capability and scalability of the FPGA-based FTRT emulation platform are better than RT simulators. For example, the 141-bus system with 38 generators is simulated using the RTDS® simulator, and 4 PB5 racks were needed [24]. In order to reduce the hardware resources and reduce the cost, only 5 buses and 2 generators were simulated on RTDS®, while the rest of the system parts were simulated on FPGA boards. As shown later in this paper, two 500-bus systems with 180 generators in total can be executed on a single Xilinx® VCU128 board, which demonstrates the FPGA's capability in emulating a large power system. The reconfigurability and the sufficient hardware resources allow the entire grid to be deployed on the platform after proper system partitioning and allocation. Meanwhile, a specific AC/DC grid interface using dynamic voltage injection is proposed to maintain a constant admittance matrix despite the HVDC converter outputs being time-varying, which consequently reduces hardware resources utilization and expedite the emulation. As a result, the FTRT DSA emulation is more than 208 times faster than real-time.

Since the FTRT emulation enables a high computation speed above real-time, the grid can be emulated much faster and therefore it can accelerate planning schedules, predict the upcoming disturbances, and help in devising new control strategies. The proposed FTRT emulation can also be used in the energy control center to provide sufficient time to take remedial actions, recommend an optimal control strategy to mitigate adverse impacts, and enhance the overall stability and security of the system.

The rest of the paper is organized as follows: Section II introduces transient stability simulation, including modeling and solution of the AC grid. The DC grid modeling and its interfacing technique are specified in Section III. Section IV illustrates the hardware design on the proposed multiple FPGA based platform. The emulation results of more than 5500 contingencies, as well as their analysis and validation, are provided in Section V. Section VI presents the conclusion and prospective work.

II. AC Grid Model for Dynamic Security Analysis

A. Transient Stability Problem

The transient stability simulation for DSA is based on a set of differential algebraic equations (DAEs). The dynamic processes of the synchronous generators in a power transmission system can be summarized as

$$\dot{\mathbf{x}}(t) = F(\mathbf{x}, \mathbf{u}, t), \tag{1}$$

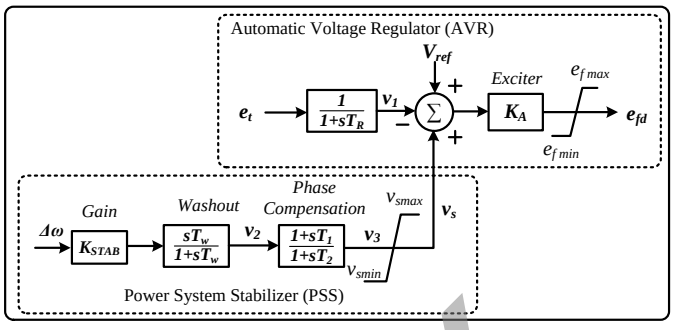

Fig. 1. Excitation system of the synchronous generator.

$$\mathbf{x}_0 = \mathbf{x}(t_0). \tag{2}$$

The network including transmission lines, transformers, and various loads are represented by the algebraic equation (3).

$$G(\mathbf{x}, \mathbf{u}, t) = \mathbf{0}, \tag{3}$$

where $\mathbf{x}$ refers to the vector of state variables of the synchronous generator, $\mathbf{u}$ represents the vector of the inputs, such as the mechanical torque (T_m) from governor, and field voltages (E_{fd}) calculated in the exciter model. (2) provides the initial conditions of the synchronous machines, which can be obtained from the solution of the power flow data.

The accuracy of the transient stability simulation is highly dependent on the solution strategies of the DAEs, which can be roughly classified into two categories: implicit and explicit integration methods. The former is essentially iterative methods such as Newton-Raphson, which has a higher accuracy under large time-steps. However, a large dimension of the DAEs may lead to more iterations in every single time-step and consequently extra execution time. Furthermore, due to the inherently sequential iterations until convergence, the iterative method is not suitable for parallel processing in FPGAs. Therefore, the explicit method 4th-order Runge-Kutta (RK4) is adopted in the hardware emulation for the high efficiency and low hardware resource demand, as given below

$$\mathbf{RK}_1 = h \cdot F(\mathbf{x}_n, \mathbf{u}_n, t_n), \tag{4}$$

$$\mathbf{RK}_2 = h \cdot F(\mathbf{x}_n + \mathbf{RK}_1/2, \mathbf{u}_n, t_n + h/2), \tag{5}$$

$$\mathbf{RK}_3 = h \cdot f(\mathbf{x}_n + \mathbf{RK}_2/2, \mathbf{u}_n, t_n + h/2), \tag{6}$$

$$\mathbf{RK}_4 = h \cdot f(\mathbf{x}_n + \mathbf{RK}_3, \mathbf{u}_n, t_n + h), \tag{7}$$

$$\mathbf{x}_{n+1} = \mathbf{x}_n + \frac{1}{6}(\mathbf{RK}_1 + 2\mathbf{RK}_2 + 2\mathbf{RK}_3 + \mathbf{RK}_4), \tag{8}$$

where $\mathbf{x}_{n+1}$ represents the vector of state variables for next time-step, and h refers to the emulation time-step, which is defined as 1 ms in this work.

B. Formulation of Synchronous Generators

To achieve high fidelity, a detailed 9^{th}-order synchronous generator model, which includes two mechanical equations, four electrical equations containing 2 windings on the d-axis and 2 damping windings on the q-axis, and an excitation system, is applied for dynamic security analysis.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPWRS.2022.3161561, IEEE Transactions on Power Systems

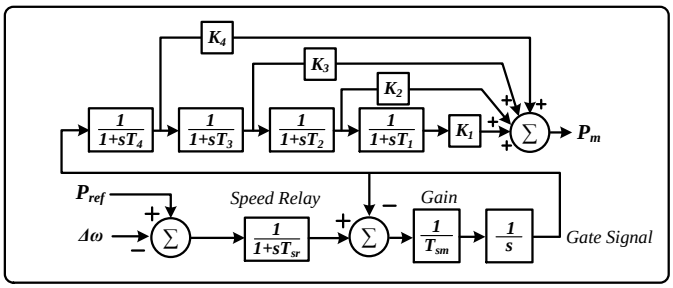

Fig. 2. Turbine governor system of the synchronous generator.

The 2 mechanical and 4 electrical equations describing the generator are given as

$$\dot{\delta(t)} = \omega_R \cdot \Delta\omega(t), \tag{9}$$

$$\dot{\Delta\omega(t)} = \frac{[T_m(t) - T_e(t) - D \cdot \Delta\omega(t)]}{2H}, \tag{10}$$

$$\dot{\psi}_{fd}(t) = \omega_R \cdot [e_{fd}(t) - R_{fd} i_{fd}(t)], \tag{11}$$

$$\dot{\psi}_{1d}(t) = -\omega_R \cdot R_{1d} i_{1d}(t), \tag{12}$$

$$\dot{\psi}_{1q}(t) = -\omega_R \cdot R_{1q} i_{1q}(t), \tag{13}$$

$$\dot{\psi}_{2q}(t) = -\omega_R \cdot R_{2q} i_{2q}(t), \tag{14}$$

and the excitation system model given in Fig. 1 is comprised of the following power system stabilizer (PSS) and automatic voltage regulator (AVR) equations

$$\dot{v}_1(t) = \frac{[v_t(t) - v_1(t)]}{T_R}, \tag{15}$$

$$\dot{v}_2(t) = K_{stab} \cdot \dot{\Delta\omega}(t) - \frac{v_2(t)}{T_\omega}, \tag{16}$$

$$\dot{v}_3(t) = \frac{[T_1 \dot{v}_2(t) + v_2(t) - v_3(t)]}{T_2}. \tag{17}$$

As an expansion of (1), the time-varying quantities in (9)-(17) contribute to vectors $\mathbf{u}$ and $\mathbf{x}$, and the remaining coefficients such as ω_R, H, D, R_{fd}, R_{1d}, R_{1q}, R_{2q}, T_R, K_{stab}, T_ω, T_1, and T_2 are constant parameters of generators and the excitation system.

The detailed mechanical equations and swing equations of a synchronous machine are given above. In a practical power transmission system, the mechanical power is provided by the turbine governing system. In order to obtain a higher accuracy of the dynamic security analysis results, a four-stage governor system is also included as given in Fig. 2. To reduce the computational burden and execution time of the hardware emulation, the governor system equations are solved by Forward Euler with a time-step of 1 ms, which are not included in the 9^{th}-order DAEs.

C. AC Network Equations

The AC network mainly comprises transmission lines, transformers, loads, and shunt capacitors. The transmission lines and the transformers are represented as lumped π models. The fixed loads and shunt capacitors are treated as the admittance which is associated with the buses, given as

$$Y_{Load} = \frac{P_{Load} + jQ_{Load}}{V_{Bus}^2}, \tag{18}$$

where V_{Bus} refers to the voltage of the local bus, P_{Load} is the active power of the load, and Q_{Load} represents the reactive power of the load or the shunt capacitor. Following the derivation of the admittance matrix of the AC network, the output current of the generators can be solved by the following matrix equations:

$$\begin{bmatrix} \mathbf{I_N} \\ \mathbf{I_R} \end{bmatrix} = \begin{bmatrix} \mathbf{Y_{NN}} & \mathbf{Y_{NR}} \\ \mathbf{Y_{RN}} & \mathbf{Y_{RR}} \end{bmatrix} \begin{bmatrix} \mathbf{U_N} \\ \mathbf{U_R} \end{bmatrix}, \tag{19}$$

where the subscription N and R refer to the generator nodes and the remaining nodes, respectively. Due to the absence of current injections to the non-generator buses, the current vector $\mathbf{I_R} = [\mathbf{0}]$. The relationship of the generator output voltages and currents can also be derived by the network equations in (19), given as:

$$\mathbf{I_N} = \mathbf{Y_{reduced}} \cdot \mathbf{U_N}, \tag{20}$$

where $\mathbf{Y_{reduced}} = \mathbf{Y_{NN}} - \mathbf{Y_{NR}} \mathbf{Y_{RR}^{-1}} \mathbf{Y_{RN}}$ is the reduced admittance matrix of $n \times n$ dimension. The vectors $\mathbf{I_N}$, $\mathbf{U_N}$ and $\mathbf{U_R}$ in (19) are not yet known. The algebraic equations (21) and (22) provide the relationship between $\mathbf{I_N}$ and $\mathbf{U_N}$ by expressing voltages e_d and e_q as functions of the known state variables and the components of the currents.

$$e_d = -r_a i_d + (i_q(X''_{aq} + X_l) - X''_{aq}(\frac{\psi_{1q}}{X_{1q}} + \frac{\psi_{2q}}{X_{2q}})), \tag{21}$$

$$e_q = -r_a i_q - (i_d(X''_{ad} + X_l) - X''_{ad}(\frac{\psi_{fd}}{X_{fd}} + \frac{\psi_{1d}}{X_{1d}})), \tag{22}$$

where r_a, X''_{aq}, X_{1q}, X_{2q}, X''_{ad}, X_{fd}, and X_{1d} are constant parameters of the synchronous machine. After solving the $\mathbf{I_N}$ and $\mathbf{U_N}$ by combining (21)-(20), the non-generator bus voltages group in vector $\mathbf{U_R}$ can be calculated directly.

III. HVDC Grid Modeling and Integration

A. HVDC Converter Average Value Model

The configuration of a 3-phase (N+1)-level modular multilevel converter (MMC) interconnecting the AC grid and DC grid is given in Fig. 3(a), where each phase contains 2 arms and each arm has N half-bridge submodules (HBSMs) and an arm inductor. In order to reveal the dynamics of the MMCs, the electromagnetic transient (EMT) simulation with a time-step of 200 μs is selected for emulating the HVDC grid, which can meet the requirements of DSA. The time-step of 200 μs also leads to a higher FTRT emulation speed than a regular time-step used in EMT simulation.

The FPGA-based hardware FTRT emulation prefers the models that induce low latency, and therefore, the average value model (AVM) of MMCs is adopted for contingency screening due to its simplicity in addition to the capability of being interactive with a basic converter controller to study its impact on the primary system. The HBSMs are simplified into controlled voltage sources as shown in Fig. 3(b). When the upper switch S_1 is turned on, the capacitor is inserted; while it is bypassed when S_2 is turned on. Assuming that the capacitor voltages are well balanced in each arm, which means the average values of capacitor voltages are equal, given as

$$v_{cap1} = v_{cap2} = ... = v_{capN} = \frac{U_{dc}}{N}, \tag{23}$$

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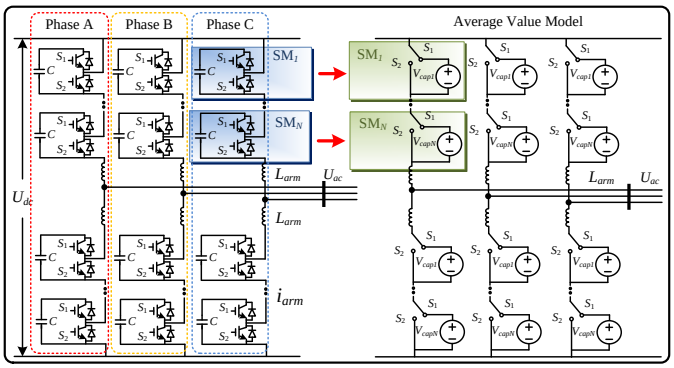

Fig. 3. Illustration of modular multilevel converter modeling: (a) three-phase topology, (b) average value model.

the equivalent voltage source of an arbitrary submodule (SM_i) can be expressed as

$$v_{SMi} = \frac{U_{dc}}{N} \cdot S_i, \tag{24}$$

where S_i refers to the switching function that takes the value 1 when the submodule capacitor is inserted and 0 when the SM is bypassed. As a result, the arm voltage can eventually be derived by the switching functions given as

$$v_{arm} = \frac{U_{dc}}{N} \cdot \sum_{i=1}^{N} S_i + L_{arm} \frac{di_{arm}}{dt}. \tag{25}$$

Since the well-balanced condition in the AVM yields no circulating current, the differential term in (25) can be neglected and the AC side output voltage is formulated as

$$v_{arm} = \frac{U_{dc}}{N} \cdot (\sum_{i=1}^{N} S_{ui} + \sum_{i=1}^{N} S_{li}), \tag{26}$$

where S_{ui} and S_{li} represent the switching functions of upper and lower arms, respectively.

In the HVDC grid, the reactive components such as the capacitor and inductor expressed by ordinary differential equations should be discretized for EMT simulation. The one-step integration method Trapezoidal rule is adopted for HVDC grid numerical calculation so that a discrete-time Norton equivalent circuit is utilized. The impedance of the capacitor and inductor take the form of $Z_C = \Delta t/2C$ and $Z_L = 2L/\Delta t$, respectively. The corresponding current sources of the Norton equivalent circuit are given as

$$I_{Ceq}(t) = -i_C(t-\Delta t) - \frac{2C}{\Delta t} v_C(t-\Delta t), \tag{27}$$

$$I_{Leq}(t) = i_L(t-\Delta t) + \frac{\Delta t}{2L} v_L(t-\Delta t). \tag{28}$$

Since the small time-step Δt guarantees the accuracy of EMT emulation, higher order integration methods are not adopted to reduce the computational burden.

B. AC-DC Grid Interface

The single-line diagram of the hybrid AC/DC grid is shown in Fig. 4, where the 6 ACTIVSg 500-bus systems [25] connect

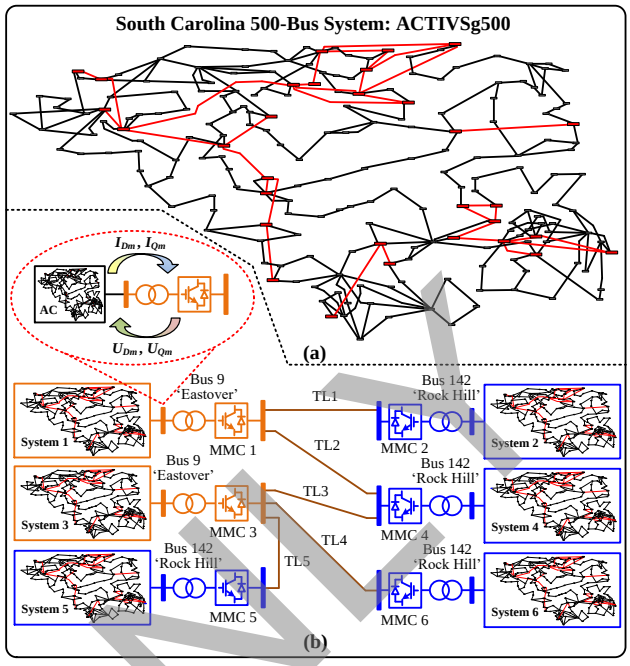

Fig. 4. Topology of hybrid AC/DC grid: (a) transient stability simulation part: South Carolina 500-bus system (ACTIVSg500), (b) EMT simulation part: six-terminal HVDC grid.

with a 6-terminal (6-T) HVDC system. MMC 1 and MMC 2 operate as inverter stations and connect with AC System 1 and 2 via Bus 9, respectively, while the remaining four terminals, all acting as rectifier stations, each delivers 100 MW active power from the connected AC grid via Bus 142. Since the AC grid undergoes transient stability simulation with a time-step of 1 ms, and the EMT emulation with a time-step of 200 μs is applied to the HVDC system, the latter part should be calculated five times more frequent than the former before data synchronization to keep numerical stability. Furthermore, the distinct emulation strategies prompts an interface based on dynamic voltage injection strategy which enables the two types of simulations to be compatible in one program, in addition to maintaining a constant admittance matrix that results in acceleration of the hardware emulation.

The synchronous machines can not only be represented in detail by Park's equation as given in (9)-(14), but also constant voltage sources in the D-Q frame when their dynamics are not concerned. The HVDC converter stations in the EMT simulation can be treated as time-varying voltage injections to the AC grid, which are equivalent to the non-detailed machines in transient stability simulation. The dynamic voltages $\mathbf{U_{Dm}}$ and $\mathbf{U_{Qm}}$ in Fig. 4 (b) of the HVDC converter stations are directly delivered to the AC grid and integrated with the AC network equations without updating the admittance matrix. Due to the voltage injection method, (20) can be expanded as:

$$\begin{bmatrix} \mathbf{I_n} \\ \mathbf{I_m} \end{bmatrix} = \begin{bmatrix} \mathbf{Y_{nn}} & \mathbf{Y_{nm}} \\ \mathbf{Y_{mn}} & \mathbf{Y_{mm}} \end{bmatrix} \begin{bmatrix} \mathbf{U_n} \\ \mathbf{U_m} \end{bmatrix}, \tag{29}$$

where the subscription n refers to the synchronous machine

nodes represented by the detailed Park's equations, m are the nodes where converter stations locate, and $n+m$ denotes the N generator nodes in (20).

As the voltages calculated by the HVDC system are in D- and Q- axis, (29) which is based on complex numbers yields 4 real matrix equations:

$$\mathbf{I_{Dn}} = \mathbf{G_{nn}U_{Dn}} - \mathbf{B_{nn}U_{Qn}} + \mathbf{G_{nm}U_{Dm}} - \mathbf{B_{nm}U_{Qm}}, \tag{30}$$

$$\mathbf{I_{Qn}} = \mathbf{G_{nn}U_{Qn}} + \mathbf{B_{nn}U_{Dn}} + \mathbf{G_{nm}U_{Qm}} - \mathbf{B_{nm}U_{Dm}}, \tag{31}$$

$$\mathbf{I_{Dm}} = \mathbf{G_{mn}U_{Dn}} - \mathbf{B_{mn}U_{Qn}} + \mathbf{G_{mm}U_{Dm}} - \mathbf{B_{mm}U_{Qm}}, \tag{32}$$

$$\mathbf{I_{Qm}} = \mathbf{G_{mn}U_{Qn}} + \mathbf{B_{mn}U_{Dn}} + \mathbf{G_{mm}U_{Qm}} - \mathbf{B_{mm}U_{Dm}}, \tag{33}$$

where $\mathbf{G}$ and $\mathbf{B}$ refer to the real part and the imaginary part of the corresponding $\mathbf{Y}$ matrix. Following the solution of DC grid, the components $\mathbf{U_{Dm}}$ and $\mathbf{U_{Qm}}$ in the above equations are known, while the values of $\mathbf{U_{Dn}}$ and $\mathbf{U_{Qn}}$ associated with the detailed synchronous machines are not directly known. After each step of integration, the synchronous voltages can be evaluated by the state variables. Since the values of $\mathbf{U_{Dn}}$ and $\mathbf{U_{Qn}}$ are available after (30) and (31) are solved, the subsequent equation (32) and (33) can then be solved. Meanwhile, the calculated current vectors $\mathbf{I_{Dm}}$ and $\mathbf{I_{Qm}}$ in D-Q frame are sent to the HVDC system for its next time-step emulation, as given in Fig. 4 (b).

IV. Hardware Emulation on Multi-FPGA Platform

The proposed hybrid AC/DC grid is implemented on the integrated Xilinx Virtex® UltraScale+™ FPGA platform, which includes 2 VCU118 boards equipped with XCVU9P FPGA and 2 VCU128 boards containing XCVU37P FPGA. System 1 and 2 in Fig. 4(b) are deployed on the 2 VCU118 boards, respectively. Due to abundant hardware resources of VCU128 boards, System 3 and 4 including the 6-T HVDC system are implemented on VCU128 Board 1, while the remaining 2 AC systems (System 5 and 6) are calculated on VCU128 Board-2. The reconfigurability of the FPGAs enables each circuit part or subsystem to be designed as a hardware module, and allows programming its function according to the application. After linking the hardware modules and designing the parallel components properly, the integrated AC/DC grid can be executed on the proposed platform.

The subsystems and functions which consist of the proposed integrated AC/DC grid written in C/C++ code are transformed into hardware modules by Xilinx Vivado® high-level synthesis (HLS) tool. Then they, termed as IP cores, are imported into Vivado® for block-level design. Due to the dynamic voltage injection strategy, the PCC voltages in the D-Q frame are chosen as the communication data among different FPGA boards, which is realized by the build-in IP Aurora 66B/64B core. The hardware block diagram along with the data stream is given in Fig. 5.

Table I provides the latency and the hardware resource utilization of each circuit part in the proposed integrated AC/DC system, where the latency is defined in clock cycles which is 10 ns under the FPGA frequency of 100

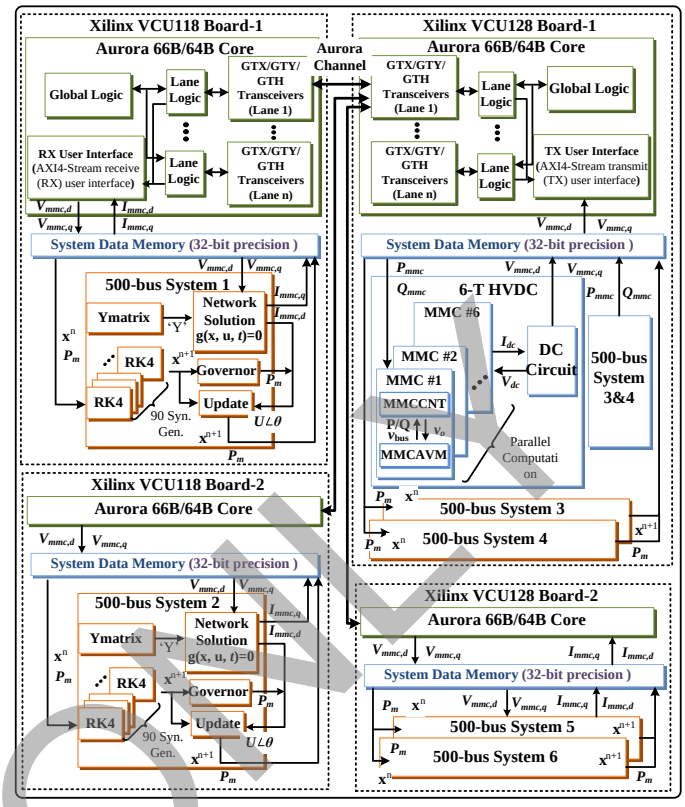

Fig. 5. Hardware implementation block design for the proposed FTRT DSA platform.

MHz. The total latency of the AC grid can be calculated as $29+196+114+21=360T_{clk}$, with a transient stability time-step of 1 ms, the FTRT ratio of the AC system is over $\frac{1ms}{360\times10ns}=277$. Since the hardware modules *PQcontrol*, *MMCAVM*, and *MMCCNT* can be solved in parallel, the overall hardware delay is determined by their maximum latency which is 96 $Tclk$, resulting in an FTRT ratio of $\frac{200\mu s}{96\times10ns}=208$. Thus, the overall FTRT ratio of the hybrid AC/DC grid as Case I is determined by the EMT emulation part, which gives a final 208 times speedup over real-time. In contrast, if a single ACTIVSg 500-bus system without DC grid is analyzed as Case II, the FTRT ratio of the pure AC grid is more than 277, where six 500-bus systems can be executed concurrently in the integrated FPGA boards.

Fig. 6 provides the hardware platform for FTRT emulation. The functions which represent the target power transmission system and the initial conditions of the synchronous generators are downloaded from the host computer via the Joint Test Action Group (JTAG) interface. Since multiple FPGA boards are assembled, data communication among them is also a challenge in emulating such a complex system. The Xilinx Virtex® UltraScale+™ series FPGA boards provide efficient communication ports, such as Quad Small Form-factor Pluggable (QSFP), Samtec® FireFly interfaces, which can significantly accelerate the communication speed, since both interfaces can provide a maximum bidirectional communication rate of 4×28 $Gbps$, which can be utilized for delivering the current operating conditions from real power transmission system or

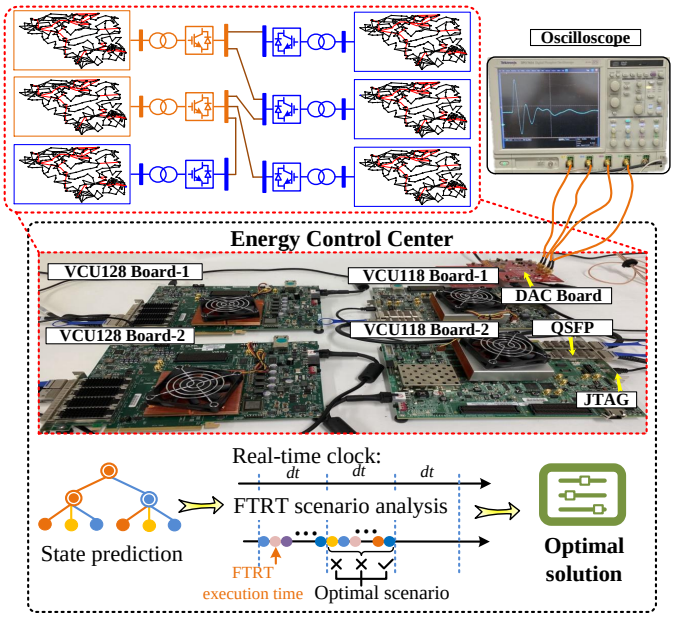

Fig. 6. Hardware implementation platform for FTRT DSA emulation and scenario analysis in the energy control center.

other FPGA boards, making the proposed FTRT emulation suitable for online DSA in the energy control center. Once a disturbance is detected, the real-time operation data from the field will be delivered to the control center. Meanwhile, there could be hundreds of scenarios being emulated in the FTRT emulation platform for a comprehensive study. Since a more than 208 FTRT ratio can be achieved, the power control center has sufficient time to come up with optimal strategies for contingencies in various subsystems that help maintain the stability of the entire system.

The scalability of the proposed FTRT emulation is demonstrated by interconnecting four FPGA boards in realizing the FTRT emulation, and more FPGA boards can be connected along with a further expansion of the AC/DC grid. Table I indicates that the hardware resources such as DSP and LUT of VCU128 board are nearly full for two 500-bus systems with 180 generators. Although the *Network* module will increase along with the size of the system, its influence can be neglected if multiple synchronous generators are included since the *Network* module is only calculated once in a single time-step. The hardware resource utilization is proportional to the synchronous generators, and therefore, a Xilinx® VCU128 board is able to accommodate about 180 generators with excitation and governor system in parallel. With a larger power system scale, the multiple FTRT emulators can be employed in the dynamic security assessment for HIL emulation or predictive control.

V. Contingency Screening Results and Validation

A. Dynamic Security Index

The contingency screening for dynamic security analysis is based on the system in Fig. 4. The transient stability analysis focuses on the rotor angle stability, voltage stability, and frequency stability, and the rotor angle stability is described

TABLE I
Specifics of Major AC/DC Grid Hardware Modules

Module	Latency	BRAM	DSP	FF	LUT
ACTIVSg 500-bus system on VCU128 ($100MHz$)					
RK4	29 T_{clk}	0	18	1939	2045
Network	196 T_{clk}	16	678	48921	54732
Governor	114 T_{clk}	0	19	4046	4132
Update	21 T_{clk}	0	35	3639	3970
HVDC system on VCU128 ($100MHz$)					
PQcontrol	45 T_{clk}	0	62	4398	5372
MMCAVM	96 T_{clk}	0	16	2582	5270
MMCCNT	86 T_{clk}	0	62	5829	6320
HVDCNetwork	73 T_{clk}	0	20	2488	3710
Total_VCU128	–	0.79%	93.15%	42.82%	97.46%
Total_VCU118	–	0.37%	59.11%	25.00%	51.99%
Available hardware resources					
VCU128	–	4032	9024	2607360	1303680
VCU118	–	4320	6840	2364480	1182240

as the power angle-based stability margin (ASM), which is defined as follows for each AC grid in the system.

$$ASM = \frac{360 - \delta_{max}}{360 + \delta_{max}} \times 100, \tag{34}$$

where δ_{max} is the maximum angle separation of any two generators in the same AC subsystem at the same time in the post-fault response, which is illustrated in Fig. 7 (a). The transient stability index of a contingency is chosen as the smallest index among all 6 AC grids. ASM is directly proportional to rotor angle separation so it provides an indication of severity of a disturbance. A smaller-than-zero ASM indicates that the δ_{max} is larger than 360 unit, which means the generators lose synchronism and the system is under unstable condition, while ASM>0 corresponds to a secure system status.

B. Case 1: Hybrid AC/DC Grid

At t = 1 s a three-phase-to-ground fault lasting 180 ms occurs at *Bus* 16 in *System 1*, the imminent impacts including severe disturbances to the rotor angles, bus voltages, and frequencies, as shown in Fig. 7 (a)-(c). Fig. 7 (a) demonstrates that the maximum angle separation (δ_{max}) is less than 360 unit, and therefore, the system is under secure condition. Although one of the frequencies exceeds the $\pm 1\%$ threshold after the three-phase fault, it restores to the normal operation eventually. Fig. 7 (d)-(f) provide the emulation results after a long-term over-load. At 1 s, a 90% over-load occurs to the load at *Bus* 392 in *System 1*. There are no significant impacts on the rotor angles of the synchronous generators as given in Fig. 7 (d). However, the bus voltages and the frequencies of the generators keep decreasing after the over-load disturbance and cannot be recovered by the generators' control system. The whole system enters the unstable condition at around 9 s when the frequencies reach below 59.4 Hz. The dashed lines represent the results calculated from the simulation tool TSAT®, while the solid lines refer to the FTRT emulation results from FPGA boards. The zoomed-in plots in Fig. 7 (b) and (f) demonstrate that the accuracy of the proposed FTRT emulation since the waveforms of the hardware emulation are identical to TSAT® off-line simulation results.

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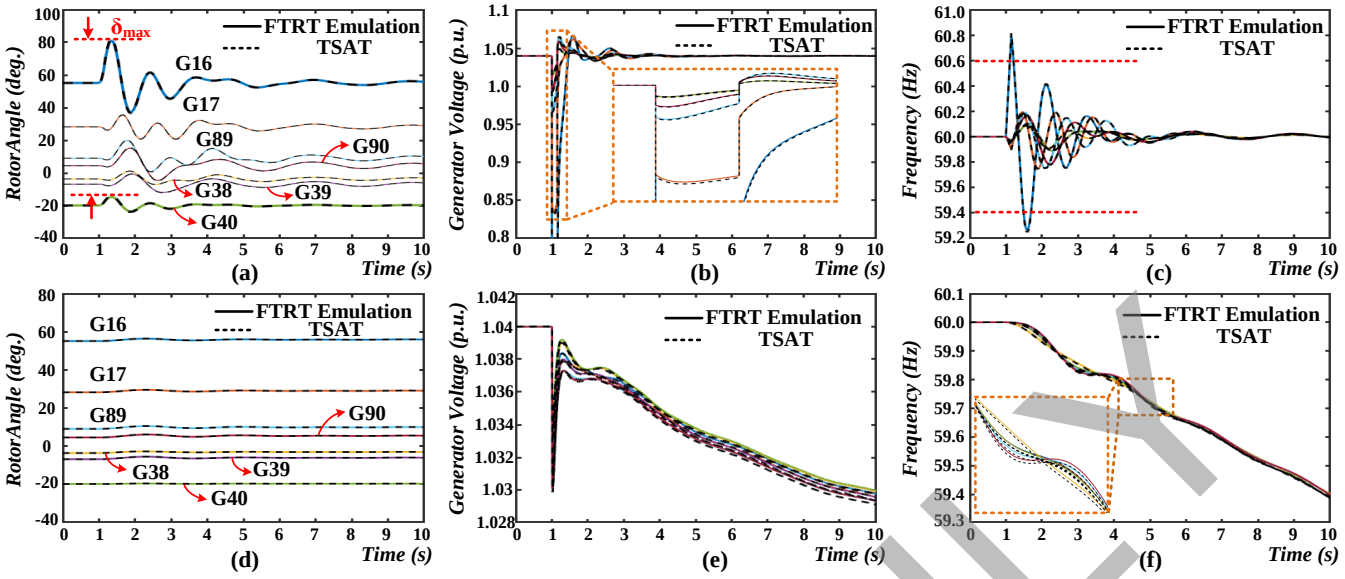

Fig. 7. FTRT emulation results: (a) generator rotor angles under three phase fault, (b) generator output voltages under three phase fault, (c) generator frequencies under three phase fault, (d) generator rotor angles under long term over-load, (e) generator output voltages under long term over-load, (f) generator frequencies under long term over-load.

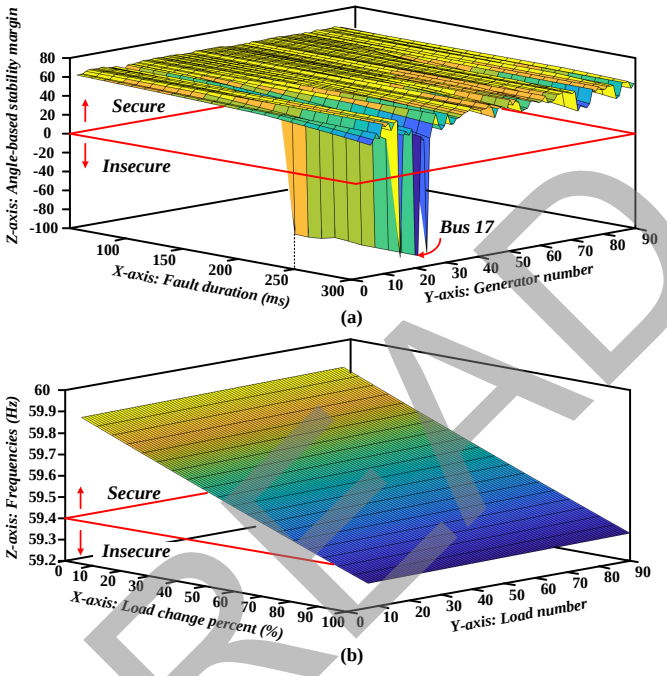

Fig. 8. Dynamic security indices of extensive contingencies: (a) ASM results of three phase fault contingencies, (b) frequencies of long term over-load contingencies.

TABLE II
CONTINGENCY SCREENING RESULTS AND ERRORS FOR 300MS THREE-PHASE-TO-GROUND FAULTS IN SYSTEM 1

Fault Gen.	ASM FTRT	ASM TSAT®	Error (%)	Fault Gen.	ASM FTRT	ASM TSAT®	Error (%)	Fault Gen.	ASM FTRT	ASM TSAT®	Error (%)
17	-86.64	-86.52	0.14	22	52.40	52.34	0.11	37	59.06	58.92	0.24
11	-85.42	-85.31	0.13	61	52.78	52.80	0.04	45	59.60	59.48	0.2
20	-85.34	-85.27	0.08	30	53.37	53.24	0.24	76	59.72	59.60	0.2
16	-85.23	-85.16	0.08	47	53.45	53.41	0.07	51	59.75	59.63	0.2
19	36.42	36.55	0.36	3	53.50	53.58	0.15	81	59.77	59.68	0.15
21	37.75	37.91	0.42	8	53.77	53.80	0.06	46	60.07	59.81	0.43
71	38.89	39.00	0.28	62	53.91	53.96	0.09	34	60.13	59.99	0.23
74	40.64	40.72	0.2	89	54.09	54.08	0.02	36	60.15	60.13	0.03
18	40.92	40.96	0.1	63	54.29	54.17	0.22	65	60.40	60.26	0.23
1	41.16	41.22	0.15	58	55.10	55.10	0.00	64	60.55	60.29	0.43
73	43.05	43.05	0.00	31	55.27	55.23	0.07	87	60.56	60.48	0.13
72	44.56	44.56	0.00	77	56.62	56.47	0.27	70	60.61	60.53	0.13
25	44.57	44.63	0.13	**32**	**56.86**	**56.58**	**0.49**	78	60.87	60.80	0.12
75	44.64	44.70	0.13	38	56.93	56.71	0.39	82	60.89	60.81	0.13
14	44.74	44.73	0.02	59	57.26	57.14	0.21	68	60.98	60.83	0.25
84	45.06	45.12	0.13	56	57.31	57.21	0.17	60	61.38	61.30	0.13
12	45.76	45.81	0.11	57	57.41	57.27	0.24	67	61.39	61.32	0.11
4	46.27	46.30	0.06	55	57.53	57.36	0.3	9	61.50	61.38	0.2
2	46.59	46.58	0.02	80	57.67	57.57	0.17	27	61.59	61.44	0.24
43	47.56	47.52	0.08	49	57.71	57.63	0.14	86	61.64	61.50	0.23
85	47.57	47.63	0.13	79	57.92	57.92	0.00	7	61.74	61.66	0.13
26	48.38	48.39	0.02	69	58.19	57.96	0.40	66	61.80	61.72	0.13
29	48.54	48.57	0.06	90	58.26	58.20	0.10	88	61.96	61.78	0.29
28	48.55	48.59	0.08	40	58.31	58.24	0.12	50	62.45	62.40	0.08
52	48.92	48.96	0.08	39	58.38	58.31	0.12	23	62.68	62.55	0.21
13	49.24	49.21	0.06	6	58.60	58.43	0.29	5	62.82	62.78	0.06
24	50.04	50.03	0.02	33	58.78	58.65	0.22	35	62.87	62.80	0.11
53	50.71	50.73	0.04	44	58.83	58.75	0.14	10	62.96	62.82	0.22
15	50.77	50.75	0.04	83	58.84	58.85	0.02	41	63.04	62.86	0.29
54	51.39	51.44	0.10	42	58.92	58.92	0.00	48	63.91	63.90	0.02

Fig. 8 (a) provides ASM results calculated from FTRT emulation under 1890 three-phase-to-ground fault contingencies in *System* 1. The x-axis denotes the fault duration ranging from 100 ms to 300 ms, and the y-axis is the fault locations at *Bus* 1 to 90, which are generator buses. As mentioned, the ASM results below zero represent the unstable conditions, and therefore, the whole system may come to an insecure state if a three-phase-to-ground fault lasting more than 250 ms occurs at *Bus* 17. Fig. 8 (b) demonstrates the frequencies after 9 s of the overload happening on the load number 1 to 90 with various overload percentages. It shows that the entire system is insecure regardless of which bus is overloaded by more than 80% for 9 s.

Aiming at demonstrating the accuracy of the proposed FTRT emulation, Table II gives the contingency screening results and errors for 90 300-ms three-phase-to-ground faults at each generator bus. The relative errors given in Table II are calculated by the following formula:

$$\epsilon = \frac{abs(ASM_{FTRT} - ASM_{TSAT})}{abs(ASM_{TSAT})} \times 100\%. \qquad (35)$$

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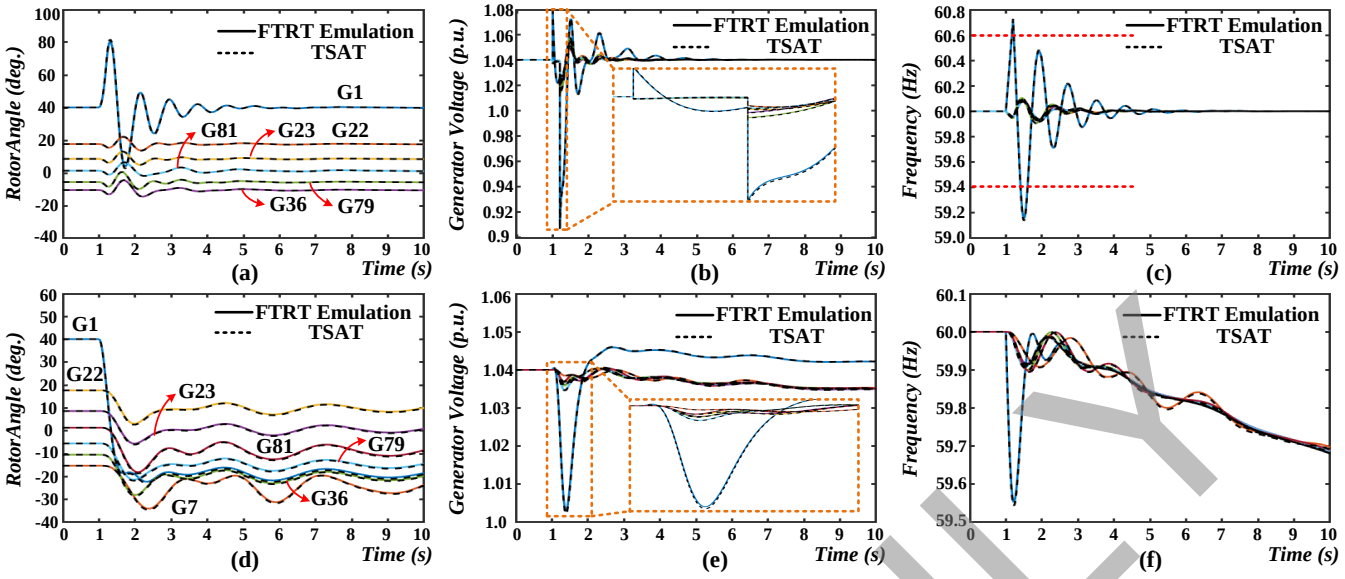

Fig. 9. FTRT emulation results: (a) generator rotor angles under open circuit on *Bus* 1, (b) generator output voltages under open circuit on *Bus* 1, (c) generator frequencies under open circuit on *Bus* 1, (d) generator rotor angles under generation reduction on *Generator* 1, (e) generator output voltages under generation reduction on *Generator* 1, (f) generator frequencies under generation reduction on *Generator* 1.

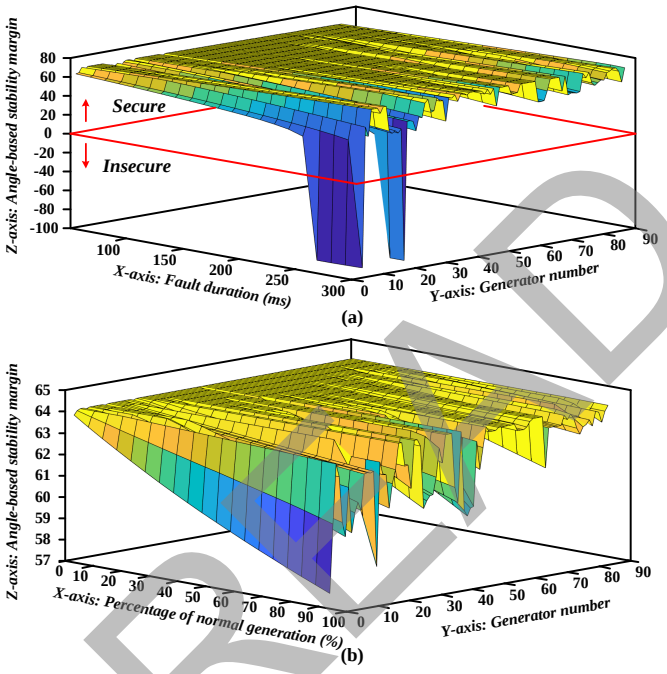

Fig. 10. Dynamic security indices of extensive contingencies: (a) ASM results of open circuit contingencies, (b) frequencies of generation reduction contingencies.

TABLE III
CONTINGENCY SCREENING RESULTS AND ERRORS FOR 300MS OPEN CIRCUIT FAULTS ON GENERATORS IN SYSTEM 1

Fault Gen.	ASM FTRT	ASM TSAT®	Error (%)	Fault Gen.	ASM FTRT	ASM TSAT®	Error (%)	Fault Gen.	ASM FTRT	ASM TSAT®	Error (%)
2	-88.18	-87.66	0.59	26	55.46	55.48	0.04	38	67.52	67.53	0.01
16	-86.96	-87.34	0.44	81	56.32	56.16	0.28	58	67.52	67.54	0.03
1	**-86.17**	**-86.88**	**0.82**	64	56.41	56.34	0.12	56	67.54	67.56	0.03
20	38.51	38.61	0.26	79	56.85	56.8	0.09	55	67.54	67.56	0.03
14	39.42	39.36	0.15	83	57.53	57.55	0.03	57	67.54	67.57	0.04
12	40.07	40.11	0.10	82	58.35	58.23	0.21	59	67.55	67.57	0.03
4	40.99	41.03	0.10	52	59.06	58.83	0.39	65	67.56	67.59	0.04
13	42.25	42.13	0.28	53	59.65	59.39	0.44	76	67.59	67.61	0.03
11	42.67	42.73	0.14	54	59.88	59.6	0.47	60	67.6	67.61	0.01
15	43.09	42.96	0.30	34	60.54	60.8	0.43	87	67.64	67.66	0.03
30	43.32	43.25	0.16	8	61.68	61.82	0.23	40	67.66	67.67	0.01
62	46.85	46.79	0.13	45	62.17	62.36	0.30	86	67.67	67.67	0.00
61	46.99	46.91	0.17	77	63.0	62.88	0.19	39	67.67	67.67	0.00
63	47.29	47.26	0.06	43	63.54	63.56	0.03	44	67.67	67.7	0.04
19	48.48	48.41	0.14	88	63.63	63.96	0.52	46	67.7	67.7	0.00
71	48.95	48.92	0.06	28	64.24	64.03	0.33	27	67.7	67.71	0.01
74	49.28	49.29	0.02	29	64.25	64.03	0.34	36	67.74	67.74	0.00
17	49.37	49.37	0.00	84	64.46	64.43	0.05	78	67.74	67.75	0.01
18	49.57	49.58	0.02	23	64.74	64.54	0.31	9	67.75	67.75	0.00
47	49.83	49.8	0.06	32	64.97	65.07	0.15	50	67.75	67.75	0.00
73	49.86	49.87	0.02	37	65.41	65.56	0.23	51	67.75	67.75	0.00
72	50.29	50.3	0.02	85	65.56	65.66	0.15	24	67.75	67.75	0.00
75	50.31	50.33	0.04	31	65.72	65.74	0.03	70	67.75	67.75	0.00
22	50.51	50.45	0.12	90	66.5	66.48	0.03	33	67.76	67.75	0.01
3	50.62	50.58	0.08	42	66.94	66.88	0.09	10	67.76	67.76	0.00
21	52.67	52.58	0.17	5	67.01	67.15	0.21	35	67.76	67.76	0.00
89	52.84	52.85	0.02	6	67.1	67.19	0.13	48	67.76	67.76	0.00
69	53.9	53.82	0.15	41	67.23	67.32	0.13	68	67.76	67.76	0.00
80	54.01	53.92	0.17	49	67.27	67.4	0.19	67	67.76	67.76	0.00
25	54.44	54.42	0.04	7	67.51	67.49	0.03	66	67.77	67.77	0.00

The maximum relative error among the 90 contingencies is 0.49 %, which thoroughly demonstrates the accuracy of the proposed method.

C. Case 2: Purely AC grid

In Case 2, the 6-T HVDC system is omitted, and a single ACTIVSg 500-bus system is taken into consideration. The utilization of the integrated FPGA platform enable six contingencies to run concurrently in the FTRT emulation platform with 277 FTRT ratios. The dynamic emulation results are provided in Fig. 9, where Fig. 9 (a)-(c) refer to an open circuit lasting 180 ms occurs at 1 s on generator *Bus* 1. The emulation results indicate that the system is under stable condition after the fault is cleared. Meanwhile, Fig. 9 (d)-(f) show the emulation results of 90% generation reduction on *Generator* 1. Fig. 9 (f) indicates that the frequencies of synchronous generators keep decreasing and cannot be restored.

Fig. 10 (a) gives the ASM results for 1890 open circuit contingencies that occur on each generator bus under various fault duration, which demonstrates that the entire system is

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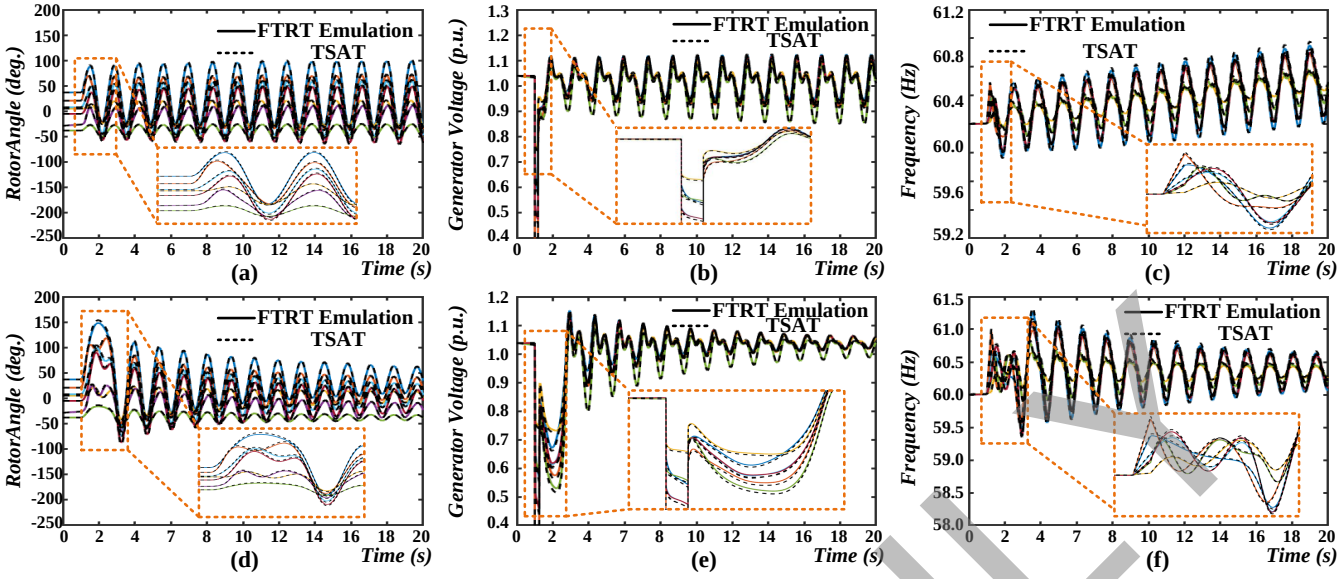

Fig. 11. Three-phase-to-ground fault for underdamped synchronous generators: (a) generator rotor angles, (b) generator output voltages, (c) generator frequencies; FTRT emulation results of three-phase-to-ground fault lasting 249 ms: (d) generator rotor angles, (e) generator output voltages, (f) generator frequencies.

more likely to be insecure with a longer fault. Fig. 10 (b) provides 900 ASM results for various generation reduction percentages of each generator. Although the ASM results show that the system is secure, the frequencies after the generation reduction will not be restored without extra power injection as given in Fig. 9 (f). It indicates that the proposed DSA platform may reveal more potential risks with the utilization of time-domain emulation. The contingency screening results for 90 open circuit faults are given in Table III. The maximum relative error is merely 0.81%, which demonstrates that the accuracy of the proposed FTRT emulation is suitable for online DSA in the energy control center.

D. Accuracy Validation

In order to validate the the accuracy of the proposed modeling and hardware implementation approaches, an underdamped case is emulated. Fig. 11 (a)-(c) provide the emulation results for an underdamped excitation system, where the PSSs for all synchronous generators have been removed. At $t = 1s$, a three-phase-to-ground fault lasting 180 ms occurs on *Bus* 17, the generator rotor angles start to oscillate without recovery. The zoomed-in plots in Fig. 11 (a)-(c) demonstrate that the FTRT emulation results are matched well with the results calculated from TSAT in an underdamped system.

Furthermore, the emulation results are also provided to validate the accuracy of the proposed FTRT emulation under a three-phase-to-ground fault which is cleared near the critical clearing time (CCT), as given in Fig. 11 (d)-(f). As Fig. 8 (a) shows the CCT of the three-phase-to-ground fault at the bus of *Bus* 17 is 250 ms. Therefore, Fig. 11 (d)-(f) provides the emulation results of a three-phase-to-ground fault lasting 249 ms at *Bus* 17. Fig. 11 (d)-(f) indicate that the fault causes a severe oscillation including rotor angles, bus voltages, and frequencies. The zoomed-in plots demonstrated the accuracy

TABLE IV
ASM RESULTS FOR THREE-PHASE-TO-GROUND FAULTS CLEARED NEAR THE CCT.

Fault Bus (*Bus* 17)				Fault Bus (*Bus* 20)			
Fault Dur.	ASM FTRT	ASM TSAT®	Error (%)	Fault Dur.	ASM FTRT	ASM TSAT®	Error (%)
248 ms	39.09	39.15	-0.10	295 ms	39.22	39.22	0.00
249 ms	36.22	36.28	-0.16	296 ms	36.62	36.61	0.03
250 ms	**-83.92**	**-83.78**	**0.17**	297 ms	-85.16	-85.12	0.05
251 ms	-85.41	-85.35	0.07	298 ms	-86.12	-86.07	0.07

of the proposed FTRT emulation can still be guaranteed even when the fault is cleared near the CCT. Meanwhile, the ASM results for two serious three-phase-to-ground faults calculated from FTRT emulation and TSAT are provided in Table IV, which indicates that the accuracy of the proposed method can be guaranteed for the contingencies that are cleared around the CCT.

The emulation time-step Δt is another important factor, which could influence the performance and accuracy of the FTRT emulation. As mentioned, 1 ms is utilized in the AC grid for DSA, while the time-step of 200 μs is adopted in the HVDC part for EMT emulation. The adoption of 200 μs is justified by the type of study in this work, where the converter system-level dynamics such as output power and reactive power, instead of the converter electromagnetic transient details, are the main focus. In the dynamic security assessment, the commonly used time-step ranges from 1 ms to 10 ms. A dramatic computational advantage can be achieved with the time-step of 200 μs, and a $\frac{200\mu s}{96\times 10ns} = 208$ FTRT ratio can be obtained. On the other hand, with the time-step of 50 μs, the FTRT emulation can still be achieved, given as $\frac{50\mu s}{96\times 10ns} = 52$. The emulation results of output active power of the *MMC* 1 and 3 under various time-steps and relative errors are given in Fig. 12.

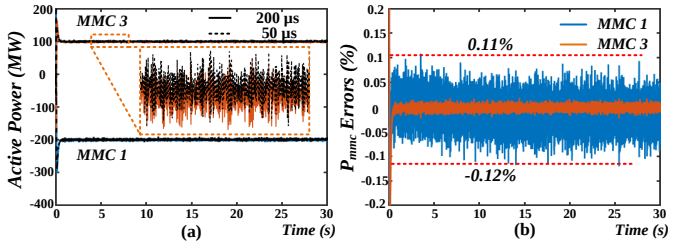

Fig. 12. FTRT emulation results: (a) active power of MMC 1 and 3 under different time-steps, (b) relative errors.

Fig. 12 (b) indicates that there is no significant improvement in emulation accuracy under the time-step of 50 μs. However, the acceleration has a significant drop if 50 μs is adopted. Therefore, after a trade-off between the emulation accuracy and computational speed, the 200 μs is selected as the emulation time-step of the HVDC grid.

VI. Conclusion

This paper proposed a screening strategy of extensive contingencies in faster-than-real-time mode of execution for a comprehensive dynamic security analysis of large-scale integrated AC/DC grid. Due to the pipelined hardware design method and parallelism of AC/DC grid modules, the EMT and TS co-simulation is introduced to provide more detailed operation conditions of the integrated AC/DC grid for dynamic security analysis. A dynamic voltage injection interface for AC/DC grid is proposed, which enables the EMT and TS co-simulation executing as one program without updating the admittance matrix in every time-step. The proposed interface strategy is also suitable for the data communication among FPGA boards as its less data transferred, which can further accelerate the FTRT emulation by reducing the communication delay. An FTRT ratio of 208 can be obtained for the hybrid AC/DC grid, while the FTRT ratio is over 277 times for a pure AC system. The contingency screening results of the more than 5500 contingencies from the FTRT DSA hardware emulation platform are well matched with those of TSAT® off-line simulation. Therefore, a guaranteed accuracy and execution speed of the proposed FTRT emulation methodology suggest its importance in planning and operation of a practical power system in scenarios such as online DSA.

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