Advanced Non-Uniform Sampling Techniques for Energy-Efficient Data Acquisition

by

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Abstract

With the growing demand for power-efficient data acquisition systems, particularly in low-power sensor applications that rely on energy harvesting or limited energy stored in small batteries, non-uniform sampling (NUS) techniques have gained attention as an effective approach to managing a restricted power budget while preserving the accuracy of the acquired data. Conventionally, signals are sampled uniformly independent of their shapes and frequency content, but NUS techniques intelligently reduce the overall collected data by selecting the most valuable data points for reconstructing sensed input signals. This approach remarkably aids data acquisition systems to reduce unnecessary power consumption in the critical system building blocks such as analog-to-digital converters (ADCs), digital signal processors (DSPs), and transceivers.

This thesis addresses the key challenges in designing and implementing NUS techniques to highlight their potential in developing power-efficient data acquisition systems. The primary objective of this research is to introduce new NUS schemes to further enhance the energy efficiency of the data acquisition systems and to conduct a comprehensive review study of NUS schemes. This research presents two innovative NUS schemes: The first scheme is an ultra-low-power clock-based non-uniform sampling scheme that uses a novel derivative-based algorithm that maintains accuracy comparable with prior clock-based non-uniform sampling schemes but with reduced complexity and lower power consumption. The second proposed scheme is a clockless NUS approach that employs a derivative-dependent mechanism that provides enhanced accuracy for high-frequency content compared to other clockless NUS

schemes while consuming less power. Both the proposed clock-based and clockless NUS techniques have been fabricated in CMOS technology and their performance has been characterized by experimental results when processing both real-world and ideal signals. The proposed clock-based Non-Uniform Sampling (NUS) system can operate with a clock frequency of up to 100 kHz, where power consumption scales proportionally to this frequency and is less than ∼155 nW at 1 kHz of the clock. The proposed clockless NUS scheme is presented in two versions of low- and high-speed designs where their maximum power consumption is 1.15 μW (@1 MHz) and 8.81 μW (@20 MHz), respectively. As the third contribution, this thesis provides a thorough quantitative and qualitative comparison of the prior art on NUS techniques; discussing their proposed implementations, design considerations, and/or limitations, and ultimately, evaluating their performance metrics.

Preface

This thesis is a compilation of original first-author works by Mohammad Elmi.

Chapter 2 of this dissertation is based on a study of a clocked non-uniform sampling technique that achieves high accuracy while consuming less power compared to prior state-of-the-art methods. This work has been published in the following journal paper, with minor modifications made after publication:

- M. Elmi, M. Lee and K. Moez, "An Ultra-Low-Power Non-Uniform Derivative-Based Sampling Scheme With Tunable Accuracy," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 70, no. 7, pp. 2788-2801, July 2023.

Chapter 3 presents a clockless non-uniform sampling scheme that offers higher compression of high-frequency content in signals compared to prior state-of-the-art techniques. This work has been submitted to the IEEE Internet of Things (IoT) Journal, with the following citation:

- M. Elmi, M. M. Elbadry, N. Jiang, and K. Moez, "A Clockless Derivative-Dependent Sampling Scheme for Energy-Efficient IoT Applications," in IEEE Internet of Things Journal (DOI: 10.1109/JIOT.2024.3440320, accepted for publication in Aug. 2024).

For these contributions, I was responsible for the concept, chip design, layout, and measurements. My supervisor, Dr. Kambiz Moez, assisted with the formation of the concept, chip layout, and measurements, and helped improve the manuscript quality.

Chapter 4 of this dissertation is a comprehensive review of prior non-uniform sampling techniques. This work is based on extensive simulations that the performance of different non-uniform sampling methods and presents various implementations, design considerations, and limitations. This review study will soon be submitted to IEEE Transactions on Circuits and Systems I: Regular Papers. Throughout this process, Dr. Moez provided valuable suggestions for the research and improvements to the manuscript quality. In preparing this thesis and contributing articles, Grammarly has been utilized as a writing aid tool to enhance the clarity and quality of the text.

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Special thanks to my supervisor, Dr. Kambiz Moez, whose guidance, insight, and encouragement have been pivotal in the completion of this thesis.

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"When will you begin that long journey into yourself?"

−Rumi

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Abbreviations

ADC Analog-to-Digital Converter.

AFE Analog Front-End.

AM Amplitude-Modulated.

BPM Beats Per Minute.

CB-ALC Clock-Based Adaptive Level Crossing.

CB-AR Clock-Based Adaptive Rate.

CB-LC Clock-Based Level Crossing.

CB-SDS Clock-Based Slope-Dependent Sampling.

CB-DDS Clock-Based Derivative-Dependent Sampling.

CF Compression Factor.

CL-MDLC Clockless Multi-Dimensional Level-Crossing.

CL-ADLC Clockless Adaptive Derivative Level Crossing.

CL-DLC Clockless Derivative Level Crossing.

CL-ALC Clockless Adaptive Level Crossing.

CL-LC Clock-Less Level Crossing.

CL-DDS Clock-Based Derivative-Dependent Sampling.

CMOS Complementary Metal-Oxide Semiconductor.

CPU Central Processing Unit.

CS Compressed Sensing.

DAC Digital-to-Analog Converter.

DSP Digital Signal Processor.

ECG Electrocardiography.

EEG Electroencephalogram.

FPGA Field-Programmable Gate Array.

HR Heart rate.

IC Integrated Circuit.

LC Level Crossing.

MDLC Multi-Dimensional Level-Crossing.

NUS Non-Uniform Sampling.

PA Power Amplifier.

PPG Photoplethysmography.

PR-SNDR Post-Reconstruction Signal-to-Noise plus Distortion Ratio.

PSD Power Spectral Density.

PSF Power Saving Factor.

RF Radio Frequency.

RMSD Root Mean Square Deviation.

SAR Successive Approximation Register.

SNR Signal-to-Noise Ratio.

TSMC Taiwan Semiconductor Manufacturing Company.

VGA Variable-Gain Amplifier.

Chapter 1

Introduction

Power-efficient data acquisition systems have become an integral part of modern data-driven technology with their growing applications in a variety of areas such as healthcare [1–5], industry [6, 7], and environmental monitoring [8, 9], where the collection, processing, and analysis, and/or utilization of data are essential. In the design of a power-efficient data acquisition system for such applications, the characteristics of the analog sensed input, such as amplitude range and frequency content, and the targeted output quality must be well investigated [3–5, 10–16]. Furthermore, the design might be restricted due to practical limitations such as power consumption, cost, complexity, and technology. Figure 1.1 illustrates the major trade-offs between the above parameters that can be observed in the design of a data acquisition system [14, 17–23], where the conversion of an input signal with a small amplitude range (a few μV) or higher frequency content (several gigahertz) generally requires a higher targeted accuracy leading to a more complex and power-consuming design. Among the above trade-offs, the relationship between the targeted output accuracy and overall power consumption is the greatest concern, which several prior studies attempted to overcome [14, 15, 18–23]. This is accomplished by employing novel techniques that allow a data acquisition system to minimize the amount of data (number of signal sampled points) by wisely choosing only the most essential sampled points of the received signal required to reconstruct it with a representation of acceptable accu-

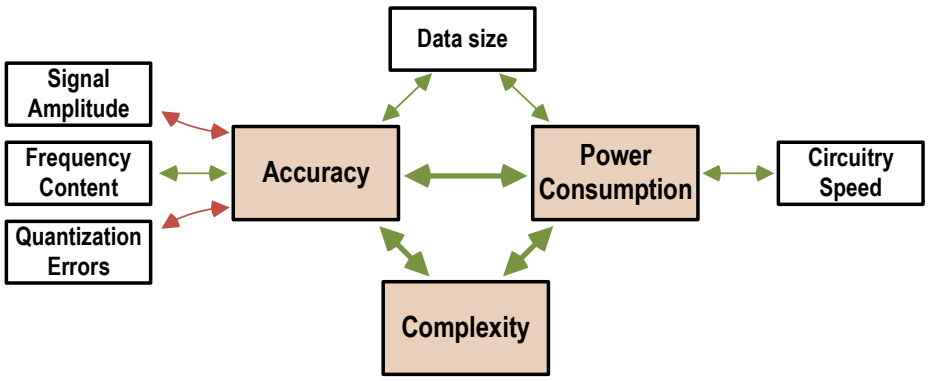
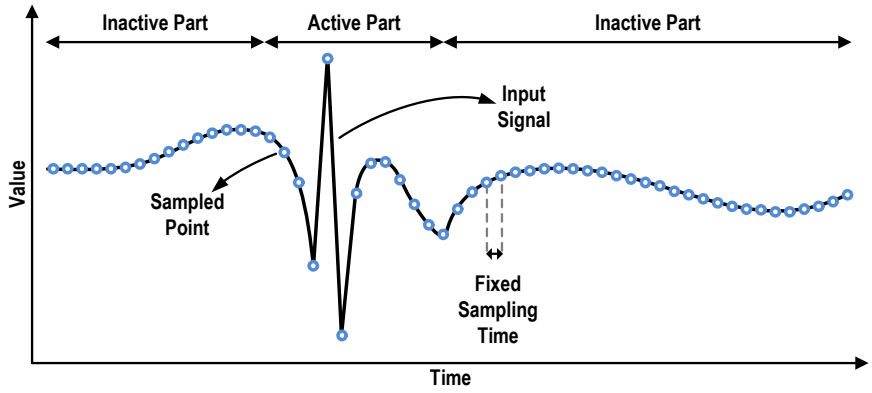


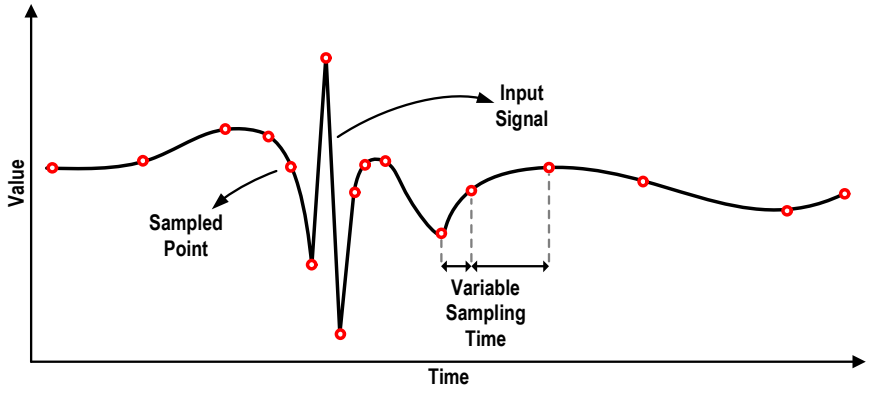
Figure 1.1: Major trade-offs in the design of a data acquisition system.

racy. It is important to note that both the signal power and accuracy (represented by the quality of the recovered signal) are primarily dependent on the amount of data collected by an acquisition system.

The issue of the power-accuracy trade-off cannot be easily solved in a conventional data acquisition system, where the input signal is still uniformly sampled at a fixed frequency, without taking into account any characteristics of the signal except its bandwidth (Figure 1.2(a)). In such an acquisition system, a considerable amount of power is inevitably dissipated in several scenarios, such as low-frequency content or inactive parts of the original signal, where unnecessary sampled points are converted to digital data, then processed, stored, and/or transferred [14–16]. As an example, only a few selected points in the inactive areas of the signal, shown in Figure 1.2(b), are sufficient to reach almost the same accuracy as conventional uniform sampling. A solution to avoid this unnecessary power dissipation might be to reduce the sampling rate to reduce the amount of data; however, for a uniform sampling scheme, the sampling rate must be higher than the Nyquist rate to permit accurate output signal reconstruction [14, 16, 24]. Another solution to alleviate this problem might be using digital data compression techniques such as Compressed Sensing (CS). Although the received signal is uniformly sampled, the volume of data is compressed on average (especially for the sparse signals [14, 25]) at the cost of a slight reduction in accuracy. In particular, this can reduce the power dissipation of some system building blocks



(a)



(b)

Figure 1.2: Sampling an example signal by (a) uniform and (b) non-uniform methods.

such as the transmitter, for example, which sometimes contributes the most power dissipation, up to 95% in some sensor system designs [14, 24, 26]. However, digital compression techniques may not be easily achieved, especially at higher frequencies, as they require high-speed processors that implement relatively complex equations. Additionally, CS-based techniques suffer from other limitations such as sensitivity to noise [27] and greater design complexity [28] as well as the fundamental limitations of uniform sampling [14, 15].

An alternative solution to satisfy the critical power budget of a data acquisition system while having a good output quality is to use NUS techniques rather than conventional uniform sampling ones. In a NUS scheme, a set of the most valuable points for the reconstruction of a signal are wisely selected, stored, and converted to digital data. Figure 1.2(b) depicts a scenario in which a NUS scheme is applied to the signal

and certain points are selected at certain events, called significant events. Compared to the uniform sampling shown in Figure 1.2(a), the output signal in this scenario can be reconstructed with a noticeably smaller number of points while the accuracy is fairly similar. This means in a NUS scheme, unlike in uniform sampling, power is consumed only when a significant event is detected, which is a great assistance in many applications, especially for those powered by a small battery or energy harvesting [29, 30]. Implantable and ingestible biomedical devices and environmental sensors might be a few examples of these applications where the signal includes long periods of silence and where a uniform sampling would waste significant dynamic power in the Analog-to-Digital Converter (ADC), Digital Signal Processor (DSP), transceivers, and other building blocks of a system [16, 17, 31].

The process of significant event detection in an NUS scheme is generally accomplished through analog signal prepossessing by a NUS block that utilizes analog circuits that implement the mathematical definition of significant events in the analog domain according to the scheme. Figure 1.3 shows a general overview of possible implementations of the uniform and NUS schemes. A uniform sampling scheme simply collects the data using a clocked ADC (Figure 1.3(a)) while the NUS block in a NUS scheme first operates an analog signal pre-processing stage to detect the next significant event in the signal, and only then triggers/activates the ADC to convert the present analog signal level to digital data. Depending on the NUS scheme, the NUS block might be placed in the receiving path by the ADC, as shown in Structure I in Figure 1.3(b), and thus, it degrades the Signal-to-Noise Ratio (SNR) during signal pre-processing. However, in other schemes, the NUS block can be separated from the receiving path, as shown in Structure II in Figure 1.3(c), where the ADC is directly connected to the input signal. Additionally, the conversion and the NUS blocks might be indistinguishable from some other NUS techniques, as will be explained in the following sections. Unlike the first two clockless NUS structures, an NUS block can also operate with an external clock, as shown in Structure III in Figure 1.3(d). In such a

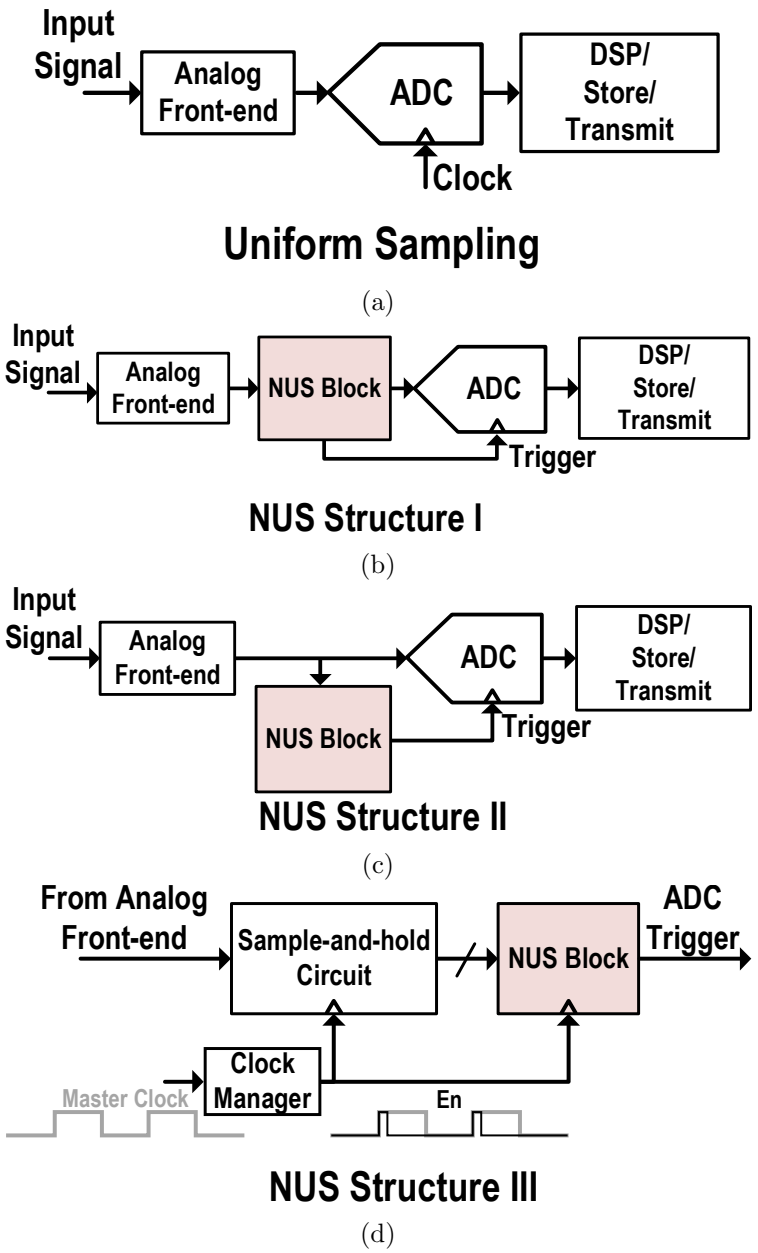


Figure 1.3: An overview of different implementations of uniform and NUS schemes.

structure, the signal is initially sampled and then the NUS block determines if there is any significant event based on one or a set of initial sampling points.

The initial sampling and detection process by a clock-based NUS block can be completed in a fraction of the clock pulse width, as shown in Figure 1.3(d), therefore, a substantial power saving is expected compared to a clockless NUS which continuously consumes the power to monitor the signal for significant events. On the other

hand, a clock-based NUS scheme is mostly used for low-frequency applications as it shows significant errors in the reconstruction of signals with high-frequency content unless a high power is consumed. This is due to the minimum time required for the initial sampling and the subsequent signal pre-processing, which limits the bandwidth of the scheme. The current consumption reported in [14], for example, is around 10 μA at the clock frequency of 10 kHz, while the technique consumes 10 times less power ($\sim$ 1 μA) at the clock frequency of 1 kHz. In general, the power consumption of a clock-based NUS linearly scales with the frequency of the clock, while the clockless schemes show almost a constant behavior over an operating frequency range. Figure 1.4 confirms this behavior by presenting the power consumption of the two clock-based NUS schemes proposed in [14] and [15], and comparing them with a clockless NUS (presented in this thesis in Chapter 3). It is clear that the power advantage of the clock-based schemes diminishes at frequencies higher than 10 kHz, whereas the clockless scheme exhibits almost constant power consumption across the covered frequency range. The initial sampling required for the clock-based NUS scheme poses a difficulty at the high-frequency regime of the clock, especially in the presence of noise. In contrast, the clockless NUS schemes can process high-frequency content thanks to their continuous monitoring of the signal; to achieve this, the NUS building blocks should have sufficient speed for monitoring the fast-changing parts of the signal. As a result, clockless schemes can achieve enhanced reconstruction accuracy at higher frequencies while consuming less power consumption as they do not require synchronization with an external clock. However, clock synchronization in clock-based schemes facilitates the reconstruction process on the receiver side, particularly in wireless systems, as it reduces the transfer of essential data for reconstruction since the signal level data at significant events and the interval between these events are sufficient for a precise reconstruction when synchronized with a clock. Table 1.1 summarizes the above discussion on the clock-based and clockless NUS.

The concept of sampling based on prior events inside the signal was originally

Table 1.1: Clock-based vs. clockless NUS schemes.

Clock-based NUS	**Clockless NUS**
Discrete Monitoring (Significant events in sampled points)	Continuous Monitoring (Significant events at input signal)
✓Ultra-low-power @ low freq. ✗Relatively higher power @ high freq.	✗Relatively higher power @ low freq. ✓Low-power @ high freq.
✗Mostly limited to low-freq. applications	✓Able to process high-freq. content
✗Requires an external clock	✓No need for an external clock
✗Requires initial sampling	✓No need for initial sampling

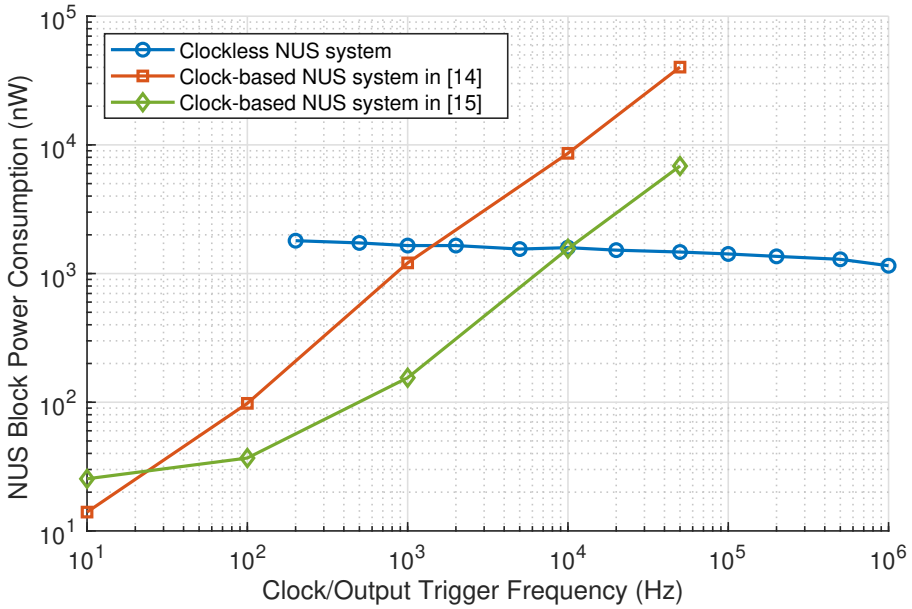


Figure 1.4: Power comparison clock-based and clockless.

introduced to aid control systems [32–34]. Difficulties and limitations associated with analog implementations of the equations that define the significant events delayed its involvement in the data acquisition techniques. The applications, mostly known as NUS methods, in ADCs and DSP are more recent and growing [16]. Particularly, the growing demand for batteryless or compact battery-powered devices has attracted attention as methods for increasing power efficiency [16, 17, 29–31].

1.1 A Review of Prior Non-Uniform Sampling Techniques

As stated, the NUS schemes can be categorized into clock-based and clockless methods. In clock-based schemes, the input signal is initially sampled at a master clock rate retaining the sampled points whenever a pre-defined significant event is detected, and all other sampled points are dropped. The ADC is then triggered at only the significant event times to convert the retained sampling points, the points detected by the scheme as the most valuable points for reconstruction, while remaining off for the rest of the time. Therefore, the number of required sampling points for representing the input signal is reduced in comparison to a uniform Nyquist-rate sampling scheme, thereby reducing the power consumption of the overall system by processing, storing, and/or transmitting fewer sampled points. In clockless NUS schemes, the input signal level is continuously monitored for the detection of significant events without any initial sampling. Therefore, the retained points are not necessarily sampled at multiple fixed intervals (master clock periods). Similar to clock-based schemes, the power consumption of the overall system is reduced as a result of processing fewer sampled points compared to a uniform sampling scheme. The following subsections briefly review some of the clock-based and clockless NUS schemes and compare their performance in terms of accuracy, power consumption, and maximum operating frequency.

1.1.1 Clock-based NUS Schemes

In this subsection, we discuss two clock-based sampling schemes: (i) Clock-based Level Crossing (CB-LC) and (ii) Clock-Based Slope-Dependent Sampling (CB-SDS). In CB-LC, the significant events are detected by comparing the input signal voltage level to predefined reference levels, while the other scheme, CB-SDS, monitors signal changes over time to produce the ADC triggers. Figure 1.5 illustrates how these two

sampling schemes detect significant events when applied to an arbitrary input signal. In the CB-LC technique, Figure 1.5(a), the initial sampling points (X_{00} to X_{20} gray points) are compared to some predefined reference levels ($R0$ to $R4$ green lines) so that whenever the signal crosses any of the reference levels, the sampling point is retained (blue points). The reference levels can be defined with regular intervals (known as the quantization steps) or varied depending on the characteristics of the input signal [35]. A zero-order hold is generally used for the reconstruction of the signal using the retained sampling points, but a first-order or higher-order linear interpolation can be also utilized for higher accuracy of the reconstructed signal often at the expense of higher power consumption and complexity [14, 15, 35]. A Compression Factor (CF) can be computed in a clock-based NUS scheme by dividing the number of initial sampling points (known as the number of points sampled and stored in a uniform sampling) by the number of the retained sampled points decided by the NUS scheme. The calculated CF directly corresponds to the power consumption saving of the overall system, often quantified by the Power Saving Factor (PSF), as it represents the reduction in the number of points that need to be stored, processed, and/or transmitted [14, 15]. In the sample scenario shown in Figure 1.5(a), a CF of 2 is achieved, which can be decreased or increased by adding or removing reference levels, respectively.

The CB-SDS scheme, proposed in [14], monitors the rate of the change in the signal slope to detect significant events. The scheme calculates (a) the slope of the last two sampled points and (b) the slope of the second last sampled point and the last retained point. Then it compares the difference between these two slopes to a predefined threshold value, known as ε. If the difference is greater than the threshold, the scheme considers it a significant event in the signal and retains the second last sampled point. This mathematical equation for the significant event, implemented

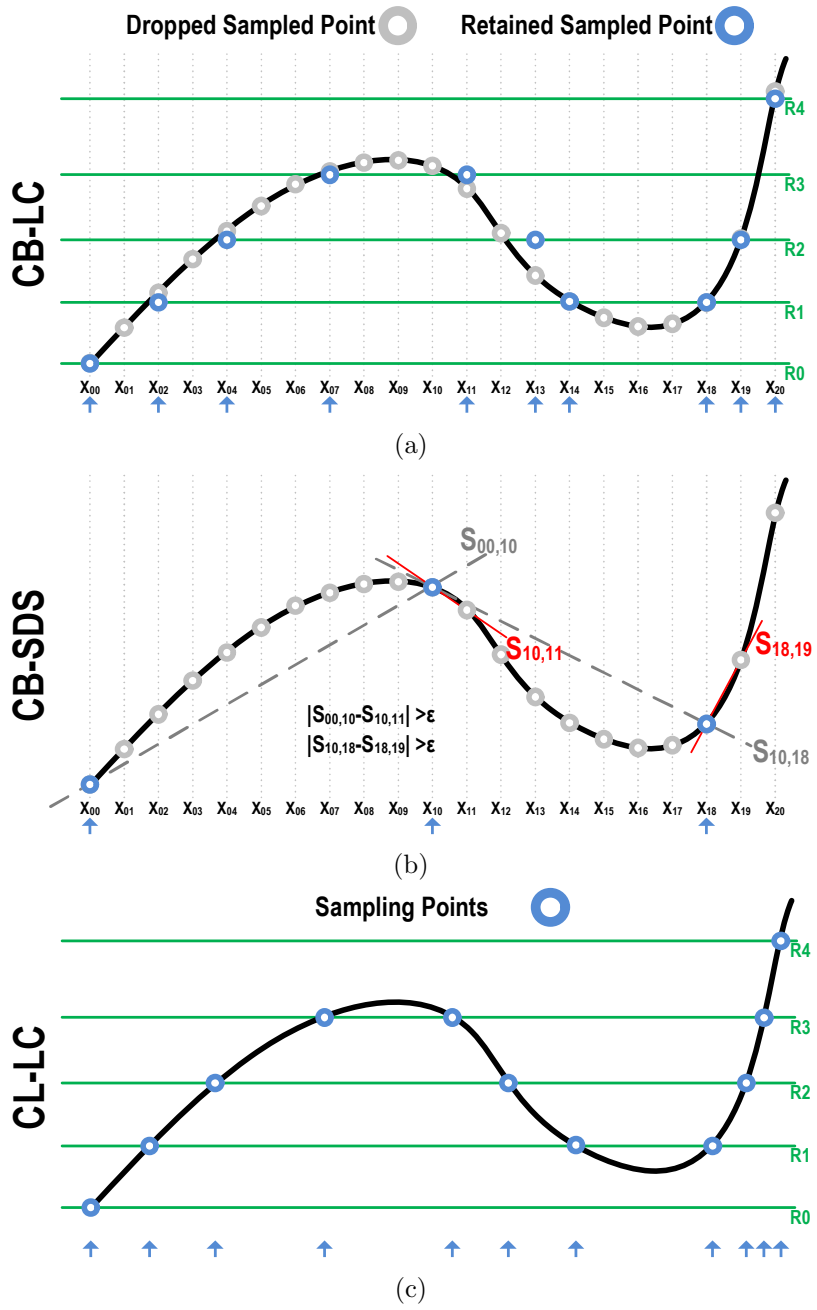


Figure 1.5: Detection of significant events in an arbitrary signal by three NUS schemes: (a) CB-LC, (b) CB-SDS, and (d) CL-LC.

by CB-SDS scheme using an analog circuit, can be written as

$$|S_{n,n-1}{-}S_{n-1,m}| = \left| \frac{X_n{-}X_{n-1}}{T_s} - \frac{X_{n-1}{-}X_m}{(n{-}m{-}1) \times T_s} \right| \geq \varepsilon, \tag{1.1}$$

where X_m, X_{n-1}, and X_n are the last retained, the second last, and the last sampled points, respectively, T_s is the sampling period, and ε is the threshold value. In the

example shown in Figure 1.5(b), two significant events have been detected, therefore, three sampling points (X_{00}, X_{10}, and X_{18}) are retained to reconstruct the input signal. Decreasing or increasing the threshold value results in retaining more or fewer sampling points (decreasing or increasing CF), respectively.

For the above clock-based schemes to effectively reduce the power consumption of the NUS block, the process to determine the significant event must be completed in a small fraction of the master clock period. Accordingly, they have to turn on the circuits implementing the clock-based NUS block for only a short time interval and turn them off for the rest of the clock period [14, 15]. This makes the clock-based NUS blocks more power-efficient in low-frequency applications; however, the power consumption of these blocks increases linearly with the master clock frequency, making them less power-efficient at higher frequencies. In addition, the required initial sampling time in the clock-based NUS schemes limits the maximum operating frequency as the signal cannot be properly sampled in an overly small fraction of the master clock period for high sampling rates. For example, the maximum operating frequencies reported for the CB-SDS scheme is 50 kHz [14, 15].

Generally, there is always a trade-off between the CF and the accuracy of the reconstructed signal in an NUS scheme; the greater the CF, the less the accuracy, and vice versa. The state-of-the-art NUS schemes try to achieve higher accuracy by enhancing the detection mechanism of the significant event such that the reconstructed signal is more accurate while having the same CF. However, it also makes the implementation of the NUS scheme more complex as the mathematical equation defining the significant event is more complicated. It may also lead to more power consumption in the detection process as more building blocks are required.

Table 1.2 compares the above two clock-based NUS schemes in terms of their complexity, power consumption, decision delay, SNR degradation in the detection process, and accuracy. Among these two schemes, CB-SDS implements a complex mathematical relation, defined for the detection of its significant events, requiring

Table 1.2: A performance comparison between clock-based NUS schemes.

	CB-LC	CB-SDS
Complexity	Low	High
Power Consumption	Low	High
Decision Delay	Low	Two Clock Cycles
SNR Degradation	Yes (Low)	Yes (High)
Accuracy (in a given CF)	Low to Moderate	High

three sample-and-hold circuits, three subtraction amplifier stages, and an analog divider in addition to the clock manager and control logic gates [14]. The more complex decision-making helps CB-SDS to achieve higher accuracy at the cost of higher power consumption. The CB-LC offers the minimum complexity in the design as it only needs to compare the input voltage level to the reference levels [15]. However, it achieves a lower accuracy while offering a lower power consumption.

The decision delay is also another important performance parameter in the NUS systems. In a clock-based NUS scheme, the decision delay mostly depends on the master clock frequency, as the detection process requires collecting more than a single sampling point, and/or the decision process is often completed in the next clock cycle after the last sampled point. The CB-LC can offer the least decision delay as the reference levels can be fixed at certain thresholds; however, the CB-SDS requires two clock cycles for generating a decision on the significant events. Some SNR degradation is expected due to the NUS block's decision delay since it results in a delay in triggering the ADC. Additional analog signal processing required in some NUS schemes may also result in further SNR degradation [15].

In summary, the clock-based NUS schemes have been proven to be effective in reducing the power of a data acquisition system as they adaptively change the sampling rate based on the signal characteristics only triggering/enabling ADC and other power-hungry blocks of the system when significant events are detected. The clock-

based NUS building blocks themselves do not consume significant amounts of power by operating within a small fraction of the master clock period. However, the implementation of the mathematical relation for the detection of significant events is performed at regular time intervals dictated by the frequency of the master clock, making them incapable of detecting significant events that occur between the sampled points. This can be potentially resolved by increasing the master clock frequency; however, the clock-based NUS blocks require a minimum time to properly sample and process the signal, which limits the highest master clock frequency. For example, the maximum clock frequency is 50 kHz for the reported CB-SDS scheme [14, 15]. Moreover, in some NUS schemes the decision process to detect a significant event requires more than one sampled point producing a delay that may be equal to two or three clock cycles [15]. As a result, these schemes cannot be applied to high-frequency signals as the signal may significantly change while the decision is being made resulting in considerable inaccuracy in these applications. It is worth noting that the required external clock generator also adds complexity and power consumption to the design. The aforementioned drawbacks make employing the clock-based NUS systems difficult for higher frequency applications with acceptable accuracy.

1.1.2 Clockless NUS Schemes

As opposed to clock-based NUS, the input signal is continuously monitored for the detection of significant events in clockless NUS schemes. The continuous monitoring of the input signal ensures that no significant event will be missed at the cost of the static power consumed by the continuous operation of the NUS block. For example, the input signal level is continuously compared to the reference levels in a CL-LC scheme, the only reported clockless scheme, without any initial sampling (Figure 1.5(c)). Therefore, the sampled point is retained when the input signal crosses a reference level, not limited to any time frame. The scheme is expected to retain more sampling points in the fast-moving segments of the signal as the signal crosses

more reference levels in these parts while triggering the rest of the system at a much lower rate for slow-moving parts of the signal. This results in a significant reduction in the power consumption of the overall system. The implemented equation for the significant event in CL-LC is the same as in the clock-based one except that the input signal is not sampled at regular time intervals. While the decision process is no longer controlled by a master clock frequency, allowing the clockless NUS scheme to be applied to higher frequency signals, the speed of the detection circuitry trades off with the accuracy of the reconstructed signal: the faster the clockless NUS block, the less decision delay and the more accurate the reconstructed signal but the higher the power consumption of the NUS block. The accuracy of a CL-LC scheme is also dependent on the number of reference levels, considering that the power increases for the higher resolution.

Various circuit implementations have been proposed for the CL-LC scheme in the literature [16, 35–37] with the principle idea of comparing the signal level to a reference level or a quantization step. The reference levels or the quantization step can be tuned depending on the signal characteristics as well, e.g., the quantization step is increased in [35] in the fast-moving segments of the signal, helping the system to enhance monitoring of the signal. These modifications, however, have no impact on the principal idea of crossing levels.

1.2 Motivation

There are many applications that have to be powered by small batteries or energy harvesting [14, 16], so their critical power budget should be spent carefully. Implantable and ingestible biomedical devices and environmental sensors are a few examples of these applications [16]. The signals acquired in these applications generally include a long period of silence and uniform sampling would waste remarkable dynamic power of ADCs, Digital Signal Processors (DSPs), transceivers, and other building blocks of system [14–16]. As stated earlier, utilizing an NUS scheme can greatly help with

these applications by reducing the overall power consumption while preserving an acceptable output signal quality. This may provide remarkable opportunities to (a) reduce the size of batteries or possibly even eliminate them so that smaller, lighter, and lower-cost devices can be fabricated; (b) increase the lifetime of the batteries so that devices can perform within a longer time; (c) making wired power devices wireless and opening opportunities to other applications, and (d) saving the critical power budget to enhance the overall performance of the device.

Although NUS schemes considerably benefit the data acquisition systems, the usage of a NUS scheme may encounter many challenges that should be carefully considered. Some of these challenges are:

(I) Classified into two major categories of clock-based and clockless methods, prior NUS schemes have defined various significant events and have implemented them with analog circuits in different structures. The lack of a comprehensive study on the different NUS schemes and their implementations makes selecting a suitable one for any particular application more challenging. There are design considerations and non-idealities that need to be investigated more so that pragmatic applications can be achieved.

(II) There are certain challenges in the design and usage of clock-based NUS schemes. Most of the prior clock-based NUS methods potentially degrade the input SNR by the presence of NUS block in the signal path. Furthermore, the process of decision-making in these schemes suffers from trade-offs between accuracy, power consumption, and complexity. The prior proposed clock-based techniques that can produce significantly higher output accuracy than others have the drawbacks of higher complexity in design and higher power consumption. In contrast, prior low-complex, clock-based NUS structures with lower power consumption achieve lower output quality.

(III) Although the clockless NUS schemes do not require an external clock and can operate at considerably higher frequencies with respect to clock-based schemes, they face their own challenges. Prior proposed clockless NUS schemes require relatively

high-speed, power-hungry building blocks when dealing with higher frequency content in the signal; otherwise, the output quality might not be satisfactory. In addition, prior clockless NUS schemes may not sufficiently reduce the overall number of points required for an acceptable reconstruction of an input signal.

1.3 Thesis Objectives

This thesis looks for innovative solutions to the aforementioned challenges. In summary, the thesis objectives can be expressed as follows:

(I) To address the challenge regarding the lack of comprehensive study on NUS schemes, this thesis provides a comparative study of the NUS schemes where various NUS techniques and their suggested implementations are introduced, and their different design considerations are discussed, and ultimately, their performance in terms of most important parameters such as power consumption, signal reconstruction accuracy, signal frequency coverage, design complexity, cost, *etc*, is compared to each other. This thesis also investigates the non-idealities and the challenges they cause in the design of NUS techniques.

(II) To address the second challenge regarding the trade-off between accuracy, complexity, and power consumption in the clock-based NUS schemes, this thesis develops and proposes a novel clock-based NUS technique that monitors the changes in the derivative of the input signal, and compares these changes to a tunable threshold to detect significant events. This novel Clock-Based Derivative-Dependent Sampling (CB-DDS) technique breaks this trade-off by presenting a comparable complexity and power consumption to the clock-based NUS schemes with minimal complexity and power consumption while resulting in a high accuracy on par with the clock-based schemes with maximal complexity and power consumption. The proposed CB-DDS technique also does not affect the input SNR by providing a separate path for the NUS block. The proposed CB-DDS technique is fabricated in TSMC's 0.13-μm CMOS technology and tested with real-world biomedical signals.

(III) To address the third challenge regarding a need for high-speed power-hungry building blocks in a clockless NUS scheme when dealing with high-frequency content of an input signal, this thesis develops and proposes a novel clockless NUS technique using a derivative-dependent mechanism that provides enhanced accuracy compared to other non-uniform sampling schemes while consuming less power. This Clockless Derivative-Dependent Sampling (CL-DDS) scheme also reduces the overall number of points required for the reconstruction of the signal while presenting an accuracy approximately as same as prior clockless NUS schemes. In the proposed scheme, the change in the derivative of the signal is continuously compared to the threshold references to obtain any desired accuracy. The proposed scheme can be scaled and can cover higher frequencies, and is implemented in low- and high-speed systems that target the low- and high-frequency applications, respectively, and fabricated in TSMC's 0.13-μm CMOS technology. The overall performance is evaluated by the experimental results from the real-world and ideal signals.

Chapter 2

An Ultra-Low-Power Clock-Based Non-Uniform Derivative-Based Sampling Scheme with Tunable Accuracy

As discussed earlier, the process of decision-making in the prior proposed clock-based schemes suffers from trade-offs between accuracy, power consumption, and complexity. Therefore, in this thesis we propose a scheme that can produce significantly higher accuracy than the CB-LC method while implementing it with less complexity and power dissipation than the CB-SDS technique.

2.0.1 Proposed Clock-based Derivative-Dependent Sampling (CB-DDS) Scheme

As depicted in Figure 2.1(a), in the CB-DDS method the difference between the instantaneous derivative of the signal ($D2$) and the last retained derivative ($D1$) is compared to a threshold value (ε). Exceeding this difference from the threshold value (*i.e.* $|D_2 - D_1| > \varepsilon$), represents a significant event and thus the point corresponding to the instantaneous derivative is converted by the ADC and $D2$ is stored. To implement an ideal CB-DDS system, the input signal is first connected to a differentiator producing an instantaneous derivative of the input signal at its output. Considering that the sample-and-hold circuit ($S\&H_m$) retains the derivative at the last sampled input,

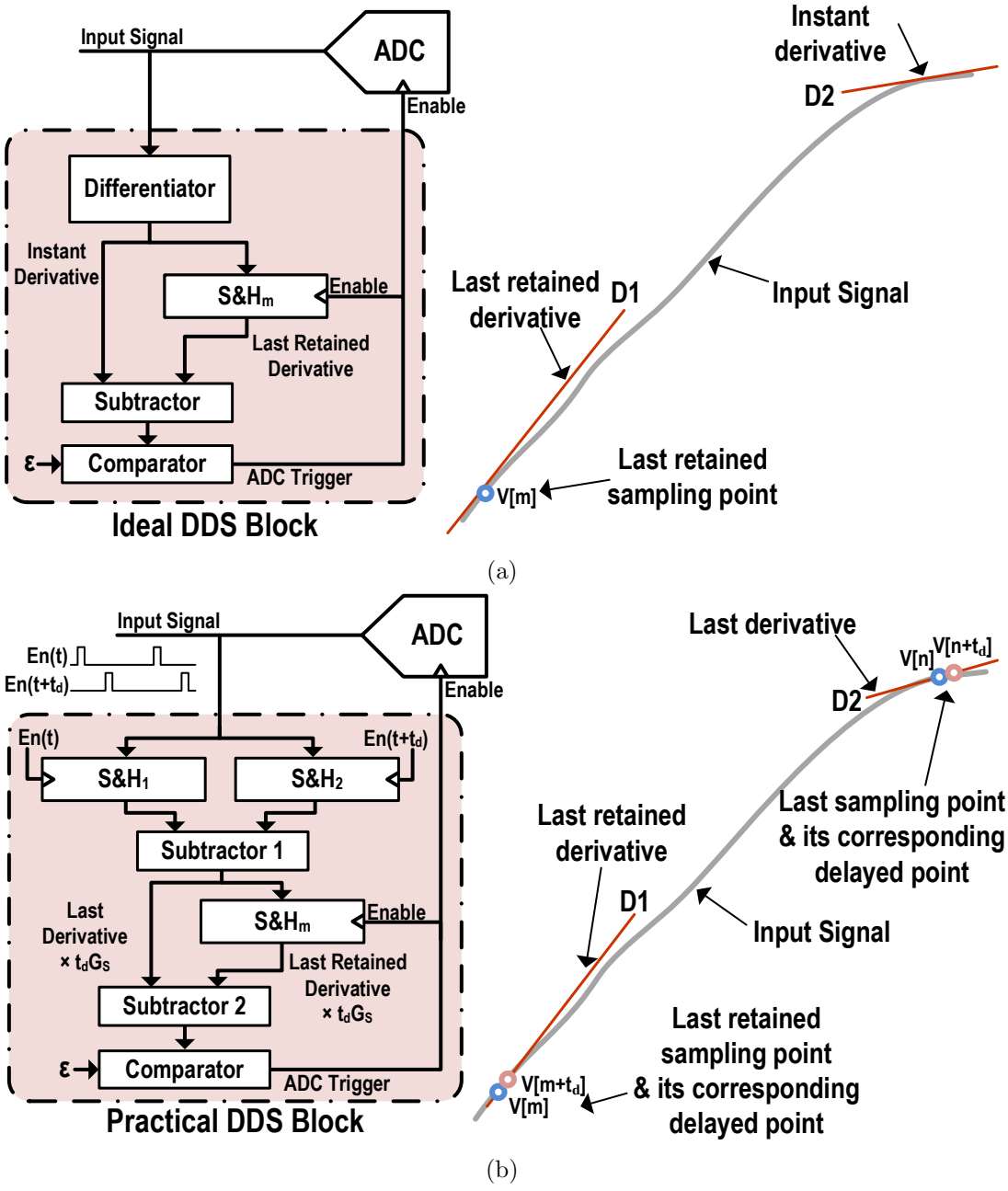


Figure 2.1: Implementation of the proposed CB-DDS scheme: (a) in a conceptual case by using a differentiator, and (b) in a practical case using sample-and-hold blocks and a subtractor.

a unity gain subtractor then produces the difference between the current derivative of the input signal and the last retained derivative. Then, this difference is compared to the threshold value of ε using a comparator. If the difference between the two derivatives is greater than ε, an ADC trigger signal is generated to enable the ADC

and the sample-and-hold circuit.

Since using an analog differentiator along with an analog comparator dissipates a considerable amount of power, we propose to implement this differentiator based on calculating the rate of the level change at two consecutive points. In the structure shown in Figure 2.1(b), the input is sampled by two sample-and-hold circuits (S&H_1 and S&H_2) which are enabled by non-overlapped enable signals, En(t) and En($t+t_d$) where t_d is a predefined constant delay time. The frequency of the enabling signals is the same as the ADC's main clock frequency if the ADC is working with uniform sampling. Then, a subtractor provides the difference between the outputs of S&H_1 and S&H_2, which is related to the derivative of the signal assuming that t_d is small enough with respect to the signal changes. Considering the sample-and-hold circuit S&H_m stores the output of the first subtractor at the last retained sampling point, $V[m]$, then the mathematical expression for the structure, shown in Figure 2.1(b), can be written as

$$G_{S1}G_{S2}\,|(V[n+t_d]-V[n])-(V[m+t_d]-V[m])| \geq \varepsilon, \tag{2.1}$$

where G_{S1} and G_{S2} are the subtractors' voltage gain, $V[n]$ and $V[n+t_d]$ are the last sampling point and its corresponding delayed point, respectively, and $V[m]$ and $V[m+t_d]$ are the last retained sampling point and its corresponding delayed point, respectively. Dividing both sides of equation by t_d, we have

$$\left|\frac{V\,[n+t_d]-V\,[n]}{t_d}-\frac{V\,[m+t_d]-V\,[m]}{t_d}\right| \geq \frac{\varepsilon}{G_{S1}G_{S2}t_d}. \tag{2.2}$$

The left-hand side of the above equation represents the difference between the current derivative and the last retained derivative of the signal, or $|D_2-D_1|$. If the condition in Equation (2.2) is satisfied, then this will be considered a significant event and the system generates an enable signal triggering ADC to convert the last sampling point.

Applying the proposed CB-DDS to a sawtooth wave signal, as an example, the method only selects the sampling points on the edges of the signal as the change in

the derivative is high at these points. Since the reconstructed signal is generated by the simplest interpolation of the retained points, a large CF with high accuracy can be obtained for this type of signal. This is because two sampling points are sufficient in the CB-DDS method to reconstruct a ramp signal rather than several points that are needed with the CB-LC method since a ramp signal crosses several reference levels. In the next subsection, the proposed CB-DDS technique is applied to other types of signals to more thoroughly evaluate its performance compared to prior NUS methods.

2.0.2 Comparison with Other NUS Methods

Figure 2.2 summarizes the process of detecting significant points in the proposed CB-DDS, CB-SDS, and CB-LC techniques by applying them to the same input signal. In the proposed CB-DDS technique, the system tracks the derivative of the input signal to find a significant change in it, while in the CB-SDS, the system subtracts the slope between the last two sampled points from the slope between the last retained and next to the last sampled points. Three sampling points, three mathematical subtractions, and an analog division are needed to calculate the above slopes [14]. This makes the implementation more complex with respect to the CB-DDS and CB-LC methods as several analog building blocks are required to achieve the CB-SDS system. In contrast, the CB-LC scheme can be implemented with minimum complexity, where the system compares the signal level to the fixed or adaptive reference levels to detect a change in the voltage level status. In this example with the specified setup, the CB-DDS, CB-SDS, and CB-LC systems retain 5, 3 and 9 points, respectively.

To compare the proposed CB-DDS technique with the CB-SDS and CB-LC techniques, their accuracy performance is evaluated with a sinusoid and a real-world ECG input signal while keeping a similar CF for all schemes for a fair comparison. The accuracy of the reconstruction can be evaluated using either the Root Mean Square Deviation (RMSD) or Post-Reconstruction Signal-to-Noise Distortion Ratio

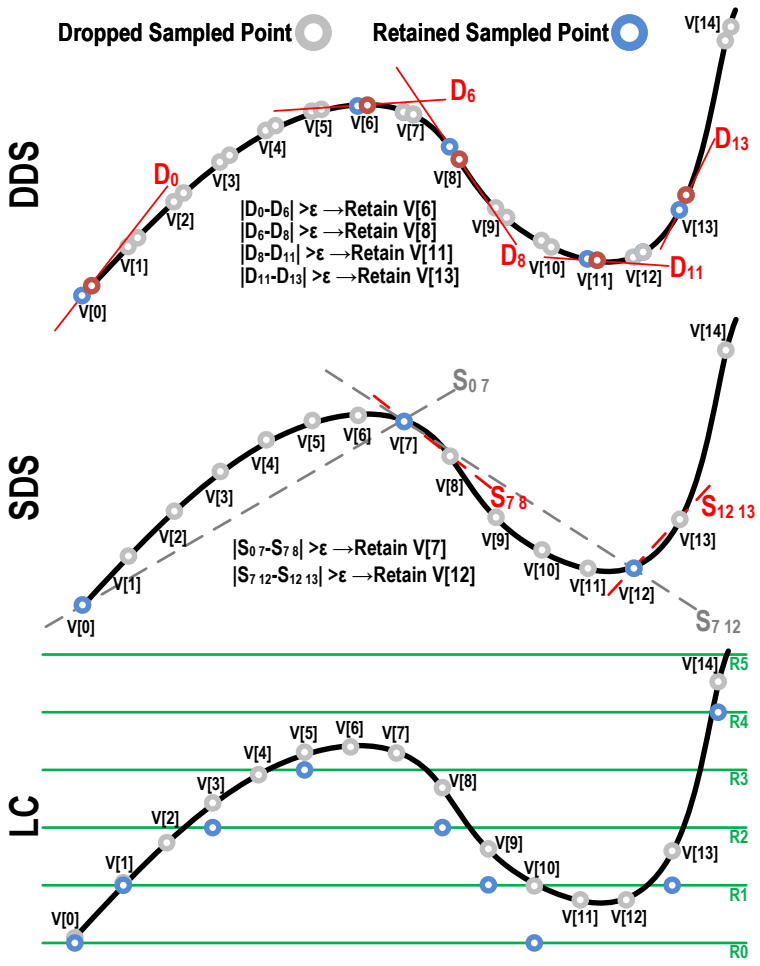


Figure 2.2: Detection of significant events in the CB-DDS, CB-SDS and CB-LC schemes.

(PR-SNDR) defined as follows

$$\begin{aligned} \text{RMSD} &= \sqrt{\frac{\sum_{N}^{i=1} x_e^2}{N}}, \text{ and} \\ \text{PR-SNDR} &= 10 \log \frac{Power\left(x_i - mean\left(x_i\right)\right)}{Power\left(x_e\right)}, \end{aligned} \tag{2.3}$$

where x_i and x_e are input and error values, respectively. Note that a larger PR-SNDR or RMSD indicates a greater accuracy in reconstruction and a larger CF indicates a greater saving in overall power consumption by the overall data acquisition system. Figure 2.3 shows the reconstructed and error signals of the three NUS techniques along with their RMSD and CF for the two input signals. For a sinusoidal signal, the RMSD is found to be 0.008, 0.007, and 0.046 for the proposed CB-DDS, CB-SDS, and

CB-LC techniques, respectively. The reconstructed signals for the proposed CB-DDS and the CB-SDS schemes are generated by connecting the retained sampled points using first-order linear interpolation. For the CB-LC method, a zero-order hold, in which the reconstruction level remains constant until the signal passes another level, is utilized as it produces a higher PR-SNDR than the first-order linear interpolation. No post-processing reconstruction method has been applied to the reconstructed signals for all three methods to ensure a fair comparison. The retained sampling points in the rising and falling parts of the sinusoidal signal in the CB-DDS and CB-SDS techniques are asymmetric. This is mostly due to the fact that the detection process is clock-based and depends on the initial phase/sampled points. In the CB-DDS scheme, for example, the derivative of the next points is compared to the first retained sampling point. Therefore, changing the first retained point changes the set of the next retained sampling points and, consequently, the CF and PR-SNDR might slightly change.

For the ECG signal, the RMSD is found to be 0.0058, 0.0054, and 0.0095 for the proposed CB-DDS, CB-SDS, and CB-LC techniques, respectively. In both scenarios, the performance of the CB-LC technique is found to be worse than the other two NUS techniques despite having a lower CF. Increasing the number of reference levels in the CB-LC method can decrease the error but at the cost of decreasing the CF. The proposed CB-DDS method is able to achieve a similar performance compared to the CB-SDS method while keeping the same CF; however, the proposed CB-DDS detection process is significantly simpler than the CB-SDS technique. This saves power while being less sensitive to non-idealities and design variations. Note that in the above, the input signal is assumed to be isolated from the NUS systems; however, potential degradation in SNR is expected in the CB-SDS and CB-LC techniques as signal integrity is degraded during the detection process by these schemes.

Figures 2.4(a) to 2.4(c) show the Power Spectral Density (PSD) of the reconstructed ECG signals plotted in Figures 2.3(d) to 2.3(f) for the proposed CB-DDS, CB-SDS, CB-LC and uniform sampling schemes. There is no significant difference in

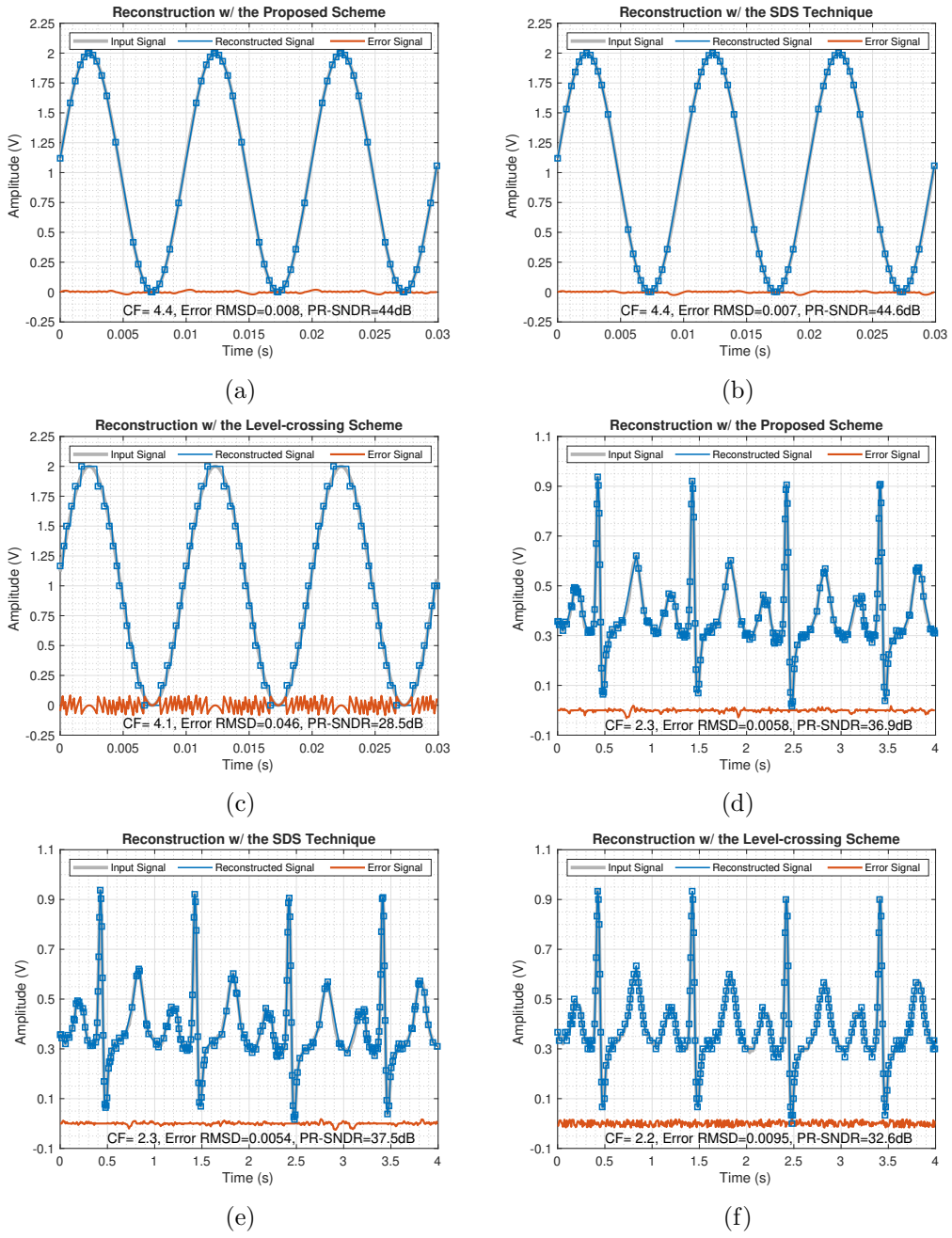


Figure 2.3: A comparison between NUS methods by applying (a) the proposed CB-DDS, (b) CB-SDS and (c) CB-LC techniques on a 100-Hz sinusoidal signal, and by applying (d) proposed CB-DDS, (e) CB-SDS and (f) CB-LC techniques on a real ECG signal.

the PSD of all methods at frequencies below 20 Hz. The PSD of the reconstructed signal by the CB-LC method shows a greater deviation from the uniform sampling at higher frequencies while the PSD of the proposed CB-DDS and CB-SDS schemes

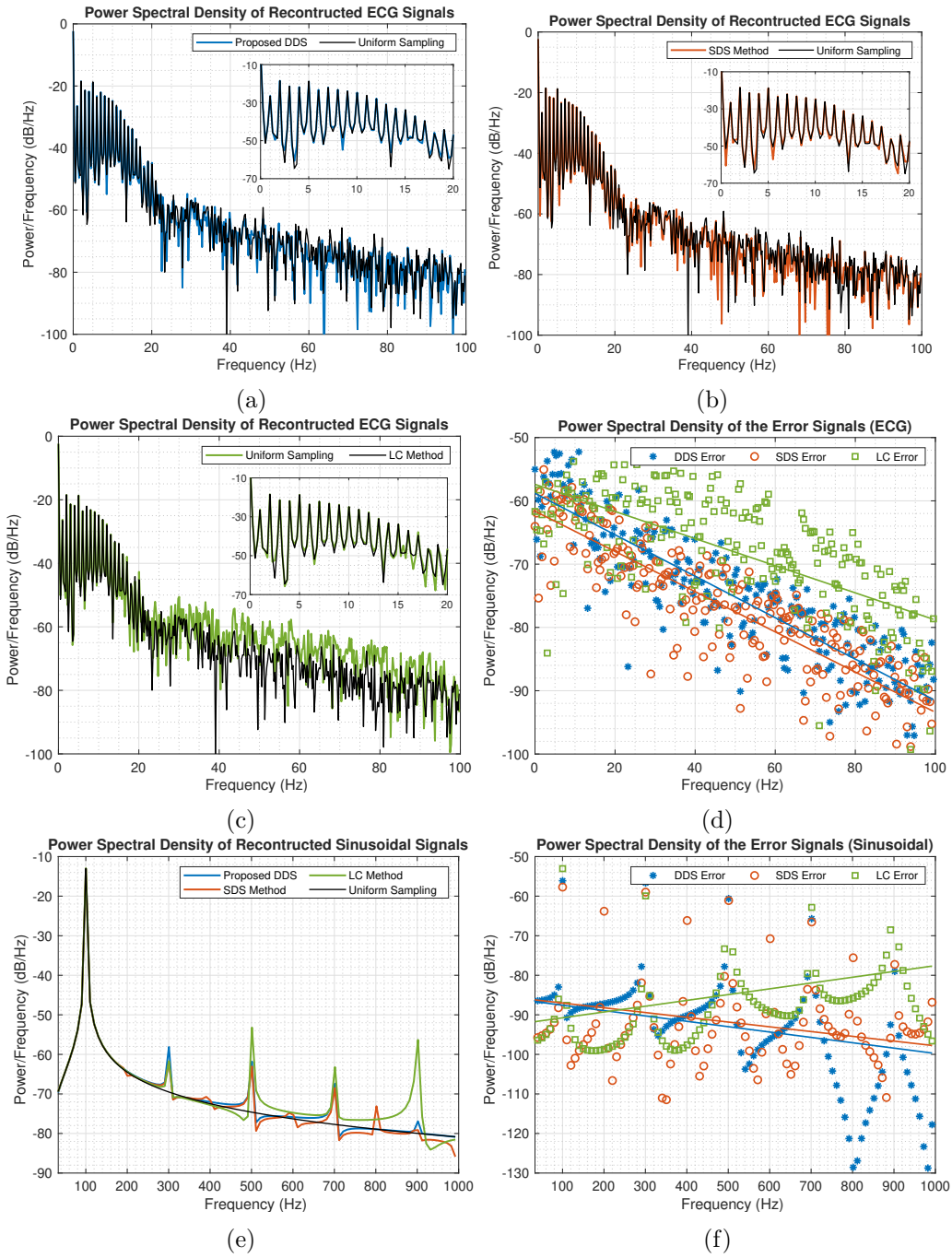


Figure 2.4: PSD of the reconstructed ECG signals in Figure 2.3(d)-(f) using (a) the proposed CB-DDS, (b) the CB-SDS and (c) the CB-LC methods along with uniform sampling method, (d) PSD of error signals after reconstruction of ECG signals, (e) PSD of the reconstructed sinusoidal signals in Figure 2.3(a)-(c) using the proposed CB-DDS, the CB-SDS, and the CB-LC methods along with the uniform sampling method and (f) PSD of error signals after reconstruction of sinusoidal signals.

follow the PSD of the uniform sampling. The PSD of the error signals along with their linear regression is shown in Figure 2.4(d). Although the PSD of the error signal generated in the CB-LC system has smaller values at frequencies close to DC (smaller frequency content), it shows larger errors at higher frequencies. The PSD of the error signals of the proposed CB-DDS and CB-SDS are in the same range while the CB-SDS scheme shows marginally smaller frequency components. Figures 2.4(e) and 2.4(f) also show the PSD of the reconstructed sinusoidal signals and corresponding error signals plotted in Figures 2.3(a) to 2.3(c) for the proposed CB-DDS, CB-SDS, CB-LC and uniform sampling schemes, where a similar observation can be made. As expected, the PSD of reconstructed signals in all methods peaks at 100 Hz, the fundamental frequency of the single-tone sinusoidal signal, and there is no significant difference in the PSD of all methods at frequencies below 200 Hz. At frequencies higher than 200 Hz, the PSD of the reconstructed signal from the CB-LC method shows greater deviation from the PSD of uniform sampling, especially at the harmonics of the fundamental frequency, and this is confirmed by the PSD of the corresponding error signal. The PSD of the reconstructed sinusoidal and corresponding error signals in CB-SDS and CB-DDS methods show similar behavior within the spectrum with only slight differences. The RMSD values shown in Figures 2.3(a) to 2.3(c) and the linear regressions depicted in Figure 2.4(f) also confirm these observations.

It should be noted that several modifications to the Level Crossing (LC) scheme, mostly clockless ones, have been also proposed. For example, the adaptive LC scheme introduced in [35] and [38] aims to adjust the comparator thresholds (window) to have a greater quantization step in the fast-moving parts of the signal so that the scheme samples the signal less frequently in these parts. Additional blocks for analog signal preprocessing and a feedback control loop are needed to implement the adaptive LC technique, which increases the structural complexity and power consumption of the NUS block compared to the conventional LC. The derivative LC proposed in [39] also applies LC sampling on the derivative of the signal (rather than the signal

itself) at the transmitter side, then sends the sampled data to the receiver side as the zero-order-hold data, and ultimately applies an integration at the receiver side to represent a first-order reconstruction of the input. As an advantage, the error and the power consumption of the reconstruction process on the receiver side are expected to be reduced if there is a limited power budget on the receiver side. However, the static power consumption of the required clockless analog differentiators and integrators makes the design of the NUS block less energy-efficient and more complex in comparison to that of the conventional LC. The CB-DDS scheme proposed in this work tracks the changes in the derivative of the signal by comparing the current derivative with the previously stored derivative. This scheme further reduces the sampling rate if the slope of the signal is not significantly changed, resulting in higher CF and lower system power consumption compared to the LC method and its variants. Moreover, it implements the derivative function utilizing sampled-and-hold circuits without any static power consumption rather than that caused by the transistors' leakage. The CB-DDS block can be also implemented separately from the ADC, triggering it at significant events while not degrading the SNR.

Although all the above NUS techniques are signal-dependent, we can discuss scenarios in which the maximum error occurs in these methods, as illustrated in Figure 2.5. For the CB-DDS case, the input signal shown in Figure 2.5(a) is analyzed. Here, the last retained derivative, D_0, is calculated at $V[0]$. The input signal direction changes as it is sampled at $V[1]$ to $V[5]$, however, the difference between the derivative calculated at these points, D_1 to D_5, may come close but does not exceed the threshold value. As a result, these sampled points are dropped. It is only until the sample point $V[6]$ arrives that the difference in its derivative, D_6 compared to the last retained derivative, D_0, exceeds the threshold value and the system retains the sampling point $V[6]$. The reconstructed signal from the retained sample points is shown in blue and Err_{max} denotes the maximum error observed. In the worst-case scenario, we can assume that $V[0]$ and $V[6]$ are equal to the lowest and highest

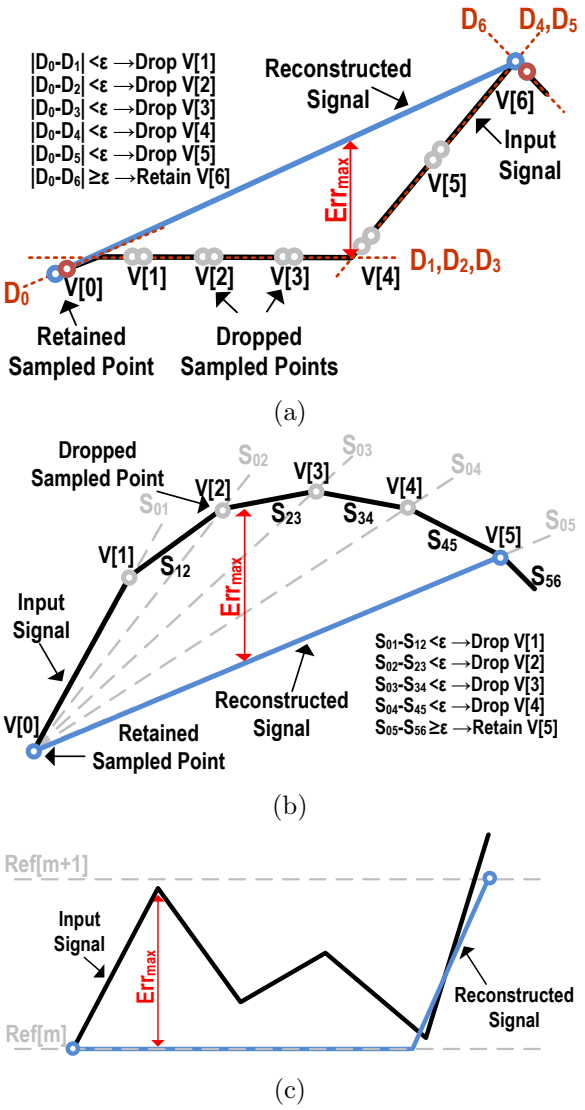


Figure 2.5: An example of the worst-case scenario of the error in (a) the proposed CB-DDS, (b) CB-SDS [14], and (c) CB-LC techniques.

possible voltage levels, *e.g.* 0 and VDD, and $D_0 \approx \varepsilon$ and $D_4 \approx 2\varepsilon$. Therefore, the maximum error occurs at $V[4]$ in this scenario. Assuming that p and q are the number of silent clock cycles (cycles without significant events) in the flat direction and in the rising direction, respectively, the maximum error can be calculated as

$$\frac{Err_{max}}{\text{VDD}} \approx \frac{p \times T}{(p+q) \times T} \quad \text{or} \quad Err_{max} \approx \frac{p}{p+q}\text{VDD}, \tag{2.4}$$

where T is the clock period. Accordingly, the maximum error approaches VDD by increasing p while keeping q constant.

Similarly, a maximum error of VDD can occur using the CB-SDS technique. The worst-case scenario in this technique is discussed in [14] and presented in Figure 2.5(b). The signal direction deviates for each clock cycle in such a way that the slope between the last retained point and the second last sampling point, or $S_{0\,i-1}$, is not significantly greater than the slope between the last two sampling points, or $S_{i-1\,i}$. Thus,

$$|S_{0\,i-1} - S_{i-1\,i}| < \varepsilon \quad \text{for} \quad i = 2, 3, 4, 5 \tag{2.5}$$

Consequently, the scheme drops the sampling points $V[1]$ to $V[4]$ in the silent clock cycles. Assuming that at the fifth sampling point, we have

$$|S_{05} - S_{56}| \geq \varepsilon, \tag{2.6}$$

the system retains the sampling point $V[5]$. Similar to the CB-DDS technique, as the number of silent clock cycles increases, the maximum error shown in Figure 2.5(b) will approach VDD.

In contrast to the CB-DDS and CB-SDS techniques, the maximum error is equal to the quantization step in the CB-LC method, as shown in Figure 2.5(b). This can be reduced by increasing the number of reference levels and the threshold, but this will reduce the CF. While the maximum error is less than the other methods, the overall error power or RMSD will be greater for this method in real-world signal cases as presented in Figure 2.3.

The worst-case scenario described for CB-DDS is very unlikely to occur with a real-world signal, in contrast to the worst-case scenario for the CB-SDS method where the shape of the signal resembles a Photoplethysmography (PPG) or a low-frequency sinusoidal signal. Furthermore, since the polarity of the derivative changes with a change in the direction of the signal, any peaks presented in the input signal are retained through reconstruction in the CB-DDS method, unlike in the CB-SDS and CB-LC methods. There are some solutions to limit this error. One solution would be to reduce the threshold value. Another solution would be to set a limit on the

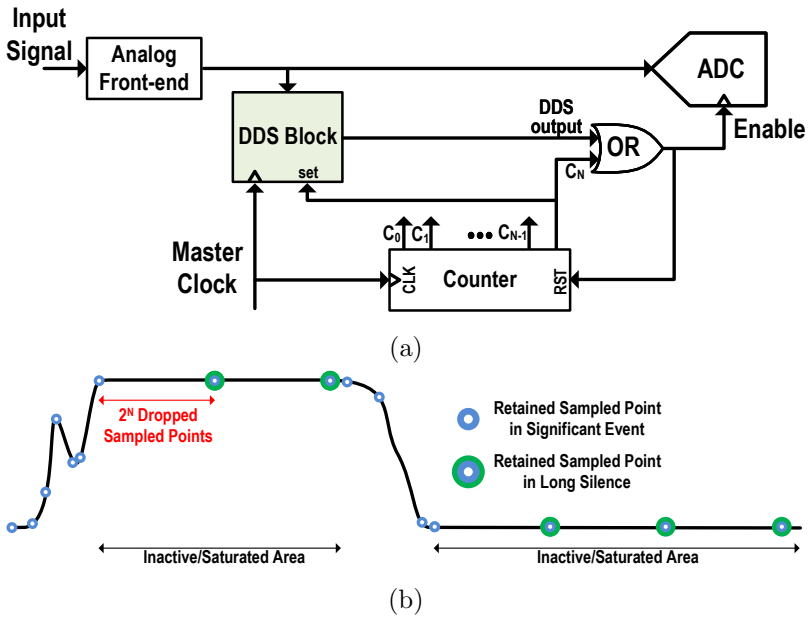


Figure 2.6: (a) Limiting the number of silent/dropped clock cycles by using a counter in parallel to the CB-DDS block to set 2^N as the limit number, and (b) applying to an example scenario of a saturated signal.

number of silent clock cycles, as suggested in [14], which can be simply implemented with a parallel low-power counter and an OR gate (shown in Figure 2.6(a)). When the number of silent/dropped clock cycles reaches a determined limit, 2^N in this example, the ADC is enabled and the system retains the sampling point, whether there is a significant event or not. This technique is especially helpful when no significant event occurs for a long period of time, and prevents error due to the long hold time of the sample-and-hold circuits. An example of this scenario may be a saturated signal (shown in Figure 2.6(b)), possibly due to a large analog front-end gain. In the inactive/saturated part of this input signal example, the system is adjusted to work at the least sampling rate defined by a controllable counter. Although this might be a concern in some applications, in most of the real-world signal cases that we considered, the number of silent/dropped sampling points did not reach the limit, especially when N and the master clock frequency are selected properly.

To summarize the above discussion, the accuracy, complexity, number of building blocks and power consumption of the above NUS schemes are mostly dependent on the

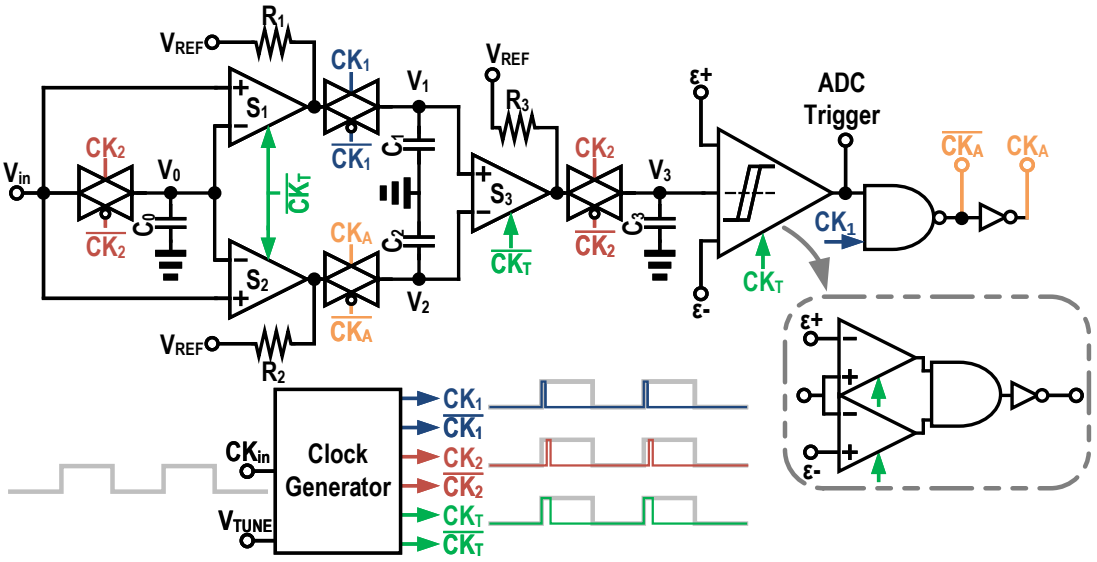
complexity of the corresponding equation implemented at the circuit level to detect the significant events. Therefore, among the CB-LC, CB-SDS and CB-DDS schemes, the CB-LC method is expected to have the least complexity and power consumption but possibly the worst accuracy (especially with respect to higher frequency content), while the CB-SDS has the most complexity and power consumption with possibly the best accuracy. The proposed CB-DDS presents a comparable accuracy to the CB-SDS while the complexity and power consumption are considerably less. Note that there is no significant difference in the response time (decision delay) between the CB-DDS, CB-SDS, and CB-LC techniques since that time is mostly dependent on the master clock frequency. The response time of a clockless CB-LC system, on the other hand, is mainly dependent on the supported bandwidth of the system and it scales directly with its power consumption. As the main parts of the CB-DDS, CB-SDS, and CB-LC systems that are responsible for the detection of significant events are clocked by a predetermined or fixed master clock, their power consumption does not vary based on the signal activities. However, the power consumption of the other part of the system, which is activated only when significant events are detected to produce the output trigger signals, scales with the input signal activities, but it only accounts for a very small percentage of the total power consumption. Therefore, the total power consumption of these NUS systems does not vary noticeably depending on signal activity.

2.1 Implementation of the Proposed Scheme

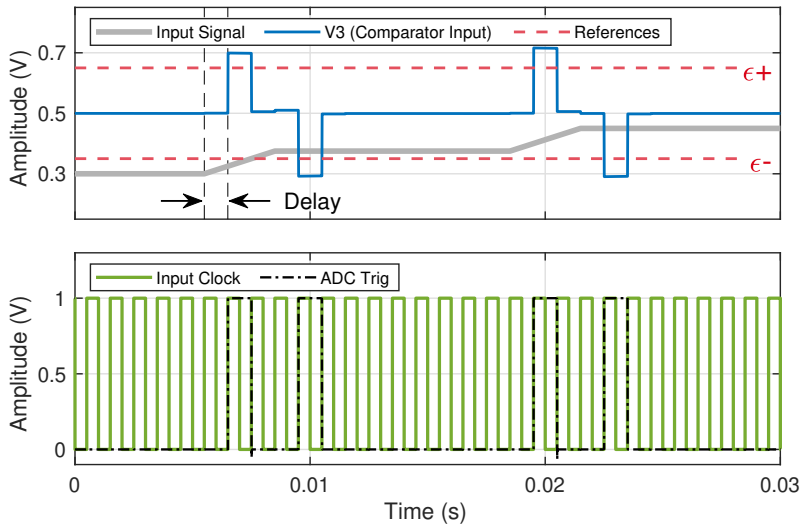
As described in Section 2.0.1, if the time delay between the two sampled points is constant and small enough, the derivative of the signal can be approximately calculated by dividing the change in the signal level over a short time delay. Therefore, the circuit implementation does not require the actual derivative to be computed and a combination of sample-and-hold circuits and subtractors can be used to find and compare the input signal's last derivative and retained derivative. Figure 2.7(a) il-

lustrates the proposed circuit implementation of the CB-DDS system. The structure incorporates a clock manager that generates six clock signals from an input master clock, CK_{in}, with a frequency of f_s. It generates CK_1 at the rising edge of the master clock in addition to CK_2, which is a delayed non-overlapping version of CK_1. A third clock signal, CK_T, is generated for the subtractor and window comparator amplifiers, which is equal to the union of CK_1 and CK_2, with a rising edge before the rising edge of CK_1 and a falling edge after the falling edge of CK_2. The clock signal CK_T ensures that the amplifiers are turned on only when the system should be active. A controller voltage, V_{TUNE}, is used to tune the pulse width of CK_1 and CK_2. It is typically set to the smallest practical value that can guarantee proper sampling (proper settling time) with minimal power overhead. The low-duty cycle of the generated clock signals improves the overall power efficiency of the system.

The input signal is sampled at the first stage, V_0, using a sample-and-hold circuit driven by CK_2. The following subtractors, S_1 and S_2, take and amplify the difference between the input signal and V_0 to find the approximate derivative of the input signal. The outputs of the subtractors are passed to two sample-and-hold circuits, one is driven by CK_1 and the other is driven by CK_A produced by ANDing the CK_1 with the system output, the ADC trigger. Therefore, V_1 is updated with the last approximated derivative at every rising edge of CK_1, and at node V_2, the last retained approximated derivative is kept until the next significant event occurs. Similarly, subtractor S_3 takes and amplifies the difference between the last derivative and the retained derivative of the input, and passes it to V_3 on the rising edge of CK_2. At the final stage, a window comparator circuit compares V_3 with a threshold value ε. The output of the comparator, the ADC trigger, is high when V_3 is greater than $\varepsilon+$ or less than $\varepsilon-$. Note that node V_3 is DC-biased at V_{REF}, therefore we have $\varepsilon+ = V_{REF} + \varepsilon$ and $\varepsilon- = V_{REF} - \varepsilon$ where ε is the threshold value. The output of the comparator goes low at the rising edge of the next cycle when the feedback CK_A enables the second sample-and-hold circuit, thus V_1 equals V_2, and then V_3 will be approximately equal



(a)



(b)

Figure 2.7: (a) Implementation of proposed CB-DDS system at the circuit level, and (b) System response to an arbitrary input signal.

to V_{REF}. Although the performance of the structure depends on the signal type, the CF can be controlled by adjusting the threshold values.

Figure 2.7(b) shows the comparator input (V_3) in response to an arbitrary input signal. As depicted, the ADC trigger is changed from low to high when V_3 reaches the $\varepsilon+$ or $\varepsilon-$ thresholds. The decision delay, a clock cycle delay for the detection of significant events, is also shown in this figure. In this example, significant events

occur at the edges of the input signal, thus the ADC trigger output goes high in response after one clock cycle. Note that the ADC trigger signal can be ANDed with the master clock or its inverted version, if needed, to be applied to the system ADC.

Some important design considerations for the implementation are as follows:

(a) Using two independent subtractors at the first stage, instead of a single shared subtractor, helps to avoid the undesired charge sharing between C_1 and C_2. This reduces the likelihood of false alarms in the detection process.

(b) A larger transmission gate size provides a smaller on-resistance, which is desirable for reducing the settling time, but it also increases the parasitic capacitance, which could be a problem for proper sampling in addition to the increasing power of the clock manager. The size of these transistors must be optimized considering this trade-off.

(c) The capacitors in the sample-and-hold circuits should be properly sized; an overly small capacitor results in a significant offset due to charge sharing or leakage, while an overly large capacitor increases the settling time or dissipates more power.

(d) A significant event can be defined by setting the threshold value (ε), subtractor voltage gain (G_S) and time difference (t_d), as shown in Equation (3.1). The t_d is fixed to reduce complexity, but the voltage gain of the subtractors can be controlled by tuning the large resistors, R_1 to R_3, at the output of amplifiers. Note that the V_{REF} is ac grounded by large off-chip capacitors.

(e) $\varepsilon+$ and $\varepsilon-$ can be unbalanced when there is an offset in V_{REF} or in cases where we prefer to have a different threshold value for ascending and descending parts of the input.

(f) If we apply CK_1 to the first sampling circuit and CK_2 to the next sampling stage after the subtractor, then the small delay between CK_1 and CK_2, *i.e.* small t_d in Equation (2.2), necessitates a higher voltage gain in the subtractor stage. This will increase the sensitivity of the significant event detection with respect to noise. Moreover, V_3 would be generated before V_1 and V_2 settle if there is no delay for

the second subtraction stage. To avoid these difficulties, CK_2 is applied to the first sampling circuit transmission gate and CK_1 is applied to the output of the subtractor. This delays the decision by a clock cycle as mentioned above, but this delay can be compensated if the input signal is delivered to the ADC with the same delay or ignored for a low-frequency signal.

The transistor-level design of the main building blocks of the systems is discussed in the following subsections:

2.1.1 Subtractor

Three subtractors have been used in the first and second stages of the CB-DDS system where they take and amplify the difference between their inputs. It is expected that the difference between their inputs is small, therefore, the subtractor requires an accurate, high-voltage gain amplifier with high input common-mode range and high common-mode rejection ratio (CMRR). To meet all the above criteria, we have chosen the circuit topology shown in Figure 2.8(a). The circuit consumes around 1.44 μA in regular operation from a supply voltage of 1 V. Its voltage gain can be expressed as

$$V_{OUT} = \frac{g_{m_{P1,P2}}}{g_{ds_{P3}} + g_{ds_{N3}} + \frac{1}{R_{out}}} \times \left(V^+ - V^-\right), \tag{2.7}$$

where $g_{m_{P1,P2}}$ is the transconductance of the transistors M_{P1} and M_{P2}, and $g_{ds_{N3}}$ and $g_{ds_{P3}}$ are the drain to source conductance of M_{N3} and M_{P3}, respectively. The R_{out} is the variable resistor placed at the output which is the R_1 to R_3 resistors in Figure 2.7(a).

To build a power-efficient system, an enable signal, connected to CK_T, is applied to M_{EN1} to M_{EN3} to turn them on only when necessary. These transistor widths should satisfy the trade-off between low on-resistance and low parasitic capacitance. The former is to avoid significant drop-off from the voltage supply and the latter is to avoid the long charging time of parasitic capacitors to make the circuit ready for operation. As discussed earlier, the rising edge of CK_T as the enable signal should

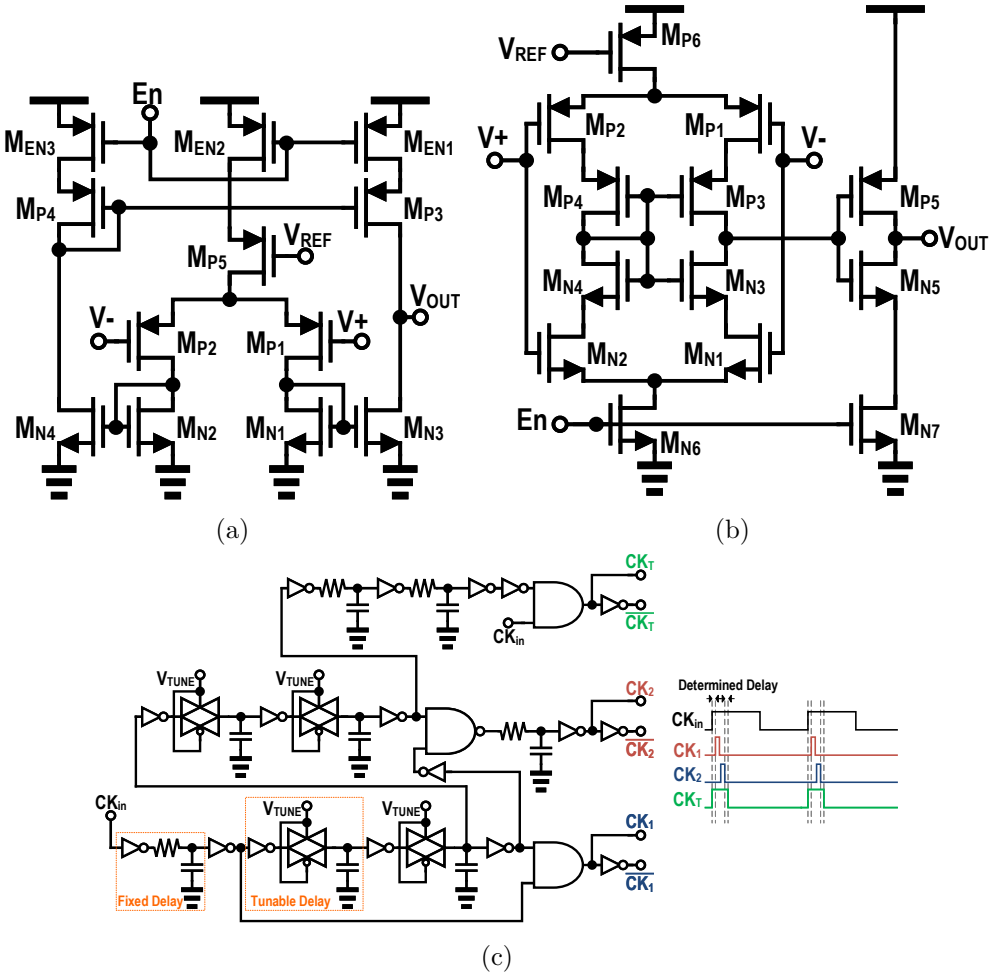


Figure 2.8: Circuit implementation of (a) the subtractor, (b) the proposed current reuse comparator, and (c) the proposed clock generator.

arrive before the rising edge of CK_1, and also CK_2. This is to establish the amount of parasitic capacitance and prepare the amplifiers for subtraction. The greater the width of M_{EN1} to M_{EN3}, the smaller the on-resistance and the larger the parasitic capacitance, therefore, the larger the time difference between CK_T and CK_1. In this design, the on-resistance of M_{EN1}-M_{EN3} is set around 100 Ω.

2.1.2 Comparator

Figure 2.8(b) shows the circuit implementation of the amplifiers used in the comparator design. The proposed current reuse structure is used for the first stage to save power ($I_{total,comp} \approx 306$ nA) and to obtain a high voltage gain (≈ 36 dB). An

NMOS differential pair, $MN_{1,2}$, and a PMOS differential pair, $MP_{1,2}$, are used in the first stage to build the current reuse structure. The cascade transistors, $MN_{3,4}$ and $MP_{3,4}$, provide greater output resistance; therefore, a higher gain is used for the first stage. The input range decreases when using multiple stacked transistors, however, this effect is negligible as the reference levels, $\varepsilon+$, and $\varepsilon-$, are normally chosen to be close to half of the voltage supply. This is fed to a buffer inverter to further improve the gain. The output transistors of both stages (MN_{3-5} and MP_{3-5}) are sized to reduce the parasitic capacitance, which reduces the power consumption and makes the comparator faster. The parasitic capacitance of the input is negligible since the comparator input is connected to either a constant voltage ($\varepsilon+$ or $\varepsilon-$) or the sample and hold capacitor (C_3).

The threshold values of $\varepsilon+$ or $\varepsilon-$ can be set to be fixed or can be adaptively adjusted through a feedback-controlled loop. In the adaptive CB-LC proposed in [35, 38], for example, a self-calibration circuit adjusts the reference levels to have larger quantization steps for fast-moving parts of the signal and finer quantization steps during segments of low activity. This may be at the cost of an additional analog signal preprocessing implemented by several analog building blocks which may add complexity and power consumption. A similar strategy can be applied to the CB-DDS system to achieve an adaptive threshold value based on signal characteristics, e.g., reducing ε for an ECG signal with a smaller amplitude. A calibration procedure through DSP or other possible analog implementation can be also utilized for achieving a targeted CF, and correspondingly, a targeted accuracy. A simple analog calibration, for example, is to calculate the CF in a certain period (e.g., 2^M clock cycles) using a simple counter that counts the number of ADC triggers, and accordingly, adjusts the resolution threshold, ε.

2.1.3 Clock Generator

The implementation of the proposed clock manager and its generated time signals are shown in Figure 2.8(c). Two types of delay circuit is utilized in the structure as follows:

(a) A fixed delay is achieved by a simple on-chip R-C circuit followed by an inverter. This delay box is mainly used to provide a predetermined delay between CK_T and CK_1, as well as CK_2 and CK_T. It is also used at the last stage of CK_2 generation to guarantee that CK_1 and CK_2 do not overlap.

(b) A tunable delay is produced by a transmission gate driving an on-chip capacitor. As the on-resistance of the transmission gate switch can be controlled by the gate voltage, V_{TUNE}, the RC delay of the gate can be varied accordingly. This delay is used to provide the tunable pulse width of CK_1 and CK_2, and it is duplicated to provide the width required for the charging time of the sampled-and-hold capacitors.

As shown in Figure 2.8(c), the master clock is ANDed with its delayed version to generate CK_1. The same blocks are successively used for CK_2, except for an additional fixed delay at the final stage producing non-overlapping CK_1 and CK_2. Moreover, ANDing the master clock and its delayed version after multiple delay blocks generates CK_T with a pulse width equal to the sum of pulse widths of CK_1 and CK_2.

As discussed above, the pulse width of CK_1 (and CK_2) is frequency-independent and is tuned to the smallest possible value that provides proper settling time for all building blocks of the system. However, the smallest possible pulse width may change based on the type of signal and due to process variations, it may need to be calibrated. In the proposed clock generator, shown in Figure 2.8(c), the delay blocks can be controlled by V_{TUNE} that adjusts the on-resistance of the switches to change the pulse width of CK_1, and CK_2. Figure 2.9 shows the change in pulse width and power of the clock generator with V_{TUNE} with a 1-kHz master clock. An optimal range of V_{TUNE} is found to lie between 0.35 V and 0.5 V, where the clock generator

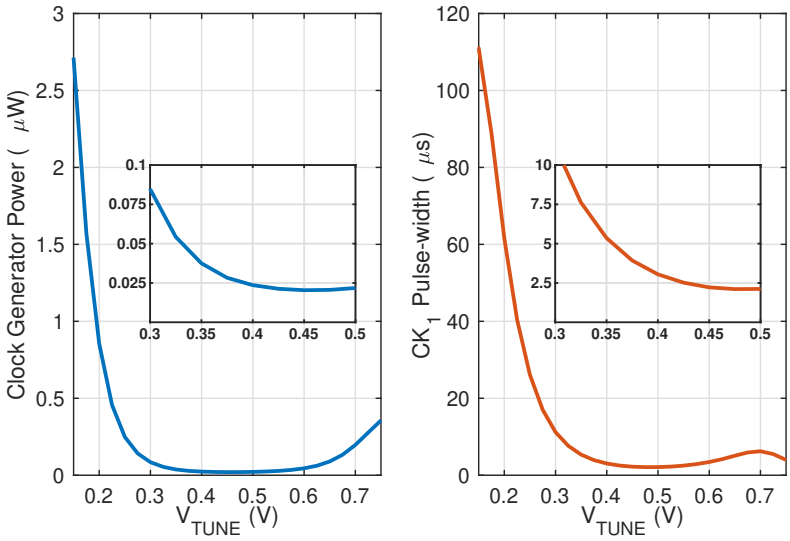
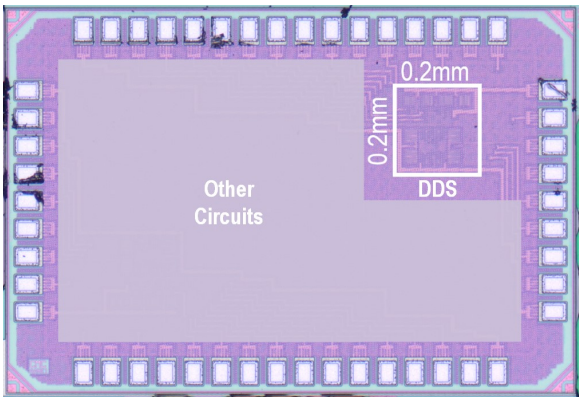


Figure 2.9: Tuning voltage V_{TUNE} versus the pulse-width of CK_1 and the overall power consumption of the clock manager.

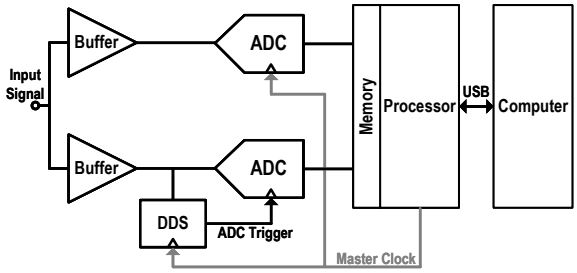
consumes less than 35 nW while providing a pulse width between 2.5 μs and 5 μs for proper operation of the system.

2.2 Experimental Results

The proposed CB-DDS system was implemented in TSMC's 130-nm CMOS technology. The fabricated circuit occupies a die area of 0.04 mm^2, as shown in Figure 2.10(a). To compare the performance of the proposed CB-DDS scheme to prior state-of-the-art schemes, the test bench shown in Figure 2.10(b) was used. The input analog signal is applied to analog buffers and their outputs are connected to two external identical 12-bit Successive Approximation Register (SAR) ADCs; one of the ADCs is operating with the uniform sampling scheme and the other is triggered by the proposed CB-DDS building block. Note that the CB-DDS technique is not dependent on the type of ADC or its characteristics (e.g., the resolution bits). The master clock generated by the micro-controller is applied to the CB-DDS system and the ADC that uses a uniform sampling scheme. As the system has been tested with various signals, the master clock frequency and the comparator references, $\varepsilon+$ and $\varepsilon-$, can



(a)



(b)

Figure 2.10: (a) Die micrograph of the CB-DDS block and (b) diagram of test bench.

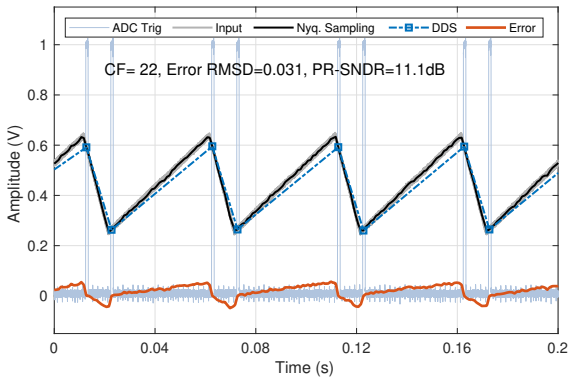
be tuned to any desired values to achieve higher CF (higher power saving) or higher PR-SNDR (higher accuracy). The master clock frequency, $\varepsilon+$ and $\varepsilon-$ are not fixed for a given input signal.

2.2.1 Test Procedure

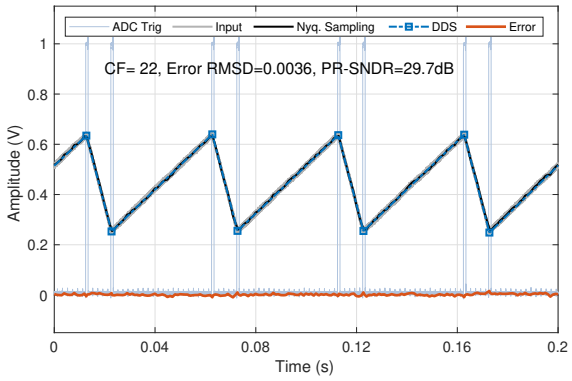
The system has been tested using various ideal and real-world signals. Figure 2.11 depicts the measured system response to ideal sawtooth and sinusoidal signals. The reconstructed signal using the uniform scheme (black), the reconstructed signal with the proposed CB-DDS scheme (blue), the output ADC trigger signal (light blue), and the error signal (red) are depicted in each case. The first-order linear interpolation used in reconstruction might be not considered for applications with a tight power budget on the receiver side, as it may need intensive computations in the process. However, the main purpose of the proposed CB-DDS system is to reduce the number of data points at the transmitter side to further reduce the overall power consumption

of the data acquisition system. Therefore, no power limit is considered on the receiver side in the experimental results. Note that no other post-processing reconstruction method has been applied to the reconstructed signals to provide a fair comparison to the other state-of-the-art schemes. As shown in Figure 2.11(a), the system generates its output, the trigger signal, one clock cycle after the edge of the sawtooth signal when the derivative of the signal changes. With an input clock of 1 kHz, the CB-DDS system achieves an 11.1 dB PR-SNDR with a compression factor of 22. The input signal to the ADC can be delayed to compensate for the error due to the decision delay. The system response in this scenario is shown in Figure 2.11(b), where using the same setup and compression factor results in a PR-SNDR of 29.7 dB. For input signals with higher frequency content, the effect of this compensation would be more noticeable. This delay for compensation can be simply implemented by a two-stage sample-and-hold circuit or a buffer delay, although they are not used in the following measurements to isolate the pre-signal processing from the ADC. Figure 2.11(c) presents the measured system response to an ideal 20-Hz sinusoidal signal, where the system achieves a PR-SNDR of 21.4 dB (CF=6.1).

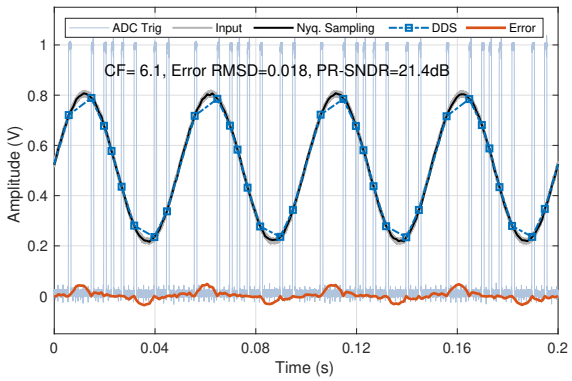
Figure 2.12 shows the response of the proposed system to various real-world biomedical signals with both high and low CFs, such as ECG, PPG and Electroencephalogram (EEG). No post-processing methods have been utilized for reconstruction. The effects of noise and sampling rate are also shown for the ECG signal. In this figure, the ADC trigger signal pulses are shown separately in a subplot below the main plot. In Figure 2.12(a) and Figure 2.12(b), an ECG signal with a heart rate of 60 bpm is applied to the system with a 1-kHz master clock. PR-SNDRs of 19.1 dB and 26.6 dB are obtained for 9.7 and 6.7 CF, respectively. The comparator window can be also narrowed to reduce the CF for a better PR-SNDR. Figure 2.12(c) shows that the system is functional at different sampling frequencies. Using a modified 250-Hz master clock, shown in Figure 2.12(c), the system achieves an 18.7 dB PR-SNDR with a 4.9 CF. Modifying the sampling frequency may change the number of stored data points



(a)



(b)



(c)

Figure 2.11: System measured responses to ideal case signals, (a) sawtooth signal, (b) sawtooth signal with compensated delay, and (c) sinusoidal signal.

(the number of times the ADC is turned on), as well as the CF. For example, in the case of Figure 2.12(c), with a 250 Hz master clock and CF of 5, the ADC turns on half as often compared to Figure 2.12(b) with a 1 kHz master clock and CF of 10.

To evaluate the effect of input noise, a non-periodic noisy ECG signal is applied

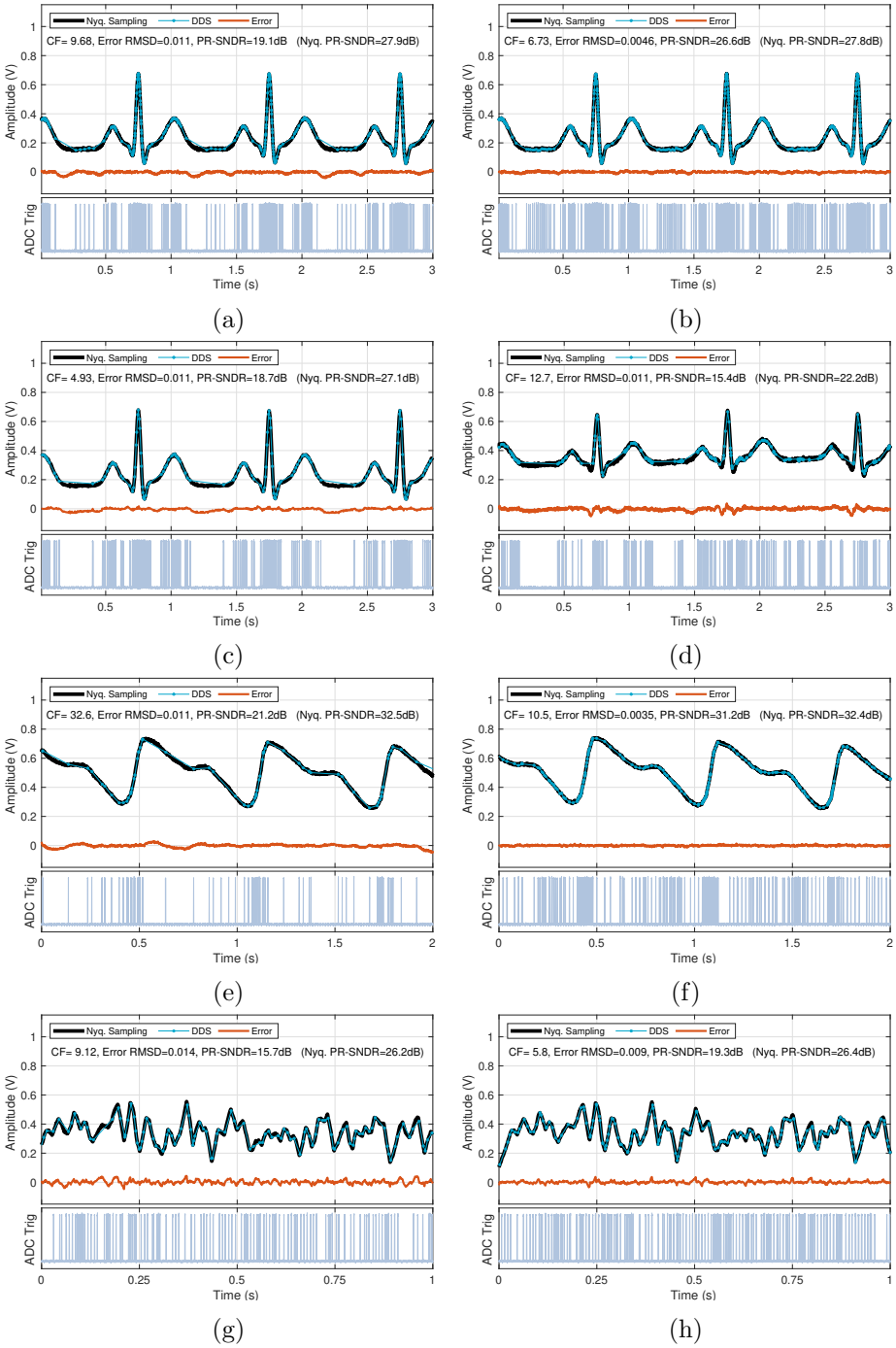


Figure 2.12: Experimental results of the CB-DDS system, (a) ECG signal with high-CF setup and a 1-kHz clock, (b) ECG signal with low-CF setup and a 1-kHz clock, (c) ECG signal with 250-Hz clock, (d) Noisy ECG signal with high CF setup and a 1-kHz clock, (e) PPG signal with high-CF setup, (f) PPG signal with low-CF setup, (g) EEG signal with high-CF setup, and (h) EEG signal with low-CF setup.

to the system in Figure 2.12(d). The noisy signal combined with a high CF of 12.7 represents a suboptimal scenario for the CB-DDS system, where a PR-SNDR around 15.4 dB is measured. As a result of the noise, the system incorrectly detects significant events in the signal, especially in the flat segments of the signal. However, the system is still able to properly detect active parts of the signal. While the effects of noise in an ECG signal are shown, it should be noted that the effects of noise are typically reduced by a filter stage in the analog front end. Various approaches such as blanking and linear interpolation [40] can be also used to deal with noise and artifact cancellation in bio-signals.

Figure 2.12(e) and Figure 2.12(f) show the results of the system in response to a PPG signal (1-kHz clock frequency) using a high and low CF, respectively. With a CF of 32.6 and 10.5, 21.2 dB and 31.2 dB PR-SNDR are measured, respectively. High CF and PR-SNDR values are obtained for a PPG signal due to its low-frequency contents combined with a low number of edges, similar to a sawtooth signal. Figure 2.12(g) and Figure 2.12(h) also show the high and low CF reconstruction of an EEG signal (1-kHz clock frequency), where PR-SNDR of 15.7 dB and 19.3 dB for CF of 9.1 and 5.8 have been measured, respectively. Due to the presence of sharp edges in an EEG signal, the decision delay has a larger effect on EEG signals compared to PPG and ECG signals.

2.2.2 PVT Variation Effects

Figure 2.13 shows Monte Carlo simulation results on the CF and PR-SNDR with 1000 random iterations to investigate the performance of the designed CB-DDS system in the presence of PVT variations. A noisy ECG signal is selected as the input signal and the resolution values are set for achieving approximately high CF (at 1-kHz master clock) since greater variations in the Monte Carlo results are expected when the number of retained sample points by the CB-DDS system is smaller. The mean values achieved for CF and PR-SNDR are 6.28 and 28.058 dB, respectively, and

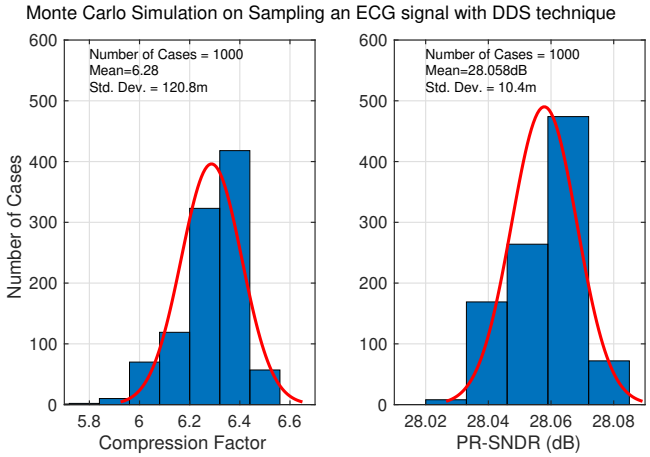


Figure 2.13: Monte Carlo simulation on CF and PR-SNDR resulted in sampling a noisy ECG signal using the proposed CB-DDS system to investigate the effects of PVT variations.

the standard deviations for normal distribution are approximately 0.12 and 0.01 dB, respectively. The achieved CF and PR-SNDR are close to the nominal values in most iterations, therefore, the designed system performance is sufficiently robust to PVT variations.

2.2.3 Power Consumption

The implemented CB-DDS system shown in Figure 2.7(a) can be divided into four principal main building blocks: (1) three subtractors, (2) two comparators, (3) a clock generator, and (4) several digital logic gates. The total power consumption of the system can be expressed as

$$P_{total} = P_{Subt} + P_{Comp} + P_{Clk} + P_{Logic}, \tag{2.8}$$

where P_{Subt}, P_{Comp}, P_{Clk} and P_{Logic} are the power dissipation in subtractors, comparators, the clock manager and digital logic gates, respectively. Note the power described in the first three terms is in direct relation to the pulse width of CK_T and the master clock frequency, $f_{CK_{in}}$. Therefore, a higher clock frequency or enabling time will result in higher power dissipation. Except for P_{Clk}, all other terms depend on the input signal type that can also affect output switching activity.

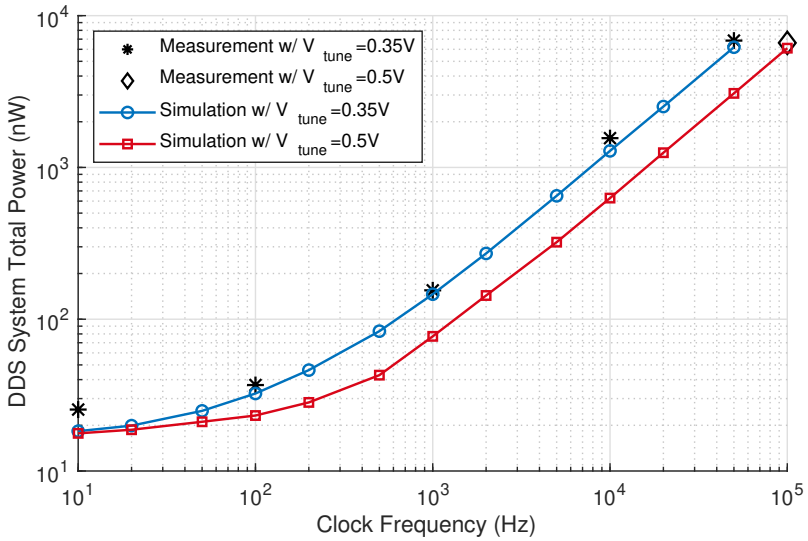


Figure 2.14: CB-DDS system power dissipation vs clock frequencies.

Figure 2.14 shows the measured and simulated power consumption of the CB-DDS system at its maximum activity (CF=1) for different input clock frequencies, $f_{CK_{in}}$. As expected, the static leakage power is dominant at clock frequencies lower than 100 Hz. As the total power varies with the pulse width of the enable signal (CK_T), we have reported the simulated power dissipation for V_{TUNE} equal to 0.35 V and 0.5 V. The measured power dissipation is with V_{TUNE} set to 0.35 V, except for when the clock frequency is at 100 kHz, where V_{TUNE} is set to 0.5 V because of the shorter period. Note that the ADC's power is not included in the graph as it varies depending on the utilized ADC.

Table 2.1 shows the power distribution of the CB-DDS system in three different scenarios in simulation. The maximum activity, where the CF is equal to 1, is considered for the first two scenarios, while in the last scenario, an ECG signal is applied to the system with a CF of around 6. Although the total power is doubled in scenario II with V_{TUNE} equal to 0.35 V because of a larger pulse width compared to Scenario I, the percentage of power consumed by the blocks does not change significantly. A comparison between Scenario II and III also shows that the CF has a negligible effect on the power dissipation of the blocks, except for the dynamic logic gates, since these

Table 2.1: Power distribution of the system with a 1-kHz master clock.

	Clock Generator (nW)	Subtractors (nW)	Comparators (nW)	Logic Gates (nW)	Total Power (nW)
Scenario I	28.1	41.5	6.7	0.8	77.2
Scenario II	54.1	79.4	11.2	1.4	146.2
Scenario III	54.1	79.2	9.1	0.7	143.2
Percentage	∼36-38%	∼52-55%	∼6-9%	∼1%	∼100%

Scenario I. Maximum output activity, V_{TUNE}=0.5V
Scenario II. Maximum output activity, V_{TUNE}=0.35V
Scenario II. ECG input signal, CF≈6, V_{TUNE}=0.35V

Table 2.2: Performance comparison with the prior state-of-the-art designs.

	This Work	**[14]**	**[41]**	**[42]**	**[43]**	**[22]**
Topology	CB-DDS+ADC	CB-SDS+ADC	CL-LC +ADC	CB-LC +ADC	CS-AFE (RMPI)	Data CS
Sampling Scheme	Nonuniform	Nonuniform	Nonuniform	Nonuniform	Uniform	Uniform
Implementation	Analog	Analog	Analog	Analog	Analog	Digital
Technique Isolation from Sampling	**Yes**	No	No	No	N/A	N/A
Input Signal Type	All	All	All	All	Bio-Signals	Bio-Signals
ADC Resolution Bits	12[a]	12[a]	6	8	10	10
CF	Widely Tunable	Widely Tunable	N/A[b]	N/A	Tunable	Fixed (2.38)
Voltage Supply (V)	1	2	0.8	1.8-2.4	0.9	1
Power Consumption	**578nW**[c] for ECG @CF≈6 (1 kHz Clock)	1.7μW[c] for ECG @CF≈6 (1 kHz Clock)	313-582 nW for 5 Hz-5 kHz Input Sinewave	0.6-1.7 μW for ECG (32 kHz Clock)	1.8 μW for ECG (2 kHz S.R.)	170 μW for ECG (256 Hz S.R.)
CMOS Technology	0.13-μm	0.18-μm	0.18-μm	0.35-μm	0.13-μm	65-nm

[a]The test bench ADC resolution bits (this varies with the selected ADC attached to the NUS block) [b]Not applicable for clockless CB-LC [c]The reported power consumption includes both the NUS block and test bench ADC (this varies with the selected ADC's power and CF)

blocks have to be on at the time of the decision. A counter may also be required to count the distance between two stored sampling points. A typical design of a counter may add around 10 nA current (1-kHz master clock) to the total current dissipation.

Table 2.2 compares the performance of the implemented CB-DDS technique with recent state-of-the-art uniform and non-uniform sampling techniques. Compared to other methods, the CB-DDS block is entirely isolated from the sampling path, therefore, its effect on the signal-to-noise ratio during the decision-making process is minimized, and it can be used with any available ADCs. The CB-DDS method is not

limited to specific signal types, unlike [22, 23, 43], and its CF and PR-SNDR are widely tunable by adjusting the reference thresholds, voltage gain and/or clock frequency. The accuracy of the different methods presented in Table 2.2 cannot be easily compared since they are inherently signal-dependent. An ECG signal similar to the one analyzed in Figure 2.12 has been applied to the CB-SDS method in [14]. The reported PR-SNDR of 28.7 dB with a CF of 6.1 is comparable to our measured PR-SNDR of 26.6 dB with a CF of 6.7 for the proposed CB-DDS method. However, the CB-DDS method achieves higher CFs than those of CB-SDS method for PPG signals while having better PR-SNDR.

As discussed, using the implemented CB-DDS technique in a data acquisition system allows it to wake up only when a significant event occurs, therefore, the dynamic power is reduced by decreasing the operating time. The PSF in a data acquisition system using an NUS block can be defined as [14]:

$$\text{PSF} = \left(1 - \frac{\text{System Power w/ NUS}}{\text{System Power w/o NUS}}\right) \times 100\%. \tag{2.9}$$

If the entire system power is mostly determined by the dynamic power, the maximum PSF is equal to $(1 - 1/\text{CF}) \times 100\%$, assuming that the power consumption of the NUS block is negligible compared to the system, *i.e.,* with a common CF of 6, a maximum PSF of 83.3% can be achieved. For example, when measured with a Texas Instruments CC2650 RF microcontroller, commonly used in low-power wireless sensor systems, the standalone microcontroller consumes 1.7 mW. With the CB-DDS block, the microcontroller power can be reduced by a PSF of 81%. On its own, the CB-DDS system only consumes 155 nW, which is 8 times less than the power consumption of the CB-SDS system in [14]. Due to the low complexity of the CB-DDS technique, the area of the fabricated circuit (0.04 mm^2) is one of the smallest among the reported works in Table 2.2. The area is comparable to the fabricated LC systems in [41, 42], while it is three times less than the chip area used by CB-SDS system [14].

2.3 Summary

In this chapter, we proposed an ultra-low-power, clock-based non-uniform sampling scheme using a derivative-based algorithm. The derivative-based algorithm can maintain accuracy comparable to other sampling schemes; however, the algorithm can be implemented with relatively simple analog blocks that reduce its complexity and, thereby, its power consumption compared to other schemes. Several techniques have been used to further reduce the power and improve the tunability of the system. The reference threshold and voltage gain of the proposed system can be tuned to achieve any desirable PR-SNDR or CF. The proposed system is interfaced to, but isolated from, the ADC in an acquisition system which enables it when necessary to reduce the total power dissipation of the system. It was fabricated in TSMC's 0.13-μm CMOS technology and tested with real-world and ideal signals. The CB-DDS system consumes less than 155 nW. By adding the proposed CB-DDS system to a data acquisition system chain, the power dissipation of the entire system can be significantly reduced.

Chapter 3

A Clockless Derivative-Dependent Sampling Scheme for Power-Efficient Data Acquisition Systems

As discussed earlier in Chapter 1, a signal having multiple time intervals with little or no activity represents the best use case for NUS schemes where parts of inactivity in the signal often contain little or no information and can be represented accurately by fewer samples than would be retained using a uniform sampling scheme. The NUS schemes define a significant event to decide whether to retain a sample of the signal or not. For instance, the CL-LC schemes use constant predefined voltage levels as references. Assuming the signal voltage value lies between the $(n)^{\text{th}}$ and $(n+1)^{\text{th}}$ reference levels, only when this value crosses the reference voltage level above it ($V_{ref,n+1}$) or below it ($V_{ref,n}$) a significant event is detected, shown in Figure 3.1(a). This can be mathematically expressed as

$$\begin{aligned} v_{in}(t) &\leq V_{ref,n}, \\ v_{in}(t) &\geq V_{ref,n} + V_q = V_{ref,n+1}, \end{aligned} \tag{3.1}$$

where $v_{in}(t)$ is the instant voltage level of the signal, and V_q is the quantization step. Accordingly, as long as the signal value is between two levels, it is considered as a low-activity part and no significant event is detected so that no sample is retained. This means that the CL-LC scheme tracks the signal in the horizontal direction only

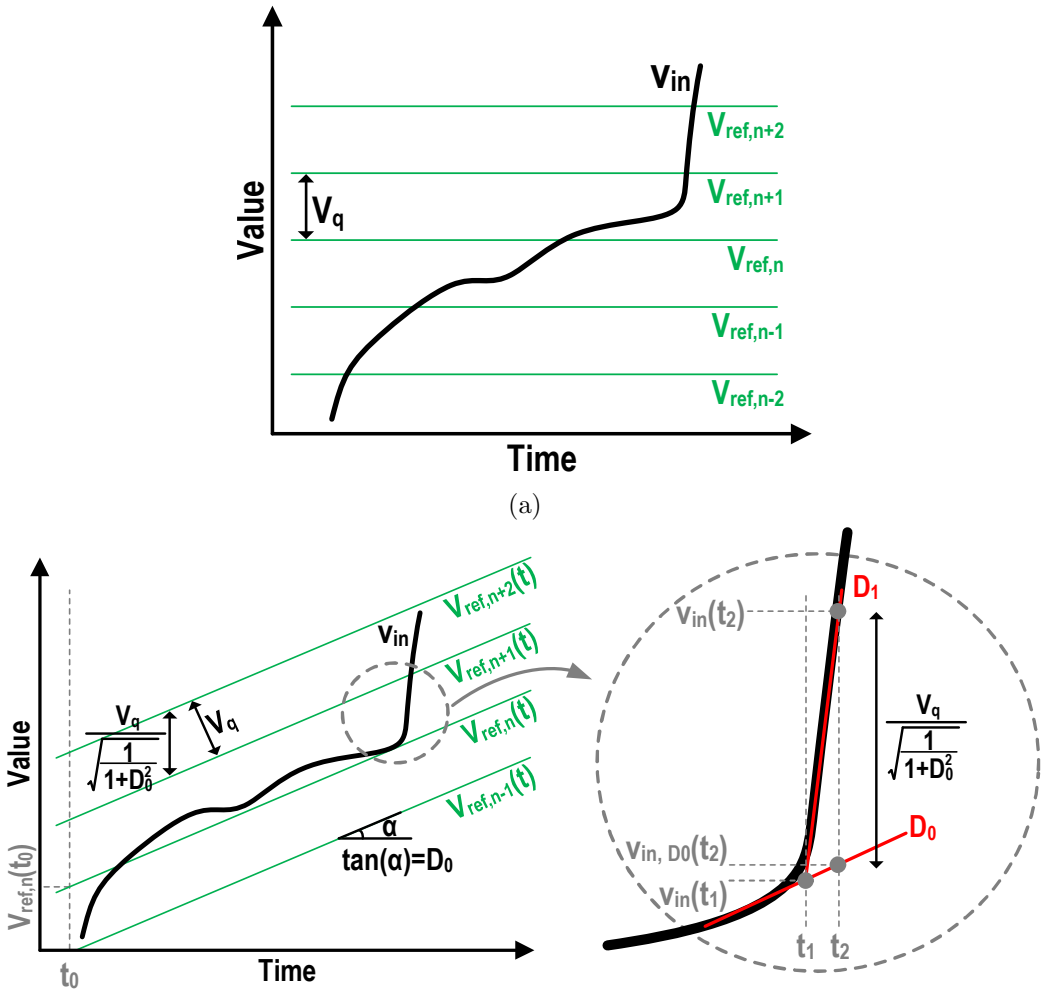


Figure 3.1: Reference levels in (a) conventional CL-LC, and (b) CL-MDLC schemes.

as the reference levels are constant. However, we may argue that a more robust scheme would be able to track the signal in multiple directions where an inactive part of the signal occurs when the variations are bounded between any two parallel straight lines with any arbitrary slope/direction. Therefore, we present a Clockless Multi-Dimensional Level-Crossing (CL-MDLC) scheme, as shown in Figure 3.1(b). This scheme adds another degree of freedom by introducing sloped reference levels, where their significance is evident by the fact that in first-order interpolation, each pair of consecutive retained samples is joined by a straight line that can have any slope, not just horizontal lines. The mathematical representation of such a scheme

can be defined as

$$\begin{aligned} v_{in}(t) &\leq V_{ref,n}(t_0) + D_0 \times (t - t_0) = V_{ref,n}(t), \\ v_{in}(t) &\geq V_{ref,n}(t_0) + D_0 \times (t - t_0) + \frac{V_q}{\sqrt{\frac{1}{1+D_0^2}}} = V_{ref,n+1}(t), \end{aligned} \tag{3.2}$$

where $V_{ref,n}(t_0)$ is the initial voltage of the $(n)^{\text{th}}$ reference line, t_0 is the initial time, and D_0 is the derivative of the sloped reference levels. The term $V_q/\sqrt{1/(1+D_0^2)}$ can be considered as the quantization step of the CL-MDLC scheme which is dependent on the derivative of the references, D_0. Note that having $D_0 = 0$, the reference levels are horizontal lines similar to the conventional CL-LC scheme shown in Figure 3.1(a), and therefore, Equation (3.2) would be the same as Equation (3.1) in this case. In other words, the CL-LC scheme is a special case of the CL-MDLC scheme.

If the signal's average derivative remains D_0, a significant event is not detected in the CL-MDLC scheme as the signal stays between the $(n)^{\text{th}}$ and $(n+1)^{\text{th}}$ sloped reference lines. Assuming the signal changes its direction to an average derivative of D_1 ($D_1 > D_0$) starting from t_1, shown in Figure 3.1(b), we would have

$$v_{in}(t) = D_1 \times (t - t_1) + v_{in}(t_1), \tag{3.3}$$

$$v_{in_{D0}}(t) = D_0 \times (t - t_1) + v_{in}(t_1). \tag{3.4}$$

where $v_{in_{D0}}(t)$ represents the line with the derivative D_0. If $v_{in}(t) - v_{in_{D0}}(t)$ exceeds $V_q/\sqrt{1/(1+D_0^2)}$, it indicates the signal has crossed the $V_{ref,n+1}$ reference line. Assuming the crossing happened as t_2 this can be given by,

$$v_{in}(t_2) - v_{in_{D0}}(t_2) = (D_1 - D_0) \times (t_2 - t_1) = \frac{V_q}{\sqrt{\frac{1}{1+D_0^2}}}, \tag{3.5}$$

Therefore, if a significant event is to be detected at or before t_2, D_1 can be found using

$$D_1 \geq D_0 + \frac{V_q}{(t_2 - t_1) \times \sqrt{\frac{1}{1+D_0^2}}}, \tag{3.6}$$

Note that a set of similar equations can be written for the cases that $D_1 < D_0$ or the cases that D_0 has a negative value. In summary, it can be claimed that the significant changes in the derivative of the signal with respect to the sloped reference lines in the

CL-MDLC scheme can be interpreted as an equivalent substitute for the significant event of crossing the horizontal lines in the CL-LC scheme.

If the signal's average derivative remains D_0, a significant event is not detected in the CL-MDLC scheme as the signal stays between the $(n)^{\text{th}}$ and $(n+1)^{\text{th}}$ sloped reference lines. Assuming the signal changes its direction to an average derivative of D_1 (D_1>D_0) starting from t_1, shown in Figure 3.1(b), we would have

$$v_{in}(t) = D_1 \times (t - t_1) + v_{in}(t_1), \tag{3.7}$$

$$v_{in_{D0}}(t) = D_0 \times (t - t_1) + v_{in}(t_1). \tag{3.8}$$

where $v_{in_{D0}}(t)$ represents the line with the derivative D_0. If $v_{in}(t) - v_{in_{D0}}(t)$ exceeds $V_q/\sqrt{1/(1+D_0^2)}$, it indicates the signal has crossed the $V_{ref,n+1}$ reference line. Assuming the crossing happened as t_2 this can be given by,

$$v_{in}(t_2) - v_{in_{D0}}(t_2) = (D_1 - D_0) \times (t_2 - t_1) = \frac{V_q}{\sqrt{\frac{1}{1+D_0^2}}}, \tag{3.9}$$

Therefore, if a significant event is to be detected at or before t_2, D_1 can be found using

$$D_1 \geq D_0 + \frac{V_q}{(t_2 - t_1) \times \sqrt{\frac{1}{1+D_0^2}}}, \tag{3.10}$$

Note that a set of similar equations can be written for the cases that $D_1 < D_0$ or the cases that D_0 has a negative value. In summary, it can be claimed that the significant changes in the derivative of the signal with respect to the sloped reference lines in the CL-MDLC scheme can be interpreted as an equivalent substitute for the significant event of crossing the horizontal lines in the CL-LC scheme.

Since the CL-MDLC scheme can reconstruct a signal with fewer points compared to the conventional CL-LC scheme, the overall power consumption of the data acquisition system can be significantly reduced if such an NUS scheme is applied to the input signal. However, the implementation of the CL-MDLC requires complex circuitry and introduces additional power consumption to the NUS block itself to perform extensive computations in the analog domain; this demands a practical alternative based on the same principle.

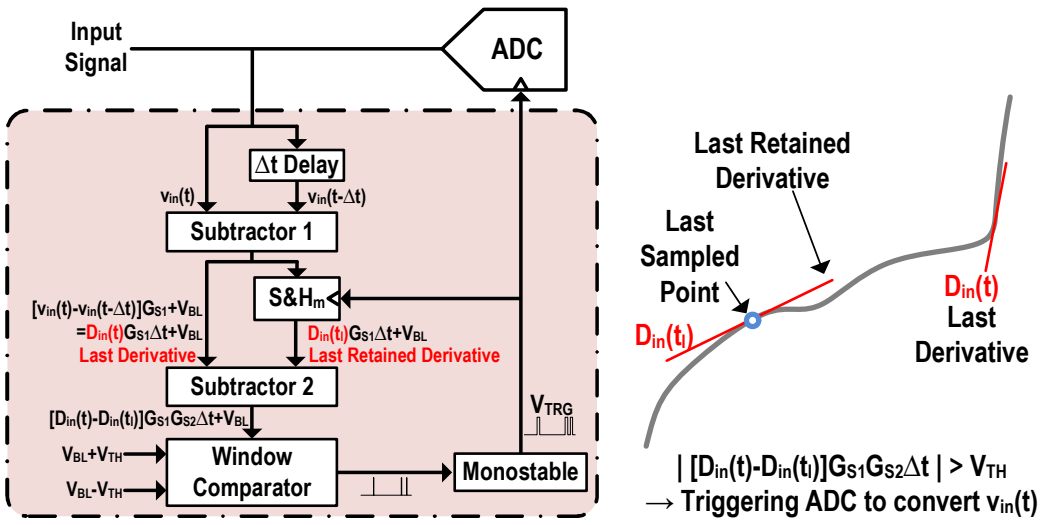


Figure 3.2: Overall block diagram of the CL-DDS scheme.

3.1 Proposed Clockless Derivative-Dependent Sampling (CL-DDS) Scheme

A CL-DDS method is proposed in this work (Figure 3.2) as a substitute for the discussed CL-MDLC scheme. The proposed CL-DDS scheme detects significant changes in the signal derivative and accordingly generates an output trigger pulse according to the following procedure:

(1) The first subtractor receives the input signal ($v_{in}(t)$) and its delayed version ($v_{in}(t-\Delta t)$) and produces an amplified approximation of the signal derivative at its output as follows

$$v_{S1}(t) = (v_{in}(t) - v_{in}(t-\Delta t))\, G_{S1} + V_{BL}$$
$$= \frac{v_{in}(t) - v_{in}(t-\Delta t)}{\Delta t} G_{S1}\Delta t + V_{BL} = D_{in}(t) G_{S1}\Delta t + V_{BL}, \quad (3.11)$$

where G_{S1} is the first subtractor voltage gain, V_{BL} is its output DC voltage baseline, and $D_{in}(t)$ is the relative derivative of the signal.

(2) The second subtractor amplifies the difference between the first subtractor output, the current derivative, and the last retained derivative of the signal (at the time t_l) stored on a sample-and-hold capacitor as follows

$$v_{S2}(t) = (D_{in}(t)G_{S1}\Delta t - D_{in}(t_l)G_{S1}\Delta t) \times G_{S2} + V_{BL}$$
$$\approx (D_{in}(t) - D_{in}(t_l)) \times G_{S1}G_{S2}\Delta t + V_{BL} \quad (3.12)$$

where G_{S2} is the second subtractor voltage gain and $D_{in}(t_l)$ is the last retained derivative of the signal at the time t_l.

(3) If the second subtractor output exceeds the references of the window comparator, $V_{BL} + V_{TH}$ or $V_{BL} - V_{TH}$, the comparator will generate an output signal indicating that a significant event is detected. This can be mathematically represented by

$$|(D_{in}(t) - D_{in}(t_l)) \times G_{S1}G_{S2}\Delta t| \geq V_{TH} \quad (3.13)$$

$$\Rightarrow \begin{cases} D_{in}(t) \geq D_{in}(t_l) + \frac{V_{TH}}{G_{S1}G_{S2}\Delta t} \\ D_{in}(t) \leq D_{in}(t_l) - \frac{V_{TH}}{G_{S1}G_{S2}\Delta t} \end{cases} . \quad (3.14)$$

Equation (3.14), the significant event definition in the proposed CL-DDS, provides a relation similar to Equation (3.10) (presented by the CL-MDLC) with some additional constants.

(4) The monostable receives the comparator output and generates a single pulse (the output trigger, V_{TRG}) with a tunable width when a transition from low to high occurs at its input.

(5) The sample-and-hold circuit is enabled by the monostable output (V_{TRG}) to store the current derivative as the last retained derivative of the signal for future computations. The ADC is also enabled by V_{TRG} to convert the input voltage.

(6) Accordingly, the second subtractor is then reset to low as the current derivative is now equal to the last retained derivative stored on the sample-and-hold capacitor.

(7) The comparator output is also restored from high to low as the second subtractor shows a value less than the threshold close to zero.

The resolution of the proposed CL-DDS technique, indicated in Equation (3.14), is then specified by Δt (the initial time delay), V_{TH} (window comparator thresholds), and $G_{S1}G_{S2}$ (the accumulated gain of amplifiers). This resolution should be tuned based on the targeted application, frequency content, and output quality. In this regard, setting a lower threshold value, increasing the initial delay, or a higher

voltage gain in the amplifiers enhances the resolution and output accuracy, while increasing the number of sampled points. Conversely, a higher threshold, lower initial delay, or lower gain relaxes the resolution, resulting in lower output accuracy but with a reduced number of points. The scheme resolution can be calibrated with the fixed elements for specific applications and quality, or manually adjusted by tuning the thresholds, the initial delay, or the gain. It can be also dynamically calibrated through a feedback response by a processor or external analog circuitry to obtain a targeted accuracy or number of sampled points. Note that in the proposed CL-DDS scheme, the proceeding ADC receives the input signal directly, therefore, negligible degradation in the SNR is expected as the NUS block is separated, and isolated from the signal receiving path. This is in contrast to most conventional NUS schemes, where the input signal needs to be processed by the NUS block [35, 37, 42].

3.2 Comparing CL-LC and CL-DDS

The power budget saving in a data acquisition system using an NUS scheme is at the cost of increasing the reconstruction error (or degrading the accuracy). Note that the accuracy of a reconstructed signal over the time interval of $t_1 < t < t_2$ can be represented by either RMSD or PR-SNDR, as mathematically defined below:

$$\text{RMSD} = \sqrt{\frac{1}{t_2 - t_1} \int_{t_1}^{t_2} |v_e(t)|^2 dt}, \tag{3.15}$$

$$\begin{aligned} \text{PR-SNDR} &= 10 \log \frac{Power\left(v_i(t) - mean\left(v_i(t)\right)\right)}{Power\left(v_e(t)\right)} \\ &= 10 \log \frac{\int_{t_1}^{t_2} \left| v_i(t) - \left(\frac{1}{t_2 - t_1} \int_{t_1}^{t_2} v_i(t) dt \right) \right|^2 dt}{\int_{t_1}^{t_2} |v_e(t)|^2 dt}, \end{aligned} \tag{3.16}$$

where $v_i(t)$ and $v_e(t)$ are the input and the error/deviation after reconstruction, respectively. To compare the performance of the CL-DDS scheme to the conventional CL-LC method, a portion of the arbitrary signal is sampled and reconstructed with these schemes, and the results are shown in Figure 3.3 and Table 3.1. Note that

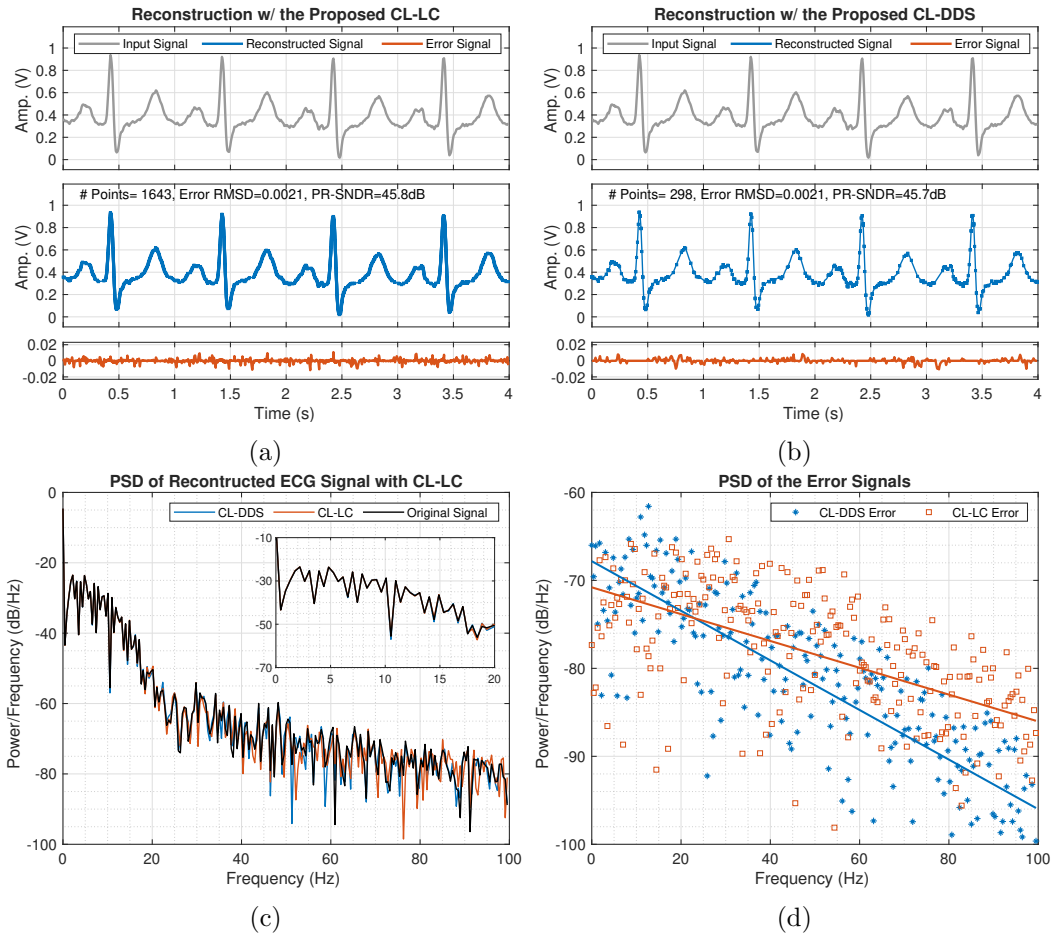


Figure 3.3: A comparison between clockless NUS methods by applying (a) CL-LC, and (b) the proposed CL-DDS on a real-world ECG signal, (c) PSD of the reconstructed ECG signals by CL-LC and CL-DDS, and (d) PSD of error signals after reconstruction of ECG signal.

first-order linear interpolation has been used for reconstruction in both schemes. The number of points required for the reconstruction to obtain a specific accuracy is reported for each scheme and is compared within the same scenario to show which scheme is able to save the power of a data acquisition system the most while having the same PR-SNDR or RMSD.

A real-world ECG signal is sampled using both CL-LC and CL-DDS schemes and the results are shown in Figures 3.3(a) and 3.3(b), respectively. High accuracy of post-reconstruction is targeted in this case by increasing the number of reference levels for the CL-LC scheme and by setting a finer threshold for CL-DDS. Thus, a PR-SNDR

of 45.7dB and an RMSD of 0.0021 are obtained for both schemes. However, the number of points required to achieve such accuracy is 298 and 1643 for the CL-DDS and CL-LC schemes, respectively. Note that the number of sampled points directly correlates with the total power dissipation of the overall sensor/device during storing, processing, and/or transmitting of data. Consequently, an ECG monitoring device employing CL-DDS scheme for data acquisition is expected to save more power, by a factor of over 5 ($1643/298 = 5.5$), compared to a similar device using CL-LC scheme. The PSD of the reconstructed signal using CL-LC and CL-DDS schemes are also shown in Figure 3.3(c). Compared to the PSD of the input signal, there is no significant difference at lower frequencies (<20 Hz) for both schemes; however, the deviation from the input signal spectrum is larger at higher frequencies for the CL-LC scheme. The PSD of the error signal for each scheme along with the linear regression (Figure 3.3(d)) also confirms this observation. The PSD of the error for the CL-LC scheme is larger than that of CL-DDS at higher frequencies (>20 Hz) while it is smaller at lower frequencies. This means the CL-DDS technique is a better option for processing higher-frequency contents.

The CL-LC and CL-DDS schemes are also applied to several other example cases including a saw-tooth signal, a one-tone sinusoidal signal, a two-tone signal, and real-world ECG and EEG signals, and the results are shown in Table 3.1. This set of cases has been selected to investigate the performance of CL-LC and CL-DDS schemes in the presence of different signal characteristics such as high-frequency components (i.e., sharp edges), low-frequency components, noise, etc. The level of the signals is also assumed to be only between 0 to $1V$, and the number of required points in a time interval of one second to achieve a targeted PR-SNDR is reported as N_{CLLC} and N_{CLDDS} for the CL-LC and CL-DDS schemes, respectively. The ratio of $n_r = N_{CLDDS}/N_{CLLC}$ provides a comparison regarding the efficiency of each scheme when targeting the same accuracy in reconstruction. In the following, the example cases are discussed:

Table 3.1: Summary of the simulation results on various signals.

Signal Type	Time Interval	Targeted PR-SNDR	$N_{CL\text{-}DDS}$	CL-DDS Resolution	$N_{CL\text{-}LC}$	CL-LC # of Refs.	n_r
Saw-tooth (1 Hz)	2 s	∼40 dB	5	5e-4	139	40	0.036
One-tone (20-Hz Sine)	0.2 s	47.5 dB	137	7.5e-5	272	35	0.5
		28.7 dB	41	3e-4	48	8	0.85
Two-tone (10-Hz Sine +1-Hz Sine)	2 s	45.2 dB	315	2e-4	1488	128	0.21
		37.8 dB	203	3.4e-4	704	64	0.29
		30.2 dB	131	5e-4	329	32	0.4
ECG	4 s	45.8 dB	298	1e-4	1648	150	0.18
		37.3 dB	214	1.8e-4	669	64	0.32
		27.5 dB	157	8.5e-4	239	25	0.65
EEG	4 s	46 dB	45	5e-4	587	80	0.07
		29 dB	32	1.6e-3	99	16	0.32

1) A saw-tooth signal may be a perfect scenario for the CL-DDS scheme as we only need the points at the peaks for the reconstruction. However, for the CL-LC scheme, the number of required points varies depending on the phase and amplitude of the signal and the number of reference levels. Therefore, as indicated in Table 3.1, with a fewer number of points ($N_{CLDDS} = 5$) a high PR-SNDR has been achieved for the CL-DDS scheme while in CL-DDS a considerably greater number of points are required ($N_{CLLC} = 139$).

2) For the single-tone and two-tone example cases, most of the points required for reconstruction with CL-DDS are expected to be at the peaks of the signal due to significant changes in the derivative of the signal in these parts. However, in the reconstruction with CL-LC several points are generated in the fast-moving parts (i.e., rising or falling transitions) due to having a fixed quantization step. This makes the reconstruction with CL-LC scheme less efficient since in the first-order linear interpolation the middle points in the fast-moving parts are less useful to obtain a good PR-SNDR than the points at the peaks.

3) The CL-DDS scheme is a better option for the EEG signal since the signal consists of several sharp edges, similar to a saw-tooth signal. As with the first-order linear interpolation, the edges of the signal are necessary to be detected, and the threshold value in CL-DDS scheme can be set to the smaller values. However, a finer quantization step (more reference levels) is needed to detect the edges in the CL-LC scheme which increases the required number of points.

4) An ECG signal can be considered as an arbitrary signal that consists of relatively flat areas (inactive areas) and sharp edges (active areas). The number of required points to reconstruct the flat areas of the signal may be fairly close for both schemes; however, depending on the threshold and quantization step set for the CL-DDS and CL-LC schemes respectively, the difference might be more evident in the fast transition parts, especially in the most active (peak) interval.

To demonstrate the advantages of the proposed CL-DDS over the CL-LC method

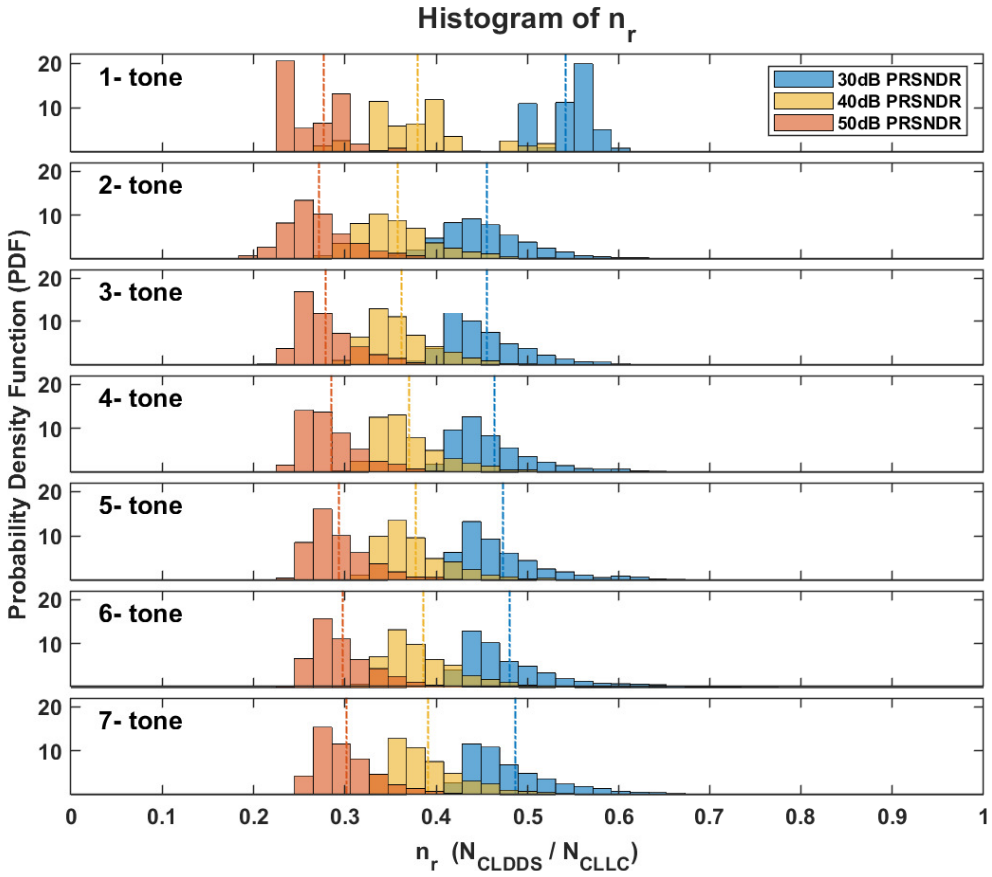


Figure 3.4: Distribution of n_r for different tones and multiple targeted PR-SNDR values for 2000 iterations.

across various scenarios, the results of a comprehensive simulation are presented in Figure 3.4. According to the Fourier series, a real-world signal, $v_{\text{sig}}(t)$, can be expressed as the sum of the frequency components, f_n, as

$$v_{\text{sig}}(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(2\pi f_n t + \phi_n), \tag{3.17}$$

where a_n and ϕ_n are the amplitude and phase of each corresponding frequency, respectively. In this simulation, signals comprising varying numbers of components (ranging from one to seven) are applied to both the CL-DDS and CL-LC methods, and the ratio of sampled points (n_r) is calculated while targeting the same PR-SNDR for both schemes. Three PR-SNDR levels of 30 dB, 40 dB, and 50 dB have been targeted in this simulation. By randomly selecting values for a_n (from 0 to 1), ϕ_n (from 0 to 2π), and f_n (from 1 Hz to 10 MHz), 1000 iterations are conducted for each

scenario, and distribution of 1000 values of n_r is obtained to provide insights into the performance of CL-DDS and CL-LC schemes over different signal compositions. The simulation results shown in Figure 3.4 reveal the following observations: (a) In all iterations, $n_r < 1$, indicating that the CL-DDS consistently achieves the targeted PR-SNDR with fewer sampled points, regardless of the signal type or complexity. (b) With a higher targeted PR-SNDR level, the value of n_r decreases, indicating that the advantages of CL-DDS are more pronounced when a higher quality of reconstruction is targeted.

3.3 Circuit Implementation of the Proposed Scheme

Figure 3.5(a) illustrates the circuit implementation of the proposed CL-DDS scheme, the block diagram of which is shown in Figure 3.2. A tunable RC delay circuit first provides a delayed version of the input signal, and the following amplifiers (S_1 and S_2) subtract the input signal from its delayed version to produce an amplified approximation of signal derivative at their output (Equation (3.11)). The following inverting operational amplifier (op-amp) stages (O_1 and O_2) provide more amplification in addition to a more robust DC baseline voltage. The output of O_2 is connected to a sample-and-hold circuit clocked by the output trigger signal so that it can be stored as the last retained derivative of the signal. In other words, while the output of O_1 represents the current derivative of the signal, the signal across C_S represents the last retained derivative of the signal (sampled at the latest significant event). Note that the system incorporates two separate paths (S_1-O_1 and S_2-O_2 paths) to avoid charge sharing between the paths. The subtractor amplifier, S_3, amplifies the difference between the current and the last derivatives of the signal, Equation (3.12), and follows by another inverting op-amp stage, O_3. A window comparator then compares the output of O_3 with the threshold values, Equations (3.13) and (3.14), changing its output from low to high whenever it is greater than $VDD/2 + V_{TH}$ or less than $VDD/2 - V_{TH}$, noting that the threshold references can be also unbalanced. Then

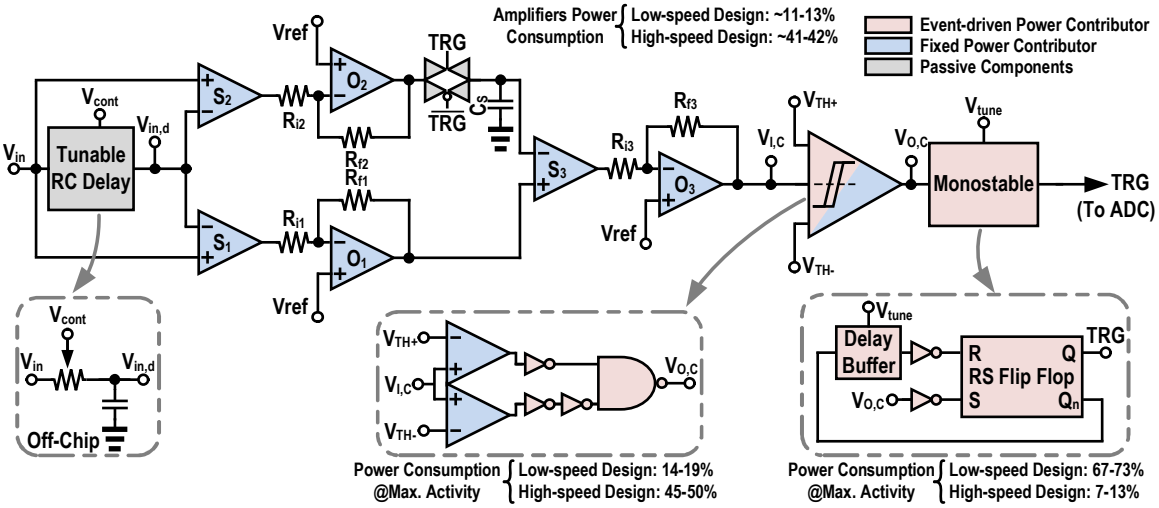


Figure 3.5: (a) Circuit implementation of the proposed CL-DDS system, and (b) a sample response to a sawtooth signal.

the comparator triggers the monostable circuit to generate a pulse signal with the predetermined pulse width. This pulse signal, as an indication of a significant event, triggers the next ADC to convert the analog input to digital.

Figure 3.5(b) shows the proposed CL-DDS system response to a sawtooth wave where significant events have been detected when the signal changes its direction at the signal edges. The comparator input ($V_{I,C}$) and output ($V_{O,C}$) in addition to the monostable response (TRG) to the comparator output are also shown in this figure.

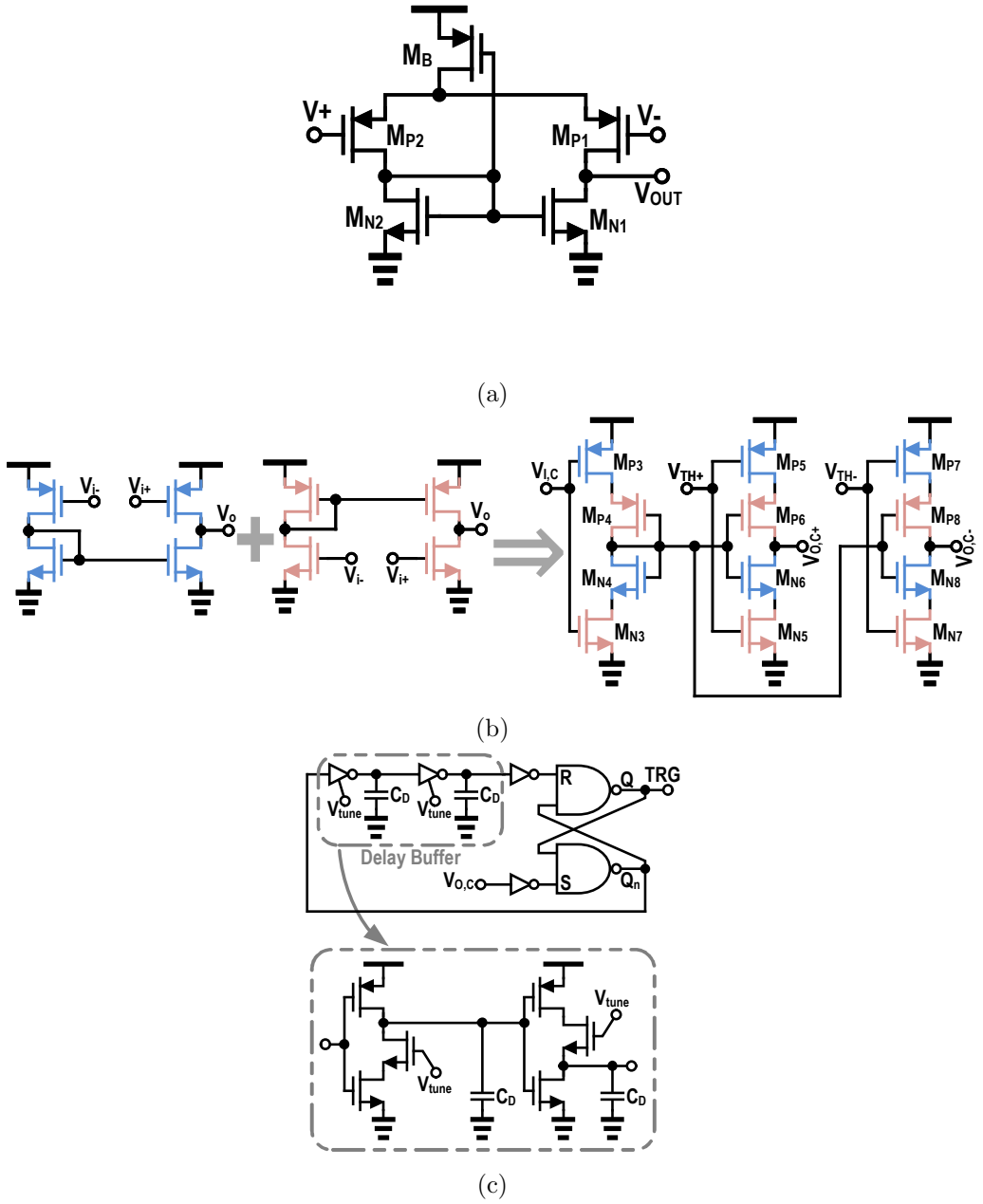


Figure 3.6: Circuit implementation of (a) the main amplifiers, (b) the window comparator, and (c) the monostable.

At signal edges where the derivative of the signal changes, the comparator input ($V_{I,C}$) gradually changes until it crosses one of the threshold references. Then the comparator produces a short impulse at its output ($V_{O,C}$) triggering the monostable circuit to generate the TRG signal with a predetermined pulse width. Note that the above procedure results in a certain time delay (decision delay) in the proposed CL-

DDS system output response which includes (a) the time interval that $V_{I,C}$ is changing until crosses one of the thresholds, (b) the time interval that the comparator reacts and produces the short impulse $V_{O,C}$, and (c) the time interval that the monostable is triggered and generates TRG signal. All the above time intervals mainly depend on the amount of circuit parasitic capacitance and the charging currents through them, or equivalently, the slew rate of the implemented circuits. Therefore, there is a trade-off between the power consumption and the decision delay of the CL-DDS system.

The effect of decision delay on the accuracy of reconstruction in a clockless NUS scheme might be ignored when the signal only comprises low-frequency content; however, when the signal contains high-frequency components the error due to the decision delay would be increased. Figure 3.7 investigates the PR-SNDR of different signals versus decision delay through CL-DDS where bio-signals such as EEG and ECG signals are affected the least compared to sawtooth signals. This is mainly due to low-frequency components of the bio-signals that make the signal movement through time smoother so that the error due to decision delay after a significant event might be ignored. On the other hand, the high-frequency components of a sawtooth signal, generated at their sharp edges, make this type of signal more sensitive to the decision delay by the scheme. A decision delay of 1 μs, for example, may reduce the achieved PR-SNDR by more than 40 dB in the reconstruction of a high-frequency saw-tooth signal (Figure 3.7).

Nonidealities, such as noise and offset caused by CL-DDS blocks, may result in the misdetection of a significant event and eventually increase the number of sampled points, although it would not affect the integrity of the retained sample due to the isolation of the CL-DDS technique from ADC sampling. The structural noise can be added to the signal that feeds the window comparator ($V_{I,C}$), and depending on its strength and/or the window size can result in a false detection of a significant event. To avoid this, it is preferable to widen the size of the window, for example,

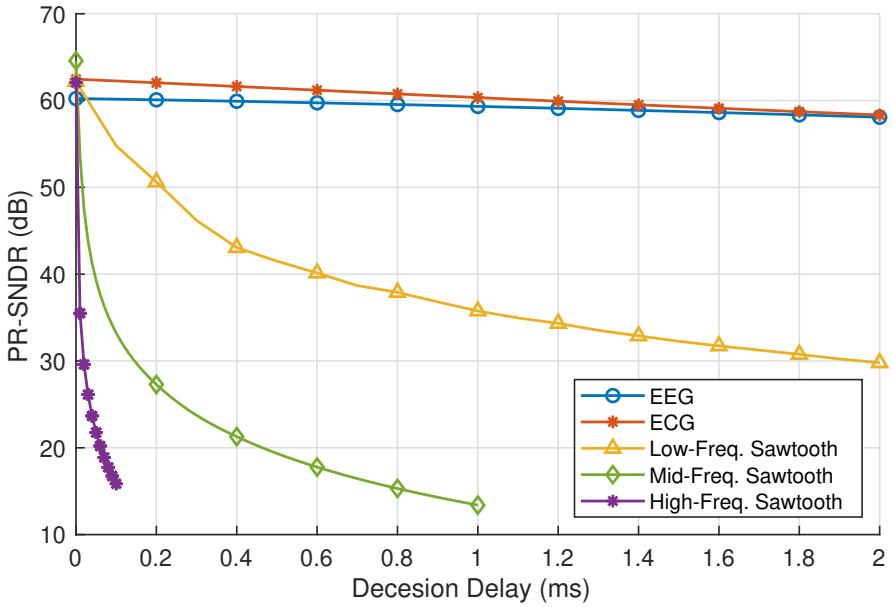


Figure 3.7: The effect of decision delay on the quality of reconstruction for various signals with different frequency contents.

10 times greater than the accumulated noise strength, so that the effect of noise is negligible. The baseline of $V_{I,C}$ might also be changed by the offset of CL-DDS building blocks which leads to the same issue. In such case, two solutions are provided by the structure of CL-DDS, (a) calibration of V_{ref} applied to amplifiers O_1-O_3 to have the least offset at the comparator input, and/or (b) providing the comparator with unbalanced references to compensate the offset. Assuming an accumulated offset of V_{OS} has shifted up the $V_{I,C}$ baseline, for example, the window thresholds can be also shifted up and be calibrated to $V_{TH+} + V_{OS}$ and $V_{TH-} + V_{OS}$, to minimize the effect of offset on the detection of significant events.

The versatility of the frequency components of the input might also affect the performance of the proposed CL-DDS technique. When the signal comprises both low- and high-frequency components (which is not typically the case for most targeted applications) the initial delay indicated in Equation (3.14) and provided by the RC circuit results in different voltage gains experienced by low- and high-frequency contents. This has no impact on the integrity of the original signal due to isolation of technique, but it results in either false detection of significant events which increases

the number of sampled points, or missing some significant event which may result in the loss of valuable signal information. The scheme resolution, determined by comparator window size, the initial delay, or the gain of amplifiers, can be then adjusted to obtain either a higher accuracy (maintaining both low- and high-frequency content at the expense of increasing power) or a lower number of sampled points (losing high-frequency contents at the advantage of power reduction). However, the RC cut-off corner frequency should be greater than the highest valuable frequency content (preferably 10 times higher) to avoid filtering through this stage. Moreover, the threshold values are limited to GND and VDD of the structure and must be significantly greater than the maximum expected noise voltage at the input of the comparator (preferably 100 times greater). This ensures that the circuit noise does not impact the detection process of the circuit. Note that the initial derivative in the CL-DDS scheme can also be achieved through a wideband analog differentiator, instead of a delay and a subtractor. This might be preferable when the signal contains very high-frequency and low-frequency contents simultaneously, although the remarkable power dissipation by an analog differentiator must be considered.

To verify that the proposed CL-DDS system is capable of operating over a wide frequency range for a large variety of applications, it has been designed and implemented in two versions: one for low-speed applications for triggering the ADCs with sampling rate up to 1 MHz and another for high-speed applications with the ADCs operating with a sampling rate up to 20 MHz. This helps to achieve the most power-efficient implementation in each case while producing appropriate decision delays for processing the lower- and the higher-frequency signals, respectively. Note that the scheme resolution indicated in Equation (3.14) must be adjusted for each targeted application and output quality, and it is specified by Δt (determined by RC time constant), V_{TH} (determined by window comparator references), and the accumulated gain of amplifiers. In this regard, the RC value, and V_{TH} are correlated; the greater the RC value, the greater the threshold required. However, the RC cut-off corner

frequency should be greater than the highest valuable frequency content (preferably 10 times higher) to avoid filtering through this stage. Moreover, the threshold values are limited to GND and VDD of the structure and must be significantly greater than the maximum expected noise voltage at the input of the comparator (preferably 100 times greater). This ensures that the circuit noise does not impact the detection process of the circuit. The following subsections discuss the proposed transistor-level implementation of each building block:

3.3.1 Main Amplifiers

Figure 3.6(a) shows the topology utilized in designing the subtractors and inverting op-amps. The structure utilizes a differential pair of PMOS transistors at the input with a self-biased current tail, which eliminates the need for any external biasing in the design. The structure should provide an acceptable common-mode rejection ratio (CMRR) to cancel out the common input signal and noise to amplify only the difference between the input and its delayed version which is directly proportional to the derivative of the signal. Note that a higher current consumption is considered for the high-speed design to provide the system with sufficient speed in the detection of significant events (i.e., less decision delay) as the signal is expected to have higher-frequency contents. The sizing of the transistors is accordingly optimized to achieve the desired quality of the reconstruction for the targeted applications and is reported in Table 3.2.

3.3.2 Window Comparators

Figure 3.6(b) illustrates the circuit evolution of the proposed current-reused window comparator. The proposed structure is self-biased and combines two NMOS- and PMOS-input differential pair amplifiers, without using a current tail. A conventional window comparator incorporates two separate comparators, where one branch of each comparator is connected to the input signal, and the other branch of each comparator is connected to a different reference voltage. In contrast, as the proposed window

Table 3.2: Sizing of transistors for low- and high-speed designs.

Transistor	Size W/L ($\mu m/\mu m$)	
	Low-speed Design	High-speed Design
M_B	0.15 / 5	0.15 / 0.2
$M_{N1,2}$	0.15 / 12	0.15 / 0.48
$M_{N3,5,7}$	0.15 / 12	0.15 / 1.5
$M_{N4,6,8}$	0.15 / 1.8	0.15 / 0.13
$M_{P1,2}$	0.15 / 2	0.3 / 0.13
$M_{P3,5,7}$	0.15 / 4.5	2 / 0.13
$M_{P4,6,8}$	0.15 / 1.8	0.15 / 0.13

comparator does not employ a current tail, a single common branch is connected to the input signal. Therefore, the comparator incorporates a total of three circuit branches rather than four, helping the proposed CL-DDS structure to reduce power consumption. The size of the transistors is chosen to have greater transconductance (g_m) for the input transistors and greater output resistance for the output transistors. This helps to produce a high voltage gain in a single stage in addition to reducing the output parasitic capacitors. The inverter buffers are also employed at the output to increase the overall gain and to produce sharper transitions. Note that multiple stacked transistors reduce the input dynamic range, however, the reference thresholds are not normally chosen close to the voltage boundaries (*VDD* or *GND*).

3.3.3 Monostable

Figure 3.6(c) illustrates the proposed monostable circuit implementation. The input inverter receives comparator output and if it is greater than the higher threshold voltage of the inverter, the RS flip-flop is set, and Q_n changes from 0 to 1. The RS flip-flop is then reset when it receives the delayed Q_n through two tunable delay buffers. In this way, when it is triggered by the comparator output at significant events, the monostable circuit generates a pulse signal with a certain pulse width tuned by the control voltage of the delay buffers (V_{tune}). The same circuit implementation, except

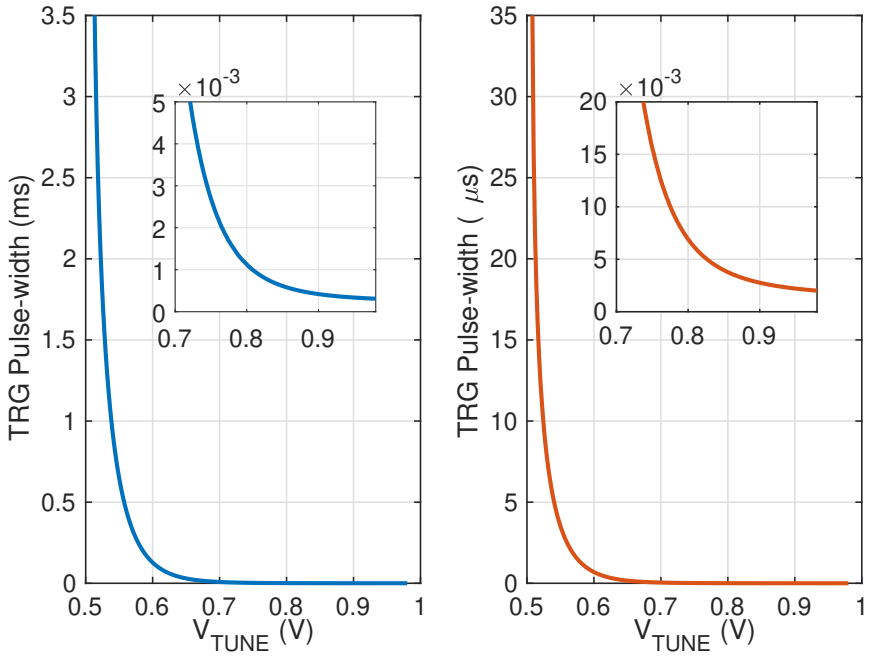
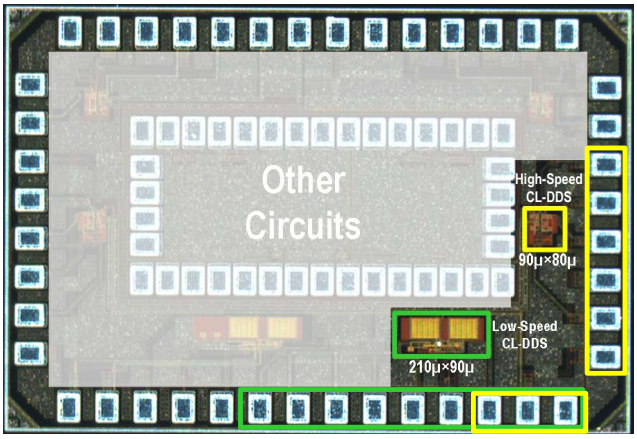


Figure 3.8: Tuning the width of output TRG pulse by V_{tune} in the proposed low- and high-speed design of monostable circuit.

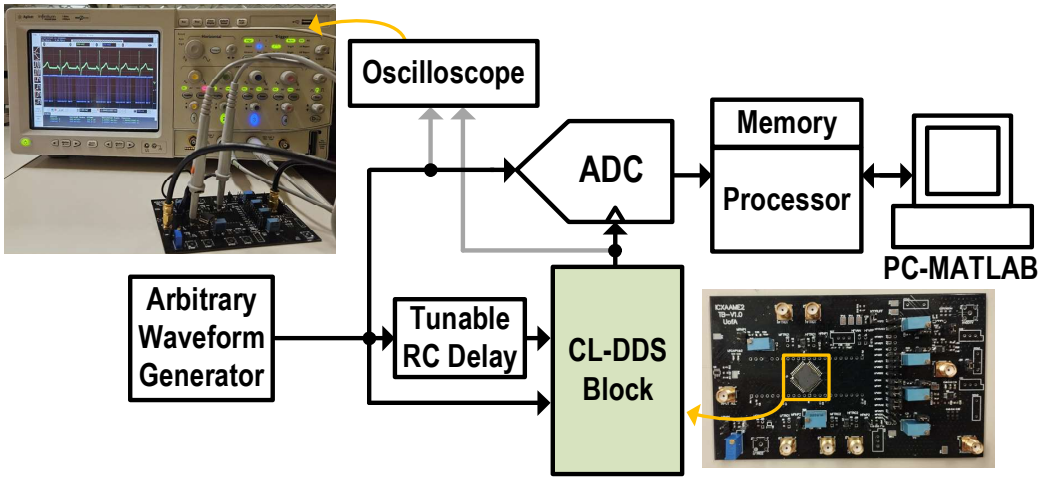
for the amount of capacitor utilized in the delay buffers, has been employed for both low- and high-speed designs. Figure 3.8 shows the width of the pulse signal generated by the monostable circuit versus V_{tune}. To obtain the required range for the width of the trigger pulse, a C_D of $\sim$ 5 pF and $\sim$ 30 fF are utilized for the low- and high-speed designs, respectively.

3.4 Experimental Results

The proposed CL-DDS system is fabricated in TSMC's 130-nm CMOS technology. The fabricated low- and high-speed CL-DDS systems occupy a die area of 0.019 mm^2 and 0.007 mm^2, respectively, as shown in Figure 3.9(a). The test bench shown in Figure 3.9(b) has been employed to measure the performance of the fabricated circuits. The test setup is the same for both low- and high-frequency designs, although distinct 8-bit ADCs have been utilized for each. A DC power source provides the main supply voltage of *VDD*, and other required bias voltages are generated from *VDD* using a set of variable large off-chip resistors. The external bias voltages include V_{tune} for



(a)



(b)

Figure 3.9: (a) Die micrograph of the proposed CL-DDS, and (b) test-bench.

adjusting the width of the generated TRG pulse, V_{TH+} and V_{TH-} for tuning the CL-DDS system resolution/threshold references, V_{ref} as the reference baseline ($VDD/2$). The power consumption for the generation of these voltages is negligible compared to the overall power consumption ($< 1\%$). The original signals are sampled/extracted using a high-speed high-resolution oscilloscope (1-GHz, 16-bit), and the reconstructed output signal has been generated by the MATLAB software on a personal computer. An off-chip variable R-C circuit has been employed to provide a tunable delay at the input side as different types of signals with a wide range of frequency components have been tested. In the following subsection, we describe the responses to the tested signals for both the low- and high-speed designs.

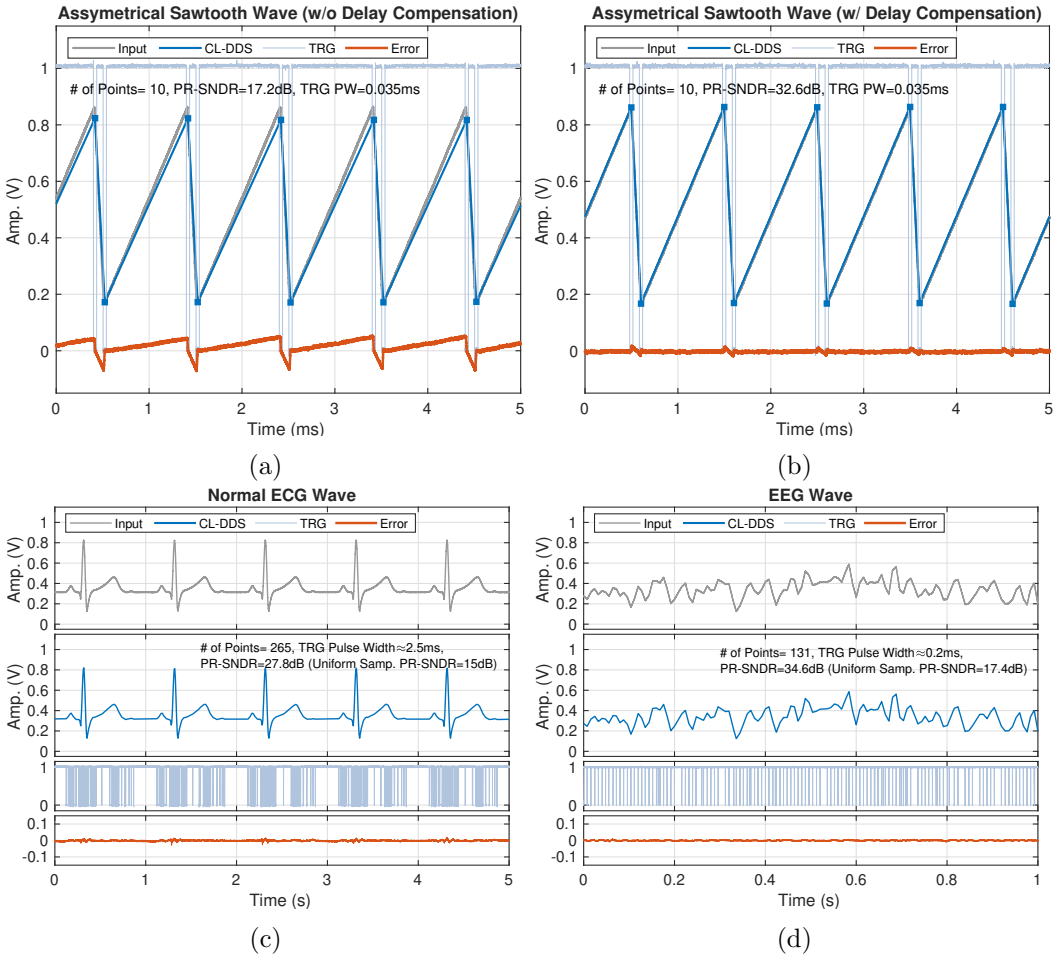


Figure 3.10: Measurement of system responses to a saw-tooth signal (a) without a compensation delay, and (b) with a compensation delay. Experimental results of the proposed low-speed CL-DDS system for (c) normal ECG and (d) EEG.

3.4.1 Tested Signals

The proposed CL-DDS system has been tested using various types of signals in different scenarios. For each case, the number of points required for reconstruction, and the achieved PR-SNDR are reported. For all experimental results, first-order linear interpolation, without any post-processing technique, is used for signal reconstruction. Figure 3.10(a) shows the proposed CL-DDS system response (low-speed design) to a 1 KHz sawtooth wave with 90% asymmetry. The CL-DDS system has picked the sharp edges of the sawtooth wave (10 points in total) where there is a significant change in the derivative of the signal, and 5 cycles of the signal have been

reconstructed with a PR-SNDR of $17dB$ (TRG pulse width $\approx 35\ \mu s$). Although the retained points are close to the edges of the sawtooth wave, the proposed CL-DDS system has been not able to exactly pick the edge points due to the decision delay. To compensate for the effect of decision delay, a delayed version of the input signal can be applied to the ADC. Figure 3.10(b) shows the CL-DDS system response to a similar sawtooth wave with a delay compensation to improve the resulted PR-SNDR to 32 dB through the same number of points. Note that a compensation delay can be applied to the input signal through an active buffer or a passive delay line/circuit. Since the impact of decision delay on the quality of the targeted application is negligible (as discussed earlier), no compensation delay is applied to other experimental results.

A normal ECG signal with a heart rate of 60 bpm (i.e., one beat per second) has been applied to the proposed low-speed CL-DDS system, and the results are shown in Figure 3.10(c). For the sake of clarity, the input, the reconstructed, the output TRG pulse, and the after-reconstruction error signals are separately shown in the subplots of this figure. In this scenario, with a pulse width of $\sim 2.5\ ms$ for the output TRG signal, 265 points have been retained within 5 s and a PR-SNDR of $\sim 28\ dB$ has been obtained. As expected, the CL-DDS system does not detect any significant events in the flat/inactive parts of the ECG signal; however, a dense accumulation of the TRG pulses is noticeable in the active region. Note that if a uniform sampling scheme is applied to this ECG signal and the sampling rate of the ADC is adjusted so that the same number of points (265 points) are converted by the uniform ADC, the obtained PR-SNDR would drop to 15 dB (using the same linear interpolation for reconstruction). This indicates the smartness and accuracy of the CL-DDS scheme in selecting the points to be retained and converted. It should be also noted that a narrower or wider comparator window can be also set to achieve a higher or lower PR-SNDR through a larger or smaller number of retained points, respectively.

An EEG signal is applied to the proposed low-speed CL-DDS system and the results

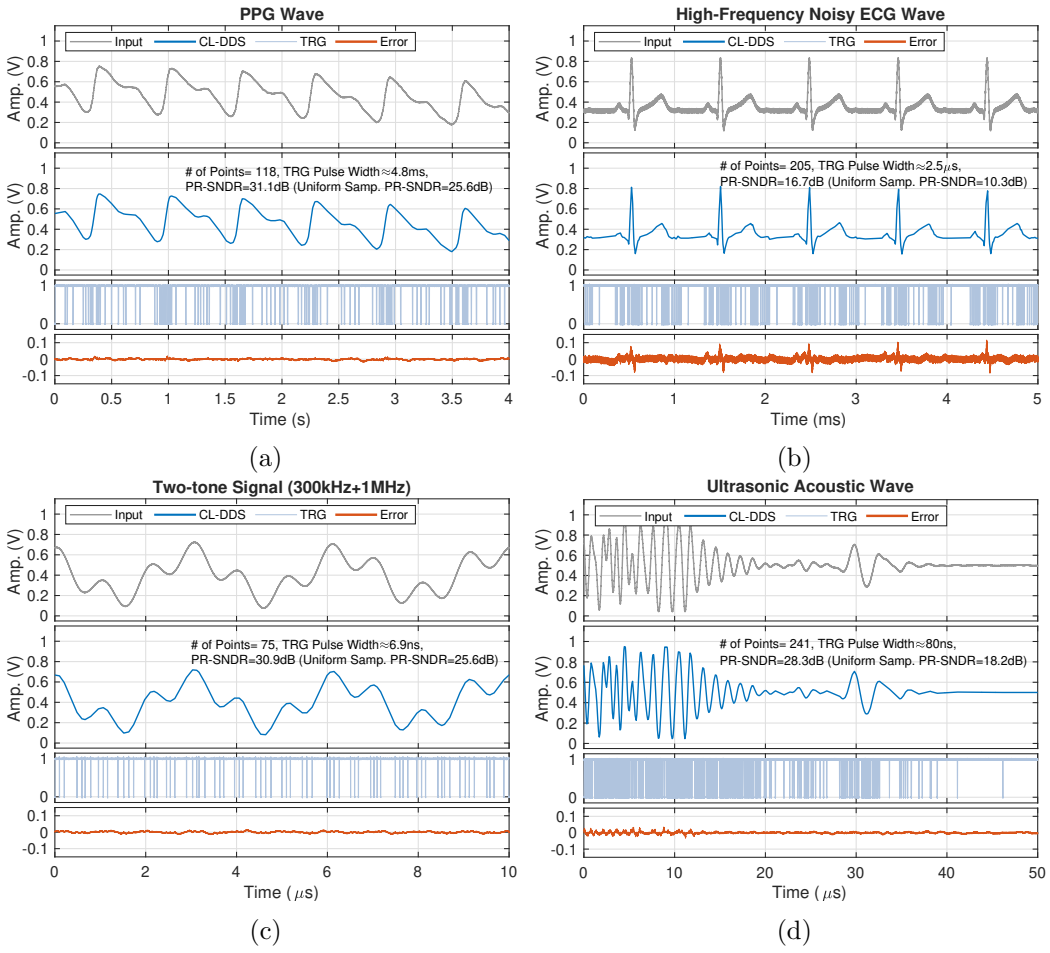


Figure 3.11: Experimental results of the proposed low-speed CL-DDS system for (a) PPG and (b) high-frequency noisy ECG. Experimental results of the proposed high-speed CL-DDS system for (g) two-tone signal and (h) Ultrasonic signal.

are shown in Figure 3.10(d). As expected, the TRG pulses are mostly produced at the edges of the signal, where the signal derivative experiences larger changes. As a result, a PR-SNDR of 34.6 dB is obtained with 131 retained points within 1 s and with a TRG pulse width of 0.2 ms, suitable for triggering ADCs with a $2.5 - kHz$ sampling rate. If uniformly sampled with a clock of 131 Hz to obtain the same number of points, the PR-SNDR would be reduced to 17.4 dB. An EEG signal might be an ideal case for the proposed CL-DDS scheme given the signal comprises edges with significant derivative changes while the frequency components are sufficiently low mitigating the impact of decision delay. This may also apply to PPG signal cases

As shown in Figure 3.11(a), with a low number of points (as low as approximately 30 Samples/second) a PR-SNDR of 31 dB is achieved, whereas that ratio would drop to 25 dB if uniformly sampled.

The effect of noise and higher frequency content is investigated in the scenario shown in Figure 3.11(b) where a noisy ECG signal (SNR=35.4 dB) with a rate of 60 k bpm (i.e., one beat per millisecond) has been applied to the low-speed CL-DDS system. A variety of sources may be responsible for the accumulated noise over a received ECG signal, including improper electrode-to-skin connections, physical activity, muscle noise, etc [44]. In this case, the width of the TRG pulse is tuned to $\sim$ 2.5 μs in this scenario, and a PR-SNDR of $\sim$ 17 dB is obtained by the signal reconstruction through the 205 retained points within 5 ms. This case, with such a high heartbeat rate, is not a real-world human ECG signal, and it only evaluates the performance of the CL-DDS system in the presence of noise. The CL-DDS system might detect some unnecessary significant events, especially in the quiet parts of the ECG signal, as a result of the high noise; however, it properly detects the significant events at the active parts. Note that to mitigate the signal noise effect, additional filters in the analog front end may also be advantageous.

Figures 3.11(c) and 3.11(d) show scenarios where three cycles of a two-tone signal (with two frequencies at 300 kHz+1 MHz) and an ultrasonic acoustic wave (obtained from a biomedical sonar sensor) are applied to the proposed high-speed CL-DDS system, respectively. The two-tone signal has been tested to investigate the scenarios where the signal comprises frequency components that are widely separated from each other. A PR-SNDR of $\sim$ 31 dB and $\sim$ 28 dB are obtained through 75 (within 10 μs period) and 241 (within 50 μs period) retained points for the two-tone and ultrasonic signal cases, respectively. As expected, the monostable produces fewer TRG pulses at periods of inactivity (quiet times) while it is more active at the onset.

3.4.2 Power Consumption

Table 3.3 reports the maximum power consumption of different building blocks of the proposed low- and high-speed CL-DDS systems, when the systems operate at their maximum speed by producing a TRG signal toggling at twice the pulse width rate (TRG frequency= $1/(2 \times PW_{TRG})$). The power dissipation in the subtractor amplifiers experiences negligible variation over frequency as the systems are clockless and the amplifiers' static power consumption is not affected by the frequency of the comparison operation. The comparator's power, however, varies more with TRG frequency as part of this power is dissipated for the dynamic operation of the output generation whenever the system detects a significant event. Although the power dissipation in the logic gates and buffers also varies with TRG frequency, their contribution to the total power is negligible (less than 1.3%). While most of the power is consumed in the comparator and subtractor amplifiers in the high-speed design, the monostable operation requires about 70% of the total power in the proposed low-speed CL-DDS. This is mainly due to the mechanism of monostable for the generation of TRG pulse based on the delay. As the RC time constant of the delay cells in the monostable has to be increased (by tuning the voltage across the gate-controlled transistor) to generate a wider width of the TRG pulse, an increase in the total power of the monostable is expected at lower frequencies. A time counter or a bank of resistors can be employed instead of delay cells to help reduce the power consumption of monostable at lower frequencies at the cost of design complexity, more occupation area, narrower tuning range, and/or requiring an external clock.

Figure 3.12 plots the overall power consumption of the proposed low- and high-speed CL-DDS measured at different frequencies of the TRG pulse when the systems operate at their maximum activity. This occurs when the monostable of the systems persistently generates an output pulse as the CL-DDS system continuously detects significant events. To achieve this, a high-frequency sawtooth signal with a fast-

Table 3.3: Power distribution in the low- and high-speed CL-DDS systems.

	Power Dissipation / Distribution Percentage					
System	Low-Speed CL-DDS			High-Speed CL-DDS		
TRG Freq.*	1 kHz	10 kHz	200 kHz	0.1 MHz	1 MHz	20 MHz
Comparator	213nW (14.7%)	216nW (15.7%)	233nW (18.8%)	3.9μW (45.4%)	3.97μW (46.6%)	4.25μW (50%)
Amplifiers	161nW (11.1%)	161nW (11.7%)	162nW (13.1%)	3.56μW (41.4%)	3.56μW (41.8%)	3.59μW (42.2%)
Monostable	1.06μW (73.1%)	981nW (71.4%)	830nW (66.8%)	1.11μW (12.9%)	0.95μW (11.2%)	0.6μW (7.1%)
Logic Gates	16nW (1.1%)	16nW (1.2%)	17nW (1.3%)	27nW (0.3%)	35nW (0.4%)	58nW (0.7%)
Total	1.45μW (100%)	1.37μW (100%)	1.24μW (100%)	8.6μW (100%)	8.52μW (100%)	8.5μW (100%)

∗At maximum activity of the system

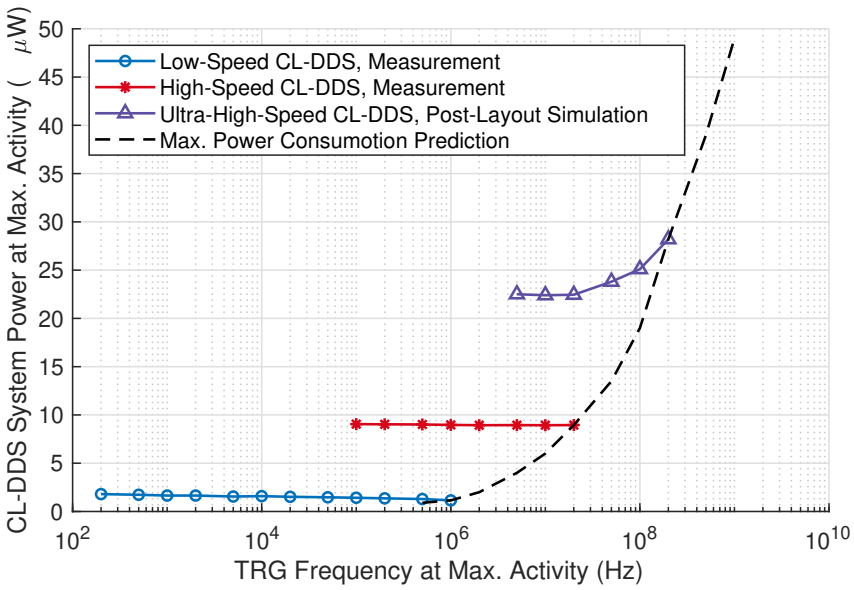


Figure 3.12: Maximum power dissipation of the CL-DDS system vs. TRG frequency at the maximum activity of the system.

changing derivative is applied to the low- and high-speed CL-DDS designs and the comparator window has been narrowed to ensure the nonstop detection of significant events. Note that the power dissipation by the CL-DDS systems is maximized in such

cases as the dynamic power of the system for digital parts and monostable is at a maximum. Accordingly, the maximum power consumption for the low-speed CL-DDS block at its maximum activity is less than 1.7 μW ($VDD = 1V$) over the frequency range of 200 $Hz - 1$ MHz, while for the high-speed design, it is less than 9.1 μW over the frequency range of 100 $kHz - 20$ MHz. In the best case, the maximum overall power consumption is 1.15 μW at 1 MHz and 8.81 μW at 20 MHz for the low- and high-speed CL-DDS systems, respectively. A post-layout simulation result is also depicted for the ultra-high-speed CL-DDS system design to investigate the overall power consumption at higher frequencies as the design is scalable for different frequency ranges. In such a design, as the monostable circuit contribution to the total power is negligible, the increase in the power of the comparator and logic gates over the frequency range would be more noticeable. The maximum overall power is then less than 28.2 μW over the frequency range of 5 MHz-200 MHz. A prediction on the maximum overall power of a CL-DDS design at the end of the covered frequency range is also depicted in Figure 3.12. At a lower frequency range, the monostable circuit's power consumption is dominant, while at a higher frequency range, the dynamic power dissipation of the comparator and logic gates scales linearly with the TRG frequency.

3.4.3 Performance Comparison

Table 3.4 compares the proposed CL-DDS scheme with the state-of-the-art sampling techniques grouped in three major categories of clockless non-uniform, clock-based non-uniform, and uniform sampling methods in terms of power consumption, operation frequency range and resolution bits, among other parameters. The proposed CL-DDS accepts all signal types at the input and the reference thresholds and/or initial R-C delay of the CL-DDS system can be tuned accordingly to obtain a desired accuracy (PR-SNDR). Unlike most of the other works reported in Table 3.4, the CL-DDS system is completely isolated from the ADC sampling path, and hence it does

not further degrade the SNR during the decision-making process, so it can be used with available ADCs. The resolution of the CL-DDS system is determined by the accompanied ADC resolution bit, which is 8-bit in this particular test bench. The speed of the proposed CL-DDS system can be scaled in design by increasing the speed/current consumption of its building blocks to cover higher frequency applications as the implemented scheme produces an ADC trigger pulse signal by itself without requiring any external clock. For low-frequency applications, the proposed low-speed CL-DDS system accepts frequency contents up to 100 kHz, which exceeds the requirements of many sensors/devices. On the other hand, the other reported clock-based and clockless systems with approximately the same or more power consumption can operate up to a few kilohertz. The input signal of the proposed high-speed CL-DDS system can comprise up to 5 MHz frequency content, suitable for applications such as biomedical ultrasound, while the overall power consumption is remarkably less than the other reported work in the same frequency range. As NUS schemes are signal-dependent, case-specific power consumption is reported in Table 3.4 where for each case, the signal type, the number of sampled points, and the achieved PR-SNDR along with the power consumption are compared. For the ECG signal case with an average sampling rate of 53 Samples/s and 28 dB PR-SNDR, a power of 1.45 μW has been consumed by the proposed low-speed design. In comparison, [**NUS˙Had**] requires more sampled points (160 Samples/s) and more power consumption (1.7 μW) to achieve the same accuracy for an ECG signal, with lower bandwidth and higher resolution bits. Similarly, [15] and [42] achieve comparable and higher PR-SNDR with lower power consumption, but at the expense of many more sampled points. The structure in [45] achieves a lower power consumption but with limited resolution bits and bandwidth (6 bits and 1 kHz, respectively). The DSP-level compression techniques implemented in [43] and [22] degraded the overall power consumption compared to analog NUS techniques.

Table 3.4: Performance comparison with the prior state of the arts.

	Clockless Non-uniform				**Clock-based Non-uniform**				**Uniform**	
	This Work		**[45]**	**[35]**	**[NUS'Had]**	**[15]**	**[42]**	**[46]**	**[22]**	**[43]**
Topology	CL-DDS		CL-LC	CL-LC	CB-SDS	CB-DDS	CB-LC	CB-LC	Data CS	CS-AFE
Implementation	Analog		Analog	Analog	Analog	Analog	Analog	Analog	Digital	Analog
CMOS Technology	0.13-μm		0.18-μm	0.13-μm	0.18-μm	0.13-μm	0.35-μm	28-nm	65-nm	0.13-μm
Voltage Supply	1V		0.5V	0.8V	1.8V	1V	1.8-2.4V	1V	1V	0.9V
Input signal Type	All		All	All	All	All	All	All	Bio-Signals	Bio-Signals
Isolation from ADC Sampling	Yes		No	No	No	Yes	No	No	N/A	N/A
Resolution Bits	8[a]		5.6[b]	8	12[a]	12[a]	8	8.5[b]	10	10
Reconstruction Interpolation	1st Order		1st Order	N/A	1st Order	1st Order	3rd Order	1st Order	N/A	1st Order
Application Freq.	Low Freq.	High Freq.	Low Freq.	Low Freq.	Low Freq.	Low Freq.	Low Freq.	High Freq.	Low Freq.	Low Freq.
ADC Trigger/Clock Freq.	Up to 1 MHz	Up to 20 MHz	N/A	N/A	Up to 50 kHz	Up to 100 kHz	Up to 1 MHz	N/A	N/A	N/A
Max. Input Freq.	100 kHz	5 MHz	1 kHz	20 kHz	~5 kHz	~5 kHz	1 kHz	1.78 MHz	N/A	N/A
Power Consumption	1.45μW (ECG, 53 S/s ~28dB PR-SNDR)	23.6μW (Two-tone 0.3+1MHz, 7.5 S/μs ~31dB PR-SNDR)	0.22μW (1 kHz Sinewave, <35dB PR-SNDR)	5μW (1 kHz Sinewave, ~47dB PR-SNDR)	1.7μW (ECG, ~160 S/s ~28dB PR-SNDR)	0.58μW (ECG, ~160 S/s ~28dB PR-SNDR)	0.6-2μW (ECG, >500 S/s 37-48dB PR-SNDR)	410μW (1.78 MHz Sinewave, <48dB PR-SNDR)	170μW (ECG @256 Hz S.R.)	1.8μW (ECG @2 kHz S.R.)

[a]Determined by the accompanied ADC resolution bits and may vary accordingly, [b] Reported ENOB

3.5 Summary

In this chapter, a power-efficient clockless derivative-dependent sampling (CL-DDS) scheme for low- and high-frequency applications has been proposed. The proposed scheme generalizes the mechanism of the prior clockless level crossing techniques to an advanced derivative-dependent scheme that introduces a more power-efficient method of sampling while maintaining signal accuracy after reconstruction. The proposed CL-DDS scheme has been implemented in low- and high-speed systems using several analog low-power circuit techniques and fabricated in TSMC's 0.13 μm CMOS technology and its efficacy has been proven by the obtained experimental results from the real-world signals. The proposed system can be tuned by controlling reference thresholds to obtain a targeted accuracy after the reconstruction. The maximum power consumption of the CL-DDS at its maximum activity is 1.15 μW (@1 MHz) and 8.81 μW (@20 MHz) for the low- and high-speed design, respectively. Employing the proposed scheme in data acquisition systems reduces their overall power dissipation by minimizing the number of sample points that need to be stored, processed, and transmitted.

Chapter 4

A Comparative Study of Non-Uniform Sampling Schemes

Classified into two major categories of clock-based and clockless methods, prior NUS schemes have defined various significant events and have implemented them with analog circuits in different structures; the lack of a comprehensive study on the different NUS schemes and their implementations makes selecting suitable one for a given application more challenging. There are design considerations and non-idealities that need to be investigated so that a pragmatic application can be achieved. The primary objectives of this detailed review study are to introduce various NUS schemes and their suggested implementations, to discuss NUS scheme design considerations, and ultimately, to compare their performance in terms of the most important parameters such as power consumption, signal reconstruction accuracy, signal frequency coverage, design complexity, cost, etc.

4.1 Clockless NUS Techniques

A clockless NUS scheme continuously monitors the input signal to find out a significant event. Since a clockless NUS scheme does not require any initial sampling because the points detected as significant events are not necessarily located at integer multiples of a fixed interval. This frame-less sampling allows tracking significant events in the signal even if the time distance between two successive significant events

is extremely short, *i.e.,* when the signal comprises high-frequency contents. The only limitation becomes the speed of the analog circuits; the shorter the time interval between two successive significant events, the higher the required speed, and the higher the power consumption of the NUS system. The following subsections introduce some of the conventional and state-of-the-art clockless NUS schemes.

4.1.1 Clockless Level Crossing (CL-LC)

The conventional Clockless Level Crossing (CL-LC) scheme continuously compares the signal voltage level to a set of predefined reference levels so that a significant event is defined as the signal crossing one of these levels. Assuming the current level of the input signal is $v_i(t)$ and that it moves between the two reference levels of $V_{r,n}$ and $V_{r,n+1}$, a significant event occurs at the time t where one of the below conditions are satisfied

$$\begin{cases} v_i(t) \leq V_{r,n}, \\ v_i(t) \geq V_{r,n+1} = V_{r,n} + V_q, \end{cases} \tag{4.1}$$

where V_q is the distance between every two levels considered constant in a conventional CL-LC and is called the quantization step. Figure 4.1(a) shows an arbitrary signal where a conventional CL-LC scheme is applied and a set of significant events have been detected at the crossing points. As expected, more significant events are detected in the fast-moving parts of the signal while the inactive parts of the signal comprise fewer significant events, and thus, are less dense. This makes the CL-LC scheme a suitable candidate for signals with long silence periods with minimal activity, such as ECG, PPG, and other bio-signals. The accuracy of a CL-LC is dependent on the number of reference levels, called resolution bits. Although a higher number of resolution bits helps to achieve better accuracy, it may also result in a higher power consumption. The signal can be reconstructed at the receiver side using simple zero-order hold reconstruction, linear or higher-order interpolation techniques, depending on the required reconstruction accuracy, and power budget at the receiver side. For

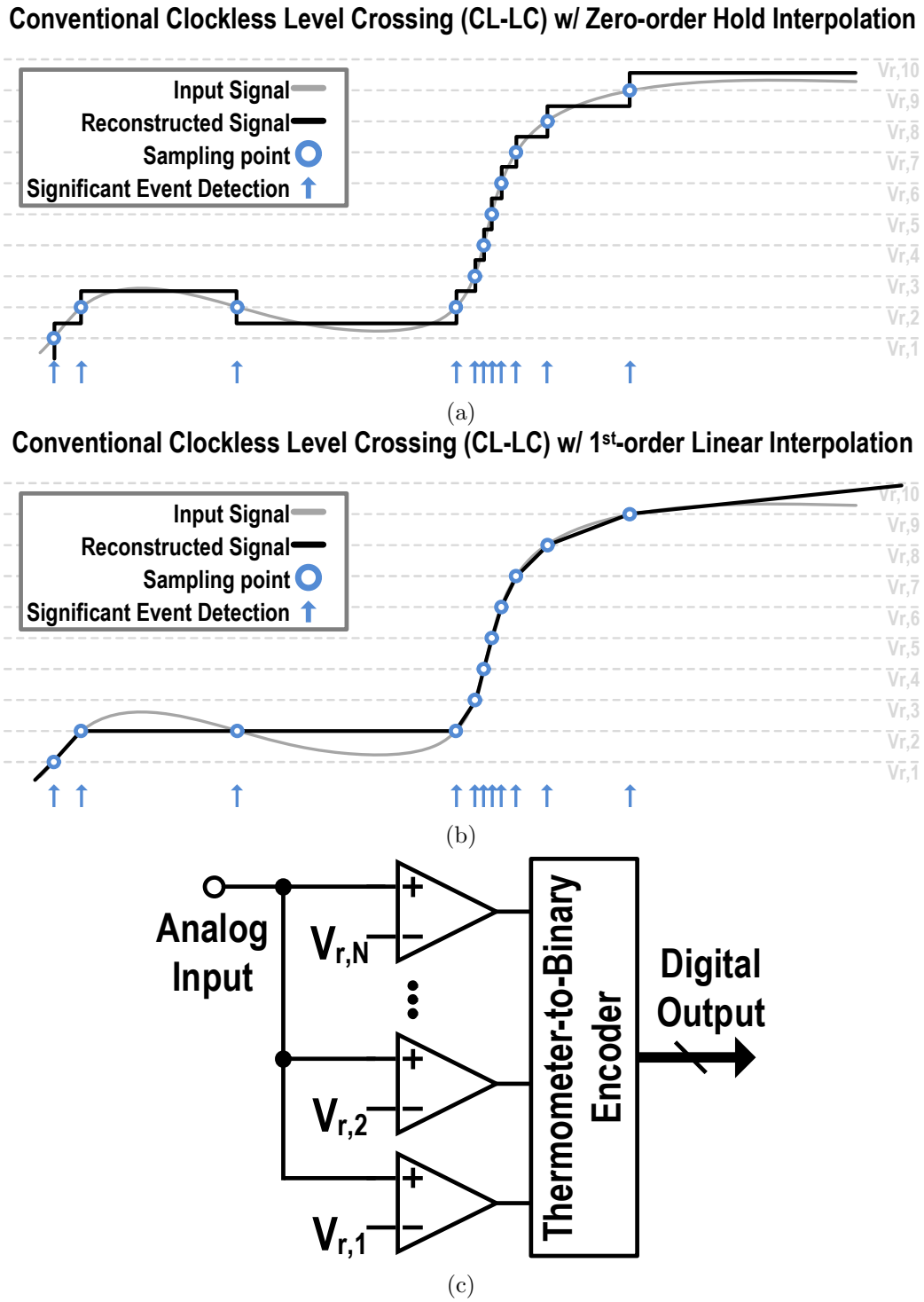


Figure 4.1: An arbitrary signal sampled by conventional (CL-LC) method and reconstructed with (a) zero-order hold, and (b) first-order linear interpolation techniques. (c) a conventional implementation of CL-LC with parallel N comparators and fixed references (Topology I CL-LC).

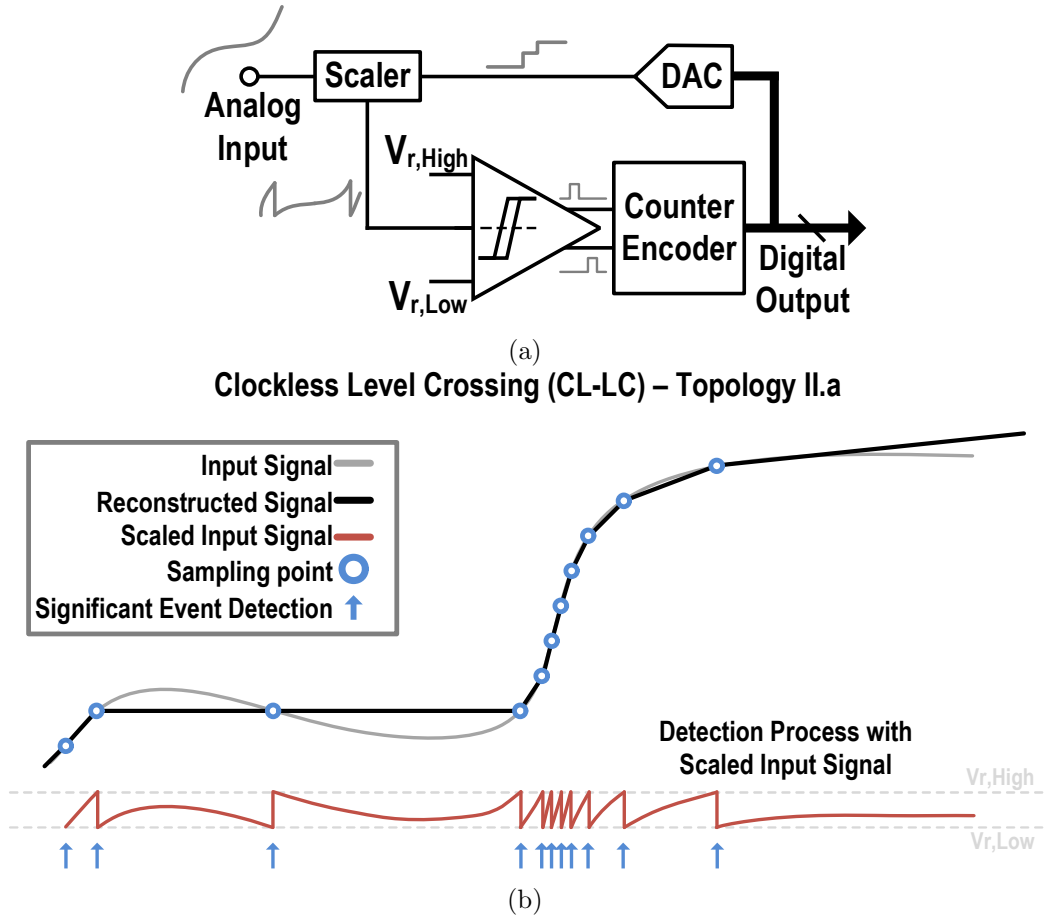


Figure 4.2: (a) Implementation of CL-LC with two comparators and fixed references (Topology II.a CL-LC). (b) An arbitrary signal sampled by CL-LC scheme through Topology II.a detection process.

the systems with a limited power budget at the receiver side, such as biomedical sensors/actuators, the zero-order hold technique shown in Figure 4.1(a) might be a better option as it requires the lowest power consumption [39]. If higher accuracy is targeted, a first-order linear interpolation illustrated in Figure 4.1(b) can result in better accuracy in most signal cases. A higher PR-SNDR can be obtained using a higher-order interpolation; a third-order cubic interpolation, for example, would result in less error in most cases using the same set of sampled points. However, to be consistent, the first-order linear interpolation is used for the reconstruction of all signals in the rest of this study.

A typical implementation of conventional CL-LC is shown as Topology I in Fig-

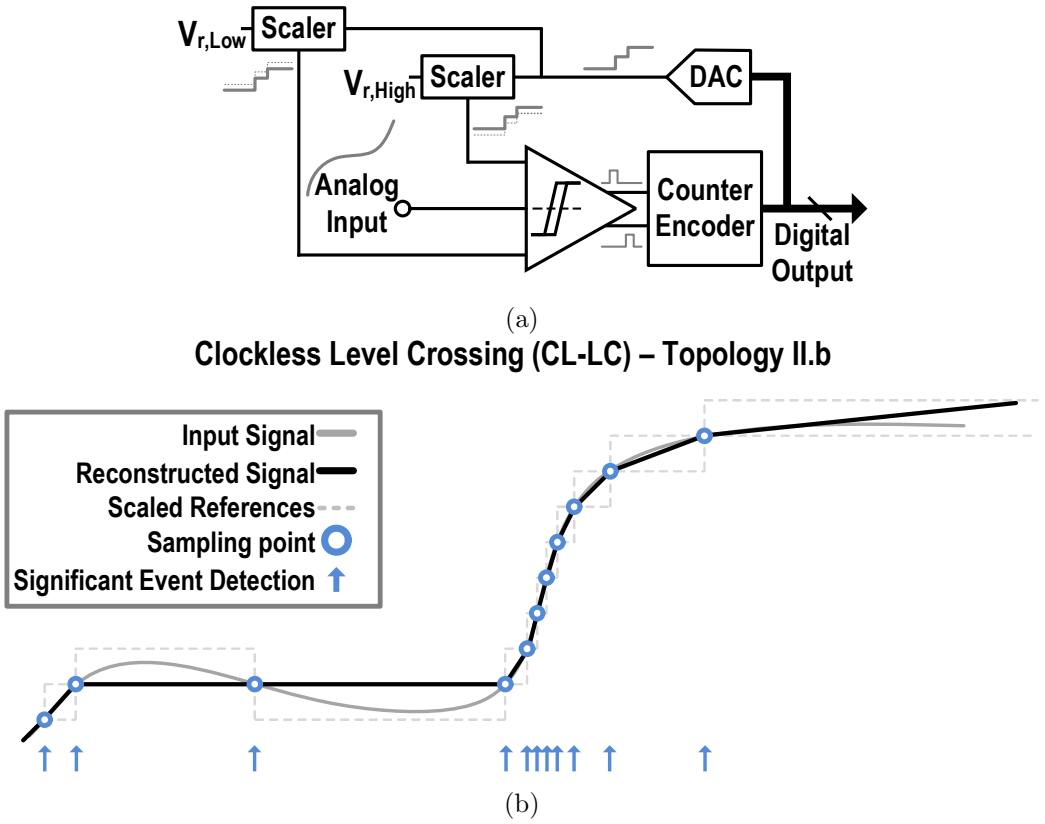


Figure 4.3: (a) Implementation of CL-LC with two comparators and scaled references (Topology II.b CL-LC). (b) An arbitrary signal sampled by CL-LC scheme through Topology II.b detection process.

ure 4.1(c), which represents an asynchronous conventional flash ADC [47–50]. In this topology, each fixed reference level, generated by a resistor divider, is connected to a comparator to be compared to the input signal followed by a thermometric to binary converter stage. Any change in the output of the comparators is considered a significant event. The simplicity of topology I design leads to an advantage where the fixed reference levels and the input signal are independent of the output and thus less vulnerable to errors due to feedback loops or any additional building blocks required for making a decision. Although this makes the structure robust, the high power consumption by the comparators used for each reference line makes employing them less reasonable, especially when the bit resolution is high.

Implementation of CL-LC with Topology II.a, shown in Figure 4.2(a), may solve

this issue by using only a single window comparator [37, 51, 52]. In this topology, a Digital-to-Analog Converter (DAC) converts the last/present digital output to analog and is subtracted from the input signal voltage. The resulting difference value is then compared to the reference thresholds of the window comparator so that whenever it crosses the upper or the lower reference the output counter will add up or subtract the output by one, respectively. Figure 4.2(b) illustrates the detection process through CL-LC with Topology II.a, where the scaled input is now compared to fixed references; however, the reconstructed signal is the same as shown in Figure 4.1(b) since the scheme mechanism does not change with the implementation.

Although Topology II.a can save significant power consumption compared to Topology I, scaling the input signal up/down could cause a changing offset. This issue is more noticeable when the signal is closer to the voltage boundaries or when the signal contains high-frequency contents such as noise. Topology II.b, illustrated in Figure 4.3(a), solves the offset issue by scaling the references of the window comparator up/down instead of the input signal [35, 53]. Additionally, the generated references can be calibrated to compensate for the resulting offset after the scaler. Yet, the topology is still vulnerable to input signal noise or high-frequency contents because both topologies II.a and II.b are considerably impacted by the performance of the DAC and scalers which play the principal role in the resulting accuracy of reconstruction. Figure 4.3(b) depicts the detection process by Topology II.b implementation of CL-LC, where the references are scaled at every significant event. The reconstructed signal is still the same as Figure 4.1(b) and Figure 4.2(b), as the difference is only in implementation and not the mechanism. There are multiple additional topologies for implementing the conventional CL-LC scheme proposed and discussed in the literature. However, the proposed modifications in these topologies do not alter the definition of significant events discussed earlier.

4.1.2 Clockless Adaptive Level Crossing (CL-ALC)

The Clockless Adaptive Level Crossing (CL-ALC) scheme implements a similar mechanism and definition of the significant event as conventional CL-LC except that the reference levels are adaptively redefined during the process [35, 38]. In other words, while in a conventional CL-LC the comparator(s) window size is consistently fixed and set to a quantization step (V_q), in a CL-ALC it is adaptively varying over time. Figure 4.4 illustrates an example case where a set of significant events are detected by a CL-ALC applied to an arbitrary signal. In this example, the comparator window size is adaptively set to three values; it is first set to $5V_q$, and if there is no significant event in a pre-fixed period (denoted by τ_d) it is adjusted to $3V_q$. If no significant event is detected in another period of τ_d, it is eventually set to V_q indefinitely until a significant event is detected so that the procedure is reset. Accordingly, in the fast-moving parts of the signal, the CL-ALC detects less significant events compared to a conventional CL-LC. This improves the scheme's ability to track the signal and the overall power consumption as the signal can now be reconstructed with fewer sampled points. A significant event in this example of CL-ALC can be mathematically represented as

$$\begin{cases} |v_{in}(t) - V_{out,L}| \leq 5V_q/2 & t - t_{out,L} \leq \tau_d \\ |v_{in}(t) - V_{out,L}| \leq 3V_q/2 & \tau_d < t - t_{out,L} \leq 2\tau_d \\ |v_{in}(t) - V_{out,L}| \leq V_q/2 & 2\tau_d < t - t_{out,L} \end{cases} \tag{4.2}$$

where $V_{out,L}$ is the latest output voltage level retained at the moment of the last significant event, $t_{out,L}$. The adaptive reference values can also be adjusted to arbitrary values depending on the application and the signal and do not necessarily need to be a multiple of the quantization step. The adaptive references can be also set unbalanced; in the proposed implementation in [35], the upper reference, $V_{r,High}$ is larger than the lower reference, $V_{r,Low}$, for rising segments of the signal, and vice versa for the falling segments of the signal.

Figure 4.4(b) depicts one possible circuitry for CL-ALC block that implements the

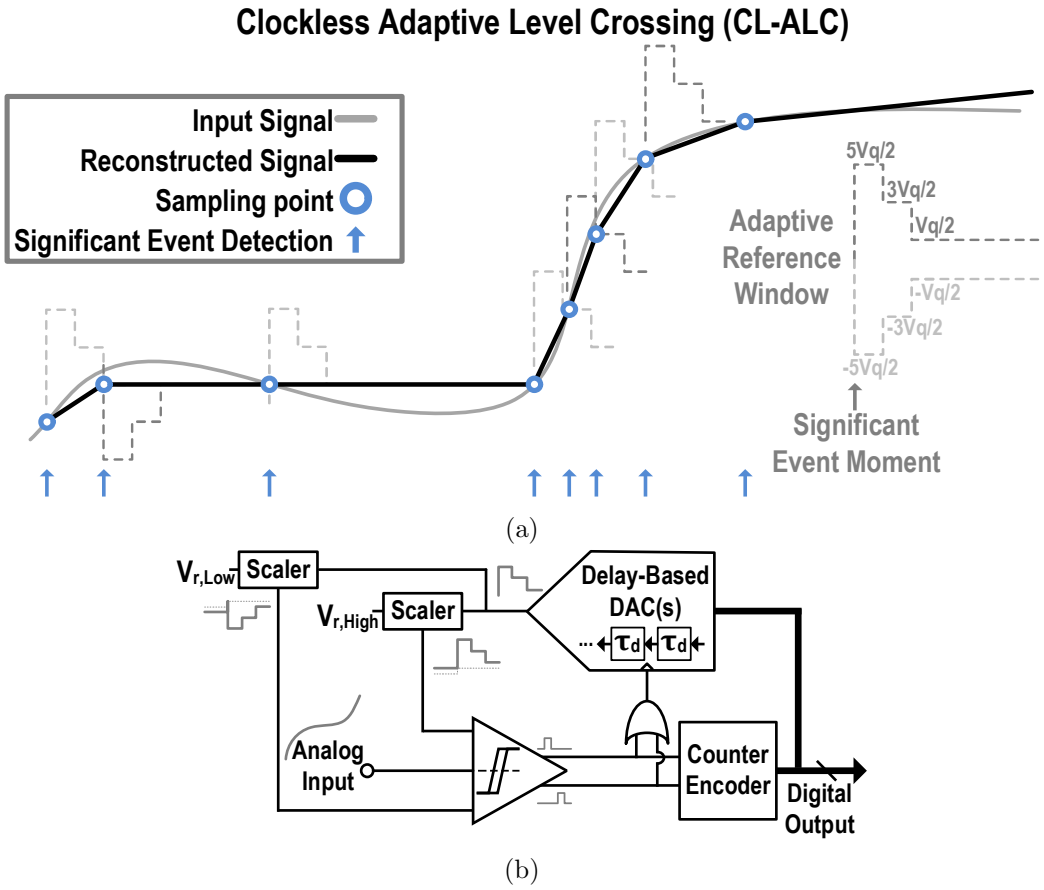


Figure 4.4: (a) An arbitrary signal sampled by a CL-ALC scheme. (b) An implementation example of CL-ALC.

example scheme shown in Figure 4.4(a) [35, 38]. This example topology is a modified version of Topology II.b of the conventional CL-LC (Figure 4.3(a)), where the delay-based DAC(s) is reset by the comparator whenever a significant event is detected and generates an adaptive staircase approximation signal to be added/subtracted to the current level of references. This provides the comparator with an adaptive reference that levels down from $5V_q$ to V_q after $2\tau_d$. The CL-ALC structure presented Figure 4.4(b) suffers from the same limitations of Topology II.b in conventional CL-LC, therefore, an accuracy degradation is expected due to the presence of signal noise or high-frequency contents. The resolution controller required for generating the adaptive reference level also increases the power consumption and complexity. Nonetheless, as mentioned earlier, the number of detected significant events is typically lower than

the conventional CL-LC, which helps save the power consumption by the overall data acquisition system.

4.1.3 Clockless Derivative Level Crossing (CL-DLC)

The Clockless Derivative Level Crossing (CL-DLC) scheme, shown in Figure 4.5(a), incorporates a zero-order hold conventional CL-LC as the core block, where its input is the derivative of the input signal (rather than the original signal itself) and its output is applied to an integrator to reverse for the differentiation [39]. Therefore, the condition for a significant event in a CL-DLC is similar to Equation (4.1) and is defined as follows:

$$\begin{cases} D_i(t) \leq V_{r,n}, \\ D_i(t) \geq V_{r,n+1} = V_{r,n} + V_q, \end{cases} \tag{4.3}$$

where $D_i(t)$ represents the instantaneous derivative of the signal. The integration step at the ending stage of this scheme achieves a first-order reconstruction of the signal without using computationally intensive reconstruction techniques. This is due to the fact that an integration of a staircase signal, such as the zero-order reconstruction of the signal derivative in this scheme, results in a ramp signal. This considerably relieves the power-consuming reconstruction step at the receiver side. Hence, the CL-DLC technique principally targets applications where the receiver side suffers from an extremely limited power budget [39]. Note that similar to the prior technique, the CL-DLC can be modified to CL-ADLC if a resolution controller is added to the topology to make its resolution adaptive. The controller presented in [39] tunes the resolution based on the activity of second-order derivation (Figure 4.5(b)); however, it can be done through different methods.

A set of simulation results using Matlab software tools have been presented in [39] to show the superiority of CL-DLC and CL-ADLC schemes over the conventional CL-LC with a zero-order hold reconstruction. However, the lack of implementation at the analog circuit level makes a fair comparison more difficult. As a fact, the CL-DLC

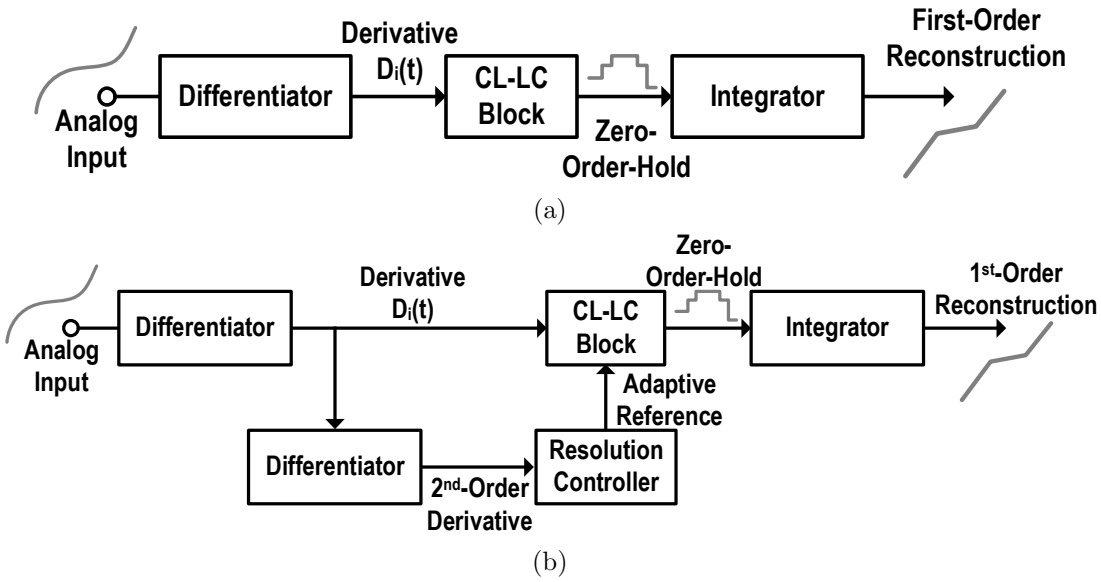


Figure 4.5: (a) Diagram of CL-DLC scheme with a CL-LC as the core block.(b) Diagram of CL-ADLC with adaptive resolution.

and CL-ADLC schemes rely on power-consuming analog building blocks, like the differentiator and the integrator, which may limit these schemes to specific applications. Moreover, other challenges associated with analog differentiators and integrators raise concerns about the feasibility, such as the signal cases with sharp/fast-moving segments which could suffer from saturation, unless a high voltage headroom and high power consumption are considered in the design. Furthermore, according to the simulation results presented in [39], the conventional CL-LC achieves better reconstruction accuracy than CL-DLC at lower frequencies.

4.1.4 Clockless Multi-Dimensional Level-Crossing (CL-MDLC)

The conventional CL-LC and its modified versions introduced above track the input signal only in the horizontal direction. A generalized method introduced and discussed in Chapter 3 of this research is Clockless Multi-Dimensional Level-Crossing (CL-MDLC), where sloped reference levels are defined depending on the derivative of the signal at the last retained sample rather than level with horizontal constant slopes. Compared to conventional CL-LC, this scheme reduces the number of required

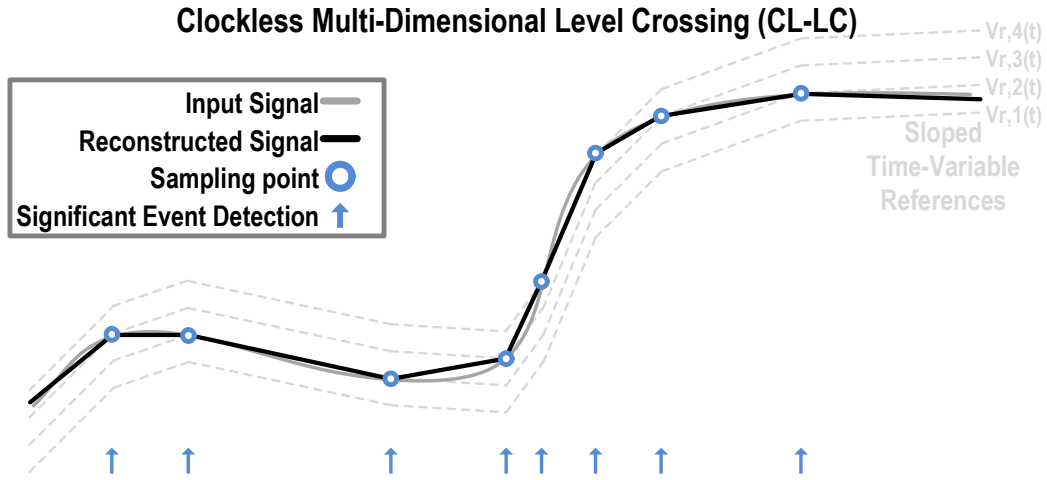


Figure 4.6: The process of significant event detection by CL-MDLC applied to an arbitrary signal.

sampled points to achieve the same accuracy and process high-frequency better. The advantage of this method is based on the fact that in first-order interpolation the reconstructed signal is formed from sloped straight lines between each two retained samples. Figure 4.6 illustrates an example case where the CL-MDLC scheme is applied to an arbitrary signal and a set of significant events are detected when the signal crosses the sloped reference levels. If the current voltage level, $v_{in}(t)$, lies between the $(n)^{\text{th}}$ and $(n+1)^{\text{th}}$ sloped reference lines, $V_{r,n}(t_0)$ and $V_{r,n+1}(t_0)$, respectively, a significant event in a CL-MDLC can be then mathematically defined as

$$\begin{cases} v_i(t) \leq V_{r,n}(t) = V_{r,n}(t_0) + D(t_0) \times (t - t_0), \\ v_i(t) \geq V_{r,n+1}(t) = V_{r,n}(t_0) + D(t_0) \times (t - t_0) + V_q / \sqrt{1/(1 + D^2(t_0))}, \end{cases} \tag{4.4}$$

where t_0 is the last significant event moment where the slope of references is renewed with a value of $D(t_0)$. As Equation (4.4) suggests, the reference levels and the quantization step, $V_q/\sqrt{1/\left(1+D^2(t_0)\right)}$, are no longer constant and vary with time and the slope of the reference levels. These would make an analog implementation for the CL-MDLC highly challenging and impractical as it requires a complex analog circuitry with high power consumption that realizes the variable parameters. However, this can be accomplished by a DSP after conversion. For example, reference [54] has implemented a scheme similar to CL-MDLC, called slope level-crossing, at the DSP

using Field-Programmable Gate Array (FPGA) and targeted low-frequency applications, such as wearable biomedical applications. The DSP-level implementations of NUS schemes are discussed in more detail in Section 4.2.4.

4.1.5 Clockless Derivative Dependent Sampling (CL-DDS)

A Clockless Derivative Dependent Sampling (CL-DDS) (proposed in Chapter 3 as part of this research) defines a significant event as a significant change in the current derivative of the signal compared to the last-retained derivative. If the current and the last-retained derivative of the input signal are $D_i(t)$ and $D_i(t_l)$, then a significant event in a CL-DDS can be expressed as

$$|D_i(t) - D_i(t_l)| \geq V_R, \tag{4.5}$$

where V_R is the scheme resolution that identifies a significant event. Figure 4.7(a) illustrates an example case where CL-DDS is applied to an arbitrary signal. Note that the resolution could be tuned to detect more significant events, thereby increasing accuracy. Figure 4.7(b) shows an ideal topology for the implementation of CL-DDS where a differentiator takes the derivative of the signal, and then a subtractor provides the comparator with the difference of the current and last-retained derivative. Whenever the comparator output changes to high, *i.e.,* if a significant event is detected, the monostable generates a single pulse with tunable width that triggers the ADC to sample the signal. The monostable output also enables the sample-and-hold circuit to replace the last-retained derivative of the signal with a new one.

Although using an analog differentiator would output an accurate value for the derivative, implementing one might be challenging, particularly with a wide bandwidth and low power consumption. A practical alternative to analog differentiator is an approximation derivative which can be implemented using a subtractor and a delay circuit. If this delay circuit provides a delay of Δt and the voltage gains of

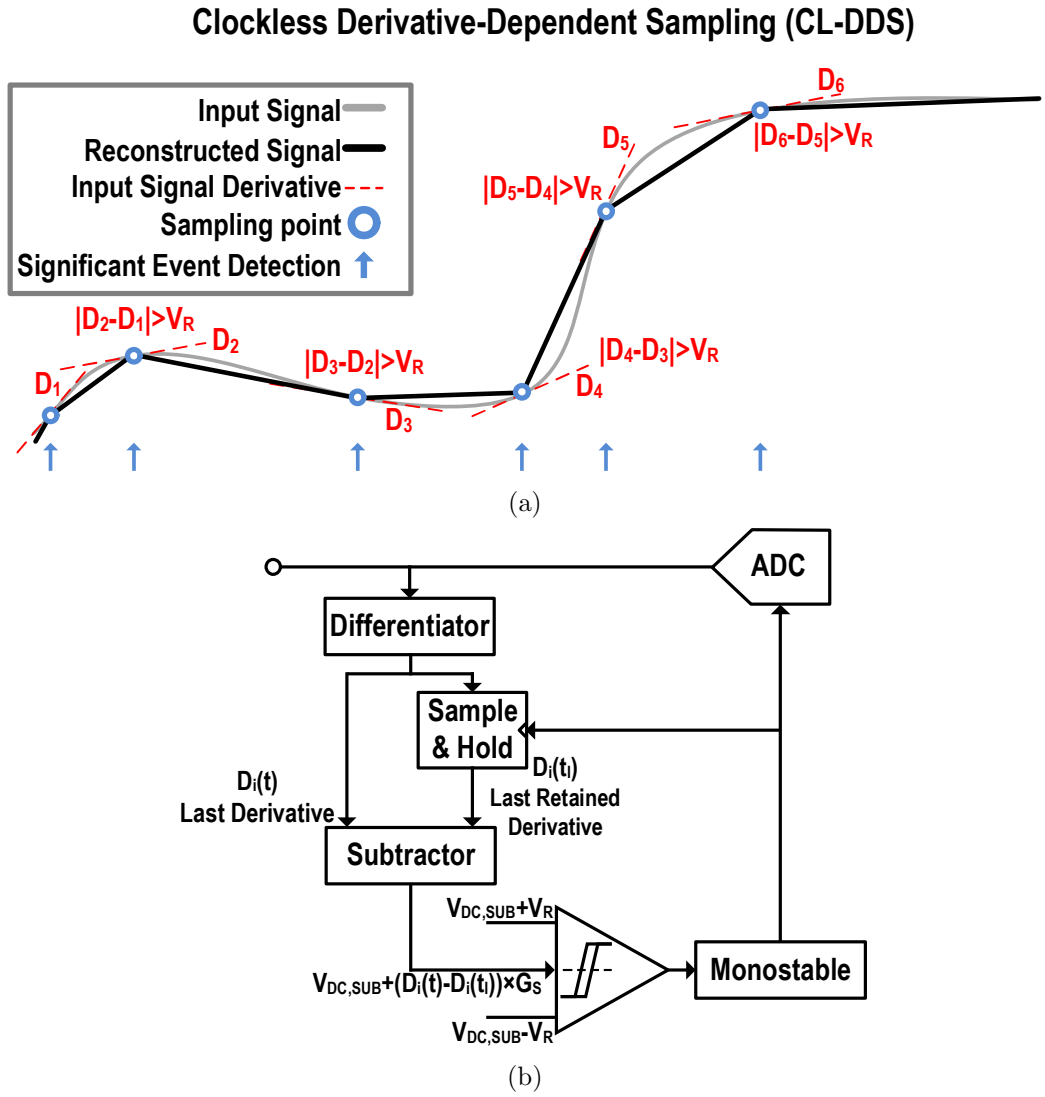


Figure 4.7: (a) An arbitrary signal applied to the CL-DDS scheme. (b) An ideal implementation of CL-DDS with an analog differentiator.

subtractors are G_1 and $G2$, thus Equation (4.5) can be written as

$$\left|\frac{v_i(t)-v_i(t-\Delta t)}{\Delta t}-\frac{v_i(t_l)-v_i(t_l-\Delta t)}{\Delta t}\right| \geq \frac{V_R}{G_1 G_2 \Delta t}, \tag{4.6}$$

where the left-hand side represents $|D_i(t) - D_i(t_l)|$ and the right-hand side is the scheme resolution. Although this approximate derivative facilitates the implementation of a low-power differentiator, it may cause either an accuracy reduction or misdetection of significant events. Since the required delay varies for different frequency ranges, the approximation derivative might be considerably inaccurate for

signals with a wide frequency spectrum, *e.g.,* when the signal comprises high- and low-frequency components simultaneously. However, this might not be an issue for many applications, such as biomedical sensors, where the frequency spectrum is sufficiently close.

4.2 Clock-based NUS Techniques

The clock-based NUS schemes detect significant events in a set of initial sampling points and retain them as valuable points while dropping non-significant event points. This means that the mathematical relations defined for the significant events are in the discrete domain in clock-based NUS schemes, therefore, these schemes provide discrete monitoring of the signal. As discussed in the introduction section, the discrete monitoring of clock-based schemes inherently presents lower efficacy in processing high-frequency contents compared to clockless schemes. The linear increment of power in the clock-based NUS schemes is a special concern that limits the applications at lower frequencies. The need for an external clock, and non-idealities associated with clock management, such as offset due to clock feedthrough and on-resistance, are other concerns in designing a clock-based scheme.

The synchronization with a clock, however, benefits an NUS scheme in two principal ways: (a) the building blocks can operate in a small portion of the clock period, as shown in Figure 1.3(d), which helps save substantial power, and (b) it eases the reconstruction of the signal, as the digitized values of the signal level at significant events and the number of silent clock cycles between each two significant events are sufficient for reconstruction. The former makes an NUS scheme ultra-low-power consumption for low-frequency applications, achieving a level of power efficiency that a clockless scheme cannot achieve, for example, [14] and [15] consume a few nanowatts for operation at sub-kilohertz frequencies. The latter is beneficial when implementing an asynchronous data acquisition system is infeasible, such as in wireless sensor systems where the receiver requires synchronization and time information to reconstruct

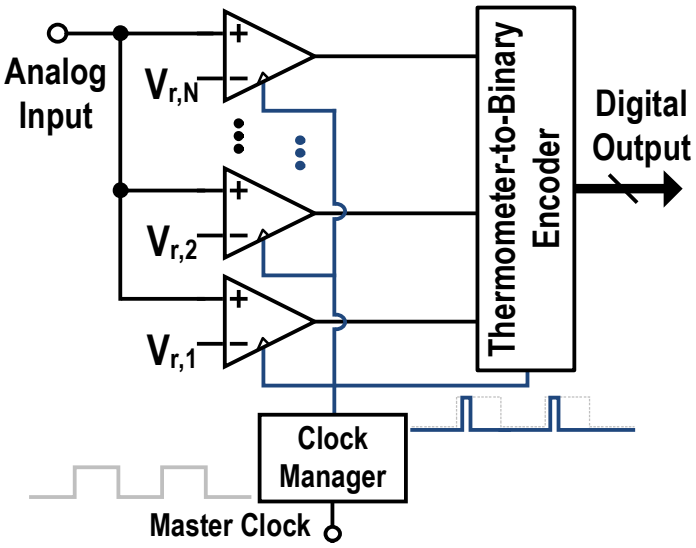
the signal.

Some of the clockless NUS schemes introduced in the previous section might be easily converted to clock-based schemes using the structure shown in Figure 1.3(d). For example, Figure 4.8(a) illustrates some modifications applied to the conventional CL-LC Topology I shows in Figure 4.1(c) to synchronize it with an external clock and implement a conventional CB-LC structure Topology I. Adding a sample-and-hold circuit operating with the clock and applying appropriate enabling switches to the comparators are sufficient for this example. Similar to Equation (4.1), a significant event in a conventional CB-LC scheme can be defined as

$$\begin{cases} v_i[m] \leq V_{r,n}, \\ v_i[m] \geq V_{r,n+1} = V_{r,n} + V_q, \end{cases} \tag{4.7}$$

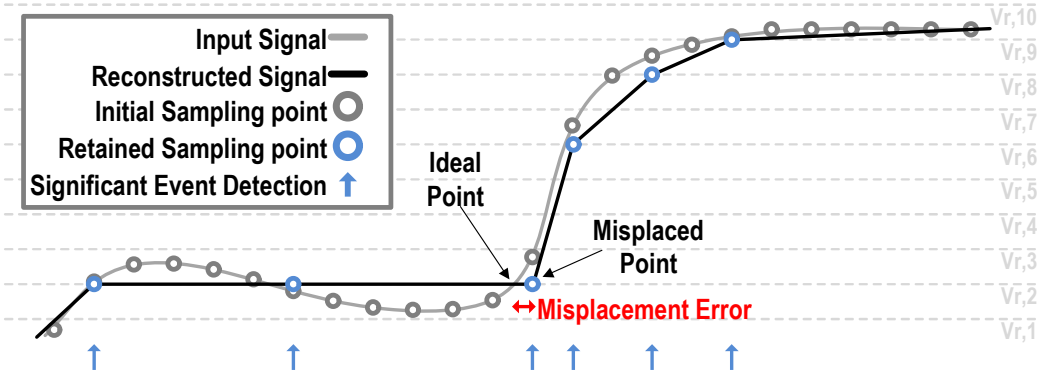
where $v_i[m]$ is the input signal level in discrete domain. Figure 4.8(b) shows an example similar to Figure 4.1(b) where the signal and the reference levels are the same, however, since a CB-LC is applied to the signal the significant events are placed at different locations from the locations of the clockless scheme. In several cases shown in Figure 4.8(b), the placement of retained points differs from the crossing-level point. This would reduce the accuracy of the reconstruction as the sampled points no longer coincide with the instants when the signal crosses the levels. This misplacement of the locations of the retained points also occurs in other clock-based schemes and can be the dominant source of the error unless the master clock of the scheme is sufficiently high, beyond the Nyquist rate or multiple of it, so that these misplacements are rare or negligible. Moreover, aside from the nonidealities discussed in Section 4.1.1, such as offset and noise, the imperfections associated with clock switching would further degrade reconstruction quality. The offset in the initial sampling stage and glitches caused by periodically switching on/off the comparators might add extra noise, resulting in the misdetection of significant events.

Implementation of CB-LC through a clock-based structure similar to Topology II, shown in Figure 4.2(a) and Figure 4.3(a), results in a different scheme than Topology



(a)

Clock-Based Level Crossing (CB-LC)



(b)

Figure 4.8: (a) Adding clock to the blocks of structure depicted in Figure 4.1(c) and building a conventional CB-LC Topology I structure. (b) The process of detection of significant events in a CB-LC scheme with Topology I implementation.

I, shown in Figure 4.1(c). An extra error is expected in such implementation since the up/down counter at the output stage can add/subtract only a single quantization step for each clock cycle this leads to the the scheme lagging behind the signal if more than one reference level is crossed by the signal in one period of the clock. Figure 4.9 illustrates an example signal applied to both conventional CB-LC Topology I and Topology II, where the latter suffers from an extra error as it is unable to track the signal consistently in the fast-moving segments of the signal. Although this

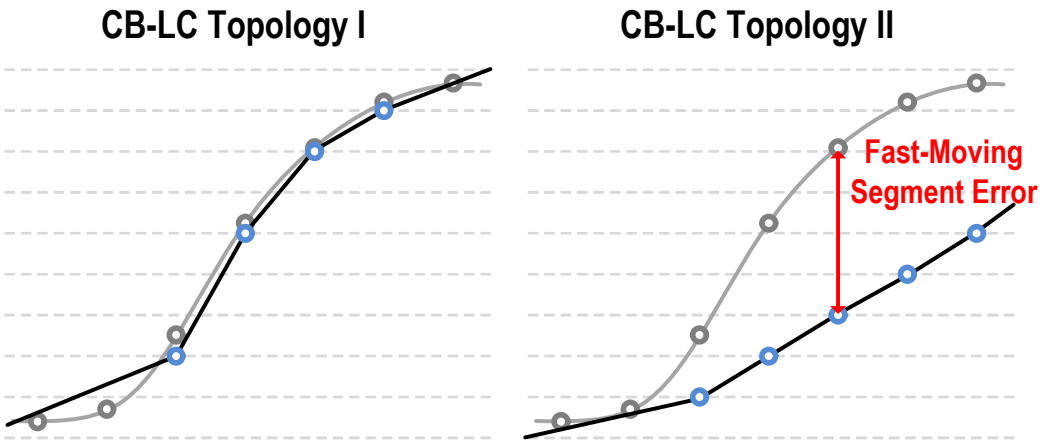


Figure 4.9: An arbitrary signal sampled with CB-LC Topology I and II, and the generation of error due to fast-moving segments of signal with Topology II.

problem can be solved by increasing the clock frequency, it will lead to higher power consumption. Another solution can be using Clock-Based Adaptive Level Crossing (CB-ALC) as it shows better/faster tracking of the signal in fast-moving parts due to using a larger quantization step after detecting a significant event. Recalling the example of adaptive levels discussed in Section 4.1.2, a $5V_q$ quantization step could be enough to follow all rapid changes in the signal value. Moreover, the delay period (τ) required for adjusting the levels can be implemented as integer multiples of the clock period.

4.2.1 Clock-Based Adaptive Rate (CB-AR)

The CB-AR sampling scheme adjusts the sampling frequency of the ADC based on the activity of the signal. In [23], for example, the sampling frequency is set to 1024 Hz for active parts of ECG signal, and it is adjusted to a lower rate of 64 Hz for the inactive parts. A CB-AR can then be considered as an application-specific method since it requires detecting the interesting segments of the signal with the most activity and distinguishing them from non-interesting parts. The analog circuitry that implements this recognition varies for each application. For example, a circuit that detects the R-peaks of an ECG signal can be used to distinguish the active and inactive segments.

However, for applications where the signal is consistently active or the segments of interest are difficult to define, a CB-AR scheme is less practical. In such cases, a DSP-level implementation might be a better option as the power consumption required for complex analog processing exceeds that for uniform sampling plus a DSP.

4.2.2 Clock-Based Slope Dependent Sampling (CB-SDS)

The Clock-Based Slope Dependent Sampling (CB-SDS) calculates two slope values between three sampled points and defines the significant event as the sample where the absolute value of the difference between the two slopes is greater than or equal to a certain threshold[14]. The first slope is calculated between the last two sampled points based on the clock and the second slope is defined between the second-to-last sampled point and the last retained point (the sampled point retained at the most recent significant event). Then a subtractor outputs the difference between these two to be compared to a threshold value. A significant event in a CB-SDS can be expressed as

$$\left|S_{[n],[n-1]}-S_{[n-1],[m]}\right|=\left|\frac{v_i[n]-v_i[n-1]}{T}-\frac{v_i[n-1]-v_i[m]}{(n-m-1)\times T}\right|\geq V_R, \tag{4.8}$$

where $v_i[m]$, $v_i[n-1]$, and $v_i[n]$ represent the last-retained, the second-to-last, and the last sampled points, respectively, T is the sampling period, and V_R is the scheme resolution. Although this complicated relation leads to higher reconstruction accuracy compared to other clock-based techniques [15], it needs relatively complex power-consuming building blocks for implementation. Implementing Equation (4.8) demands an analog divider to calculate the second slope where the denominator of the second term of the equation $n-m-1$ is not a constant value. The implementation of this analog divider is even more challenging at higher frequencies. In [14], A bank of binary switches and a counter are employed to provide an analog current-based division following two trans-conductance amplifiers (Gm cells). Figure 4.10(a) shows an example where the CB-SDS scheme is applied to an arbitrary signal and four

points are detected as significant events. Please note that the reconstructed signal is not shown to provide a clearer representation of the decision process. Section 4.2.2 also illustrates the proposed topology where the ADC receives the input signal after two sampled-and-hold stages whose offsets cause an additional degradation of the SNR before conversion by the ADC. Another source of error is the mismatch between switches that provide analog division which exacerbates at higher frequencies due to digital counter imperfections. Since the CB-SDS scheme requires three previous sampled points to detect a significant event, a decision delay of one clock cycle is inevitable. This would add extra error if the signal contains high-frequency contents or fast-moving parts.

4.2.3 Clock-Based Derivative Dependent Sampling (CB-DDS)

The Clock-Based Derivative Dependent Sampling (CB-DDS) looks for a considerable change in the approximation of the derivative of the signal at the latest sampled point compared to the last-retained one [15]. Figure 4.11(a) shows a proposed implementation for the CB-DDS, where the derivative approximation is obtained through two sampled-and-hold circuits and a following subtractor; one sampled-and-hold block is enabled after a delay of Δt [15]. Considering the targeted low-frequency applications, subtracting the signal from its delay to achieve the relative derivation would be more practical in design than an analog differentiator with static power. Another subtractor provides a difference between the current derivative from the last-retained derivative to be compared with the tunable threshold, V_R, in the next stage. If a significant event is detected, the comparator output changes from low to high, triggering the ADC and enabling the sampled-and-hold block to replace the last-retained derivative. Accordingly, a significant event can be expressed as

$$\left| \frac{v_i[n] - v_{i,\Delta t}[n]}{\Delta t} - \frac{v_i[m] - v_{i,\Delta t}[m]}{\Delta t} \right| \geq V_R, \tag{4.9}$$

where $v_i[m]$, and $v_i[m]$ are the last retained, and the last sampled points, respectively,

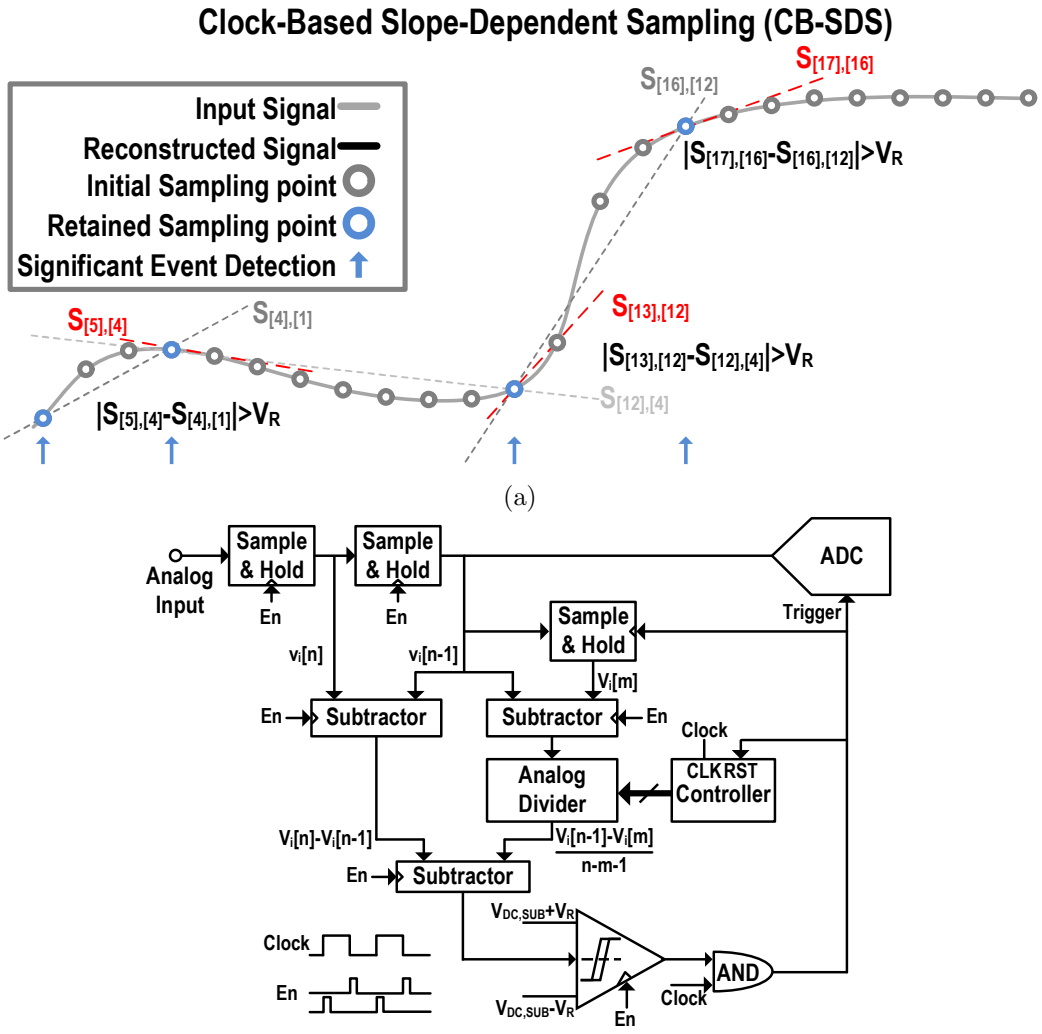


Figure 4.10: (a) An arbitrary signal applied to CB-SDS technique. (b) The proposed implementation of CB-SDS scheme in [14].

and V_R is the scheme resolution value. Note that the amplification gains through subtractors should be added to the above equation; which adds another degree of freedom to the design. Figure 4.11(b) shows an example where the CB-DDS scheme is applied to a signal and 5 points are detected as significant events. Note that by changing the scheme threshold, V_R, or the delay time, Δt, a different set of significant events would be detected.

The CB-DDS scheme presents an accuracy of reconstruction sufficiently close to CB-SDS but with a simpler implementation as an analog divider and three previous

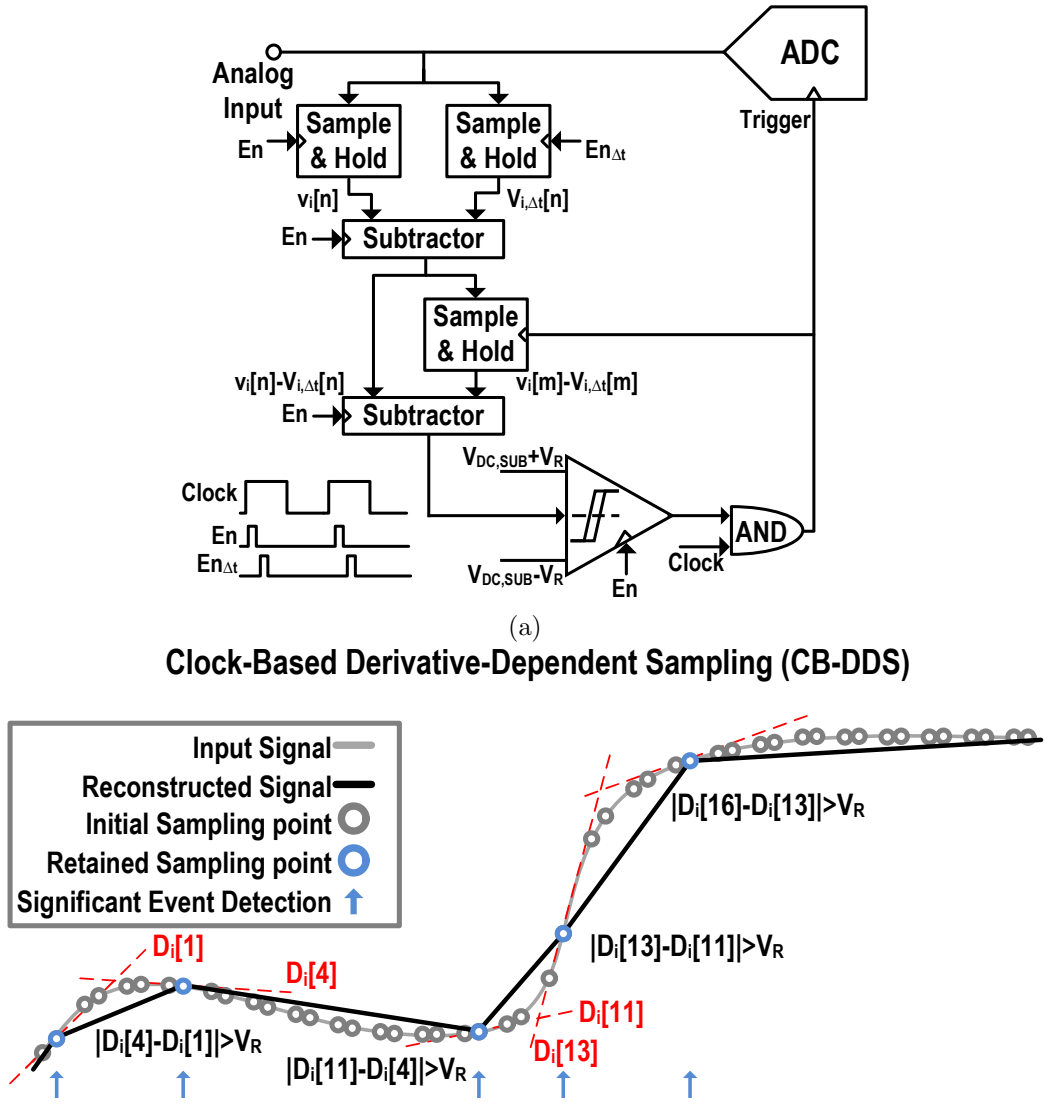


Figure 4.11: The proposed implementation for CB-DDS scheme in [15]. (b) An arbitrary signal sampled with CB-DDS scheme.

sampling points are no longer required [15]. Unlike other clock-based schemes, the ADC receives the input signal directly without interruption. This prohibits further SNR degradation before the conversion stage. However, the limitations of a clocking structure discussed earlier are involved in the CB-DDS scheme as well. This includes offset in sample-and-hold stages, the clock feedthrough, glitches due to blocks switching on/off, etc.

Although adding a clock to CL-DLC and CL-MDLC schemes is possible, the prac-

ticality of the analog circuit implementation of these schemes is questionable. The clock introduces further complexity to the structure, along with the non-idealities associated with a clocking system. Since there is no reported circuit implementation for the clock-based version of these NUS schemes in the literature, even at the simulation level these techniques are not included in this section.

4.2.4 DSP-level NUS Schemes

The NUS schemes can be implemented as part of a Digital Signal Processor (DSP) after conversion by a uniform ADC. By adopting this approach, the advantages of an analog implementation would be diminished; however, it may still have some valuable applications. If the power budget allocated for the data conversion stage (ADC) and the DSP is minor compared to other building blocks of a data acquisition system, a DSP-level implementation of an NUS scheme might achieve a power reduction comparable to its analog implementation. For example, in a wireless ECG monitoring device using a TI-CC2650 micro-controller as reported in [55], the power consumption of analog blocks is negligible; the power consumption is mainly dominated by the RF-core (including Power Amplifier (PA)) and the digital blocks of the microcontroller (including memory, CPU, and clock manager). Therefore, although an NUS scheme can remarkably save the overall power of the device (more than 90%) [55], there is no significant difference between an analog and a DSP implementation of the scheme as both would achieve almost the same level of overall power saving. It should be noted that this does not apply to most low-power data acquisition systems where an analog implementation of a NUS significantly shows better power saving compared to a DSP-level one. Another application of a DSP-level NUS scheme is when a more complex significant event is defined and a complicated mathematical relation is required for implementation. A complex scheme similar to CL-MDLC, for example, has been implemented using an FPGA [54], as discussed in Section 4.1.4.

4.3 Performance Comparison

This section compares the performance of various NUS techniques introduced above in terms of design complexity, power consumption, and accuracy. It also provides qualitative and quantitative analysis of the non-idealities that impact their performance, such as decision delay, offset, noise, etc.

4.3.1 Complexity

Table 4.1 summarizes the introduced NUS schemes in terms of the mathematical relation for a significant event defined for each scheme and the essential building blocks to implement them. The mathematical operations are classified as easy, moderate, and difficult to implement through analog circuitry by the superscripts of 1, 2, and 3, respectively. The analog division, derivation, and integration operations can be considered the most complex operations as they require intricate structures comprising many devices and circuits. In general, clock-based schemes have more complex structures than clockless schemes as they require an external clock and a clock manager, although they may reach a lower power consumption for the NUS scheme at low-frequency applications and ease the post-reconstruction at the reader side with a power-efficient synchronous mechanism.

Among the schemes presented in Table 4.1, the Topology I implementation for conventional CL-LC and CB-LC schemes has the least required operations where a comparison with fixed reference levels is sufficient to detect a significant event. However, depending on the targeted accuracy (resolution bits), the number of comparators increases exponentially, making the scheme less efficient regarding power consumption, and occupation area. Topology II implementation for level-crossing schemes solves this issue, although it adds complexity to the design. The derivative-based schemes, CL-DLC, CL-DDS, CB-AR, and CB-DDS, increase the design complexity by adding the derivative to the mathematical expression defined for a significant

event. The CL-DLC represents the highest complexity in design with higher required power consumption as an analog differentiator and integrator are both essential to implement the scheme. The CL-DDS and CB-DDS reduce the complexity by applying a derivative approximation using a delay plus subtraction at the cost of reducing the bandwidth and accuracy of reconstruction. The analog division operation is also considered complex to implement and has to be derived through a bank of switches (resistors) and trans-conductance amplifiers.

4.3.2 Power Consumption

Comparing the power consumption of different NUS schemes might not be trivial based on the reported performance in the literature, as the required power is inherently input signal-dependent. Furthermore, the circuitry design also impacts the overall dissipated power by the NUS scheme. Regardless, this section attempts to provide an intuition regarding the performance of different schemes with respect to power and justify it by the reported values of prior works. Table 4.2 investigates the reported power dissipation in prior NUS systems, notably at specific setups for tests as the power of an NUS depends on the signal and obtained reconstruction accuracy. Considering that there is no reported circuit implementation for some of the introduced schemes, such as CL-MDLC and CL-DLC, they are not included in this table.

Some observations can be concluded as follows:

(1) the clock-based schemes show lower power consumption at lower frequencies compared to their clockless versions. The CL-DDS system proposed in Chapter 3 of this research dissipates 1.45 μW while the clock-based version, CB-DDS, only consumes 0.58 μW with a similar setup and higher ADC resolution. However, this is reversed at high frequencies; For example, the CL-LC and CB-LC Topology II systems reported in [47] and [19] consume 438 μW and 3 mW, respectively. Note that the power consumption for generating an external clock is not included in the report. The above

observations align with Figure 1.4 that the clock-based NUS systems present an excellent power efficiency at low-frequency applications; however, as the frequency of operation increases, the power is expected to increase linearly, which makes these schemes less power-efficient at higher frequencies. It should be noted that the clockless NUS systems show less dependency on the frequency of operation as the building blocks consistently consume power to provide continuous monitoring of the signal.
(2) The Topology I implementations for conventional CL-LC and CB-LC show considerable power dissipation, especially compared to the corresponding Topology II implementations, as more comparators are required for this architecture.
(3) The complexity of a scheme and the number of essential blocks required for its implementation directly impact its overall power consumption. The CB-DDS scheme in [15], for example, consumes one-third of the power dissipated by the CB-SDS scheme [14] for the same setup and the same reconstruction accuracy.
(4) The overall power consumption increases with covered input bandwidth and resolution bits which correlates with the resulting accuracy of reconstruction.

Note that the above observations might not be universal for all reported works in the literature as they are also dependent on the architecture design and the tested signal.

Table 4.1: A comparison between the complexity of different NUS schemes in terms of their mathematical expression for the significant event and essential building blocks for analog implementation.

Scheme	CL-LC Top.I	CL-LC Top. II	CL-ALC	CL-DLC[a]	CL-DDS	CB-LC Top. I	CB-LC Top. II	CB-AR[b]	CB-SDS	CB-DDS
Math. Operation(s)	Comparison[1]	Comparison[1] Subtraction/Add[1]	Comparison[1] Subtraction/Add[1] Delay[1]	Comparison[1] Subtraction/Add[1] Derivation[3] Integration[3]	Comparison[1] Subtraction[1] Derivation[2] (Delay+Subtraction)	Comparison[1]	Comparison[1] Subtraction/Add[1]	Comparison[1] Subtraction[1] Derivation[3]	Comparison[1] Subtraction[1] Division[3]	Comparison[1] Subtraction[1] Derivation[2] (Delay+Subtraction)
Essential Building Blocks	Comparators[c]	2 Comparators Counter 1 or 2 Scalers DAC	2 Comparators Counter 2 Scalers Calibrator DAC	2 Comparators Counter 1 or 2 Scalers DAC Differentiator Integrator	2 Comparators 2 or 3 Subtractors Delay (Passive) S&H Monostable ADC[d]	Clock Manager Comparators[c]	Clock Manager 2 Comparators Counter 1 or 2 Scalers DAC	Clock Manager 2 Comparators Differentiator Filters Subtractor Multiplexer ADC[d]	Clock Manager 2 Comparators 3 Subtractors 3 S&H Analog Divider Counter ADC[d]	Clock Manager 2 Comparators 2 Subtractors 2 or 3 S&H ADC[d]
Complexity	Low	Low to Moderate	Low to Moderate	High	Moderate	Low to Moderate	Low to Moderate	Moderate to High	high	Moderate to High

[a]No analog implementation is reported [b]Only for ECG applications [c]Number of required comparators varies with resolution bits [d]The scheme triggers the attached ADC

[1]Low complexity [2]Moderate complexity [3]High complexity

Table 4.2: A comparison between the power consumption of different NUS schemes based on experimental results reported in the literature.

Scheme		CL-LC Top. I		CL-LC Top. II		CL-ALC	CL-DDS		CB-LC Top. I	CB-LC Top. II	CB-AR[a]	CB-SDS	CB-DDS
Reference		[47]	[47]	[45]	[37]	[35]	[Chapter 3]	[Chapter 3]	[19]	[56]	[23]	[14]	[15]
Input BW		1 kHz	5 MHz	1 kHz	1 kHz	20 kHz	100 kHz	5 MHz	20 MHz	<1 kHz	<200 Hz[b]	5 kHz	5 kHz
Test Setup	**Resolution Bits**	4	4	5.6	8	8	8[c]	8[c]	4	8	10.6	12[c]	12[c]
	Clock Frequency	N/A	N/A	N/A	N/A	N/A	N/A	N/A	4 GHz	1 Khz / 2 MHz	1 kHz	1 kHz	1 kHz
	Signal	N/A	N/A	1 kHz Sinewave	1 kHz Sinewave	1 kHz Sinewave	ECG 53 Samples/s	Two-tone 0.3+1 MHz 7.5 Samples/s	19 MHz Sine wave Full scale	125 Hz Sinewave	ECG 64 to 1024 Hz Sample Rate	ECG ∼160 Samples/s	ECG ∼160 Samples/s
	Resulted PR-SNDR	N/A	N/A	<35 dB	∼41 dB	∼47 dB	∼28 dB	∼31 dB	N/A	<49 dB	N/A	∼28 dB	∼28 dB
Power (uW)		34.4	437.8[d]	0.22	0.7	5	1.45	23.6	∼3000	9.32	8.4	1.7	0.58
Power Usage		Very High		Low		Low to Moderate	Low to Moderate		Very High[e]	Low[e]	High[e]	Moderate to High[e]	Low to Moderate[e]

[a]Exclusively for ECG Applications [b]ECG signal bandwidth [c]Resolution of attached ADC (test-bench) [d]Simulation results
[e]Graded relative to other clock-based schemes; the power usage principally depends on the clock frequency and linearly increases with the frequency

4.3.3 Reconstruction Accuracy vs. Number of Sampling Points

Comparing the output accuracy of different NUS schemes fairly requires using the same input signal and the same interpolation method used for reconstruction. However, achieving these two conditions based on the reported results in prior works in literature is impossible as the reported works use different signals and reconstruction methods for their respective experiments. Therefore, this research has included the Matlab simulation codes implementing the introduced NUS schemes to provide a fairer comparison by applying the same signal and reconstruction method to the schemes. Figures 4.12 and 4.13 shows the simulation results for an ECG signal with a period of 2 s applied to the NUS schemes introduced in prior sections. For a fair comparison, the simulation has targeted the same accuracy after reconstruction at the output and has reported the number of retained sampling points by each scheme. Note that the reconstruction accuracy is typically quantified by PR-SNDR which can be expressed as

$$\text{PR-SNDR} = 10\log\frac{Power\left(v_i(t) - mean\left(v_i(t)\right)\right)}{Power\left(v_e(t)\right)} \tag{4.10}$$

where $v_i(t)$ and $v_e(t)$ are the input and the difference (error) between the input signal and the signal after reconstruction, respectively. The retained sampling points at the significant events are marked by small dots, and a linear interpolation is used for reconstruction and the error signal is included as the subplot of each simulation.

Table 4.3 also summarizes the results achieved in this simulation to ease a quantitative comparison of the methods. Given that the same PR-SNDR of ∼35 dB is achieved for all schemes, the number of retained sampling points is a critical factor that reveals the effectiveness of an NUS. This metric highlights how robust the scheme is in selecting the most valuable points for signal reconstruction irrespective of its complexity and limitations. In other words, if an NUS scheme can reconstruct a signal with a specific PR-SNDR using fewer points than another scheme, this demonstrates its superiority. In this regard, CL-MDLC, shown in Figure 4.12(d), has achieved the

targeted accuracy with the smallest number of points (1067 points) significantly outperforming other schemes. This is due to the highly complex time-variable mechanism of this scheme in the detection of significant events. CL-DDS, using an approximated definition of the CL-MDLC scheme, achieves the second fewest number by retaining 1585 points(Figure 4.12(c)). The CL-ALC (Figure 4.12(b) has retained fewer points than CL-LC (Figure 4.12(a) thanks to its adaptive mechanism of reference levels.

The CB-SDS scheme, shown in Figure 4.13(c), has achieved the smallest number of retained points among the clock-based schemes, with 1866 number of points at 1 kHz clock. CB-AR shown in Figure 4.13(b) follows this scheme closely with 1957 points, however, this has been achieved with a high-frequency clock of 131.072 kHz required for the detection process. Note that the CB-AR scheme is an application-specific scheme where a master high-frequency clock is required for the detection of the significant event and once detected, the sampling frequency of signal changes from low (64 Hz) to high (1024 Hz). The clock rate plays a key role in clock-based schemes; when the rate of a clock is significantly higher than the signal bandwidth, the initial sampling of the signal required for clock-based schemes practically resembles an analog signal helping the scheme to reduce error associated with the clock. This is evident from comparing the results of CB-LC (Figure 4.13(a)) and CL-LC (Figure 4.12(a)) where with the same number of points and reference levels, both obtained the same accuracy. Overall, clock-based NUS schemes required a higher number of points than clockless schemes, mostly due to misplacement errors. Note that the error would increase when nonidealities associated with switching and circuit implementation of the clock managers are involved.

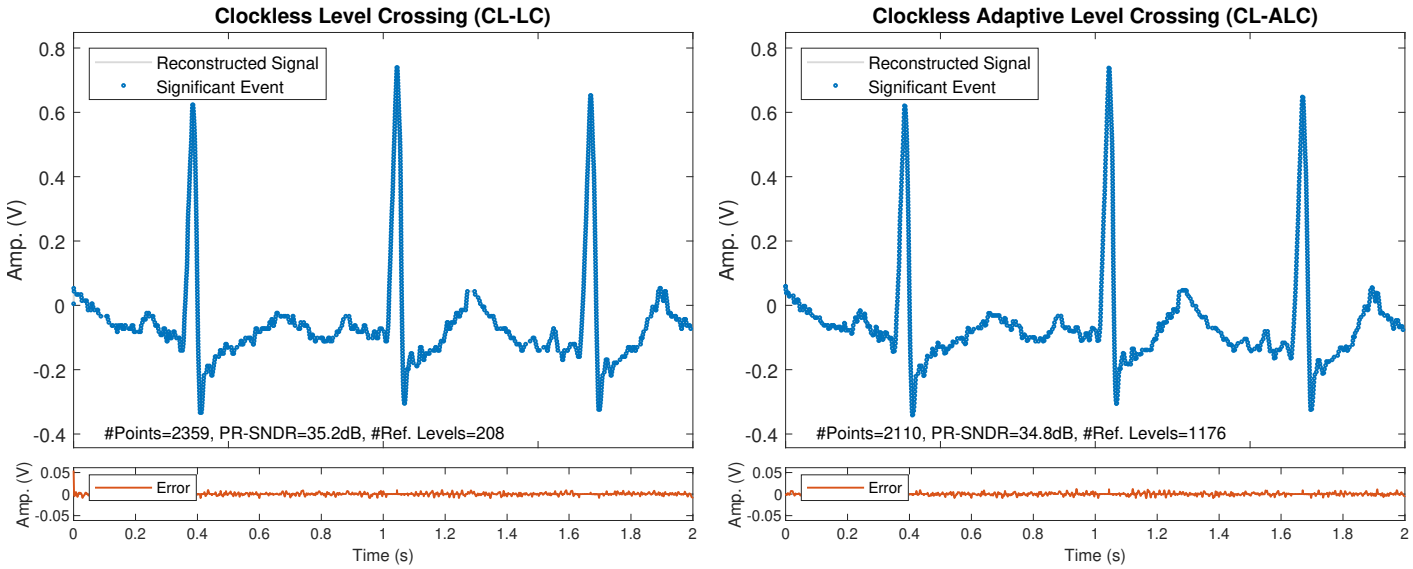
Although, the same signal is applied for simulation presented in Figures 4.12 and 4.13, several considerations should be carefully taken into account. For less complex schemes, setting up to achieve a targeted accuracy is simpler in real implementation; the number of reference levels in a CL-LC, for example, is the only parameter needed to be tuned. In contrast, for more complex techniques more pa-

rameters must be adjusted, although it provides more degrees of freedom in designing and implementing the scheme. Table. 4.3 shows the parameters of each NUS scheme that defines its significant event. Another factor is the resolution bits of attached ADC for the CL-DDS, CB-SDS, and CB-DDS. In the simulation, this parameter is set fairly close to level-crossing schemes (8bits) to have a fair comparison.

Table 4.3: A comparison between the output accuracy of different NUS schemes based on the simulation results reported in Figures 4.12 and 4.13.

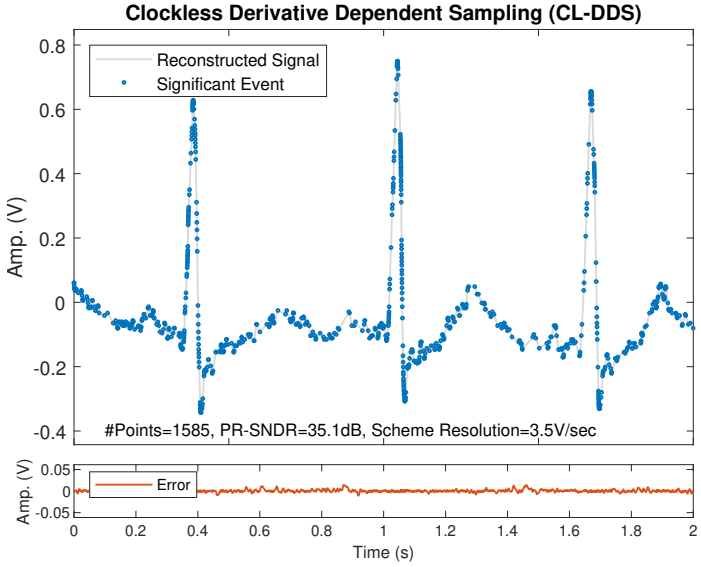
Scheme	CL-LC	CL-ALC	CL-DDS	CL-MDLC	CB-LC	CB-AR	CB-SDS	CB-DDS
PR-SNDR	35.2 dB	34.8 dB	35.1 dB	34.7 dB	35.1 dB	34.9 dB	35.2 dB	34.9 dB
# Retained Points	2359	2110	1585	1067	2345	1957	1866	2141
Scheme Resolution / # Reference Levels	208 Refs.	1176 Refs.	3.5V/s	315 Refs.	208 Refs.	256 Refs.	3 V/s	9.9 V/s
Clock Frequency	N/A	N/A	N/A	N/A	10 kHz	131.072 kHz	1 kHz	1 kHz
Parameters Defining Significant Event	# Ref. Levels	# Ref Levels # Steps Step Delay (τ)	Scheme Resolution[a]	# Ref. Levels	# Ref. Levels Clock Frequency	# Ref. Levels Input Master Clock High Sampling Clock Low Sampling Clock	Scheme Resolution[a] Clock Frequency	Scheme Resolution[a] Clock Frequency
Accuracy	Low	Low to Moderate	High	Very High	Low	Moderate	Moderate to high	Moderate

[a] If implemented with analog circuits, defined by comparator window size, the overall voltage gain of amplification stages, and/or initial time delay required for derivation (Δt)

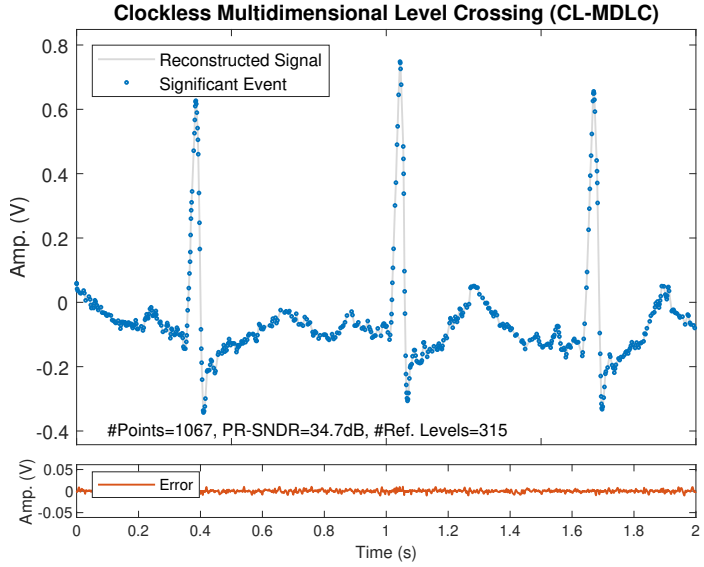


(a)

(b)



(c)



(d)

Figure 4.12: The Matlab simulation results for applying a real ECG to (a) CL-LC, (b) CL-ALC, (c) CL-DDS, and (d) CL-MDLC.

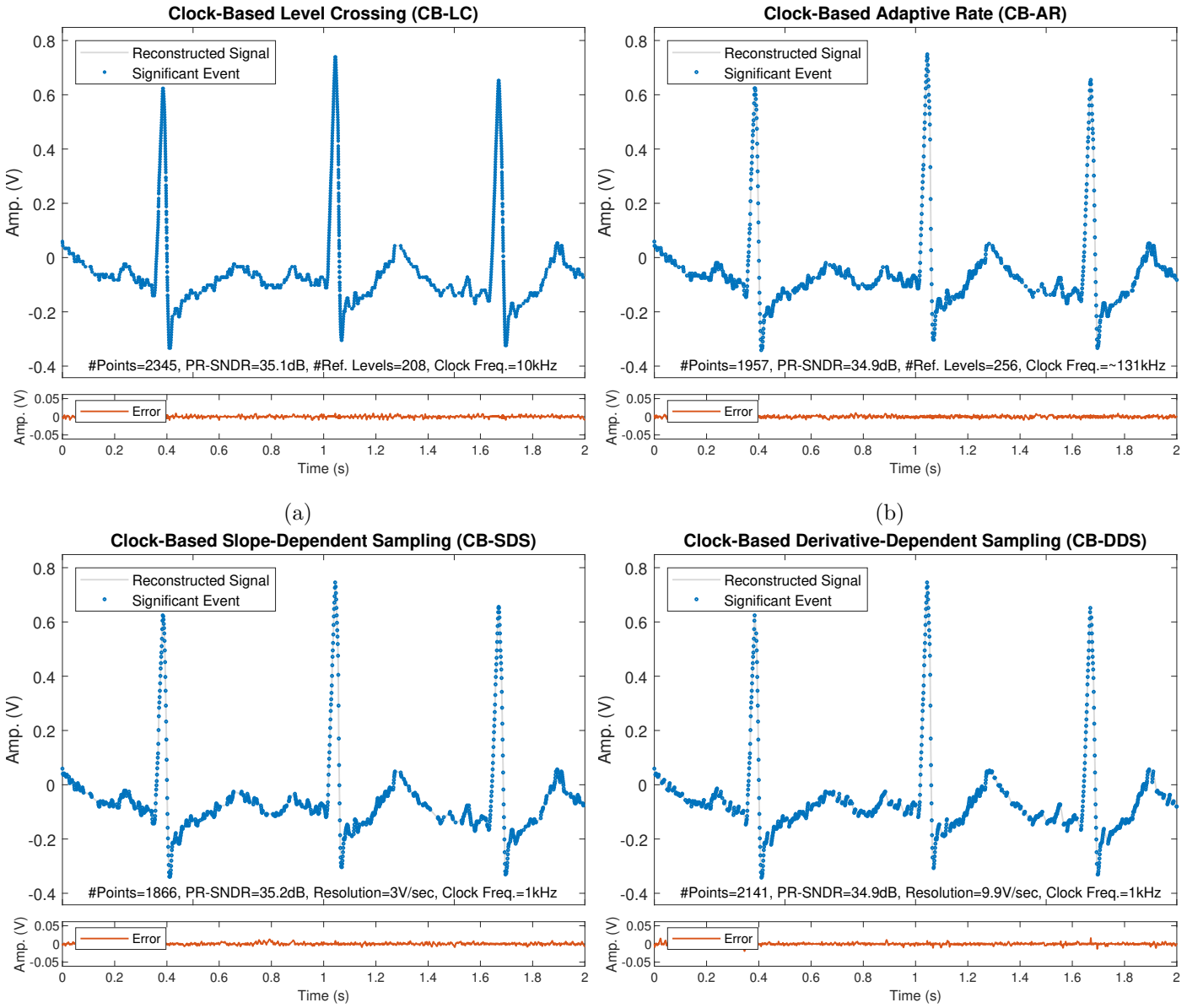


Figure 4.13: The Matlab simulation results for applying a real ECG to (a) CB-LC, (b) CB-AR, (c) CB-SDS, and (d) CB-DDS.

4.4 Summary

Non-uniform data acquisition is an efficient method for exploiting the trade-off between accuracy and power consumption in various applications. This comparative study introduces several NUS schemes, detailing their mechanisms for signal processing, analog circuit implementations, and limitations. The mathematical expressions that define significant events are presented for each scheme and their decision process for detecting a significant event is provided using arbitrary signal example cases. The design complexity, power consumption, and output quality of the introduced NUS schemes are discussed and compared based on our analysis, reported performance in the literature, and several simulations.

Chapter 5

Conclusions

5.1 Summary of Contributions

Non-uniform Sampling (NUS) techniques offer a promising solution to manage power budgets in data acquisition systems, particularly in many applications with limited power budgets. However, the design and usage of NUS schemes pose challenges, such as limitations in high-frequency applications or the difficulty of obtaining the desired accuracy without employing relatively complex or high-power designs.

This research investigated innovative solutions to these challenges. As the first contribution to this work, we proposed an ultra-low-power clock-based non-uniform sampling scheme using a derivative-based algorithm. This derivative-based mechanism provides comparable accuracy to other clock-based sampling schemes; however, it can be implemented using simple analog blocks that reduce the design complexity, and therefore, the NUS block power consumption compared to other schemes. To further reduce the power and to provide tunability to the scheme, several circuitry techniques have been utilized. Tunability is provided via the reference threshold and the voltage gain of the proposed system to achieve tunable accuracy (PR-SNDR) or degree of data compression (CF). The proposed clock-based derivative-dependent sampling (CB-DDS) system is placed next to, but isolated from, the ADC in a data acquisition system and enables the ADC only when necessary to reduce the total power dissipation of the system. The proposed system is fabricated in TSMC's 130-

nm CMOS technology and tested with real-world and ideal signals. The proposed CB-DDS system consumes less than 155 nW, covering up to 100 kHz frequency content. By adding the proposed DDS system to a data acquisition system chain, the power dissipation of the entire system can be significantly reduced. This work has been published in IEEE Transactions on Circuits and Systems I: Regular Papers [15].

As the second contribution, we have proposed a power-efficient clockless derivative-dependent sampling (CL-DDS) scheme for low- and high-frequency applications. The proposed scheme generalizes the mechanism of the prior clockless level-crossing techniques to an advanced derivative-dependent scheme that introduces a more power-efficient method of sampling while maintaining accuracy after reconstruction. Compared to other clockless NUS schemes, the proposed scheme is able to cover higher frequency content in the signal and to further compress the amount of data while maintaining the overall power consumption and providing the same accuracy as other schemes. The proposed CL-DDS scheme has been implemented in low- and high-speed systems using several analog low-power circuit techniques and fabricated in TSMC's 130-nm CMOS technology and its efficacy has been demonstrated by the obtained experimental results from the real-world and ideal signals. The proposed system can be tuned by controlling reference thresholds to obtain a targeted accuracy after the reconstruction. The maximum power consumption of the CL-DDS at its maximum activity is 1.15 μW (@1 MHz) and 8.81 μW (@20 MHz) for the low- and high-speed design, respectively. This work has been submitted to IEEE Internet of Things Journal and has been pre-published on TechRxiv website.

There are various mechanisms to develop an NUS scheme as prior state-of-the-art designs have been proposed and there are several circuit implementations for each of these mechanisms. Despite the abundance of previously proposed NUS techniques, the lack of a comprehensive study makes selecting a suitable one for a required application challenging. As the third contribution, we prepared a comparative review study on NUS schemes that introduces various prior NUS techniques and their sug-

gested implementations, discusses different design considerations and limitations, and compares their performance, quantitatively and qualitatively, with respect to power consumption, output signal reconstruction accuracy, and design complexity. This study has implemented several NUS schemes in MATLAB codes for a further fair comparison between them.

5.2 Future Work

The proposed NUS techniques in this thesis can be integrated into existing ADCs in sensor systems, such as wearable healthcare monitoring devices. The fabricated chips can be then incorporated into such systems to enhance their power management and extend their battery lifetime. This advancement might also provide an opportunity to develop batteryless wireless sensors that rely on energy harvesting as their primary power source. Eliminating batteries from the devices/sensors would reduce their size and weight, meeting the growing demand for compact and lightweight solutions for healthcare applications. Future work could explore the development of a batteryless wireless healthcare monitoring device with wireless energy harvesting that uses the proposed NUS scheme as part of data acquisition.

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