NOVEL CONTROL APPROACHES TO IMPROVE SINGLE AND MODULAR DC-DC CONVERTERS DYNAMICS IN DATA CENTERS

by

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Abstract

In many modern power electronics applications such as data centers, there are specific requirements such as fast load dynamics and sensitive power, voltage or current sharing. Therefore, power converters need to provide and maintain ultra fast responses to achieve a certain control objective. For example, for voltage regulators connected to the points of the load in data centers, very fast load step changes pose an extra challenge on the design of the power converter such that conventionally, excessive passive components are used to regulate the output voltage. On the other hand, in higher power applications such as data centers or electric vehicles, modular power converters are used to guarantee perfect power sharing and optimum system dynamics and voltage/current regulations for fast load transients. Recently, researchers are trying to tackle these challenges through advanced control systems without over-designing the hardware and passive components, to reduce the cost, and increase lifetime of power converters. This research addresses advanced control methods to improve converter performances for both single and modular DC-DC converters.

This research first proposes a new controller to achieve fast load transient responses in the load-connected DC-DC converters of power management systems in data centers. The controller is designed to achieve identical dynamics for all state variables in the converter and is able to provide load transient responses with recovery times of less than one switching cycle and low overshoot/undershoot levels. A systematic design approach is introduced for the controller, for both continuous and discontinuous conduction modes of operation.

Moreover, for DC-DC converters used in the intermediate stage of the power management system in a data center, a controller is proposed to compensate for low system damping levels in high load currents, or equivalently, low load resistance values. The controller is based on decoupling system dynamics from the load resistance

value, once the controller is applied to the system. The proposed approach improves the load transient response of the converter in large load steps, while achieving a converter with small energy storage requirements. At the same time, the controller enables converter dynamics enhancements without auxiliary circuits, to reduce the cost, volume, and complexity of the system.

Finally, a controller is proposed to improve steady-state and dynamical performances of modular DC-DC converters. This controller can achieve very fast power sharing among the modules, while obtaining an accurate voltage/current regulation for fast load dynamics. The introduced approach is applicable to all converter topologies and is robust against parameter uncertainties and parameter mismatches among the modules. The proposed distributed control system is formulated for Input-Series Output-Parallel (ISOP), Input-Parallel Output-Series (IPOS), and Input-Series Output-Series (ISOS) DC-DC converters. For all the controllers proposed in this thesis, a proof of stability is provided. Also, the appropriate performances of the controllers are verified through simulation and experimental results.

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Abbreviations

UPS	Uninterruptible Power Supply
CPU	Central Processing Unit
DDR	Double Data Rate
MPC	Model Predictive Control
PWM	Pulse Width Modulation
DPWM	Digital Pulse Width modulation
HVDC	High Voltage Direct Current
EV	Electric Vehicle
ISOP	Input-Series Output-Parallel
IPOS	Input-Parallel Output-Series
ISOS	Input-Series Output-Series
IPOP	Input-Parallel Output-Parallel
IVS	Input Voltage Sharing
OCS	Output Current Sharing
OVR	Output Voltage Regulation
OCR	Output Current Regulation
SMC	Sliding Mode Control
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
DSP	Digital Signla Processor
DAB	Dual Active Bridge
CPL	Constant Power Load
ZOH	Zero Order Hold

List of Symbols

i_o	Output Current
i_L	Inductor Current
v_o	Output Voltage
$v_{o,ref}$	Reference Output Voltage
$i_{o,ref}$	Reference Output Current
d	Duty Cycle
L	Inductance
C	Capacitance
R	Resistance
n	Transformer Turns Ratio
N	Number of Modules
x_i	i-th State Variable
θ_i	phase Shift Applied to i-th Module
v_{in}	Input Voltage
$i_L(0)$	Inductor Current at the Beginning Instant of a Switching Cycle
$i_L(T_s)$	Inductor Current at the Ending Instant of a Switching Cycle
T_s	Switching Period
f_s	Switching Frequency
k_p	Proportional Gain
k_i	Integral Gain
$\hat{i_L}$	Inductor Current Estimated by observer
$\hat{v_o}$	Output Voltage Estimated by observer
$\tilde{i_L}$	Small Signal Variations of Inductor Current
$\tilde{v_o}$	Small Signal Variations of Output Voltage
R_{cont}	Load Resistance Value Used by Controller
i_{oc}	Output Current Used by Controller
T_d	Delay Time
P^*	power Level of Constant Power Load
m_1, m_2	Luenberger Observer Gains
K_1	Distributed Control Gain for Battery Charging Mode
K_2	Distributed Control Gain for Battery Discharging Mode
$v_{C,ref}$	Reference DC-link Voltage for ISOP Structure
$v_{C,i}$	Input DC-link Voltage of i-th Module in ISOP Structure
$v_{in,i}$	Input DC-link Voltage of i-th Module in ISOS Structure
$v_{o,i}$	Output DC-link Voltage of i-th Module in ISOS Structure
K_{ia}	Integral Gain for Automatic Reference Setting Algorithm
K_{pa}	Proportional Gain for Automatic Reference Setting

Chapter 1

Introduction

Today, modern power converter applications have introduced new trends and approaches to meet the emerging requirements of the power electronics industry. Some of the most important approaches used by power electronics system designers in recent years include using more complex converter structures such as modular converters [17], boosting system performances in applications with fast-changing loads [18, 19], increasing the switching frequency, and finally reducing the converter sizes to achieve higher power densities. These approaches are taken to achieve suitable steady-state and transient performances for power converters and any failure in this mission forces the system designers to make compromises in the converter design process. For instance, it might be necessary to over-design converter components to compensate for deficiencies in control systems. Therefore, it can be stated that the current trend in the power electronics industry is to design power converters with minimum energy storage requirements and more complicated controllers.

Generally speaking, modern DC-DC converter applications such as power management systems in data centers, use different power converter and control system configurations for low power converters with small or large load changes and high power modular converters. Specifically, the power conversion system used in a data center can be divided into three stages of high-power high-voltage modular DC-DC converters, and single high-power low-voltage and low-power low-voltage DC-DC converters. This chapter discusses the requirements and the components of the power management system in a data center. The existing challenges to fulfill these requirements are also explained and the proposed solutions in the literature to overcome these challenges are reviewed. While the main focus is on power management systems in data centers, application examples will be provided for different DC-DC converter configurations. This will better illustrate the significance of the challenges associated with the applications discussed.

1.1 Overview of Power Management Systems in Data Centers

This section explains the significance of data centers in performing computational duties and other tasks associated with portable electronic devices. It also discusses components and requirements of the power management system in a data center. To explain system requirements better, typical numerical ranges for different system parameters are provided.

1.1.1 Power Management System Components, Challenges, and Requirements

This subsection discusses the significance of data centers and presents details about the compoents and requirements of the power management system in a data center. Nowadays, these are mostly data centers which perform the operational duties of portable electronic devices [20]. The communication among these data centers and the associated portable electronic devices are established through cloud services [20]. To be able to fulfill operational requirements, data centers are equipped by a large number of fast speed processors [20]. Based on the system objectives, many of these processors are constantly plugged in and out of the network and from the power management system point of the view, these changes are seen as load steps. The voltage regulators respond to these load steps by entering into a transient period and recovering from it after a number of switching cycles. This can limit the speed of data centers.

At present, two power management architectures are used for data centers, each of which transfer power to the loads using a separate DC link voltage level [9]. One of these architectures uses a 12V DC link, while the other uses a 48V one [9]. In the first configuration, the first power conversion stage is a 60Hz transformer converting a 4160V,AC to a 480V,AC voltage [9]. The obtained AC voltage is processed by an uninterruptible power supply (UPS) and a power distribution unit (PDU) to form a 220V,AC voltage [9]. The power supply unit processes this voltage by a rectifier and an isolated DC-DC converter, to form a 12V DC link voltage [9]. In the second architecture, however, the UPS in the 12V configuration is eliminated to form a 48V DC link voltage [9, 21, 22]. The 48V architecture has the advantage of an increased efficiency over its 12V counterpart [9, 21, 22]. This increased efficiency is obtained as a result of the existence of a fewer number of power conversion stages in the system for the 48V architecture [9, 21, 22].

In data center applications, the supply voltage of the motherboards in service is

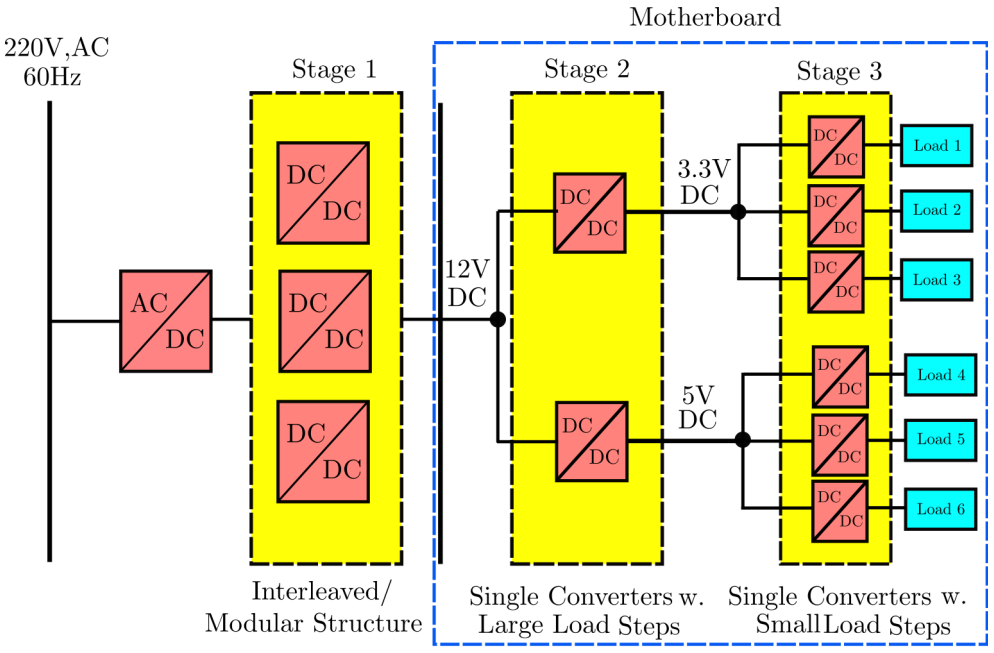


Figure 1.1: Structure of the Power Management System in a 12V-based Data Center [9]

either 48V or 12V, based on the system architecture. Moreover, the voltage level at the point of the load can vary from below 1V to near 2V [20, 23]. For example, a CPU load requires a 1.3-1.8V voltage, and a DDR load requires a 1.2V voltage for operation [23]. The switching frequencies of DC voltage regulators are selected between 200KHz and 1.1MHz and the converters need to have a power density in the range of 300-500 W/in^3 [20, 24]. Most importantly, the typical efficiency range of voltage regulators is reported as 94-96 percent [20, 24]. The modern trend is to add the number of high-performance processors in each data center and this way, the entire load current can reach up to 200A [25].

While the proposed methods in this dissertation are applicable to both 12V and 48V data center architectures, the main focus is on providing control strategies for the 12V architecture. The schematic of the power management system for a 12V-based data center is observable in Fig. 1.1.

The power management system in a data center is composed of three different power conversion stages [9] as shown in Fig. 1.1. These conversion stages are marked as Stage 1-3 in this figure. The power and control challenges associated with each of these stages are explained below.

Stage 1 Challenges: The converters in this stage has a DC input voltage of 380V and an output voltage of 12V [9]. For the 48V-based data center, however, the input DC voltage in 400V and the output voltage is 48V [9]. The switching frequency

is selected around 100KHz and typically, modular multi-phase LLC or Dual-Active-Bridge converters are used for data center applications [9]. Stage 1 is characterized by high input voltage and high load current levels. Also, the voltage gain of this stage is considerably high. This increases the voltage and current stresses of the system components and increases the failure risk of the system. Besides, achieving a good efficiency level becomes more difficult in Stage 1. Most importantly, in a conversion system with a high voltage gain and high nominal voltage and current values, passive components must have larger sizes to achieve acceptable ripple levels. This decreases the variation rates of voltages and currents in the converter during transient periods. As a result, the converter dynamics is degraded. Concluding all these, the challenges in Stage 1 include achieving good efficiency, reliability, and dynamics at the same time.

Stage 2 Challenges: DC-DC converters in this stage convert a 12V input voltage to either a 3.3V or a 5V output voltage inside the motherboard of a computer in a data center. The switching frequencies of these converters are also in the range of 100-200KHz. All load steps at points of the load such as the loads 1-6 in Fig. 1.1, are summed up and seen as a single large load step by the converters in stage 2. Also, the equivalent load resistance seen by the output node of these converters is equal to the paralleled combination of the load resistances of each individual load. Therefore, the total load resistance value for power converters in stage 2 is small. As a result, the system damping is reduced and the overall recovery time of the system from a transient is increased. Therefore, the supply voltages for the processor loads remain either higher or lower than their reference values for longer periods of time, which can cause the processors and other loads to either get damaged or stop working. In fact, in stage 2 converters, the main challenge is the slow dynamics of the system.

Stage 3 Challenges: The converters in this stage convert a 3.3V input voltage to an output voltage in the range of 1-2.5V [19]. Their switching frequency is normally selected around 1MHz and their maximum load current is around 1A [19]. Stage 3 converters are characterized by their low-voltage low-current level features. As these converters directly deliver the power to processors, they need to provide the fastest possible dynamical profile. This way, processors do not face any speed limitations during operating, from the power management point of the view. Hence, the main challenge in stage 1 is to improve the dynamical performance of the system in load steps.

As mentioned above, the most important challenges for power management systems used in data centers communicating with portable electronic devices include

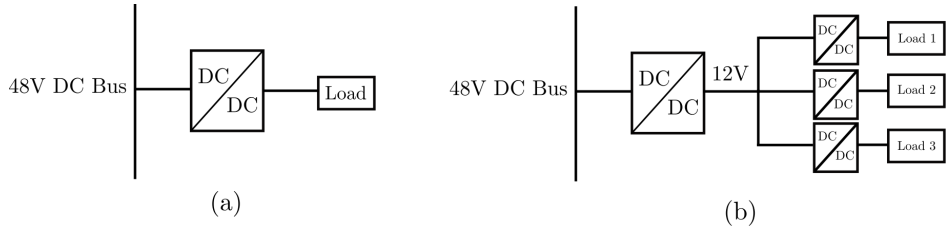


Figure 1.2: (a) Single-stage (b) Multi-stage Systems for Power Management Units in 48V-based Data Centers Handling Electronic Portable Devices

efficiency, power density, and the speed limitation of the system due to load steps. The architecture of the power management system and the controller used are the two main factors affecting power density, load step dynamics, and efficiency [26]. There are two power management architectures used in 48V-based data centers which are called single-stage and multi-stage systems [20, 26, 27, 28, 29, 30]. In single-stage systems, just one DC-DC converter is used to convert the 48V DC bus voltage to 1V [26]. In the multi-stage system, however, several DC-DC converters are cascaded to form the power conversion system [26]. The first conversion stage converts the 48V input voltage to 12V, and the remaining voltage regulators convert this 12V voltage to voltage levels needed by the loads (ex. 3.3V, 1V,etc.) [24]. In the single-stage architecture, the dynamic response of the system is improved in load steps, at the cost of lower power density and lower efficiency [26]. In contrast, multi-stage structure increases the power density and efficiency of the system, at the cost of degraded load transient responses due to large load steps [26]. Fig. 1.2 illustrates the structure of multi-stage and single-stage systems.

1.2 Literature Review

This section presents a literature review for control system solutions associated with power converters dealing with fast dynamic loads in data centers. The discussed solutions in this section are proposed in the literature to solve the challenges mentioned in the previous section. The contents of this section are presented in four different subsections, including DC-DC converter controllers for small load steps, DC-DC converter controllers for large load steps, and controllers for modular DC-DC converters.

1.2.1 Review of DC-DC Converter Controllers for Small Load Steps with Fast Dynamics

This section presents an introduction on DC-DC converter controllers used in stage 3 of the power management system in a center. To improve the load transient responses of low-power small load step DC-DC converters, one approach taken in the literature is the simultaneous usage of simple controllers and auxiliary circuits [18, 31, 32, 33]. Such auxiliary circuits can increase the converter's cost and complexity. These circuits use either coupled inductors [31], or an auxiliary inductor in parallel [18, 32] or series [33] with the converter's main inductor. This is done to increase the slew-rate of the main inductor's current, during load transients.

As auxiliary circuits add to the cost and complexity of the system, if possible it is desired to enhance the dynamics using only control systems. For example, typical non-linear controllers such as model-predictive controllers (MPC) [34],[35], adaptive controllers [36], and intelligent controllers [37] are proposed to improve the load transient responses. Although model predictive control systems are interesting for fast response applications, the design methodologies are not very systematic. Moreover, overall transient responses, load step change recovery time [34] and overshoot/undershoots [35], are not superior compared to other existing methods in the literature [19], [38]. In comparison with other methods such as [19], [38], adaptive controllers [36] exhibit longer recovery times. It should also be mentioned that intelligent controllers seem to be complicated and sometimes cannot be designed in a systematic way [39] and a formal proof of stability for such methods is not possible. Although typical non-linear control systems can be powerful tools for special applications, according to the existing literature for fast load transients, they have not shown very optimum dynamics and they normally compromise one of the control objectives such as overshoots and settling times.

To achieve fast transients, high-performance minimal dynamic control methods such as [19],[38],[40, 41, 42, 43, 44, 45] are proposed, which are specifically constructed and designed, based on the requirements of the applications. An active ramp tracking control is proposed in [19], which provides fast load transient responses. Still, steady-state errors in output voltage are sometimes observed, when the load current varies largely. In [38], an improved I^2 controller is proposed that requires auxiliary circuits, resulting in a higher cost of converter. A peak-capacitor-current pulse-trained controller is proposed in [40], which provides good performances for wide load range applications. However, in some cases, the ripple levels of the output voltage can become large. A second-order sliding mode controller is presented in [41], where the switching frequency is a function of inductor's value

and its variations can reduce controller's robustness. A relatively complex digital controller with cycle-controlled DPWM is designed in [42]. Also, a constant-on-time controller with pseudo-wave tracking technique is developed in [43], which provides fast load transient responses. In this method, an operational trans-conductance amplifier is used, which increases converter's cost. Time optimal controllers are also used to improve the load transient responses of buck converters. These controllers rely on either circuitry approaches or the theory of time-optimal controllers. Two time optimal controllers are proposed in [44] and [45], based on capacitor charge balance technique. Although the load transient responses provided by these controllers are fast, the associated recovery times can be large for some large load variations. A low-cost digital implementation of the capacitor charge balance technique is proposed in [46]. However, the load transient responses can become slow for larger load steps. Finally, digital geometrical controllers based on time-optimal control theory are developed in [47, 48, 49, 50, 51]. However, these methods may result in large overshoot/undershoot levels for some load variations.

Depending on the feasible operation modes, fast transient response controllers in the literature may operate only for DCM [52, 53, 54], only for CCM [19, 38, 1], or for both modes of operation [40]. Linear control design approaches such as bode plots or system transfer functions are widely used in the literature. In these design methods, there is no closed-form solution to determine control parameters and the results cannot be used for different sets of converter parameters. Moreover, in such approaches, it is not clear how optimal the system performance is and how much the system can tolerate the converter parameter uncertainties and variations.

1.2.2 Review of DC-DC Converter Controllers for Large Load Steps

This section provides a literature review on the existing controllers which are used to control stage 2 converters in the power management system of a data center. DC-DC converters with good performance characteristics and suitable dynamic profiles are desired for many applications with either high or low load current levels [2]. Data centers are one of these applications, which perform the operational duties of portable electronic devices [20]. The communications among these data centers and the associated portable electronic devices are established through cloud services [20]. To be able to fulfill operational requirements, data centers are equipped by a large number of fast speed processors [20]. Many of these processors are operated randomly and sporadically and these changes act as load steps in the system. The voltage regulators respond to these load steps by entering into a transient period

and recovering from it after a number of switching cycles. This can limit the speed of data centers.

Stage 2 converters in the power management system of a data center convert a 12V input voltage to either a 3.3V or a 5V output voltage inside the motherboard of a computer. All load steps at the point of loads in stage 3 converters are summed up and seen as a single large load step by stage 2 converters with low equivalent output resistances, as opposed to higher equivalent resistances for stage 3 converters. The higher resistances in stage 3 are obtained as each of stage 3 converters are connected to a single smaller load. Due to the higher load resistances of stage 3 converters, the system damping is high and simple control without auxiliary circuits can provide satisfactory transient responses as discussed in [19, 55, 56, **?**] for various applications, such as wireless portable devices [19, **?**].

For the stage 2 converters where large load steps occur at high frequencies, DC-DC converters are required to handle higher load current levels [3]. In these converters, the typically-low values of load resistances reduce systems' damping, creating slow load transient responses. Also, the dynamical profile of a stage 2 converter is impacted by the load resistance and may be significantly changed during large load steps in this stage. As a result, controller design for stage 2 converters becomes a challenge and stage 3 converter controllers such as [19, **?**] may not maintain their high performances, if they are applied to stage 2 converters. To solve this problem and enhance system dynamics, widely adopted approaches in the literature include adding auxiliary circuits during the transient periods [2], [3, 57, 4, 58, 59, 60, 61, 62, 63], or using more complex and high-performance controllers [64, 65, 19, 66, 67, 68].

Some of the existing auxiliary circuits reduce the total inductance of the converter during transients [3, 57, 4, 58, 59, 60]. This approach achieves better load transient responses by increasing inductor current's rates of variation [57]. Auxiliary circuit currents are injected to or drawn from the load side in [3] to improve the response at the expense of efficiency degradation [3]. In another approach, an inductor is inserted in parallel with the main inductor during transients [57]. Although this method improves the dynamics, it increases overshoot levels in the main inductor's current. Auxiliary currents are injected to the load using a parallel buck converter, resulting in fast system dynamics [4] at the expense of duplicating the power circuit. The buck converter's inductor is replaced by a flyback-based converter in [58]. This approach requires an auxiliary circuit with a similar power rating compared to the main circuit. Using the capacitor charge balance control and a series auxiliary inductor in [59] resulted in major dynamic improvements. However, large instantaneous variations and overshoots in inductor current and output voltage can be ob-

served. An improved topology of inductor-switching DC-DC converter is proposed in [60], with higher efficiency and reduced overshoot/undershoot levels. However, the number of passive components are increased, resulting in higher energy storage requirements. Other methods to improve converter's dynamics include changing the resistance value seen by the converter's output terminal [61], and inserting a current source branch at the load node [62, 63]. Although the auxiliary circuits generally improve load transient responses, they increase system's cost and complexity and normally introduce additional losses [61], along with more complex control [63], and possible stability issues [62] due to switching the power auxiliary circuits on and off repetitively.

High-performance controllers are also proposed to improve converter's dynamics [64, 65, 19, 66, 67, 68]. However, the levels of dynamics improvements are limited for large load steps. The proposed controllers can be classified into three categories. In the first category, linear controllers based on feedback and feed-forward are proposed [64, 65]. The system dynamics is a function of the load resistance value and is changed considerably in large load steps. Therefore, a single linear controller cannot achieve suitable dynamic responses for such load steps. The second category of controllers either maximize or minimize the duty cycle during transients [19, 66]. Although this approach makes system dynamics faster, it leads to step changes in the duty cycle, which in turn create new transient states in the system. As a result, the system dynamics becomes slower than expected. Finally, another category belongs to the family of I^2 controllers [67, 68], which can enhance system dynamics considerably. This approach normally requires compromises between the stability of the system and its steady-state performance indicators such as ripple levels.

1.2.3 Review of Controllers for Modular DC-DC Converters

This section provides a literature review on controllers and their requirements in modular DC-DC converters with fast dynamic loads. Today, modular DC-DC converters are used in applications such as data centers, HVDC transmission systems, electric vehicles (EV), and traction applications [17, 69]. In this subsection, the focus is on stage 1 converters in the power management system of a data center. Generally speaking, using several DC-DC converters instead of a single one to transfer power from source to the load or vice-versa, reduces voltage and current stresses on each converter. In such a case, if each converter is controlled separately, a modular system with higher reliability will be obtained. Common system configurations include input-series-output-parallel (ISOP), input-parallel-output-series (IPOS), and the input-series-ouput-series (ISOS) connection schemes [17, 70], where the parallel

and series connections reduce current and voltage stresses on each module, respectively [17, 69, 70]. In a modular DC-DC converter system, the topology used for converters may vary depending on the application. These topologies normally provide galvanic isolation between the input and output. In this regard, Dual-Active-Bridge (DAB) converters are widely used as the main building blocks of modular DC-DC systems, due to their high power densities and bi-directional power-flow capabilities [69, 71].

To utilize the full capacity of a modular DC-DC converter system, power sharing is normally desired to have all modules transfer the same power levels at all instants during transient or steady-state conditions [69, 72]. For ISOP configuration, all modules share the same input currents and output voltages. Therefore, power sharing for this configuration can be achieved by input voltage sharing (IVS), and output current sharing (OCS). Also, depending on the control objective, either one of output voltage regulation (OVR) or output current regulation (OCR) is normally required.

To realize IVS and either OVR or OCR in modular DC-DC converter systems, different control methods have been proposed in the literature [17, 69]. A few methods use well-known control approaches such as Model Predictive Controllers (MPC) and Sliding Mode Controllers (SMC) [70, 71, 72]. MPC controllers improve system dynamics considerably and SMC controllers are robust against parameter mismatches between modules. However, MPC controllers require knowledge of system parameters to achieve a suitable performance, without which robustness issues may arise. Also, SMC controllers may create large overshoots/undershoots in applications dealing with high load currents. This is beacuse the sliding surfaces are usually defined as a linear combination of voltage error signals and their time-integrals and SMC controller keeps this sliding surface constant over time [72]. Therefore, the voltage error signals become exponential and as exponential signals cannot have a zero level at their beginning time instants, large overshoots or undershoots may sometimes be observed. Peak Current Control method is used in [17] to improve the performances of modular DC-DC converters. Such controllers are suitable for applications with fast changing supply voltages [17]. However, applying peak current controllers to applications with fixed switching frequencies may cause stability issues [73]. In fact, using peak-current controllers can lead to instabilities due to sub-harmonics, chaos, bifurcations, and duty cycle saturation phenomena [74, 73, 75].

Other methods in the literature use linear controllers and master/slave or cross-duty cycle structures [6, 76, 77]. These controllers mitigate isolation issues in designing sensors, and enhance dynamic responses of the system and they have simple

control structures [6, 76, 77]. However, they require communications between different modules, reducing the system reliability. Other controllers rely on solving non-linear control equations to find the required duty cycle, where the non-linear equations include the non-linear voltage/current gain equations [69, 71, 78]. These controllers enhace the dynamic responses of the system considerably and provide fast transient responses with low overshoots/undershoots. However, they need to estimate system parameters to provide accurate power sharing between modules, which might make system operation and controller structure complex.

Droop/Inverse Droop controllers and gradient-based control methods are also used to improve the performances of modular DC-DC converters [7, 16, 79]. These controllers have simple structures and they improve the dynamic characteristics of the system. However, as they build a linear relationship between DC link voltage errors and output voltage errors, they create trade-offs between input voltage sharing and output voltage regulation. Applying common duty-ratios to all modules is another control approach for modular converters [80, 81, 82]. Although these methods provide simple control structures, they cannot provide satisfactory power sharing between modules at steady-state, in case the parameter mismatches between modules are significant [69, 83, 84]. Instead of relying on control systems, some approaches propose topological modifications to modular DC-DC converters, to realize power sharing and output voltage regulation [85, 86, 87, 88]. Some use voltage equalizing circuits in parallel with the DC link capacitors of different modules [85]. in other approaches, switched-capacitor circuits and buck-boost balancing circuits are connected [86] to the input sides of modules. Alternatively, it is also shown that power sharing can be achieved by common mode coupled inductors [87], or flying capacitors [88]. The topological modifications made above realize systematic power sharing and increase the modularity of the system. However, they increase the system complexity and cost.

1.2.4 Review of Controllers for Input-Series output-Series DC-DC Converters

This subsection discusses the proposed control systems in the literature for Input-Series Output-Series (ISOS) DC-DC converters. Today, power conversion systems with high voltage level requirements are demanded in many applications. Instead of relying on a single conversion unit, these systems use several converters to form modular structures, realizing system-level objectives more efficiently. In particular, the Input-Series Output-Series (ISOS) modular structure is preferred for systems with both high level input and output voltages. In ISOS configuration, switches

with lower voltage ratings may be used in the converter development process [89]. The cascaded structure of the ISOS configuration increases modularity, reduces the maintenance cost [90], and enables systematic expansion of system functionalities [91]. Finally, as system components need to tolerate lower electrical and thermal stresses in ISOS, the reliability is increased [91].

The advantages mentioned make ISOS DC-DC conversion systems a perfect solution for space exploration systems [90], solid state transformers [91, 92], DC transformers [91, 92], and subsea distribution systems [93]. Some of control challenges associated with ISOS DC-DC converters include power sharing among modules [89, 90, 91], and stability issues [89]. Also, controllers applicable to other modular configurations might fail to guarantee a stable system operation in ISOS [89].

For accurate power sharing among modules in an ISOS system, some of the existing approaches use auxiliary circuits or special converter topologies with natural power sharing [90],[94, 95, 96, 97, 98]. These circuitry approaches increase system's modularity and reduce the control burden. However, they either increase the cost and complexity of the system or may be unable to achieve some features such as high power densities, or bidirectional power flow. [90] uses a parallel branch including a MOSFET and a coupled inductor for power sharing, and is applicable to all topologies [90]. However, the auxiliary inductors increase magnetic losses. [94] and [95] achieve power sharing using paralleled MOSFETs, and a MOSFET-inductor combination, respectively. Although these approaches are systematic, they increase the number of circuitry components as well as cost and losses for a high number of modules. [96] uses a full-bridge based topology for natural power sharing with reduced control burden. However, large-sized input capacitors are required, slowing down input voltage sharing dynamics. [96]. [97] uses a flyback-based topology for power sharing, which limits efficiency in high power applications due to an increased number of diodes used [97]. Finally, [98] proposes a two-transistor forward converter achieving active power sharing. However, as additional magnetic couplings between modules are required, the transformer's and converter's volumes are increased.

Control methods are also used in the literature for power sharing in an ISOS structure. The duty cycle applied to a specific module in one of these control classes is generated by processing the voltage/current signals of all other modules except that module itself [89, 99]. These controllers avoid sensing high-level input voltages [99] and enhance system dynamics [99], while reducing reliability due to communications among modules. Another control class uses droop/ inverse droop and gradient-based control methods for power sharing [100, 101, 102]. Although these controllers provide a distributed system with increased modularity [100], they create trade-offs between

input voltage sharing and output voltage regulation. Peak-current controllers with effective rejection of input voltage disturbances are proposed in [8, 103]. However, implementation delays and reduced reliability arise from inter-modular communications the controllers require [103].

Some of existing controllers need system model or parameters for power sharing, reducing system robustness [104, 105, 106]. [104] uses model-predictive controllers with enhanced dynamics and reduced costs [104, 105]. [105] proposes a tunable power sharing method, and [106] provides new hot plug-in and out features. Miscellaneous methods such as applying a common duty ratio to all modules [107], or modular decoupling are also proposed [108]. The first method has a simple structure [107] with sensitivity to parameter mismatches among modules, and the latter requires inter-modular communications. The next section discusses the proposed solutions in this dissertation.

1.3 Proposed Solutions

This section briefly discusses the main concepts regarding the solutions proposed in this dissertation to address the challenges mentioned in the previous sections. In this section, only general concepts and main ideas are presented and further details will be presented in the next chapters. In this section, the proposed solutions are provided in three different subsections.

1.3.1 Identical States Dynamics Control

This subsection briefly discusses the proposed controller to improve load transient responses of DC-DC converters with small load steps.

Generally speaking, the bahavior of a DC-DC converter can be described by a nonlinear state-space representation, if capacitors voltages and inductors currents are selected as state variables. In a typical DC-DC converter, some of the state variables associated with the system have faster dynamics than the others. For instance, in a buck converter, the inductor current passes through a parallel R-C branch, to generate the output voltage. As the impedance of this R-C branch converges to zero at high frequencies, it can be understood that the capacitor voltage waveform is obtined by applying the inductor current signal to a low-pass filter. Therefore, the inductor current has faster dynamics, compared with the capacitor voltage. This issue implies that if a disturbance such as a load step or an input voltage step occurs in a closed-loop converter system, different state variables reach their reference values through different dynamics. This issue causes the dynamical profile of the system to

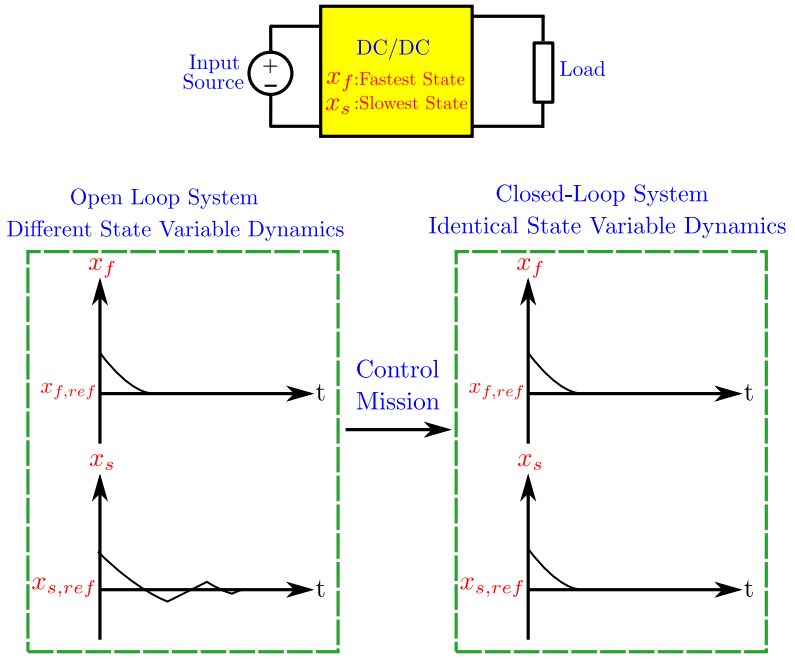


Figure 1.3: Illustration of the Concept of Identical State Dynamics Control

be limited by the state variable with the weakest dynamics, or i.e. the state variable with the slowest dynamics in the system.

To solve this problem, a controller is proposed in this dissertation which uses a control law to force similar dynamics for all state variables in the system. This is achieved by analyzing the converter topology, finding the state variables with the fastest and slowest dynamics, and finally enforcing identical dynamics to these two state variables. If the dynamics of the slowest and fastest state variables are equally fast, then all other state variables in the system will also have the same dynamics as these two state variables. If the state variables with the fastest and the slowest dynamics are denoted by x_f and x_s, and their corresponding reference values are given by $x_{f,ref}, x_{s,ref}$, the control objective is to make (1.1) valid at any time instant.

$$x_f - x_{f,ref} = K(x_s - x_{s,ref}). \tag{1.1}$$

In (1.1), K is a control parameter by the aid of which the dynamics of load transient responses in the converter can be controlled. In general, according to the Nyquist Stability Theorem, the settling time associated with a state variable in a converter cannot become less than $2T_s$, in which T_s is the switching period. If this settling time is going to become less than this value, the system will become unstable. Therefore, the settling time associated with x_s can never reach $2T_s$ in normal cases, as the settling time associated with x_f will become less than the stability threshold and the system becomes unstable. However, using the controller proposed in this

dissertation, the value of K in (1) can be selected such that the recovery times associated with x_f and x_s are both equal to $2T_s$. Therefore, the dynamics of x_s which is the output voltage in most cases, can be optimized, without compromising the system stability. The main concepts regarding the proposed controller are reflected in Fig. 1.3.

As Fig. 1.3 illustrates, x_f and x_s in an open loop system reach their steady-state values through different dynamics. However, once the proposed controller is applied to the converter, x_f and x_s both converge to their reference values through similar dynamics. All the other remaining state-variables inherit the dynamical profile of x_f and x_s, in the proposed closed-loop system.

1.3.2 Decoupling Converter Dynamics from the Load

This section presents the approach proposed to improve DC-DC converter dynamics in large load steps. In DC-DC converter applications such as electronic portable devices, the load current values are small and small load steps occur in the system. Therefore, the load resistance values are relatively high enough to damp the disturbances created by small load steps. In DC-DC converter applications with large load steps, however, the maximum load current levels are typically high. This causes the load resistance values to have small values in high level load currents. As a result, the system damping level is low and thus, the disturbances created by large load steps cannot be easily rejected with the existing controllers. In fact, the converter dynamics is a function of load resistance and this degrades the system dynamics in DC-DC converter applications with large load steps.

To solve this problem, this dissertation proposes a controller that decouples the output voltage dynamics from the load resistance value, when the proposed controller is applied to the converter. In fact, a differential equation can be written for the output voltage, when the proposed controller is applied to the converter. The purpose is to eliminate all terms which are functions of the load resistance value in this differential equation. This way, the converter shows a similar behavior for both small and large load steps. Fig. 1.4. presents the main concepts discussed in this subsection. In this figure, v_{in} is the input voltage, v_o is the output voltage, d is the duty cycle, $v_{o,ref}$ is the reference output voltage, R is the load resistance, and e is the output voltage error. The basic concept is to derive a differential equation for the output voltage, $v_o = f(v_{in}, R)$, when the proposed controller is applied to the converter, and to eliminate all terms which are functions of the load resistance value in this differential equation to achieve $v_o = f(v_{in})$ as shown in the figure. This way, the converter shows a similar behavior for both small and large load steps.

1.3.3 Control Approach for Modular Fast Dynamic Load DC-DC converter

This section presents a new distributed control approach for modular ISOP and IPOS DC-DC converters specifically when fast dynamic loads are considered. This approach is extendable to IPOP/ISOS configurations, as well. For a single DC-DC converter in a modular configuration and a specific power flow direction, a converter duty cycle, denoted by d, can be defined such that the transferred power is increased, when d increases. Fig. 1.5(a) shows a Modular ISOP DC-DC Converter System containing N modules and Fig. 1.5(b) shows the general structure of the proposed controller.

In Fig. 1.5, the following notations are used: C_i is the value of DC-link capacitors for different modules, v_{Cj}, $0 < j < N+1$ is the voltage across the DC-link capacitor of the j-th module, N is the number of modules, i_{inj}, $0 < j < N+1$ is the input current of the j-th module, i_{oj}, $0 < j < N+1$ is the output current of the j-th module, C_o is the output capacitor, i_o is the load current, v_{in} is the input voltage, and L_o is the output-side inductor. Also, v_o denotes the output voltage and d_k denotes the duty cycle associated with the k-th module. Moreover, $v_{C,ref}$ and $i_{o,ref}$ denote the reference values for v_{Ci} and i_o, respectively.

Fig. 1.5(b) shows the general controller structure. In this figure, f is a nonlinear function of v_{Ci} and i_o, and one of the control objectives includes regulation of v_{Ci} and i_o. In other words, it is desired to have $v_{Ci} = v_{C,ref}, i_o = i_{o,ref}$, in steady-state conditions. Therefore, at steady-state, $f(v_{Ci}, i_o) = f(v_{C,ref}, i_{o,ref})$. Let us assume that the amount of instantaneous power transferred by the k-th converter is denoted by $p_k(t)$. As it was stated earlier, d_k is defined so that $p_k(t)$ increases by increasing d_k. The proposed controller in Fig. 1.5(b) is composed of two parts: the Nonlinear function error or i.e. $f(v_{Ci}, i_o) - f(v_{C,ref}, i_{o,ref})$, an integrator which forces the error

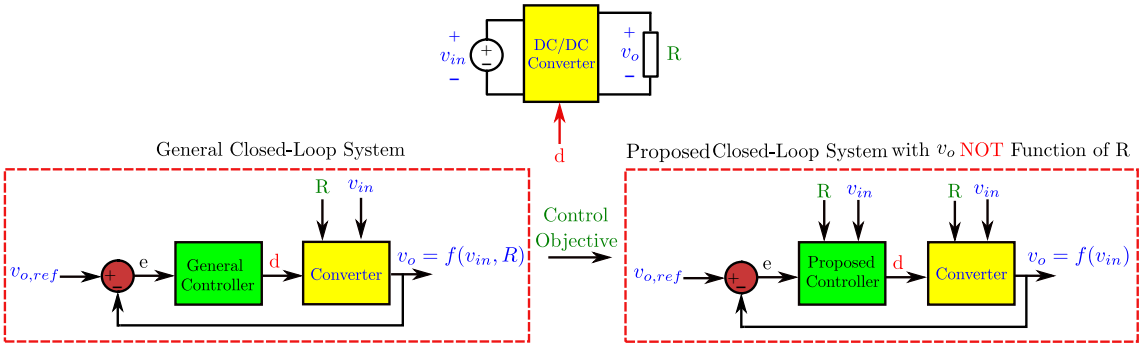


Figure 1.4: Illustration of the Concept of Decoupling Converter Dynamics from the Load

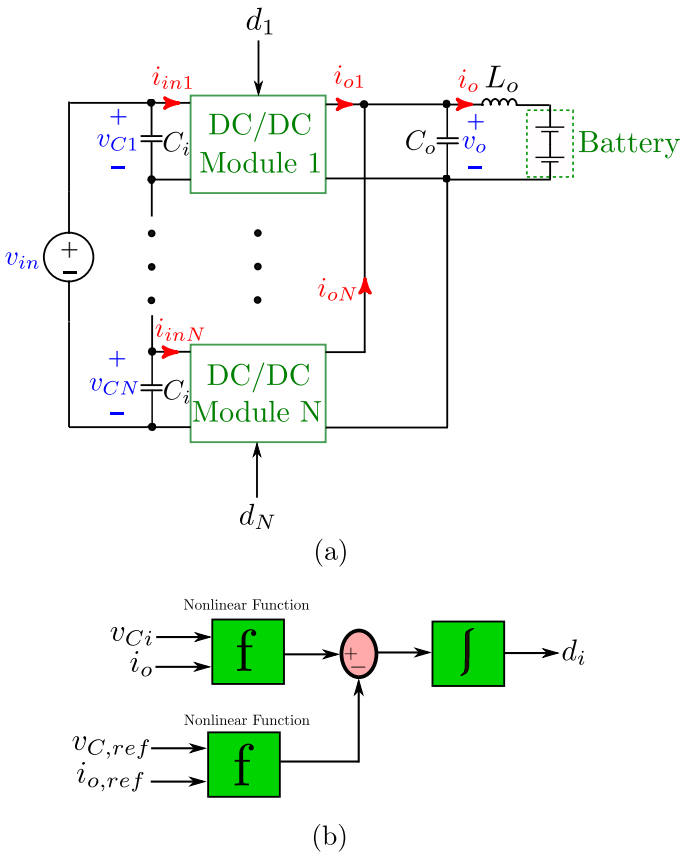


Figure 1.5: (a) ISOP DC-DC Converter System (b) General Controller Structure

generated by the first part to be equal to zero at steady-state. Let us denote the load power by $p_o(t)$ and assume that the power is being transferred from the input side to the battery. In this case, if for example $p_o(t)$ is greater than its reference value, excessive power is being transferred to the load and to reduce this excessive power, every module such as the k-th module needs to adjust its contribution by reducing $p_k(t)$ through d_k reduction. To this end, the function f should be chosen such that the controller properly adjusts d_k. To select the f function, first it should be determined whether each of the controller variables including v_{Ci} and i_o, has a proportional or an inverse relationship with $p_i(t)$, that is the transferred power by the i-th module. For example, in the converter shown in Fig. 1.5(a), i_o is proportional to p_i and v_{Ci} is inversely proportional to p_i. Next, f should be selected such that for example in our discussed case, $f(v_{Ci}, i_o)$ is reduced if there is excessive p_o. This way, if there is extra output power during a transient, the signal integrated to produce d_i will have a negative sign and d_i will be decreased, resulting in the reduction of $p_i(t)$. It is worth mentioning that for an accurate system performance, the f function must be selected in a way that $f(v_{Ci}, i_o) = f(v_{C,ref}, i_{o,ref})$ guarantees $v_{Ci} = v_{C,ref}, i_o = i_{o,ref}$. This way, appropriate power sharing among the modules and voltage/current regulation

are achieved at the same time.

The integrator in the proposed control structure increases the system's robustness and ensures appropriate power sharing among the modules, even in the presence of considerable parameter mismatches among the modules. Also, the proposed controller does not use the values of circuitry parameters, reducing the effect of parameter uncertainties. In the next chapters, it will be shown that the value of the f function is proportional to v_{Ci}. This increases the sensitivity of the f function to the differences between the DC link voltages of different modules. Also, the integrator provides a more robust control performance. So, the combined usage of the f function and the integrator significantly reduces the maximum power mismatches among the modules in the transient period and provides a better power sharing, in the transient period. It is worth mentioning that the proposed controller is applicable to all modular ISOP/IPOS/ISOS/IPOP DC-DC converters, regardless of the topologies used for each module.

1.4 Investigation of Data Center Power Conversion Archietectures

So far in this chapter, a specific data center power conversion archietecture has been inbestigated. This section presents a literature review on other common power distribution architectures in a data center.

One of the conventional power architectures in data centers uses an AC-based system to transfer power from the grid to the data center equipment [10, 109, 11]. In this architecture, a UPS system composed of a rectifier and an inverter convert the grdi voltage to a 100-200V AC voltage [10, 109, 11]. This AC voltage is then applied to ICT (Information and Computer Technology) equipment, including the data center and CPU racks [10, 11]. There are two operational challenges regarding this architecture, which motivates using alternative power architectures for data centers. The first challenge is that the DC nature of UPS batteries does not allow them to be directly connected to ICT equipment, which in turn results in reduced system reliability [10, 11]. The second challenge is the high number of converters required to interface the grid with CPU racks in the data center [10, 11]. In other words, in the AC-based architecture, two rectifiers, one inverter, and one DC-DC converter is required to supply power to CPU racks [10, 11]. This will reduce the efficiency and reliability at the same time [10, 11].

To tackle these challenges, an option is to substitute the AC-based system with a 48V DC data center architecture [10, 11]. The schematic of this system is shown

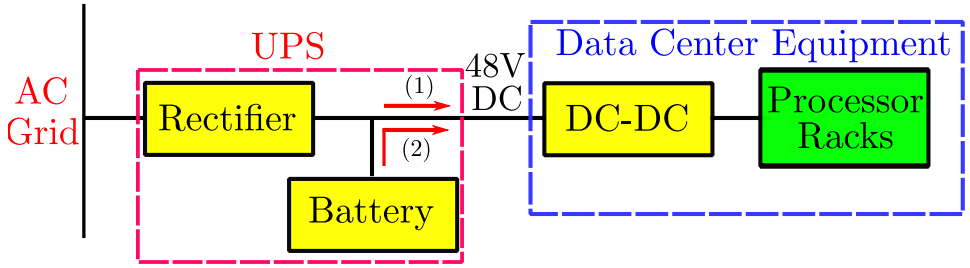


Figure 1.6: Structure of the Power Management System in a 48V DC based Data Center [10, 11] : (1) is for Normal Operation, (2) is for Supply Outage

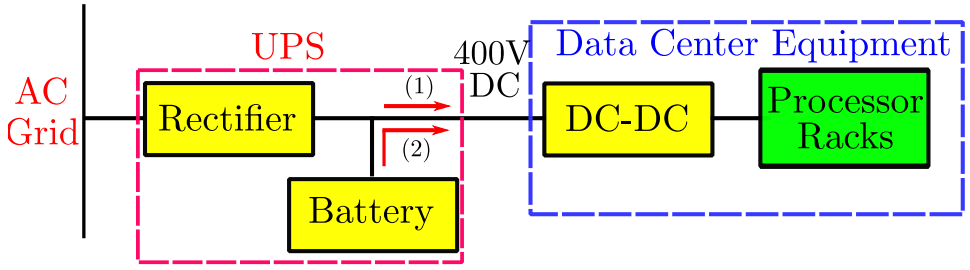


Figure 1.7: Structure of the Power Management System in a HVDC 400V DC based Data Center [10, 11] : (1) is for Normal Operation, (2) is for Supply Outage

in Fig. 1.6 [10, 11].

As Fig. 1.6 shows, the power is transferred to the data center equiment using a UPS system, which is composed of a rectifier and a battery [10, 109, 11]. During normal operational mode, the grid supplies power to the load side [10, 109, 11]. However, as soon as there is a grdi outage, the battery starts transferring power to the data center equiement [10, 109, 11]. In this regard, the arrows marked as (1) and (2) in Fig. 1.6 correspond to normal operation mode and supply outage mode, respectively. It is known that the total load power demands in data center applications is constantly increasing, Therefore, if the DC link voltage is set at a low voltage of 48V, the bus current will become too high, necessiating installation of larger-sized cables with more copper usage [10, 11]. Therefore, the conventional trend is to substitute the power conversion system shown in Fig. 1.6 with a HVDC 400V system [10, 109, 11]. This way, the high voltage DC link causes the bus current to decrease, leading to easier cable installations [10, 11]. The schematic of the HVDC 400V DC power architecture for data center application is shown in Fig. 1.7 [10, 11]. This figure corresponds to a case in which the load voltages are not required to vary in a narrow range [10, 11]. It is worth mentioning that in a HVDC data center, the DC link may sometimes be selected as 380V instead of 400V [109].

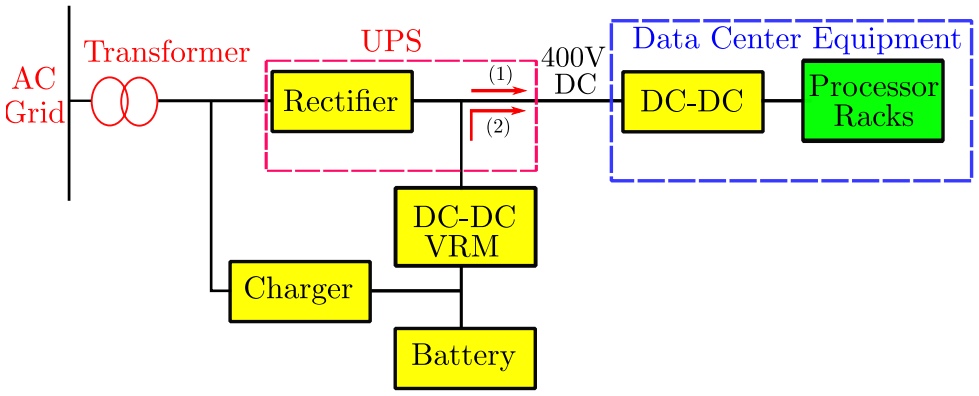


Figure 1.8: Structure of the Power Management System in a HVDC 400V DC based Data Center with Narrow Variation Range for Load Voltages [10, 12] : (1) is for Normal Operation, (2) is for Supply Outage

As it is evident, the basic features of a 400V HVDC system is the same as the 48V DC system [10, 11], except for lower bus currents and installation costs in the 400 V HVDC system [10, 11]. If the load voltages need to be restricted in a narrow variation range, the data center architecture of 400V HVDC needs to be modified as shown in Fig. 1.8 [10, 12]. In this architecture, the 400V HVDC bus is controlled using a DC-DC voltage regulator [10, 12].

One of the important aspects of power converters in data center applications is their efficiency [110]. The efficiency of these converters are degraded when load voltages are of low levels [110]. Therefore, a method proposed in the literature to handle this situation is to control th amount of power transferred to the load from the grid adaptively, using data center load conditions in real time [110]. This way, the performance of the data center is further optimized [110].

1.5 Research Objectives

This research aims to propose alternative controllers to improve the performances of single and modular DC-DC converters in transient and steady-state conditions. The main goals of this research can be summarized as follows:

1. To develop a new controller to improve the load transient responses of DC-DC converters for small load steps with fast dynamics. The load transient response improvements are going to be achieved for DC-DC converters used in Stage 3 converters in the power management system of a data center shown in Fig. 1.1. They can also be used in low-power applications such as portable electronic devices, and etc.

2. To propose a controller to enhance DC-DC converter dynamics and increase

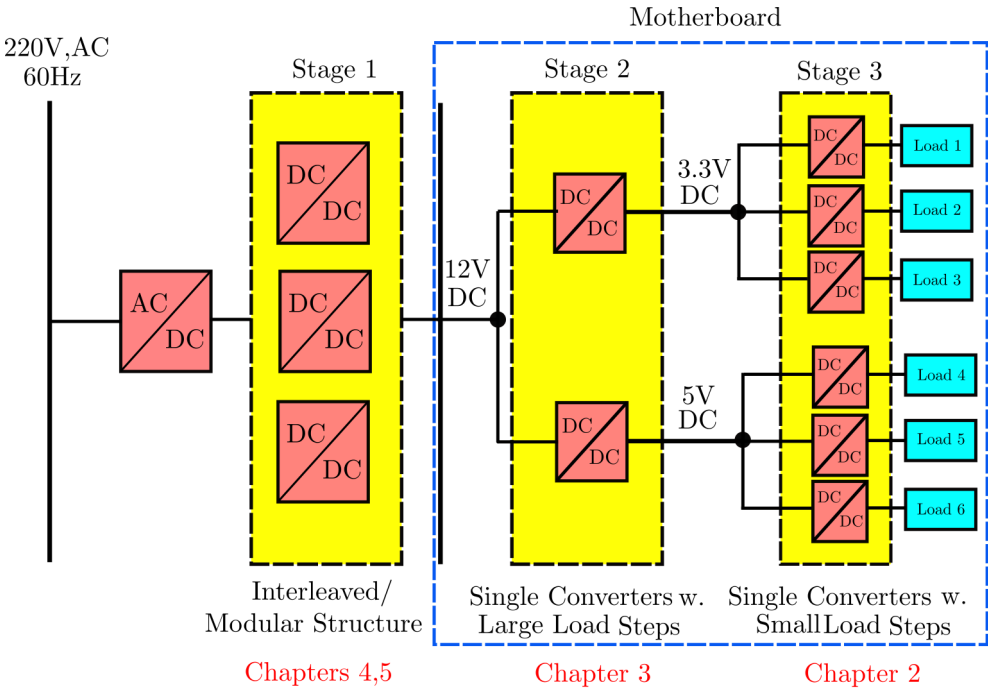


Figure 1.9: Relevance of Dissertation Chapters and Different Power Conversion Stages in a Data Center

system's damping levels in large load steps. The dynamic enhancements are going to be accomplished for DC-DC converters used in Stage 2 of the power management system of a data center as shown in Fig. 1.1.

3. To present a control system for modular ISOP/IPOS/ISOS/IPOP DC-DC Converters. Specific goals include improving power sharing among modules in transient and steady-state conditions, appropriate voltage/current regulation, and reducing the sensitivity of the control system's performance to parameter mismatches among the modules and parameter uncertainties in the system. The presented control scheme can be used in the Stage 1 of the power management system of a data center, as shown in Fig. 1.1.

1.6 Dissertation Outline

This section provides an outline of chapters 2-5 in this dissertation. In Chapter 2, a new controller is proposed to improve the load transient responses of DC-DC converters in Stage 3 of the power management system in a data center, as shown in Fig. 1.9. This chapter provides simulation and experimental results to validate the controller's performance. Also, comparisons are made between the performances of the proposed controller and other controllers in the literature.

Chapter 3 proposes a new controller to enhance system dynamics in DC-DC converters of Stage 2 in Fig. 1.9. In this chapter, the controller's performance is validated by simulation and experimental results. Also, the controller's performance is compared with other existing ones, to show the effectiveness of the proposed controller.

An new controller is proposed in Chapter 4, to improve the performances of modular ISOP/IPOS DC-DC converters, in terms of voltage/current regulation, power sharing among the modules, and load transient responses in the system. Simulation and experimental results are provided in this chapter to validate the controller s performance. Also, comparisons are provided to illustrate the suitable performance of the controller. The proposed controller is used in Stage 1 converters in Fig. 1.9.

In chapter 5, the controller proposed in chapter 4 is applied to ISOS and IPOP DC-DC converters, to show the effectiveness of the controller for these structures. Also, a framework is proposed to analyze the closed-loop response of modular DC-DC controllers. The presented framework is then formulated for ISOS Dual Active Bridge converters controlled by the system proposed in chapter 4, as an example.

Finally, chapter 6 will provide a summary of the dissertation and will suggest directions towards which this research can be continued and extended.

Chapter 2

A Novel Control Approach to Achieve Fast Load Transient Responses in DC-DC Converters

This chapter proposes a controller to achieve optimal dynamics for point-of-load (POL) connected DC-DC converters in power management system of a data center. As discussed in Chapter 1, these converters belong to power conversion stage 3 in a data center and frequently deal with small load steps. The proposed controller in this chapter is developed based on the concept of Identical States Dynamics Control, which is discussed in section 1.3.1 of Chapter 1. The proposed controller can achieve load transient responses with recovery times of less than one switching cycle and low overshoot/undershoot levels. From the discussions in section 1.2.1, it can be concluded that the compromises between control objectives, controller stability, and the possibility to design the controller systematically, are among the most important concerns in designing a controller to achieve optimum load transient responses. To address these concerns, this chapter proposes a design methodology and a new controller, which is specifically constructed to provide optimum load transient responses for DC-DC converters dealing with small load steps. This controller is developed for two different operation modes: Continuous Conduction Mode (CCM), and Discontinuous Condition mode (DCM). It is shown that the load transient responses are negligible in CCM, and fast transient responses with small overshoots/undershoots are observed in DCM. Unlike some of the existing methods, the proposed controller does not require any additional auxiliary components, which reduces the total cost of the converter. Using the proposed controller, there is no steady-state error in the converter's output voltage and the voltage ripple levels always remain in the desired range. Also, the proposed controller has a simple structure and is robust against various uncertainties in the converter and it is shown that the values for

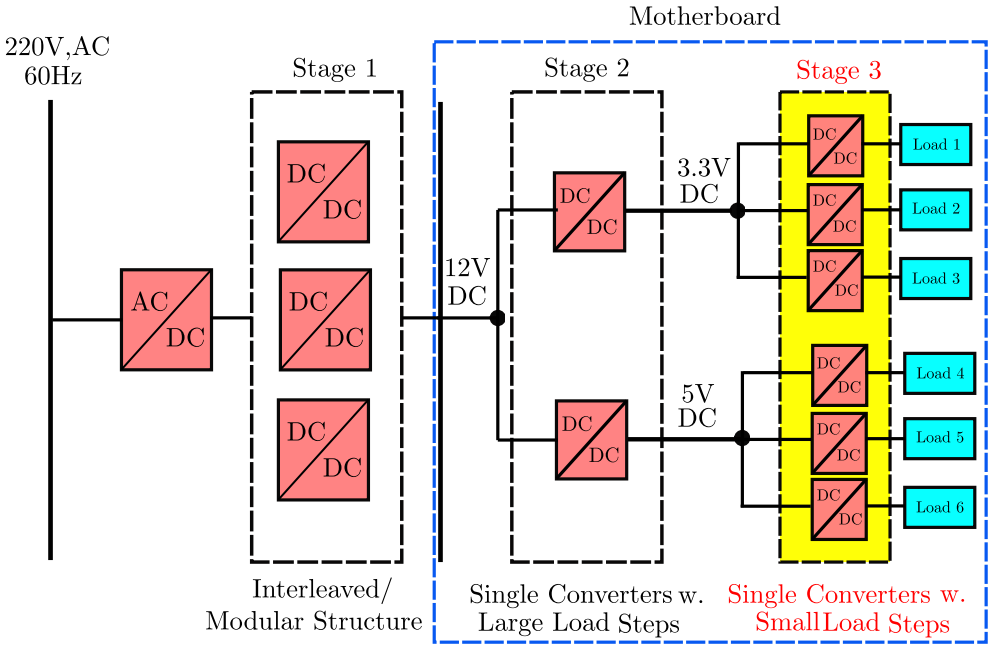


Figure 2.1: Load-Connected DC-DC Conversion Stage i.e. Stage 3 Highlighted by Yellow in Data Center Power Management System

voltage recovery time and overshoot/undershoot levels are optimal. Moreover, a systematic approach is proposed for controller design, that provides closed-form and optimal solutions. The proposed controller design procedures are applicable and can be extended to different types of converters, considering the stability and parameter variations.

This chapter is organized as follows: First, the controller's derivation, analyses, and design steps are discussed for the buck converter in CCM and DCM modes of operation. Next, simulation results verifying the effectiveness of the proposed controller are presented and it is shown that the controller can be applied to other DC-DC converters, as well. Finally, experimental results validating the controller's performance are provided.

2.1 Chapter Challenges, Literature Review, and Contributions

2.1.1 Challenges

The architecture of the power management system of a data center is shown in Fig. 2.1, in which the load-connected DC-DC conversion stage is highlighted by yellow color. As mentioned in the introduction chapter, DC-DC converters in the

load-connected power conversion stage of a data center, supply power to different load types such as processors, memories, etc. These loads operate in various modes and power levels, including idle and full-power operational modes. At the points of the load, transitions among power levels and operational modes occur stochastically at high frequencies. These changes are seen as load steps by DC-DC converters in the load-connected power conversion stage. The output voltage levels of these DC voltage regulators deviate from their reference values during the load steps discussed. As a result, DC voltage regulators need high-performance control systems to restore their default values with the smallest possible recovery time and overshoot/undeshoot levels. Achieving both minimum overshoot and undershoot levels is necessary to avoid load damages and operational interruptions due to overvoltages and voltage drops. Also, to minimize controller-related limitations on operational speed of processo loads, it is important to achieve the minimum possible recovery times. In summary, this chapter aims to propose a new controller to optimize converter dynamics in power conversion stage 3 highlighted in yellow in Fig. 2.1.

2.1.2 Literature Review

The existing approaches to achieve enhanced load step dynamics for load-connected DC voltage regulators in data centers are already discussed in detail in section 1.2.1. As a summary of this section, the existing methods include using auxilary circuits (ex. [18]), popular controller classes (ex. Model Predictive Control in [34]), and high performance controllers specifically designed for load step dynamics enhancement (ex. [19]). The proposed auxiliary circuits modify the converter topology during load steps, to increase the variation rate of inductor current and reduce recovery times [18, 31, 32, 33]. Although these auxiliary circuits improve the dynamical performance of the converter, they increase the cost and complexity of the system. Popular nonlinear controller classes such as model-predictive controllers (MPC) [34],[35], adaptive controllers [36], and intelligent controllers [37] are reported to effectively enhance load step dynamics in the literature. However, lacking of systematic design approaches [39], stability issues, control system complexity, and compromises between recovery times and overshoot/undershoot levels are among the challenges faced while using these controllers. Finally, high-performance controlelrs including Active Ramp Tracking Control [19], I^2 control [38], peak-current controller [40], constant on-time controllers [43], and time optimal controllers [44], are specifically designed in the literature to achieve improved load step dynamics. Achieving fast load transients [19], and wide load range capabilities [40] are among the benefits these controllers provide. However, steady-state errors [19], larger ripple levels [40],

reduced robustness [41], and finally controller performance degradation in large load steps, are among the existing challenges associatesd with these controllers.

2.1.3 Targets and Contributions

The current chapter in this dissertation aims to propose a controller for load-connected DC voltage regulators in a data center, to tackle the challenges mentioned in this section. The main target of the chapter is to propose a controller which can reach the following targets:

1. Minimizing load step recovery times in power conversion stage 3 of a data center i.e. load connected converters.

2. Minimizing overshoot/undershoot levels in load steps.

3. Minimizing compromises between recovery times and overshoot/undershoot levels.

4. Guaranteeing system stability.

and finally,

5. Possibility to design the controller systematically.

Contributions: This chapter proposes a controller to achieve optimal dynamics for point-of-load (POL) connected DC-DC converters in power management system of a data center. As discussed in Chapter 1, these converters belong to power conversion stage 3 in a data center and frequently deal with small load steps. The proposed controller in this chapter is developed based on the concept of Identical States Dynamics Control, which is discussed in section 1.3.1 of Chapter 1. The proposed controller can achieve load transient responses with recovery times of less than one switching cycle and low overshoot/undershoot levels. From the discussions in section 1.2.1, it can be concluded that the compromises between control objectives, controller stability, and the possibility to design the controller systematically, are among the most important concerns in designing a controller to achieve optimum load transient responses. To address these concerns, this chapter proposes a design methodology and a new controller, which is specifically constructed to provide optimum load transient responses for DC-DC converters dealing with small load steps. This controller is developed for two different operation modes: Continuous Conduction Mode (CCM), and Discontinuous Condition mode (DCM). It is shown that the load transient responses are negligible in CCM, and fast transient responses with small overshoots/undershoots are observed in DCM. Unlike some of the existing methods, the proposed controller does not require any additional auxiliary components, which reduces the total cost of the converter. Using the proposed controller, there is no steady-state error in the converter's output voltage and the voltage rip-

ple levels always remain in the desired range. Also, the proposed controller has a simple structure and is robust against various uncertainties in the converter and it is shown that the values for voltage recovery time and overshoot/undershoot levels are optimal. Moreover, a systematic approach is proposed for controller design, that provides closed-form and optimal solutions. The proposed controller design procedures are applicable and can be extended to different types of converters, considering the stability and parameter variations.

2.2 Chapter Main Control Concept

This section discusses the general concepts associated with the controller proposed in this chapter. In a closed-loop power electronic converter, the control input, which is typically a duty cycle or a phase-shift, starts getting updated as soon as the converter output level deviates from its reference value. Every such update in the control input is later on processed by a number of converter components, to reach the output and contribute to output level modification. These converter components, including inductors and capacitors, increase the dynamical order of the converter. Therefore, there is some time delay between control input getting updated based on output level error, and the consequent output level modification. This time delay on its own, reduces the dynamical speed of the system and lets the output level vary independently from the control input updates, for larger amounts of time. Therefore, this phenomenon results in not only larger recovery times, but also increased overshoot/undershoot levels.

To reduce this time delay, or equivalently enhance converter dynamics, a possible approach is to reduce the converter dynamical order. In other words, if the control input is set to result in identical dynamical profiles for all converter state variables, this time delay is eliminated and the transient response is improved. In conclusion, the control objective in this chapter is to achieve (2.1) for each pair of state variables (x_i, x_j).

$$x_i - x_{i,ref} = K(x_j - x_{j,ref}). \tag{2.1}$$

In (2.1), $x_{i,ref}$ and $x_{j,ref}$ are the reference values for x_i and x_j, respectively. As the proposed controller results in identical dynamics for all state variables of the converter, the presented controller is called Identical State Dynamics Control in this dissertation. For the fastest and slowest converter state variables denoted by x_f and x_s, Fig. 2.2 illustrates the concept of Identical State Dynamics Control.

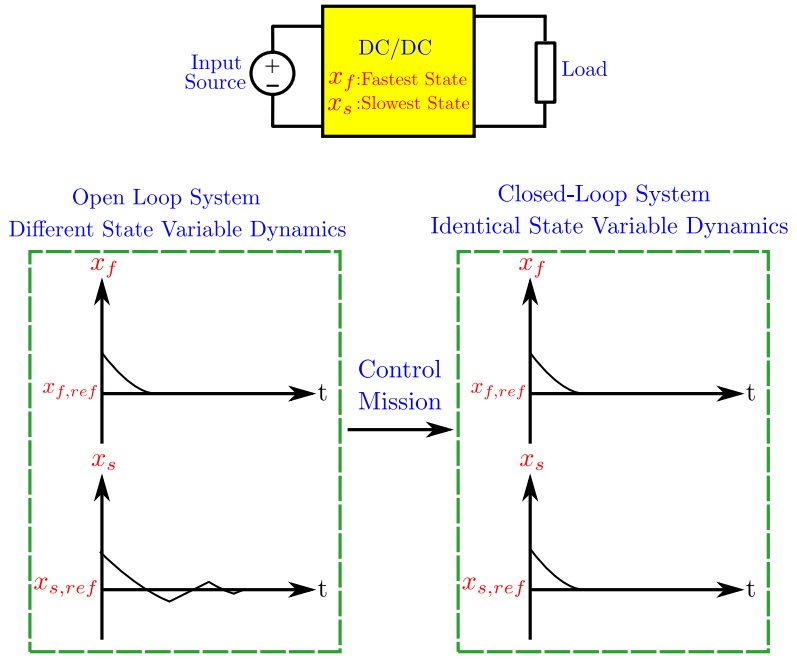


Figure 2.2: Illustration of the Concept of Identical State Dynamics Control

2.2.1 Application of Identical States Dynamics Control in a 2nd Order LTI System

in this part, the goal is to show why the proposed concept of identical state dynamics control improves system dynamics. For simplicity, this concept is applied to a 2nd order LTI system with a single control input. If the state variables of a 2nd order LTI system are denoted by x_1 and x_2, and the control input is denoted by u, the state-space representation of the system is given by:

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} B_1 \\ B_2 \end{bmatrix} u. \tag{2.2}$$

According to the concept of identical states dynamics control, the target is to set u such that:

$$x_1 - x_{1,ref} = K(x_2 - x_{2,ref}). \tag{2.3}$$

In (2.3), $x_{1,ref}$ and $x_{2,ref}$ correspond to the reference values for their associated state variables. From (2.3), the relationship between $\dot{x_1}$ and $\dot{x_2}$ can be obtained as:

$$\dot{x_1} = K\dot{x_2}. \tag{2.4}$$

From (2.2) and (2.4), the control law is obtained as:

$$u = \frac{(A_{11} - KA_{21})x_1 + (A_{12} - KA_{22})x_2}{KB_2 - B_1}. \tag{2.5}$$

Using (2.2) and (2.5), the dynamics of the closed-loop system can be expressed by:

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \end{bmatrix} = \begin{bmatrix} \frac{K(A_{11}B_2 - b_1A_{21})}{KB_2 - B_1} & \frac{K(A_{12}B_2 - B_1A_{22})}{KB_2 - B_1} \\ \frac{A_{11}B_2 - b_1A_{21}}{KB_2 - B_1} & \frac{A_{12}B_2 - B_1A_{22}}{KB_2 - B_1} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}. \tag{2.6}$$

The eignevalues of the closed-loop system in (2.6) can be obtained as 0 and $\lambda_{cl} = \frac{K(A_{11}B_2 - B_1A_{21}) - B_1A_{22} + B_2A_{12}}{KB_2 - B_1}$. Considering the fact that an eignevalue of zero is associated with a constant DC level, $x_1 = x_{1,ref} + a_1 e^{\lambda_{cl}t}$ and $x_2 = x_{2,ref} + a_2 e^{\lambda_{cl}t}$. In other words, the closed-loop system is equivalent to a first order system with a time constant of $\frac{-1}{\lambda_{cl}}$. By appropriate selection of K, the dynamical speed of the closed-loop system can be adjusted.

2.3 Controller Formulation and Basic Concepts

In this section, to clarify the basic concepts, the proposed controller is investigated in a buck converter. For this purpose, the derivation, analysis, and design procedures of the proposed controller are discussed in a regular buck converter for CCM and DCM operating modes.

2.3.1 Proposed Controller in CCM

Principles and Derivation

Fig. 2.3 illustrates the circuit schematic of a buck converter and the proposed controller's block diagram. In this figure, v_o is the output voltage, i_o load current, i_L inductor current, d the duty cycle, and v_{in} is the input voltage. Moreover, $v_{o,\text{ref}}$ denotes the reference value of the output voltage.

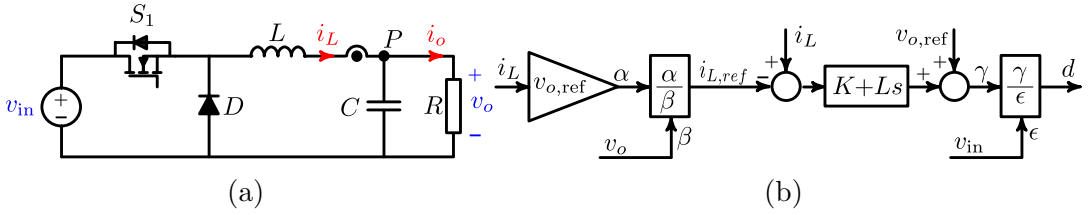


Figure 2.3: (a) Schematic of regular buck converter and (b) proposed controller in CCM

In the steady-state condition, the mean value of inductor current is equal to the load current ($I_L = I_O$ and it is desired that $v_o = v_{o,ref}$. Thus, $i_{L,ref}$ which is the reference value for the inductor current must be equal to $\frac{v_{o,ref}}{R}$, which is the load current in steady-state conditions. It is worht mentioning that the value of R is

measured by $\frac{v_o}{i_L}$, since the proposed controller makes the inductor current reach the load current in just one switching cycle. THis issue is clarified in the next subsection. Once $i_{L,ref}$ is calculated by the controller, it is subtracted from the inductor current and this error is fed into a proportional-derivative controller and the result is added to $\frac{v_{o,ref}}{v_{in}}$, which is the nominal voltage gain of the buck converter at steady state. The feedback in this structure compensates for the parameter uncertainties and parasitic components and regulates the output voltage.

At the instant of a load change, the controller changes the duty cycle to make the output voltage equal to its reference value. Before the output voltage sees the effect of the duty cycle, the inductor current is affected by the duty cycle change. Moreover, the inductor current passes through a parallel RC branch, in order to create the output voltage waveform. Since the impedance of a parallel RC branch converges to zero at high frequencies, this parallel branch acts as a low-pass filter, and the output voltage is varied on average by the low-frequency components of the inductor current. Therefore, the output voltage reaches its reference value slower than the inductor current. A faster dynamics for the output voltage can be achieved by setting the duty cycle such that the output voltage ripple is equal to the inductor's current ripple multiplied by a constant K. This way, the output voltage inherits the fast response of the inductor's current to a load and duty cycle change. This is consistent with the concept of Identical States Dynamics Control introduced in section 1.3.1. Therefore, the proposed controller is based on the idea of achieving

$$v_o - v_{o,\text{ref}} = K(i_L - i_{L,\text{ref}}), \tag{2.7}$$

where

$$i_{L,\text{ref}} = \frac{v_{o,\text{ref}}}{R} = \frac{i_L v_{o,\text{ref}}}{v_o}. \tag{2.8}$$

It must be mentioned that the main objective of the controller is to make i_L reach i_o (which are equal in steady-state), in just one switching cycle. So, it is assumed that $v_o = Ri_L$ instead of $v_o = Ri_o$. Once the control law is derived, a mathematical proof is provided to prove that this objective is satisfied.

The KVL and state-space averaging for the buck converter can be utilized to obtain the basic equation of the converter, which is expressed as:

$$v_{\text{in}}d - v_o = L\frac{di_L}{dt}. \tag{2.9}$$

It is assumed that at $t = 0$, there is a load step change and therefore, for all $t > 0$, $i_{L,\text{ref}}$ is constant and its time-derivative is zero. It is worth mentioning that this assumption does not negatively affect the generality of the proposed controller and

the method can be well applied to any other load change profile, as well. The reason is that any load change profile can be seen as a series of consecutive small instantaneous load steps. Consequently, $\frac{d}{dt}i_{L,\text{ref}} = 0$, and (2.7), (2.8) and (2.9) are combined to derive the proposed control law in CCM as:

$$d = \frac{L\dfrac{d(i_L - i_{L,\text{ref}})}{dt} + K(i_L - i_{L,\text{ref}}) + v_{o,\text{ref}}}{v_{\text{in}}}. \tag{2.10}$$

Verification of Assumptions in Controller Derivation

In the previous subsection, it was assumed that i_L reaches i_o in just one switching cycle. Now, the objective is to show that using the control law expressed by (2.10), this is indeed valid. Denoting the deviations of i_L, v_o, and d from their steady-state values by $\tilde{v_o}$, $\tilde{i_L}$, and $\tilde{d}$, and noting that the steady-state values for these variables are $\frac{v_{o,ref}}{R}$, $v_{o,ref}$, and $\frac{v_{o,ref}}{v_{in}}$, as well as using (2.8), lead to:

$$v_{in}\tilde{d} = \frac{L}{v_{o,ref}}\frac{d}{dt}[\tilde{v_o}\tilde{i_L}] + \frac{L}{R}\frac{d\tilde{v_o}}{dt} + \frac{K\tilde{v_o}}{R}. \tag{2.11}$$

The controller parameter and power circuit components must be designed properly such that $\tilde{v_o} << v_{o,ref}$ during a load transient period. If this condition is satisfied, writing KCL in node P in Fig. 2.3 leads to:

$$LCR\frac{d^2\tilde{v_o}}{dt} + (R - K)\tilde{v_o} = 2L\frac{d\tilde{v_o}}{dt}\frac{\tilde{v_o}}{v_{o,ref}}. \tag{2.12}$$

Assuming that $\frac{\tilde{v_o}}{v_{o,ref}}$ is small enough, the right hand-side of (2.12) can be substituted by 0. In this way, $\tilde{v_o}$ and $\tilde{i_L}$ become sinusoidal signals with zero means after one switching cycle and they act as steady-state ripples. This means that using the proposed controller, the system reaches its steady-state condition in just one switching cycle and therefore, i_o can be substituted by i_L in (2.8). To satisfy $\tilde{v_o} << v_{o,ref}$, the power circuit and the controller should be designed based on a "Harmonic Analysis" in section 2.3.1. It is shown in this section that for having small ripple levels, the values of $|K|$ and C must be large enough and the inductance L must have a small value.

State Space Analysis

Combining (2.8) , (2.9), and (2.10), result in the state-space model of:

$$\frac{di_L}{dt} = \frac{v_o}{v_{o,\text{ref}}}\left[\frac{v_{o,\text{ref}} - v_o}{L} - \frac{Ki_L(v_{o,\text{ref}} - v_o)}{v_o L} + \frac{i_L v_{o,\text{ref}}}{C{v_o}^2}(i_L - \frac{v_o}{R})\right] \tag{2.13}$$

$$\frac{dv_o}{dt} = \frac{-v_o}{RC} + \frac{i_L}{C}. \tag{2.14}$$

The equilibrium point of the system, $({i_L}^*, {v_o}^*)$, is found as $(\frac{v_{o,\text{ref}}}{R}, v_{o,\text{ref}})$. By linearizing the obtained non-linear state-space model around this equilibrium point, the Jacobian matrix associated with the system is:

$$J = \begin{bmatrix} \frac{1}{RC} & \frac{-R^2C+KRC-L}{R^2LC} \\ \frac{1}{C} & \frac{-1}{RC} \end{bmatrix}. \tag{2.15}$$

Both eigenvalues of the Jacobian matrix are on the imaginary axis. This can mean an oscillation and there are no damping effects in the system. If the amplitudes of these oscillations are minimized using an appropriate selection of inductor and capacitor and accurate controller design, these voltage oscillations can be treated as output voltage ripples.

Harmonic Analysis

As mentioned earlier, the output voltage has constant oscillations that appear as ripples. To find voltage ripple levels, both i_L and v_o can be approximated by their first-order harmonics. In other words, these signals are assumed to have dc components (that is the equilibrium point of the system), and sinusoidal components whose amplitudes and frequencies are unknown. The phase difference between these sinusoidal ripples is also unknown. In other words, v_o and i_L are expressed as:

$$v_o = v_{o,\text{ref}} + V_d \sin(\omega_0 t),\ \ i_L = \frac{v_{o,\text{ref}}}{R} + I_d \sin(\omega_0 t + \phi). \tag{2.16}$$

By substituting these into the state-space equations, the output voltage ripple level (V_d) is obtained as:

$$V_d = \sqrt{\frac{2{v_{o,\text{ref}}}^2 - 0.5}{\frac{-KRC}{2L} - 0.25}}. \tag{2.17}$$

The following observations may be made from (2.17): (i) to have low voltage ripple levels, the inductor L must have a small value; (ii) the value of C should be large enough to keep the output voltage ripple low; and (iii) the value of K should be chosen according to the desired voltage ripple level. Frequency and amplitude of the output voltage ripple can be obtained respectively by (2.12) and (**??**) and these equations are verified by the simulations and experimental results. Also note that K in the proposed controller has a negative value.

Case-Study: In order to show the accuracy of equation (2.17), let us consider a buck converter with an input voltage of 3.3V, an output voltage of 1.8V, an inductor of 800nH, a capacitor of 100μF, a load resistance of 1.8Ω, and a switching frequency

of 900KHz. The value of the control parameter K is changed within the range of $[2, 200]$. The values of V_d obtained by (2.17) and computer simulations are compared in Fig. 2.4. As this figures shows, there is a good consistency between the simulation

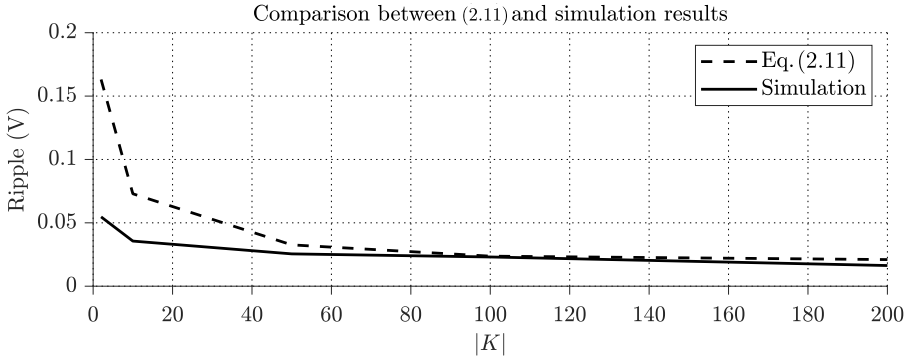


Figure 2.4: Comparison between the theoretical and simulation values of ripple Levels

results and the values obtained by (2.17) for most of K variation range. Even when this is not very accurate, the predicted values are greater than the actual ones and a reliable controller design can always be achieved.

Design Procedure in CCM

Step 1: Find the value of L at which the converter will operate at the boundary condition. The designed value of the inductor L must be chosen slightly larger than this value. According to (2.17), the inductor size should be small to keep voltage ripple levels low.

Step 2: From (2.17), it can be observed that the higher the variable $|K|$ is selected, the less the ripple levels become and hence, a smaller-sized capacitor is required. However, $|K|$ cannot exceed a certain limit, as a very large $|K|$ saturates the duty cycle during a transient. Considering this issue and (2.10), the maximum possible value for $|K|$ is given by $\frac{v_{\text{in}}-v_{o,\text{ref}}}{i_{o,\max}-i_{o,\min}}$, which corresponds to the load current changing from the minimum load current, $i_{o,\min}$, to the maximum load current, $i_{o,\max}$. The value of K is chosen slightly less than this threshold to ensure system robustness in all circumstances.

Step 3: Based on the values chosen for the inductor and K, a suitable value for C is chosen according to (2.17), to maintain the output voltage ripple at a desired level.

In Fig. 2.5, a flowchart diagram corresponding to these design steps is provided. In this figure, $v_{\text{in},\max}$ and $v_{\text{in},\min}$ show the maximum and minimum input voltages, $i_{o,\min}$ and $i_{o,\max}$ the minimum and maximum load currents, v_d the ripple level, and

R the load resistance. In Fig. 2.5, L is calculated such that the converter works in the border line between CCM and DCM, and C is calculated by (**??**).

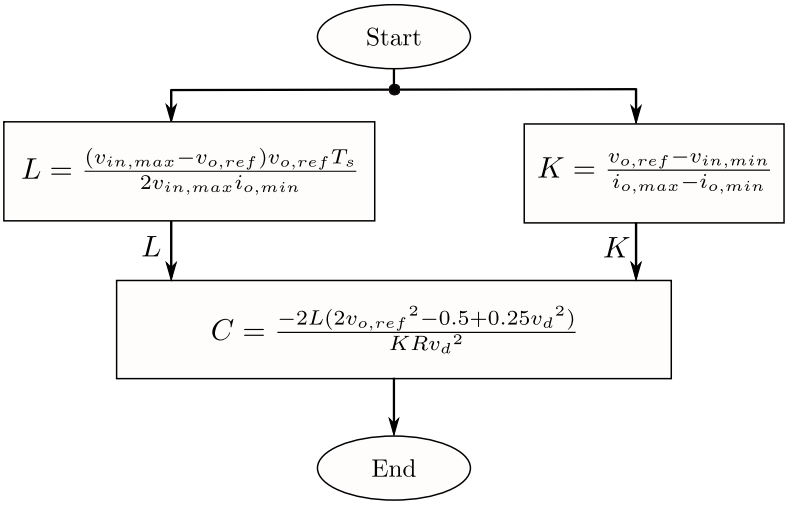


Figure 2.5: Flowchart of controller and power circuit design steps in CCM

2.3.2 Stability Analysis in CCM

The stability analysis for the proposed controller in CCM is provided in [111]. In this analysis, Equivalent Series Resistances (ESR) of r_L and r_C are considered, for the inductor and the capacitor, respectively. Further details are provided in [111]. In the following, a case-study is presented to showcase the stable operation of the controller in CCM.

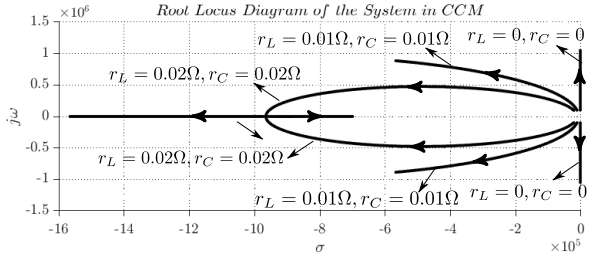


Figure 2.6: Root locus for the proposed controller in CCM

Case-Study: Consider a buck converter with $C = 100\ \mu F, L = 1\ \mu H, v_{in} = 3.3\ V, v_{o,ref} = 1.8\ V, R = 1.8\ \Omega, f_s = 900\ KHz$. If the non-linear system obtained by the stability analysis in [111] is linearized around its equilibrium point, loci of the system poles for K values ranging from [-200,0] are as shown in Fig. 2.6. Different r_C and r_L values change the system poles, but they are always in the negative half of s-plane. According to the Nyquist Theorem and the fact that the sampling frequency is equal to the switching frequency, the real part of system poles cannot

be made less than $\frac{-f_s}{2}$. Therefore, to ensure the system's stability, value of the controller parameter K can be designed through the root-locus provided in Fig. 2.6.

2.3.3 Proposed Controller in DCM

In the previous subsection, it was shown that if the control law in CCM is set to make the output voltage ripple equal to a factor of the inductor's current ripple, the converter will have a fast load transient response. In this section, the same concept is extended to DCM.

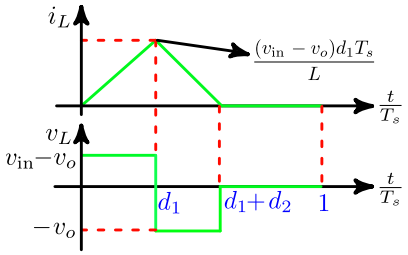


Figure 2.7: Inductor current's waveform in DCM within one switching cycle

Principles and Derivation

In DCM, the inductor current and voltage waveforms are as shown in Fig. 2.7 where d_1 is the converter duty cycle, d_2 is the fraction of switching period when the switch is off and diode is ON before the inductor current reaches zero, v_L is the inductor voltage, T_s is the switching period. According to volt-second balance principle for the inductor's voltage and Fig. 2.7,

$$(v_{\text{in}} - v_o)d_1 - v_o d_2 = 0. \tag{2.18}$$

Moreover, in the steady state condition, the average value for the inductor's current is equal to the load current, i_o. Using the inductor current waveform shown in Fig. 2.7,

$$i_{\text{avg}} = \frac{(v_{\text{in}} - v_o)d_1 T_s(d_1 + d_2)}{2L} = \frac{v_o}{R}. \tag{2.19}$$

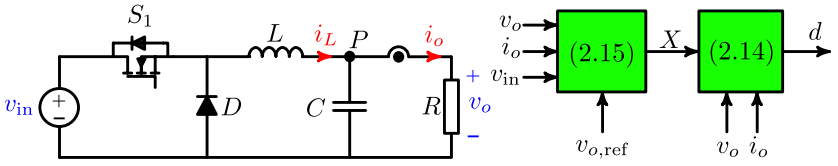
If $\frac{v_o}{v_{\text{in}}}$ is denoted by X, these two equations yield to

$$d_1 = \sqrt{\frac{X^2}{\frac{RT_s(1-X)}{2L}}}. \tag{2.20}$$

The controller's mission is to make sure (2.7) is valid. From the definition of X and (2.7), we get:

$$X = \frac{Ki_o\frac{v_o - v_{o,\text{ref}}}{v_o} + v_{o,\text{ref}}}{v_{\text{in}}}. \tag{2.21}$$

Diagram of the proposed controller in DCM is shown in Fig. 2.8.



(a) (b)

Figure 2.8: (a) Schematic of a buck converter and (b) block diagram of the proposed controller in DCM.

Analysis

In DCM operation, each switching cycle can be divided into three sections as shown in Fig. 2.7. The analysis approach taken here is to solve circuit equations to find the output voltage at the end of a switching cycle as a function of its value at the beginning of that switching cycle. This approach is taken, in order to make a precise model of the converter operating in DCM. It is assumed that at the beginning and ending instants of a switching cycle, the output voltage values are $v_o(0)$ and $v_o(T_s)$, respectively. As the corresponding circuit equations are straightforward to solve, they are not discussed in this chapter and only the final results have been provided. Following the proposed approach, the system model in DCM is obtained as

$$v_o(T_s) = \sqrt{\frac{R^2C}{R^2C+L}P} \tag{2.22}$$

$$\begin{aligned} P = {v_{\text{in}}}^2 + (v_o(0) - v_{\text{in}})^2 + \frac{v_o(0)^2 L}{R^2 C} \\ + 2v_{\text{in}}\left[(v_o(0) - v_{\text{in}})\cos\left(\frac{d_1 T_s}{\sqrt{LC}}\right) - \frac{v_o(0)}{R}\sqrt{\frac{L}{C}}\sin\left(\frac{d_1 T_s}{\sqrt{LC}}\right)\right]. \end{aligned} \tag{2.23}$$

Equations (2.22) and (2.23) represent a first-order non-linear system, where v_o is the state variable. The derivative of this state variable can be estimated through the equation

$$\frac{dv_o(0)}{dt} = \frac{v_o(T_s) - v_o(0)}{T_s}. \tag{2.24}$$

If the system is linearized around $v_o^* = v_{o,\text{ref}}$, which is the equilibrium point of the first order system, the system pole (denoted by λ) will be obtained as:

$$\lambda = \frac{1}{T_s}\left(\frac{N}{\sqrt{D}} - 1\right), \tag{2.25}$$

$$\begin{aligned} N =& (v_{o,\text{ref}} - v_{\text{in}}) + v_{\text{in}}\cos\left(\frac{d_1 T_s}{\sqrt{LC}}\right) + v_{\text{in}}\frac{T_s}{\sqrt{LC}}(v_{o,\text{ref}} - v_{\text{in}}) \\ &\times \left(-\sin\left(\frac{d_1 T_s}{\sqrt{LC}}\right)\right)\frac{2KT_s v_{\text{in}} - KT_s v_{o,\text{ref}}}{4{v_{\text{in}}}^2 L\frac{RT_s}{2L}\left(1 - \frac{v_{o,\text{ref}}}{v_{\text{in}}}\right)^{\frac{3}{2}}}, \end{aligned}$$

$$D = {v_{\text{in}}}^2 + (v_{o,\text{ref}} - v_{\text{in}})^2 + 2v_{\text{in}}(v_{o,\text{ref}} - v_{\text{in}}) \cos\left(\frac{d_1 T_s}{\sqrt{LC}}\right).$$

The recovery time (denoted by t_r) can be obtained as $t_r = \frac{4}{|\lambda|}$ (4 times the system's time-constant).

Case-Study: In order to show the accuracy of the above equations, let us consider a buck converter with an input voltage of 3.3V, a reference output voltage of 1.8V, an inductor of 80nH, a capacitor of 100μF, a switching frequency of 900KHz and a load resistance changing from 3.6Ω to 1.8Ω. Also, $|K|$ varies within the range of $[2, 35]$. The recovery time(t_r) is plotted vs. $|K|$ in Fig. 2.9. This figure shows that the simulation results match the results obtained by (2.25).

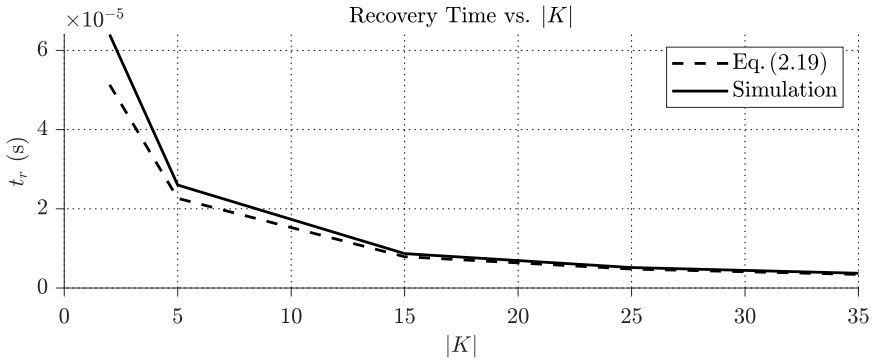


Figure 2.9: Comparison between simulation and analytical results in DCM

2.3.4 Stability Analysis in DCM

Equation (**??**) shows the single pole of the system. Fig. 2.10 is the root locus corresponding to the case study provided in the previous subsection and it shows that the single pole of the system for different K values is always stable.

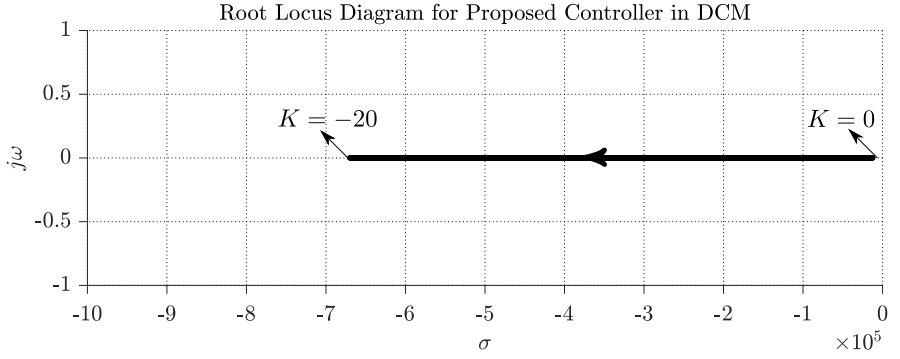


Figure 2.10: Root locus diagram for the controller in DCM

2.3.5 Power Circuit and Controller Design in DCM

From (2.25), it is clear that a smaller K leads to a slower recovery time. According to the Nyquist theorem, the sampling frequency must be at least two times larger than the bandwidth of the system. Assuming the sampling frequency equal to the switching frequency, the system bandwidth is equal to $\frac{1}{t_r}$. Therefore, the recovery time t_r cannot be less than $2T_s$. So, the value of K must be set such that $t_r > 2T_s$ for all operating conditions $v_{\text{in,min}} < v_{\text{in}} < v_{\text{in,max}}$ and $R_{\min} < R < R_{\max}$. Accordingly, it is required to calculate the K value resulting in $t_r = 2T_s$ for each operating point of (v_{in}, R). This is done with the aid of (2.19) and the fact that $t_r = \frac{4}{|\lambda|}$. The K value found in this process is the minimum possible value at any operating point. So, the maximum of these threshold values for K must be found over the entire possible operating points. This maximum is denoted by K_d, which represents the designed value for K. Following this process and using (2.19), along with $t_r = \frac{4}{|\lambda|}$, the following optimization problem $K_d = \text{Argmax } K(v_{\text{in}}, R)$ or equally:

$$K_d = \text{Argmax } \frac{-\sqrt{D} + v_{\text{in}} - v_{o,\text{ref}} - v_{\text{in}} \cos\left(\frac{d_1 T_s}{\sqrt{LC}}\right)}{v_{\text{in}} \frac{T_s}{\sqrt{LC}} \left(v_{\text{in}} - v_{o,\text{ref}}\right) Q} \tag{2.26}$$

is formed, in which

$$Q = \sin\left(\frac{d_1 T_s}{\sqrt{LC}}\right) \frac{2T_s v_{\text{in}} - T_s v_{o,\text{ref}}}{4{v_{\text{in}}}^2 L \frac{RT_s}{2L} \left(1 - \frac{v_{o,ref}}{v_{in}}\right)^{\frac{3}{2}}} \tag{2.27}$$

subject to: $v_{\text{in,min}} < v_{\text{in}} < v_{\text{in,max}}$ and $R_{\min} < R < R_{\max}$. In the above optimization problem, if $\alpha = \frac{d_1 T_s}{\sqrt{LC}}$, (2.28) can be obtained using (2.20) and (2.21):

$$\alpha = \sqrt{\frac{2T_s v_{o,ref}^2}{RC v_{in}(v_{in} - v_{o,ref})}}. \tag{2.28}$$

For a DC-DC converter, the converter parameters and the switching frequency must be selected such that the time constants associated with the output voltage are always much larger than the switching period. This condition must be fulfilled for all different time intervals in a switching period, to make sure that the output voltage is approximately constant. In a buck converter operating in DCM, the inductor current is zero in the last interval of a switching cycle. Therefore, the time constant associated with the output voltage in this case is equal to RC and according to the above discussions, T_s is much smaller than RC. In typical applications, the value of $\frac{2{v_{o,ref}}^2}{v_{in}(v_{in} - v_{o,ref})}$ is small enough such that $T_s << RC$ results in $\alpha \approx 0$, according to (2.22). Therefore, the approximations $\sin\alpha \approx \alpha$ and $\cos\alpha \approx 1$ hold valid. Using these approximations, (2.29) can be obtained as:

$$K_d = Argmax K(v_{in}, R) = Argmax \sqrt{\frac{8LR^3C^2}{{T_s}^3}} \times \frac{(v_{o,ref} - v_{in})}{2v_{in} - v_{o,ref}}. \tag{2.29}$$

From (2.29), it can be seen that $\frac{\partial K}{\partial v_{in}} < 0$ and $\frac{\partial K}{\partial R} < 0$. Therefore, the optimum point $({v_{in}}^*, R^*)$, which corresponds to the introduced optimization problem) is equal to $(v_{in,min}, R_{min})$. As a result, the value of K_d can be obtained as follows:

$$K_d = \sqrt{\frac{8LR_{min}{}^3C^2}{{T_s}^3}} \times \frac{(v_{o,ref} - v_{in,min})}{2v_{in,min} - v_{o,ref}}. \tag{2.30}$$

The design steps are given below and shown in Fig. 2.11.

Step 1: Calculate the inductance value which makes the converter operate at the border line between CCM and DCM. Next, select a value smaller than the obtained inductance.

Step 2: Select the capacitance value such that the output voltage ripple level is low enough.

Step 3: Find the control parameter K by solving the optimization problem represented by (2.26) and (2.27). The solution to this optimization problem is given by (2.30).

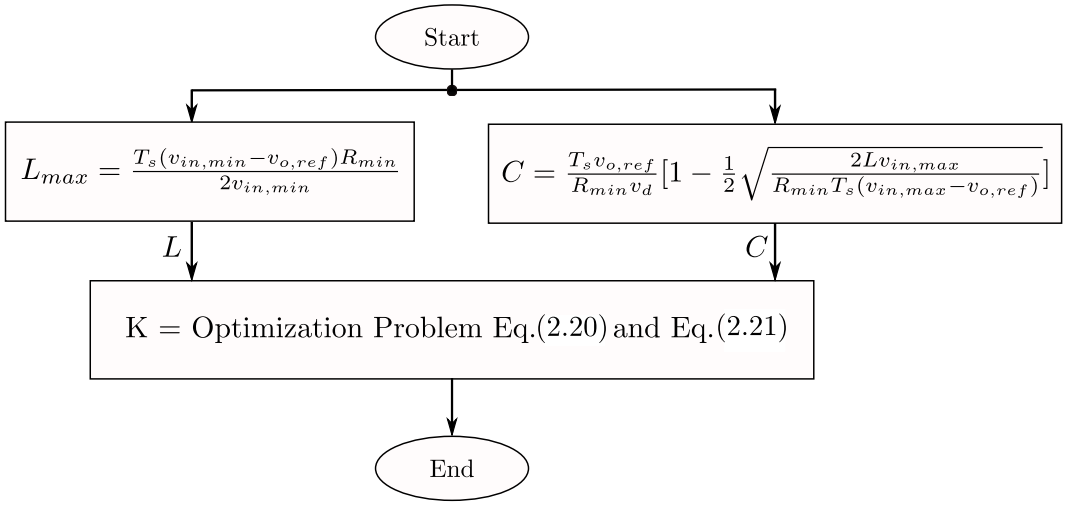


Figure 2.11: Flowchart of controller and power circuit designs in DCM

Case Study: To validate (2.30), a buck converter is assumed with these parameters: $v_{in,min} = 2.3V, v_{in,max} = 3.3V, R_{min} = 1.8\Omega, R_{max} = 18\Omega, v_{o,ref} = 1.8V, L = 80nH, C = 90\mu F, f_s = 900KHz$.This converter is operating in DCM. Using provided results, Fig. 2.12 plots the precise $K(v_{in}, R)$ vs. v_{in} and R. Also, this figure shows the estimated $K(v_{in}, R)$.

Using (2.30) or equivalently the estimated K function in Fig. 2.12, the answer to the optimization problem is $K_d = -26.51$. Also, using the precise K function in Fig. 2.12, the answer is $K_d = -26.44$. Therefore, (2.30) can be used to accurately design K_d. It is worth mentioning that according to Fig. 2.12, the precise K function

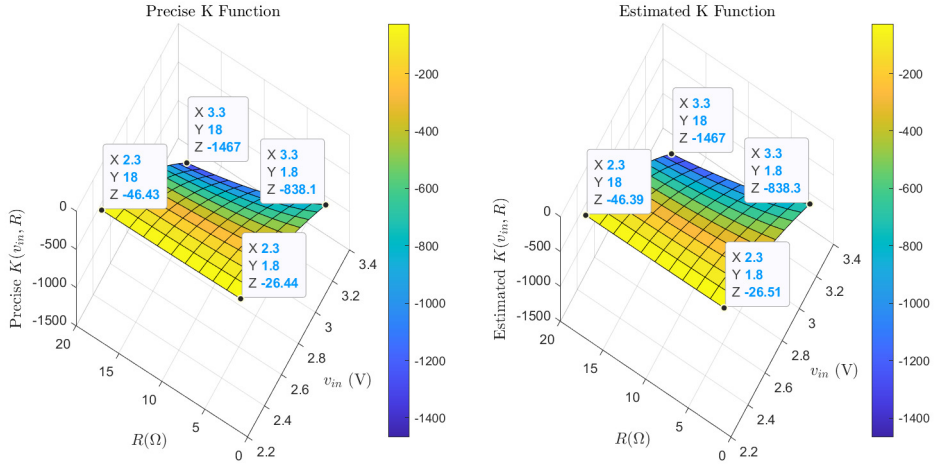


Figure 2.12: Precise and Estimated $K(v_{in}, R)$ vs. v_{in} and R

and its estimated counterpart are tightly matched, for all input voltage and load resistance values.

2.4 Simulation Results

Scenario 1: In this scenario, the converter operates in CCM and there is no ESR for inductor and capacitor and also there is zero uncertainty in the values of the inductor and the capacitor. Furthermore, v_{in}=3.3 V, $v_{o,\text{ref}}$=1.8 V, $i_o = 1.5 + 1.5u(t - 0.001s)$ A , $L = 100$ nH , $C = 100$ μF and the switching frequency is 900 kHz. In the above equations, $u(t)$ is the unit step function. The converter output voltage, shown in Fig. 2.13, illustrates that the load transient response is eliminated.

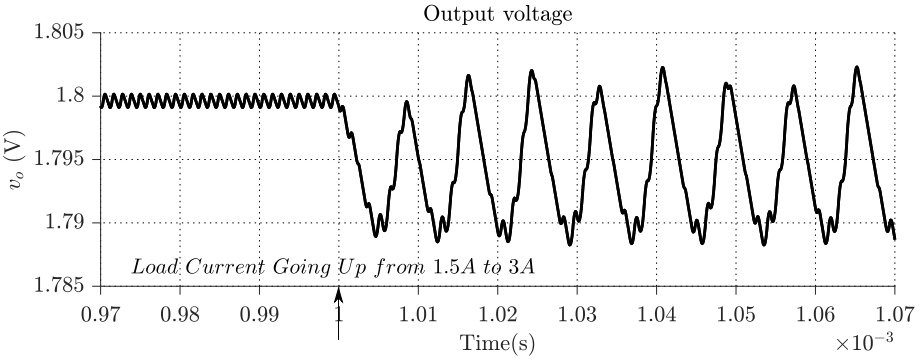


Figure 2.13: Converter output voltage in CCM mode in Scenario 1

Scenario 2: In this scenario, there is a 20 percent uncertainty in the inductor's value. Also, an ESR of 1 mΩ is considered for the inductor and an ESR of 3 mΩ is considered for the capacitor. Furthermore, in this scenario, $i_o = 1.5 + 1.5u(t -$

0.0008s) A, while other circuit and control parameters are the same as Scenario 1. The converter output voltage, shown in Fig. 2.14, illustrates that the load transient response is successfully eliminated.

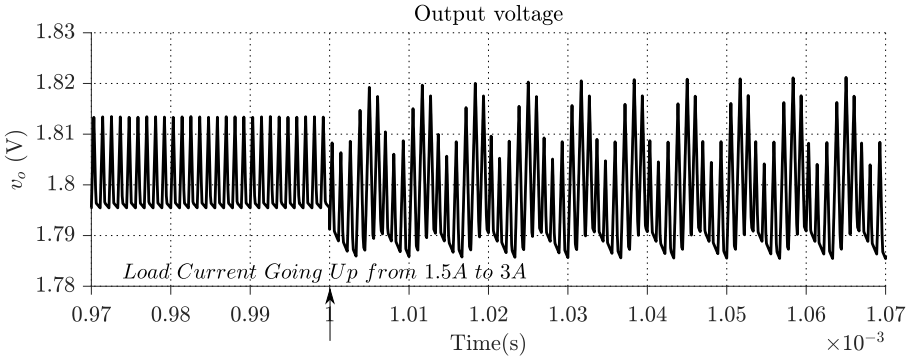


Figure 2.14: Converter output voltage in CCM (Scenario 2)

Scenario 3: In this scenario, the converter operates in DCM and there is an ESR of 1 mΩ for the inductor and and 3 mΩ for the capacitor. Also, there is an uncertainty of 20 percent in the inductor's value. Furthermore, v_{in}=3.3 V, $v_{o,\text{ref}}$=1.8 V, $i_o = 0.5+1.5u(t-0.001s)$ A , $L = 80$ nH , $C = 90$ μF and the switching frequency is 900 kHz. The converter output voltage, provided in Fig. 2.15, illustrates an undershoot of 0.03V in the output voltage and the recovery time is 1.2 μs. So,the transient response is eliminated.

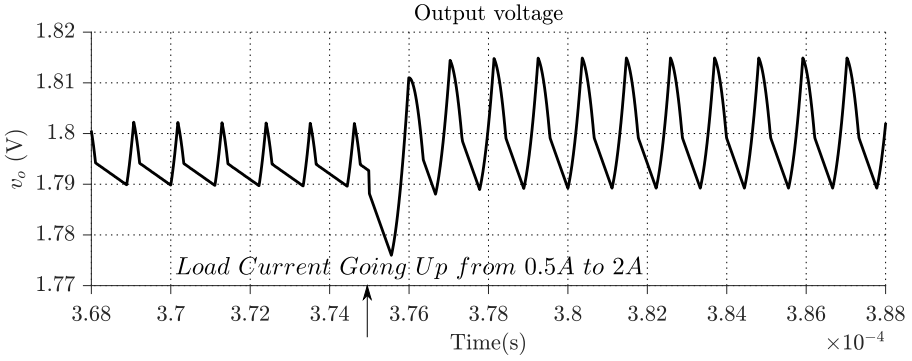


Figure 2.15: Converter output voltage in DCM (Scenario 3)

Scenario 4: In this scenario, the effects of parasitic resistances and inductances are investigated. The input voltage of 3.3 V, an output voltage of 1.8 V, an inductor of 0.8 μH and a capacitor of 100 μF with an ESR of 10 mΩ are considered. The load current is changed between 0.5 A and 1 A in CCM and the parasitic inductance in series with the load is 50 nH. The converter responses are shown in Fig. 2.16.

It can be observed that the load transients are not eliminated. However, as the corresponding recovery times are less than one switching period, it can be stated that the load transients are minimized.

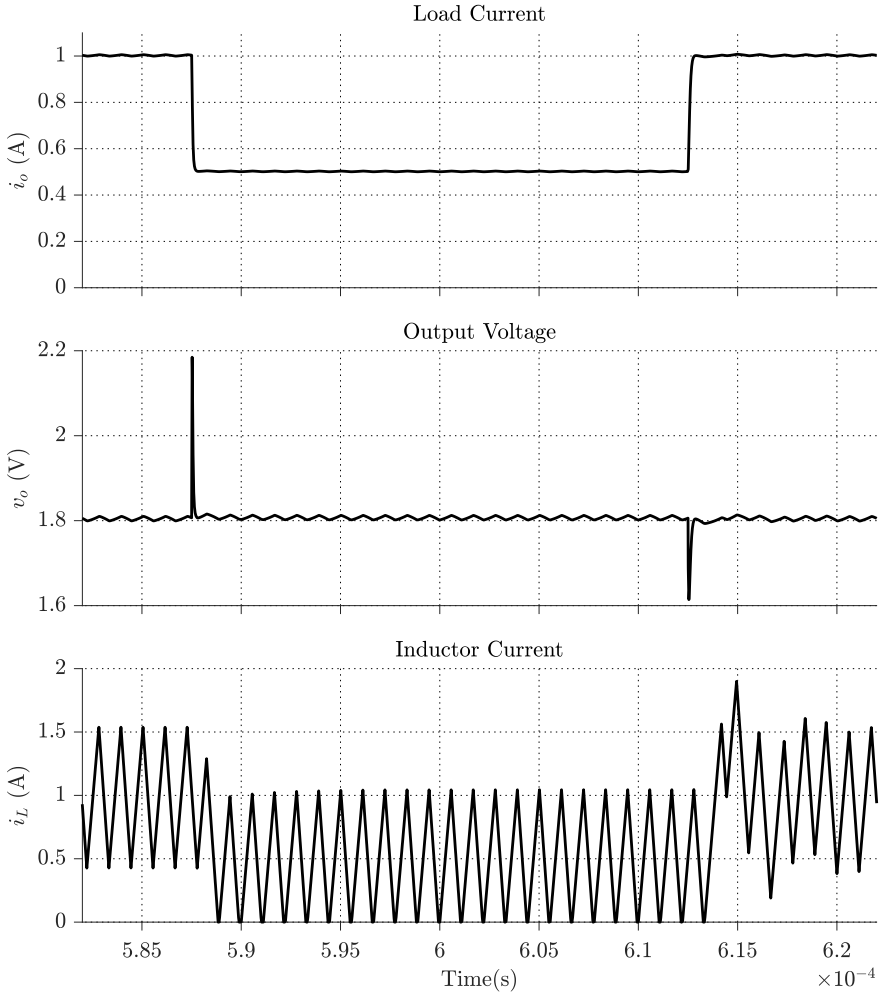


Figure 2.16: From top to bottom: load current, output voltage, and inductor current (Scenario 4)

In Table 2.1, the simulation results provided in this section are compared with other existing controllers. A figure of merit (FOM) is defined in this table to accurately compare different simulation scenarios. The definition of this FOM is based on the fact that the best system performance is achieved when for the same load current step, the sizes of inductor and capacitor, the switching frequency, the recovery times and overshoot/undershoot levels are all minimized.

Table 2.1: Comparison of simulation results with other methods

	Scenario 2	Scenario 3	Scenario 4	[38]
Input Voltage v_{in} (V)	3.3	3.3	3.3	3.6
Output Voltage v_o (V)	1.8	1.8	1.8	1.8
Inductor L(μH)	0.1	0.08	0.8	4.7
Capacitor C(μF)	100	90	100	10
Switching Frequency f_s (MHz)	0.9	0.9	0.9	1
Max. Load Current $i_{\text{o,max}}$ (A)	3	2	1	0.6
Load Transient Step ΔI_o (A)	1.5	1.5	0.5	0.3
Overshoot Recovery $t_{\text{r,ov}}$ (ns)	N/A	N/A	400	1800
Undershoot Recovery $t_{\text{r,un}}$ (ns)	0	2000	400	1900
Overshoot Level v_{ov} (V)	N/A	N/A	0.4	0.033
Undershoot Level v_{un} (V)	0	0.025	0.18	0.025
FOM= $\dfrac{\Delta I_o}{LCf_s t_{\text{r,ov/un}} v_{\text{ov/un}}}$	infinite	4.6×10^{-3}	6×10^{-5}	1.2×10^{-4}

2.5 Application to Other Converters: Noninverting Buck-Boost Converter Example

This section extends the proposed controller to a non-inverting buck-boost converter and the control law is derived for CCM operating mode as shown in Fig. 2.17. Such a converter with the proposed controller can be used in battery-powered power supplies, telecommunication systems, and power factor correction circuits in fuel cell applications [1].

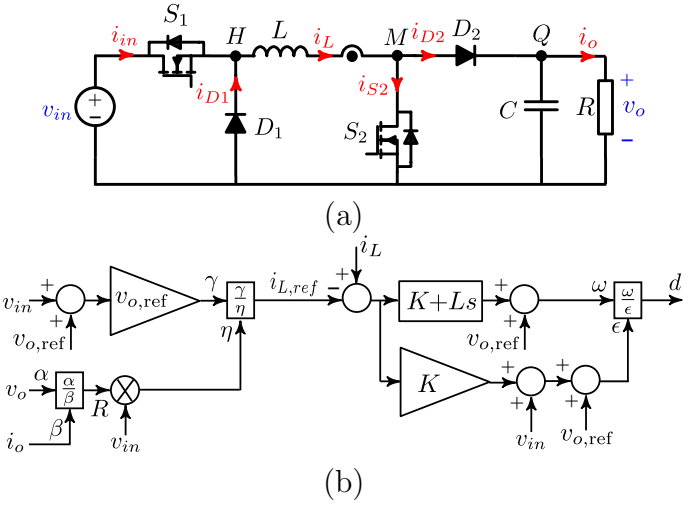


Figure 2.17: (a) Non-inverting buck-boost converter (b) Proposed controller in CCM

In Fig. 2.17, i_{D1} and i_{D2} are currents flowing through D_1 and D_2, respectively, i_{S2} is the current flowing through S_2 and T_s is the switching period. If KVL and KCL equations for this converter are averaged over one switching cycle, the control

law will become as

$$d = \frac{K(i_L - \frac{v_{\mathrm{o,ref}}(v_{\mathrm{in}}+v_{\mathrm{o,ref}})}{Rv_{\mathrm{in}}}) + v_{\mathrm{o,ref}} + L\frac{di_L}{dt}}{K(i_L - \frac{v_{\mathrm{o,ref}}(v_{\mathrm{in}}+v_{\mathrm{o,ref}})}{Rv_{\mathrm{in}}}) + v_{\mathrm{o,ref}} + v_{\mathrm{in}}}. \tag{2.31}$$

Case-Study: Consider a non-inverting buck-boost converter with an input voltage of 3.3 V, an output voltage of 5 V, a switching frequency of 1 MHz, an inductor of 600 nH, and a capacitor of 100 μF is used. If the proposed controller is applied to this converter and the load current goes up from 1 A to 2 A, the transient response of converter will be as shown in Fig. 2.18. The load transient response is minimized for the converter. In Table 2.2, the performance of the proposed controller is compared with the method of [1]. It shows that the proposed controller has a better performance.

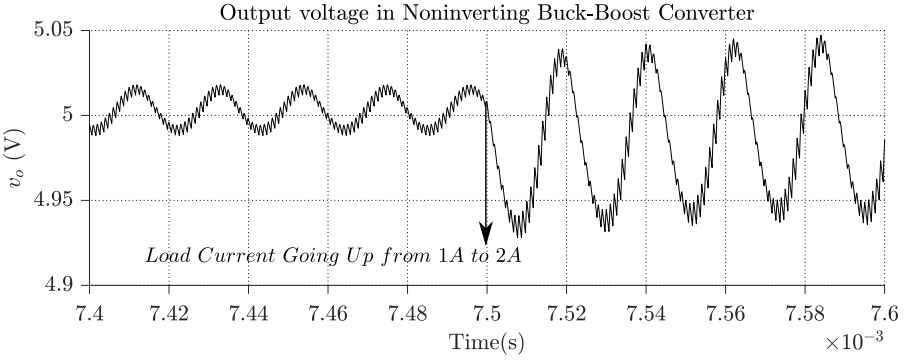


Figure 2.18: Transient response of a non-inverting buck-boost converter with the proposed controller to a load current from 1 A to 2 A

Table 2.2: Comparison of the proposed method and [1]

	Proposed	[1]
Input Voltage v_{in} (V)	12	12
Output Voltage v_o (V)	19	19
Inductor L (μH)	20	76
Capacitor C (μF)	250	200
Switching Frequency f_s (KHz)	100	100
Maximum Load Current $i_{\mathrm{o,max}}$ (A)	5	5
Load Transient Step ΔI_o (A)	4	4
Overshoot Recovery $t_{\mathrm{r,ov}}$ (ms)	3	9
Undershoot Recovery $t_{\mathrm{r,un}}$ (ms)	2	5
Overshoot Level v_{ov} (V)	0.55	1.2
Undershoot Level v_{un} (V)	0.88	3

2.6 Proposed Controller Application in Converters with High Order Dynamics

This section discusses the extension of the proposed controller to DC-DC converters with high-order dynamics, which have several capacitors and inductors. When the converter duty cycle is modified by a general controller in response to output voltage error, the effect of this control action typically propagates through the converter from the input source to the load side. Therefore, different inductor currents experience the changes made by the control action at different speeds. In other words, inductors closer to the source will typically exprinc control action results sooner than the load-side inductors. This phenomenon degrades the transient responses of converters and produces excessive overshoots. Particularly, the impacts of this phenomenon are most highlighted in converters with high-order dynamics, which are composed of several inductor and capacitors. To mitigate this problem in general controllers, the proposed controller in this chapter is extended to converter with high-order dynamics. Similar to the previous section, the output voltage level and its reference value are denoted by v_o and $v_{o,ref}$, respectively. Assuming that the converter topology is composed of m inductors and the current flowing through the j-th inductor L_j (0 < j < m+1) is denoted by $i_{L,j}$, the controller sets the duty cycle to achieve:

$$\sum_{j=1}^{m} k_j \frac{di_{L,j}}{dt} = v_o - v_{o,ref}. \tag{2.32}$$

In (2.32), the inductors are numbered in an ascending order based on their proximity to the load side. In other words, inductor 1 and inductor m are the furthest and the closest inductors to the load side, respectively. Also, for every n and p satisfying 0 < n < p < m+1 in (2.32), $|k_n| > |k_p|$. This is because as inductor p is closer to the load, there is a stronger dynamical correlatioship between v_o and $i_{L,p}$ and any changes in $i_{L,p}$ as a result of a control action is experienced by the output voltage sooner, compared with inductor n. Therefore, to develope a stronger dynamcal correlationship between inductor n and the utput voltage, $|k_n| > |k_p|$. To achieve (2.32), the average model of the converter is written and (2.32) is solved in terms of d. This way, the control law is derived. A sample process as well as the simulation results is given in the following case study.

Extended Controller Case Study: Fig. 2.19 shows the schematic of a Cuk converter. By state space averaging, $\frac{di_{L1}}{dt} = \frac{v_{C1}(d-1)+v_{in}}{L_1}$ and $\frac{di_{L2}}{dt} = \frac{-v_{C1}d-v_o}{L_2}$. Based on the discussion in this section, the control objective is set as $\frac{di_{L1}}{dt} = k\frac{di_{L2}}{dt} + p(v_o -$

$v_{o,ref}$). Using this objective and state space averaging results mentioned above, the control law for a Cuk converter is explained as:

$$d = \frac{L_2(v_{C1} - v_{in}) - kv_oL_1 + pL_1L_2(v_o - v_{o,ref})}{(L_2 + kL_1)v_{C1}}. \tag{2.33}$$

Assuming $L_1 = L_2$ =10μH, $C_1 = C_2$ =30μF, v_{in} =3.3V, $v_{o,ref}$ =1.8V, and f_s =200KHz, the load transient response of the converter using the proposed extended controller in (2.33) for a 1A to 2A load step is as shown in Fig. 2.20.

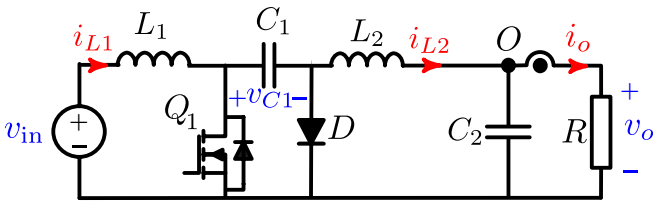


Figure 2.19: Scehmatic of a Cuk Converter

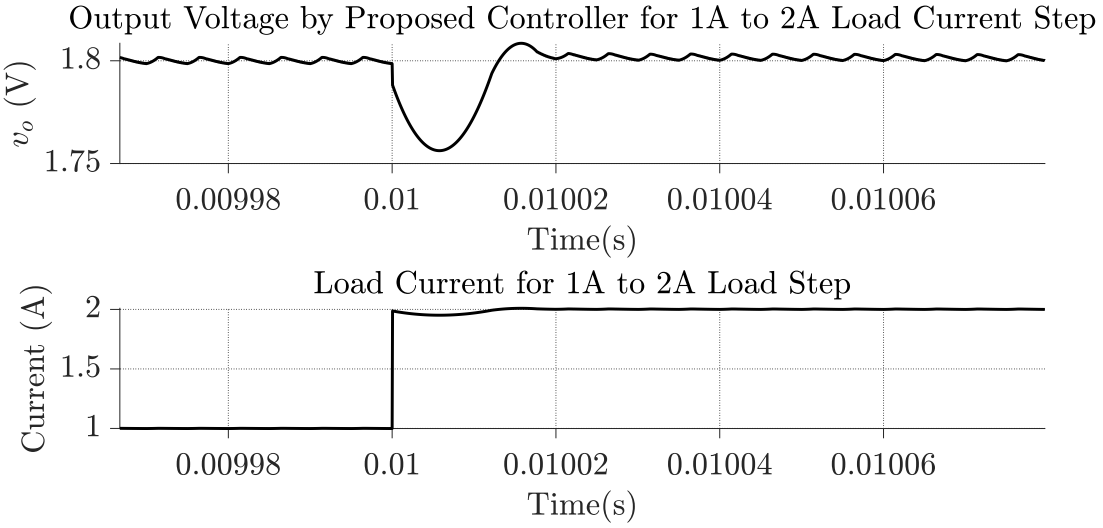


Figure 2.20: Load Transient Response of the Closed-loop Cuk Converter Using the Proposed Extended Controller in This Chapter

2.7 Experimental Results

Performance of the controller is experimentally validated on a buck converter with an input voltage of 3.3 V, an inductor of 1 μH, a capacitor of 100 μF and a switching frequency of 900 kHz. A TI TMS320F28335 DSP is used for implementing the proposed control algorithm.

Fig. 2.21 shows the corresponding waveforms when the output voltage is set to 1.8 V and the output current is changed from 0.7 A to 1 A and vice versa. In this figure, from top to bottom, the waveforms correspond to the load current, the output voltage, and the inductor current waveforms, respectively. The overshoots and undershoots are created by the parasitic inductances which are in series with the load. The recovery time of the transient response is around 300 ns. The transient response is negligible.

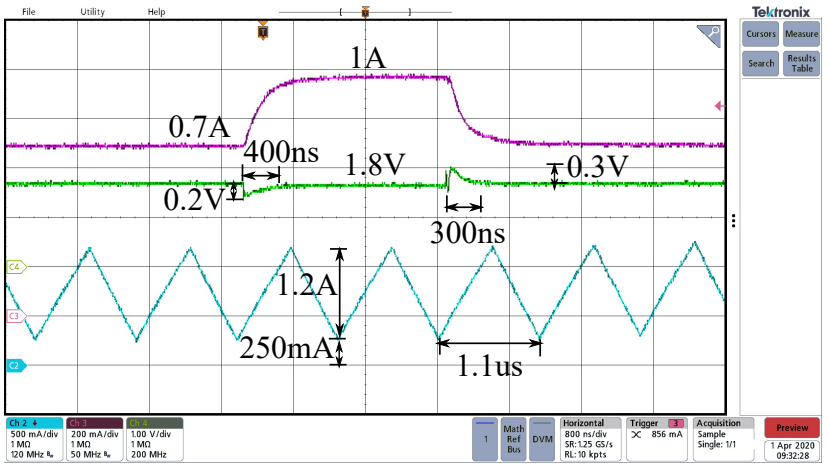


Figure 2.21: Experimental results: (from top to bottom) load current, output voltage, and inductor current when the load current is changed from 0.7 A to 1 A and vice versa.

Fig. 2.22 shows the experimental results when the output voltage is set to 1.3 V and the load current is changed from 0.4 A to 0.7 A and vice versa. The load transient dynamics is fast. Fig. 3.35 shows the results when the reference value for the output voltage is changed from 1.3 V to 1.8 V and vice versa. The output voltage has successfully reached its steady state value. The start-up transients of the buck converter are shown in Fig. 3.36 for the output voltage set point of 1.7 V. This figure shows that during start-up, the output voltage reaches its reference value without any overshoots. The capacitor voltage is shown in Fig. 3.37 which confirms the simulation results. The undershoot level is 12 mV, which can be neglected. In Fig. 2.26, the load transient response in DCM is shown. This figure shows a fast transient response.

Table 2.3 provides further comparison among the performances of the proposed controller and several other controllers in the literature. As the table illustrates, the recovery times associated with transient responses made by the proposed controller are much lower than other methods. Also, the overall sizes of the used capacitor and inductor in DCM are smaller than other methods. Therefore, it is more advantageous

to implement the proposed controller in DCM.

To achieve a fast transient response, one can use a controller such as PI or any other types of controllers with large gains and proper saturation limits to achieve an optimal time system response. Such a controller is proposed in [19], in which the converter works in full or zero duty ratios during load transients. Table 2.3 provides a comparison between the proposed controller and [19]. The comparison is made using a Figure of Merit (FOM) defined based on system performance indicators such as recovery times, overshoot and undershoots achieved during load transient periods, minimum required capacitance and inductance, and switching frequency. The FOM is calculated for all controllers under the same voltage gain and load

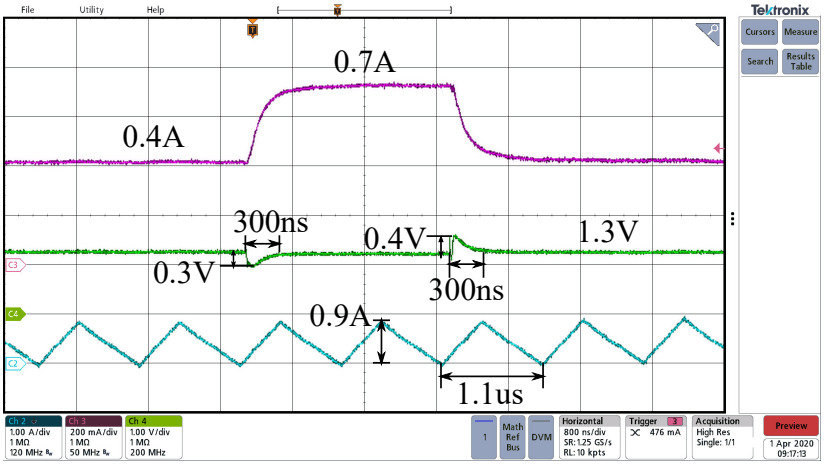


Figure 2.22: Experimental results: (from top to bottom) load current, output voltage, and inductor current when the load current is changed from 0.4 A to 0.7 A and vice versa.

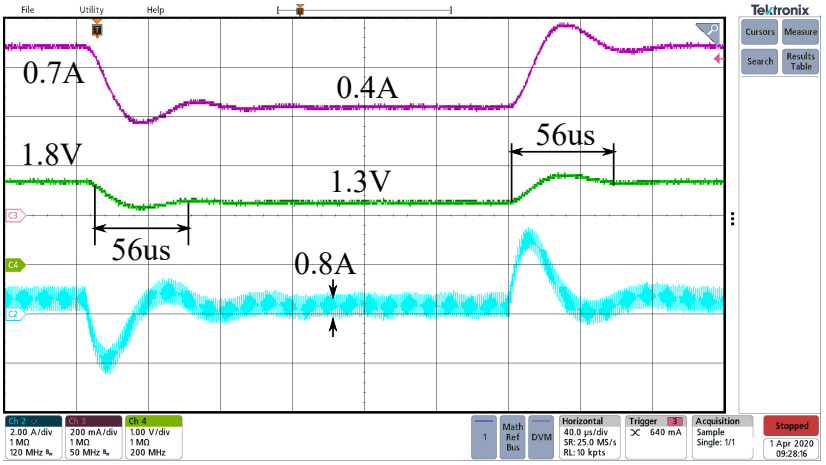


Figure 2.23: Experimental results: (from top to bottom) load current, output voltage, and inductor current when the reference output voltage is changed from 1.3 V to 1.8 V and vice versa

current steps. As Table 2.3 illustrates, the performance of the proposed controller in CCM is similar to [19], which is implemented in CCM as well. However, the FOM

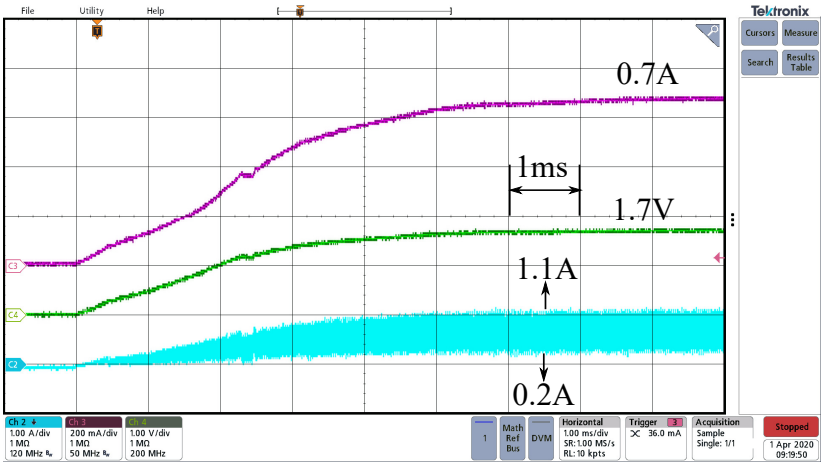


Figure 2.24: Experimental results: (from top to bottom) load current, output voltage, and inductor current during start-up

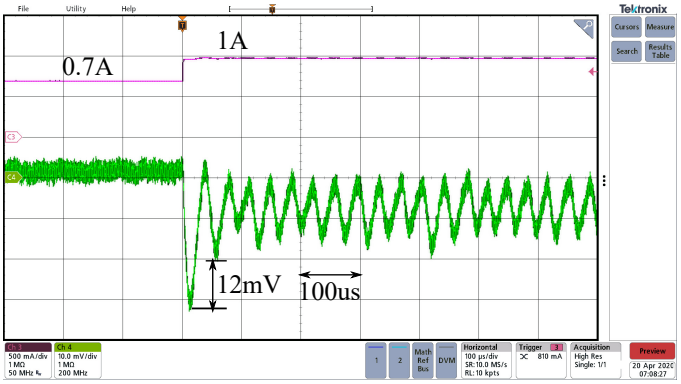


Figure 2.25: Experimental results: (from top to bottom) load current, and output voltage in CCM

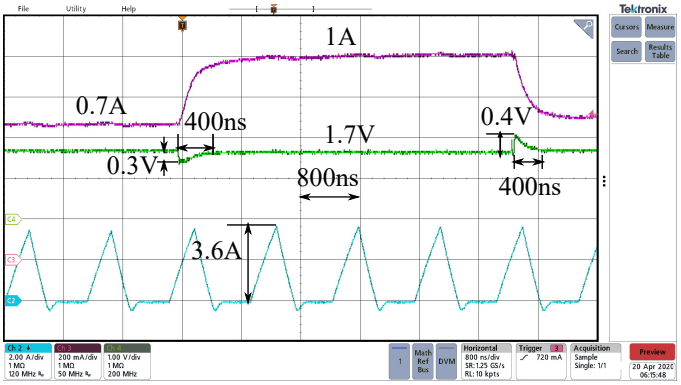


Figure 2.26: Experimental results: (from top to bottom) load current, and output voltage and inductor current in DCM

Table 2.3: Comparison of the proposed method and other controllers

	Proposed (CCM)	Proposed (DCM1)	Proposed (DCM2)	[19]	[38]	[112]
Input Voltage v_{in} (V)	3.3	3.3	3.3	3.3	2.6-4	3.6
Output Voltage v_o (V)	1.8	1.8	1.8	1-2.5	1-2	2.5
Max. Voltage Gain $g_{\max}$	1.83	1.83	1.83	3.3	4	1.44
Inductor L (μH)	0.8	0.08	0.08	4.7	4.7	2.2
Capacitor C (μF)	100	90	100	4.7	10	22
Switching Frequency f_s (MHz)	0.9	0.9	0.9	1	1	1
Max. Load Current (mA)	700	1000	3000	900	600	1050
Load Transient Step ΔI_o(mA)	300	300	2700	450	300	400
Overshoot Recovery $t_{\text{r,ov}}$(μs)	0.3	0.4	2.7	4	2.5	68
Undershoot Recovery $t_{\text{r,un}}$ (μs)	0.3	0.4	7.3	4	2.8	60
Overshoot Level v_{ov} (V)	0.4	0.4	0.09	0.07	0.18	0.027
Undershoot Level v_{un} (V)	0.3	0.3	0.09	0.085	0.167	0.022
Stability	Stable	Stable	Stable	Stable	Stable	Stable
Noise Level $\frac{v_{\text{noise}}}{v_{\text{ripple}}}$	1	1	1	4	N/A	0.33
FOM= $\frac{\Delta I_o}{LCf_s t_{\text{r,ov/un}} v_{\text{ov/un}}}$	695	4427	4296	707.14	121.45	4.91

of the proposed controller in this chapter is superior in DCM compared to [19]. The proposed controller in [19] cannot use a small inductor in DCM, as in DCM a full duty ratio causes the inductor current to have a large overshoot during transient period and if this overshoot is blocked by the overcurrent monitoring system, the controller will not be time-optimal and its performance gets degraded and both of these result in a lower FOM in DCM. It can be observed that achieving superior transient performance using an advanced controller such as the one proposed in [19], or a simple PI controller with saturation limit is not a trivial task. Another example is the PID controller in [112] which is compared with the proposed method in this chapter in Table 2.3, and the superiority of the proposed method can be observed.

The proposed controller improves the transient response of the converter while it guarantees the steady state operation. As the switching frequency of the converter is constant, it does not create any abnormal operating condition for the converter during transients. In addition, the controller enables a more optimal design of the converter to achieve high power density. Using this controller in DCM, the inductor size can be reduced significantly, and it becomes possible to achieve ZVS

for all operating conditions resulting in a higher switching frequency, more integrated design and faster transient response while achieving acceptable efficiency.

Chapter 3

A New Load-Dynamics Decoupling Controller to Improve Load Step Transients in Data Centers

This chapter proposes a dynamically optimized controller for DC-DC converters in the intermediate power conversion stage i.e. stage 2 of the power management system of a data center. As discussed in Chapter 1, the converters in this stage deal with high load currents and large load steps. It is worth mentioning that the previous chapter i.e. Chapter 2 discusses a controller solution for stage 3 converters, which unlike stage 2 converters, deal with small load steps. Therefore, when applied to stage 2 converters, the conventional methods applicable to stage 3 converters lead to degraded dynamical responses and cannot meet system requirements. This necessiates development of a new control system for stage 2 converters in power management system of a data center and forms the main taget of the current chapter.

In Chapter 1, it is mentioned that in stage 2 converters of the power manaegment system in a data center, low system damping in high load currents causes the load step disturbances not to be easily removable by the existing controllers. Therefore, using auxiliary circuits is the most commonly-used method in the literature, which results in efficiency degradation and system complexity. To achieve a desired performance without any auxiliary circuit, this chapter proposes an alternative controller to enhance load transient responses of DC-DC converters in large load steps. This controller decouples system dynamics from the load side. Hence, the system dynamics does not get degraded in large load steps. Also, the controller does not create any step changes in the duty cycle, resulting in no extra transient states in the system. Furthermore, the system stability is not compromised, as the controller always ensures stability according to the root locus analysis presented in this chapter. Finally, as no auxiliary components are used, system complexity, and

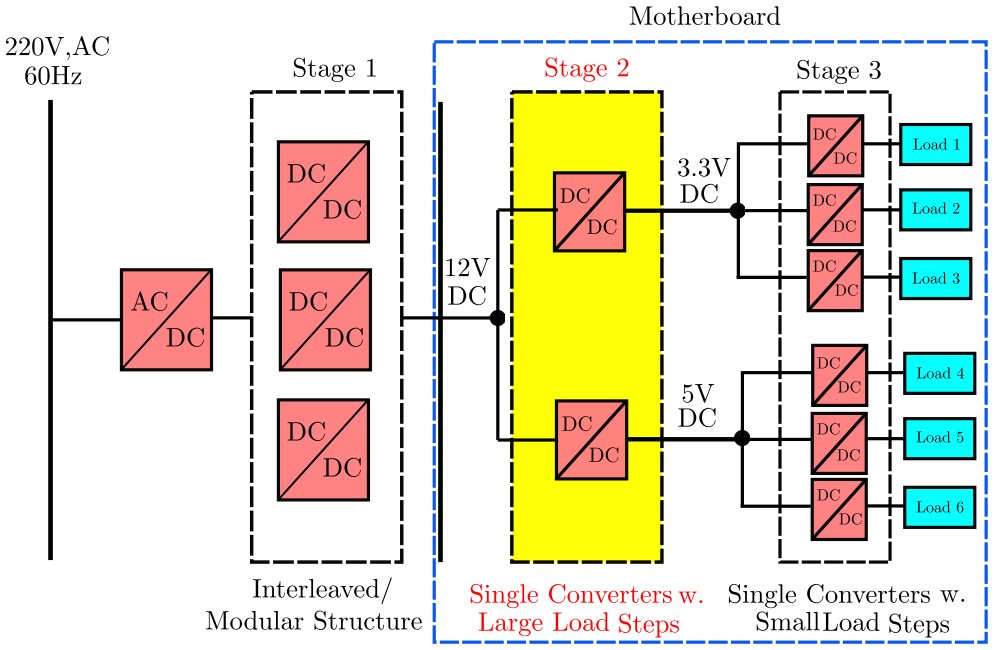


Figure 3.1: Intermediate DC-DC Conversion Stage i.e. Stage 2 Highlighted by Yellow in Data Center Power Management System

large instantaneous jumps in voltages and currents are avoided. This chapter first presents the detailed controller derivation for buck converters in both Continuous (CCM) and Discontinuous (DCM) Conduction Modes. In addition, it is shown that the proposed approach can be applied to other converter topologies, such as the Cuk converter, too. Finally, an extneded version of the controller is proposed such that it can be applied to various load types such as constant power loads and closed-loop converter loads. Once the proposed controller is derived, analyzed and designed, the performance is verified by simulations and experimental results. A per-unit model of buck converter is also proposed to conduct comparisons among various existing approaches.

3.1 Chapter Challenges, Literature Review, and Contributions

3.1.1 Challenges

The architecture of the power management system of a data center is shown in Fig. 3.1, in which the intermediate DC-DC conversion stage i.e. stage 2 is highlighted by yellow color. According to this figure, each converter is stage 2 supplies power to several stage 3 converters, each of which is connected to a point of the load (POL).

The stochastic load steps in different POLs which occur at high frequencies are summed up and sen as a single large load step by a converter in stage 2. To meet power demands of the loads duing load steps, each stage 3 converter recieves power from the input voltage and as discusssed above, the these power levels are summed up and seen as a single large load step by a stage 2 converter. Therefore, if not appropriately compensated for, the output voltages of stage 2 converters which simultaneously act as input voltages of stage 3 converters will drop. This phenomenon deteriorates the steady-state and dynamical performance of stage 3 converters and may cause stage 3 converters to be unable to provide load power demands, leading to load interruptions due to power shortages. Therefore, it is critical to use appropriate control methods to regulate the output voltages of stage 2 converters in a fixed level, both in steady-state and transient conditions. The fact that stage 2 converters deal with large load steps makes it challenging to achieve an optimum system dynamics with reasonable overshoot/undershoot levels. Therefore, control systems need to be developed to specifically focus on improving DC-DC converter dynamics in large load steps.

3.1.2 Literature Review

The existing approaches to achieve enhanced converter dynamics for large load steps in stage 2 converters in a data center are already discussed in detail in section 1.2.2. A summary of this section is presented in this section. widely adopted approaches in the literature to improve stage 2 converter dynamics in a data center include adding auxiliary circuits during the transient periods [2], [3, 57, 4, 58, 59, 60, 61, 62, 63], or using more complex and high-performance controllers [64, 65, 19, 66, 67, 68].

Some of the existing auxiliary circuits reduce the total inductance of the converter during transients [3, 57, 4, 58, 59, 60]. This approach achieves better load transient responses by increasing inductor current's rates of variation [57]. Auxiliary circuit currents are injected to or drawn from the load side in [3] to improve the response at the expense of efficiency degradation [3]. In another approach, an inductor is inserted in parallel with the main inductor during transients [57]. Although this method improves the dynamics, it increases overshoot levels in the main inductor's current. Auxiliary currents are injected to the load using a parallel buck converter, resulting in fast system dynamics [4] at the expense of duplicating the power circuit. The buck converter's inductor is replaced by a flyback-based converter in [58]. This approach requires an auxiliary circuit with a similar power rating compared to the main circuit. Using the capacitor charge balance control and a series auxiliary inductor in [59] resulted in major dynamic improvements. However, large instanta-

neous variations and overshoots in inductor current and output voltage can be observed. An improved topology of inductor-switching DC-DC converter is proposed in [60], with higher efficiency and reduced overshoot/undershoot levels. However, the number of passive components are increased, resulting in higher energy storage requirements. Other methods to improve converter's dynamics include changing the resistance value seen by the converter's output terminal [61], and inserting a current source branch at the load node [62, 63]. Although the auxiliary circuits generally improve load transient responses, they increase system's cost and complexity and normally introduce additional losses [61], along with more complex control [63], and possible stability issues [62] due to switching the power auxiliary circuits on and off repetitively.

High-performance controllers are also proposed to improve converter's dynamics [64, 65, 19, 66, 67, 68]. However, the levels of dynamics improvements are limited for large load steps. The proposed controllers can be classified into three categories. In the first category, linear controllers based on feedback and feed-forward are proposed [64, 65]. The system dynamics is a function of the load resistance value and is changed considerably in large load steps. Therefore, a single linear controller cannot achieve suitable dynamic responses for such load steps. The second category of controllers either maximize or minimize the duty cycle during transients [19, 66]. Although this approach makes system dynamics faster, it leads to step changes in the duty cycle, which in turn create new transient states in the system. As a result, the system dynamics becomes slower than expected. Finally, another category belongs to the family of I^2 controllers [67, 68], which can enhance system dynamics considerably. This approach normally requires compromises between the stability of the system and its steady-state performance indicators such as ripple levels.

3.1.3 Targets and Contributions

According to the topics discussed, the targets of this chapter can be summarized as:

1. Proposing a new controller to improve load transient responses of stage 2 converters in data centers for large load steps originating from stage 3 converters.
2. Extension of the proposed controller to different load types
3. Comparison between the proposed controller and other existing approaches
4. Validation of the proposed method using experimental and simulation results.

Contributions: To achieve a desired performance without any auxiliary circuit, this chapter proposes an alternative controller to enhance load transient responses of stage 2 DC-DC converters in large load steps. This controller decouples system dynamics from the load side. Hence, the system dynamics does not get degraded in

large load steps. Also, the controller does not create any step changes in the duty cycle, resulting in no extra transient states in the system. Furthermore, the system stability is not compromised, as the controller always ensures stability according to the root locus analysis presented in this chapter. Finally, as no auxiliary components are used, system complexity, and large instantaneous jumps in voltages and currents are avoided. This chapter first presents the detailed controller derivation for buck converters in both Continuous (CCM) and Discontinuous (DCM) Conduction Modes. In addition, it is shown that the proposed approach can be applied to other converter topologies, such as the Cuk converter, too. Once the proposed controller is derived, analyzed and designed, the performance is verified by simulations and experimental results. A per-unit model of buck converter is also proposed to conduct comparisons among various existing approaches.

3.2 Chapter Main Control Concept

This section presents the main control concept of this chapter which is about converter control based on decoupling converter dynamics from the load. For simplicity, this section assumes a buck converter and a resistive load to present the control concept. It should be mentioned that the generality of the proposed concept is not affected by converter topology and load type. The notations used in this chapter include v_{in} for input voltage, i_L for inductor current, i_C for capacitor current, R for load resistance, v_o for output voltage, L for inductance, C for capacitance, and $v_{o,ref}$ for the reference output voltage. Also, d denotes the duty cycle.

If the buck converter shown in Fig. 3.2 experiences a large load step, the load resistance value R changes considerably. Therefore, the transfer function $G_p(s) = \frac{V_o(s)}{D(s)}$ changes considerably. For a general control system shown in Fig. 3.2(b), the fixed genral control system does not take the variations of the plant $G_p(s)$ due to the load step into account. Therefore, the general controller in Fig. 3.2(a) cannot reach acceptable undershoot/overshoot level and recovery times during load step transients.

To compensate for this problem, the current chapter proposes a new controller based on decoupling converter dynamics from the load. The proposed controller takes R and v_{in} as inputs and is designed such that v_o becomes independent from R and becomes only a function of v_{in}. This way, large load steps affecting R do have only a negligible effect on v_o. As a result, overshoot/undershoot levels and recovery times associated with large load steps are improved.

In fact, to solve the problem of performance dependency on the load, this chapter

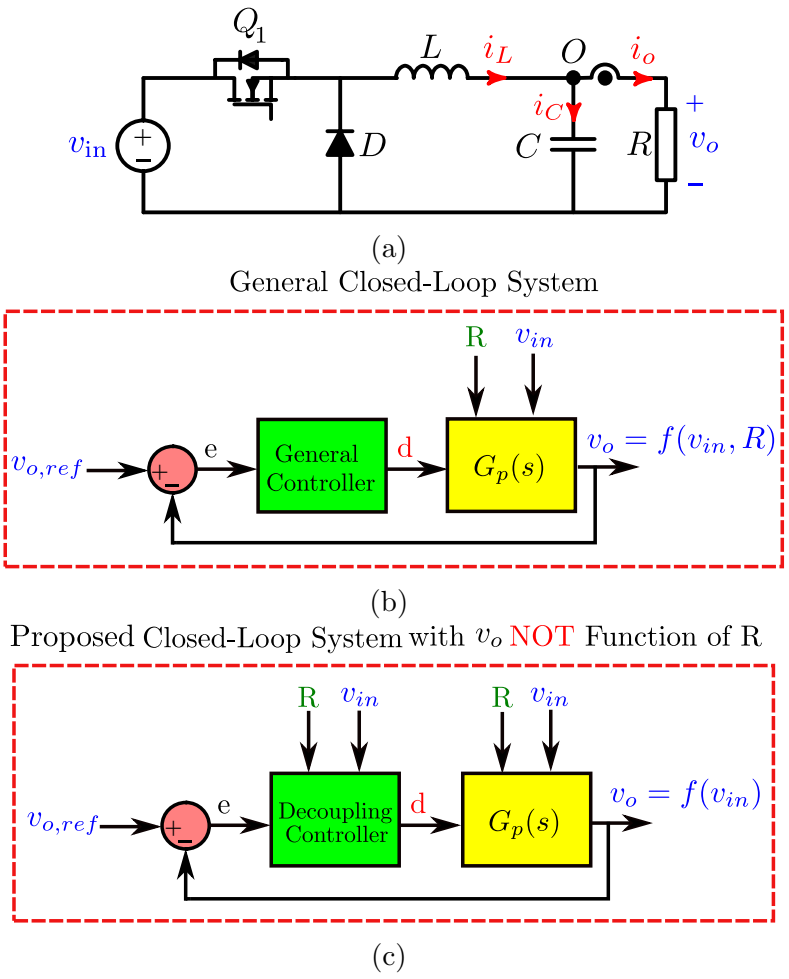


Figure 3.2: (a) Schematic of a buck converter (b) General Control Structure for a Buck Converter (c) Proposed Control Loop with v_o Dynamics Decoupled from R

proposes a controller to decouple output voltage dynamics from the load resistance value. Therefore, when the controller is designed to achieve a fast response at light load, the performance is not degraded significantly at other load levels. This is done by deriving the closed loop differential equation of the system and finding all terms that are functions of the load resistance. Next, a control mechanism is developed to minimize the effects of these terms on system dynamics. Once this is achieved, the controller adjusts the dynamical profile of the system. Further details are provided in the next sections. The underlying control concept discussed above can be illustrated by Fig. 3.2(c).

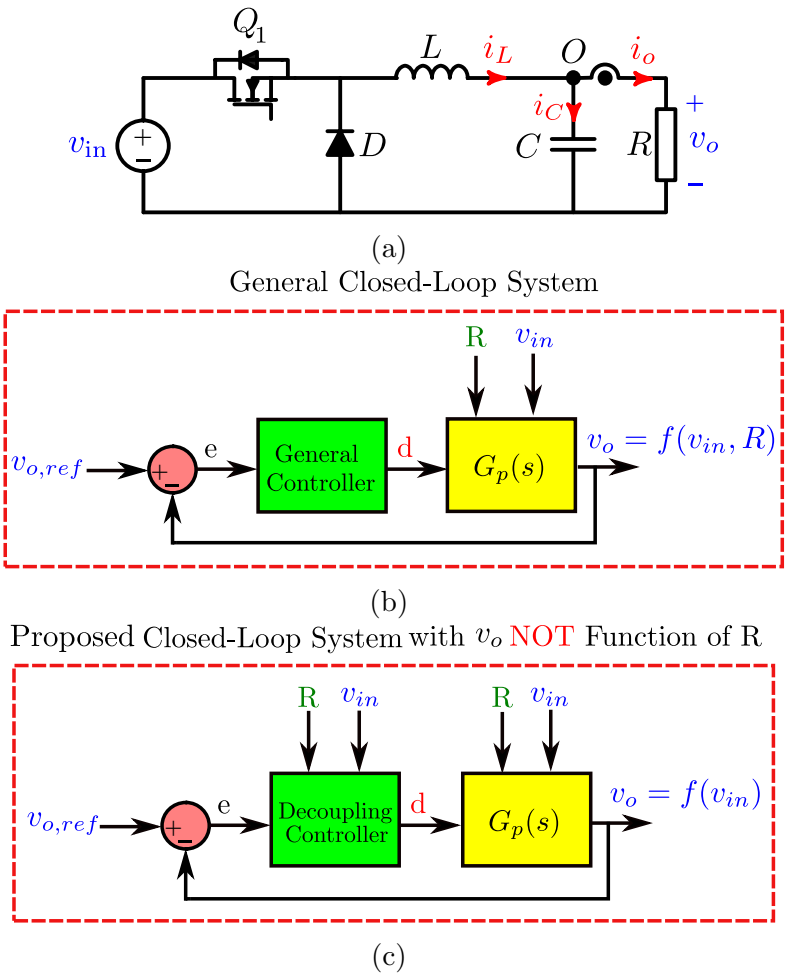


Figure 3.3: (a) Schematic of a buck converter (b) General Control Structure for a Buck Converter (c) Proposed Control Loop with v_o Dynamics Decoupled from R

3.3 Problem Definition

In this section, a particular challenge that is caused by the operation of buck converters with high load currents, is investigated. Fig. 3.3(a) illustrates the schematic of a buck converter and Fig. 3.3(b) shows its general control structure. The notations used in the chapter include i_L for inductor current, i_c for capacitor current, i_o for load current, R for load resistance value, L for inductance value, C for capacitance value, T_s for switching period, v_{in} for input voltage, and v_o for output voltage. Also, $v_{o,ref}$ is the reference value for the output voltage and d is the duty cycle. In Fig. 3.3(b), $G_p(s)$ denotes the control-to-output transfer function of a buck converter and can be given by [64]:

$$G_p(s) = \frac{v_{in}}{LCs^2 + \frac{L}{R}s + 1}. \tag{3.1}$$

Equation (3.1) shows that in high load current levels or equivalently low R values,

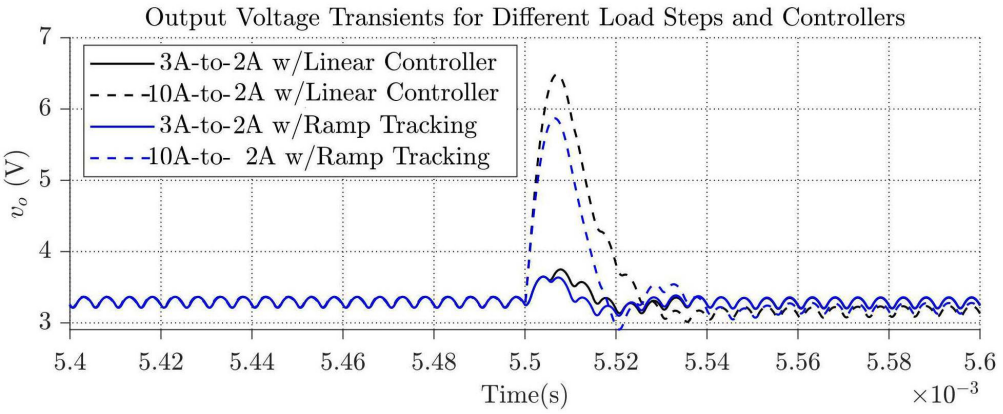


Figure 3.4: Output Voltage Transients for Different Load Steps using Linear and High-performance Controllers

$|G_p(j\omega)|$ and arg $G_p(j\omega)$ are decreased and increased, respectively. This reduces system's bandwidth, which results in a reduced system speed and a degraded load transient response. This can limit the system speed in applications where large load steps occur repetitively and the system speed is crucial, such as processor applications. In fact, Fig. 3.3(b) illustrates that for a general control structure, the dynamics of v_o is a function of R. Case Study 1 is provided to better illustrate the mentioned concepts.

Case Study 1: A buck converter is considered with v_{in}=12V, $v_{o,ref}$=3.3V, L=5μH, C=10μF, f_s=200KHz. Using (3.1), the phase margin is reduced by increasing R. Therefore, a linear controller is designed at i_o=1.25A, which is the minimum load current in continuous conduction mode (CCM). The controller is designed to achieve a phase margin and a bandwidth of 45 degrees and 50KHz, respectively. The designed controller is expressed as:

$$C(s) = \frac{483}{s}\left(\frac{34.2\times10^{-6}s+1}{1.8\times10^{-6}s+1}\right)^2. \tag{3.2}$$

This case study investigates the two cases of using just the controller expressed by (3.2) and using it along with a high-performance controller, Active Ramp Tracking Control [19, 66]. The load transient responses for 3A-to-2A and 10A-to-2A load steps are plotted in Fig. 3.4 for both cases. According to Fig. 3.4, the load transient responses are degraded in the 10A-to-2A load steps and need major improvements. This case study illustrated how the dependency of system dynamics to R can degrade the load transient responses. This chapter aims to provide a controller to tackle this problem by decoupling the dynamics of the output voltage from R. The block diagram of the closed-loop system associated with this controller is observable in

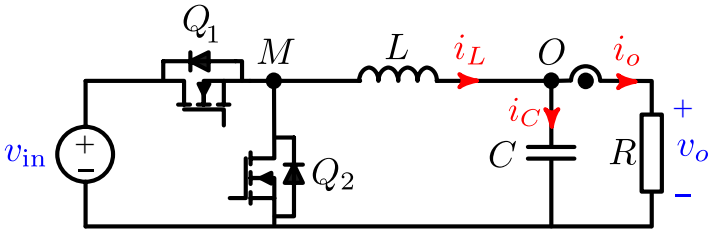


Figure 3.5: Schematic of a Standard Synchronous Buck Converter

Fig. 3.3(c). As this figure illustrates, the decoupling controller takes R as an input and is designed such that v_o is just a function of v_{in} and not R.

3.4 Proposed Controller

3.4.1 Underlying Control Concept

To solve the problem of performance dependency on the load, this chapter proposes a controller to decouple output voltage dynamics from the load resistance value. Therefore, when the controller is designed to achieve a fast response at light load, the performance is not degraded significantly at other load levels. This is done by deriving the closed loop differential equation of the system and finding all terms that are functions of the load resistance. Next, a control mechanism is developed to minimize the effects of these terms on system dynamics. Once this is achieved, the controller adjusts the dynamical profile of the system. Further details are provided in the next subsections. The underlying control concept discussed above can be illustrated by Fig. 3.3(c). Throughout this section, the controller is developed for a buck converter as an example. But as shown in one of the next sections, this approach can be similarly applied to other types of converters as well.

3.4.2 Derivation of Control Law in CCM and Controller Design

Based on the underlying control concept discussed, the controller can be formulated for a buck converter in CCM. Fig. 3.5 shows the schematic of a standard synchronous buck converter operating in CCM. In Fig. 3.6, the inductor current, i_L, is plotted versus time for one switching cycle. To obtain the inductor current waveform, it is assumed that the output voltage of the buck converter is constant in one switching period and is equal to $v_o(0)$. Also, from $0 < t < dT_s$, the voltage across the inductor is $v_{in} - v_o(0)$ and for the rest of a switching cycle, the inductor voltage is $-v_o(0)$.

KCL at node O of Fig. 3.5 results in:

$$i_L = C\frac{dV_o}{dt} + \frac{V_o}{R}. \tag{3.3}$$

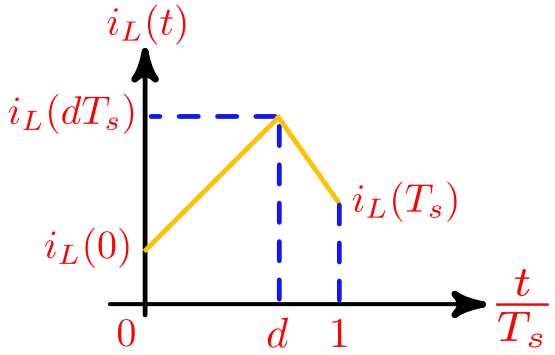


Figure 3.6: Inductor Current Waveform in CCM Operation Mode of A Buck Converter

From Fig. 3.6, $i_{L,avg}$ denoting the average value of the inductor current over one switching cycle can be obtained as:

$$\begin{aligned} i_{L,avg} &= \frac{1}{T_s}\int_0^{T_s} i_L(t)dt \\ &= i_L(0) + \frac{-v_{in}T_s d^2 + 2v_{in}T_s d - v_o(0)T_s}{2L}. \end{aligned} \tag{3.4}$$

An approximately constant output voltage is assumed for one switching period. Also, the output voltage levels at $t = 0$ and $t = T_s$ are denoted by $v_o(0)$ and $v_o(T_s)$, respectively. With these assumptions and notations, both sides of (3.3) are averaged over one switching cycle and (3.4) is also used to obtain:

$$\begin{aligned} i_L(0) + \frac{-v_{in}T_s d^2 + 2v_{in}T_s d - v_o(0)T_s}{2L} &= C\frac{v_o(T_s) - v_o(0)}{T_s} \\ &\quad + \frac{v_o(0)}{R}. \end{aligned} \tag{3.5}$$

The mathematical model of a buck converter operating in CCM can be derived using (3.5), which expresses the averaged model and is valid for both transient and steady state conditions. This equation is used to adjust the dynamical profile of the system and design an appropriate control law. To enable systematic design of output voltage dynamics, the approach used here is to select the control law such that the output voltage satisfies a 2nd order linear differential equation and no terms related to the inductor current exist in this differential equation. This will enable direct selection of system poles related to the output voltage. Next, the coefficients of the 2nd order differential coefficient discussed can be designed to make pole locations independent from the load resistance. This way, the output voltage dynamics will be decoupled from the load, that is the main control target. The process of designing the coefficients of the 2nd order differential equation to

meet this target is shown in the forthcoming paragraphs. As discussed, the output voltage must satisfy a differential equation which does not include any terms related to the inductor current. Therefore, the desired output voltage dynamics is selected as $\frac{d^2\tilde{v_o}}{dt^2} + \frac{1}{C}\left(-k_p + \frac{1}{R}\right)\frac{d\tilde{v_o}}{dt} - \frac{k_i}{C}\tilde{v_o} = 0$. To achieve such dynamics, d in (3.5) is selected such that the term $i_L(0)$ is eliminated from both sides of (3.5). In fact d is selected such that:

$$\begin{aligned}\frac{-v_{in}T_s d^2 + 2v_{in}T_s d - v_o T_s}{2L} &= \left(-i_L + \frac{v_{o,ref}}{R}\right) \\ &+ k_p(v_o - v_{o,ref}) \\ &+ k_i \int (v_o - v_{o,ref})dt.\end{aligned} \tag{3.6}$$

By solving (3.6) for d, the control law in CCM is obtained as:

$$d = 1 - \sqrt{\begin{aligned}&1 - \frac{v_o}{v_{in}} + \frac{2L}{v_{in}T_s}\left(i_L - \frac{v_{o,ref}}{R}\right) \\ &- \frac{2Lk_p}{v_{in}T_s}(v_o - v_{o,ref}) - \frac{2Lk_i}{v_{in}T_s}\int (v_o - v_{o,ref})dt\end{aligned}}. \tag{3.7}$$

Assuming $\tilde{v_o} = v_o - v_{o,ref}$, and based on (3.5) and (3.7), the dynamics of the closed-loop system can be given by:

$$\frac{d^2\tilde{v_o}}{dt^2} + \frac{1}{C}\left(-k_p + \frac{1}{R}\right)\frac{d\tilde{v_o}}{dt} - \frac{k_i}{C}\tilde{v_o} = 0. \tag{3.8}$$

To make the system dynamics independent from R, k_p is selected as $k_p = \frac{1}{R_{cont}} - \alpha$, $\alpha > 0$. Using this approach, the term $\frac{1}{R_{cont}}$ approximately neutralizes the impact of the term $\frac{1}{R}$ in (4.20). Also, the value of α must be positive to meet the stability requirements of the system. Moreover, the value of α must be selected such that the condition $|\frac{1}{R_{cont}} - \frac{1}{R}| << \alpha$ is satisfied. This way, α plays the main role in shaping the dynamics instead of the load resistance. The characteristic polynomial of the closed-loop system can be given by $s^2 + \frac{\alpha}{C}s - \frac{k_i}{C} = 0$. The final step is to design k_i such that the roots of this polynomial acting as the system poles, have appropriate values. This completes the controller derivation and design, to achieve load-dynamics decoupling and fast load transient responses.

3.4.3 Discussions on the Proposed Control System

To implement the proposed controller more efficiently by using a reduced number of sensors and without load resistance calculation, one option is to use state observers and an adaptive algorithm to select the nominal load resistance value. As it can

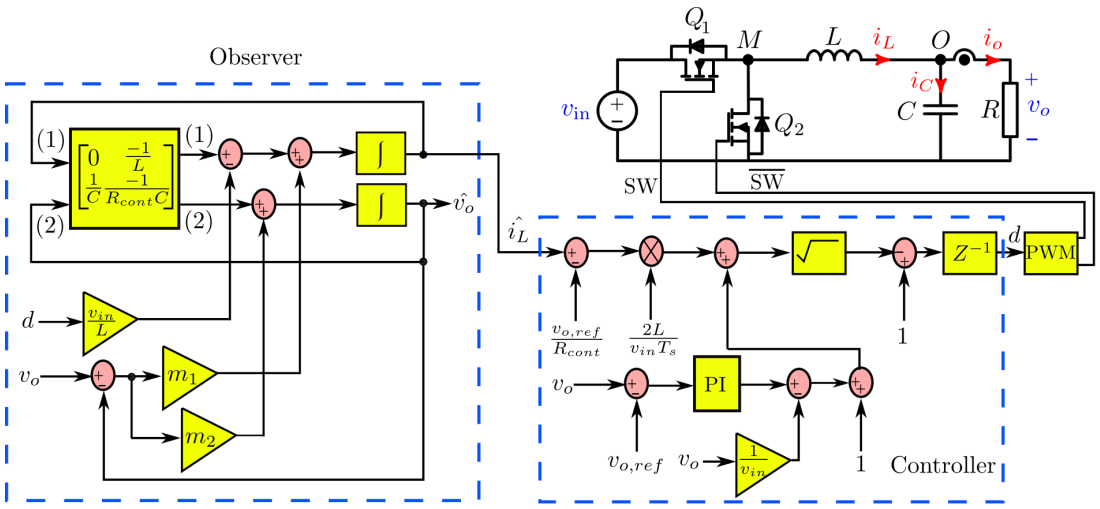


Figure 3.7: Buck Converter Schematic in CCM and Final Controller with Observer and Adaptive R selection Algorithm

be seen, terms including the inductor current i_L and the load resistance R exist in (3.7). In order to avoid an additional sensor for the inductor current, the control law is modified such that the inductor current i_L is estimated by a Luenberger observer. Moreover, as an integral term is applied to the difference between the output voltage and its reference value in (3.7), there is no need to know the exact value of L, C, and R to implement the control law. In order to improve the performance of the state observer used to estimate i_L, an adaptive algorithm is proposed to select the value of R in the control law, which will be discussed in the forthcoming sections. Fig. 3.7 shows the block diagram of the final controller embedded with state observer and adaptive R selection algorithm. As it can be seen in Fig. 3.7, the inductor current estimated by the observer $\hat{i_L}$, and the R value selected by the adaptive algorithm R_{cont} are applied to the control system.

3.4.4 State Observer Design in CCM

According to the above discussions, the inductor current should be estimated by a state observer. Therefore, a Luenberger observer is designed in this chapter and incorporated into the control law expressed by (3.7). To design the observer, the averaged model of a buck converter needs to be derived for the CCM operating mode. Using KVL in Fig. 3.5 and KCL at node O, the averaged model is derived as:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \\ \frac{dv_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L} \\ \\ \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{v_{in}}{L} \\ \\ 0 \end{bmatrix} d. \tag{3.9}$$

If the estimated values of i_L and v_o are denoted by $\hat{i_L}$ and $\hat{v_o}$, the Luenberger observer is implemented by:

$$\begin{bmatrix} \frac{d\hat{i_L}}{dt} \\ \\ \frac{d\hat{v_o}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L} \\ \\ \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} \hat{i_L} \\ \\ \hat{v_o} \end{bmatrix} + \begin{bmatrix} \frac{v_{in}}{L} \\ \\ 0 \end{bmatrix} d + \begin{bmatrix} m_1 \\ m_2 \end{bmatrix} (v_o - \hat{v_o}). \tag{3.10}$$

The observer gains m_1 and m_2 are designed such that the poles of the observer system in the Laplace domain lie at $\frac{-K_1}{2T_s}$ and $\frac{-K_2}{2T_s}$, in which K_1 and K_2 are positive values between 0 and 1. The goal is to set the observer speed, while complying with the Nyquist stability theorem. The characteristic polynomial of the observer is given by $s^2 + (\frac{1}{RC} + m_2)s + (\frac{m_1}{C} + \frac{1}{LC})$, according to (3.10). The observer gains are designed to make this polynomial equivalent to $(s + \frac{K_1}{2T_s})(s + \frac{K_2}{2T_s})$. Therefore, m_1 and m_2 are given by:

$$\begin{aligned} m_1 &= \frac{K_1 K_2 C}{4{T_s}^2} - \frac{1}{L} \\ m_2 &= \frac{K_1 + K_2}{2T_s} - \frac{1}{RC}. \end{aligned} \tag{3.11}$$

3.4.5 Adaptive Algorithm for R Value Selection in CCM

Based on previous discussions, an adaptive algorithm should be designed to select the value of R used to implement the controller. This value is different from the actual R value and is denoted by R_{cont}. In fact, to reduce the computational burden of the proposed controller, the real value of R is not used to implement the controller in CCM mode. Instead, the value of R is selected based on the load current level and a series of comparison actions. It is assumed that for a specific application, $i_{o,min} < i_o < i_{o,max}$. The $[i_{o,min}, i_{o,max}]$ interval is divided into N sub intervals with equal lengths. In this regard, the n-th sub-interval is denoted by $[i_{o,min,n}, i_{o,max,n}]$, in which $i_{o,min,n} = i_{o,min} + (n-1)\frac{i_{o,max} - i_{o,min}}{N}$ and $i_{o,max,n} = i_{o,min,n} + \frac{i_{o,max} - i_{o,min}}{N}$, $0 < n < N + 1$. Next, for every switching cycle during converter operation, successive comparisons are made to indicate which of these sub-intervals i_o belongs to. Assuming that the load current belongs to the j-th sub-interval, the value of R_{cont} is given by:

$$R_{cont} = \frac{2v_{o,ref}}{i_{o,min,j} + i_{o,max,j}} \tag{3.12}$$

The process of calculating R_{cont} is shown in Fig. 3.8. The load current i_o is compared with the maximum and minimum values of all sub-intervals and this indicates which of these sub-intervals i_o belongs to. Next, (3.12) is used to evaluate R_{cont}. In the next subsection, the block diagram of the controller is provided.

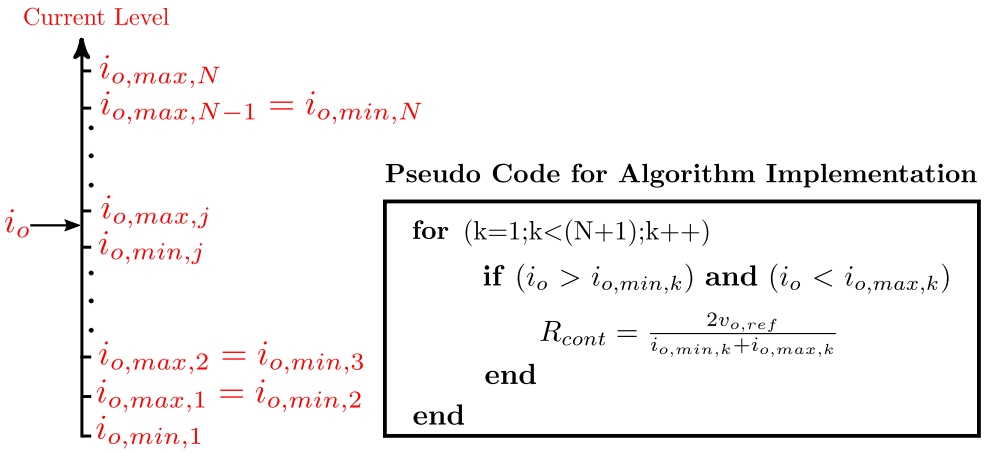


Figure 3.8: Implementation of R_{cont} Calculation Algorithm

3.4.6 Final Formulation and Block Diagram of Proposed Controller in CCM

In this subsection, the block diagram and the final formulation of the proposed controller are developed. In this regard, R_{cont} and the estimated inductor current $\hat{i_L}$ are incorporated into (3.7), to obtain the final control law expressed as:

$$d = 1 - \sqrt{\begin{array}{l} 1 - \frac{v_o}{v_{in}} + \frac{2L}{v_{in}T_s}\left(\hat{i_L} - \frac{v_{o,ref}}{R_{cont}}\right) \\ - \frac{2Lk_p}{v_{in}T_s}(v_o - v_{o,ref}) - \frac{2Lk_i}{v_{in}T_s}\int (v_o - v_{o,ref})dt \end{array}}. \tag{3.13}$$

The block diagram of the proposed control system is observable in Fig. 3.7. As this figure shows, the inductor current is first estimated by a Luenberger observer and then the estimated current is applied to the control system. Moreover, the controller uses R_{cont} as the nominal value for the load resistance.

3.4.7 Derivation of State Space Model of Closed-Loop System and Steady-State Analysis in CCM

To make a comprehensive analysis of the proposed controller, the state space representation of the closed-loop system should be derived. This enables performing steady-state, dynamics, stability, and sensitivity analyses for the proposed closed-loop system. Finding the equilibrium point of the system using the state-space representation enables steady-state analysis. Also, by linearizing the state-space model around the equilibrium point, the system poles can be found. The location of these poles indicate the stability status of the system, as well as its dynamical profile. Moreover, by changing different contoller and system parameters, it can be investigated that how sensitive the poles' locations are to these changes. The closed-loop system associated with the proposed controller can be described using (3.9) the

averaged model of a buck converter in CCM, (3.10) the observer model, and (3.13) the control law. To conduct the analysis, the term $f = \int (v_o - v_{o,ref})dt$ is defined. Also, it is assumed that instead of the real L and C values, the observer and the controller use L_f and C_f for the inductance and capacitance values. Considering i_L, v_o, $\hat{i_L}$, $\hat{v_o}$, and f as state variables of the system, (3.9), (3.10), (3.13) may be used to obtain the state space model of the closed-loop system as:

$$\begin{aligned}
\frac{di_L}{dt} &= -\frac{v_o}{L} + \frac{v_{in}}{L}\left[1 - \sqrt{\begin{aligned}&1 - \frac{v_o}{v_{in}} + \frac{2L_f}{v_{in}T_s}\left(\hat{i_L} - \frac{v_{o,ref}}{R_{cont}}\right)\\ &- \frac{2L_f k_p}{v_{in}T_s}(v_o - v_{o,ref}) - \frac{2L_f k_i}{v_{in}T_s}f\end{aligned}}\right]\\
\frac{dv_o}{dt} &= \frac{i_L}{C} - \frac{v_o}{RC}\\
\frac{d\hat{i_L}}{dt} &= -\frac{\hat{v_o}}{L_f} + \frac{v_{in}}{L_f}\left[1 - \sqrt{\begin{aligned}&1 - \frac{v_o}{v_{in}} + \frac{2L_f}{v_{in}T_s}\left(\hat{i_L} - \frac{v_{o,ref}}{R_{cont}}\right)\\ &- \frac{2L_f k_p}{v_{in}T_s}(v_o - v_{o,ref}) - \frac{2L_f k_i}{v_{in}T_s}f\end{aligned}}\right]\\
&+ m_1(v_o - \hat{v_o})\\
\frac{d\hat{v_o}}{dt} &= \frac{\hat{i_L}}{C_f} - \frac{\hat{v_o}}{R_{cont}C_f} + m_2(v_o - \hat{v_o})\\
\frac{df}{dt} &= v_o - v_{o,ref}.
\end{aligned} \tag{3.14}$$

The values of the states variables of the system at the equilibrium point are denoted by ${i_L}^*$, ${v_o}^*$, ${\hat{i_L}}^*$, ${\hat{v_o}}^*$ and f^*, respectively. If the time-derivatives of the state variables of the system are set equal to zero in (3.14), the equilibrium point values are found as ${v_o}^* = {\hat{v_o}}^* = v_{o,ref}$, ${i_L}^* = \frac{v_{o,ref}}{R}$, ${\hat{i_L}}^* = \frac{v_{o,ref}}{R_{cont}}$, and $f^* = \frac{v_{in}v_{o,ref}T_s - {v_{o,ref}}^2 T_s}{2L_f v_{in}k_i}$. The detailed derivation process of this equilibrium point is provided below. Using the $\frac{df}{dt}$ mathematical expression in (3.14), the equilibrium point f^* can be found as $\frac{df}{dt}@(f = f^*) = {v_o}^* - v_{o,ref} = 0$. In other words, ${v_o}^* = v_{o,ref}$. Using the mathematical expression for $\frac{dv_o}{dt}$ in (3.14) results in $\frac{dv_o}{dt}(v_o = {v_o}^*) = \frac{{i_L}^*}{C} - \frac{{v_o}^*}{RC} = 0$. As a result, ${i_L}^* = \frac{{v_o}^*}{R} = \frac{v_{o,ref}}{R}$. Similarly, setting $\frac{di_L}{dt}@(i_L = {i_L}^*) = 0$ in (3.14) results in:

$$\left[1 - \sqrt{\begin{aligned}&1 - \frac{{v_o}^*}{v_{in}} + \frac{2L_f}{v_{in}T_s}\left({\hat{i_L}}^* - \frac{v_{o,ref}}{R_{cont}}\right)\\ &- \frac{2L_f k_p}{v_{in}T_s}({v_o}^* - v_{o,ref}) - \frac{2L_f k_i}{v_{in}T_s}f^*\end{aligned}}\right] = \frac{v_{o,ref}}{v_{in}}. \tag{3.15}$$

Using $\frac{d\hat{i_L}}{dt}$ in (3.14) as well as (3.15) results in $\frac{d\hat{i_L}}{dt}@(\hat{i_L} = {\hat{i_L}}^*) = -\frac{{\hat{v_o}}^*}{L_f} + \frac{v_{in}v_{o,ref}}{L_f v_{in}} + m_1(v_{o,ref} - {\hat{v_o}}^*) = 0$. As a result, ${\hat{v_o}}^* = v_{o,ref}$. Using this result and expression of $\frac{d\hat{v_o}}{dt}$ in (3.14) result in $\frac{d\hat{v_o}}{dt}@(\hat{v_o} = v_{o,ref}) = \frac{\hat{i_L}}{C_f} - \frac{\hat{v_o}}{R_{cont}C_f} + m_2(v_{o,ref} - v_{o,ref})$. From this equation, ${\hat{i_L}}^* = \frac{v_{o,ref}}{R_{cont}}$ is obatined. This result as well as other obtaine dequilibrium point values, along with (3.15) yield $f^* = \frac{v_{in}v_{o,ref}T_s - {v_{o,ref}}^2 T_s}{2L_f v_{in}k_i}$. This completes the

derivation process for the equilibrium point of the closed-loop system. As observed from the derivation, there is no steady-state error in the output voltage of the converter, regardless of mismatches between L_f and L, C_f and C, and R_{cont} and R.

3.4.8 Dynamics, Stability, and Sensitivity Analyses in CCM

In this subsection, the dynamics of the system is investigated for the proposed controller in CCM. Next, the system poles are calculated and shown to be on the left half of s-plane, guaranteeing a stable operation.

To conduct the analysis, the state space model presented in (3.14) is linearized around the equilibrium point. Following this method, the Jacobian matrix associated with the system J can be calculated. Using this matrix, the system poles can be calculated and used later on to investigate the dynamical characteristics of the system, as well as the system stability. Also, the effect of controller and converter parameter values on the locations of the poles can be investigated using case studies and the root locus analysis. The Jacobian matrix J is given by:

$$J = \left[\; J_1 \mid J_2 \mid J_3 \mid J_4 \mid J_5 \; \right] \tag{3.16}$$

in which, J_1, J_2, J_3, J_4, and J_5 are the first, second, third, fourth, and fifth columns of the Jacobian matrix and are given by:

$$\begin{gathered}
J_1 = \begin{bmatrix} 0 \\ \frac{1}{C} \\ 0 \\ 0 \\ 0 \end{bmatrix}, J_2 = \begin{bmatrix} \frac{2L_f k_p v_{in} - v_{in} T_s + 2T_s v_{o,ref}}{2LT_s(v_{in} - v_{o,ref})} \\ \frac{-1}{RC} \\ \frac{(2L_f k_p + T_s)v_{in} + 2L_f T_s m_1 (v_{in} - v_{o,ref})}{2L_f T_s (v_{in} - v_{o,ref})} \\ m_2 \\ 1 \end{bmatrix} \\
J_3 = \begin{bmatrix} \frac{-L_f v_{in}}{LT_s(v_{in} - v_{o,ref})} \\ 0 \\ \frac{-v_{in}}{T_s(v_{in} - v_{o,ref})} \\ \frac{1}{C_f} \\ 0 \end{bmatrix}, J_4 = \begin{bmatrix} 0 \\ 0 \\ \frac{-m_1 L_f - 1}{L_f} \\ \frac{-1 - m_2 R_{cont} C_f}{R_{cont} C_f} \\ 0 \end{bmatrix} \\
J_5 = \begin{bmatrix} \frac{L_f k_i v_{in}}{LT_s(v_{in} - v_{o,ref})} \\ 0 \\ \frac{k_i v_{in}}{T_s(v_{in} - v_{o,ref})} \\ 0 \\ 0 \end{bmatrix}.
\end{gathered} \tag{3.17}$$

To investigate the stability of the system and the sensitivity of the system poles to the mismatches between L and L_f, C and C_f, and R and R_{cont}, the following case-study is provided.

Case Study 2: A buck converter with v_{in}=12V, $v_{o,ref}$=3.5V, L=6 μH, f_s=200 KHz, and C=30μF and R=1.8Ω is assumed. It is also assumed that k_i=-5000 and $k_p = \frac{1}{R_{cont}} - \alpha$, in which $4 < \alpha < 9$ and R_{cont}=1.25 Ω. Two cases are considered. In the first case, $L_f = L$ and $C_f = C$), while $L_f = 1.5L$ and $C_f = 1.5C$ in the latter. The poles of the system which are the eigenvalues of the matrix J based on (3.16) and (3.17) are plotted for $4 < \alpha < 9$. The obtained root-locus diagram is given in Fig. 3.9. As this figure shows, the sensitivity of the system poles to the variations of L_f and C_f is low. Moreover, as the system poles are on the left half of the s-plane, the system is stable. As Fig. 3.9 suggests, the real values of the system poles are comparable to f_s. Therefore, the closed-loop system has fast dynamics. In the next subsection, the proposed controller is extended to DCM for a buck converter.

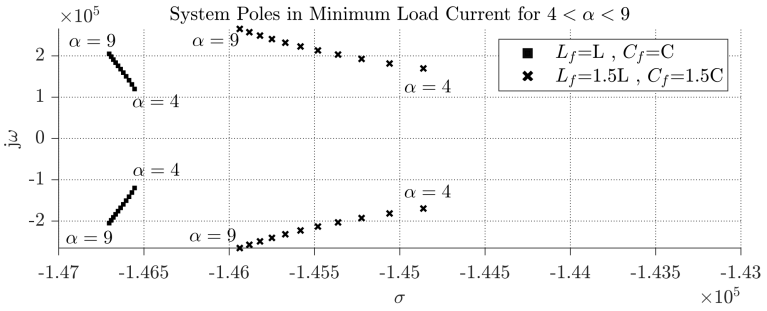


Figure 3.9: Root Locus Diagram for Proposed Controller in Case Study 2

3.4.9 Controller Design Procedure in CCM

In this subsection, the controller design procedure for a buck converter operating in CCM is presented. The approach used here is based on derivation of open loop transfer function of the system and desingning controller parameters to obtain optimal phase margin, gain margin, and bandwidth levels. In this subsection, $\tilde{V_o}(s)$, $\tilde{V}_{o,ref}(s)$, $\tilde{\hat{V}_o}(s)$, $\tilde{\hat{I}_L}(s)$ $\tilde{D}(s)$, and $\tilde{R}(s)$ denote small signal variations of the output voltage, reference output voltage, observer estimated output voltage, observer estimated inductor current, duty cycle, and the load resistance in Laplace domain, respectively. Also, the signal values in the equilibrium point are marked by $*$ sign, similar to the previous subsection. If (3.10) is linearized around the equilibrium point, rewritten in the Laplace domian, and finally solved for $\tilde{\hat{I}_L}(s)$ in terms of $\tilde{V_o}$ and $\tilde{D}$,$\tilde{\hat{I}_L}(s)$ is obtained as:

$$\begin{aligned}
\tilde{\hat{I}_L} &= H_1(s)\tilde{D} + H_2(s)\tilde{V_o} \\
H_1(s) &= \frac{\frac{v_{in}}{L}s + \frac{v_{in}}{L}(m_2 + \frac{1}{R_{cont}C})}{s^2 + (m_2 + \frac{1}{R_{cont}C})s + \frac{m_1 L+1}{LC}} \\
H_2(s) &= \frac{m_1 s + \frac{m_1}{R_{cont}C} - \frac{m_2}{L}}{s^2 + (m_2 + \frac{1}{R_{cont}C})s + \frac{m_1 L+1}{LC}}.
\end{aligned} \tag{3.18}$$

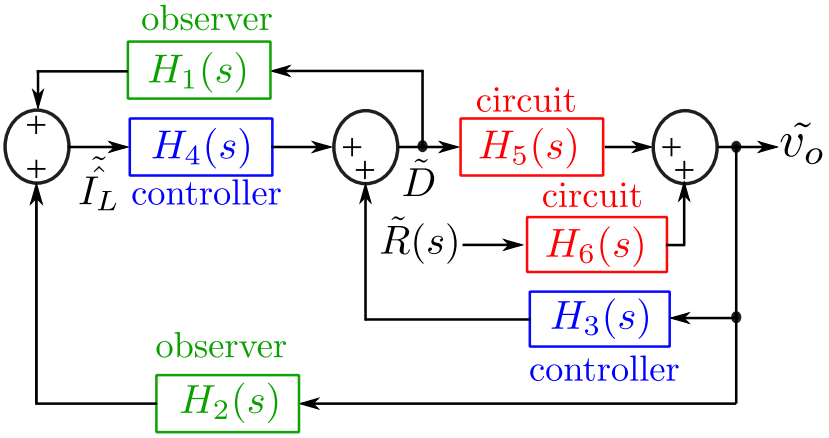


Figure 3.10: Small-signal Model of the Closed-loop System in Laplace Domain

In this subsection, only the effect of $\tilde{R}(s)$ on the output voltage is of interest. Therefore, it is assumed that $v_{o,ref}$ is constant during load step i.e. $\tilde{V}_{o,ref}(s) = 0$. This assumption, along with linearizing (3.13) around the equilibrium point and rewriting the obtained equation in the Laplace domain lead to:

$$\begin{aligned} \tilde{D} &= H_3(s)\tilde{V}_o + H_4(s)\tilde{\hat{I}}_L \\ H_3(s) &= \frac{\left(\frac{-1}{v_{in}} - \frac{2Lk_p}{v_{in}T_s}\right)s - \frac{2Lk_i}{v_{in}T_s}}{(2d^* - 2)s} \\ H_4(s) &= \frac{2L}{v_{in}T_s(2d^* - 2)}. \end{aligned} \tag{3.19}$$

By writing KCL in node O of the buck converter in Fig. 3.7, linearizing it around the equilibrium point, and rewriting the resultant equation in the Laplace domain, $\tilde{I}_L(s)$ is obtained as:

$$\tilde{I}_L(s) = \left(Cs + \frac{1}{R^*}\right)\tilde{V}_o - \frac{{v_o}^*}{{R^*}^2}\tilde{R}. \tag{3.20}$$

Also, from the same figure, it is known that $v_{in}\tilde{d} - \tilde{v_o} = L\frac{d\tilde{i_L}}{dt}$. Rewriting this equation in Laplace domian as well as (3.20) lead to:

$$\begin{aligned} \tilde{V_o}(s) &= H_5(s)\tilde{D}(s) + H_6(s)\tilde{R}(s) \\ H_5(s) &= \frac{v_{in}}{LCs^2 + \frac{L}{R}s + 1} \\ H_6(s) &= \frac{L{v_o}^*s}{{R^*}^2(LCs^2 + \frac{L}{R}s + 1)}. \end{aligned} \tag{3.21}$$

The controller, circuit, and observer loops are shown in Fig. 3.10. According to this figure, the open loop transfer function of the system $\Gamma(s)$ is given by:

$$\Gamma(s) = \frac{-H_5(s)(H_4(s)H_2(s) + H_3(s))}{1 - H_1(s)H_4(s)} = \frac{\sum_{l=1}^{3} a_l s^l}{\sum_{o=1}^{5} b_o s^o} \tag{3.22}$$

in which,

$$\begin{aligned}
&a_3 = 2RCR_{cont}k_pL^2 + RR_{cont}CT_sL \\
&a_2 = -2CL^2RR_{cont}(-m_1 + k_i + k_pm_2) + 2L_2Rk_p + LRT_s \\
&+ LCRR_{cont}T_sm_2 \\
&a_1 = -2L^2R(m_1 - k_i - R_{cont}k_pm_1 - CR_{cont}k_im_2) + R \\
&\times R_{cont}(T_s + 2Lk_p + LT_sm_1 + 2LCm_2) \\
&a_0 = k_iL(m_1L + 1)
\end{aligned} \tag{3.23}$$

and,

$$\begin{aligned}
&b_5 = 2C^2L^2RR_{cont}T_s(d^* - 1) \\
&b_4 = 2CL^2T_s(d^* - 1)(R + R_{cont}) - 2C^2L^2RR_{cont} \\
&\times(1 + T_sm_2(1 - d^*)) \\
&b_3 = [T_s(d^* - 1) - CR_{cont}(1 + T_s(1 - d^*)(m_2 + Rm_1))] \\
&\times 2L^2 - 2C^3L^2R - 2C^2L^2RR_{cont}m_2 \\
&- 4LCRR_{cont}T_s(1 - d^*) \\
&b_2 = 2LT_s(d^* - 1)(R_{cont} + R + LR_{cont}m_1) - 2CL^2R_{cont} \\
&\times m_2 - 2L^2C^2 - 2LCRR_{cont}(1 + T_sm_2(1 - d^*)) \\
&b_1 = -2LRC^2 - 2LRR_{cont}(m_2C + m_1T_s(1 - d^*)) - 2R \\
&\times R_{cont}T_s(1 - d^*) \\
&b_0 = 0.
\end{aligned} \tag{3.24}$$

Also, the transfer function $H_7(s) = \frac{\tilde{V}_o(s)}{\tilde{R}(s)}$ can be obtained as:

$$H_7(s) = \frac{\tilde{V}_o(s)}{\tilde{R}(s)} = \frac{H_6(s)}{1 + \Gamma(s)}. \tag{3.25}$$

Case Study 3: This case study verifies the accuacy of (3.25). A buck converter operating in CCM is assumed with v_{in} =12V, $v_{o,ref}$=3.3V, L =6.3μH, C =30μF, and f_s =200KHz. The buck converter feeds a resistive load and the load current changes from 5.1A to 1.7A in a load step. The closed-loop system is simulated in PSIM and the output voltage waveform during transient period is recorded and averaged over each individual switching cycle. Next, in MATLAB, an equivalent load step is applied to a system expressed by $H_7(s)$ in (3.25) and the output voltage waveform is observed. The output voltage waveforms obtained by PSIM simulation and transfer function simulation in MATLAB are compared with each other in Fig. 5.6. As this figure illustrates, these two waveforms are appoximately identical after the first four switching cycles during load step transient. The differences observed in the first four switching periods is due to the fact that the proposed system model is an averaged model and may be not exactly equal to the actual system model at high frequencies close to the switching frequency. However, the undershoot level and recovery time values and other dynamical characteristics are predicted well by (3.25) in Fig. 5.6. This validates the accuracy of system model derived in this subsection.

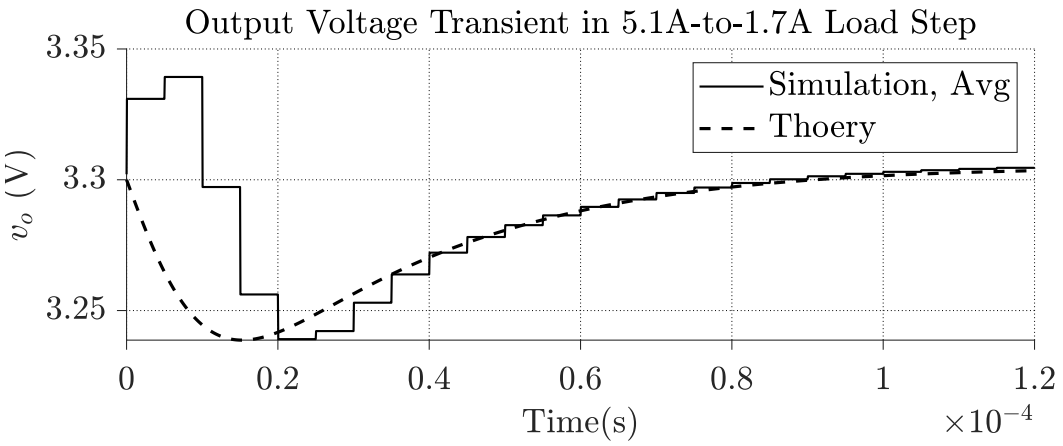


Figure 3.11: Comparison between Theoretical and Simulation Load Step Responses Using the Proposed Controller in Case Study 3

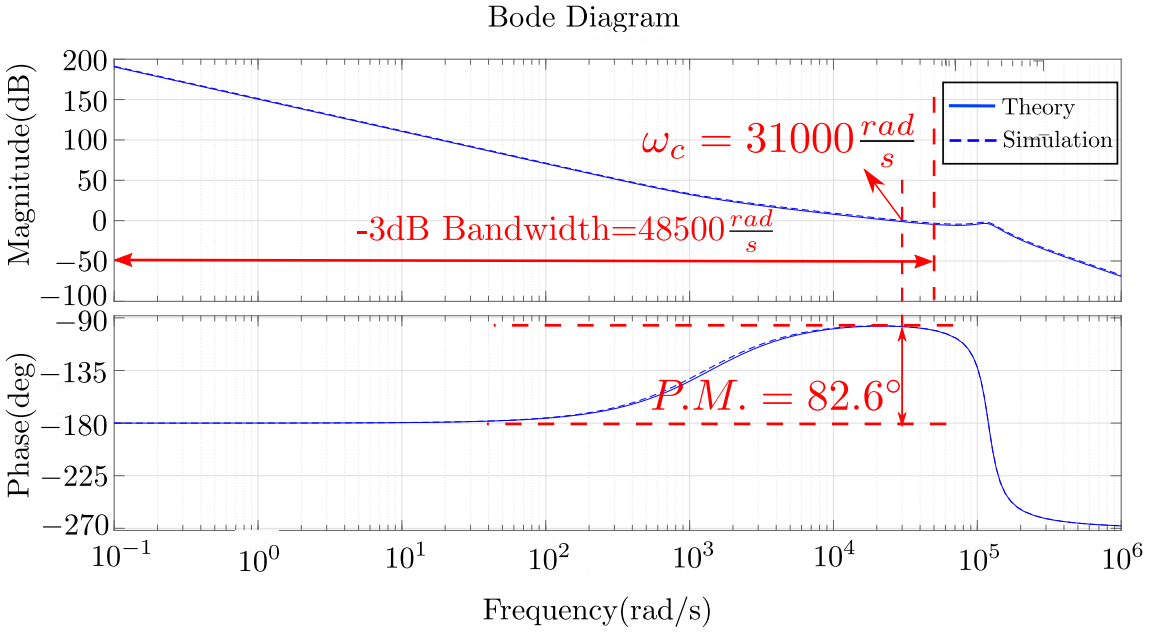


Figure 3.12: Bode plot Associated with Open Loop Transfer Functon γ(s) in Case Study 3

Fig. 5.6 is obtained using these control parameters: $k_1 = k_2$=0.5, $k_p = \frac{-1}{R_{cont}}$+18, $k_i = -40000$, and R_{cont} =1.53Ω. The bode plot associated with the open loop transfer function γ(s) of the system with these control parameters in this case study is plotted in Fig. 3.12. As this figure shows, the crossover frequency and the phase margin values are 1.12e+5 rad/s and 62.8°, respectively. The parameters are designed such that the phase margin becomes close to the ideal value of 60 degrees. According to Fig. 5.6, the undershoot levels is below 2 percent of the nominal output voltage. Also, the recovery time is 8 switching cycles. This is in accordance with a suitable phase margin and bandwidth level in Fig. 3.12.

To ensure the propsoed controller is designed with sutiable phase margin and

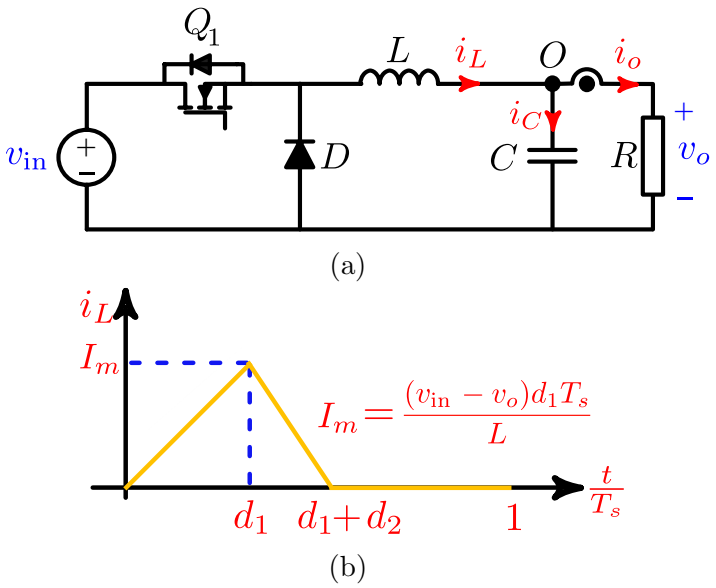


Figure 3.13: (a) Schematic of a buck converter in DCM and (b) inductor current waveform in DCM

bandwidth levels, the controller design procedure should include the following steps:

Step 1:: The parameter values for k_1 and k_2 are selected to set observer dynamics. Typically, $k_1 = k_2 = 0.5$ is suitable. The observer gains m_1 and m_2 are then calculated based on (3.11).

Step 2: Assuming $i_{o,min} < i_o < i_{o,max}$, a value is selected for N and R_{cont} is evaluated online based on Fig. 3.8.

Step 3: Since the proposed controller decouples converter dynamics from the load, the open loop transfer function Γ)(s) in (3.22), (3.23), and (3.24) approximately remains unchanged with variations of R. Therefore, by arbitrarily taking $R = \frac{v_{o,ref}}{i_{o,max}}$, (3.22),(3.23), and (3.24) are used to design k_p and k_i values to obtain target values for ω_c and phase margin. Normally, a phase margin of 60 degrees is desirable. In fact, to reach the target ω_c and phase margin levels, two nonlinear equations based on $|\Gamma(j\omega)|$ and the phase of $\Gamma(j\omega)$ should be solved using numerical methods. The process mentiond in Steps 1-3 is done for Case Study 3 and the resultant control parameters and bode diagram are discussed in previous paragraphs.

3.4.10 Controller Derivation and Design for Buck Converter in DCM

This subsection shows how the proposed controller discussed in the previous subsections can be extended to a buck converter operating in Discontinuous Conduction Mode (DCM). The schematic of a buck converter operating in DCM, as well as the inductor current waveform are shown in Fig. 3.13. KCL at node O in Fig. 3.13 results in:

$$i_L = i_c + i_o = C\frac{dv_o}{dt} + \frac{v_o}{R}. \tag{3.26}$$

By averaging both sides of (3.26) over one switching cycle during transient, $i_{L,avg}$ is obtained as follows:

$$i_{L,avg} = \frac{C(v_o(T_s) - v_o(0))}{T_s} + \frac{v_o(0)}{R}. \tag{3.27}$$

In (3.27), $v_o(T_s)$ and $v_o(0)$ are output voltage values at the ending and the beginning instants of a switching cycle, respectively. Also, in the averaging process used to derive the second term in the right hand side of (3.27), it is assumed that the output voltage approximately remains constant during one switching cycle. This assumption results in the average of v_o to be equal to $v_o(0)$, within one switching cycle. Using the inductor current waveform shown in Fig. 3.13(b), the average inductor current can be found as:

$$i_{L,avg} = \frac{(v_{in} - v_o(0))T_s d_1(d_1 + d_2)}{2L}. \tag{3.28}$$

In Fig. 3.13, when Q_1 is conducting, the inductor voltage is $v_{in} - v_o$ and when D is conducting, the inductor voltage is $-v_o$. Therefore, using Fig. 3.13(b) and considering the time-derivative of the inductor current imposed by the inductor voltage during a switching cycle, (20) is obtained as:

$$\frac{d_2}{d_1} = \frac{v_{in} - v_o(0)}{v_o(0)}. \tag{3.29}$$

By eliminating d_2 between (3.28) and (3.29), $i_{L,avg}$ is obtained as follows:

$$i_{L,avg} = \frac{(v_{in} - v_o(0))T_s v_{in} {d_1}^2}{2Lv_o(0)}. \tag{3.30}$$

From (3.27) and (3.30):

$$\frac{(v_{in} - v_o(0))T_s v_{in} {d_1}^2}{2Lv_o(0)} = C\frac{dv_o}{dt} + \frac{v_o(0)}{R}. \tag{3.31}$$

As stated earlier, the system's dynamic profile gets degraded at high load current levels, or equivalently low R values. So, based on (3.31), the control law is designed to decouple $\frac{dv_o}{dt}$ from R. The control law is selected to artificially produce a term of $\frac{v_o(0)}{R}$ in the left hand side of (3.31). This way, the two terms of $\frac{v_o(0)}{R}$ in both sides of (3.31) cancel out each other and the system dynamics gets decoupled from R. The targeted dynamics for v_o is $\frac{dv_o}{dt} = g(v_o)$, in which $g(v_o)$ is a function of v_o. To realize this dynamics, the control law is desgined as:

$$d_1 = \sqrt{\frac{2L{v_o}^2}{RT_s v_{in}(v_{in} - v_o)} + f(v_o)} \tag{3.32}$$

where, $f(v_o)$ is a function of the output voltage, which directly stipulates the system dynamics and should be selected. Equations (3.31) and (3.32) result in the closed-loop dynamics expressed by:

$$\frac{dv_o}{dt} = \frac{(v_{in} - v_o)T_s v_{in}}{2LCv_o} f(v_o) = g(v_o). \tag{3.33}$$

At this point, the constraints associated with $f(v_o)$ need to be derived. To have the equilibrium point at $v_o = v_{o,ref}$, the requirement of $g(v_{o,ref}) = 0$ must be met. Using this requirement and (3.33), along with the Taylor series of the function $g(v_o)$ around the point of $v_o = v_{o,ref}$, (3.34) is obtained. In derivation of (3.34), terms with order 2 and above are ignored.

$$\frac{dv_o}{dt} = \left[\frac{\partial g(v_o)}{\partial v_o}@(v_o = v_{o,ref})\right](v_o - v_{o,ref}) \tag{3.34}$$

Equation (3.34) represents a first-order dynamic system with the pole of $-\frac{\partial g(v_o)}{\partial v_o}@(v_o = v_{o,ref})$. According to the Nyquist stability criterion, the system pole cannot be made less than $\frac{-1}{2T_s}$, which itself provides the fastest system dynamics possible. As (3.34) is derived by ignoring terms with order 2 and above in the Taylor series, the system pole must be placed at $\frac{-K}{2T_s}$, in which K is a real number between 0 and 1. The K's value must be selected slightly less than 1 to ensure system stability regardless of the mentioned ignored terms. The discussed concepts and (3.34) result in:

$$\frac{\partial g(v_o)}{\partial v_o}@(v_o = v_{o,ref}) = \frac{-K}{2T_s}. \tag{3.35}$$

Equations (3.34) and (3.35) result in:

$$\frac{df}{dv_o}@(v_o = v_{o,ref}) = \frac{-KLCv_{o,ref}}{(v_{in} - v_{o,ref}){T_s}^2 v_{in}}. \tag{3.36}$$

There are many functions satisfying (3.36) and $f(v_{o,ref}) = 0$. In this chapter, the following linear function is selected:

$$f(v_o) = \frac{-KLCv_{o,ref}}{(v_{in} - v_{o,ref}){T_s}^2 v_{in}}(v_o - v_{o,ref}). \tag{3.37}$$

To satisfy the Nyquist stability criterion, the fastest possible rate for $\frac{dv_o}{dt}$ can be expressed by $\frac{-1}{2T_s}(v_o - v_{o,ref})$. Moreover, selecting the linear function expressed by (3.37) results in a $\frac{dv_o}{dt}$ which is equal to $g(v_o)$, as illustrated by (3.33). Equations (3.32) and (3.37) result in (3.38), which expresses the final control law for DCM.

$$d_1 = \sqrt{\frac{2L{v_o}^2}{RT_s v_{in}(v_{in} - v_o)} + \frac{-KLCv_{o,ref}(v_o - v_{o,ref})}{(v_{in} - v_{o,ref}){T_s}^2 v_{in}}} \tag{3.38}$$

The overall control system is shown in Fig. 3.14. As Fig. 3.14 illustrates, the load resistance value applied to the controller R_{cont}, is calculated by dividing the output voltage by the load current. Next, using (3.38), the duty cycle is calculated.

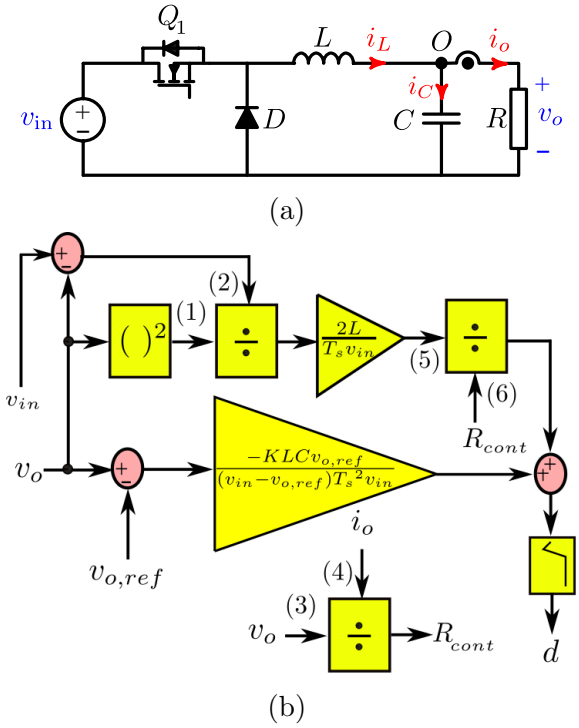


Figure 3.14: (a) Schematic of a buck converter in DCM and (b) Proposed Controller

3.4.11 Verification of the Controller's Derivation Process

In this subsection, the accuracy of the controller derivation process is shown. As mentioned earlier, the proposed controller places the system's pole at $\frac{-K}{2T_s}$. This suggests that the system's time constant is $\frac{2T_s}{K}$, regardless of the load step magnitude. To validate the provided equations, the following case studies are provided.

Case Study 3: This case study assumes a 1A-to-10A load step in a buck converter with $v_{in} = 12V$, $v_{o,ref} = 3.3V$, $f_s = 200KHz$, $L = 500nH$, $C = 600\mu F$. Using computer simulations, the system's time constants are measured and plotted vs. K in Fig. 3.15. This figure compares simulation results with the time constant equation of $\frac{2T_s}{K}$ obtained by theoretical analysis. Fig. 3.15 shows that the theoretical and the simulation results are matched well.

Case Study 4: This case study assumes the two load steps of 1A-to-4A and 1A-to-10A and $K = 0.7$, in the same converter as in Case Study 3. Fig. 3.16 shows the associated voltage transients, suggesting identical dynamic speeds for both load steps. After a load step, it takes one switching cycle for the controller to see the R's value change and another cycle to calculate the required duty cycle. In the third switching cycle, the duty cycle is updated and the output voltage starts to recover, resulting in presence of an inevitable overshoot/undershoot. The overshoot/undershoot level is determined by load step magnitude, as a current with the same level flows through the capacitor within the first two cycles after a load step. The proposed controller minimizes the overshoot/undershoot level and the output voltage starts recovering after these two cycles, avoiding any extra voltage deviations. Fig. 3.16 illustrates the concepts discussed.

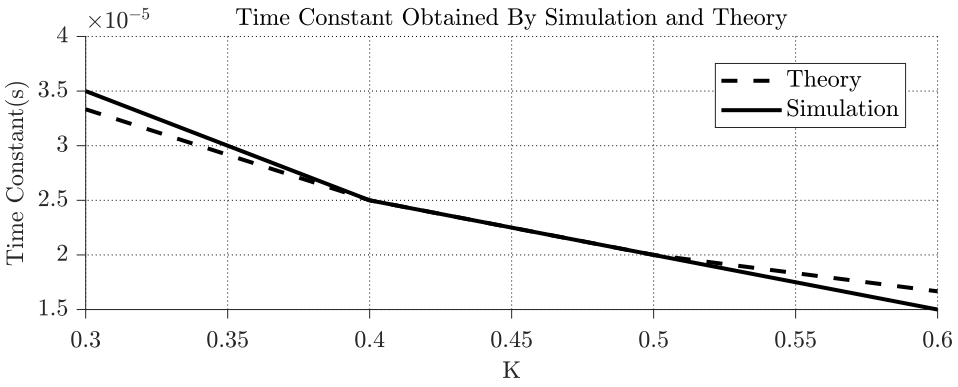


Figure 3.15: Comparison between the theoretical and simulation values of Time Constants

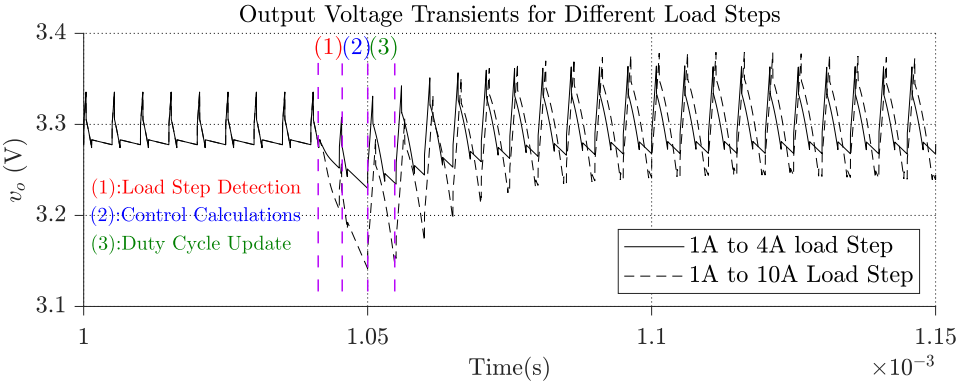


Figure 3.16: Output Voltage Transients for Different Load Steps

3.4.12 Controller Analysis

Stability Analysis: To conduct the stability analysis, (3.31) and (3.38) can be used to derive the closed-loop system model as:

$$\frac{dv_o}{dt} = \frac{-Kv_{o,ref}(v_o - v_{o,ref})(v_{in} - v_o)}{2T_s v_o(v_{in} - v_{o,ref})}. \tag{3.39}$$

Applying $v_o = v_{o,ref}$ to (3.39), $\frac{dv_o}{dt} = 0$ is obtained. Linearizing (3.39) around the system equilibrium point $v_o = v_{o,ref}$ leads to:

$$\frac{dv_o}{dt} = \frac{-K}{2T_s}(v_o - v_{o,ref}). \tag{3.40}$$

Equation (3.40) shows that the system has one pole at $\frac{-K}{2T_S}$ which is always in the negative half of s-plane, ensuring system stability. Fig. 3.17 shows the root locus diagram of the system for $f_s = 200$KHz and $0.2 < K < 1$.

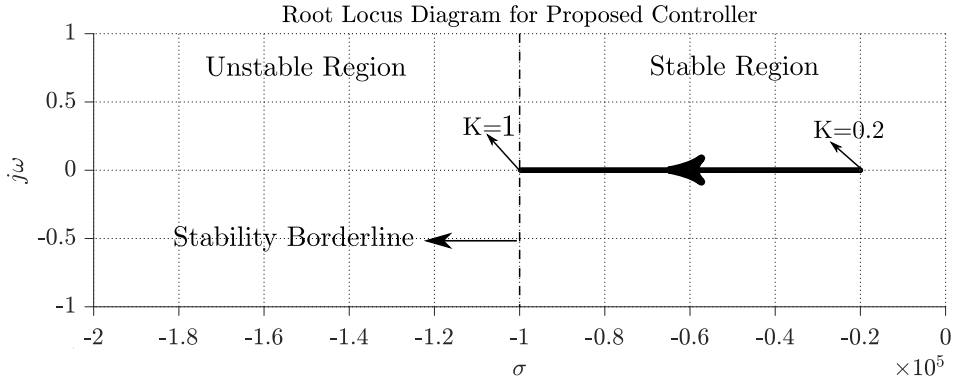


Figure 3.17: Root Locus Diagram for the Proposed Controller

Sensitivity Analysis for Steady-State: This part investigates how the uncertainties in L and C values affect the system performance. It is assumed that the controller uses L_f and C_f as inductance and capacitance values, while the corresponding actual values are L and C, respectively. Equations (3.31) and (3.38) result in (3.41), which expresses the system model in state-space domain under these assumptions.

$$\frac{dv_o}{dt} = \frac{(L_f - L)v_o}{LRC} + \frac{KL_fC_f(v_o - v_{in})v_{o,ref}(v_o - v_{o,ref})}{2LCv_oT_s(v_{in} - v_{o,ref})} \tag{3.41}$$

The steady-state value of the output voltage is denoted by $v_o{}^*$, which is assumed to be close to $v_{o,ref}$ in value. This assumption will later be verified. Using this assumption, the right hand side of (3.41) can be approximated by its first-order equivalent Taylor series around $v_o = v_{o,ref}$. Setting $\frac{dv_o}{dt} = 0$ in (3.41) and writing the first-order Taylor series of right hand side of (3.41) around $v_o = v_{o,ref}$ result in:

$$\frac{v_o{}^* - v_{o,ref}}{v_{o,ref}} = \frac{2(L_f - L)T_s}{RC_fKL_f}, \tag{3.42}$$

which expresses the steady-state error in the output voltage as a function of uncertainties in L and C values. Case Study 5 validates (3.42).

Case Study 5: To validate (3.42), a buck converter is assumed with L=500nH, C=600μF, K=0.7, $v_{o,ref}$=3.3V, f_s=200KHz, v_{in}=12V, and R=0.33Ω. Also, it is assumed that L_f and C_f vary between 80 percent and 120 percent of L and C, respectively. Fig. 3.18 makes a comparison between the output voltage error in percent obtained by (3.42) and simulations. The waveforms correspond to either $L_f \neq L, C_f = C$ or $C_f \neq C, L_f = L$. Fig. 3.18 shows that the general profiles of waveform variations are the same in simulation and theoretical results. There is just a small constant difference of 0.25 percent between simulation and theoretical results, which arises from assuming the output voltage constant in a switching cycle while deriving the controller. Fig. 3.18 suggests a maximum output voltage error of 1.5 percent, validating the previous assumption in derivation of (3.42). This also shows that the proposed controller has a low steady-state sensitivity.

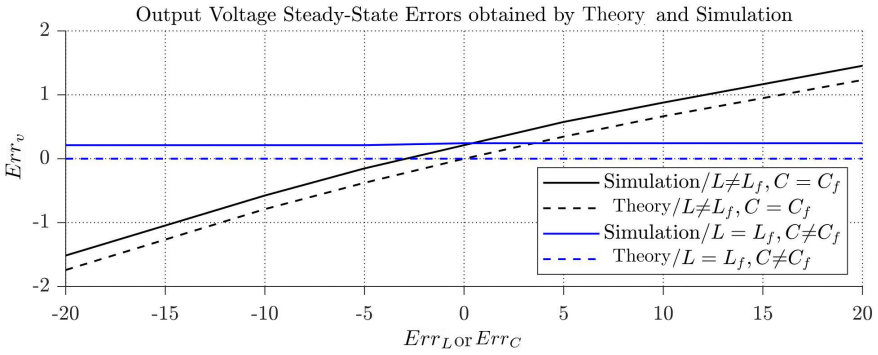


Figure 3.18: Comparison Between Output Voltage Error in Percent Predicted by (3.42) and Obtained by Simulation: Err_v: Output Voltage Error in Percent, Err_L: Error Percentage for the Inductor Value Used by the Controller, Err_C: Error Percentage for the Capacitor Value Used by the Controller

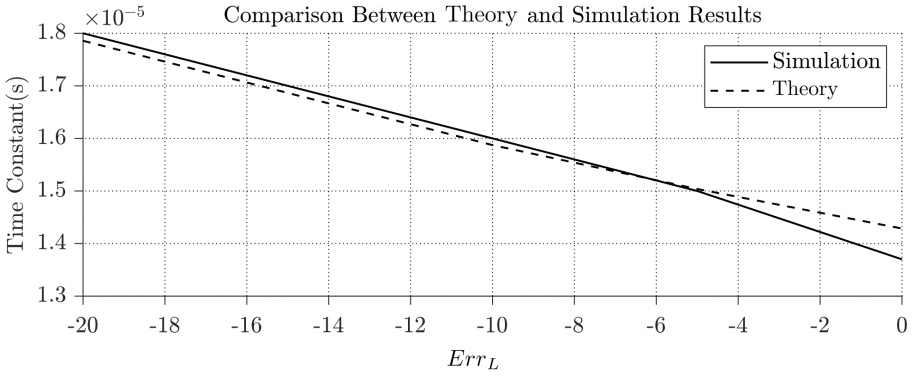


Figure 3.19: Comparison Between Output Voltage's Time Constant Predicted by (3.43) and Obtained by Simulation: Err_L: Error Percentage for the Inductor Value Used by the Controller

Sensitivity Analysis for Load Transient Recovery Times: To analyze the system performance in the transient period, equation (3.41) must be linearized around the equilibrium point. For this purpose, the derivative of right hand side of (3.41) with respect to v_o is calculated at $v_o{}^*$. Using this approach, the system pole λ is found as expressed by (3.43). Case Study 6 validates (3.43).

$$\lambda = \left(\frac{-K}{2T_s}\right)\left(\frac{L_f C_f}{LC}\right) = \left(\frac{-K}{2T_s}\right)\alpha \tag{3.43}$$

Case Study 6: In this case study, the system parameters are the same as in Case Study 5. The time constants of the output voltage predicted by (3.43) and obtained by simulations are compared in Fig. 3.19, showing matched values. This validates (3.43).

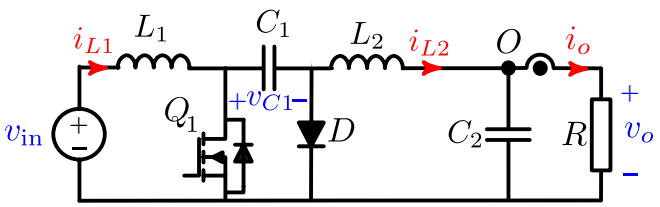


Figure 3.20: Schematic of a Cuk Converter

3.5 Application of Proposed Controller in Other Converters

As an example of applying the proposed control concept to other converters, this section presents the formulation of the controller for the Cuk converter. In this section, just the final results and the final control law are presented. Fig. 3.20 presents the schematic of a Cuk converter.

Following the same methodology used to derive the controller for a buck converter operating in CCM, the control law for a Cuk converter operating in CCM is expressed as:

$$d = 1 - \sqrt{\begin{array}{l} 1 + \dfrac{v_o}{\hat{v_{C1}}} + \dfrac{-2L_2}{\hat{v_{C1}} T_s}\left(\hat{i_{L2}} - \dfrac{v_{o,ref}}{R_{cont}}\right) \\ + \dfrac{2L_2 k_p}{\hat{v_{C1}} T_s}(v_o - v_{o,ref}) + \dfrac{2L_2 k_i}{\hat{v_{C1}} T_s}\displaystyle\int (v_o - v_{o,ref})dt \end{array}}. \tag{3.44}$$

In (3.44), $\hat{v_{C1}}$ and $\hat{i_{L2}}$ are the values estimated by the observer, corresponding to v_{C1} and i_{L2}.

Case-Study 7: This case-study assumes a Cuk converter with $L_1 = L_2 = 4\mu$H and $C_1 = c_2 = 50\mu$F. The input voltage is 12V, the switching frequency is 200KHz, and $v_{o,ref} = 3.3$V. Also, for each inductor and capacitor, a 5mΩ equivalent series resistance (ESR) is assumed. If the load current increases from 1.7A to 5A at $t = 0.01$s and the proposed controller is applied to the converter, the output voltage waveform will be as shown in Fig. 3.21. As this figure illustrates, the recovery time of the output voltage is equal to 2 switching cycles and the undershoot level is 0.12V. This verifies the effectiveness of applying the proposed controller to the Cuk converter. In the next section, simulation results are provided.

3.6 Formulation of a Generalized Version of Proposed Controller for Other load Types

So far throughout this chapter, resistive loads have been assumed for DC-DC converters. However, DC-DC converters may supply power to other passive or active load types, such as secondary DC-DC converters or DC motors. Therefore, while maintaining the underlying control concept, it is important to modify the proposed controller to make it applicable to all load types.

It is worth mentioning that DC-DC converters used in the intermediate stage of

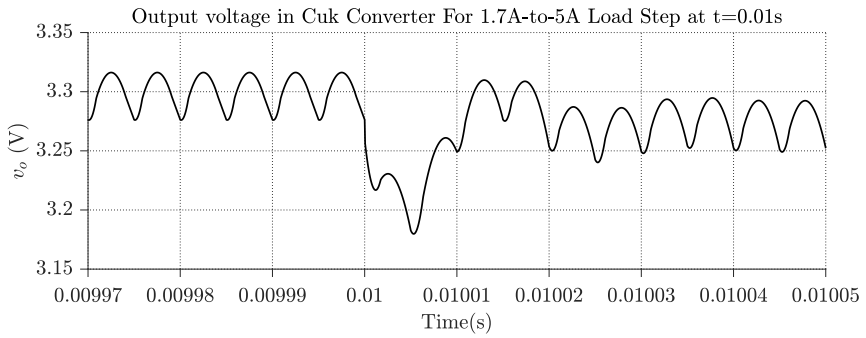


Figure 3.21: Load Transient Response of a Cuk Converter with the Proposed Controller for 1.7A-to-5A Load Step

a data center architecture supply power to several DC-DC converters connected to points of load. Load-connected DC-DC converters regulate voltage levels at their output terminals and based on these voltages and load types, a current passes through each load. Therefore, the amount of power consumed by each load is directly a function of the voltages at points of load and is changed in load steps. Therefore, the load seen from the output terminals of an intermediate stage DC-DC converter in a 12V data center power management system, can be modeled by a constant power load (CPL).

The buck converter model expressed by (3.5) is valid for resistive loads and its generalized version can be obtained by substituting the term $\frac{v_o(0)}{R}$ by $i_o(0)$. Therefore, the genralized buck converter model in CCM is derived as:

$$i_L(0) + \frac{-v_{in}T_s d^2 + 2v_{in}T_s d - v_o(0)T_s}{2L} = C\frac{v_o(T_s) - v_o(0)}{T_s} + i_o(0). \tag{3.45}$$

To eliminate the effect of i_o on v_o in (3.45) or equivalently, to extend the controller to all load types, the duty cycle d is selected such that:

$$\begin{aligned}\frac{-v_{in}T_s d^2 + 2v_{in}T_s d - v_o T_s}{2L} &= (-i_L + i_o) \\ &+ k_p(v_o - v_{o,ref}) \\ &+ k_i \int (v_o - v_{o,ref})dt.\end{aligned} \tag{3.46}$$

Similar to the case of resistive loads, i_L is estimated by an observer and the estimated inductor current is denoted by $\hat{i_L}$. Based in (3.46), the control law is expressed as:

$$d = 1 - \sqrt{\begin{aligned}&1 - \frac{v_o}{v_{in}} + \frac{2L}{v_{in}T_s}\left(\hat{i_L} - i_o\right) \\ &- \frac{2Lk_p}{v_{in}T_s}(v_o - v_{o,ref}) - \frac{2Lk_i}{v_{in}T_s}\int (v_o - v_{o,ref})dt\end{aligned}}. \tag{3.47}$$

The luenberger observer used to estimate the inductor current value can be derived using the same approach introduced in this chapter. The final observer is represented as:

$$\begin{aligned}\frac{d\hat{i_L}}{dt} &= -\frac{\hat{v_o}}{L} + \frac{v_{in}d}{L} + m_1(v_o - \hat{v_o}) \\ \frac{d\hat{v_o}}{dt} &= \frac{\hat{i_L}}{C} - \frac{i_o}{C} + m_2(v_o - \hat{v_o}).\end{aligned} \tag{3.48}$$

Case studies 8 and 9 investigate the performance of the proposed controller, when a buck converter supplies power to a constant power load (CPL). To derive the generalized controller in this section, the duty cycle was selected to induce an artificial i_o term in the left hand side of (3.45). This approach was taken to cancel out the $i_o(0)$ term in the right hand side of the same equation and decouple the v_o dynamics from the load type and current. However, the output current level used by the controller, i_{oc} is different with the actual output current i_o. This is because i_o is sensed by a bandwidth-limited sensor and later passes through zero-order hold and analog to digital converters to form i_{oc}. While case study 8 investigates the controller performance for the ideal case of $i_{oc} = i_o$, case study 9 presents controller performance for a system with bandwidth-limited current sensors and zero-order hold and quantization effects.

Case Study 8: A buck converter is assumed with an input voltage of 12V, a reference output voltage of 3.3V, $L = 30\mu$H, $C = 30\mu$H, and f_s =200KHz. At $t = 18$ms, the constant load power is changed from 40W to 20W. The effects of the zero-order hold and analog to digital converters, as well as the bandwidth of the output current sensors are ignored. The output voltage waveform is shown in Fig. 3.22. As this figure illustrates, the output voltage reaches the 1 percent band around $v_{o,ref} = 3.3V$ ithin 8 switching cycles. So, the recovery time is 8 cycles and the overshoot level is 0.1V.

Case Study 9: In this case study, the system parameters are the same as the previous one. However, the bandwidth of the output current filter is assumed to be 1KHz. Also, i_o passes through a zero-order hold block with a sampling frequency of 200KHz and is quantized through an analog to digital converter. The obtained signal i_{oc} is used by the controller later on. The constant load power is changed from 40W to 0W at $t = 18$ms. The transient response of the buck converter is shown in Fig. 3.23. As this figure shows, the filtered current value is different from the actual load current. However, the output voltage reaches the 1 percent band around 3.3V within 9 switching cycles. So, the recovery time is 9 cycles and the overshoot level is 0.22V.

3.6.1 Dynamical Analysis for CPL Loads at Different Output Current Filter Bandwidths

This subsection provides a dynamical analysis for the proposed controller applied to a buck converter feeding a CPL load. The effects of the zero-order hold and A/D blocks, as well as the output current filter bandwidth are considered in the analysis.

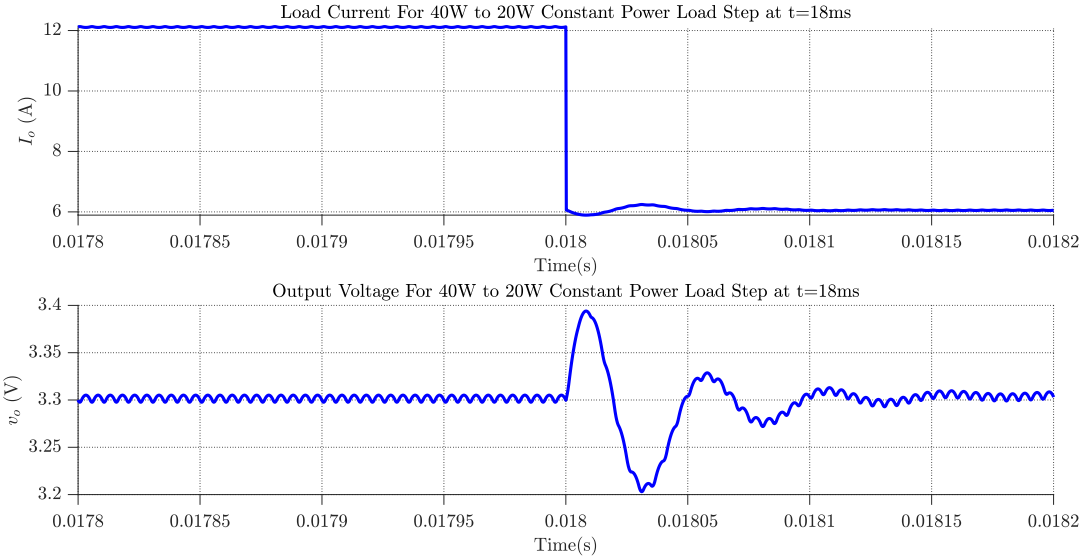


Figure 3.22: Load Transient Response of a Buck Converter Feeding a CPL with the Proposed Controller for 40W-to-20W Load Step in CCM

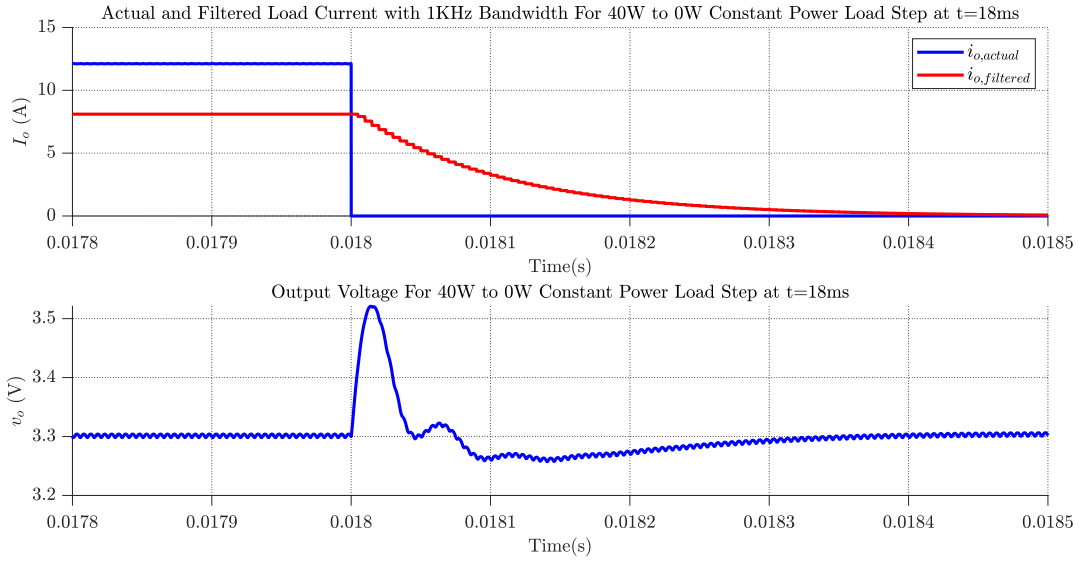


Figure 3.23: Load Transient Response of a Buck Converter Feeding a CPL with 1KHz current filter and ZOH blocks for a 40W-to-0W Load Step

It is assumed that the output current filter for the current sensor can be modeled by a first-order butterworth filter. In other words, the transfer function of the output current sensor filter is assumed as $\frac{1}{1+\alpha s}$, in which α is the reciprocal of the bandwidth in rad/s. According to [113], the overall effect of the zero-order hold and A/D blocks can be modeled by a time delay with the length T_d. In the Laplace domain, this time delay is modeled by $e^{-T_d s}$, which can be approximated by $\frac{1-\frac{T_d}{2}s}{1+\frac{T_d}{2}s}$ [113]. Therefore, the relationship between i_{oc} and i_o is expressed as:

$$I_{oc} = I_o \frac{1}{1+\alpha s} \frac{1-\frac{T_d}{2}s}{1+\frac{T_d}{2}s} = \frac{(2-T_d s)I_o}{\alpha T_d s^2 + (T_d+2\alpha)s + 2}. \tag{3.49}$$

Converting (3.49) into its equivalent differential equation in time domain leads to:

$$\alpha T_d \frac{d^2 i_{oc}}{dt^2} + (T_d + 2\alpha)\frac{di_{oc}}{dt} + 2i_{oc} = 2i_o - T_d \frac{di_o}{dt}. \tag{3.50}$$

To obtain the state-space representation of the system for a CPL load, new state variables $x_1 = i_{oc}, x_2 = \frac{di_{oc}}{dt}, x_3 = i_o$ are defined based on (3.50). If the power level of the CPL load is denoted by P^*, then $v_o i_o = P^*$. As P^* is constant for a CPL load, $\frac{dP^*}{dt} = 0$. This yeilds $\frac{dv_o}{dt} i_o + \frac{di_o}{dt} v_o = 0$. Therefore, the relationship between v_o and i_o for a CPL load can be expressed by:

$$\frac{di_o}{dt} = \frac{-i_o}{v_o}\frac{dv_o}{dt} = \frac{-i_L i_o + {i_o}^2}{C v_o}. \tag{3.51}$$

Following the same methodologies used before in this chapter and by using the equations in this section, the state space representation of the system is obtained as (3.52).

In the next case study, this state space representation in linearized around the equilibrium point of the system and the system poles are plotted in a root locus diagram. It is shown that the real values of the system poles are approximately independent from the output current filter bandwidth, ensuring fast system dynamics at even low sensor bandwidth levels.

$$\begin{aligned}
&\frac{di_L}{dt} = -\frac{v_o}{L} + \frac{v_{in}}{L}\left[1 - \sqrt{\begin{array}{l}1 - \frac{v_o}{v_{in}} + \frac{2L_f}{v_{in}T_s}\left(\hat{i_L} - x_1\right) \\ - \frac{2L_f k_p}{v_{in}T_s}(v_o - v_{o,ref}) - \frac{2L_f k_i}{v_{in}T_s} f\end{array}}\right] \\
&\frac{dv_o}{dt} = \frac{i_L}{C} - \frac{x_3}{C} \\
&\frac{d\hat{i_L}}{dt} = -\frac{\hat{v_o}}{L_f} + \frac{v_{in}}{L_f}\left[1 - \sqrt{\begin{array}{l}1 - \frac{v_o}{v_{in}} + \frac{2L_f}{v_{in}T_s}\left(\hat{i_L} - x_1\right) \\ - \frac{2L_f k_p}{v_{in}T_s}(v_o - v_{o,ref}) - \frac{2L_f k_i}{v_{in}T_s} f\end{array}}\right] \\
&+ m_1(v_o - \hat{v_o}) \\
&\frac{d\hat{v_o}}{dt} = \frac{\hat{i_L}}{C_f} - \frac{x_1}{C_f} + m_2(v_o - \hat{v_o}) \\
&\frac{df}{dt} = v_o - v_{o,ref} \\
&\frac{dx_1}{dt} = x_2 \\
&\frac{dx_2}{dt} = \frac{(-T_d - 2\alpha)x_2 - 2x_1 + 2x_3 + \frac{T_d i_L x_3}{C v_o} - \frac{T_d {x_3}^2}{C v_o}}{\alpha T_d} \\
&\frac{dx_3}{dt} = \frac{-i_L x_3 + {x_3}^2}{C v_o}.
\end{aligned} \tag{3.52}$$

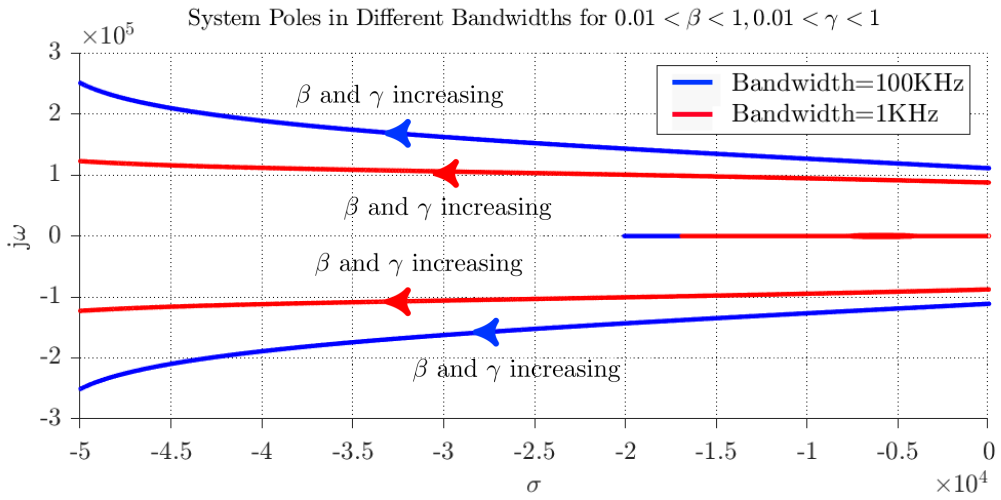


Figure 3.24: Root Locus Diagram for Case Study 10

Case Study 10: A buck converter feeding a CPL load is assumed with v_{in} =12V, $v_{o,ref}$ =3.3V, f_s =200KHz, P^* =40W, L = 30μH, and C = 30μF. By linearizing (3.14) around the equilibrium point of the system, the root locus diagram shown in Fig. 3.24 is obtained. This figure shows the root locus diagrams for the output current sensor filters with 1KHz and 100KHz bandwidth. As illustrated by Fig. 3.24, the real values of the poles are approximately imilar for different bandwidth levels. This verifies that the output current sensor filter do not make a noticeable impact on system dynamical speed. To obtain this figure, it is assumed that $T_d = 2T_s$. Also, $k_p = \frac{-\beta-\gamma}{CT_s}$ and $k_i = -\frac{\alpha\beta C}{4{T_s}^2}$. To obtain the root locus diagram at every point, it is assumed that $\beta = \gamma$ and the system poles are designed at $\frac{-\alpha T_s}{2}$ and $\frac{-\beta T_s}{2}$.

Case Study 11: This case study investigates the behavior of the proposed controller when the load is another closed-loop converter and therefore, has a negative input impedance. In this case study, a buck converter with parameters identical to [5] is assumed. The parameters of this buck converter are already provided in Table 3.4. This buck converter acts as the main buck converter numbered as converter 1, and is feeding another buck converter numbered as 2. The main buck converter is controlled by the proposed controller in this chapter and the second buck converter has an input voltage of 10V, a reference output voltage of 3.3V, a switching frequency of 2MHz, an inductor of 50μH, and a capacitor of 30μF. The second buck converter feeds a resistive load and experiences a load step current from 6A to 10A. A PI controller is applied to buck converter 2, with kp=0.1, ki=100. This controller is intentionally designed to have slow dynamics with considerable undershoot level, such that the performance of the main controller in presence of major negative load impedance can be assessed. Fig. 3.25 shows the waveforms associated with the main buck converter 1 and buck converter 2. As this figure shows, the output voltage waveform of main buck converter has an overshoot level of 0.06V, that is below 1 percent of 10V i.e. the nominal voltage. Therefore, the recovery time can be ignored.

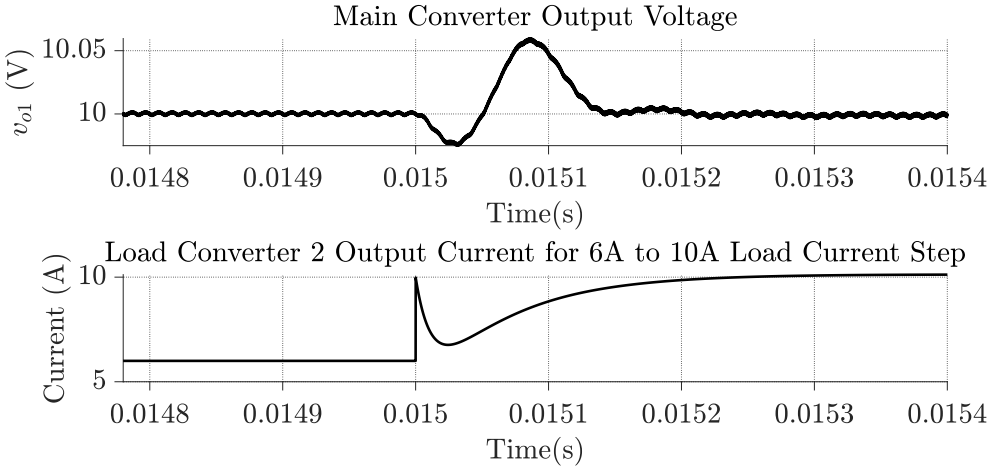


Figure 3.25: Load Transient Response of the System Composed of Two Buck Converters in Case Study 11

This is while the output current of converter 2 reaches its steady-state value slowly and this only has minimal impact on the main converter output voltage. Therefore, the modofied proposed controller is able to deal with the negative input impedance of the next power stage.

3.7 Simulation Results

This section provides simulation scenarios to validate the controller's performance.

Scenario 1: A buck converter operating in CCM is assumed with v_{in} =12V, $v_{o,erf}$ =3.3V, L =6μH, C = 30μF, and f_s =200KHz. Using the proposed controller, if the load current increases from 1.7A to 5A, the inductor current, load current, and the output voltage waveforms are as shown in Fig. 3.26. As this figure illustrates, the undershoot level for the output voltage is 0.18V. Assuming that the output voltage is recovered from a transient state once $|v_o - v_{o,ref}| < 0.02v_{o,ref}$, the recovery time associated with the output voltage is equal to 8 switching cycles.

Scenario 2: A buck converter operating in DCM is assumed with v_{in}=12V, $v_{o,ref}$=3.3V, L=500nH, C=600μF, and f_s=200KHz. The inductor has an equivalent series resistance (ESR) of 1.15mΩ and the capacitor has an ESR of 0.01Ω. Also, the capacitor has an equivalent series inductance (ESL) of 2.5nH. Moreover, the diode has a forward voltage of 0.27V and a conducting resistance of 6mΩ. The MOSFET has a drain-to-source resistance of 1.9mΩ. Fig. 3.27 shows the transient response in a 10A-to-1A load step. As Fig. 3.27 shows, the output voltage recovers in 7 switching cycles and the overshoot level is 0.11V. The recovery time is measured based on the number of switching cycles it takes for the output voltage to enter the ripple band corresponding to the situation before the load step. Moreover, the overshoot level is defined based on the difference between the maximum output voltage within a typical switching cycle before the load step and the maximum voltage observed during the transient period.

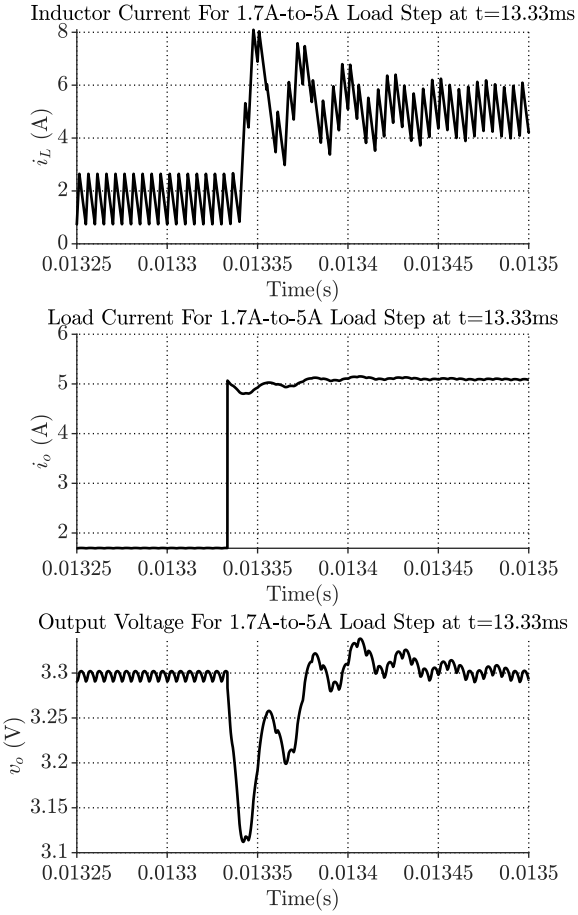


Figure 3.26: Load Transient Response of a Buck Converter with the Proposed Controller for 1.7A-to-5A Load Step in CCM

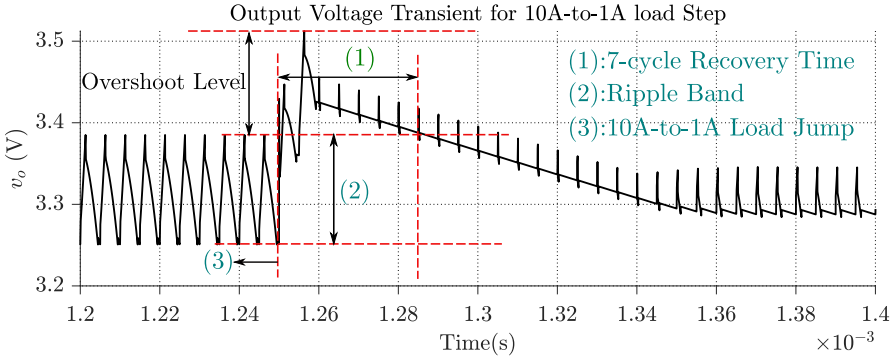


Figure 3.27: Load Transient Response of Buck Converter Using the Proposed Controller in a 10A-to-1A Load Jump

Scenario3: In this scenario, a buck converter with the same parameters as in scenario 2 is assumed. In this part, the controller is designed to achieve na phase margin of 60 degrees, to eliminate oscillations in the output voltage. For a single load step from 5.1A to 1.65A, the system response is as shown in Fig. 3.28. Moreover,

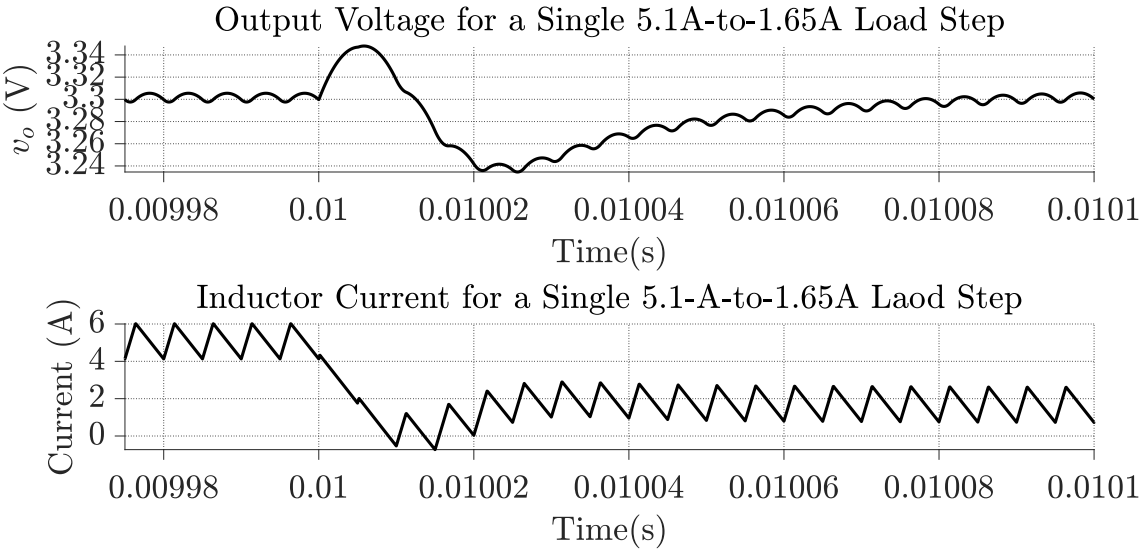


Figure 3.28: Load Transient Response of Buck Converter Using the Proposed Controller in a 5.1A-to-1.65A Load Jump

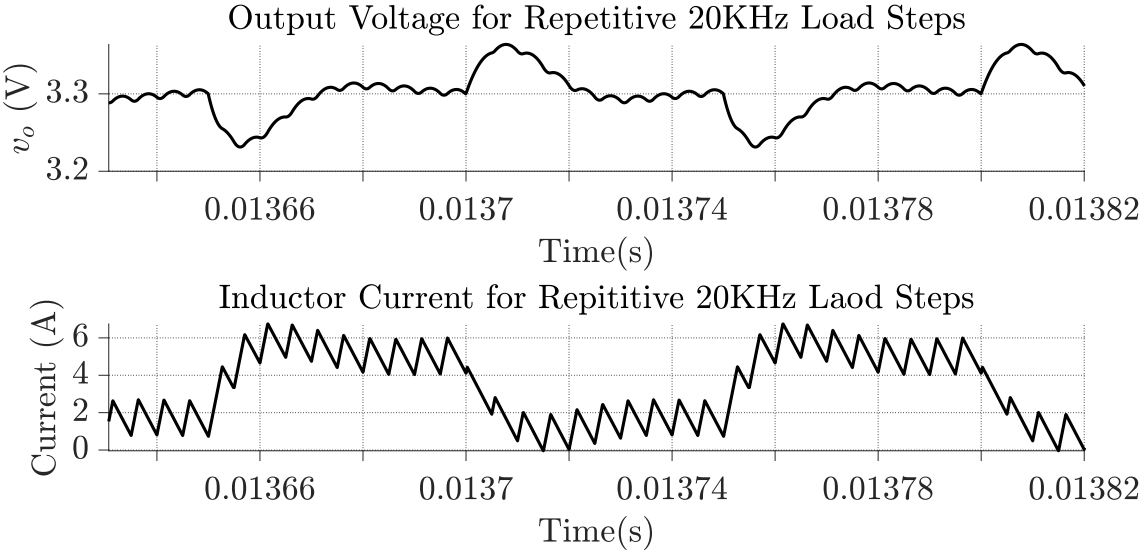


Figure 3.29: Load Transient Response of Buck Converter Using the Proposed Controller in 20KHz Repetitive Load Jumps

for repetitive load steps with frequencies of 20KHz and 2KHz, the output voltage and inductor current waveforms are shown in Fig. 3.29, Fig. **??**, respectively.

Scenario 4: This simulation scenario investigates the proposed controller behavior in buck converter transitions between CCM and DCM modes. The proposed controller for CCM buck converter is applied to a hybrid CCM/DCM buck converter with same parameters and it is figured out that the controller proposed in CCM can indeed be applied to a hybrid CCM/DCM buck converter as well. Although the observer model developed for CCM predicts false values for inductor current in DCM nonsynchronous buck converter, the simulation results show that the observer model

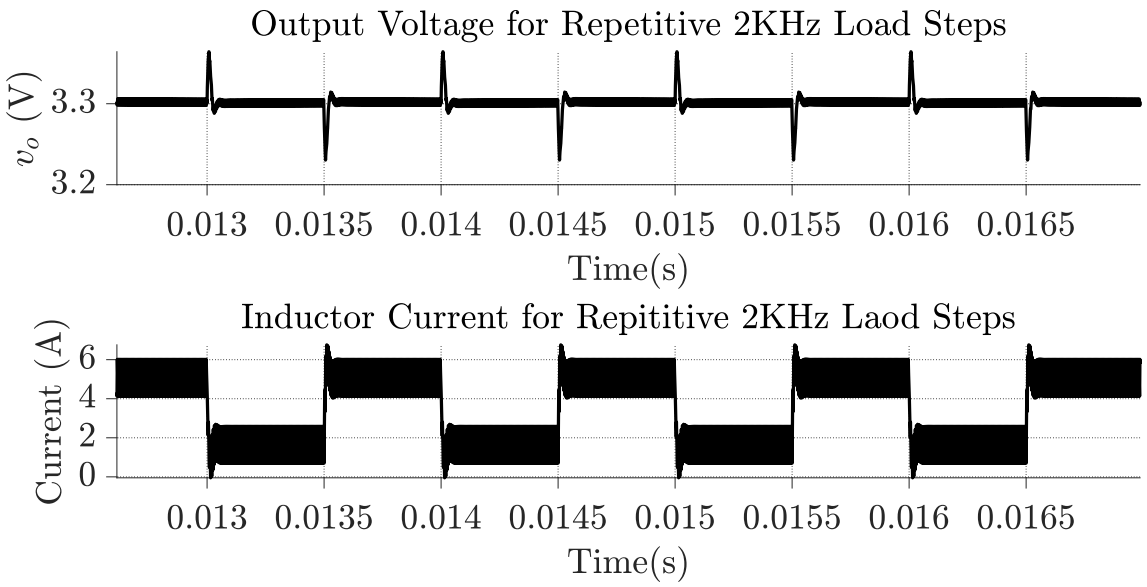


Figure 3.30: Load Transient Response of Buck Converter Using the Proposed Controller in 2KHz Repetitive Load Jumps

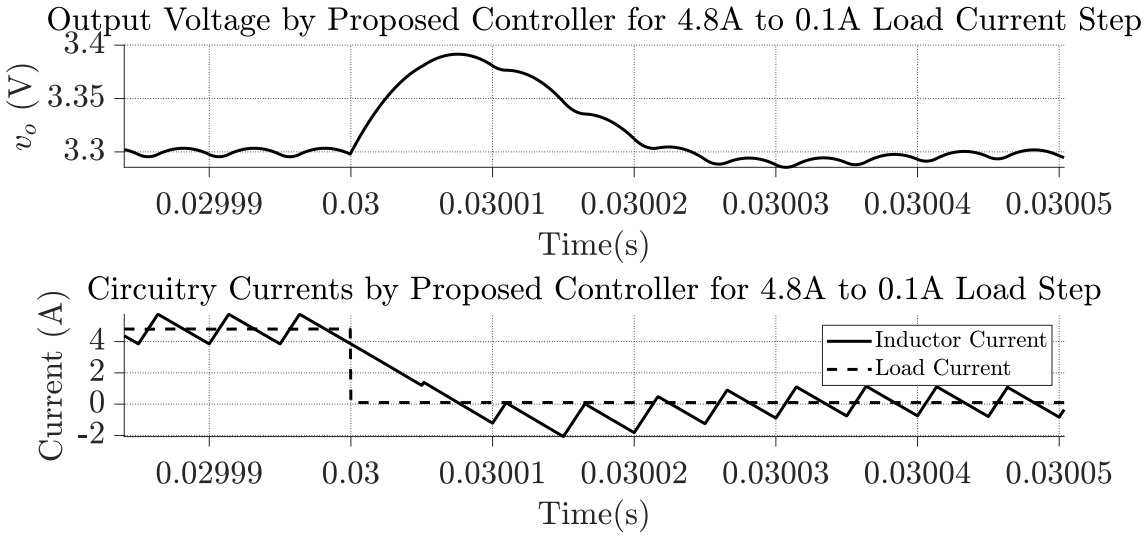


Figure 3.31: Controller Response for CCM to DCM Transition in Synchronous buck Converters

used for CCM can provide voltage regulation and fast transient response and the observer structure does not need to be updated. For a 12V/3.3V synchronous buck converter with load current step from 4.8A (CCM) to 0.1A (DCM), the controller response is shown in Fig. 3.31. According to this figure, the recovery time is 8 switching cycle and the overshoot level is 80mV.

For a 12V/3.3V nonsynchronous buck converter with load current step from 4.8A (CCM) to 0.1A (DCM), the controller response is shown in Fig. 3.32. According to this figure, the recovery time is 28 switching cycle and the overshoot level is 80mV. As it is observed, the estimated inductor current considerably differs from the actual

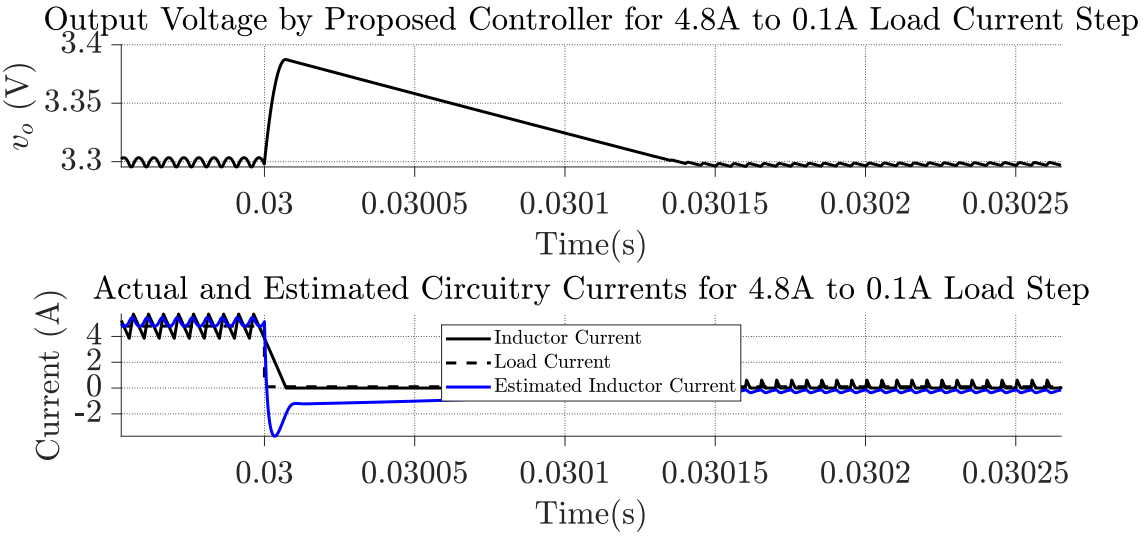


Figure 3.32: Controller Response for CCM to DCM Transition in Nonsynchronous buck Converter

inductor current level. This is because the CCM observer is applied to estimate the inductor current in both CCM and DCM modes. However, the proposed controller can still provide low overshoot levels with suitable recovery times. Of course, to further reduce recovery times, larger controller gains can be used in this case.

3.8 Experimental Results

This section provides experimental results to validate the effectiveness of the proposed controller. Two buck converters operating in CCM and DCM modes were implemented. For the buck converter operating in CCM, $v_{in} = 12V, v_{o,ref} = 3.3V, f_s = 200KHz, L = 6\mu$H and $C = 30\mu$F. For DCM operating mode, the buck converter parameters include $v_{in} = 12V, v_{o,ref} = 3.3V, f_s = 200KHz, L = 1.3\mu$H and $C = 150\mu$F. The proposed control algorithm was implemented using a TI TMS320F28335 DSP with 12-bit Analog-to-Digital converters. For a 1.7A to 5.25A load step in CCM operating mode, the corresponding waveforms for inductor current, load current, and output voltage are shown in Fig. 3.33. As this figure illustrates, the recovery time for the output voltage is equal to 10 switching cycles and the undershoot level is 0.2V. This figure shows load transient responses similar to Fig. 3.26 in Scenario 1 in Simulation Results section.

For a 5A to 1.7A load step in CCM operating mode, the corresponding waveforms for inductor current, load current, and output voltage are shown in Fig. 3.34. As this figure illustrates, the recovery time for the output voltage is equal to 5 switching cycles and the overshoot level is 0.3V.

For a 1.6A to 5.1A load step in DCM operating mode, the corresponding waveforms for inductor current, load current, and output voltage are shown in Fig. 3.35. As Fig. 3.35 illustrates, the output voltage recovery time is 5 switching cycles and the undershoot level is 0.12V. This figure is similar to Fig. 3.16 in terms of the

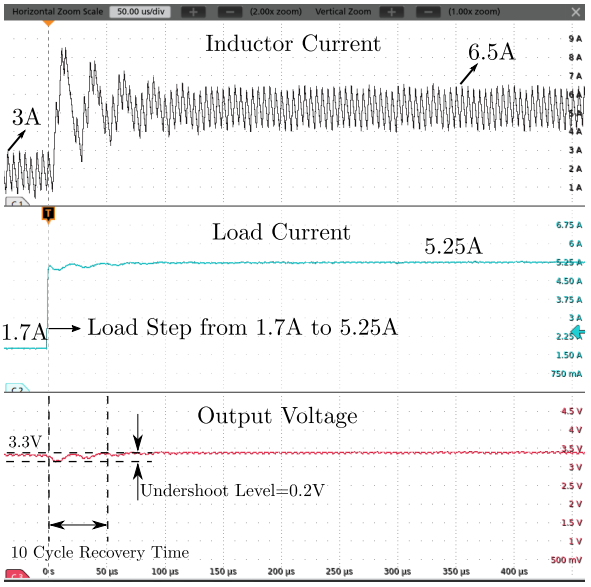


Figure 3.33: Inductor Current, Load Current, and Output Voltage Waveforms for 1.7A-to-5.25A Load Current Step

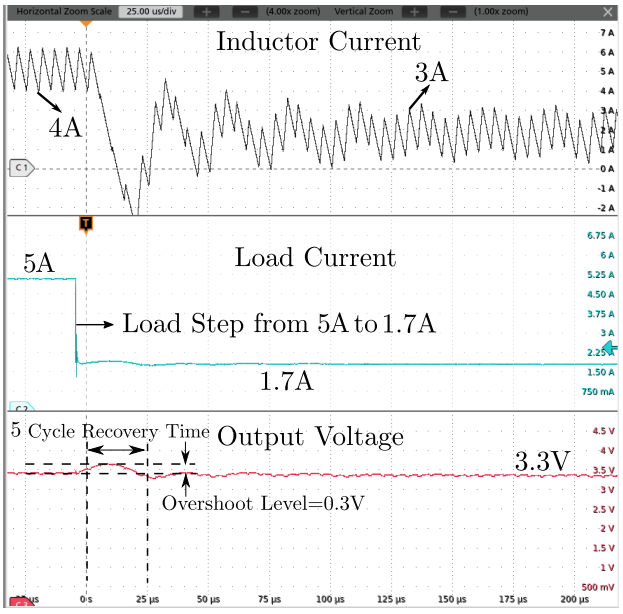


Figure 3.34: Inductor Current, Load Current, and Output Voltage Waveforms for 5A-to-1.7A Load Current Step

system's dynamic speed and the fact that in both figures, the output voltage starts to recover two cycles after the load step. In conclusion, Fig. 3.16 shows an enhanced load transient response. Finally, the waveforms for a load step from 5.1A to 1.8A in DCM mode are shown in Fig. 3.36. According to Fig. 3.36, overshoot level and recovery time are equal to 0.15V and 7 switching cycles, respectively and the dynamic profile of the output voltage is similar to Fig. 3.27. As it can be observed, the converter dynamics is enhanced for the load step shown in this figure. Fig. 3.37

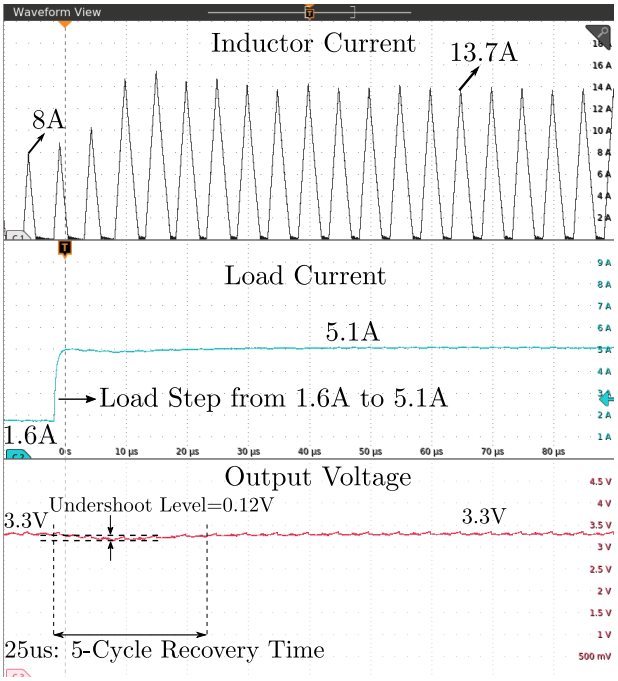


Figure 3.35: From Top to Bottom: Inductor Current, Load Current, and Output Voltage Waveforms for a 1.6A-to-5.1A Load Step

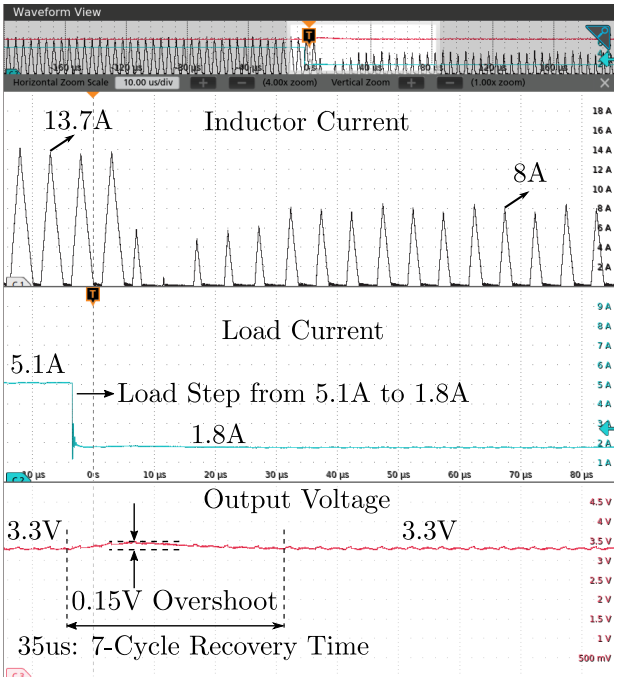


Figure 3.36: From Top to Bottom: Inductor Current, Load Current, and Output Voltage Waveforms for a 5.1A-to-1.8A Load Step

shows the converter's waveforms for the case in which the output voltage reference is changed from 3.3V to 2.3V in DCM mode. As it can be observed, the output voltage has successfully tracked its reference value.

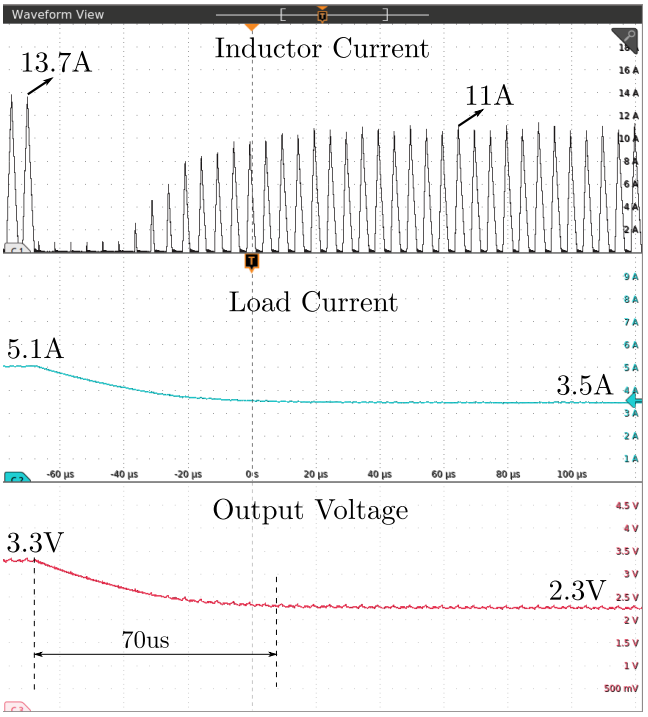


Figure 3.37: From Top to Bottom: Inductor Current, Load Current, and Output Voltage Waveforms for a 3.3V-to-2.3V Change in the Reference Value of the Output Voltage

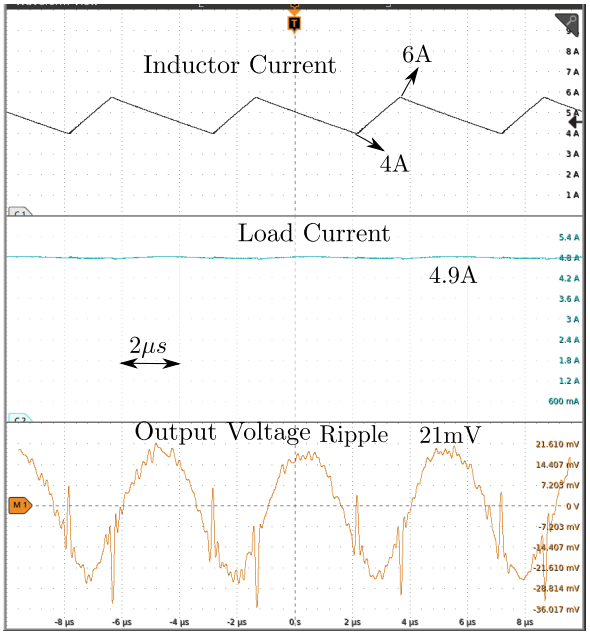


Figure 3.38: From Top to Bottom: Inductor Current, Load Current, and Output Voltage Ripple Waveforms in Steady-state for CCM

Fig. 3.38 and Fig. 3.39 show buck converter waveforms in at steady-state, in CCM and DCM modes, respectively.

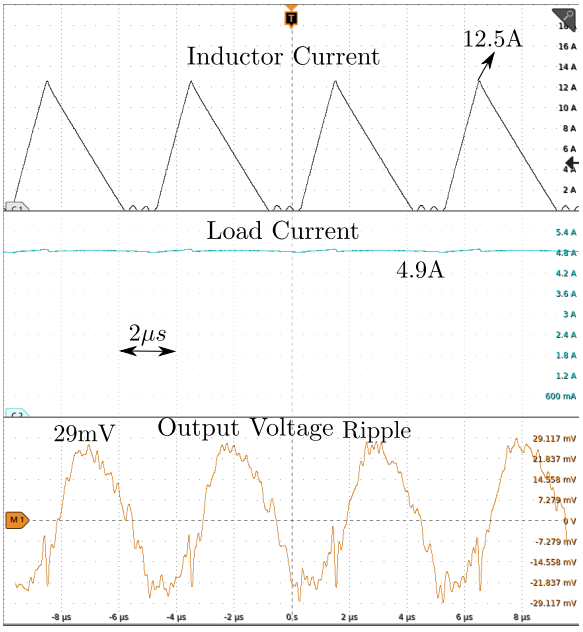


Figure 3.39: From Top to Bottom: Inductor Current, Load Current, and Output Voltage Ripple Waveforms in Steady-state for DCM

3.9 Comparison Results

3.9.1 Comparison with Existing Methods in the Literature

This subsection provides comparison tables to compare the peformance of the proposed controller with other existing methods. A separate comparison table is provided for each comparison case. In each table, identical converter parameters are assumed for the two methods compared. Table 3.1 compares the proposed control method's performance with [2]. In [2], a high-performance controller is proposed to enhance load step dynamics of a buck converter. However, it is demonstrated that for obtaining acceptable load transient responses and further dynamical response improvements, it is necessary to use auxiliry circuits in the mean time [2]. Table 3.1 proposes comparison results in two cases of the auxiliary ciruit enabled and disabled.

As table 3.1 shows, the recovery times as well as inductor current and outpu voltage overshoot/undershoot levels are smaller in the proposed controller, compared with the method used in [2] with auxiliary circuit disabled i.e. third column of the table. Moreover, the inductor current overshoot/undershoot levels obtained by the proposed controller are considerably smaller than [2] with auxiliary circuits, while approximately achieving similar dynamical performances. This considerably reduces the inductor current ratings in the converter. Also, the second column in Table 3.1 corresponds to two auxiliary switching during transients and two auxiliary components. However, the proposed method does not use swtiching frequencies higher than the steady-state switching frequency during transients and does not use any auxiliary devices in the meantime. A sample controller performance for a 11.3A-to-1.3A corresponding to Table 3.1 is obtained using computer simulations,

Table 3.1: Comparison of the Proposed Controller with [2]

References	Proposed	[2] w. Auxiliary	[2] w.o Auxiliary
Input Voltage v_{in} (V)	12	12	12
Output Voltage v_o (V)	3.3	3.3	3.3
Switching Frequency in Overshoot/Undershoot Transient $f_{s,transient}$ (KHz)	100/100	120/200	100/100
Switching Frequency at Steady-State $f_{s,steadystate}$ (KHz)	100	100	100
Inductor Size (μH)	8.5	12.85	12.85
Capacitor Size (μF)	300	200	200
Max. Load Current $i_{o,max}$ (A)	11.3	11.3	11.3
Load Current Step Magnitude ΔI_o (A)	10	10	10
Number of Auxiliary Switchings in Overshoot/Undershoot Transients	**0/0**	**2/2**	**0/0**
Output Voltage Overshoot/Undershoot v_{ov}, v_{un} (V)	0.32,0.2	0.32,0.13	0.81,0.32
Number of Transient Cycles during Overshoot/Undershoot Recovery Time ($t_r \times f_{s,transient}$)	4.7,3	4.15,3.56	8.1,4.15
Peak-to-Peak Output Voltage Ripple (V)	0.012	0.012	0.012
Inductor Current Undershoot/Overshoot(A)	**4.3,3.4**	**9,10**	**7.5,4.2**
No. of Aux. Components	**0**	**2**	**0**

which is presented in Fig. refcomp1fig. As this figure shows, the proposed controller has provided a fast load transient response with low overshoot level.

Table 3.2 compares the performance of the proposed controller with [3].

As table. 3.2 illustrates, the proposed conroller has provided smaller overshoot and recovery time levels compared with [3]. The system response obtained using the proposed controller is shown in Fig. 3.41.

Table 3.3 compares the performance of the proposed controller with the method presented in [4]. As this table illustrates, overshoot/undershoot levels and recovery times obtained using the proposed controller are lower than [4]. Fig. 3.42 shows the converter waveforms corresponding to the proposed controller applied to the buck converter with parameters reflected in table 3.3.

Table 3.4 compares the performance of the proposed controller with the method presented in [5]. As it can be seen, the undershoot level and revoery time using the proposed controller is less than in [5]. The system response waveforms using the proposed controller are shown in Fig. 3.43.

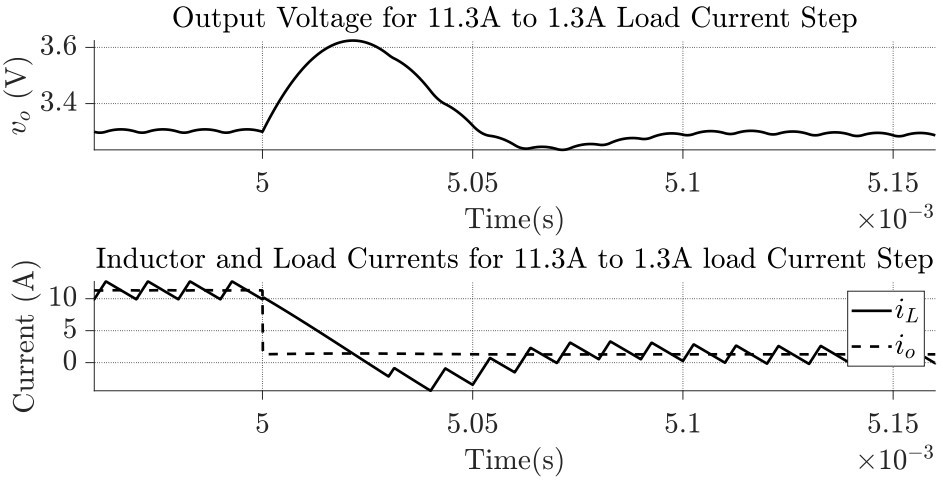


Figure 3.40: Proposed Controller Performance in 11.3A to 1.3A Load Step for Comparison with [2]

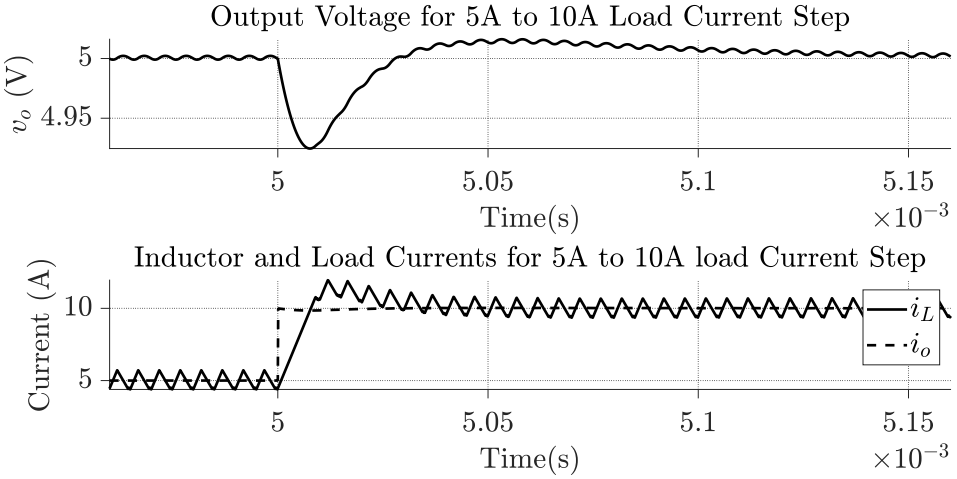


Figure 3.41: Proposed Controller Performance in 5A to 10A Load Step for Comparison with [3]

3.9.2 Comparison with Traditional Controllers

In this subsection, the performance of the proposed controller is compared with two traditional controllers, including PI and model-predictive (MPC) controllers. The notations used in this part are the same as those used in previous sections to denote time-domain small-signal variations and Laplace domain signals. In the first step, a closed-loop buck converter with PI controller is analyzed and the system poles are derived. The results will be used in the next step to design the best PI controller with smallest overshoot levels and recovery times. For this purpose, the buck converter which operates is CCM and is shown in Fig. 3.7, is considered. In this converter, writing KVL and linearizing the resultant equation around the oprating point lead to:

$$v_{in}\tilde{d} - \tilde{v_o} = L\tilde{i_L}. \tag{3.53}$$

Table 3.2: Comparison of the Proposed Controller with [3]

References	Proposed	[3] w. Auxiliary	[3] w.o Auxiliary
Input Voltage v_{in} (V)	12	12	12
Output Voltage v_o (V)	5	5	5
Switching Frequency in Overshoot/Undershoot Transient $f_{s,transient}$ (KHz)	200/200	200/200	200/200
Switching Frequency at Steady-State $f_{s,steadystate}$ (KHz)	200	200	200
Inductor Size (μH)	10	10	10
Capacitor Size (μF)	280	280	280
Max. Load Current $i_{o,max}$ (A)	10	10	10
Load Current Step Magnitude ΔI_o (A)	5	5	5
Number of Auxiliary Switchings in Overshoot/Undershoot Transients	**0/0**	**2/2**	**0/0**
Output Voltage Undershoot v_{un} (V)	0.08	0.2	0.36
Number of Transient Cycles during Undershoot Recovery Time ($t_r \times f_{s,transient}$)	3.8	3.8	7.6
Peak-to-Peak Output Voltage Ripple (mV)	3	3	3
Inductor Current Overshoot(A)	**1.25**	**N/A**	**N/A**
No. of Aux. Components	**0**	**6**	**0**

Writing KCL in node O in Fig. 3.7 and linearizing the resultant equation around the operating point leads to:

$$\tilde{i_L} = C\frac{d\tilde{v_o}}{dt} + \frac{\tilde{v_o}}{R^*} + \frac{-{v_o}^*}{{R^*}^2}\tilde{R}. \tag{3.54}$$

Also, the control law for a PI controller can be expressed as:

$$d = k_p(v_o - v_{o,ref}) + k_i \int (v_o - v_{o,ref})dt. \tag{3.55}$$

If (3.55) is linearized around the system operating point and the resultant small-signal equation is rewritten in the Laplace domain, the Laplace-domain small-signal control law is obtained as:

$$s\tilde{D} = (k_p s + k_i)(\tilde{V_o} - \tilde{V}_{o,ref}). \tag{3.56}$$

Table 3.3: Comparison of the Proposed Controller with [4]

References	Proposed	[4] w. Auxiliary
Input Voltage v_{in} (V)	15	15
Output Voltage v_o (V)	3.3	3.3
Switching Frequency in Undershoot Transient $f_{s,transient}$ (KHz)	200	400
Switching Frequency at Steady-State $f_{s,steadystate}$ (KHz)	200	200
Inductor Size (μH)	2	10
Capacitor Size (μF)	220	220
Max. Load Current $i_{o,max}$ (A)	15	15
Load Current Step Magnitude ΔI_o (A)	11	11
Number of Auxiliary Switchings in Undershoot Transients	**0**	**4**
Output Voltage Undershoot v_{un} (V)	0.04	0.064
Number of Transient Cycles during Undershoot Recovery Time ($t_r \times f_{s,transient}$)	1.5	6
Inductor Current Overshoot(A)	**1**	**8**
No. of Aux. Components	**0**	**3**

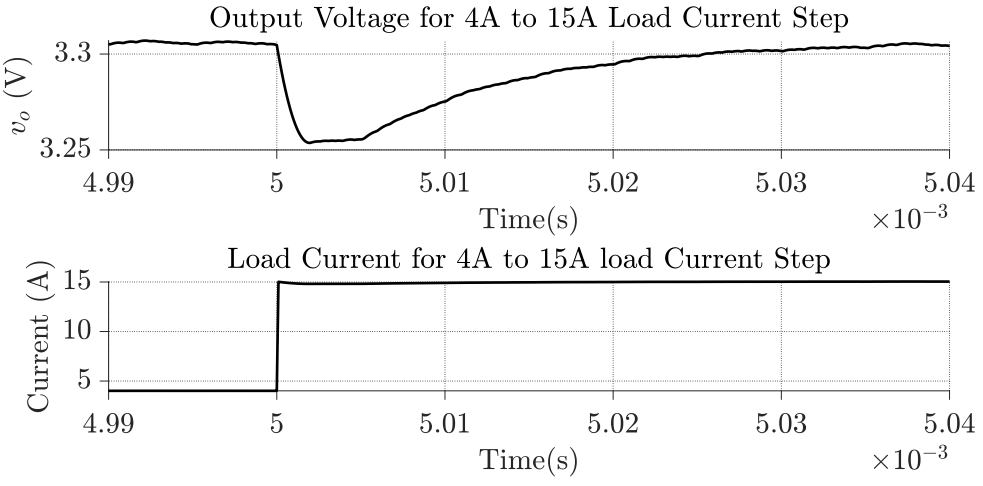


Figure 3.42: Proposed Controller Performance in 4A to 15A Load Step for Comparison with [4]

In this part, the goal is to investigate the load transient response of the buck

Table 3.4: Comparison of the Proposed Controller with [5]

References	Proposed	[5] w. Auxiliary	[5] w.o Auxiliary
Input Voltage v_{in} (V)	20	20	20
Output Voltage v_o (V)	10	10	10
Switching Frequency in Undershoot Transient $f_{s,transient}$ (KHz)	100/100	N/A	N/A
Switching Frequency at Steady-State $f_{s,steadystate}$ (KHz)	100	100	100
Inductor Size (μH)	46.85	46.85	46.85
Capacitor Size (μF)	300	300	300
Max. Load Current $i_{o,max}$ (A)	27	27	27
Load Current Step Magnitude ΔI_o (A)	21	21	21
Output Voltage Undershoot v_{un} (V)	2	3	3.5
Recovery Time t_r ms	0.22	0.42	0.47
No. of Aux. Components	**0**	**4**	**0**

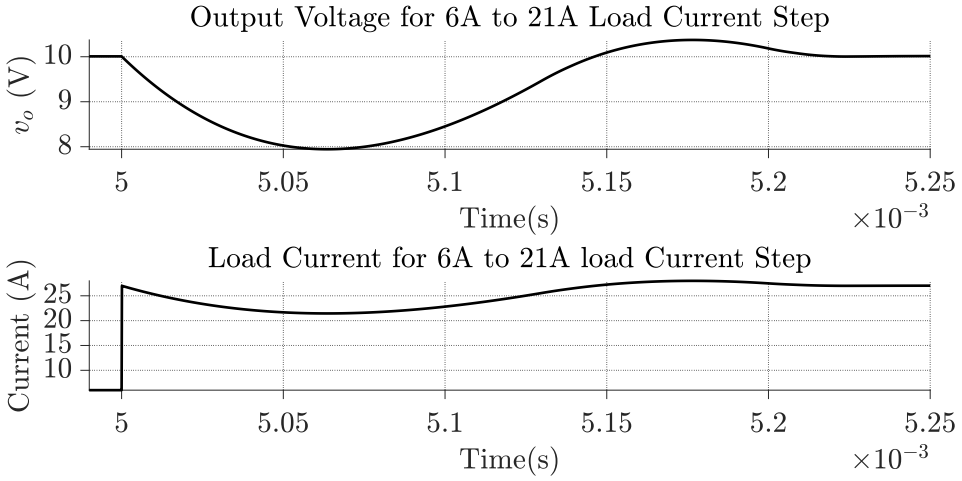


Figure 3.43: Proposed Controller Performance in 6A to 27A Load Step for Comparison with [5]

converter. Therefore, it is assumed that $\tilde{V}_{o,ref}(s) = 0$ and only the effect of $\tilde{R}(s)$ on $\tilde{V}_o(s)$ is investigated. Using this assumption, as well as rewriting (3.53) and (3.54) in the Laplace domain, along with (3.56) yield:

$$J(s) = \frac{\tilde{V}_o(s)}{\tilde{R}(s)} = \frac{L{v_o}^* s^2}{\begin{bmatrix} LCR^{*2}s^3 + LR^* s^2 \\ + (1 - v_{in}k_p)R^{*2}s - v_{in}k_i R^{*2} \end{bmatrix}}. \tag{3.57}$$

The demonator of J(s) in (3.57) is the characteristic polynimial of a closed-loop buck converter with PI controller. From control logic, it is evident that $k_i, k_p < 0$. By using Routh-Hurwitz stability critetion for the denominator of J(s), the stability

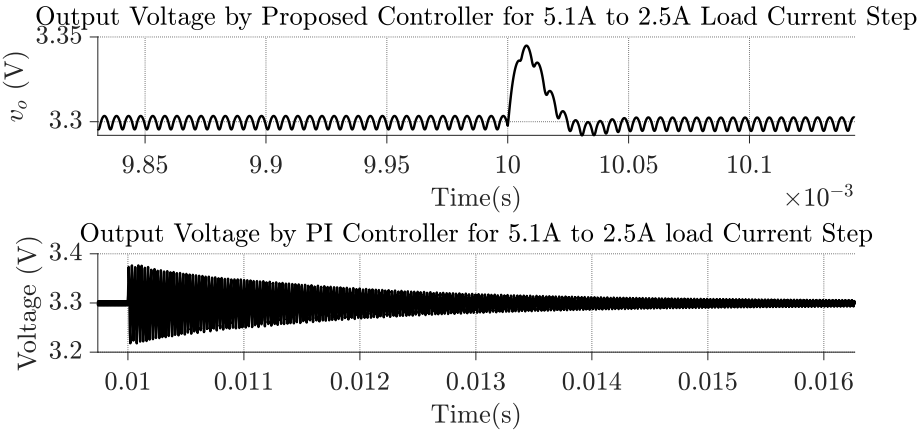


Figure 3.44: Proposed Controller and PI Controller Performances in 5.1A to 2.5A Load Step Presented for Comparison

criteion for the proposed controler is obtained as $k_i > \frac{v_{in}k_p - 1}{v_{in}CR^*_{max}}$, assuming $R^*_{min} < R^* < R^*_{max}$. Next, root locus analysis is required to design k_p and k_i values.

Case Study: A buck converter with parameters similar to Simulation Scenario 1 is assumed. The proposed controller in this chapter and the traditional PI controller are designed and applied to this system to compare their dynamic performances. The results are shown in Fig. 3.44, according to which the output voltage overshoot levels for the proposed controller and PI controller in a 5.1A to 2.5A load step are 45mV and 75mV, respectively. Also, the recovery times associated with the proposed controller and PI controller for the same load step are 0.05ms and 2ms, respectively. The PI controller is designed as $k_i = -6874$,$k_p = -4$ and the design is done based on the system poles derived from (3.57). Fig. 3.44 verifies the advantages of the proposed controller over PI controller, as a traditional and commonly-used control method.

3.9.3 Comparison with Load-side Current Feedforward Controllers

This subsection compares the performance of the proposed controller with methods using load-side current feedforward. The proposed controller is applied to the buck converter system with parameter values mentioned in [13]. These values include v_{in}=7V, $L = 1\mu H$, $C = 300\mu F$, v_o =1.3V, and f_s =780KHz. The system performance using the proposed controller for a 10A to 2.5A load step is shown in Fig. 3.45.

Fig. 3.45 shows that the output voltage overshoot level, recovery time, and inductor current undershoot level for the proposed controller are 60mV, 17.5μs, and 2.5A. According to the figures provided in [13], the associated values for the same parameters in [13] are 100mV, 20μs, and 5.5A [13]. Therefore, the comparison results show that the proposed controller performance is better compared with [13].

To compare the proposed controller performance with [14], the proposed controller is applied to a buck converter with an input voltage of 9V, an inductor of

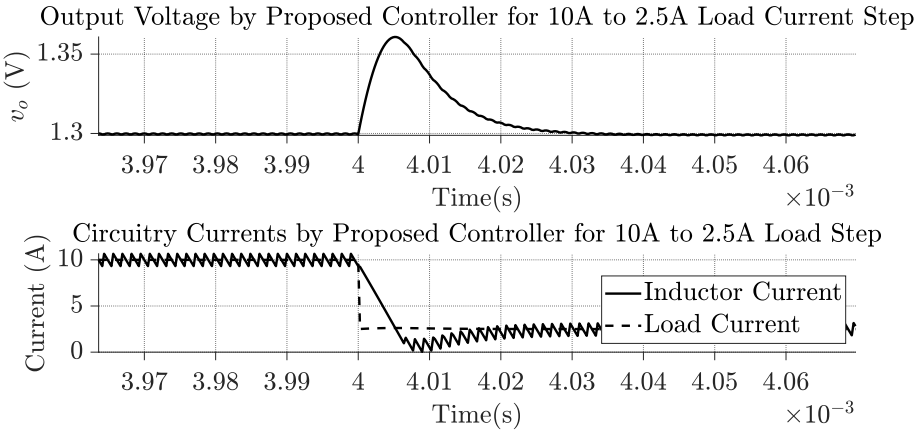


Figure 3.45: Proposed Controller Response to 10A to 2.5A Load Step for Comparison with [13]

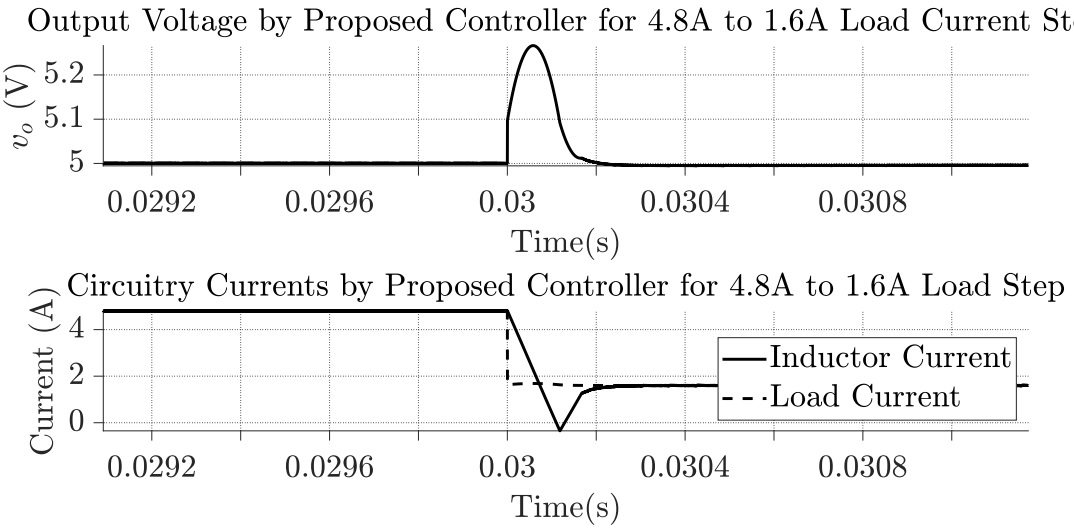


Figure 3.46: Proposed Controller Response to 4.8A to 1.6A Load Step for Comparison with [14]

120μH, a capacitor of 440μF, a switching frequency of 16.4kHz, and an output voltage of 5V. The system response using the proposed controller for a load step from 4.8A to 1.6A is shown in Fig. 3.46. The recovery time and overshoot levels obtained using the proposed controller are 0.26V and 0.2ms, which are lower than the values of 0.6V and 0.46ms obtained in [14]. It is worth mentioning that better transient response in comparison with [14] is obtained using a smaller-sized inductor (120μH), compared with the inductor size of 320μH in [14].

3.9.4 Comparison with Time Optimal Controllers

This subsection compares the performance of the proposed controller with a sample time optimal controller presented in [15]. The pcomparison is made, assuming a buck converter with an input voltage of 12V, an output voltage of 3.3V, an inductor

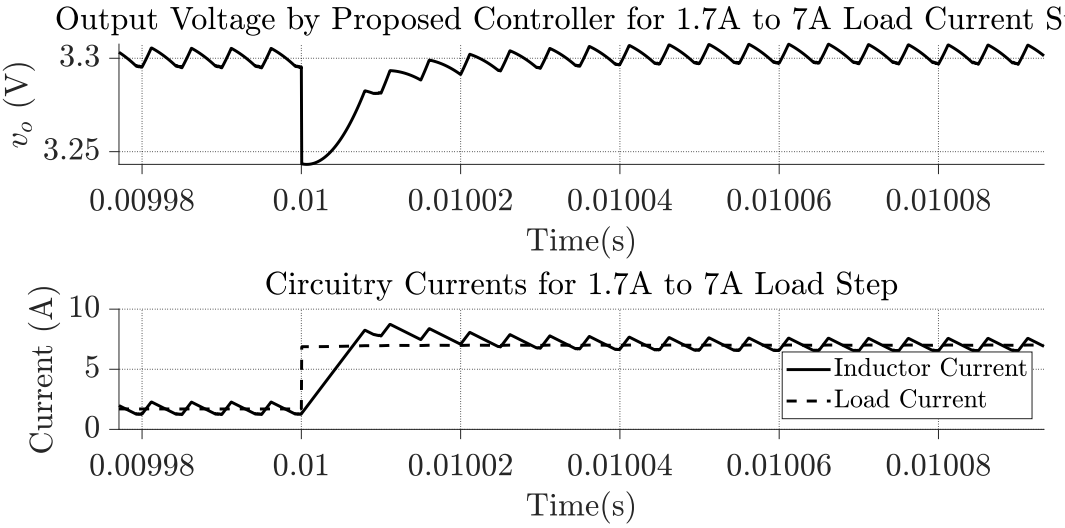


Figure 3.47: Controller Response for 1.7A to 7A load Step with the Same Capacitor Size in [15]

of 10μH with an ESR of 2.2mΩ, a capacitor of 570μF with an ESR of 10mΩ, and a switching frequency of 200KHz. [15] discusses a time-optimal buck converter controller based on a switching surface and capacitor current feedforward. Fig. 3.47 shows controller response for a 1.7A to 7A load step, when the proposed controller is applied to the buck converter with the same parameters (including same capacitor sizes) as in [15]. As Fig. 3.47 shows, the output voltage undershoot level is 0.06V, compared with 0.13V in 3.47. Also, the recovery time is 3 switching cycles, vs. the 5 switching cycle in 3.47.Therefore, the proposed controller has better performance with similar capacitor size compared with 3.47.

Fig. 3.48 on next page shows the proposed controller response, if the capacitor size used is half the capacitor size used in [15]. The recovery time and undershoot levels is the same as in [15]. However, these results have been obtained with half of the capacitor size used in [15].

3.9.5 Concept of Per-Unit Representation of Converters

This section proposes a per-unit representation of converters, which enables making accurate comparisons among the performances of different systems. Using this method, all of the converter parameters are converted to dimensionless scalars, which makes the input and output voltages and switching frequencies of different systems identical. This enables more accurate comparisons among different system performances. The per-unit representation of a buck converter operating in CCM is provided, which can be similarly extended to DCM. Considering Fig. 3.5, the CCM operating mode is assumed. A switching function $s(t)$ can be defined as 1 for $0 < t < dT_s$ and 0 for the rest of the cycle. Writing KVL in Fig. 3.5 results in:

$$L\frac{di_L}{dt} + v_o = v_{in}s(t). \tag{3.58}$$

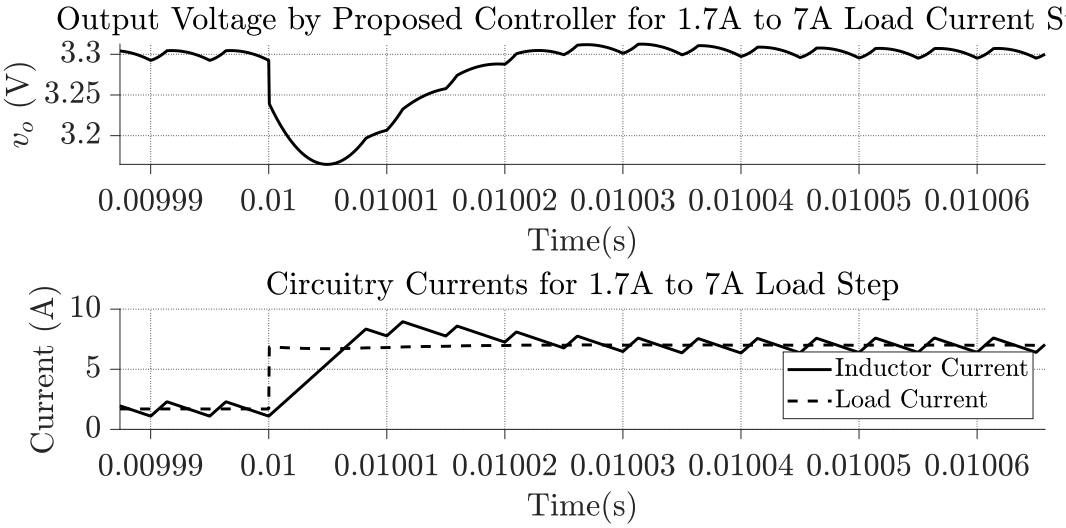


Figure 3.48: Controller Response for 1.7A to 7A load Step with the Half of the Capacitor Size in [15]

The next step is to select the base values for the voltages, currents, and time. The base voltage is denoted by v_g, and T_s is selected as the base time. The base current is selected as $i_{base} = \frac{P_{max}}{v_g}$, in which P_{max} is the maximum load power. The time t, the voltage v, and the current i, can be represented in the per-unit system by v_{pu}, t_{pu}, and i_{pu}, respectively. The relationships between these values can be expressed by $v = v_g v_{pu}$, $t = T_s t_{pu}$, and $i = i_{pu} i_{base}$. Using these definitions, (3.58) can be rewritten as follows:

$$\left(\frac{LP_{max}}{{v_g}^2 T_s}\right)\frac{di_{pu}}{dt_{pu}} + v_{opu} = v_{inpu}s(t). \tag{3.59}$$

By comparing (3.58) and (3.59), the per-unit inductance L_{pu} can be found as $L_{pu} = \frac{LP_{max}}{{v_g}^2 T_s}$. Following the same method for KCL in the output node of buck converter, the per-unit capacitance C_{pu} can be found as $C_{pu} = \frac{C{v_g}^2}{P_{max}T_s}$. It can be shown that for both DCM and CCM modes, the per-unit representation is the same.

3.9.6 Comparison Table

Using a Figure-of-Merit (FOM), Table 3.1 presents a comparison among the proposed controller and other existing methods. This FOM is defined as shown in the last table row and the definition relies on the fact that for the same load step magnitude and switching frequency, a better system performance is achieved when, (i) the overshoot/undershoot levels and recovery times are minimized (ii) less amount of total energy is stored in the converter. Table 3.1 presents comparison results for this work and [2, 3, 4, 5]. The parameter values are represented in the per-unit domain using the concept of per-unit representation of converters, introduced in the previous section. According to Table 3.1, the proposed controller in which no auxiliary component is used, has a higher FOM compared with the cases in

Table 3.5: Comparison of the proposed controller and other controllers using per-unit parameter values

References	Proposed (DCM)	Proposed (CCM)	[2]	[3]	[4]	[5]
Input Voltage v_{in} (p.u.)	1	1	1	1	1	1
Output Voltage v_o (p.u.)	0.275	0.275	0.275	0.41	0.22	0.5
Max. Switching Frequency $f_{s,max}$ (p.u.)	1	1	1	1	1	1
Inductor Energy, and Size (p.u.)	0.2,0.03	0.92,0.14	29,4.4	11.5,4	94,9.1	63,31.6
Capacitor Energy, and Size (p.u.)	9.7,256.7	1.94,51.3	0.2,5.8	2.3,28	0.2,9.7	5.5,44
Total Stored Energy E_{tot} (p.u.)	9.9	2.86	29.3	14	93.9	68.8
Switching Frequency f_s (p.u.)	1	1	1	1	1	1
Max. Load Current $i_{o,max}$ (p.u.)	3.6	3.6	3.6	2.4	4.5	2
Load Current Step ΔI_o (p.u.)	2.4	2.4	3.2	2.2	3.3	1.55
Overshoot Level v_{ov} (p.u.)	0.01	0.025	0.08	0.033	0.035	0.275
Undershoot Level v_{un} (p.u.)	0.01	0.016	0.03	0.02	0.025	0.175
Average Voltage Deviation Level $v_{dev,av}$ (p.u.)	0.01	0.02	0.055	0.026	0.03	0.225
Overshoot Recovery Time $t_{r,ov}$ (p.u.)	7	10	6.8	6.4	14	270
Undershoot Recovery Time $t_{r,un}$ (p.u.)	5	5	4.3	6.4	13.6	47
Average Recovery Time $t_{r,av}$ (p.u.)	6	7.5	5.55	6.4	13.8	158.5
No. of Aux. Components	0	0	0	0	0	0
FOM= $\frac{\Delta I_o}{E_{tot} f_s t_{r,av} v_{dev,av}}$	3.47	5.6	0.36	0.93	0.085	0.0006

which auxiliary components are disabled and only control systems are used. Also, the proposed controller has a higher FOM than methods which use controllers and auxiliary circuits simultaneously. Compared with these methods, the proposed controller benefits from using no auxiliary circuits, which reduces the system's cost and complexity. Moreover, the comparison table shows that the proposed controller has a higher FOM, when it is applied in CCM rather than DCM.

As a conclusion to this chapter, This chapter proposed a dynamic decoupling controller to enhance converter responses in applications with large load steps, such as data center applications. In a DC-DC converter, the load level affects the dynamics of the system and in large load steps, the system plant changes significantly, degrading system dynamics. To tackle this problem and improve system dynamics in load steps, the proposed controller reduces the impact of the load level on the dynamics of a closed-loop DC-DC converter. This is achieved by selecting a control law to make the differential equation of the closed-loop system almost independent

from the load level.

Without using any auxiliary components, the proposed controller reduces the system's cost and complexity, while reducing the total energy storage components in the system. The formulation of the controller is developed for Cuk and buck converters for various operating modes. Simulations and experimental results show that for a 2.4 p.u. load current step, the controller provides a 7-switching cycle recovery time and a 0.01-0.02 p.u. overshoot/undershoot level. Also, comparisons are made with other existing methods to show the effectiveness of the presented controller.

Chapter 4

New Decentralized Control Laws for Modular ISOP and IPOS DC-DC Converters with Bi-Directional Power Flow Capabilities

In previous chapters, the load-connected and intermediate power conversion stages of a data center power management system were investigated and control methods were proposed to tackle their associated challenges. This chapter focuses on stage 1 converters in data center power management systems. Stage 1 converters are characterizied by high input voltages and large load currents and therefore, they cannot be realized efficiently using a single converter. Alternatively, to process power in stage 1, multiple converter modules are connected in series or parallel in their input and output terminals. This way, each converter module only tansfers a fraction of total power and can be implemented using smaller-sized passive compoentns and lower switch ratings. Of course, modular DC-DC conversion systems introduce new challenges and requirements, including equal power sharing among modules, stability challenges, fast dynamics requirements, and fault-ride-thorugh capabilities.

This section proposes a new decentralized controller for ISOP/IPOS DC-DC converters in powr conversion stage 1 of a data center, which improves system performance in terms of dynamical response, power sharing among modules, and voltage/current regulation. The proposed method does not assume any system parameter values, does not need inter-modular communications, is applicable to all converter topologies, and does not use complicated nonlinear calculations. Also, the proposed control structure is simple and does not create trade offs between IVS and OVR. It should be mentioned that the controller's performance is not degraded by parameter mismatches among modules and the controller does not increase system cost, by avoiding additional hardware and measurement sensors. In this chapter, the controller's effectiveness is verified by simulation and experimental results and the performance is also compared with other existing methods, to demonstrate the

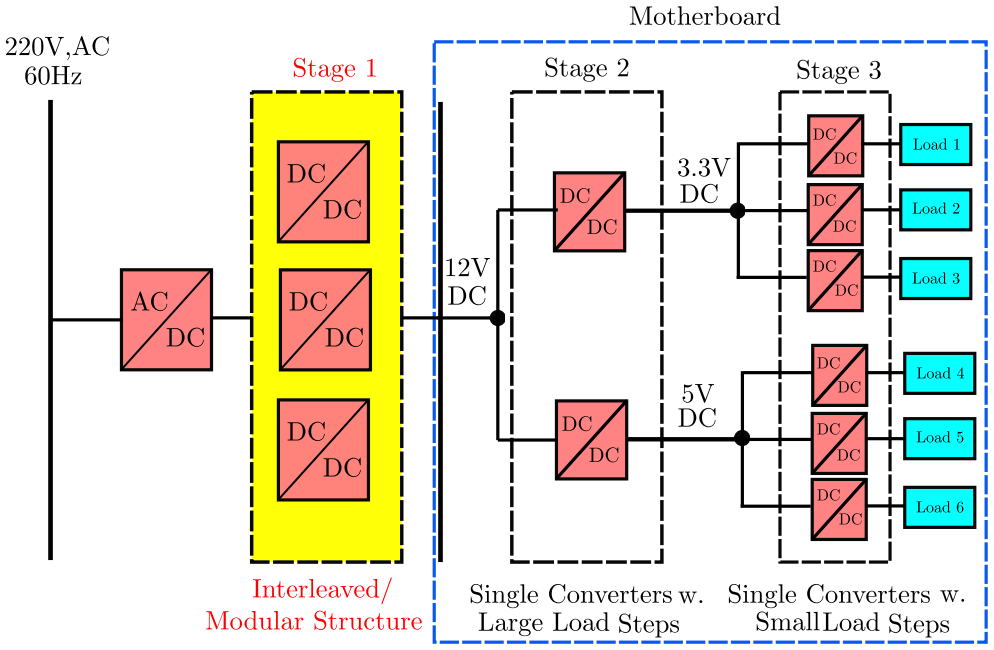


Figure 4.1: Modular DC-DC Conversion Stage i.e. Stage 1 Highlighted by Yellow in Data Center Power Management System

advantages of the proposed controller.

4.1 Chapter Challenges, Literature Review, and Contributions

4.1.1 Challenges

The architecture of the power management system of a data center is shown in Fig. 4.1, in which the modular DC-DC conversion stage i.e. stage 1 is highlighted by yellow color. As this figure illustrates, stage 1 is responsible to convert a 220V input DC voltage to a 12V output DC voltage. Therefore, the DC voltage gain of stage 1 converters need to be considerably large. At the same time, the total input voltage level i.e. 220V is high compared with ooutput voltage level. Moreover, the output 12V DC link must transfer power to a large number of various loads and converters. Therefore, the total transferred power and consequntly, electrical current flowing through this 12V DC link is considerably high in a data center. In conclusion, stage 1 converters need to process high input voltages and high outout currents and this requires implementation of the converter with large-sized passive components and high-rating switches. In this regard, large-sized passive elements are required to reach acceptable voltage and current ripples, and high-ratings switches are needed to avoid converter damage as a result of overvoltages or overcurrents. Using large-sized and high-rating components not only increases system cost, but also leads to reductions in converter efficieny, power denity, and dynamical speed.

The conventional approach to tackle these problems is by implmentation of stage 1 conversion system through multiple converter modules instead of a single module. These converter modules are connected in series or parallel in their input and output terminals and can handle high voltage and current levels efficiently. For example, an Input-Series-Output-Parallel (ISOP) DC-DC conversion system is composed of several identical converter modules, which are connected in series and parallel in their input and output terminals, respectively [17, 70]. By connecting the modules in series at their input terminals, the total voltage is divided between the converters and each module need to handle lower voltage levels, enabiling converter implementation with lower-rating components [17, 69, 70]. Similar to ISOP conversion systems, Input-Series-Output-Series (ISOS), Input-Parallel-Output-Series (IPOS), and Input-Parallel-Output-Parallel (IPOP) converters can also be defined [17, 70]. For example, the ISOP configuration can handle high input voltage and high output current levels in stage 1 converters of a data center.

Modular DC-DC converters can be controlled in either centralized or decentralized method. In centralized control scheme, the information regarding voltages and currents of all modules is recieved by a common processor, which is responsible for processing this information and generating control inputs for all modules. These control inputs are passed on to the modules, once generated by the central DSP. On the other hand, in decentralized control technique, each module is controlled by a separate DSP controller, which only relies on the voltage and current information of its associated module to generate control inputs. The centralized controllers benefit from optimized system dynamics as a result of having access to all the system information. However, they require communications among modules and this creates delays and reduces system reliability. On the other hand, decetralized control approaches benefit from increased reliability and removed delays. But they may not provide the most optimum dynamics owing to have limited access to system information.

The control challenges in stage 1 modular conversion system include sharing transferred power equally among converter modules to maximize modularity [69, 72, 89, 90, 91], dynamical enhancements, and stability issues [89]. In this regard, the transferred power must be equally shared among all modules such that high voltage and current levels are equally divided among modules and the modulairy is maximized [69, 72, 89, 90, 91]. This concept is also referred to as power sharing [69, 72, 89, 90, 91]. Moreover, the entire modular system should possess fast dynamics in response to disturbances. Finally, conventional control methods applicable to a single DC-DC converter might fail to provide a stable operation, when applied to modular conversion systems [89]. Therefore, it is most important to ensure system stability while designing controllers for modular DC-DC converters.

4.1.2 Literature Review

This section provides a literature review on controllers and their requirements in modular DC-DC converters with fast dynamic loads. Today, modular DC-DC converters are used in applications such as data centers, HVDC transmission systems,

electric vehicles (EV), and traction applications [17, 69]. In this subsection, the focus is on stage 1 converters in the power management system of a data center. Generally speaking, using several DC-DC converters instead of a single one to transfer power from source to the load or vice-versa, reduces voltage and current stresses on each converter. In such a case, if each converter is controlled separately, a modular system with higher reliability will be obtained. Common system configurations include input-series-output-parallel (ISOP), input-parallel-output-series (IPOS), and the input-series-ouput-series (ISOS) connection schemes [17, 70], where the parallel and series connections reduce current and voltage stresses on each module, respectively [17, 69, 70]. In a modular DC-DC converter system, the topology used for converters may vary depending on the application. These topologies normally provide galvanic isolation between the input and output. In this regard, Dual-Active-Bridge (DAB) converters are widely used as the main building blocks of modular DC-DC systems, due to their high power densities and bi-directional power-flow capabilities [69, 71].

To utilize the full capacity of a modular DC-DC converter system, power sharing is normally desired to have all modules transfer the same power levels at all instants during transient or steady-state conditions [69, 72]. For ISOP configuration, all modules share the same input currents and output voltages. Therefore, power sharing for this configuration can be achieved by input voltage sharing (IVS), and output current sharing (OCS). Also, depending on the control objective, either one of output voltage regulation (OVR) or output current regulation (OCR) is normally required.

To realize IVS and either OVR or OCR in modular DC-DC converter systems, different control methods have been proposed in the literature [17, 69]. A few methods use well-known control approaches such as Model Predictive Controllers (MPC) and Sliding Mode Controllers (SMC) [70, 71, 72]. MPC controllers improve system dynamics considerably and SMC controllers are robust against parameter mismatches between modules. However, MPC controllers require knowledge of system parameters to achieve a suitable performance, without which robustness issues may arise. Also, SMC controllers may create large overshoots/undershoots in applications dealing with high load currents. This is beacuse the sliding surfaces are usually defined as a linear combination of voltage error signals and their time-integrals and SMC controller keeps this sliding surface constant over time [72]. Therefore, the voltage error signals become exponential and as exponential signals cannot have a zero level at their beginning time instants, large overshoots or undershoots may sometimes be observed. Peak Current Control method is used in [17] to improve the performances of modular DC-DC converters. Such controllers are suitable for applications with fast changing supply voltages [17]. However, applying peak current controllers to applications with fixed switching frequencies may cause stability issues [73]. In fact, using peak-current controllers can lead to instabilities due to sub-harmonics, chaos, bifurcations, and duty cycle saturation phenomena [74, 73, 75].

Other methods in the literature use linear controllers and master/slave or cross-duty cycle structures [6, 76, 77]. These controllers mitigate isolation issues in designing sensors, and enhance dynamic responses of the system and they have simple

control structures [6, 76, 77]. However, they require communications between different modules, reducing the system reliability. Other controllers rely on solving non-linear control equations to find the required duty cycle, where the non-linear equations include the non-linear voltage/current gain equations [69, 71, 78]. These controllers enhace the dynamic responses of the system considerably and provide fast transient responses with low overshoots/undershoots. However, they need to estimate system parameters to provide accurate power sharing between modules, which might make system operation and controller structure complex.

Droop/Inverse Droop controllers and gradient-based control methods are also used to improve the performances of modular DC-DC converters [7, 16, 79]. These controllers have simple structures and they improve the dynamic characteristics of the system. However, as they build a linear relationship between DC link voltage errors and output voltage errors, they create trade-offs between input voltage sharing and output voltage regulation. Applying common duty-ratios to all modules is another control approach for modular converters [80, 81, 82]. Although these methods provide simple control structures, they cannot provide satisfactory power sharing between modules at steady-state, in case the parameter mismatches between modules are significant [69, 83, 84]. Instead of relying on control systems, some approaches propose topological modifications to modular DC-DC converters, to realize power sharing and output voltage regulation [85, 86, 87, 88]. Some use voltage equalizing circuits in parallel with the DC link capacitors of different modules [85]. in other approaches, switched-capacitor circuits and buck-boost balancing circuits are connected [86] to the input sides of modules. Alternatively, it is also shown that power sharing can be achieved by common mode coupled inductors [87], or flying capacitors [88]. The topological modifications made above realize systematic power sharing and increase the modularity of the system. However, they increase the system complexity and cost.

4.1.3 Targets and Contributions

The objective of this chapter is to propose a new control framework for modular ISOP and IPOS DC-DC conversions systems which can:

1. Achieve equal power sharing among all modules.
2. Provide fast converter dynamics.
3. Provide a stable operation.
4. Operate in both power flow directions i.e. source-to-load and load-to-source directions.
5. Maintain a suitable performance in presence of parameter variations among modules.

Contributions: This chapter proposes a new decentralized controller for ISOP and IPOS DC-DC converters, which improves system performance in terms of dynamical response, power sharing among modules, and voltage/current regulation. The proposed approach can be applied in data center stage 1 converters to enhance system dynamics, power sharing, and transferred power regulation independently and without trade-offs. Furthermore, the presented control system can facilitate

bi-directional power flow between the source and loads. Also, the proposed controller is decentralized and does not need any communications among modules. Moreover, the proposed method does not use complicated nonlinear calculations like the square root and it uses rather-simple nonlinear operators such as multiplication and division. This avoids extra processing calculation delays, during the controller implementation process. The proposed control structure is simple and unlike inverse-droop controllers, there is no trade off between IVS and OVR. It should be mentioned that the controller performance is not degraded by parameter mismatches among modules and the controller does not increase system cost, by avoiding additional hardware and measurement sensors. Finally, the proposed controller can be used for topologies such as DAB, flyback, and forward converters, in ISOP or IPOS configurations. The controller effectiveness is verified by simulation and experimental results and the performance is also compared with other existing methods, to demonstrate the advantages of the proposed controller.

4.2 Chapter Main Control Concept

This section presents a new distributed control approach for modular ISOP and IPOS DC-DC converters specifically when fast dynamic loads are considered. This approach is extendable to IPOP/ISOS configurations, as well. For a single DC-DC converter in a modular configuration and a specific power flow direction, a converter duty cycle, denoted by d, can be defined such that the transferred power is increased, when d increases. Fig. 4.2(a) shows a Modular ISOP DC-DC Converter System containing N modules and Fig. 4.2(b) shows the general structure of the proposed controller.

In Fig. 4.2, the following notations are used: C_i is the value of DC-link capacitors for different modules, v_{Cj}, $0 < j < N+1$ is the voltage across the DC-link capacitor of the j-th module, N is the number of modules, i_{inj}, $0 < j < N+1$ is the input current of the j-th module, i_{oj}, $0 < j < N+1$ is the output current of the j-th module, C_o is the output capacitor, i_o is the load current, v_{in} is the input voltage, and L_o is the output-side inductor. Also, v_o denotes the output voltage and d_k denotes the duty cycle associated with the k-th module. Moreover, $v_{C,ref}$ and $i_{o,ref}$ denote the reference values for v_{Ci} and i_o, respectively.

Fig. 4.2(b) shows the general controller structure. In this figure, f is a nonlinear function of v_{Ci} and i_o, and one of the control objectives includes regulation of v_{Ci} and i_o. In other words, it is desired to have $v_{Ci} = v_{C,ref}, i_o = i_{o,ref}$, in steady-state conditions. Therefore, at steady-state, $f(v_{Ci}, i_o) = f(v_{C,ref}, i_{o,ref})$. Let us assume that the amount of instantaneous power transferred by the k-th converter is denoted by $p_k(t)$. As it was stated earlier, d_k is defined so that $p_k(t)$ increases by increasing d_k. The proposed controller in Fig. 4.2(b) is composed of two parts: the Nonlinear function error or i.e. $f(v_{Ci}, i_o) - f(v_{C,ref}, i_{o,ref})$, an integrator which forces the error generated by the first part to be equal to zero at steady-state. Let us denote the load power by $p_o(t)$ and assume that the power is being transferred from the input side to the battery. In this case, if for example $p_o(t)$ is greater than its reference value, excessive power is being transferred to the load and to reduce this excessive power,

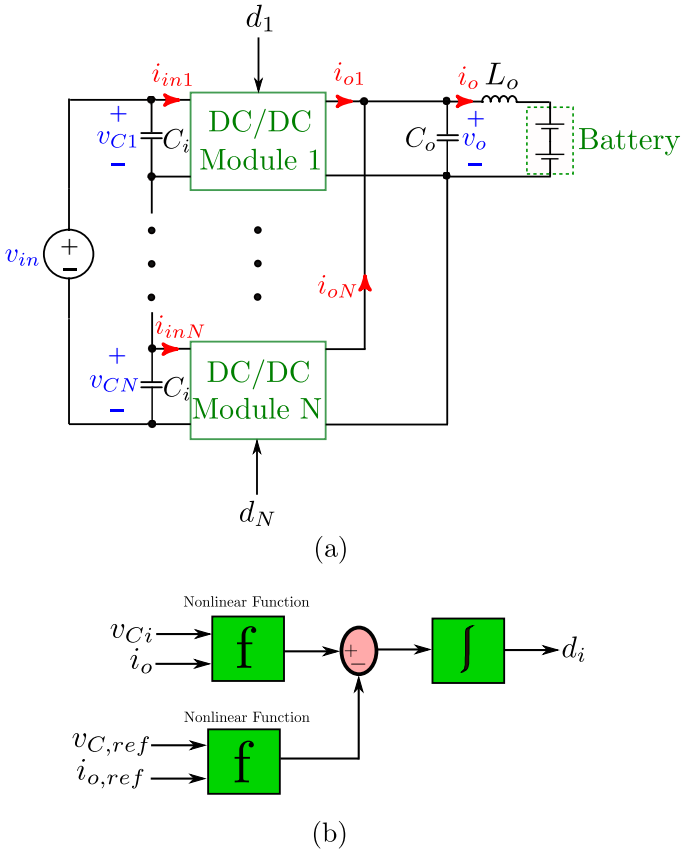


Figure 4.2: (a) ISOP DC-DC Converter System (b) General Controller Structure

every module such as the k-th module needs to adjust its contribution by reducing $p_k(t)$ through d_k reduction. To this end, the function f should be chosen such that the controller properly adjusts d_k. To select the f function, first it should be determined whether each of the controller variables including v_{Ci} and i_o, has a proportional or an inverse relationship with $p_i(t)$, that is the transferred power by the i-th module. For example, in the converter shown in Fig. 4.2(a), i_o is proportional to p_i and v_{Ci} is inversely proportional to p_i. Next, f should be selected such that for example in our discussed case, $f(v_{Ci}, i_o)$ is reduced if there is excessive p_o. This way, if there is extra output power during a transient, the signal integrated to produce d_i will have a negative sign and d_i will be decreased, resulting in the reduction of $p_i(t)$. It is worth mentioning that for an accurate system performance, the f function must be selected in a way that $f(v_{Ci}, i_o) = f(v_{C,ref}, i_{o,ref})$ guarantees $v_{Ci} = v_{C,ref}, i_o = i_{o,ref}$. This way, appropriate power sharing among the modules and voltage/current regulation are achieved at the same time.

The integrator in the proposed control structure increases the system's robustness and ensures appropriate power sharing among the modules, even in the presence of considerable parameter mismatches among the modules. Also, the proposed controller does not use the values of circuitry parameters, reducing the effect of parameter uncertainties. In the next chapters, it will be shown that the value of the f function is proportional to v_{Ci}. This increases the sensitivity of the f function to

the differences between the DC link voltages of different modules. Also, the integrator provides a more robust control performance. So, the combined usage of the f function and the integrator significantly reduces the maximum power mismatches among the modules in the transient period and provides a better power sharing, in the transient period. It is worth mentioning that the proposed controller is applicable to all modular ISOP/IPOS/ISOS/IPOP DC-DC converters, regardless of the topologies used for each module.

4.3 Formulation of the Proposed Controller

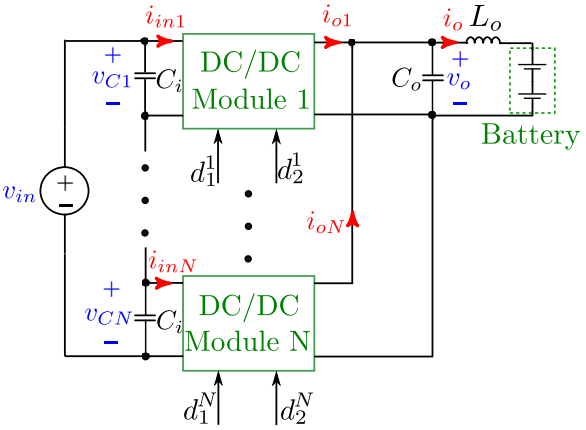
4.3.1 System Description

Fig. 4.3 shows a modular ISOP/IPOS DC-DC converter system composed of N modules. The modular structure shown in Fig. 4.3 can be connected either to a battery or a resistive load.

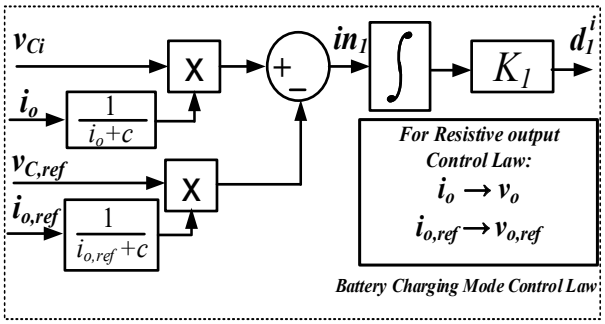
In Fig. 4.3, the following notations are used: Each module operates with two duty cycles of ${d_1}^i$ and ${d_2}^i$ for charging and discharging modes, respectively, and has an input capacitor of C_i, input voltage of v_{Ci}, input current of i_{ini}, and output current of i_{oi}, where $1 \leq i \leq N$. As the modules' outputs are connected in parallel, there is only one equivalent output capacitor C_o with an output voltage of v_o. This capacitor is connected to an inductive filter of L_o, which is in series with a battery. The duty cycles applied to a module are defined such that in each power flow direction mode, an increase in the associated duty cycle will increase the power transferred by the module. It is worth mentioning that the structure shown in Fig. 4.3 acts as an ISOP and IPOS structure, in the battery charging and discharging modes, respectively. In the next subsection, the distributed control system is formulated so that all the modules can collaboratively regulate the output voltage/current and maintain power sharing without any inter-modular high bandwidth communication system.

4.3.2 Controller Formulation

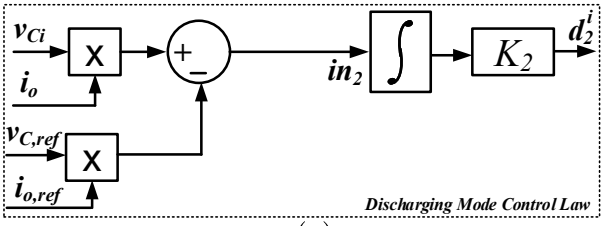
This subsection presents the process of controller derivation for the case in which a battery is connected to the output of ISOP DC-DC converters. In this case, the objective is to keep the load (Battery) current level i_o constant at its reference, denoted by $i_{o,ref}$. In fact, the battery is being charged or discharged based on a given reference current $i_{o,ref}$, that is provided by the energy management system. The energy management system provides the maximum safe reference values based on charging curves to achieve fast charging while maximizing the life-time of the Battery. When the battery is used as an energy storage unit for a microgrid, $i_{o,ref} = \frac{P_req}{v_{nom}}$. In this equation, P_{req} is the power required for the stable operation of the grid and v_{nom} is the nominal voltage of the battery. To realize the power sharing among modules, v_{Cj} must be regulated at $v_{C,ref} = \frac{v_{in}}{N}$, in which $v_{C,ref}$ denotes the reference value for the voltage across the DC-link capacitor of each module. Below, the control law for battery charging and discharging modes is proposed under two separate parts.



(a)



(b)



(c)

Figure 4.3: (a) Schematic of Modular ISOP/IPOS DC-DC Converters (b) Proposed Controller for Battery Charging Mode in i-th Module, $1 \leq i \leq N$ (c) Proposed Controller for Battery Discharging Mode in i-th Module, $1 \leq i \leq N$

Charging mode Control Law: When the battery is being charged and i_o becomes larger than $i_{o,ref}$, this means that an excessive amount of power is being transferred and thus, less amount of power should be transferred from the input side by reducing ${d_1}^j$. However, when v_{Cj} becomes larger than $v_{C,ref}$, the input capacitor of the j-th module must be discharged more, or equivalently, more amount of power should be transferred from the input side to the battery, which can be done by increasing ${d_1}^j$. Therefore in charging mode, ${d_1}^j$ is directly proportional to v_{Cj} and inversely proportional to i_o. This means that ${d_1}^j$ is directly proportional to $\frac{v_{Cj}}{i_o}$. Considering that in steady-state condition, $\frac{v_{Cj}}{i_o} = \frac{v_{C,ref}}{i_{o,ref}}$, the following decentralized control law is proposed for module j in the charging mode:

$$ {d_1}^j = k_1 \int \left(\frac{v_{Cj}}{i_o} - \frac{v_{C,ref}}{i_{o,ref}} \right) dt. \tag{4.1} $$

In (4.1), $v_{C,ref}$ is set as follows:

$$v_{C,ref} = k_{i1} \int (i_o - i_{o,ref}) + k_{p1}(i_o - i_{o,ref}). \tag{4.2}$$

In fact, (4.2) includes an integrator to force i_o to track $i_{o,ref}$. At the same time, this formula obtains the accurate reference for input DC link capacitor voltages. As the battery current level is negative in the battery discharging mode, the control law in (4.1) is modified by inserting a constant number c in the denominator of the existing fractions. This is done to avoid the denominators to change sign or become zero during load steps. The modified control law for charging mode is expressed as:

$$d_1{}^j = k_1 \int \left(\frac{v_{Cj}}{i_o + c} - \frac{v_{C,ref}}{i_{o,ref} + c} \right) dt. \tag{4.3}$$

Eq. (4.3) forces $\frac{v_{Cj}}{i_o+c}$ to track its reference value due to the integrator. In this part, the voltage across the input DC link capacitor of module i at steady-state is denoted by V_{Ci}. Moreover, the output current level at steady-state is denoted by I_o. If all modules implement the same controller, (4.3) yeilds:

$$\frac{V_{C1}}{I_o + c} = \frac{V_{C2}}{I_o + c} = ... = \frac{V_{CN}}{I_o + c} = \frac{v_{C,ref}}{i_{o,ref} + c}. \tag{4.4}$$

From (4.4) and Fig. 4.3(a), it can be seen that $V_{C1} = V_{C2} = ... = V_{CN}$. Therefore, appropriate power sharing is achieved among the modules. This is while KVL in the input side of the circuit along with power sharing imply $V_{Ci} = V_{Cj} = \frac{v_{in}}{N}$ for modules i and j. Also, The integrator in (2) sets $I_o = i_{o,ref}$. Therefore, power sharing and (4.4) result in $V_{Ci} = V_{Cj} = v_{C,ref} = \frac{v_{in}}{N}$. This way, power sharing and output current regulation are both achieved.

Discharging Mode Control Law: When the battery is discharged to be used as an energy storage device, $i_o < 0, i_{o,ref} < 0$. Using the same approach provided above for the battery charging mode, it can be seen that the required control law for the battery discharging condition is as below:

$$d_2{}^j = k_2 \int (v_{Cj} i_o - v_{C,ref} i_{o,ref})\, dt. \tag{4.5}$$

Similar to the charging mode, $v_{C,ref}$ is obtained by applying the battery current error to a PI controller. This causes i_o to track $i_{o,ref}$, or equivalently $I_o = i_{o,ref}$. Eq. (4.5) includes an integrator, resulting in:

$$V_{C1} I_o = V_{C2} I_o = ... = V_{CN} I_o = v_{C,ref} i_{o,ref}. \tag{4.6}$$

From this equation, $V_{C1} = V_{C2} = ... = V_{CN}$ and power ssharing is achieved among modules. Equation (4.6) and the fact that $I_o = i_{o,ref}$, result in $V_{C1} = v_{C,ref}$ at steady-state condition. therefore, both power sharing and current regulation are achieved in the discharging mode. The general block diagram of the proposed contoller is shown in Fig. 4.3 and a more detailed version is shown in Fig. 4.4 It is worth mentioning that Fig. 4.4 uses a Soft Transition Control, which will be introduced in the next subsection.

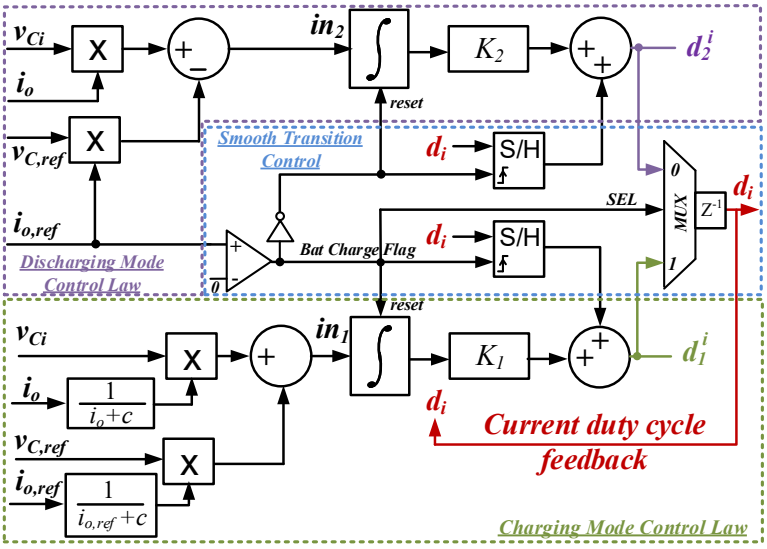


Figure 4.4: Schematic of the Proposed Controller for ISOP/IPOS DC-DC Converters with Soft Transition Control

4.3.3 Soft Transition Control Concept

As it can be seen, (1) and (5) express the control laws associated with battery charging and discharging conditions, respectively. Therefore, in a transition between these two modes, the controller architecture needs to be changed. This might cause undesired overshoots/undershoots in the load current. To solve this issue, a soft transition control is proposed where control integrators are switched from one control law to another and initialized with the previous duty cycle. So, for example, in a transition from charging to discharging modes, the control law in (5) should be used for the discharging mode and right at the transition, the integrator in (5) will be initialized from the previous duty cycle in the charging mode. Thus, no jump in the duty cycle is generated. In the proposed soft transition control, $i_{o,ref}$ is compared with zero to assess the power flow direction in the system. If $i_{o,ref}$ does not change sign, the soft-transition blocks are not activated. Using the approaches discussed above, the transitions from charging to discharging mode or vice-versa become seamless by a smooth change in duty cycle, resulting in no overshoots/undershoots in the system voltages and currents. This method enables the controller to maintain its stable operation in a wide load range while supporting transitions from high positive load currents to high negative load currents or vice-versa.

It is worth mentioning that for resistive load cases, the control law can be simplified to chaging mode control law according to (4.3), as the power is unidirectional to the load and the control structure becomes simpler. In this case, the value of the load resistance which is denoted by R, can be calculated by dividing the output voltage by the load current. After obtaing R, $i_{o,ref}$ can be obtained using $i_{o,ref} = \frac{v_{o,ref}}{R}$, in which $v_{o,ref}$ is the reference value for the output voltage.

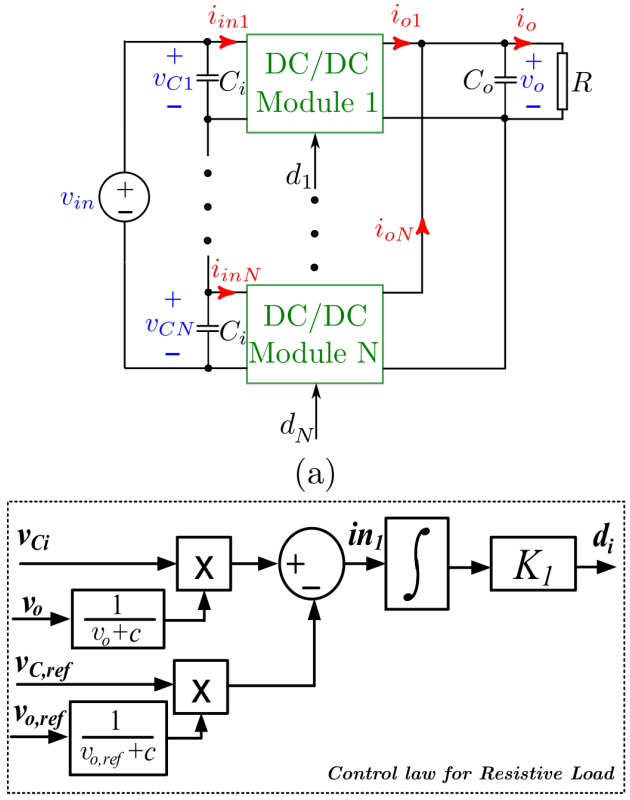


Figure 4.5: (a) Schematic of Modular ISOP DC-DC Converters with Resistive Load (b) Proposed Controller Block Diagram

4.4 Dynamical Characteristics Analysis of the Proposed Controller

This section investigates the characteristices of the proposed controller. In particular, the dynamical profile of a closed-loop ISOP/IPOS DC-DC conversion system with the presented control is explained. It should be mentioned that this chapter compares the performance of the proposed controller only with the existing controllers that do not use communications among modules. Fig. 4.5(a) shows the schematic of an ISOP modular DC-DC conversion system comprising N modules. This system interfaces an input voltage source to a resistive load. Fig. 4.5(b) shows the block diagram of the proposed controller for this system. The control system should regulate the output voltage v_o at $v_{o,ref}$.

When the load resistance value in Fig. 4.5(a) changes from R_1 to R_2 in a load step, the level of total power transferred to the load by the modules in steady-state needs to change from $\frac{{v_{o,ref}}^2}{R_1 N}$ to $\frac{{v_{o,ref}}^2}{R_2 N}$. This is because the controller must regulate both input DC-link and output voltages at their reference values simultaneously and if equal power sharing is lost as a result of a load step during the transient period, both input DC link and output voltages require a longer amount of time to reach their steady-state values due to sharing a portion of controller capacity

with each other. The most important control objective during a load step transient is to maintain equal power sharing among the modules, to avoid modular input DC-link overvoltages and potential damages. Therefore, it is important to make sure that for module i ($0 < i < N + 1$), the recovery time and overshoot levels associated with input DC link voltage of i-th module v_{Ci} are minimal. Once this objective is achieved, the control system can allocate most of its capacity to regulate the output voltage and will be able to reduce the output voltage recovery time and overshoot/undershoot. In conclusion, the control system should apply larger changes to i-th module duty cycle d_i in response to v_{Ci} deviating $v_{C,ref}$, compared to a case in which v_o deviates $v_{o,ref}$. Based on this conclusion, the proposed controller in Fig. 4.5(b) is designed such that v_{Ci} is in the nominator of the fraction and v_o is in the denominator. Therefore, the entire fraction is more sensitive to changes of v_{Ci} compared with changes of v_o. The mathematical proof for this is given below. Denoting $\widetilde{v_o} = v_o - v_{o,ref}$ and $\widetilde{v_{Ci}} = v_{Ci} - v_{C,ref}$, as well writing the Taylor series for the function $g\left(v_{Ci}, v_o\right) = \frac{v_{Ci}}{v_o + c}$ around the point $({v_{Ci}}^*, {v_o}^*) = (v_{C,ref}, v_{o,ref})$ up to the 2-nd order polynomial result in:

$$\begin{aligned} g\left(v_{Ci}, v_o\right) = g(v_{Ci}^*, v_o^*) + \frac{\widetilde{v_{Ci}}}{v_{o,ref} + c} - \frac{v_{C,ref}\widetilde{v_o}}{\left(v_{o,ref} + c\right)^2} \\ + \frac{2v_{C,ref}{\widetilde{v_o}}^2}{\left(v_{o,ref} + c\right)^3} - \frac{2\widetilde{v_{Ci}}\widetilde{v_o}}{\left(v_{o,ref} + c\right)^2} \end{aligned} \tag{4.7}$$

Also, according to Fig. 4.5(b) the control law is given by:

$$\begin{aligned} d_i &= K_1 \int \left(\frac{v_{Ci}}{v_o + c} - \frac{v_{C,ref}}{v_{o,ref} + c} \right) dt \\ &= K_1 \int \left(g(v_{Ci}, v_{o,ref}) - g(v_{Ci}^*, v_o^*) \right) dt \end{aligned} \tag{4.8}$$

According to (4.7) and (4.8), the time derivative of d_i can be expressed as:

$$\begin{aligned} \frac{d(d_i)}{dt} = \frac{K_1\widetilde{v_{Ci}}}{v_{o,ref} + c} - \frac{K_1 v_{C,ref}\widetilde{v_o}}{\left(v_{o,ref} + c\right)^2} \\ + \frac{2K_1 v_{C,ref}{\widetilde{v_o}}^2}{\left(v_{o,ref} + c\right)^3} - \frac{2K_1\widetilde{v_{Ci}}\widetilde{v_o}}{\left(v_{o,ref} + c\right)^2} \end{aligned} \tag{4.9}$$

Now, if $\widetilde{v_{C1}} = \alpha v_{C,ref}$,$\widetilde{v_o} = 0$, (4.9) yileds $\frac{d(d_i)}{dt} = \frac{K_1 \alpha v_{C,ref}}{v_{o,ref} + c} = K_1 \alpha g\left(v_{Ci}^*, v_o^*\right) = P_1$. However, assuming $\widetilde{v_{C1}} = 0, \widetilde{v_o} = \alpha v_{o,ref}$ results in $\frac{d(d_i)}{dt} = K_1 \frac{v_{o,ref}\left[\left(2\alpha^2 - \alpha\right)v_{o,ref} - \alpha c\right]}{\left(v_{o,ref} + c\right)^2} \times g\left(v_{Ci}^*, v_o^*\right) = P_2$. If $\alpha \ll 1$, then $|\frac{P_2}{P_1}| = \frac{v_{o,ref}}{v_{o,ref} + c}$. In controller design, the value of c is designed such that it is comparable with $v_{o,ref}$. This results in $|P_2| < |P_1|$. In other words, the controller produces a stronger response when the input DC link voltage deviates from its reference, compared to a condition in which the output voltage deviates from its reference value. Also, from the above discussion and mathematical equations, it can be observed that $P_1 \propto \alpha$ and $P_2 \propto \alpha$. In other words, the proposed controller varies the duty cycle proportionally in response to

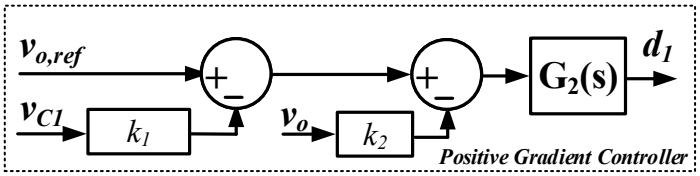


Figure 4.6: Schematic of Positive Output Voltage Gradient Control Method [16]

power sharing mismatches and output voltage error. This increases the dynamical speed of the system using the proposed controller. However, in other existing controllers, this does not occur. For example, in the positive output voltage gradient controller [16] which is shown in Fig. 4.6, $v_{o,ref} - k_1 v_{C1} - k_2 v_o$ is applied to $G_2(s)$ to generate the duty cycle. To illustrate the concepts better and to avoid unnecessary complications, in this part it is assumed that $G_2(s)$ is purely integrative and is equal to $G_2(s) = \frac{\beta}{s}$. The results remain valid for other types of controllers such as PI controller, etc. Using this assumption, the time derivative of duty cycle of one module is $\frac{d(d_1)}{dt} = \beta(v_{o,ref} - k_1 v_{C1} - k_2 v_o)$. If $\widetilde{v_{C1}} = \alpha v_{C,ref}$ and $\widetilde{v_o} = 0$, $\frac{d(d_1)}{dt} = \beta\left(v_{o,ref} - (\alpha+1)\, v_{C,ref} - k_2 v_{o,ref}\right)$. In other words, unlike what observed when the proposed controller was applied, the duty cycle?s time derivative is not proportional with α. Therefore, the dynamical speed will be slower in the positive output vltage gradient controller, compared with the proposed controller in this chapter.

In conclusion, there are two reasons for fast dynamical response of the proposed controller from the conceptual perspective. The first one is that the proposed controller changes the duty cycle of a module in proportion to input DC-link voltage errors and output voltage errors. Also, the controller produces larger responses for power sharing mismatches in comparison to output voltage errors. This is done in order to maintain equal power sharing among modules during transients and prevent overvoltages and potential increases in recovery times in the first place. Therefore, the controller can devote a larger portion of its capacity to output voltage regulation right after the load step, by avoiding simultaneous modifications made to both input DC-lonk voltages and output voltage. As a result, better dynamical responses with reduced overshoot/undershoots and reduced recovery times are obtained.

4.5 Controller Analysis for Modular ISOP/IPOS DAB Converters

In this section, the stability analysis for the proposed controller is provided for modular IPOS/ISOP DAB Converters, and a simulation case-study is presented to verify the accuracy of the stability analysis. It is assumed that each module is a DAB converter and the stability analysis is conducted for the battery charging mode only as the discharge mode is similar.

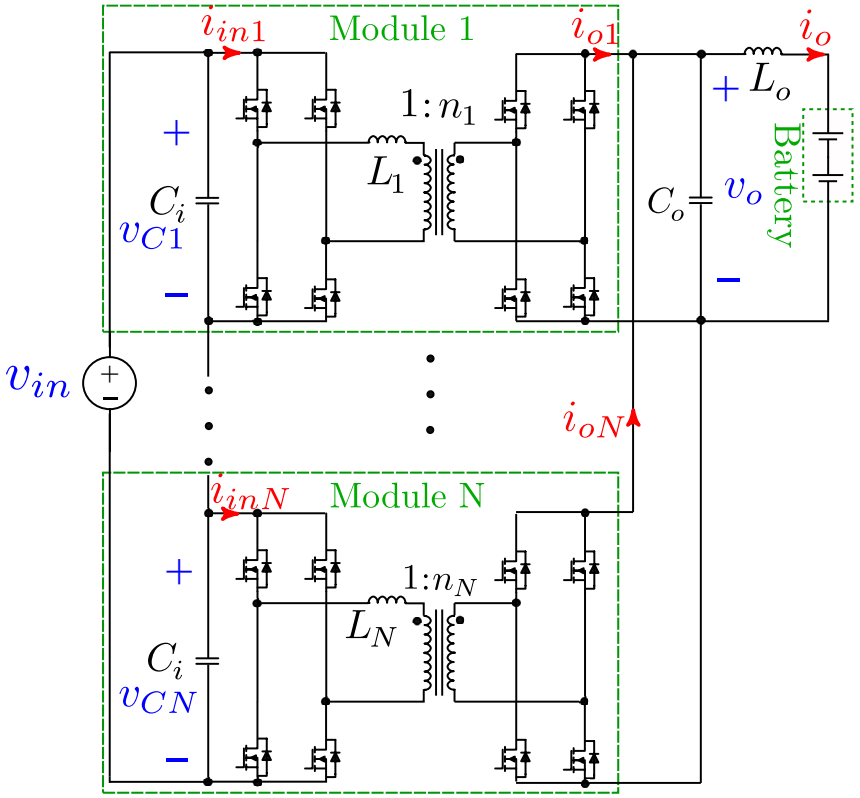


Figure 4.7: Schematic of ISOP/IPOS DAB Converters

4.5.1 System Description

Fig. 4.7 shows an ISOP/IPOS DAB converter structure. This figure uses the same notations as before and the following new notations for the j-th module: n_j: primary to secondary turns ratio, L_j: tank inductance, and D_j:the phase-shift ratio which is related to the phase-shift angle (θ_j) between the two bridges by $\theta_j = \pi D_j$.

4.5.2 Controller Analysis

To analyze the control system, first, gain relationships for the system shown in Fig. 4.7 are derived. In a DAB converter, the output current-to-input voltage gain can be obtained [78, 114] as:

$$\frac{i_o}{v_{in}} = \frac{T_s}{2nL} D(1-D) = \lambda D(1-D). \tag{4.10}$$

It should be stated that (4.10) is valid even during transient states [78, 115]. Based on (4.10) and Fig. 4.7, the relationships between output currents and input voltages in different modules can be written as:

$$i_{o1} = \lambda_1 v_{C1} D_1(1-D_1), ..., i_{oN} = \lambda_N v_{CN} D_N(1-D_N). \tag{4.11}$$

Assuming ideal DAB modules, $v_{Cj} i_{inj} = v_o i_{oj}$, and the following equations can be obtained using (4.10) and (4.11):

$$i_{in1} = \lambda_1 v_o D_1(1-D_1), ..., i_{inN} = \lambda_N v_o D_N(1-D_N). \tag{4.12}$$

If KCL is written for the input side of modules in Fig. 4.7, the following equation is obtained ($i \neq j, 0 < i, j < N+1$):

$$\lambda_i v_o D_i(1-D_i) + C_i \frac{v_{Ci}}{dt} = \lambda_j v_o D_j(1-D_j) + C_i \frac{v_{Cj}}{dt}. \tag{4.13}$$

By KVL, it is known that $v_{C1}+v_{C2}+...+v_{CN} = v_{in}$. Thus, $\frac{dv_{C1}}{dt}+\frac{dv_{C2}}{dt}+...+\frac{dv_{CN}}{dt} = \frac{dv_{in}}{dt} = 0$. Using this fact and by summing up all the sides of (4.13):

$$\sum_{i=1}^{N} \lambda_i v_o D_i(1-D_i) = N\lambda_1 v_o D_1(1-D_1) + NC_i \frac{dv_{C1}}{dt}. \tag{4.14}$$

From (4.14), the following can be obtained ($0 < j < N+1$):

$$\frac{dv_{Cj}}{dt} = \frac{(1-N)\lambda_j D_j(1-D_j) + \sum_{i=1, i\neq j}^{N} \lambda_i D_i(1-D_i)}{NC_i}. \tag{4.15}$$

Using KCL for the load-side node of modular DAB converters leads to:

$$\lambda_1 D_1(1-D_1)v_{C1} + ... + \lambda_N D_N(1-D_N)v_{CN} = C_o \frac{dv_o}{dt} + i_o. \tag{4.16}$$

Let us assume that the battery connected to ISOP DAB converters can be modeled by a series branch composed of an ideal voltage source with voltage V_b and a resistor with a resistance of R_b. Using KVL in the converter output leads to:

$$V_b + R_b i_o + L_o \frac{di_o}{dt} = v_o. \tag{4.17}$$

From (4.3), the control law can be obtained as ($0 < j < N+1$):

$$\frac{dD_j}{dt} = K\left(\frac{v_{Cj}}{i_o + c} - \frac{v_{Cref}}{i_{o,ref} + c}\right). \tag{4.18}$$

Equation (4.15), (4.16), (4.17), and (4.18) express the dynamical equations of the system in state-space domain. In order to perform the stability analysis, this system has to be linearized around its equilibrium points and the poles of the linearized system must be found. For the sake of demonstration and to simplify the derivations, let us assume there are two DAB converters connected by ISOP configuration. In this way, the small-signal state vector is defined as $x = \left[\tilde{v_{C1}}, \tilde{v_o}, \tilde{i_o}, \tilde{D_1}, \tilde{D_2}\right]^T$, and $\frac{dx}{dt} = Ax$ is found by linearizing the system around its equilibrium point. It should be mentioned that the values of D_1 and D_2 at the equilibrium point of the system are denoted by $D_1{}^*$ and $D_2{}^*$, respectively. Matrix A can be found as:

$$A = \begin{bmatrix} 0 & 0 & 0 & -\frac{\lambda_1 v_{o,ref}(1-2D_1{}^*)}{2C_i} & \frac{\lambda_2 v_{o,ref}(1-2D_2{}^*)}{2C_i} \\ 0 & 0 & \frac{-1}{C_o} & \frac{\lambda_1 v_{Cref}(1-2D_1{}^*)}{C_o} & \frac{\lambda_2 v_{Cref}(1-2D_2{}^*)}{C_o} \\ 0 & \frac{1}{L_o} & \frac{-R_b}{L_o} & 0 & 0 \\ \frac{K}{i_{o,ref}+c} & 0 & \frac{-Kv_{Cref}}{(i_{o,ref}+c)^2} & 0 & 0 \\ \frac{-K}{i_{o,ref}+c} & 0 & \frac{-Kv_{Cref}}{(i_{o,ref}+c)^2} & 0 & 0 \end{bmatrix} \tag{4.19}$$

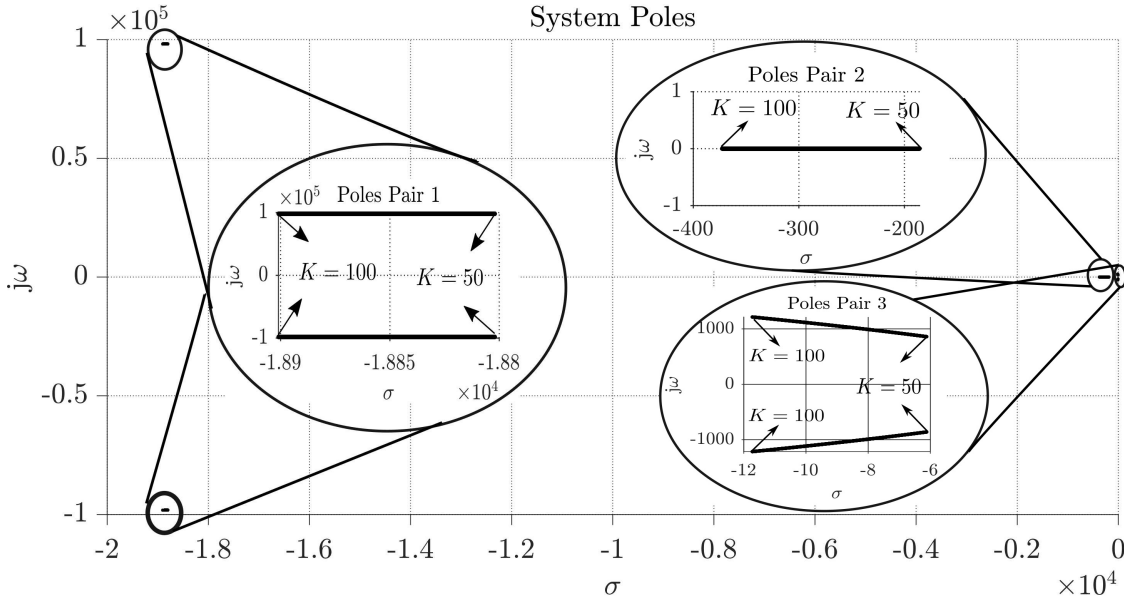


Figure 4.8: Root Locus Diagram for System Poles in Case-Study with 20A Load Current and $50 < K < 100$.

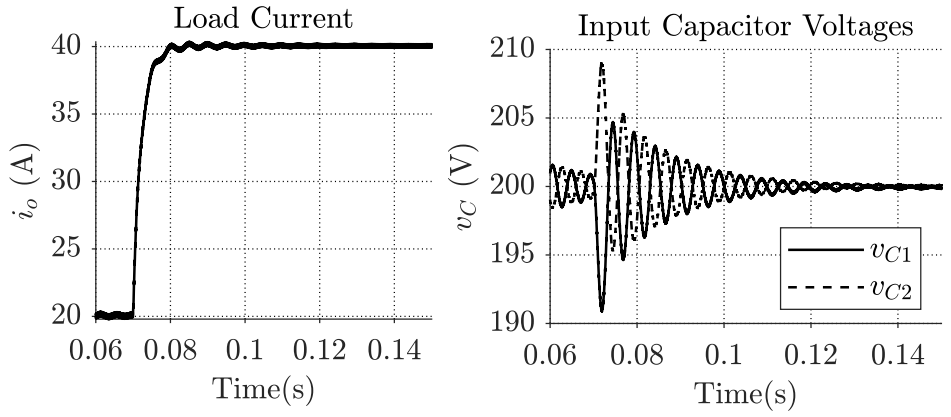


Figure 4.9: System Response to a 20A-to-40A Load current Step in Case-Study

Case Study: Let us consider an ISOP two-module DAB converter system with the following parameters: $C_{i1} = 20\mu$F, $C_{i2} = 30\mu$F, tank inductances of 9μH and 12μH for the first and second DAB modules, transformer turns rations of 3.4:1, 2.8:1 for the first and second modules, switching frequency of 100KHz, $C_o = 100\mu$F, $v_{in} = 400$V, $V_b = 56$V, $R_b = 38m\Omega$. In this system, $i_{o,ref}$ experiences a step change from 20A to 40A. If matrix A is calculated and its eignevalues are plotted in a root-locus diagram for $50 < K < 100$, Fig. 4.8 will be obtained. The simulation result of the system response to a 20A-to-40A load current step is illustrated in Fig. 4.9.

As Fig. 4.9 and (4.19) illustrate, there are 5 poles associated with the system. These poles include two complex-conjugate pole pairs and a pole with zero imaginary part. These are shown under pair 1, pair 2, and pair 3 in Fig. 4.8. As this figure

shows, all of system poles are located on the left half of s-plane and therefore, the system is stable. By comparing Fig. 4.9 with Fig. 4.8, the accuracy of (4.19) is validated. It should be mentioned that Fig. 4.9 corresponds to K=100. Using Fig. 4.8, it can be observed that the system pole pairs 2 and 3 are much closer to the $j\omega$ axis, compared with pole pair 1. Thus, pole pairs 2 and 3 are the dominant poles of the system, which describe the system behavior. As Fig. 4.9 illustrates, the time constant of the exponential waveform associated with load current transient is consistent with the real pole shown in Fig. 4.8 under pole pair 2. As it can be observed, for K=100, this pole is predicted as -370/s, which is correspondent to a time constant of 0.0027s. From Fig. 4.9, this time constant is 0.0024s. As it can be observed, these values are reasonably close to each other, noting that the analysis was conducted based on small signal assumptions and the change from 20A to 40A is large signal variations. Moreover, the frequency of the damping oscillations observed in the voltage waveform of DC-link capacitors are calculated as 181.8 Hz, using Fig. 4.9. This frequency is associated with the imaginary part of the system pole pair 2 in Fig. 4.8. Using Fig. 4.8, the frequency of the oscillations is predicted to be $\frac{1214}{2\pi}$ =193.3Hz, which is again in agreement with the 181.8 Hz obtained from simulation results. The reason why the oscillations in Fig. 4.9 are damped slowly is that ISOP DAB converters are connected to a battery and unlike resistive loads, a battery does not have any significant damping resistors. But as a battery is going to be charged for minutes and the overshoots/undershots for DC-link capacitor voltages are less than 5 percent, these slow damping waveforms do not make a negative impact on the system's performance. In the next section, simulation results are provided to verify the effectiveness of the proposed controller.

4.6 Proposed Controller Design procedure

This section discusses and derives control parameters design procedure for the proposed controller in both power flow directions. As observed from previous sections, k_1, k_{p1}, and k_{i1} for battey charging mode, as well as k_2, k_{p2}, and k_{i2} for the discharging mode, are control parameters that need to be designed. To design these parameters, the open loop tranfer function of the system is derived using the linearized model of the system around its operating point in Laplace domain. After that, the controller parameters are designed to achieve a target bandwidth and phase margin. This section also analyzes the effect of each controller parameter on bandwidth and phase margin.

4.6.1 Derivation of Open Loop Transfer Function

To begin with, the equations found in the previous section must be linearized around the system operating point. In this regard, the notations of $v_{Cj} = {v_C}^* + \tilde{v_{Cj}}$, $i_o = {i^*}_o + \tilde{i_o}$, $i_{o,ref} = {i^*}_{o,ref} + \tilde{i}_{o,ref}$, and $D_j = D^* + \tilde{D}_j$ are used. The parameters with $*$ and $\tilde{}$ signs represent the operating point values and small signal variations, respectively. Linearization of (4.17) around the system operating point and rewriting the linearized equation in Laplace domain yiled:

$$\tilde{V_o} = (R_b + L_o s)\tilde{I_o} \tag{4.20}$$

in which, V_o and I_o represent the output voltage and output current in Laplace domain, respectively. In this section, the equilibrium point value of v_{Cj} $(0 < j < n+1)$ is denoted by ${v^*}_{C,ref}$. Lineaizing (4.16) around the equilibrium point of the system, along with (4.20) and rewiritng the equations in Laplace domain lead to:

$$\begin{aligned} &\lambda {v^*}_{C,ref}(1-2D^*)\sum_{i=1} N\tilde{D_i} + \lambda D^*(1-D^*)\sum_{i=1}^{N}\tilde{V_{Ci}} \\ &= (L_o C_o s^2 + R_b C_o s + 1)\tilde{I_o}. \end{aligned} \tag{4.21}$$

According to Fig.4.7, $\sum_{i=1}^{N} v_{Ci} = v_{in}$.Therefore, $\sum_{i=1}^{N}\tilde{V_{Ci}} = 0$ in Laplace domain. Hence, (4.21) can be rewritten as:

$$\lambda {v^*}_{C,ref}(1-2D^*)\sum_{i=1} N\tilde{D_i} = (L_o C_o s^2 + R_b C_o s + 1)\tilde{I_o}. \tag{4.22}$$

Similarly, by linearizing (4.15) around the equilibrium point, $\tilde{V_{Cj}}$ in Laplace domain is obtained as:

$$\tilde{V_{Cj}} = \frac{\lambda {v_o}^*(1-2D^*)\left[(1-N)\tilde{D_j} + \sum_{i=1,i\neq j}^{N}\tilde{D_i}\right]}{NC_i s}. \tag{4.23}$$

In battery charging mode, the control law for module j duty cycle is expressed as $D_j = k_1 \int \left(\frac{v_{Cj}}{i_o+c} - \frac{v_{C,ref}}{i_{o,ref}+c}\right) dt$ in which, $v_{C,ref} = k_{p1}(i_o - i_{o,ref}) + k_{i1}\int (i_o - i_{o,ref})dt$. By linearizing the control law around the operating point and rewiritng it in the Laplace domain, the small signal version of the control law in Laplace domain can be expressed as:

$$\begin{aligned} \tilde{D_j} =& \frac{k_1\tilde{V_{Cj}}}{({i^*}_o + c)s} + \frac{\begin{bmatrix} -k_1({v^*}_{C,ref} + k_{p1}({i^*}_o + c))s \\ -k_1 k_{i1}({i^*}_o + c) \end{bmatrix}}{({i^*}_o + c)^2 s^2}\tilde{I_o} \\ &- \frac{\begin{bmatrix} -k_1({v^*}_{C,ref} + k_{p1}({i^*}_o + c))s \\ -k_1 k_{i1}({i^*}_o + c) \end{bmatrix}}{({i^*}_o + c)^2 s^2}\tilde{I}_{o,ref} \end{aligned} \tag{4.24}$$

in which, $\tilde{d_j}(0)$ denotes the initial value of small signal variations in duty cycle applied to module j at $t = 0$. Denoting $H_1(s) = \frac{(1-N)\lambda(1-2D^*){v_o}^*}{NC_i s}$ and $H_2(s) = \frac{\lambda(1-2D^*){v_o}^*}{NC_i s}$, (4.23) can be rewritten as:

$$\tilde{V_{Cj}} = H_1\tilde{D_j} + H_2\sum_{i=1,i\neq j}^{N}\tilde{D_i}. \tag{4.25}$$

Denoting $H_3(s) = \frac{\lambda {v^*}_{C,ref}(1-2D^*)}{L_o C_o s^2 + R_b C_o s + 1}$, (4.22) can be rewritten to obtain:

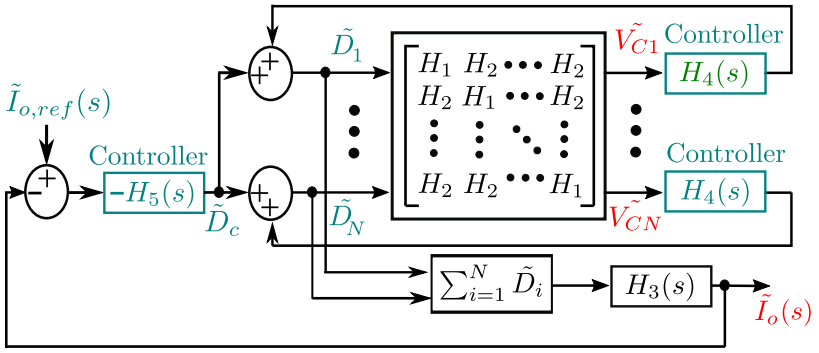


Figure 4.10: Schematic of Linearized Control and Circuitry Loops for Proposed Controller in an ISOP/IPOS DAB Converter System

$$\tilde{I}_o = H_3 \sum_{i=1}^{N} \tilde{D}_i. \tag{4.26}$$

Finally, denoting $H_4(s) = \frac{k_1}{(i_{o,ref}+c)s}$ and $H_5(s) = \frac{\left[-k_1(v^*_{C,ref}+k_{p1}(i_{o,ref}+c))s - k_1 k_{i1}(i_{o,ref}+c)\right]}{(i_{o,ref}+c)^2 s^2}$ in (4.24) yields:

$$\tilde{D}_j = H_4 \tilde{V_{Cj}} + H_5 \tilde{I}_o - H_5 \tilde{I}_{o,ref}. \tag{4.27}$$

The schematic of linearized system circuitry and control loops is provided in Fig. 4.10. Writing (4.25) for all modules in matrix form yileds:

$$\begin{bmatrix} \tilde{V_{C1}} \\ \vdots \\ \tilde{V_{CN}} \end{bmatrix} = \begin{bmatrix} H_1 & H_2 & \cdots & H_2 \\ H_2 & H_1 & \cdots & H_2 \\ \vdots & \vdots & \ddots & \vdots \\ H_2 & H_2 & \cdots & H_1 \end{bmatrix} \begin{bmatrix} \tilde{D}_1 \\ \vdots \\ \tilde{D}_N \end{bmatrix}. \tag{4.28}$$

Similarly, (4.26) and (4.27) can be written for all modules in matrix form to obtain:

$$\tilde{I}_o = \begin{bmatrix} H_3 & H_3 & \cdots & H_3 \end{bmatrix} \begin{bmatrix} \tilde{D}_1 \\ \vdots \\ \tilde{D}_N \end{bmatrix} \tag{4.29}$$

and,

$$\begin{aligned} \begin{bmatrix} \tilde{D}_1 \\ \vdots \\ \tilde{D}_N \end{bmatrix} = & \begin{bmatrix} H_4 & 0 & \cdots & 0 \\ 0 & H_4 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & H_4 \end{bmatrix} \begin{bmatrix} \tilde{V_{C1}} \\ \vdots \\ \tilde{V_{CN}} \end{bmatrix} + \begin{bmatrix} H_5 \\ \vdots \\ H_5 \end{bmatrix} \tilde{I}_o \\ & + \begin{bmatrix} -H_5 \\ \vdots \\ -H_5 \end{bmatrix} \tilde{I}_{o,ref}. \end{aligned} \tag{4.30}$$

Let us denote $\tilde{D}_c = H_5(\tilde{I}_o - \tilde{I}_{o,ref})$ in the Laplace domain, as shown in Fig. 4.10. Equations (4.28), (4.29), and (4.30) can be used to obtain:

$$\begin{bmatrix} 1-H_4H_1 & -H_2H_4 & \cdots & -H_2H_4 \\ -H_2H_4 & 1-H_1H_4 & \cdots & -H_2H_4 \\ \vdots & \vdots & \ddots & \vdots \\ -H_2H_4 & -H_2H_4 & \cdots & 1-H_1H_4 \end{bmatrix} \begin{bmatrix} \tilde{D}_1 \\ \vdots \\ \tilde{D}_N \end{bmatrix} = \begin{bmatrix} \tilde{D}_c \\ \vdots \\ \tilde{D}_c \end{bmatrix}. \tag{4.31}$$

Equation (4.31) shows N linear equations in matrix form. By summing up all these equations with together, $\sum_{i=1}^{N} \tilde{D}_i$ is obtained as:

$$\sum_{i=1}^{N} \tilde{D}_i = \frac{N\tilde{D}_c}{[(1-N)H_2H_4 + 1 - H_1H_4]} \tag{4.32}$$

Using the mathematical expressions of $H_1(s)$ and $H_2(s)$, it can be understood that $H_1(s) = (1-N)H_2(s)$. Substututing this result into (4.32) yields $\sum_{i=1}^{N} \tilde{D}_i = N\tilde{D}_c$. Therefore, by considering Fig. 4.10, the open loop transfer function of output current regulation loop $T_{io}(s)$ is given by:

$$\begin{aligned} T_{io}(s) &= \frac{\begin{array}{l}[k_1({v^*}_{C,ref} + k_{p1}(i_{o,ref} + c))s + k_1k_{i1}(i_{o,ref} + c)] \\ \times N\lambda {v^*}_{C,ref}(1-2D^*)\end{array}}{(i_{o,ref} + c)^2 s^2(L_oC_os^2 + R_bc_os + 1)} \\ &= -NH_3H_5. \end{aligned} \tag{4.33}$$

From (4.33), the following results can be obtained regarding the effects of control parameters on phase margin and bandwidth.

Result 1: An increase in the value of k_1, k_{i1} and k_{p1} increases $|T_{io}(j\omega)|$. Therefore, the system bandwidth is increased by increasing k_1, k_{i1}, or k_{p1}. As the magnitude of the open loop transfer function is proportional with k_1, the value of k_1 has the most significant impact on bandwidth among the three existing control parameters.

Result 2: From (4.33), it is observed that increasing k_{p1} and k_{i1} lead to decreases and increases in the phase of the open loop transfer function, respectively. Moreover, k_1 value does not affect the transfer function phase. Therefore, it can be concluded that increasing k_{p1} reduces phase margin. On the ohter hand, increasing k_{i1} leads to increase of the phase margin. Finally, the phase margin is not affected by k_1.

From Fig. 4.10 and (4.33), the closed loop tansfer function of the system can be given by $\frac{-NH_3H_5}{1-NH_3H_5}$. The denominator of the closed loop transfer function is denoted by $F(s)$ and is equivalent to the characteristic polynomial of the system in charging mode. This characeristic polynomial can be expressed as:

$$\begin{aligned} &F(s) = (i_{o,ref} + c)^2(L_oC_os^4 + R_bC_os^3 + s^2) + N\lambda {v^*}_{C,ref} \\ &\times(1-2D^*)k_1\left[({v^*}_{C,ref} + k_{p1}(i_{o,ref} + c))s + k_{i1}(i_{o,ref} + c)\right]. \end{aligned} \tag{4.34}$$

The closed-loop system poles can be calculated by solving $F(s) = 0$. Case Study 2 verifies the validity of (4.33).

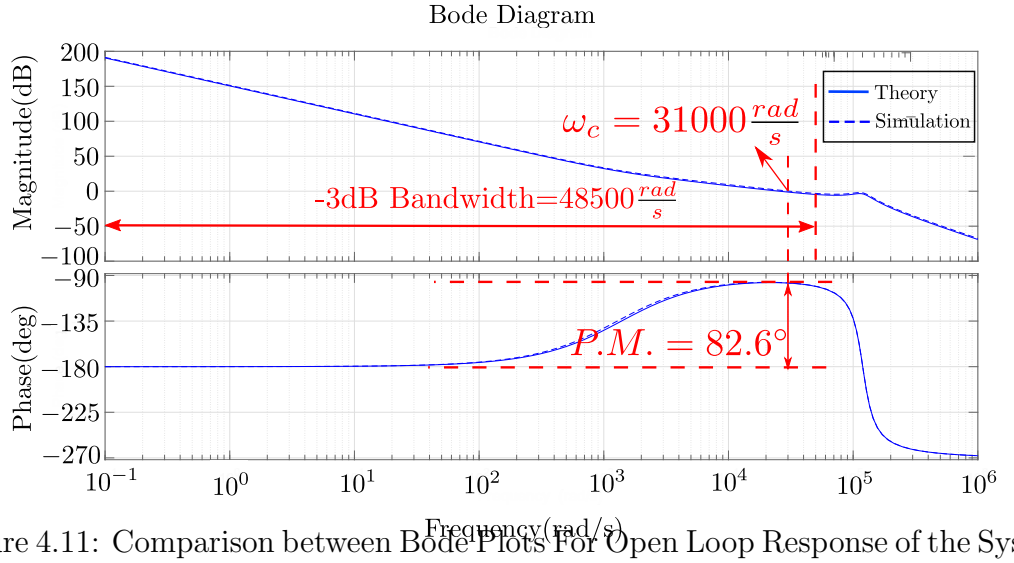


Figure 4.11: Comparison between Bode Plots For Open Loop Response of the System Obtained by Theory and Simulations for Case Study 2

Case Study 2: A system composed of two dual active bridge converters connected in ISOP is assumed in this case study. The ISOP system connects a 200V input voltage source to a 25V output DC source. The tank inductances of DAB modules are 16.7μH and 15μH. Also, the input DC link capacitances of the modules are 11.4μF and 13μF, and the output DC link capacitances are 70μF. Moreover, the turns ratios of the transformers are 20:6 and 20:7 for the two modules. The switching frequency of both modules is 70KHz and R_b =38$m\Omega$. The magnitude and phase associated with the open loop transfer function of the system obtained by theoretical analysis and computer simulations are shown in Fig. 4.11. The control parameters are designed as $k_1 = 150$, $k_{i1} = 11000$, and k_{p1}=0.3. As Fig. 4.11 shows, the achieved phase margin value and -3dB bandwidth level are 82.6 degree and 48500$\frac{rad}{s}$ i.e. 7.72KHz, respectively. As Fig. 4.11 illustrates, the bode plots obtained by simulation results and (4.33) are matched. This verifies the accuracy of (4.33).

Using a method similar to the approach taken for battery charging mode, the open loop transfer function of the system in charging mode is derived as:

$$T_{io,d}(s) = \frac{\begin{array}{l}[-k_2(v^*{}_{C,ref} - k_{p2}i_{o,ref})s + k_2k_{i2}i_{o,ref}] \\ \times N\lambda v^*{}_{C,ref}(1-2D^*)\end{array}}{s^2(L_oC_os^2 + R_bc_os + 1)}. \tag{4.35}$$

The characteristic polynomial of the system in battery discharging mode $F_d(s)$ is given by:

$$\begin{array}{l}F_d(s) = L_oC_os^4 + R_bC_os^3 + s^2 - N\lambda v^*{}_{C,ref}(1-2D^*)k_2 \\ \times\left[(v^*{}_{C,ref} - k_{p2}i_{o,ref})s - k_{i2}i_{o,ref}\right].\end{array} \tag{4.36}$$

As (4.36) shows, the mathematical expression of $F_d(s)$ is very similar to $F(s)$, and $-k_2$, $-K_{p2}$, $-k_{i2}$ have duality with k_1, k_{p1}, and k_{i1}, respectively. Therefore,

substituting control parameters in charging modes by their dual counterparts in discharging mode, *Result 1* and *Result 2* can be extended to discharging mode as well.

4.6.2 Controller Design Procedure in Charging and Discharging Modes

Assuming $i_{o,min} < i_{o,ref} < i_{o,max}$ in battery charging mode and $v_{in,min} < v_{in} < v_{in,max}$, (4.33) suggests that the closed-loop system has its minimum bandwidth when $i_{o,ref} = i_{o,max}, v_{in} = v_{in,min}$. This is because (4.33) suggest that $|T_{io}(j\omega)|$ has its minimum value in this operating point among all possible conditions. Therefore, the system is designed at $i_{o,ref} = i_{o,max}, v_{in} = v_{in,min}$, to ensure fast system dynamics in this case and equivalently, in other cases. At this design operating point, $v^*{}_{C,ref} = \frac{v_{in,min}}{N}$. To design the controller in charging mode, the first step is to select an appropriate value for K_1. For this purpose, $k_{i1} = k_{p1} = 0$ is assumed and a crossover frequency ω_{c1} is selected. Using (4.33) and the assumptions mentioned, the value of k_1 is designed as $k_1 = k^*{}_1$ to achieve a crossover frequency of ω_{c1}. The value of ω_{c1} is selected such that the acheived -3dB bandwidth level of the system is below half of the switching frequency to satisfy nyquist staility criterion. In the next step, $k_{p1} = 0$ is assumed and a target phase margin corresponding to ω_{c1} is set for the system. Using these assumtions, as well as $k_1 = k^*{}_1$ and (4.33), the value of k_{i1} is designed as $k_{i1} = k^*{}_{i1}$ to achieve the target phase margin. In the third step, a small value of $k_{p1} = k^*{}_{p1}$ is selected such that $k^*{}_{p1}(i_{o,ref} + c) << v^*{}_{C,ref}$ and the phase margin of the system is not reduced considerably. The final step is to redesign $k_1 = k^*{}_{1,f}$ to achieve the previously obtained phase margin of ω_{C1}. The controller design procedure discussed above for battery charging mode can be exactly extended to the discharging mode, with designing converter in $i_{o,ref} = i_{o,max}, i_{o,max} < 0, v_{in} = v_{in,min}$ and substituitng k_{p1}, k_{i1}, and k_1 by $-k_{p2}$, $-k_{i2}$, and $-k_2$, respectively. This is due to the similarities between (4.33) and (4.35). The flowchart of the proposed controller design procedure in charging mode is provided in Fig. 4.12. The design flowchart for the discharging mode is the same as the flowchart shown in Fig. 4.12, if the differences mentioned ar taken into account.

Case Study 3: For this case tudy, the same system as in Case Study 2 is assumed and the controller design procedure shown in Fig. 4.12 is implemented. Assuming $i_{o,min}$ =1A, $i_{o,max}$ =10A, $v_{in,min}$ =180V, and $v_{in,max}$ =220V and $N = 2$, the target phase margin and crossover frequency are selected as $\phi_1 = 60^\circ$ and $\omega_{c1} = 50000\frac{rad}{s}$, respectively. In the next step, $i_{o,ref} = i_{o,max}$ =10A, and $v^*{}_{C,ref} = \frac{v_{in,min}}{2}$ =90V are set. Setting $k_{p1} = k_{i1}$ =0, $k_1 = k^*{}_1 = \frac{(i_{o,ref}+c)^2\omega_{c1}\sqrt{(1-L_oC_o{\omega_{c1}}^2)^2+{R_b}^2{C_o}^2{\omega_{c1}}^2}}{N\lambda{v^*{}_{C,ref}}^2(1-2D^*)}$ =706.5 results in a crossover frequency of 50kHz. The phase of $T_{io}(j\omega)$ at $\omega_c = \omega_{c1}$ is equal to $\arctan\frac{v^*{}_{C,ref}\omega_{c1}}{(i_{o,ref}+c)k_{i1}} - \pi - \arctan\frac{R_bC_o\omega_{c1}}{1-L_oC_o{\omega_{c1}}^2}$. Based on this result, a value of $K^*{}_{i1}$ =95420 is required to obtain a phase margin of 60 degrees. Finally, the value of k_p must be selected such that k_{p1} <<5. Therefore, a value of k_p =0.3 is selected. Fianlly, $k_1 = k^*{}_{1,f} = 510$ is set to restore the target crossover frequency. Therefore, the final design is $k_1 = 510, k_{p1} = 0.3$, and $k_{i1} = 95420$.

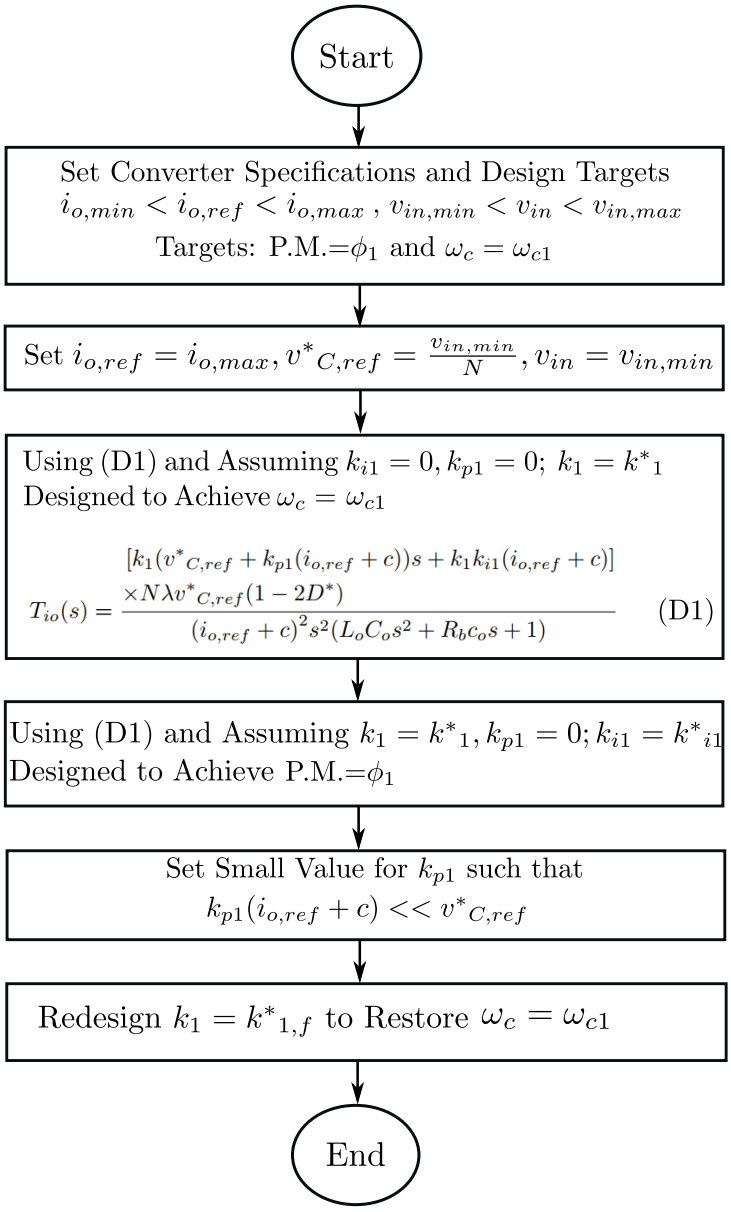


Figure 4.12: Flowchart of Proposed Control Design Procedure in Battery Charging Mode

4.7 Simulation Results with DAB, Flyback, and Full Bridge Converter Modules

In this section, simulation results are provided to verify the effectiveness of the controller proposed in this chapter. The simulation results are provided through simulation scenarios.

Scenario 1: In this simulation scenario, a system composed of two dual active bridge converters connected in ISOP is assumed. The ISOP system connects a 200V input voltage source to a 25V output DC source. The tank inductances of DAB modules are 16.7μH and 15μH. Also, the input DC link capacitances of the modules

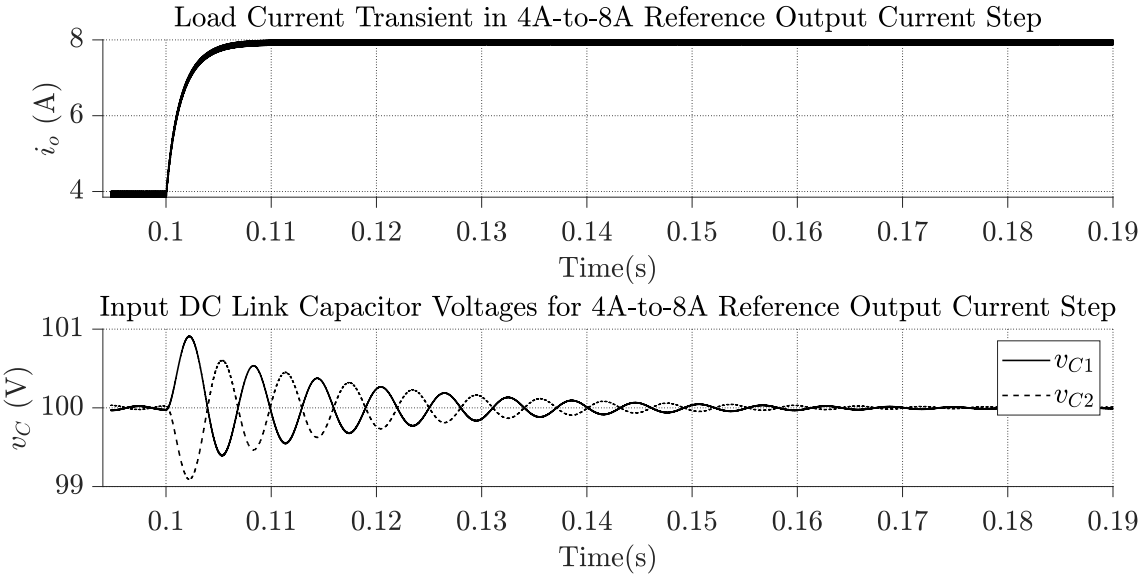


Figure 4.13: System Responses to 4A-to-8A Reference Output Current Step in Simulation Scenario 1 at t=0.1s

are 11.4μF and 13μF, and the output DC link capacitances are 70μF. Moreover, the turns ratios of the transformers are 20:6 and 20:7 for the two modules. The switching frequency of both modules is 70KHz. Fig. 4.13 shows the system transient response for a 4A-to-8A reference load current step. As this figure shows, the input DC-link capacitor voltages for both modules are equal to 100V in steady-state and this verifies the accurate power sharing performance of the proposed controller. Moreover, the maximum deviation of input DC link voltages from 100V is below 1V during the transient period, which can be therefore neglected. Finally, Fig. 4.13 shows that the output current has accurately tracked its reference value and the output current recovery time is 6ms.

From Fig. 4.13, it can be observed that despite parameter mismatches between the two modules in terms of transformer turns rations, DC-link capacitances, and tank inductances, accurate power sharing between is achieved between modules.

Scenario 2:In this scenario, the same system as in the previous simulation scenario is assumed and the reference output current experiences a step from -4A to 4A at t=82ms. Fig. 4.14 shows the system response to this step change. As this figure illustrates, the recovery time for the output current is 3ms and the maximum deviation of input DC link capacitor voltages from their 100V steady state level is just 1V. Therefore, the input DC link voltage transients can be neglected. As Fig.4.14 shows, the controller has been able to provide accurate power sharing between modules in both transient and steady-state conditions.

Scenario 3: This simulation scenario aims to investigate the performance of the proposed controller when a high number of modules are used. For this purpose, a system comprising 10 forward converters connected in ISOP is assumed. The total input voltage is 900V and the reference output voltage is 15V. The load resistance value varies from 0.25Ω to 0.167Ω at t=35ms. The switching frequency is 100KHz.

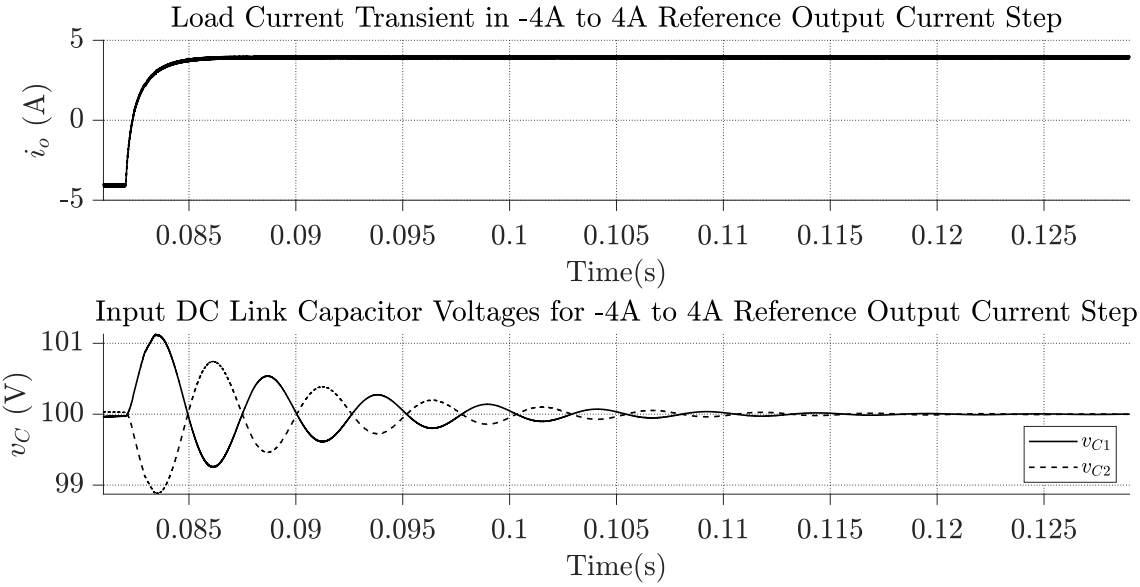


Figure 4.14: System Responses to -4A to 4A Reference Output Current Step in Simulation Scenario 2 at t=0.082s

Numbering forward converter modules 1-10, the input DC link capacitors of modules are 20μF, 25μF, 15μF, 18μF, 20μF, 22μF, 23μF, 19μF, 20μF, and 16μF, respectively. The transformer turns ratios of these modules include 1:0.75, 1:0.75, 1:0.75, 1:0.7, 1:0.72, 1:0.65, 1:0.7, 1:0.65, 1:0.69, and 1:0.68, respectively. Finally, the module inudctor sizes include 56μH, 52μH, 52μH, 56μH, 56μH, 54μH, 59μH, 57μH, 58μH, and 53μH, respectively. For a load resistance step from 0.25Ω to 0.167Ω at t=35ms, the system response is provided in Fig. 4.15. According to this figure, the maximum deviation of input DC link voltage of modules from its reference value i.e. 90V, is 0.22V. Also, as it can be seen in this figure, accurate power sharing is achieved at steady-state. Moreover, the output voltage undershoot is 0.75V and the recovery time is approximately equal to 10 switching cycles. Therefore, a suitable controller performance is achieved using a high number of modules.

Scenario 4: In this simulation scenario, the proposed controller is applied to a system comprising three ISOP flyback converters, which interfaces a 300V input voltage to a resistive load. The input DC link capacitances for the modules are 50μF, 60μF, and 45μF. Also, the magnetization inductances of transformers for all modules is 70μH and the transformers turns rations are 3:1, 3.2:1, and 3.4:1. The output DC link capacitance for each module is also 80μF. The reference output voltage is 10V and the switching frequency is 200KHz. If the system experiences a resistive load step resulting in the load current change from 7A to 10A, the input DC link voltage waveforms for different modules and the output current waveform will be as shown in Fig. 4.16. As tis figure shows, the controller has been able to provide accurate power sharing among the modules and the output current has also tracked its reference signal accurately. According to Fig. 4.16, the overshoot/undershoot level experienced by input DC link capacitor voltages is 0.2 percent, which can be neglected. Also, this figure verifies a fast dynamical response for the output current.

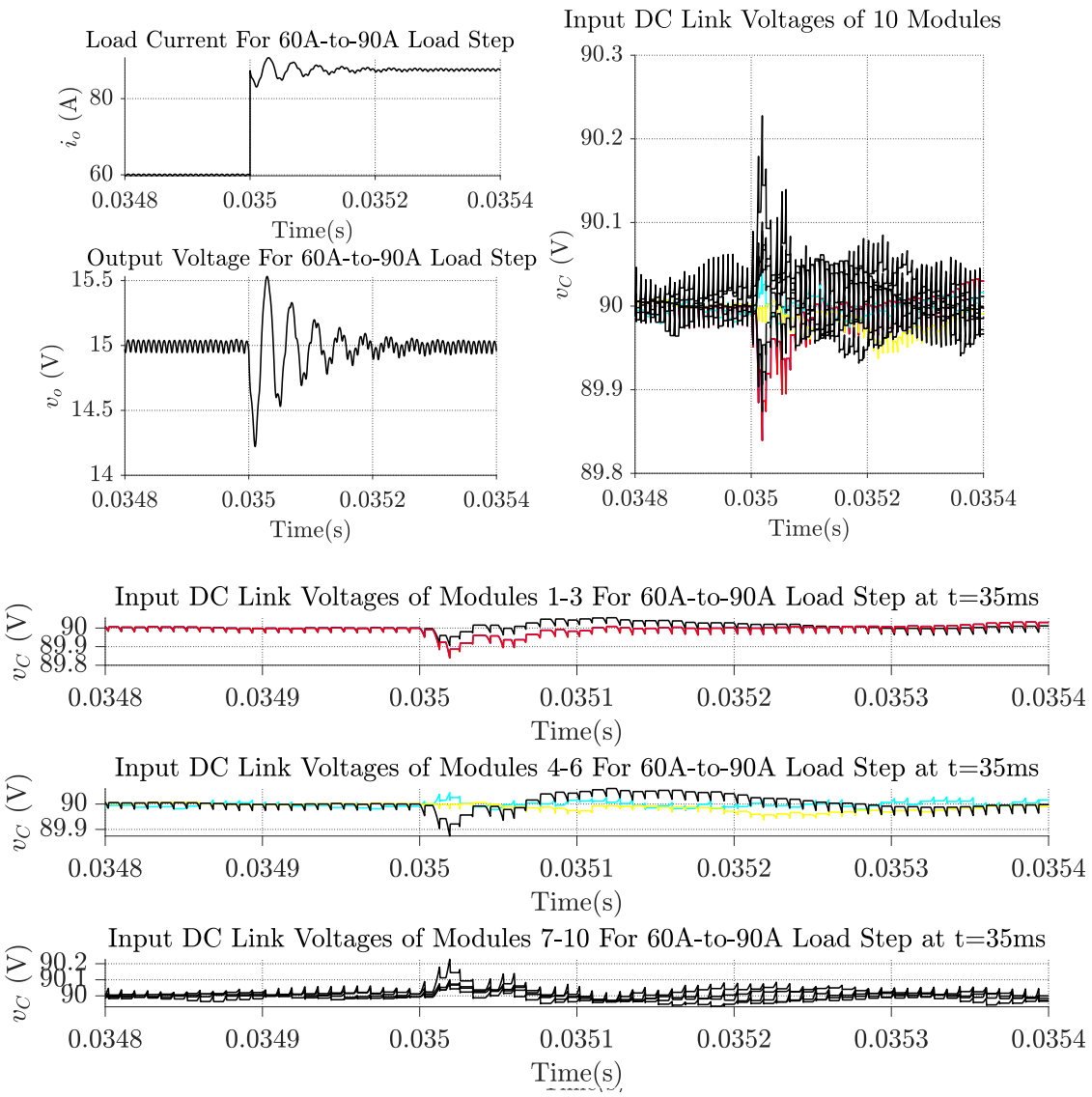


Figure 4.15: System Responses to 60A to 90A Load Current Step in Simulation Scenario 3 at t=0.35s to Verify Controller Performance in a Modular System with 10 Modules, Parameter Mismatches between Modules: Input DC Link Cap. 15μF-25μF, Transformers Turns Ratio 1:0.75-1:0.68, Module Inductors:52 μ-59μ

Scenario 5: In this scenario, two DC-DC converters with a full bridge-based topology [7] are connected in ISOP. This topology is shown in Fig. 4.17. The system has a total input voltage of 320V, input DC link capacitors of 20μF, transformer turns ratios of 0.9:1 and 1.1:1, filter inductances of 300μH, filter capacitances of 1100μF, and a switching frequnecy of 50KHz [7]. This system delivers power to a resistive load and the reference output voltage is 50V [7]. The system response to a 5A-to-10A load current step is provided in Fig. 4.18. This figure verifies accurate power sharing, fast dynamical response, and accurate load current regulation for the proposed controller.

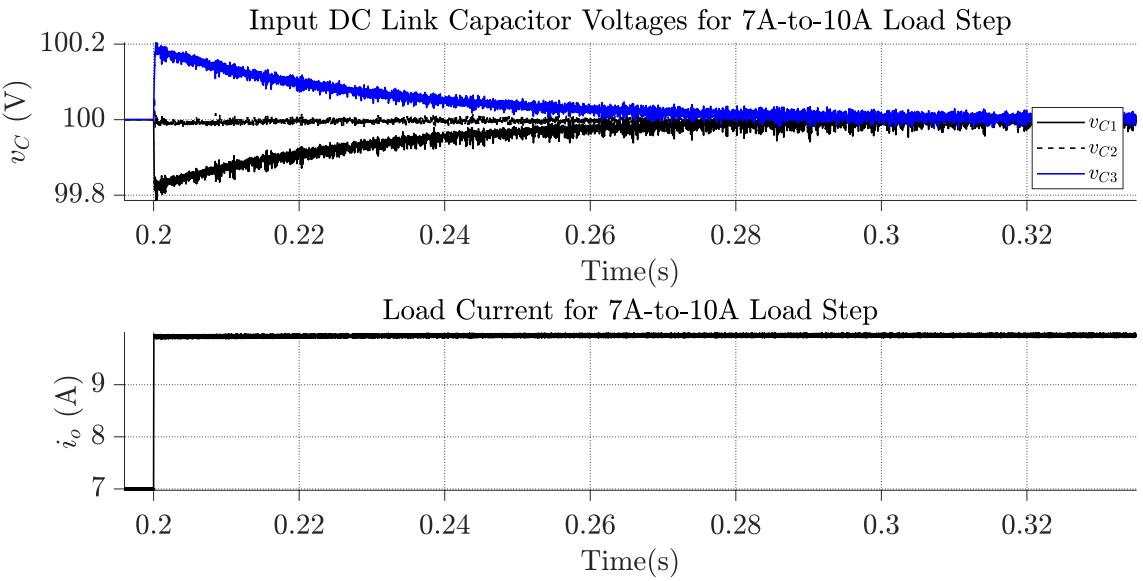


Figure 4.16: System Responses to 7A to 10A Load Current Step in Simulation Scenario 4 with 3 ISOP Flyback Converters

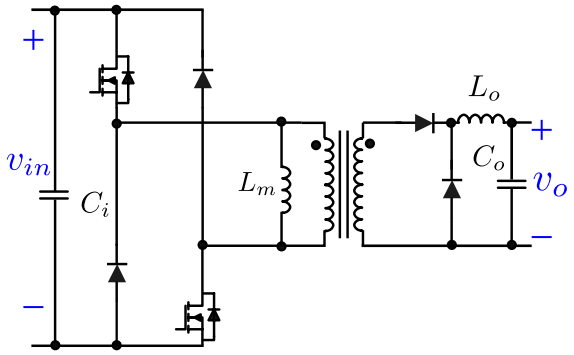


Figure 4.17: Full-bridge Based Converter Topology for A Single Module in Scenario 5 [7]

4.8 Comparison Results with Forward Converter Modules

To evaluate the performance of the proposed controller, a comparison is conducted between the proposed controller and the controller proposed in [6], which uses three forward converters in ISOP configuration connected to a resistive load with system parameters in Table 4.1. The same system is simulated for conducting accurate comparisons in this section. In this system, the load current is changed from 15A to 30A and the dynamics of DC-link capacitor voltages and the output voltage of the converter are compared for both controllers. It is worth mentioning that in this system, resistive loads are assumed. The system parameters for this system are shown in Table 4.1. The waveforms associated with the system response are observable in Fig. 4.19. All waveforms in this figure correspond to the controller

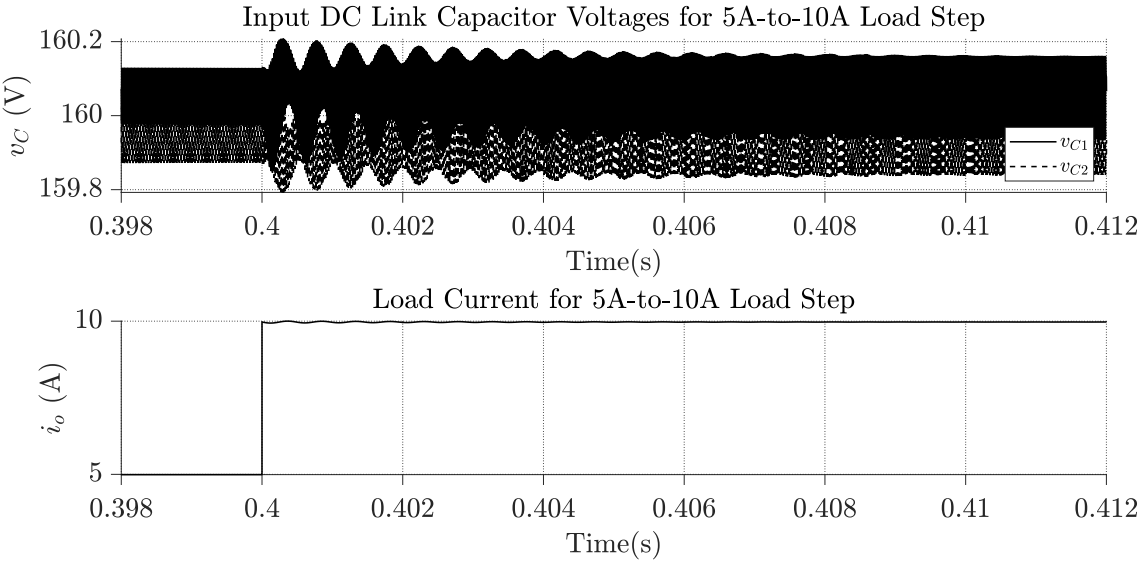


Figure 4.18: System Responses to 5A to 10A Load Current Step in Simulation Scenario 5 with 2 ISOP Full-bridge Based Converters in Fig. 4.17 [7]

Table 4.1: Comparison of the proposed method and [6]

	Proposed	[6]
Input Voltage v_{in} (V)	270	270
Output Voltage v_o (V)	15	15
Switching Frequency f_s (KHz)	100	100
Inductor L (μH)	56	56
Input Capacitor C_i (μF)	20	20
Maximum Load Current $i_{o,max}$ (A)	30	30
Load Current Step ΔI_o (A)	15	15
Output Capacitor $C_o(\mu F)$	200	200
Transfomer Turns Ratios	$\frac{1}{0.75}, \frac{1}{0.75}, \frac{1}{0.65}$	$\frac{1}{0.75}, \frac{1}{0.75}, \frac{1}{0.65}$
Output Voltage Over/Under-shoot $v_{dev,out}$ (V)	0.58	1
Output Voltage Recovery Time $t_{r,out}$ (ms)	0.3	0.2
Input Cap. Voltage Over/Under-shoot $v_{dev,in}$ (V)	0.17	1
Input Voltage Recovery Time $t_{r,in}$ (ms)	0.2	2
Power Mismatch P_e(percent)	0.39	1.5
FOM= $v_{dev,out} \times t_{r,out} \times v_{dev,in} \times t_{r,in}$	0.002	0.6

proposed in this chapter.

To quantitatively compare the proposed controller and [6], a Figure of Merit

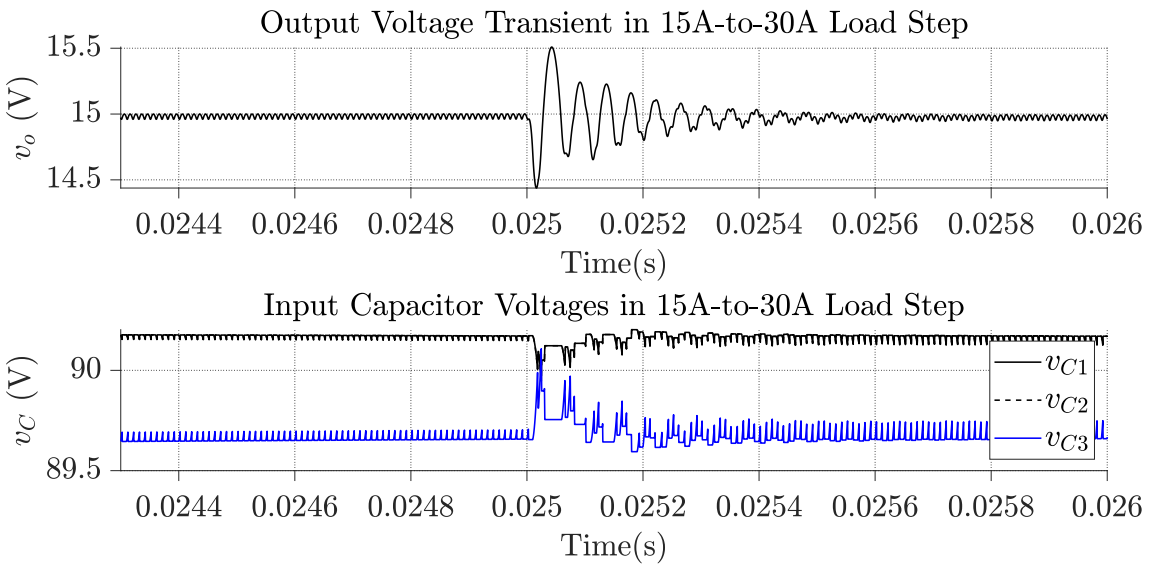


Figure 4.19: System Response to a 15A to 30A Load Current Step Using Proposed Controller and [6]

(FOM) is used. This FOM is defined in Table 4.1 and based on the fact that a better controller performance includes lower voltage overshoots/undershoots in output voltage and DC-link voltage, as well as lower recovery times for these voltages in load transients. As it can be observed, the lower the FOM, the better controller performance is achieved. According to this table, the proposed controller provides a better performance for the same system, compared with [6]. Fig. 4.19 shows that the proposed controller has managed to provide an appropriate power sharing among the modules, as well as providing suitable dynamics for DC-link voltages and output voltage.

The bandwidth and phase margin levels associated with power sharing and output voltage/current regulation control loops directly affect recovery times and overshoot/undershoot levels during transient periods. A higher bandwidth level results in reduced transient state recovery times, while a reduced phase margin limits the maximum bandwidth level with stable system operation [116]. A limited system bandwidth due to reduced phase margin in turn results in slower disturbance rejections by the controller, which is equivalent to higher overshoot levels [116]. Therefore, the proposed controller parameters are readjusted to obtain an output voltage recovery time of 0.2ms, which is identical to [85] and suggests a similar output voltage regulation bandwidth. The performance of the proposed controller is again compared with [85] in Table 4.2. As Table 4.2 illustrates, the output voltage undershoot level is 0.4V using the proposed controller. Also, the maximum input DC-link voltage is 0.32V and the power sharing recovery time is 0.1ms. According to Table 4.2, these values which are obtained with output voltage regulation recovery times identical to [85], are smaller than the values for the same parameters reported in [85]. The system response using the proposed controller in this case is provided in Fig. 4.20.

Table 4.2: Comparison of the proposed method and [6] with Identical Output Voltage Regulation Recovery Times

	Proposed	[6]
Input Voltage v_{in} (V)	270	270
Output Voltage v_o (V)	15	15
Switching Frequency f_s (KHz)	100	100
Inductor L (μH)	56	56
Input Capacitor C_i (μF)	20	20
Maximum Load Current $i_{o,max}$ (A)	30	30
Load Current Step ΔI_o (A)	15	15
Output Capacitor $C_o(\mu F)$	200	200
Transfomer Turns Ratios	$\frac{1}{0.75}, \frac{1}{0.75}, \frac{1}{0.65}$	$\frac{1}{0.75}, \frac{1}{0.75}, \frac{1}{0.65}$
Output Voltage Over/Under-shoot $v_{dev,out}$ (V)	0.4	1
Output Voltage Recovery Time $t_{r,out}$ (ms)	0.2	0.2
Input Cap. Voltage Over/Under-shoot $v_{dev,in}$ (V)	0.32	1
Input Voltage Recovery Time $t_{r,in}$ (ms)	0.1	2
Power Mismatch P_e(percent)	0.39	1.5
FOM= $v_{dev,out} \times t_{r,out} \times v_{dev,in} \times t_{r,in}$	0.0025	0.6

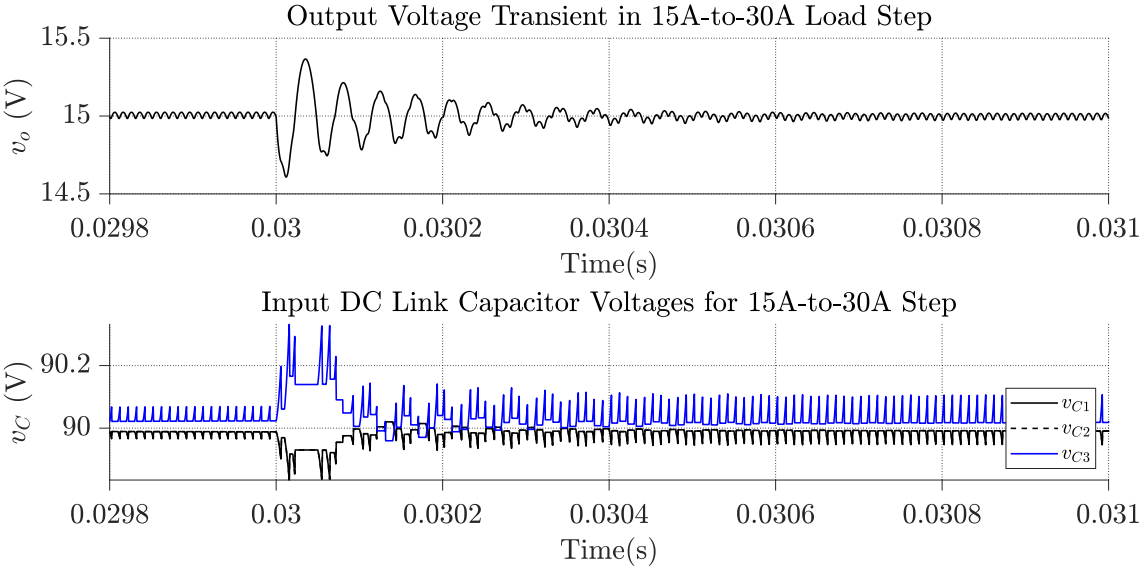


Figure 4.20: System Response to a 15A to 30A Load Current Step Using Proposed Controller and [6] with Identical Output Voltage Recovery Times

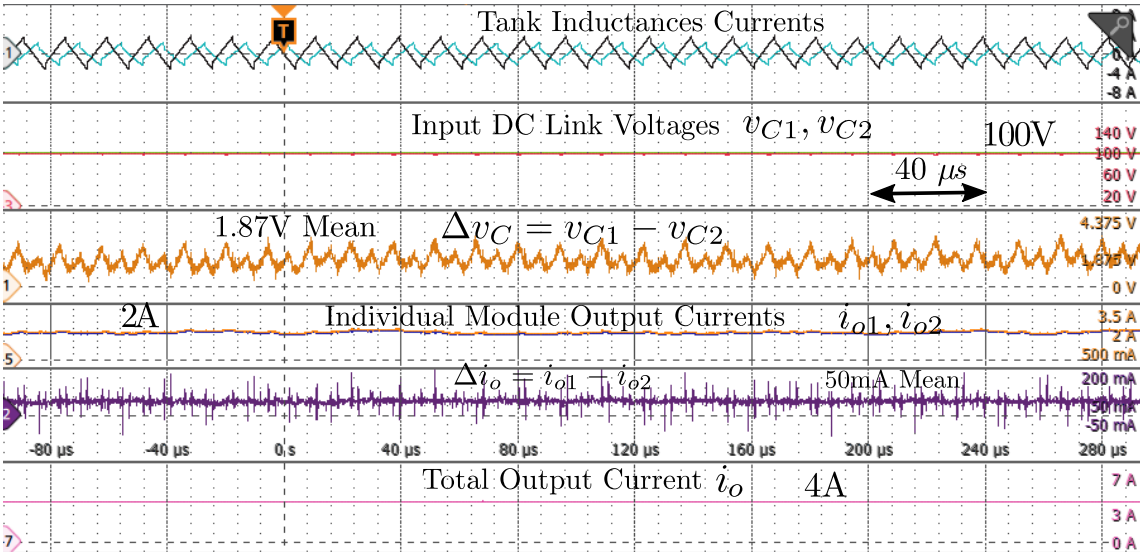


Figure 4.21: Controller Response in Steady State and 4A Reference Output Current. From Top to Bottom: Tank Inductance Currents, Input DC Link Voltages v_{C1} and V_{C2},$\Delta v_C = v_{C1} - v_{C2}$,Individual Module Output Currents i_{o1} , i_{o2}, $\Delta i_o = i_{o1} - i_{o2}$, and Total Output Current $i_o = i_{o1} + i_{o2}$

4.9 Experimental Results with DAB Converter Modules

A system composed of two dual active bridge converters connected in ISOP was built in the laboratory to validate the control approach. The ISOP system connects a 200V input voltage source to a 25V output DC source. The tank inductances of DAB modules are 16.7μH and 15μH. Also, the input DC link capacitances of the modules are 11.4μF and 13μF, and the output DC link capacitances are 70μF. Moreover, the turns ratios of the transformers are 20:6 and 20:7 for the two modules. The switching frequency of both modules is 70KHz.

Each module has one TI TMS320F28335 DSP processor and one separate DSP to implement the controller without any other communication link.

Fig. 4.21 shows the system response when the proposed controller in this chapter is applied to the system and the reference output current $i_{o,ref}$ is 4A. From top to the bottom, this figure shows the tank inductance currents of the 2 modules, input DC link voltages v_{C1} and v_{C2}, $\Delta v_C = v_{C1} - v_{C2}$, Individual module output currents i_{o1} and i_{o2}, $\Delta i_o = i_{o1} - i_{o2}$, and finally total output current $i_o = i_{o1} + i_{o2}$. As the total input voltage is 200V and the difference between the steady state values of v_{C1} and v_{C2} is 1.87V, the power sharing mismatch between the modules is just 0.93 percent of the total transferred power. This power sharing is achieved considering 10 percent, 14 percent, and 16 percent mismatches in tank inductances, input DC link capacitances, and transformers' turns ratios between the two modules. Also, the proposed controller regulates both output currents in 2A and the total output current in 4A, as shown by Fig. 4.21.

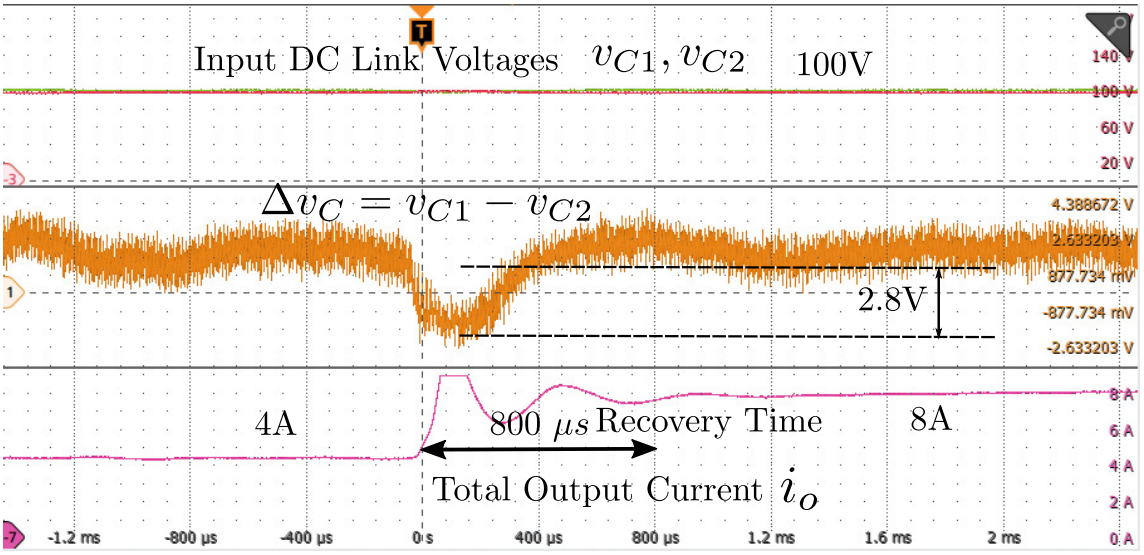


Figure 4.22: Controller Response in 4A to 8A Output Current Reference Step. From Top to Bottom: Input DC Link Voltages v_{C1} and V_{C2},$\Delta v_C = v_{C1} - v_{C2}$, and Total Output Current $i_o = i_{o1} + i_{o2}$

The controller response is shown in Fig. 4.22, for a reference output current change from 4A to 8A. As this figure illustrates, both input DC link voltages are 100V at steady state and the difference between the input DC link voltages changes by a maximum of 2.8V in transients, compared with steady state condition. Moreover, the output current successfully reaches 8A within 800μs.

Fig. 4.23 shows the closed-loop system response to an output current reference step from -4A to -7A. As this figure shows, the output current has successfully tracked its reference signal within 600μs.

Fig. 4.24 shows the system response to a -8A to -5A reference output current step. As this figure illustrates, the output current tracks its reference value after 800 μs. Finally, Fig. 4.25 shows the transient response of the system, when the output reference current is changed from -4A to 4A. As this figure shows, the soft transition control concept has successfully been able to provide the capability of transitions between different power flow directions.

As Fig.4.25 shows, the maximum difference between the DC link capacitor voltages at the input side is 9.6V in a -4A to 4A output current transient. This is equivalent to a power mismach of 4.8 percent of the total output power between the two modules during this transient. Moreover, the identical power sharing between the two modules is achieved after 800μs.

The proposed controller is also applied to a system composed of three ISOP/IPOS DAB converter modules in the laboratory. The new experimental setup includes three ISOP/IPOS DAB converters with nominal tank inductances of 16.7μH, 15μH, and 20 μH. Also, the input DC link capacitances of the modules are 11.4μF, 13μF, and 15.2μF. The output DC link capacitance for all modules is 70μF and the turns ratios of the transformers are 20:6, 20:7, and 20:7 for the three modules. The switching frequency of all modules is 70KHz. The total input voltage is 120V and

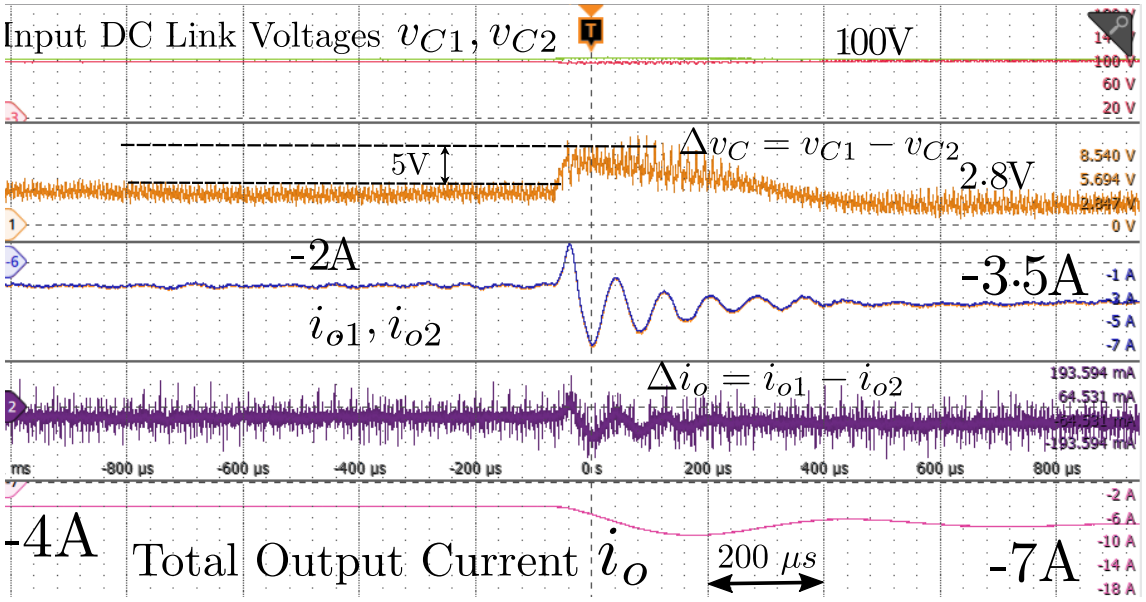


Figure 4.23: Controller Response in -4A to -7A Output Current Reference Step. From Top to Bottom: Input DC Link Voltages v_{C1} and V_{C2},$\Delta v_C = v_{C1} - v_{C2}$, Individual Module Output Currents i_{o1} , i_{o2}, $\Delta i_o = i_{o1} - i_{o2}$, and Total Output Current $i_o = i_{o1} + i_{o2}$

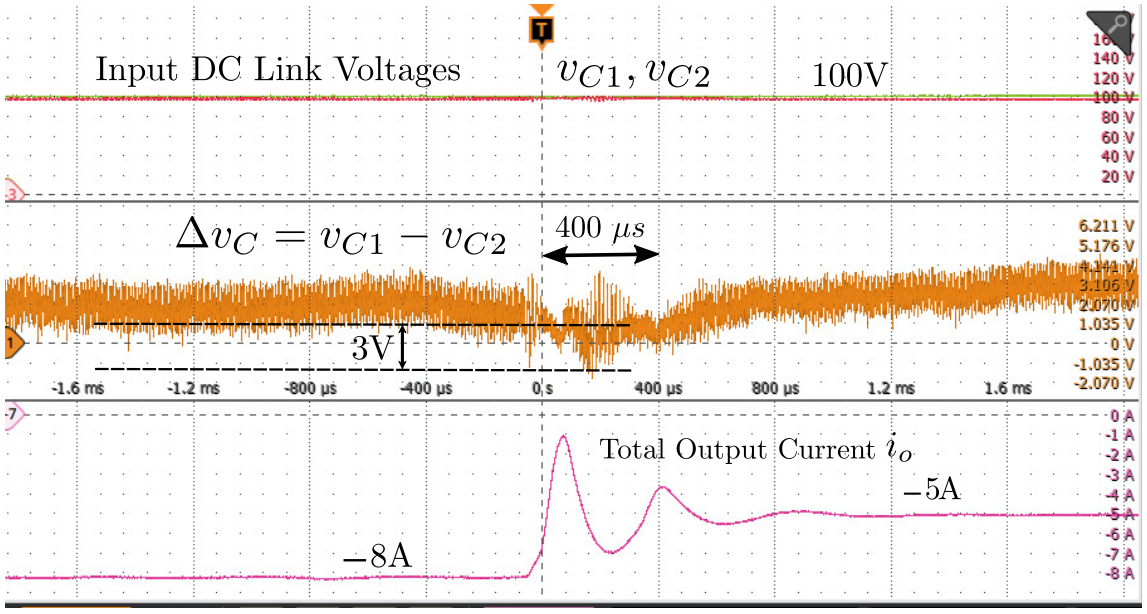


Figure 4.24: Controller Response in -8A to -5A Output Current Reference Step. From Top to Bottom: Input DC Link Voltages v_{C1} and V_{C2},$\Delta v_C = v_{C1} - v_{C2}$, and Total Output Current $i_o = i_{o1} + i_{o2}$

the output voltage is 10V. The output current varies between -12A to 13A. When the reference output current is 6A, the waveforms of input DC link capacitor voltages v_{C1}, v_{C2}, and v_{C3}, as well as the tank inductance currents and total output current in

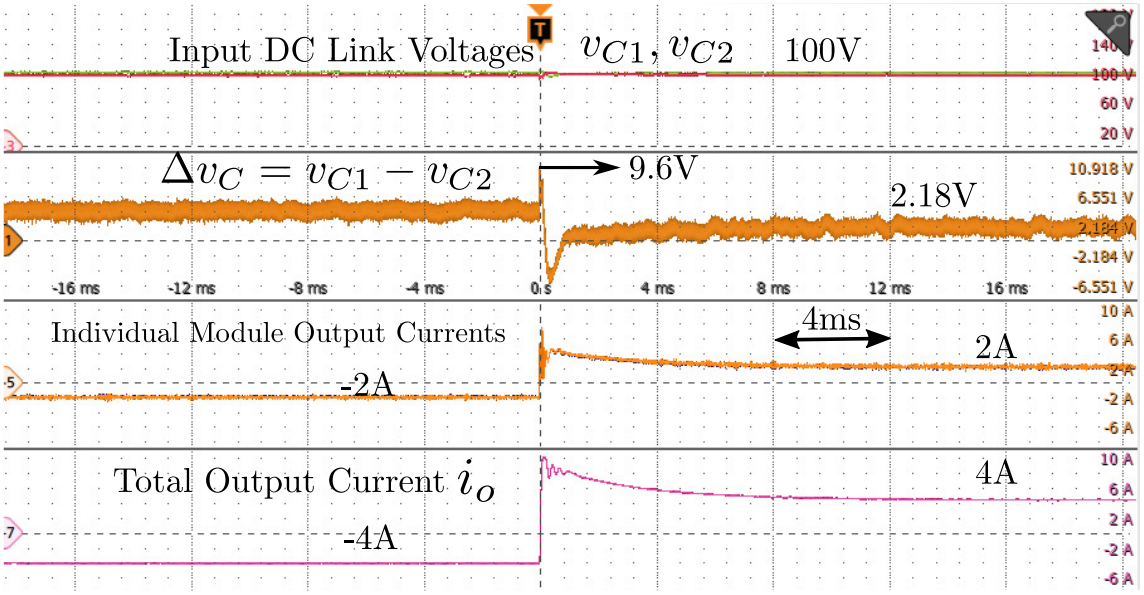


Figure 4.25: Controller Response in -4A to 4A Output Current Reference Step. From Top to Bottom: Input DC Link Voltages v_{C1} and V_{C2},$\Delta v_C = v_{C1} - v_{C2}$, Individual Modules Output Currents i_{o1} and i_{o2}, and Total Output Current $i_o = i_{o1} + i_{o2}$

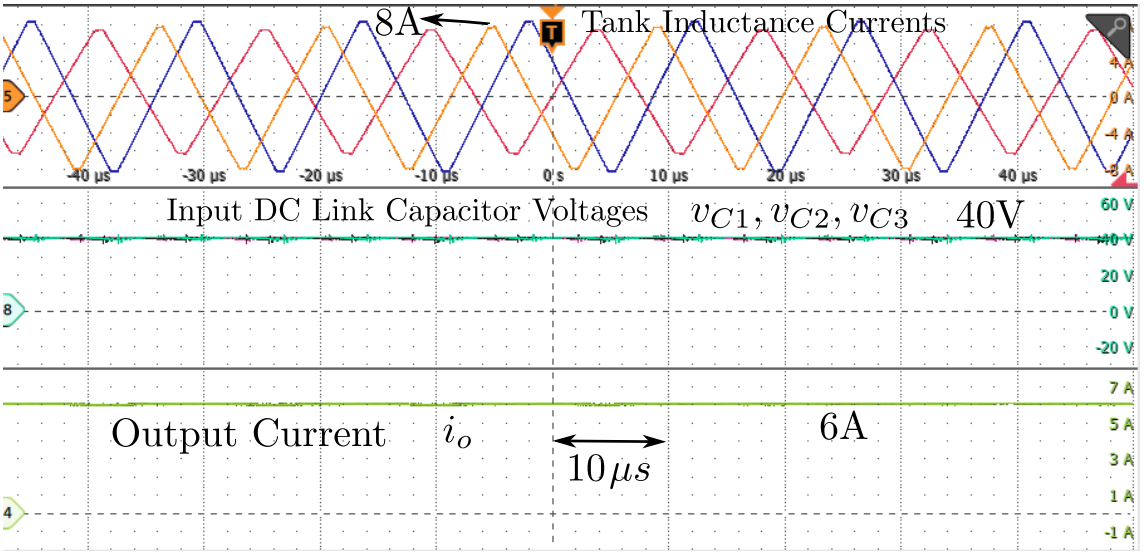


Figure 4.26: Steady-State Response of the Closed-loop System with Three ISOP/IPOS DAB Converters and 6A Reference Output Current.

steady-state are shown in Fig. 4.26. As Fig. 4.26 shows, the controller has provided accurate power sharing among the modules by setting all input DC link capacitor voltages at 40V. Also, the controller has regulated the output current at its reference level of 6A.

If the reference output current experiences a step from 7A to 13A, the system response will be as shwn in Fig. 4.27. As this figure shows, the maximum difference between input DC link voltages in transient period is 1.5V an all modules have the

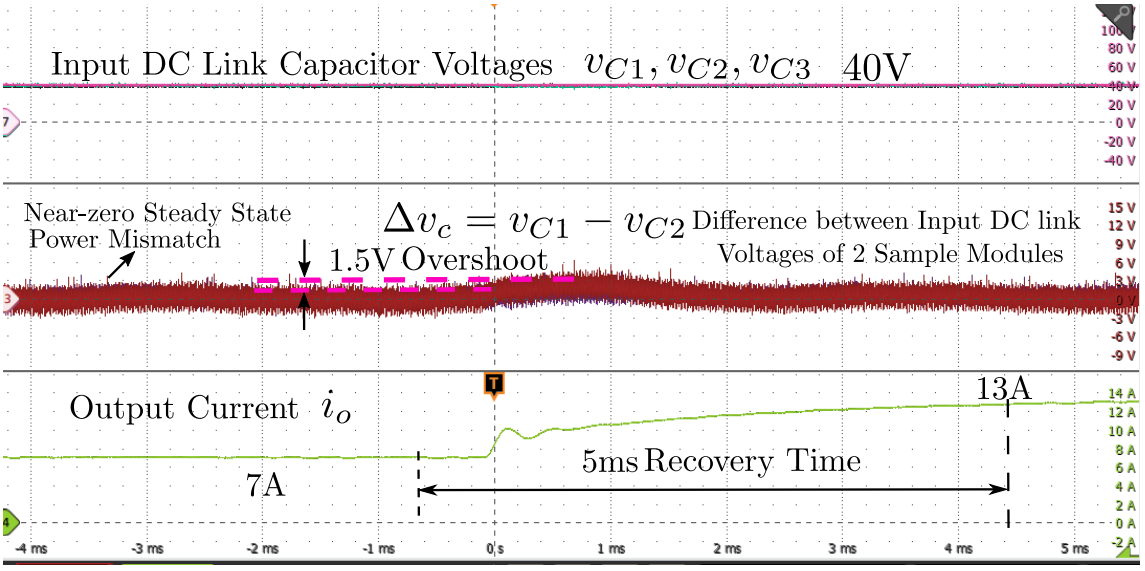


Figure 4.27: Response of the Closed-loop System with Three ISOP/IPOS DAB Converters and 7A-to-13A Reference Output Current Step.

similar input DC link voltage of 40V in steady-state. Finally, the output current recovery time is 5ms.

Fig. 4.28 shows the open loop response of the system, when a common phase shift is applied to all DAB modules such that the total output current is equal to -3A. As seen from this figure, the input DC link capacitor voltages of different modules are 80V, 25V, and 10V and vary considerably. The same issue is valid for the individual module output currents. Therefore, the unbalanced power sharing between the modules in the open loop condition highlights the necessity of a closed-loop control system.

Fig. 4.29. shows the system response of the closed loop system in the discharging mode, when the reference output current is changed from -6A to -12A. As this figure illustrates, there is a near-zero steady-state power mismatch between modules. By comparing Fig. 4.29 to Fig. 4.28, it is understood that the proposed controller has managed to eliminate significant power imbalances between the modules in the open loop condition. This can also be verified from the fact that the individual module output currents are equal in Fig. 4.29. Also, the maximum difference between input DC link voltages of two modules during transient period is 3V and the output current recovery time is 9ms.

Finally, Fig. 4.30. shows the system response of the closed loop system in the discharging mode, when the reference output current is changed from -12A to -6A. The controller has managed to provide accurate power sharing between modules. This can also be verified from the fact that the individual module output currents and input DC link voltages are equal in Fig. 4.30. Also, the output current has accurately tracked its reference signal and the output current recovery time is 11.5ms.

Table 4.3 provides a comparison between the features of the proposed controller and other methods in the literature. As it can be seen, the proposed approach

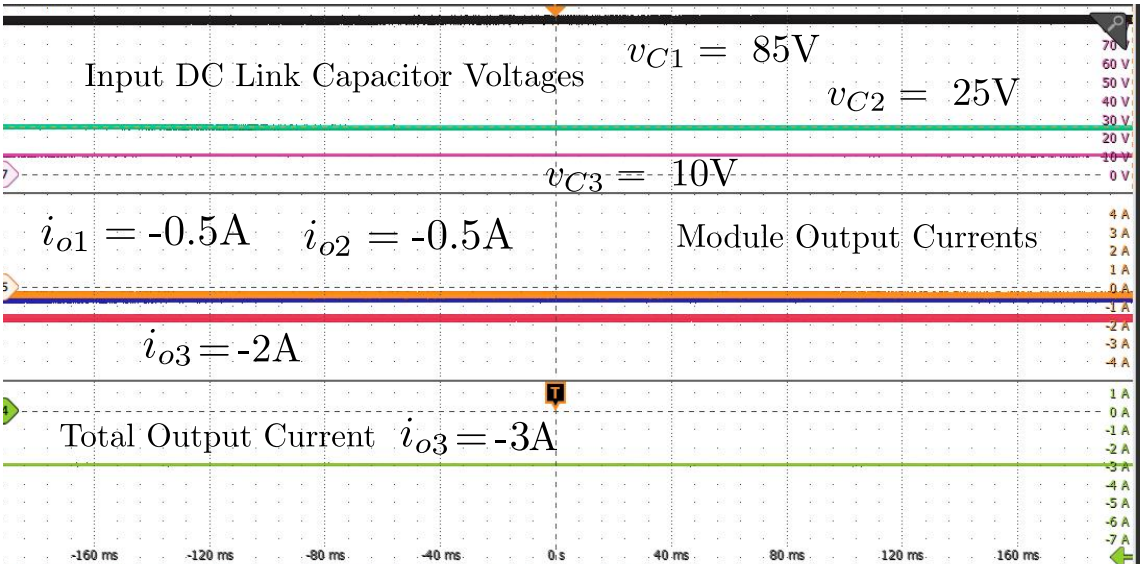


Figure 4.28: Response of the Open loop System with Three ISOP/IPOS DAB Converters and Common Phase Shift Applied to All Modules in Discharging Mode.

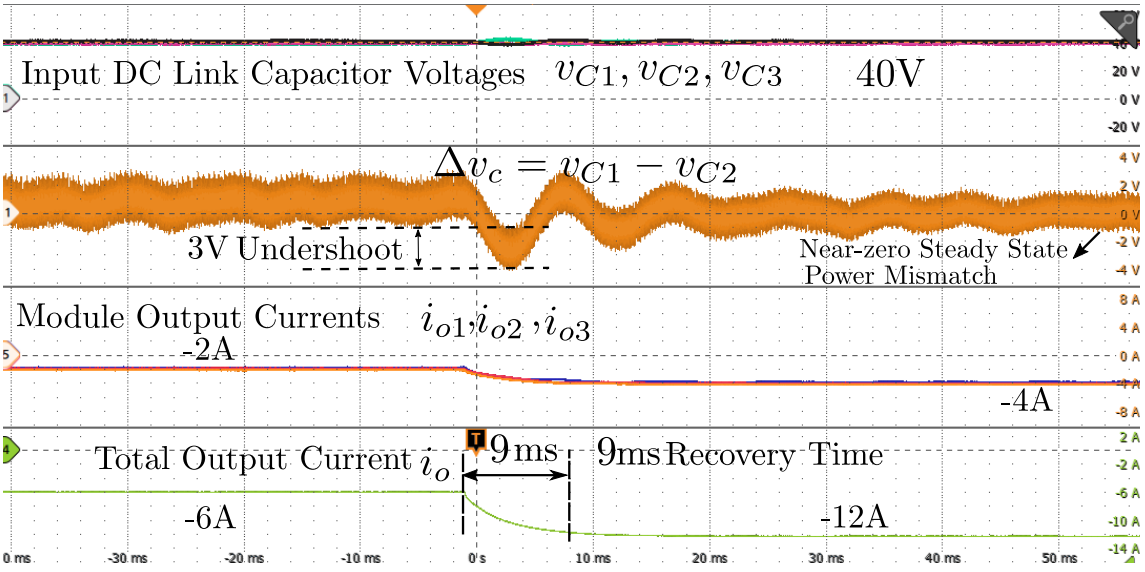


Figure 4.29: Response of the Closed-loop System with Three ISOP/IPOS DAB Converters and -6A to -12A Reference Output Current Step.

is a distributed controller which avoids extra communications among the modules. Therefore, it results in a system with a higher level of reliability.

Another feature of the proposed controller is that it is general and can be applied to any converter topology and it does not require system model or parameters. Otherwise, the system may be prone to instability or degraded dynamical response. In this chapter, the controller was applied to the DAB converter in simulations and experiments, and to forward converter for comparisons with [6] in Fig. 4.19 and Fig. 4.20. Finally, the number of sensors required to implement a controller is important

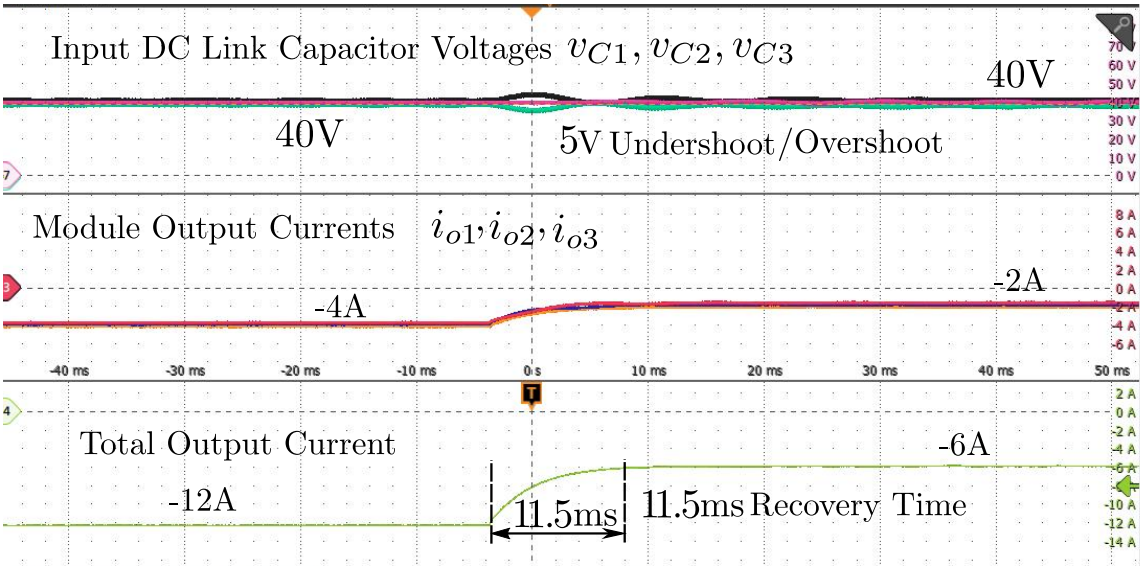


Figure 4.30: Response of the Closed-loop System with Three ISOP/IPOS DAB Converters and -12A to -6A Reference Output Current Step.

Table 4.3: Comparison of the proposed method and Other Existing Methods From Method Features Point of View

	This Work	[1]	[10]	[4]	[5]
Distributed	Yes	No	No	Yes	Yes
Not Limited to One Topology	Yes	Yes	Yes	No	No
Converter Dynamical Model Implemented by Control Law	No	No	No	No	Yes
Sensors Per Module	2	3	3	3	2

because an increased number of sensors can increase the cost of the system. Moreover, sensors may be required to measure high voltage or high frequency signals, which might impose practical limitations on the system design.

In addition to the features already mentioned, the proposed controller can provide accurate power sharing among modules in the presence of parameter mismatches among them. This is shown in the simulation and experimental results sections. Concluding this section, experimental results were provided to show the effectiveness of the proposed controller and the features of the proposed control method were compared with other existing methods in the literature.

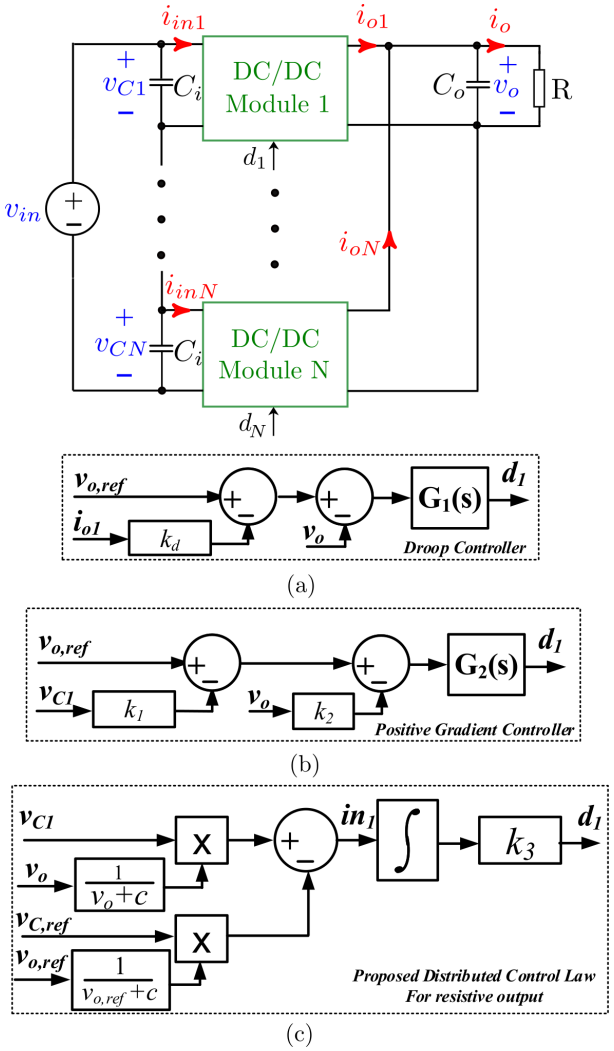


Figure 4.31: Schematic of Modular ISOP/IPOS DC-DC Converters (a) Conventional Droop Controller [7] (b) Positive Output Voltage Gradient Controller [16] (c) Proposed Controller in This Chapter

4.10 Comparison of Proposed Controller Features with Other Existing methods

This section presents information regarding some of the features of the proposed controller and compares them with other existing methods, based on mathematical grounds. Fig. 4.31 shows the schematic of N DC-DC converter modules connected in ISOP, along with the proposed control diagrams for conventional droop controller [7], positive output voltage gradient controller [16], and the proposed controller in this chapter. The modular power conversion system in this figure transfers power to a resistive load.

Droop Controller: Fig. 4.31(a) shows the block diagram of a conventional droop controller. As the input signal processed by $G_1(s)$ to generate the duty cycle has a DC constant value at steady-state condition, $G_1(s)$ has to have a zero pole

for accurate reference traking according to internal model principle. Also, at steady state, the input signal of $G_1(s)$ must have a zero value due to the zero poles of this transfer function. Therefore, the droop controller makes the following equation valid at steady-state for modules x and y:

$$v_{o,ref} - V_o - k_d I_{ox} = v_{o,ref} - V_o - k_d I_{oy} = 0. \tag{4.37}$$

In (4.37), I_{ox} and V_o denote the steady-state values for the x-th module output current and output voltage, respectively. Equation (4.37) suggests that for two arbitrarily-chosen modules of x and y, $I_{ox} = I_{oy} = I_{ss}$ with I_{ss} denoting the output current level for each module at steady-state. This condition and KCL in for the load node in Fig. 4.31 yield to:

$$I_{o1} + I_{o2} + ... + I_{oN} = NI_{ss} = \frac{V_o}{R}. \tag{4.38}$$

Equation (4.38) suggests $I_{ss} = \frac{V_o}{RN}$. Also, Equation (4.37) shows that $I_{ss} = \frac{v_{o,ref} - V_o}{k_d}$. These two results yield:

$$V_o = \frac{v_{o,ref}}{1 + \frac{k_d}{RN}}. \tag{4.39}$$

Equation (4.39) shows that $V_o \neq v_{o,ref}$. In other words, using the droop controller, there is always a steady-state error for the output voltage. In order to minimize this error, the condition $k_d << RN$ must be valid for all load conditions according to (4.39). For high load current levels or identically low R values, this issue implies the essence of using small values for k_d. This is while according to Fig. 4.31(a), k_d is the droop coefficient and the coefficient of an individual module output current in the control law. Therefore, a small k_d value degrades the power sharing performance of the controller, as the duty cycle of a single module is less sensitive to changes in its output current, or equivalently, the amount of power it transfers. In this regards, if the output current of a specific module gets larger than the other modules, less modifications will be made to its duty cycle, resulting in either a slower power sharing dynamics, or degraded power sharing at steady-state. To quantitatively show the effect of a small k_d on power sharing dynamics, it is assumed that each module in Fig. 4.31 is a DAB converter and the droop controller in Fig. 4.31(b) is applied. According to (6) and by writing KCL in the input side for two arbitrarily-selected modules of x and y, the following equation is obtained:

$$C_i \frac{dv_{Cx}}{dt} + \lambda d_x(1 - d_x)v_o = C_i \frac{dv_{Cy}}{dt} + \lambda d_y(1 - d_y)v_o. \tag{4.40}$$

It is assumed that the nominal parameter values for all modules include D^* for duty cycle, ${v_C}^*$ for the input DC-link voltage, i_{os} for output current of an individual module, and ${v_o}^*$ for the output voltage. It is also assumed that all modules operate around this nominal operating point and each parameter can be written as a sum of a large-signal DC value, and a small-signal component. This way, the equations $d_x = D^* + \tilde{d_x}$, $v_{Cx} = {v_C}^* + \tilde{v_{Cx}}$, $i_{ox} = i_{os} + \tilde{i_{ox}}$, and $v_o = {v_o}^* + \tilde{v_o}$ can be written

for module x. Defining $\Delta v_C = \tilde{\Delta v_C} = v_{cx} - v_{cy}, \Delta i_o = \tilde{\Delta i_o} = i_{ox} - i_{oy}$, and $\Delta d = \tilde{\Delta} d = d_x - d_y$, as well as (4.40) result in:

$$C_i \frac{d\Delta v_C}{dt} = C_i \frac{d\tilde{\Delta v_C}}{dt} = \lambda {v_o}^* (2D^* - 1)\Delta d. \tag{4.41}$$

By linearizing (4.11) around the operating point, $\tilde{i_{ox}}$ is derived as:

$$\tilde{i_{ox}} = \lambda {v_C}^* (1 - 2D^*)\tilde{d_x} + \lambda (D^* - {D^*}^2)\tilde{v_C}. \tag{4.42}$$

Using (4.42), Δi_o can be derived as:

$$\tilde{\Delta i_o} = \lambda {v_C}^* (1 - 2D^*)\tilde{\Delta} d + \lambda (D^* - {D^*}^2)\tilde{\Delta v_C}. \tag{4.43}$$

Finally, from the control law in Fig. 4.31(a), $\Delta D(s)$ in Laplace domain is obtained as:

$$\Delta D(s) = -k_d \Delta I_o(s) G_1(s). \tag{4.44}$$

Using (4.41), (4.43), and (4.44) leads to:

$$\Delta v_C(s) = \frac{-C_i \Delta v_C(0)}{-C_i s + \frac{\lambda^2 {v_o}^* (1-2D^*) k_d G_1(s)(D^* - {D^*}^2)}{1 + \lambda {v_C}^* (1-2D^*) k_d G_1(s)}} \tag{4.45}$$

where, $\Delta v_C(0)$ is the initial difference between the input DC-link voltages of modules x and y. The condition $k_d << RN$ required for appropriate voltage regulation imposes selecting a small k_d value for load steps dealing with low R values. From (4.45), it can be seen that the system poles associated with power sharing dynamics become zero in case $k_d \approx 0$. Therefore, selecting a small k_d value to achieve appropriate output voltage regulation results in degradation of power sharing dynamics.

Positive Output Voltage Gradient Method: The block diagram of the control system associated with output voltage gradient method is observable in Fig. 4.31(b). A method similar to what was already used for droop controllers in this chapter can be followed, to show that $V_o = \frac{v_{o,ref} + k_1 \frac{v_{in}}{N}}{k_2}$. As this condition shows, $V_o \neq v_{o,ref}$. To obtain acceptable voltage regulation, $k_2 \approx 1, k_1 << k_2$. Using the same approach used above for dynamic analysis of droop controllers, it can be shown that the system poles associated with power sharing are the roots of $C_i s + (1 - 2D^*)\lambda {v_o}^* G_2(s) k_1 = 0$. As it can be seen, if $k_1 \approx 0$, then the system pole will become near zero. Therefore, the condition $k_1 << 1$ needed to meet voltage regulation requirements, reduces power sharing dynamics.

Proposed Controller: This part discusses different aspects of the proposed controller for resistive loads. According to the concepts already discussed, there is just one power flow direction from the input side to the load for resistive loads. Also, for resistive loads, the goal is to regulate the output voltage instead of the output current. Therefore, the control law in equation (1) should be rewritten as:

$$d_j = k_3 \int \left(\frac{v_{Cj}}{v_o} - \frac{v_{C,ref}}{v_{o,ref}} \right) dt \tag{4.46}$$

Table 4.4: Comparison of the proposed method and [7]

	Proposed	[7]
Input Voltage v_{in} (V)	320	320
Output Voltage v_o (V)	50	50
Switching Frequency f_s (KHz)	50	50
Inductor L (μH)	300	300
Input Capacitor C_i (μF)	20	20
Maximum Load Current $i_{o,max}$ (A)	10	10
Load Current Step ΔI_o (A)	5	5
Output Capacitor $C_o(\mu F)$	1100	1100
Transfomer Turns Ratios	$\frac{0.9}{1}, \frac{1.1}{1}$	$\frac{0.9}{1}, \frac{1.1}{1}$
Module Output Current Over/Under-shoot $i_{dev,out}$ (A)	0.07	0.25
Average Module Output Current Recovery Time $t_{r,out}$ (ms)	3.35	17
Power Mismatch P_e(percent)	0	0

,in which d_j is the duty cycle applied to the j-th module and the block diagram of the controller is shown in Fig. 4.31(c).

In this part, the voltage across the input DC link capacitor of module i at steady-state is denoted by V_{Ci}. Moreover, the output voltage level at steady-state is denoted by V_o. The integrator included in the proposed controller, which is observed in Fig. 4.31(c) and expressed by (4.46), results in $\frac{V_{Ci}}{V_o} = \frac{V_{Cj}}{V_o} = \frac{v_{C,ref}}{v_{o,ref}}$ for modules i and j. In other words, $V_{Ci} = V_{Cj}$ and the power sharing is achieved by the controller. This is while KVL in the input side of the circuit along with power sharing imply $V_{Ci} = V_{Cj} = \frac{v_{in}}{N}$. Also, the output voltage is regulated at $V_o = v_{o,ref}\frac{V_{Ci}}{v_{C,ref}} = v_{o,ref}\frac{v_{in}}{Nv_{C,ref}}$. This result shows that to achieve accurate output voltage regulation i.e. $V_o = v_{o,ref}$, the condition $v_{C,ref} = V_{Ci}$ must be met. Therefore, similar to (2), $v_{C,ref}$ is obtained as:

$$v_{C,ref} = k_{p1}(v_o - v_{o,ref}) + k_{i1}\int (v_o - v_{o,ref})dt. \tag{4.47}$$

As illustrated above, $V_o = v_{o,ref}$ if and only if, $v_{C,ref} = V_{Ci}$. Therefore, the accurate value for $v_{C,ref}$ can be automatically found using applying a PI control loop to $v_o - v_{o,ref}$.

Using the same methodology presented for droop controller, it can be shown that the system pole associated with power sharing dynamics is expressed by $\frac{-{v_C}^*(1-2D^*)k_3}{D^*(1-D^*){v_o}^*}$. As this result shows, the real value of the pole decreases by increasing k_3, resulting in faster system responses for power sharing. As a conclusion to this section, the proposed controller in this chapter enables accurate output voltage regulation and power sharing simultaneously and independently.

Simulation Case Study: In this simulation case study, the performance of the proposed controller is compared with inverse droop controller [7]. A system composed of two ISOP full bridge-based converters with total input voltage of 320V,

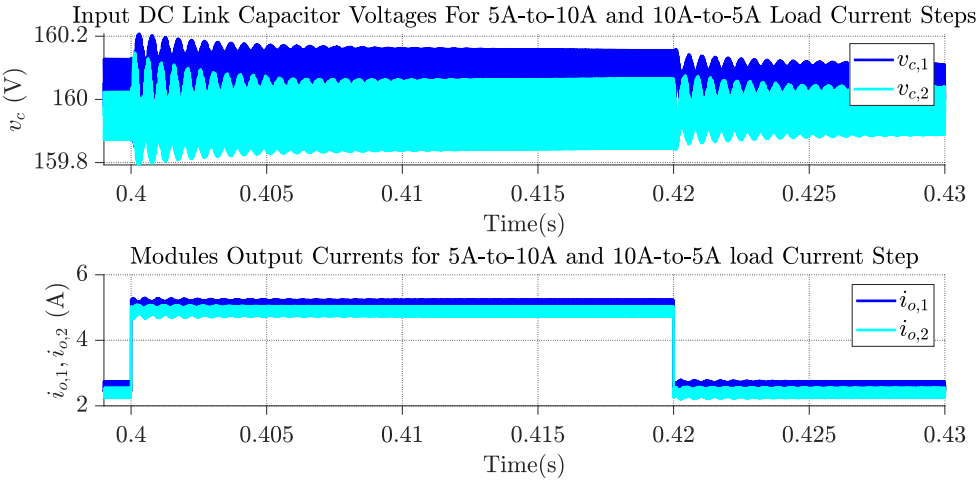


Figure 4.32: Simulation Results for Comparison between the Proposed Controller and Inverse Droop Controller in [7]

input DC link capacitors of 20μF, transformer turns ratios of 0.9:1 and 1.1:1, filter inductances of 300μH, filter capacitances of 1100μF, and switching frequnecy of 50KHz is assumed [7]. This system delivers power to a resistive load and the reference output voltage is 50V [7]. For two consecutive load steps from 10Ω to 5Ω and vice-versa, the load transient response of the proposed controller in this chapter is shown in Fig. 4.32. Table 4.4 shows the controller performance indices and system parameters for the proposed controller and inverse droop controller in [7]. As Table 4.4 shows, overshoot/undershoot levels and recovery times for the module output currents are smaller using the proposed controller, compared with [7]. Also, Fig. 4.32 shows that the proposed controller has managed to provide accurate current regulation and power sharing independently and without trade-offs.

Chapter 5

Application of Proposed Distributed Controller in Other Modular Configurations and an Analysis Framework

In the previous chapter, a decentralized control framework was introduced to tackle control challenges associated with stage 1 converters of a data center, if ISOP or IPOS configuration is used to implement this stage. The control challenges for ISOP DC-DC converters, including appropriate power sharing, fast dynamics, bidirectional power flow, and system stability were also discussed. As it was stated in Chapter 4, the modular configuration used to implement stage 1 converters depends on their voltage and current ratings, which in turn is a function of the data center power management architecture. Motivated by this fact, this chapter extends the application of the control system proposed in Chapter 4 to other modular configurations. Throughout this chapter, the special focus is on ISOS DC-DC converters and their specific control challenges. The current chapter also provides a general control framework applicable to various modular configurations. Finally, an analysis framework for battery-connected ISOS DC-DC converters is also presented.

As mentioned in Chapter 1, some of the challenges associated with ISOS DC-DC conversion systems include appropriate power sharing among modules [89, 90, 91], stability issues [89], system modularity [94, 95, 96, 97, 98], and dynamics [99]. To solve these challenges, this chapter extends the application of the distributed control system introduced in chapter 4, to other modular configurations specially the Input-Series Output-Series (ISOS) structure. In this chapter, the roots of system instability in ISOS DC-DC converters are investigated and it is figured out that the resonances between the input and output DC-link capacitors are the reason behind the stability issues. Next, the stability problems are resolved by inserting an extra term in the control law, in the process of controller extension from Chapter 4. This new term damps the oscillations between input and output DC link capacitors in an ISOS system. It also stabilizes the system and enhances the dynamical response of the system.

Chapter 5 also presents a framework to analyze closed-loop ISOS DC-DC converters. The proposed framework is applicable to all converter topologies and controllers. It also provides clear insights about the stability issues in ISOS converters, by obtaining input and output impedance, as well as gain transfer functions for every individual module in the closed-loop system. To calculate these transfer functions for a specific module, the effects of other modules are also considered. The obtained transfer functions gives insights about system dynamics and stability. It is worth mentioning that the proposed controller increases system modularity using a distributed approach instead of centralized methods. The system dynamics and power sharing among the modules are also improved by using the division operator in the control law, which will be discussed further in the chapter.

The proposed framework in this chapter for ISOS converters is applied to ISOS dual active bridge converters, with the control system introduced in Chapter 4. It is shown that applying this controller to ISOS DC-DC converters leads to no trade-offs between input and output voltage sharing. The control system also supports the operation of the converters in both power flow directions. Also, the proposed controller does not require to use the converter models and parameters, improves power sharing and system dynamics, and finally does not increase the cost and complexity of the system by avoiding any extra auxiliary component.

5.1 Chapter Challenges, Literature Review, and Contributions

5.1.1 Challenges

The architecture of the power management system of a data center is shown in Fig. 5.1, in which the modular DC-DC conversion stage i.e. stage 1 is highlighted by yellow color. In the current chapter, it is assumed that stage 1 DC-DC converters are connected using modular Input-Series-Output-Series (ISOS) configuration.

Most of control challenges associated with ISOS converters are similar to ISOP and IPOS DC-DC converters. These challenges include power sharing, low sensitivity to intermodular parameter mismtaches, and fast dynamics. However, stability requirements have differences in ISOS DC-DC converters. The schematic of an ISOS DC-DC conversion system is shown in Fig. 5.2.

In an ISOS DC-DC conversion system, there exists an inherent positive feedback phenomenon which can lead to instability. For simplicity, it is assumed that in Fig. 5.2,there are just 2 ISOS modules i.e. N=2. Assuming that at a specific switching cycle, the input DC link voltage of module 1 denoted by $v_{in,1}$ is increased. This step is marked as (1) in Fig. 5.2.The input DC link voltage increase in module 1 requires power absorption from the output node of module 1, leading to a decrease in output voltage of the module $v_{o,1}$. This output voltage decrease is marked by step (2) in Fig. 5.2.Since N=2, according to KVL, $v_{o,1}+v_{o,N} = v_{bat}$ in which v_{bat} is the constant battery voltage. According to this fact, a decrease in $v_{o,1}$ results in an increase in $v_{o,N}$. This step is marked as (3) in Fig. 5.2. The increase of the output voltage of

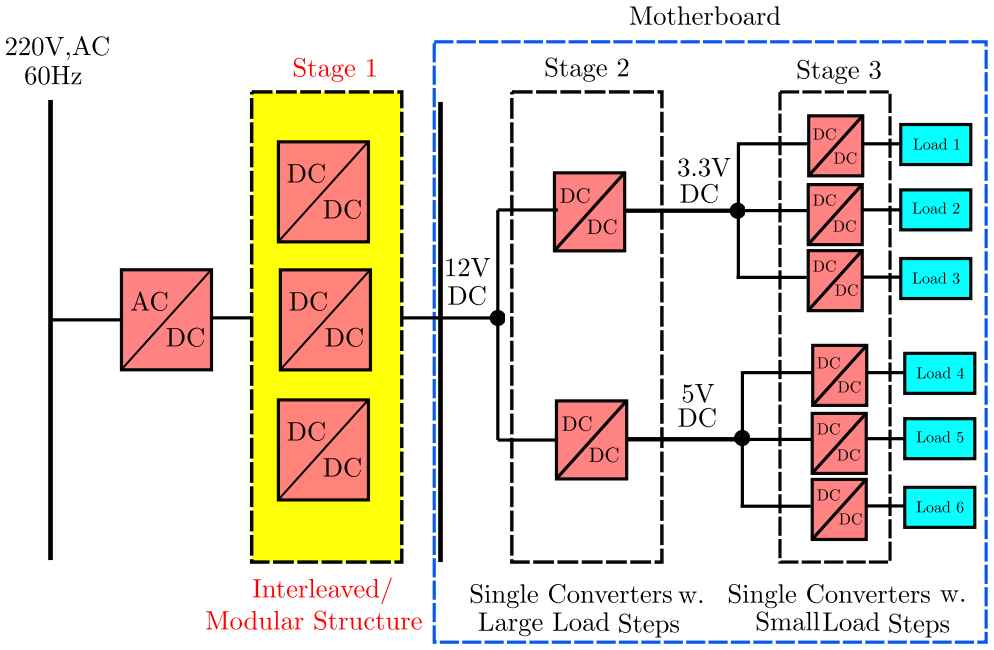


Figure 5.1: Modular DC-DC Conversion Stage i.e. Stage 1 Highlighted by Yellow in Data Center Power Management System

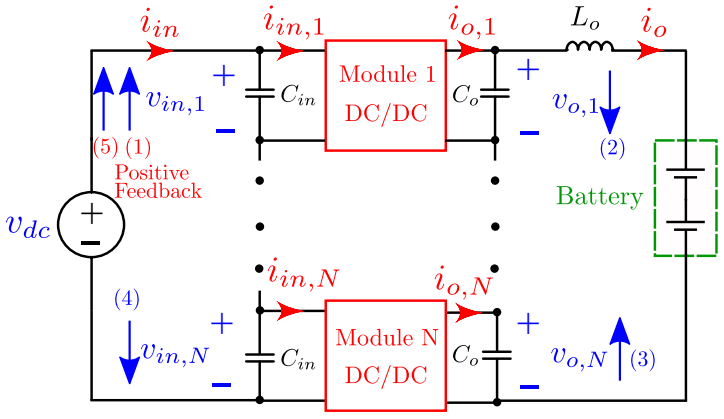


Figure 5.2: Modular Input-Series-Output-Series (ISOS) DC-DC Conversion System

module N demands power absorption from th input terminal of the same module, leading to reduction of $v_{in,N}$. This stp is marked as (4) in Fig. 5.2. Finally, according to the KVL in the input side, $v_{in,1} + v_{in,N} = v_{dc}$. Therefore, a decrease in $v_{in,N}$ will result in an increase of $v_{in,1}$. This step is marked as (5) in Fig. 5.2. Assuming steps (1) and (5) simultaneousl in Fig. 5.2, a positive feedback on the input voltage of module 1 is observed. This positive feedback causes an inherent instability of an ISOS DC-DC converter system. The generality of the mentioned concept is not lost in case N is greater than 2. In fact, the energy in an ISOS DC-DC conversion system is constantly circulated between the input and output DC link capacitors of all modules in a pattern similar to the 5 step phenomenon discussed above. This results in low-frequency oscillations in input and ouput DC-link capacitor voltages

of all the modules. Later in this chapter, the frequency of these oscillations f_osc will be shown to be expressed as:

$$f_{osc} = \frac{1}{2\pi\sqrt{C_{in}C_o}}. \tag{5.1}$$

The controller applied to an ISOS DC-DC conversion system needs to be designed adequately to damp these oscillations. Therefore, in the current chapter, an additional control term is added to the proposed control system in the previous chapter, to damp the oscillations. The basic idea is to add a coefficient of the input DC-link voltage error of each module to the phase-shift or duty cycle control law. This additional term acts as a virtual resistor and damps the osillations in the ISOS system. Further detailed aer presented in the next sections of the chapter.

5.1.2 Literature Review

This subsection discusses the proposed control systems in the literature for Input-Series Output-Series (ISOS) DC-DC converters. Today, power conversion systems with high voltage level requirements are demanded in many applications. Instead of relying on a single conversion unit, these systems use several converters to form modular structures, realizing system-level objectives more efficiently. In particular, the Input-Series Output-Series (ISOS) modular structure is preferred for systems with both high level input and output voltages. In ISOS configuration, switches with lower voltage ratings may be used in the converter development process [89]. The cascaded structure of the ISOS configuration increases modularity, reduces the maintenance cost [90], and enables systematic expansion of system functionalities [91]. Finally, as system components need to tolerate lower electrical and thermal stresses in ISOS, the reliability is increased [91].

The advantages mentioned make ISOS DC-DC conversion systems a perfect solution for space exploration systems [90], solid state transformers [91, 92], DC transformers [91, 92], and subsea distribution systems [93]. Some of control challenges associated with ISOS DC-DC converters include power sharing among modules [89, 90, 91], and stability issues [89]. Also, controllers applicable to other modular configurations might fail to guarantee a stable system operation in ISOS [89].

For accurate power sharing among modules in an ISOS system, some of the existing approaches use auxiliary circuits or special converter topologies with natural power sharing [90],[94, 95, 96, 97, 98]. These circuitry approaches increase system's modularity and reduce the control burden. However, they either increase the cost and complexity of the system or may be unable to achieve some features such as high power densities, or bidirectional power flow. [90] uses a parallel branch including a MOSFET and a coupled inductor for power sharing, and is applicable to all topologies [90]. However, the auxiliary inductors increase magnetic losses. [94] and [95] achieve power sharing using paralleled MOSFETs, and a MOSFET-inductor combination, respectively. Although these approaches are systematic, they increase the number of circuitry components as well as cost and losses for a high number of modules. [96] uses a full-bridge based topology for natural power sharing with

reduced control burden. However, large-sized input capacitors are required, slowing down input voltage sharing dynamics. [96]. [97] uses a flyback-based topology for power sharing, which limits efficiency in high power applications due to an increased number of diodes used [97]. Finally, [98] proposes a two-transistor forward converter achieving active power sharing. However, as additional magnetic couplings between modules are required, the transformer's and converter's volumes are increased.

Control methods are also used in the literature for power sharing in an ISOS structure. The duty cycle applied to a specific module in one of these control classes is generated by processing the voltage/current signals of all other modules except that module itself [89, 99]. These controllers avoid sensing high-level input voltages [99] and enhance system dynamics [99], while reducing reliability due to communications among modules. Another control class uses droop/ inverse droop and gradient-based control methods for power sharing [100, 101, 102]. Although these controllers provide a distributed system with increased modularity [100], they create trade-offs between input voltage sharing and output voltage regulation. Peak-current controllers with effective rejection of input voltage disturbances are proposed in [8, 103]. However, implementation delays and reduced reliability arise from inter-modular communications the controllers require [103].

Some of existing controllers need system model or parameters for power sharing, reducing system robustness [104, 105, 106]. [104] uses model-predictive controllers with enhanced dynamics and reduced costs [104, 105]. [105] proposes a tunable power sharing method, and [106] provides new hot plug-in and out features. Miscellaneous methods such as applying a common duty ratio to all modules [107], or modular decoupling are also proposed [108]. The first method has a simple structure [107] with sensitivity to parameter mismatches among modules, and the latter requires inter-modular communications.

5.1.3 Contributions and Targets

This chapters aims at:

1. Extending the control system proposed in Chapter 4 to ISOS DC-DC conversion systems.

2. Adding new control terms to suppress oscillations mentioned in the previous subsection. This will stabilize the inherently unstable ISOS DC-DC system.

3. The proposed controller should have fast dynamics and suld not be sensitive to intermodular parameter mismaches

4. This chapter proposes an analysis framework for battery-connected ISOS DC-DC converters.

5. A general control framework for modular DC-DC converters is derived.

6. A comparison table is presented to compare various existing control methods with the presented control in this dissertation.

Contributions: This chapter presents a distributed control system for Input-Series Output-Series (ISOS) structure and a framework to analyze closed-loop ISOS DC-DC converters. The proposed approach is applicable to various topologies and controllers, as it provides clear insights into stability issues in the ISOS set-up by

computing input and output impedance and gain transfer functions for each module. When calculating these transfer functions, the effects of other modules are also taken into account. The framework is applied to ISOS dual active bridge converters controlled by the control system proposed in this chapter. The presented controller does not increase converter cost, complexity, losses, and volume. Furthermore, no tradeoffs between inputs/outputs voltage sharing occur when the controller is applied. The proposed control system also supports operation of converters in both power flow directions without needing converter models/parameters or communications among modules. As a result of using the introduced controller, power sharing and system dynamics are both improved. The effectiveness of methods and solutions presented in this chapter is demonstrated using simulations and experimental results.

5.2 Chapter main Control Concept

This section discusses the solution to the stability challenges mentioned in secion 5.1.1 for ISOS DC-DC converters. To tackle the positive feedback phenomenon mentioned in section 5.1.1 and avoid oscillations, it is required that the controller responds quickly to any errors in input DC link voltages of a specific modules. For example, in Fig. 5.2, let us assume that $v_{in,1}$ has become greater than its reference value. If the decentralized controller applied to module 1 is designed such that an amplified version of this input voltage error is reflected in the generated duty cycle at the next switching cycle, the transferred power level from the input to the output terminals will be increased. As a result, the excessive input DC link voltage starts to decrease immediately and it will not have time to endure by discharging the output capacitor. Therefore, the input and output capacitors cannot oscillate with each other any longer. In fact, the input terminal power error is compoensated for by the controller just locally at the input node and not by power exchange between input and output terminals. As a result, avoiding this power exchange damps the oscillations and avoids system instability.

The most straightforward method to reflect input DC link voltage error of module j in the control law with the shortest time delay after error occurence, is by adding a new term proportional to this voltage error to the duty cycle expression. Denoting the reference value of the input DC link voltage of module j by $v_{C,ref}$ and considering the controller proposed in chapter 4, the modified control law for the battery charging mode will be expressed as:

$$d_j = k_1 \int_t \left(\frac{v_{in,j}}{i_o + c} - \frac{v_{C,ref}}{i_{o,ref} + c} \right) + k_c (v_{in,i} - v_{C,ref}) \tag{5.2}$$

in which d_j, $v_{in,j}$, $v_{C,ref}$, i_o, $i_{o,ref}$, k_1, k_c, and c denote the duty cycle of module j, input DC link voltage of module j, reference input voltage of module j, output current, reference ouput current, integral gain, proportional gain, and denominator constant respectively. Further details will be provided in the next sections.

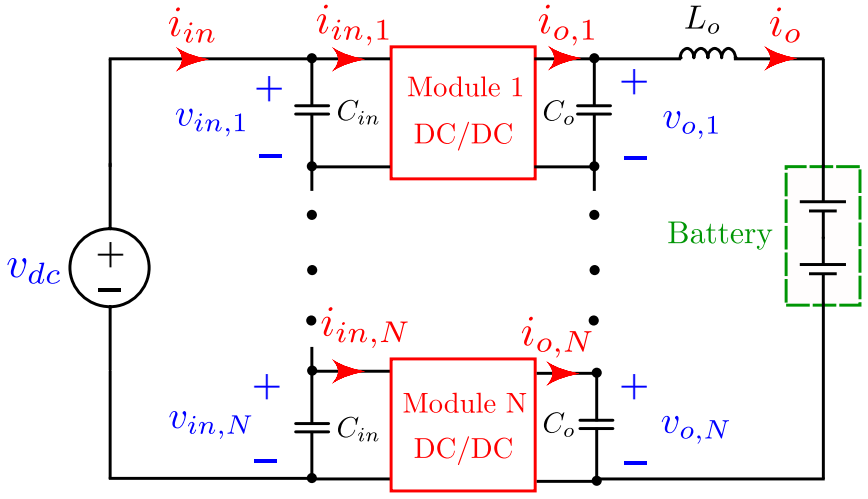


Figure 5.3: Schematic of Battery-connected ISOS DC-DC Converters

5.3 Framework to Analyze ISOS DC-DC Converters

This section provides an analysis framework for closed-loop ISOS DC-DC converters interfacing the rectified grid voltage and a battery. Fig. 5.3 presents the system schematic. In Fig. 5.3, v_{dc} is the total input voltage, i_{in} is the total input current, v_{bat} is the battery voltage, i_o is the total output current, C_{in} and C_o are input and output DC link voltage capacitors for each module, and finally L_o denotes the total output inductance of the system. Since the size of L_o inductance is small and it is used to prevent paralleling capacitors and the battery, it is assumed that it plays only a negligible role in forming the system dynamics and its effects can be ignored in this regard. Also, the ISOS structure in Fig. 5.3 interfaces N modules using the ISOS configuration. For the j-th module ($0 < j < N + 1$), $v_{in,j}$, $i_{in,j}$, $v_{o,j}$, and $i_{o,j}$ denote the input voltage, input current, output voltage, and the output current of the module, respectively. If a control system is applied to the j-th module and the closed-loop model of this module is derived and linearized around its operating point, the module's model at terminals is obtained as:

$$\begin{bmatrix} V_{o,j}(s) \\ I_{o,j}(s) \end{bmatrix} = \begin{bmatrix} A_{j,11} & A_{j,12} \\ A_{j,21} & A_{j,22} \end{bmatrix} \begin{bmatrix} V_{in,j}(s) \\ I_{in,j}(s) \end{bmatrix}. \tag{5.3}$$

It is worth mentioning that $A_{j,11}$, $A_{j,12}$, $A_{j,21}$, and $A_{j,22}$ in (5.3), are all transfer functions in the Laplace domain and they depend on the converter topology and the associated control system. For a specific converter topology and control system, these transfer functions need to be calculated. As all the modules are connected in series at their input terminals, their total input current are equal according to KCL. Therefore, for two arbitrary modules such as the j-th and k-th modules, KCL yields:

$$i_{in,j} + C_{in}\frac{dv_{in,j}}{dt} = i_{in,k} + C_{in}\frac{dv_{in,k}}{dt}. \tag{5.4}$$

Moreover, as the total input and output voltages are equal to the sum of input and output voltages of all modules, writing KVL in the input and output sides leads to:

$$\sum_{j=1}^{N} v_{in,j} = v_{dc} \tag{5.5}$$

and,

$$\sum_{j=1}^{N} v_{o,j} = v_{bat}. \tag{5.6}$$

Similarly, writng KCL at the output terminals of the two arbitrary modules j and k leads to:

$$i_{o,j} - C_o \frac{dv_{o,j}}{dt} = i_{o,k} - C_o \frac{dv_{o,k}}{dt}. \tag{5.7}$$

Equations (5.4) and (5.5) can be used to derive:

$$\sum_{j=1}^{N} i_{in,j} = N i_{in,j} + N C_{in} \frac{dv_{in,j}}{dt}. \tag{5.8}$$

From 5.8, the mathematical equation governing the input DC link voltage of modules can be found as:

$$\frac{dv_{in,j}}{dt} = \frac{1}{NC_{in}} \sum_{k=1,k\neq j}^{N} i_{in,k} + \frac{1-N}{NC_{in}} i_{in,j}. \tag{5.9}$$

Similarly, from (5.6) and (5.7), the dynamical equation for the output voltage of a module is found as:

$$\sum_{j=1}^{N} i_{o,j} = N i_{o,j} - N C_o \frac{dv_{o,j}}{dt} \tag{5.10}$$

By summing up (5.10) for all modules, the output voltage dynamics for a specific module is obtained as:

$$\frac{dv_{o,j}}{dt} = \frac{-1}{NC_o} \sum_{k=1,k\neq j}^{N} i_{o,k} + \frac{N-1}{NC_o} i_{o,j}. \tag{5.11}$$

If equation (5.9) is written in the matrix format, its equivalent in the Laplace domain is obtained as:

$$\begin{bmatrix} V_{in,j} \\ I_{in,j} \end{bmatrix} = \begin{bmatrix} \frac{1}{NC_{in}s} & 0 \\ . & . \\ . & . \\ . & . \\ \frac{1-N}{NC_{in}s} & 1 \\ . & . \\ . & . \\ . & . \\ \frac{1}{NC_{in}s} & 0 \end{bmatrix}^T \begin{bmatrix} I_{in,1} \\ . \\ . \\ . \\ I_{in,j} \\ . \\ . \\ . \\ I_{in,N} \end{bmatrix}. \tag{5.12}$$

Similarly, equation (5.11) results in:

$$\begin{bmatrix} V_{o,j} \\ I_{o,j} \end{bmatrix} = \begin{bmatrix} \frac{-1}{NC_{o}s} & 0 \\ . & . \\ . & . \\ . & . \\ \frac{N-1}{NC_{o}s} & 1 \\ . & . \\ . & . \\ . & . \\ \frac{-1}{NC_{o}s} & 0 \end{bmatrix}^T \begin{bmatrix} I_{o,1} \\ . \\ . \\ . \\ I_{o,j} \\ . \\ . \\ . \\ I_{o,N} \end{bmatrix}. \tag{5.13}$$

Equations (5.3), (5.12), and (5.13) result in:

$$i_{o,j} = \frac{A_{21}}{NC_{in}s} \sum_{k=1,k\neq j}^{N} i_{in,k} + \left[\frac{A_{21}(1-N)}{NC_{in}s} + A_{22} \right] i_{in,j} \tag{5.14}$$

and,

$$\begin{aligned} \frac{-1}{NC_{o}s} \sum_{k=1,k\neq j}^{N} i_{o,k} + \frac{N-1}{NC_{o}s} i_{o,j} = \frac{A_{11}}{NC_{in}s} \sum_{k=1,k\neq j}^{N} i_{in,k} \\ + \left[\frac{A_{11}(1-N)}{NC_{in}s} + A_{12} \right] i_{in,j}. \end{aligned} \tag{5.15}$$

Using (5.14) and summing up all the expressions for all the modules lead to:

$$\sum_{j=1}^{N} i_{o,j} = A_{22} \sum_{j=1}^{N} i_{in,j}. \tag{5.16}$$

Finally, (5.14) and (5.15) and (5.16) yield:

$$\frac{i_{o,j}(s)}{i_{in,j}(s)} = \frac{(A_{22}A_{11} - A_{12}A_{21})C_{o}s - A_{22}A_{21} + {A_{22}}^2 C_{in}s}{A_{11}C_{o}s - A_{21} + A_{22}C_{in}s}. \tag{5.17}$$

Equation (5.17) expresses the current gain transfer function for a specific module, in a closed-loop ISOS DC-DC conversion system. Using (5.3) and (5.17), all other

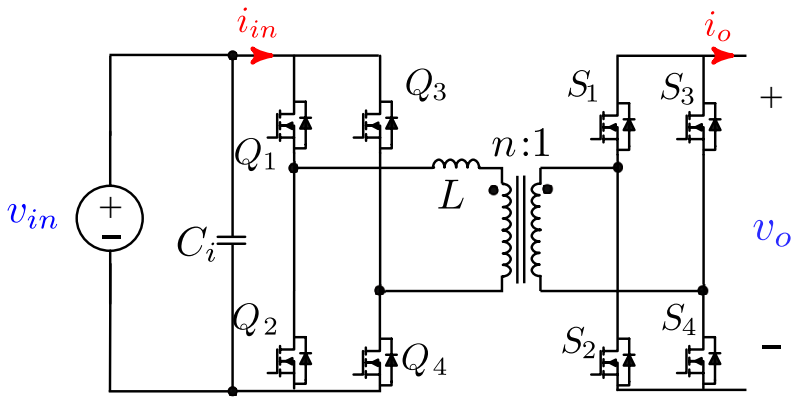


Figure 5.4: Schematic of a Dual Active Bridge Converter

transfer functions can also be obtained for a specific module. Therefore, the proposed framework to analyze battery-connected ISOS DC-DC converters can be explained as follows:

Step 1: For a given topology and control system, $A_{j,11}$-$A_{j,22}$ matrices in 5.3 need to be calculated.

Step 2: Using (5.3) and (5.17), all transfer functions for a specific module can be calculated. The next section describes the application of the control system proposed in chapter 4, to ISOS dual active bridge converters.

5.4 Application of Proposed Controller to ISOS DAB Converters

This section discusses the application of the proposed controller in chapter 4, to ISOS DAB converters. Fig. 5.4 illustrates a DAB converter, which is used as a modular unit in Fig. 5.3.

The notations used for the DAB converter are the same as those used in chapter 4. Using the same method as in chapter 4, the phase-shift applied to the j-th module can be given by $\theta_j = \pi D_j$. Also, D_j is defined such that an increase in its value increases the power transferred by the module.

Considering the i-th module in Fig. 5.3 and assuming the battery charging mode, if $v_{in,i}$ is greater than its reference value, this means that the DC link capacitor of the module is discharged less as expected by the battery. Therefore, more power must be transferred from the input to the output side, to discharge the DC link capacitor as required and set $v_{in,i}$ back to its reference value. To increase the transferred power of the module, its duty cycle d_i must be increased. Similarly, if i_o is greater than its reference value, this means excessive power is transferred to the battery by the entire structure and to help reduce it down, each module must contribute by reducing its own transferred power. Equivalently, d_i must be reduced. In conclusion, d_i must be increased and decreased, if $v_{in,i}$ and i_o are greater than their reference values,

respectively. This can be achieved using the division function and by setting d_i in battery charging mode as :

$$d_i = K_1 \int_t \left(\frac{v_{in,i}}{i_o + c} - \frac{v_{C,ref}}{i_{o,ref} + c} \right) dt, K_1 > 0. \tag{5.18}$$

However, if the power flows from the output side to the input side, the duty cycle applied to the i-th converter is calculated by:

$$d_i = K_2 \int_t \left(\frac{v_{in,i}}{i_o + c} - \frac{v_{C,ref}}{i_{o,ref} + c} \right) dt, K_2 < 0. \tag{5.19}$$

In fact, instead of using both division and multiplication functions as in ISOP or IPOS configurations, only division function is used in ISOS configuration for both power flow directions. However, the controller gain is either greater or less than zero using the division function, based on the power flow direction. The reason why unlike ISOP or IPOS converters, division is required for both power flow directions for ISOS converters, is that an ISOS system behaves the same if input and output sides are reversed based on the power flow direction. However, an ISOP structure in battery charging mode becomes IPOS in the battery discharging mode and the system characteristics change. It is worth mentioning that a division function is selected to enable the modules to react faster to power mismatches among themselves and hold an appropriate power sharing, while changing their transferred power levels during transients. This feature is important to guarantee a stable operation and is obtained because $v_{in,i}$ is in the nominator of the division function. Fig. 5.5 illustrates the block diagram of the proposed controller for ISOS DAB converters.

As Fig. 5.5 illustrates, two different control architectures based on the division function are used for different power flow directions. To enable soft transitions between the two modes, the same methodology as in chapter 4 is used. First, $i_{o,ref}$ is compared with zero to determine the power flow direction. Next, the duty cycle applied to the converter is sampled at the instant of the power flow change and the integrator is reset. Finally, one of the generated duty cycles is applied to the converter by a 2-input MUX, based on the power flow direction.

5.5 Stability Challenges in ISOS Converters and Modified Version of Proposed Controller

Selecting the ISOS configuration to connect several DC-DC converter modules can bring challenges in controller design to achieve a stable system operation. By taking ISOS DAB converters as an example and assuming common phase-shift control for all modules, this section illustrates the inherent instability in the ISOS structure. The system schematic is given in Fig. 5.3 and Fig. 5.4. It is assumed that the common duty ratio d_{com} is applied to all modules. Considering Fig. 5.4 and from chapter 4, it is known that for a DAB converter, the converter gain is given by:

$$\frac{i_o}{v_{in}} = \frac{i_{in}}{v_o} = \lambda d(1-d). \tag{5.20}$$

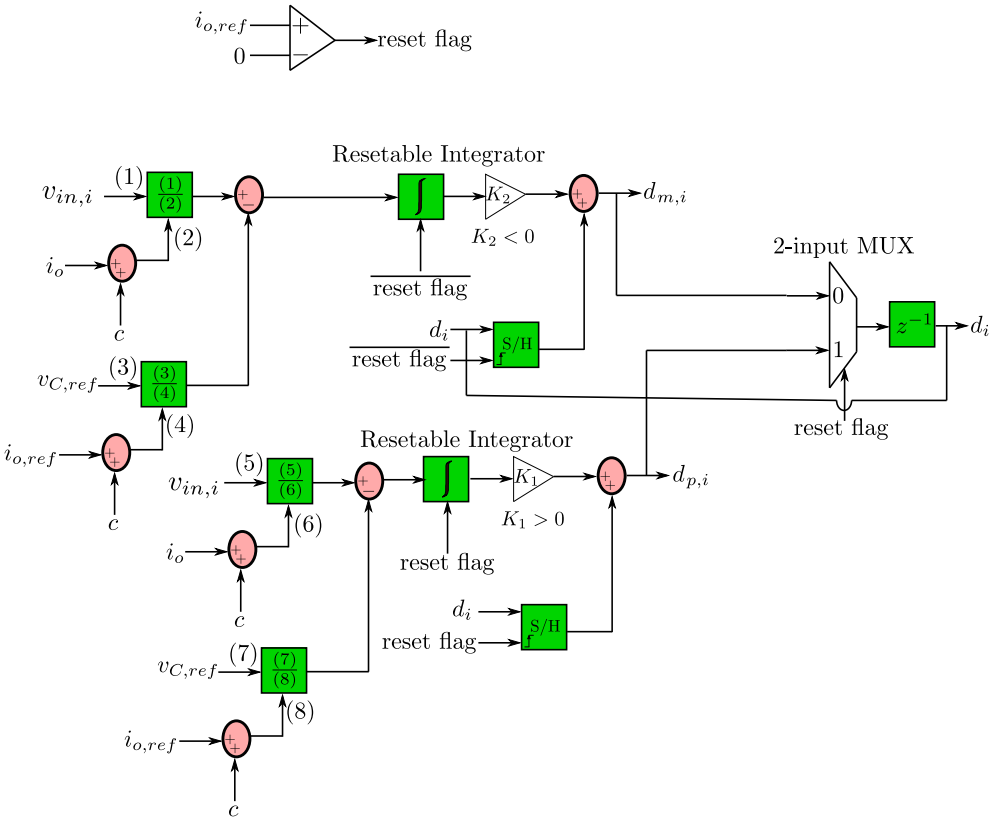


Figure 5.5: Proposed Control System for ISOS DAB Converters

Using (5.7) and (5.20) leads to:

$$\lambda d_{com}(1-d_{com})(v_{in,j}-v_{in,k}) = C_o \frac{d(v_{o,j}-v_{o,k})}{dt}. \tag{5.21}$$

Similarly, using (5.4) and (5.20) leads to:

$$\lambda d_{com}(1-d_{com})(v_{o,j}-v_{o,k}) = -C_{in} \frac{d(v_{in,j}-v_{in,k})}{dt}. \tag{5.22}$$

Denoting $\Delta v_{in} = v_{in,j} - v_{in,k}$, (5.21) and (5.22) can be used to derive:

$$\frac{d^2 \Delta v_{in}}{dt^2} + \frac{\lambda^2 {d_{com}}^2 (1-d_{com})^2}{C_{in} C_o} \Delta v_{in} = 0. \tag{5.23}$$

The 2-nd order differential equation expressed by (5.23) suggests low-frequency ripples on DC-link voltages of the modules. The frequency of these oscillations are calculated as:

$$f = \frac{DAB\ Gyrator\ Gain}{2\pi\sqrt{C_{in} C_o}}. \tag{5.24}$$

In the above equation, the DAB Gyrator Gain is the output current-to- input voltage gain of a DAB converter module, which acts as a Gyrator. In fact, this

equation shows a resonance and power exchange between input and output DC link capacitances in ISOS structure. As these oscillations are of low frequencies and are not equal to the switching frequency, they can be interpreted as a marginally stable system which can become unstable in practice. This is because these oscillations are related to a joint of complex poles on $j\omega$ axis in s-plane.

The inherent tendency of an ISOS system to become unstable can be addressed by appropriate controller design. The proposed analysis framework in this chapter is capable of evaluating the stability of a closed-loop ISOS structure by deriving the system poles in the obtained transfer functions. To eliminate low-frequency ripples on DC-link voltages of modules, a coefficient of the term $\frac{d\Delta v_{in}}{dt}$ can be added in (5.24). In the analysis provided in this section, common duty ratios were applied to both modules to derive (5.24) and as a result, the term $\frac{d\Delta v_{in}}{dt}$ was absent in this equation. So, the control law in (5.18) can be modified as:

$$d_i = K_1 \int_t \left(\frac{v_{in,i}}{i_o + c} - \frac{v_{C,ref}}{i_{o,ref} + c} \right) dt + K_c v_{in,i}, K_1 > 0, K_c > 0. \tag{5.25}$$

Similarly, (5.26) can be modified as:

$$d_i = K_2 \int_t \left(\frac{v_{in,i}}{i_o + c} - \frac{v_{C,ref}}{i_{o,ref} + c} \right) dt + K_d v_{in,i}, K_2 < 0, k_d < 0. \tag{5.26}$$

This way, the difference between the duty ratios applied to both modules directly includes a new Δv_{in} term. To eliminate the low-frequency ripples in (5.24), K_c and k_d should be designed such that Δv_{in} disappear as fast as possible during system operation. The next section analyzes the proposed control system for ISOS converters.

5.6 Application of Proposed Analysis Framework for Analysis of Proposed Closed-loop ISOS System

In this section, the proposed framework in this chapter is used to analyze the proposed closed-loop ISOS DAB converters. For this purpose, the matrix indices in (5.3) must be calculated first. Considering Fig. 5.4 and linearizing (5.20) around the operating point of the converter lead to:

$$v_o = \frac{i_{in}}{\lambda d(1-d)} = \frac{{i_{in}}^*}{\lambda d^*(1-d^*)} + \frac{1}{\lambda d^*(1-d^*)} \tilde{i_{in}} + \frac{{i_{in}}^*(2d^*-1)}{\lambda {d^*}^2(1-d^*)^2} \tilde{d} \tag{5.27}$$

in which, the parameters accompanied by $*$ denote the values at the operating point of the converter. From (5.27), the small-signal model of a DAB converter is expressed as:

$$\tilde{v_o} = \frac{1}{\lambda d^*(1-d^*)} \tilde{i_{in}} + \frac{{i_{in}}^*(2d^*-1)}{\lambda {d^*}^2(1-d^*)^2} \tilde{d}. \tag{5.28}$$

From (5.20), the gain expression of a DAB converter using the single phase shift modulation can be rewritten as:

$$i_o = \lambda({v_o}^* + \tilde{v_{in}})(d^* - {d^*}^2 + (1 - 2d^*)\tilde{d}). \tag{5.29}$$

Finally, from (5.29), the linear model of a DAB converter is obtained as:

$$\tilde{i_o} = \lambda(d^* - {d^*}^2)\tilde{v_{in}} + \lambda {v_{in}}^*(1 - 2d^*)\tilde{d}. \tag{5.30}$$

If the power flows from the voltage source to the battery, (5.25) and KCL in the output side of the module result in:

$$\frac{d(\tilde{d})}{dt} = \frac{K_1}{i_{o,ref} + c}\tilde{v_{in}} - \frac{K_1 {v_{in}}^*}{(i_{o,ref} + c)^2}\tilde{i_o} + \frac{K_1 {v_{in}}^* C_o}{(i_{o,ref} + c)^2}\frac{d\tilde{v_o}}{dt} + K_c\frac{d\tilde{v_{in}}}{dt}. \tag{5.31}$$

From (5.28), (5.30), and (5.31), all the matrice indices in (5.3) can be calculated in s-domain. Due to the complication of the equations in parametric format, these transfer functions are numerically calculated below for a case study. This case study also shows the dynamic response of the converter for the battery charging mode, when $i_{o,ref}$ experiences a step change. It is shown that the predicted waveforms using these transfer functions are matched with simulation results.

Case Study 1: Two ISOS DAB converters are assumed with 22μF and 25μF input DC link capacitors, 16.7μH and 15μH tank inductances, and finally 60μF and 70μF output DC link capacitors. The turns ratios of the transformers are 20:6 and 20:7, for the modules, respectively. The total input and output coltages are 400V and 100V, respectively. The modules transfer power from the input to the battery side and the controller parameters are designed as $K_1 = 500$ and $K_c = 0.02$. Using the proposed analysis in this chapter, the input current-to-output current transfer function of a module is given by:

$$g(s) = \frac{I_{o,j}(s)}{I_{in,j}(s)} = -1.32\frac{s^2 - 31500s - 184365000}{s^2 + 15000s + 42130000}. \tag{5.32}$$

For a 8A-to-9A output current step, the transfer function expressed by (5.32) is applied to the input current of a module. The actual output current obtained by simulation and the predicted output current obtained by the transfer function are compared in Fig. 5.6. As this figure shows, these two currents match each other and this verifies the effectiveness of the proposed analysis framework in this chapter. Also, it can be seen that all system poles in (5.32) are in the negative half of s-plane. Therefore, the system is stable.

5.7 Investigation of System Stability with Proposed Controller

Using the proposed framework to obtain system transfer functions, all the system poles can be calculated for ISOS DC-DC converters with the proposed controller.

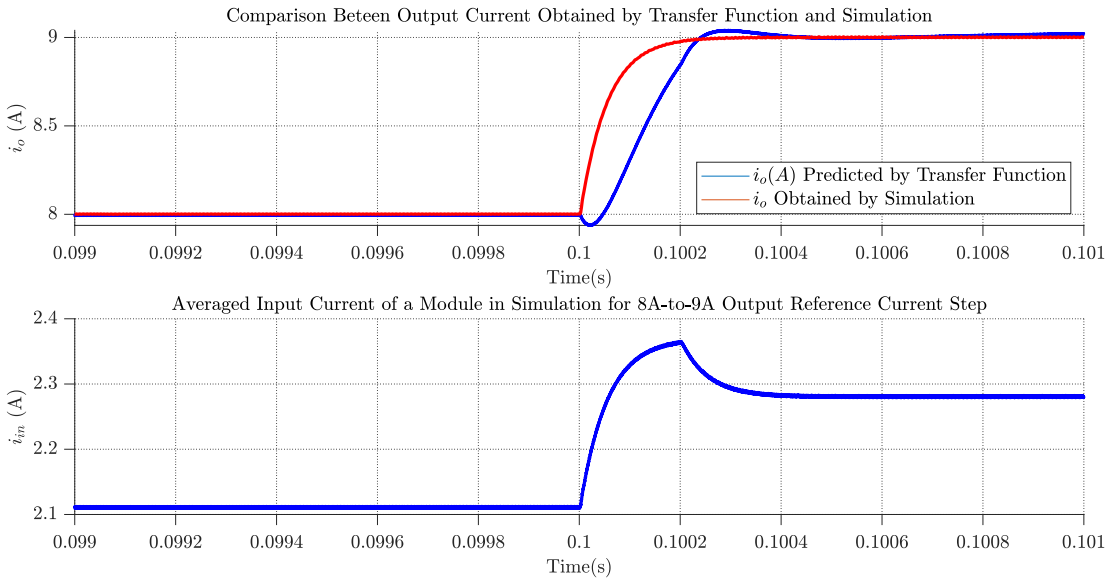


Figure 5.6: Comparison Between the Predicted Output Current by Transfer Functions and Actual Output Current Obtained by Simulation

This section provides a case study to investigate system stability with the proposed controller. For this purpose, the root locus diagram is plotted for different values of k_1 in the battery charging mode.

Case Study 2: In this case study, the system parameters are the same as in case study 1. The transfer functions associated with the system are obtained using the proposed framework and the dominant poles of the system are plotted in a root locus diagram for $200 < K_1 < 10000, K_c = 0.02$. As a result, the root locus diagram in Fig. 5.7 is obtained. According to this figure, the system poles are in the negative half of s-plane. Therefore, the system is always stable. It can also be observed that the greater K_1, the faster system dynamical profile is achieved. This is because by increasing K_1, the system poles are transferred further left from the $j\omega$ axis in s-plane.

According to the Nyquist stability criterion, the real value of tall system poles must be greater than $\frac{-f_s}{2}$ in order to have a stable operation. Therefore, the real values of the dominant poles cannot be less than -50000 in the stable operation region. This condition is fulfilled according to the root locus diagram for the variation range of K_1.

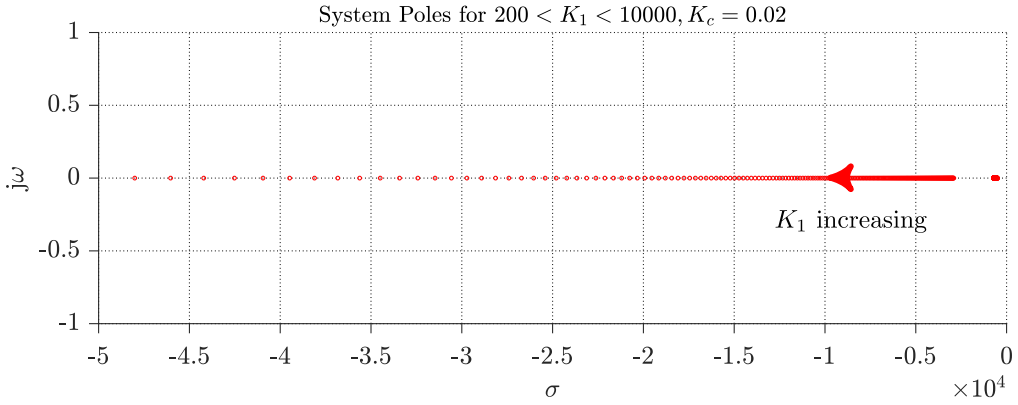


Figure 5.7: Root Locus Diagram for ISOS DAB Converters with Proposed Controller

5.8 Simulation Results

This section validates the performance of the proposed controller for ISOS DAB converters using several simulation scenarios.

One of the applications in which ISOS DC-DC converters are frequently used include electrical transportation vehicles such as railways and electric vehicles [8]. In an electric vehicle, for example, the vehicle battery should be charged fast and normally, the constant current-constant voltage approach is used for this purpose. The electric vehicle battery is charged using an electric grid and is also used as an energy storage device, to provide the grid with the power it needs at other times.

The amount of power the battery is required to provide to the grid, and the power flow changes during the system operation. Therefore, ISOS converters must be able to provide bi-directional power flow capabilities and the system dynamics in reference load current steps has to be optimized, so that electric vehicles can provide the grid with its required power in the shortest possible time period.

Motivated by the above discussions, the performance of the proposed controller is simulated for various reference load current steps in this section. The results show that the proposed controller can handle reference load current steps in battery charging, discharging, and transitions between charging and discharging modes.

Scenario 1: Two ISOS DAB converters are assumed with 22μF and 25μF input DC link capacitors, 16.7μH and 15μH tank inductances, and finally 60μF and 70μF output DC link capacitors. The turns ratios of the transformers are 20:6 and 20:7, for the modules, respectively. The total input and output coltages are 400V and 100V, respectively. If the modules transfer power from the input to the battery side and the controller parameter is designed as $K_1 = 500$ and $K_c = 0.02$, the system response to a 8A-to-15A step for the reference battery current is as shown in Fig. 5.8.

As Fig. 5.8 illustrates, the controller has provided accurate power sharing between modules both at steady state and transient conditions. Also, the battery current has tracked its reference command accurately without any overshoots or undershoots. Moreover, the controller has enabled a fast system response.

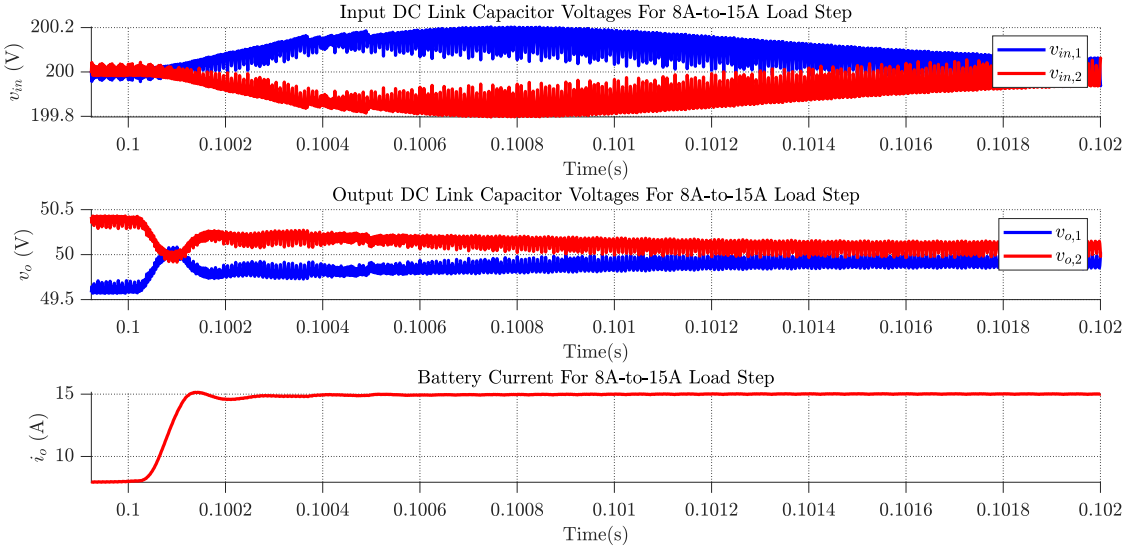


Figure 5.8: System Response For a 8A-to-15A Reference Battery Current Step: Input and Output DC Link Voltages and Battery Current Waveforms

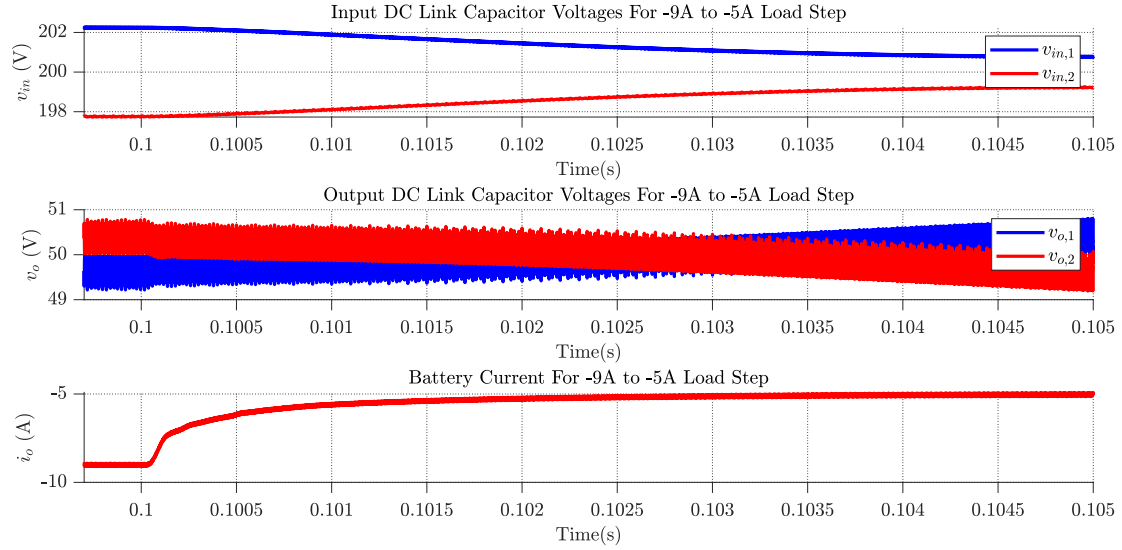


Figure 5.9: System Response For a -9A to -5A Reference Battery Current Step: Input and Output DC Link Voltages and Battery Current Waveforms

Scenario 2: Two ISOS DAB converters are assumed with the same parameters as in scenario 1. If the reference battery current experiences a step from -9A to -5A, the system response waveforms are shown in Fig. 5.9. As this figure implies, the battery current reaches its steady-state value within 10ms and the DC link voltages guarantee appropriate power sharing in both transient and steady-state conditions.

Scenario 3: Two ISOS DAB converters are assumed with the same parameters as in scenario 1. If the reference battery current experiences a step from -4A to 4A, the system response waveforms are shown in Fig. 5.10. As this figure implies, the battery current reaches its reference steady-state value and the DC link voltages

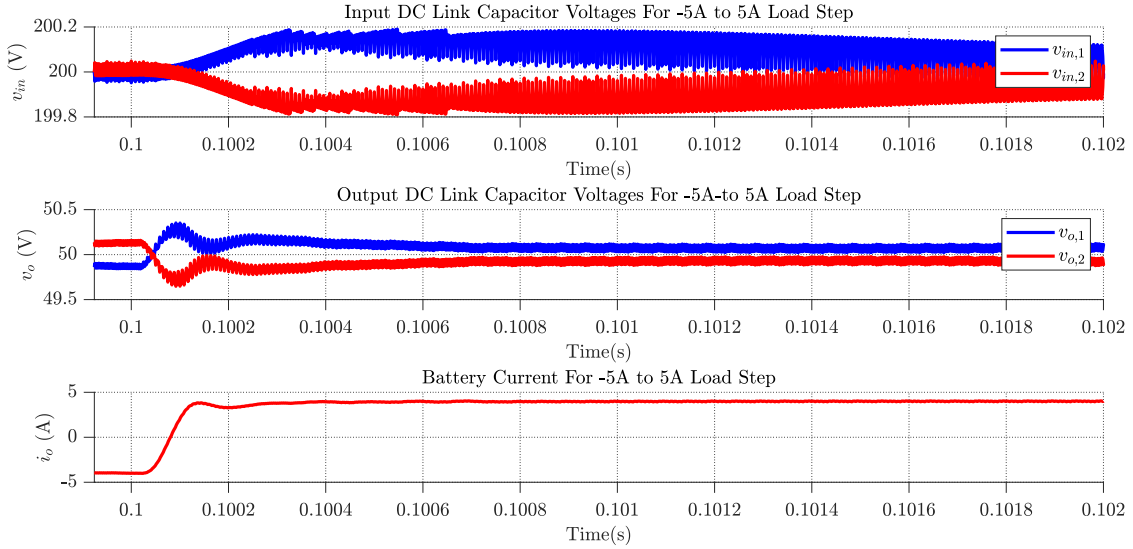


Figure 5.10: System Response For a -4A to 4A Reference Battery Current Step: Input and Output DC Link Voltages and Battery Current Waveforms

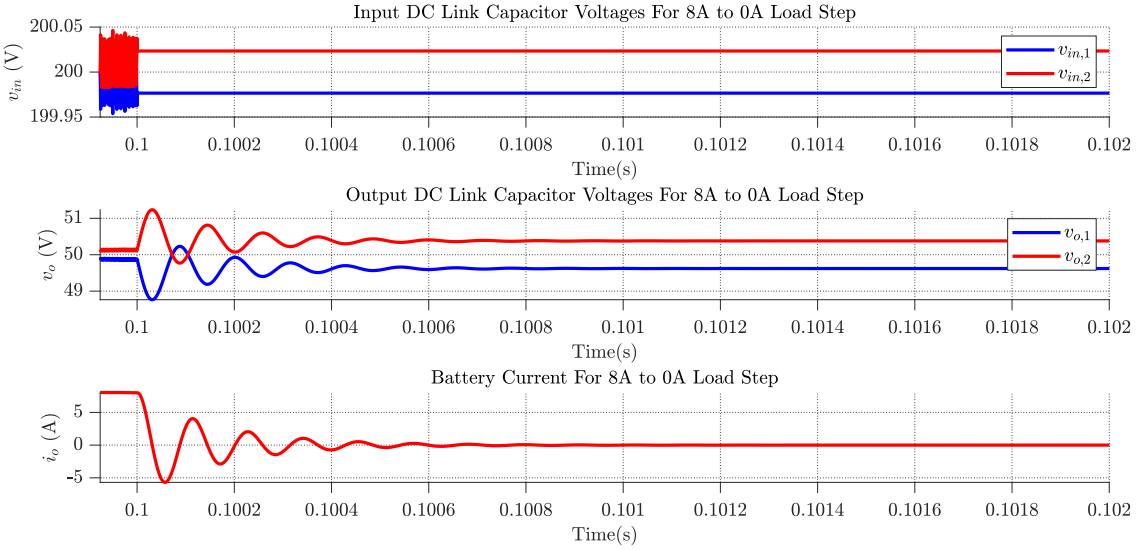


Figure 5.11: System Response For a 8A to 0A Reference Battery Current Step: Input and Output DC Link Voltages and Battery Current Waveforms

guarantee appropriate power sharing in both transient and steady-state conditions.

Scenario 4: in this scenario, the system parameters are the same as in the previous ones. The output reference current references a step from 8A to 0A. In fact, the system experiences a transition from the full load battey charging condition to the no load condition. The system response is given in Fig. 5.11.

5.9 Reference Generation Approach with Application to ISOS Forward Converters

This section discusses the procedure of setting the reference signal for the input DC link voltage using the proposed controller. Also, a case study is presented for ISOS forward converters, to demonstrate the effectiveness of the presented method. In case the total input voltage applied to the ISOS structure is changed, or some of the modules are either plugged in or out of the system, the reference value for the input DC link voltage changes. This is because this reference value shuld be equal for all modules, to enable appropriate power sharing among them. Thus, the reference value is equal to the total input voltage divided by the number of modules and a change in either of these parameters lead to a change in the reference value. In order to keep the controller structure distributed and avoid any additional supervision on the controller performance when a reference value change is required, the procedure of setting the reference value should be done automatically. This section modifies the controller structure, to enable this feature.

Considering modules i and j and assuming that the power flows from the input to the output side, the integrator in (5.18) yields:

$$\frac{v_{in,i}}{i_o + c} = \frac{v_{in,j}}{i_o + c} = \frac{V_{C,ref}}{i_{o,ref} + c}. \tag{5.33}$$

Because the ISOS configuration is used, i_o is common for all modules and (5.33) yields $v_{in,i} = v_{in,j}$. Therefore, power sharing among the modules is guaranteed at steady-state, apart from any differences between i_o and $i_{o,ref}$. So, if the total input voltage V_1 is applied to the system, $v_{in,j} = v_{in,k} = \frac{V_1}{N}$, in which N is the number of modules. Let us assume that just in the start up condition, $v_{C,ref} = \frac{V_1}{N}$manually by external supervision. If the total input voltage is changes to V_2 during system operation, the above discussions suggest that $v_{in,i} - v_{in,j} = \frac{V_2}{N}$. At this point, (5.18) yields:

$$\frac{\frac{V_2}{N}}{i_o + c} = \frac{\frac{V_1}{N}}{i_{o,ref} + c}. \tag{5.34}$$

As illustrated by (5.34), i_o is not equal to $i_{o,ref}$, after a step in the total input voltage. However, the power sharing is automatically maintained by the controller. This forms the basis of the first proposed approach for automatic reference setting for $V_{C,ref}$. This method is called Two Stage Reference Setting. When $v_{in,i} = v_{in,j} = \frac{V_2}{N}$ at steady-state, if $v_{C,ref} = \frac{V_2}{N}$ is set, (5.34) suggests that $i_o = i_{o,ref}$. Therefore, the Two Stage Reference Setting Algorithm can be implemented using the following steps:

Step 1: In start-up condition, $v_{C,ref} = \frac{v_{in}}{N}$ should be set manually. *Step 2*: During system operation and at steady-state, whenever $i_o \neq i_{o,ref}$, the value of $v_{C,ref}$ for module i should be set equal to the value of $v_{C,i}$ at the same steady-state condition.

The second method proposed to set $v_{C,ref}$ automatically is called Reference Setting Without Start Up Planning. In this method, the value of $v_{C,ref}$ is set automatically both at start-up and during the system operation. Therefore, unlike the Two

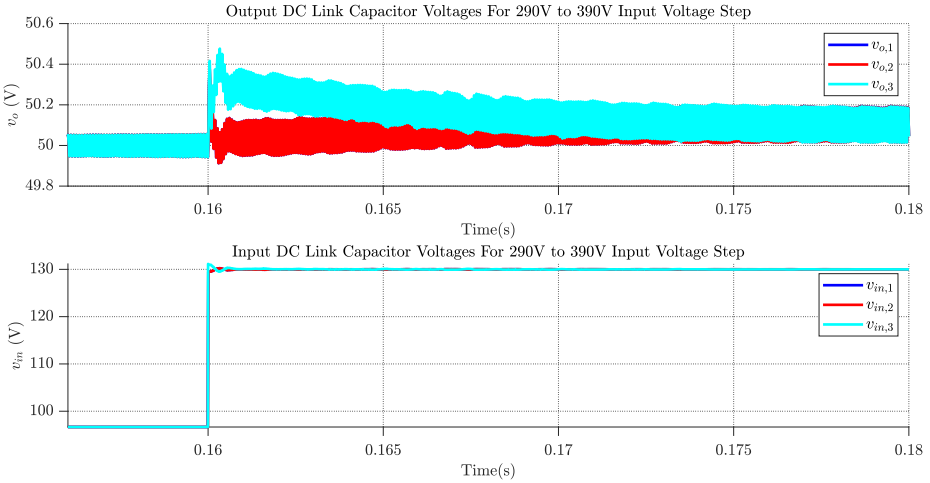


Figure 5.12: Comparison Between the System Performances Using the Proposed Controller and [8] in a 290V to 390V Input Voltage Step

Stage Reference Setting Algorithm, it is not required to set the initial value of $v_{C,ref}$ at start-up condition. This method uses a PI control loop to set the value of $V_{C,ref}$. In fact:

$$v_{C,ref} = K_{ia} \int_t (i_o - i_{o,ref})dt + K_{pa}(i_o - i_{o,ref}). \tag{5.35}$$

While discussing the two stage reference setting algorithm, it was pointed out that the value of $v_{C,ref}$ must be modified whenever $i_o \neq i_{o,ref}$. In the reference setting without start up planning, the value of $v_{C,ref}$ is selected to make $i_o = i_{o,erf}$ at steady-state, by means of a PI control loop. This method is implemented using simulations in the next section, while comparing the proposed controller with an existing one in the literature.

Finally, it is worth mentioning that the two stage reference setting algorithm allows the system to reach its new steady-state condition when the number of modules and the input voltage change. Once this new steady-state condition is reached, the control parameters are modified automatically. Therefore, compared with the second approach, this method benefits from a higher system reliability. This is because if the control parameter modifications and the system structural changes happen simultaneously, it can lead to faults in the system. On the other hand, the second proposed method benefits from faster dynamical responses and requiring no reference values to be set at start-up.

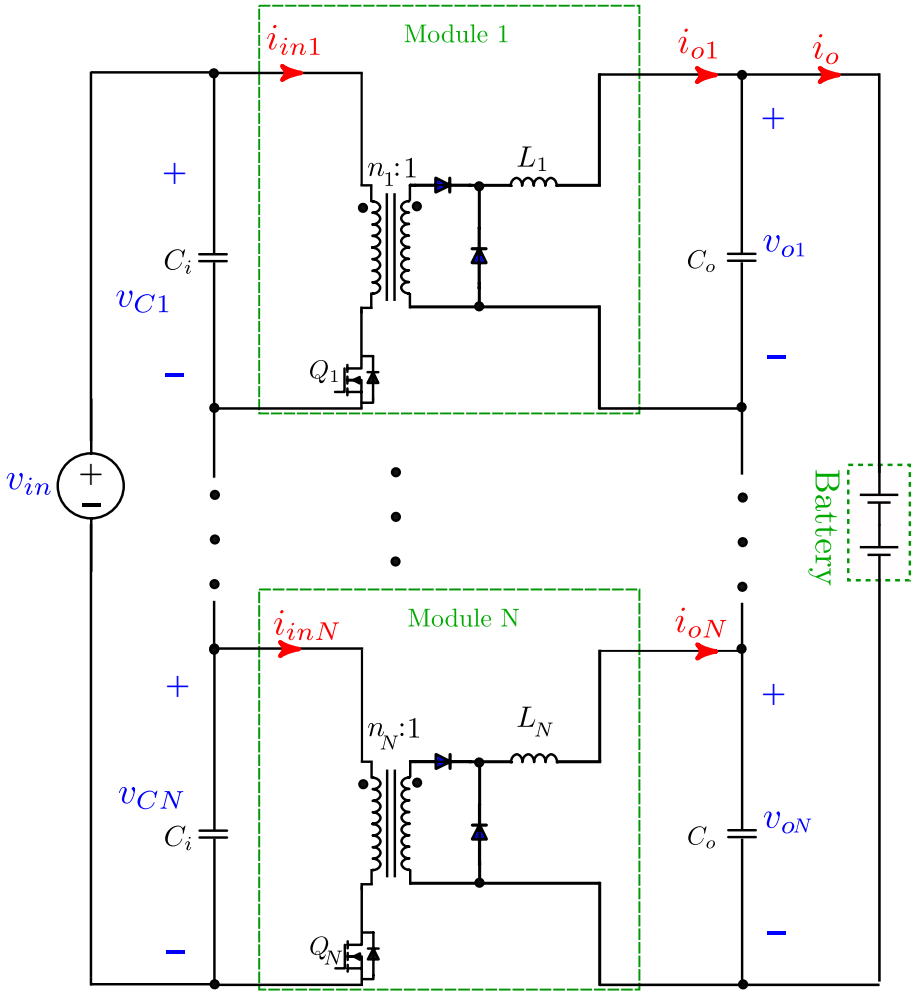


Figure 5.13: Schematic of Three ISOS Forward Converters for Comparison Case Study

5.10 Comparison Results for ISOS Forward Converters

In this section, the proposed controller in this chapter is compared with [8]. Three ISOS forward converters are considered in Fig. 5.13 with the parameters shown in Table 5.1.

The total input voltage is changed from 290V to 390V and the reference output current is 3A. Fig. 5.12 shows the system response for input and output DC link capacitor voltages, when the proposed controller in this chapter is applied as the total input voltage increases from 290V to 390V. From comparing the first two columns of Table 5.1 and Fig. 5.12, the proposed controller considerably reduces overshoot/undershoot levels and recovery times associated with output DC link voltages compared with [8]. Also, these simulation results verify the effectiveness of the proposed methods for automatic reference setting proposed in the previous

Table 5.1: Comparison of the proposed method and [8]

	Proposed:Dynamics	[8]	Proposed:Component Sizes
Minimum Input Voltage $v_{\text{in,min}}$ (V)	290	290	290
Maximum Input Voltage $v_{\text{in,max}}$ (V)	390	390	390
Output Voltage v_o (V)	150	150	150
Switching Frequency f_s (KHz)	100	100	100
Inductor L (μH)	300	300	300
DC-link Capacitor C_i (μF)	20,20,10	20,20,10	15,15,7.5
Output Capacitor $C_o(\mu F)$	282	282	50
Reference Load Current $i_{o,ref}$ (A)	3	3	3
Transfomer Turns Ratios	$\frac{1}{1.85}$	$\frac{1}{1.85}$	$\frac{1}{1.85}$
Maximum Output Voltage Error in Transient $v_{dev,out}$ (V)	0.5	3	3
Output Voltage Recovery Time $t_{r,out}$ (ms)	4	15	15

section. It is worth mentioning that the last column of Table 5.1 corresponds to the case in which the proposed controller achieves a system dynamical profile similar to [8], using smaller-sized input and output DC-link capacitors. Therefore, the proposed controller in this chapter enables using smaller sized components in the system.

Table 5.2 makes a comparison between the proposed controller in this chapter and several other methods in the literature, in terms of method features. As it is observable, the proposed control system is modular due to using a distributed control approach. Also, it can handle different converter topologies and does not need to use converter model or parameters. Therefore, it can acheive appropriate power sharing among the modules in the presence of parameter mismatches among them. Finally, it does not use any extra components to achieve power sharing among modules and therefore, reduces the cost and complexity of the system.

Table 5.2: Comparison of the Proposed Method and Other Existing Methods From Method Features Point of View

	Modular	Topology-free	Converter Model Needed	$\frac{\text{Circuitry Component}}{\text{Module}}$	Increased Cost
This Work	Yes	Yes	No	0	No
[90]	No	Yes	No	2	Yes
[95]	Yes	Yes	No	3	Yes
[8]	No	Yes	No	0	No
[100]	Yes	No	Yes	0	No

5.11 General Decentralized Control Framework for Modular DC-DC Converters

Fig. 5.14 shows the schematic of a DC-DC converter module, denoted by module j, which constitutes a part of a modular DC-DC conversion system composed of N modules 0 <j<N+1. $v_{in,j}$ and $v_{o,j}$ denote the input and output voltage of module j, respectively. Similarly, $i_{in,j}$ and $i_{o,j}$ denote the input and output currents of module j, respectively. Finally, $P_{in,j}$ and $P_{o,j}$ denote the power level transferred by input and output terminals of module j, and d_j denotes the control input applied to module j. This control input can be either duty ratio or phase shift, according to the converter topology and switching modulation scheme used. The terminology used in this section is provided below. The "input terminal" of module j in Fig. 5.14 is defined as the converter terminal receiving power from the source i.e. $P_{in,j} > 0$. Also, the "output terminal" of module j in Fig. 5.14 is defined as the converter terminal supplying power to the load i.e. $P_{o,j} > 0$. Based on the modular configuration used, each of the input and output terminals of module j in Fig. 5.14 are either connected in series or parallel. Taking the input terminal as an example, if the input terminal of module j is connected in series with the input terminals of other modules, the input current flowing through all the input terminals of different modules are equal

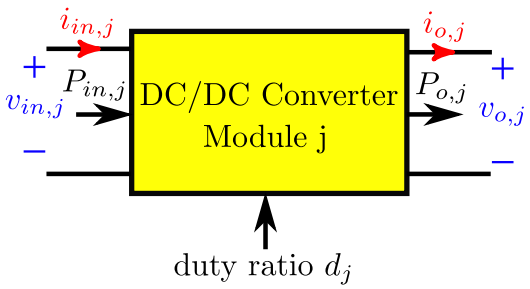


Figure 5.14: Schematic of a DC/DC Converter Module (Module j) in a Modular DC/DC Conversion System Composed of N Modules

i.e. $i_{in,j} = i_{in,k}$, $j \neq k$, $0 < j < N+1$, $0 < k < N+1$. Therefore, to share equal power among the modules, the control system needs to operate such that $v_{in,j} = v_{in,k}$, $j \neq k$, $0 < j < N+1$, $0 < k < N+1$. Similarly, in case parallel configuration is used for modules at their input terminals, the control system needs to set $i_{in,j} = i_{in,k}$, $j \neq k$, $0 < j < N+1$,$0 < k < N+1$. Therefore, in this section, $i_{in,j}$ and $v_{in,j}$ are named **Input Terminal Control Sharing Variable $\mathbf{IN_j^{Sh}}$**, in case parallel and series modular configurations are used in the input terminals of the modules, respectively. The reference command set by the control system for this input terminal control sharing variable is named **Reference Input Terminal Variable $\mathbf{IN_{ref}^{Sh}}$**. Using an exactly similar approach, **Output Terminal Control Sharing Variable $\mathbf{OUT_j^{Sh}}$** and **Reference Output Terminal Variable $\mathbf{OUT_{ref}^{Sh}}$** can be defined.

General Decentralized Control Law: In general control law, the control input applied to module j, i.e. d_j, is defined such that an increase in d_j leads to an increase in $P_{o,j}$ in Fig. 5.14. Considering this in MODSAR, d_j is obtained using (5.36), in which f is a function of IN_j^{Sh} and OUT_j^{Sh} such that $\frac{df}{d(\mathrm{IN}_j^{Sh})} > 0$ and $\frac{df}{d(\mathrm{OUT}_j^{Sh})} < 0$.

$$d_j = k \int \left(f(\mathrm{IN}_j^{Sh}, \mathrm{OUT}_j^{Sh}) - f(\mathrm{IN}_{ref}^{Sh}, \mathrm{OUT}_{ref}^{Sh}) \right) dt. \tag{5.36}$$

This control law is applicable to all DC/DC modular configurations including ISOP, IPOS, ISOS, and IPOP. The MODSAR controller realizes equal transferred power sharing among all modules. It also regulates the total power transferred to the load side at its reference value. IN_{ref}^{Sh} and OUT_{ref}^{Sh} are the same for all modules and the control law in (5.36) is simultaneously applied to all modules in the system, to form a decentralized controller. In this decentralized control system, all modules cooperate to share equal power and regulate the total output power transferred to the load. In (5.36), k is the controller gain.

Remark 1: During system operation, the controller applied to module j must closely monitor IN_j^{Sh} to ensure appropriate power sharing is maintained among all modules. This is important to prevent large overshoot/undershoot levels in voltages and currents during system transient states. Selecting the f function in (5.36) as the division operator can provide better power sharing with lower undershoot/overshoot levels in transients and faster recovery times. Using the division operator, (1) is implemented as:

$$d_j = k \int \left(\frac{\mathrm{IN}_j^{Sh}}{\mathrm{OUT}_j^{Sh}} - \frac{\mathrm{IN}_{ref}^{Sh}}{\mathrm{OUT}_{ref}^{Sh}} \right) dt. \tag{5.37}$$

The control law in (5.37) produces a larger $\frac{d(d_j)}{dt}$ in response to power mismatch between modules at the input side, in comparison with $\frac{d(d_j)}{dt}$ produced in case of output power regulation error. This is because the proposed general decentralized controller manages power sharing and output power regulation in the numerator and denominator of the fraction in (5.37), respectively. Once power sharing is precisely maintained between modules during a transient period, the controller can achieve most of its resources to achieve output power regulation faster. This is why the division operator is preferred in MODSAR control law i.e. (5.37).

Remark 2: If the input terminals are connected in parallel, (5.36) may be implemented using a multiplication function for f, to obtain enhanced system dynamics. This way, the control law can be written as in (5.38).

$$d_j = k \int \left(\mathrm{IN}_j^{Sh} \times \mathrm{OUT}_j^{Sh} - \mathrm{IN}_{ref}^{Sh} \times \mathrm{OUT}_{ref}^{Sh} \right) dt. \tag{5.38}$$

5.11.1 Concept of General Decentralized Control Method

In this part, it is assumed that in a specific time instant during system operation, $\mathrm{IN}_j^{Sh} > \mathrm{IN}_{ref}^{Sh}$. This means that excessive power is being absorbed by the input terminal of module j and to reduce the power level absorbed by the input terminal, more power should be transferred to the output terminal. In other words, $P_{o,j}$ needs to be increased. Based on the definition of d_j, the control system needs to increase d_j. Therefore, the time derivative of d_j should be positive i.e., $\frac{d(d_j)}{dt} > 0$. Now, if it is assumed that at some time instant during controller operation, $\mathrm{OUT}_j^{Sh} > \mathrm{OUT}_{ref}^{Sh}$, this means excessive power is transferred to the output side by module j and to help fix this issue, $P_{o,j}$ and consequently, d_j should be reduced by the controller. Therefore, $\frac{d(d_j)}{dt} < 0$. Concluding these two scenarios and noting that the f function in (5.36) satisfies $\frac{df}{d\left(\mathrm{IN}_j^{Sh}\right)} > 0$ and $\frac{df}{d\left(\mathrm{OUT}_j^{Sh}\right)} < 0$, if $f(\mathrm{IN}_j^{Sh}, \mathrm{OUT}_j^{Sh}) > f(\mathrm{IN}_{ref}^{Sh}, \mathrm{OUT}_{ref}^{Sh}), \frac{d(d_j)}{dt} > 0$. Therefore, (5.36) can be derived.

5.11.2 Example for General Decentralized Control

Fig. 5.15 shows a modular ISOP DC-DC converter system composed of N modules. The modular structure shown in Fig. 5.15 is supposed to charge a battery. In Fig. 5.14, the following notations are used: Each module operates with a duty cycle of d_i, and has an input capacitor of C_i, input voltage of v_{Ci}, input current of i_{ini}, and output current of i_{oi}, where $0 < i < N + 1$. As the modules outputs are connected in parallel, there is only one equivalent output capacitor C_o with an output voltage of v_o. This capacitor is connected to an inductive filter of L_o, which is in series with a battery. The duty cycle applied to a module is defined such that an increase in the associated duty cycle will increase the power transferred by the module. To

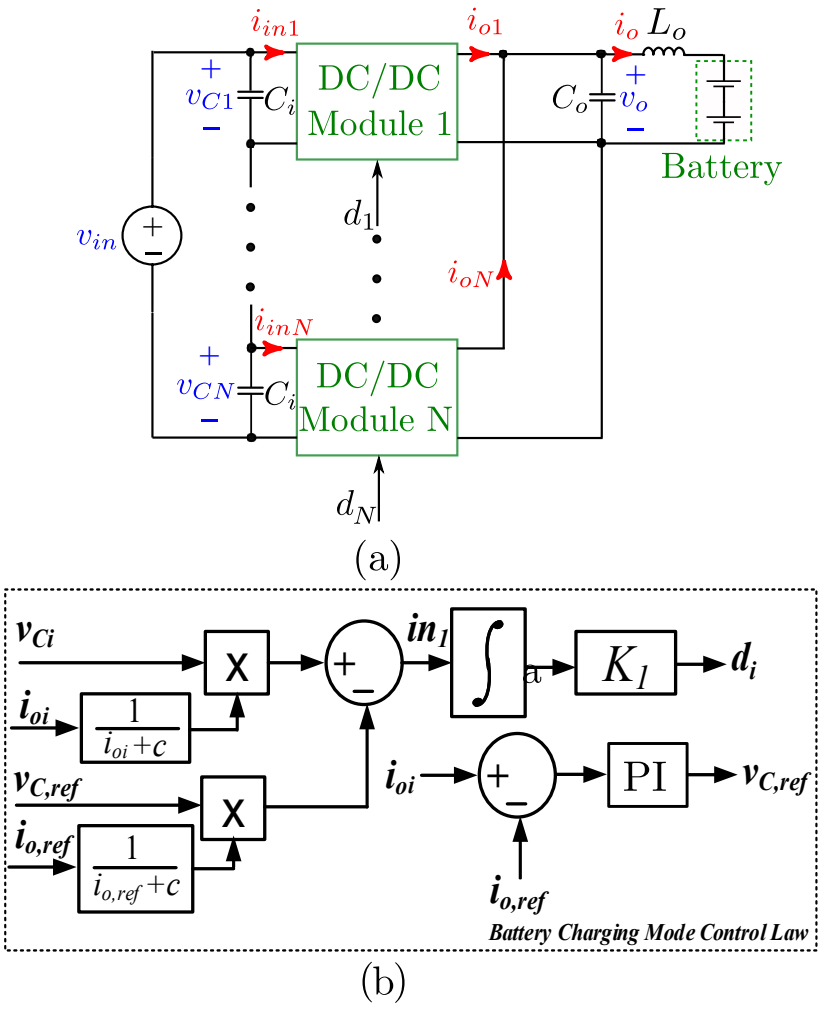


Figure 5.15: (a) Schematic of Modular ISOP DC-DC Converters (b) Proposed MODSAR Controller in Battery Charging Mode for i-th Module, $0 < i < N + 1$.

formulate the proposed MODSAR controller for the structure in Fig. 5.15, it should be noted that $\text{IN}_j^{Sh} = v_{Cj}$ and $\text{OUT}_j^{Sh} = i_{oj}$, due to series and parallel connection schemes in the input and output terminals. In this part, the reference values for IN_j^{Sh} and OUT_j^{Sh} are denoted by $v_{C,ref}$ and $i_{o,ref}$, respectively. Therefore, according to (5.36) and (5.37), the MODSAR controller is formulated as $0 < j < N + 1$:

$$d_j = k_1 \int \left(\frac{v_{Cj}}{i_{oj} + c} - \frac{v_{C,ref}}{i_{o,ref} + c} \right) dt, \; v_{C,ref} = \; k_{p1}(i_{oj} - i_{o,ref}) + k_{i1} \int (i_{oj} - i_{o,ref}). \tag{5.39}$$

In (5.39), $i_{o,ref}$ is set based on the reference total output power and the number of modules N. The constant number c is used in fraction denominators of (5.39), to prevent the denominator to change sign in case of battery discharging mode. The integrator applied to the term $(i_{oj} - i_{o,ref})$ in (5.39) sets $i_{oj} = i_{o,ref} (0 < j < N + 1)$ for all modules. This realizes accurate output power regulation and output power sharing for all modules. Next, the other integrator in (5.39) sets $\frac{v_{Cj}}{i_{oj}+c} = \frac{v_{C,ref}}{i_{o,ref}+c}$ for module i. As $i_{oj} = i_{o,ref}$ is already set by the first integrator, $v_{Ci} = v_{C,ref}$

Table 5.3: Comparison of the Proposed Controller and Other Existing Methods

Control Method	$\frac{\text{Sensors}}{\text{Module}}$	No Inter-Mod. Communication	Without Parameter Estimation	Decentralized	Not Toplogy Dependent	Trade-offs Eliminated	Applied Structures	Automatic Parameter Update
This Work	2	✓	✓	✓	✓	✓	ISOP,IPOS, ISOS,IPOP	✓
Linear Controllers [117, 118, 119]	2	✘	✓	✘	✓	✓	ISOP	✘
Common Duty Cycle [120, 80, 81, 82]	2	✘	✓	✘	✓	✘ power sharing vs. simplicity	ISOP,IPOP	✘
Droop [121, 7], [16, 122, 123, 124, 125]	2	✓	✓	✓	✓	✘ power sharing vs. regulation	ISOP,IPOS	✘
Master/Slave Control [126, 127, 128, 129]	1	✘	✓	✘	✓	✘ dynamics vs. reliability	ISOP,IPOP ,IIOP	✘
Nonlinear Control [71, 130, 131], [69, 132, 72]	2-3	✓	✘	✓	✘	✘ dynamics vs. robustness	IPOP,IIOP	✓
Peak Current Control [17, 133, 134]	2	✘	✓	✘	✓	✓	ISOP,ISOS	✘

is also achieved. By regulating v_{Cj} as $v_{Cj} = v_{C,ref}$ and putting it in the fraction numerator in (5.39), the proposed genral decentralized control approach minimizes overshoot/undershoot levels in input DC link capacitor voltage of module j during transients.

5.12 Comparison of Proposed General Decentralized Controller with Other Methods

This section provides a comparison table, which compares the performance and characteristics of the proposed general decentralized control method in this dissertation with other exsiting methods. In this regard, table 5.3 provides detailed comparison

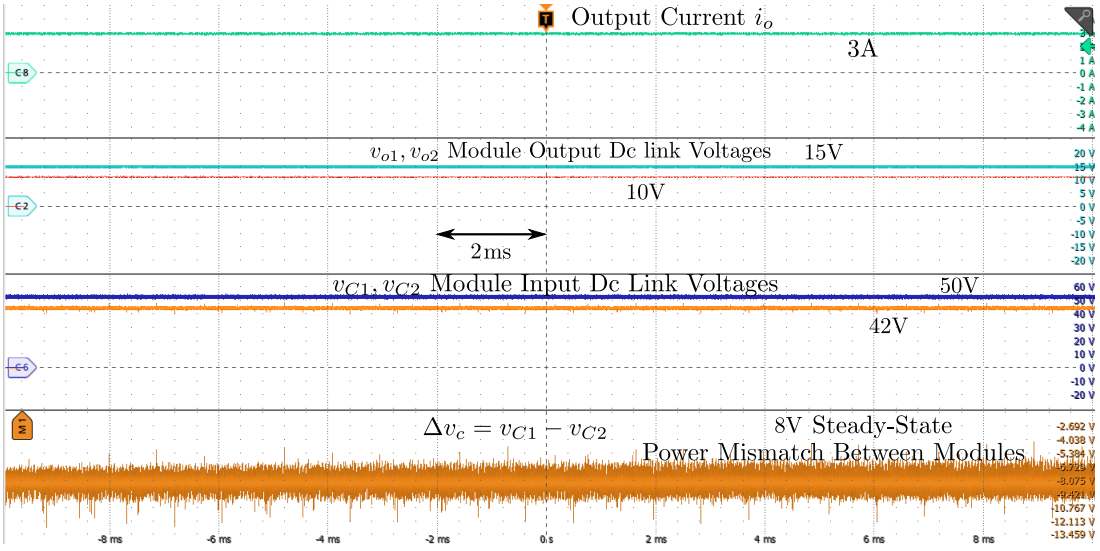


Figure 5.16: Open Loop System Response for 2 ISOS DAB Converters with Common phase Shifts for Both Modules: Output Current i_o, Module Output DC-link Voltages (v_{o1}, v_{o2}), Module Input DC-link Voltages v_{C1}, v_{C2}, $\Delta v_c = v_{C1} - v_{C2}$

between different control strategies based on different aspects. These aspects include number of sensors per module, intermodular communications, parameter estimation, controller structure in terms of whether it is decentralized, toplogy independency, trade-offs, applied structures, and automatic parameter update. As it can be observed from the table, the presented control approach uses 2 modules per sensor and does not use intermodular communications. Also, the controller is decentralized, does not use parameter estimation, and is topology independent. Finally, it facilitates automatic parameter update, eliminates trade-off, and is applicable to ISOP, IPOS, ISOS, and IPOP structures. As it can be seen from the table, other control methods lack at least two of these features. Therefore, the better performance of the presented method over other existing approaches is validated.

5.13 Experimental Results

This section presents experimental results to validate the performance of the controllerproposed for ISOS DC-DC converters. The experimental setup is composed of two ISOS DAB converters with a total input voltage of 100V, a battery load of 25V, input DC-link capacitancesof 11μF, output DC link capacitances of 70μF, tank inducatances of 25μH, and switching frequency of 70kHz. Fig. 5.16 shows the open loop response of the system, when identical phase shift values are applied to both DAB converters and the current charging the battery is 3A. As Fig. 5.16 illustrates, parameter mismatches between the two modules has caused 8V steady-state input DC link mismtach (power mismtach) between the modules in the open loop mode.

Fig. 5.17 shows closed-loop system response in steady-state, when the proposed controller is applied to both converters. As this figure shows, despite parameter

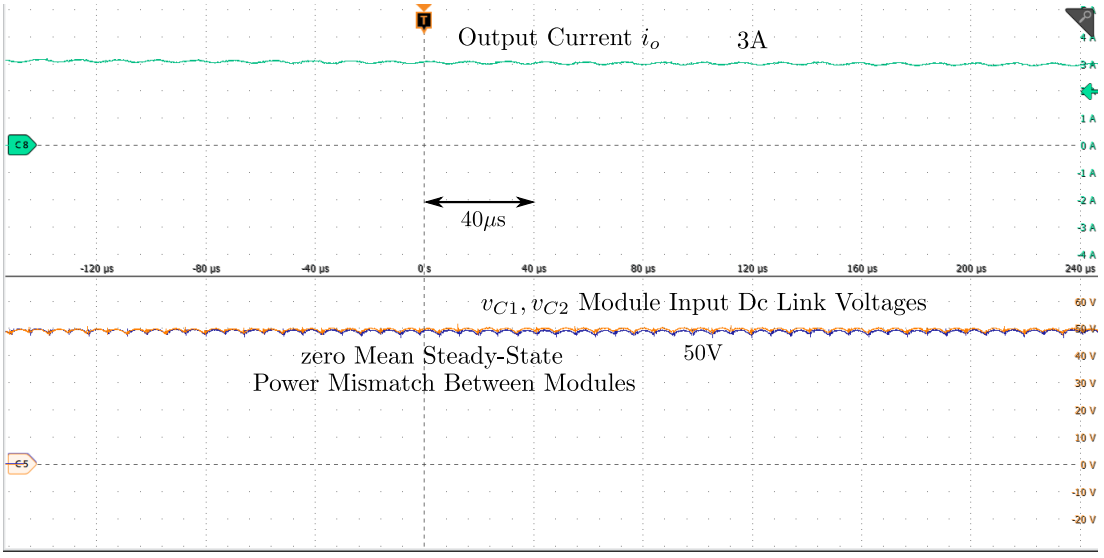


Figure 5.17: Closed Loop System Response for 2 ISOS DAB Converters with Proposed Decentralized Controller for Both Modules in 3A Load Current: Output Current i_o, Module Input DC-link Voltages v_{C1}, v_{C2}

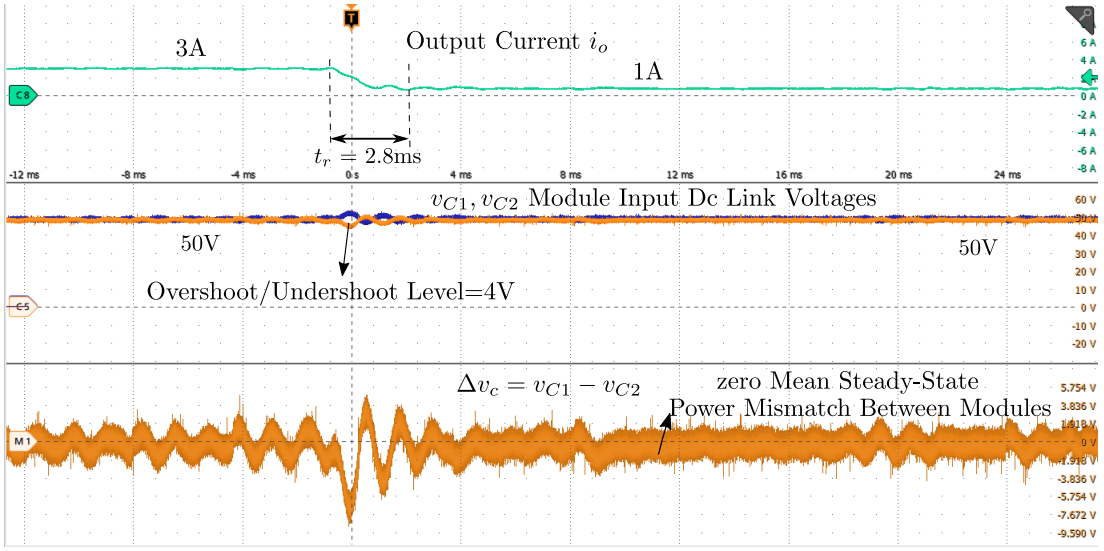


Figure 5.18: Closed Loop System Response for 2 ISOS DAB Converters with Proposed Decentralized Controller for Both Modules in 3A-to-1A Load Current Step: Output Current i_o, Module Input DC-link Voltages v_{C1}, v_{C2}, $\Delta v_c = v_{C1} - v_{C2}$

mismtaches between modules, both input DC-link voltages are 50V and there is zero steady-state power mismatch between the converters. Also, the battery current is 3A. Therefore, the controller has provided accurate reference tracking and power sharing between modules.

Fig. 5.18 shows the closed-loop system response for reference output current step from 3A to 1A. As this figure shows, the recovery time is 2.8ms and the controller has provided accurate reference tracking. Also, input DC link voltage over-

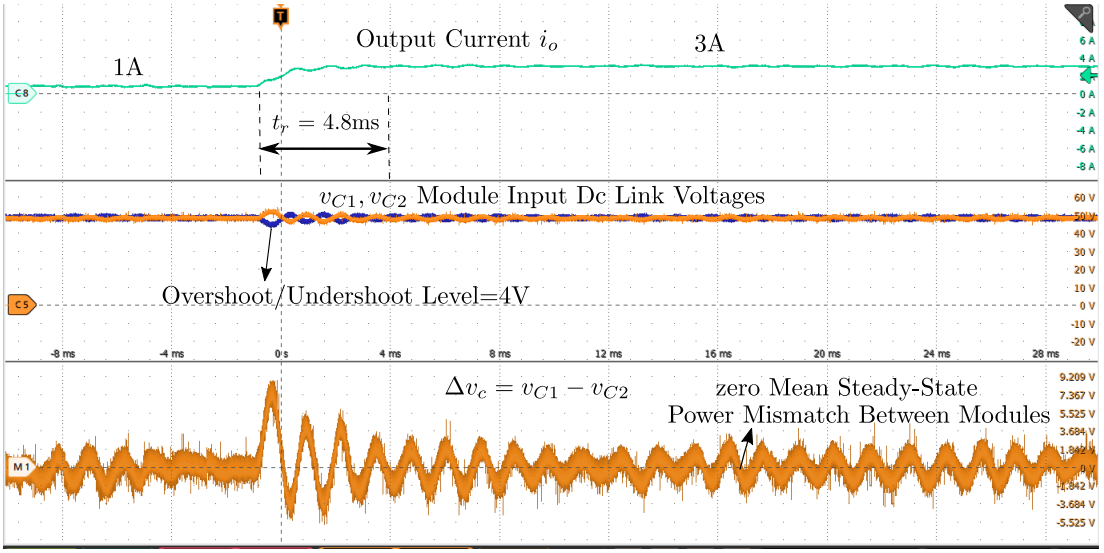


Figure 5.19: Closed Loop System Response for 2 ISOS DAB Converters with Proposed Decentralized Controller for Both Modules in 1A-to-3A Load Current Step: Output Current i_o, Module Input DC-link Voltages v_{C1}, v_{C2}, $\Delta v_c = v_{C1} - v_{C2}$

shoots/undershoots are 4V and there is zero mean steady state power mismatch between the two modules before and after the load step.

Finally, Fig. 5.19 shows the closed-loop system response for reference output current step from 1A to 3A. As this figure shows, the recovery time is 4.8ms and the controller has provided accurate reference tracking. Also, input DC link voltage overshoots/undershoots are 4V and there is zero mean steady state power mismatch between the two modules before and after the load step.

Chapter 6

Conclusion

6.1 Thesis Summary and Contributions

This thesis proposes novel controllers to improve the performances of single and modular DC-DC converters in power management systems of data centers. The power conversion system in data centers is investigated and divided into three power conversion stages namely stage 1-3. The proposed control methods are aimed to improve the performance indices of DC-DC converters in these three stages and solve the challenges associated to each conversion stage. These challenges include data center CPU speed limitations due to limited POL-connected converter dynamics in repetitive stochastic load steps, large voltage drops or overshoots in intermediate conversion stage due to large load steps, power sharing requirements, stability issues, etc. The targeted improvements include various steady-state and transient performance indices, such as load transient responses, overshoots/undershoots and recovery times, power sharing among modules, and finally output voltage/current regulation, in single and modular DC-DC converters. The main contributions of this thesis are summarized below:

(i) A controller is proposed based on Identical States Dynamics Control, to improve the load transient responses of DC-DC converters in stage 3 converters of data centers. This controller solves the challenge of limited CPU speed in data centers due to limited converter dynamical speed in repetitive stochastic load steps. The proposed controller can achieve load transient responses with recovery times of less than one switching cycle and low overshoot/undershoot levels. From the discussions in chapter 1, it can be concluded that the compromises between control objectives, controller stability, and the possibility to design the controller systematically, are among the most important concerns in designing a controller to achieve optimum load transient responses. To address these concerns, this dissertation proposes a design methodology and a new controller, which is specifically constructed to provide optimum load transient responses for DC-DC converters dealing with small load steps. This controller is developed for two different operation modes: Continuous Conduction Mode (CCM), and Discontinuous Condition mode (DCM). It is shown that the load transient responses are negligible in CCM, and fast transient responses with small overshoots/undershoots are observed in DCM. Unlike some of the existing

methods, the proposed controller does not require any additional auxiliary components, which reduces the total cost of the converter. Using the proposed controller, there is no steady-state error in the converter's output voltage and the voltage ripple levels always remain in the desired range. Also, the proposed controller has a simple structure and is robust against various uncertainties in the converter and it is shown that the values for voltage recovery time and overshoot/undershoot levels are optimal. Moreover, a systematic approach is proposed for controller design, that provides closed-form and optimal solutions. The proposed controller design procedures are applicable and can be extended to different types of converters, considering the stability and parameter variations. In this dissertation, performance of the proposed controller is validated by simulations and experiments.

(ii) To improve the load transient responses of DC-DC converter in large load steps in stage 2 converters of data centers, a controller is proposed based on the proposed principle of decoupling converter dynamics from the load. THis contoller solves the challenge of large output voltage drops and overshoots in intermediate stage due to large load steps inherited from the load-connected stage. The proposed controller can achieve DC-DC converters with less energy storage requirements. Also, it improves the load transient responses of DC-DC converters without requiring to use auxiliary circuits, resulting in a simpler system structure with a higher efficiency level. In fact, to overcome the problems mentioned in chapter 1, this dissertation proposes an alternative controller to optimize load transient responses of buck converters in large load steps. This controller decouples system dynamics from load resistance values. Hence, the performance of the proposed controller is not get degraded under large load steps. In addition, the controller reduces the total amount of energy stored in the converter to achieve lower converter sizes. In this dissertation, the controller's analysis and derivation are provided and the controller's performance is verified by simulation and experimental results.

(iii) A controller is proposed based on the Non-linear Function Error Tracking control, to improve the performances of IPOS/ISOP modular DC-DC converters in stage 1 converters of data centers. The proposed controller can improve the load transient responses of modular DC-DC converters, while improving the power sharing among the modules. Also, the proposed method can provide accurate voltage/current regulations and is applicable to all DC-DC converter topologies. It should be mentioned that the accurate performance of the controller is not affected by significant parameter mismatches among the modules and parameter uncertainties. The proposed controller improves the system dynamics in terms of both DC-link voltages of different modules and the output voltage, during load steps. This controller can operate for both resistive and battery loads and is capable of controlling the converter in both positive and negative load currents. The controller improves the system dynamics in wide load range applications and in transitions from the battery charging mode to the discharging mode or vice-versa. The controller performance and effectiveness is validated by simulation and experimental results. The experimental results present controlelr performance for two cases of two and three ISOP or IPOS DAB converters.

(iv) The proposed distributed control system for ISOP and IPOS DC-DC convert-

ers is generalized and applied to Input-Series Output-Series (ISOS) DC-DC converters in chapter 5. This modified control system solves stability challenges for ISOS converters as discussed in chapter 5. Moreover, a general analysis framework is proposed to systematically analyze system dynamics and stability in DC-DC converters. The performance of the proposed controller is compared with other methods in the literature and validated by simulation and experimental results.

(v) The accurate performances of the proposed controllers in this thesis are shown using experimental and simulation results. Also, stability analysis is performed for all the controllers and the performances of these controllers are compared with the existing ones in the literature. Finally, the process of controller design to reach controller objectives such as bandwidth and phase margin are discussed for the presented controllers.

6.2 Suggested Areas for Future Research

This section presents some areas in which the current research can be developed further.

(i) As the control concept proposed in chapter 4 is general, it can be applied to other converter types and modular configurations. A sample generalization process is presented in chapter 5 for ISOS DC-DC converters. One of the possible areas towards which this research can be continued in to extend the control system introduced in chapter 4 to other conversion systems. Example include Input-Parallel Output-Parallel (IPOP) DC-DC converters and inverters.

(ii) The concept of decoupling converter dynamics from the load was introduced in chapter 1 and 3 for a single DC-DC converter. This method can be extended to modular DC-DC converters. Such extension will enable better system dynamics and power sharing for modular DC-DC converters, especially in large load steps.

(iii) If a centralized control system is used to control modular DC-DC converters, the concept of identical states dynamics control introduced in this thesis can be applied to the system. This will regulate all DC-link capacitor voltages at their reference values using same dynamical properties, resulting in better transient ans steady-state power sharing aming modules.

(iv) The application of the proposed control system for modular DC-DC converters in data centers can be studied in other applicatons such as HVDC systems, electric vehicles, etc.

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