Dynamics and Sensitivity Analysis of a Voltage-Source Converter Connected to a Weak Grid

by

Wael Abdulwahab Telmesani

A thesis submitted in partial fulfillment of the requirements for the degree of

Master of Science

in

Energy Systems

Department of Electrical and Computer Engineering
University of Alberta

Abstract

As the call to action on global warming is rising yearly, the integration of renewable and clean energy resources in the energy sector is gaining high interest. In grid-tied converter applications, power system stability becomes very sensitive in weak grid conditions. Due to the penetration level of the integration of renewable energy resources and the rapid increase of converters in power grid systems, preserving the overall system stability becomes a vital objective. In such demanding applications, controlling the voltage of interlinking DC-link capacitance is crucial to preserving system stability. Furthermore, the DC-link capacitor is a critical component because it determines the stability and dynamic performance in such systems. This critical element might face uncertainty due to loading/and unloading on the DC-side or changing in ambient temperature but not limited to these factors. Therefore, this thesis aims to develop a comprehensive analysis to investigate the dynamic interactions between the DC-link capacitance uncertainty and different grid strength conditions in inversion and rectification modes of operation. This study considers the influence of controller bandwidths, grid-angle variations, and AC-side faults under the dynamics of DC-link capacitance. In addition, the impacts of grid-side parameters that maintain the system stability in weak-grid conditions have been investigated. This thesis addresses the interaction dynamics by linearizing the nonlinear grid-connected voltage source converter (VSC) system around a certain equilibrium point. To capture the stability of the system dynamics, a small-signal state-space model is derived from the linearized model. To validate the analysis results, the small-signal was verified with the time-domain model under a MATLAB/Simulink environment. The results demonstrate that, at a stiff grid condition, the influence of the DC-link capacitance variations did not significantly affect system stability in inversion and rectification modes as it did in weak grid conditions. Furthermore, at weak grid conditions, increasing the DC-link capacitance and controller bandwidths enhanced system stability in the inversion mode and degraded stability in the rectification mode, except when increasing the bandwidth of the AC-voltage controller. Regarding the effect of the grid-angle variations at short circuit ratio (SCR) < 3, increasing the grid angle and decreasing the DC-link capacitance leads to worse stability conditions in the inversion mode and vice-versa for the rectification mode. In terms of fault assessment, the settling time increased when the DC-link capacitance decreased after the fault was cleared in

inversion mode at $SCR < 3$. At the same level of SCR, the system becomes less capable of overriding the fault when the DC-link capacitance increases in rectification mode. Regarding the grid impedance and AC-line inductance filter, grid inductance is not the only factor influencing system stability; the grid resistance also had an effect. In addition, the results revealed that a slight variation in AC-line inductance can significantly affect system stability, especially at a very weak grid condition. In conclusion, the effect of the DC-link capacitance uncertainty on system stability is higher in the rectification mode than in the inversion mode, in weak grid conditions. In addition, the selection of the DC-link capacitance depends not only on the ripple percentage in the DC-bus voltage but also on the grid strength level, which can affect system stability.

Dedication

This work is dedicated to my great parents and family. I also dedicate this dissertation to my lovely wife Rana and my heart Nahlah.

Muhammed Ali, "*I hated every minute of training, but I said, don't quit. Suffer now and live the rest of your life as a champion*"

Vince Lombardi, "*Winners never quit, and quitters never win"*

Albert Einstein, "*Life is like riding a bicycle to keep your balance you must keep moving*"

Al-Hasan Al-Basri, "*You are no more than a few days whenever a day passes, a part of you passes away*"

Tony Robbins, "*No matter how many mistakes you make or how slow you progress, you are still way ahead of everyone who is not trying"*

Plato, "*Never discourage anyone who continually makes progress, no matter how slow"*

Albert Einstein, "*In the middle of difficulty lies opportunity*"

Acknowledgements

First of all, I want to thank God for giving me the opportunity to achieve this work.

I would like to express my gratitude to my advisors Prof. Yasser A.-R. I. Mohamed and Dr. Amr Ahmed A. Radwan for their guidance during the entire process of my MSc studies. I appreciate their patience, insightful discussions, valuable feedback that led to the completion of this research.

It was my honor to have been educated by leading professors in the area of Energy Systems at the University of Alberta. Also, I would like to express my thanks to the examiners committee Prof. Dinavahi and Dr. Liang, and the chair Prof. Karumudi for their valued time and interests in my thesis.

I would like to extend my deepest gratitude and respect to my whole family, especially my lovely parents for their continuous support and encouragement during my studies. Indeed, I owe all the success in my life to them. I ask God to protect and reward them for everything they did for me. Also, I ask God to forgive me for bothering them during my difficult time completing this work. Without them, I would never have reached this great moment. In addition, I would like to thank my uncle Dr. Ammar and my brother Dr. Amr Telmesani for their continuous motivation and encouragement to obtain my degree.

I am so grateful for my wife Dr. Rana and my lovely daughter Nahlah for their patience during my research. They are always the source of my motivation to work. Truly, no words can express my appreciation and this achievement would not be possible without them. I ask God to bless and reward them.

I would like to extend my gratitude to my friends, especially Dr. Amr Munshi for his support. Finally, I would like to acknowledge the financial support provided by Umm Al Qura University.

Table of Contents

List of Figures

List of Tables

List of Acronyms

VSC	Voltage Source Converter
CSC	Current Source Converter
DERs	Distributed Energy Resources
DG	Distributed Generation
PLL	Phase Locked Loop
dq	rotating reference frames known as Direct-Quadrature
$\alpha\beta$	stationary reference frames known as alpha-beta
$Bw_{cc,dc,ac,PLL}$	Bandwidth of current, DC-link voltage, AC-voltage and PLL controllers, respectively
PWM	Pulse Width Modulation
DC	Direct Current
L-L	Line-to-Line
L-G	Line-to-Ground
AC	Alternating Current
rms	Root Mean Square
PI	Proportional Integral compensator
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
ESS	Energy Storage Systems
PCC	Point of Common Coupling
SCR	Short Circuit Ratio
LCC	Line-Commutated Converters
THD	Total Harmonic Distortion
DFIG	Doubly-Fed Electric Machine
PMG	Permanent Magnet Generator
FACTS	Flexible AC Transmission Systems
STATCOM	Static Synchronous Compensator
HVDC	High-Voltage Direct Current

Chapter 1

Introduction

1.1 Background and Motivations

In modern civilization life, energy is considered an integral part of comfort. Among several form of energy, electricity is the most often used in a modern life. Therefore, the electricity is representing one of the most essential elements in our life, which almost no basic facilities such as universities, hospitals and industries can operate without the existence of electricity. Thus, researchers and industries are working in energy sector development relentlessly to meet the electricity global growth demand that became a life priority. Although generate the electricity by a conventional way can meet the accumulated growth demand but it has a significant impact on environment [1].

Due to global environmental and economic challenges in the energy sector, the concept of distributed generation (DG) has been emerged and gaining more interest [2]. Shifting the energy production from remote areas into residential areas is one of the characteristics that make renewable resources more attractive compared with conventional ones. The advancement of power electronics converter technology plays a pivotal role in facilitating the integration of renewable resources into the utility-grid [3]-[5]. As a result, the new capacity installed of distributed energy resources (DERs) has increased by approximately 90% from 2001 to 2019 as shown in Fig. 1.1 [6]. This figure clearly shows the rapid deployment of renewable energy compared with conventional energy resources over years. Several type of power electronics converters are presented in the literature, where the type and power rating of applications usually determines the suitable selection of converter. Currently, the Voltage Source Converter (VSC) is dominated the markets due to several merits like high efficiency, high reliability and cost effective which makes it more attractive [7]. The other remarkable reasons for this rapid deployment are devoted to microgrids [8],[9]. Microgrids are an efficacious method for integrating sources such as photovoltaics, wind, and energy storage systems (ESS) with modern electric loads such as computers and telecom systems. In addition, they can be installed in the middle of the city rather than in remote areas [10]. Among several types of microgrids, the propagation of DC microgrids is rapidly increasing as they have several benefits over other microgrids. Complicated control

strategies, bulky transformer utilization, and less efficient short-circuit protection in AC microgrids make the DC microgrids more favorable [11]. Furthermore, the majority of modern applications, including DERs, electric vehicles, motors, and computers, are inherently DC type-based, which means no additional converters are needed. Indeed, the key elements to deliver and receive active and reactive power in microgrids are converters.

Predominantly, power electronics applications require a DC-link stage for interconnection between the DC and AC sides. The importance of DC-link capacitance is considered in improving the density of energy system and diminish some physical challenges like filtering converter switching ripples [12]. The DC-link capacitor is a critical component in power converters applications, as it determines the stability and dynamic performance [13]. Hence, a slight deviation in the DC-link capacitance range might lead to a power imbalance in the system caused by DC-bus voltage variation [14]. Furthermore, this deviation could induce dynamic stability issues.

In AC systems, the stiffness of the grid is determined by its impedance at the Point of Common Coupling (PCC). The system is defined as weak if the AC system impedance is higher than the converter input DC power. In other words, to determine the stiffness level of the AC grid, a Short Circuit Ratio (SCR) of the grid is used as a quantifying measure [15]. The SCR can be defined as a ratio of the AC-grid short circuit capacity to the generated power at the DC-link. Therefore, the power grid is categorized as stiff when $SCR > 3$ and weak when $2 \leq SCR \leq 3$ [16]. It is worth mentioning that the long distance of connections between the DERs and utility grid is the main reason for causing the weak grid condition [17]. It is well known that the system stability becomes very sensitive in weak grid conditions.

As the penetration level of integration of renewable energy resources and converters increases rapidly in power grid systems, preserving the overall system stability becomes a vital objective. In grid-connected power electronics applications, controlling the voltage of interlinking DC-link capacitance is crucial to preserve system stability. Furthermore, the DC-link capacitor itself is a critical component, as it determines the stability and dynamic performance in such systems as well. Therefore, careful attention should be paid to regulating the DC-bus, especially in a weak grid condition. For this reason, the main focus of this work is developing a comprehensive analysis to investigate the dynamic interactions between the DC-link capacitance uncertainty and different grid strength conditions. It has to be mentioned that the source of the uncertainty in the DC-link capacitance could be occurred due to several reasons such as variable loading/sources conditions

in the DC-side or changing the ambient temperature. This study can be also highly beneficial for both: a) industries that are dealing with film DC-link capacitance instead of electrolytic capacitance, and b) DC-microgrids encountering uncertainty in the DC-link capacitance for various reasons as mentioned earlier.

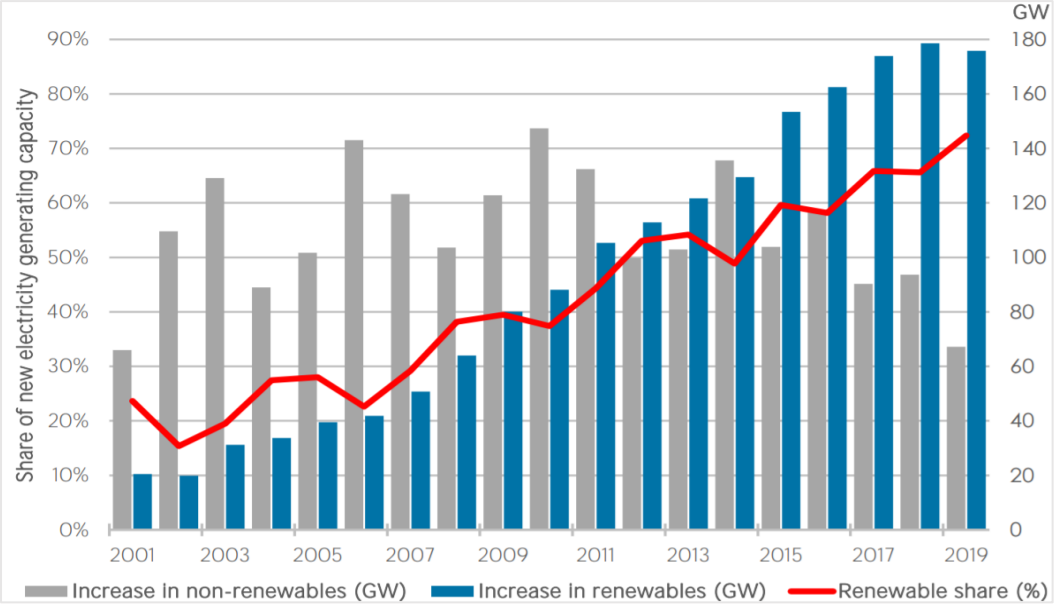


Figure 1.1 Growth of renewable energy resources generating capacity

1.2 Research Objectives

This research aims to conduct a comprehensive modeling and analysis of the dynamic interactions of the VSC connected grid under inversion and rectification modes. The key objectives of this thesis can be epitomized as follows:

1. Designing a grid-connected VSC system with controllers in detail and implementing the system in a MATLAB/SIMULINK environment. Further, developing an accurate state-space small-signal model for the grid-connected VSC in different operating modes.
2. Conducting a thorough stability analysis of VSC connected to weak and very weak grid using linear analysis tools such as eigenvalues, participation factors, and bode-plots.

1.3 Thesis Contributions

The contributions of this work can be summarized as follows:

- Studying the interaction dynamics among different grid strengths and the uncertainty in a DC-link capacitance that could occur due to the variable loading/sources conditions in

different operating modes, to show that the sizing of the DC-link capacitor of VSCs at weak grid conditions is very critical and might induce severe instabilities.

- Investigating the interaction dynamics of grid angle, AC-side fault and controllers' bandwidth, with the dynamics of the DC-link capacitance uncertainty under weak grid conditions in inversion and rectification modes.
- Exploring the limitations of AC filter and grid impedance parameters on the stability of the weak grid-connected converter system in inversion and rectification modes.

1.4 Thesis Layout

The reminder of the thesis is organized as follows:

Chapter 2 introduces conventional power system limitations and the advancement of power electronics technology. A review of the VSC in terms of principles, operations, and essential control strategies is shown. Furthermore, this chapter includes a comparison of the system structure and operation of the VSC and the CSC. A literature review of a dynamic interaction analysis for the VSC connected to different grid strength conditions is reported.

Chapter 3 presents the methodology used for analyzing the grid-connected VSC system under different conditions. In this chapter, a description of the studied system is provided. Moreover, the structural diagram of the studied system with its nominal parameters is also presented. This chapter includes a detailed discussion of the essential controllers' design that is applied in this study. In order to conduct the analysis, a large signal model for the grid-connected VSC is provided. From this model, a complete detailed state-space small-signal model that represents all the dynamics of the system is derived. Lastly, this chapter includes a validation of the small-signal model against the simulation model under different grid strength conditions in both inversion and rectification modes.

Chapter 4 provides the analysis and evaluation results of the dynamic stability interactions between the DC-link capacitance and the grid in different strength conditions. Furthermore, the stability analysis also considers the impact of controllers' gains, grid angle variations, fault and grid filters in accordance with the dynamics of DC-link capacitance that are presented.

Chapter 5 consists of the summary and conclusion of the thesis, as well as suggestions for future work related to this framework.

Chapter 2

Background and Literature Review

2.1 Introduction

This chapter presents the literature review and explains some methods, principles and semiconductor technology that are used in this research. The limitations of conventional power generation, such as gas and oil, are discussed in this chapter to justify the importance of using renewable energy. Recently, the rapid growth in renewable energy has been mostly due to the contributions of power electronics technology, the advancement of which will be discussed in this chapter. The principles and operations of VSC are also presented, as well as a comparison between VSC and Current Source Converters (CSC). Finally, the most recent related work is reported in this chapter in order to point out the limitations that are covered by this work.

2.2 Limitations of the Conventional Power System

The conventional power system refers to power that is generated by fossil fuels such as oil, coal, or natural gas. These energy sources have been used for well over a century and have several advantages such as cost-effectiveness, well-established infrastructure, and widespread use. Despite these advantages, there are several drawbacks that necessitate consideration [18]. The main concerns of this type of energy source are related to environmental and operational issues. Regarding the environmental issue, burning oil, coal or gas to generate electricity is the main reason for the increasing levels of carbon dioxide (a potent greenhouse gas) and sulphur dioxide in the atmosphere that contribute to global warming and acid rain, some statistics can found in [19], [20]. Several studies show that continuing to rely on these resources will eventually threaten the environment [2]. In terms of operational concern, several factors reduce the reliability of the conventional power system, including unidirectional power flow and centralized power generation as shown in Fig. 2.1; any failure in this radial cascaded system could lead to major power outages. For example, in 1996, two major power outages occurred in North America affecting millions of consumers because of damage to a single cable [21], [22]. Additionally, the overall stability of such systems is greatly affected by variations in voltage and frequency that could be caused by load changes. Conventional power stations are normally centralized (installed in remote areas), which increase the power losses, due to their bulk sizes and generated pollution [23].

Currently, the energy industry is striving to alleviate and mitigate the drawbacks of conventional power systems while attempting to meet growth in both global energy demand and environmental issues. Integrating renewable energy sources, such as solar and wind, within the utility grid is one promising solution that could meet these objectives. The integration of these renewable energy resources introduces new operational concepts known as microgrids and smart grids [10]. The decentralized characteristics of these new operational concepts greatly increase the reliability of the network, unlike the centralization of conventional power systems.

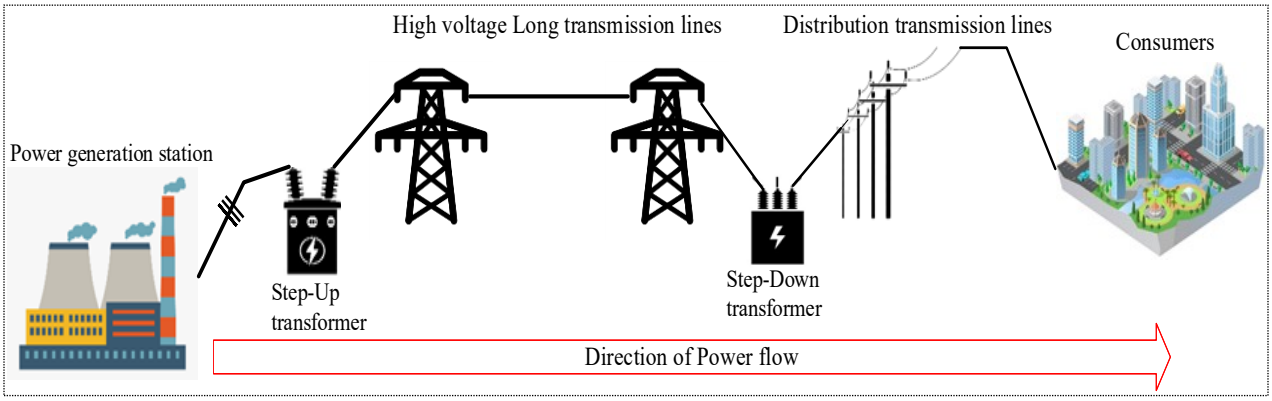


Figure 2.1 Network of conventional power grid structure

2.3 Advancement of Power-Electronic Switches

The advent of power electronics plays a significant role in ensuring the rapid deployment of renewable energy resources. The advancement of switch and converter topologies of power electronics technology represents a pivotal shift in facilitating the integration of renewable resources such as photovoltaic cells and wind energy with the utility [4], [5] this technology has become the gold standard for most of the leading industrialized countries. Recently, high-speed converter switches and real-time computer controllers have emerged as the two main factors that contribute to the deployment of power electronics technology [24]. Nevertheless, the future of the electrical grid market will be dominated by power electronics devices [25].

In general, modern power electronic converters consist of two main components. Firstly, power semiconductor switches and auxiliary components (i.e., passive components) that can be represented as action executor parts, and secondly, control systems that contain microelectronic control chips that induce and deliver the commands to the executor [26], [27]. The switches are an indispensable part of any power electronic converter and improving these switches can lead to improvements in the efficiency and size of the power systems [28]. The switches, generally, are

classified into two types: electronic (or semiconductors) and mechanical [29]. Most of the power electronic converter applications use electronic semiconductor switches rather than mechanical ones. This is due to the semiconductor switches being characterized by long lifetimes and high-speed repetitive switching [30]. Different power electronic semiconductor switches have been introduced in the literature. The most commonly power electronic switches used in medium and high-power applications are Integrated Gate Commutated Thyristor (IGCT) and Insulated Gate Bipolar Transistor (IGBT) [31],[32], which consider in this work. Table 2.1 presents a comparison between both switches based on their key characteristics.

Table 2.1: Comparison of the characteristics of IGBT and IGCT semiconductor switches [33]-[36]

Elements of comparison\Device	**IGBT**	**IGCT**
Invented	1980s by Baliga	1990s by ABB
Semiconductor Switches Family	Transistor	Thyristor
Applications	[1]Low to medium voltage (VSCs)	Medium to high voltage (CSCs)
Voltage Ratings	3.3 kV	4.5 kV
Current Ratings	1.2 kA	3.1 kA
Gate Drive Power Losses	Low	Low
Cost ($)	Low to medium	Low
Active Clamping Circuit	Needed	Not needed
Limiter for Short Circuit Current	Needed	Not needed
Safety Against Short Circuit	Lower	Higher

[1] *It can also be used in high-voltage applications, but it is most commonly applied in low and medium voltage applications*

As this research is concerned with studying dynamic stability, further details and features of these semiconductor switches have been omitted, more information can be found in [37], [38]. Furthermore, extensive and ongoing research is being conducted on improving the characteristics of semiconductor switches to increase their efficiency.

2.3.1 Power Converters and Power Electronic Converters' Applications

Power converters generally consist of several semiconductor switches that are connected in a certain manner to achieve the desired function, such as boosting voltage, through injecting the gating signal generated from control units. Predominantly, the merits of power converters, such as current flow capability, are determined by the characteristics of semiconductor devices as mentioned earlier. One of the main functions of power converters is facilitating energy exchange

between systems [3]. In other words, the power converters in power systems are considered to be a bridge for exchanging energy. As power converters are used in many modern power system applications, these converters are classified into four types based on the forms of energy transformation that determine by the host electric system interfaced [39] :1) AC to DC (Rectifier), 2) DC to AC (Inverter), 3) DC to DC and 4) AC to AC. Furthermore, the converters can be classified based on the commutation process into, a) line-commutated converters or b) force-commutated converters [40], [41]. In line-commutated converters (LCC), the commutation process is done by relying on voltage reversal polarity. The converter switches are not capable of a switching off process. This converter type is often favoured to use in high-power applications. Force-commutated converters are more popular due to having converter switches that are capable of fully controlling the process of switching on and off. Additionally, some other advantages mentioned in [42] make the force-commutated converters more favourable and attractive for industrial requirements.

The definition of power converters in the previous section is confined to semiconductor switches. However, in power converters systems applications, systems consist of one or more power converters and control units in order to gain the desired functions. Power electronics converters are inevitable in most energy systems and renewable energy applications. Thus, power electronics contribute greatly to improving the applications that are used in the market nowadays, such as FACTS, STATCOM, back-to-back HVDCs, grid-connected DC/AC converter systems and systems that interface renewable energy resources to the utility grid. Furthermore, the role of power converters also extends to facilitating the growth of smart grids and microgrids that could mark a revolutionary change in today's energy sector. As the concept of microgrids has rapidly gained traction, as well as greatly contributing to spreading and expanding green energy resources, it is worth giving a brief introduction as to how this concept operates.

Based on ABB, microgrids can be defined as an electrical network containing distributed resources (i.e., photovoltaic, wind), electrical energy storage systems, and loads that can be worked when connected or completely disconnected from the main utility grid [43]. This means that power plants can now also be installed closer to populated areas, which can increase their efficiency, reliability, stability and flexibility. By applying this concept, consumers can have access to two types of power sources: one from distributed resources and one from a regular utility network. In case any disturbances occur in one of these sources, the other one can cover without interruption

[44], [45]. Microgrids can be categorized into different types such as AC, DC, and hybrids microgrids. Currently, the propagation of DC microgrids is rapidly increasing owing to several advantages that they have over other types. Complicated control strategies, bulky transformer utilization and less efficient short circuit protection in AC microgrids make the DC microgrids more favorable [11], [46], [47] Furthermore, most of the more widespread modern applications, such as DERs, electric vehicles, motors, and computers, are inherently DC, meaning that no additional converters are needed.

In power converters applications, it should be pointed out that the functions of the power converters can facilitate the exchange of power and can also enhance power quality and stability as well as maximize the power transfer capability and efficiency. Among several power electronics converters, VSCs are most widely used in industries, so more details about VSCs are provided in the next section.

2.4 Voltage Source Converter (VSC)

A concept and operation of VSC, and comparison between VSC and CSC converters are presented in this subsection. Further, the control strategies of VSC will be presented as wee. One should mention that the limited applications of the CSCs mean that VSCs predominate in the markets [48], [49]. Based on this fact, this work only considers the VSC, with CSCs being beyond the scope of this thesis. However, more details of CSCs can be found in [50]- [52].

2.4.1 Concept and Operation

Concept: The main semiconductor switch cell of a VSC is IGBT connected with an anti-parallel diode, which is considered a bipolar and bidirectional switch and is shown in Fig. A.2.1 in Appendix. Additionally, this switch cell is categorized as a force-commutated switch, which makes it more attractive compared with line-commutated converters. The general concept of VSC configuration is derived from the idea of a combination of DC-DC boost and buck converters. As clarified in [42], [53], combining both DC-DC converters forms the basic configuration of the half-bridge VSC, which can deliver power in two directions (bidirectional power flow) as shown in Fig. 2.2. In VSCs, the DC-side is considered a constant voltage source, so it can exchange power between subsystems by changing the polarities of the DC-side current; this represent the basic concept of VSC.

Operation: Based on the switching operation, VSC can be categorized into three types [54]: a) pulse width modulation (PWM), b) square wave, and c) voltage cancellation converters. As the first type is the commonly used, the other types will not be discussed. In this work, a three-phase two-level VSC has been considered, but for the sake of simplicity the operation of two-level VSC is explained in a half-bridge, single phase depicted in Fig. 2.2. It is called two-level due to the switched voltage in AC-side changes between two values only which are $+V_{dc}/2$ and $-V_{dc}/2$. Further, it is worth mentioning that the VSC can be extended to multilevel converter through adding more semiconductor switches and/or connecting more legs, then form them in a certain topology. The principle and mechanism of sinusoidal PWM (a type of PWM) is presented in Fig. A.2.2, which shows that the switching pattern is developed based on a comparison of the modulating signal (reference signal) with a carrier signal (periodic triangular signal).

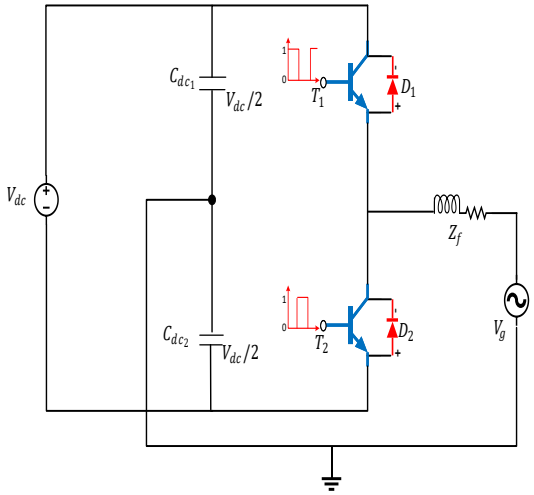
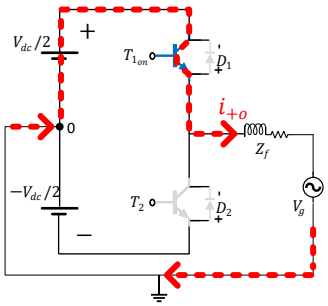
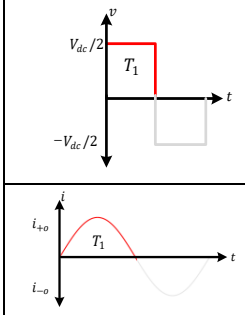
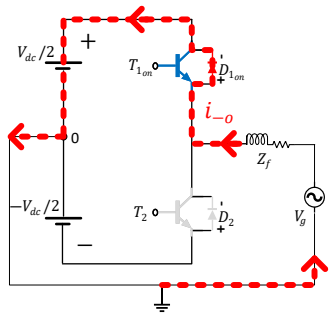
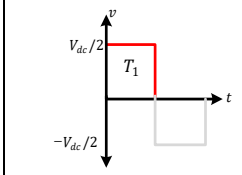
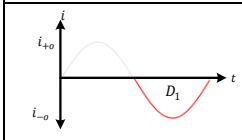
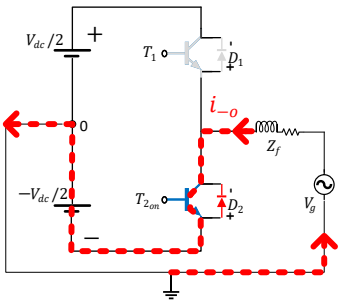
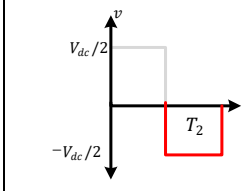
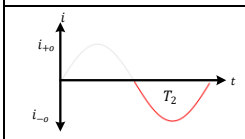
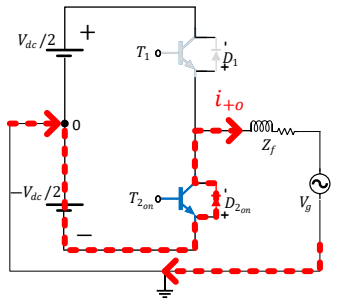
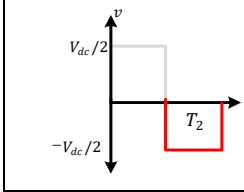
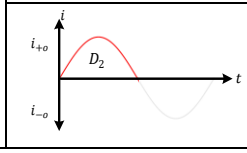


Figure 2.2 Diagram of bidirectional, single phase, one-leg, two-level voltage source converter (VSC).

It is worth mentioning that the VSC works based on the command received by PWM, which is responsible for controlling the frequency and magnitude of the output AC voltage through varying the pattern of modulation. The operation of VSC for transferring power is clearly illustrated in Table 2.2. In each case the type of power transfer, state of switch and conducting element are presented. From the four cases showed in the table, it can be noted that the VSC can works in the four quadrants which are leading and lagging power factor rectifier and leading and lagging power factor inverter.

Table 2.2: Concept of power transfer in single-phase one-leg VSC based systems

Half-bridge VSC	Waveforms	Status	
		Power transfer	DC to AC (**inversion**)
		State of switch	T_1 ➔ on , T_2 ➔ off
		State of diodes	D_1 ➔ off , D_2 ➔ off
		Conducting element	T_1
		Power transfer	AC to DC (**rectification**)
		Position of switch	T_1 ➔ on , T_2 ➔ off
		State of diodes	D_1 ➔ off
		Conducting element	D_1
		Power transfer	DC to AC (**inversion**)
		State of switch	T_1 ➔ off , T_2 ➔ on
		State of diodes	D_1 ➔ off , D_2 ➔ off
		Conducting element	T_2
		Power transfer	AC to DC (**rectification**)
		State of switch	T_1 ➔ off , T_2 ➔ on
		State of diodes	D_2 ➔ off
		Conducting element	D_2

2.4.2 Control Strategies

As mentioned, the power converters consist of semiconductor switches and control units. This subsection clarifies the control strategies for VSC. Fine controlling the active and reactive power flow has a pivotal role in stabilizing the operation of any power system [55]. However, different

control strategies have been proposed in the literature to exchange active and reactive power with an AC system through VSC technology. Vector control technique is the most widely used for such systems compared with direct power control (DPC) technique. Two main drawbacks make the former technique more favorable than the latter. First, the DPC control does not have an inner current controller by which the coupling between active and reactive power increases and does not depend on the PWM modulator strategy [56]-[58]. Second, the switching frequency varies depend on the operating conditions of the system, such as the power and controller bandwidth. It is also difficult to evaluate the power loss of the VSC as well as designing the AC filters as the broadband harmonic varies broadly that makes it difficult to be determined [59]. This drawback leads to large AC filters such as bulk inductances having to be used, which means high power losses and high costs, in order to avoid high harmonics entering and damaging the system. For this reason, the vector control technique is considered in this work.

The principle of vector control is the conversion of the AC three-phase (ABC frame) into a space phasor vector, which is rotated in a complex plane as seen in Fig 2.3. This space phasor vector contains the information necessary for a three-phase frame, namely amplitude, frequency, and phase-angle. For the sake of facilitating control design and analysis, it is preferable to map the transformed space vector by using real and imaginary orthogonal vectors, which are considered to be two-dimensional frames [60]-[62]. The literature shows that these two-dimensional frames can be classified into stationary and rotating reference frames known as alpha-beta ($\alpha\beta$) and direct-quadrature (dq) frames, respectively.

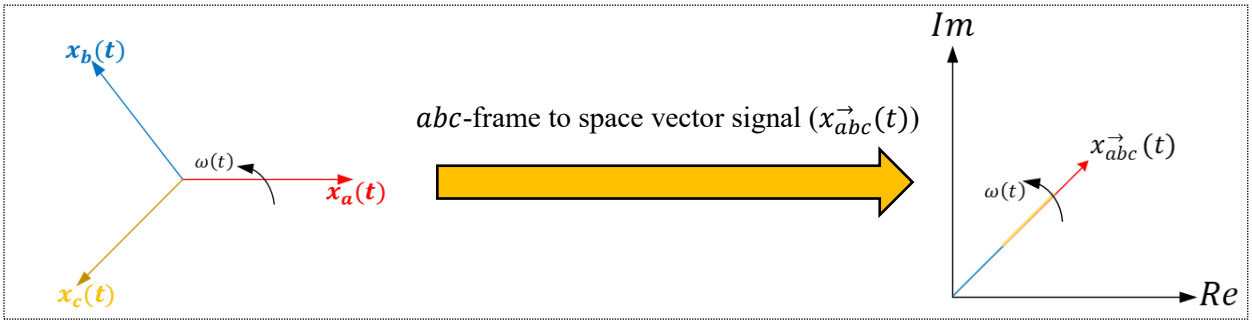


Figure 2.3 Representation of three-phase components into two orthogonal components

In order to convert the three-phase quantities into stationary and rotating reference frames, the well-known Clark and Park mathematical transformations are needed, as clear in Appendix (A.2.1)-(A.2.3). Further, Fig. A.2.3 shows the representation of three-phase into two components in axes form.

For control purposes, it is preferable to track DC components by using simple control like (PI) rather than variable components that need a more complicated control like proportional resonant (PR) [63]. The rotating reference frame, as a result, is broadly used in VSC applications [27], [64].

It is worth mentioning that there are two types of vector control, which are vector voltage control and vector current control. The latter is the commonly used and will be discussed in the next subsection, while the former is predominantly applied in high-power applications.

2.4.2.1 Vector Current Control (Current mode control)

Vector current control is the most widely used control for several VSC applications such as the grid-tied VSCs application. Unlike the voltage control mode, this control technique controls active and reactive power based on line-current phase-angles and amplitude due to the existence of the inner current controller, which will be discussed in the next chapter. This control strategy was characterized by previous controls by having an inner current controller. This provided several advantages, including protection against overcurrent, precise decoupling, and the controlling of active and reactive power and higher dynamic performance [65]. Due to these merits of inner current mode control, it is considered in this framework.

The first step to apply the vector current control is applying the frame transformation to the AC three-phase signals. Among the frame transformation methods mentioned earlier, the dq frame representation is taken into account. In the dq frame, however, the way to communicate the converter with an integrated system (i.e. utility grid) is using some synchronization control techniques that are obligatory in weak grid and can be neglected in stiff grid [66], [67]. A great deal of research has been conducted in the area of synchronization control, but phase locked loop control (PLL) has become the dominant control technique due to its simplicity [68]. As this research is focused on weak grid condition, details of the PLL control are presented below.

- *Phase Locked Loop (PLL)*

Unlike other types of converter, such as a DC-DC converter, grid-connected converter systems need to synchronize with the utility grid [69]. Therefore, different synchronization techniques, such as the synchronous reference frame phase locked loop control (PLL) and power synchronization control, have been introduced in the literature [70]-[72]. PLL, rather than other types, is the most common strategy used as mentioned [73]. To clarify the concept of the PLL technique, the converter control is virtually represented by two dq_s frames. These frames can then

be divided into grid and controller (VSC) reference frames as shown in Fig. 2.4. As the main goal of the vector control is controlling active and reactive power separately, the q component measured from PCC should be set to zero. To do so, the PLL has to accurately determining the position of the angular frequency and angle of the utility grid voltage through classical feedback control. The PI controller can be used as a compensator for the PLL feedback control; more details are provided in chapter 3.

To represent the functionality of the PLL control, Fig. 2.4 shows the representation of dq frames in two case scenarios, which are stiff and weak grid conditions. In a steady-state condition, the synchronization angle δ between the two frames is approximately equal to zero, where both frames are aligned together as shown in Fig. 2.4 (a). Thus, the PLL control in this case can be neglected as it has no action to do. In contrast, under transient and/or weak grid conditions, both frames are no longer aligned, as shown in Fig. 2.4 (b). The angle δ begins to oscillate until it resynchronizes successfully with the grid, whereby the system reaches a steady state again. Therefore, the synchronous PLL is an inevitable part of the dq vector control, especially in a weak grid condition.

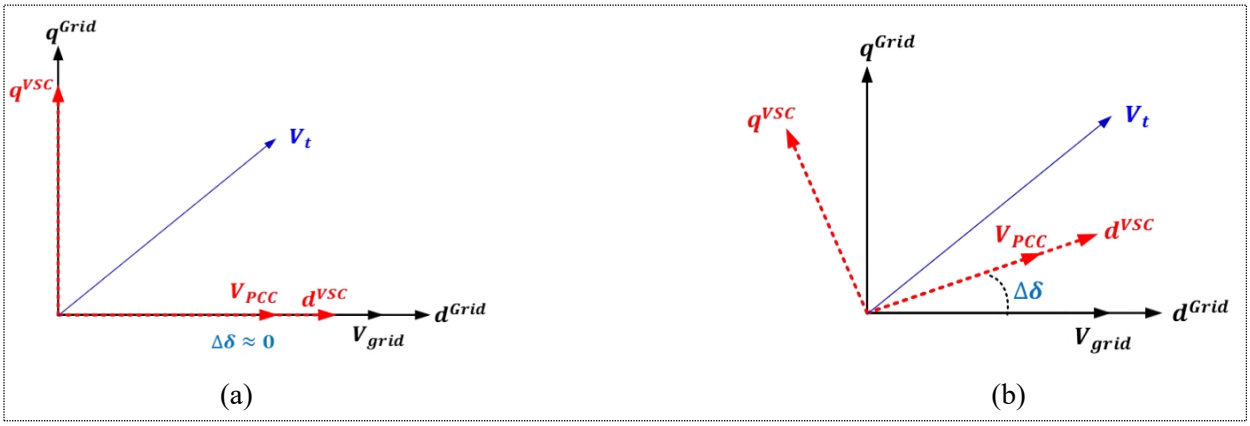


Figure 2.4 Grid and converter dq frames of vector current control. a) stiff grid, b) weak grid

2.4.3 Comparison between VSC and CSC

Although the CSC is not considered in this work, Table 2.3 presents a comparison between VSC and CSC to clarify the key differences between them. The comparison has been conducted based on the latest semiconductor switch development of these converters, so the LCC switch is not considered. The duality of the VSC and CSC can be clearly depicted from the table below.

Table 2.3: Comparison between VSC and CSC power converters in terms of their features [15], [74]-[78]

Item	VSC	CSC
Semiconductor switching device	Asymmetrical with anti-parallel diode like IGBT	Thyristor (LCC) or Symmetrical like IGCT
Dc-side energy storage	Electrolytic or film DC-capacitor (C_{dc})	Bulk DC choke (L_{dc})
Power losses in dc-side filters	Low-power losses reach approximately 0.5%	High power losses are between 2 and 4%
Grid filter	Inductance L_f	Capacitance C_f
Footprint	Compact	Large
Converter structure	Relatively complex	Simple
Reliability	Lower	Higher
Applicability	High DC-link voltage ($V_{dc} \geq 2\ V_{grid}$) is required to avoid over-modulation when connecting to the grid	More flexibility when connecting to the grid
Harmonics	Medium	High
Unity power factor	Yes	No
Switching losses and (dv/dt)	High (might break the insulation)	Low
Overcurrent or short circuit protection	Difficult with IGCT, but effective with (IGBT)	More Effective and reliable
Dynamic performance	High	Low
Common PWM technique	Space vector, Carrier-based, SHE, and hysteresis (delta modulation)	Space vector, carrier-based, SHE
Dc voltage and current	V_{dc} is determined by the voltage source	I_{dc} is dictated by the magnitude of the required AC-side
Applications	[1]Efficient in low and medium voltage applications	More efficient in high-voltage applications
Direction of power flow	Determined by changing DC-current polarities	Determined by changing DC voltage polarities

[1] *Multilevel topologies of VSC are required in high-power applications, whereas 2-level VSC is suitable for medium and low voltage applications*

2.5 Related Work

As the DERs experience rapid expansion, maintaining the overall system stability is vital. Therefore, this research investigates grid-connected VSC dynamic stability under different case scenarios and operation modes. Furthermore, this study is devoted to studying the dynamic interactions between DC-link capacitance uncertainty and utility grid strength. As the best of the authors' knowledge, this type of dynamic interaction stability analysis study has not been rigorously reported in literature. It is noteworthy to mention that variations in the DC-link capacitance is an actual case that could occur due to variable loading and/or source conditions or changing the ambient temperature. These variations might significantly influence the DC-link voltage dynamic stability, causing stability issues [79]-[81].

Some research has been carried out on the study of the dynamic interactions between grid-connected VSCs. Reference [82] presents a stability analysis of VSC connected to a weak grid. Also, a sensitivity analysis of AC system parameters and controllers' gains have been studied in accordance with the weak-grid condition. In this reference, all the analysis has been done in inversion mode, but the rectifications have not been addressed. Furthermore, the DC-side terminal is considered to be a fixed DC voltage source, so the dynamics of the DC-link capacitor and DC-link voltage controller were not included in this study. Most importantly, the effect of DC-link capacitance was out of the scope. The efforts in references [83], [84] are devoted to studying the impact of the control loops interactions on the stability performance of VSCs that are connected to weak and very weak grids. In [83], the concept of damping and restoring components is proposed for analyzing the control loop interactions. However, the effect of the AC voltage controller (reactive power controller) on the DC-link voltage controller has been addressed under different SCR levels. It has also been proven that the stability of the DC-link voltage control is affected by AC voltage control. In [84], the analysis was conducted using the state-space, small-signal model to assess the system's stability by considering several effects such as the operating point and controllers' gains. In this study, the analyses mainly address the impact of PLL control on DC-link voltage control under different SCR levels. The analyses clearly show the dynamic interactions between both controllers. Besides which, it has been revealed that when the bandwidth of the PLL controller is almost identical to the bandwidth of the DC-link voltage controller, the system's stability worsens. In both of the studies, the analysis was conducted in inversion mode

while the rectification mode was not included. These studies also considered the effect of DC-link voltage control and other controls on the system stability, whereas the impact of DC-link capacitance on system stability has not been reported under weak grid conditions. In [79], [85] the effect of the DC-side parameters' variation on the dynamic stability of the grid-connected VSC system was studied. In the former reference, the analysis applied to a utility-scale PV system that was connected to a utility grid. Front-end converters (boost DC/DC) and grid side inverters, including their controllers, have been applied in order to harvest the maximum PV power for delivering active/reactive power to the grid. This study contributes by investigating the effect of the DC-link and front-end converter parameters on the dynamic stability of the power system. It has also been revealed that the dynamic stability of the power system is affected by the DC-side. Also, the most influential element that affects the dynamic stability of the power system in the DC-side is the DC-link capacitance. The analysis did not consider the rectification mode, and the weakness of the utility grid was not investigated. The contribution of the latter study is the proposition of a non-linear controller for enhancing the stability of the system against the variations in the DC-side parameters (i.e. L_{dc}, C_{dc}). The effect of variations in the DC-link capacitance on system stability has been addressed in both studies but with a stiff grid. Nevertheless, the effect with weak and weak grid conditions has not been evaluated. In the latter study the effect of the DC-link capacitance variations was only investigated under the rectification mode. Both studies confirmed that increasing the value of the DC-link capacitance negatively affected the damping of the system and vice versa. Moreover, the impact of controllers' bandwidth and the grid side parameters on the system stability has also not been reported. In [86], a feedforward compensation was proposed in order to overcome the side-effects of reducing DC-link capacitance such as increasing the THD in the grid current. This paper focused on applications that used a converter-based diode bridge front-end, which means that the targeted applications are only DC-type (i.e. an Electrolyzer). Nonetheless, the bidirectional VSC is beyond the scope of this study, and the effect of the DC-link capacitance is only considered in one mode, the rectification mode. The effect of the AC-side was disregarded, and the effect of the DC-link capacitance with a weak grid was also not achieved. An extensive modelling and analysis work using a very weak, grid-connected VSC was implemented in [87]. This study aimed to overcome the limitations of the converter power injection in a very weak grid condition using robust controls technique. The interaction stability analysis, however, was not the aim of this study.

Another analysis of permanent magnet generator (PMG) and doubly-fed electric machine (DFIG) for wind application connected to a weak grid through three-phase back-to-back VSC was conducted in [88] and [89], respectively. The contribution of reference [88] is controlling the DC-link voltage via the Permanent magnet generator (PMG) converter side instead of the grid converter side, while [89] proposed a new approach for modelling the grid-connected Doubly-fed electric machine (DFIG) system for the sake of stability analysis. Also, the active and reactive power controls are controlled through the rotor side converter rather than the grid converter side. However, the interaction dynamics between the DC-link capacitance uncertainty, utility grid and AC-side parameters on system stability has not been reported in both studies. For this purpose, a comprehensive dynamic stability analysis is conducted to investigate and evaluate the stability of the system under uncertainty in the DC-link capacitance along with very weak grid in inversion and rectification modes.

2.6 Summary

This chapter has revealed the importance of shifting from conventional power systems, that increase global warming, to renewable energy resources. The limitations of the conventional power system have been discussed by mentioning the advantages and disadvantages of such systems. With renewable energy systems, the revolution of power electronics converter technology is the key element behind the huge growth of these resources. The advancement of power electronics converters was therefore discussed in detail. This chapter has also shown that a converter is formed from one or more semiconductor switches. This implies that semiconductor switches are important and improving these switches will lead to improvements in the converters' performance and efficiency. The different types and characteristics of semiconductor switches were presented along with a comparison of the most two advanced switches: IGBT and IGCT. Among several power electronics converters, VSCs are currently dominant in the market due to several competitive features mentioned earlier. The concept, operation, and control strategies of VSC are presented in detail, with a comparison between VSC and CSC based on their key features also being shown. Lastly, a literature review of the dynamic stability study of grid-connected VSC system in term of studying the dynamic interactions between DC-link capacitance uncertainty and utility grid strength in different modes was reported.

Chapter 3

Small-Signal Modeling of Grid-connected VSC Under Different Operational Modes

3.1 Introduction

This chapter introduces the mathematical model of the VSC connected to a grid for the purpose of analysis. The concept of linearization is briefly discussed, and the studied system is presented with clear explanation. Furthermore, the parameters and values of each component are shown in this section. This section includes a detailed description of the general design method that was applied for the controllers. The mathematical large-signal model for the grid-connected VSC is presented. From this model, the linearized state-space model is derived. To validate the analytical results, verification of the small-signal model against the large-signal model is reported under different critical case scenarios.

3.2 Linear Analysis Method for Dynamic Interaction Studies

The majority of existing power systems, such as power converters applications, are nonlinear which make them difficult to analyze [90]. Using the nonlinear model in simulation can provide limited information, including the response of the system to disturbances, but cannot provide information about the system's inherent dynamic stability and the effect of parameter [91], [92]. Therefore, linearizing a nonlinear system around a certain equilibrium point is a simple and optimum method for studying and analyzing the inherent dynamic characteristics of power systems. This method also assists in designing the power systems and the controllers for such systems. To apply this method to any nonlinear system equation, it is assumed that there is a perturbation and an average value as shown in (3.1). As is clear from Fig. 3.1, the perturbation quantity is considerably small compared with the DC quantity.

$$\langle x(t)\rangle = \underbrace{\bar{X}}_{Dc} + \underbrace{\Delta x(t)}_{Ac}$$

$$\bar{X} >> \Delta x(t) \tag{3.1}$$

Therefore, any two multiplied nonlinear time-variant quantities (or high-order terms) result in a very small negligible quantity. Thus, these quantities are then transformed into a linear equation. This linearization method called Taylor series expansion [93], [94]. It is worth mentioning that a linear model is only valid for small perturbations around a certain equilibrium point. In the case of large perturbations, the system might enter the nonlinear region and the derived linear model is no longer validated to use. This linear model is, therefore, called small-signal linearization model. As the core of this work is to capture the dynamic characteristics of a grid-connected VSC, the small-signal linearization method was applied.

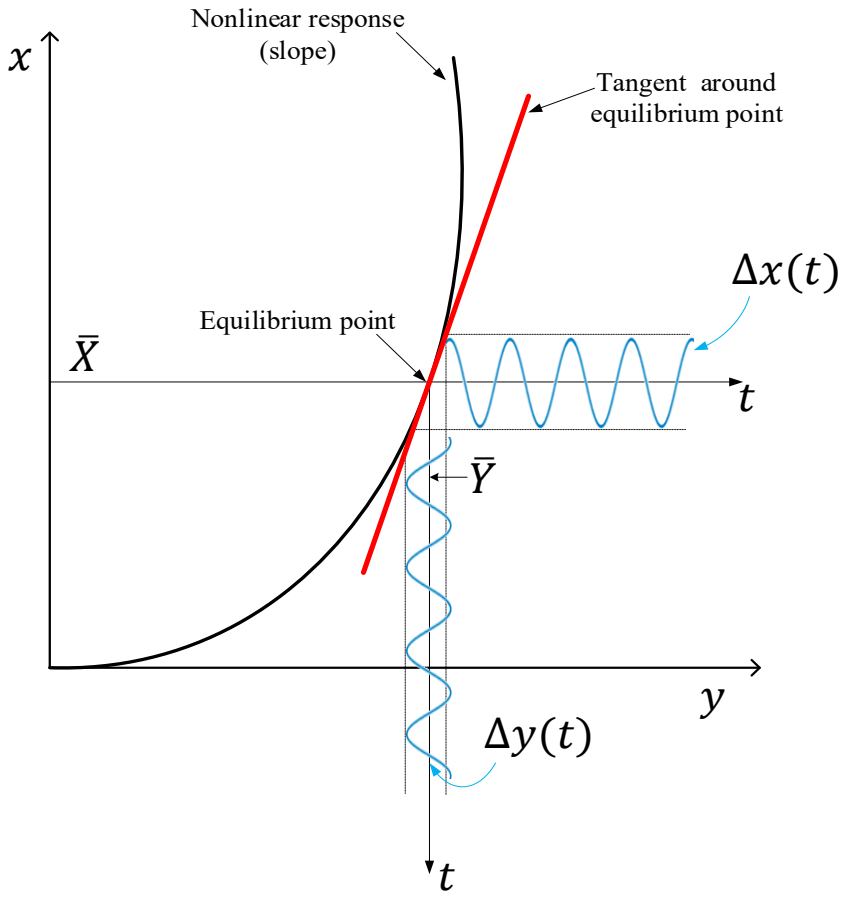


Figure 3.1 Linearization concept for nonlinear system.

3.3 System Description

Figure 3.2 illustrates the bidirectional grid-connected VSC system that was considered in this study. The block diagrams below the system are related to the following: controllers, direct-quadrature (dq) transformation, and pulse width modulation (PWM). In this system, it is assumed that the DC-side consists of several loads and generators connected to the DC-bus, which can be assumed to be a DC microgrid.

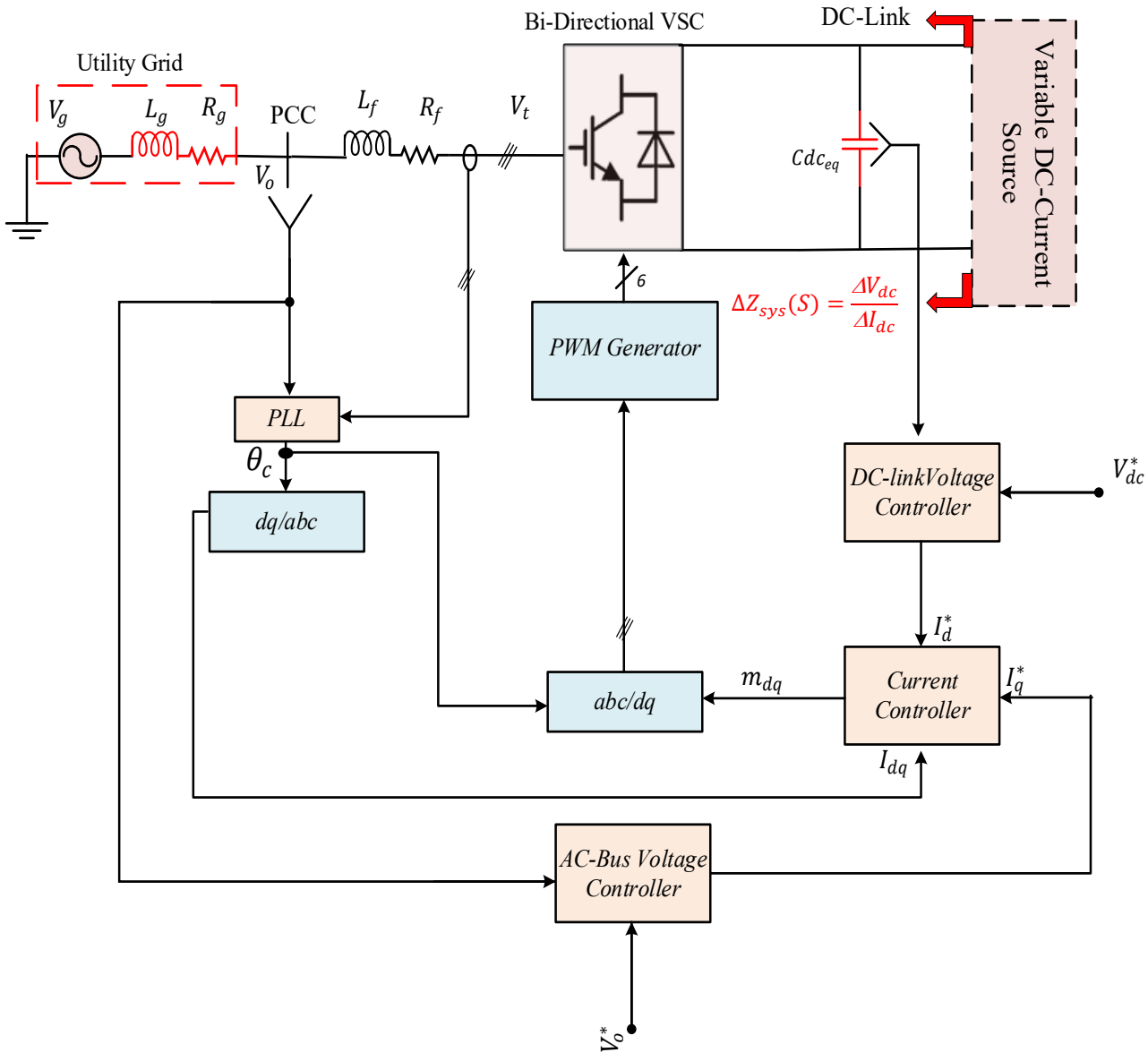


Figure 3.2 Bidirectional grid-connected VSC interfacing controlled DC-current source.

For the sake of simplicity, these assumed sources and generators are represented by a controlled DC-current source. The red highlighted parts of this diagram refer to DC-link capacitance and grid impedance, which were the main focuses of this study.

Cdc_{eq} refers to the equivalent DC-link capacitance;V_t, V_o, and V_g are AC-side converter output terminal voltage, voltage at PCC, and grid voltage, respectively; L_f and R_f are inductance filter and reactor internal resistance, respectively; and L_g and R_g represent the grid impedance that determines the strength of the grid. The parameters of the system are illustrated in Table 3.1.

Table 3.1: Parameters of the System [27] :

Parameters	Values
Rated power of the system (P_s)	2.5 MW
Switching frequency (f_{sw})	1680 Hz
Utility grid line-to-line (L-L) rms voltage ($V_{g_{abc}}$)	480 V
AC filter inductance (L_f) and resistance (R_f)	200 μH , 3.26 $m\Omega$
Equivalent DC-link capacitance (Cdc_{eq})	9625 μF
DC-link voltage (V_{dc})	1750 V
Grid impedance ratio (X_g/R_g)	10

3.4 Controllers' Design

Most of the grid-connected power converters use a classical vector control approach [17]. As previously mentioned, the principle of vector control is converting the AC three phase into two orthogonal vectors to facilitate the controller operation. A classical vector control approach for a power converter usually consists of two control levels: upper-level control (outer loop) and lower-level control (inner loop). The role of the outer loop controller is to control the active and reactive power and regulate the DC-link and PCC voltages. The output current from the outer loop controller in dq components is processed by the inner loop controller through the grid coupling filter and then generates the modulation signals for the VSC through PWM as shown in Fig. 3.2.

In the following section, the design approach for AC-current, DC-link voltage, AC-bus voltage, and PLL controllers of the VSC is discussed in detail.

3.4.1 AC-Current Controller (Inner-Loop)

This type of controller is mainly implemented based on vector current control type. The main role of the current controller is controlling the current flow in the AC inductance filter by using a proportional and integral controller (PI). The decoupling terms illustrated in Fig. 3.3 (red signals) permit the current controller to independently regulate the dq-axis, which is considered the distinctive feature of vector control. In Fig. 3.3, the mathematical expression of the current controller loop can be given in a vector representation as follows:

$$\overline{\mathbf{V_t^c}} = \left(\bar{\mathbf{I}}_\mathbf{f}^{\ *} - \bar{\mathbf{I}}_\mathbf{f}^{\boldsymbol{c}}\right) K_i(s)\, j\omega\, L_f\, \bar{\mathbf{I}}_\mathbf{f}^{\boldsymbol{c}} + \bar{\boldsymbol{V}}^{\boldsymbol{c}}{}_{\boldsymbol{o}} \tag{3.2}$$

where $K_i(s) = \left(K_{pi} + \frac{K_{ii}}{s}\right)$, K_{pi} and K_{ii} are the proportional and the integral gains, respectively. The superscripts " * ", " ^{c} " denote the reference values of the targeted signal and the converter reference frame, respectively. The open- and closed-loop transfer functions of the current controller can be derived from Fig. 3.3 as follows:

$$i(s) = \left(K_{pi} + \frac{K_{ii}}{s}\right)\left(\frac{1}{L_f\, S + R_f}\right) \tag{3.3}$$

$$Gpi(s) = \frac{I_d}{I_d^*} = \frac{K_{pi}\, S + K_{ii}}{L_f\, S^2 + \left(R_f + K_{pi}\right) S + K_{ii}} \tag{3.4}$$

Using a pole-zero cancellation property in (3.4) by choosing $\frac{R_f}{L_f} = \frac{K_{ii}}{K_{pi}}$, the closed-loop transfer function can be re-written as:

$$Gpi(s) = \frac{I_d}{I_d^*} = \frac{1}{\tau_i\, S+1}, \text{ where } \tau_i = \frac{L_f}{K_{pi}} \tag{3.5}$$

For the purpose of controller design, a high bandwidth must be considered for a fast tracking current control [95]. As a general rule of thumb, the bandwidth of the current controller ($\mathrm{Bw_{cc}}$) must be less than the switching frequency (f_{sw}). Therefore, it is recommended to select a $\mathrm{Bw_{cc}}$ that is 0.1–0.2 times the f_{sw} of the VSC. The gains of the current controller, therefore, can be obtained

from (3.5) by using the following expressions, through a process called the internal model method [96], [97]:

$$K_{pi} = \omega_b L_f \tag{3.6}$$

$$K_{ii} = \omega_b R_f \ , \ \omega_b = \frac{1}{\tau_i} \tag{3.7}$$

In this project, the $\mathrm{Bw_{cc}}$ was selected to be $=0.1*2\pi f_{sw} = 336\pi$ rad/sec as illustrated in Fig. 3.4. Using (3.6) and (3.7), the gains K_{pi} and K_{ii} are found to be 0.2 and 3.26 /S, respectively.

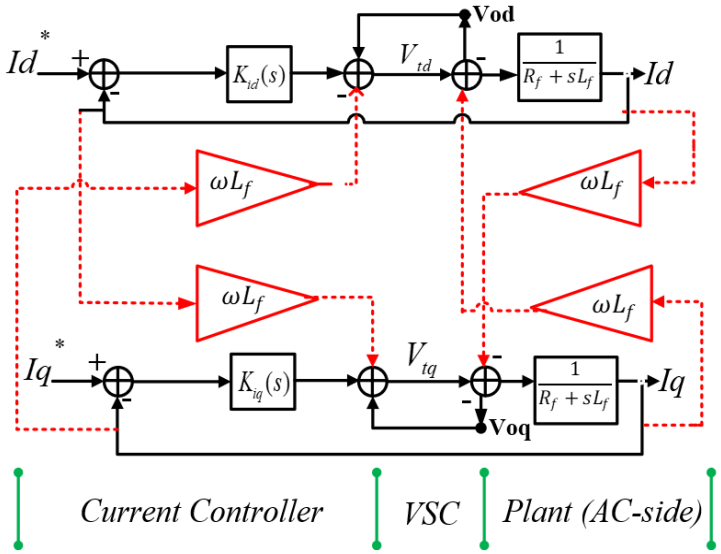


Figure 3.3 Current controller schematic for the grid-connected VSC.

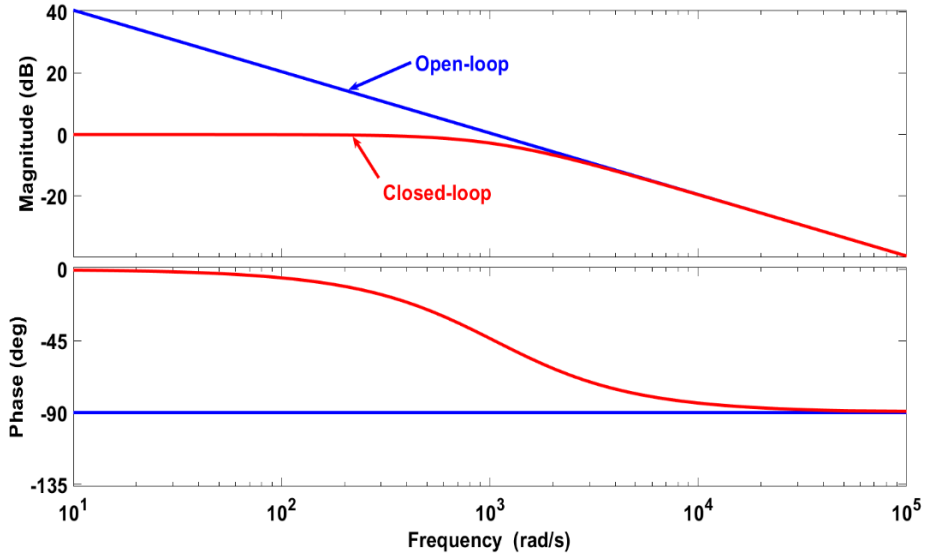


Figure 3.4 Frequency response (bode-plot) of open- and closed-loop transfer function for the AC-current controller.

3.4.2 DC-link Voltage Controller (Outer-Loop)

The main role of this controller is obtaining the desired range of active power and amplitude of the DC-link voltage. As is shown in Fig. 3.2, the input and output of the DC-link voltage controller are references of the DC-link voltage (V_{dc}^{*}) and the $d-axis$ current (I_{d}^{*}), respectively. The error between the reference values and actual values of the DC-link voltage controller is processed by the PI controller, which in turn generates the I_{d}^{*}. Referring to Fig. 3.5, the dynamics of the DC-link voltage controller equation can be described in a vector form as:

$$Real\{\bar{\mathbf{I}}_{\mathbf{f}}{}^{*}\} = \frac{2}{3V_{od}}\left[\left(V_{dc}^{2} - V_{dc}^{2}{}^{*}\right) K_{v}(s)\right] \tag{3.8}$$

Where $K_{v_{dc}}(s) = \left(K_{pv_{dc}} + \frac{K_{iv_{dc}}}{s}\right)$, $K_{pv_{dc}}$ and $K_{iv_{dc}}$ are proportional and integral gains, respectively.

The open- and closed-loop transfer functions of the DC-link voltage controller can be derived from Fig. 3.5 as follows:

$$l_{v_{dc}}(s) = \left(K_{pv_{dc}} + \frac{K_{iv_{dc}}}{S}\right)\left(\frac{2}{3*V_{o}}\right)\left(\frac{1}{\tau_{i}\,S+1}\right)(1.5V_{d})\left(\frac{2}{C_{dc}\,S}\right) \tag{3.9}$$

$$Gv_{dc}(s) = \frac{V_{dc}^{*}}{V_{dc}} = \frac{l_{v_{dc}}(s)}{1 + \ l_{v_{dc}}(s)} \tag{3.10}$$

For the sake of controller design, the bandwidth of the DC-link voltage controller ($\mathrm{Bw_{dc}}$) must be adequately slower than that of the inner controller to avoid any dynamic interference between the controllers. Therefore, the gain crossover frequency of the voltage controller (ω_{c}) should be selected between 0.15 to 0.3 of the bandwidth of the inner current control loop [27]. In this study, the $\mathrm{Bw_{dc}}$ was chosen to be = $0.2*2\pi f_{sw} = 70\pi$ rad/sec as illustrated in Fig. 3.6. The controller gains $K_{p_{dc}}$ =0.875 and $K_{i_{dc}}$ =50/S have been designed based on the symmetrical optimum technique [98].

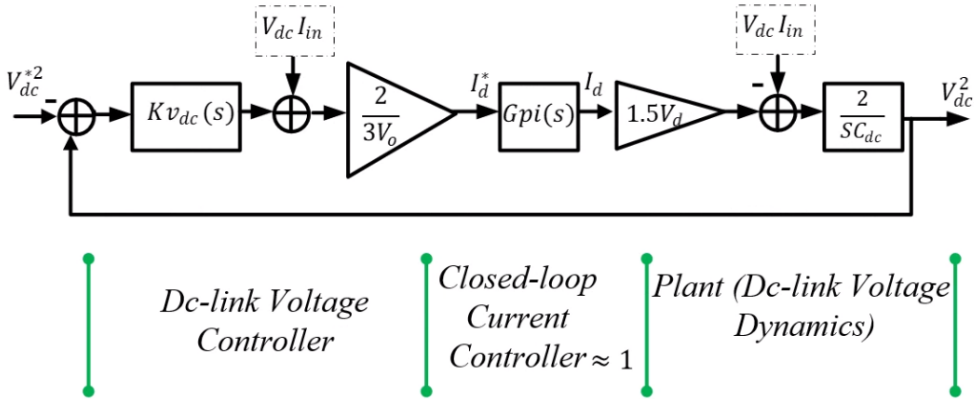


Figure 3.5 Closed-loop block diagram of the VSC DC-link voltage controller.

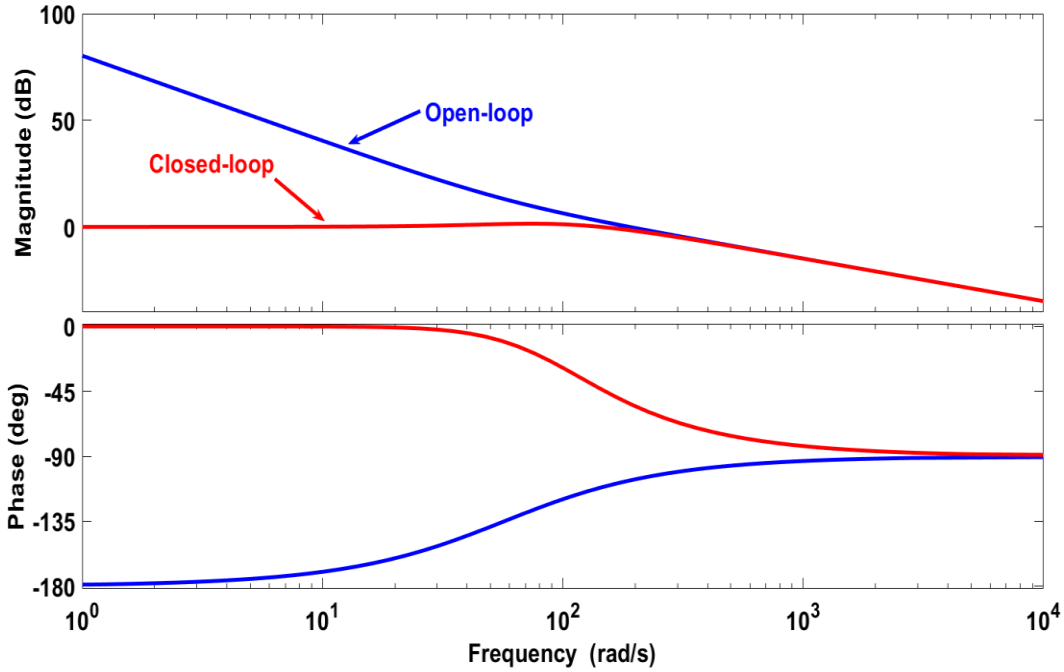


Figure 3.6 Frequency response (bode-plot) of open- and closed-loop transfer function for the DC-link voltage controller.

3.4.3 Phase-Locked Loop (PLL)

A PLL is implemented to synchronize the angle of the VSC with the AC grid and generate the dq-components of the measurements that applied in other controller loops as shown in Fig. 3.7. It can be also depicted from the aforementioned figure that the q −component of the PCC is set to zero by the PI controller. In the steady state conditions, the synchronization angle θ between the grid and converter reference frames is equal to zero, as both frames are aligned together. Under transient conditions, both frames are no longer aligned, and the angle θ begins to oscillate until a

resynchronization is successfully achieved [99], [100]. To account for the PLL dynamics in this work, all measured signals denoted by the superscript "c" are transformed to the grid reference frame " ^{g}" by using the general frame transformation equations as follows (3.11)-(3.13):

$$x^{g} = x^{c} e^{j\theta} \tag{3.11}$$

$$\begin{bmatrix} \Delta x_d^c \\ \Delta x_q^c \end{bmatrix} = \begin{bmatrix} cos\,(\theta_0) & sin(\theta_0) & (-x_{d_0}^g sin(\theta_0) + x_{q_0}^g cos(\theta_0)) \\ -sin(\theta_0) & cos(\theta_0) & (-x_{d_0}^g cos(\theta_0) - x_{q_0}^g sin(\theta_0)) \end{bmatrix} \begin{bmatrix} \Delta x_d^g \\ \Delta x_q^g \\ \Delta\theta \end{bmatrix} \tag{3.12}$$

$$\begin{bmatrix} \Delta x_d^g \\ \Delta x_q^g \end{bmatrix} = \begin{bmatrix} cos\,(\theta_0) & -sin(\theta_0) & (-x_{d_0}^c sin(\theta_0) - x_{q_0}^c cos(\theta_0)) \\ sin(\theta_0) & cos(\theta_0) & (x_{d_0}^c cos(\theta_0) - x_{q_0}^c sin(\theta_0)) \end{bmatrix} \begin{bmatrix} \Delta x_d^c \\ \Delta x_q^c \\ \Delta\theta \end{bmatrix} \tag{3.13}$$

It is worth mentioning that the frame of all signals of the system must be unified, either for the grid or the converter reference frame. Referring to Fig. 3.7, the mathematical model of the PLL controller is provided by (3.14) and (3.15) in a vector form:

$$\omega_{pll} = K_{PLL}(S)\ \mathrm{Im}\{\overline{\boldsymbol{V}}_{\boldsymbol{o}}{}^{\boldsymbol{c}}\} \tag{3.14}$$

$$\frac{d\theta}{dt} = \left(\omega_g^{\circ} + \omega_{pll}\right) \tag{3.15}$$

Where $K_{PLL}(S) = \left(K_{p_{pll}} + \frac{K_{i_{pll}}}{s}\right)$, $K_{p_{pll}}$ and $K_{i_{pll}}$ are the proportional and integral gains of the PLL, respectively; ω_g° and ω_{pll} are nominal values of the grid angular synchronous frequency and PLL instantaneous angular frequency, respectively; and the superscript "o" denotes the operating point of the variable. The open- and closed-loop transfer functions of the PLL can be derived from Fig. 3.7 as follows:

$$l_{p_{ll}}(s) = \left(\frac{1}{S}\right)\left(K_{p_{pll}} + \frac{K_{i_{pll}}}{s}\right) V_{oq}^{c} \tag{3.16}$$

$$Gp_{pll}(s) = \frac{l_{p_{ll}}(s)}{1 + l_{p_{ll}}(s)} \tag{3.17}$$

As the PLL controller is a critical part in vector control and all the controllers relay on it as shown in Fig. 3.2, the ω_{pll} must be limited between certain amounts to avoid large deviations. Based on [69], [101] the bandwidth of the PLL ($\mathrm{Bw_{PLL}}$) is recommended to sit within the range of the outer-

loop controller, which adequately smaller than inner controller's bandwidth. Therefore, designing the $\mathrm{Bw_{PLL}}$ at 65π rad/sec, as illustrated in Fig. 3.8, can be achieved by setting the gains to $K_{p_{pll}}$= 180 and $K_{i_{pll}}$= 3200/S [27].

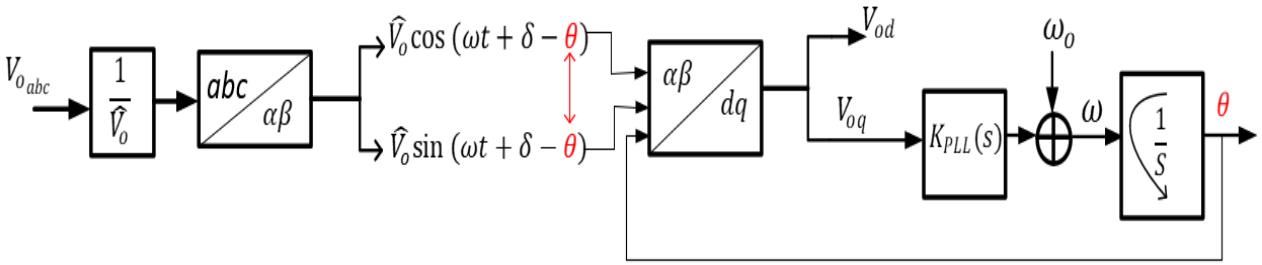


Figure 3.7 PLL schematic for the grid-connected VSC.

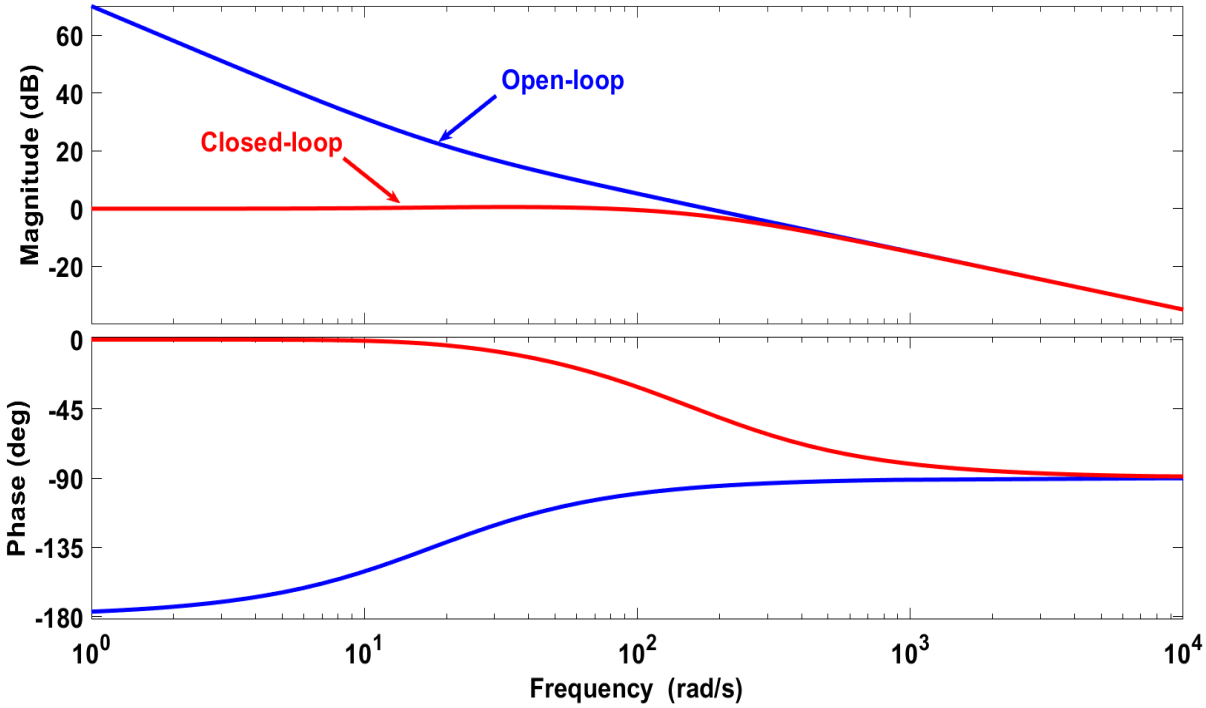


Figure 3.8 Frequency response (bode-plot) of open- and closed-loop transfer function for the PLL controller.

3.4.4 AC-Voltage Controller (Outer-Loop)

The main function of this controller is obtaining the desired range of reactive power and amplitude of the PCC voltage. The input and output of the AC-bus voltage controller are references of the AC-bus voltage (V_{od}^*) and the $q-axis$ current (I_q^*), respectively, as shown in Fig. 3.9. The error between the reference values and actual values of the AC-bus voltage controller is processed

by the PI controller, which in turn generates the I_q^*. Referring to Fig. 3.9, the dynamics of the AC-bus voltage controller equation can be represented in a vector form as (3.18):

$$\mathrm{Im}\{\bar{\mathbf{I}}_{\mathbf{f}}{}^{*}\} = \frac{-2}{3V_o^{\wedge}}\left[\left(V_{od}^{*} - \mathrm{Real}\{\bar{\boldsymbol{V}}_{\boldsymbol{o}}{}^{\boldsymbol{c}}\}\right) K_{v_{ac}}(s)\right] \tag{3.18}$$

Where $K_{v_{ac}}(s) = \left(K_{pv_{ac}} + \frac{K_{iv_{ac}}}{s}\right)$, $K_{pv_{ac}}$ and $K_{iv_{ac}}$ are proportional and integral gains, respectively. The open- and closed-loop transfer functions of the AC-bus voltage controller can be derived from Fig. 3.9 as follows:

$$l_{v_{ac}}(s) = \left(K_{pv_{ac}} + \frac{K_{iv_{ac}}}{S}\right)\left(\frac{-2}{3*V_o}\right)\left(\frac{1}{\tau_i S+1}\right)(\omega_o L_g) \tag{3.19}$$

$$Gv_{dc}(s) = \frac{V_{dc}^{*}}{V_{dc}} = \frac{l_{v_{ac}}(s)}{1 + l_{v_{ac}}(s)} \tag{3.20}$$

The design criteria for this controller is similar to that of the DC-link voltage controller. Therefore, the AC-bus voltage controller bandwidth ($\mathrm{Bw_{ac}}$) was selected at $0.15* \mathrm{Bw_{cc}} = 55\pi$ rad/sec as shown in Fig. 3.10. This can be achieved by setting the controller gains $as\ K_{pi} = 1$ and $K_{ii} = 1.1e6/S$. As this project was devoted to weak grid condition, the controller gains were designed at high grid impedance (Z_{grid}).

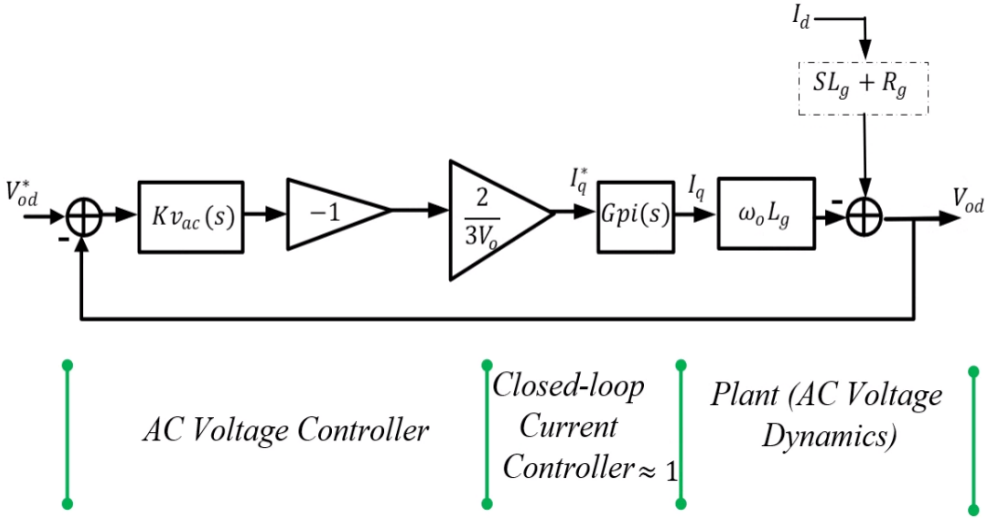


Figure 3.9 Closed-loop block diagram of the VSC AC-bus voltage controller.

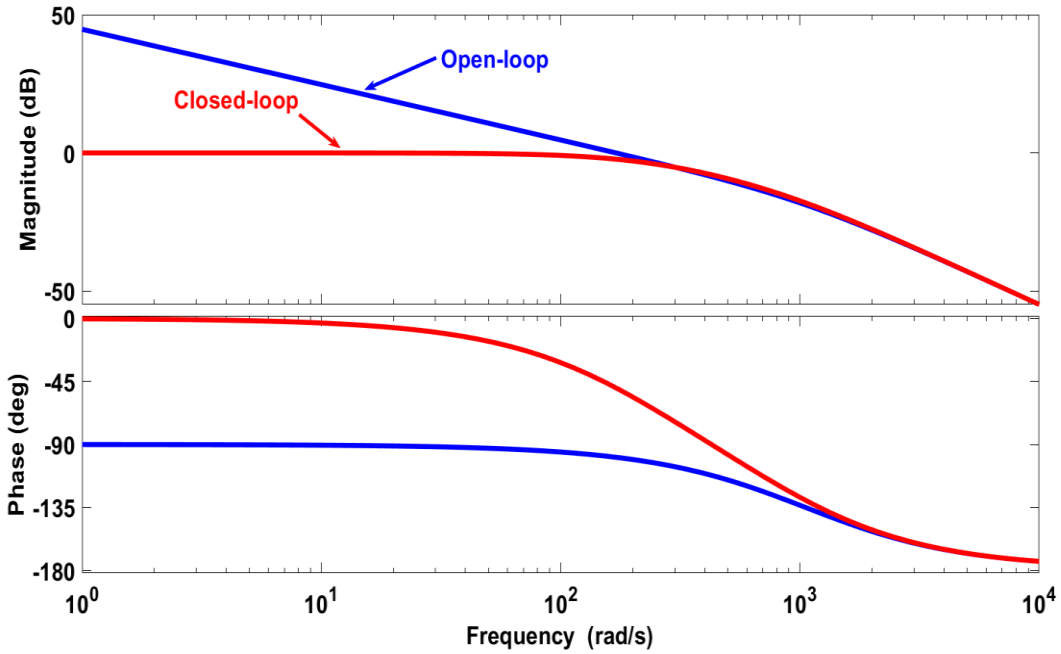


Figure 3.10 Frequency response (bode-plot) of open- and closed-loop transfer function for the AC-bus voltage controller.

3.5 Mathematical Modeling

Normally, modeling technique can be categorized into state-space models and impedance models. Both methods are used for the same purpose, which is analyzing the dynamic stability of the targeted systems. In this work, the state-space model method was chosen to analyze the dynamic interactions of the system shown in Fig. 3.2.

3.5.1 Large-Signal Model

Figure 3.2 represents the circuit diagram of the DC-AC bidirectional grid-connected VSC system. The details of the complete large-signal model are presented in this section.

3.5.1.1 Power Circuit Model

a) AC-side dynamics

As is clear from the system diagram in Fig. 3.2, the dynamics of power circuits are modeled by (3.21) - (3.23). To simplify the analysis, the model of the AC-side was considered in the dq synchronous reference frame.

$$V_{td} - V_{od} = I_d\left(R_f + pL_f\right) - \omega L_f I_q \tag{3.21}$$

$$V_{tq} - V_{oq} = I_q\left(R_f + pL_f\right) + \omega L_f I_d \tag{3.22}$$

$$V_{od} - V_{gd} = I_{gd}\left(R_g + pL_g\right) - \omega L_g I_{gq} \tag{3.23}$$

$$V_{oq} - V_{gq} = I_{gq}\left(R_g + pL_g\right) + \omega L_g I_{gd} \tag{3.24}$$

V_{td}, V_{tq}, I_d, and I_q are the dq- axis converter's terminal output currents and voltages, PCC voltage, and grid voltage, respectively; V_{od} , V_{oq}, I_{gd} and I_{gq} are dq- axis voltages and injected currents at the point of common coupling; p denotes the time-derivative operator. The mathematical representation of instantaneous active (P_{pcc}) and reactive (Q_{pcc}) power delivered to the PCC can be modeled in the dq synchronous reference frame by (3.25) and (3.26):

$$P_{pcc} = 1.5(I_d V_{od} + I_q V_{oq}) \tag{3.25}$$

$$Q_{pcc} = 1.5\left(I_q V_{od} - I_d V_{oq}\right) \tag{3.26}$$

b) DC-side dynamics

In this study, the converter was assumed to be lossless, which means it is a highly efficient power electronic converter. Considering this assumption, the power injected to the inverter terminal from the DC-link bus is equal to the power delivered from the inverter. However, the power balance equation of DC-AC is:

$$V_{dc} I_{in} = 1.5(I_d V_{td} + I_q V_{tq}) \tag{3.27}$$

The dynamic of the DC-side is represented by the DC-link capacitance:

$$Cdc_{eq}\, pV_{dc} = I_{dc} - I_{in} \tag{3.28}$$

where I_{dc} is the injected current to the DC-link bus coming from the virtual DC-microgrid that is represented by a controlled current source, I_{in} is the current delivered from the DC-link bus to the converter; and V_{dc} is the voltage across DC-link capacitance. Rewriting (3.27) in terms of power, the power balance on the DC-link bus is given by (3.29):

$$\underbrace{\tfrac{1}{2} Cdc_{eq} pV_{dc}^2}_{P_{cap}} = \underbrace{V_{dc} I_{dc}}_{P_{dc}} - \underbrace{1.5\left(I_d V_{td} + I_q V_{tq}\right)}_{P_{conv}} \tag{3.29}$$

where $P_{cap}, P_{dc}, and\ P_{conv}$ are the power across the DC-link bus, the exogenous power that comes from virtual DC microgrid, and the converter power delivered to the AC-side terminal, respectively; and the term $\left(\frac{1}{2}Cdc_{eq}pV_{dc}^2\right)$ represents the rate of DC-link capacitor energy change.

3.5.1.2 Controllers' Model

In the previous subsection, the mathematical power circuit model in Fig. 3.2 was presented. In order to represent all the dynamics of the system, the controllers of the system are also modeled. Therefore, the mathematical representation of DC-link voltage, AC-bus voltage, AC-current, and PLL controllers is governed by (3.30) -(3.34), respectively:

$$I_d^* = \frac{2}{3V_{od}}\left[\left(V_{dc}^2 - V_{dc}^{2\,*}\right) K_{v_{dc}}(s)\right] \tag{3.30}$$

$$I_q^* = \frac{-2}{3V_o}\left[\left(V_{od}^* - V_{od}^c\right) K_{v_{ac}}(s)\right] \tag{3.31}$$

$$V_{td}^c = (I_d^* - I_d^c)K_{id}(s) - \omega\, L_f I_q^c + V_{od}^c \tag{3.32}$$

$$V_{tq}^c = \left(I_q^* - I_q^c\right)K_{iq}(s) + \omega\, L_f I_d^c + V_{oq}^c \tag{3.33}$$

$$\Delta\omega = K_{pll}(s)V_{oq}^c \tag{3.34}$$

$$p\theta = \Delta\omega$$

3.5.2 Small-Signal Model

In this section, the small-signal modeling of the entire system is derived. Applying the small-signal linearization, which is described in section 3.2, to (3.21) -(3.24) and (3.29) -(3.34), results in the following equations:

$$L_f S\Delta I_d^g = R_f \Delta I_d^g - \omega L_f \Delta I_q^g - \Delta V_{td} + \Delta V_{od}^g \tag{3.20}$$

$$L_f S\Delta I_q^g = R_f \Delta I_q^g + \omega L_f \Delta I_d^g - \Delta V_{tq}^g + \Delta V_{oq}^g \tag{3.21}$$

$$L_g S\Delta I_{gd}^g = R_g \Delta I_{gd}^g - \omega L_g \Delta I_{gq}^g - \Delta V_{od}^g + \Delta V_{gd}^g \tag{3.22}$$

$$L_g S\Delta I_{gq}^g = R_g \Delta I_{gq}^g + \omega L_g \Delta I_{gd}^g - \Delta V_{oq}^g + \Delta V_{gq}^g \tag{3.23}$$

$$\left(V^{o}{}_{dc} C dc_{eq} S\Delta V_{dc}\right) = V^{o}{}_{dc}\,\Delta I_{dc} + I^{o}_{dc}\,\Delta V_{dc} - 1.5\left(I^{o}_{d}\Delta V_{td} + V^{o}_{td}\Delta I_{d} + I^{o}_{q}\Delta V_{tq} V^{o}_{tq}\Delta I_{q}\right) \quad (3.35)$$

$$\Delta I^{*}_{d} = \frac{2}{3V^{o}_{od}}\left[\left(2V^{o}_{dc}\Delta V_{dc} - 2V^{o*}_{dc}\Delta V^{*}_{dc}\right) K_{p_{v_{dc}}} + \Delta\varphi_{vdc}\right] \quad (3.36)$$

$$S\Delta\varphi_{dc} = \left(2V^{o}_{dc}\Delta V_{dc} - 2V^{o*}_{dc}\Delta V^{*}_{dc}\right) K_{i_{v_{dc}}} \quad (3.\dot{3}6)$$

$$\Delta I^{*}_{d} = \frac{-2}{3V^{o}_{o}}\left[\left(\Delta V^{*}_{od} - \Delta V^{c}_{od}\right) K_{p_{v_{ac}}} + \Delta\varphi_{vac}\right] \quad (3.37)$$

$$S\Delta\varphi_{ac} = \left(\Delta V^{*}_{od} - \Delta V^{c}_{od}\right) K_{i_{ac}} \quad (3.\dot{3}7)$$

$$\Delta V^{c}_{td} = \left(\Delta I^{*}_{d} - \Delta I^{c}_{d}\right)K_{p_{id}} + \Delta\varphi_{id} - \omega\, L_{f\Delta} I^{c}_{q} + \Delta V^{c}_{od} \quad (3.38)$$

$$S\Delta\varphi_{id} = \left(\Delta I^{*}_{d} - \Delta I^{c}_{d}\right) K_{i_{id}} \quad (3.\dot{3}8)$$

$$\Delta V^{c}_{tq} = \left(\Delta I^{*}_{q} - \Delta I^{c}_{q}\right)K_{p_{iq}} + \Delta\varphi_{iq} + \omega\, L_{f\Delta} I^{c}_{d} + \Delta V^{c}_{oq} \quad (3.39)$$

$$S\Delta\varphi_{id} = \left(\Delta I^{*}_{q} - \Delta I^{c}_{q}\right) K_{i_{iq}} \quad (3.\dot{3}9)$$

$$\Delta\omega = K_{p_{pll}}\Delta V^{c}_{oq} + \Delta\varphi_{pll} \quad (3.40)$$

$$S\Delta\theta_{PLL} = \Delta\omega \;\; ; \; S\Delta\varphi_{pll} = K_{i_{pll}}\,\Delta V^{c}_{oq} \quad (3.\dot{4}0)$$

This represents the complete small-signal equations for the grid-connected VSC system. In order to study the dynamic stability of the grid-connected VSC system, the small-signal linearization equations are expressed in a state-space form as follows:

$$\Delta\dot{\boldsymbol{x}} = \boldsymbol{A}\,\Delta\boldsymbol{x} + \boldsymbol{B}\Delta\boldsymbol{u} \quad (3.41)$$

$$\Delta\boldsymbol{y} = \boldsymbol{C}\,\Delta\boldsymbol{x} + \boldsymbol{D}\Delta\boldsymbol{u}$$

In the following, all the above equations are re-written in the form of matrices. The equations from (3.21) – (3.29) are represented by a power circuit model, while the rest of the equations are represented by a controller model. As this work focused on a very weak grid condition, the detailed frame transformation model was considered instead of the simplified model.

3.5.2.1 Matrix form Representation of Power Circuit Model

$$\begin{bmatrix} \Delta\dot{V}_{dc} \\ \Delta\dot{I}_d^g \\ \Delta\dot{I}_q^g \\ \Delta\dot{I}_{gd}^g \\ \Delta\dot{I}_{gq}^g \end{bmatrix} = \underbrace{\begin{bmatrix} \frac{I_{in}^\circ}{C_{dc}V_{dc}^\circ} & \frac{-3V_d^\circ}{2C_{dc}V_{dc}^\circ} & \frac{-3V_q^\circ}{2C_{dc}V_{dc}^\circ} & 0 & 0 \\ 0 & -\left(\frac{R_f+R_L}{L_f}\right) & \omega^\circ & \frac{R_f}{L_f} & 0 \\ 0 & -\omega^\circ & -\left(\frac{R_f+R_L}{L_f}\right) & 0 & \frac{R_f}{L_f} \\ 0 & \frac{R_L}{L_g} & 0 & -\left(\frac{R_L+R_g}{L_g}\right) & \omega^\circ \\ 0 & 0 & \frac{R_L}{L_g} & -\omega^\circ & -\left(\frac{R_L+R_g}{L_g}\right) \end{bmatrix}}_{\mathrm{A}_{pc}} \begin{bmatrix} \Delta V_{dc} \\ \Delta I_d^g \\ \Delta I_q^g \\ \Delta I_{gd}^g \\ \Delta I_{gq}^g \end{bmatrix}$$

$$+ \underbrace{\begin{bmatrix} \frac{-3I_d^\circ}{2C_{dc}V_{dc}^\circ} & \frac{-3I_q^\circ}{2C_{dc}V_{dc}^\circ} \\ \frac{1}{L_{fg}} & 0 \\ 0 & \frac{1}{L_{fg}} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}}_{\mathrm{B}_{pc1}} \begin{bmatrix} \Delta V_d^g \\ \Delta V_q^g \end{bmatrix} + \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ \frac{-1}{L_{fg}} & 0 \\ 0 & \frac{-1}{L_{fg}} \end{bmatrix}}_{\mathrm{B}_{pc2}} \begin{bmatrix} \Delta V_{gd}^g \\ \Delta V_{gq}^g \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{C_{dc}} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{\mathrm{B}_{pc3}} [\Delta I_{dc}] \tag{3.42}$$

$$\begin{bmatrix} \Delta V_{od}^g \\ \Delta V_{oq}^g \end{bmatrix} = \underbrace{\begin{bmatrix} R_L & 0 \\ 0 & R_L \end{bmatrix}}_{V_{o1}} \begin{bmatrix} \Delta I_d^g \\ \Delta I_q^g \end{bmatrix} + \underbrace{\begin{bmatrix} -R_L & 0 \\ 0 & -R_L \end{bmatrix}}_{V_{o2}} \begin{bmatrix} \Delta I_{gd}^g \\ \Delta I_{gq}^g \end{bmatrix} \tag{3.43}$$

3.5.2.2 Matrix form Representation of Controller Model

- *AC and DC Voltage Controllers*

$$\begin{bmatrix} \Delta\dot{\varphi}_{dc} \\ \Delta\dot{\varphi}_{ac} \end{bmatrix} = \underbrace{\begin{bmatrix} 2V_{dc}K_{iv} \\ 0 \end{bmatrix}}_{B_{v1}} [\Delta V_{dc}] + \underbrace{\begin{bmatrix} 0 \\ -K_{i_{ac}} \end{bmatrix}}_{B_{v2}} [\Delta V_{od}^c] + \underbrace{\begin{bmatrix} -2V_{dc}K_{iv} \\ 0 \end{bmatrix}}_{B_{v3}} [\Delta V_{dc}^*] + \underbrace{\begin{bmatrix} 0 \\ K_{i_{ac}} \end{bmatrix}}_{B_{v4}} [\Delta V_{od}^*] \tag{3.44}$$

$$\begin{bmatrix} \Delta I_d^* \\ \Delta I_q^* \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 \\ 0 & \frac{-2}{3\left(480\sqrt{\frac{2}{3}}\right)} \end{bmatrix}}_{C_{v1}} \begin{bmatrix} \Delta\varphi_{dc} \\ \Delta\varphi_{ac} \end{bmatrix} + \underbrace{\begin{bmatrix} 2V_{dc}K_{pv} \\ 0 \end{bmatrix}}_{D_{v1}} [\Delta V_{dc}] + \underbrace{\begin{bmatrix} 0 \\ \frac{2K_{pac}}{3\left(480\sqrt{\frac{2}{3}}\right)} \end{bmatrix}}_{D_{v2}} [\Delta V_{od}^c] +$$

$$\underbrace{\begin{bmatrix} -2V_{dc}K_{pv} \\ 0 \end{bmatrix}}_{D_{v3}} [\Delta V_{dc}^*] + \underbrace{\begin{bmatrix} 0 \\ \frac{-2K_{pac}}{3\left(480\sqrt{\frac{2}{3}}\right)} \end{bmatrix}}_{D_{v4}} [\Delta V_{od}^*] \tag{3.45}$$

- *AC Current Controller*

$$\begin{bmatrix}\Delta\dot{\varphi}_{id}\\ \Delta\dot{\varphi}_{iq}\end{bmatrix}=\underbrace{\begin{bmatrix}K_{ii} & 0\\ 0 & 0\end{bmatrix}}_{B_{cc1}}\begin{bmatrix}\Delta I_d^*\\ \Delta I_q^*\end{bmatrix}+\underbrace{\begin{bmatrix}-K_{ii} & 0\\ 0 & -K_{ii}\end{bmatrix}}_{B_{cc2}}\begin{bmatrix}\Delta I_d^c\\ \Delta I_q^c\end{bmatrix} \tag{3.46}$$

$$\begin{bmatrix}\Delta V_d^c\\ \Delta V_q^c\end{bmatrix}=\underbrace{\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}}_{C_{cc1}}\begin{bmatrix}\Delta\varphi_{id}\\ \Delta\varphi_{iq}\end{bmatrix}+\underbrace{\begin{bmatrix}-K_{pi} & -\omega^{\circ}L_f\\ \omega^{\circ}L_f & -K_{pi}\end{bmatrix}}_{D_{cc1}}\begin{bmatrix}\Delta I_d^c\\ \Delta I_q^c\end{bmatrix}+\underbrace{\begin{bmatrix}K_{pi} & 0\\ 0 & 0\end{bmatrix}}_{D_{cc2}}\begin{bmatrix}\Delta I_d^*\\ \Delta I_q^*\end{bmatrix}+\underbrace{\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}}_{D_{cc3}}\begin{bmatrix}\Delta V_{od}^c\\ \Delta V_{oq}^c\end{bmatrix} \tag{3.47}$$

- *SRF-PLL*

$$\underbrace{\begin{bmatrix}\Delta\dot{\theta}_{PLL}\\ \Delta\dot{\varphi}_{pll}\end{bmatrix}}_{\Delta x_{ll}}=\underbrace{\begin{bmatrix}0 & 1\\ 0 & 0\end{bmatrix}}_{A_{pll}}\begin{bmatrix}\Delta\theta_{PLL}\\ \Delta\varphi_{pll}\end{bmatrix}+\underbrace{\begin{bmatrix}0 & K_{p_{pll}}\\ 0 & K_{i_{pll}}\end{bmatrix}}_{B_{ll}}\begin{bmatrix}\Delta V_{od}^c\\ \Delta V_{oq}^c\end{bmatrix} \tag{3.48}$$

$$[\Delta\omega]=\underbrace{[0 \quad 1]}_{C_{ll}}\begin{bmatrix}\Delta\theta_{PLL}\\ \Delta\varphi_{pll}\end{bmatrix}+\underbrace{\begin{bmatrix}0 & K_{p_{pll}}\end{bmatrix}}_{D_{ll}}\begin{bmatrix}\Delta V_{od}^c\\ \Delta V_{oq}^c\end{bmatrix} \tag{3.49}$$

- *Frame Transformation*

$$\begin{bmatrix}\Delta v_{od}^c\\ \Delta v_{od}^c\end{bmatrix}=\left[\underbrace{\begin{matrix}cos\theta_{r0} & sin\theta_{r0}\\ -sin\theta_{r0} & cos\theta_{r0}\end{matrix}}_{T_{vo1}}\right]\begin{bmatrix}\Delta v_{od}^g\\ \Delta v_{od}^g\end{bmatrix}+\left[\underbrace{\begin{matrix}(-v_{od}^0 sin\theta_{r0}+v_{oq}^0 cos\theta_{r0})\\ (-v_{od}^0 cos\theta_{r0}-v_{oq}^0 sin\theta_{r0})\end{matrix}}_{T_{vo2}}\right]\Delta\theta_{PLL} \tag{3.50}$$

$$\begin{bmatrix}\Delta v_d^c\\ \Delta v_d^c\end{bmatrix}=\underbrace{\begin{bmatrix}cos\theta_{r0} & sin\theta_{r0}\\ -sin\theta_{r0} & cos\theta_{r0}\end{bmatrix}}_{T_{v1}}\begin{bmatrix}\Delta v_d^g\\ \Delta v_d^g\end{bmatrix}+\left[\underbrace{\begin{matrix}(-v_d^0 sin\theta_{r0}+v_q^0 cos\theta_{r0})\\ (-v_d^0 cos\theta_{r0}-v_q^0 sin\theta_{r0})\end{matrix}}_{T_{v2}}\right]\Delta\theta_{PLL} \tag{3.51}$$

$$\begin{bmatrix}\Delta i_d^c\\ \Delta i_d^c\end{bmatrix}=\left[\underbrace{\begin{matrix}cos\theta_{r0} & sin\theta_{r0}\\ -sin\theta_{r0} & cos\theta_{r0}\end{matrix}}_{T_{i1}}\right]\begin{bmatrix}\Delta i_d^g\\ \Delta i_d^g\end{bmatrix}+\left[\underbrace{\begin{matrix}(-i_d^0 sin\theta_{r0}+i_q^0 cos\theta_{r0})\\ (-i_d^0 cos\theta_{r0}-i_q^0 sin\theta_{r0})\end{matrix}}_{T_{i2}}\right]\Delta\theta_{PLL} \tag{3.52}$$

For the sake of simplicity, the small-signal power circuit model was consolidated and can be written as:

$A_{Power-ckt}=[A_{pc}]_{5\times5}$, $B_{power-ckt}=[B_{pc3} \quad B_{pc2} \quad B_{pc1}]_{5\times5}$, $C_{power-ckt}=[0_{2\times1} \quad V_{o1} \quad V_{o2}]_{2\times5}$

This consolidation has also been done for small-signal controller models and is shown as:

$$A_{Cont}=\begin{bmatrix} 0_{2\times2} & 0_{2\times2} & [B_{v2}T_{vo2}\ \ 0_{2\times1}]_{2\times2} \\ B_{cc1}C_{v1} & 0_{2\times2} & B_{cc2}T_{i2}+[B_{cc2}D_{v2}T_{vo2}\ \ 0_{2\times1}]_{2\times2} \\ 0_{2\times2} & 0_{2\times2} & A_{pll}+[B_{ll}T_{vo2}\ \ 0_{2\times1}]_{2\times2} \end{bmatrix}_{6\times6},$$

$$B_{Cont}=\begin{bmatrix} \underbrace{\begin{pmatrix} B_{v1} \\ B_{cc1}D_{v1} \\ 0_{2\times1} \end{pmatrix}}_{B_{Cont1}} & \underbrace{\begin{pmatrix} [B_{v2} & 0_{2\times1}]T_{vo1} \\ [B_{cc1}D_{v2} & 0_{2\times1}]T_{vo1} \\ B_{ll}T_{vo1} \end{pmatrix}}_{B_{Cont2}} & \underbrace{\begin{pmatrix} B_{v3} \\ B_{cc1}D_{v3} \\ 0_{2\times1} \end{pmatrix}}_{B_{Cont3}} & \underbrace{\begin{pmatrix} B_{v4} \\ B_{cc1}D_{v4} \\ 0_{2\times1} \end{pmatrix}}_{B_{Cont4}} & \underbrace{\begin{pmatrix} 0_{2\times2} \\ B_{cc2}T_{i1} \\ 0_{2\times2} \end{pmatrix}}_{B_{Cont5}} \end{bmatrix}$$

$$C_{Cont}=\begin{bmatrix} \underbrace{T_{v1}^{-1}D_{cc2}C_{v1}}_{C_{cont1}} & \underbrace{T_{v1}^{-1}C_{cc1}}_{C_{cont2}} & \underbrace{(T_{v1}^{-1}(D_{cc1}T_{i2}-T_{v2}+[D_{cc2}D_{v2}\ \ 0_{2\times1}]_{2\times2}+D_{cc3}))T_{vo2}}_{C_{cont3}} \end{bmatrix}_{2\times6}$$

$$D_{Cont}=$$

$$\begin{bmatrix} \underbrace{T_{v1}^{-1}D_{cc2}D_{v1}}_{D_{cont1}} & \underbrace{(T_{v1}^{-1}([D_{cc2}D_{v2}\ \ 0_{2\times1}]_{2\times2}+D_{cc3}))T_{vo1}}_{D_{cont2}} & \underbrace{T_{v1}^{-1}D_{cc2}D_{v3}}_{D_{cont3}} & \underbrace{T_{v1}^{-1}D_{cc2}D_{v4}}_{D_{cont4}} & \underbrace{T_{v1}^{-1}D_{cc1}T_{i1}}_{D_{cont5}} \end{bmatrix}_{2\times6}$$

where,

$$A_{Cont}=B_{Cont}=[\Delta\varphi_{dc}\quad \Delta\varphi_{ac}\quad \Delta\varphi_{id}\quad \Delta\varphi_{iq}\quad \Delta\theta_{pll}\quad \Delta\varphi_{pll}]^T$$

$$C_{Cont}=D_{Cont}=\left[\Delta V_{dc}\quad \Delta V_{odq}^{g}\quad \Delta V_{dc}^{*}\quad \Delta V_{od}^{*}\quad \Delta I_{dq}^{g}\right]^T$$

Combining both power circuit and controller models together and conducting algebraic manipulation as in Appendix A.3.1, the final small-signal state-space model of the grid-connected VSC system in a grid frame is as follows (3.53):

$$A_{Sys-tot}=$$

$$\begin{bmatrix} A_{pc}+B_{pc1}[D_{cont1}\quad D_{cont5}^{-}\quad D_{cont2}^{-}]_{2\times5} & B_{pc1}[C_{cont1}\ \ C_{cont2}\ \ C_{cont3}]_{2\times6} \\ [B_{cont1}\quad B_{cont5}^{-}\quad B_{cont2}^{-}]_{6\times5} & A_{cont} \end{bmatrix}_{11\times11}$$

$$B_{Sys-tot}=\begin{bmatrix} B_{pc3} & B_{pc2} & D_{cont3} & D_{cont4} \\ 0_{6\times1} & 0_{6\times2} & B_{cont3} & B_{cont4} \end{bmatrix}_{11\times5} \tag{3.53}$$

where,

$$[A_{Sys}]= \begin{bmatrix} \Delta V_{dc} & \Delta I_d^g & \Delta I_q^g & \Delta I_{gd}^g & \Delta I_{gq}^g & \Delta\varphi_{dc} & \Delta\varphi_{ac} & \Delta\varphi_{id} & \Delta\varphi_{iq} & \Delta\theta_{pll} & \Delta\varphi_{pll} \end{bmatrix}^T$$

$$B_{Sys-tot} = \begin{bmatrix} \Delta I_{dc} & \Delta V_{gdq}^g & \Delta V_{dc}^* & \Delta V_{od}^* \end{bmatrix}^T$$

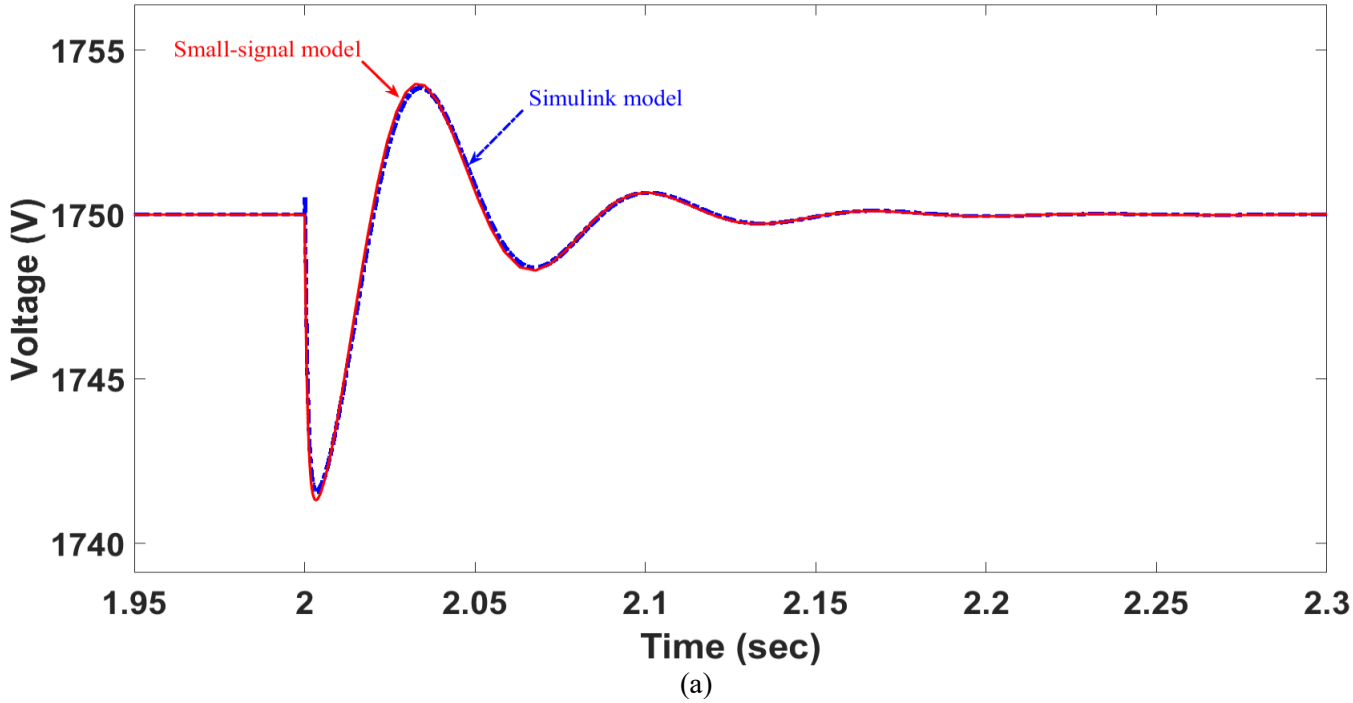
Capturing all the dynamics of the system in Fig 3.2, can be presented by A_{Sys}. It also can be founded by the input impedance ($\Delta Z_{sys} = \Delta V_{dc}/\Delta I_{dc}$) after applying the transformation from state space to impedance model, shown in Appendix A.3.2. [102], in the final small-signal model of the system (3.53).

3.5.3 Verification of Small-Signal Model Against Large-Signal Model

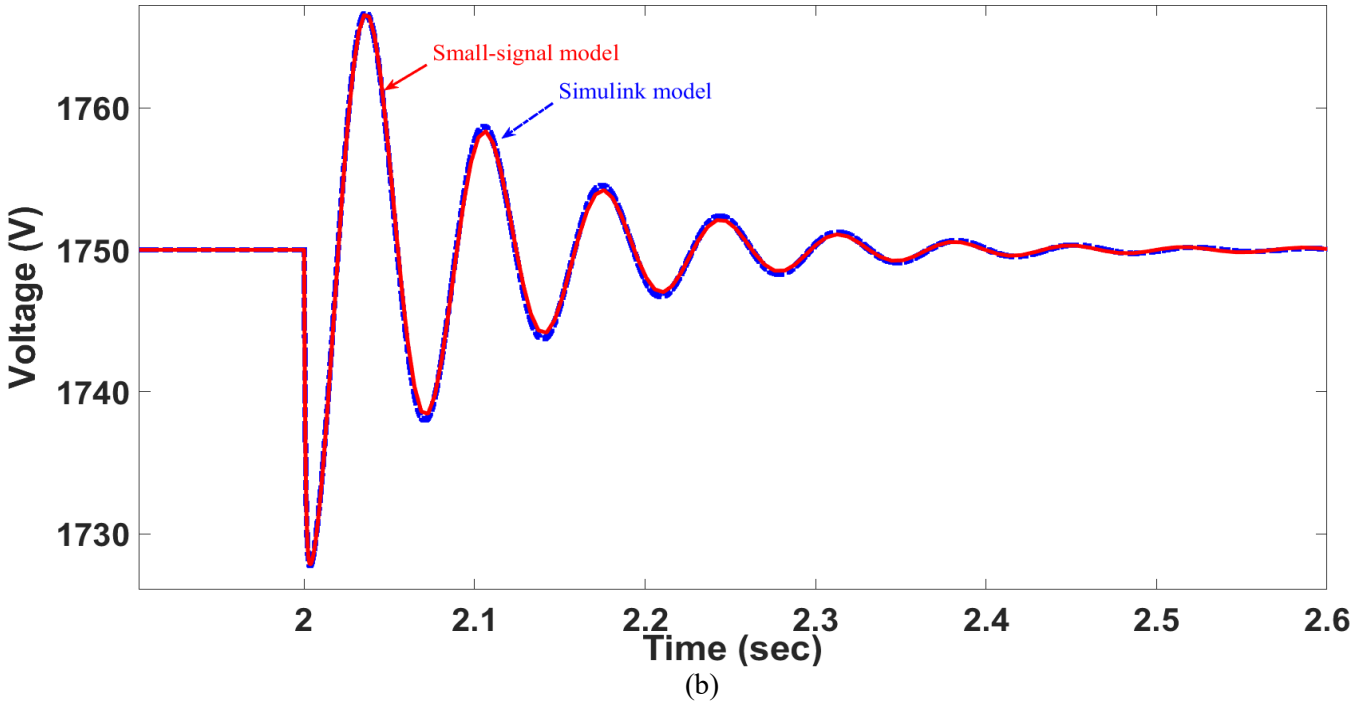
To validate the analytical results, the proposed linearized model must be verified. For this reason, a detailed time-domain model of the grid-connected VSC was simulated in a MATLAB/Simulink environment. The state-space small-signal model in (3.53) was examined under different critical operating points, and then the response of the small-signal model was compared to the constructed nonlinear time-domain model. The verification between the two models was completed under two different case scenarios in inversion and rectification modes. The first case was at *SCR*=10 and the second case was at *SCR*=2. In both cases, the active power injected from the DC side was set to 1 pu and PCC voltage was regulated at 1 pu. For accurate verification, both models were examined under the same parameters and deliberately induced disturbances. Verifying both models by checking only one signal response is not a certified method. Therefore, verification was completed for two different signals to ensure that all the responses from both models were compatible. These two signals included DC-link voltage and PLL angular frequency (ω_{pll}). In verification case I, both models were verified under P_{in}= ±1 pu and *SCR*=10 in inversion and rectification mode. For the sake of verification, a deliberate 5% disturbance in DC-side input active power was applied at t = 2 s. In Figs. (3.11 and 3.12), it can be clearly noted that the nonlinear time-domain model (blue signal) and linear small-signal model (red signal) have the same responses for the three different signals in inversion and rectification modes, respectively. In order to examine the robustness of the linearized small-signal model, both models were verified under critical conditions, meaning at a very weak grid condition, as will be shown in verification case II. The verification steps for the second case were similar to the previous case, except the SCR changed from 10 to 2 for the purpose of adjusting the grid strength. An accurate compatibility between both models in inversion and rectification modes is clearly

illustrated in Figs. (3.11 and 3.12). As a result, the developed linearized small-signal model is certified and ready to use for analysis.

3.5.3.1 Case I: At $SCR \geq 10$



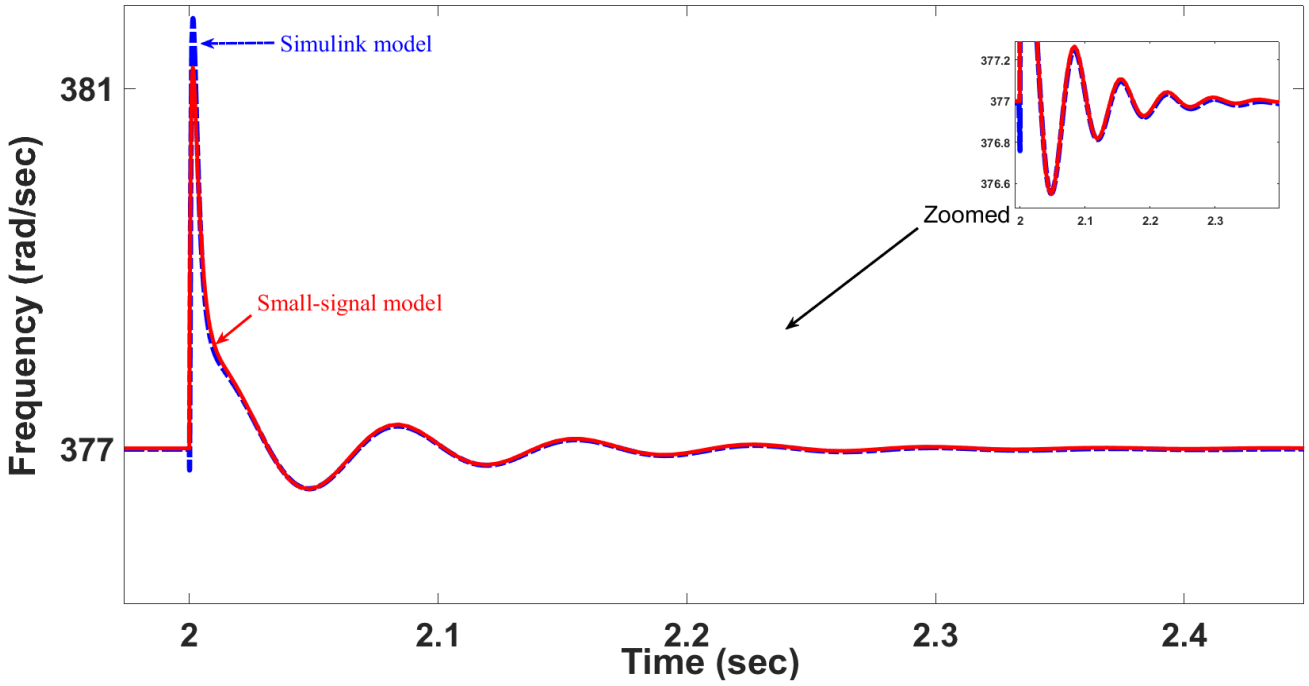
(a)



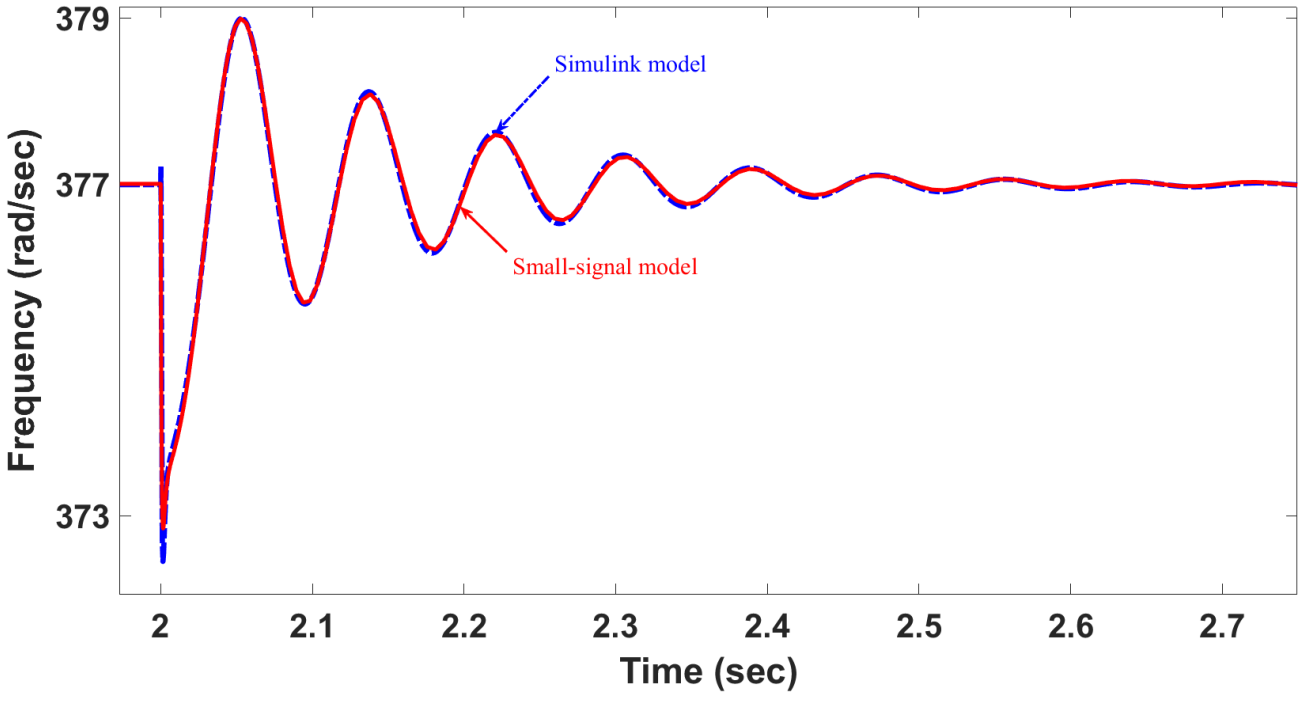
(b)

Figure 3.11 Verification of the small-signal model against the time-domain model at P_{in}= ±1 pu a) response of DC-link voltage in inversion mode, b) response of DC-link voltage in rectification mode

3.5.3.2 Case II: At $SCR \leq 2$



(a)



(b)

Figure 3.12 Verification of the small-signal model against the time-domain model at P_{in}=± 1 pu a) response of PLL angular frequency (ω_{pll}) in inversion mode, b) response of PLL angular frequency (ω_{pll}) in rectification mode.

3.6 Summary

This chapter presented a detailed diagram of the studied system, which was a grid-connected voltage source converter with controllers. Moreover, the parameters of each component of the system were reported, and the methodology of linearization was clarified. This method has been applied to the studied system to analyze the dynamic interactions. The controllers of the system have been discussed in detail. The four main controllers used in this study were: AC-current, DC-link voltage, AC-bus voltage, and PLL controllers. These controllers have been used for the VSC to control the active and reactive power separately in both directions while maintaining the system stability. It is worth mentioning that all the controllers have been applied under the classical vector control approach. The design criteria for each controller of the VSC has also been illustrated. The dynamics of the system have been represented mathematically for the purpose of analysis. Firstly, this chapter reported the nonlinear mathematical model. Then the small-signal model that represents the dynamics of the system was derived from the nonlinear model and presented. In order to validate the derived small-signal model, a detailed time-domain model of the grid-connected VSC was constructed and simulated in a MATLAB/Simulink environment. Different critical case scenarios were applied to test the validity and reliability of the model. The presented validation figures clearly show a close match between the two models. Therefore, the mathematical approach was validated and is ready to be implemented for analysis, as will be discussed in the next chapter.

Chapter 4

Analysis and Evaluation Results

4.1 Introduction

Using the linearization model derived from the state-space small-signal model in the preceding chapter, this chapter provides a stability interaction analysis of how VSC stability depends on grid connectivity. The analysis is focused on studying the impact of a weak and very weak grid on the VSC when the DC-link capacitance is subjected to variation. Furthermore, the impact of line filter inductance, grid impedance is also examined by using linear tools such as eigenvalue analysis. All of the results in this chapter are produced using the system parameters' initial values as shown in Table 3.1. For this analysis, the value of the SCR is deliberately chosen as the critical stability condition in each operation mode to maximize the accuracy of the analysis. The analysis in this chapter comprises five main case studies: 1) the effect of DC-link capacitance uncertainty on different grid strength conditions, 2) the effect of DC-link capacitance uncertainty on the controllers' bandwidth, 3) the effect of DC-link capacitance uncertainty on grid-angle variations, 4) fault analysis and 5) The impacts of parameters L_g , R_g and L_f on the dynamic stability of grid-connected VSC.

4.2 The Effect of DC-link Capacitance Uncertainty on Different Grid Strength Conditions

4.2.1 Inversion Mode

This case scenario study when input active power is equal 1 pu and SCR changes from 3 to 1.1, and the equivalent DC-link capacitance changes from 0.6 to 1 pu. From the eigenvalue loci plotted in Fig 4.1, the system stability trend is changed when the grid strength becomes very weak. Each SCR value is marked by a different symbol shape to clearly show the associated eigenvalue migration. When $SCR < 2$, the modes $\lambda_{6,7}$ rapidly migrate to the right side which means that the system stability is greatly degraded. The influence that drives modes $\lambda_{6,7}$ toward the right belongs to the state of the AC-voltage controller ($\Delta\varphi_{ac}$).

Different system stability behaviors are shown in Fig 4.1, depending on the equivalent DC-link capacitance and SCR. When the grid is strong, reducing the DC-link capacitance moves the poles

toward the left side of the dashed line, which enhances system stability. This result is confirmed with analysis conducted in [85]. Conversely, as the grid weakens, reducing DC-link capacitance significantly degrades system stability. At *SCR*<1.15 the system stability degraded to the most when decreasing the Cdc_{eq}. It is worth mentioning that, under weak grid conditions, the system can be destabilized even if the reduction of Cdc_{eq} varied by 10% or less.

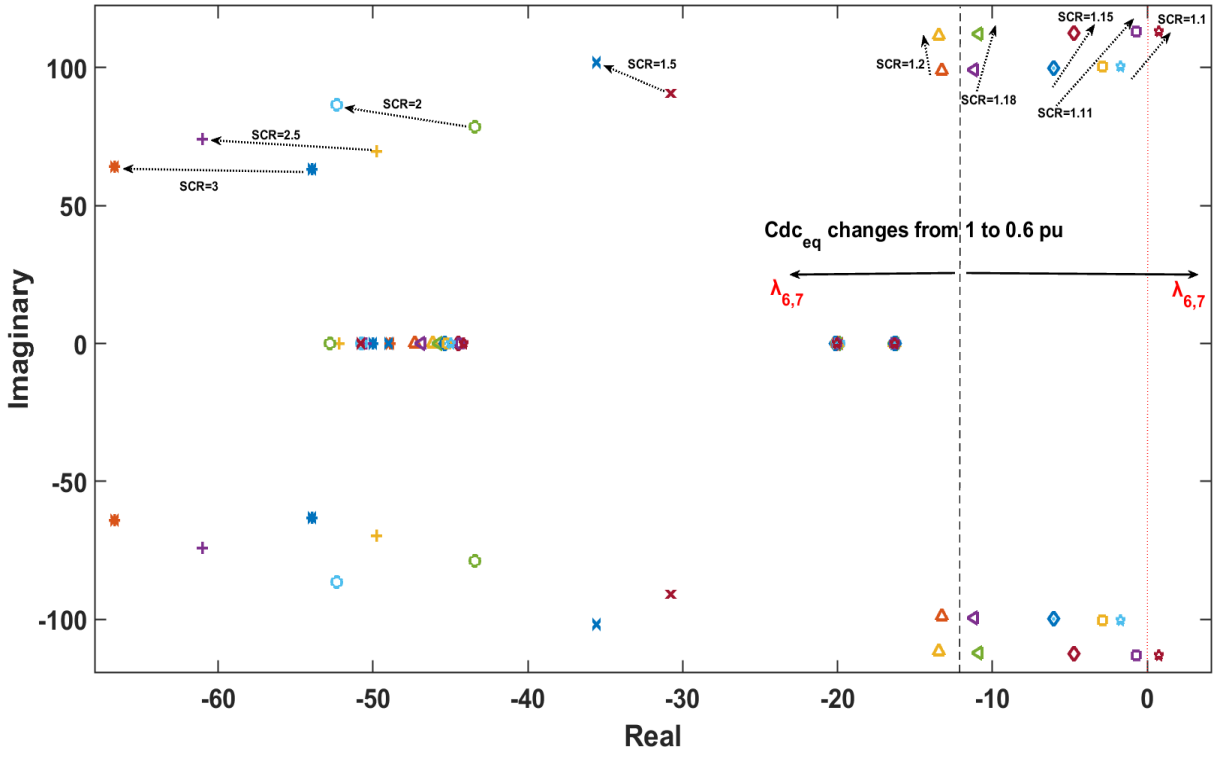


Figure 4.1 Eigenvalues of the grid-connected VSC system with varying SCR and DC-link capacitance.

These findings can be more deeply understood via a 3D visualization. Figure 4.2 represents the relation between DC-link capacitance, SCR and damping factor. The z-axis represents the DC-link capacitance and damping factor. The DC-link capacitance varies between 0.6 and 1 pu. for each value of SCR (bars close to the z-axis). It can be noted that, as SCR changes from 1.5 to 1.2, the damping factors decrease when Cdc_{eq} increases. When *SCR* < 1.2, the system stability degrades when Cdc_{eq} decreases (dashed bars). The system tends to be marginally stable at *SCR*=1.11 and Cdc_{eq}= 0.6 pu. (orange dashed bar).

Figures (4.3 and 4.4) show the time-domain and small-signal models at *SCR*=1.5 and 1.11, and Cdc_{eq}= 0.6 and 1 pu., respectively. It can be observed from Fig. 4.3 that increasing the DC-link capacitance leads to increased settling time at *SCR*= 1.5. On the other hand, decreasing the DC-

link capacitance at *SCR*=1.11 leads to significantly increased settling time, which implies to degrading system stability.

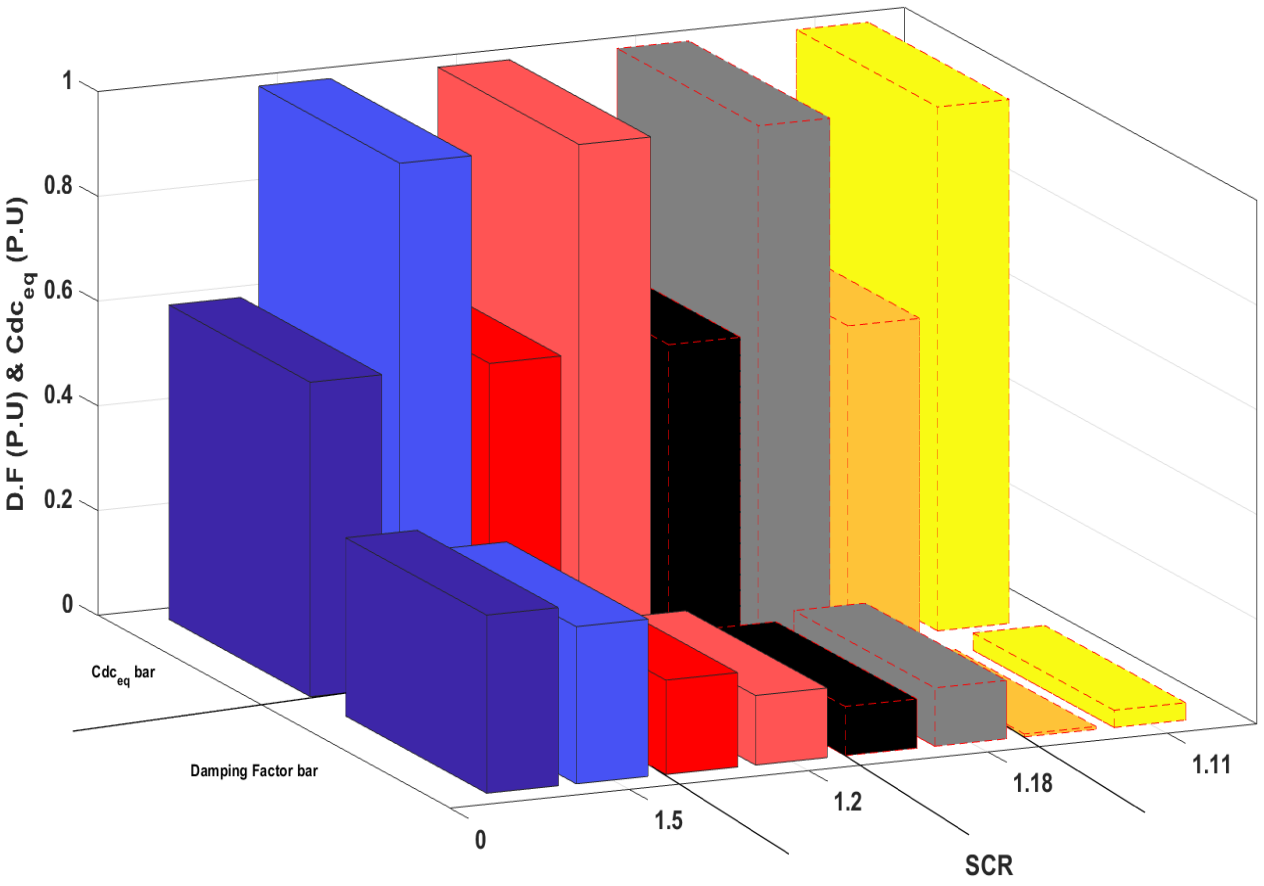


Figure 4.2 Relation between DC-link capacitance, SCR and damping factor of the grid-connected VSC system in inversion mode

4.2.2 Rectification Mode

In this subsection, the same stability study of the preceded subsection will be addressed but in rectification mode. The analysis has been done with the SCR varied from 2.5 to 1.42, and the equivalent DC-link capacitance changed from 0.35 to 1.15 pu. The SCR range is chosen between 2.5 and 1.42 to examine the effect of the DC-link capacitance uncertainty under challenging grid condition. Further, it has been found that, under stiff grid conditions, the effect of DC-link capacitance uncertainty is minimal on system stability as shown in Fig. A.4.1. The locus of eigenvalues plots in Figs. (4.5 and 4.6) illustrate the stability of the grid-connected VSC system under different ranges of SCR and Cdc_{eq}. Figure 4.5 shows that system stability is not highly

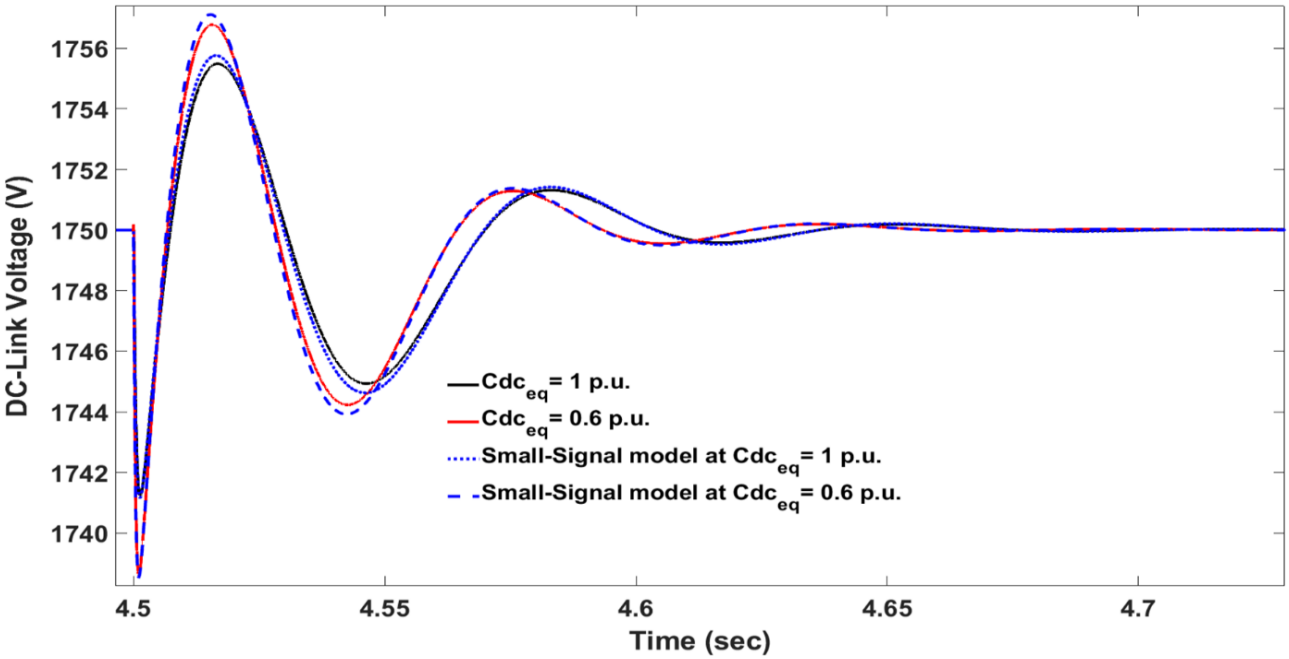


Figure 4.3 Time-domain model of the grid-connected VSC system at *SCR*=1.5, Cdc_{eq}= 0.6 and 1 pu.

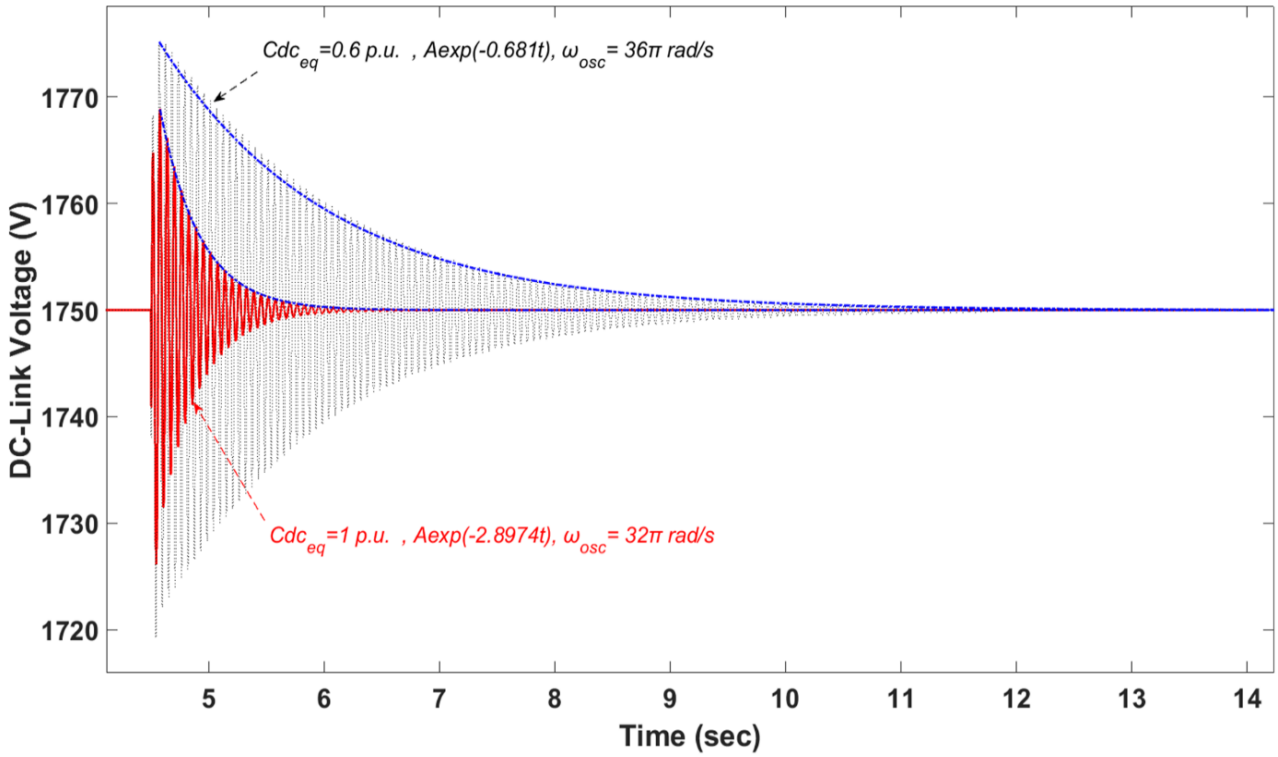


Figure 4.4 Time-domain model of the grid-connected VSC system at *SCR*=1.11, Cdc_{eq}= 0.6 and 1 pu.

affected when the DC-link capacitance varies from 0.35 to1.65 pu. at *SCR*=2.5, which is similar to the previous operational mode at *SCR* > 1.2. The most important observation here is that

decreasing the DC-link capacitance shifts the eigenvalues to the left side, which indicates increase in the damping factor. This result has been also confirmed for $SCR \geq 2.5$. On the other hand, Fig. 4.6 (a) and (b) illustrate that, when $SCR \leq 1.42$, variations in the DC-link capacitance clearly affect system stability in a very weak grid. From these plots, the eigenvalues show that system stability is confined to a certain range for DC-link capacitance variations.

From participation factor analysis, it is shown that, when the DC-link capacitance increases (i.e. Cdc_{eq}=1.5), the influence that drives mode $\lambda_{6,7}$ toward the right belongs to the state of the DC-link voltage controller ($\Delta\varphi_{dc}$). Whereas, when the DC-link capacitance decreases (i.e. Cdc_{eq}=0.35 pu), the influence that drives mode $\lambda_{4,5}$ toward the right side is related to the state of the DC-link voltage (ΔV_{dc}). Although in Fig. 4.6(b) at Cdc_{eq}=0.35 pu. the poles ($\lambda_{6,7}$) are located on the left hand side (red dashed circle), poles ($\lambda_{4,5}$) of the same DC-link capacitance value are located on right hand side as shown in Fig. 4.6(a).

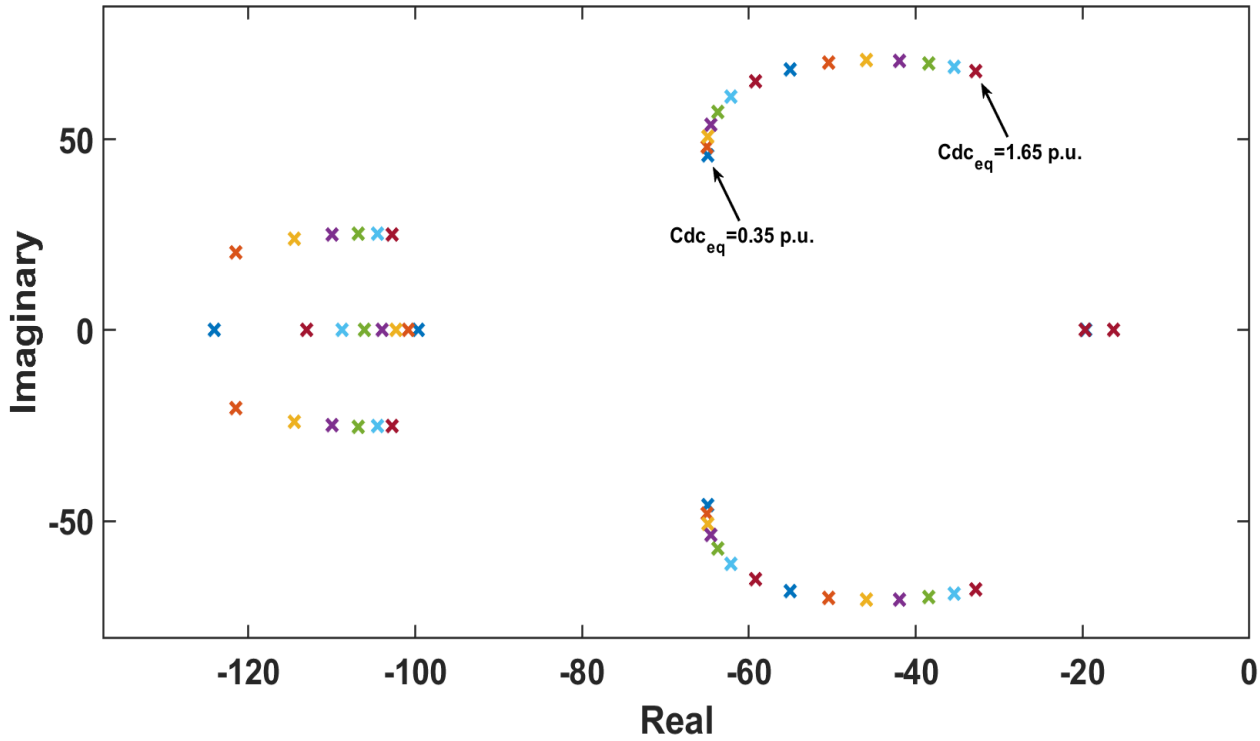
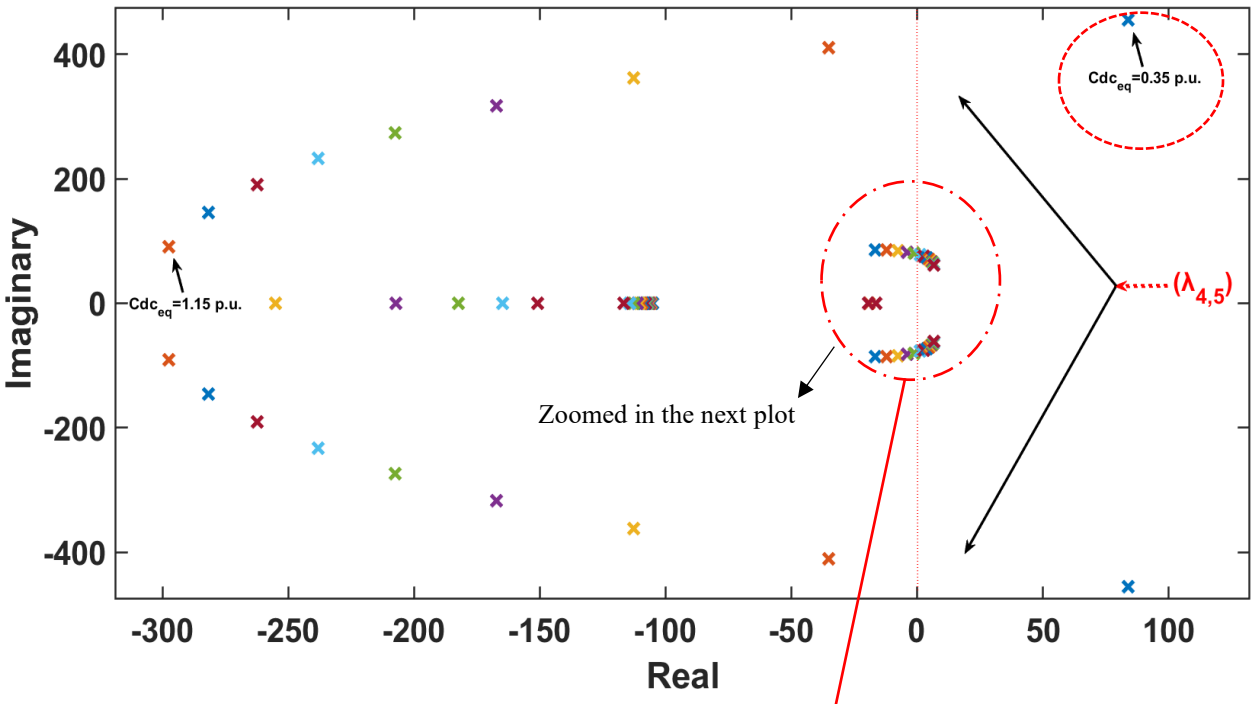
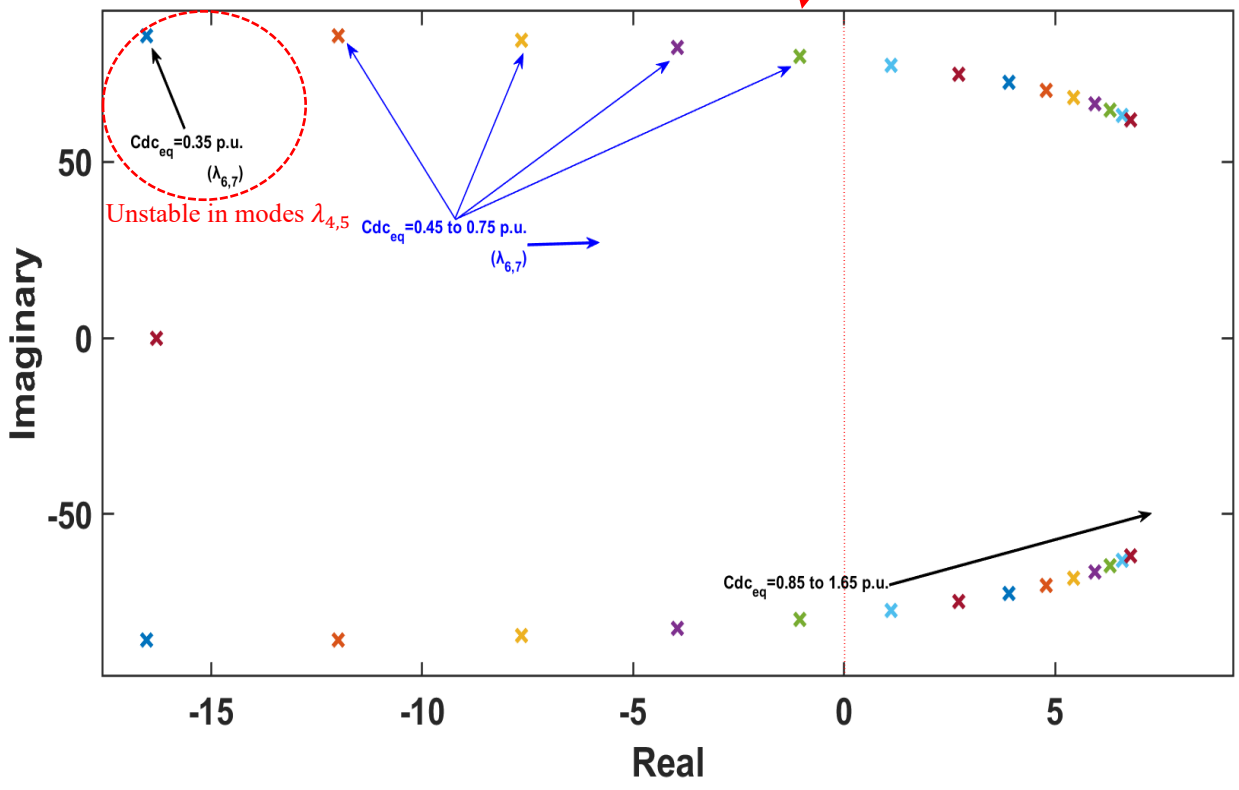


Figure 4.5 Eigenvalues of the grid-connected VSC system at *SCR*= 2.5 with varying DC-link capacitance between 0.35 and 1.65 pu.

Similar to the 3D plot in Fig. 4.2, Fig. 4.7 represents the relation between DC-link capacitance, SCR and damping factor in rectification mode. The DC-link capacitance varies among 0.5, 1 and 1.5 pu. at each SCR value (bars close to the *z*-axis).



(a)



(b)

Figure 4.6 Eigenvalues of the grid-connected VSC system. a) At *SCR*= 1.42 with varying DC-link capacitance between 0.35 and 1.15 pu., b) Zoomed plot

From the plot, it can be noted that for lower SCR values, the damping factors generally decrease when Cdc_{eq} increases. When the grid becomes very weak ($SCR < 2$), the DC-link capacitance on system stability has a stronger effect as the damping factor is significantly decreasing. At SCR=1.5, system stability becomes very weak when Cdc_{eq}=1.5 pu. (yellow dashed bar).

Figures (4.8 and 4.9) show the time-domain and small-signal models at SCR= 4 and 1.5, and Cdc_{eq}= 0.5 and 1.5 pu., respectively. In both figures, increasing DC-link capacitance leads to increases in settling time and oscillations die-off period.

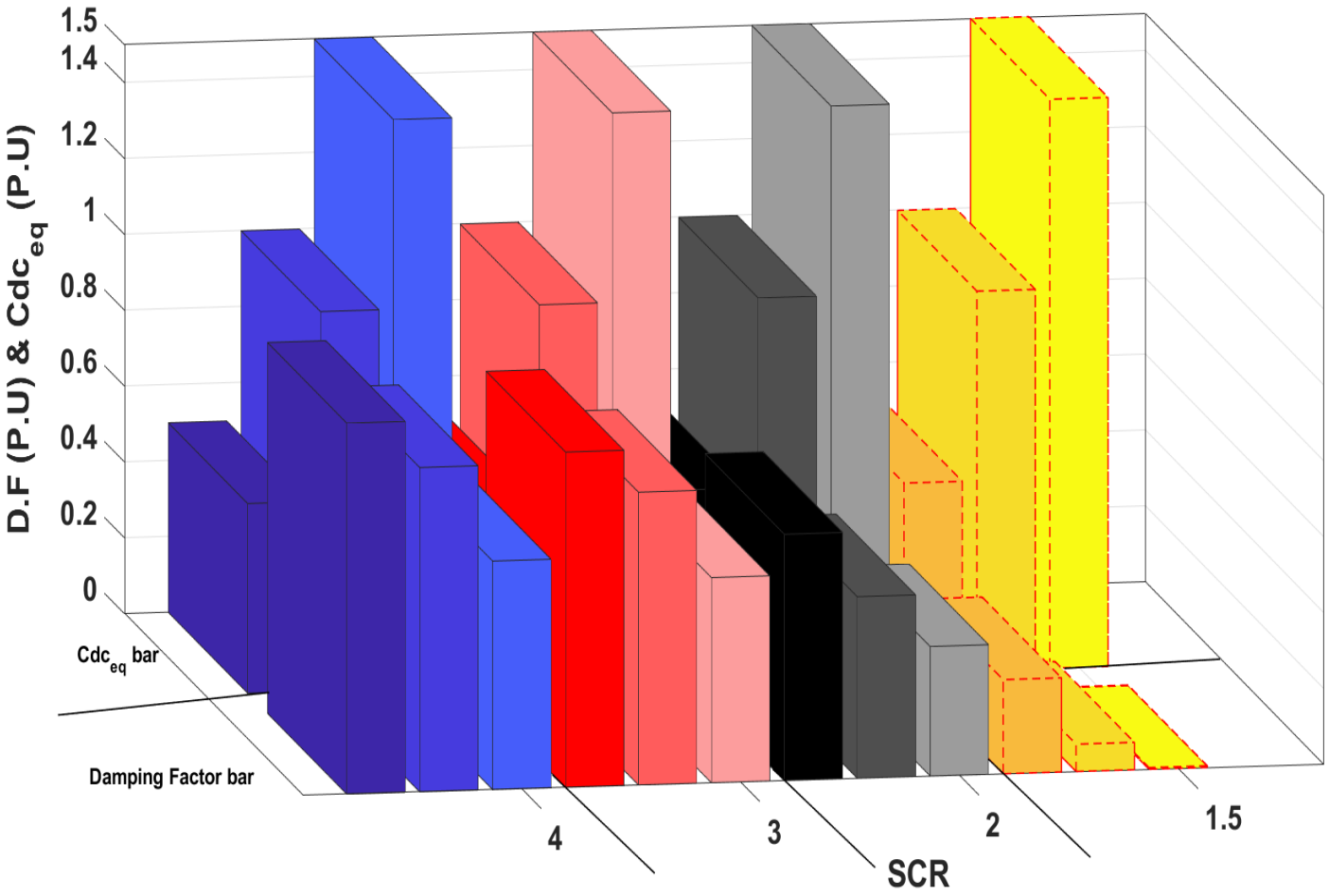


Figure 4.7 Relation between DC-link capacitance, SCR and damping factor of the grid-connected VSC system in rectification mode

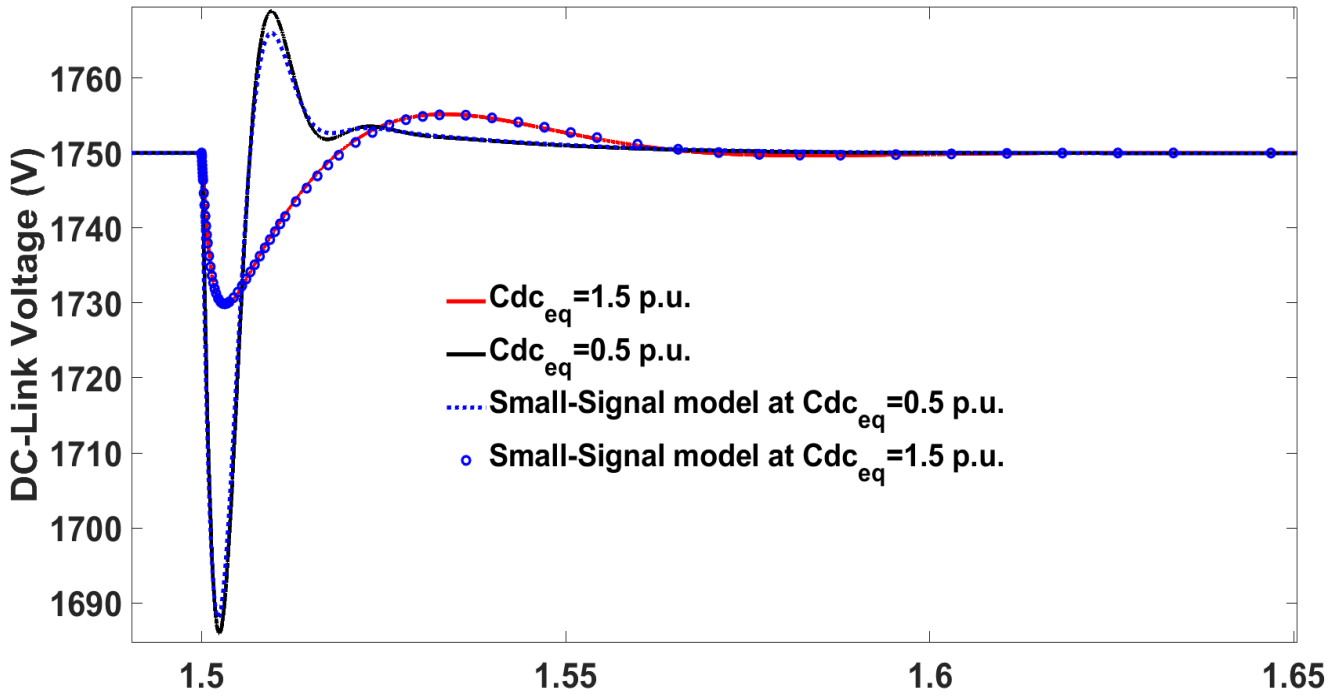


Figure 4.8 Time-domain model of the grid-connected VSC system at *SCR*=4, Cdc_{eq}= 0.5 and 1.5 pu.

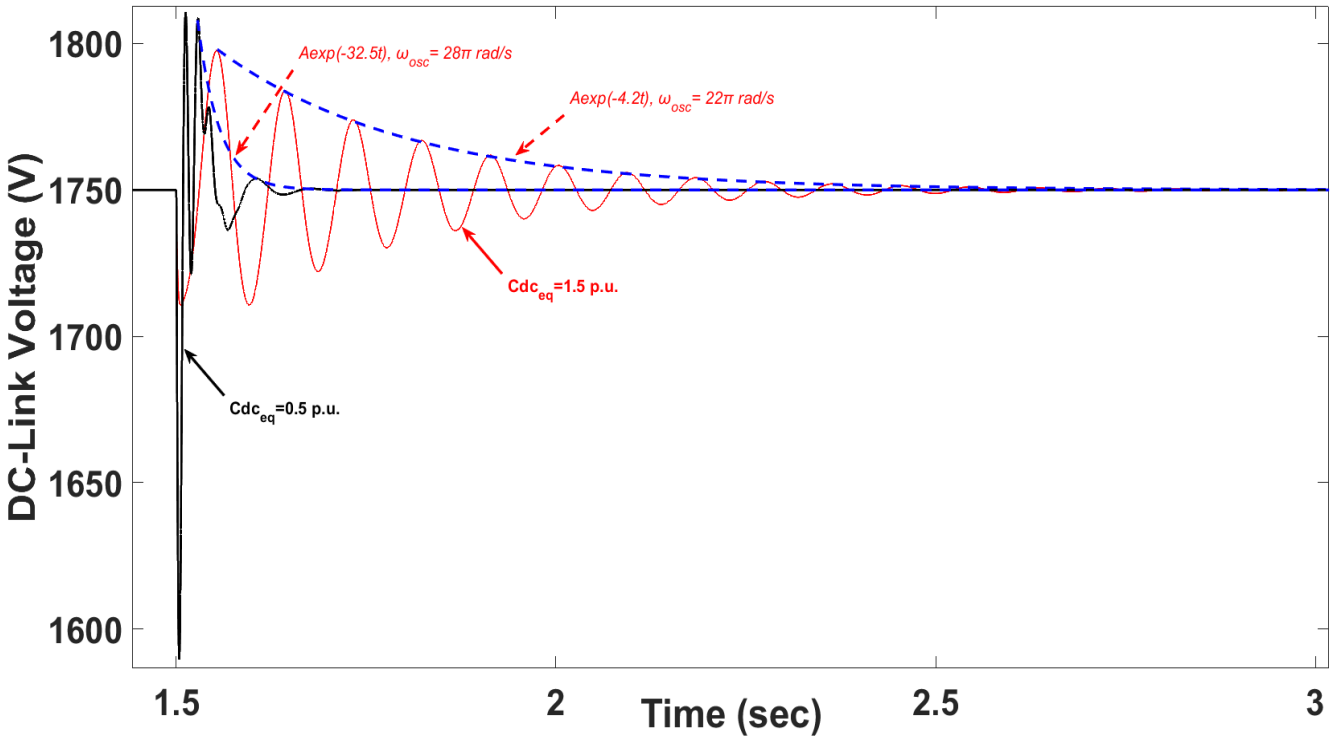
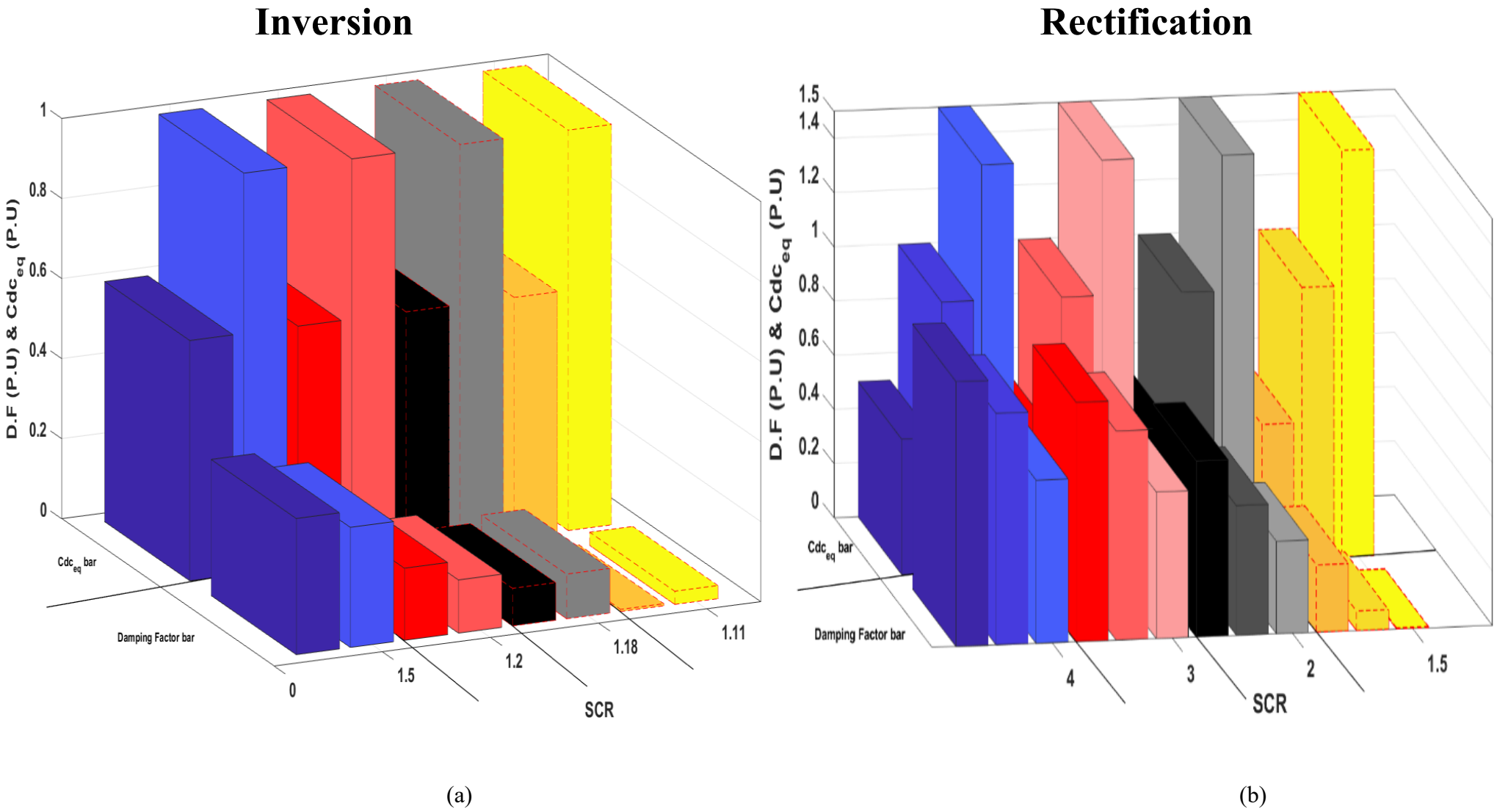


Figure 4.9 Time-domain model of the grid-connected VSC system at *SCR*=1.5, Cdc_{eq}= 0.5 and 1.5 pu.

Figure 4.10 combines the results of inversion and rectification modes to clearly present the impact of the DC-link capacitance, SCR and damping factor on the stability of the grid-connected VSC system. Further, the key results of this section can be concluded as in the following table:

Table 4.1 Key outcomes from investigating the effect of Cdc_{eq} in accordance with different grid strength conditions

Inversion	**Rectification**
• At *SCR* ≥1.2 the effect of DC-link capacitance uncertainty on system stability is not significant. Further, increasing the DC-link capacitance value leads to decreasing the damping factor. • At *SCR* < 1.2, the system stability enhances as the DC-link capacitance increases.	• The system stability performance has same trend even at very weak-grid condition in term of DC-link capacitance variations, unlike the inversion mode. • At *SCR* ≥2, the reduction of damping factor percentage with increasing the DC-link capacitance is almost having same pattern. • At *SCR* < 2, the damping factor is steeply decreased when the DC-link capacitance increases. In addition, the system stability is confined to a certain range for DC-link capacitance variations.



(a) (b)

Figure 4.10 Relation between DC-link capacitance, SCR and damping factor of the grid-connected VSC system. a) Inversion mode, b) Rectification mode

4.3 The Impact of DC-link Capacitance Uncertainty on Controller Bandwidth

4.3.1 Effect of DC-link Capacitance and SCR on DC-Bus Voltage Controller Bandwidth

4.3.1.1 Inversion Mode

This subsection addresses the effects of DC-link capacitance uncertainty and DC-link voltage controller on the system stability. Figures 4.11 and 4.12 show an eigenvalue analysis of the system when the bandwidth of the DC-link voltage controller (BW_{dc}) and DC-link capacitance value are varied. Commonly, the bandwidth of DC-link voltage controller is chosen to be one-fifth of the current controller bandwidth (BW_{cc}), as mentioned in chapter 3. In both figures, however, the default case is BW_{dc} =0.2 BW_{cc}. Two conditions have been studied to carefully investigate the effect of both components when the system is stable (i.e., *SCR*=1.5) and critically stable (*SCR*=1.11). In this analysis, the study is conducted by varying BW_{dc} from 0.1 to 0.5 of BW_{cc} and varying Cdc_{eq} at each bandwidth value. Figure 4.11 shows that, at *SCR*=1.5, the system remains stable over all the changes in bandwidth and DC-link capacitance values. It is clear that the decreasing BW_{dc} and increasing Cdc_{eq} degrades the system stability. As is clear in the figure, when Cdc_{eq} =0.5 pu. and the DC-link capacitance bandwidth changes between 0.1 and 0.5 BW_{cc}, the damping ratio increases from 0.25 to 0.42 as shown in Table 4.2. The damping ratio, therefore, increases by almost 60%. When SCR is reduced 1.11, system stability degrades with decreases in DC-link capacitance and DC-link voltage controller bandwidth, as shown Fig. 4.12. The effect of Cdc_{eq} in this case is the opposite of when *SCR*=1.5. in this case, modes ($\lambda_{6,7}$) are the dominant and the influencing states related $\Delta\varphi_{ac}$ and ΔV_{dc} as illustrated in Table 4.3. A time-domain simulation was confirmed these findings as clear in Fig. 4.13. Further, this result confirms the findings in the previous section. From both figures, it can be noted that, when the grid become very weak or critically stable, the stability behaviour changes as Cdc_{eq} changes. At the key point, when SCR decreases to low ranges, increasing the DC-link voltage controller bandwidth and decreasing the DC-link capacitance restore a system stability behaviour similar to that associated with higher SCR, which increases system stability. This trend can be surmised by looking at the case of BW_{dc} =0.5 BW_{cc} and BW_{dc} =0.2 BW_{cc} in both figures. The former case shows a similar stability pattern while the latter shows the opposite.

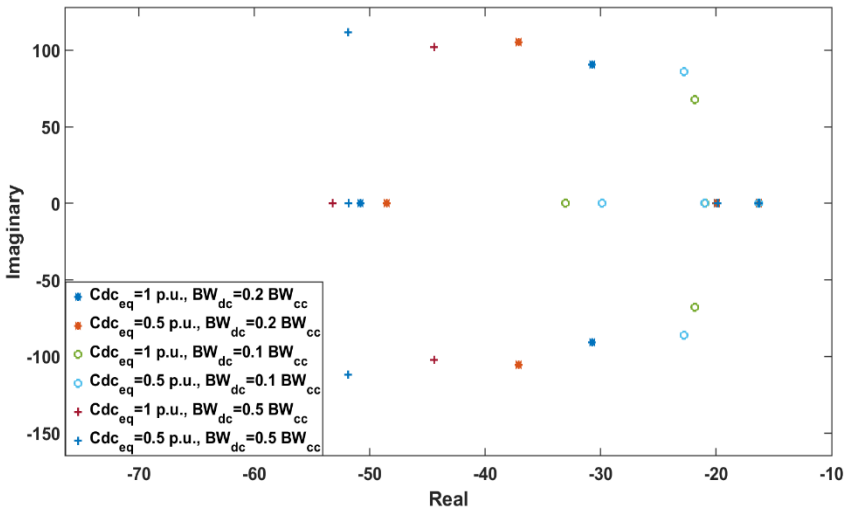


Figure 4.11 Root-locus of grid-connected VSC system at $P_{dc} = 1\ pu$ and *SCR*=1.5.

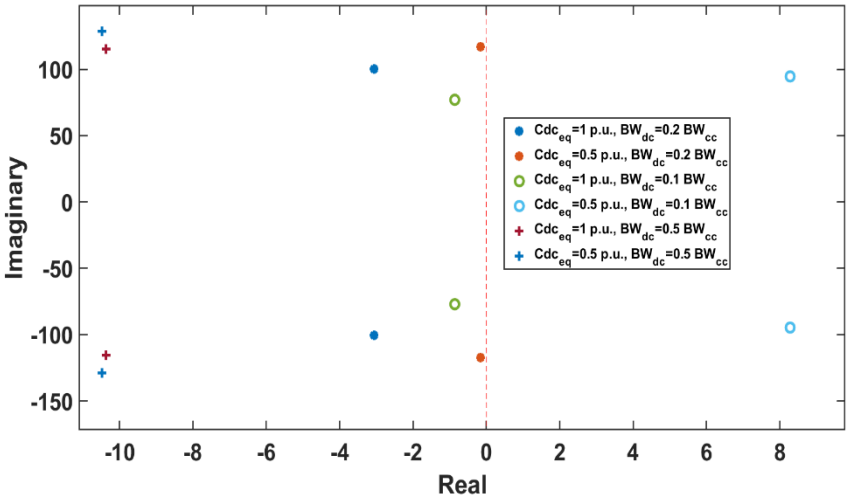
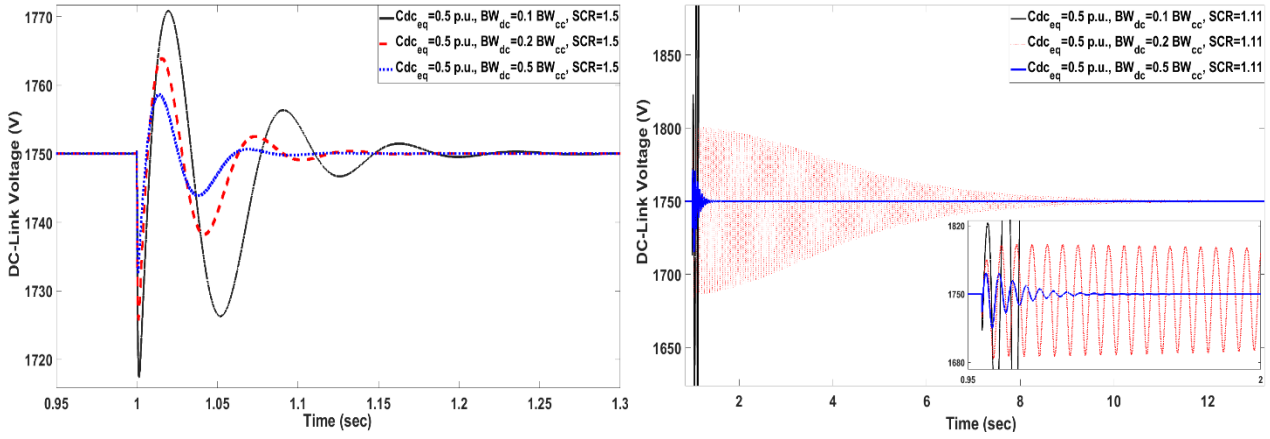


Figure 4.12 Root-locus of grid-connected VSC system at $P_{dc} = 1\ pu$ and *SCR*=1.11



(a) (b)

Figure 4.13 Time-domain of grid-connected VSC system at $P_{dc} = 1\ pu$, and *SCR*: a) *SCR*=1.5, b) *SCR*=1.11

Table 4.2 Damping factors corresponding to $\boldsymbol{\lambda_{6,7}}$, present the effect of DC-link capacitance and SCR on DC-bus voltage controller bandwidth in inversion mode

***SCR*=1.5**			
$\boldsymbol{Cdc_{eq}\ (pu)\backslash\ BW_{dc}(rad/sec)}$	0.1 BW_{cc}	0.2 BW_{cc}	0.5 BW_{cc}
0.5	0.2556	0.3326	0.4207
[1] **1**	0.3069	0.3208	0.4190
	Damping Factor (ζ)		
***SCR*=1.11**			
$\boldsymbol{Cdc_{eq}\ (pu)\backslash\ BW_{dc}(rad/sec)}$	0.1 BW_{cc}	0.2 BW_{cc}	0.5 BW_{cc}
0.5	Unstable	0.0013	0.0811
1	0.0112	0.0304	0.0895
	Damping Factor (ζ)		

[1] *The red color shows the damping factor of the nominal values of* Cdc_{eq} *and* BW_{cc}

Table 4.3 Participation factors corresponding to $\lambda_{6,7}$, present the effect of DC-link capacitance and SCR on DC-bus voltage controller bandwidth in inversion mode		
***SCR*=1.11, $\mathbf{BW_{dc} = 0.1\ BW_{cc}}$**		
DC-link capacitance value (PU)	Cdc_{eq}=0.5	Cdc_{eq}=1
Mode and Eigenvalue	$\lambda_{6,7}$= 8.3± 94.6i	$\lambda_{6,7}$= -0.862 ± 77.1i
Participation factors	$\Delta\varphi_{ac} = 0.47,\ \Delta\theta_{PLL} = 0.275, \Delta V_{dc}$=0.274	$\Delta\varphi_{ac} = 0.41,\ \Delta V_{dc}$=0.397, $\Delta\theta_{PLL}$=0.25, $\Delta\varphi_{dc}$=0.14
Dominant response mode	AC voltage controller	AC voltage controller
***SCR*=1.11, $\mathbf{BW_{dc} = 0.2\ BW_{cc}}$**		
DC-link capacitance value (PU)	Cdc_{eq}=0.5	Cdc_{eq}=1
Mode and Eigenvalue	$\lambda_{6,7}$= -0.157± 117.1i	$\lambda_{6,7}$= -3.07 ± 100.4i
Participation factors	$\Delta\varphi_{ac} = 0.5,\ \Delta\theta_{PLL} = 0.31, \Delta V_{dc}$=0.18	$\Delta\varphi_{ac} = 0.43,\ \Delta V_{dc}$=0.28, $\Delta\theta_{PLL}$=0.27, $\Delta\varphi_{dc}$=0.14
Dominant response mode	AC voltage controller	AC voltage controller

4.3.1.2 Rectification Mode

Figure 4.14 shows that, in the rectification mode, system stability can be reduced when the controller bandwidth and DC-link capacitance are subjected to variations not only in a very weak grid but also in stiff and weak grids. At *SCR*=3, system stability is lost when $BW_{dc} > 0.2\ BW_{cc}$ as shown in Fig 4.14. When *SCR*=1.45, Fig 4.15 shows that, and the bandwidth of the DC-link voltage controller decreases, system stability is slightly affected by changes in Cdc_{eq}. For instance, when $BW_{dc} < 0.2\ BW_{cc}$, modes ($\lambda_{4,5}$) move slowly toward the left but the damping ratio decreases

slightly from 0.85 to 0.82 when Cdc_{eq} changes from 1 to 0.5 pu., respectively as shown in Table 4.4. It is worth mentioning that, as indicated by the root locus in both figures, the dominant modes that determine system stability are $\lambda_{4,5}$. Participation factor analysis shows that the highest influencing state for theses modes is related to ΔV_{dc} as shown in Table 4.5. On the other hand, when the bandwidth of the voltage controller increases, the system becomes very sensitive to any variation in DC-link capacitance. At $BW_{dc} \geq 0.2\, BW_{cc}$ as shown in Fig. 4.15, the eigenvalues rapidly migrate to the right-side when the DC-link capacitance decreases. For instance, at $BW_{dc} = 0.2\, BW_{cc}$ and as Cdc_{eq} changes from 1 to 0.5 pu, the damping ratio decreases dramatically from 0.87 to 0.214. Figure. 4.17 illustrates the time-domain simulation that agreed with these findings.

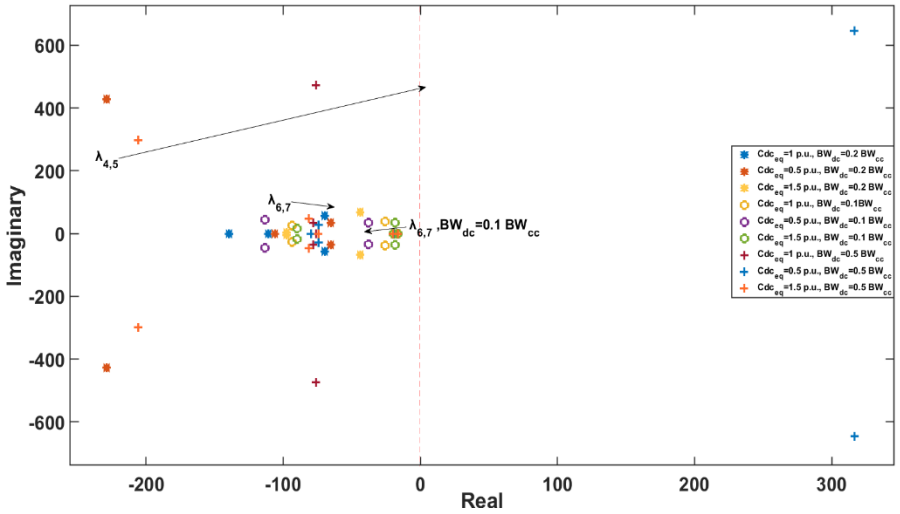


Figure 4.14 Root-locus of grid-connected VSC system at $P_{dc} = -1\ pu$ and $SCR = 3$.

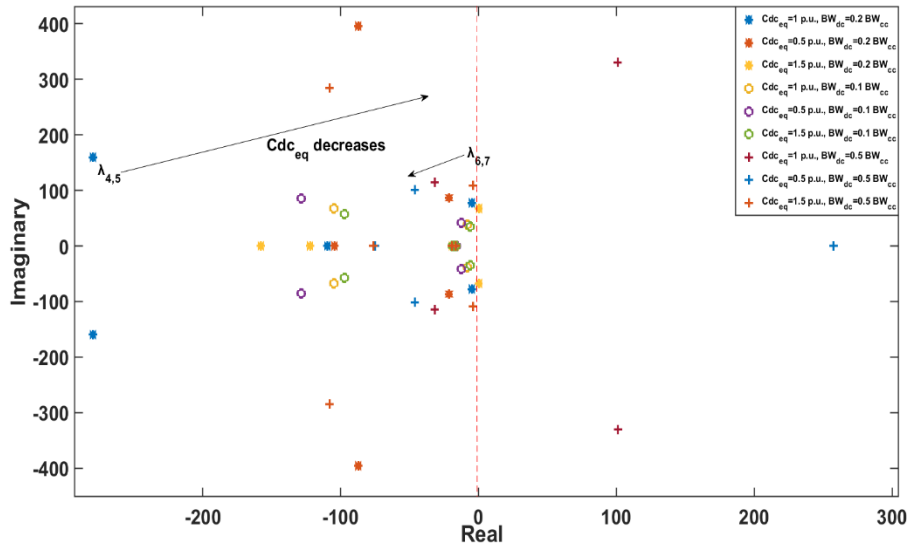


Figure 4.15 Root-locus of grid-connected VSC system at $P_{dc} = -1\ pu$ and $SCR = 1.45$

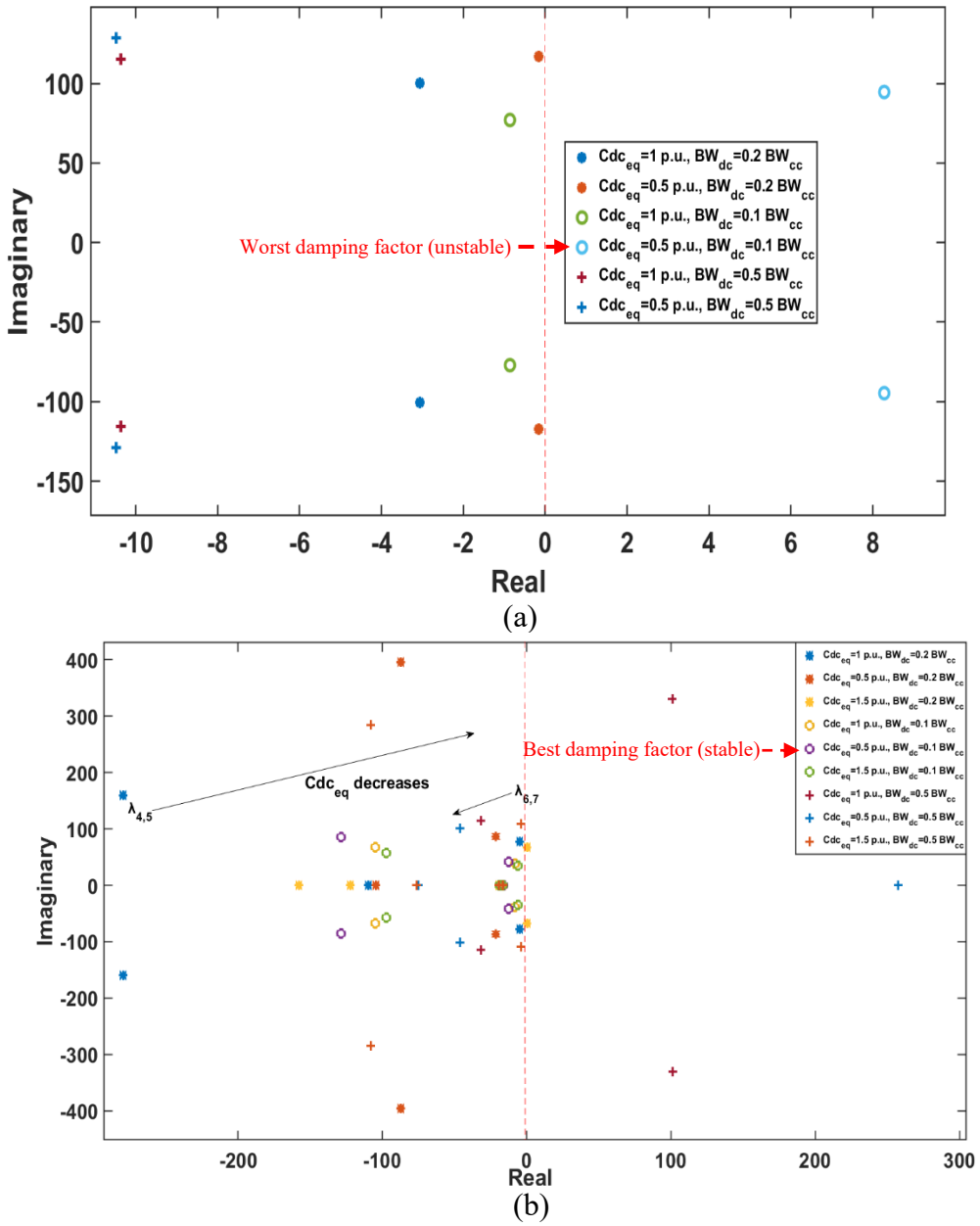


Figure 4.16 Root-locus of grid-connected VSC system at $P_{dc} = \pm 1\ pu$; (a) *SCR*=1.11 (Inversion), (b) *SCR*=1.45 (Rectification)

It can be concluded that increasing and decreasing the bandwidth BW_{dc} affects the system stability in both rectification mode and inversion mode. Figures 4.16 (a) and (b) show that, if the system is chosen to work at $BW_{dc} = 0.1\ BW_{cc}$ and Cdc_{eq} = 0.5 pu then the system is totally stable in the rectification mode but unstable in the inversion mode. Due to this duality, both modes must be considered when designing the DC-link voltage controller to maintain system stability especially in a very weak-grid condition and variation in the DC-link capacitance.

Table 4.4 Damping factors corresponding to $\boldsymbol{\lambda_{4,5}}$, present the effect of DC-link capacitance and SCR on DC-bus voltage controller bandwidth in rectification mode

***SCR*=3**			
$\boldsymbol{Cdc_{eq}\ (pu.)\backslash BW_{dc}(rad/sec)}$	0.1 BW_{cc}	0.2 BW_{cc}	0.5 BW_{cc}
0.5	0.9300	0.4713	Unstable
1	0.9630	0.7719	0.1588
1.5	0.9837	0.5411	0.5681
	Damping Factor (ζ)		
***SCR*=1.45**			
$\boldsymbol{Cdc_{eq}\ (pu.)\backslash BW_{dc}(rad/sec)}$	0.1 BW_{cc}	0.2 BW_{cc}	0.5 BW_{cc}
0.5	0.8249	0.2149	Unstable
1	0.8518	0.8689	Unstable
1.5	0.8594	$\lambda_{6,7}$ Unstable	0.3542
	Damping Factor (ζ)		

Table 4.5 Participation factors corresponding to $\lambda_{6,7}$ and $\lambda_{4,5}$, present the effect of DC-link capacitance and SCR on DC-bus voltage controller bandwidth in rectification mode		
***SCR*=3, $\mathbf{BW_{dc} = 0.5\ BW_{cc}}$**		
DC-link capacitance value (PU)	Cdc_{eq}=0.5	Cdc_{eq}=1
Mode and Eigenvalue	$\lambda_{6,7}$= -74.33± 28i	$\lambda_{6,7}$= -78.23 ± 35.7i
	$\lambda_{4,5}$= 317 ± 646i	$\lambda_{4,5}$= -76.2 ± 473.85i
Participation factors	$\Delta\varphi_{ac} = 0.95,\ \Delta\theta_{PLL} =$ 0.63, $\Delta\varphi_{dc}$=0.32	$\Delta\varphi_{ac} = 0.7, \Delta\theta_{PLL} =$ 0.6 ΔV_{dc}=0.23, $\Delta\varphi_{dc}$ =0.2
	ΔV_{dc}=1.1, ΔI_d=0.83	ΔV_{dc}=1.12, ΔI_d=0.9
Dominant response mode	AC voltage controller	AC voltage controller
	DC-ink voltage	DC-ink voltage
***SCR*=1.45, $\mathbf{BW_{dc} = 0.5\ BW_{cc}}$**		
DC-link capacitance value (PU)	Cdc_{eq}=0.5	Cdc_{eq}=1
Mode and Eigenvalue	$\lambda_{6,7}$= -46.3± 101.45i	$\lambda_{6,7}$= -31.7 ± 114.4i
	λ_4= 1057	$\lambda_{4,5}$= 101.44 ± 331i
	λ_5= 257.7	
Participation factors	$\Delta\theta_{PLL} = 0.52, \Delta\varphi_{ac} = 0.46$	$\Delta\theta_{PLL} = 0.57,\ \Delta\varphi_{ac} =$ 0.48, ΔV_{dc}=0.45, $\Delta\varphi_{dc}$ =0.3
	ΔV_{dc}=2.4, ΔI_{gd}=1.2	ΔV_{dc}=1.7, ΔI_d=0.92, $\Delta\varphi_{dc}$ =0.4
	ΔV_{dc}=1.22, ΔI_{gd}=0.9, $\Delta\varphi_{dc}$ =0.5	
Dominant response mode	AC voltage controller	AC voltage controller
	DC-ink voltage	DC-ink voltage
	DC-ink voltage	

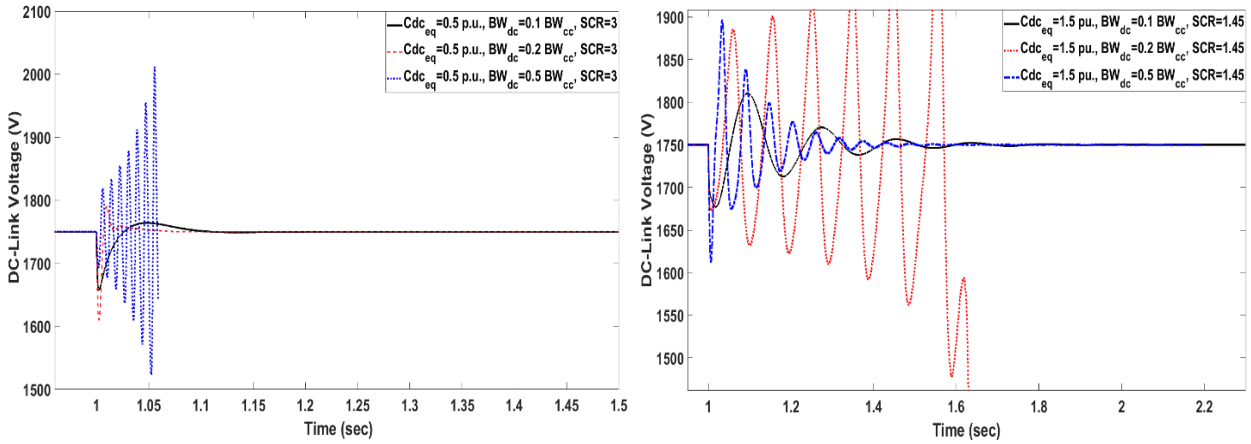
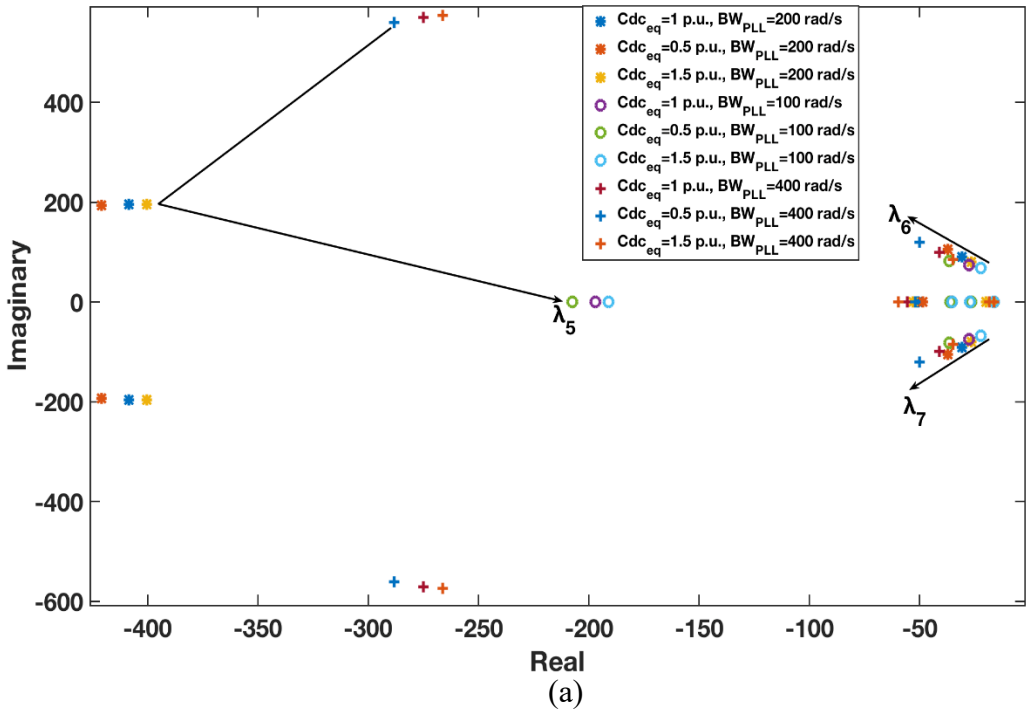


Figure 4.17 Time-domain of grid-connected VSC system at $P_{dc} = -1\,pu$ and *SCR*: a) *SCR*=3, b) *SCR*= 1.45

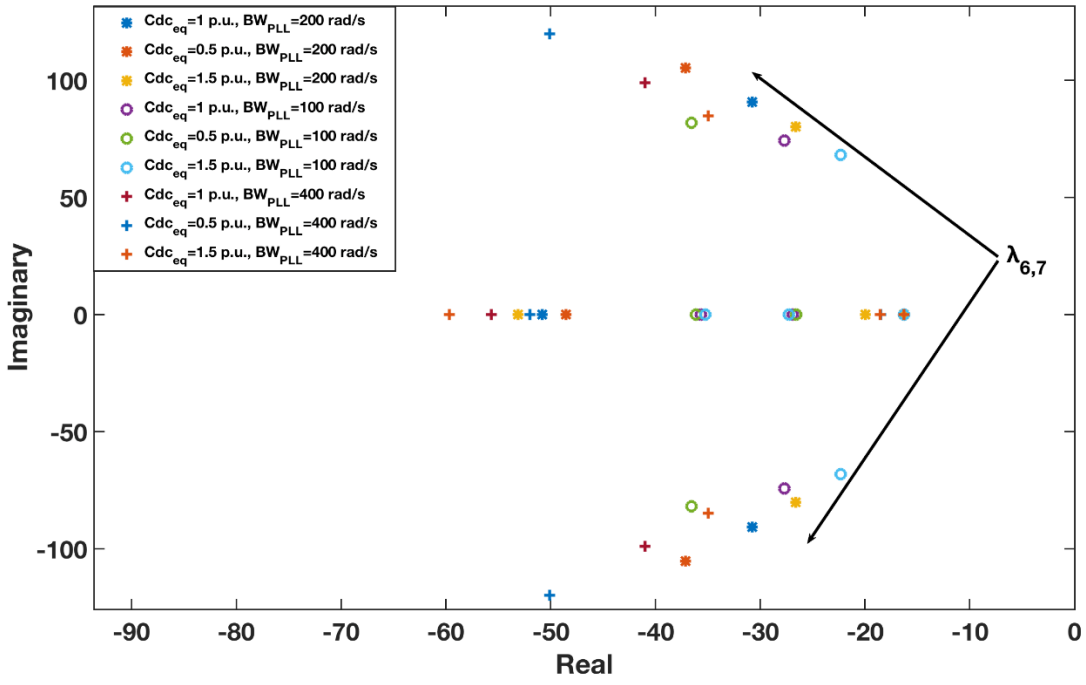
4.3.2 Effect of DC-Link Capacitance and SCR on SRF-PLL Bandwidth

4.3.2.1 Inversion Mode

Figures. 4.18 (a) and (b) show that system stability is not highly affected by PLL bandwidth (BW_{PLL}) and DC-link capacitance variations in the inversion mode at *SCR*=1.5. Figure 4.18 (b) illustrates that the damping ratio is slightly affected when Cdc_{eq} and BW_{PLL} are subjected to change, as clear in modes $\lambda_{6,7}$. The damping ratio is changed by only 10% to 15% when Cdc_{eq} and/or BW_{PLL} varies, as can be observed from Table 4.6.



(a)



(b)

Figure 4.18 Root-locus of grid-connected VSC system. a) at $P_{dc} = 1\ pu$ and *SCR*=1.5, b) Zoomed plot.

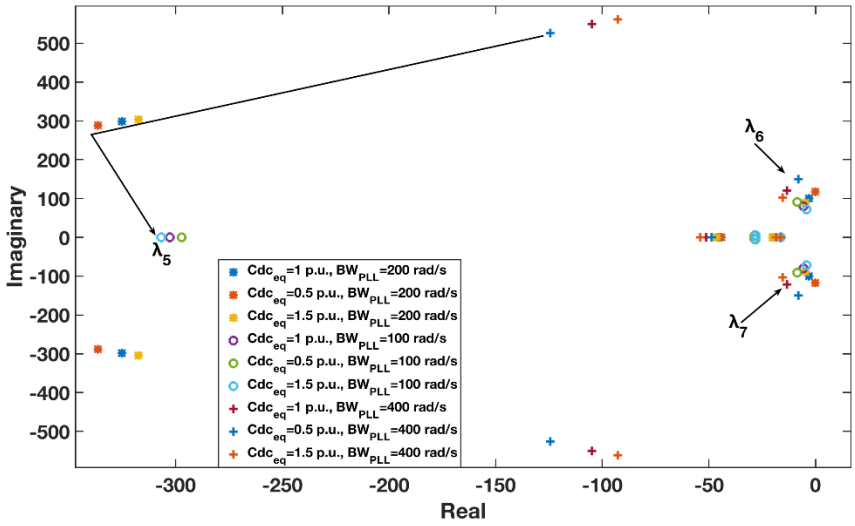
In Figs. 4.19 (a) and (b), it can be observed that system stability is highly affected by variations in DC-link capacitance and PLL bandwidth when the system becomes weaker (SCR decreasing from 1.5 to 1.11). From Fig. 4.19 (a), it can be seen that mode (λ_5) does not affect system stability as much as the dominant modes $\lambda_{6,7}$. The states responsible for controlling $\lambda_{6,7}$ are related to $\Delta\varphi_{ac}$ and $\Delta\theta_{pll}$ as shown in Table 4.7. Figure 4.19 (b) shows a lower-stability performance at BW_{PLL}= 200 rad/sec, in contrast to the greater stability at BW_{PLL}= 100 and 400 (rad/sec). These results agree with the analysis in [84], which studies the interactions between controllers' loops analytically on system stability. This work shows that, when the bandwidth of PLL approaches the bandwidth of the DC-link voltage controller, the system stability worsens. The plot used to demonstrate this situation in this reference can be found in Appendix A.4.2. This work also shows how the stability is enhanced when the PLL bandwidth is chosen to be faster or slower than the DC-link voltage controller bandwidth. Therefore, the worst-stability performance is observed at BW_{PLL}= 200 rad/sec due to its closeness to the bandwidth of the DC-link voltage controller. It can be noted from Fig. 4.19 (b) that system stability is enhanced by increasing the DC-link capacitance at BW_{PLL}= 200 and 400 rad/sec. Increasing the DC-link capacitance, therefore, can contribute to

enhancing the system stability if the PLL bandwidth is set close to that of the DC-link controller. Conversely, at BW_{PLL}= 100 rad/sec, increasing the DC-link capacitance leads to an eigenvalue shift toward the left half-plane, as is clear in Fig. 4.19 (b) (circles). A time-domain simulation clearly reflected these results as illustrated in Fig. 4.20.

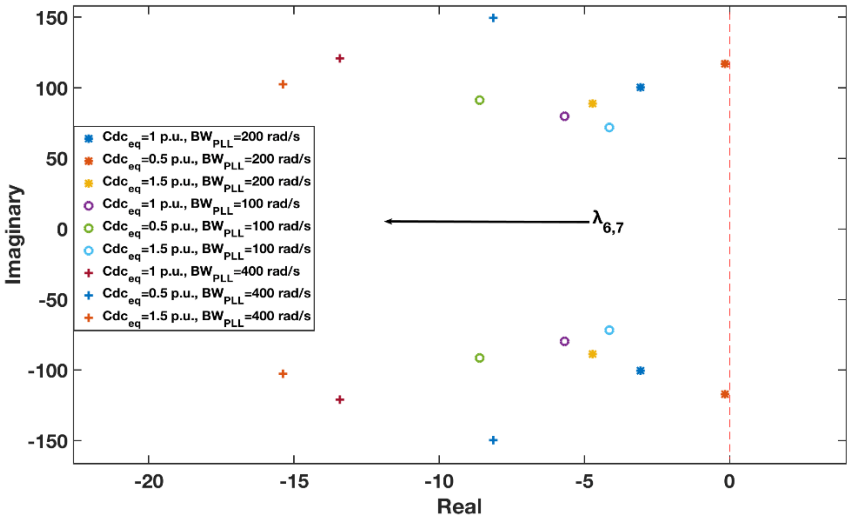
Table 4.6 Damping factors corresponding to $\boldsymbol{\lambda_{6,7}}$, present The effect of DC-link capacitance and SCR on SRF-PLL Bandwidth in inversion mode

***SCR*=1.5**			
$\boldsymbol{Cdc_{eq}\ (pu)\backslash\ BW_{pll}(rad/sec)}$	100	200	400
0.5	0.4077	0.3329	0.3854
1	0.3494	0.3210	0.3825
1.5	0.3118	0.3151	0.3813
	Damping Factor (ζ)		
***SCR*=1.11**			
$\boldsymbol{Cdc_{eq}\ (pu)\backslash\ BW_{pll}(rad/sec)}$	100	200	400
0.5	0.0938	0.0013	0.0543
1	0.0711	0.0304	0.1103
1.5	0.0575	0.0531	0.1482
	Damping Factor (ζ)		

Table 4.7 Participation factors corresponding to $\lambda_{6,7}$, present The effect of DC-link capacitance and SCR on SRF-PLL Bandwidth in inversion mode		
$\boldsymbol{SCR = 1.11, BW_{pll} = 200\ rad/sec}$		
DC-link capacitance value (PU)	Cdc_{eq}=0.5	Cdc_{eq}=1.5
Mode and Eigenvalue	$\lambda_{6,7}$= -0.16± 117.1i	$\lambda_{6,7}$= -4.72 ± 88.8i
Participation factors	$\Delta\varphi_{ac}$ =0.5, $\Delta\theta_{PLL}$ =0.31, ΔV_{dc}=0.18	$\Delta\varphi_{ac}$ =0.38, ΔV_{dc}=0.34, $\Delta\theta_{PLL}$=0.25, $\Delta\varphi_{dc}$=0.17
Dominant response mode	AC voltage controller	AC voltage controller
$\boldsymbol{SCR = 1.11, BW_{pll} = 100\ rad/sec}$		
DC-link capacitance value (PU)	Cdc_{eq}=0.5	Cdc_{eq}=1.5
Mode and Eigenvalue	$\lambda_{6,7}$= -8.6± 91.3i	$\lambda_{6,7}$= -4.1 ± 71.8i
Participation factors	$\Delta\varphi_{ac}$ = 0.47, $\Delta\theta_{PLL}$ =0.35, ΔV_{dc}=0.16	$\Delta\varphi_{ac}$ =0.33, ΔV_{dc}=0.3, $\Delta\theta_{PLL}$=0.3, $\Delta\varphi_{dc}$=0.2
Dominant response mode	AC voltage controller	AC voltage controller

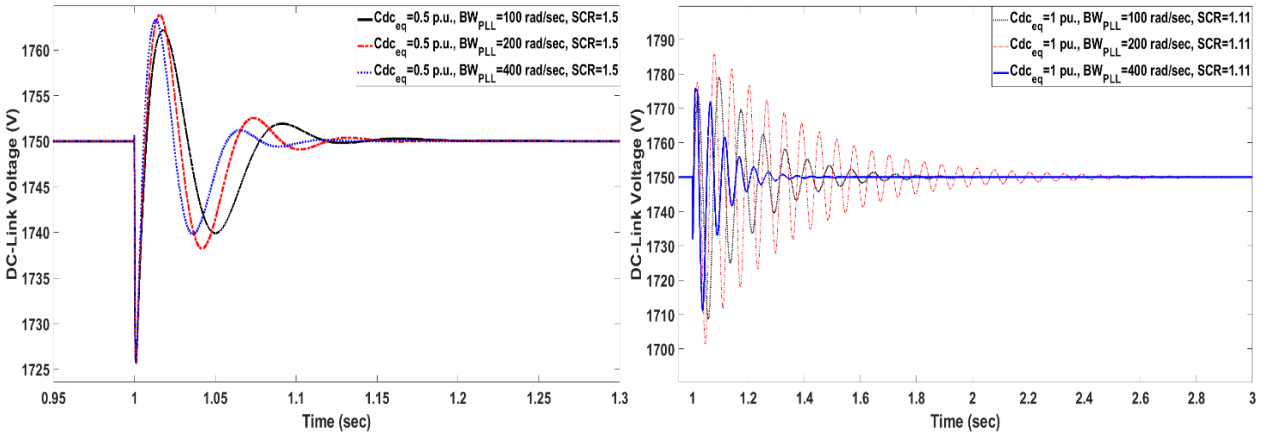


(a)



(b)

Figure 4.19 Root-locus of grid-connected VSC system. a) at $P_{dc} = 1\ pu$ and $SCR = 1.11$, b) Zoomed plot.



(a) (b)

Figure 4.20 Time-domain of grid-connected VSC system at $P_{dc} = 1\ pu$ and *SCR*: a) *SCR*=1.5, b) *SCR*=1.11

4.3.2.2 Rectification Mode

From Fig 4.21, at *SCR*=1.45, it can be noted that the effect of PLL bandwidth and DC-link capacitance variations on system stability is more severe than in inversion mode at case scenario of *SCR*=1.11. The case scenario at *SCR*=3 has almost the same result as when *SCR*=1.5 in inversion mode, in terms of stability condition. Hence, the root-locus plot of this case is omitted. Table 4.8 shows the damping factor of this case. In the rectification mode, system stability is significantly affected by BW_{PLL} and DC-link capacitance at a very weak-grid (*SCR*=1.45). From Fig 4.21, it is clear that mode (λ_7) is the dominant one that is greatly related to state $\Delta\varphi_{dc}$ as illustrated in Table 4.9. It is noteworthy that, in this mode, increasing BW_{PLL} and Cdc_{eq} destroys the system stability. At BW_{PLL} = 400 (rad/sec), for example, the stability is restored when decreasing the DC-link capacitance from 1 to 0.5 pu. The adverse effect of setting BW_{PLL} close to BW_{dc} does not appear in this mode as it does in inversion mode. Regarding the system stability condition, it can also be observed from the figure that the sensitivity of the DC-link capacitance increases as BW_{PLL} increases. For instance, at BW_{PLL} = 200 (rad/sec), the damping ratio (ζ) decreases from 0.24 to 0.062 when Cdc_{eq} increases from 0.5 to 1 pu., respectively; whereas the stability is lost when Cdc_{eq} increases from 1 to 0.5 pu at BW_{PLL} = 400 (rad/sec) as verified by the time-domain simulation in Fig.4.22.

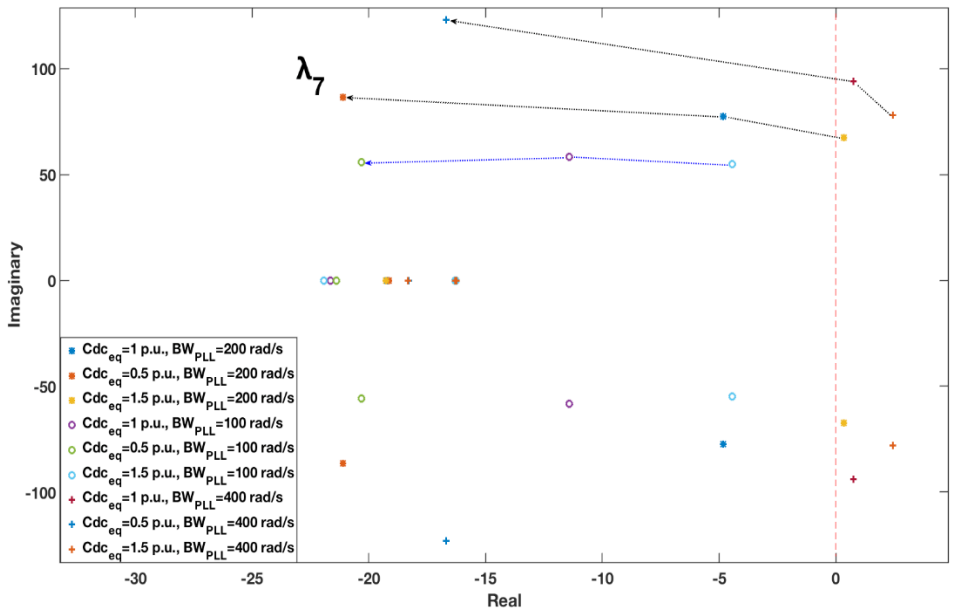


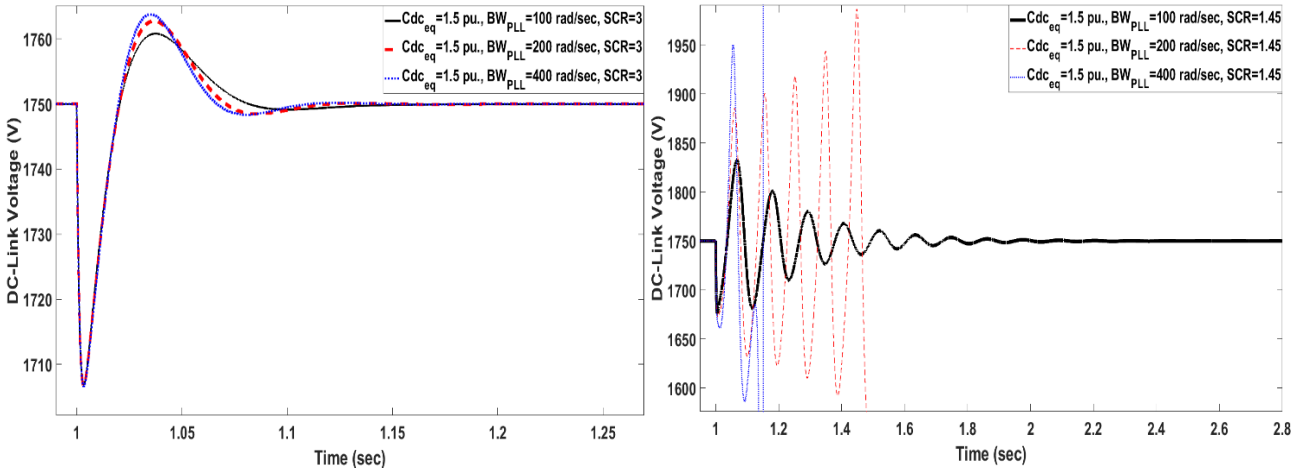
Figure 4.21 Root-locus of grid-connected VSC system at $P_{dc} = -1\ pu$ and *SCR*=1.45

Table 4.8 Damping factors corresponding to $\boldsymbol{\lambda_7}$, present the effect of DC-link capacitance and SCR on SRF-PLL bandwidth in rectification mode

***SCR*=3**			
$\boldsymbol{Cdc_{eq}\ (pu)\backslash\ BW_{pll}(rad/sec)}$	100	200	400
0.5	0.8068	0.8802	0.9518
1	0.8034	0.7719	0.7488
1.5	0.6539	0.5407	0.5337
	Damping Factor (ζ)		
***SCR*=1.45**			
$\boldsymbol{Cdc_{eq}\ (pu)\backslash\ BW_{pll}(rad/sec)}$	100	200	400
0.5	0.3416	0.2371	0.1345
1	0.1923	0.0621	Unstable
1.5	0.0805	Unstable	Unstable
	Damping Factor (ζ)		

Table 4.9 Participation factors corresponding to $\lambda_{6,7}$, present The effect of DC-link capacitance and SCR on SRF-PLL bandwidth in rectification mode

***SCR* =1.45 , $\mathbf{BW_{pll}}$ = 200 rad/sec**		
DC-link capacitance value (PU)	Cdc_{eq}=0.5	Cdc_{eq}=1.5
Mode and Eigenvalue	$\lambda_{6,7}$= -21.1± 86.4i	$\lambda_{7,8}$= 0.338± 67.4i
Participation factors	$\Delta\varphi_{ac}$ = 0.47, $\Delta\theta_{PLL}$ = 0.46, $\Delta\varphi_{dc}$=0.43	$\Delta\varphi_{dc}$ = 0.43, ΔV_{dc}=0.39, $\Delta\varphi_{ac}$=0.3, $\Delta\theta_{PLL}$=0.22
Dominant response mode	AC voltage controller	DC-link voltage controller
***SCR* =1.45 , $\boldsymbol{Cdc_{eq}}$=1 pu**		
Bandwidth of PLL in (rad/sec)	BW_{pll}=200	BW_{pll}=400
Mode and Eigenvalue	$\lambda_{6,7}$= -4.83± 77.5i	$\lambda_{6,7}$= 0.73 ± 94i
Participation factors	$\Delta\varphi_{dc}$ = 0.45,, ΔV_{dc}=0.38, $\Delta\varphi_{ac}$=0.36 , $\Delta\theta_{PLL}$=0.3	$\Delta\varphi_{dc}$ = 0.47,, ΔV_{dc}=0.46, $\Delta\varphi_{ac}$=0.42 , $\Delta\theta_{PLL}$=0.16
Dominant response mode	DC-link voltage controller	DC-link voltage controller



(a) (b)

Figure 4.22 Time-domain of grid-connected VSC system at $P_{dc} = -1\ pu$ and *SCR*: a) *SCR*=3, b) *SCR*=1.45

4.3.3 Effect of DC-link Capacitance and SCR on AC Voltage Controller

4.3.3.1 Inversion Mode

Figures 4.23 and 4.24 show system stability through eigenvalues when the DC-link capacitance and AC voltage controller bandwidth are subjected to change under weak grid conditions. At *SCR*=1.5 in Fig 4.23, it is clear that increasing the bandwidth of the AC voltage controller drives the eigenvalues to the left half-plan through modes ($\lambda_{6,7}$), which enhances stability. Changing BW_{ac} from 100 to 400 rad/sec leads to increase the damping ratio by approximately more than 50% as shown in Table 4.10. Conversely, changing the DC-link capacitance from 0.5 to 1.5 pu at each bandwidth setting does not greatly affect the system stability and the effect of DC-link capacitance becomes higher at lower BW_{ac}. As shown in Table 4.10, when Cdc_{eq} changes from 1.5 to 0.5 pu at BW_{ac} values of 100, 200, and 400 rad/sec, the damping ratio increases by around 17%, 6%, and 2.5%, respectively. In Fig 4.24, system stability is highly affected by changes Cdc_{eq} and BW_{ac} at *SCR*=1.11.

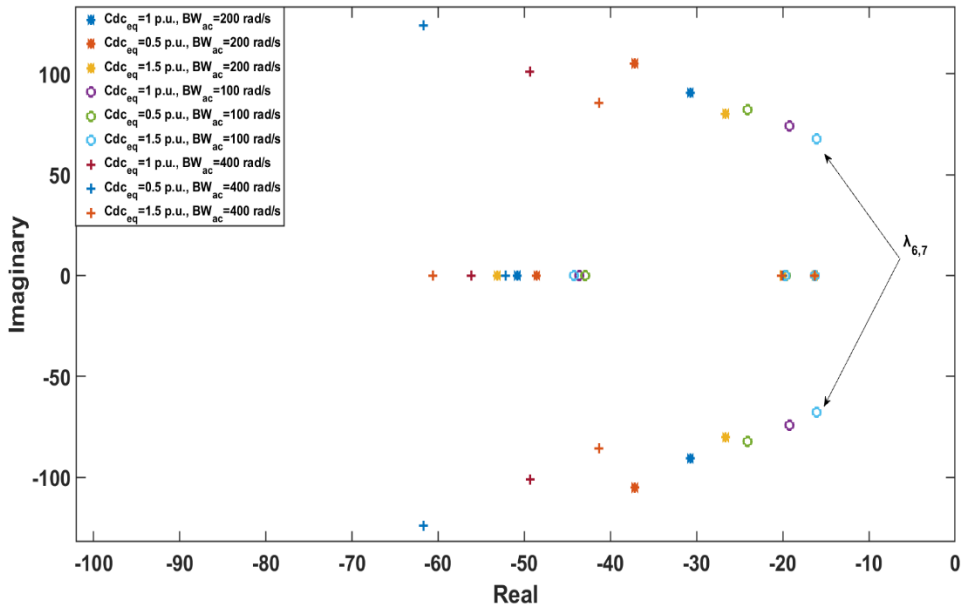


Figure 4.23 Root-locus of grid-connected VSC system at $P_{dc} = 1\ pu$ and *SCR*=1.5

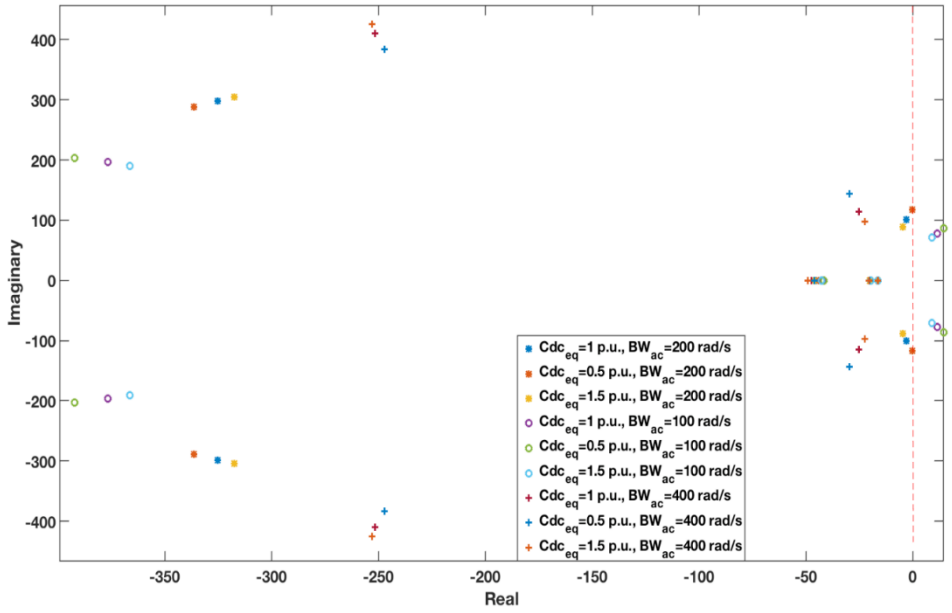


Figure 4.24 Root-locus of grid-connected VSC system at $P_{dc} = 1\ pu$ and $SCR = 1.11$

As shown in Fig 4.23, decreasing BW_{ac} degrades the system stability. However, it is expected that the system could enter the unstable region at a lower BW_{ac} when the SCR reduces to 1.11. As is clear from the Fig 4.24, at BW_{ac} 100 rad/sec (circles) the system is unstable, and almost marginally stable at BW_{ac} 200 rad/sec (stars). In this case, the state $\Delta\varphi_{ac}$ is the most influencing state that affect the stability of the system as shown in the participation factor analysis in Table 4.11. Increasing BW_{ac} can contribute strongly to enhancing system stability against very low SCR and

uncertainty in the DC-link capacitance. As illustrated in Fig 4.10 (a), increasing Cdc_{eq} at very low SCR enhances system stability; this stability behaviour is also reflected when BW_{ac} = 100 and 200 rad/sec as shown in Fig 4.24. These results were verified with the time-domain simulation as shown in Fig. 4.25.

Table 4.10 Damping factors corresponding to $\boldsymbol{\lambda_{6,7}}$, present the effect of DC-link capacitance and SCR on AC Voltage Controller in inversion mode

***SCR*=1.5**			
$\boldsymbol{Cdc_{eq}\ (pu)\backslash\ BW_{ac}(rad/sec)}$	100	200	400
0.5	0.2811	0.3329	0.4453
1	0.2506	0.3210	0.4385
1.5	0.2310	0.3151	0.4341
	Damping Factor (ζ)		
***SCR*=1.11**			
$\boldsymbol{Cdc_{eq}\ (pu)\backslash\ BW_{ac}(rad/sec)}$	100	200	400
0.5	Unstable	0.0013	0.2031
1	Unstable	0.0304	0.2154
1.5	Unstable	0.0531	0.2245
	Damping Factor (ζ)		

Table 4.11 Participation factors corresponding to $\lambda_{6,7}$, present the effect of DC-link capacitance and SCR on AC Voltage Controller in inversion mode

***SCR*=1.11, $\boldsymbol{Cdc_{eq}}$=0.5 pu**		
Bandwidth of AC-voltage control in (rad/sec)	BW_{pll}=200	BW_{pll}=400
Mode and Eigenvalue	$\lambda_{6,7}$= -0.16± 117.1i	$\lambda_{6,7}$= -29.8 ± 143i
Participation factors	$\Delta\varphi_{ac} = 0.5,\ \Delta\theta_{PLL} = 0.31, \Delta V_{dc}$=0.18	$\Delta\varphi_{ac} = 0.52,, \Delta\theta_{PLL}$=0.35 , ΔV_{dc}=0.27
Dominant response mode	AC voltage controller	AC voltage controller

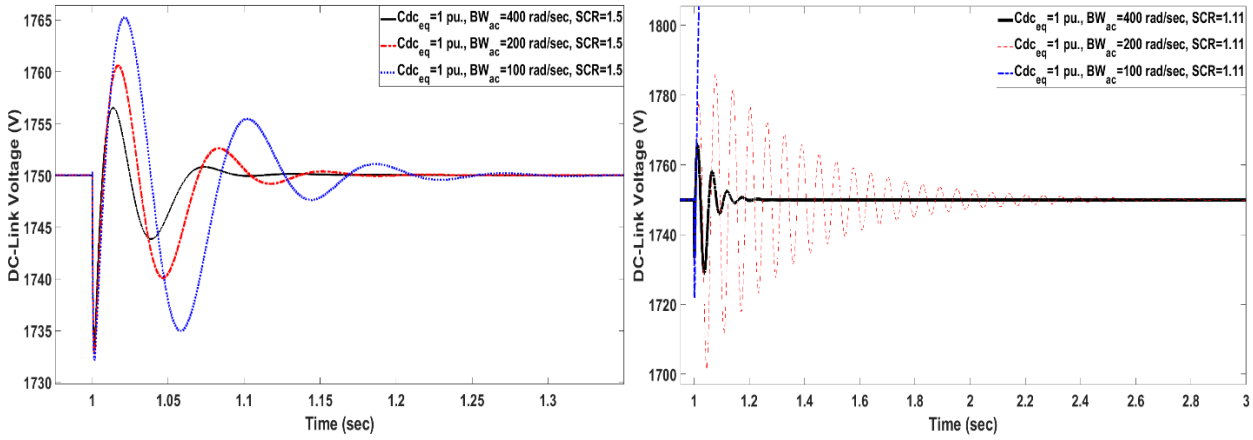


Figure 4.25 Time-domain of grid-connected VSC system at $P_{dc} = 1\ pu$ and *SCR*: a) *SCR*=1.5, b) *SCR*=1.11

4.3.3.2 Rectification Mode

Increasing the AC voltage controller bandwidth in rectification mode degrades the system stability as shown in Fig 4.26. Further, at *SCR*=3 decreasing BW_{ac} from 400 to 200 rad/sec enhances the system stability by approximately 14%, which does not greatly influence system stability. Decreasing Cdc_{eq} from 1.5 to 0.5 pu upgrades system stability by around 62% over all ranges of BW_{ac}. Because it is difficult to see the effects of Cdc_{eq} and BW_{ac} from the eigenvalues in Fig 4.26, the damping factor is given in Table 4.12.

Table 4.12 Damping factors corresponding to $\boldsymbol{\lambda_{7,8}}$, the effect of DC-link capacitance and SCR on AC Voltage Controller in rectification mode

***SCR*=3**			
$\boldsymbol{Cdc_{eq}\ (pu)\backslash\ BW_{ac}(rad/sec)}$	100	200	400
0.5	0.9779	0.8802	0.8571
1	0.8831	0.7719	0.6919
1.5	0.6018	0.5407	0.5207
	Damping Factor (ζ)		
***SCR*=1.45**			
$\boldsymbol{Cdc_{eq}\ (pu)\backslash\ BW_{ac}(rad/sec)}$	100	200	400
0.5	0.1016	0.2371	0.39882
1	Unstable	0.0621	0.16314
1.5	Unstable	Unstable	0.083465
	Damping Factor (ζ)		

When the grid becomes very weak, both DC-link capacitance and AC voltage controller bandwidth strongly influence system stability. At *SCR*=3 in Fig 4.26, decreasing BW_{ac} brings about better stability over all values of Cdc_{eq}. Conversely, at *SCR*=1.45, decreasing BW_{ac} brings system stability to a worse condition as shown in Fig 4.27. Moreover, it can be surmised from this figure that the Cdc_{eq} can contribute greatly to stabilizing the system. From Fig 4.27, it can be observed that the best stability performance can be achieved at Cdc_{eq}=0.5 pu over all bandwidths. Whereas the worst the stability performance at BW_{ac} = 100 rad/sec. At *SCR*= 1.45 and BW_{ac} = 100 rad/sec, the system stability is highly affected by the states $\Delta\varphi_{ac}$ and $\Delta\varphi_{dc}$ as clear in Table 4.13. In Table 4.12, the damping factor illustrates the effect of Cdc_{eq} and BW_{ac}. Increasing BW_{ac} from 100 to 400 rad/sec and decreasing Cdc_{eq} from 1.5 to 0.5 pu increases the damping ratio by more than 100%. The presented analytical results have been verified with the time-domain simulation shows in Fig. 4.28.

Table 4.13 Participation factors corresponding to $\lambda_{7,8}$, present The effect of DC-link capacitance and SCR on AC Voltage Controller in rectification mode

SCR*=1.45, BW_{pll} = 100 *rad/sec		
DC-link capacitance value (PU)	Cdc_{eq}=0.5	Cdc_{eq}=1
Mode and Eigenvalue	$\lambda_{7,8}$= -6.7± 86.4i	$\lambda_{7,8}$= 1.37± 60.17i
Participation factors	$\Delta\varphi_{ac}$ = 0.47, $\Delta\varphi_{dc}$=0.4 $\Delta\theta_{PLL}$ = 0.33,	$\Delta\varphi_{dc}$ = 0.42, $\Delta\varphi_{ac}$=0.4 ΔV_{dc}=0.3, $\Delta\theta_{PLL}$=0.24
Dominant response mode	AC voltage controller	DC-link voltage controller

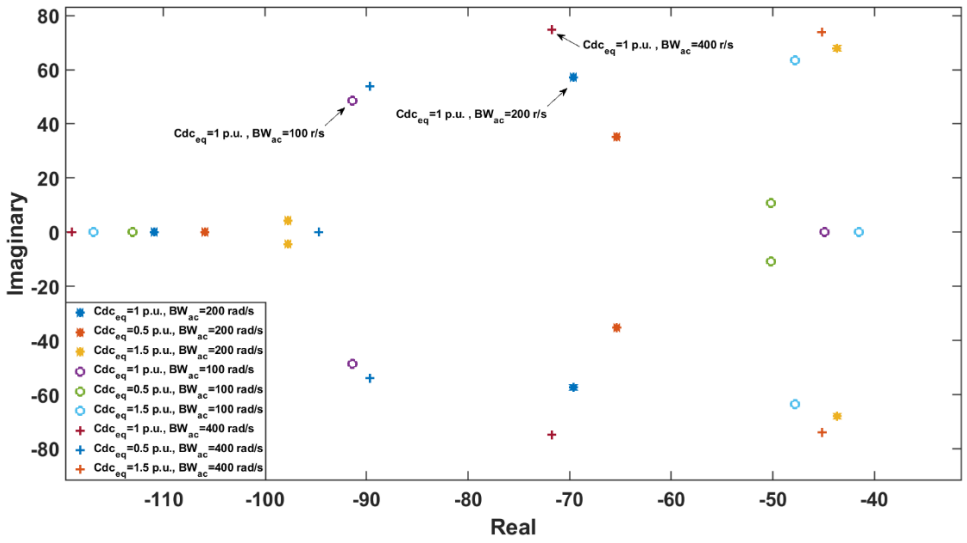


Figure 4.26 Root-locus of the grid-connected VSC system at $P_{dc} = -1\ pu$ and $SCR = 3$

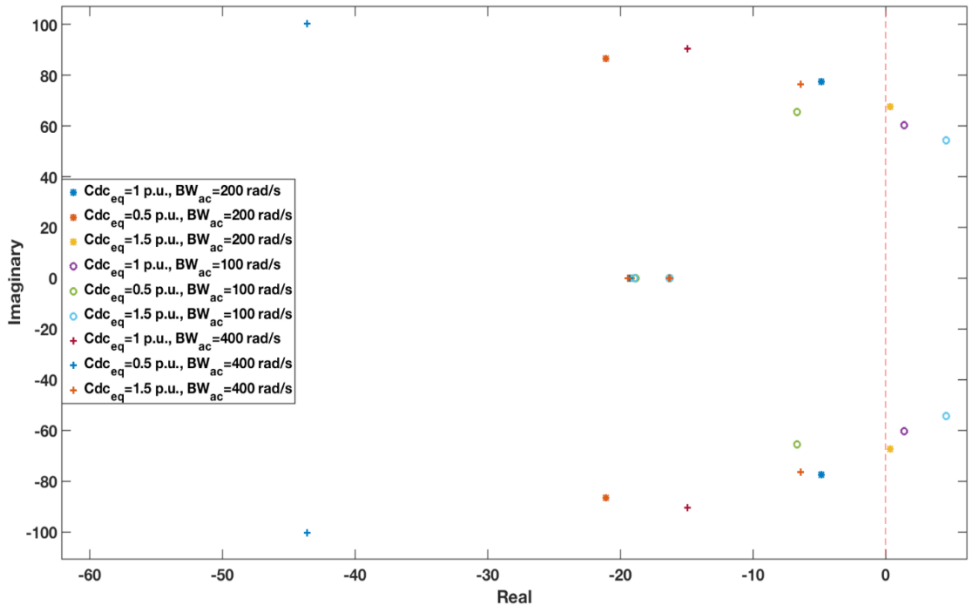


Figure 4.27 Root-locus of the grid-connected VSC system at $P_{dc} = -1\ pu$ and *SCR*=1.45

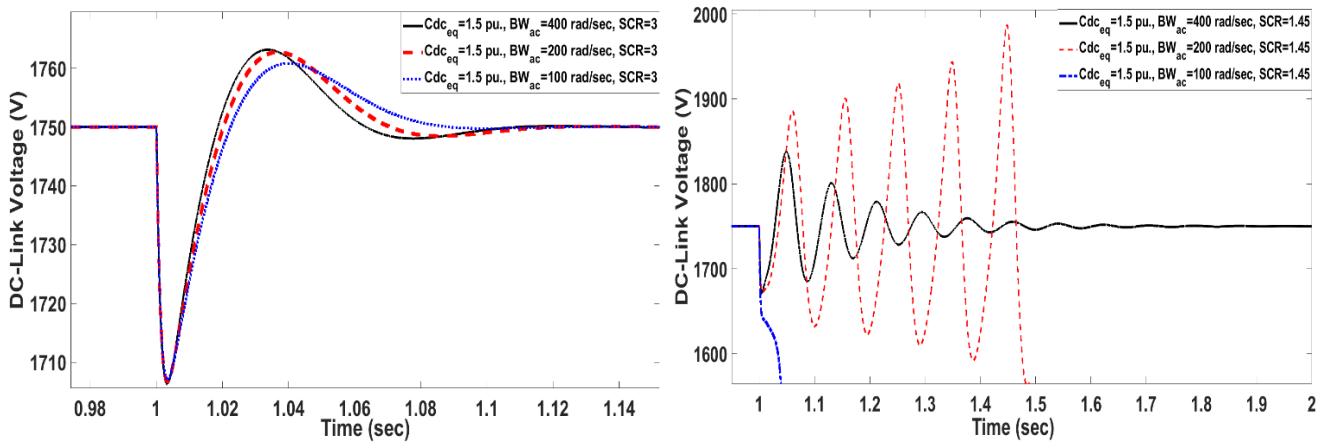


Figure 4.28 Time-domain of grid-connected VSC system at $P_{dc} = -1\ pu$ and *SCR*: a) *SCR*=3, b) *SCR*=1.45

4.3.4 Analysis Results Summary of The Impact of DC-Link Capacitance Uncertainty on Different Controllers' Bandwidth

Table 4.14 Stability performance of the system can be concluded as following:

			Stability	
BW and Cdc_{eq} situation	BW and Cdc_{eq}\ Mode		Inversion (*SCR*=1.11)	Rectification (*SCR*=1.45)
INCREASING	Cdc_{eq}	DC-link controller	Enhanced	Degraded
		PLL controller	Enhanced	Degraded
		AC controller	Enhanced	Degraded
	BW_{dc}	DC-link controller	Enhanced	Degraded
	BW_{PLL} [1]	PLL controller	Enhanced	Degraded
	BW_{ac}	AC controller	Enhanced	Enhanced

[1] *Except at very low BW_{PLL} (i.e. 100 rad/s) this effect is reversed*

4.4 The Effect of DC-link Capacitance Uncertainty on Grid-Angle Variations

In this section, the effect of the DC-link capacitance uncertainty with grid impedance angle variations is addressed at different SCR levels. The grid angle varies by varying the *X*/*R* ratio. At the nominal condition, *X*/*R* = 10, the grid angle (θ_g) is 83°. In this analysis, however, the grid angle changed from 79° to 87°. In the inversion and rectification modes, at *SCR* = 3, the effect of the DC-link capacitance uncertainty slightly affects the dynamic stability of the system when the grid angle increases or decreases, as illustrated in Figs. 4.29 and 4.32.

In inversion mode, the worst damping factor, ζ= 0.0079, is reported at θ_g=87°(*X*/*R* = 20) and Cdc_{eq} = 0.5 pu, as listed in Table 4.15. Figure 4.30 presents two different modes affected by varying the grid angle and DC-link capacitance, which are $\lambda_{4,5}$ and $\lambda_{6,7}$. Because modes $\lambda_{6,7}$ are closer to the origin, they most likely consider dominant modes. Table 4.16 indicates that these modes are highly influenced by the state of the AC-voltage controller ($\Delta\varphi_{ac}$) and PLL angle ($\Delta\theta_{pll}$). These results were verified by the time-domain simulation as demonstrated in Fig. 4.31.

Table 4.15 Damping factors corresponding to $\boldsymbol{\lambda_{6,7}}$, present the effect of DC-link capacitance and grid angle variations in inversion mode

***SCR*=3**			
$\boldsymbol{Cdc_{eq}}$ **(*pu.*)\ $\boldsymbol{\theta_g^{\circ}}$**	79°	83°	87°
0.5	$0.75026\boldsymbol{\lambda}_{6,7}$	$0.74289\boldsymbol{\lambda}_{6,7}$	$0.7409\boldsymbol{\lambda}_{6,7}$
1	$0.66508\boldsymbol{\lambda}_{6,7}$	$0.64957\boldsymbol{\lambda}_{6,7}$	$0.64306\boldsymbol{\lambda}_{6,7}$
1.5	$0.60072\boldsymbol{\lambda}_{6,7}$	$0.58281\boldsymbol{\lambda}_{6,7}$	$0.57495\boldsymbol{\lambda}_{6,7}$
	Damping Factor (ζ)		
***SCR*=1.15**			
$\boldsymbol{Cdc_{eq}}$ **(*pu.*)\ $\boldsymbol{\theta_g^{\circ}}$**	79°	83°	87°
0.5	$0.10869\boldsymbol{\lambda}_{6,7}$ $0.80828\boldsymbol{\lambda}_{4,5}$	$0.042146\boldsymbol{\lambda}_{6,7}$ $0.77226\boldsymbol{\lambda}_{4,5}$	$0.00799\boldsymbol{\lambda}_{6,7}$ $0.74969\boldsymbol{\lambda}_{4,5}$
1	$0.136\boldsymbol{\lambda}_{6,7}$ $0.78813\ \boldsymbol{\lambda}_{4,5}$	$0.06652\boldsymbol{\lambda}_{6,7}$ $0.75174\boldsymbol{\lambda}_{4,5}$	$0.031198\boldsymbol{\lambda}_{6,7}$ $0.73034\boldsymbol{\lambda}_{4,5}$
1.5	$0.15266\boldsymbol{\lambda}_{6,7}$ $0.77812\boldsymbol{\lambda}_{4,5}$	$0.080925\boldsymbol{\lambda}_{6,7}$ $0.74165\boldsymbol{\lambda}_{4,5}$	$0.044517\boldsymbol{\lambda}_{6,7}$ $0.72084\boldsymbol{\lambda}_{4,5}$
	Damping Factor (ζ)		

Table 4.16 Participation factors corresponding to $\lambda_{6,7}$ and $\lambda_{4,5}$, present the effect of DC-link capacitance and grid angle variations in inversion mode

***SCR*=3,** X/R=20 (θ_g=87°)		
DC-link capacitance value (PU)	Cdc_{eq}=1.5	
Mode and Eigenvalue	$\lambda_{6,7}$= -42.9± 61i	
Participation factors	ΔV_{dc}=0.41, $\Delta\varphi_{dc}$ = 0.4	
Dominant response mode	DC-ink voltage	
	DC-ink voltage controller	
***SCR*=1.15,** X/R=20 (θ_g=87°)		
DC-link capacitance value (PU)	Cdc_{eq}=0.5	
Mode and Eigenvalue	$\lambda_{6,7}$= -1 ± 116i	$\lambda_{4,5}$= -326 ± 288i
Participation factors	$\Delta\varphi_{ac}$ = 0.47, $\Delta\theta_{pll}$=0.3	$\Delta\theta_{pll}$=0.7, Δi_{g_q}=0.6
Dominant response mode	AC- voltage controller	PLL angle
	PLL angle	Grid current (q-component)

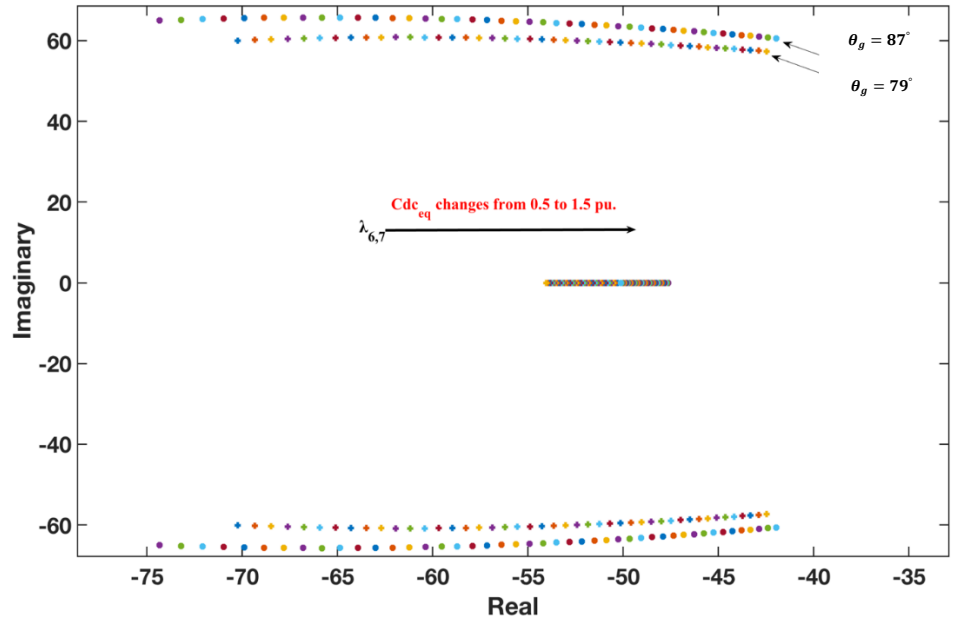
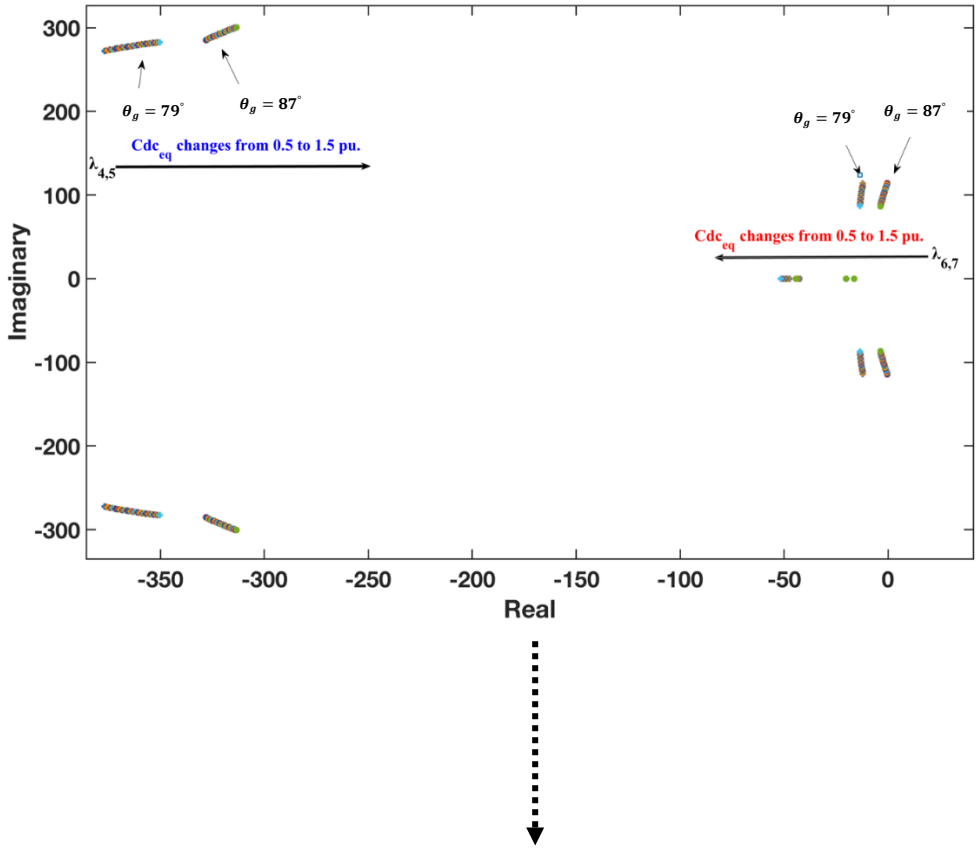
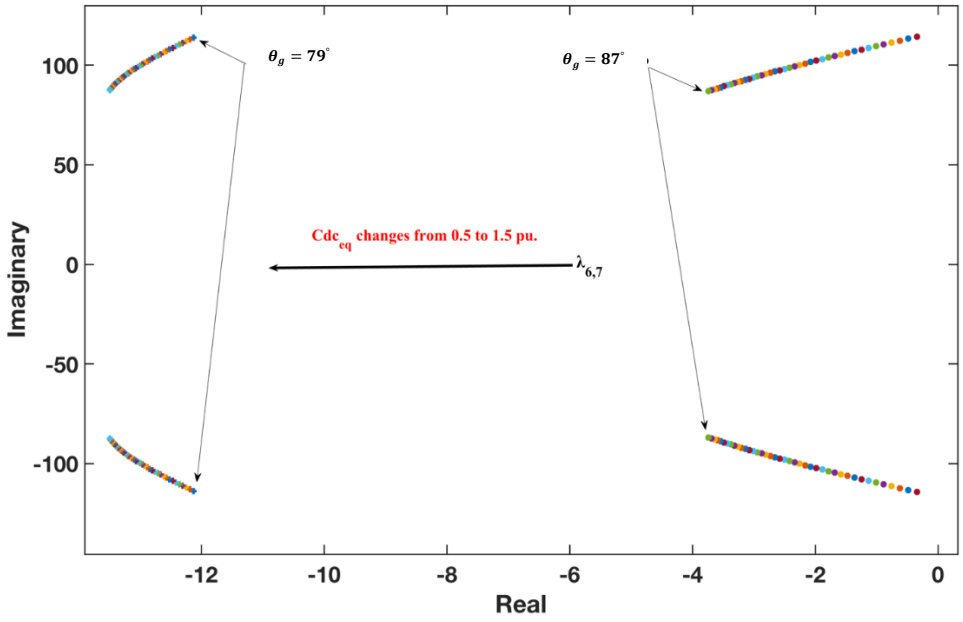


Figure 4.29 Root-locus of the grid-connected VSC system at $P_{dc} = 1\ pu$, *SCR*=3 and θ_g varies from 79° to 87°.





(Zoom in modes $\lambda_{6,7}$)

Figure 4.30 Root-locus of the grid-connected VSC system at $P_{dc} = 1\ pu$, *SCR*=1.15 and θ_g varies from 79° to 87°.

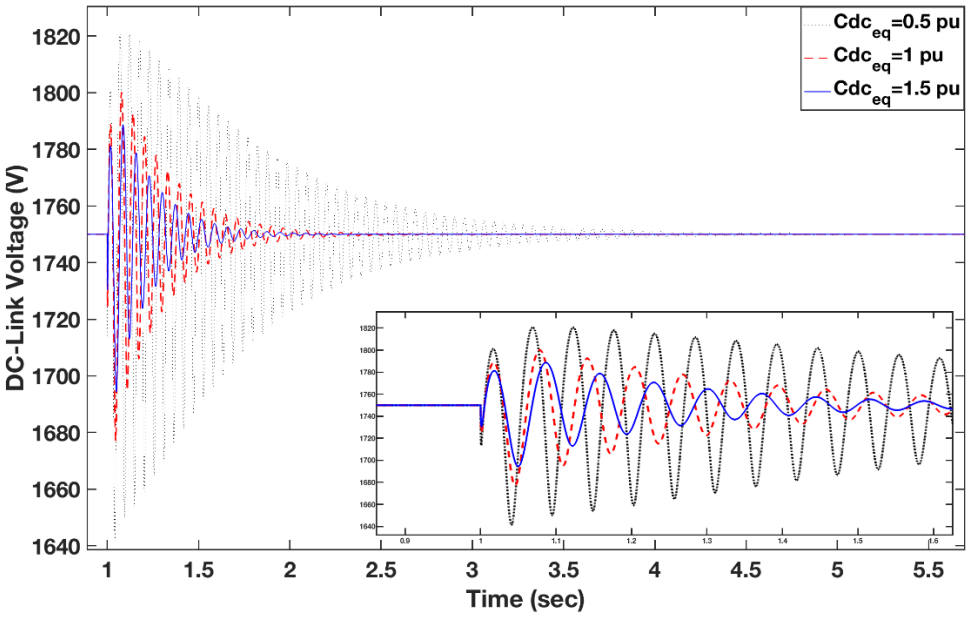


Figure 4.31 Time-domain of grid-connected VSC system at $P_{dc} = 1\ pu$, *SCR*=1.15 and θ_g= 87° (*X*/*R*=20).

In rectification mode, when SCR decreases from 3 to 1.7, the system stability is highly affected by the grid angle and DC-link capacitance variations. Table 4.17 and Fig. 4.33 reveal that decreasing the grid angle and increasing the DC-link capacitance lead to the worst stability condition. From Table 4.17, the damping factor decreases from 0.3338 to 0.0287 when Cdc_{eq}

varies from 0.5 to 1.5 pu. Modes $\lambda_{7,8}$ are the dominant modes that drive the poles toward the right-hand side when the DC-link capacitance increases, as illustrated in Fig. 4.33. The influencing state of modes $\lambda_{7,8}$ are highly related to the DC-link voltage controller state ($\Delta\varphi_{dc}$) as listed in Table 4.18. This finding has been confirmed by the time-domain simulation in Fig. 4.34.

Table 4.17 Damping factors corresponding to $\boldsymbol{\lambda_{5,6}}$ and $\boldsymbol{\lambda_{7,8}}$, present the effect of DC-link capacitance and grid angle variations in rectification mode at *SCR*=3 and *SCR*=1.7, respectively.

***SCR*=3**			
$\boldsymbol{Cdc_{eq}}$ **(pu.)\ $\boldsymbol{\theta_g^\circ}$**	79°	83°	87°
0.5	0.8694	0.88018	0.88383
1	0.71581	0.77196	0.79043
1.5	0.48959	0.54065	0.56377
	Damping Factor (ζ)		
***SCR*=1.7**			
$\boldsymbol{Cdc_{eq}}$ **(pu.)\ $\boldsymbol{\theta_g^\circ}$**	79°	83°	87°
0.5	0.3338	0.29014	0.28956
1	0.1156	0.32035	0.38289
1.5	0.0287	0.21339	0.27227
	Damping Factor (ζ)		

Table 4.18 Participation factors corresponding to $\lambda_{7,8}$, present the effect of DC-link capacitance and grid angle variations in rectification mode	
***SCR*=1.7,** *X/R*=20 (θ_g=87°)	
DC-link capacitance value (PU)	Cdc_{eq}=1.5
Mode and Eigenvalue	$\lambda_{7,8}$= -20.391 ± 72.064i
Participation factors	ΔV_{dc}=0.46, $\Delta\varphi_{dc}$ = 0.45
Dominant response mode	DC-ink voltage
	DC-ink voltage controller
***SCR*=1.7,** *X/R*=5 (θ_g = 79°)	
DC-link capacitance value (PU)	Cdc_{eq}=1.5
Mode and Eigenvalue	$\lambda_{7,8}$= -1.97 ± 68.5i
Participation factors	$\Delta\varphi_{dc}$ =0.48, ΔV_{dc}=0.41
Dominant response mode	DC-ink voltage controller
	DC-ink voltage

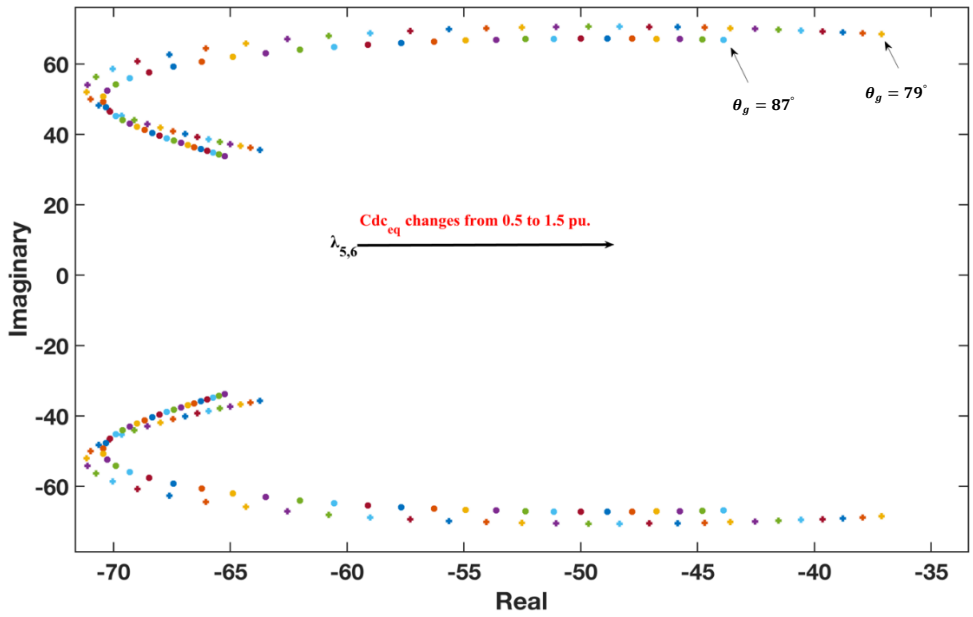
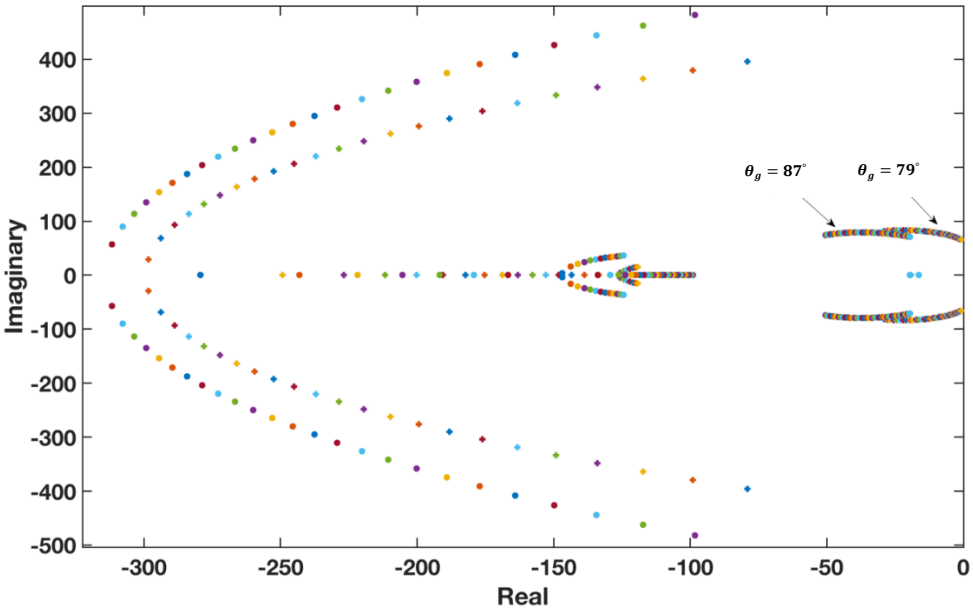
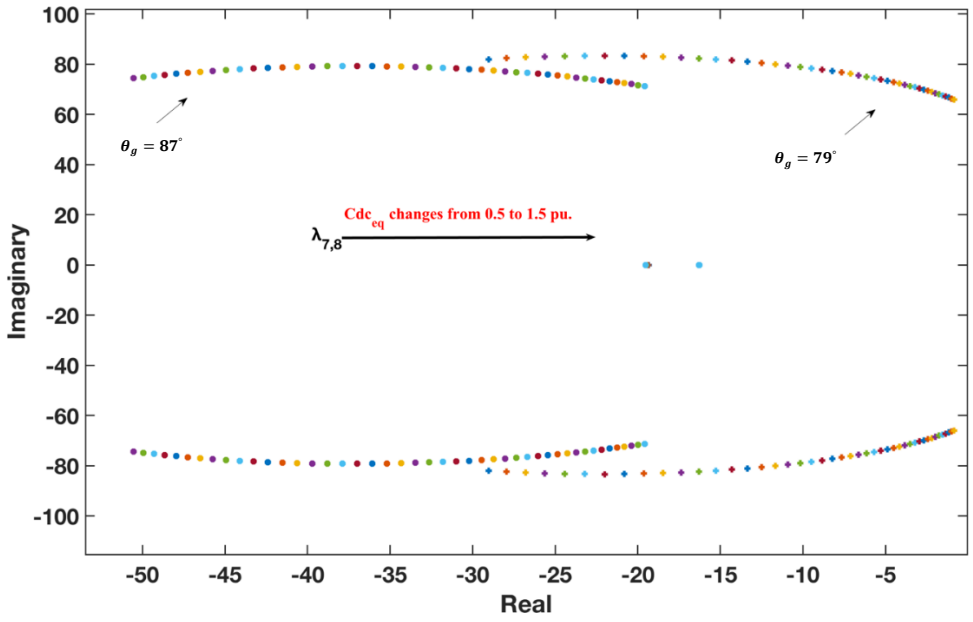


Figure 4.32 Root-locus of the grid-connected VSC system at $P_{dc} = -1\ pu$, SCR=3 and θ_g varies from 79° to 87°.



(a)



(Zoom in modes $\lambda_{7,8}$)

Figure 4.33 Root-locus of the grid-connected VSC system at $P_{dc} = -1\ pu$, *SCR*=1.7 and θ_g varies from 79° to 87°.

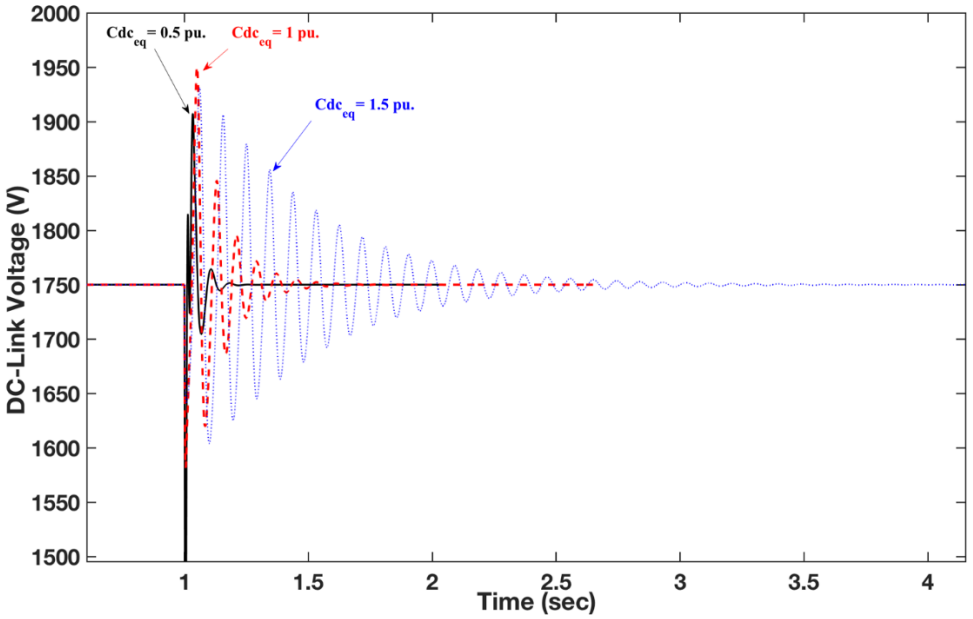


Figure 4.34 Time-domain of grid-connected VSC system at $P_{dc} = -1\ pu$, *SCR*=1.7 and θ_g= 79° (*X/R*=5).

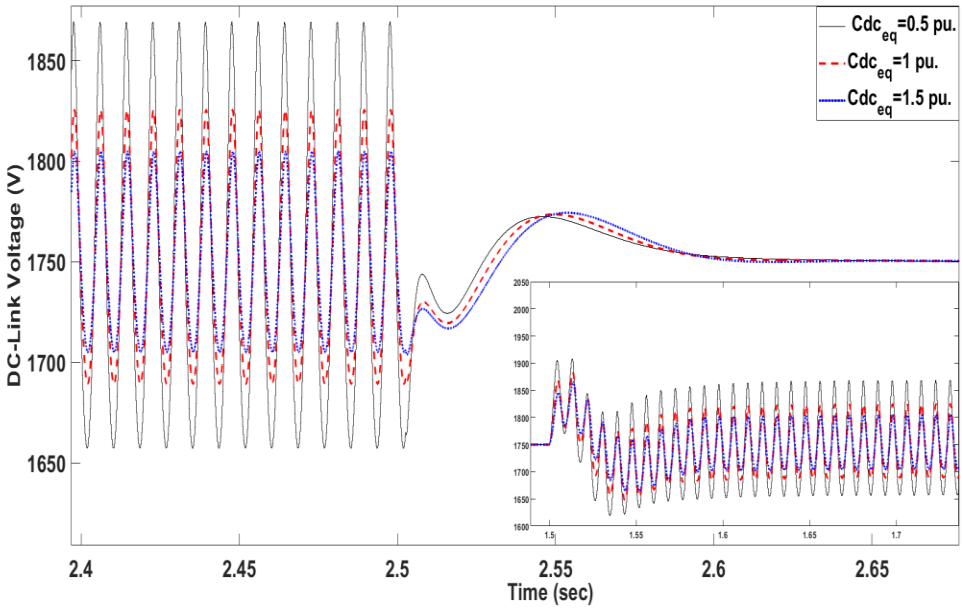
4.5 Fault analysis

4.5.1 Fault Assessment of the Interactions between DC-link Capacitance Uncertainty and SCR

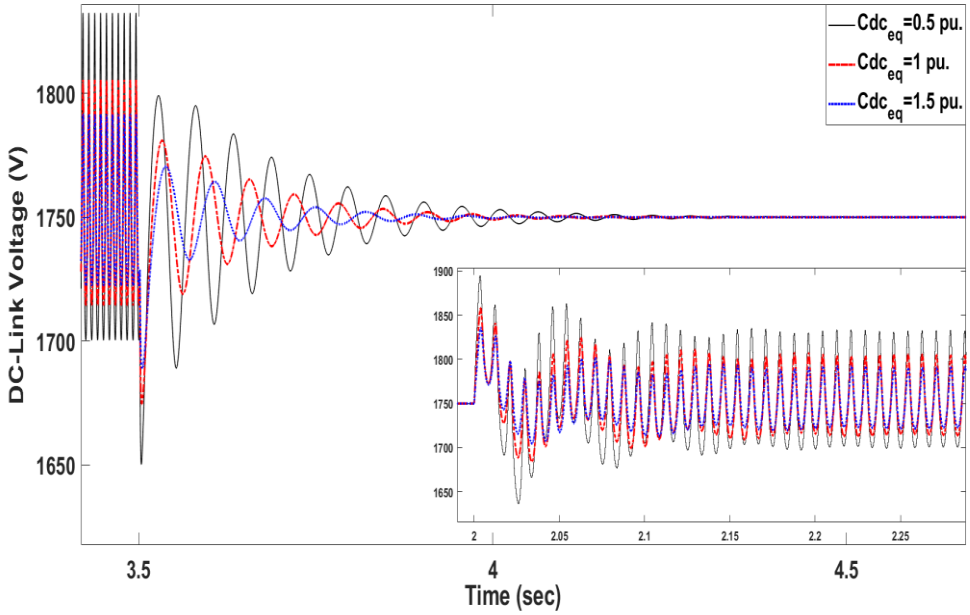
The performance of the grid-connected VSC system is examined under fault conditions that could occur in the AC-sides at PCC. Several case scenarios have been conducted to assess the effect of the DC-link capacitance uncertainty along with the weak grid on the system dynamics under faulty conditions. Only significant results are presented in this section. Figures 4.35 and 4.36 illustrate the DC-link voltage response to a single line-to-ground (L-G) fault on the AC-side in inversion and rectification modes, respectively. In Fig. 4.35 (a) and (b), the fault starts at time t = 1.5 and 2 s and clears at t = 2.5 and 3.5 s, respectively. In Fig. 4.35(a), during the fault, the magnitude of the DC-link voltage changes by approximately 3% when the DC-link capacitance varies from 1.5 to 0.5 pu and returns to the steady-state value, 1750 V, after the fault is cleared in 0.125 s. The effect of the DC-link capacitance uncertainty, however, is minimum in this case. However, at *SCR* = 1.15, the effect of the DC-link capacitance uncertainty is clearly noted when the fault is cleared, as illustrated in Fig. 4.35(b). Decreasing the DC-link capacitance leads to increase the magnitude during the fault and increase the oscillations and settling time after clearing the fault of the DC-link voltage.

In rectification mode, the magnitude of the DC-link voltage significantly increases during the fault compared with the inversion mode when the DC-link capacitance decreases, as depicted in Fig. 4.36. In Fig. 4.36(a), the magnitude of the DC-link voltage increased by almost 16% when the DC-link capacitance changed from 1.5 to 0.5 pu through the duration of the fault. In this case, the settling time after the fault clears slightly improves when the value of the DC-link capacitance decreases. In Fig. 4.36 (b), when the SCR decreases from 3 to 2.5, the effect of the DC-link capacitance uncertainty is tangible. At t = 2 s, the system cannot override the fault at Cdc_{eq} = 1 and 1.5 pu. Reducing the DC-link capacitance to 0.5 pu allows the system to withstand the fault without significantly increasing the settling time after clearing the fault, as in the case of the inversion mode. The oscillations in the DC-link voltage contain a second harmonic ripple at the double of the AC-grid frequency (120 Hz). The reason for the second harmonic is the condition of unbalanced power transfer between both sides, AC and DC, at the time of the fault occurs. In both

cases, the system succeeds in recovering to its normal stable operation after the fault is cleared, which maintains the fault ride-through characteristic.

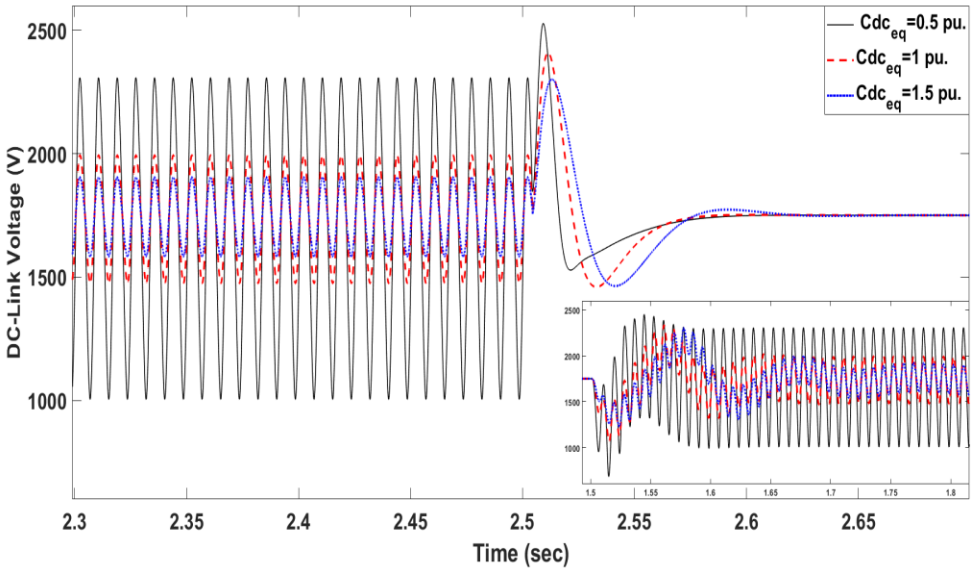


(a)

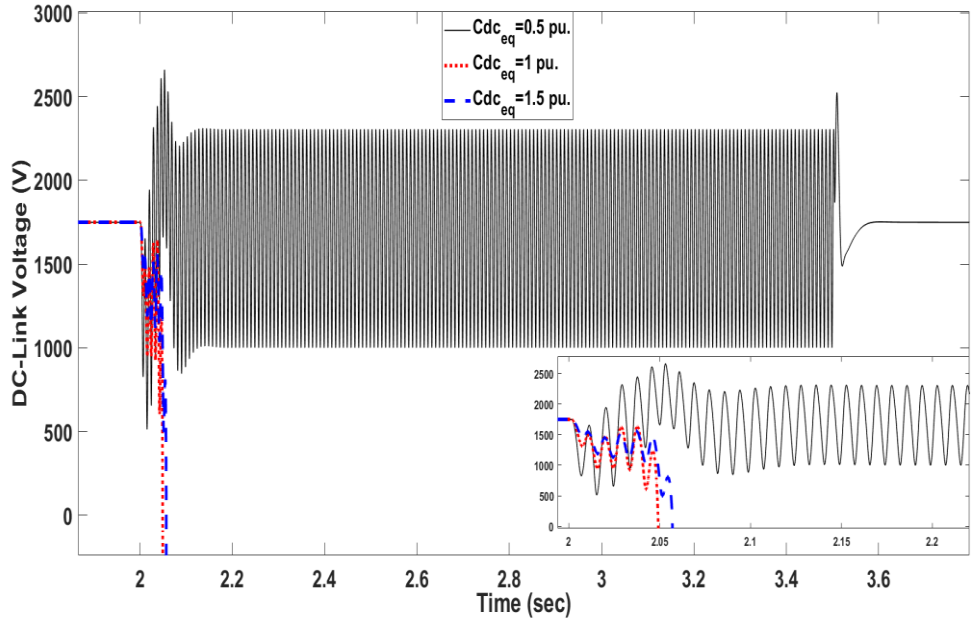


(b)

Figure 4.35 DC-link voltage response to L-G ac-grid fault at $P_{dc} = 1\,pu.$, and *SCR* : a) *SCR*=3, b) *SCR*=1.15.



(a)



(b)

Figure 4.36 DC-link voltage response to L-G ac-grid fault at $P_{dc} = -1\ pu.$, and *SCR* : a) *SCR*=3, b) *SCR*=2.5

4.5.2 Fault Assessment of the Interactions Between DC-link Capacitance Uncertainty and Controller Bandwidth

In rectification mode, the system is less tolerant of the fault occurring on the AC-side at low SCR levels compared to the inversion mode, as shown earlier. In Fig. 4.36(b), when $BW_{dc} = 0.2\ BW_{cc}$, the system can override the fault only at Cdc_{eq}= 0.5 pu. Reducing the DC-link voltage control

bandwidth to $BW_{dc} = 0.1\, BW_{cc}$ increases the ability of the system to override the fault over several values of the DC-link capacitance, as presented in Fig. 4.37. The increase in the bandwidth of the DC-link voltage control to 0.5 BW_{cc} did not allow the system to override the fault for all proposed DC-link capacitance values.

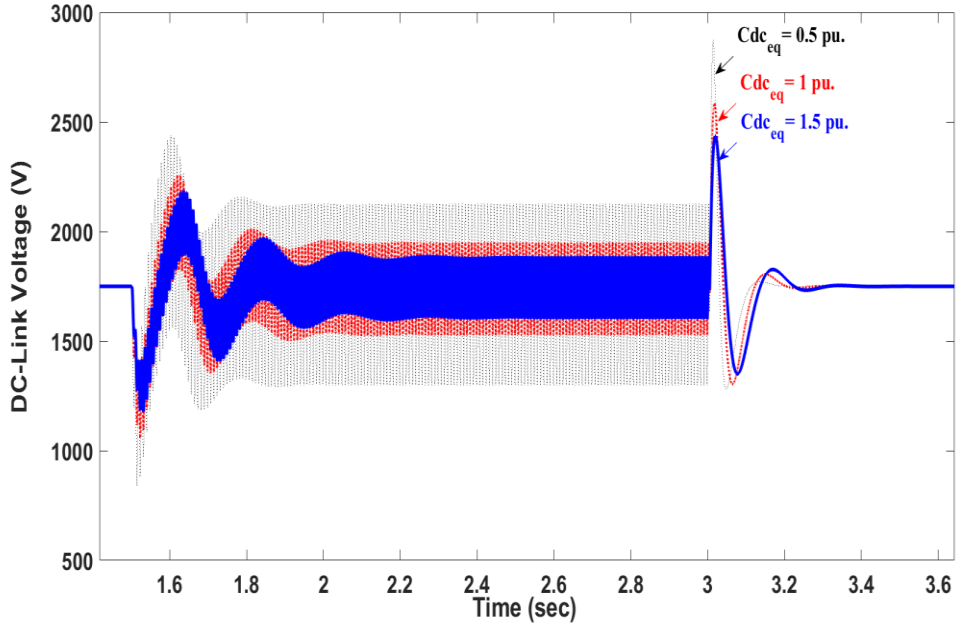


Figure 4.37 DC-link voltage response to L-G ac-grid fault at $P_{dc} = -1\ pu$, *SCR*=2.5 and $BW_{dc} = 0.1\ BW_{cc}$ in rectification mode.

In cases of changing the bandwidth of the AC-voltage and PLL controls, the amplitude oscillations during the fault are almost the same under different DC-link capacitance values, as illustrated in Figs. 4.38 and 4.39. In Fig. 4.38, when the AC-voltage control bandwidth decreases, the system is less vulnerable to override the fault, as demonstrated at BW_{ac}= 100 rad/sec. Figures 4.39 and 4.40 indicate that increasing the bandwidth of the PLL and DC-link capacitance degrades the system stability during the fault. Figure 4.40 reveals that the system can override the fault at both Cdc_{eq}= 0.5 and 1 pu, when decreasing the bandwidth of PLL from 200 to 100 rad/sec.

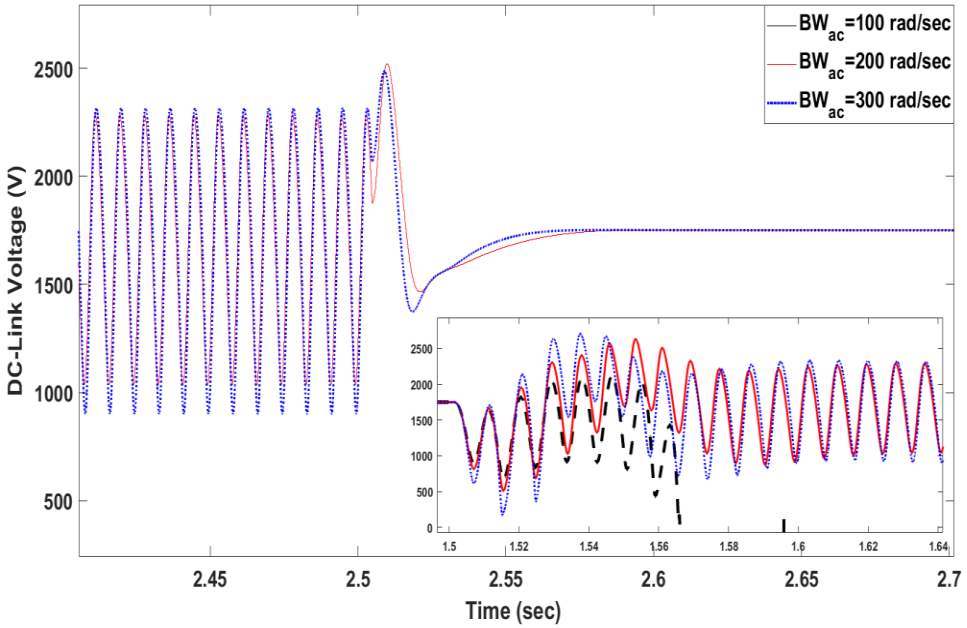


Figure 4.38 DC-link voltage response to L-G ac-grid fault at $P_{dc} = -1$ pu., *SCR*=2.5 and Cdc_{eq}= 0.5 pu., in rectification mode.

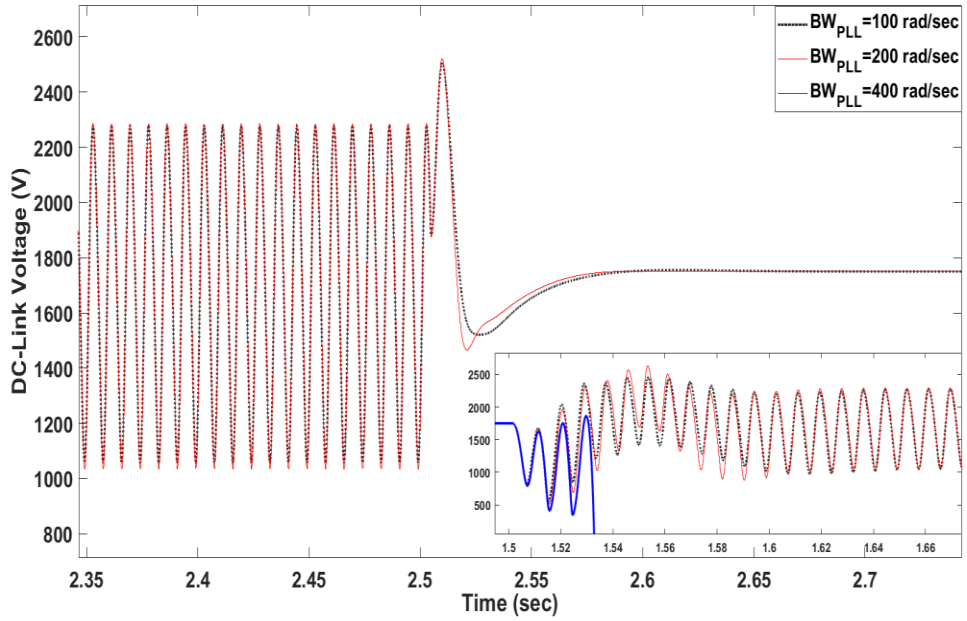


Figure 4.39 DC-link voltage response to L-G ac-grid fault at $P_{dc} = -1$ pu., *SCR*=2.5 and Cdc_{eq}= 0.5 pu., in rectification mode.

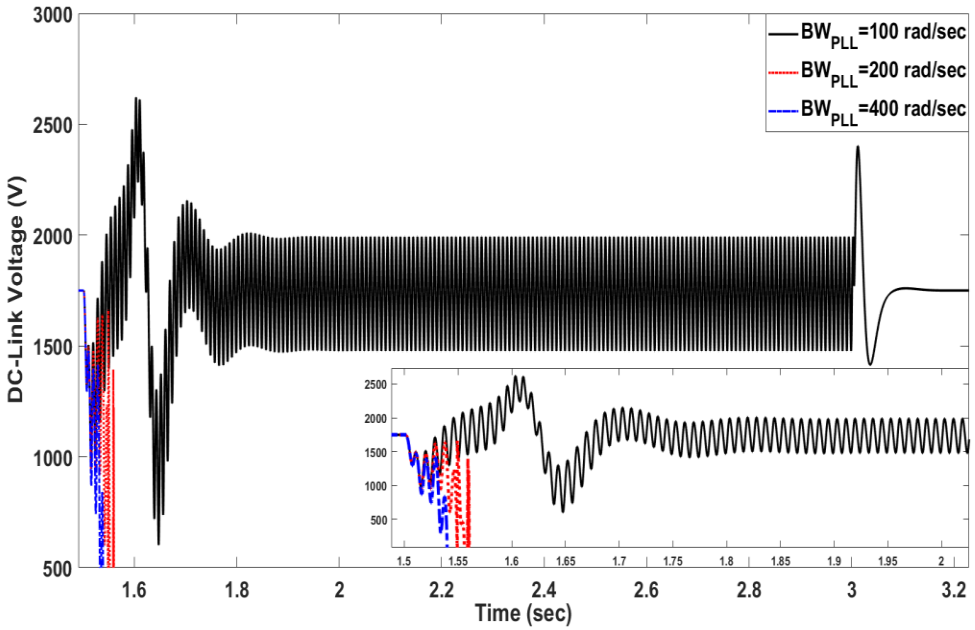


Figure 4.40 DC-link voltage response to L-G ac-grid fault at $P_{dc} = -1$ pu., *SCR*=2.5 and Cdc_{eq}= 1 pu., in rectification mode.

In the inversion mode, the effect of changing the controller bandwidth is considered in the worst-case scenario, which is at a very weak grid when Cdc_{eq}= 0.5 pu. Figures 4.41 to 4.43 present the influence of changing the control bandwidth when a single L-G fault occurs from t = 2.25 to 3.5 s. From these figures, increasing the controller bandwidth reduces the oscillation amplitude during the fault and settling time after clearing the fault. Except in Fig. 4.43, the post-fault recovery time increases when the bandwidth of the PLL control becomes closer to the DC-link voltage control bandwidth, as mentioned earlier. In Fig. 4.41, the recovery time decreases from 0.8 to 0.25 s after the fault clears when the DC-link voltage control bandwidth increases from 0.2 BW_{cc} to 0.5 BW_{cc}, respectively. In Figs. 4.42 and 4.43, the recovery time when the fault clears decreases from 0.8 to 0.12 s and from 0.73 to 0.35 s when the bandwidth of the AC-voltage and PLL control increases from 200 to 400 rad/s, respectively.

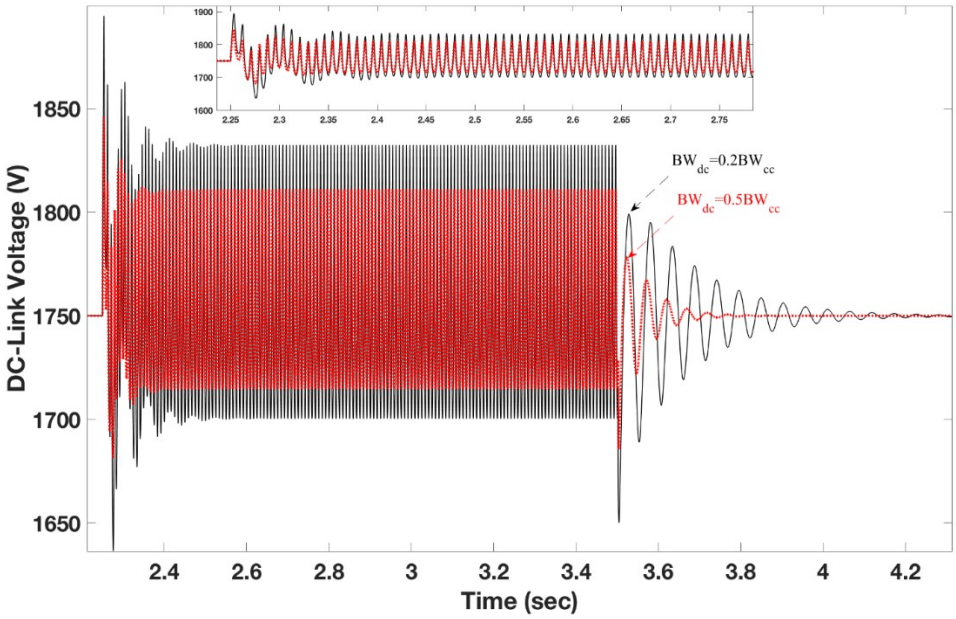


Figure 4.41 DC-link voltage response to L-G ac-grid fault at $P_{dc} = 1$ pu., *SCR*=1.15 and Cdc_{eq}= 0.5 pu., in inversion mode.

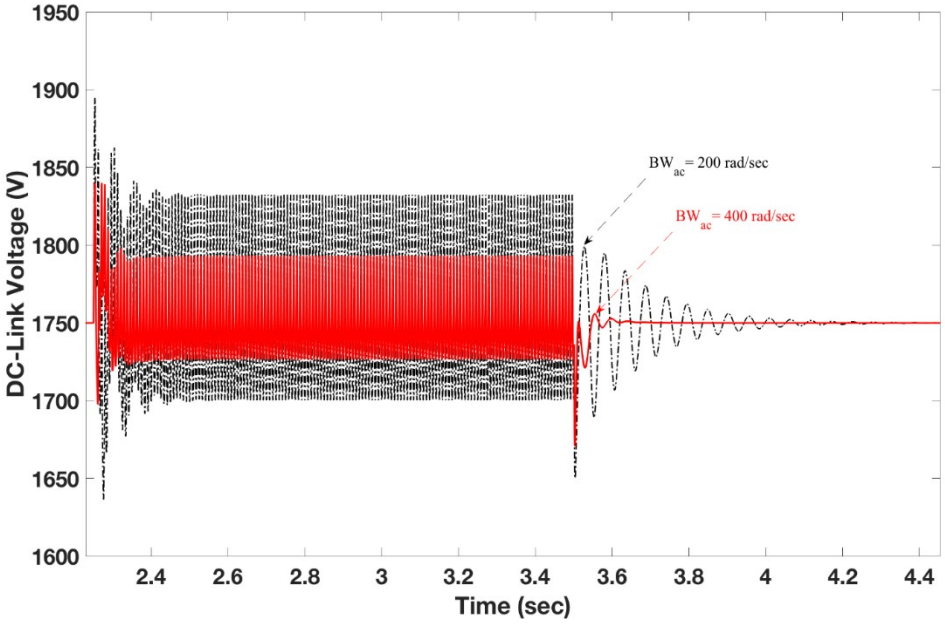


Figure 4.42 DC-link voltage response to L-G ac-grid fault at $P_{dc} = 1$ pu., *SCR*=1.15 and Cdc_{eq}= 0.5 pu., in inversion mode.

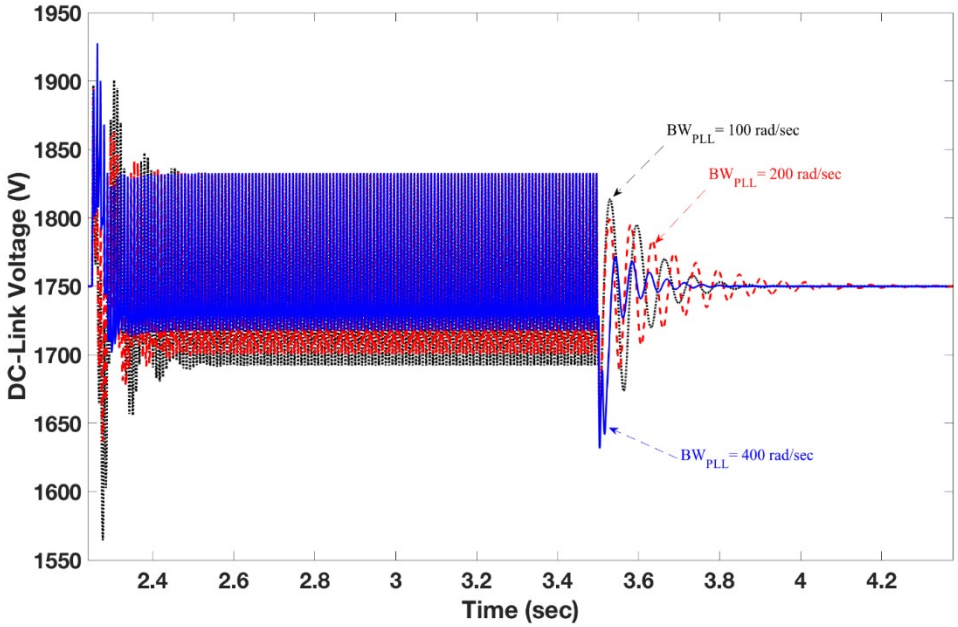


Figure 4.43 DC-link voltage response to L-G ac-grid fault at $P_{dc} = 1$ pu., *SCR*=1.15 and Cdc_{eq}= 0.5 pu., in inversion mode.

4.6 The Impacts of Parameters L_g , R_g and L_f on The Dynamic Stability of Grid-Connected VSC

As the main goal of this research work is studying the dynamic stability of VSC connected to weak and very weak grids, it is important to address the effects of AC-side filters and grid impedance on the overall stability. In this section, each parameter will be examined to find ranges that maintain system stability under weak grid conditions.

4.6.1 The Limitations of Grid Impedance Parameters that Maintain the System Stability

4.6.1.1 Inversion Mode

a) The limitations of grid inductance

Figures 4.44 and 4.45 show the impact of X_g/R_g (grid impedance ratio) and grid inductance on grid-connected VSC system stability. The default X_g/R_g ratio used in the analysis is 10. This ratio, however, will be gradually changed to illustrate its effect on the system stability. In this analysis, the grid impedance ratio is varied by changing the value of grid inductance according to $\left(X_g/R_g = \frac{\omega L_g}{R_g}\right)$. Therefore, increasing the value of grid inductance from 120 µH to 310 µH shifts

X_g/R_g from 5.5 to 14 when R_g =0.0084 Ω. The results plotted in this figure show that increases in X_g/R_g ratio push the poles toward the right-hand side. This is confirmed by looking at dominant modes ($\lambda_{6,7}$) that highly affected by increases in X_g/R_g. By examining these modes, the stability range of the system can be confined to $X_g/R_g \leq 10.5$. Conversely, modes ($\lambda_{4,5}$, $\lambda_{7,8}$) are not highly affected by varying the grid impedance ratio except that, when this ratio rises to 14, these poles leap to the unstable region.

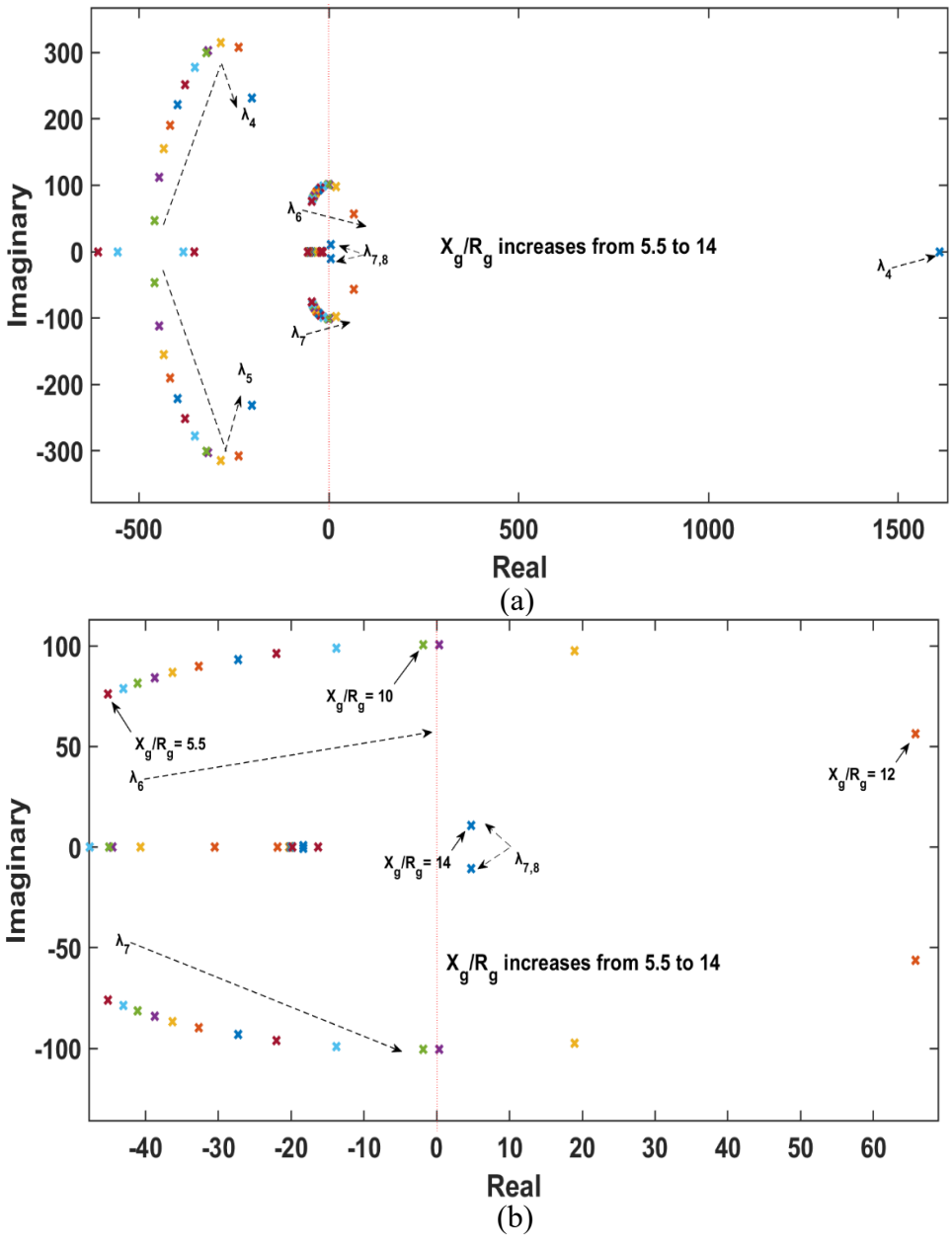


Figure 4.44 Root-locus of grid-connected VSC system at $P_{dc} = 1$ pu. and $SCR = 1.11$; a) $L_g$changes from 120 µH to 310 µH, b) Zoomed plot.

Figure 4.45 shows the minimum value of grid inductance that stabilizes the system at a worse case condition, viz. *SCR*=1. In this case, the system parameters are the default settings given in Table 3.1. The value of the grid inductance varies from 220 µH to 244.5 µH when R_g= 9.2 mΩ. From the figure, it is clear that the system will remain stable when $L_g < 225\ \mu$H. The cases of *SCR*=1 has been verified by time-domain simulation as shown in Fig. 4.46.

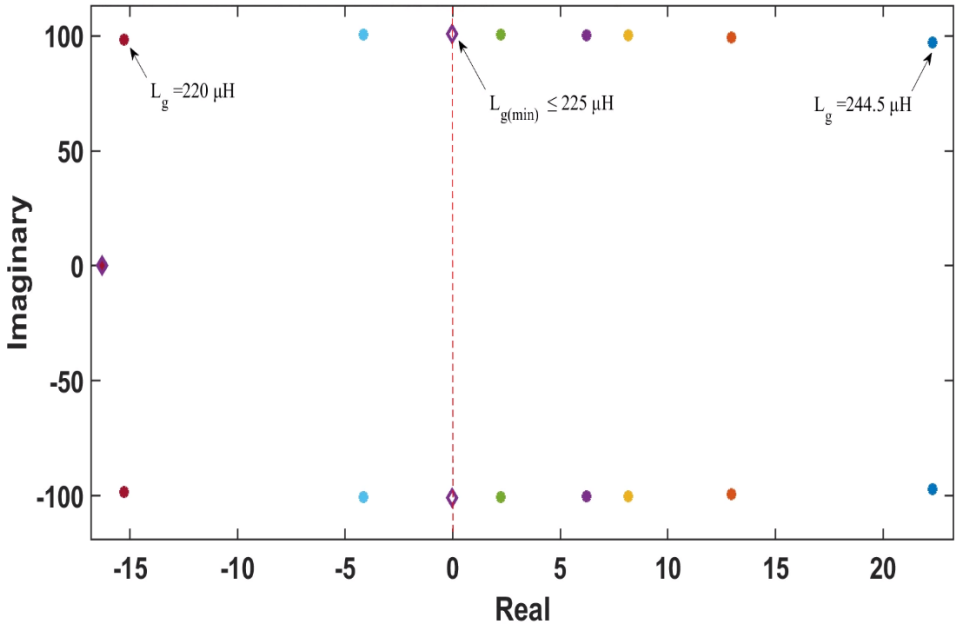


Figure 4.45 Root-locus of grid-connected VSC system at $P_{dc} = 1$ pu. and $SCR = 1$

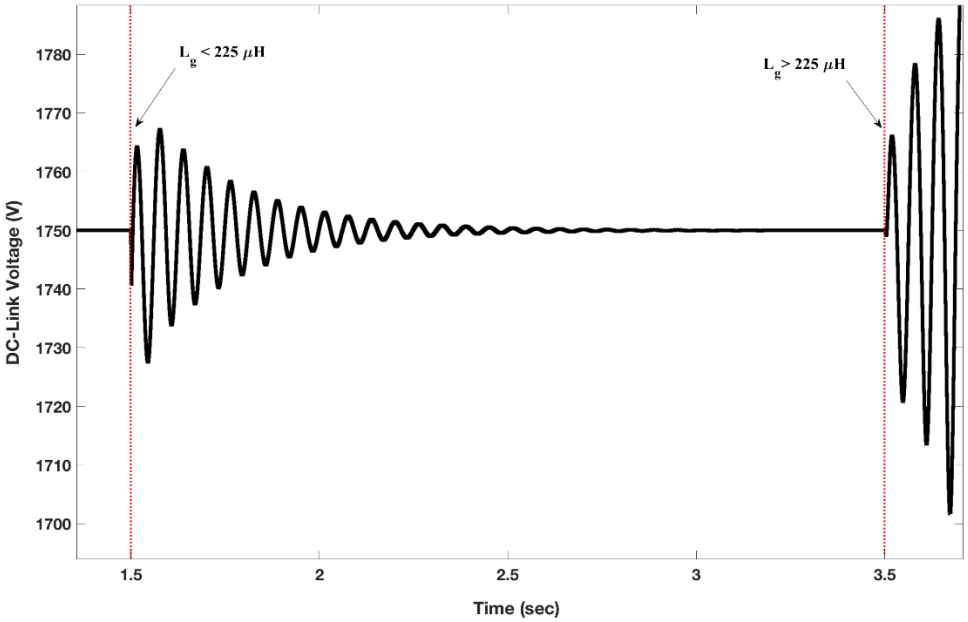
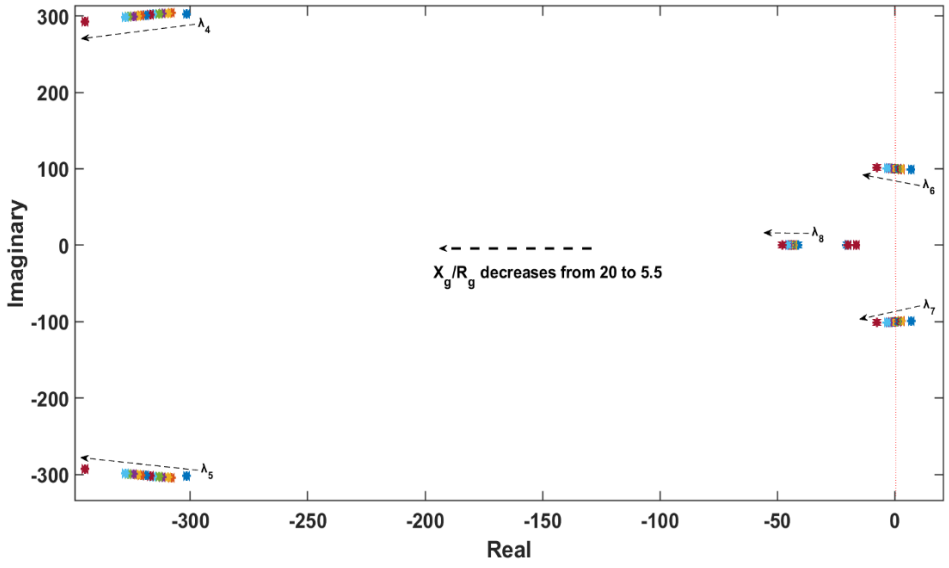


Figure 4.46 Time-domain of grid-connected VSC system at $P_{dc} = 1\ pu$ and *SCR*=1

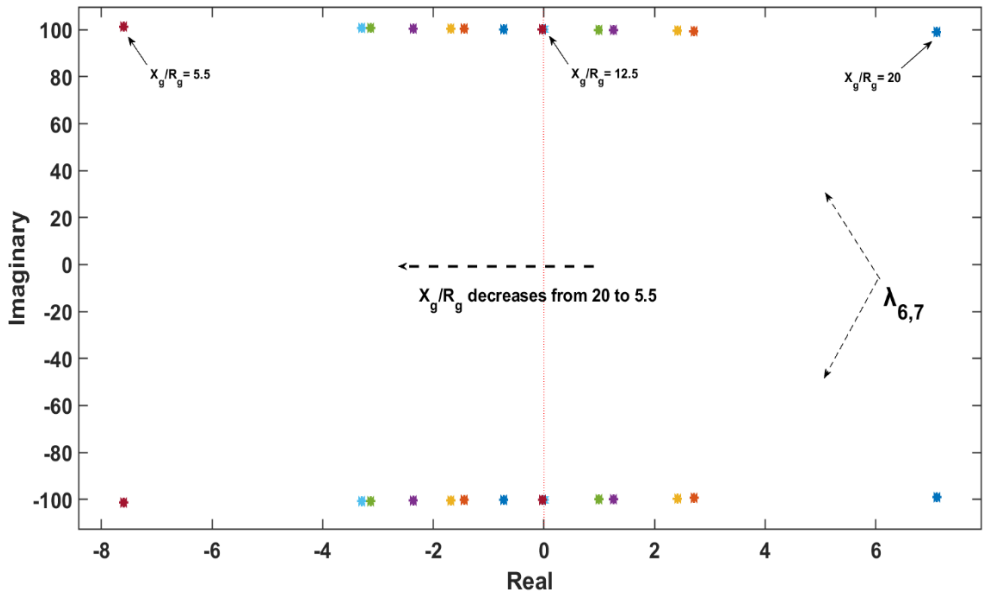
b) The limitations of grid resistance

In the previous case, the effect of the grid impedance ratio on system stability was studied in terms of grid inductance. Here, a similar case will be studied but in terms of grid resistance. In this analysis, the grid impedance ratio is varied by changing the grid resistance according to the same equation. As a result, increasing the grid resistance R_g from 4.1 mΩ to 15 mΩ changes X_g/R_g from 20 to 5.5 when $L_g = 220$ μH. Figure 4.25 shows that decreasing X_g/R_g pushes the poles toward the stable region. This is confirmed by looking at dominant modes ($\lambda_{6,7}$) highly affected by increases and decreases in X_g/R_g as seen in Fig. 4.47 (b). From this figure, the minimum range that maintain the system stability can be identified as $X_g/R_g \leq 12.5$. Also, it can be clearly seen that modes ($\lambda_{4,5}$, λ_8) are not strongly affecting the system stability by varying the grid impedance ratio, unlike the previous case.

The effect of grid resistance that stabilize the system at worse case condition (*SCR*=1) is presented in Fig. 4.48. In this figure, the minimum value of grid resistance is analytically showed. All the parameters of the system are set to the default setting as seen in Table 3.1. The value of R_g varies from 9.2 mΩ to 50 mΩ when L_g= 244.46 µH. As mention earlier, at the very weak grid condition the system enters the unstable region. Figure 4.48 illustrates that, at this critical condition, system stability can be achieved by increasing R_g. Therefore, it has been analytically proven that the system will remain stable when $R_g \geq$ 25 mΩ and $X_g/R_g \leq 3.7$ as seen in the figure below. This case has been verified by the time-domain simulation as shown in Fig. 4.49.



(a)



(b)

Figure 4.47 Root-locus of grid-connected VSC system at $P_{dc} = 1$ pu. and $SCR = 1.11$; a) X_g/R_g changes from 5.5 to 20 b) Zoomed plot.

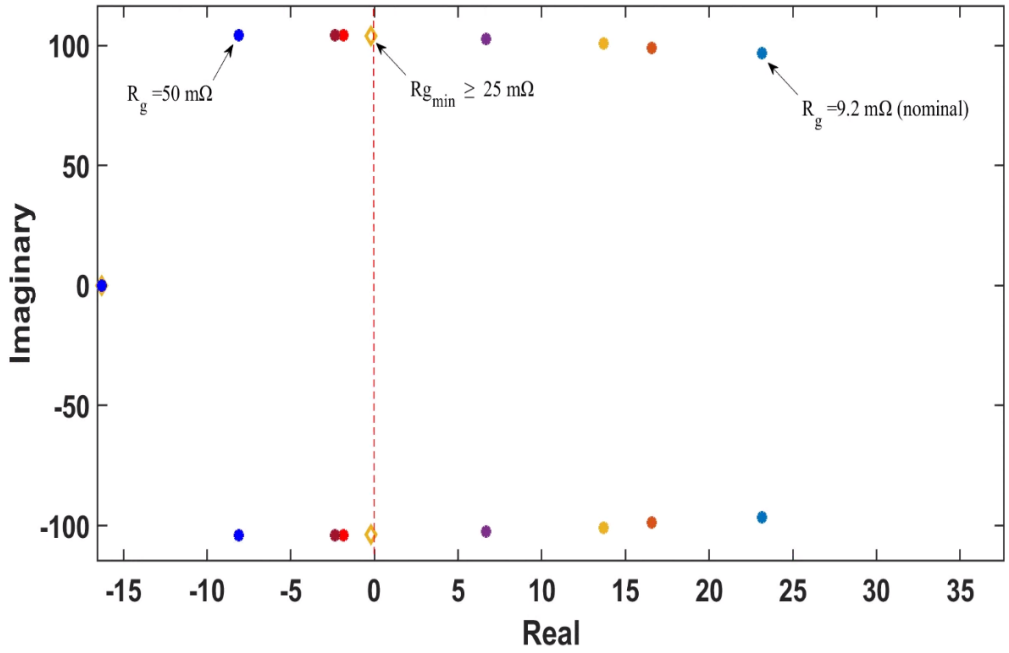


Figure 4.48 Root-locus of grid-connected VSC system at $P_{dc} = 1$ pu and $SCR = 1$

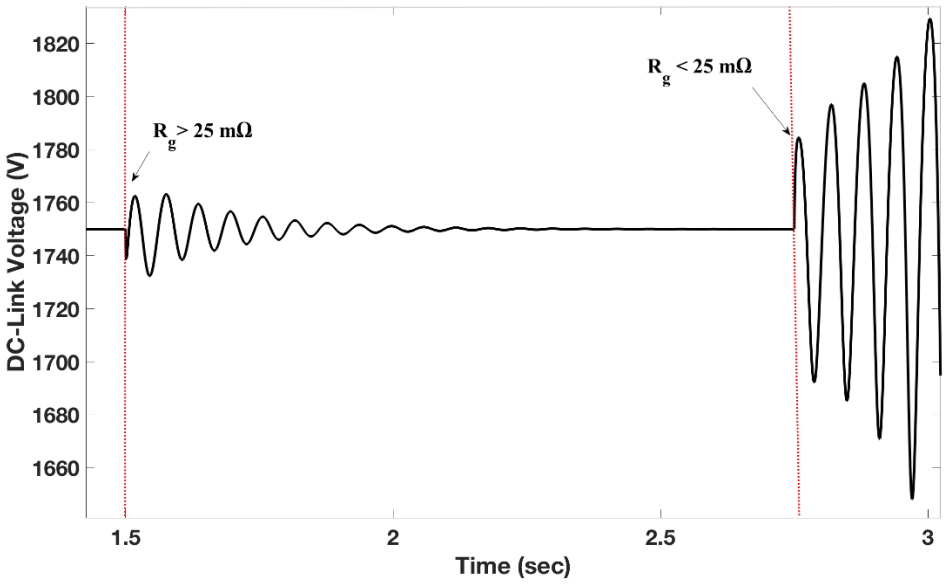


Figure 4.49 Time-domain of grid-connected VSC system at $P_{dc} = 1\ pu$ and *SCR*=1

4.6.1.2 Rectification Mode

a) The limitations of grid inductance

Figure 4.50 shows the impact of the X_g/R_g ratio and grid inductance on grid-connected VSC system stability in rectification mode. The default X_g/R_g ratio used in the analysis is 10. This ratio, however, will be gradually changed to illustrate its effect on system stability. In this analysis, X_g/R_g ratio is varied by changing the grid inductance according to $\left(X_g/R_g = \frac{\omega L_g}{R_g}\right)$. Therefore, increasing L_g from 120 µH to 210 µH raises X_g/R_g from 7 to 13 when $R_g = 6.2$ mΩ. The results in this figure show that decreasing X_g/R_g pushes the poles toward the left-hand side. This finding can be confirmed by looking at dominant modes ($\lambda_{6,7}$) that are highly affected by increases in X_g/R_g. From these modes, the stability range of the system can be identified as $X_g/R_g \leq 10.7$. Conversely, modes ($\lambda_{4,5}$, $\lambda_{7,8}$) are not highly affected by varying X_g/R_g except that, when this ratio goes up to 12 and 13, these poles leap to the unstable region.

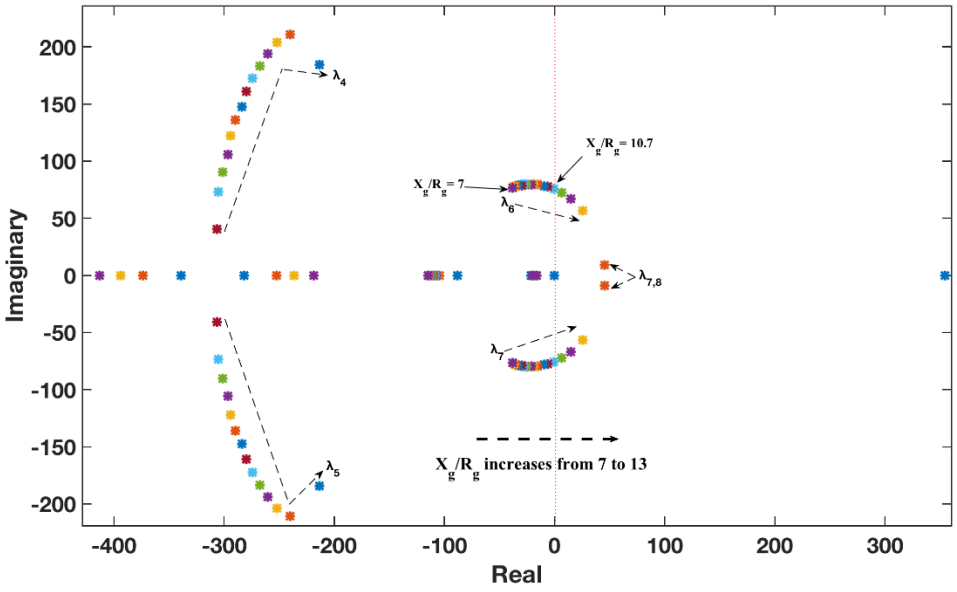
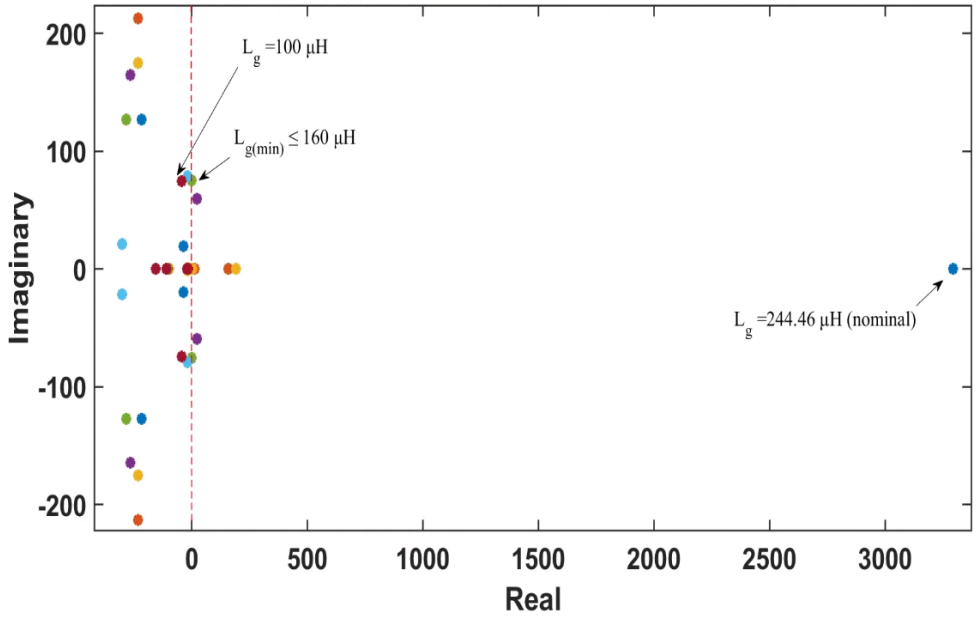
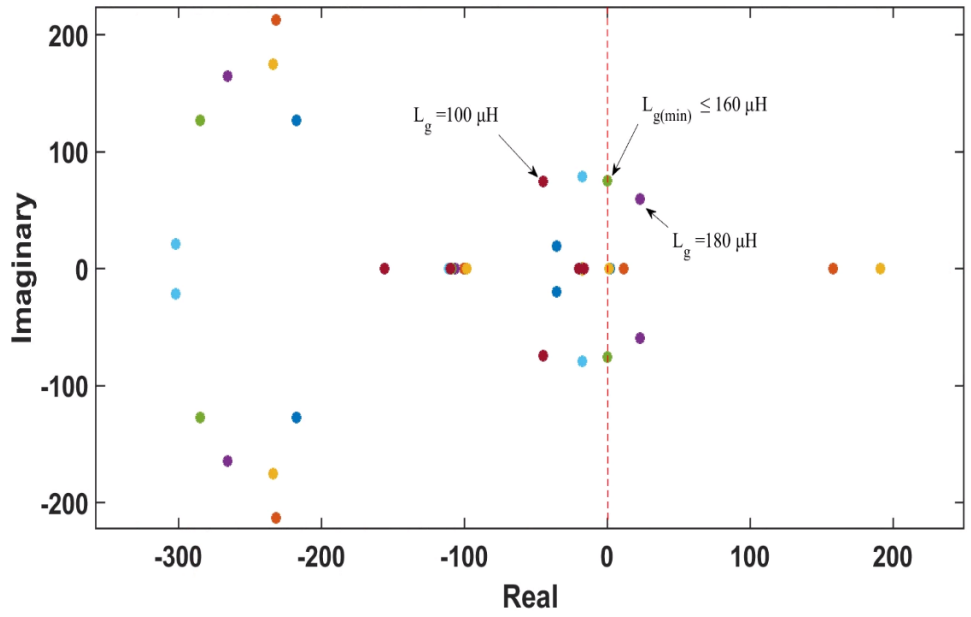


Figure 4.50 Root-locus of the grid-connected VSC system when at $P_{dc} = -1\ pu$ and $SCR = 1.45$.

Figures 4.51 show the minimum value of grid inductance that stabilizes the system at the worse-case condition, which is *SCR*=1. In this case, the parameters of the system are set to the default. The value of $L_g$varies from 100 µH to 180 µH when R_g= 9.2 mΩ. From Fig. 4.51 (b), it is clear that the system will remain stable when $L_g < 160\ \mu$H as also verified by the time-domain simulation shows in Fig. 4.52.



(a)



(b)

Figure 4.51 Root-locus of grid-connected VSC system. a) $L_g$changes from 100 µH to 180 µH, b) Zoomed plot.

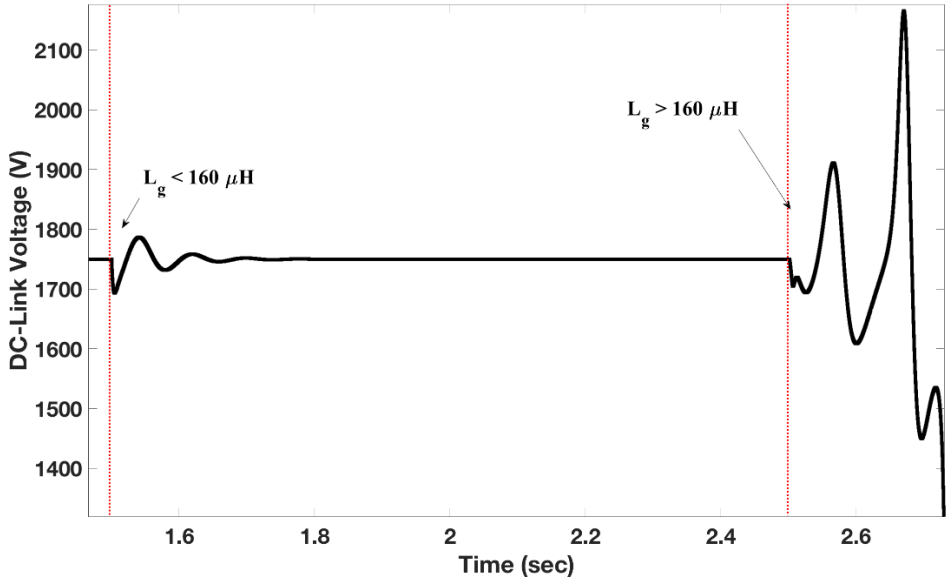
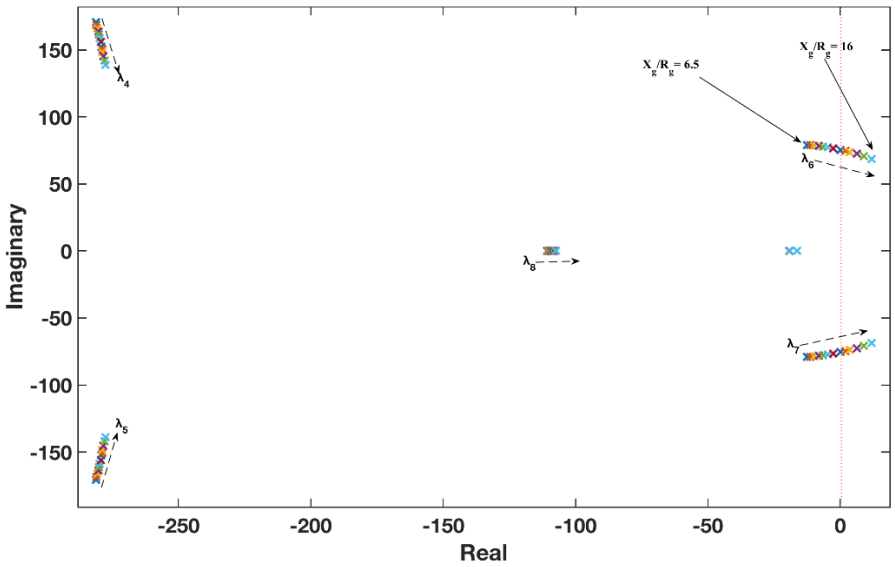


Figure 4.52 Time-domain of grid-connected VSC system at $P_{dc} = -1\ pu$ and $SCR = 1$

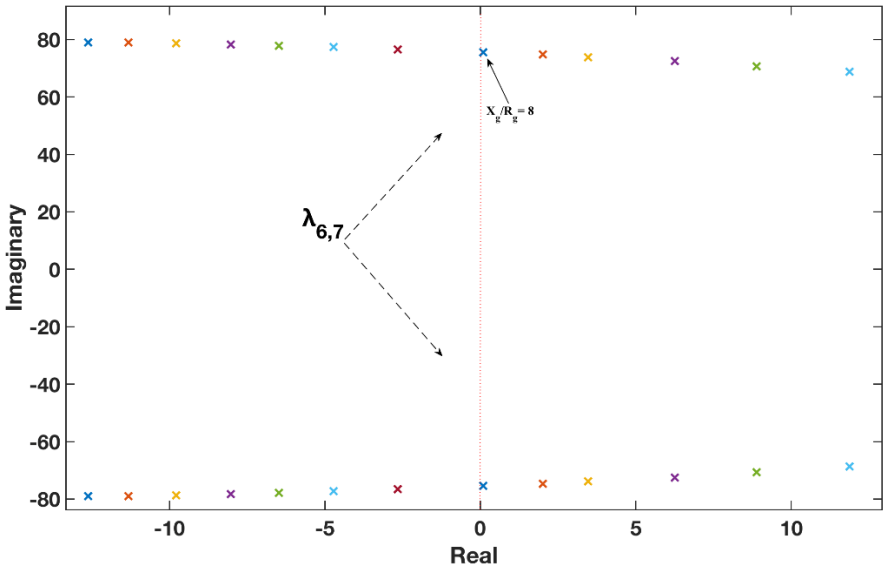
b) The limitations of grid resistance

In the previous case, the effect of X_g/R_g on system stability was studied in terms of grid inductance. Here, a similar case will be studied but in terms of grid resistance. In this analysis, X_g/R_g ratio varies by changing the grid resistance based on the aforementioned equation. Thus, increasing R_g from 4.1 mΩ to 10 mΩ decreases X_g/R_g from 16 to 6.5 when $L_g = 168\ \mu$H. Figure

4.53 show that decreasing X_g/R_g ratio adversely affects system stability. This is confirmed by looking at the dominant modes ($\lambda_{6,7}$) that are affected by increases and decreases in X_g/R_g as seen in Fig. 4.53 (b). From this figure, the minimum range that maintains system stability can be identified as $X_g/R_g \leq 8$. It can be clearly noted that modes ($\lambda_{4,5}$, λ_8) are not greatly impacting the stability of the system by varying the X_g/R_g ratio, which is similar to what happens in inversion mode. Although, decreasing the grid resistance enhances the system stability in the rectification mode, but it could not stabilize the system at *SCR*=1 as in inversion mode.



(a)



(b)

Figure 4.53 Root-locus of grid-connected VSC system. a) $R_g$changes from 4 mΩ to 10 mΩ, b) Zoomed plot.

4.6.2 The Limitations of AC-side Filter Parameters that Maintain the System Stability

4.6.2.1 Inversion Mode

In the previous section, the effect of grid resistance and inductance was examined. However, it is also important to study the effect of the AC-side inductance filter on the overall system stability as will be presented in this section. In this analysis, all the parameters are set as shown in Table 3.1, except that the value AC-side inductance filter is varied to study its impact on system stability. Figures 4.54 and 4.55 show the eigenvalues of the system when L_f is varied over a certain range at *SCR* = 1.5 and 1.11, respectively that has been used in aforementioned analysis. At the former case, it can be noted that when L_f changes from 0.85 to 1.1 pu system stability is slightly affected. As clear in Fig. 4.54, at L_f = 0.85 pu. the damping ratio ζ=0.28 while, at L_f = 1.1 pu., the damping ratio ζ=0.34. System stability, therefore, is slightly enhanced when L_f increases.

When SCR reduces to 1.11, system stability becomes very sensitive to variations in the AC-side inductance filter, as seen in Fig. 4.55. In this case, decreasing L_f by 15% is enough to make the system unstable (yellow diamond). From this figure, it can be noted that the minimum range of AC-side inductance filter that ensures system stability is $L_f \geq$ 0.9 pu. This result was agreed with the time-domain simulation shown in Fig. 4.56.

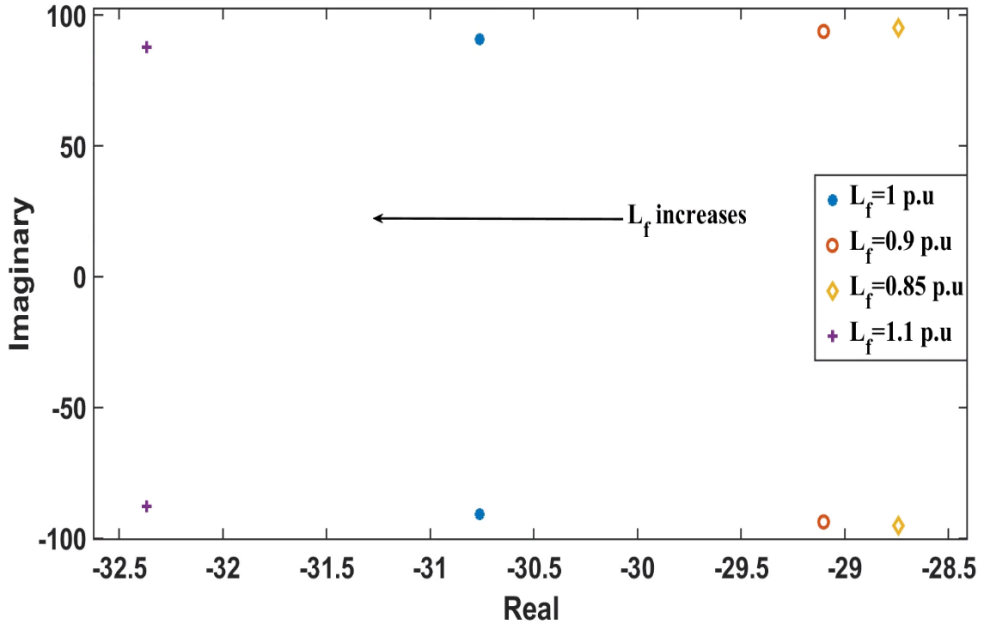


Figure 4.54 Root-locus of grid-connected VSC system at P_{dc} = 1 pu., *SCR*=1.5.

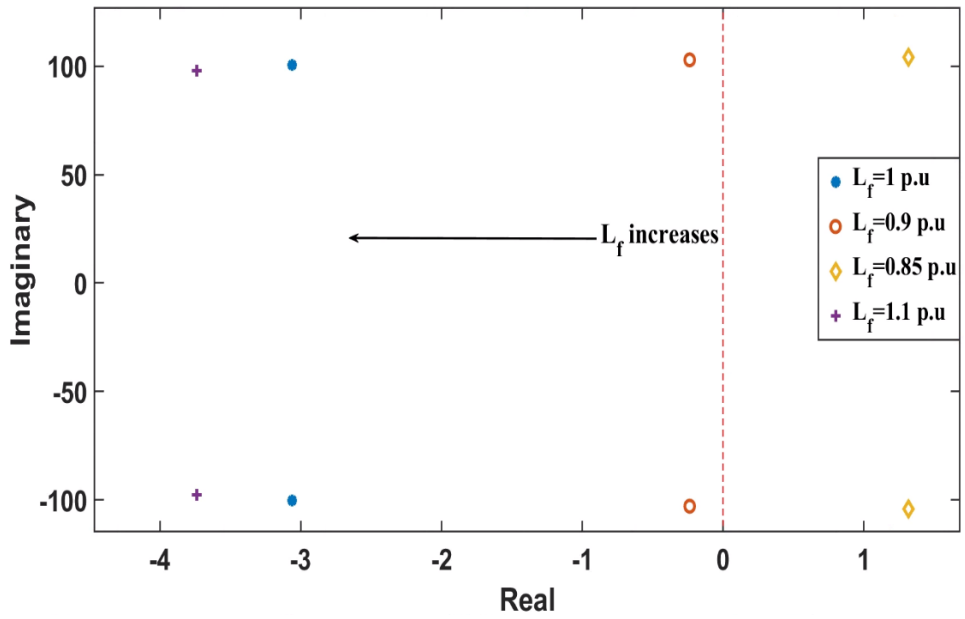


Figure 4.55 Root-locus of grid-connected VSC system at $P_{dc} = 1$ pu. , $SCR = 1.11$.

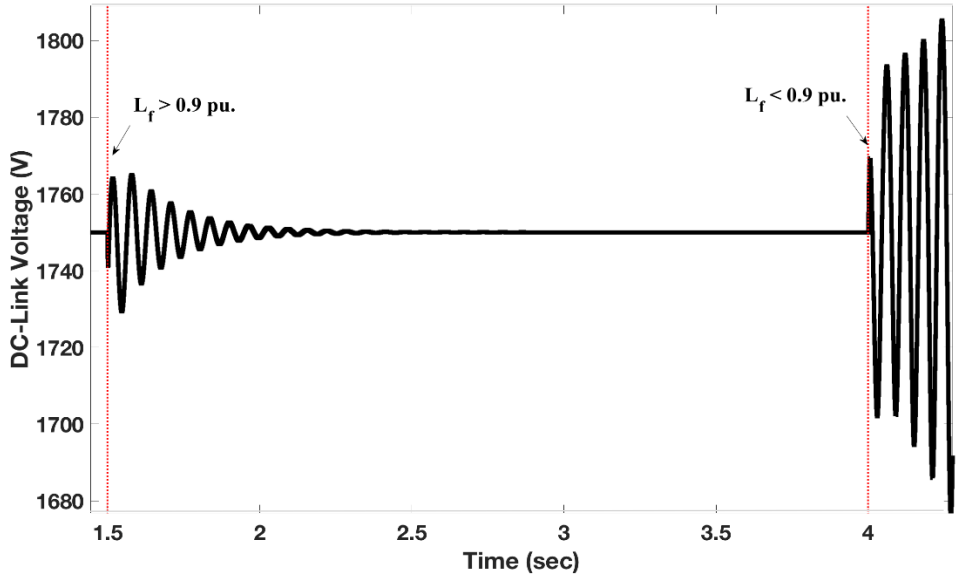


Figure 4.56 Time-domain of grid-connected VSC system at $P_{dc} = 1\ pu$ and $SCR = 1.11$

4.6.2.2 Rectification Mode

Figures 4.57 and 4.58 show the eigenvalues of the system when L_f is subjected to change from 0.9 to 1.15 pu. at *SCR* = 3 and 1.45, respectively. From the plots, it is clear that increasing and/or decreasing the ac inductance filter by approximately ± 10 % highly affects the system stability in a very weak grid condition (i.e. *SCR*=1.45), and lightly in weak and strong grid conditions. To achieve a reliable stability for the system in a very weak grid condition, the ac inductance limit shall be chosen as $L_f \leq 1.12$ pu. This limit of ac inductance has also been proofed by the time-domain simulation presented in Fig. 4.59. It is worth mentioning that, at *SCR*=1.45, the poles of the system move toward the right-hand side faster than at *SCR*=3 in the rectification mode.

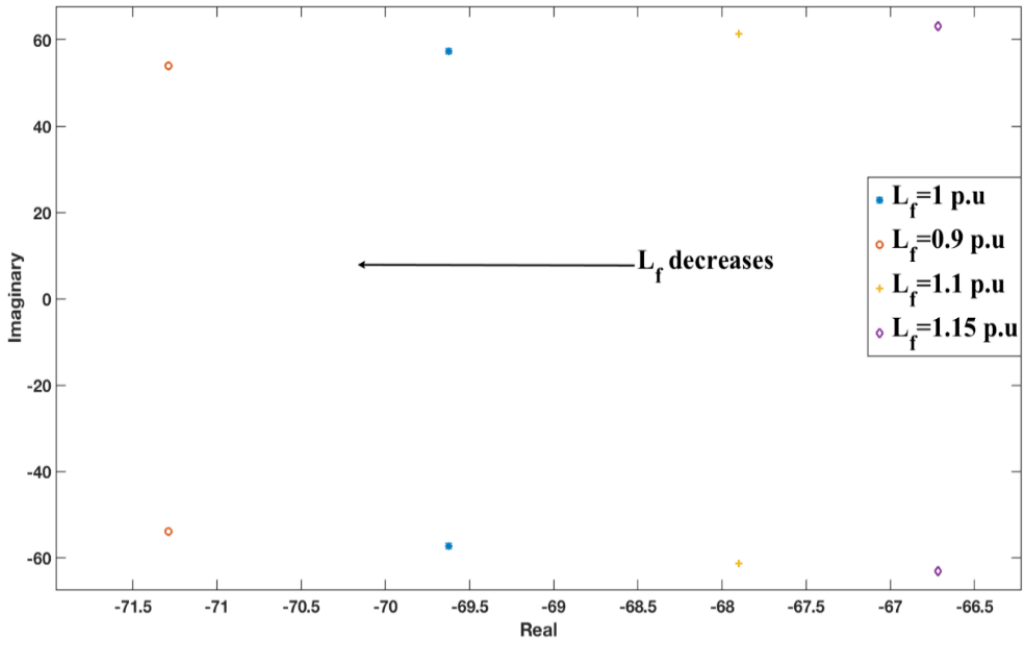


Figure 4.57 Root-locus of grid-connected VSC system at $P_{dc} = -1$ pu., $SCR = 3$.

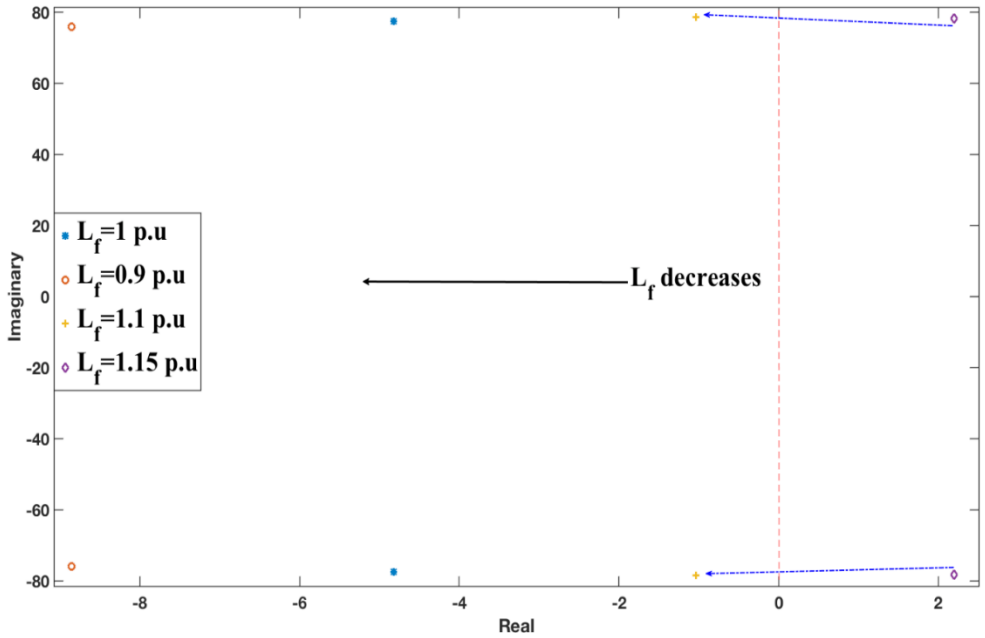


Figure 4.58 Root-locus of grid-connected VSC system at $P_{dc} = -1$ pu., SCR =1.45

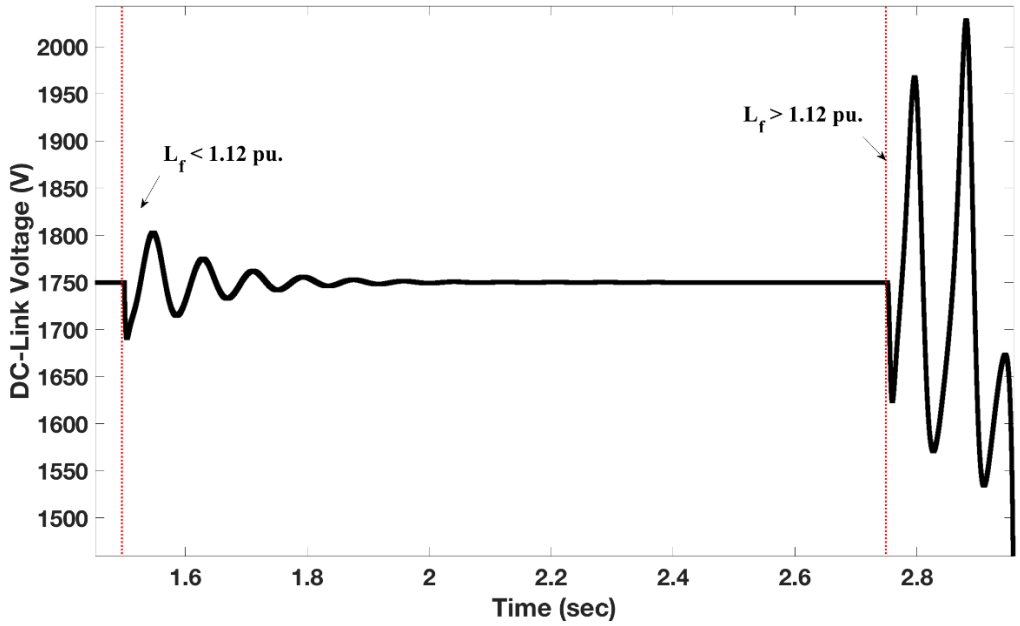


Figure 4.59 Time-domain of grid-connected VSC system at $P_{dc} = -1\ pu$ and $SCR = 1.45$

4.7 Summary

Several stability analyses of grid-connected VSC system have been considered in this chapter. The first analysis is aimed to observe the dynamic interactions between DC-link capacitance uncertainty and grid strength. In inversion mode, it has been proven that increasing the DC-link capacitance not always enhances the system stability. It also has been shown that increasing the DC-link capacitance at very low ranges of SCR enhances the system stability, unlike high level of SCR. In rectification mode, increasing the DC-link capacitance degrades the system stability even at a very low SCR level. In this mode, the stability of the system is confined to a certain limit of Cdc_{eq}variations. The second analysis is investigated the impact of DC-link capacitance uncertainty on controllers' bandwidth, which are DC-bus voltage, SRF-PLL and AC voltage controllers' bandwidth. For a DC-bus voltage controller, in inversion mode, decreasing the BW_{dc} and Cdc_{eq} slightly degrades the system stability at high to low SCR levels. Whereas this effect greatly degraded the system stability at a very low SCR level. The opposite results have been observed in the rectification mode. For a SRF-PLL voltage controller, it has been reported that worst-stability performance is observed at BW_{PLL}= 200 rad/sec due to its closeness to the bandwidth of the DC-link voltage controller in inversion mode, unlike rectification mode. In this case, it has shown that increasing the DC-link capacitance, therefore, can contribute to enhancing the system stability. In rectification mode, it is observed that the sensitivity of the DC-link capacitance increases as BW_{PLL} increases. For an AC-bus voltage controller, increasing BW_{ac} can contribute strongly to enhancing system stability against very low SCR and uncertainty in the DC-link capacitance in inversion mode. In rectification mode, both DC-link capacitance and AC voltage controller bandwidth strongly influence system stability at very low SCR. Furthermore, the Cdc_{eq} can contribute greatly to stabilizing the system. It can be concluded that the effect of controllers' bandwidth under stiff-grid conditions are minimal, whereas dynamics interactions are increased in a very weak-grid condition. The objective of third analysis is study the interactions between grid angle and DC-link capacitance variations in a very weak-grid condition. It has been found that at $SCR \geq 3$, the effect of the DC-link capacitance uncertainty slightly affects the dynamic stability of the system when the grid angle increases or decreases in both modes. In a very weak-grid condition, it has been shown that increasing the grid angle and decreasing the DC-link capacitance leads to worst stability condition in inversion mode and vise-versa for rectification

mode. The fourth analysis is fault assessment in case of uncertainty in the DC-link capacitance. It shown that at $SCR \geq 3$, the system can override the fault in both modes of operations. At $SCR < 3$, the settling-time increases when the DC-link capacitance decreases after the fault is cleared in inversion mode. At the same SCR the system become less capable to override the fault when the DC-link capacitance increases in rectification mode. Last analysis is studying the impacts of grid impedance and AC inductance filter on the dynamic stability of grid-connected VSC. It has been proven that grid inductance is not the only factor influencing system stability; grid resistance and impedance ratio also affect the stability. The minimum value of L_g and R_g represented by X_g/R_g that maintain the system stability has been founded at very low SCR for both mode of operations. Further, the effect of these parameters has been investigated under worst-case condition, SCR=1. It has been found that the system can be re-stabilized when decreasing L_g or increasing R_g to certain values in inversion mode. The same thing for rectification mode but changing R_g is not capable to stabilize the system. Regarding the effect of AC inductance filter, slight variations can significantly affect system stability especially at weak grid conditions. It has been founded that, decreasing L_f by 15% is enough to make the system unstable in inversion mode. In rectification mode, increasing and/or decreasing the L_f by approximately ± 10 % greatly affects the system stability.

Chapter 5

Summary and Future Work

5.1 Conclusion

This research was facilitated to develop a comprehensive analysis of a VSC connected to weak grid conditions. As the DC-link capacitance is an inevitable component in most converter systems, the evaluation in this thesis focused on how the interaction between the equivalent DC-link capacitance uncertainty and the grid strength affect the system stability.

Chapter 2 provided an overview of the advancement of power electronics technology. Further, principles and operation of the VSC were presented in detail. A comparison between the VSC and the CSC was also shown. As the main focus of this research was the VSC, this chapter illustrated the control type that was adopted in this work. A thorough literature review on the stability analysis of the VSC connected to weak and very weak grids was reported.

Chapter 3 clearly showed and explained the structure of the studied system and the methodology that was applied. It was demonstrated that the DC-side in the grid-connected VSC system was set as a controlled current source, which was represented as a virtual DC microgrid. The DC-link capacitance, therefore, might face uncertainty due to loading/and unloading on the DC-side or changing in ambient temperature. Furthermore, this chapter presented the parameter values of each component and began a brief discussion of the concept of linearization. The general design method for the main four types of controllers used in the study was depicted in detail. The mathematical large-signal model for the grid-connected VSC was given. From this model, the linearized state-space model was derived and presented in detail. To validate the analytical results, a report of the verification of the small-signal model against the MATLAB/Simulink model under different critical case scenarios was included.

Chapter 4 presented the comprehensive stability analysis for the grid-connected VSC system, using the linearization model that was derived in Chapter 3. Further, chapter 4 showed the framework of this thesis, which was to study the impact of a weak and very weak grid on a VSC with uncertainty in the DC-link capacitance. The evaluation was not only confined to studying the effect of DC-link capacitance, but also involved investigating the effect of the inductance line filter and grid impedance when subjected to variations. Eigenvalue analysis was used to investigate the

stability of the system. The analysis in this chapter was categorized into five sections: the effect of DC-link capacitance uncertainty on different grid strength conditions, the impact of DC-link capacitance uncertainty on the controllers' bandwidth, the effect of DC-link capacitance uncertainty on grid-angle variations, fault assessment, and the limitations of parameters L_f, L_g, and R_g that maintain the system's stability. In the first section, it was shown that, at a stiff grid condition (i.e. $SCR \geq 3$), the impact of the DC-link capacitance variations did not significantly affect the system stability in inversion and rectification modes as it did at weak grid conditions. At stiff and weak grid conditions, in the inversion mode, the system stability slightly degraded as the DC-link capacitance value increases. Conversely, at a very weak grid condition, the system stability was enhanced as the DC-link capacitance increased. In the rectification mode, the stability of the system degraded when the DC-link capacitance increased at stiff and weak grid conditions. Whereas, at a very weak grid condition, the system stability highly degraded when the DC-link capacitance increased. In the second section, it was revealed that the effect of the controllers' bandwidth on a stiff grid was minimum, whereas dynamics interactions increased remarkably when the grid condition was very weak. At $SCR < 3$, increasing the DC-link capacitance and controllers' bandwidth enhanced the system stability in the inversion mode and degraded stability in rectification mode, except when increasing the bandwidth of the AC voltage controller. In the third section, it has been studied the interactions between grid angle and DC-link capacitance variations in a weak-grid conditions. It has been found that at $SCR \geq 3$, the effect of the DC-link capacitance uncertainty slightly affects the dynamic stability of the system when the grid angle increases or decreases in both modes. In a very weak-grid condition, it has been shown that increasing the grid angle and decreasing the DC-link capacitance leads to worst stability condition in inversion mode and vise-versa for rectification mode. In the fourth section, a fault assessment in case of uncertainty in the DC-link capacitance has been conducted. It shown that at $SCR=3$, the system can override the fault in both modes of operations. At $SCR < 3$, the settling-time increases when the DC-link capacitance decreases after the fault is cleared in inversion mode. At the same SCR the system become less capable to override the fault when the DC-link capacitance increases in rectification mode. In the last section, it was demonstrated that grid inductance is not the only factor influencing the system stability, as grid resistance also has an effect. Moreover, the results showed that a slight variation in the AC line inductance can significantly affect the stability of the system, especially at weak grid conditions.

Finally, the impact of the DC-link capacitance uncertainty on the system stability is higher in rectification than in inversion mode in a weak-grid condition. Moreover, the selection of the DC-link capacitance depended not only on the ripple percentage in the DC-bus voltage, but also on the grid strength level, which can affect the system stability. This is especially true in a very weak grid.

5.2 Future Work

Based on the comprehensive analysis that was considered in this work, further studies can touch on the following areas:

- Solutions that can immunize the effect of the DC-link capacitance and grid uncertainties and increase the stability of the system need to be investigated. This could include active damping technique, among others.
- In this analysis, it was shown that there are interactions between controllers' loops affect the stability of the system. Therefore, further research should identify how minimizing these interactions can improve system stability.
- This research analyzed how the interaction between the equivalent DC-link capacitance uncertainty and the grid strength affected the system stability. Consequently, conducting the same type of analysis while considering the equivalent DC-link inductance might also be necessary to be addressed in future studies.

Bibliographies:

[1] G. Putrus and E. Bentley, "Integration of distributed renewable energy systems into the smart grid," in *Electric Renewable Energy Systems*, ed. Boston: Academic Press, 2016, pp. 487-518.

[2] P. A. Owusu and S. Asumadu-Sarkodie, "A review of renewable energy sources, sustainability issues and climate change mitigation," *Cogent Engineering,* vol. 3, 2016.

[3] F. B. a. Z. Chen, "Power Electronics as an Enabling Technology for Renewable Energy Integration," *J. Power Electron,* vol. 3, pp. 81-89, 2003.

[4] F. Blaabjerg and K. Ma, "Future on power electronics for wind turbine systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 1, pp. 139-152, 2013.

[5] T. Dragičević, "Dynamic Stabilization of DC Microgrids with Predictive Control of Point-of-Load Converters," *IEEE Transactions on Power Electronics,* vol. 33, pp. 10872-10884, 2018.

[6] "Renewable capacity highlights," International Renewable Energy Agency, Abu Dhabi2020.

[7] N. Mohan, T. M. Undeland, and W. P. Robbins, "Power Electronics: Converters, Applications and Design," 2003.

[8] L. Che, X. Zhang, M. Shahidehpour, A. Alabdulwahab, and A. Abusorrah, "Optimal Interconnection Planning of Community Microgrids with Renewable Energy Sources," *IEEE Transactions on Smart Grid,* vol. 8, pp. 1054-1063, 2017.

[9] H. Wang and J. Huang, "Cooperative Planning of Renewable Generations for Interconnected Microgrids," *IEEE Transactions on Smart Grid,* vol. 7, pp. 2486-2496, 2016.

[10] G. Venkataramanan and C. Marnay, "A larger role for microgrids," in IEEE Power and Energy Magazine, vol. 6, no. 3, pp. 78-82, May-June 2008.

[11] A. A. A. Radwan and Y. A. R. I. Mohamed, "Linear active stabilization of converter-dominated DC microgrids," *IEEE Transactions on Smart Grid,* vol. 3, pp. 203-216, 2012.

[12] "DC-Link Design Tips," Oct. 1st, 2019. [Online]. Available: https://ec.kemet.com/blog/dc-link-design-tips/

[13] J. H. Jung, H. J. Heo, J. M. Kim, and S. U. Choi, "DC-link voltage stabilization and source THD improvement using d-axis current injection in reduced DC-link capacitor system," *IECON Proceedings Industrial Electronics Conference,* pp. 2737-2742, 2016.

[14] M. Hosseinzadeh, S. Member, F. R. Salmasi, and S. Member, "Robust Optimal Power Management System for a Hybrid AC / DC Micro-Grid," *IEEE Transactions on Sustainable Energy,* vol. 6, pp. 675-687, 2015.

[15] A. A. A. Radwan and Y. A. R. I. Mohamed, "Improved Vector Control Strategy for Current-Source Converters Connected to Very Weak Grids," *IEEE Transactions on Power Systems,* vol. 31, pp. 3238-3248, 2016.

[16] D. Committee, "IEEE Guide for Planning DC Links Terminating at AC Locations Having Low Short-Circuit Capacities," 2003.

[17] A. Egea-alvarez, G. S. Member, and S. Fekriasl, "Advanced Vector Control for Voltage Source Converters Connected to Weak Grids," *IEEE Transactions on Power Systems,* vol. 30, pp. 3072-3081, 2015.

[18] F. Rahman, M. A. Baseer, and S. Rehman, "Assessment of Electricity Storage Systems," in *Solar Energy Storage*, ed: Elsevier Ltd., 2015, pp. 63-114.

[19] (2018). *Sources of Greenhouse Gas Emissions*.

[20] "Global Energy Review 2020," Paris, 2020, p. 56: international energy agency (IEA).

[21] C. W. Taylor and D. C. Erickson, "Recording and analyzing the July 2 cascading outage [Western USA power system]," in IEEE Computer Applications in Power, vol. 10, no. 1, pp. 26-30, Jan. 1997.

[22] D. N. Kosterev, C. W. Taylor, and W. A. Mittelstadt, "Model validation for the august 10,1996 wscc system outage," *IEEE Transactions on Power Systems,* vol. 14, pp. 967-979, 1999.

[23] J. A. Momoh, S. Meliopoulos, and R. Saint, "Centralized and Distributed Generated Power Systems - A Comparison Approach: Future Grid Initiative White Paper," 2012.

[24] J. M. Carrasco *et al.*, "Power-electronic systems for the grid integration of renewable energy sources: A survey," *IEEE Transactions on Industrial Electronics,* vol. 53, pp. 1002-1016, 2006.

[25] J. M. Guerrero, M. Chandorkar, T. L. Lee, and P. C. Loh, "Advanced control architectures for intelligent microgridspart i: Decentralized and hierarchical control," *IEEE Transactions on Industrial Electronics,* vol. 60, pp. 1254-1262, 2013.

[26] K. Boutros, R. Chu, and B. Hughes, "Recent advances in GaN power electronics," in *Proceedings of the Custom Integrated Circuits Conference*, ed. San Jose, CA, 2013, 2013, pp. 1-4.

[27] A. Yazdani and R. Iravani, Voltage-Sourced Converters in Power Systems. New York, NY, USA: Wiley, 2010.

[28] B. Jayant Baliga, "Trends in power semiconductor devices," *IEEE Transactions on Electron Devices,* vol. 43, pp. 1717-1731, 1996.

[29] K. Satoh and M. Yamamoto, "The Present State of the Art in High-Power Semiconductor Dvices," *Proceedings of the IEEE,* vol. 89, pp. 813-820, 2001.

[30] S. Saddow and A. Agarwal, Advances in Silicon Carbide Processing and Applications: Semiconductor Materials and Devices Series. Norwood, MA: Artech House, 2004

[31] M. Hiller, R. Sommer, and M. Beuermann, "Converter topologies and power semiconductors for industrial medium voltage converters," *Conference Record - IAS Annual Meeting (IEEE Industry Applications Society),* pp. 1-8, 2008.

[32] ABB, "Switching the subject," Zürich, Switzerland, 2016, p. 5.

[33] S. Bernet, R. Teichmann, S. Member, A. Zuckerberger, and P. K. Steimer, "Comparison of High-Power IGBT ' s and Hard-Driven GTO ' s for High-Power Inverters," vol. 35, pp. 487-495, 1999.

[34] F. Filsecker, R. Alvarez, and S. Bernet, "Comparison of 4.5-kV press-pack IGBTs and IGCTs for medium-voltage converters," *IEEE Transactions on Industrial Electronics,* vol. 60, pp. 440-449, 2013.

[35] ABB, "Applying IGBTs," Zürich, Switzerland, 2013, p. 22.

[36] ABB, "Applying IGCTs," Zürich, Switzerland, 2016, p. 23.

[37] H. S. J. Lutz, U. Scheuermann, and R. W. De Doncker, "Semiconductor Power Devices Physics, Characteristics, Reliability," 2011.

[38] R. Ramshaw, *Power Electronics Semiconductor Switches*, 2nd ed. London, U.K., 1993.

[39] B. K. Bose, *Power Electronics and Motor Drives: Advances and Trends*. Amsterdam: Elsevier/Academic Press, 2006.

[40] P. Li, S. J. Finney and D. Holliday, "Grid-connection of active-forced-commutated bridge: Power quality and DC fault protection," IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society, Beijing, 2017, pp. 1192-1197.

[41] A. J. Humphrey, "Inverter Commutation Circuits," *IEEE Trans. Ind. Gen. Appl,* vol. 4, pp. 104-110, 1968.

[42] M. H. Rashid, *Power Electronics Handbook*, 4th ed. ed. San Diego, CA: Academic Press Series in Engineering, 2001.

[43] ABB, "Introduction to Microgrids."

[44] S. Lamichhane, H. Nazaripouya, and S. Mehraeen, "Micro grid stability improvements by employing storage," *IEEE Green Technologies Conference,* pp. 250-258, 2013.

[45] R. Majumder, "Modeling , Stability Analysis and Control of Microgrid," ed, 2010.

[46] M. S. Sadabadi, Q. Shafiee, S. Member, and A. Karimi, "Plug-and-Play Robust Voltage Control of DC Microgrids," *IEEE Transactions on Smart Grid,* vol. 9, pp. 6886-6896, 2018.

[47] B. T. Patterson, "DC, Come Home: DC Microgrids and the Birth of the "Enernet"," *IEEE Power and Energy Magazine,* vol. 10, pp. 60-69, 2012.

[48] J. Rodriguez, S. Member, S. Bernet, P. K. Steimer, and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," vol. 57, pp. 2219-2230, 2010.

[49] J. Dai, D. Xu, and B. Wu, "A novel control system for current source converter based variable speed PM wind power generators," *PESC Record - IEEE Annual Power Electronics Specialists Conference,* pp. 1852-1857, 2007.

[50] B. Wu and M. Narimani, "Current Source Inverter Fed Drives," in *High-Power Converters and AC Drives*, ed: IEEE, 2017.

[51] B. Wu and M. Narimani, "PWM Current Source Rectifiers," in *High-Power Converters and AC Drives*, ed: IEEE, 2017.

[52] M. Morawiec and Z. Krzeminski, "The Electrical Drive Systems with the Current Source Converter," *Power Electronics for Renewable Energy Systems, Transportation and Industrial Applications,* vol. 9781118634, pp. 630-663, 2014.

[53] H. A. Alsiraji, "Cooperative Power Sharing control in Multi- terminal VSC-HVDC," ed, 2014, pp. 1-86.

[54] D. G. H. a. T. A. Lipo, "Pulse Width Modulation for Power Converters: Principles and Practice," 2003.

[55] M. C. Chandorkar, D. M. Divan, and R. Adapa, "Control of parallel connected inverters in standalone ac supply systems," *IEEE Transactions on Industry Applications,* vol. 29, pp. 136-143, 1993.

[56] L. Xu, D. Zhi, and L. Yao, "Direct power control of grid connected voltage source converters," *2007 IEEE Power Engineering Society General Meeting, PES,* pp. 1-6, 2007.

[57] M. Malinowski, M. Jasiński, and M. P. Kazmierkowski, "Simple direct power control of three-phase PWM rectifier using space-vector modulation (DPC-SVM)," *IEEE Transactions on Industrial Electronics,* vol. 51, pp. 447-454, 2004.

[58] T. Noguchi, H. Tomiki, S. Kondo, and I. Takahashi, "Direct power control of PWM converter without power-source voltage sensors," *IEEE Transactions on Industry Applications,* vol. 34, pp. 473-479, 1998.

[59] Y. Gui, X. Wang, and F. Blaabjerg, "Vector Current Control Derived from Direct Power Control for Grid-Connected Inverters," *IEEE Transactions on Power Electronics,* vol. 34, pp. 9224-9235, 2019.

[60] J. Dannehl, C. Wessels, and F. W. Fuchs, "Limitations of voltage-oriented PI current control of grid-connected PWM rectifiers with LCL filters," *IEEE Transactions on Industrial Electronics,* vol. 56, pp. 380-388, 2009.

[61] W. Zahoor and S. H. Zaidi, "Synchronization and dq current control of grid-connected voltage source inverter," *17th IEEE International Multi Topic Conference: Collaborative and Sustainable Development of Technologies, IEEE INMIC 2014 - Proceedings,* pp. 462-466, 2015.

[62] S. A. Khajehoddin, M. Karimi-Ghartemani, P. K. Jain, and A. Bakhshai, "A control design approach for three-phase grid-connected renewable energy resources," *IEEE Transactions on Sustainable Energy,* vol. 2, pp. 423-432, 2011.

[63] D. N. Zmood and D. G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady-state error," *IEEE Transactions on Power Electronics,* vol. 18, pp. 814-822, 2003.

[64] A. Yazdani and R. Iravani, "Grid-Imposed Frequency VSC System: Control in -Frame," in *Voltage-Sourced Converters in Power Systems: Modeling, Control, and Applications*, ed: IEEE, 2010, p. 1.

[65] M. P. Kazmierkowski and L. Malesani, "Current control techniques for three-phase voltage-source PWM\nconverters: a survey," *IEEE Transactions on Industrial Electronics,* vol. 45, pp. 691-703, 1998.

[66] J. Xu, S. Xie, and T. Tang, "Evaluations of current control in weak grid case for grid-connected LCL-filtered inverter," *IET Power Electronics,* vol. 6, pp. 227-234, 2013.

[67] M. K. Bakhshizadeh *et al.*, "Couplings in Phase Domain Impedance Modeling of Grid-Connected Converters," *IEEE Transactions on Power Electronics,* vol. 31, pp. 6792-6796, 2016.

[68] Z. Ali, N. Christofides, L. Hadjidemetriou, E. Kyriakides, Y. Yang, and F. Blaabjerg, "Three-phase phase-locked loop synchronization algorithms for grid-connected renewable energy systems: A review," *Renewable and Sustainable Energy Reviews,* vol. 90, pp. 434-452, 2018.

[69] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Transactions on Industrial Electronics,* vol. 53, pp. 1398-1409, 2006.

[70] Z. Lidong, L. Harnefors, and H. P. Nee, "Power-Synchronization Control of Grid-Connected," *IEEE Transactions on Power Systems, Power Systems, IEEE Transactions on, IEEE Trans. Power Syst.,* vol. 25, no. 2, pp. 809-820, 2010.

[71] H. Guan-Chyun and J. C. Hung, "Phase-Locked Loop Techniques-A Survey," *IEEE Transactions on Industrial Electronics, Industrial Electronics, IEEE Transactions on, IEEE Trans. Ind. Electron.,* vol. 43, no. 6, pp. 609-615, 1996.

[72] A. Nicastri and A. Nagliero, "Comparison and evaluation of the PLL techniques for the design of the grid-connected inverter systems," *IEEE International Symposium on Industrial Electronics,* pp. 3865-3870, 2010.

[73] B. Wen, D. Boroyevich, R. Burgos, P. Mattavelli, and Z. Shen, "Analysis of D-Q Small-Signal Impedance of Grid-Tied Inverters," *IEEE Transactions on Power Electronics,* vol. 31, pp. 675-687, 2016.

[74] Y. W. Li, "Control and resonance damping of voltage-source and current-source converters with LC filters," *IEEE Transactions on Industrial Electronics,* vol. 56, pp. 1511-1521, 2009.

[75] E. P. Wiechmann, P. Aqueveque, R. Burgos, and J. Rodriguez, "On the efficiency of voltage source and current source inverters for high-power drives," *IEEE Transactions on Industrial Electronics,* vol. 55, pp. 1771-1782, 2008.

[76] A. VanderMeulen and J. Maurin, "Current source inverter vs. voltage source inverter topology," *Technical Data TD02004004E, Eaton,* pp. 1-8, 2010.

[77] W. Zheng, W. Bin, X. Dewei, and N. R. Zargari, "A Current-Source-Converter-Based High-Power Switching Frequency," *IEEE Transactions on Industrial Electronics, Industrial Electronics, IEEE Transactions on, IEEE Trans. Ind. Electron,* vol. 59, no. 7, pp. 2970-2981, 2012.

[78] A. Rodríguez, F. Huerta, E. J. Bueno, and F. J. Rodríguez, "Analysis and performance comparison of different power conditioning systems for smes-based energy systems in wind turbines," *Energies,* vol. 6, pp. 1527-1553, 2013.

[79] M. Davari and Y. A.-R. I. Mohamed, "Dynamics and Robust Control of a Grid-Connected VSC in Multiterminal DC Grids Considering the Instantaneous Power of DC- and AC-Side Filters and DC Grid Uncertainty," *IEEE Transactions on Power Electronics,* vol. 31, pp. 1942-1958, 2016.

[80] W. J. Lee and S. K. Sul, "DC-link voltage stabilization for reduced DC-link capacitor inverter," *IEEE Transactions on Industry Applications,* vol. 50, pp. 404-414, 2014.

[81] M. E. De Oliveira Filho, J. R. Gazoli, A. J. S. Filho, and E. R. Filho, "A control method for voltage source inverter without dc link capacitor," *PESC Record - IEEE Annual Power Electronics Specialists Conference,* pp. 4432-4437, 2008.

[82] A. Adib, B. Mirafzal, X. Wang, and R. Blaabjerg, "On stability of voltage source inverters in weak grids," *IEEE Access,* vol. 6, pp. 4427-4439, 2017.

[83] Y. Huang, X. Yuan, and J. Hu, "Effect of reactive power control on stability of DC-link voltage control in VSC connected to weak grid," *IEEE Power and Energy Society General Meeting,* vol. 2014-Octob, pp. 1-5, 2014.

[84] Y. Huang, S. Member, X. Yuan, and S. Member, "Modeling of VSC Connected to Weak Grid for Stability Analysis of DC-Link Voltage Control," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 3, pp. 1193-1204, 2015.

[85] Z. Moradi-Shahrbabak and A. Tabesh, "Effects of Front-End Converter and DC-Link of a Utility-Scale PV Energy System on Dynamic Stability of a Power System," *IEEE Transactions on Industrial Electronics,* vol. 65, pp. 403-411, 2018.

[86] L. Torok, L. Mathe, C. K. Nielsen, and S. Munk-Nielsen, "Modeling and Control of Three-Phase Grid-Connected Power Supply with a Small DC-Link Capacitor for Electrolyzers," *IEEE Transactions on Industry Applications,* vol. 53, pp. 4634-4643, 2017.

[87] M. Davari and Y. A. R. I. Mohamed, "Robust Vector Control of a Very Weak-Grid-Connected Voltage-Source Converter Considering the Phase-Locked Loop Dynamics," *IEEE Transactions on Power Electronics,* vol. 32, pp. 977-994, 2017.

[88] X. Yuan, F. Wang, D. Boroyevich, R. Burgos, and Y. Li, "DC-link voltage control of a full power converter for wind generator operating in weak-grid systems," *IEEE Transactions on Power Electronics,* vol. 24, pp. 2178-2192, 2009.

[89] J. Hu, Y. Huang, D. Wang, H. Yuan, and X. Yuan, "Modeling of grid-connected DFIG-based wind turbines for dc-link voltage stability analysis," *IEEE Transactions on Sustainable Energy,* vol. 6, pp. 1325-1336, 2015.

[90] J. G. Ciezki and R. W. Ashton, "The application of feedback linearization techniques to the stabilization of DC-to-DC converters with constant power loads," in *1998 IEEE International Symposium on Circuits and Systems (ISCAS)* vol. 3, ed, 1998, pp. 526-529 vol.3.

[91] C. W. Taylor, D. Maratukulam, and N. J. Balu, *Power System Voltage Stability*. United States: McGraw-Hill, 1994.

[92] J. Sun, "Small-signal methods for AC distributed power systems-A review," *IEEE Transactions on Power Electronics,* vol. 24, pp. 2545-2554, 2009.

[93] N. Y. P. Kundur, NY, USA: McGraw-Hill,, *Power System Stability and Control*. 1994.

[94] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed ed. Norwell, MA: Kluwer, 2001.

[95] A. A. A. Radwan, Y. A.-R. I. Mohamed, and E. F. El-Saadany, "Assessment and performance evaluation of DC-side interactions of voltage-source inverters interfacing

renewable energy systems," *Sustainable Energy, Grids and Networks,* vol. 1, pp. 28-44, 2015.

[96] L. Harnefors and H. P. Nee, "Model-based current control of ac machines using the internal model control method," *IEEE Transactions on Industry Applications,* vol. 34, pp. 133-141, 1998.

[97] A. Yazdani and P. P. Dash, "A control methodology and characterization of dynamics for a photovoltaic (PV) system interfaced with a distribution network," *IEEE Transactions on Power Delivery,* vol. 24, pp. 1538-1551, 2009.

[98] W. Leonhard, *Control of electrical drives*, 3rd ed. 2001.

[99] A. Kulkarni and V. John, "Design of synchronous reference frame phase-locked loop with the presence of dc offsets in the input voltage," *IET Power Electronics,* vol. 8, pp. 2435-2443, 2015.

[100] V. Kaura, Vladimir, "Vikram Kaura,," *IEEE Transactions on Industry Applications,* vol. 33, pp. 58-63, 1997.

[101] L. Harnefors, M. Bongiorno, and S. Lundberg, "Input-admittance calculation and shaping for controlled voltage-source converters," *IEEE Transactions on Industrial Electronics,* vol. 54, pp. 3323-3334, 2007.

[102] D. Rowell, " State-space representation of LTI systems," MIT, Cambridge2002, Available: http://web.mit.edu/214/www/Handouts/StateSpace.pdf.

Appendix A.2

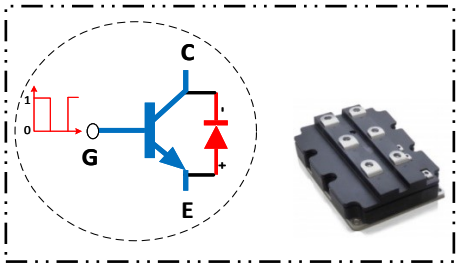


Figure A.2.1 IGBT with antiparallel deiod (switching cell) of VSC.

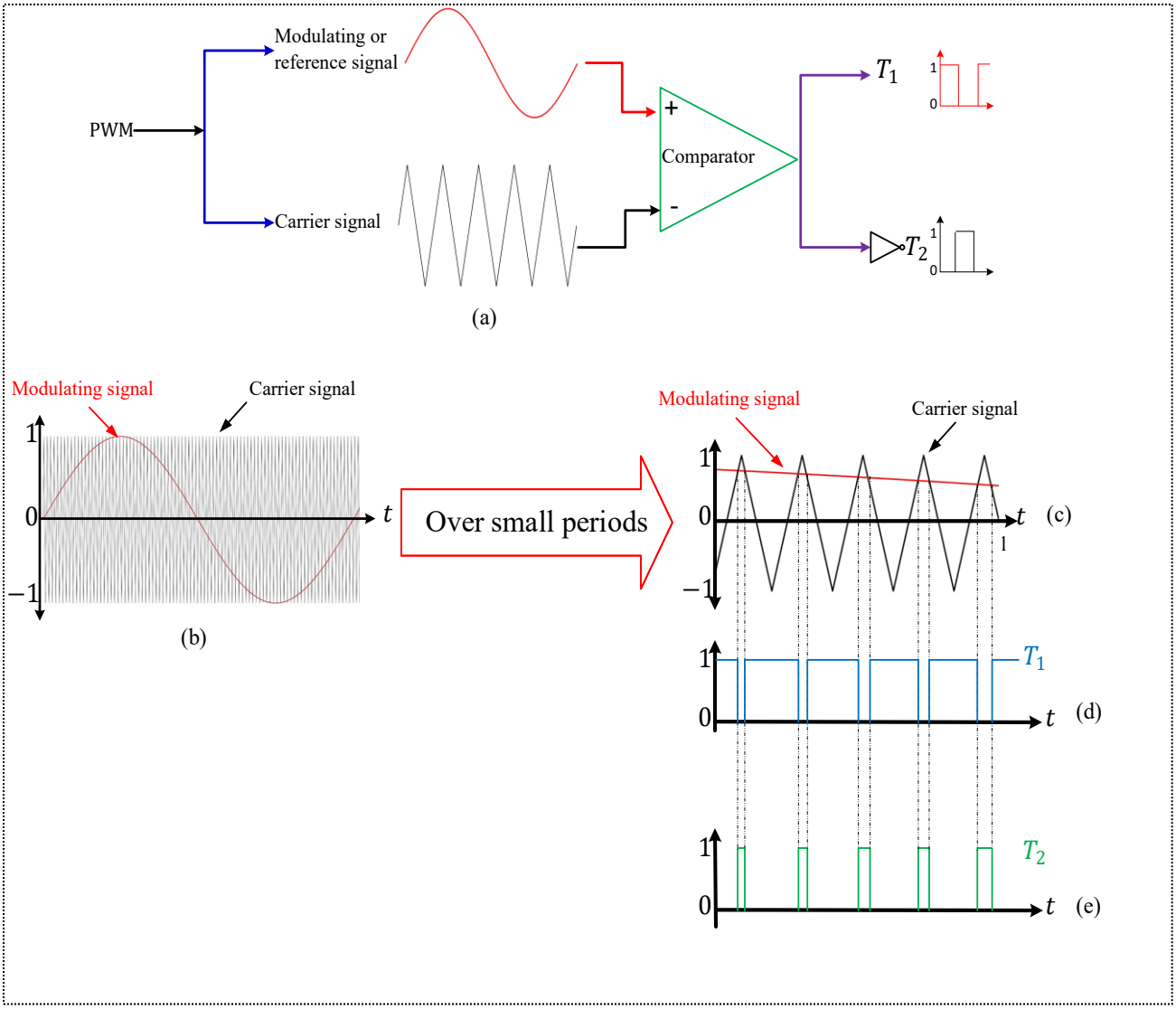


Figure A.2.2 a) Mechanism of PWM to generate gating signals for switches T_1 and T_2, b) high frequency carrier signal and low frequency modulating signal, c) short periods of both signals captured from (b), d & e) switching pattern of switches T_1 and T_2

$$\begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} = 0.667 \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x_a(t) \\ x_b(t) \\ x_c(t) \end{bmatrix} \quad \text{(A.2.1)}$$

$$\begin{bmatrix} x_d(t) \\ x_q(t) \end{bmatrix} = 0.667 \begin{bmatrix} cos\ \theta(t) & cos\ [\theta(t) - 120] & cos\ [\theta(t) - 240] \\ sin\ \theta(t) & sin\ [\theta(t) - 120] & sin\ [\theta(t) - 240] \end{bmatrix} \begin{bmatrix} x_a(t) \\ x_b(t) \\ x_c(t) \end{bmatrix} \quad \text{(A.2.2)}$$

$$\begin{bmatrix} x_d(t) \\ x_q(t) \end{bmatrix} = \begin{bmatrix} \cos\ \theta(t) & -\sin\ \theta(t) \\ -\sin\ \theta(t) & \cos\ \theta(t) \end{bmatrix} \begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} \quad \text{(A.2.3)}$$

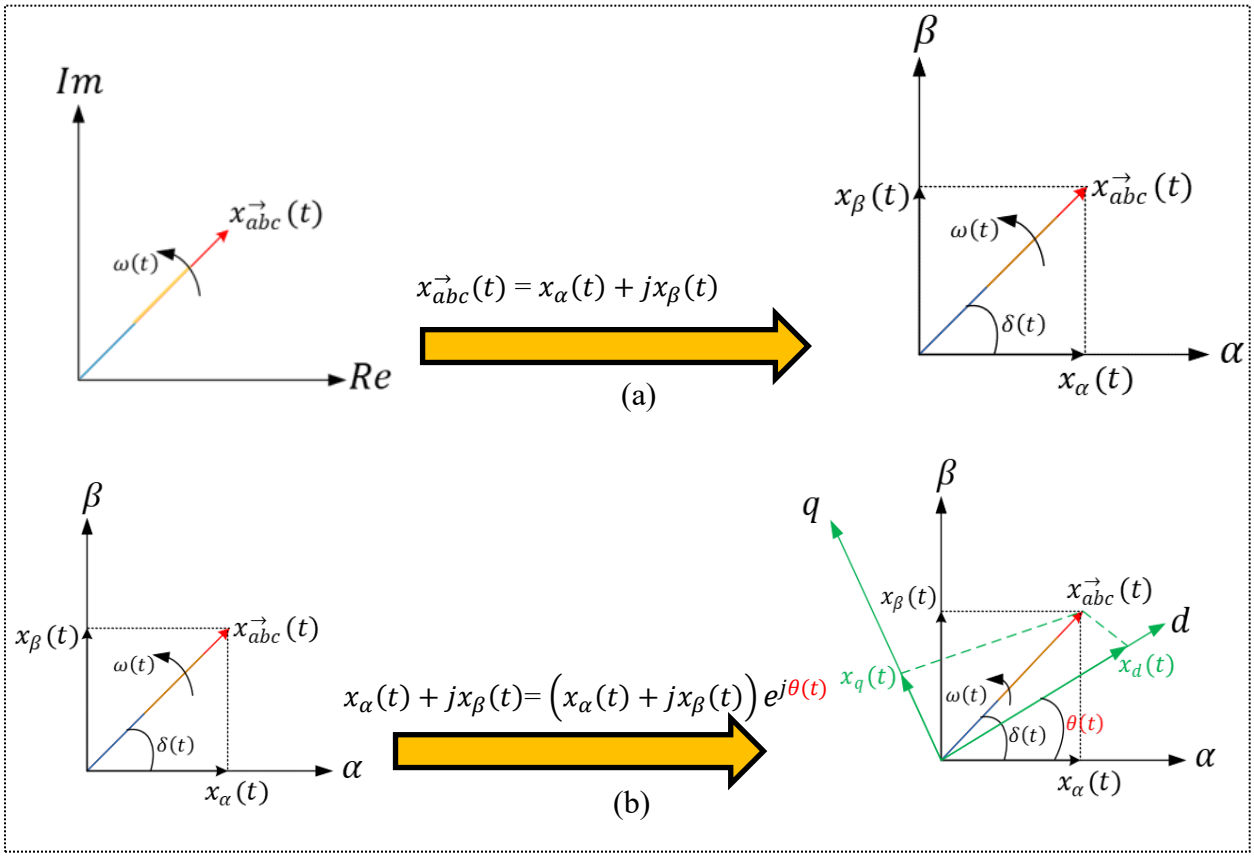


Figure A.2.3 Three-phase components represented by two reference frames: a) stationary frame ($\alpha\beta$), and b) synchronous reference frame.

Figure A.2.3 (a) shows the stationary reference frame representation that results in AC voltage variable quantities due to the converted space vector ($\vec{x}_{abc}(t)$) rotating over fixed frames ($x_\beta(t)$ and $x_\alpha(t)$); whereas Fig A.2.3 (b) shows the rotating reference frame that results in constant quantities (DC components) due to the frames ($x_d(t)$ and $x_q(t)$) rotating relatively at the same speed as the space vector, making the projected vector seem constant. This can be achieved through accurate synchronization with angle ($\theta(t)$) as clarify in Fig. A.2.3 (b).

Appendix A.3

A.3.1) Compensating for V_{odq}^{g} in controller model by $V_{o1}\Delta I_{dq}^{g} + V_{o2}\Delta I_{gdq}^{g}$ in power circuit model, the new B_{Cont} and D_{Cont} is giving as following:

$B_{\overline{Cont}}=$

$$\left[\underbrace{\begin{pmatrix} B_{v1} \\ B_{cc1}D_{v1} \\ 0_{2\times1} \end{pmatrix}}_{B_{Cont1}} \quad \underbrace{\begin{pmatrix} ([B_{v2} \quad 0_{2\times1}]T_{vo1})V_{o2} \\ ([B_{cc1}D_{v2} \quad 0_{2\times1}]T_{vo1})V_{o2} \\ B_{ll}T_{vo1}V_{o2} \end{pmatrix}}_{B_{\overline{Cont2}}} \quad \underbrace{\begin{pmatrix} B_{v3} \\ B_{cc1}D_{v3} \\ 0_{2\times1} \end{pmatrix}}_{B_{Cont3}} \quad \underbrace{\begin{pmatrix} B_{v4} \\ B_{cc1}D_{v4} \\ 0_{2\times1} \end{pmatrix}}_{B_{Cont4}} \quad \underbrace{\begin{pmatrix} ([B_{v2} \quad 0_{2\times1}]T_{vo1})V_{o1} \\ B_{cc2}T_{i1} + ([B_{cc1}D_{v2} \quad 0_{2\times1}]T_{vo1})V_{o1} \\ B_{ll}T_{vo1}V_{o1} \end{pmatrix}}_{B_{\overline{Cont5}}}\right]$$

$D_{\overline{Cont}}=$

$$\left[\underbrace{T_{v1}^{-1}D_{cc2}D_{v1}}_{D_{cont1}} \quad \underbrace{T_{v1}^{-1}(([D_{cc2}D_{v2} \quad 0_{2\times1}]_{2\times2} + D_{cc3})T_{vo2})V_{o2})}_{D_{\overline{cont2}}} \quad \underbrace{T_{v1}^{-1}D_{cc2}D_{v3}}_{D_{cont3}} \quad \underbrace{T_{v1}^{-1}D_{cc2}D_{v4}}_{D_{cont4}} \quad \underbrace{T_{v1}^{-1}((D_{cc1}T_{i1}[D_{cc2}D_{v2} \quad 0_{2\times1}]_{2\times2} + D_{cc3})T_{vo1})V_{o1})}_{D_{\overline{cont5}}}\right]_{2\times6}$$

A.3.2) Mathematical transformation from state-space model to impedance model:

Based on the general form of state-space model:

$$\Delta\dot{\boldsymbol{x}} = \boldsymbol{A}\,\Delta\boldsymbol{x} + \boldsymbol{B}\Delta$$

$$\Delta\boldsymbol{y} = \boldsymbol{C}\,\Delta\boldsymbol{x} + \boldsymbol{D}\Delta\boldsymbol{u}$$

Taking Laplace transforms ($\mathscr{L}\{f\}$) of the above equations and conducting algebraic manipulation, the general formula for converting state-space model to transfer function is as follows:

$$\frac{Y(s)}{U(s)} = [\boldsymbol{C}(s\boldsymbol{I_n} - \boldsymbol{A})^{-1}\boldsymbol{B} + \boldsymbol{D}]$$

Appendix A.4

A.4.1) The Effect of DC-link Capacitance Uncertainty on Different Grid Strength Conditions

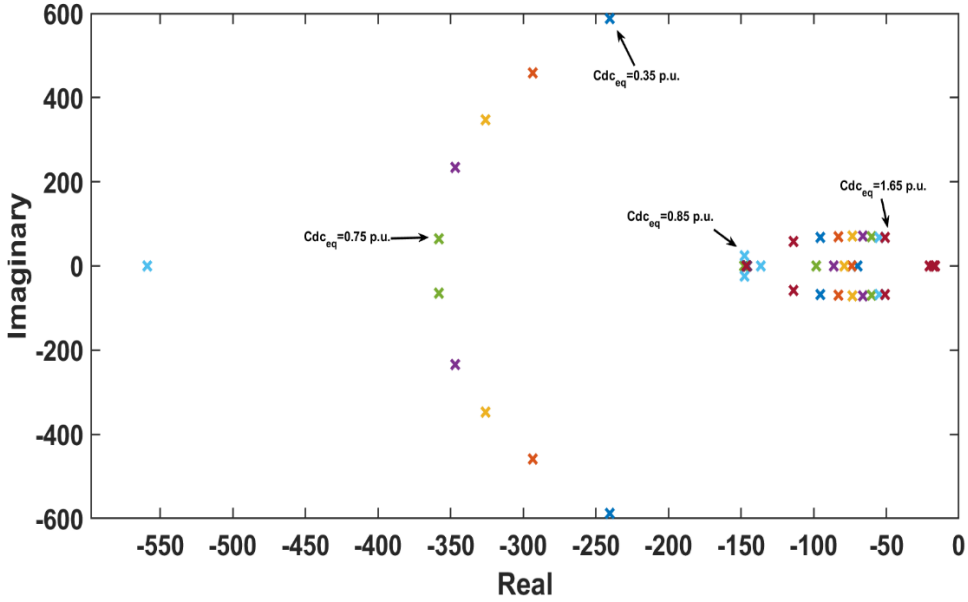


Figure A.4.1 Eigenvalues of the grid-connected VSC system at *SCR*= 10 with varying DC-link capacitance between 0.35 and 1.65 pu in rectification mode.

A.4.2) Plot that Shows the Interactions Dynamics Between BW_{cc} and φ_{dc} in The Study that has been Conducted in [84].

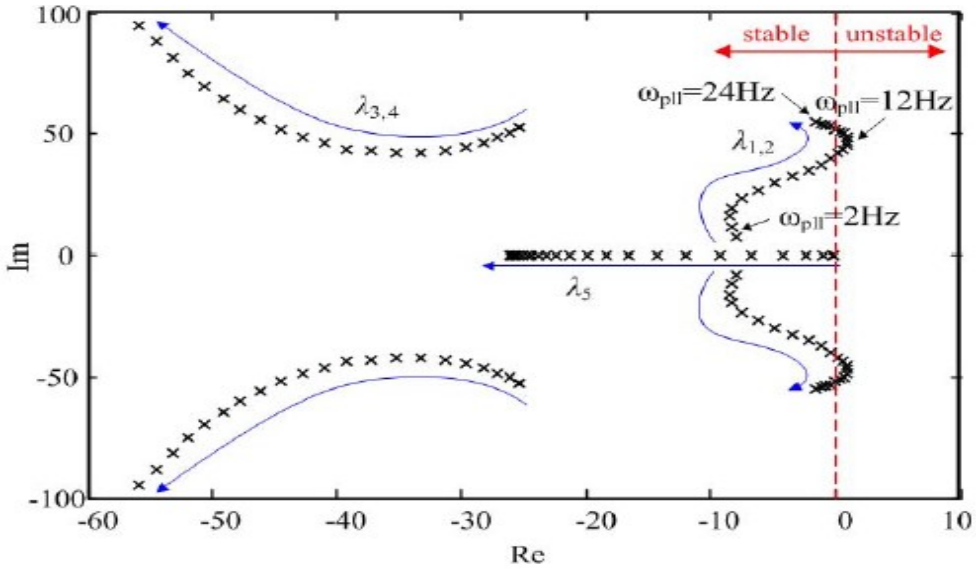


Figure A.4.2 “Fig. 11. Stability analysis of dc-link voltage control with varying PLL bandwidths”.

In [84] the dc-link voltage control is set to 10 Hz. It is clear from Fig. A.4.2 when the bandwidth of PLL close to 10 Hz the system stability reaches to the worse case.