Real-Time Device-level Modeling of Power Converters for Advanced Transportation Application

by

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Abstract

The advance of the transportation system has helped human beings to change their standard of living dramatically through the facilitation of trade, travel and exchange in both time and energy-efficient way. The modern transportation system consists of a complex multi-domain system: electrical, mechanical, hydraulic, thermal, multi-body dynamics, etc. Among these systems, the electrical system is considered as the most critical one, that can provide conditioned and reliable power to essential loads for the other physical systems. Thus, emulating the detailed electrical system accurately in real-time can help engineers and scientists to predict and control the whole transportation system dynamics efficiently, which can be extended to the application of repeatedly evaluating the newly designed power switch, protection circuit and algorithm, power converter and controller for design optimization and tuning in a non-destructive emulation environment. There is a demanding need for accurate detailed device-level modeling in real-time hardware-in-the-loop (HIL) emulation, especially under extreme and extensive range of conditions for advanced transportation application. These electrical system devices come in many shapes and sizes and often have to connect and correlate with many other devices inside the electrified transportation system. Discrete-time solution of a complete topology of the equivalent represented nonlinear circuit model can provide the detailed device dynamics with iteration calculation. However, these developed analytical and numerical models lead to the heavy computational burden of the real-time capable hardware, which introduces extra execution time-delay and makes real-time problem-solving infeasible.

Introducing model order reduction methods and implementing these methods in dedicated real-time capable hardware are common techniques for reducing the computational complexity of mathematical models and shortening the model execution delay time to the nanosecond-level timing margin. Based on the common nonlinear system identification method, block-structured behavioral models, such as Hammerstein, Wiener-Hammerstein configuration, are introduced as the first model order reduction methods for the simplicity of their real-time implementation in the following three chapters (3, 4, 5). Then,

hybrid kNN-RNN neural networks are introduced as the second model order reduction method for their real-time adaptive features of deviated parasitic parameters in Chapter 6. These methods require both highly sequential clocking and massive parallel structure in problem-solving. By utilizing state-of-the-art hardware platforms of multi-processing system-on-chip (MPSoC) or field programmable gate array (FPGA), both system-level and device-level transients were captured in real-time, which is also the first time of deploying the block-structured and neural network models on state-of-the-art System-on-Chip (SoC) and FPGA hardware platform for nanosecond-level real-time device-level power electronic converter emulation.

Practical advanced transportation applications have also been investigated in the thesis, including three-phase self-balancing traction power system, massive existing Beijing-Shanghai AC high speed rail (HSR) traction system, future medium voltage DC traction network, and electromagnetic rail gun (EMRG) in all electrical ship (AES) system. With the anticipated increasing demand placed on the land, sea, and air, these above mentioned novel transportation model can be installed, constructed, and testified repeatedly by the proposed real-time device-level modeling scheme.

Preface

The material presented in this thesis is based on original work by Tian Liang. As detailed in the following, material from some chapters of this thesis has been published as journal articles under the supervision of Dr. Venkata Dinavahi in concept formation and by providing comments and corrections to the article manuscript.

Chapter 3 includes the results from the following paper:

- T. Liang and V. Dinavahi, "Real-time system-on-chip emulation of electro-thermal models for power electronic devices via Hammerstein configuration," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 1, pp. 203–218, Mar. 2018.

Chapter 4 includes the results from the following paper:

- T. Liang and V. Dinavahi, "Real-time device-level simulation of MMC-based MVDC traction power system on MPSoC," *IEEE Trans. Transp. Electrific.*, vol. 4, no. 2, pp. 626–641, Jun. 2018.

Chapter 5 includes the results from the following paper:

- T. Liang, Q. Liu and V. Dinavahi, "Detailed Real-Time HIL Emulation of High-Speed Rail Power System with SiC-Based MMC," *Under revision in IEEE Trans. Ind. Electron*, pp. 1–11, Dec. 2019.

Chapter 6 includes the results from the following papers:

- T. Liang, Z. Huang and V. Dinavahi, "Adaptive real-time hybrid neural network based device-level modeling for DC traction drive," *Under revision in IEEE Access*, pp. 1–13, Nov. 2019.

To my parents

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List of Acronyms

AC	Alternating Current
APU	Application Processing Unit
ASIC	Application Specific Integrated Circuit
AXI	Advanced eXtensible Interface
BLM	Bergeron Line Model
BRAM	Block Random Access Memory
CC	Charging Circuit
CLB	Configurable Logic Blocks
CPU	Central Processing Unit
DAC	Digital to Analog Converter
DSP	Digital Signal Processing (Processor)
EMRG	Electro-Magnetic Rail-Gun
EMT	Electro-Magnetic Transient
FBSM	Full-Bridge Sub-Module
FF	Flip-Flop
FFT	Fast Fourier Transform
FMC	FPGA Mezzanine Card
FPGA	Field-Programmable Gate Array
FPU	Floating Point Unit
FSM	Finite State Machine
GPIO	General Purpose IO
GPU	Graphical Processing Unit
GT	Gigabit Transceiver
HBSM	Half-Bridge Sub-Module
HCM	Hammerstein Configuration Model
HIL	Hardware-In-the-Loop
HLS	High-Level Synthesis
I/O	Input/Output
IGBT	Insulated Gate Bipolar Transistor
JTAG	Joint Test Action Group
LUT	Look-up Table
MMC	Modular Multi-Level Converter
MPSoC	Multi-Processor System-on-Chip
MVDC	Medium-Voltage DC
NPC	Neutral-Point-Clamped
N-R	Newton-Raphson
PD	Phase-Disposition
PFN	Pulse Forming Network

PL	Programmable Logic, Piecewise Linearization
PLL	Phase Locked Loop
PS	Processing System
PSC	Phase-Shifted Carrier
PWM	Pulse Width Modulation
QSFP	Quad Small Form-Factor Pluggable
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RPU	Real-Time Processing Unit
RTL	Register-Transfer Level
SDK	Software Development Kit
SFP	Small Form-Factor Pluggable
SM	Sub-Module
SPWM	Sinusoidal Pulse Width Modulation
TSSM	Two State Switch Model
USB	Universal Serial Bus
VHDL	Very High-Speed Integrated Circuit Hardware Description Language

1 Introduction

Computer-aided design (CAD) tools help engineers in the creation, modification, analysis, or optimization of designs in a wide range of disciplines. In power system analysis and simulation, the professional commercial software, such as SaberRD® and PSCAD/EMTDC®, provides detailed power electronics and equipment package in component library, and utilize nodal analysis and Trapezoidal rule integration for the circuit transient solution. These off-line software may apply nonlinear components in the design. However, they use piecewise linear approximation, and in certain case, Newton-Raphson iteration becomes a must to get the solution. It takes long execution delay in the off-line software, which makes it inappropriate for hardware-in-the-loop (HIL) application.

Commonly, model simplification and hardware execution optimization are the efficient ways to shorten the delay in the HIL study case. For example, in power electronics, the model computation complexity varies widely based on the model selection. Generally, the system-level model requires less computing power than the device-level model. In the specific application, the device-level power electronic models, which is non-real-time in off-line software, has a non-negligible impact on the HIL design. Thus, there is a need to develop the real-time device-level power electronic model. The HIL execution hardware also plays an essential role in computation optimization. Massively parallel execution hardware, such as graphics processing unit (GPU) and field programmable gate array (FPGA), is available with the fast development of semiconductor and microelectronic technology. With proper system separation, the subsystem circuit solution can be calculated in parallel structure and the delay time can be shortened enormously.

Even though the parallel compute hardware can accelerate the parallelized program to some extent, several device-level models desire both high operating frequency of sequential and parallelized execution hardware to meet the real-time requirement. In each

time-step, the GPU needs to communicate with the CPU for next iteration information, which takes several microseconds. For the device-level model, the time-step is set to several hundred nanoseconds which make GPU unusable in device-level HIL application. FPGA can be utilized for massively parallel computation but operate at low frequency in practical application (around 100MHz). The Xilinx® Zynq® Ultrascale+™ multi processing system-on-chip (MPSoC) combines high operating frequency ARM® cores, Mali GPU and FPGA resource into one single chip. The communication time between the heterogeneous execution hardware is shortened into several hundred nanoseconds while the communication mechanism is optimized with dedicated protocol, which makes real-time device-level power electronic model applicable in practical HIL hardware.

Meanwhile, rapid urbanization demands ultra-efficient transportation in practice. Before the implementation of the project, device-level HIL emulation can reduce the manufacturing cost by selecting cost-effective power modules and verify the design in a non-destructive environment repetitively. In this report, the study cases are carefully selected for the optimized hardware execution of real-time device-level power electronic modeling for advanced transportation applications.

1.1 Background

1.1.1 Device-Level Modeling of Power Electronics

Various system-level and device-level power electronic models have been utilized in modeling and simulation of power converters and network behavior. The performance of the models has been a vital issue for selecting the appropriate model for a specific application. The system-level power electronic model can be mainly categorized into three types: 1) ideal model [1], 2) switching function model [2], 3) averaged model [3]. The ideal model employs on and off state resistances for simulation. The switching function model describes the behavior of the converter by controlled voltage and current sources. The averaged model considers the average behavior of the system while ignoring the switching behavior. In general, the averaged model consumes less compute power than the rest with less accuracy while the ideal model costs the most compute power with higher precision.

In the literature, the following device-level power electronic models have been utilized in circuit simulation: 1) analytical model [4] - [9], 2) behavioral model [10] - [16], 3) numerical model [17], [18], 4) hybrid model [19]. The analytical model, which could accurately describe the device steady-state and transient operation is based on device physics. The behavioral model provides a good prediction of device performance while ignoring the detailed physical characteristics. The numerical model can simulate the device electrical, thermal and optical characteristics by using the finite element method (FEM) without fabricating the physical device, however, it is prohibitively time-consuming. The hybrid model combines the accelerated physics-based calculation of the analytical model, low computa-

tional consumption of the behavioral model and the accurate geometrical properties of the numerical model. In general, behavioral models are the fastest and require least computation resources while the rest of the models are expected to be both resource and execution time intensive.

Both the Hammerstein and the Wiener models are utilized in common behavioral models for various applications. The single Hammerstein model contains a nonlinear static block and a linear time-invariant (LTI) dynamic block, which can not represent the exact prerequisites for physical processes. With the help of Wiener-Hammerstein structure, the proposed models can present the exact carrier charge processes before the turn-on and turn-off switching transient of the IGBT.

With the development of artificial intelligence concepts for decades, applying an appropriate neural network for device-level power electronic modeling can also help to reduce calculation latency for solving the reasonably large application circuits. Several types of ANNs have been investigated for device transient emulation: 1) multi-layer perceptron (MLP) [20], 2) Radial-basis function (RBF) [21], 3) time-delay neural network (TDNN) [22], and 4) recurrent neural network (RNN) [23].

1.1.2 Advanced Transportation Application

High-speed rail (HSR) delivers fast, efficient, and reliable transportation in all weather conditions, fosters economic development in second-tier cities along train routes, links cities together into integrated regions that can then function as a single stronger economy, broadens labor markets and offers workers a wider network of employers to choose from. The future HSR system relies on high efficiency, operating temperature and switching frequency next-generation power semiconductor. The invention of the silicon (Si) power device inexorably paved the way for the modern HSR era. Silicon carbide (SiC) and gallium nitride (GaN), both wide bandgap (WBG) semiconductors, have emerged as the front-running solutions to the slow-down in silicon in the high power, high-temperature segments [24]. The SiC characteristic enables dramatic reductions in conductivity and switching loss and prevents the flow of leakage current at high temperature. Innovative SiC power module may lead the way of advanced HSR transportation for a low-carbon sustainable future.

Oceanic industries desire high speed and reliability, and low lifespan cost and environmental impact shipping for transportation. Compared to highly congested land shipment and high-cost air freight, all electric ship (AES) can reduce the lifespan energy consumption and transport huge volume of freight at a lower rate. The medium voltage DC (MVDC) topology has been proposed and recommended for AES in IEEE standard. The main merits of MVDC system can be listed as follow: 1) reduction of bulky ferromagnetic transformers, 2) simplified parallel connection or disconnection for dc power sources, 3) elimination of harmonic, imbalance and synchronization problems, and reactive power

flow control compared with its AC counterpart. The possibility to reduce the fuel consumption (by implementing variable-speed diesel generators) and to cut down the power system volume and weight become the main drivers attracting investments in this research field. In the meantime, the long-existing bottleneck of MVDC system power electronic apparatus has been alleviated to a great extent as the performance and ability of power electronic technology are ongoing increasing at a remarkable rate. The MVDC power system is deemed as a promising next-generation technology in AES application.

1.2 Literature Review

This section provides the literature review of the several common system identification methods and the simulation hardware, which are beneficial for the understanding of the proposed real-time device-level power electronic emulation schemes in the dedicated hardware.

1.2.1 Nonlinear System Identification

System identification, which identifies the dynamic model of an unknown system, has become an essential topic across an extensive range of real systems and processes. The applications of which cover any system where the inputs and outputs can be measured, including industrial processes, control systems, economic data and financial systems, biology and the life sciences, medicine, social systems, etc.

Nonlinearity is considered as the key feature in any physical system which hardly satisfied with the superposition principle of any linear approximation. Thus, there is a need to make reasonable assumptions in some aspects to simplify the modeling procedures for enabling their high-efficiency executability.

1. **State-Space Model:** In both the discrete-time and continuous-time domains, state-space models are often used where all the states can be observed or estimated, and have the advantage that some state variables may be directly related to measurable system variables. Representing the most generic representations for dynamical systems, state-space models can be linear or nonlinear, time-invariant or time-varying ones. However, every coin has two sides. One of the advantages of the state-space model is that some of the state variables may represent physical variables in the system under study while the disadvantage is that all the states need to be measured or estimated for a complete identification based on this model class, and this can be very challenging, especially when encountering the nonlinear system. The most general state-space representation of a linear system with p inputs, q outputs and n state variables is written in the following form:

$$\dot{x}(t) = A(t)x(t) + B(t)u(t), \tag{1.1}$$

$$y(t) = C(t)x(t) + D(t)u(t), \tag{1.2}$$

where x, u and y are the state, input and output vector, respectively; A, B, C and D are the state, input, output, feedforward matrix, respectively [25].

2. **Piecewise Linear Model:** A nonlinear system can be approximated by a series of locally linear models, which is defined as the piecewise linear modeling method. The main motivation of the piecewise linear approach is that pre-known linear algorithms can be used to identify the models and develop control and design strategies available for linear systems. A drawback of the piecewise linear approach is that the resulting locally linear models may provide a poor approximation to the nonlinear system under study, so that simplicity in the analysis is obtained at the expense of an inadequate model. Another disadvantage and difficulty for most piecewise approaches is how to reasonably partition the system operating region, since the estimation of the piecewise models cannot be easily separated from the task of finding the domain for each sub-model [26].

3. **Volterra Series Model:** The volterra series is considered as an extension of the linear convolution integral. Early Volterra series identification algorithms assumed that just the first two, linear and quadratic terms. Volterra kernels utilized Gaussian-like white noise and correlation methods to identify the kernels. This class of model has some constraints including the necessity of knowing the certain number of Volterra series terms, the use of special inputs, and the large number of identified estimation. For example, for a system where the first order Volterra kernel is numbered as 50 samples, 50x50 points for the second order kernel, 50x50x50 for the third order, etc. Thus, the amount of data required to provide good estimates becomes excessively large. These numbers can be reduced by exploiting certain symmetries but the requirements are still excessive for the specific implementation [26].

4. **Block-Structured Model:** Block-structured models, also known as block-oriented models, are a class of nonlinear systems that can be described by connections of groups of linear dynamic and static nonlinear elements or blocks. The most well known block-structured models are the Hammerstein and Wiener models which are made of transfer functions. These types of modeling method will be explained further in the following chapters [26].

5. **Neural Network:** Neural networks are excellent candidates for predictive fitting models, but the models do not provide the transparent translation mechanism between physical parameters and the neural networks' weights and biases. In supervised learning processes, the network is trained by operating on the difference between the actual and desired output of the network, and change the connection strengths between the nodes. By several epoch of iterating, the weights and biases

are modified until the output error reaches an acceptable level. This type of model will be exploited further in Chapter 6 [26].

6. **NARMAX:** The nonlinear autoregressive moving average model with exogenous inputs (NARMAX) can represent a wide class of nonlinear systems, and is defined as

$$y(k) = F[y(k-1), ..., y(k-n_y), u(k-d), ..., u(k-d-n_u), e(k-1), ..., e(k-n_e)] + e(k), \tag{1.3}$$

where $y(k)$,$u(k)$,$e(k)$ are the system output, input, and noise sequences, respectively; n_y,n_u,n_e are the maximun lags for the system output, input, and noise; $F[]$ is some nonlinear function and d is the time delay. The Volterra series, the block structured models and many neural network architectures can all be considered as subsets of the NARMAX model [26].

1.2.2 State-of-the-Art Computation Hardware

Modern compute hardware has witnessed the changes from mechanic, electro-mechanic, analog computing, microelectronic digital processing, optical and quantum computing. Based on the specific application and the consideration of non-recurring engineering cost, today the processing system has been evolved to different branches of processors, for example, economical digital control unit, digital signal processing, power-efficient mobile application, graphic, neural network, reprogrammable device, etc. The commercially available hardware has been explored for the possibility of real-time or faster than real-time EMTP application. Some researchers have paved their way to the fundamental mathematics operations in the non-commercially available hardware, which is essential and vital for the early investigation.

1. **MCU:** A microcontroller unit (MCU), which contains one or more processor cores along with memory and programmable input/output, peripherals is a small computer on a single integrated circuit. Microcontrollers are designed for embedded applications, in contrast to the microprocessors used in personal computers or other general purpose applications consisting of various discrete chips. By reducing the size and cost compared to a design that uses a separate microprocessor, memory, and input/output devices, microcontrollers make it economical to digitally control even more devices and processes [27].

2. **DSP:** A digital signal processor (DSP) is a specialized microprocessor with its optimized architecture for the operational needs of digital signal processing. The goal of DSP is usually to measure, filter or compress continuous real-world analog signals. Most general-purpose microprocessors can also execute digital signal processing algorithms successfully, but may not be able to keep up with such processing continuously in real-time and the better power efficiency capability. Thus, they are more

suitable in portable devices such as mobile phones because of power consumption constraints [28].

3. **ARM:** ARM®, previously Advanced RISC Machine, originally Acorn RISC Machine, is a family of reduced instruction set computing architectures for computer processors. ARM® holdings develops the architecture and licenses it to the companies who design their own product include the ARM architecture for SoC and SoM, also designs cores that implement this instruction set and licenses these designs to a number of companies that incorporate those core designs into their own products. Processors that have a RISC architecture typically require fewer transistors than those with a complex instruction set computing architecture, which improves cost, power consumption, and heat dissipation. These characteristics are desirable for light, portable, battery-powered devices including smartphones, laptops and tablet computers, and other embedded systems. For supercomputers, which consume large amount of electricity, ARM® could also be a power-efficient solution [29].

4. **CPU:** Since the introduction of the first commercially available microprocessor, the Intel 4004 in 1971, and the first widely used microprocessor, the Intel 8080 in 1974, this class of central processing unit (CPU) has almost completely overtaken all other CPU implementation methods. Previous generations of CPUs were implemented as discrete components and numerous small integrated circuits (ICs) on one or more circuit boards. The overall smaller CPU size, as a result of being implemented on a single die, means faster switching time because of physical factors like decreased gate parasitic capacitance. This has allowed synchronous microprocessors to have clock rates ranging from tens of megahertz to several gigahertz [30].

5. **GPU:** A graphics processing unit (GPU) is a specialized electronic circuit designed to rapidly manipulate and alter memory to accelerate the creation of images in a frame buffer intended for output to a display device. GPUs are used in embedded systems, mobile phones, personal computers, workstations, and game consoles. Modern GPUs are very efficient at manipulating computer graphics and image processing. Their highly parallel structure makes them more efficient than general-purpose CPUs for algorithms that process large blocks of data in parallel. GPUs were initially used to accelerate the memory-intensive work of texture mapping and rendering polygons, later adding units to accelerate geometric calculations such as the rotation and translation of vertices into different coordinate systems. Because most of these computations involve matrix and vector operations, engineers and scientists have increasingly studied the use of GPUs for non-graphical calculations, especially for massively parallel problems [31].

6. **TPU:** The tensor processing unit (TPU) was announced in May 2016 at Google I/O, when the company said that the TPU had already been used inside their data centers

for over a year. The chip has been specifically designed for Google's TensorFlow framework, a symbolic math library which is used for machine learning applications such as neural networks. Compared to a GPU, it is designed for a high volume of low precision computation with higher input/output operations, and lacks hardware for rasterisation/texture mapping [32].

7. **PLD:** Programmable logic device (PLD) is a general term that refers to any type of integrated circuit used for implementing digital hardware including programmable logic array(PLA), programmable array logic (PAL), complex programmable logic device (CPLD), and field programmable gate array (FPGA), where the chips can be configured by the end user to realize different designs. PLA is a relatively small PLD that contains an programmable AND-plane and an programmable OR-plane logic while PAL is a relatively small PLD that has a programmable AND-plane followed by a fixed OR-plane logic. CPLD consists of an arrangement of multiple PLA or PAL-like blocks on a single chip. FPGA is an PLD featuring a general structure that allows very high logic capacity. Whereas CPLDs feature logic resources with a wide number of inputs (AND planes), FPGAs offer more narrow logic resources. FPGAs also offer a higher ratio of flip-flops to logic resources than do CPLDs. All these PLDs are able to conduct a massively parallel high-performance computing in nature [33]. The detailed mechanism of FPGA will be introduced in Chapter 2.

8. **FPAA:** A field-programmable analog array (FPAA) is an integrated circuit device containing computational analog blocks (CAB) and interconnects between these blocks offering field-programmability. Unlike their digital cousin, the FPGA, the devices tend to be more application driven than general purpose as they may be current mode or voltage mode devices. For voltage mode devices, each block usually contains an operational amplifier in combination with programmable configuration of passive components. The blocks can be utilized as summers or integrators. The disadvantage of FPAA is that the commercially available device only contains limited CAB resource. For example, The AN231E04 device only consists of a 2x2 matrix of fully CABs, surrounded by programmable interconnect resources and analog input/output cells with active elements [34].

9. **Optical Device Computing:** Optical techniques have shown great potential in various computing areas. The main advantage of optical systems resides in their inherent parallelism, which suggests the possibility to realize integrated high-speed parallel processors within complex optical networks. Some researchers have paved the way in the area of optical matrix multiplication and matrix inversion in femtosecond level which are the most resource-demanding and time-sensitive part in the traditional microelectronic-based computing [35], [36].

10. **ASIC:** An application-specific integrated circuit (ASIC) is an integrated circuit cus-

tomized for a particular use, rather than intended for general-purpose use. By implementing the higher-clocking capable and optimized circuit design, an EMTP type of ASIC can execute the electromagnetic emulation in real-time or faster than real-time for the energy-efficient and timedelay-sensitive scenario. However, the non-recurring engineering (NRE) cost of ASIC, which refers to the one-time cost to research, design, develop and test a new product or product enhancement, can run into the millions of dollars not even mentioning the time-consuming processes in the manufacturing. FPGA are the modern-day technology for building a breadboard or prototype from standard parts; programmable logic blocks and programmable interconnects allow the same FPGA to be used in many different applications. For smaller designs or lower production volumes, FPGAs may be more cost effective than an ASIC design, even in production. Therefore, device manufacturers typically prefer FPGAs for prototyping and devices with low production volume and ASICs for very large production volumes where NRE costs can be amortized across many devices [37].

11. **SoC:** Systems-on-Chip (SoC) is in contrast to the common traditional motherboard-based PC architecture, which separates components based on function and connects them through a central interfacing circuit board. Whereas a motherboard houses and connects detachable or replaceable components, SoCs integrate all of these components into a single integrated circuit, as if all these functions were built into the motherboard. A SoC will typically integrate a CPU, GPU and memory interfaces, hard-disk and USB connectivity, random-access and read-only memories and secondary storage on a single circuit die, whereas a motherboard would connect these modules as discrete components or expansion cards [38]. Chapter 2 will introduce the concept of SoC further.

12. **Quantum computing:** Quantum computing is the use of quantum-mechanical phenomena such as superposition and entanglement to perform computation. There are currently two main approaches to physically implementing a quantum computer: analog and digital. Analog approaches are further divided into quantum simulation, quantum annealing, and adiabatic quantum computation while digital quantum computers use quantum logic gates to do computation. Today's physical quantum computers are very noisy and quantum error correction is a burgeoning field of research [39].

1.3 Motivation and Objectives

The motivation of this thesis is consistent with the general development trend of real-time electromagnetic transient emulation, which is to generate more accurate and detailed results for the device-level power electronic converter for practical advanced transportation

application. The emerging technologies of power electronics devices, converter and grid topologies also require the corresponding developments of the modeling and emulation techniques. Such challenges come from the higher demand of emulation quality and the complexity of the modern power converter, which requires the solutions from both the algorithm and the optimized hardware-software co-design implementation platform.

The specific research objectives and the corresponding motivations are listed as follows:

- **Block-Structured Configuration of Real-Time Modeling Power Electronic Devices**
  Device-level electromagnetic transient simulation of power electronic is a particular challenge due to the requirements of accurate representation and efficient solution. Device-level electromagnetic transients can happen in very short time-period, which requires nanosecond-level time-step for accurate emulation. Simplifying the device-level power electronic model can help the nanosecond-level emulation running in real-time. The block-structured configuration can simplify the electromagnetic transient procedures into several efficient modeling calculation subsystems without solving the complex non-linear equation which might introduces extra iteration during the simulation.

- **Neural Network Based Device-Level Modeling of Power Electronics**
  Power electronic device datasheet can provide standard operation transient information. However, in reality, the power electronic device features vary from device to device and for specific application. Even though the power electronic device is consistent with the device datasheet at the beginning, the switching on-off characteristics change overtime when suffered from the aging processes. Thus, there is a need to develop an adaptive real-time device-level modeling method to mitigate the difference between the datasheet-based modeling method and field testified operation. By importing the field test waveform to the neural network based device-level model, the hybrid neural network can produce up-to-date device-level switching on-off transients.

- **Development of Emulation Platform for Testing Power Converter Stresses**
  The high-speed rail (HSR) delivers fast, efficient, and reliable transportation for connecting large cities and to integrate regions in a country. The DC traction system has been utilized to reduce land commute congestion for intercity traffic and subway transportation since the late nineteenth century. Due to the insulation constraint, the DC traction voltage level was limited to several hundred volts in the nineteenth century. The high energy loss of overhead line restricted the development of high-speed DC traction. Meanwhile, AC traction dominated the market of high-speed traction in the twentieth century with the help of on-board high-voltage capable equipment which reduced the loss in the power conversion stage. However, existing AC trac-

tion systems suffer from the reactive power loss, inductive line voltage drop, bulky transformer, and extra on-board AC-DC converters. With the development of power semiconductor and isolation technology, high-voltage DC circuit breaker, motor, and power electronic components are being increasingly adopted in the medium voltage DC (MVDC) electrified system. There is a potential trend that some of the current AC high-speed traction systems will be replaced or upgraded to MVDC high-speed traction systems to reduce the manufacturing and maintenance costs.

- **MPSoC-FPGA Platform Development and Design Methodologies**
  With detailed converter models and more complex grid topologies, the computation requirement is substantially increased, which can be met by using the interconnected computing devices with high parallelism. The proposed algorithms and modeling schemes are either implemented and verified on FPGA or MPSoC device. The MPSoC-FPGA platform is developed for the real-time emulation of the advanced transportation application, which uses the small form-factor pluggable (SFP) for board-level communication. The complexity of the emulation system has been substantially increased, which naturally requires much higher design effort. To address this issue, high-level synthesis (HLS) is explored and applied to the design process.

1.4 Summary of Contributions

The major contributions of this work are summarized as follows:

- **Hammerstein Configuration Based Device-Level Power Electronic Emulation**
  The real-time device-level dynamic electro-thermal models for diode, thyristor and IGBT are proposed and emulated based on Hammerstein configuration on a SoC-based hardware and software co-design platform for the application of EMRG system. The Hammerstein configuration modeling procedures reduces the complexity of building accurate device-level power electronic models. The modeling procedure of the static and dynamic electrical model, transient power loss model and thermal network calculation is given based on the dedicated device datasheet. The proposed models have been validated in two circuits of the EMRG system and compared with the result from the off-line device level software SaberRD®.

- **Wiener-Hammerstein Configuration Based Emulation of Traction Power System**
  Wiener-Hammerstein configuration based device-level electro-thermal model for power electronic components is proposed and demonstrated with a three-phase to single-phase MMC-based traction power system in real-time emulation on the MPSoC platform. The MMC sub-module device-level transients are simulated in the Cortex®-A53 Core with the latency of $90ns$ and the three-phase to the single-phase

MMC-based traction power system is simulated on the programmable logic (FPGA) with the latency of 24.2μs. Both system-level and device-level results have been validated by professional power system software PSCAD/EMTDC® and power electronic simulation software SaberRD®.

- **SiC Device Modeling for AC Traction System**
  The technology of high-speed rail network is constantly evolving with the introduction of newer power semiconductor device, and an accurate and efficient hardware-in-the-loop simulation is necessary. Real-time device-level modeling of ultrafast power switch is demanding due to high amount of computation execution and time-sensitive condition. With proper allocation of the high-sequential clocking ARM® core and massively parallel FPGA execution resource, real-time ultra small time-step modeling of detailed power converter system can be realized for both device-level and system-level transients. A Wiener-Hammerstein based real-time modelling method for SiC IGBT module emulation is proposed in the energy conversion system of the Beijing-Shanghai HSR application.

- **Adaptive Neural-Network Based Power Electronic Modeling**
  The adaptive hybrid kNN-RNN based device-level model for the IGBT module is proposed and implemented on the FPGA platform and tested on the study case of complete DC traction system. The kNN module is utilized to distinguish the transient switching state with a latency of 360 ns. With the help of kNN module, RNN module can be operated with less hidden layer neurons and training epochs. RNN module is divided into two sections: training and prediction. The training error target is set at 0.05% within 20 epochs while the prediction can be performed within 140 ns for a 100 ns time-step transient results with MSE of 2.4%. The device-level transients are emulated with the latency of 100 ns in circuit solver. The emulation results are validated by the professional simulation tools at the system-level and device-level.

- **MPSoC-FPGA Real-Time Hardware Emulator**
  The various proposed modeling schemes and circuit topologies have been designed and implemented in optimized communication capable digital hardware with both highly sequential clocking processing system and sufficient paralleled logic resources.

1.5 Thesis Outline

This thesis consists of seven chapters. The other chapters are outlined as follows:

- **Chapter 2**
  The background information of the FPGA and MPSoC devices used for the implementation of the real-time emulator in this work is described in this chapter. The

architectures and the characteristics of the FPGA and MPSoC are introduced. The advantages and restrictions of using high-level synthesis are presented. The communication approach used in this work is introduced.

- **Chapter 3**
  Real-time emulation of device-level power electronics plays an essential role in many industrial applications for design and hardware-in-the-loop (HIL) testing of system components and controllers. Due to the complexity and heavy computational burden of the real-time hardware implementation of the analytical and the numerical models, dynamic electro-thermal behavioral models for diode, thyristor and insulated-gate bipolar transistor (IGBT) are proposed based on the Hammerstein configuration. The power electronic device model parameters are extracted from the known device datasheets and implemented in Zynq® System-on-Chip (SoC) platform with accelerated processing for real-time application. An electro-magnetic rail gun (EMRG) system has been employed as the study case to compare the performance of the proposed electro-thermal behavioral models with that of off-line simulation models on SaberRD® software.

- **Chapter 4**
  Real-time emulation of device-level power electronic converter models plays an essential role in traction power systems by allowing accurate prediction of device stre -sses to design improved control and protection schemes. The electro-thermal behavioral power electronic models for the modular multi-level converter (MMC) for medium voltage direct current (MVDC) traction power system is proposed based on the Wiener-Hammerstein configuration. The new configuration introduces the carrier charge prerequisite dynamic transients before device turn-on or turn-off operation. The equivalent carrier charge circuit is also proposed and the first-order delay assumption of turn-on and turn-off delay time has been proven by the device datasheet. The power electronic device models are implemented in Xilinx® Zynq® multi-processing system-on-chip (MPSoC) platform. By utilizing hardware and software co-design, both 25μs time-step system-level and 100ns time-step device-level transients can be captured in real-time within a single device. The three-phase unbalance issue has been resolved by introducing the three-phase to single-phase MMC topology. In the case study, the MMC-based MVDC traction power system has been utilized to validate the performance of the proposed electro-thermal behavioral power electronic models by the off-line simulation models on SaberRD® for device-level transients and PSCAD/EMTDC® for system-level transients.

- **Chapter 5**
  Real-time device-level hardware-in-the-loop (HIL) emulation of a complete high-speed rail system is challenging due to its complex modeling and high computing

demand. With higher energy-efficient and switching frequency semiconductor material being found and adopted in the power electronic electrified traction application, there is a need to develop such new material based real-time device-level power electronic models in the modern and future traction system to estimate and verify the device switching transients, energy efficiency, and power quality improvement capability. A real-time SiC IGBT model is proposed based on the Wiener-Hammerstein configuration. A complete Beijing-Shanghai AC traction application is utilized as the study case, implemented on the hybrid multiprocessor system-on-chip (MPSoC) and field-programmable gate array (FPGA) platform, to verify the system-level and device-level performance of the proposed model with comparisons to commercial software PSCAD/EMTDC® and SaberRD®. The dedicated hardware implementation enabled model execution at 100 ns for device-level transients and 10 μs for system-level transients.

- **Chapter 6**
  DC traction drive systems require high-frequency switching in the power converter whose device-level switching transients have a significant impact on the accuracy of hardware-in-the-loop emulation. Real-time device-level emulation has high computation demand on calculating the switch on and off transients. This chapter introduces a new method to estimate the switching transients by utilizing artificial intelligence in the hardware design. In the hybrid neural network, the k-nearest neighbors (kNN) concept and the recurrent neural network (RNN) have been employed to emulate the transient waveforms in the DC traction drive. The kNN module classifies the switching states while the RNN module predicts the transient waveform for a specific condition. The work also proves that the classification of the input switching states with the help of kNN can play an essential role. The hardware implementation of the study case can be executed at 100ns time-step with device-level transients. The results have been validated by PSCAD/EMTDC® at system-level and SaberRD® at device-level.

- **Chapter 7**
  This chapter summarizes the contributions of this research and discusses the future work for the advanced transportation application study.

2

Architecture, Design Methodology of MPSoC and FPGA

The previous chapter has exploited the possibility of utilizing the state-of-the-art implementation hardware for the real-time device-level emulation. However, not all the cutting edge technology can be used in the scenario of real-time power system emulation in terms of their commercially availability, manufacturering cost, scalability, time-demanding tasks. Considering the commercially availability, optical device and quantum computing are still on the way of research and development of dealing with the influence of the noise which annoys the precision of the physics-based calculation processes. When comes to manufacturing cost, ASIC provides the executability of real-time electromagnetic emulation in the energy-efficient and timedelay-sensitive scenario but the expansive NRE cost put ASIC in a worse position compared to the reconfigurable FPGA. For scalability, the commercially available FPAA only contains four full CABs which limits the simulation scale of the power system. Combining the FPAAs with external interface will introduce noise and time-delay in the execution processes. Real-time device-level power electronic emulation demands for real-time capable high-clocking and massive parallelled execution structure with optimized communication protocol. MCU and DSP suffered from their low MHz clocking frequency while GPU and TPU are for the specified graphics and neural network. Even GPU has been investigated for the acceleration of ETMP but the frequent millisecond time delay from communication between GPU and CPU makes the application of the nanosecond-level device-level power electronic emulation unapplicable. Though FPGAs benefit from their massive paralleled structure, their operating frequency can only achieve up to 100Mhz when stable. Both ARM and CPU can clock at GHz-level frequency but the lack of massive parallel structure makes the parallel algorithms unable to reach their limit. Based the above mentioned analysis of the advantages and disadvantages for different ex-

ecution hardware, the industry offers a flexible and compromised solution by combining of all the merits of the dedicated hardware into one die with highly optimized communication protocol, called system-on-chip (SoC). Currently, the commercially available SoC can package a multi-core ARM-based processor (Processing system), FPGA (Programmable logic), GPU, WIFI, and other peripherals into a single die. With increased dedicated purpose cores embedded in the SoC, the industry renames this type of hardware as multiprocessor system-on-chip (MPSoC).

MPSoC is not simply traditional multiprocessors combination into a single chip but redesigned embedded system to fulfill the specific application scenarios. Actually, it is proved that commercial MPSoC has a longer history than the commercial multicore processors. The first commercial multicore general-purpose processor was introduced in 2005 by Intel while the history of commercial MPSoC can be dated back to 2000. Whereas the first attempt of the multicore system called ILLIAC IV, which became operational in November 1975, is considered the world's first massively parallel computer system with the configuration of 256 64-bits processors which communicate and cooperate to solve large problem fast. However, this massively parallel system is not integrated in the compact IC resulting long delay of communication of memory access. Mature very large scale integration (VLSI) technology have boosted the higher levels of parallelism of uniprocessor along with programmability and block diagrams based application-specific IC. As the high-performance demanding market grows, single processor soon become the bottleneck of the high-performance computing system. Then several types of MPSoC appears in the market. Lucent Daytona, the first commercial MPSoC, was designed for wireless base stations with the architecture of four symmetric SPARC V8 based CPUs attached to a high-speed capable bus in 2000. Shortly after the Daytona appears, C-5 Network Processor, which combines RISC executive processor and generalized fabric processor in one die, has been launched on the network packet processing market in 2001. The above mention MPSoCs are considered as the homogeneous architecture, hemegeneous ones are on stage until the enormous demand of multimedia processing and personal cell phone in the early 20th century. Among them, the Texas Instruments (TI) OMAP architecture is one of the typical hemegeneous one in the history of MPSoC, whose ARM core acts as a master and its DSP acts as a slave performing signal processing hardware-accelerated algorithm. Recently, an increasing number of platforms have included the FPGA fabric in the MPSoC design which allows the user to implement their hardware/software co-design methodologies. To significantly improve the parallelism, MPSoC devices are used as the implementation platform for the real-time emulator in this research. The architecture, design methodologies, and the communication are described in the following sections with details.

2.1 MPSoC Architecture

In this section, the components of the MPSoC architecture are introduced in detail with their specific application in the hardware/software co-design scene. There are two types of MPSoCs applied in this research: Zynq®-7000 series and Zynq® Ultrascale+™ series.

- **Zynq® System-on-Chip (SoC) Platform**
  The Zynq®-7000 All Programmable SoC [40], shown in Fig. 2.1, consists of a dual-core ARM-based processing system (PS) and 28 nm FPGA-based programmable logic (PL) in a single device, which enables the integration of hardware acceleration using parallelism and high-frequency clocking sequential computation.

  The PS contains a dual-core processor, snoop control unit (SCU), Level-2 cache, on-chip memory (OCM), direct memory access (DMA), NEON, floating point unit (FPU) engine, and the peripheral devices. The NEON engine is a general purpose single instruction multiple data (SIMD) processing structure. Each ARM® core in the PS has a 128 bit width NEON engine. The engine can process four floating type data or eight integer type data simultaneously by one instruction. With the help of this engine, the parallel and repetitive operations can be significantly accelerated on large data sets.

- **Zynq® Ultrascale+™ MPSoC platform**

  The Xilinx® Zynq® Ultrascale+™ MPSoC system setup is shown in Fig. 2.2. The computer compiles and programs the Vhdl code to dedicated MPSoC board via Xilinx® Vivado® software. The FMC connector of the MPSoC board is connected to FMC-to-DAC converter board which is connected to the TI® DAC board. The DAC board converts the digital signals to the analog signals and transmit the analog signals to the oscilloscope to present the real-time implementation results.

  The Zynq® Ultrascale+™ MPSoC [40], shown in Fig. 2.3, combines the processing system (PS) and the programmable logic (PL) into the same device. The $16nm$ programmable logic fabric resources inside the device enable hardware to compute acceleration in parallelism. The processing system contains a 64-bit quad-core Cortex®-A53 processor, a real-time dual-core Cortex®-R5 processor, a Mali-400 MP2 GPU, and the peripheral device.

  PL in the Zynq® Ultrascale+™ (XCZU9EG) consists of 600,000 logic cells, 274,000 lookup tables (LUTs), 548,000 flip-flops, 912 block RAMs (BRAMs), 2,520 DSP slices, analog-to-digital converter (XADC), integrated PCI Express communication block, etc. Traditional VHDL programming is time-consuming while advanced algorithms in applications became increasingly sophisticated. With the help of Vivado High-

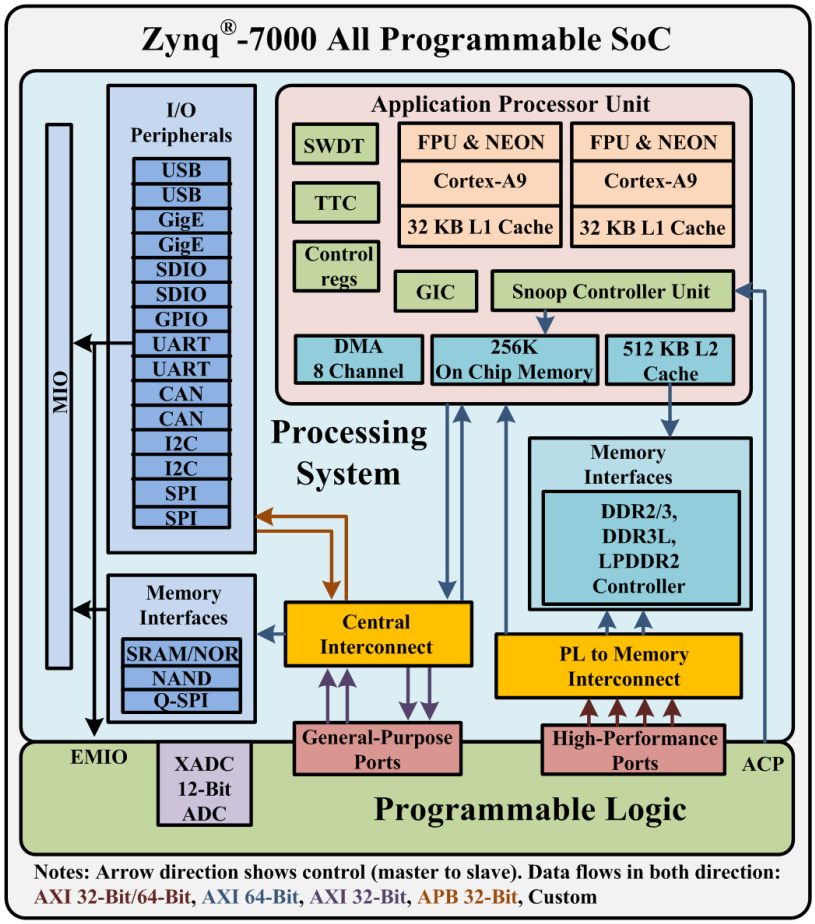

Figure 2.1: Zynq®-7000 All Programmable SoC schematic.

Level Synthesis (HLS) developed by Xilinx®, the programmer can utilize C, C++ and System C code to target the programmable logic directly.

2.2 Hardware/Software Co-design

System-level circuit emulation is applied inside the programmable logic to accelerate the computation speed. The calculation of the system-level circuit can be considered as matrix operations primarily which can be accelerated and paralleled by programmable logic (hardware design).

Device-level transients and system control are calculated in the processing system (software design). In a small-scale circuit, the simulation is highly sequential and not beneficial to be separated into multi-core operation due to high latency in core-core communication. With enough high operating frequency, a single core can be optimum for small-scale circuit simulation such as the sub-module in the MMC.

For example, in each system-level time-step, the system control signal generated

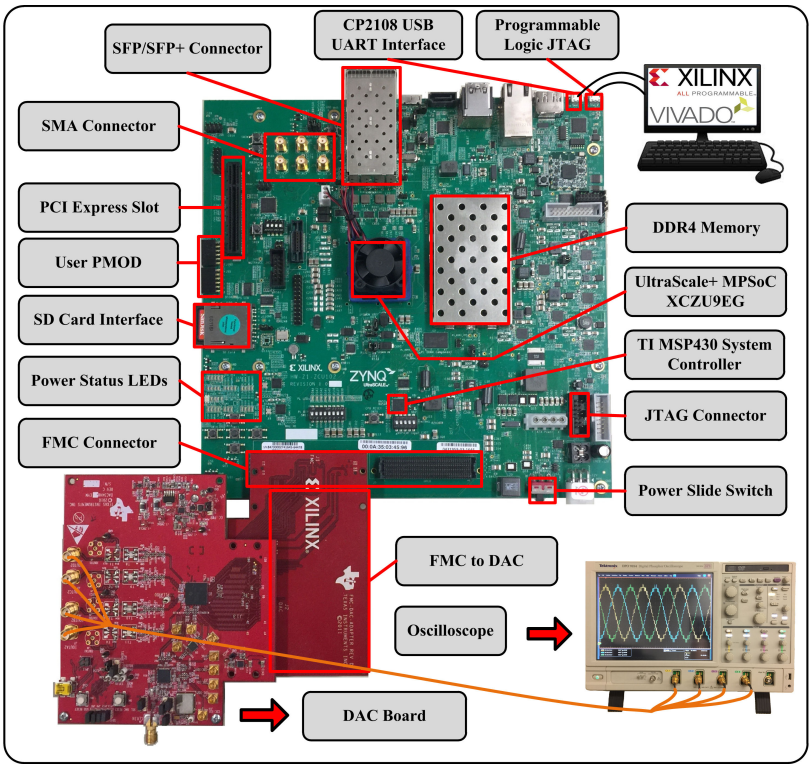

Figure 2.2: MPSoC platform setup.

from the real-time Cortex® processor will be transmitted to the programmable logic for system-level simulation and another higher clocking Cortex® processor for device-level simulation. Meanwhile, the programmable logic updates the history terms to the high clocking Cortex® processor which in-turn updates the result to programmable logic in the next time-step.

2.3 Development Tool for MPSoC

Currently, MPSoC venders provide a variety of development tool to the customer based on their operating system and development language. In this work, we give two types of development method from Xilinx®: High-level language programming method and hardware pre-defined application development method.

- **High-Level Language Programming Method**
  This type of method can offer GPU-like and familiar embedded application development and runtime experiences for C, C++ and/or OpenCL development without worrying the physical hardware design. Xilinx® provides two types of software based on the end user's programming skill and needs: SDAccel and SDSoC.

  The SDAccel IDE provides all the features of a standard software development environment: optimized compiler for host applications, cross compiler for the adapt-

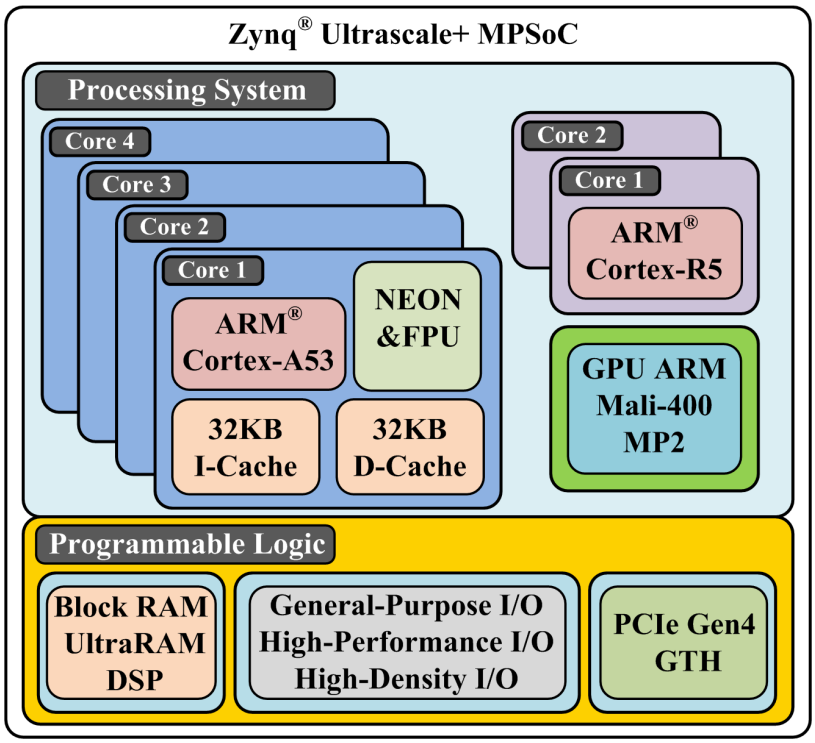

Figure 2.3: Zynq® Ultrascale+™ MPSoC schematic.

able hardware, a robust debugging environment, and profilers to identify performance bottlenecks and optimize the application. The host application is developed in C/C++ and uses standard OpenCL API calls to interact with the FPGA-accelerated functions which can be modeled in either RTL, C/C++, or OpenCL. This provides familiar entry points for hardware designers and software engineers alike.

The SDSoC™ development environment gives a familiar embedded C/C++/Open -CL application development experience including an easy to use Eclipse IDE and a comprehensive design environment for heterogeneous Zynq® SoC and MPSoC deployment. Complete with the industry's first C/C++/OpenCL full-system optimizing compiler, SDSoC delivers system level profiling, automated software acceleration in programmable logic, automated system connectivity generation, and libraries to speed programming. It also enables end user and third party platform developers to rapidly define, integrate, and verify system level solutions and enable their end customers with a customized programming environment.

- **Hardware Pre-defined Application Development Method**
  This method need to utilize Xilinx® Vivado® development tool to defined the hardware configuration before integration of the software development. Typical FPGA design flow can be implemented in two ways: Verilog/VHDL and High Level Synthesis (HLS) custom IP. After which, Vivado®, based on the configuration, will go

through the following implementation procedures: optimize design, place design, physical optimization and route design. Then the hardware design can be used as a hardware function in the software development processes after exporting the hardware to the Xilinx ® SDK IDE. After defining the processing need in the PS, there are four type of heterogeneous compute resource available for multi-processing: 1.5 GHz capable APU, 600 MHz capable RPU, 100 MHz capable PL, and 667 MHz capable GPU. With proper interconnect technique integration, the heterogeneous compute system can conduct scientific simulation in a performance-efficient way. The interconnect technique will be introduced in the following section.

2.4 Interconnect

MPSoC provides several heterogeneous execution unit in the architecture. Thus the efficiency and speed of their interconnection make a big difference in the specific electromagnetic emulation application. Among the execution units, PS core to core and PS-PL communication are the most utilized protocols in this research since the GPU counterpart is still not applicable for the electromagnetic emulation scene. We will introduce these two communication mechanisms: inter-Process interrupt and AXI interface. The Zynq UltraScale+ MPSoC device's Interconnect is at the heart of its heterogeneous architecture. It links together all of the processing blocks together and enables them to interface with the outside world through access peripherals, devices and memory. It's therefore fundamental to understand its functionality in order to best tune your system.

- **Inter-Processor Interrupt**
  Inter-Processor Interrupts (IPIs) are the underpinning of communication between processing blocks in the MPSoC device, providing a channel to interrupt a remote processor and carry and can carry a certain amount of payload. MPSoC provides multiple Cortex processors that share common memory and peripherals. Asymmetric multiprocessing (AMP) is a mechanism that allows both processors to run their own operating systems or bare-metal applications with the possibility of loosely coupling those applications via shared resources. As reported, there is a delay of over 65 clocks for the first interrupt between the interrupt being asserted and the service routing clearing the control bit. The delay of the first interrupt could vary depending on whether a DDR memory refresh is occurring at the same time as the fetching of the service routine. After the first IRQ occurs, the service routine is stored in cache so fetches of the instructions for the routine are sourced by the cache instead of the slower, less deterministic DDR memory. After the first attempt, the interrupt service completed after 25 clocks for the remaining inter-processor interrupt.

- **AXI Interfaces**
  The Zynq UltraScale+ MPSoC device's interconnect is based on ARM's Advanced

eXtensible Interface (AXI) defined as part of ARM's Advanced Microcontroller Bus Architecture (AMBA) 4.0 specification, and incorporates many other related ARM technologies such as Cache Coherent Interconnect (CCI-400) and CoreLink NIC-400 Network Interconnect. The primary mechanism for linking any pair of blocks within the Zynq UltraScale+ MPSoC device is an AXI interface. At its most basic level, an AXI interface is specified as linking an AXI Master to one or more AXI Slaves. The master issues the requests that the slave(s) needs to fulfill. The communication between the PS and the PL plays a vital role in the hardware and software co-design process used in this work. Advanced eXtensible Interface (AXI) is a high-performance communication standard for SoC designs. There are three types of AXI for PS-PL communication: AXI-ACP for coherency, AXI-GP for general purpose and AXI-HP for high performance. For a large data set, the technical bandwidth of AXI standard varies from 2400MB/s to 9600MB/s.

2.5 Summary

The background information of the FPGA and MPSoC devices used for the implementation of the real-time emulator in this work is described in this chapter. The architectures and the characteristics of the FPGA and MPSoC are introduced. The advantages and restrictions of using high-level synthesis are presented. The communication approach used in this work is introduced.

3

Real-Time System-on-Chip Emulation of Electro-Thermal Models for Power Electronic Devices Via Hammerstein Configuration

This chapter proposes dynamic electro-thermal behavioral models for diode, thyristor and insulated-gate bipolar transistor (IGBT) based on the Hammerstein configuration, which is an original work of utilizing the System-on-Chip (SoC) platform to conduct accelerated processing for real-time device-level power electronic modeling scheme. An electromagnetic rail gun (EMRG) system is employed as the study case to compare the performance of the proposed real-time electro-thermal behavioral models with that of off-line simulation models on SaberRD® software. The proposed device-level modeling method is able to achieve 90 ns execution time for 100 ns per time-step in real world, and highly consistent with the result of 0.1 ns per time-step from the compared off-line software SaberRD®. For the first time, SoC was utilized to demonstrate the flexibility of highly sequential and massive parallel problem-solving capability in the domain of real-time electromagnetic transients emulation.

3.1 Introduction

Real-time HIL technology plays a pivotal role in the design and development of power electronic system for many applications. There is a need for accurate device-level modeling in real-time HIL emulation, especially under the extreme and extensive range conditions. With the help of HIL technology, the newly designed power switch, protection circuit and algorithm, power converter and controller can be repeatedly evaluated for design optimizing and tuning in a non-destructive emulation environment [41], [42]. Field

programmable gate arrays (FPGAs) become popular candidates for real-time modeling of several power devices and systems [43] - [52]. Rapid evolution of integrated circuit technology has led to the availability of commercial System-on-Chip (SoC) platform with a large capacity of computational resources such as ARM®-based multi-core processors and field programmable gate array (FPGA) on the same device, enabling the real-time implementation for complex industrial application [53] - [59].

Behavioral models can utilize the device datasheet to achieve a comprehensive device-level simulation. However, the analytical, numerical and hybrid models require specific dimensions and fabrication description to extract the dedicated physical parameters. In general, the device datasheet does not provide such detailed manufacturer design specifications, which makes modeling of the general device arduous. Some physical parameters inside the power semiconductor are not able to be measured or estimated unless there is extensive cooperation with the semiconductor manufacturer. High-order nonlinear equations, convergence problems, sensitivity to initial conditions, which may result in incomplete or inaccurate simulation, are also some of the main challenges in these models.

The choice of the modeling approach depends on the required accuracy, compute resource, convergence properties, validity range, and time consumption of the application. The analytical, numerical and hybrid models consume a significant amount of compute resource, thereby making them inappropriate for the real-time emulation at least in the near future. Though the system-level model is simplified enough to achieve real-time execution, it can not represent the detailed switching transient of the power electronic device. It should be noted that accuracy of the model is highly related to the modeling complexity. Therefore, it is reasonable to choose a device-level power electronic behavioral model for the real-time hardware emulation with acceptable accuracy and low compute resource consumption.

The Hammerstein and the Wiener models are two of the common behavioral models which separate the static and dynamic characteristics of general physical systems, which are made of transfer functions, practically. The Hammerstein model consists of a nonlinear static block in the front of a linear time-invariant dynamic block while the Wiener model consists of a linear time-invariant dynamic block followed by a nonlinear static block. From the perspective of power electronic device model identification, the Hammerstein model is more user-friendly than the Wiener model since dynamic changes happen after applied conditions. The earliest literature of Hammerstein model can be dated back to 1966 [60]. With generations of development in nonlinear system identification theory, the Hammerstein based models have been applied in a variety of areas, such as biomedical engineering [61], power electronics [62] - [64], neural networks [65], [66], communication systems [67], [68], and mechanical engineering [69]. Applying the Hammerstein configuration technique for behavioral modeling can indeed reduce the complexity of hardware implementation of power electronic device models. The modeling of IGBT by Hammer-

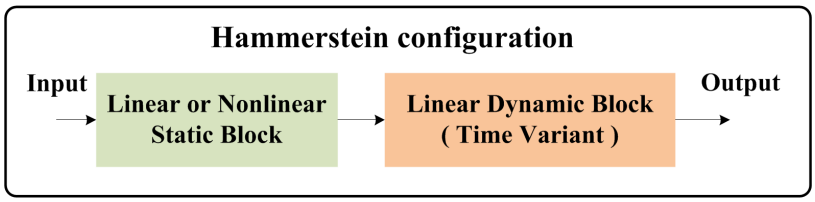

Figure 3.1: Block diagram of the Hammerstein configuration.

stein configuration was illustrated in [10] with detailed circuit experiments, however, no dynamic electro-thermal physical behavior could be predicted by the model and the highly nonlinear model equations may require iterative computation. Though the nonlinear part of the Hammerstein model can be optimized by introducing the Taylor Series technique, the requirement of iteration process is still cumbersome due to the nonlinear nature of model. If the nonlinear part of the Hammerstein model can be separated into linear parts in the equation or equivalent linear electrical element, computation burden can be significantly reduced by either circumventing iterations entirely or using only a few iteration in real-time implementation.

This chapter proposes dynamic electro-thermal nonlinear behavioral models for the diode, thyristor and IGBT using the Hammerstein configuration with the equivalent electrical component representation for real-time emulation of device-level behavior. The parameters of the Hammerstein models are extracted from the dedicated device datasheet. The performance of the proposed models is tested and validated in the electro-magnetic rail gun (EMRG) system. The chapter is organized as follows: Section 3.2 describes the construction of the Hammerstein configurations for diode, thyristor, and IGBT. Section 3.3 gives a brief introduction to the Zynq® System-on-Chip (SoC) platform. Section 3.4 explains the details of the case study implementation. Section 3.5 shows the real-time emulation results and verification using SaberRD® software, which provides device-level experimentally verified static and dynamic performance features.. Section VI gives the conclusion of this work.

3.2 Construction of Device-Level Dynamic Electro-Thermal Model Via Hammerstein Configuration

The Hammerstein model consists of a nonlinear static block followed by a linear time invariant (LTI) block while Hammerstein configuration encapsulates the idea of separating the static block from the dynamic block. The static block in the configuration can be a linear or nonlinear block. The dynamic block in the configuration is a linear time variant (LTV) system. The block diagram of Hammerstein configuration is shown in Fig. 3.1.

Iterative solution becomes necessary when the Hammerstein model is applied for system simulation due to the nonlinear static block inside the model. Hammerstein configu-

ration provides a way to simplify the nonlinear static block into linear static blocks in order to reduce the calculation burden. For the dynamic block, the configuration could utilize a LTV system instead of the LTI one if the time-varying parameters have a small impact on the system simulation results.

3.2.1 Device Static Electrical Model

The static characteristics of the power electronic devices (diode, thyristor, and IGBT) are similar (shown in Fig. 3.2) and are made up of a temperature dependent conductance $g_{on}(T_{vj})$ with a paralleled temperature dependent voltage controlled current source (VCCS) $i_{on}(T_{vj})$. The VCCS is a Thévenin equivalent expression of the $v_{on}(T_{vj})$. During the on-state, the model shows high conductance with a paralleled VCCS while under off-state the model exhibits low conductance with the paralleled zero-value VCCS. The linear interpolation method has been utilized to estimate $g_{on}(T_{vj})$ and $v_{on}(T_{vj})$ at the operating temperatures between T_{125° and T_{25°, given as

$$g_{on}(T_{vj}) = \frac{T_{vj}-T_{25^\circ}}{T_{25^\circ}-T_{125^\circ}}(g_{on}^{T_{25^\circ}} - g_{on}^{T_{125^\circ}}) + g_{on}^{T_{25^\circ}}, \tag{3.1}$$

$$v_{on}(T_{vj}) = \frac{T_{vj}-T_{25^\circ}}{T_{25^\circ}-T_{125^\circ}}(v_{on}^{T_{25^\circ}} - v_{on}^{T_{125^\circ}}) + v_{on}^{T_{25^\circ}}, \tag{3.2}$$

$$i_{on}(T_{vj}) = v_{on}(T_{vj}) \cdot g_{on}(T_{vj}). \tag{3.3}$$

3.2.2 Device Dynamic Electrical Model

The dynamic characteristic of power electronic devices varies from device to device due to the differences in physical structure and the manufacturing process. The device models of dynamic behavior will be introduced separately in this subsection. The dynamic characteristic curves for the three devices are shown in the Fig. 3.3.

$$\frac{U_o}{U_i} = \frac{\frac{1}{CS}}{R+\frac{1}{CS}} = \frac{1}{RCS+1}, \tag{3.4}$$

$$S = \frac{2}{\Delta t_{elect}} \cdot \frac{1-z^{-1}}{1+z^{-1}}, \tag{3.5}$$

$$\tau = R \cdot C, \tag{3.6}$$

$$\frac{U_o}{U_i} = \frac{\Delta t_{elect}+\Delta t_{elect}z^{-1}}{\Delta t_{elect}+2\tau+(\Delta t_{elect}-2\tau)z^{-1}}. \tag{3.7}$$

where Δt_{elect} is the electrical circuit simulation time-step; R and C are the first-order delay circuit parameters; τ is the time constant. The real values of R and C are not critical to the simulation. The product of R and C influences on the dynamic calculation significantly. Table 3.1 shows the time-based transient value of the first-order delay circuit.

3.2.2.1 Diode and Thyristor

The dynamic behavior of diode and thyristor are focused on the reverse recovery phenomenon during the turn-off time. Compared to the turn-off period, the turn-on energy

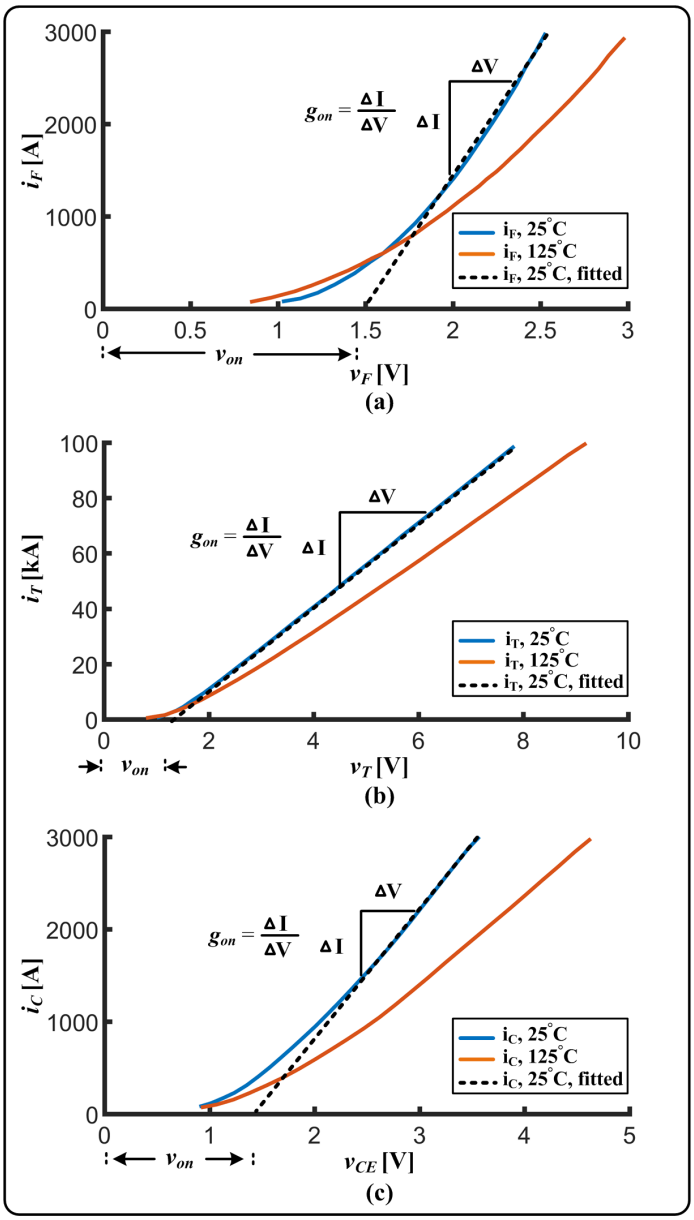

Figure 3.2: Static characteristics of: (a) Diode, (b) Thyristor, (c) IGBT.

loss and the forward recovery phenomenon are negligible. The uncontrolled and half-controlled devices such as diode and thyristor can not be turned off by the gate signal. When the devices meet turn-off conditions, the VCCS $i_{on}(T_{vj})$ inside the static block of the Hammerstein configuration plays a dominant role in the behavioral modeling while the value of the $g_{on}(T_{vj})$ inside the static block is set to the standard blocking state. The reverse recovery period can be separated into three periods for transient behavior: 1) static state before turn-off, 2) linear decrease of reverse recovery current, 3) static state decay of reverse recovery current. Fig. 3.4 shows the detailed separation of the reverse recovery period. During the Stage 1 period, the output of the static block will bypass the dynamic

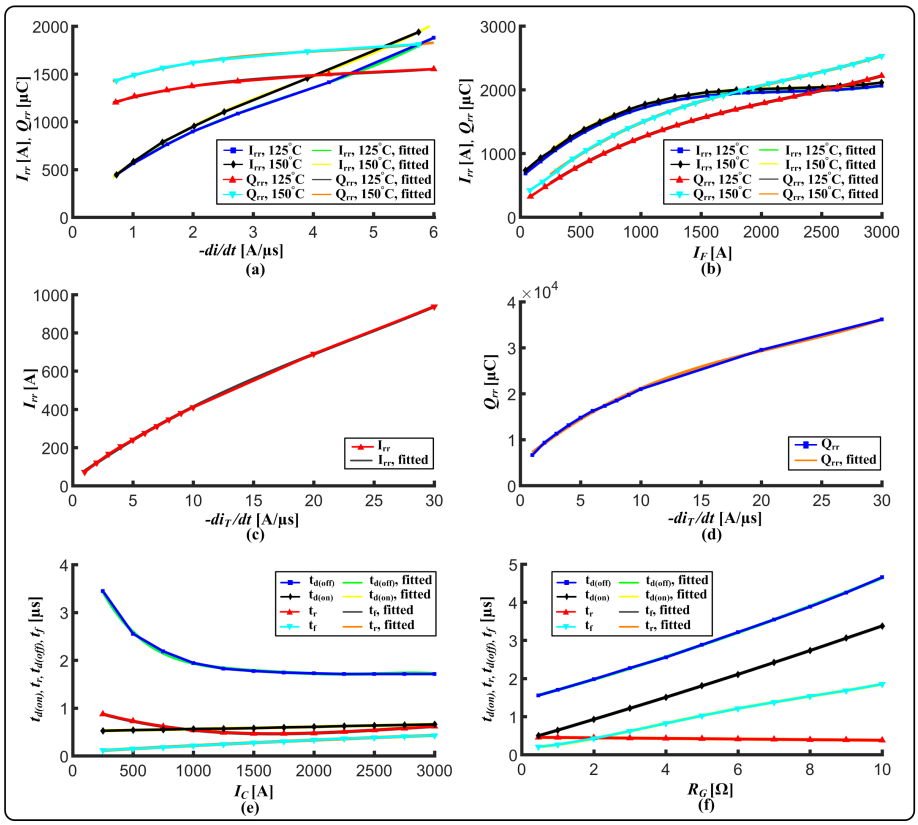

Figure 3.3: Dynamic characteristics: (a) Diode Q_{rr}- di/dt, I_{rr}- di/dt curves, (b) Diode Q_{rr}- I_F , I_{rr}- I_F curves, (c) Thyristor I_{rr}-di/dt curves, (d) Thyristor Q_{rr}-di/dt curves, (e) IGBT $t_{d,on}$- I_c, t_r- I_c, $t_{d,off}$- I_c, t_f- I_c curves, (f) IGBT $t_{d,on}$- R_G, t_r- R_G, $t_{d,off}$- R_G, t_f- R_G curves.

Table 3.1: Transient Percentage Value of the First-Order Delay Circuit

Time	Value
0.105τ	90.03%
1.386τ	25.01%
2.302τ	10.01%

block and be directly linked to the output of the Hammerstein configuration.

During the turn-off transient, the value of di/dt is determined by the default gate resistor. The reverse recovering time t_{rr} is estimated by the following equation:

$$t_{rr} = \frac{2Q_{rr}}{I_{rr}}. \tag{3.8}$$

Thus, the complete Hammerstein configuration for either the diode or thyristor can be depicted as in Fig. 3.5 (a).

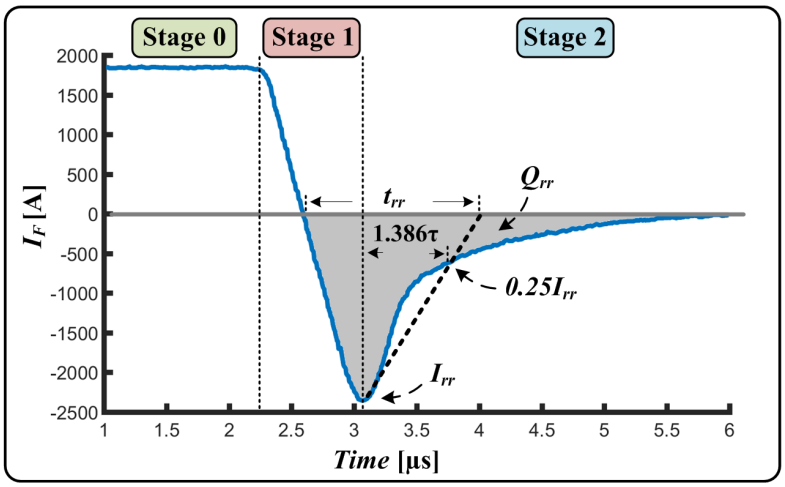

Figure 3.4: Reverse recovery phenomenon of diode.

3.2.2.2 IGBT

The main dynamic characteristics of IGBT are the rise time (during turn-on period) and the fall time (during turn-off period) of the collector current. The Fig. 3.3 (e), (f) show the collector current dependent and the gate resistance dependent curves for turn-on delay time $t_d(on)$, turn-off delay time $t_d(off)$, rise time t_r and fall time t_f.

The definition of the IGBT rise time and fall time is the period from 10% to 90% and 90% to 10% of the collector current respectively. So the rise and fall time of IGBT is equal to the normalized time 2.197τ in terms of the first-order delay circuit. By calculating τ, the dynamic part of the Hammerstein model can be determined.

In the full-controlled type devices such as the IGBT, the peak value of turn-on current can not be predicted until the circuit matrix equation is solved. During the turn-on time, the VCCS $i_{on}(T_{vj})$ in the static block will be set to zero while the value of the conductance $g_{on}(T_{vj})$ in the static block will be set from the standard blocking state to the on-state. During the turn-off time, the value of VCCS $i_{on}(T_{vj})$ will be set to zero while the conductance $g_{on}(T_{vj})$ will be set from the on-state to the standard blocking state. Thus, the complete Hammerstein configuration for the IGBT can be shown as in Fig. 3.5 (a) for turn-off condition and Fig. 3.5 (b) for turn-on condition. Fig. 3.5 (c) shows the steady-state representation for on and off state.

3.2.3 Device Transient Power Loss Model

The transient power loss model is based on a normalized turn-on or turn-off waveforms. By extracting the parameters from the datasheet, a transient power loss waveform model can be established with approximate timing and shape as shown in Fig. 3.6. The transient power loss model is separated into two periods, given as:

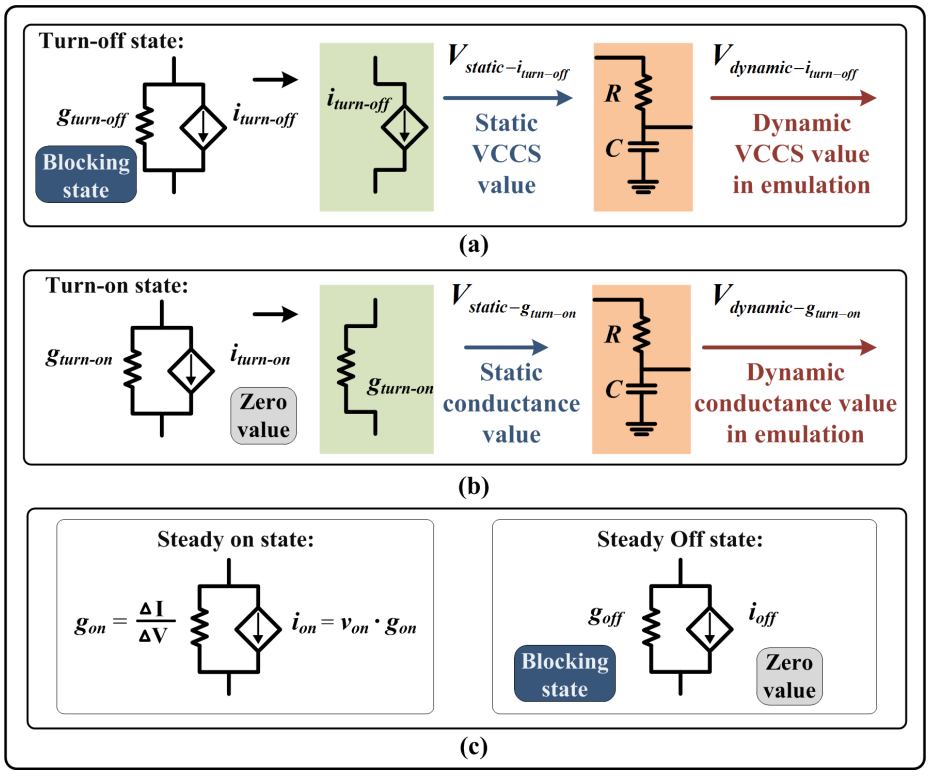

Figure 3.5: Hammerstein configuration for: (a) VCCS-based representation during turn-off, (b) Conductance-based representation during turn-on, (c) Steady-state on and off representation.

$$\begin{aligned} E_{loss} &= E_{loss-linear} + E_{loss-fod}, \\ &= \frac{1}{2} \cdot t_{linear} \cdot P_{peak} + \int_0^{\infty} P_{peak} \cdot e^{\frac{-t}{\tau_{fod}}} dt, \\ &= (\frac{t_{linear}}{2} + \tau_{fod}) \cdot P_{peak}, \end{aligned} \tag{3.9}$$

$$P_{peak} = \frac{E_{loss}}{\frac{t_{linear}}{2} + \tau_{fod}}, \tag{3.10}$$

where E_{loss} is the total power loss during the turn-on or the turn-off period, mentioned in Table 3.2; $E_{loss-linear}$ is the power loss in the linear period; $E_{loss-fod}$ is the power loss during the first-order delay approximation time; t_{linear} is the time of linear region; P_{peak} is the peak value of transient power; τ_{fod} is the timing variable of the first-order delay approximation and estimated according to the reference time given in the Fig. 3.6.

In electromagnetic transient simulation [70] of power circuits, all components and devices are modeled as a discrete-time companion models consisting of current sources and resistors. The drawback of the proposed Hammerstein configuration is that the node voltage may not represent the real device nodes due to its behavioral nature. The transient

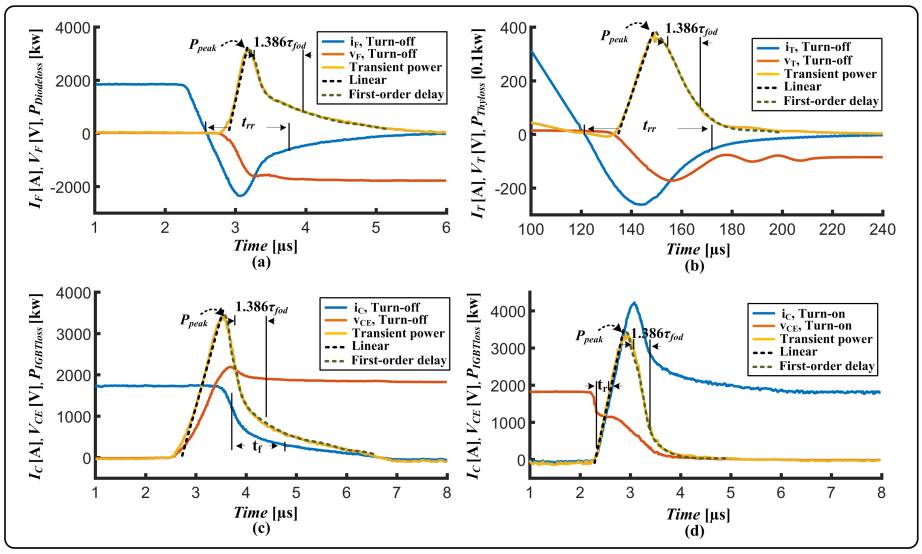

Figure 3.6: Transient power loss curves: (a) Diode turn-off curves, (b) Thyristor turn-off curves, (c) IGBT's turn-off curves, (d) IGBT turn-on curves.

power loss model works as a supplement for the proposed device Hammerstein configuration.

3.2.4 Device Thermal Network Calculation

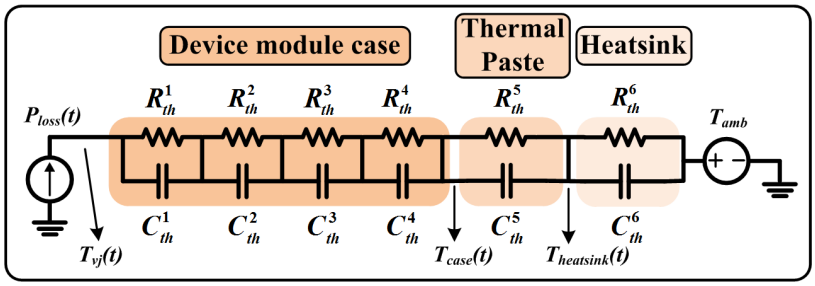

Figure 3.7: Thermal calculation circuit of the power electronic device.

The thermal network of the individual device is shown in Fig. 3.7. The power loss consumption becomes a VCCS inside this network. Cascaded combination of resistors and capacitors pairs has been utilized to compute the junction temperature, given as:

$$T_{vj}(t) = P_{loss}(t) \cdot (Z_{thjc} + Z_{thch} + Z_{thha}) + T_{amb}. \tag{3.11}$$

where $P_{loss}(t)$ is the power loss for the individual device; T_{amb} is the ambient temperature; Z_{thjc}, Z_{thch} and Z_{thha} are the thermal impedance from junction to case, case to heat sink and heat sink to ambient, respectively. In this work, each individual device is considered to be mounted on a $10K/kW$ water-cooled heat sink. The thermal impedances of the devices [77], [78], are shown in Table III. τ_{th}^{i} is the multiplication product of R_{th}^{i} and C_{th}^{i}.

Table 3.2: Thermal Impedances for Thermal Network

Thermal impedance	Z_{thjc}				Z_{thch}	Z_{thha}
	i=1	i=2	i=3	i=4	i=5	i=6
$R_{th}^{i,IGBT}[K/kw]$	5.854	1.375	0.641	0.632	9	10
$\tau_{th}^{i,IGBT}[ms]$	207.4	30.1	7.55	1.57	3000	45000
$R_{th}^{i,Diode}[K/kw]$	11.54	2.887	1.229	1.295	18	10
$\tau_{th}^{i,Diode}[ms]$	203.6	30.1	7.53	1.57	3000	45000
$R_{th}^{i,Thy}[K/kw]$	2.701	0.816	0.326	0.160	1.6	10
$\tau_{th}^{i,Thy}[ms]$	947.8	124.9	14.6	3.2	3000	45000

Higher resistance value in Z_{thjc} represents lower heat emission efficiency inside the device. Higher τ_{th}^{i} value in Z_{thjc} indicates longer delay for the temperature rising and falling. The thermal parameters of the selected thyristor show best heat emission efficiency while the ones of the diode present the worst. The calculation for the junction temperature of the device is given as

$$\begin{aligned} T_{vj}(t) &= \sum_{i=1}^{6} \Delta T_{th}^{i}(t) + T_{amb} \\ &= \sum_{i=1}^{6} \Big(\frac{R_{th}^{i} \cdot \Delta t_{thm}}{2\tau_{th}^{i} + \Delta t_{thm}} (P_{loss}(t) + P_{loss}(t - \Delta t_{thm})) \\ &\quad + \frac{2\tau_{th}^{i} - \Delta t_{thm}}{2\tau_{th}^{i} + \Delta t_{thm}} \Delta T_{th}^{i}(t - \Delta t_{thm}) \Big) + T_{amb}. \end{aligned} \tag{3.12}$$

where Δt_{thm} is the thermal time-step.

3.3 Study Case: Electro-Magenetic Rail Gun (EMRG) System in Real-Time SoC Platform

This section briefly introduces the Zynq® System-on-Chip (SoC) platform. Then it presents the details of the test circuit and its real-time implementation.

3.3.1 Test Circuit Topology

The EMRG [72] - [75], shown in Fig. 3.8, has been chosen as the study case to demonstrate the efficacy of the proposed behavioral modeling via the Hammerstein configuration. In the EMRG, two circuit topologies are implemented in the SoC. The smaller network topology is the CC for the capacitors inside the pulse forming network (PFN) which consists of the IGBT and diode. The larger network topology is the paralleled pulse forming units (PFUs) consisting of diodes and thyristors as the energy source for the EMRG.

The CC, shown in Fig. 3.9 (a), is recommended by ABB document [80]. The inductor and the capacitor can be considered as a single component. Thus, the equivalent is a one node circuit.

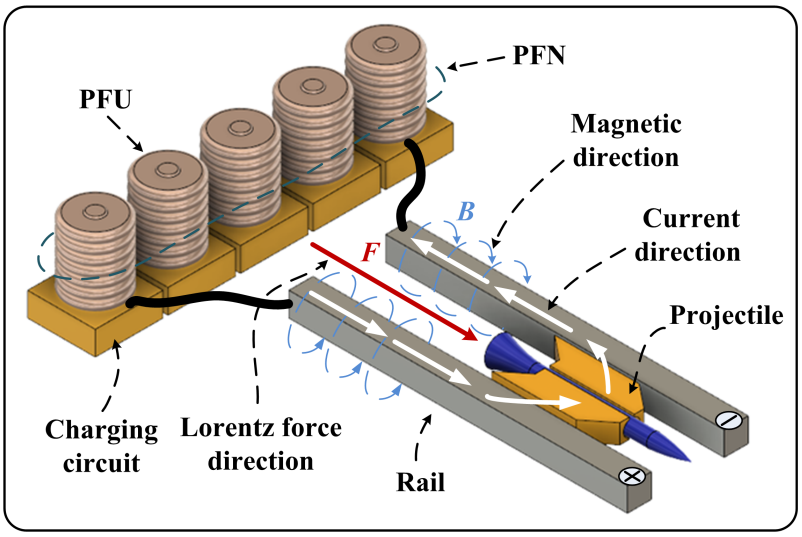

Figure 3.8: Electro-magnetic rail gun (EMRG) system.

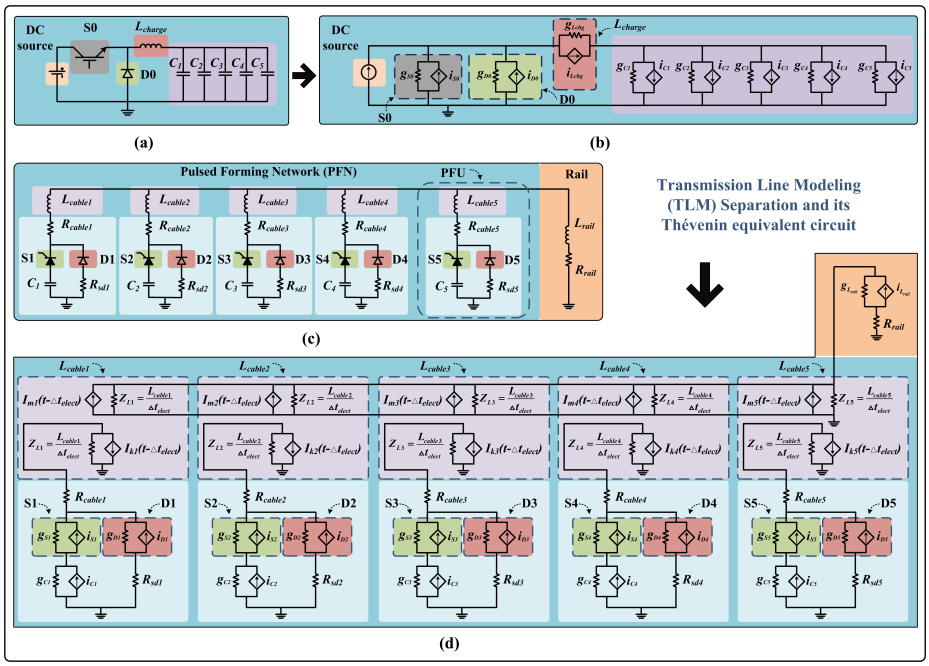

Figure 3.9: EMRG circuit topologies and their Hammerstein based Thévenin equivalents: (a) CC, (b) Thévenin equivalents for the CC , (c) PFN, (d) Thévenin equivalents for the PFN.

The pulse forming network (PFN) circuit, shown in the Fig. 3.9 (b), consists of five pulse forming units (PFUs) and an equivalent inductor and resistor for the rail. Each PFU is triggered by an optical switch in the rail. The TLM method [71] has been applied to separate the circuit topology for parallel execution. The inductor in the PFU is considered as a lossless transmission line, and the node current expressions are given as:

$$I_m(t-\tau) = I_k(t-2\tau) + \tfrac{2}{Z_L}V_k(t-\tau)), \tag{3.13}$$

$$I_k(t-\tau) = I_m(t-2\tau)) + \tfrac{2}{Z_L}V_m(t-\tau)), \tag{3.14}$$

$$Z_L = \tfrac{L}{\Delta t_{elect}}. \tag{3.15}$$

where Z_L is the equivalent TLM expression of cable inductance in discrete-time; $I_m(t-\tau)$ and $I_k(t-\tau)$ represent the past history currents of the cable. Δt_{elect} is the electrical simulation time-step.

3.3.2 Control System

The circuit control diagrams are shown in Fig. 3.10. The control method of the CC is the sliding mode control (SMC) where the charging current can be maintained in a stable range. When the voltage of the capacitor reaches the expected value, the CC will stop working.

The control method of the PFN is based on the projectile location in the rail. The optical switches are located at the specific point. When the projectile passes the optical switch, the corresponding thyristor will be triggered. The design objective of the trigger point is to maintain a stable current for the generation of Lorentz force during the acceleration process.

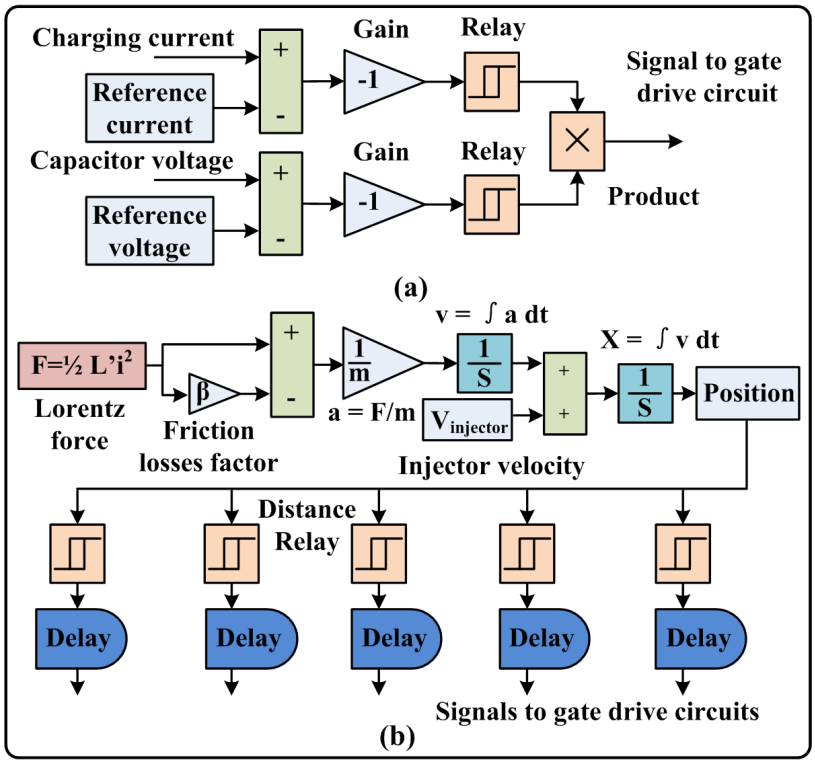

Figure 3.10: EMRG control diagram for: (a) CC, (b) PFN.

3.3.3 Implementation Method

The CC can be considered as a one node circuit after the combination of the inductor and capacitor component. The node voltage calculation for solving the CC is sequential. The PFN circuit utilizes the TLM method to separate the circuit topology consisting of a large circuit matrix into several parallel circuit sub-matrices.

A performance comparison of PS and PL for both charging and PFN circuit is demonstrated to decide the suitable compute hardware for each circuit. For this purpose, all the power electronic devices are considered as a VCCS in parallel with a resistor under the static thermal state. It should be noted that the no device-level behavioral calculations are included in the comparison because the fundamental EMTP circuit calculation can not be optimized much while the device-level behavioral calculation varies from algorithm to algorithm. After the performance test, the results proved that the processing system was suitable for the CC with NEON acceleration while the programmable logic was appropriate for PFN.

In this case, it is reasonable to implement the CC in Cortex A9 Core 0 of the PS and PFN into the PL. The device thermal circuit was implemented in the Cortex A9 Core 1 of the PS. CC and its thermal circuit are communicated by the global signal inside the PS while PFN and its thermal counterpart are communicated by the AXI standard between PS and PL. The simulation time-step for CC is $100ns$ while the time-step for PFN one is $2.5\mu s$. The thermal circuits for both circuits are calculated at a $10\mu s$ time-step.

3.3.4 State Charts

Fig. 3.11 shows the calculation procedure of the CC and the PFN. The cooperation between Cortex A9 cores and the PS-PL is also indicated in the state charts.

The green (dashed) states show the initialization of the electrical circuits or the thermal circuits calculation. The blue (dotted) and the red (solid) states indicate the repetitive calculation for the electrical and thermal circuit respectively. The background colors of the state chart specify the compute hardware resource type: either the cores of the PS or the PL.

The Cortex-A9 Core 1 execute the thermal circuit and temperature dependent parameters calculation. After the initialization, the state chart splits into two calculation loops. The loop selection depends on the charging state of the EMRG system. If the capacitor voltage reaches the desired value and the EMRG system is ready to launch the projectile, the state chart will go into the PFN thermal loop or it will go to the CC thermal loop.

The Cortex A9 Core 0 and PL execute the CC and the PFN circuit respectively, which will also update the power loss to the Core 0 and get respective parameters for the next step electrical calculation.

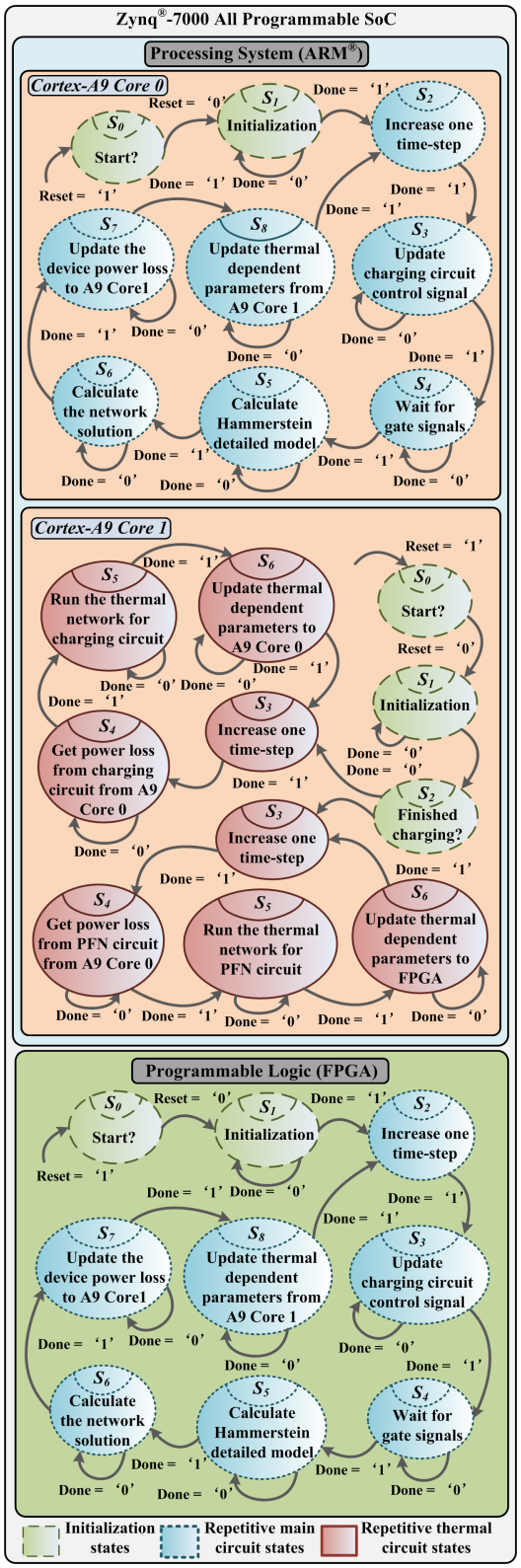

Figure 3.11: State chart of EMRG system on the Zynq® SoC platform.

Table 3.3: Execution Time Comparison per Time-Step for CC and PFN

Hardware time cost	Core 0 O0 $0.8GHz$	Core 0 O1 $0.8GHz$	Core 0 O2 $0.8GHz$	Core 0 O3 $0.8GHz$	PL HLS $0.1GHz$
CC (ns)	330	170	7.5	7.5	580
PFN (ns)	7845	3765	3590	2510	1870

Table 3.4: Programmable Logic Resource Utilization for CC and PFN

Circuit type	BRAM	DSP	FF	LUT
CC	768 (70%)	17 (1%)	9654 (2%)	47895 (21%)
PFN	314 (28%)	220 (24%)	46044 (10%)	75509 (34%)

3.4 Real-Time SoC Emulation Results and Discussion

3.4.1 Compute Hardware Resource Selection and Performance

Table 3.3 shows the performance comparison for both the CC and the PFN circuit. The hardware configurations are indicated at the top of Table 3.3. The number of the Ox is the optimization level of the NEON engine. Level-3 (O3) is the highest level of NEON instruction optimization by the compiler in Xilinx® software development kit (SDK). The NEON engine can theoretically accelerate the execution speed up to 4 times faster in floating type data processing. In the PL, high-level synthesis (HLS) is utilized to optimize the corresponding code to reduce the overall latency. In Table 3.3, the execution speed under different applied condition are shown for both CC and PFN. The Level-3 optimization achieves the shortest computation delay in the Core 0 of PS. However, the execution time of PL for PFN is 34% shorter than the one in PS. This is because the PFN consists of six paralleled sub-circuit, which fits the highly parallel FPGA execution architecture. CC is a sequential topology which can utilize the advantage of high sequential clocking computation feature in Core 0 of PS. The execution time of CC in Core 0 is 77.3 times faster than the one in PL. In this case, it can be concluded that CC is suitable for PS while PFN is appropriate for PL.

Table 3.4 illustrates the PL resource utilization in the performance comparison. Compared to the CC, the PFN circuit consumes relatively higher computational resource due to larger sized circuit topology. The thermal calculation is implemented on the other core of the PS. The proposed implementation method will be validated in the next subsection.

3.4.2 Results of Full Circuit Implementation

Fig. 3.12, Fig. 3.13 and Fig. 3.14 show the real-time implementation results of the full circuit topology. Fig. 3.12 (a) demonstrate the diode and IGBT turn-on and turn-off transient waveform. When turned on, IGBT shows overshoot phenomenon which is mainly intro-

Table 3.5: Latencies of CC with Device-Level Behavioral (Core 0) and Thermal (Core 1) Calculation and its Core - Core Communication

Core 0 O3 $0.8GHz$	Core 1 O3 $0.8GHz$	Core 0 -Core 1 $0.8GHz$	Core 1 -Core 0 $0.8GHz$	Average delay per time-step
$87.5ns$	$1540ns$	$115ns$	$52.5ns$	$89.175ns$

duced by the reverse recovery of diode inside the circuit topology. When turned off, IGBT show tail current in the transient due to the recombination of minority carriers. Fig. 3.12 (b) and (d) demonstrate the charging current and capacitor voltage respectively. The sawtooth shape of charging current is due to the sliding mode control, which intend to maintain the charging current at a stable range. With a stable charging current, the voltage of the capacitor shows a linear increase, which is regarded as a safe strategy for the device. Fig. 3.12 (c) shows the temperature variation during the charging period. CC stopped charging at t_{stop} when the capacitor voltage reached $450V$. Fig. 3.13 (a) and (b) show the averaged power loss of diode and IGBT in each thermal time-step Δt_{thm} respectively. Both turn-on and turn-off average power loss in each thermal time-step are considered in IGBT thermal network while only turn-off one is included for the diode. In Fig. 3.13 (c), the envelop of the projectile indicated different PFU energy release time in EMRG system. Fig. 3.13 (d) shows S1 current in the PFN circuit. The small difference between the results can be considered as the consequence of the extreme application condition whose physical parameters may not be precisely described in the datasheet. After releasing the energy, S1 takes a relatively long time to cool down. In Fig. 3.14 (a) and (b), the velocity and distance of the projectile are shown respectively with the peak indication of each PFU energy release. The initial injector velocity is $140m/s$ and projectile exit velocity is $2615.4m/s$ after the acceleration period. The projectile exit length is $7.23m$. Fig. 3.14 (c) and (d) show the diode's averaged power loss and the junction temperature respectively in each thermal time-step. The temperature jumped over $20°C$ in less than $1ms$, which indicates that the heat emission efficiency is relatively low. In Fig. 3.14 (e) and (f), the thyristor's averaged power loss and the junction temperature respectively in each thermal time-step. Compared to the diode, the thyristor shows relatively higher heat emission efficiency regarding temperature variation range.

Table 3.5 explains the latencies of the CC with device-level behavioral and thermal calculation. The emulation time-step of the CC is $100ns$ while the time-step of its thermal calculation is $10\mu s$. A shorter time-step in thermal calculation do not improve the accuracy in the thermal dynamic. The electrical circuit (Core 0) will update the power loss to the thermal circuit (Core 1) every 100 times. With less Core-Core data transmission, the emulation of both thermal and electrical side can be accelerated and the accuracy of both side remains the same under the circumstance. The thermal circuit (Core 1) update the

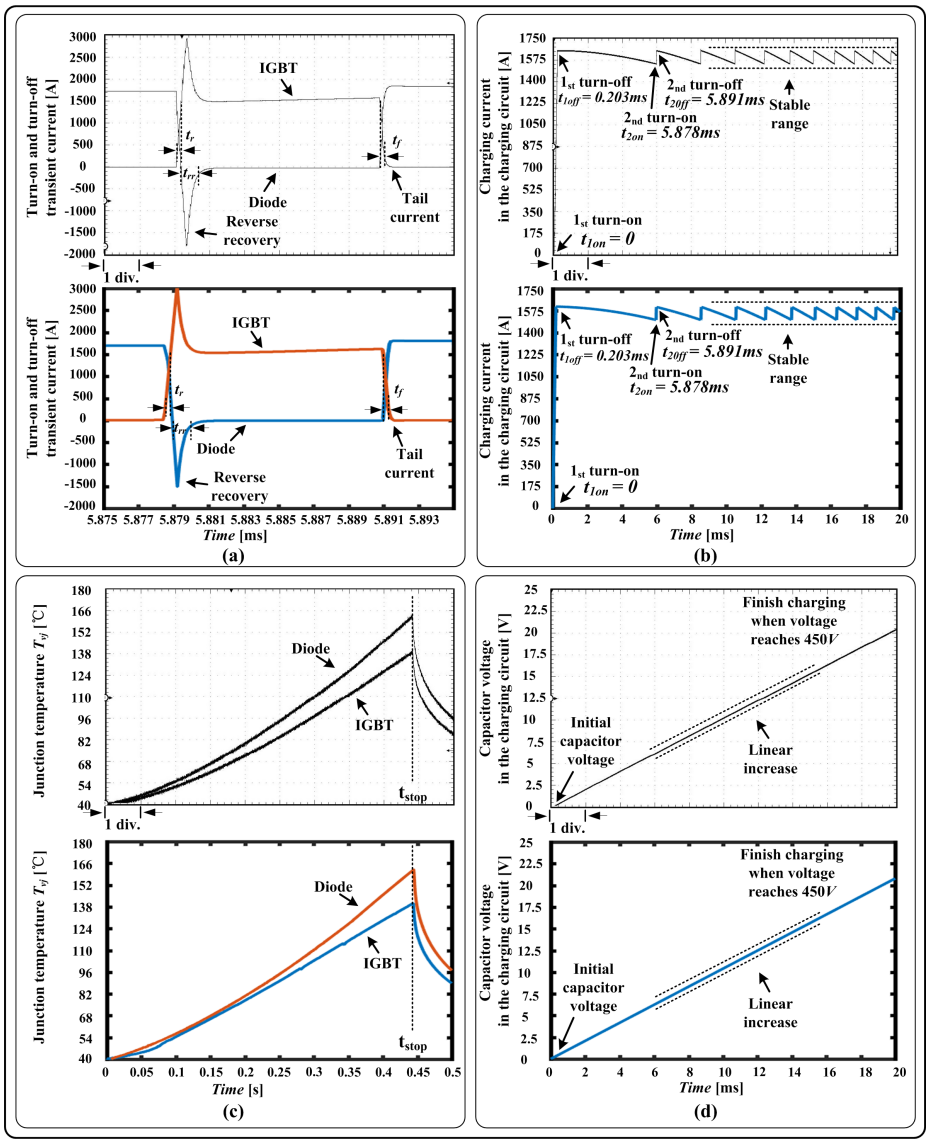

Figure 3.12: System-level and device-level results for CC and PFN from real-time hardware emulation (top sub-figure) and off-line simulation by SaberRD® software (bottom sub-figure) for: (a) IGBT and diode turn-on and turn-off transient current, (b) Charging current in the CC, (c) Junction temperature for IGBT and diode, (d) Capacitor voltage in the CC. Scale: (a) x-axis: $0.002ms$/div. (b)(d) x-axis: $2ms$/div. (c) x-axis: $50ms$/div.

temperature dependent parameters to the electrical circuit (Core 0) in the next time-step. These temperature dependent parameters are critical in the calculation of the equivalent electrical model in the equations and figures of Section II. The latency of the electrical circuit (Core 0), the thermal circuit (Core 1), electrical to thermal circuit communication (Core 0 - Core 1), and thermal to electrical circuit communication (Core 1 - Core 0) are $87.5ns$, $1540ns$, $115ns$, and $52.5ns$ respectively. The averaged delay per time-step is less than the required time-step $100ns$.

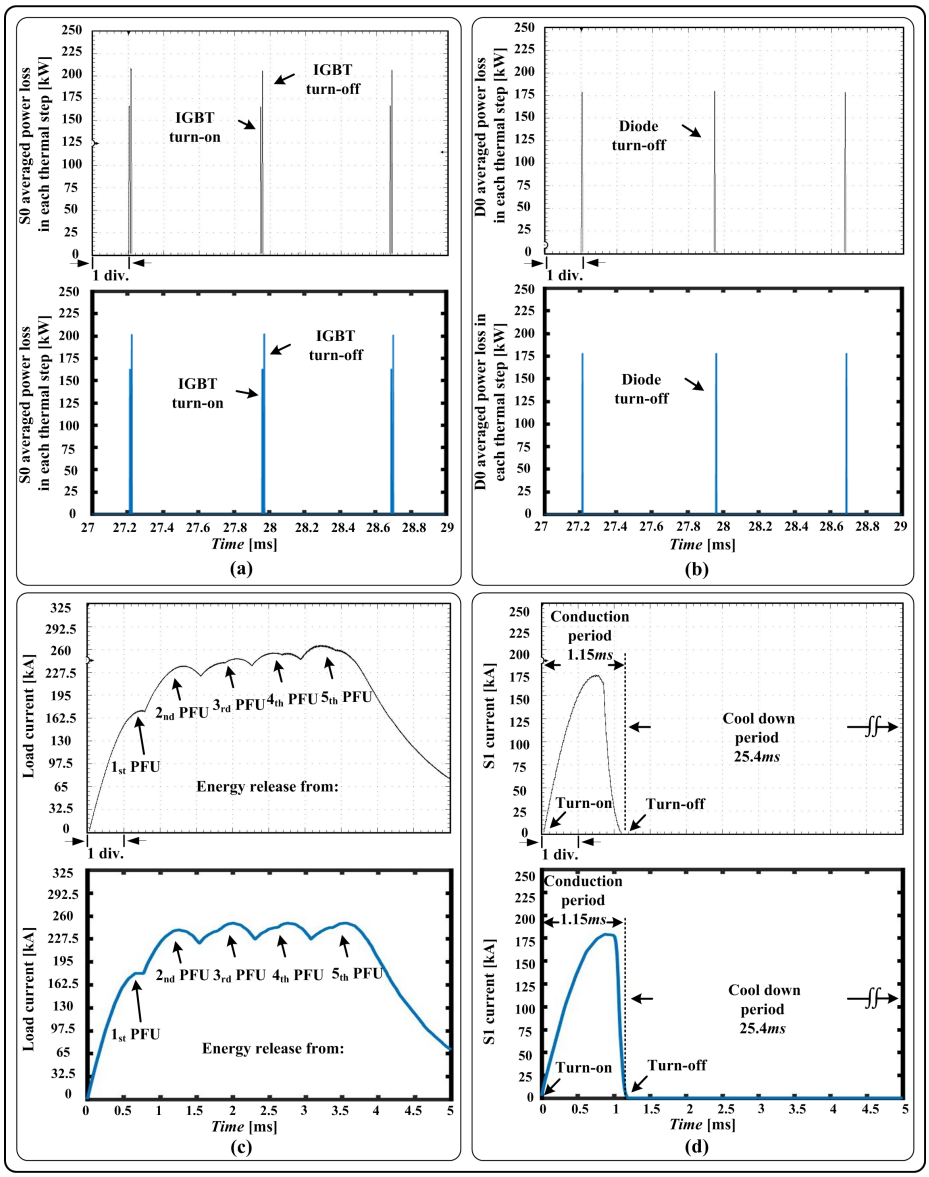

Figure 3.13: System-level and device-level results for CC and PFN from real-time hardware emulation (top sub-figure) and off-line simulation by SaberRD® software (bottom sub-figure) for: (a) S0 averaged power loss in each thermal step for the CC, (b) D0 averaged power loss in each thermal step for the CC, (c) Load current in the PFN, (d) S1 current in the PFN. Scale: (a)(b) x-axis: $0.2ms/\text{div}$. (c)(d) x-axis: $0.5ms/\text{div}$.

Table 3.6 shows the latencies of the PFN circuit with device-level behavioral and thermal calculation. The emulation time-step of the PFN is $2.5\mu s$ while the time-step of its thermal calculation is $10\mu s$. By applying smaller time-step, the accuracy of the thermal dynamic will not improved but the execution time can be enlarged enormously. The electrical circuit (PL) of the PFN updates the power loss to the thermal circuit (Core 1) every 4 steps. The thermal circuit (Core 1) updates the temperature dependent parameters to the electrical circuit (PL) in the next time-step. These temperature dependent parameters

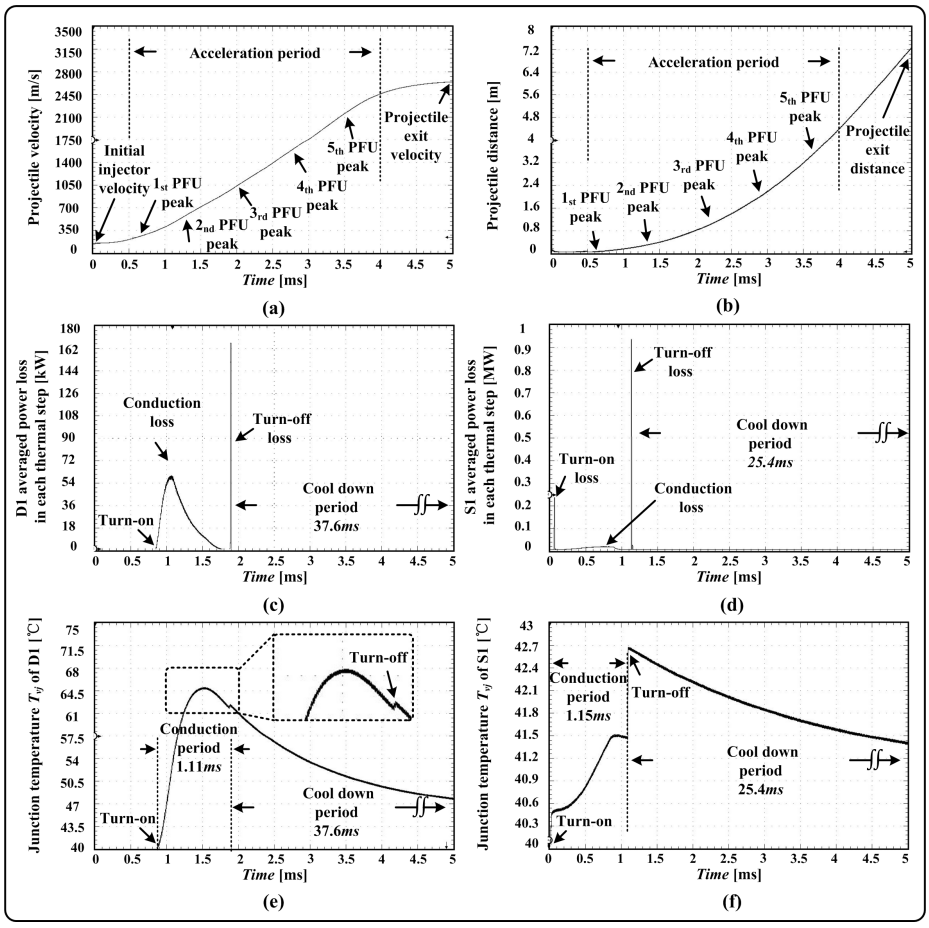

Figure 3.14: System-level and device-level results for the PFN from real-time hardware emulation for: (a) Projectile velocity, (b) Projectile distance, (c) D1 averaged power loss in each thermal step, (d) S1 averaged power loss in each thermal step, (e) Junction temperature of D1, (f) Junction temperature of S1. Scale: (a)-(f) x-axis: $0.5ms/$div.

Table 3.6: Latencies of PFN with Device-Level Behavioral (PL) and Thermal (PS-Core 1) Calculation and PS-PL Communication

PL HLS $100MHz$ (4 time-steps)	PS - Core 1 O3 $0.8GHz$	PL - PS	PS - PL	Average delay per time-step
$2280ns$	$875ns$	$2115ns$	$1525ns$	$1698.75ns$

has been applied in the Hammerstein configuration modeling in Section II. The latency of the electrical circuit (PL) of four time-steps, thermal circuit (Core 1), electrical to thermal circuit communication, and thermal to electrical circuit communication are $2280ns$, $875ns$, $2115ns$, and $1525ns$ respectively. Although the communication delay between the PS and PL is 20 times larger than the Core-Core one, the thermal and electrical circuit of PFN still run in real-time with the proper allocation of computation hardware resource. The averaged delay per time-step is less than the required time-step $2500ns$. The PL is controlled by

Table 3.7: Programmable Logic Resource Utilization for the PFN Circuit with Device-Level Behavioral Calculations

BRAM	DSP	FF	LUT
68 (6%)	390 (43%)	93418 (21%)	159979 (73%)

Core 1 and works as a hardware accelerator for the electrical circuit to compute the results of four time-steps.

Table 3.7 presents the programmable logic resource utilization of the PFN circuit. It is clear that the higher computation resource consumption is required due to the higher complexity of the device-level transient behavioral calculation.

In Fig. 3.15, the accuracy comparison of TSSM, the proposed HCM, and SaberRD® has been demonstrated. TSSM and HCM are implemented in the real-time SoC platform with a $100ns$ time-step. The execution times for the TSSM are shown in Table IV while the execution times for HCM are shown in Table VI and Table VII. The SaberRD® model is demostrated in $0.1ns$ and $20ns$ time-step. The SaberRD® model cannot converge at the $100ns$ time-step and the accuracy of the $20ns$ result gets worse in the simulation, especially during the IGBT turn-on and diode turn-off periods. SaberRD® takes 1.5 hours with a $0.1ns$ time-step and 92 seconds with a $20ns$ time-step for a $10ms$ simulation.

In Fig. 3.16, the frequency response of proposed Hammerstein behavioral models for the diode, thyristor, and IGBT are shown. The expanded windows show the normal operating frequency (circled). The highest switching frequency applied in the work for diode and IGBT is $14kHz$. Although the thyristor is not switching at $60Hz$ (circled) in this work, it can be considered as the reference for normal phase control switching frequency. The temperature variation has little impact on the frequency response. The operating range for the proposed diode, thyristor, and IGBT model are 0 - $0.882MHz$, 0 - $2830Hz$, and 0 - $0.54MHz$ respectively within 1% error.

In Table 3.8, the switching times and average power dissipation of diode, thyristor, and IGBT are compared from off-line SaberRD® simulation and real-time SoC emulation under two conditions. The first condition is that the CC is switching at a steady frequency at $14kHz$. The second condition is during the energy release period of a single PFU. The time-step for SaberRD® and SoC emulation is $0.1ns$ and $100ns$, respectively. As can be seen, there is good agreement of the results.

3.5 Summary

This chapter proposed and emulated the real-time device-level dynamic electro-thermal models for diode, thyristor and IGBT based on Hammerstein configuration on a SoC-based hardware and software co-design platform for the application of EMRG system. The Hammerstein configuration modeling procedures reduces the complexity of building

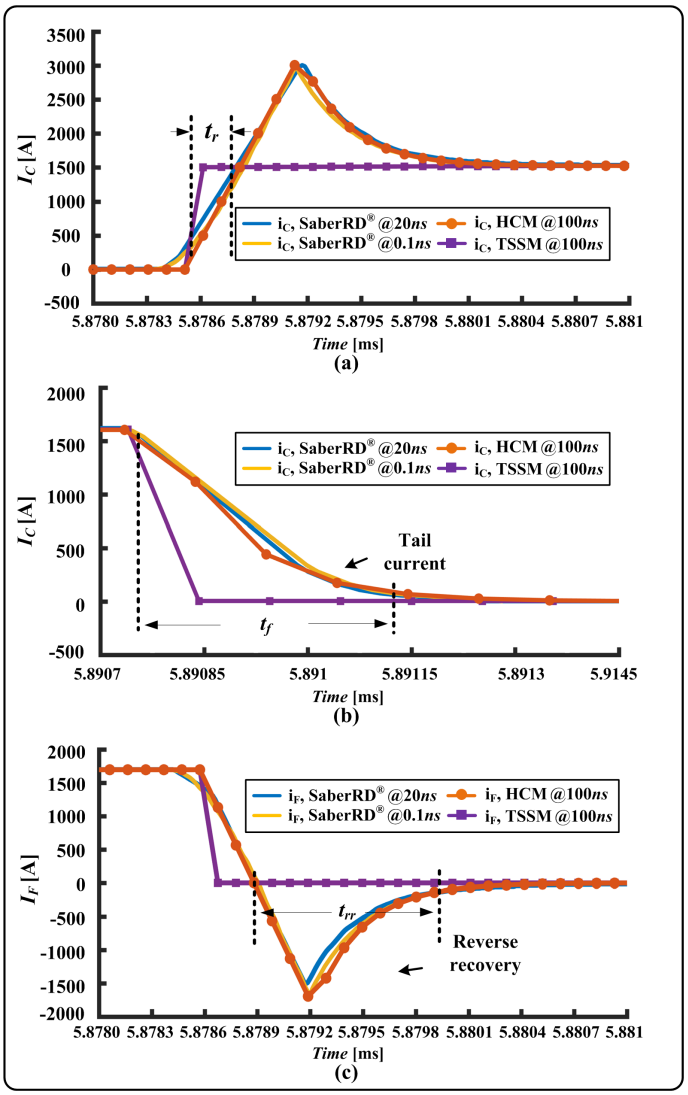

Figure 3.15: Accuracy comparison of TSSM, HCM models with SaberRD® for: (a) IGBT turn-on, (b) IGBT turn-off, (c) diode turn-off.

accurate device-level power electronic models. The modeling procedure of the static and dynamic electrical model, transient power loss model and thermal network calculation is given based on the dedicated device datasheet. The proposed models have been validated in two circuits of the EMRG system and compared with the result from the off-line device level software SaberRD®. Based on the different topology of the CC and the pulse forming network circuit inside the EMRG system, the hardware compute performance comparison, selection, and acceleration have enabled the goal of real-time execution. Future work is planned for the application of the Hammerstein based nonlinear modeling for more complex power converter systems for industrial applications.

Table 3.8: Comparison of Device Switching Times and Average Power Dissipation

	SaberRD®	SoC	Error (%)
CC switching at $14kHz$			
t_r(IGBT)	248.5ns	242.6ns	2.37
t_f(IGBT)	392.2ns	405.6ns	3.42
t_{rr}(Diode)	1041ns	1027ns	1.34
P_{on}(IGBT)	22.7kW	23.5kW	3.52
P_{off}(IGBT)	28.9kW	29.9kW	3.46
P_{cond}(IGBT)	0.38kW	0.40kW	5.26
P_{rr}(Diode)	25.2kW	25.3kW	0.47
P_{cond}(Diode)	0.16kW	0.17kW	6.25
PFU energy release in 5ms			
t_{rr}(Thyristor)	62.3μs	63.7μs	2.25
P_{rr}(Diode)	0.33kW	0.34kW	3.03
P_{cond}(Diode)	5.41kW	5.47kW	1.11
P_{rr}(Thyristor)	18.64kW	18.51kW	0.69
P_{cond}(Thyristor)	3.67kW	3.81kW	3.81

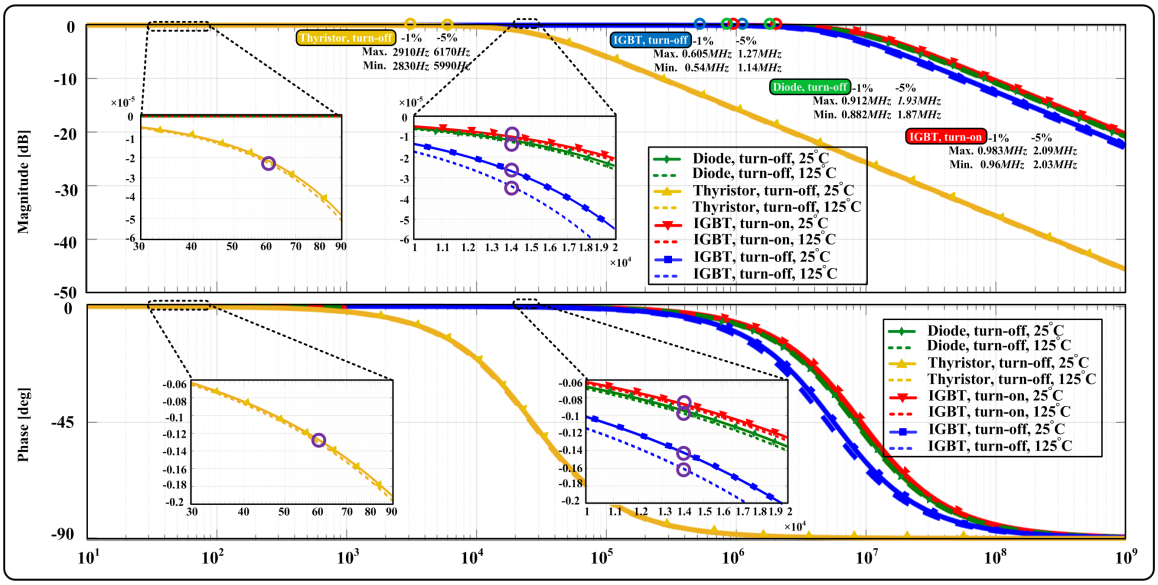

Figure 3.16: Frequency response of proposed Hammerstein configuration for diode, thyristor, and IGBT.

4

Real-Time Device-Level Simulation of MVDC Traction Power System on MPSoC

This chapter proposes the Wiener-Hammerstein configuration based device-level electro-thermal model for power electronic components, which is demonstrated with a three-phase to single-phase MMC-based traction power system in real-time emulation on the MPSoC platform. The timing of turn-on and turn-off carrier charging has been indicated and the equivalent circuit has been utilized for the dynamic calculation. The MMC sub-module device-level transients are simulated in the Cortex®-A53 Core with the latency of 90 ns for 100 ns per time-step in real world and the three-phase to the single-phase MMC-based traction power system is simulated on the programmable logic (FPGA) with the latency of 24.2μs for 25μs per time-step in real world. Both system-level and device-level results have been validated by professional power system software PSCAD/EMTDC® and power electronic simulation software SaberRD®. This is the original work for conducting large scale power converter system real-time emulation on the MPSoC-based platform.

4.1 Introduction

Modern electric railway system powered by galvanic cells dates back to early 1837. Traction power systems witnessed the significant changes at all level: switch technology (mer -cury-arc valves to IGBT) [81], [82], converter topology (mercury-arc rectifier to voltage source converter) [83] - [87], energy storage system (low energy density flywheel-based to high energy density supercapacitor-based) [88], [89], and advanced control methods (simple open-loop to complex self-adaptive) [90] - [92]. The design and development of a reliable, efficient, and cost-effective traction drive system is a complex process requiring several iterations on expensive and time-consuming hardware prototypes. Thus real-time

hardware-in-the-loop (HIL) emulation technology has come to play an essential role in the all transportation power systems and significantly reduced the cost in the early design period [93], [94]. Nevertheless, in almost all real-time system model implementation, the focus was mainly on the electric machine and propulsion components and seldom on the power electronic converters which were usually represented by simplified system-level models. With device-level model embedded into the HIL testing system, the power electronic system can be tautologically tested for the design in a non-destructive simulation environment which would allow an accurate prediction of converter stresses [95]. At the same time, advances in digital processor technology are enabling hardware acceleration HIL simulation with the integration of the multiple ARM® processors and FPGA-based programmable logic to function into a single chip [97]. FPGAs have been successfully utilized for real-time hardware emulation of detailed models of power systems and power electronic apparatus [95] - [98].

Conventional power converters, such as the two-level DC-AC converter, neutral point clamping (NPC), and flying capacitor (FC) topology, are deficient in handling high voltage and complicated voltage balancing. The MMC is considered as a strong candidate to overcome the shortcomings in conventional converters [87]. The advantages of MMC, such as flexible configuration, low applied voltage sub-modules, alternative sub-module source and strong harmonic suppression, gained broad application in wind farm [99], solar farm [100], railway system [85], and energy storage systems (ESS) [101].

Both the Hammerstein and the Wiener models are utilized in common behavioral models for various applications [102]. The single Hammerstein model contains a nonlinear static block and a linear time-invariant (LTI) dynamic block, which can not represent the exact prerequisites for physical processes. With the help of Wiener-Hammerstein structure, the proposed models can present the exact carrier charge processes before the turn-on and turn-off switching transient of the IGBT.

This chapter proposes the electro-thermal behavioral MMC models for device-level and sub-module level by using the Winner-Hammerstein configuration with the equivalent electrical element representation. For the traction power system, the detailed modeling and real-time simulation of the transformer also plays a non-negligible role in the transient analysis of traction power system. In the study case, the transformer nonlinear saturation behavior is also included in the real-time transient emulation, which presents critical technical and economic challenges to traction loads and system operators. The chapter is organized as follows: Section 4.2 explains the MMC-based traction power system, the MMC sub-module equivalent representation, and the transformer model. Section 4.3 describes the construction of IGBT module electro-thermal behavioral models by the Winner-Hammerstein configuration. Section 4.4 gives a brief introduction to the Zynq® MPSoC platform and the details of the implementation. Section 4.5 shows the device-level and system-level real-time emulation result and discussion.

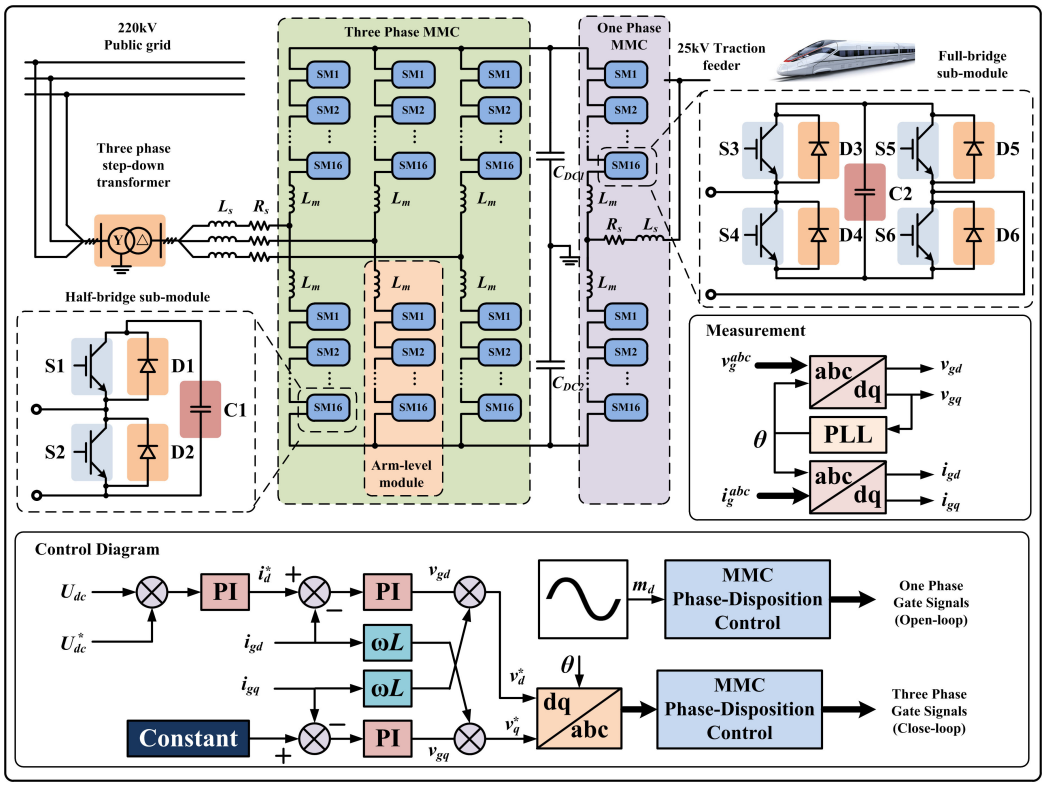

Figure 4.1: MMC-based traction power system.

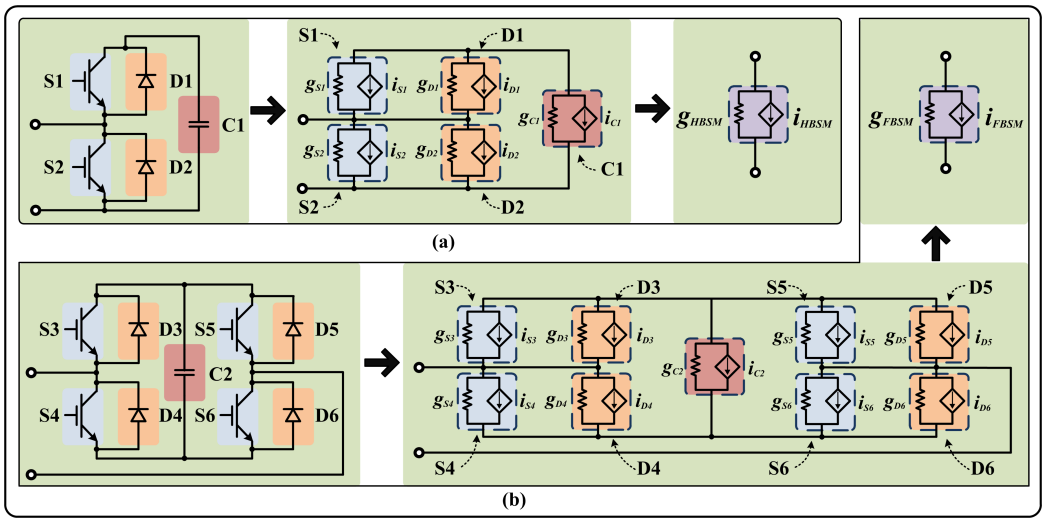

Figure 4.2: Hierarchical Norton equivalent process: (a) Half-bridge sub-module, (b) Full-bridge sub-module.

4.2 MMC-Based Traction Power System

The MMC-based traction power system, shown in Fig. 4.1, consists of the $220kV$ public grid, three-phase step-down transformer, three-phase MMC-based AC/DC converter and

single-phase MMC DC/AC converter. The three-phase MMC based AC/DC converter utilizes the half-bridge sub-module while the single-phase MMC DC/AC converter employs the full-bridge sub-module [83]. The half-bridge MMC lacks the DC fault blocking capability but requires less power electronic components, while the full-bridge MMC inherits the advantage of DC blocking features but increases the cost of the MMC system. In this work, three-phase half-bridge MMC is considered to reduce the cost on the grid side while single-phase full-bridge MMC is utilized on the load side to enable the DC fault blocking feature. The three-phase transformer includes the calculation of the nonlinear saturation behavior, and a wye-delta configuration is employed inside traction power system topology. The measurement unit calculates the dq transform of the three-phase grid-side voltage and current. With the phase-locked loop (PLL) calculation, the dq phase angle θ can be transmitted to the control system for closed-loop control. The control diagram of the traction power system is shown at the bottom of Fig. 4.1. The three-phase MMC is controlled by the DC link voltage and the objective of its control diagram is to maintain the voltage at the specific value. The single-phase MMC utilizes the open-loop control to operate at rated condition.

4.2.1 MMC Sub-Module

Fig. 4.2 shows the equivalent processes of the half-bridge and full-bridge sub-module into the combination of conductance and voltage controlled current source (VCCS). Each device inside the sub-module is reduced to a conductance paralleled with controlled current source in the Norton equivalent. After the reduction process, the half-bridge or full-bridge sub-module is equal to a conductance paralleled with VCCS. The Norton equivalent representation of half-bridge sub-module is shown in Fig. 4.2 (a), given as

$$g_{HBSM} = \frac{g_1 \cdot g_{c1}}{g_1 + g_{c1}} + g_2, \tag{4.1}$$

$$i_{HBSM} = \frac{i_1 \cdot g_{c1} - i_3 \cdot g_1}{g_1 + g_{c1}} + i_2, \tag{4.2}$$

$$i_j = i_{Sj} + i_{Dj}, j = 1, 2, \tag{4.3}$$

$$g_j = g_{Sj} + g_{Dj}, j = 1, 2, \tag{4.4}$$

where g_{HBSM} and i_{HBSM} are the equivalent conductance and VCCS of the half-bridge sub-module, respectively; g_{Sj} and i_{Sj} are equivalent conductance and VCCS of IGBT, respectively. g_{Dj} and i_{Dj} are equivalent conductance and VCCS of diode, respectively; g_j and i_j are equivalent conductance and VCCS of IGBT module, respectively.

The Norton equivalent representation of full-bridge sub-module is shown in Fig. 4.2

(b), given as

$$\begin{aligned} g_{FBSM} = (&g_3g_4g_5 + g_3g_4g_6 + g_3g_5g_6 + g_3g_5g_{C2} \\ &+ g_4g_5g_6 + g_3g_6g_{C2} + g_4g_5g_{C2} + g_4g_6g_{C2}) \\ &/(g_3g_4 + g_3g_6 + g_4g_5 + g_3g_{C2} + g_4g_{C2} \\ &+ g_5g_6 + g_5g_{C2} + g_6g_{C2}), \end{aligned} \tag{4.5}$$

$$\begin{aligned} i_{FBSM} = -(&M_1g_3g_4g_5 + M_2g_3g_4g_5 + M_1g_3g_5g_6 \\ &+ M_3g_3g_4g_5 + M_1g_3g_5g_{C2} + M_2g_3g_5g_6 \\ &+ M_3g_3g_4g_6 + M_1g_3g_6g_{C2} + M_2g_3g_5g_{C2} \\ &+ M_3g_3g_5g_6 + M_2g_4g_5g_{C2} + M_3g_3g_5g_{C2} \\ &+ M_3g_4g_5g_6 + M_3g_3g_6g_{C2} + M_3g_4g_5g_{C2} \\ &+ M_3g_4g_6g_{C2})/(g_3g_4 + g_3g_6 + g_4g_5 + g_3g_{C2} \\ &+ g_4g_{C2} + g_5g_6 + g_5g_{C2} + g_6g_{C2}), \end{aligned} \tag{4.6}$$

$$M_1 = -i_3/g_3 - i_4/g_4 + i_7/g_7, \tag{4.7}$$

$$M_2 = i_5/g_5 + i_6/g_6 - i_7/g_7, \tag{4.8}$$

$$M_3 = i_4/g_4 - i_6/g_6, \tag{4.9}$$

$$g_j = g_{Sj} + g_{Dj}, j = 3, 4, 5, 6, \tag{4.10}$$

$$i_j = i_{Sj} + i_{Dj}, j = 3, 4, 5, 6, \tag{4.11}$$

where g_{FBSM} and i_{FBSM} are the equivalent conductance and VCCS of the full-bridge sub-module, respectively. g_{Sj} and i_{Sj} are equivalent conductance and VCCS of IGBT, respectively; g_{Dj} and i_{Dj} are equivalent conductance and VCCS of diode, respectively; g_j and i_j are equivalent conductance and VCCS of IGBT module, respectively.

4.2.2 Transformer

In this work, the admittance matrix-based model is employed to model the transformer which includes the nonlinear saturation phenomena [98]. The admittance matrix is based on the mutually coupled coils concept. By applying Trapezoidal rule, the discrete-time difference equations are given as

$$\boldsymbol{i}_T(t) = \mathbf{G}\boldsymbol{v}_T(t) + \mathbf{hist}_T(t - \Delta t), \tag{4.12}$$

$$\begin{aligned} \mathbf{hist}_T(t - \Delta t) = &\mathbf{Y}_T\boldsymbol{v}_T(t - \Delta t) + \\ &(\mathbf{I}_T - 2\mathbf{G}_T\mathbf{R}_T)\,\mathbf{hist}_T(t - 2\Delta t), \end{aligned} \tag{4.13}$$

$$\mathbf{Y}_T = 2\left(\mathbf{G}_T - \mathbf{G}_T\mathbf{R}_T\mathbf{G}_T\right), \tag{4.14}$$

$$\mathbf{G}_T = \left[\mathbf{I}_T + \frac{\Delta t}{2}\mathbf{L}_T^{-1}\mathbf{R}_T\right]^{-1}\frac{\Delta t}{2}\mathbf{L}_T^{-1}. \quad (4.15)$$

where $\mathbf{R}_T$ is the diagonal matrix of winding resistance. $\mathbf{L}_T$ is the winding leakage inductances matrix; Δt is the electrical simulation time-step; $\mathbf{hist}_T(t-\Delta t)$ is nx1 history terms vector; $\mathbf{I}_T$ is the nxn identity matrix.

The nonlinear saturation phenomena can be seen in the transformer's continuous magnetization curve. Thus, the modeling of transformer with nonlinear saturation feature and Newton-Raphson iteration are necessary in the real-time simulation of traction power system, given as:

$$\mathbf{J}_T(\mathbf{i}_{j+1} - \mathbf{i}_j) = -\mathbf{F}_T(\mathbf{i}_j) \quad (4.16)$$

$$\mathbf{J}_T = \frac{\partial \mathbf{F}_T(\mathbf{i}_j)}{\partial \mathbf{i}_j} = \mathbf{R}_{thev} + \frac{\partial \mathbf{f}_T(\mathbf{i}_j)}{\partial \mathbf{i}_j} \quad (4.17)$$

$$-\mathbf{F}_T = \mathbf{v}_{oc} - \mathbf{R}_{thev}\cdot\mathbf{i}_j - \mathbf{f}_T(\mathbf{i}_j) \quad (4.18)$$

where $\mathbf{J}_T$ is the Jacobian matrix; $\mathbf{i}_j$ is the current vector at the jth iterations; $\mathbf{v}_{oc}$ is the open circuit voltage vector; $\mathbf{R}_{thev}$ is the Thévenin equivalent resistance matrix; $\mathbf{f}_T(\mathbf{i}_j)$ is the nonlinear function.

4.3 Wiener-Hammerstein Configuration Based Device-Level Behavioural Electro-Thermal Power Converter Model

In this section, Wiener-Hammerstein configuration is utilized to set up the modeling procedure in Section A. With behavioral modeling methodology, the modeling procedure is separated into the dynamic carrier charge stage in Section B, the static electrical characteristic in Section C, the dynamic electrical characteristic in Section D, and power consumption and thermal calculation in Section E. The IGBT module used in this work is 5SNA 1500E330305 from ABB® whose datasheet parameters are provided in [77]. In Table 4.1, datasheet plot utilization is shown in each modeling procedure.

4.3.1 Wiener-Hammerstein model Vs Wiener-Hammerstein Configuration

Wiener-Hammerstein model contains a nonlinear static block sandwiched between two LTI dynamic blocks while the Wiener-Hammerstein configuration separates the static block from the forward linear time variant (LTV) dynamic block and backward LTV dynamic block. The detail of Wiener-Hammerstein configuration is shown in Fig. 4.3.

The nonlinear static block of Wiener-Hammerstein model leads to iteration processes in the calculation. The Wiener-Hammerstein configuration can simplify the nonlinear static block into quasilinear one which results in reduction of computation. Compared with the LTI dynamic block, the forward and backward LTV dynamic blocks are considered have little impact on the system simulation result.

Table 4.1: Wiener-Hammerstein Configuration Modeling Procedure

Dynamic carrier charge	Static electrical characteristic	Dynamic electrical characteristic	Power consumption and thermal calculation
V_{GE}-Q_g, C-V_{CE}, $t_{d,on}$- R_G, $t_{d,off}$- R_G	I_C-V_{CE}, I_F-V_F	t_r- I_c, t_f- I_c, t_r- R_G, t_f- R_G, Q_{rr}- I_F, I_{rr}- I_F, Q_{rr}- di/dt, I_{rr}- di/dt	E_{on}^{IGBT}-I_C, E_{off}^{IGBT}-I_C, E_{on}^{IGBT}-R_G, E_{off}^{IGBT}-R_G, E_{rec}- I_F, E_{rec}- di/dt, Z_{thjc}^{IGBT}-t, Z_{thjc}^{Diode}-t

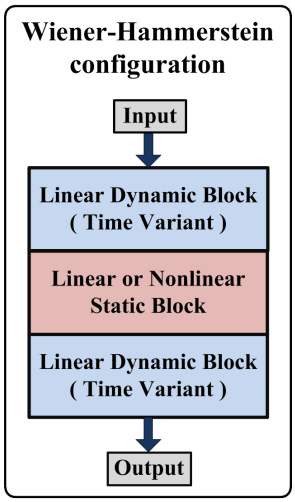

Figure 4.3: Wiener-Hammerstein configuration.

4.3.2 Dynamic Carrier Charge and Discharge Electrical Characteristic

The carrier charge and discharge stage can be considered as a prerequisite condition to the dynamic turn-on and turn-off transients. The equivalent IGBT capacitance circuit is shown in Fig. 4.4 (a). $R_{G(int)}$ represent the equivalent internal resistance. The static gate charge plot is shown in Fig. 4.4 (b) and linear approximation is applied for different V_{cc}. The relation of the parasitic and the low-signal capacitances are given as

$$C_{ies} = C_{GE} + C_{GC}, \tag{4.19}$$

$$C_{res} = C_{GC}, \tag{4.20}$$

$$C_{oes} = C_{GC} + C_{CE}. \tag{4.21}$$

where C_{ies}, C_{res} and C_{oes} are the input capacitance, the reverse transfer capacitance and output capacitance, respectively; C_{GE}, C_{GC} and C_{CE} are the gate-emitter capacitance, gate-collector capacitance and collector-emitter capacitance, respectively.

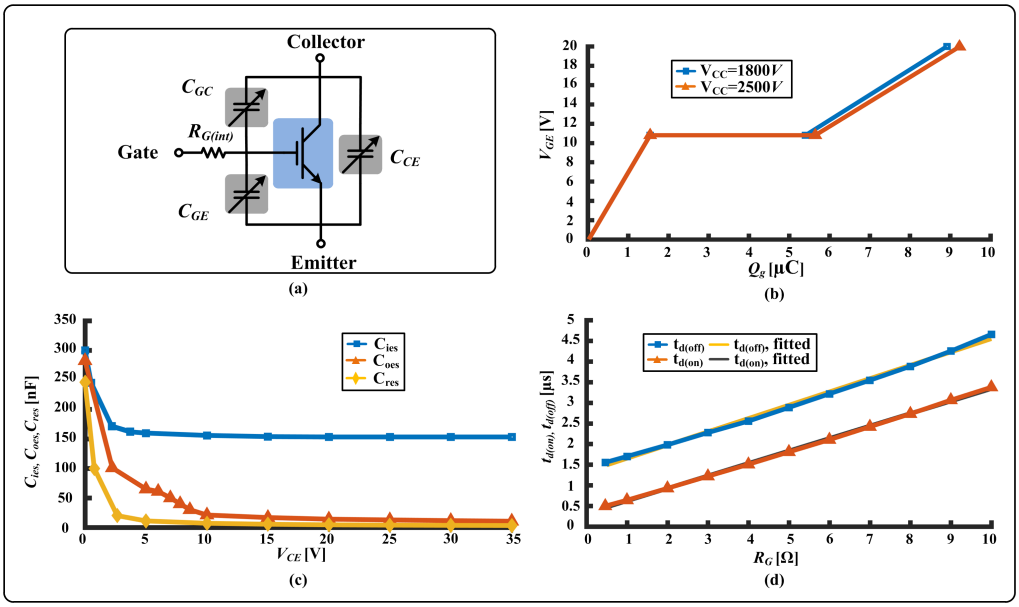

Figure 4.4: Carrier charge: (a) Capacitance equivalent circuit, (b) Static gate charge, (c) Low-signal capacitance, (d) IGBT turn-on and turn-off delay time.

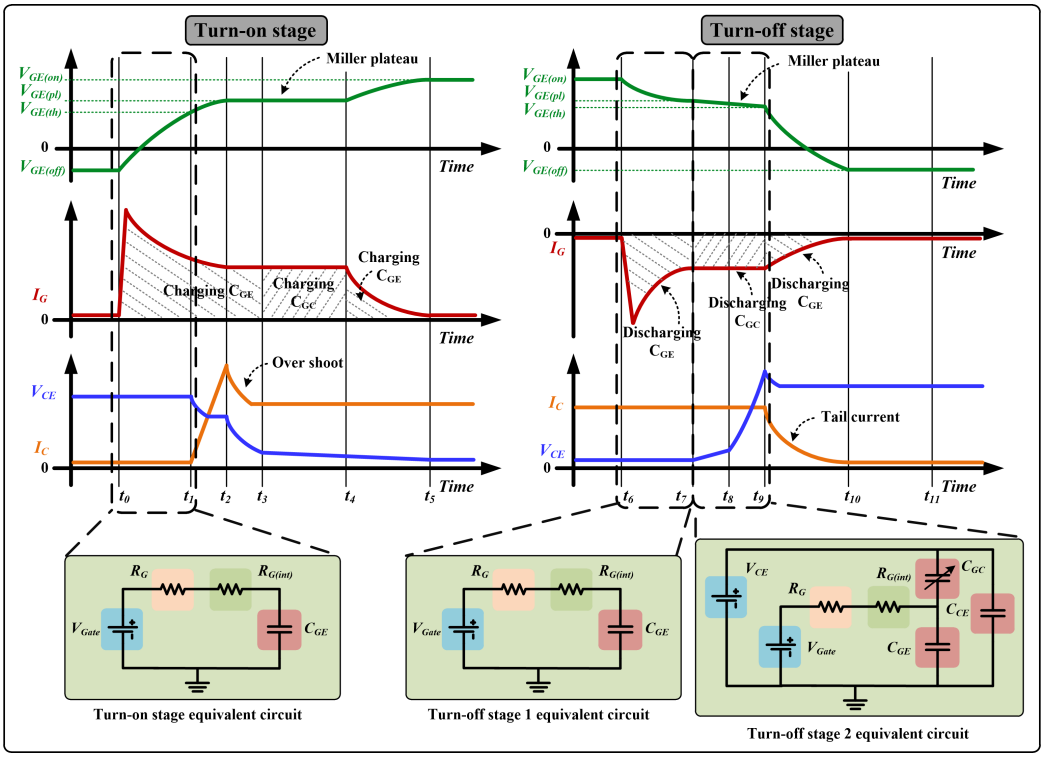

Figure 4.5: Carrier charge procedures for turn-on stage and turn-off stage and its equivalent circuit.

The low-signal capacitance is not constant in the application, and the relation between the V_{CE} and capacitance is given in Fig. 4.4 (c). The gate resistance value has a linear relation with the turn-on and turn-off delay time, shown in Fig. 4.4 (d).

The physical carrier charge and discharge procedures and the equivalent circuit are shown in Fig. 4.5. The detailed explanation of each stage will be described separately.

Turn-on stage:

t_0 - t_1: The gate current I_G rockets up and start to decay to a constant value. The gate-emitter capacitor C_{GE} is charged to the turn-on threshold voltage.

t_1 - t_2: The voltage of the gate-emitter capacitor C_{GE} reaches the threshold voltage $V_{GE(th)}$ and continue to rise to the Miller plateau voltage, which will trigger the turn-on transient. The collector current I_C starts ramping up with the overshoot phenomenon.

t_2 - t_3: The collector current I_C rising stage is finished at t_2 and V_{CE} begin to decrease. The voltage of the gate-emitter capacitor C_{GE} remain in a stable range until the Miller plateau charge procedure is finished.

t_3 - t_4: The Miller plateau charge procedure continues. The gate-collector capacitor C_{GC} is being charged.

t_4 - t_5: The charging procedure continues on the gate-emitter capacitor C_{GE} and its voltage reaches the desired gate voltage.

Turn-off stage:

t_6 - t_7: The gate current I_G cascades down and start to decay to a constant value. The gate-emitter capacitor C_{GE} is discharged to the Miller plateau voltage.

t_7 - t_8: The voltage of gate-emitter capacitor V_{GE} decrease to the Miller plateau and the collector-emitter voltage V_{CE} increase slowly due to the nonlinear features of C_{GC} which is a small value at this stage.

t_8 - t_9: The value of C_{GC} becomes large and the V_{CE} increases rapidly to the normal operating point.

t_9 - t_{10}: The voltage of gate-emitter capacitor V_{GE} decrease to threshold voltage and the collector current I_C starts to decay.

The equivalent circuit of the gate charge and discharge in Fig. 4.5. For the turn-on stage, the equivalent circuit is a typical RC first-order delay one. The turn-on delay time is highly relative to the gate resistance, given as

$$t_{d(on)} = K_{on} \cdot C_{GE} \cdot (R_{G(int)} + R_G). \tag{4.22}$$

where K_{on} is the gate charge parameter for turn-on transients and is related to the on-state gate voltage $V_{GE(on)}$ and off-state voltage $V_{GE(off)}$. $R_{G(int)}$ is considered as the internal parasitic resistance. In Fig. 4.4 (d), the linear fitted result also proves its linearity for the turn-on delay time.

For the turn-off stage, the turn-off stage 1 also is considered as an typical RC first-order delay circuit and the turn-off stage 2 can be considered as a constant time procedure. The

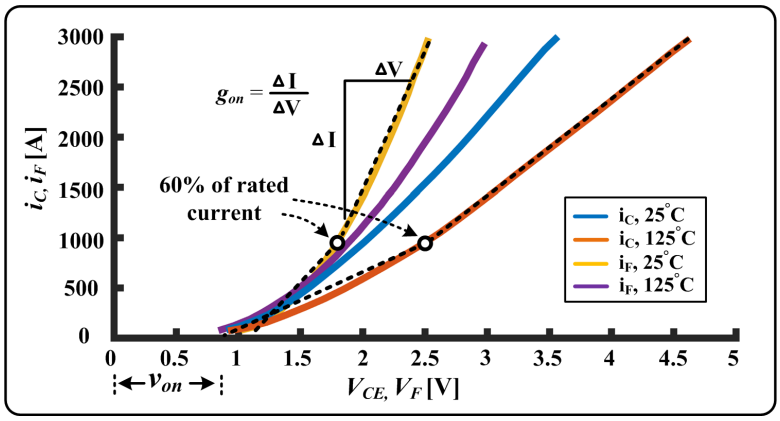

Figure 4.6: Static characteristic of IGBT and diode.

turn-off delay time is highly relative to the gate resistance, given as

$$t_{d(on)} = K_{off} \cdot C_{GE} \cdot (R_{G(int)} + R_G) + t_{stage2}. \tag{4.23}$$

where K_{on} is the gate charge parameter for turn-on transients and is related to the on-state gate voltage $V_{GE(on)}$ and off-state voltage $V_{GE(off)}$. t_{stage2} is considered as a constant time for turn-off stage 2. In Fig. 4.4 (d), the linear fitted result also proves its linearity for the turn-off delay time.

4.3.3 Static Electrical Characteristic

The IGBT and diode static characteristic is shown in Fig. 4.6. For MMC application, the collector current of the IGBT module varies each time based on the control algorithm. It is necessary to model the low current static characteristic in MMC scenario. Thus the static characteristic separates into low current and normal operating current sections and the boundary of these sections is defined as 60% of the rated current point. The static electrical model is made of a temperature dependent conductance $g_{low}(T_{vj})$ or $g_{high}(T_{vj})$ in paralleled with a temperature dependent VCCS $i_{low}(T_{vj})$ or $i_{high}(T_{vj})$ which is the Norton equivalent expression of the $v_{low}(T_{vj})$ or $v_{high}(T_{vj})$. High conductance and a paralleled VCCS represent for the on-state characteristic while low conductance behaves for the off-state characteristic. Based on the datasheet plots, the linear interpolation estimation method has been applied to $g_{low}(T_{vj})$, $g_{high}(T_{vj})$, $v_{low}(T_{vj})$ and $v_{high}(T_{vj})$, given as

$$g_{low}(T_{vj}) = \frac{T_{vj}-T_{25}}{T_{25}-T_{125}}(g_{low}^{T_{25}} - g_{low}^{T_{125}}) + g_{low}^{T_{25}}, \tag{4.24}$$

$$v_{low}(T_{vj}) = \frac{T_{vj}-T_{25}}{T_{25}-T_{125}}(v_{low}^{T_{25}} - v_{low}^{T_{125}}) + v_{low}^{T_{25}}, \tag{4.25}$$

$$i_{low}(T_{vj}) = v_{low}(T_{vj}) \cdot g_{low}(T_{vj}). \tag{4.26}$$

$$g_{high}(T_{vj}) = \frac{T_{vj}-T_{25}}{T_{25}-T_{125}}(g_{high}^{T_{25}} - g_{high}^{T_{125}}) + g_{high}^{T_{25}}, \tag{4.27}$$

$$v_{high}(T_{vj}) = \frac{T_{vj}-T_{25}}{T_{25}-T_{125}}(v_{high}^{T_{25}} - v_{high}^{T_{125}}) + v_{high}^{T_{25}}, \tag{4.28}$$

$$i_{high}(T_{vj}) = v_{high}(T_{vj}) \cdot g_{high}(T_{vj}). \tag{4.29}$$

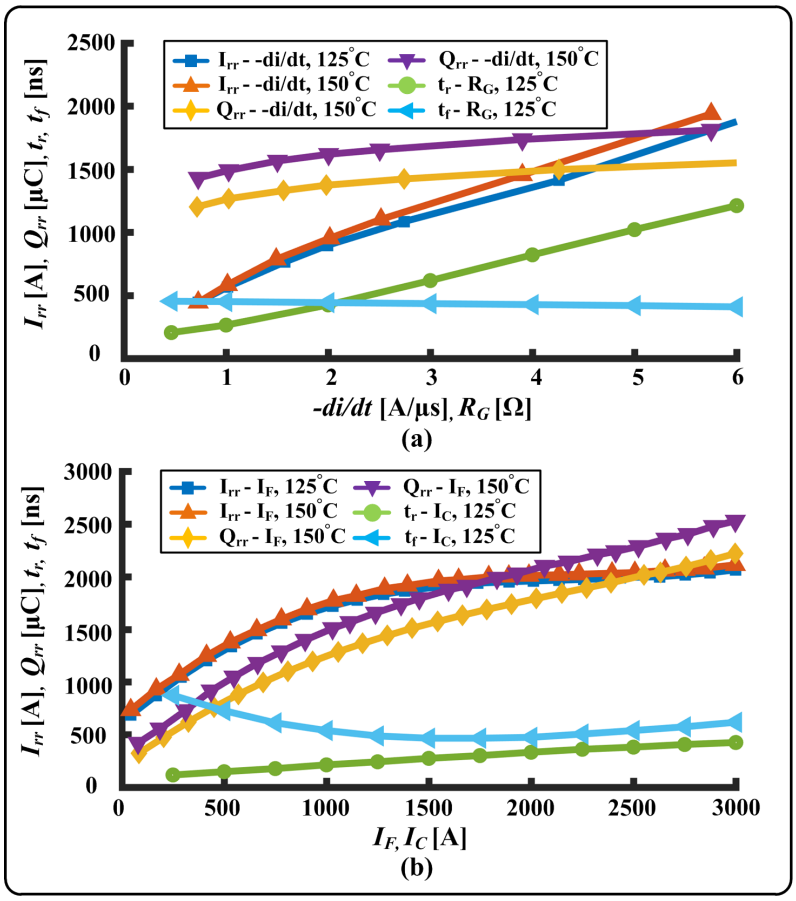

Figure 4.7: Dynamic characteristic: (a) Diode I_{rr} - di/dt, Q_{rr}- di/dt curves and IGBT t_r - R_G, t_f - R_G curves, (b) Diode I_{rr} - I_F, Q_{rr} - I_F curves and IGBT t_r - I_c, t_f - I_c curves.

where $g_{low}(T_{vj})$, $g_{high}(T_{vj})$, $i_{low}(T_{vj})$ and $i_{high}(T_{vj})$ are low-current region conductance, high-current region conductance, low-current region VCCS, high-current region VCCS, respectively.

4.3.4 Dynamic Electrical Characteristic

The dynamic characteristic parameters for the diode and IGBT are shown in the Fig. 4.7.

4.3.4.1 Diode

Compared to turn-off transient, the forward recovery phenomenon and energy loss in the turn-on period can be negligible. Reverse recovery phenomenon is considered as the major dynamic transient of diode. The VCCS $i_{low}(T_{vj})$ or $i_{high}(T_{vj})$ plays an important role in the turn-off operation with default blocking state for $g_{low}(T_{vj})$ or $g_{high}(T_{vj})$. As shown in Fig. 4.8, the dynamic transients of reverse recovery phenomenon are separated into three stages: 1) default static state, 2) linear reverse recovery current decrease, 3) decay stage of reverse recovery current. The decay of stage 3 is considered as a first-order delay

approximation curve. The reverse recovery time t_{rr} is estimated by the equation, given as

$$t_{rr} = \frac{2Q_{rr}}{I_{rr}}. \tag{4.30}$$

4.3.4.2 IGBT

The dynamic characteristics of IGBT can be separated into two part: 1) turn-on, 2) turn-off. For the turn-on period, the physic procedure of collector current I_c can be considered as a first-order delay approximation. For the turn-off period, the collector current I_c decreases at the rate of negative di/dt , given by

$$\frac{dI_c}{dt} = \frac{L_{stray}}{V_L}. \tag{4.31}$$

where V_L is the transient overshoot voltage on the IGBT at the time of t_9, shown in Fig. 4.5. After the linear decrease period, I_c begin to decay as a first-order approximation.

2.197τ is considered as the normalized time of the collector current rise and fall time of IGBT. With the calculation of the normalized variable τ, the dynamic shape of the waveform can be determined.

4.3.5 Transient Power and Voltage Reconstruction

The total power loss for a dedicated on or off transients in a single device can be derived from the datasheet under the specific circumstance. The detailed transient waveform, shown in Fig. 4.9, can be utilized to calculate the transient power loss. Both the device current and voltage have been normalized while its transient power degrades to a certain percentage in order to explain the relationship among current, voltage, transient power.

Diode turn-off transient power, shown in Fig. 4.9 (a), is separated into square and first-order delay region, given as

$$P_{Loss}^{Diode} = \int_{t_{dio1}}^{t_{dio2}} a_1 x^2 + \int_{t_{dio2}}^{\infty} (a_2 e^{-x} + c_2) \tag{4.32}$$

where P_{Loss}^{Diode} is the total power loss of the diode. t_{dio1} and t_{dio2} indicate the start time of linear region and first-order delay region, respectively; a_1 is the constant for linear approximation; a_2 and c_2 are the constants for the first-order delay approximation calculation.

IGBT turn-on transient power, shown in Fig. 4.9 (b), is separated into positive linear, square and first-order delay region, given as

$$\begin{aligned} P_{LossOn}^{IGBT} = &\int_{t_{IGBT1}}^{t_{IGBT2}} a_3 x + \int_{t_{IGBT2}}^{t_{IGBT3}} (a_4 x^2 + c_4) \\ &+ \int_{t_{IGBT3}}^{\infty} (a_5 e^{-x} + c_5) \end{aligned} \tag{4.33}$$

where P_{LossOn}^{IGBT} is the total power loss of the IGBT during the turn-on period. t_{IGBT1}, t_{IGBT2} and t_{IGBT3} indicate the start time of collector current linear region, collector current and

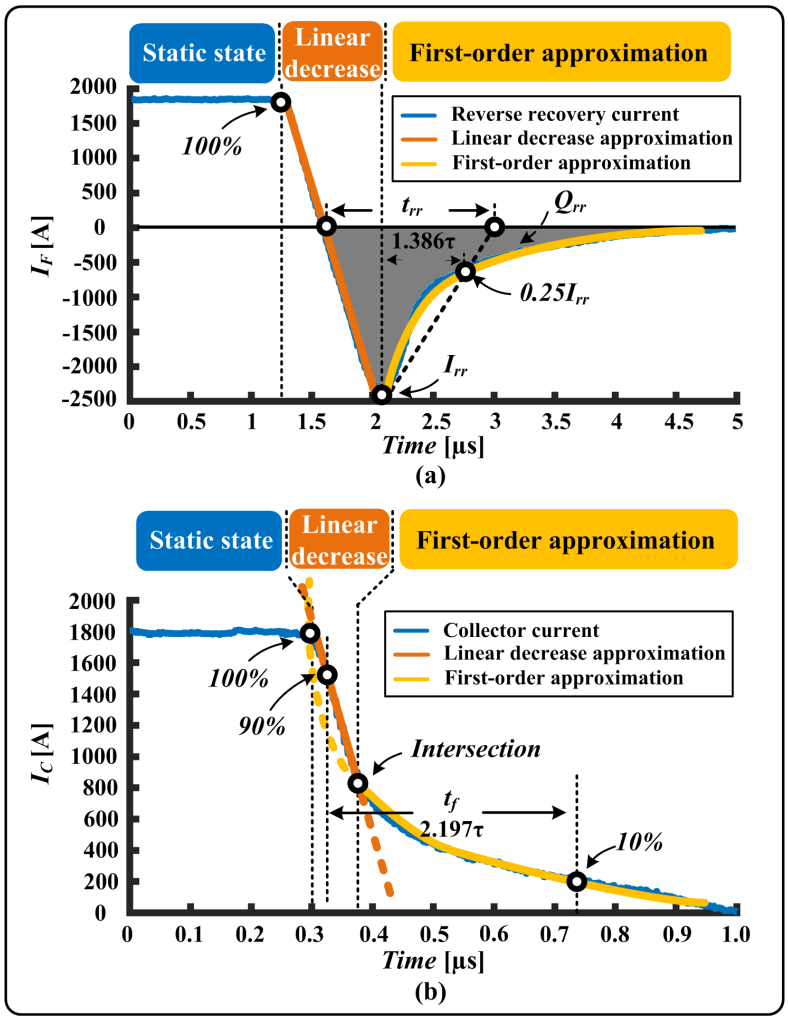

Figure 4.8: Dynamic characteristics: (a) Diode reverse recovery, (b) IGBT tail current.

collector-emitter voltage linear region and first-order delay region, respectively; a_3, a_4, c_4, a_5 and c_5 are the constants for the approximation calculation.

IGBT turn-off transient power, shown in Fig. 4.9 (c), is separated into positive linear, negative linear and first-order delay region, given as

$$P_{LossOff}^{IGBT} = \int_{t_{IGBT4}}^{t_{IGBT5}} a_6 x + \int_{t_{IGBT5}}^{t_{IGBT6}} (-a_7 x + c_7) + \int_{t_{IGBT6}}^{\infty} (a_8 e^{-x} + c_8) \tag{4.34}$$

where $P_{LossOff}^{IGBT}$ is the total turn-off power loss of the IGBT; t_{IGBT5}, t_{IGBT6} and t_{IGBT7} indicate the start time of collector-emitter voltage linear increase region, collector current linear decrease region and collector current first-order delay decrease region, respectively; a_6, a_7, c_7, a_8 and c_8 are the constants for the approximation calculation.

By calculating the above waveform, the exact transient power loss at each moment can

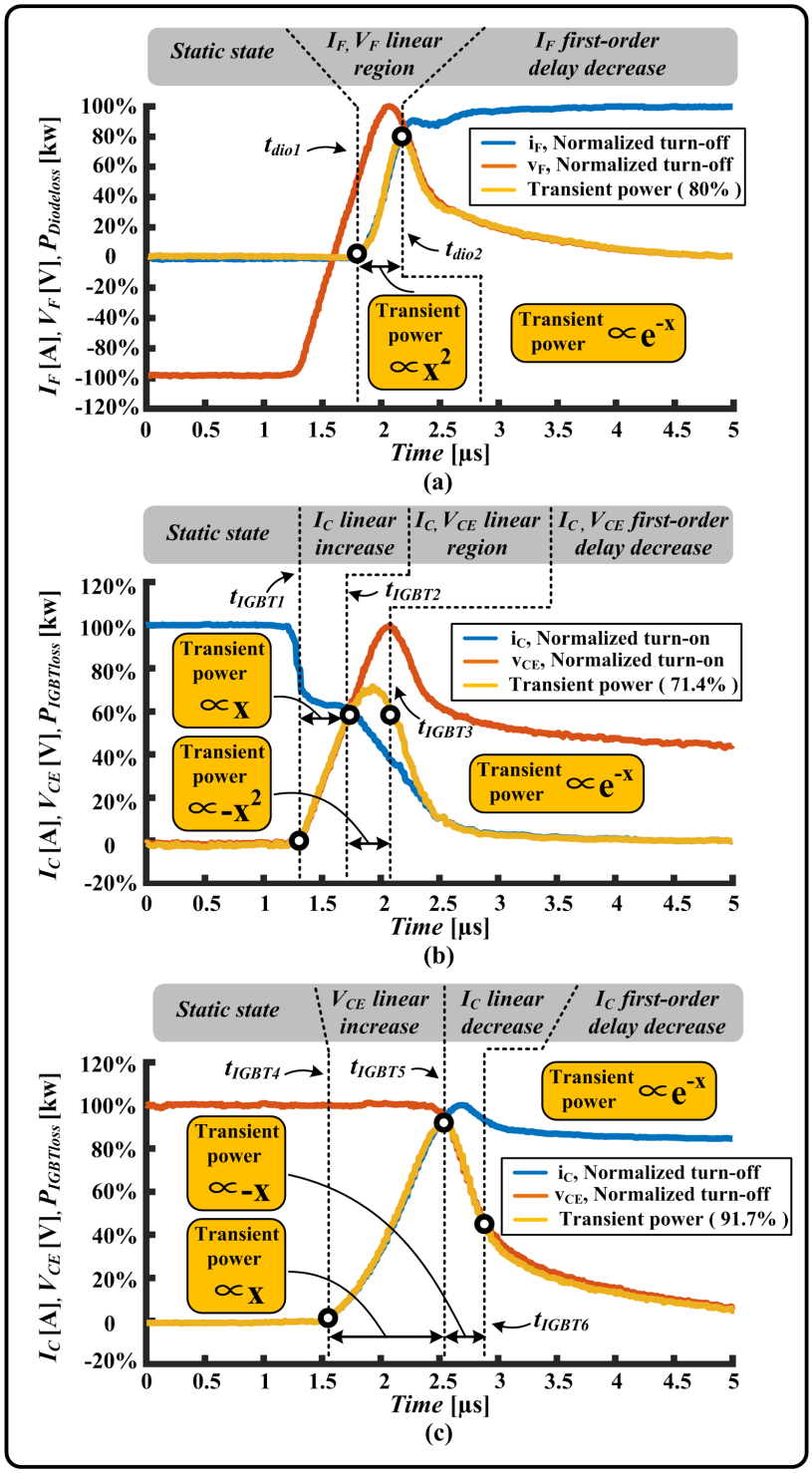

Figure 4.9: Normalized transient power waveform: (a) Diode turn-off, (b) IGBT turn-on, (c) IGBT turn-off.

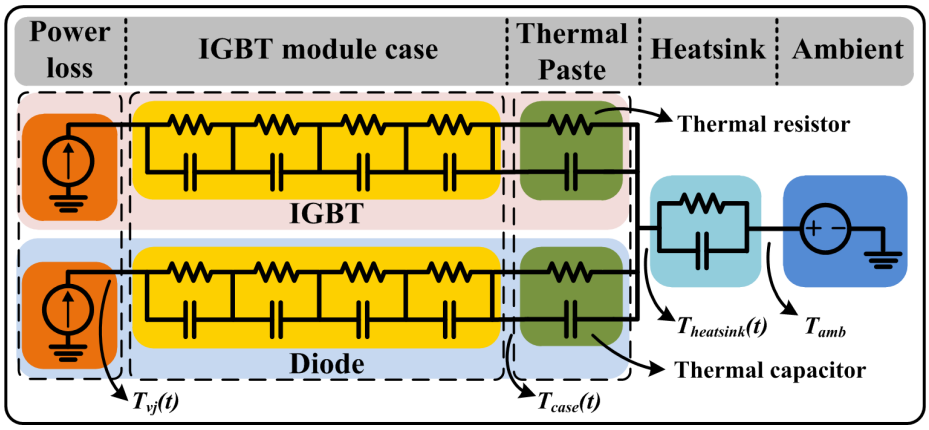

Figure 4.10: Thermal calculation circuit of IGBT module.

be determined and the device terminal voltage can be obtained.

4.3.6 Thermal Network Calculation

The thermal calculation circuit is shown in Fig. 4.10. The VCCS indicates the power loss consumption. Multiple levels of equivalent electrical components have been applied for computing the junction temperature, given as

$$T_{vj}(t) = P_{loss}(t) \cdot (Z_{thjc} + Z_{thch} + Z_{thha}) + T_{amb}. \tag{4.35}$$

where $P_{loss}(t)$ is the power loss for each device; T_{amb} is the ambient temperature; Z_{tjc} is the thermal impedance from junction to case; Z_{tch} is the thermal impedance from case to heat sink; Z_{tha} is the thermal impedance from heat sink to ambient. A 10K/kW water-cooled heat sink is mounted on each IGBT module in this work. The junction temperature numerical solution is given as

$$\begin{aligned}
T_{vj}(t) &= \sum_{i=1}^{6} \Delta T_{th}^{i}(t) + T_{amb} \\
&= \sum_{i=1}^{5} \left(\frac{R_{th}^{i} \cdot \Delta t_{thm}}{2\tau_{th}^{i} + \Delta t_{thm}} (P_{loss}(t) + P_{loss}(t - \Delta t_{thm})) \right. \\
&\left. + \frac{2\tau_{th}^{i} - \Delta t_{thm}}{2\tau_{th}^{i} + \Delta t_{thm}} \Delta T_{th}^{i}(t - \Delta t_{thm})\right) \\
&+ \frac{R_{th}^{6} \cdot \Delta t_{thm}}{2\tau_{th}^{6} + \Delta t_{thm}{}_{6}} (P_{total}(t) + P_{total}(t - \Delta t_{thm})) \\
&+ \frac{2\tau_{th}^{6} - \Delta t_{thm}}{2\tau_{th}^{6} + \Delta t_{thm}} \Delta T_{th}^{6}(t - \Delta t_{thm}) + T_{amb},
\end{aligned} \tag{4.36}$$

where Δt_{thm} is the thermal time-step; $\Delta T_{th}^{i}(t)$ is the node point junction temperature for each layer; $P_{loss}(t)$ is the power loss for the individual device; T_{amb} is the ambient

temperature; τ_{th}^{i} is the multiplication product of R_{th}^{i} and C_{th}^{i}; $P_{total}(t)$ is the total power loss for each time-step in a single device.

4.4 Hardware and Software Co-Design and Implementation of MMC-Based Tration Power System on Zynq® Ultrascale+™ MPSoC Platform

System-level circuit simulation is applied inside the programmable logic to accelerate the computation speed. The calculation of the system-level circuit can be considered as matrix operations primarily which can be accelerated and paralleled by programmable logic (hardware design).

Device-level transients and system control are calculated in the processing system (software design). The computation of system control is applied inside the real-time core Cortex®-R5 operating at $600Mhz$. In each leg of the three-phase MMC and single-phase MMC, one sub-module is selected as the device-level transient calculation in each Cortex®-A53 respectfully. In a small-scale circuit, the simulation is highly sequential and not beneficial to be separated into multi-core operation due to high latency in core-core communication. With enough high operating frequency, a single core can be optimum for small-scale circuit simulation such as the sub-module in the MMC.

In each system-level time-step, the system control signal generated from the Cortex®-R5 will be transmitted to the programmable logic for system-level simulation and Cortex®-A53 for device-level simulation. Meanwhile, the programmable logic updates the history terms to the quad-core Cortex®-A53 processor which in-turn updates the result to programmable logic in the next time-step.

4.5 Real-Time Simulation Results and Discussion

4.5.1 Computing Hardware Resource Consumption and Computation Performance

In this subsection, the resource consumption and computation performance are explained in detail. The resource consumption is focused on the FPGA hardware resource allocation. FPGA hardware resource consists of block RAMs, DSP slices, flip-flops, and LUTs. Whether the simulation system can be fitted into the hardware is depended on the highest percentage usage hardware resource. In this case, equal allocation of each type of hardware resource makes a difference in resizing the simulation system scale. Computation performance is focused on the execution speed of processing system. If the execution speed of the specific function is running faster than the real-time timing requirement, it can be considered as a real-time application.

Table 4.2 illustrates the programmable logic resource consumption for the MMC-based

Table 4.2: Resource Consumption for MMC-Based Traction Power System

Device	BRAM	DSP	FF	LUT
XCZU9EG	56 (3%)	908 (36%)	180895 (33%)	200167 (73%)

Table 4.3: Latencies of Sub-Module Device-Level Transients Simulation and Control System

A53 Core 1 O3 1.2GHz	A53 Core 2 O3 1.2GHz	A53 Core 3 O3 1.2GHz	A53 Core 4 O3 1.2GHz	R5 Core 1 O3 0.6GHz
90 ns	90 ns	90 ns	90 ns	7290 ns

traction power system. LUTs consumption percentage is the highest among all the other resources, up to 73%, followed by DSP (36%), flip-flops (33%) and BRAM (3%). The FPGA resource has been utilized for hardware computation acceleration. For example, large-scale matrix operation can be parallelized for execution in EMTP application. Since hardware resource applies low operating frequency in execution, slow processes such as the thermal calculation can also be calculated by applying FPGA hardware resource. In this case, high operating frequency cores can be allocated to highly sequential and time-consuming task.

Table 4.3 explains the latencies of each processing core. Each A53 Core is utilized to simulate the sub-module device-level transients and the resolution of the hardware timer is $10ns$. In that case, each core has an identical latency of execution ($90ns$) and exchanges the history terms to the programmable logic in the next system-level time-step. The two most common control methods are phase-shifted carrier-based PWM (PSC-PWM) and phase-disposition PWM (PD-PWM). Both methods have their advantages and disadvantages; However, based on the requirements of the real-time implementation, the consumption of the hardware resource for the control system is the most important criteria for selecting the control method for the MMC. PSC-PWM requires averaging control and balancing control on every sub-module. For a small scale (low number of levels) MMC topology, PSC-PWM does not require much hardware resources for real-time implementation. But for the scale of the study case in this manuscript, PD-PWM has a great advantage over PSC-PWM. The real-time Cortex®-R5 Core has been used for system control calculation including PD-PWM and DC link voltage balancing. Cortex®-A53 is operating at $1.2GHz$ and its code inside the MPSoC applied the highest optimization level (O3) of NEON parallel compute capability. Cortex®-R5 operates at $0.6GHz$ and also utilizes NEON O3 optimization capability. The system-level time-step is $25\mu s$ and the execution time of control system is $7.290\mu s$ which is less than the system-level time-step requirement. The maximum latencies of the Cores, calculating device-level electro-thermal models, are $90ns$ which is lower than the device-level time-step $100ns$. The communication latency is also an essential factor of the real-time implementation, which will be described in the next table.

Table 4.4: Latencies of Hardware Resource and Communication

PL HLS 100MHz	R5 Core 1 - A53 Core X	R5 Core 1 - PL	Maximun delay per time-step	Averaged delay per time-step
22.24μs	120ns	1840ns	24.6μs	24.2μs

Table 4.4 shows the latencies of hardware system-level calculation with sub-module thermal behavioral and communication. The system-level simulation time-step is 25μs. The averaged calculation and communication delay per time-step is 24.2μs which is lower than the system-level simulation time-step. The programmable logic takes 22.24μs to compute the system-level results while the sent and receive communication time of Cortex®-R5 Core to Cortex®-A53 Core and Cortex®-R5 Core to programmable logic are 120ns and 1840ns, respectively.

4.5.2 Real-Time Experimental Results

Fig. 4.11 (a) (b) (c) show the MMC terminal and source voltages. Fast Fourier Transform (FFT) has been used to analyze the high-frequency harmonic impact on the system. The three-phase and single-phase MMC terminal voltages show 17 levels voltage difference. It is not obvious to observe the stepped voltage difference in the three-phase MMC source voltage because of the resistance and inductance interconnection between the terminal and source point. From Fig. 4.11 (d) (e) (f), the most observable high harmonic frequency is about 3000Hz and its amplitude can be negligible compared to the one at 60Hz. The 3000Hz high-frequency harmonic is introduced by the carrier wave in the control system. Fig. 4.11 (g) (h) (i) give the upper arm current of the three-phase MMC. This work separates the full circuit topology 12×12 admittance matrix into two small 6×6 admittance matrix to accelerate the simulation speed by applying the transmission line modeling (TLM) method. Although the TLM may introduce small average error within 2% in the matrix calculation, the execution time make the real-time emulation possible, especially on the occasion requiring Newton-Raphson method.

The capacitance voltages of the MMC sub-module are shown Fig. 4.12. Four of the single-phase MMC capacitor voltages and zoomed-in figures are shown in Fig. 4.12 (a) and Fig. 4.12 (b), respectively. $V_{cap,a}$ varies from 2758 V and 2860 V. Four of the phase A capacitance voltage $V_{cap,a}$ from the three-phase MMC are shown on Fig. 4.12 (d) and Fig. 4.12 (e) is the zoomed-in figure. The range of $V_{cap,a}$ is between 2780 V and 2849 V and the voltage value between different capacitance varies within a small range. The variation percentage of capacitance in three-phase MMC is 2.4% while the one in single-phase MMC is 3.5%. For the selected time window, the control system and the traction MMC system became stable which is suitable for capacitance voltage value comparison on single-phase and three-phase MMC. Fig. 4.12 (c) shows the IGBT S2 turn-on and turn-off transients.

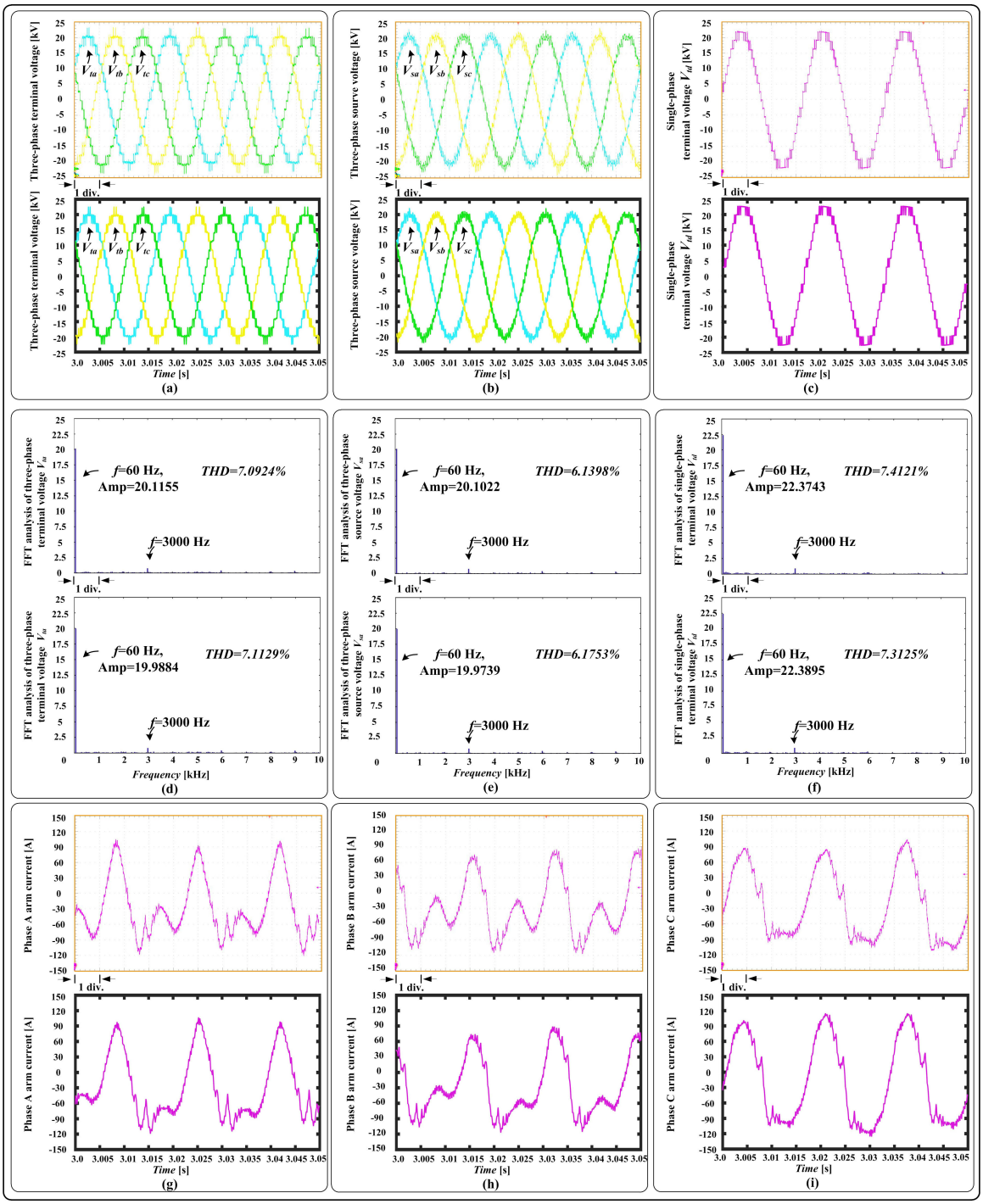

Figure 4.11: System-level results for MMC-based MVDC traction power system from real-time simulation (top oscilloscope sub-figure) and off-line simulation by PSCAD/EMTDC® software (bottom sub-figure) for: (a) Three-phase terminal voltage, (b) Three-phase source voltage, (c) Single-phase terminal voltage, (d) FFT analysis of three-phase terminal voltage, (e) FFT analysis of three-phase source voltage, (f) FFT analysis of single-phase terminal voltage, (g) Phase A arm current, (h) Phase B arm current, (i) Phase C arm current. Scale: (a) (b) (c) (g) (h) (i) x-axis: $5ms$/div. (d) (e) (f) x-axis: $1kHz$/div.

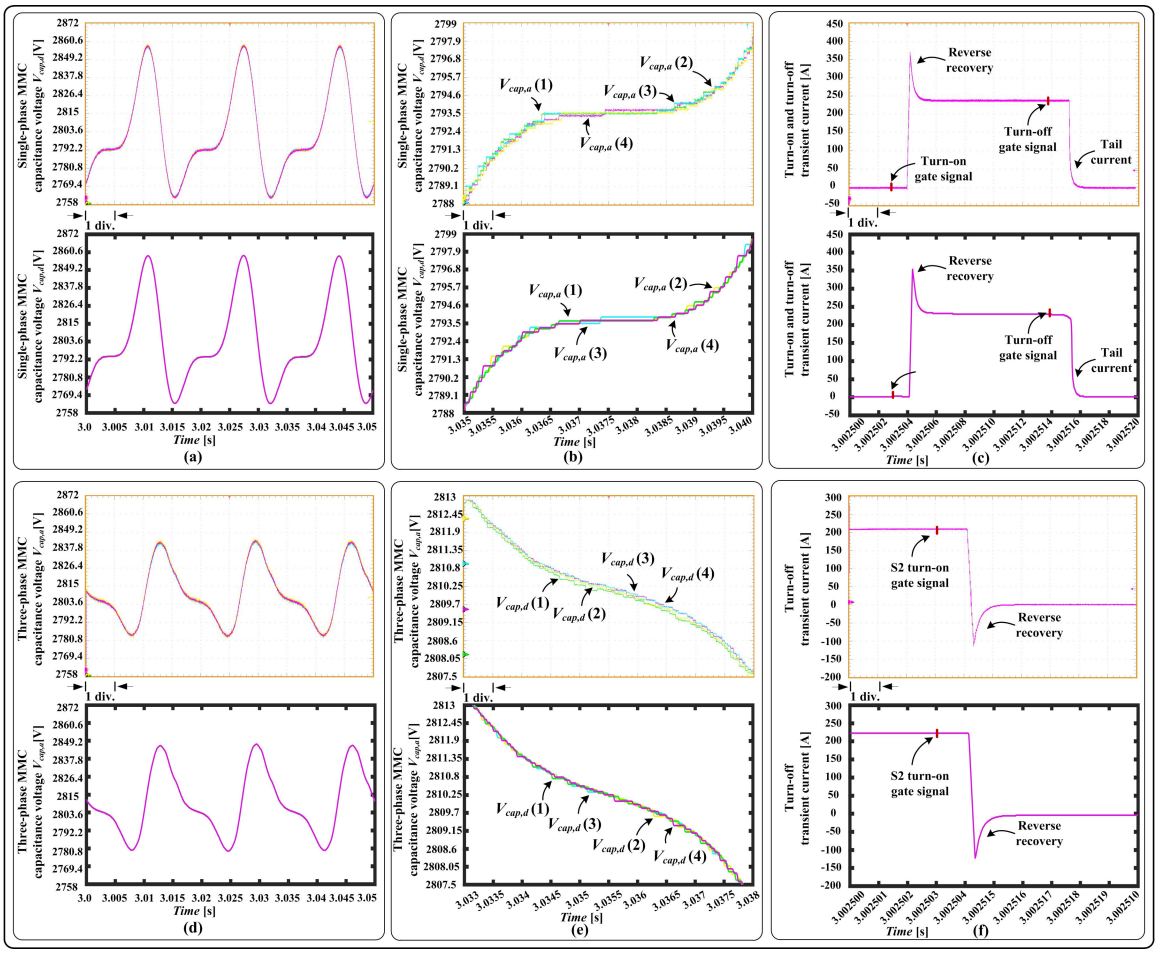

Figure 4.12: System-level and device-level results for MMC-based MVDC traction power system from real-time emulation (top oscilloscope sub-figure) and off-line simulation by PSCAD/EMTDC® or SaberRD® software (bottom sub-figure) for: (a) Single-phase MMC capacitance voltage, (b) Zoomed-in single-phase MMC capacitance voltage, (c) Turn-on and turn-off transient current for IGBT, (d) Three-phase MMC capacitance voltage, (e) Zoomed-in three-phase MMC capacitance voltage, (f) Turn-off transient current for diode. Scale: (a) (c) x-axis: $5ms$/div. (b) (e) x-axis: $0.5ms$/div. (c) x-axis: $2\mu s$/div. (f) x-axis: $1\mu s$/div.

When the turn-on gate signal is generated, the front linear dynamic block in the Wiener-Hammerstein configuration begins the calculation of carrier charge process. Once the gate-emitter capacitor inside the IGBT is charged to the turn-on threshold voltage, the front linear dynamic block triggers the linear static block and the back linear dynamic block. The linear static block calculates the device conductance and VCCS value in the static state. The back linear dynamic block estimates the transient period by first-order delay calculation. At the turn-on stage, the collector current ramps up with the overshoot phenomenon which is mainly introduced by the reverse recovery phenomenon by the diode D1, shown in Fig. 4.12 (f). When the turn-off gate signal is generated, the front linear dynamic block

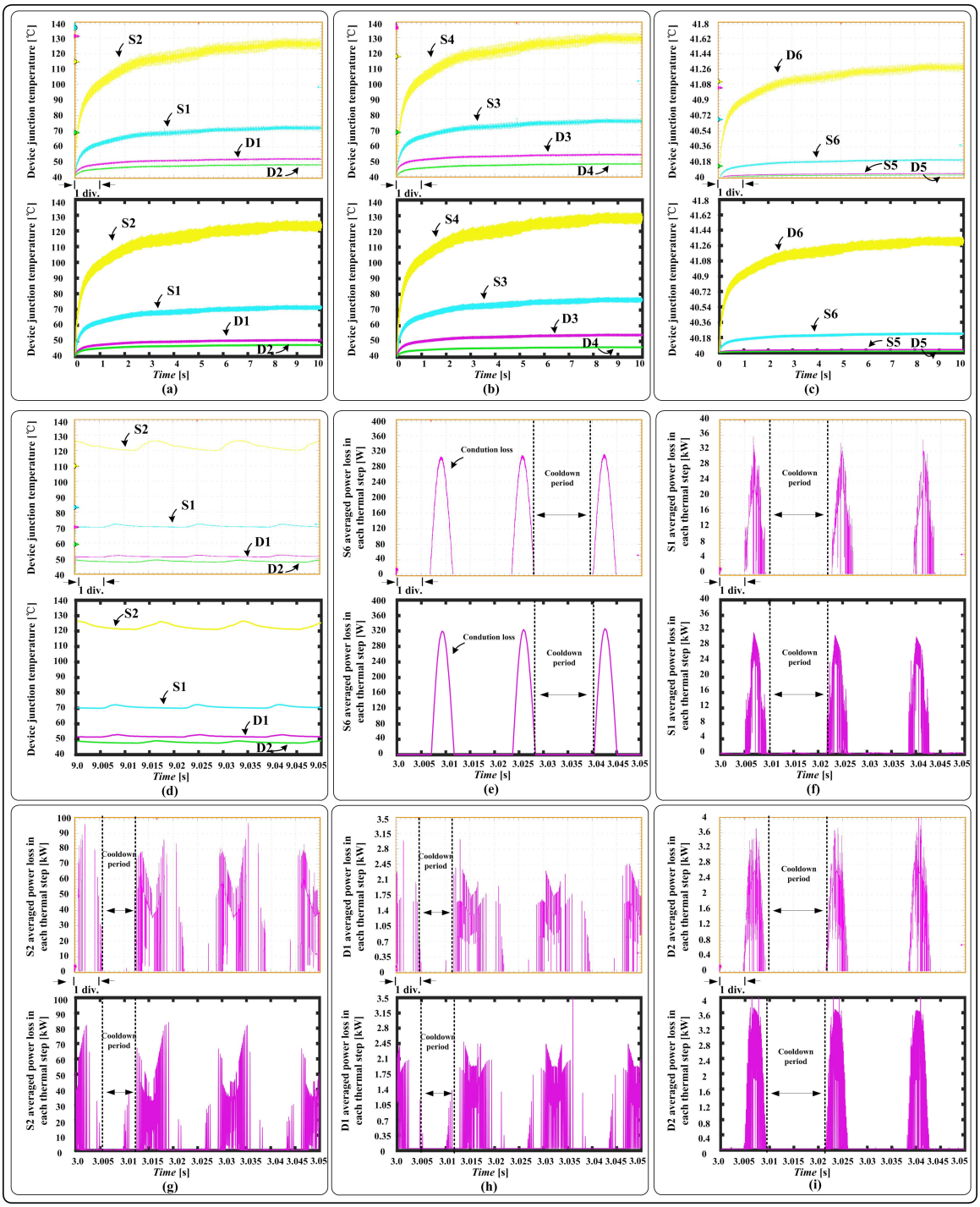

Figure 4.13: System-level and device-level results for MMC-based MVDC traction power system from real-time emulation (top oscilloscope sub-figure) and off-line simulation by PSCAD/EMTDC® or SaberRD® software (bottom sub-figure) for: (a) S1, S2, D1, and D2 junction temperature, (b) S3, S4, D3, and D4 junction temperature, (c) S5, S6, D5, and D6 junction temperature, (d) Zoomed-in S1, S2, D1, and D2 junction temperature, (e) S6 averaged power loss in each thermal time-step, (f) S1 averaged power loss in each thermal time-step, (g) S2 averaged power loss in each thermal time-step, (h) D1 averaged power loss in each thermal time-step, (i) D2 averaged power loss in each thermal time-step. Scale: (a) (b) (c) x-axis: $1s$/div. (d) (e) (f) (g) (h) (i) x-axis: $5ms$/div.

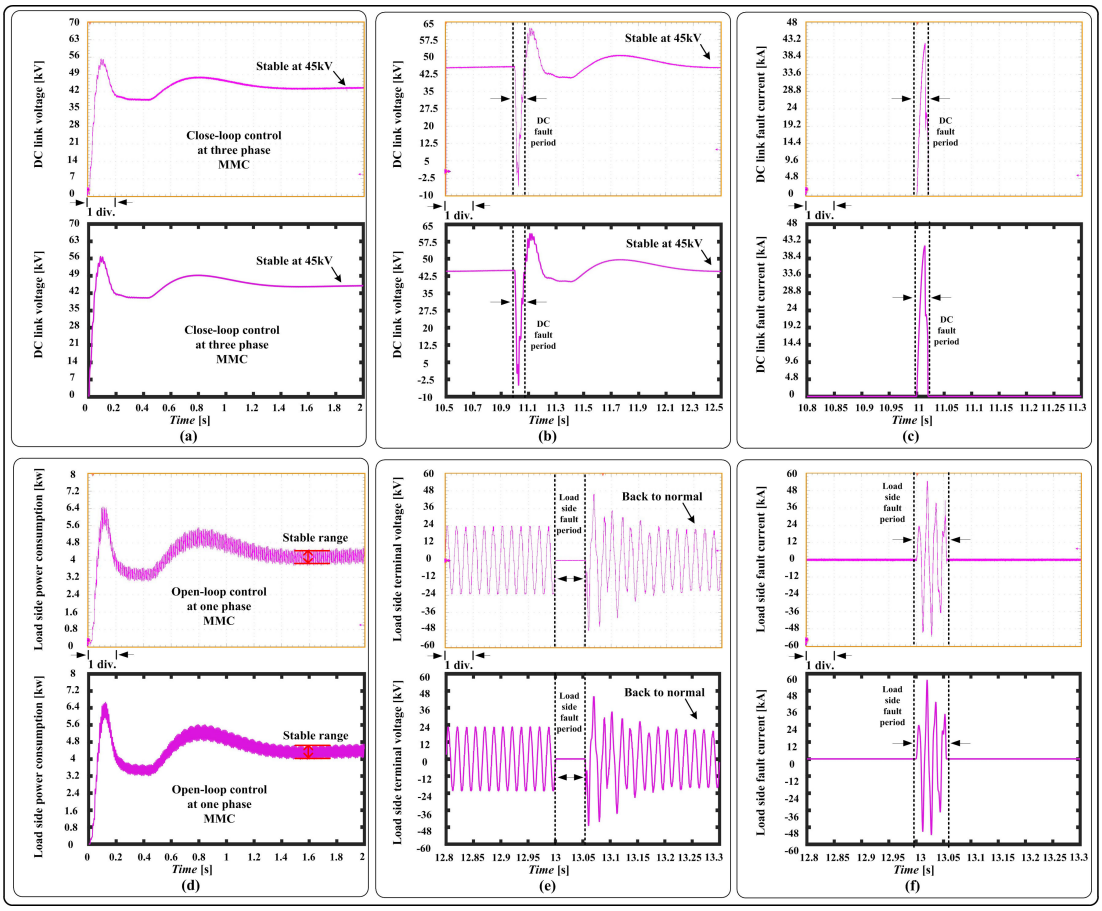

Figure 4.14: System-level results for MMC-based MVDC traction power system from real-time simulation (top oscilloscope sub-figure) and off-line simulation by PSCAD/EMTDC® software (bottom sub-figure) for: (a) DC link voltage on start-up stage, (b) DC link voltage under DC fault condition, (c) DC link fault current, (d) Load side power consumption, (e) Load side terminal voltage under load side fault condition, (f) Load side fault current. Scale: (a) (b) (d) x-axis: $0.2s$/div. (c) (e) (f) x-axis: $50ms$/div.

calculates the capacitor discharge status. Once the gate-emitter capacitor discharge voltage drop to the turn-off threshold voltage, the linear static block and the back linear block are triggered and the static state and the tail current shape can be determined.

Fig. 4.13 (a) - (d) show the device junction temperature within ten seconds and zoomed-in figures from $9.0s$ to $9.05s$ and Fig. 4.13 (e) - (i) show the device average power loss in each thermal time-step from $3.0s$ to $3.05s$. The time period with no power loss or less power loss will introduce temperature cool-down in the specific device. The IGBT S1 works with the diode D2 in the sub-module while the IGBT S2 works with the diode D1. From Fig. 4.13 (a), S1 and D2 start and end the switch power loss period at the same time while S2 and D1 have the same scenario. S1 power loss in each thermal time-step peaks at around $32kW$ and D2 peaks at about $3.4kW$. S2 power loss in each thermal time-step peaks at around $90kW$ and D1 peaks at about $2.45kW$. The IGBTs consume at least 8 times the power loss

than the diodes in the sub-module. From Fig. 4.13, IGBT S1 and S2 operate at much higher temperature than the diodes D1 and D2. In general, the amplitude variation of the average power loss is related to the temperature variation and the thermal accumulation process is highly related to time. To present the sinusoidal voltage waveform based on PD-PWM in our work, the sub-module capacitor voltage has to be cut out by conducting the lower device S2 and S4 by more than 50% of the operating time [106]. With more conducting time of the lower device, the lower device generates more conduction losses which resulted in device temperature rise and the resistance of the device increased which resulted in more conduction losses. The temperature rise of the lower device also lead to higher switching losses.

In Fig. 4.14 (a) (d), DC link voltage closed-loop control and load side power consumption open-loop control results are shown during the two seconds of startup. The close-loop control objective of the three-phase MMC is to maintain the DC link voltage stable at $45kV$. The open-loop control of the single-phase MMC help the load operate at the rated condition, while the R-L load power consumption varies at the stable range. A DC link fault is simulated at 11s and the link voltage and fault current are shown in Fig. 4.14 (b) (c). At 12.5s, the DC link voltage runs back to $45kV$. The load side fault happened at 13s and the load side terminal voltage and fault current are shown in Fig. 4.14 (e) (f). At 13.5s, the load side terminal goes back to normal condition.

4.6 Summary

This chapter proposed the Wiener-Hammerstein configuration based device-level electro-thermal model for power electronic components, which is demonstrated with a three-phase to single-phase MMC-based traction power system in real-time emulation on the MPSoC platform. The MMC sub-module device-level transients are simulated in the Cor -tex®-A53 Core with the latency of $90ns$ and the three-phase to the single-phase MMC-based traction power system is simulated on the programmable logic (FPGA) with the latency of $24.2\mu s$. Both system-level and device-level results have been validated by professional power system software PSCAD/EMTDC® and power electronic simulation software SaberRD®. The modeling procedure of Wiener-Hammerstein configuration has add -ed the carrier charge process feature, which is based on physical processes and calculated by first-order delay function. The timing of turn-on and turn-off carrier charging has been indicated and the equivalent circuit has been utilized for the dynamic calculation. The improved modeling of the static model and the first-order delay dynamic model gives the precise tailing current and reverse recovery waveform based on physical processes. The system open-loop results indicate that the R-L load is operated at the rated condition. The proposed device-level modules and real-time emulation enable a detailed evaluation of complex MVDC traction systems and controls with a low-cost and flexible hardware and software platform.

5

Real-Time HIL Emulation of High-Speed Rail Power System with SiC-Based MMC

This chapter proposes a real-time modelling method based on Wiener-Hammerstein for emulation of the SiC IGBT module in the Beijing-Shanghai HSR application's energy conversion system. For three dedicated stages, the oscillation mechanism for the SiC system was explained in detail: carrier charge stage, static characteristics, and dynamic characteristics. The complete HSR prototype and comprehensive HSR train power system were implemented in MPSoC-FPGA hardware platform with optimized communication protocol, where the device-level transients, verified by SaberRD®, are executed at 10 ns time-step resolution with proper assumption and system-level transients, verified by PSCAD/EMTDC®, are emulated at 10 μs per time-step. This original work can be used as the HIL method to estimate the performance of the SiC material based power switch for the increasing demand of future generations of HSR for energy-efficient applications. This is also the first time in literature to propose wide bandgap device based massively large power system real-time emulation in the hybrid MPSoC-FPGA platform.

5.1 Introduction

High-speed rail (HSR) delivers fast, efficient, and reliable transportation in all weather conditions, fosters economic development in second-tier cities along train routes, links cities together into integrated regions that can then function as a single stronger economy, broadens labour markets and offers populace a wider network of employers to choose from [104], and has been specifically researched for stability and compensation [105] - [107], control [108], design optimization [109], and hardware-in-the-loop (HIL) application [110]. In the twentieth and the twenty-first century, HSR has achieved some noticeable

achievements regarding test speed and operation scale. In 1903, Marienfelde–Zossen HSR line reached 200km/h for the first time and demonstrated the feasibility of the modern electrified HSR [111]. With tremendous advances of HSR field speed tests, research and development pushes the world's fastest train to the limit with a speed record of 603km/h on Japanese SCMaglev in 2015. Meanwhile, China has extended the HSR network to the operation scale of 25,000 km which is still growing rapidly today.

The future HSR system relies on high efficiency, operating temperature and switching frequency next-generation power semiconductor. The invention of the silicon (Si) power device inexorably paved the way for the modern HSR era. Silicon carbide (SiC) and gallium nitride (GaN), both wide bandgap (WBG) semiconductors, have emerged as the front-running solutions to make inroads into high power, high-temperature segments [24]. The SiC characteristic enables dramatic reductions in conduction loss by the improvement of low-impedance packaging technology and switching loss by the significant reduction of reverse recovery phenomenons, and prevents the flow of leakage current at high temperature by the higher breakdown voltage in nature [112]. Innovative SiC power module may lead the way of advanced HSR transportation for a low-carbon sustainable future. With the advantages mentioned above, there is a growing need to model the SiC power device in the existing HSR AC traction scenarios to test and evaluate the performance of the control and protection algorithm and circuits, and controller in a device-level non-destructive environment repeatedly. For this purpose, real-time HIL emulation of the HSR power system can be a promising answer in this application. To maximize the HIL emulator performance, both high sequential clocking and massive parallel compute devices have been utilized in previous works.

For simplification of the device-level behavioural model, Wiener-Hammerstein configuration, consists of two linear dynamic blocks in the front and the back with a sandwiched linear static block in the middle, is employed as the behavioural modeling tool for separating the static and dynamic characteristics in this work [113]. After generations of development in nonlinear system identification theory, the Wiener-Hammerstein-based models have been applied in various areas, such as system identification [114], [115], hysteresis phenomena [117], [118], power electronics [64], and electrical drives [120]. Different from the Wiener-Hammerstein model, the configuration extends the linear time-invariant (LTI) nonlinear static block to linear or nonlinear time-variant static one, which is considered to have little impact on the model accuracy and execution efficiency.

This chapter proposes real-time electrothermal behavioural models for the SiC hybrid IGBT module via the Wiener-Hammerstein configuration with the equivalent electrical component representation in the study case of Beijing-Shanghai HSR AC traction system based on the hybrid multiprocessor system-on-chip (MPSoC) and field-programmable gate array (FPGA) platform. The parameters of the Wiener-Hammerstein configuration model is extracted from the dedicated device datasheet from the manufacturer. The perfor-

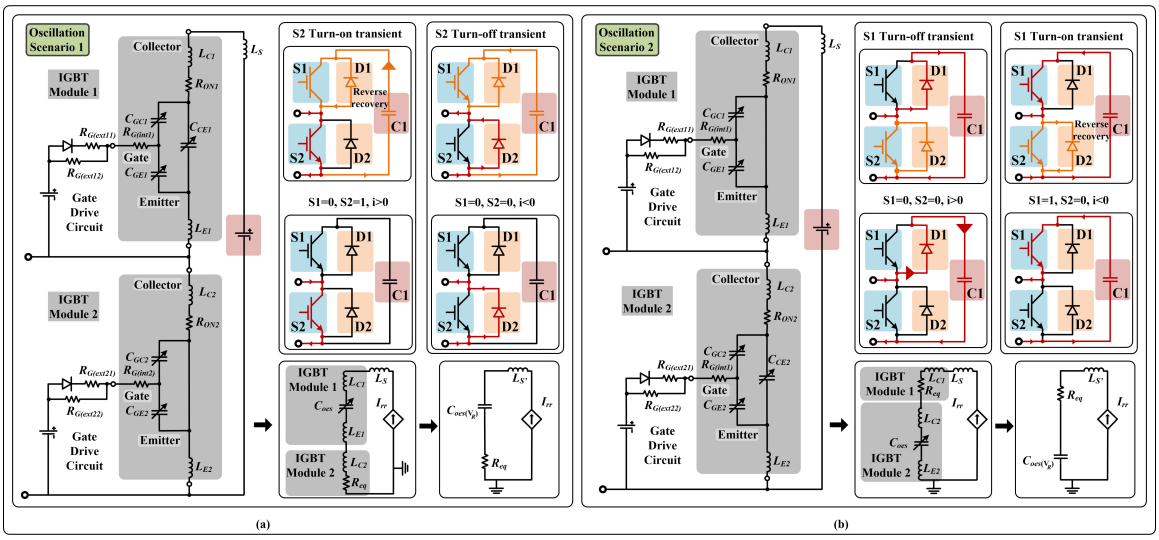

Figure 5.1: Oscillation mechanism of hybrid SiC IGBT module: (a) Oscillation Scenario 1. (b) Oscillation Scenario 2.

mance of the proposed real-time model is tested and validated with commercial software at both system-level and device-level. This chapter is organized as follows. Section 5.2 describes the construction of the Wiener-Hammerstein configurations for SiC IGBT module. Section 5.3 explains the details of the Beijing-Shanghai HSR. Section 5.4 shows the detailed hardware implementation on hybrid MPSoC-FPGA platform. Section 5.5 gives the real-time emulation results and validation.

5.2 Oscillation Mechanism and Wiener-Hammerstein Configuration Modeling of SiC IGBT Module

This section introduces the oscillation mechanism of the SiC IGBT module and the detailed modeling method based on the Wiener-Hammerstein configuration which includes the carrier charge dynamic characteristics, operating static characteristics, and operating dynamic characteristics. The voltage reconstruction is explained in the last subsection. The device datasheet utilization is listed in Table 5.1 for the Wiener-Hammerstein configuration modeling procedure.

5.2.1 Oscillation Mechanism of SiC IGBT Module

Due to the advantage of the SiC material, it enables the lower resistance and capacitance in high power switching device, which introduces the oscillation problem during both turn-on and turn-off. The low resistance worsen the damping effect while the low capacitance increases the oscillation frequency compared to the Si-based switching device.

In Fig. 5.1 (a) (b), the scenario of positive and negative current inside the MMC sub-

Table 5.1: Wiener-Hammerstein Configuration Modeling Procedure

Dynamic carrier charge	Static electrical characteristic	Dynamic electrical characteristic	Power loss and thermal calculation
$t_{d,ON}$- I_C, $t_{d,OFF}$- I_C	I_C-V_{CE}, I_F-V_F	t_r- I_C, t_f- I_C, Q_c, R_{Gon}, R_{Goff}, L_s, L_{pCE}, C_{oes} - V_{CE}, C_{ies} - V_{CE}	E_{on}-I_C, E_{off}-I_C, E_{on}-R_G, E_{off}-R_G, Z_{thjc}^{IGBT}-t, Z_{thjc}^{Diode}-t

module for the turn-on and turn-off can be observed. During the turn-on transient, the IGBT receives a current injection from both MMC submodule terminal and SiC diode reverse recovery current which creates an oscillation loop inside the submodule. The detailed oscillation loop of the MMC submodule can be seen in Fig. 5.1 (a) (b) with parasitic components where the diode symbol is considered as the ideal diode. The equivalent oscillation circuit is given in the subplot of each oscillation scenario and the parasitic parameters of the circuit in the oscillation Scenario 1 are given as:

$$\omega \approx \frac{1}{\sqrt{Ls' C_{oes}(V_R))}}, Ls' = L_{C1} + L_{E1} + L_S + L_{C2}, \tag{5.1}$$

$$R_{Gon} = R_{Int} + R_{Ext(ON)} = 1.3\Omega, \tag{5.2}$$

$$C_{ies} = C_{GC2} + C_{GE2}, X_G = R_{Gon} + \frac{1}{j\omega C_{ies}}, \tag{5.3}$$

$$R_{eq} = \left| \frac{X_G \cdot j\omega L_{E1}}{X_G + j\omega L_{E1}} + R_{ON2} \right| \approx 1.5\Omega. \tag{5.4}$$

where L_{C1}, L_{E1}, L_S are the IGBT module 1 collector and emitter parasitic inductance and circuit stray inductance, respectively. ω is the oscillation frequency. R_G, R_{Int}, $R_{Ext(ON)}$ and R_{ON2} are the total gate resistance, internal gate resistance, external turn-on gate resistance and turn-on static resistance, respectively. C_{GC2}, C_{GE2} are the IGBT module 2 gate-collector and gate-emitter capacitance, respectively. R_{eq} is the equivalent RLC oscillation circuit resistance. For oscillation Scenario 2, the calculations of the equivalent RLC components are similar.

5.2.2 Carrier Charge Stage

The carrier charge stage, shown in Fig. 5.2, is the prerequisite condition before the IGBT's turn-on and turn-off. The IGBT consists of three nonlinear capacitors C_{GC}, C_{GE}, and C_{CE}, between the three nodes: collector, gate, and emitter. When the gate signal of IGBT is on, C_{GE} and C_{GC} start charging with the nonlinear characteristic, which can be simplified to the equivalent first-order RC circuit.The resistance of the charge state is referred to as the internal and external gate resistor while the capacitor is the nonlinear node capacitor inside the IGBT module. The equivalent charging capacitor value is calculated by the turn-on and

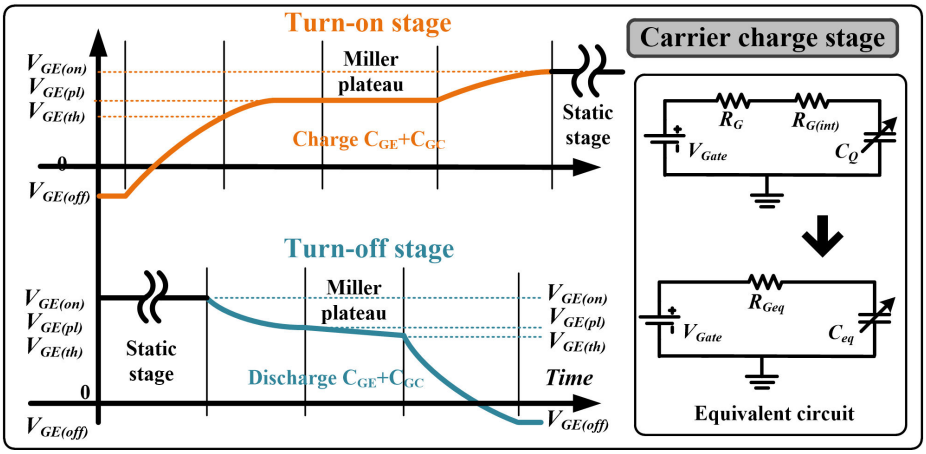

Figure 5.2: Carrier charge stage of SiC-IGBT.

turn-off delay time T_d which equals to 2.2τ=2.2$R_{Geq}C_{eq}$. Thus, the C_{eq} value is obtained by the relation given as:

$$Ceq = \frac{T_d}{2.2R_{Geq}}, \tag{5.5}$$

5.2.3 Static Characteristic

In Fig. 5.3, the static characteristics of IGBT and diode are shown with detailed component representation. IGBT and diode can be represented by a conductance g_{ION} and g_{DON} in parallel with a voltage controlled current source (VCCS). Both the conductance and the VCCS are temperature sensitive and change over time with the dedicated dynamic thermal circuit. v_{ION} and v_{DON} is the collector-emitter saturation voltage and diode forward voltage, respectively. i_{ION} and i_{DON} are the Nodal representation of v_{ION} and v_{DON} in the static characteristics. In static operating condition, the capacitive characteristic inside the SiC-based diode is negligible with the reduction of the corresponding component representation. The temperature sensitive relation of the nodal representations are given as:

$$g_{ON}(T_{vj}) = \frac{T_{vj}-T_{low}}{T_{low}-T_{high}}(g_{ON}^{T_{low}} - g_{ON}^{T_{high}}) + g_{ON}^{T_{low}}, \tag{5.6}$$

$$v_{ON}(T_{vj}) = \frac{T_{vj}-T_{low}}{T_{low}-T_{high}}(v_{ON}^{T_{low}} - v_{ON}^{T_{high}}) + v_{ON}^{T_{low}}, \tag{5.7}$$

$$i_{ON}(T_{vj}) = v_{ON}(T_{vj}) \cdot g_{ON}(T_{vj}). \tag{5.8}$$

where T_{vj}, T_{low} and T_{high} are the junction temperature, datasheet low experimental temperature, and the datasheet high experimental temperature, respectively.

5.2.4 Dynamic Characteristic

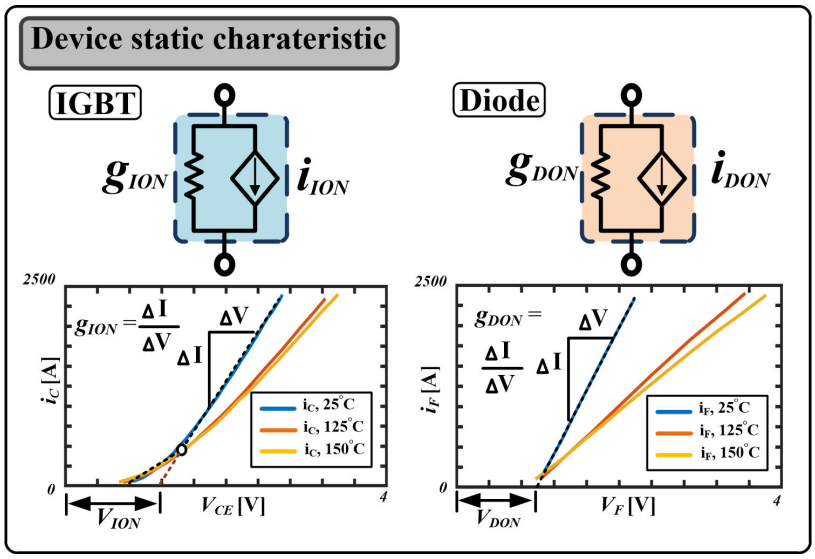

Figure 5.3: Static characteristic of SiC-IGBT.

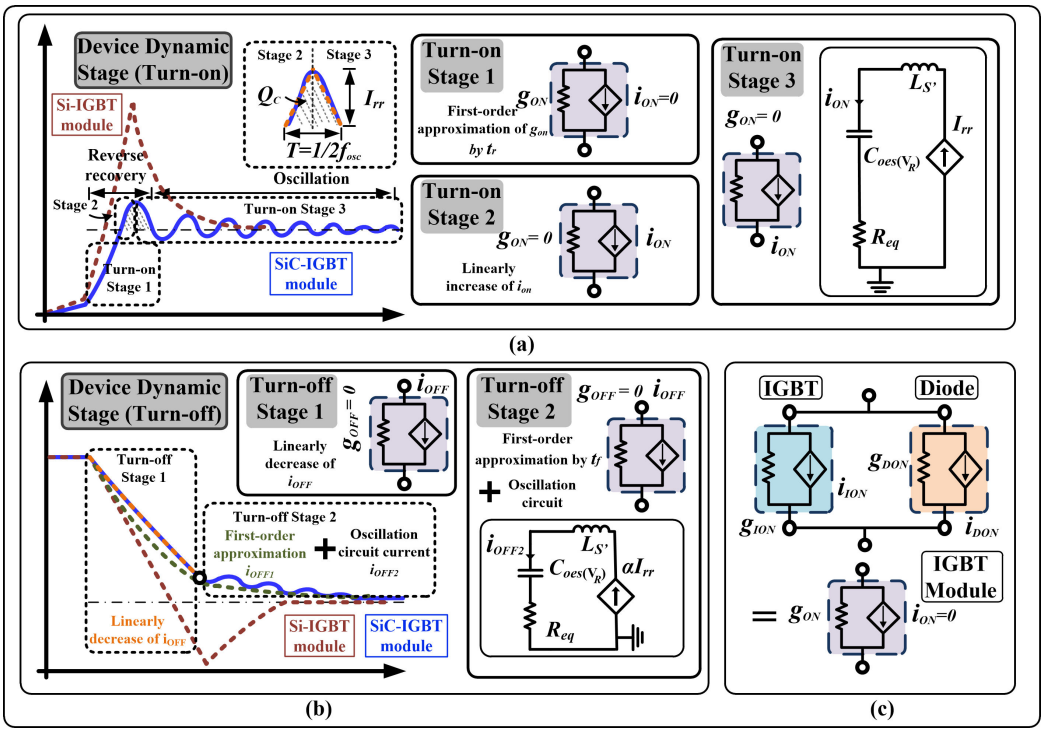

Figure 5.4: Dynamic characteristics of Si and SiC IGBT modules for: (a) Turn-on, (b) Turn-off, (c) Hybrid IGBT module Norton circuit representation.

In Fig. 5.4, the dynamic characteristics of the hybrid IGBT module are shown with three stages in turn-on transients in Fig. 5.4 (a) and two stages in turn-off transients in Fig. 5.4 (b).

In the turn-on Stage 1, the IGBT module employs a first-order approximation in the

calculation. The VCCS of IGBT is set to zero while its conductance utilized the first-order approximation which is calculated by the turn-on rise time. Stage 2 of turn-on uses the triangle shape to calculate the peak value of the reverse recovery current where the period time is obtained from the oscillation frequency and the capacitor charge value is from the device datasheet. The transient current of Stage 3 is calculated by the equivalent RLC circuit.

In the turn-off Stage 1, the IGBT module employs both a first-order approximation and the linearly decrease calculation. The conductance of IGBT is set to zero while its VCCS utilized the first-order approximation which is calculated by the turn-off rise time. But the stage 1 is approximated by the two cross points of linearly decrease curve and first-order approximation curve. After the cross point of linearly decrease curve and the first-order approximation curve, the transient current waveform utilized the combination of first-order approximation curve and oscillation circuit result in stage 2 of turn-off. The oscillation initial current is set to the previous cross point value. In the static state, the dynamic characteristics are neglected and blocked. And the whole IGBT module is set to the form of Fig. 5.4 (c).

During the turn-on or turn off transient, it is assumed that the RLC sub-circuit loop introduces the oscillation waveform. The RLC circuits equations are given as:

$$u_C + u_R + u_L = 0, \tag{5.9}$$

$$u_R = Ri_L, u_L = L\frac{di_L}{dt}, u_C = \frac{Q}{C}, i_L = \frac{dQ}{dt}, \tag{5.10}$$

$$LCp^2 + RCp + 1 = 0, p = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}. \tag{5.11}$$

where u_R, u_L, and u_C are the transient voltage of the RLC components. R, L, and C are the resistive, inductive, and capacitive component of RLC circuit, respectively. The accurate representation of RLC transient current with the initial current injection at the peak is given as:

$$i = I_0 e^{-\delta t} cos\left(\omega t\right), I_0 = I_{rr} = 4Q_{rr} f_{osc}, \delta = \frac{R}{2L} \tag{5.12}$$

$$\omega = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L},\right)^2} \approx \sqrt{\frac{1}{LC}}, R << 2\sqrt{\frac{L}{C}}. \tag{5.13}$$

where i is the transient current of the RLC circuit; I_0 is the initial current for the inductor current which is actually the reverse recovery current peak value I_{rr}; Q_{rr} is the reverse recovery charge of the IGBT module; f_{osc} is the oscillation frequency of the RLC circuit. The change of the conductance and accompanied current value of first-order approximation in the switching transient can be estimated, given as:

$$H(s) = \frac{1}{\tau S+1}, S = \frac{2}{\Delta t} \cdot \frac{1-z^{-1}}{1+z^{-1}}, h(t) = \frac{\Delta t + \Delta t z^{-1}}{\Delta t + 2\tau + (\Delta t - 2\tau)z^{-1}}. \tag{5.14}$$

where the $H(s)$ is the transfer function of the first-order approximation. Bilinear transformation is utilized with the simulation timestep Δt. $h(t)$ is the time domain transfer

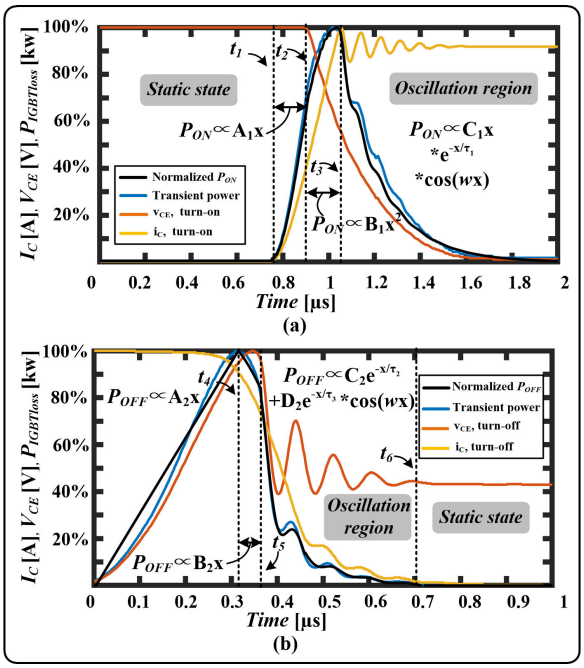

Figure 5.5: Voltage reconstruction of SiC-IGBT module for: (a) Turn-on, (b) Turn-off.

function. τ can be calculated by utilized of the value of 90.03% for 0.105τ and 10.01% for 2.302τ, which is the definition value of the rise and fall time in the datasheet.

5.2.5 Voltage Reconstruction

The transients turn-on and turn-off power loss of hybrid SiC IGBT module are shown in Fig. 5.5 under specific circumstance from the datasheet. From which, the transient voltage waveform can be obtained via the relationship of V=P/I. The current, voltage and the power loss waveform has been normalized to percentage level based on their maximum value. Both the turn-on and turn-off waveform consist of a linear or polynomial region and a mixed region of the first-order approximation and the oscillation. The turn-on and turn-off power loss are given as

$$\begin{aligned} P_{ON} = &\int_{t_1}^{t_2} (A_1 x + D_1) + \int_{t_2}^{t_3} (B_1 x^2 + E_1 x + F_1) \\ &+ \int_{t_3}^{\infty} ((C_1 x + G_1) e^{-\frac{x}{\tau_1}} cos(\omega x)), \end{aligned} \tag{5.15}$$

$$\begin{aligned} P_{OFF} = &\int_{0}^{t_4} (A_2 x + E_2) + \int_{t_4}^{t_5} (B_2 x + F_2) \\ &+ \int_{t_5}^{t_6} (C_2 e^{-\frac{x}{\tau_2}} + D_2 e^{-\frac{x}{\tau_3}} cos(\omega x) + G_2), \end{aligned} \tag{5.16}$$

where P_{ON} and P_{OFF} are the total power loss during the turn-on and turn-off transient, respectively. t_1 - t_6 indicate the start time of specific region; A_1, A_2, B_1, B_2, C_1, C_2, D_1, D_2,

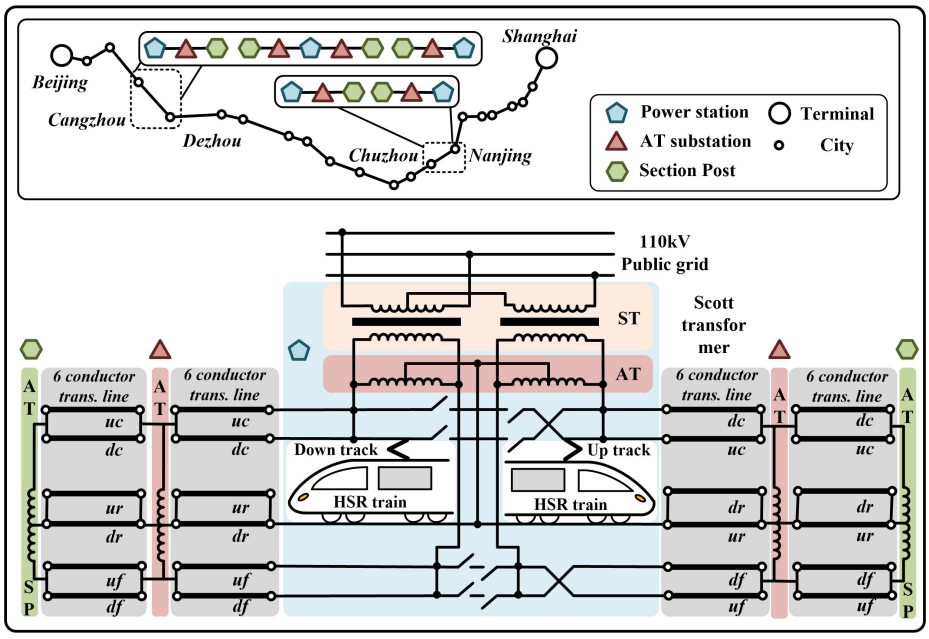

Figure 5.6: Complete topology of Beijing-Shanghai HSR network.

E_1, E_2, F_1, F_2, G_1, G_2 are the parameters for fitting; τ_1 - τ_3 are the parameters for the first-order approximation.

5.3 Case Study: Beijing-Shanghai HSR Network

5.3.1 HSR prototype

The 1318 km length Beijing-Shanghai HSR, which includes 27 power stations and 26 section posts, is selected as the study case in this work. A complete topology of the power station, AT substation, and section post is shown in Fig. 5.6 with up and down track. The connection among the section post, AT substation, and the power station employs the distributed travelling wave transmission line model.

5.3.2 Detailed HSR Train Power System

MMC-based motor drive system has been increasingly adopted in recent years [121], [122]. A complete SiC-based MMC train system is illustrated in Fig. 5.7. The train receives the energy from the contact wire with the help of the pantograph system, and scales down the voltage from 27.5kV to 3kV by the single-phase transformer. Then, the rectifier converts the AC power to the DC connection of MMC-based induction machine drive system. The rectifier employs the proportional-resonant controller due to its simplicity in the hardware implementation of single phase rectifier controller while the MMC-based induction machine is controlled by the outer induction machine drive control system.

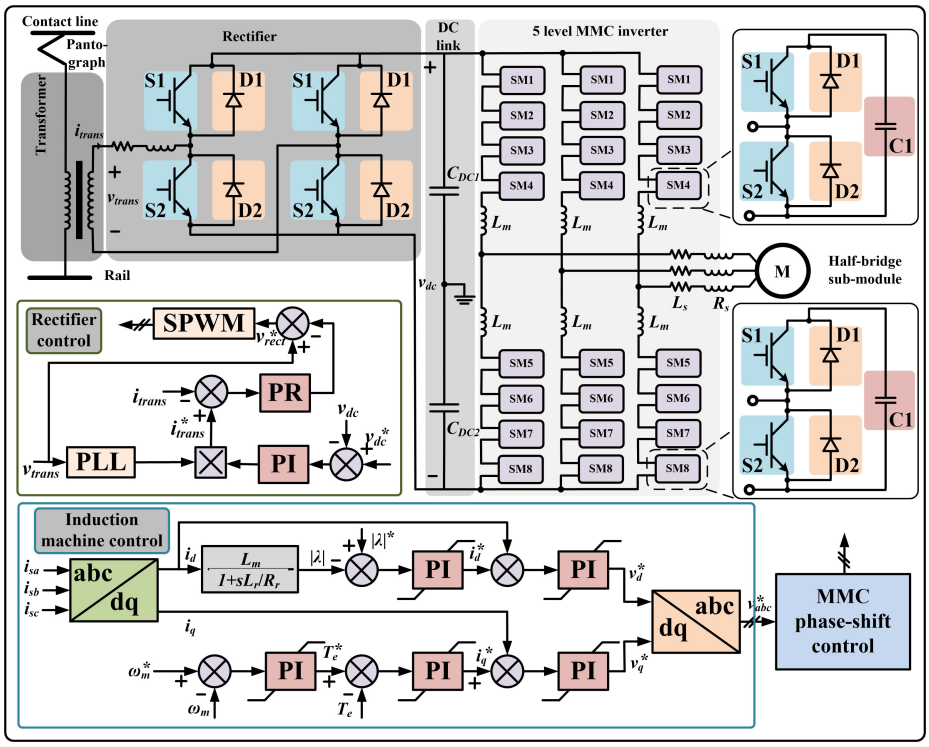

Figure 5.7: Detailed HSR traction system configuration.

5.4 Hardware Implementation of HSR System

5.4.1 MPSoC-FPGA platform

Two VCU118 boards and one ZCU102 MPSoC board are utilized for HIL platform (Fig. 5.8) for the complete HSR system emulation. The Xilinx® ZCU102 development board features a Zynq UltraScale+ MPSoC device with a quad-core ARM® Cortex-A53, dual-core real-time Cortex-R5 on 16nm FinFET+ programmable logic fabric while the Xilinx® VCU118 board provides the highest performance and integration capabilities in a FinFET node with four times larger hardware programmable logic resource capacity of ZCU102. The ZCU102 utilizes the QSFP connectors with Aurora communication protocol to exchange data from board to board, which can achieve with $650ns$ latency in the implementation.

5.4.2 Detailed System Decomposition

A comprehensive HSR topology is implemented in the MPSoC-FPGA platform with both device-level and system-level model. The detailed device-level SiC MMC-based drive train model, with nanosecond-level transient waveform, is emulated in the ZCU102 MPSoC system along one complete section including a power station, AT substation, and section post (SP). The other two VCU118 FPGA boards emulate the system-level AC traction system. The MPSoC communicates with the two VCU118 FPGA boards for train distance

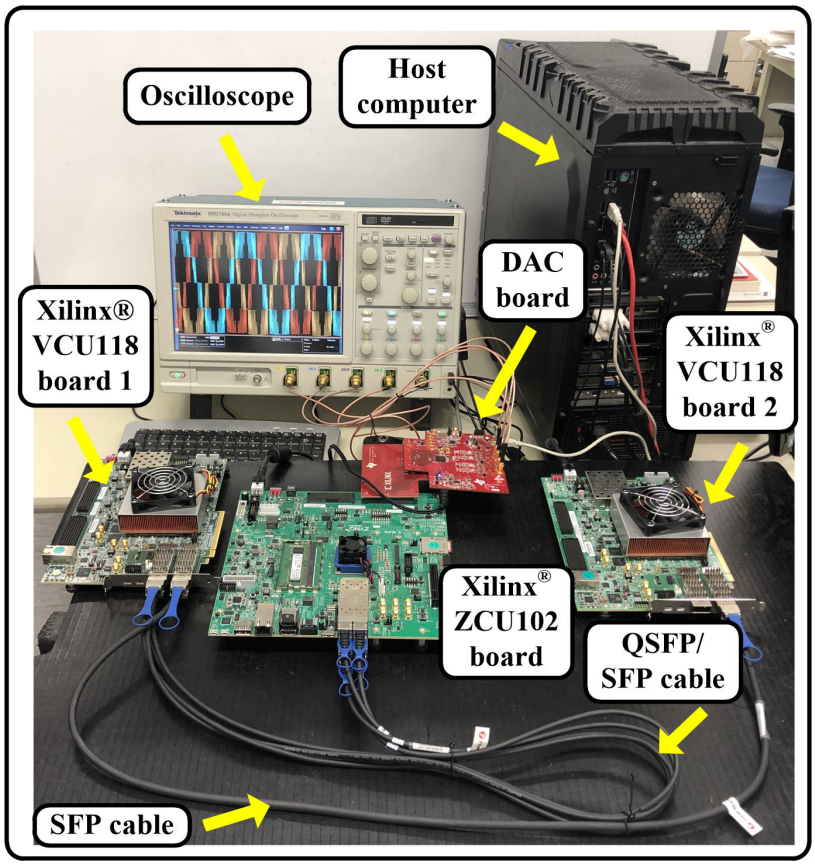

Figure 5.8: Hybrid platform configuration of HSR system.

information.

5.5 Results and Discussions

Fig. 5.9 gives the SaberRD® offline (fixed line) and the real-time experimental results (black point) comparison under datasheet standard. Fig. 5.9 (a) shows the turn-on current waveform. In the static state, the submodule is operated at 100ns. After which, the first-order approximation is employed to execute the circuit emulation also at 100ns time-step wise. In the oscillation region, the equivalent RLC circuit utilized the pre-restored historical current in the circuit emulation which results in much faster emulation speed for the single-node circuit for 6ns per time-step. The prerequisite of applying the fixed pre-restored historical current is that I_C has little influence on the reverse recovery charge Q_{rr}. All device-level results are executed in the processing system's 1.3Ghz capable ARM® cores for real-time emulation in this case. In the case of I_C equals to 168A, only one first-order approximation circuit calculation (100ns per time-step) is needed while it requires the most RLC circuit emulation results of 62 points (6ns per time-step) in the emulation. Thus the total emulation time delay is 100ns+62*6ns =472ns while the its turn-on delay time is 500ns, which

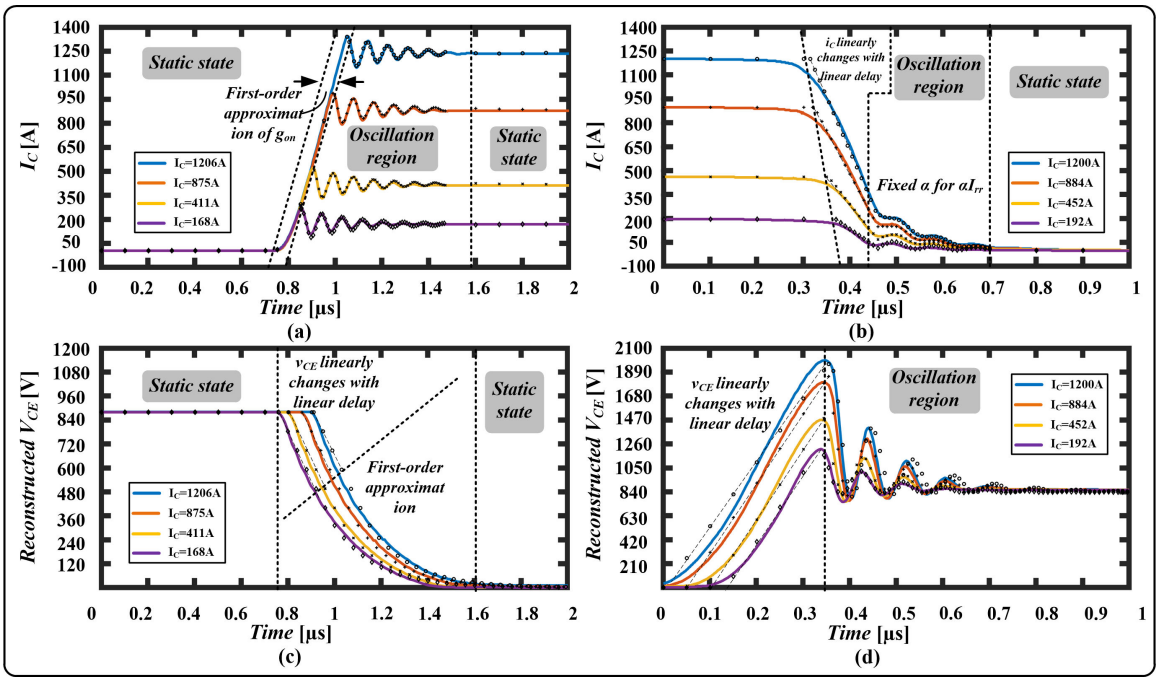

Figure 5.9: Device-level offline (SaberRD®) and real-time emulation results comparison under datasheet standard for: (a) Turn-on current, (b) Turn-off current, (c) Reconstructed turn-on voltage, (d) Reconstructed turn-off voltage.

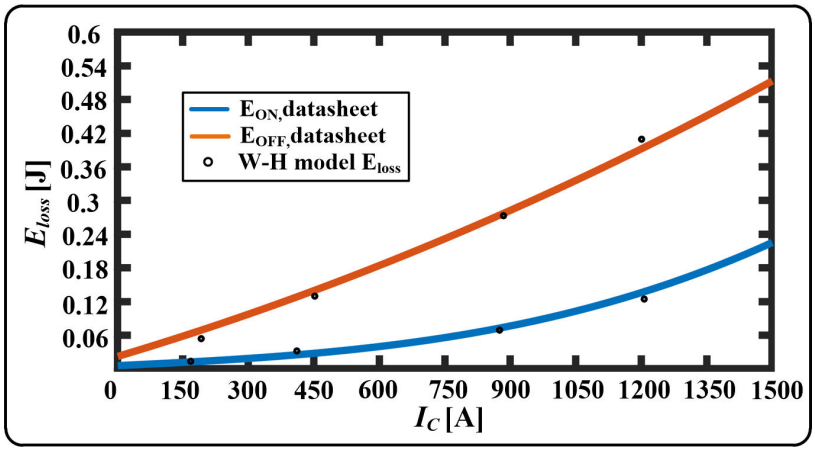

Figure 5.10: Comparison of normalized power loss and datasheet power loss.

means the emulation is real-time capable. The time-delay for the case of I_C equals to 1206A is 2*100ns+43*6ns = 458ns. In Fig. 5.9 (b), the turn-off current waveform is divided into two parts: linearly decreasing region and mixed oscillation region. In the linearly decreasing region, the first-order approximation calculations are also emulated simultaneously. After the cross point of linearly decrease and the first-order approximation, the tail current waveform is combined by the oscillation circuit result and the first-order approximation. But in Fig. 5.9 (b), the α is fixed for all the current ratings which introduces higher error rate

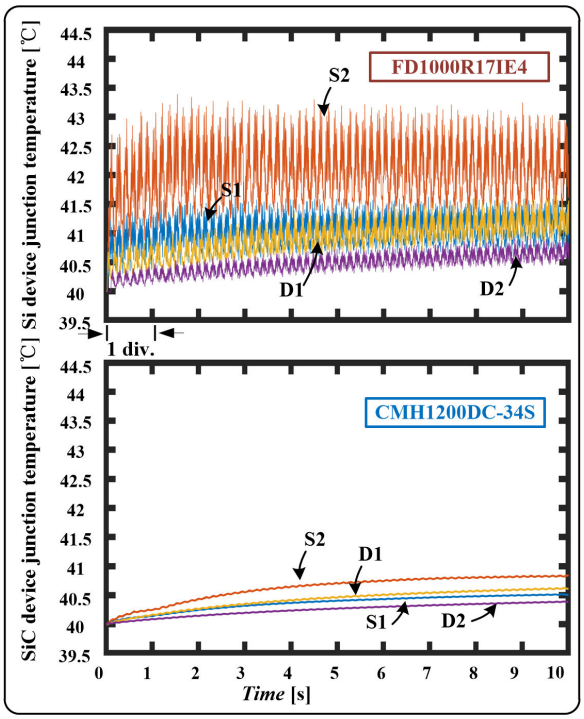

Figure 5.11: Thermal performance comparison between Si and SiC IGBT module.

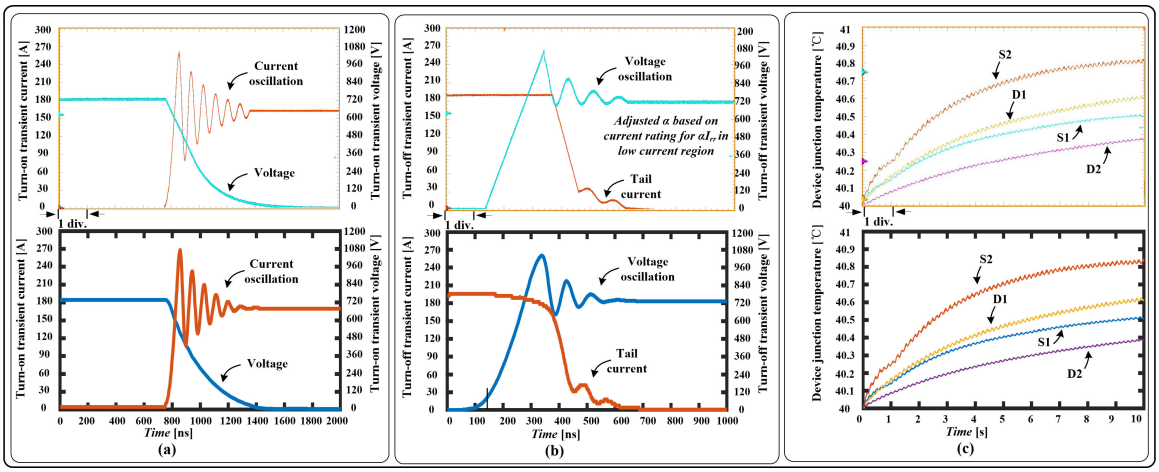

Figure 5.12: Device-level results for MMC submodule from real-time simulation (top oscilloscope sub-figure) and off-line simulation by SaberRD® software (bottom sub-figure) for: (a) Turn-on transient current, (b) Turn-off transient current, (c) Device junction temperature. Scale: (a) x-axis: 200ns/div. (b) x-axis: 100ns/div. (c) x-axis: 1s/div.

for the oscillation region under low current rating. In the final device tail current implementation, α has been adjusted to the cross point percentage value for better fitting result. Fig. 5.9 (c) (d) are the turn-off current and the reconstructed V_{CE} based on the previous normalized transient power loss waveform by utilizing the relationship of V=P/I.

Table 5.2: FPGA Hardware Resource Consumption for Device-Level and System-Level Model in Dedicated Platform

Model	BRAM	DSP	FF	LUT
Device-level Train 1 on ZCU102				
Train 1	21.81%	45.83%	26.17%	90.92%
System-level HSR system 1 on VCU118-1				
Train 2	0.07%	16.89%	6.07%	21.08%
Station 1	0%	29.78%	22.94%	46.39%
Total	0.07%	46.67%	29.01%	67.47%
System-level HSR system 2 on VCU118-2				
Train 3	0.07%	16.89%	6.07%	21.08%
Train 4	0.07%	16.89%	6.07%	21.08%
Station 2	0%	29.78%	22.94%	46.39%
Total	0.14%	63.56%	35.08%	88.55%

Table 5.3: Average Error Rate of W-H Model with SaberRD®

i_{on}	v_{on}	i_{off}	v_{off}
0.17%	4.32%	1.02%	3.72%

Table 5.4: Latencies of hardware implementation

Device-level first-order appro.	Device-level mixed osc.	System-level
$100ns$	$10ns$	$10\mu s$

Fig. 5.10 compares the proposed normalized power loss and the datasheet standard power loss. The errors are acceptable which shows the accuracy of the reconstructed switching voltage transient waveform. The device thermal calculation is not utilizing the normalized power loss value but the datasheet standard power loss value to ensure the accuracy of the device thermal behaviors.

Another thermal performance comparison is shown in Fig. 5.11 with Si-based IGBT module FD1000R171E4. The submodule is considered to be mounted on one heat sink and shares the same setup and gate signal from the SiC-based device. From the result, the temperature variation of the Si-based device shows higher fluctuation during the ten seconds, and ranges between 40 and 43°C which is nearly three times that of the range for the SiC-based device.

Fig. 5.12 (a) (b) give the IGBT S2 turn-on and turn-off transients, respectively. The front carrier charge linear dynamic block in the Wiener-Hammerstein configuration starts to operate when gate signal generated. Once charged to the threshold voltage, the front carrier charge linear dynamic block triggers the linearized static characteristic block and the back linear dynamic characteristic block. The linear static characteristic block computes its de-

vice conductance and VCCS value. The back linear dynamic characteristic block emulates the first-order delay transient. At the turn-on stage, the collector current shoots up with the oscillation phenomenon which is mainly introduced by the low capacitance and resistance by the diode D1. The lower capacitance introduces higher oscillation frequency while the lower resistance results for worse damping in the oscillation process. The ARM® core is only able to perform a $10ns$ time-step real-time device-level emulation and $6ns$ time-step for a $10ns$ time-step wise in the RLC oscillation waveform because the high-frequency oscillation requires smaller time-step to show the detailed transients. During the carrier charge stage, the IGBT module is not activated to be turned on, which can be utilized for calculating the turn-on transient. Thus, the real-time turn-on transients borrow time for $500ns$ time-step in the emulation process. In this case, the ARM® core executes the transient calculation under the $100ns$ time-step for static state or first-order approximation to emulate ten $100ns$ time-step points and RLC oscillation waveform for $10ns$ time-step wise. When the turn-off gate signal is generated, the front linear dynamic block calculates the capacitor discharge status. Once the gate-emitter capacitor discharge voltage drop to the turn-off threshold voltage, the linear static block and the back linear block are triggered and the static state and the tail current shape can be determined by first-order approximation and its RLC oscillation waveform. Fig. 5.12 (c) shows the device junction temperature within ten seconds. Temperature cooldown can be observed during the time period with less power loss for each dedicated device. Due to SiC device advanced thermal feature, all the devices do not go beyond 41°C during stable operation.

Fig. 5.13 (a) (b) show the line voltage and line current, respectively. They are captured at the time when the train is cruising between the AT substation and power station. The voltage results include feeder-rail (FR) voltage on train and section post (SP) side, catenary-rail (CR) voltage on train and SP side. The voltage of the SP is slightly smaller than the one on the train side. The locomotive connects to the traction network by its catenary-pantograph system. The connected lines include catenary and its rail from both AT substation and power station or the source (S) side. From Fig. 5.13 (b), i_{R-S}, the current on the rail to the source, shares the equal quantity with the i_{R-AT} which is the current on the rail to the AT substation. The rectifier inside the locomotive converts the AC power from the traction network to DC link and gives the result in Fig. 5.13 (c). As seen in Fig. 5.13 (d) (e), MMC capacitance forming voltage and motor voltage are given with their FFT analysis in Fig. 5.13 (g) (h) which analyzes the high-frequency harmonic impact on the grid. Due to the large inductance inside the motor, the difference of MMC terminal and source voltage are not obvious for comparison. The most observable high-harmonic frequency is about $4000Hz$ and $8000Hz$ with the negligible amplitude to the $50Hz$ one. The high-frequency harmonic is introduced by the $2000Hz$ carrier wave in the control system. The capacitance voltages of the upper arm and lower arm of the MMC sub-module are shown in Fig. 5.13 (f) (i), respectively. $V_{cap,a}$ of the upper arm varies from 727 V and 742 V while $V_{cap,a}$ of

the lower arm varies from 726 V and 741 V. The variation percentage of capacitance in the upper arm is 2.022% while the one in the lower arm is 2.024%.

The FPGA resource consumption for study case is illustrated in Table 5.2 and the highest percentage usage of resource is the LUT, with 90.92%, 67.47%, 88.55% on ZCU102, VCU118-1, and VCU118-2, respectively. In this work, it is considered that only one uptrack and one downtrack train are cursing inside the traction network that is energized by one power station. The device-level high-speed train communicates with first VCU118 to get the corresponding voltage and current information from the traction network.

The average errors are shown in Table 5.3 where the voltage average error rates are higher than the current ones. Because the front part of the normalized transient power waveform utilized linear approximation which is easier to be interpreted in terms of the linear delay. If higher order of polynomial approximation is employed, the error rate can be reduced to certain percentage but the delay part might be hard to implement and interpret. The average error of the device-level transient is less than 4.32% while the one at system-level is 0.217%.

The latencies of hardware implementation is shown in Table 5.4. The device-level transient takes 100 ns for the first-order approximation and $10ns$ for the mixed oscillation waveform in real-time with proper precalculation assignment while the system-level transients need 10 μs to conduct the emulation.

5.6 Summary

The technology of high-speed rail network is constantly evolving with the introduction of newer power semiconductor device, and an accurate and efficient hardware-in-the-loop simulation is necessary. Real-time device-level modeling of ultrafast power switch is demanding due to high amount of computation execution and time-sensitive condition. With proper allocation of the high-sequential clocking ARM® core and massively parallel FPGA execution resource, real-time ultra small time-step modeling of detailed power converter system can be realized for both device-level and system-level transients. This chapter proposed a Wiener-Hammerstein based real-time modelling method for SiC IGBT module emulation in the energy conversion system of the Beijing-Shanghai HSR application. Oscillation mechanism for SiC device has been explained in detail with three dedicated stages: carrier charge stage, static characteristic, and dynamic characteristic. The complete HSR prototype and the detailed HSR train power system have been implemented in MPSoC-FPGA hardware platform with optimized communication protocol, where the device-level transients, verified by SaberRD®, are executed at $100ns$ time-step and system-level transients, verified by PSCAD/EMTDC®, are emulated at $10\mu s$ time-step. This work can be utilized as the HIL tool to estimate the SiC material based power switch performance for the increasing demand of energy-efficient application of the future generations of HSR.

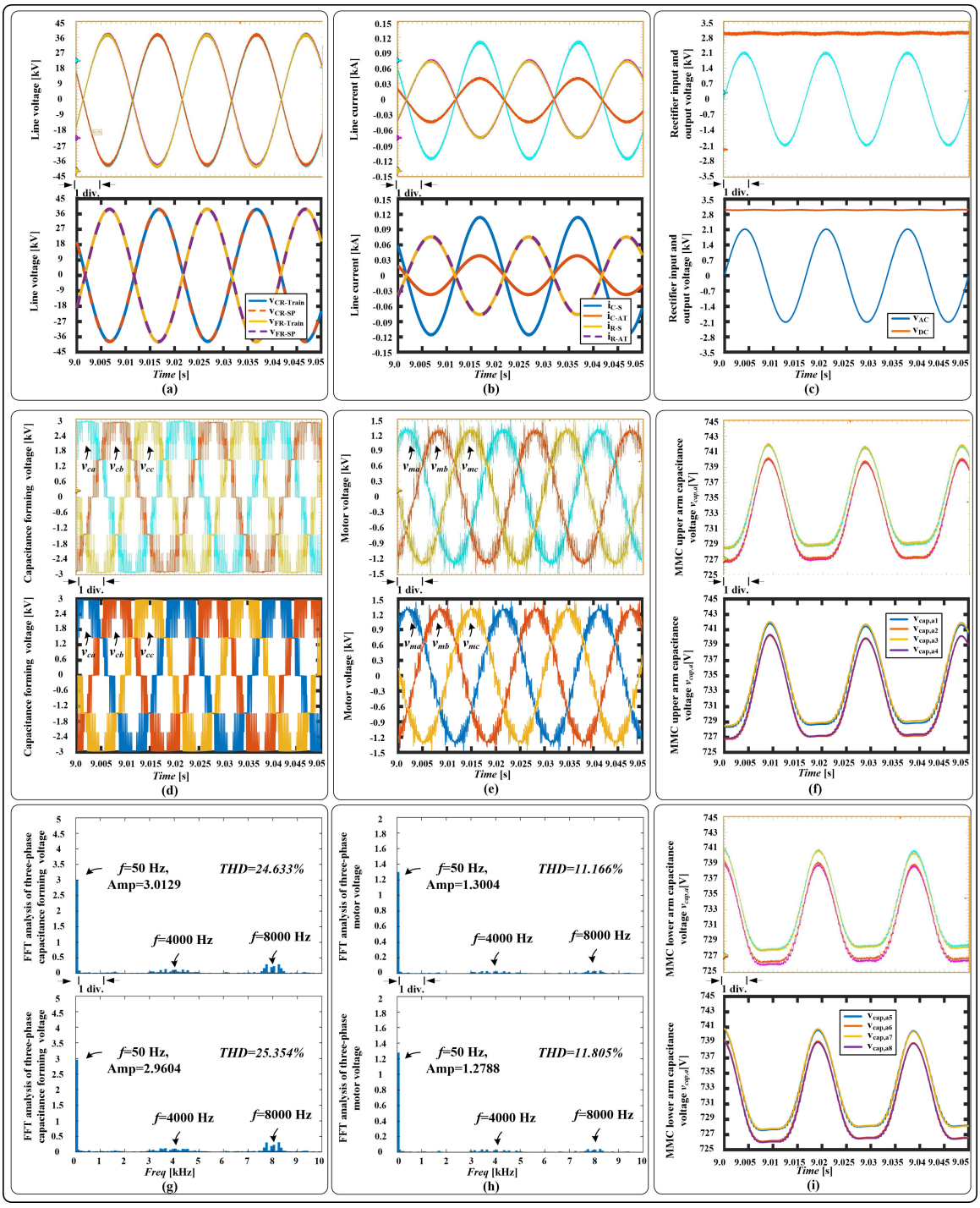

Figure 5.13: System-level results for complete traction system from real-time simulation (top oscilloscope sub-figure) and off-line simulation by PSCAD/EMTDC® software (bottom sub-figure) for: (a) Line voltage, (b) Line current, (c) Rectifier input and output voltage, (d) Capacitance forming voltage, (e) Motor voltage, (f) MMC upper arm capacitance voltage, (g) FFT analysis of capacitance forming voltage, (h) FFT analysis of motor voltage, (i) MMC lower arm capacitance voltage. Scale: (a) (b) (c) (d) (e) (f) (i) x-axis: $5ms$/div. (g) (h) x-axis: $1kHz$/div.

6

Adaptive Real-Time Hybrid Neural Network Based Device-Level Modeling for DC Traction

This chapter proposes the adaptive device-level model for the IGBT module based on the hybrid kNN-RNN structure, which is implemented on the FPGA platform and evaluated on the case study of the complete DC traction system. With a latency of 360ns, the kNN module is used to discern the transient switching condition. RNN module can be operated with less hidden layer neurons and training epochs with the aid of kNN module. The RNN module is split into two parts: training and prediction. The target for the training error is set at 0.05% within 20 epochs, while the prediction can be made within 140 ns for a transient result of 100 ns with MSE of 2.4%. The device-level transients are emulated with the latency of 100 ns for 100 ns per time-step in real world by circuit solver. The emulation results are validated by the professional simulation tools at the system-level and device-level. This hybrid neural network based modeling concept is a novel proposal in the domain of real-time device-level modeling in traction power systems.

6.1 Introduction

DC traction system, shown in Fig. 6.1, has been utilized to reduce land commute congestion for intercity traffic and subway transportation since the late nineteen century and specified into the study area of efficiency improvement [123], analysis and assessment [124] - [125], and fault detection [126]. Due to the insulation constraint, the DC traction voltage level was limited for several hundred volts in the nineteen century. The high energy loss of overhead line restrict the development of high-speed DC traction. In the mean time, AC traction dominate the market of high-speed traction for the twentieth century with the help of on-board high-voltage capable equipment which reduce the power loss

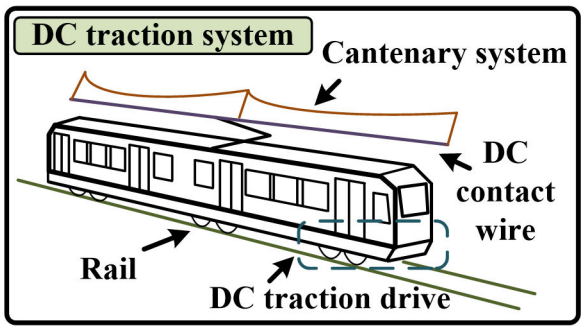

Figure 6.1: DC traction system.

in the power conversion stage. However, existing AC traction system suffers from the reactive power loss, the inductive line voltage drop, bulky transformer, and extra on-board AC-DC converter. With the development of power semiconductor and isolation technology, high-voltage capable DC circuit breaker, motor, and power electronic components are being increasingly adopted in the MVDC electrified system. There is a potential trend that some of the current AC high-speed traction system will be replaced or upgraded to MVDC high-speed traction system to reduce the manufacture and maintenance cost. However, Field testing the physical MVDC traction system is time-consuming and uneconomical, and might lead to possible device damage in certain scenarios.

Hardware-in-the-loop (HIL) technology, which can be utilized in a non-destructive environment, plays a vital role in the newly designed control algorithm, machine, and power converter topology. The performance of HIL simulator is highly related to the selection of compute hardware. Sequential computation hardware resource, such as the central processing unit (CPU), have limited cores which restrict the potential of fully extended parallel computation based on the specific application. In the future, application specific integrated circuit (ASIC) may accelerate the computation to meet the real-time requirement but the manufacturing costs increase exponentially. Multi-processor system-on-chip (MPSoC) contains high sequential clocking ARM® cores and massive parallel field programmable gate array (FPGA) resource with optimized communication between the compute hardware. However, merging the ARM® cores and FPGA into a single die lead to the shrinkage of the FPGA resource. Building the neural network based architecture requires massively parallel hardware device, such as the graphics processing unit (GPU) and FPGA. The communication time between the CPU and GPU takes several milliseconds; however the device-level transients happen within several hundred nanoseconds which make GPU unusable in the application of real-time device-level HIL emulation. Therefore, applying the FPGA is the optimal solution for utilizing the neural network which demand massive parallel compute structure and large hardware resource for real-time device-level modeling. FPGA based HIL high-performance computing hardware have been used previously to develop models for the power electronic applications.

In 1943, the artificial neural network (ANN) concept was developed with the discovery of enhanced connection in neurons and the possibility of representing the neuron connections by applying the modern electrical knowledge [127], [128] - [129]. Furthermore, several types of ANNs have been investigated in device transient simulation: 1) multi-layer perceptron (MLP) [20], 2) Radial-basis function (RBF) [21], 3) time-delay neural network (TDNN) [22], and 4) recurrent neural network (RNN) [23]. MLP requires an extremely large training set to get the accurate result for the simulation. RBF performance degrades in the dynamic characteristic simulation while the TDNN results in different training result for the same training set in different orders. RNN can provide an accurate prediction of dynamic behaviors and requires less training time. With the recurrent path, the new experimental results can be studied and learned within the expected training speed. Meanwhile, the model order reduction of RNN can also shorten the training processes and scale down the neural network topology if the negligible factors have little impact on the simulation accuracy.

However, if the power converter application scenario become complex, the number of neurons and buffers would be enlarged exponentially. There is a need to classify the switching scenarios to reduce the hardware consumption for real-time HIL application. The selected classifier needs to fulfill the real-time device-level transients timing requirement which happens within several hundred nanoseconds. Although some algorithm might be considered as a simple classifier, the computation time might not fulfill the real-time requirement. The main considerations for selecting the classifier are computation complexity, interpretability, adaptability, parallelism capability, hardware resource consumption, and execution time. Traditional classifiers have their drawbacks when implemented in FPGA hardware: 1) Logistic regression, which is considered as the simple model for classification, requires high-order nonlinear activation function to compute the result. In practice, the high-order Taylor series is applied to approximate the nonlinear function which requires up to several milliseconds to compute the result. A single division operation inside Taylor series approximation requires at least 8 clock cycles (80 ns when FPGA runs stable at 100 MHz). Besides, the logistic regression is known for high bias and its vulnerability to overfitting. Even when the nonlinear activation function can be realized by large look-up-table (LUT), it becomes hardware resource demanding. 2) Decision tree. This approach is considered an efficient way to classify the data, but it mandates people involved in preparing the classification with advanced pre-known knowledge for quantitative analysis. 3) Support Vector Machine (SVM). In order to meet the requirement of Karush-Kuhn-Tucker (KKT) conditions in SVM, the iterative calculation of estimation becomes a must for the data classification. Also, the iteration time is uncertain which makes the execution efficiency low for FPGA hardware because the design of iterative algorithm implemented in FPGA need to take the maximum iteration cycles to fulfill the condition for real-time HIL implementation. 4) Naive Bayes. It is known that Naive Bayes classi-

fier works based on the assumption that the independence of the feature. In our case, we can not prove the independence of the features (temperature and collector current). If the Gaussian Naive Bayes is applied, high-order Taylor series approximation of the exponential function takes a long delay time in hardware. Based on the FPGA hardware platform, the parallelized algorithm can be accelerated. The k-nearest neighbor (kNN) classifier consists of two major parts: distance calculation and sorting. Distance calculation can be implemented in FPGA parallel structure which only requires several clock cycles in the FPGA hardware. Traditional sorting algorithm including bubble sorting, insert sorting, selection sorting, cannot be fully implemented in parallel for FPGA architecture. Thus, tournament sorting method, which only takes O(log n) operations, is applied in this work to increase sorting speed and fit the FPGA parallel compute structure. With increasing data being collected in the future, the proposed classifier will not increase the number of execution cycles linearly and can be easily interpreted for the user. So we choose kNN as the classifier in this real-time HIL application. By applying the kNN classifier to distinguish the power electronic switch application scenario, the RNN topology can utilize less hardware compute resources during the training process [128] - [129]. Accordingly, the emulation circuit size can be enlarged for the same hardware setup with the accurate dynamic transients in multiple application scenarios.

This chapter proposes a power electronic device modeling method based on hybrid kNN-RNN neural network topology with the hardware emulation of device-level switching transients on the FPGA. A complete DC traction system is utilized as the study case to evaluate and validate the performance of the proposed real-time device-level model. The chapter is organized as follows: Section 6.2 explains the power electronic device characteristics, the concept of kNN and RNN, the proposed hybrid kNN-RNN architecture, permanent magnet synchronous machine (PMSM) model, and circuit transient solver; Section 6.3 describes the study case of the neutral point clamped (NPC) based DC traction drive system, complete DC traction system, hardware implementation platform, and detailed hardware implementation of RNN module and the circuit solver; Section 6.4 shows the proposed hybrid kNN-RNN module training performance, the system-level and device-level real-time emulation results verified by commercial off-line simulation tools, and hardware resource consumption.

6.2 Adaptive Hybrid Neural Network Modeling for Power Electronic Devices

6.2.1 IGBT and Diode Device-Level Characteristics

Normally a discrete IGBT module package consists of an IGBT and a freewheeling diode. The Norton equivalent of the IGBT module is shown in Fig. 6.2. The IGBT is represented by the conductance g_{S1} in parallel with the voltage controlled current source (VCCS) i_{S1},

while the diode acts as the conductance g_{D1} in parallel with VCCS i_{D1}. The model of IGBT module can be classified into static and switching characteristics. The static features are highly related to the junction temperature T_{vj} and the operating current. According to the value of the current, the static characteristics can be divided into two linear regions: low current region and high current region, given as:

$$g_{region}(T_{vj}) = \frac{T_{vj}-25}{25-125}(g^{25}_{region} - g^{125}_{region}) + g^{25}_{region}, \tag{6.1}$$

$$v_{region}(T_{vj}) = \frac{T_{vj}-25}{25-125}(v^{25}_{region} - v^{125}_{region}) + v^{25}_{region}, \tag{6.2}$$

$$i_{region}(T_{vj}) = v_{region}(T_{vj}) \cdot g_{region}(T_{vj}), \tag{6.3}$$

where $g_{region}(T_{vj})$ and $i_{region}(T_{vj})$ are specific region conductance and VCCS, respectively. Linear approximation has been applied to obtain the conductance and VCCS under the designated temperature.

Transient switching characteristics are also presented in Fig. 6.2 which include IGBT turn-on and turn-off, and diode turn-off transient waveforms. Diode forward recovery transient is not included because its energy loss is negligible compared to the total switching loss.

The thermal circuit, which provides the device temperature based on the power loss, consists of a series of thermal resistors in parallel with thermal capacitors, VCCS, and the voltage source. The VCCS on the left indicates the power loss and the voltage source on the right represents the ambient temperature. T_{vj}, T_{case}, T_{hs}, and T_{amb} are the temperatures of junction, case, heatsink and ambient, respectively.

6.2.2 k-Nearest Neighbor Concept

The k-nearest neighbor utilizes distance calculation and majority voting mechanism to classify the test data. With more instances, the classification can be performed with higher correctness; however, the computational burden and the hardware resource also increase linearly. The distance calculation applies the Euclidean distance function, given as:

$$Distance = \sqrt{\sum_{i=1}^{m}(a_i - b_i)^2}, \tag{6.4}$$

where a_i is the test data and b_i is the instance from the database, m is the number of the features to be classified.

In Fig. 6.3, k-nearest neighbor concept is shown with various geometrical shape treated as the different class of instances. k is the number of the nearest neighbors. For example, when k equals 3, 2 green squares and 1 red triangle are included inside the circle. Based on the majority voting mechanism, the interest point belongs to the green square class if the weights of the instances are set equally. Correspondingly, when k equals 9, 4 red triangles

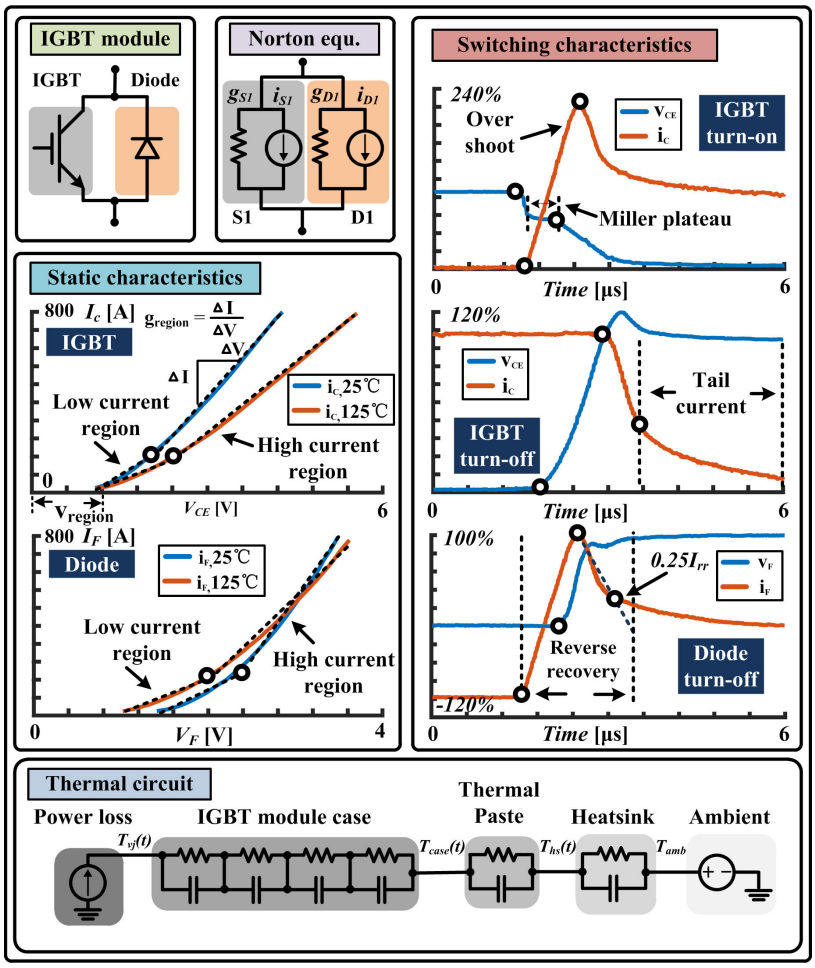

Figure 6.2: IGBT module characteristics and its thermal circuit.

and 3 green squares are encircled. If the majority voting weights are still balanced, the classification result becomes red triangle class. If the weight is set to the square of the distance, the outcome is changed to the green square class. Hence the classification result is highly related to the weight of the voting mechanism.

From the point of implementation, the kNN classifier's resource consumption increases linearly when tuning the k value or increase the number of sample points which fits the optimized parallel compute structure in FPGA hardware. kNN calculation processes can be simplified into three main portions: 1) Distance calculation, 2) Minimum sorting, 3) Majority voting. Distance calculation and minimum sorting are considered as the most time-consuming parts. Distance calculation can be implemented into the massive paralleled structure which reduces the calculation time to the same as the single distance calculation unit. Minimum sorting can apply the different sorting algorithms. For a small k value, apply traditional algorithm is time-consuming and also need to go through each element several times. By applying the tournament sorting, it only requires 7 clock cycles for a scale of 128 elements for sorting one minimum element. This work applies this sorting

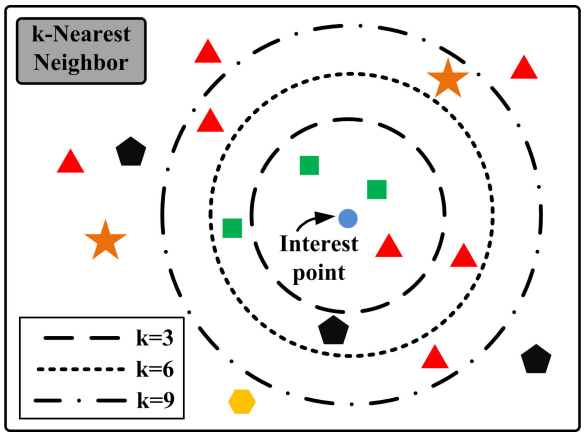

Figure 6.3: k-nearest neighbor.

method for reducing the time in the process. The k value is selected as 4 for the sorting, which is based on the sorting performance and the hardware resource consumption. The performance of the kNN is summarized by the confusion matrix which gives an error case table layout.

6.2.3 Recurrent Neural Network

A RNN is a class of ANN that allows the network to maintain a series of historical states and better performance in sequence model prediction. The typical recurrent neural network structure is shown in Fig. 6.4 with the detail of the hidden layer and output layer neurons. The historical values from the input layer and output layer are saved and delivered to hidden layer for the next time-step prediction. The hidden layer neuron receives the signals from the input layer and multiply them with weights, and provides the summation of the product. With the nonlinear activation function ψ, the multiplication and summation product θ become the input product λ of the output layer. The relation of input and hidden layer is given as:

$$\begin{aligned} \theta_m = & \sum_{c=0}^{K_p-1} \sum_{d=1}^{N_p} p_d(t - c \cdot \Delta t) w_{m[K_y N_y + c \cdot N_p + d]} \\ & + \sum_{e=1}^{K_y} \sum_{f=1}^{N_y} y_f(t - e \cdot \Delta t) w_{m[(e-1)N_y + f]} + b_m, \\ & m = 1, ..., N_h, \end{aligned} \tag{6.5}$$

$$\lambda_m = \psi(\theta_m), \tag{6.6}$$

where K_p and K_y are the number of time delay buffers for input parameters p_d of input layer and output product y_f of output layer, respectively, N_p, N_h and N_y are the number of input parameters, hidden layer products, and output products, respectively, w and b

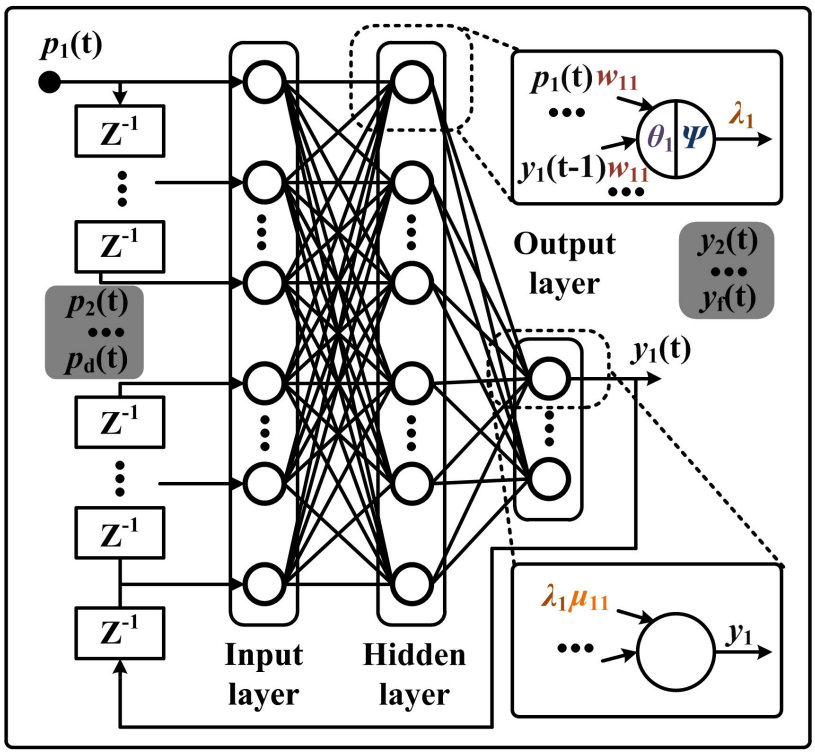

Figure 6.4: Block diagram of recurrent neural network.

are the weight and bias in the hidden layer neuron, respectively, Δt is the emulation time-step in the study case, ψ is the nonlinear activation function (Sigmoid) in the hidden layer neuron. The relation of the hidden layer and output layer is given as:

$$y_i(t) = \sum_{j=1}^{N_h} \mu_{ij} \lambda_j + \delta_i, \tag{6.7}$$

where $y_i(t)$ is the output of the output layer, μ_{ij} is the weight of the output layer, λ_j is the input of the output layer, δ_i is the bias of the output layer. The training scheme utilized the back propagation through time (BPTT) method to derive the Jacobian matrix. The training objective is to minimize the loss function, given as:

$$\min \frac{1}{2} \sum_{a=1}^{N_s} \sum_{b=1}^{N_y} \sum_{c=1}^{N_w} (y_{ab}(t) - y'_{ab}(t))^2, \tag{6.8}$$

where N_s is the total number of transient points in a single sample waveform, N_w is the total number of sample waveform, $y_{ab}(t)$ is the hybrid kNN-RNN neural network output product while $y'_{ab}(t)$ is the real test result.

6.2.4 Proposed Hybrid kNN-RNN Representation of IGBT and Diode Switching Characteristics

In Fig. 6.5, the flowchart of the proposed hybrid kNN-RNN structure is given with detailed processes. When the hybrid structure begins to function, the RNN module starts the initial training with the pre-classified (12 regions) instances which are categorized by the current rating, device junction temperature, and the switch on and off states. The pre-classified instances for training includes the following time-series data in 100 ns time-steps: 1) switch on or off transient power loss based on the static IGBT collector current I_C or diode forward current I_F, and device junction temperature T_{vj}, 2) system-level collector current (IGBT) or forward (diode) current, which can be obtained by the transient circuit solver. The training waveform of transient power loss is gathered by four sets of device junction temperature (T_{vj} =25, 35, 45, 55 ... 125 °C, within 0.5 °C error) with a step of 10 °C and device operating current (0, 50, 75, 100, 125, 200, 350, 500, 650, 900, 1200 A, within 2A error). Thus, there are 484 samples (on and off state), which are device-level simulation results from SaberRD®. 15% of the samples are utilized as the validation set to avoid over-fitting while another 15% samples are used for testing. The rest 70% of samples are for the model training. The output of the RNN module is the transient IGBT collector current i_C or diode forward current i_F. The IGBT module current combines these two currents as the output.

With the initial circuit parameters and control signals, the dynamic kNN module starts to classify the current, temperature and on-off states mentioned above. The kNN module classifies the scenarios into two current regions (low and high), three temperature regions (low, medium, high) and two states (on or off). Thus, 12 regions are classified before entering the RNN module. In the training process, each region can obtain different weight update information. Data normalization process, which converts original data to the similar range in terms of the number value, is applied to the input data to help the kNN module to get better classification result. After normalization, distance calculation with the instances can be implemented in parallel. When the product of the distance calculation comes out, the majority voting weighted by distance gives the most possible switch state transient scenarios. Based on the temperature and current rating, newly generated transient power loss for each test scenario can be obtained by linear approximation.

The dynamic RNN module loads the data from the kNN module. From the input layer to the hidden layer, the input data multiples the weights and adds up the bias and gets the product for the activation function. The result of the activation function goes into the output layer which also contains the operation of weight multiplication and summation, after which, the prediction values of the transient waveform are transmitted to the circuit transient solver.

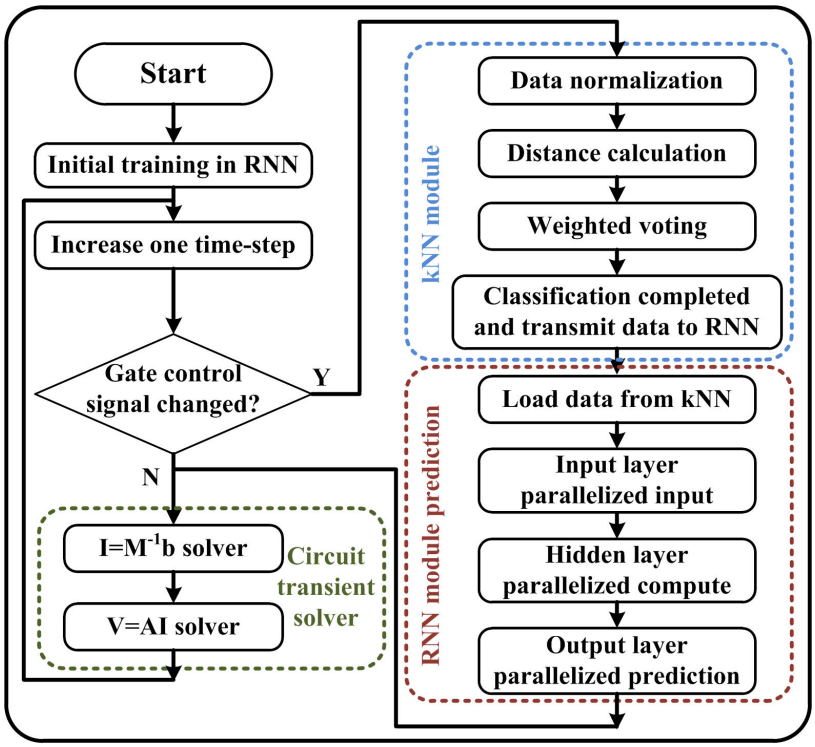

Figure 6.5: Flow chart of hybrid kNN-RNN structure for drive modeling.

6.2.5 Permanent Magnet Synchronous Machine

The PMSM is a strong candidate for DC traction system mainly due to the high power density, light weight, and advantageous energy efficiency. The flux linkage is the magnetic field linking with the coil conductor, as given below:

$$F_q = L_q i_q, \tag{6.9}$$

$$F_d = L_d i_d + F_{rm}, \tag{6.10}$$

where (i_d, i_q), (L_d, L_q), and (F_d, F_q) are d and q axis current, inductances, and flux linkage, respectively. F_{rm} is the flux linkage related to the rotor magnets linking the stator. The calculation of d and q axis voltages are given as:

$$v_d = r_s i_d + pF_d + \omega_r F_q, \tag{6.11}$$

$$v_q = r_s i_q + pF_q + \omega_r F_d, \tag{6.12}$$

where r_s and ω_r are the resistance of the stator and rotor speed, respectively. The dynamic between the electromagnetic and load torque are highly related to each other, given as:

$$T_e = 3P[F_{rm} i_q + (L_d - L_q) i_d i_q]/2, \tag{6.13}$$

$$T_e = T_L + B\omega_r + Jp\omega_r, \tag{6.14}$$

where T_e and T_L are the electric torque and the load torque, respectively, P is the number of polar pairs, B is the damping coefficient, and J is the rotational inertia.

6.2.6 Circuit Transient Solver

The circuit transient solver is mainly adopted from [130] and is based on Nodal analysis method. Linear elements are discretized by Trapezoidal rule by convention; however, to avoid a time-varying admittance matrix, the nonlinearities (including switches) are first viewed as either current or voltage sources whose values are taken from the kNN-RNN results. These current/voltage sources are then represented by an equivalent constant resistor in parallel with a time-varying current source in the circuit. In such a configuration, the following matrix equation can be constructed:

$$\mathbf{GV} = \mathbf{I}', \tag{6.15}$$

where $\mathbf{G}$ is a constant admittance matrix; $\mathbf{V}$ is the node voltage vector and $\mathbf{I}'$ is the summation vector of current source at each circuit node. Equation (6.15) then can be transformed into the following form:

$$\mathbf{GV} = \mathbf{I}' = \mathbf{TI}, \tag{6.16}$$

where $\mathbf{I}$ is the independent current source vector and $\mathbf{T}$ the corresponding current incidence matrix (whose entries are ± 1 or 0) for every individual node. Obvisouly, $\mathbf{T}$ is only determined by circuit topology and remains unchanged during simulation. The node voltage vector can be calculated using the following equation:

$$\mathbf{V} = \mathbf{G}^{-1}\mathbf{TI} = \mathbf{AI}, \tag{6.17}$$

where $\mathbf{A} = \mathbf{G}^{-1}\mathbf{T}$ is also a constant matrix. Equation (6.17) implies that as long as the companion current source of every element in the circuit is known, the node voltage is result of constant matrix-vector multiplication.

The companion current source of the linear element can be computed using the trapezoidal rule. To expedite the solution process of nonlinear elements' companion current source, the values of their equivalent resistors are chosen to be 1 so as that the matrix for solving $\mathbf{I}$ only has time-varying part on the diagonal, as given below.

$$\mathbf{MI} = \mathbf{b}, \tag{6.18}$$

where matrix $\mathbf{M}$ has time-varying diagonals and constant off-diagonals and $\mathbf{b}$ is a known vector based on historical information. Based on the feature of $\mathbf{M}$, several high efficient algorithms like Sherman-Morrison formula can be employed for solving $\mathbf{I}$. It has to mention that the varying forms of $\mathbf{M}$ are related to the switching states of the converter and $\mathbf{M}$ is always non-singular under normal switching states. Once the values of vector $\mathbf{I}$ are known, the node voltage vector $\mathbf{V}$ can be obtained easily by use of (6.17).

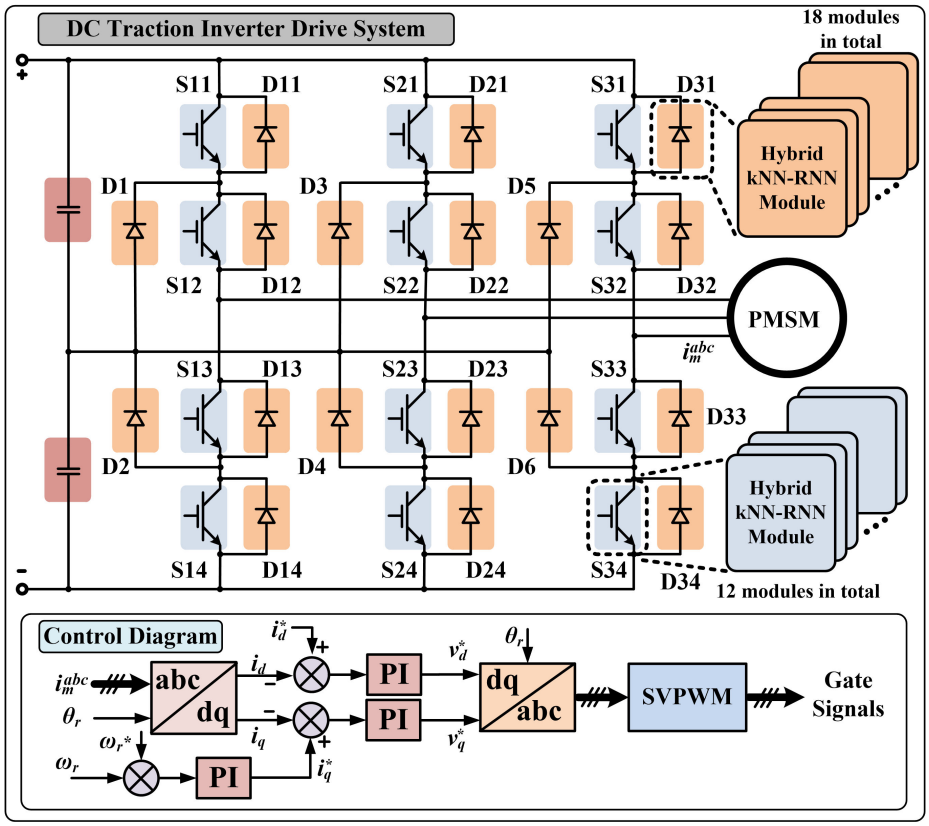

Figure 6.6: DC traction drive system case study employing the proposed hybrid kNN-RNN modules.

6.3 Hardware Emulation of Hybrid kNN-RNN based DC Traction Drive System

This section presents the DC traction drive system and its control system, complete DC traction system, implementation platform, and detailed hardware implementation of the RNN prediction module and circuit transient solver.

6.3.1 DC Traction Drive System

The three-level DC traction drive system is the study case for testing the proposed hybrid kNN-RNN neural network concept. The study case parameters and the IGBT module part number are provided in the Appendix. As presented in Fig. 6.6, the three-level DC traction inverter is composed of 12 IGBTs and 18 diodes. These switches are treated as voltage sources during turn-on transient and steady on state, and as current sources during turn-off transient and steady off state. Closed-loop speed regulator is realized and abc/dq coordinate transformation is implemented where d-axis current is always tuned to zero to keep the magnetic field constant and q-axis current is tuned by the output of speed control loop to adjust the electromagnetic torque. Space vector pulse width modulation

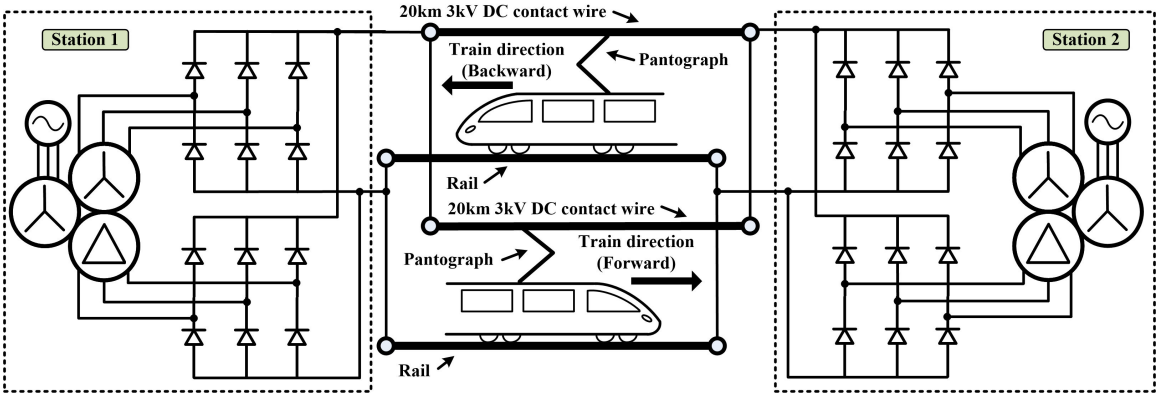

Figure 6.7: Complete DC traction system.

(SVPWM) is employed to generate the switch drive signals. The hybrid kNN-RNN module is embedded in each power electronic device. In this work, three practical IGBT modules are considered to connected in parallel as one module in the emulation to meet the current rating requirement.

6.3.2 Complete DC Traction System

The DC traction system, shown in Fig. 6.7, employs the current geometric distance and the speed requirement of the Guangzhou-Zhuhai intercity railway AC traction system. The geometric distance is 115.625 km and the designed railway speed limit is 200 km/h. Based on the requirement of the speed limit and the current station spacing distance, 3 kV is selected as the voltage rating of the system. Thus, we proposed the 3kV DC substation configuration with a 20 km substation spacing to the Guangzhou-Zhuhai intercity railway DC traction system. The proposed DC traction system consists of seven DC substations with 20 km substation spacing, which made the complete railway network as a 120 km railway configuration. Inside the DC traction system, autotransformer rectifier units (ATRUs) are considered to provide the power to train via the catenary system and DC contact wire, modeled as a traveling wave line model, in the emulation process.

Both system-level and device-level models are employed in the complete DC traction system with the proper system order-reduction modeling method. The traveling wave line model can decompose the system into two sections without any computation precision loss. For each side, the traveling wave line model represents a characteristic impedance in parallel with the VCCS which utilized the previous time step information of the other side to compute the value of the current. With this technique, the complete system can be separated into four subsystems: two DC traction drive system and two substation system. The substation system applies the system-level model while the traction drive system utilizes the device-level model. The system-level model employs the ideal model while the device-level model applies the proposed hybrid neural network topology.

6.3.3 Hardware Platform

The Virtex® Ultrascale+ VCU118 evaluation kit, shown in Fig. 6.8, employs the XCVU9P-L2FLGA2104 core which contains 2,586,000 logic cells and 6,840 DSP slices. The board consists of 2.5 GB DDR4, 120 GTY transceivers, 832 general purposes I/O, dual QSFP28 interfaces, 16-lane PCI-E interface and other components.

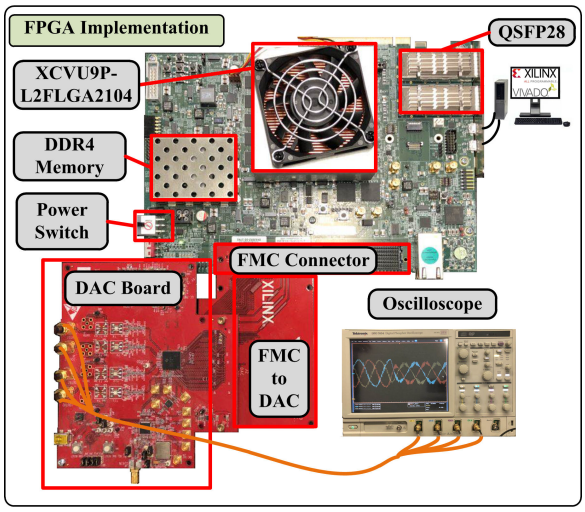

Figure 6.8: Hardware configuration of hybrid kNN-RNN based drive modeling.

6.3.4 Implementation of RNN Prediction Module

The detailed implementation of the RNN prediction module is shown in Fig. 6.9. After the initial training process of RNN, the trained weight values are stored in the look-up table of the hardware. After classification by the kNN module, the kNN module selects the appropriate RNN prediction module parameters. The weights and the input parameters are transmitted in parallel to the RNN prediction module. After the first layer of multiplication, intermediate variables need to be processed by multiple layers of summation to get the hidden layer intermediate variable θ and output layer output y. The activation function has been reshaped into the form of piece-wise linear function, which utilized the slope s and the bias l to calculate the activation output. The total RNN prediction delay time can be calculated in the following form:

$$\begin{aligned} t_{pred} = &\max[\text{ceil}(t_m + (\log_2 N_p + \log_2 K_p)t_s), \\ &\text{ceil}(t_m + (\log_2 N_y + \log_2 K_y)t_s)] + 2t_m \\ &+ \text{ceil}(\log_2 N_h + 4)t_s, \end{aligned} \tag{6.19}$$

where t_m and t_s are the delay for a single multiplication and summation operation, respectively. Multiple similar structures are also computed in parallel to get similar intermediate

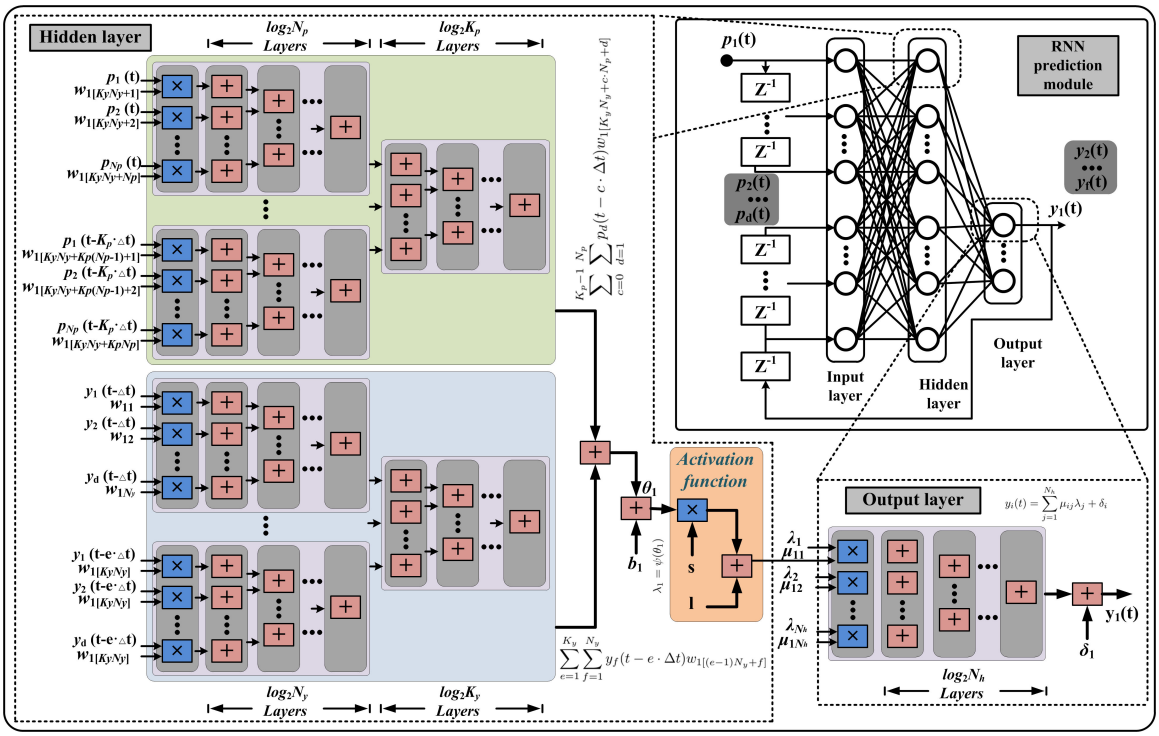

Figure 6.9: RNN prediction module hardware implementation block diagram.

variables and the final output. In this work, all the function operation utilized the 59-bit fixed point format to reduce the hardware resource consumption and meet the hybrid neural network and circuit solver accuracy requirement. Both t_m and t_s require one system clock cycle (10 ns) at 100 MHz FPGA operating frequency. Both delay buffer number K_p and K_y equal 4 while input number N_p equals 2. The hidden layer number N_p equals 10 while the output number N_y equals 1. The hardware prediction time delay is 140 ns for 100 ns time-step emulation requirement. However, the natural switching delay usually takes several microseconds. Thus, the RNN module can predict the 20 transient points before the end of switching transient.

6.3.5 Implementation of Circuit Transient Solver

The circuit transient solver is composed of two modules: one is responsible for solving the companion current sources of all components in the circuit; and the other is in charge of solving the node voltages based on the admittance matrix and the corresponding companion current sources. As illustrated in Fig. 6.10, the companion current sources of the nonlinear elements (switching devices and PMSM) are solved by $\mathbf{I} = \mathbf{M}^{-1}\mathbf{b}$ while counterparts of linear elements are computed using the trapezoidal rule. After the companion current source vector $\mathbf{I}$ is obtained, the node voltage vector is calculated by matrix-vector multiplication $\mathbf{V} = \mathbf{AI}$. The 18 switching devices are decomposed into 3 groups each corresponding to one phase leg. As a result, the matrix size of $\mathbf{M}^{-1}$ is 6×6 and $\mathbf{A}$ is 12×23.

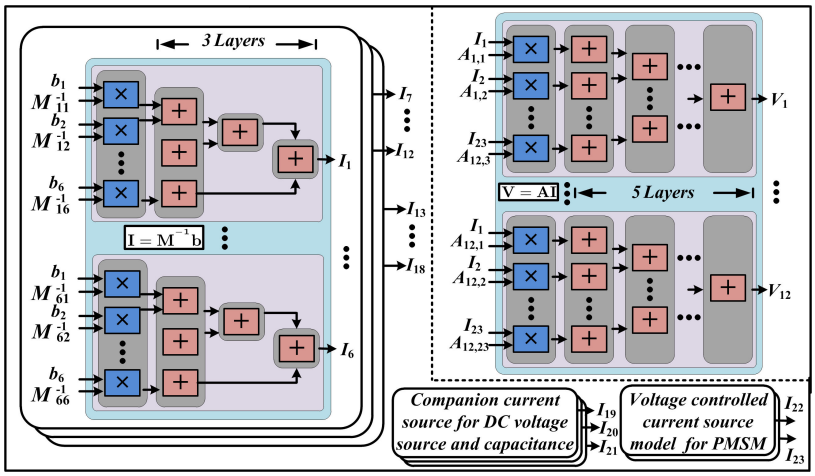

Figure 6.10: Circuit transient solver hardware implementation block diagram.

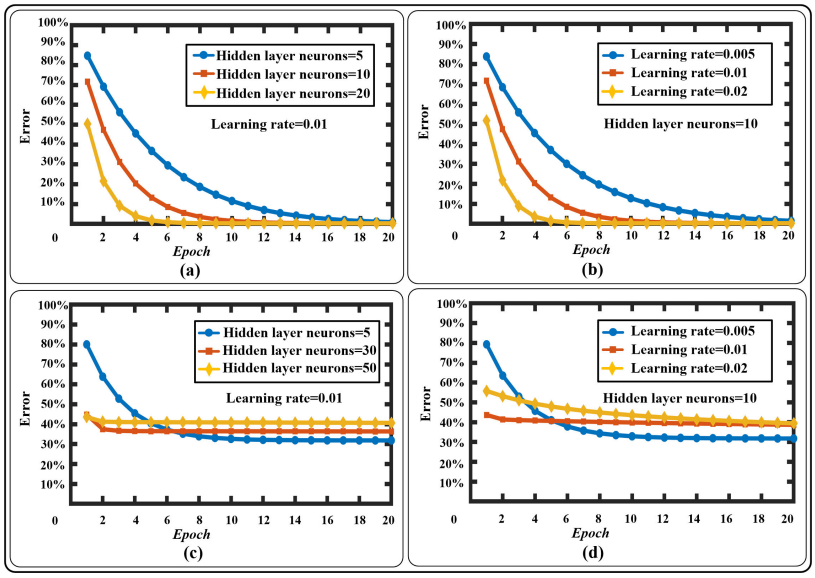

Figure 6.11: Error-cost curves of kNN-RNN: (a) With fixed learning rate and kNN classification. (b) With fixed hidden layer and kNN classification. (c) With fixed study but without kNN classification. (d) With fixed hidden layer but without kNN classification.

The total clock cycles consumed by circuit solver is $2t_m + [\text{ceil}(\log_2 6) + \text{ceil}(\log_2 23)]t_s$=10 (100 ns).

6.4 Results and Discussion

In this section, the performance of the hybrid kNN-RNN module, system-level and device-level results comparisons, hardware resource consumption are provided with detailed discussion.

In Table 6.1 and 6.2, the confusion matrix is given in both turn-on and turn-off states.

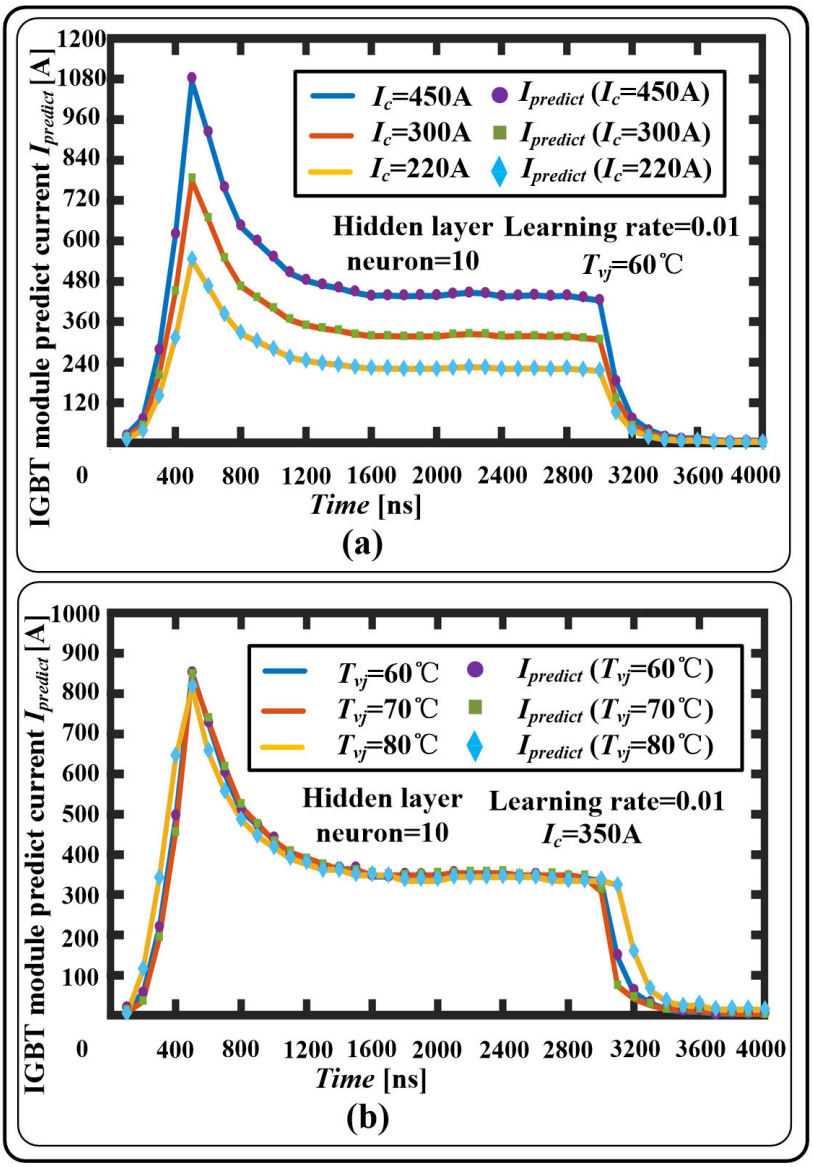

Figure 6.12: kNN-RNN prediction for IGBT module current: (a) Under specific temperature. (b) Under different temperatures.

The row stands for the ture class and the column represents the predicted class by kNN. The classification results are collected from 100 linearized data from 25 °C to 125 °C in terms of temperature and 0 to 1000 A for current value. LT, MT, and HT are the abbreviations for low temperature (25 °C - 58 °C), medium temperature (59 °C - 92 °C), and high temperature (93 °C - 125 °C), respectively. LC and HC are the abbreviations for low current (0 - 200 A) and high current (200 A and higher), respectively.

In Fig. 6.11, the hybrid kNN-RNN performance is shown with the comparison of the absence of kNN module. The training initializes the weights with random parameters. All the input parameters have been normalized in order to get the better training result with

Table 6.1: Confusion Matrix in Turn-On State for kNN

	LTLC	MTLC	HTLC	LTHC	MTHC	HTHC
LTLC	6	0	0	0	0	0
MTLC	0	7	0	0	0	0
HTLC	0	1	6	0	0	0
LTHC	0	0	0	25	0	0
MTHC	0	0	0	0	27	1
HTHC	0	0	0	0	1	26

Table 6.2: Confusion Matrix in Turn-Off State for kNN

	LTLC	MTLC	HTLC	LTHC	MTHC	HTHC
LTLC	6	0	0	0	0	0
MTLC	0	7	1	0	0	0
HTLC	0	0	6	0	0	0
LTHC	0	0	0	26	1	0
MTHC	0	0	0	0	26	1
HTHC	0	0	0	0	1	25

few epochs. In Fig. 6.11 (a), the error-cost curve with kNN classification shows the performance of a fixed learning rate and different hidden layer neuron number. With kNN classification, the RNN module with higher hidden layer neuron number under fixed learning rate gets to the target error with fewer epochs. Fig. 6.11 (c) presents the performance of the same setup parameters in training without kNN classification. It is noticeable that the error rate stops decreasing between 30% and 40%. The increase of the hidden layer neuron number cannot help to decrease the error with the same epochs but gives a higher error in return. The performance of different learning rate with fixed hidden layer neuron number is provided in Fig. 6.11 (b) and Fig. 6.11 (d). It is evident that higher learning rate can accelerate the training processes, but the error increases after epochs if the learning rate is high over the RNN training capacity. Low learning rate can make the training error decrease properly but may need more epochs to reach the target error. The possibility of finding the local optimal point increases with low learning rate in the training processes. Without kNN classification, error rate stays between 30% and 40% with different learning rates in training.

In Fig. 6.12 (a), the hybrid kNN-RNN module prediction result is provided for the different current operating condition for IGBT module with fixed hidden layer number, learning rate and junction temperature in the training processes. The thermal impact of the power electronics drive and the training results are presented in Fig. 6.12 (b). Clearly, the thermal issue shows less impact than the different rating of current.

The system-level output waveforms from the hybrid kNN-RNN based model and PS -CAD/EMTDC® are shown in Fig. 6.13 with detailed comparison. Fig. 6.13 (a) and (d) ex-

hibit the rotor electrical speed and electromagnetic torque when speed command increases from 0 to 1.0 p.u. linearly during $1 \sim 4$ s and decreases abruptly from 1.0 p.u. to 0.7 p.u. at $t = 6.0$ s and back to 1.0 p.u. at $t = 7.5$ s. Fig. 6.13 (h) and (i) show the rotor electrical speed and electromagnetic torque when speed command decreases from 1.0 p.u to 0 linearly during $360 \sim 364$ s. 6.13 (b) and (c) illustrate the three-phase machine stator currents when the speed command applied to the drive system, respectively. Fig. 6.13 (e) and (f) are the corresponding converter output voltages. Fig. 6.13 (g) is the station power output where the DC contact wire energization can be observed in the first 0.3 s. Stable output power can be seen at 5 s. Indisputably, these closed simulation results demonstrate that the hybrid kNN-RNN model provides high-precision and convincing system-level results.

In Fig. 6.14, the comparison between real-time HIL implementation and off-line software simulation results are shown with switching transients at device-level. The ideal switch model represents the off state as the low conductance and the on state as the high conductance and gives the emulation result close to the simulation result in PSCAD/EMT -DC®. SaberRD® utilizes the IGBT module behavioral model to represent the device-level model and the proposed hybrid kNN-RNN model provides the highly similar waveform in hardware emulation where current overshoot and tail current can be observed.

Fig. 15 (a) and (d) show the device junction temperature from 1 to 6 s and zoomed-in figures from 5.8 to 6 s. The time period with no power loss or less power loss would introduce temperature cooldown for the specific power electronic device. S_{11} is considered as most power demanding device in the arm and its temperature peaks at 54 °C. S_{12} temperature does not stop increase at the time of 6 s but its temperature would not exceed the one of S_{11}. D_{11} and D_{12} have a lower power loss on each switch-off transients which introduces lower temperature during the time. D_1 has both more conduction and switching time than the other two diode in the arm. Thus, a higher operation temperature have been observed from the real-time emulation and off-line simulation.

Table 6.3 exhibits the comparison result of PSCAD/EMTDC® simulation and FPGA emulation for left and right arm current of the DC traction system. Different location of the train resulted in different current distribution on the DC contact wire. 10 km, which is the middle point between the two station, requires the maximum of current summation for the train. In return, the maximum DC contact wire voltage loss can been observed in the Table 6.4 at the distance of 10 km. Thus, the middle point between the stations can be considered as the most power demanding point for the traction power conversion stage. If the design of the DC traction desires lower voltage drop, higher DC voltage rating of contact wire, up to 10.5 kv, can reduce the line loss and extend the station spacing to 55 km [125]. However, the investment of the high-voltage capable equipment might increase exponentially. High-level modular multilevel converter (MMC), high-voltage silicon carbide power electronic, high-voltage isolation equipment will become the expensive options to the high-voltage

Table 6.3: PSCAD/EMTDC® Simulation and FPGA Emulation Result Comparison of Left Arm and Right Arm Current

Dis (km)	i_{lsim} (A)	i_{lem} (A)	i_{rsim} (A)	i_{lem} (A)
0	588.34	589.60	0.75	0.31
2.5	529.72	529.10	74.91	74.90
5	462.45	463.59	154.61	154.51
7.5	388.50	388.69	232.70	233.01
10	314.17	314.62	314.17	314.62
12.5	233.32	233.18	388.90	388.80
15	154.49	155.48	463.32	463.56
17.5	75.10	75.83	529.56	530.22
20	1.15	0.786	591.76	591.42

Table 6.4: PSCAD/EMTDC® Simulation and FPGA Emulation Result Comparison of DC Contact Wire Voltage

Dis (km)	v_{dcsim} (v)	v_{dcem} (v)
0	2986.42	2986.18
2.5	2907.85	2908.40
5	2849.61	2849.90
7.5	2812.69	2814.02
10	2801.57	2800.98
12.5	2813.01	2813.59
15	2849.41	2849.76
17.5	2908.45	2908.43
20	2986.86	2986.84

Table 6.5: FPGA Hardware Resource Consumption for DC Traction Drive System and Proposed Hybrid kNN-RNN Stucture

	BRAM	DSP	FF	LUT
kNN (60)	0	0	0.5%	15%
RNN (60)	0	0	0.6%	1.8%
Train 1	4.9%	14.6%	4.2%	10.7%
Train 2	4.9%	14.6%	4.2%	10.7%
Station 1	0.4%	3.4%	0.9%	2.4%
Station 2	0.4%	3.4%	0.9%	2.4%
Total	10.6%	36%	11.3%	43.1%

capable traction drive system. There is a trade-off point for each specific application. For intercity transit, 3 kv is considered as the trade-off point.

The FPGA resource consumption for study case is illustrated in Table 6.5. 10.6% Block RAM, 36% DSP slices, 11.3% flip-flops and 43.1% look-up-table have been utilized during the implementation. The latencies of hardware implementation are shown in Table 6.6

Table 6.6: Latencies of Hardware Implementation

kNN classification	RNN prediction	Circuit transient solver
360ns	140ns	100ns

with the operating frequency of 100 MHz in FPGA. The kNN module takes 360 ns with fully paralleled and pipeline optimization hardware design in FPGA. The RNN trains the instances with 0.05% error training target, 10 hidden layer neurons, learning rate at 0.01, and 4 delay buffers. The RNN prediction takes 140 ns to perform a 100 ns time-step wise of the waveform. The mean square error (MSE) of the prediction is less than 2.4%. The delay time of the IGBT module is usually several microseconds so the RNN prediction part can give the result before switching happens. This low prediction time can ensure that the predicted waveform data is delivered to the circuit transient solver in time, which can then perform the 100 ns time-step real-time emulation.

6.5 Summary

Detailed modeling of device-level power electronic device switching transients is onerous. This chapter proposed the adaptive hybrid kNN-RNN based device-level model for the IGBT module, which is implemented on the FPGA platform and tested on the study case of complete DC traction system. The kNN module is utilized to distinguish the transient switching state with a latency of 360 ns. With the help of kNN module, RNN module can be operated with less hidden layer neurons and training epochs. RNN module is divided into two sections: training and prediction. The training error target is set at 0.05% within 20 epochs while the prediction can be performed within 140 ns for a 100 ns time-step transient results with MSE of 2.4%. The device-level transients are emulated with the latency of 100 ns in circuit solver. The emulation results are validated by the professional simulation tools at the system-level and device-level. The proposed method provides a solution to model complex power converter topologies for practical applications such as transportation power systems, which maintaining sufficient device-level accuracy.

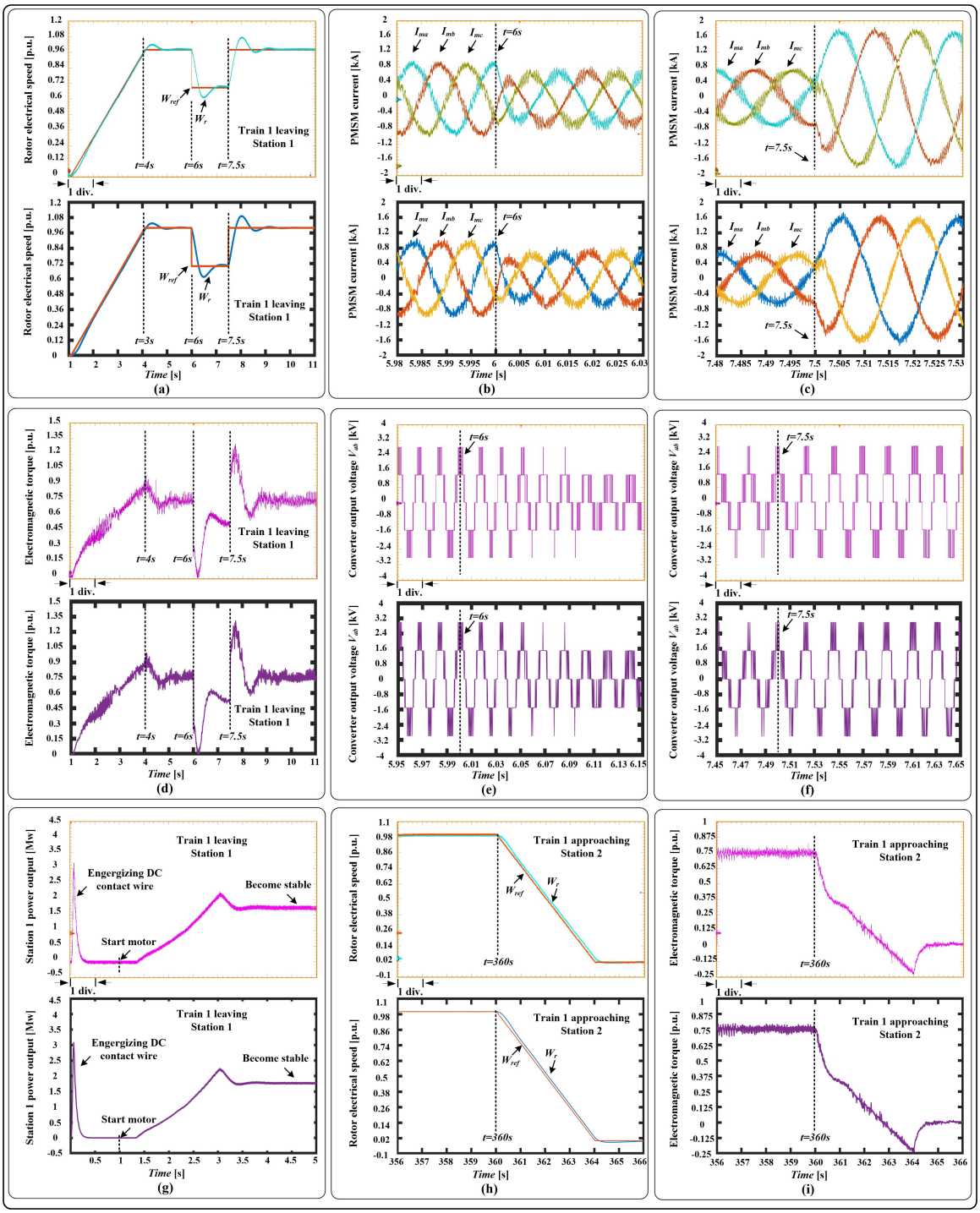

Figure 6.13: System-level results for DC traction drive system from real-time emulation (top oscilloscope sub-figure) and off-line simulation by PSCAD/EMTDC® software (bottom sub-figure) for: (a) (h) Rotor electrical speed. (b) (c) Three-phase PMSM currents. (d) (i) Electromagnetic torque. (e) (f) Converter output voltages. (g) Station 1 power output. Scale: (a) (d) (h) (i) x-axis: $1s$/div. (b) (c) x-axis: $5ms$/div. (e) (f) x-axis: $2ms$/div. (g) x-axis: $0.5s$/div.

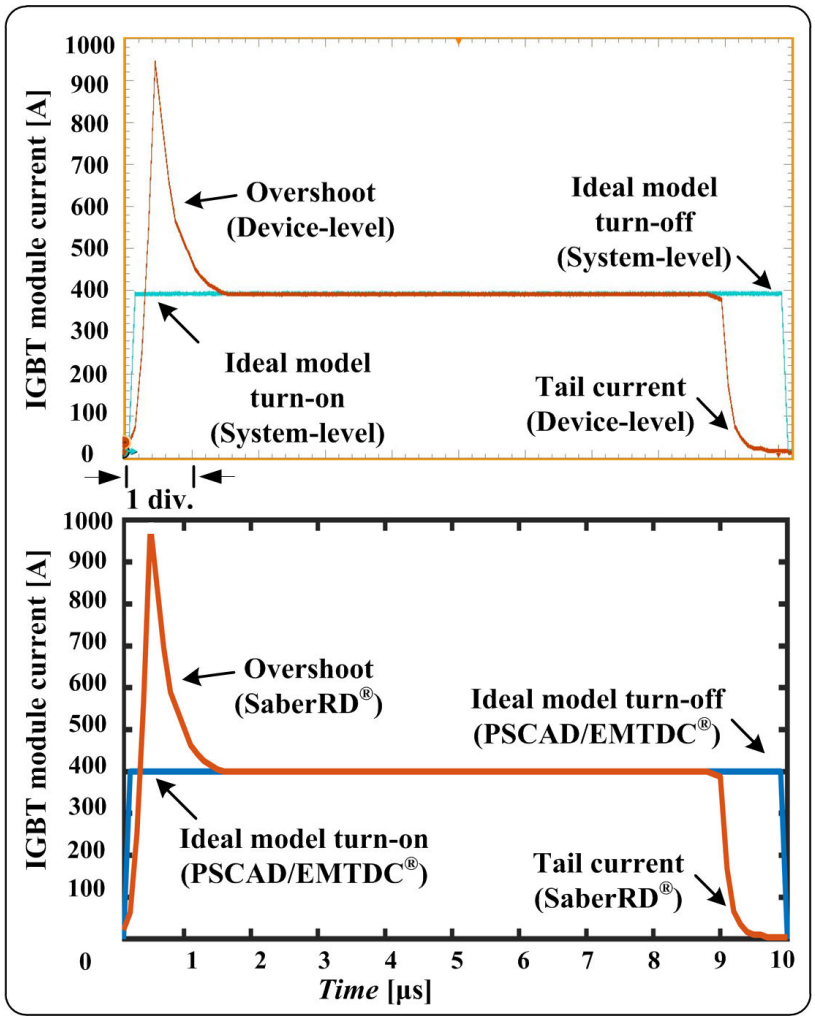

Figure 6.14: Device-level results comparison between real time HIL emulation (top oscilloscope sub-figure) and off-line simulation tool (bottom sub-figure).

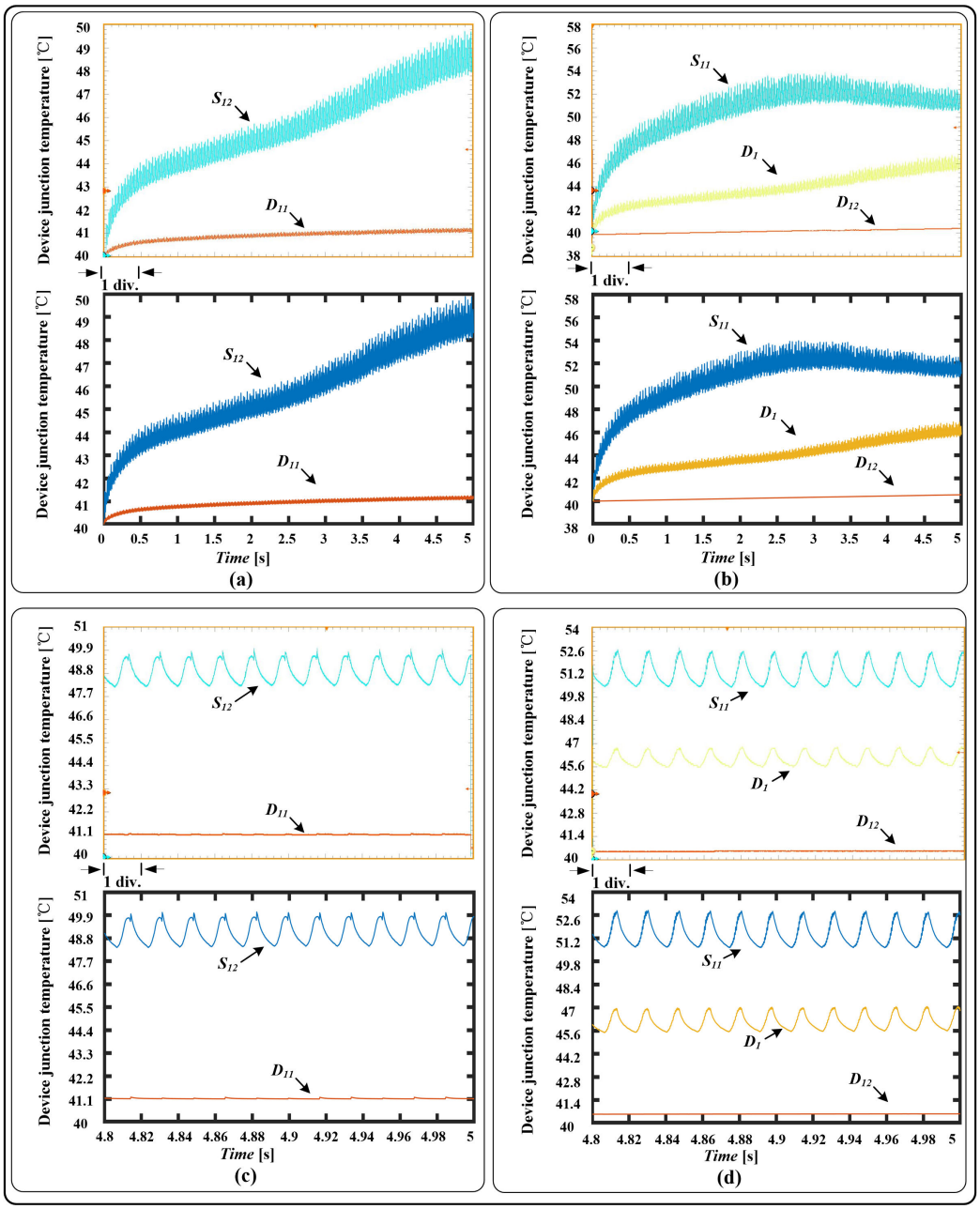

Figure 6.15: Device junction temperature from real-time emulation (top oscilloscope subfigure) and off-line simulation by SaberRD® software (bottom subfigure) for: (a) S_{12}, D_{11}, (b) S_{11}, D_1,and D_{12} (c) zoomed-in S_{12}, D_{11}, (b) S_{11}, (d) zoomed-in S_{11}, D_1,and D_{12}. Scale: (a) (b) x-axis: 0.5 s/div. (c) (d) x-axis: 0.02 s/div.

7 Conclusions and Future Work

During recent years, more advanced power electronics devices, novel sub-module and converter topologies have been developed and applied to practical transportation projects. With more MVDC systems in construction and operation, the large-scale hybrid AC/DC transportation application is also realizable in the near future. All these emerging technologies require the development of modeling, simulation, and implementation methodologies for off-line and real-time electromagnetic transient simulation. The simulation in the multi-physics domain can substantially increase the accuracy, since more realistic and detailed physical phenomena are taken into account. The advancements in IC technology and computing science can benefit the development of the real-time emulator, which has been examined in this work and requires further exploration.

In this thesis, Hammerstein, Wiener-Hammerstein configuration and hybrid neural network based, and device-level datasheet based electro-thermal power electronic models have been proposed for real-time emulation. The advanced transportation system has been simulated using hybrid modeling schemes and corresponding partition schemes in PSCAD/EMTDC® and SaberRD®. The advanced transportation system has been modeled and emulated in real-time on MPSoC-FPGA platform. The proposed methodologies in this thesis address some perspectives of the above discussion; however, substantially more work is required to be conducted in the future driven by the continuous progress on the system to be emulated and the hardware platform. The specific and detailed contributions of this thesis, corresponding applications, and the directions of future work are described in this chapter.

7.1 Contributions of This Thesis

The main contributions of this thesis are summarized as follows:

- **Hammerstein Configuration Based Device-Level Power Electronic Emulation**
  The real-time device-level dynamic electro-thermal models for diode, thyristor and IGBT are proposed and emulated based on Hammerstein configuration on a SoC-based hardware and software co-design platform for the application of EMRG system. The Hammerstein configuration modeling procedures reduces the complexity of building accurate device-level power electronic models. The modeling procedure of the static and dynamic electrical model, transient power loss model and thermal network calculation is given based on the dedicated device datasheet. The proposed models have been validated in two circuits of the EMRG system and compared with the result from the off-line device level software SaberRD®. Based on the different topology of the CC and the pulse forming network circuit inside the EMRG system, the hardware compute performance comparison, selection, and acceleration have enabled the goal of real-time execution. Future work is planned for the application of the Hammerstein based nonlinear modeling for more complex power converter systems for industrial applications.

- **Wiener-Hammerstein Configuration Based Device-Level Emulation**
  The Wiener-Hammerstein configuration based device-level electro-thermal model for po- wer electronic components was proposed and demonstrated with a three-phase to single-phase MMC-based traction power system in real-time emulation on the MPSoC platform. The MMC sub-module device-level transients are simulated in the Cortex®-A53 Core with the latency of 90ns and the three-phase to the single-phase MMC-based traction power system is simulated on the programmable logic (FPGA) with the latency of 24.2μs. Both system-level and device-level results have been validated by professional power system software PSCAD/EMTDC® and power electronic simulation software SaberRD®. The modeling procedure of Wiener-Hammer- stein configuration has added the carrier charge process feature, which is based on physical processes and calculated by first-order delay function. The timing of turn-on and turn-off carrier charging has been indicated and the equivalent circuit has been utilized for the dynamic calculation. The improved modeling of the static model and the first-order delay dynamic model gives the precise tailing current and reverse recovery waveform based on physical processes. The system-level closed-loop results show that the DC link voltage has been maintained at the dedicated voltage and it meets the requirement of the system control. The system open-loop results indicate that the R-L load is operated at the rated condition. The proposed device-level modules and real-time emulation enable a detailed evaluation of complex MVDC traction systems and controls with a low-cost and flexible hardware and

software platform.

- **SiC Device Modeling on AC Traction System**
  The technology of high-speed rail network is constantly evolving with the introduction of newer power semiconductor device, and an accurate and efficient hardware-in-the-loop simulation is necessary. Real-time device-level modeling of ultrafast power switch is demanding due to high amount of computation execution and time-sensitive condition. With proper allocation of the high-sequential clocking ARM® core and massively parallel FPGA execution resource, real-time ultra small time-step modeling of detailed power converter system can be realized for both device-level and system-level transients. This work proposed a Wiener-Hammerstein based real-time modelling method for SiC IGBT module emulation in the energy conversion system of the Beijing-Shanghai HSR application. Oscillation mechanism for SiC device has been explained in detail with three dedicated stages: carrier charge stage, static characteristic, and dynamic characteristic. The complete HSR prototype and the detailed HSR train power system have been implemented in MPSoC-FPGA hardware platform with optimized communication protocol, where the device-level transients, verified by SaberRD®, are executed at $10ns$ resolution and system-level transients, verified by PSCAD/EMTDC®, are emulated at $10\mu s$ time-step. This work can be utilized as the HIL tool to estimate the SiC material based power switch performance for the increasing demand of energy-efficient application of the future generations of HSR.

- **Adaptive Neural-Network Based Power Electronic Modeling**
  The adaptive hybrid kNN-RNN based device-level model for the IGBT module is proposed for the first time, implemented on the FPGA platform and tested on the study case of complete DC traction system. The kNN module is utilized to distinguish the transient switching state with a latency of 360 ns. With the help of kNN module, RNN module can be operated with less hidden layer neurons and training epochs. RNN module is divided into two sections: training and prediction. The training error target is set at 0.05% within 20 epochs while the prediction can be performed within 140 ns for a 100 ns time-step transient results with MSE of 2.4%. The device-level transients are emulated with the latency of 100 ns in circuit solver. The emulation results are validated by the professional simulation tools at the system-level and device-level. The proposed method provides a solution to model complex power converter topologies for practical applications such as transportation power systems, which maintaining sufficient device-level accuracy.

- **MPSoC-FPGA Real-Time Hardware Emulator**
  The various proposed modeling schemes and circuit topologies have been designed and implemented in optimized communication capable digital hardware with both

highly sequential clocking processing system and sufficient paralleled logic resources.

7.2 Applications

This section describes the applications of applying the detailed electrothermal model for off-line simulation and real-time emulation of advanced transportation application. Such applications exist in the design, testing, and operation stages of the power converter and power system, which are summarized as follows:

- In the design stage, the detailed device-level data provided by the electrothermal model can be used to evaluate the model selection of Si and SiC based IGBT modules, control algorithm, and the heatsink design from thermal perspective. In this stage, real-time emulation is not required, however, it can substantially increase the efficiency for design iterations.
- Once the control and power equipment are designed, they are often required to conduct HIL test before installing. The operator may require a comprehensive verification of the product from the manufacturer, which includes the basic functionality, security, and economy. The thermal data is useful for the verification of economic efficiency during the normal operation and the security during the fault transients. Such emulation must be conducted in real-time.
- In the operation stage, the operators need to run a large power system with sophisticated control and protection schemes. The real-time emulator can be used to train the operator for different scenarios. The detailed modeling scheme can present a high-fidelity simulation environment representing the real power system.
- The real-time emulation and the real system operate using the same control data and they respond in a very similar fashion. If the monitored electrical parameters and waveforms from the real system are very different from the simulation results, the real-time emulator can be used to detect the fault of the real system in the life cycle. It is believed that the electrothermal and other physical phenomena must be considered to achieve the high accuracy of the real-time emulation.

7.3 Directions for Future Work

The following topics are proposed for future work:

- The Wiener-Hammerstein device-level power electronic modeling schemes can be developed for the next generation wide bandgap switching devices, which can also be applied for various components, such as converters, and electrical machines.

- The advancements in IC technology and computing science can benefit the development of the real-time emulator. Faster than real-time application of testing different configuration of circuit topology and mitigation of the oscillation during the switching is possible in the very near future.
- More FPGA and MPSoC boards can be interconnected to provide significantly more logic resources and higher computing performance. More complex hybrid AC/DC transportation topology and detailed real-time capable model can be implemented to test their control and protection strategies.
- The host computer system and graphical processing unit for general-purpose computing can be integrated with the FPGA-MPSoC platform to form a more powerful computing system, which provides more flexibility and computing capability for various tasks.
- With the accurately modeled advanced transportation system on PSCAD/EMTDC® and the real-time capable device-level emulator, more tests and researches can be conducted to study the interactive phenomena of the converter stress and transportation system. Novel supervisory control and protection strategy can be verified with the emulation system.

Bibliography

[1] H. Jin, "Behavior-mode simulation of power electronic circuits," in *IEEE Trans. Power Electron.,* vol. 12, no. 3, pp. 443-452, May 1997.

[2] L. Salazar and G. Joos, "PSPICE simulation of three-phase inverters by means of switching functions," *IEEE Trans. Power Electron.,* vol. 9, no. 1, pp. 35-42, Jan. 1994.

[3] R. D. Middlebrook and S. Cuk, "A general unified approach to modeling switching-converter power stages," *Power Electronic Specialists Conference,* 1976 IEEE, Cleveland, OH, 1976, pp. 18-34.

[4] A. R. Hefner, and D. L. Blackburn, "An analytical model for the steady-state and transient characteristics of the power insulated-gate bipolar transistor," *Solid-State Electron.,* 31.10 (1988): 1513-1532.

[5] A. R. Hefner, "A dynamic electro-thermal model for the IGBT," *IEEE Trans. Ind. Appl.,* vol. 30, no. 2, pp. 394-405, Mar./Apr. 1994.

[6] P. R. Palmer, E. Santi, J. L. Hudgins, X. Kang, J. C. Joyce and P. Y. Eng, "Circuit simulator models for the diode and IGBT with full temperature dependent features," *IEEE Trans. Power Electron.,* vol. 18, no. 5, pp. 1220-1229, Sept. 2003.

[7] M. Orabi and A. Shawky, "Proposed switching losses model for integrated point-of-load synchronous buck Converters," *IEEE Trans. Power Electron.,* vol. 30, no. 9, pp. 5136-5150, Sept. 2015.

[8] S. Bellone, F. G. D. Corte, L. D. Benedetto and G. D. Licciardo, "An analytical model of the switching behavior of 4h-SiC p^{bm+}-n-n^{bm+} diodes from arbitrary injection conditions," *IEEE Trans. Power Electron.,* vol. 27, no. 3, pp. 1641-1652, Mar. 2012.

[9] A. R. Hefner, "Analytical modeling of device-circuit interactions for the power insulated gate bipolar transistor (IGBT)," *IEEE Trans. Ind. Appl.,* vol. 26, no. 6, pp. 995-1005, Nov./Dec. 1990.

[10] J. T. Hsu and K. D. T. Ngo, "Behavioral modeling of the IGBT using the Hammerstein configuration," *IEEE Trans. Power Electron.,* vol. 11, no. 6, pp. 746-754, Nov. 1996.

[11] N. Lin and V. Dinavahi, "Detailed device-level electro-thermal modeling of proactive hybrid HVDC breaker for real-time hardware-in-the-loop simulation of HVDC grids," *IEEE Trans. Power Electron.,* vol. PP, no. 99, pp. 1-1

[12] E. V. Sinkevich, "Validation of the Hammerstein-type behavioral model for the diode envelope demodulator," *2007 7th International Symposium on Electromagnetic Compatibility and Electromagnetic Ecology, Saint-Petersburg,* 2007, pp. 162-165.

[13] N. Femia, M. Migliaro, C. Pastore and D. Toledo, "In-system IGBT power loss behavioral modeling," *2016 13th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Lisbon,* 2016, pp. 1-4.

[14] W. Kang, H. Ahn and M. A. E. Nokali, "A parameter extraction algorithm for an IGBT behavioral model," *IEEE Trans. Power Electron.,* vol. 19, no. 6, pp. 1365-1371, Nov. 2004.

[15] J. L. Tichenor, S. D. Sudhoff and J. L. Drewniak, "Behavioral IGBT modeling for predicting high frequency effects in motor drives," *IEEE Trans. Power Electron.,* vol. 15, no. 2, pp. 354-360, Mar. 2000.

[16] A. Myaing and V. Dinavahi, "FPGA-based real-time emulation of power electronic systems with detailed representation of device characteristics," *IEEE Trans. Ind. Electron.,* vol. 58, no. 1, pp. 358-368, Jan. 2011.

[17] R. Chibante, A. AraÚjo and A. Carvalho, "Finite-element modeling and optimization-based parameter extraction algorithm for NPT-IGBTs," *IEEE Trans. Power Electron.,* vol. 24, no. 5, pp. 1417-1427, May 2009.

[18] A. S. Bahman, K. Ma, P. Ghimire, F. Iannuzzo and F. Blaabjerg, "A 3-d-lumped thermal network model for long-term load profiles analysis in high-power IGBT modules," *IEEE Trans. Emerg. Sel. Topics Power Electron.,* vol. 4, no. 3, pp. 1050-1063, Sept. 2016

[19] K. Sheng, B. W. Williams and S. J. Finney, "A review of IGBT models," *IEEE Trans. Power Electron.,* vol. 15, no. 6, pp. 1250-1266, Nov. 2000.

[20] K. Shirakawa, M. Shimiz, N. Okubo and Y. Daido, "A large-signal characterization of an HEMT using a multilayered neural network," *IEEE Trans. Microwave Theory Tech.,* vol. 45, no. 9, pp. 1630-1633, Sep. 1997.

[21] M. Isaksson, D. Wisell and D. Ronnow, "Wide-band dynamic modeling of power amplifiers using radial-basis function neural networks," *IEEE Trans. Microwave Theory Tech.,* vol. 53, no. 11, pp. 3422-3428, Nov. 2005.

[22] T. Liu, S. Boumaiza and F. M. Ghannouchi, "Dynamic behavioral modeling of 3G power amplifiers using real-valued time-delay neural networks," *IEEE Trans. Microwave Theory Tech.,* vol. 52, no. 3, pp. 1025-1033, Mar. 2004.

[23] Y. Fang, M. C. E. Yagoub, F. Wang and Q. Zhang, "A new macromodeling approach for nonlinear microwave circuits based on recurrent neural networks," *IEEE Trans. Microwave Theory Tech.,* vol. 48, no. 12, pp. 2335-2344, Dec. 2000.

[24] J. C. Dries, "SiC research and development at united silicon carbide inc. looking beyond 650–1200 V diodes and transistors," *IEEE Power Electron. Mag.,* vol. 2, no. 1, pp. 12-15, Mar. 2015.

[25] J. V. Candy "Model-based processing: an applied subspace identification approach," *Wiley,* 2019.

[26] S. A. Billings, "Nonlinear system identification : NARMAX methods in the time, frequency, and spatio-temporal domains," *Wiley,* 2013.

[27] K. Shirriff, "The surprising story of the first microprocessors," *IEEE Spectrum,* vol. 53, no. 9, pp. 48-54, Sep. 2016.

[28] P. Lapsley, J. Bier, A. Shoham, and E. A. Lee, "DSP processor fundamentals: architectures and features," *Wiley,* 1997.

[29] Y. Bai, "Practical microcontroller engineering with ARM technology," *IEEE,* 2016.

[30] E. Lipiansky, "Electrical, electronics, and digital hardware essentials for scientists and engineers," *IEEE,* 2013.

[31] J. Cheng, M. Grossman, T. McKercher, "Professional CUDA C programming," *Wrox Press Ltd.,* 2014.

[32] P. O. Norman, et al. "In-datacenter performance analysis of a tensor processing unit," *Comput. Archit. News,* May 2017.

[33] P. Horowitz, and W. Hill, "The art of electronics," *Cambridge University Press,* 2015.

[34] A. S. Deese and C. O. Nwankpa, "Design and testing of custom FPAA hardware with improved scalability for emulation of smart grids," *IEEE Trans. Smart Grid,* vol. 5, no. 3, pp. 1369-1378, May 2014.

[35] Y. Liang, H. K. Liu, "Optical matrix-matrix multiplication method demonstrated by the use of a multifocus hololens," *Optics letters,* vol. 9, no. 8, Mar. 1984.

[36] K. Wu, C. Soci, P. P. Shum, and N. I. Zheludev, "Computing matrix inversion with optical networks," *Optics Express,* vol. 22, no. 1, pp. 295-304, Jan. 2014.

[37] K. Barr, "Asic design in the silicon sandbox: a complete guide to building mixed signal integrated circuits," *McGraw-Hill,* 2006.

[38] W. Wolf, A. A. Jerraya and G. Martin, "Multiprocessor system-on-chip (MPSoC) technology," *IEEE Trans. CAD,* vol. 27, no. 10, pp. 1701-1713, Oct. 2008.

[39] P. W. Shor, "Algorithms for quantum computation: discrete logarithms and factoring," *Proceedings 35th Annual Symposium on Foundations of Computer Science,* Santa Fe, NM, USA, pp. 124-134, 1994.

[40] *Zynq UltraScale+ MPSoC Technical Reference Manual.* [Online]. Available: https://www.xilinx.com/support/documentation/user guides/ug1085-zynq-ultrascale-trm.pdf

[41] M. D. Omar Faruque et al., "Real-time simulation technologies for power systems design, testing, and analysis" *IEEE Power Energy Technol. Syst. J.,* vol. 2, no. 2, pp. 63-73, June 2015.

[42] M. O. Omar Faruque and V. Dinavahi, "Hardware-in-the-loop simulation of power electronic systems using adaptive discretization," *IEEE Trans. Ind. Electron.,* vol. 57, no. 4, pp. 1146-1158, Apr. 2010.

[43] Z. Shen and V. Dinavahi, "Dynamic variable time-stepping schemes for real-time FPGA-based nonlinear electromagnetic transient emulation," *IEEE Trans. Ind. Electron.,* vol. 64, no. 5, pp. 4006-4016, May 2017.

[44] N. Lin and V. Dinavahi, "Behavioral device-level modeling of modular multi-level converters in real-time for variable speed drive applications," *IEEE J. Emerging. Sel. Topics Power Electron.,* vol. PP, no.99, pp. 1-15, 2017.

[45] Z. Shen and V. Dinavahi, "Real-time device-level transient electrothermal model for modular multilevel converter on FPGA," *IEEE Trans. Power Electron.,* vol. 31, no. 9, pp. 6155-6168, Sept. 2016.

[46] N. R. Tavana and V. Dinavahi, "Real-time nonlinear magnetic equivalent circuit model of induction machine on FPGA for hardware-in-the-loop simulation," *IEEE Trans. Energy Convers.,* vol. 31, no. 2, pp. 520-530, June 2016.

[47] J. Liu and V. Dinavahi, "Detailed magnetic equivalent circuit based real-time nonlinear power transformer model on FPGA for electromagnetic transient studies," *IEEE Trans. Ind. Electron.,* vol. 63, no. 2, pp. 1191-1202, Feb. 2016.

[48] N. R. Tavana and V. Dinavahi, "A general framework for FPGA-based real-time emulation of electrical machines for HIL applications," *IEEE Trans. Ind. Electron.,* vol. 62, no. 4, pp. 2041-2053, Apr. 2015.

[49] N. R. Tavana and V. Dinavahi, "Real-time FPGA-based analytical space harmonic model of permanent magnet machines for hardware-in-the-loop simulation," *IEEE Transactions on Magnetics,* vol. 51, no. 8, pp. 1-9, Aug. 2015.

[50] J. Liu and V. Dinavahi, "A real-time nonlinear hysteretic power transformer transient model on FPGA," *IEEE Trans. Ind. Electron.,* vol. 61, no. 7, pp. 3587-3597, July 2014.

[51] Y. Chen and V. Dinavahi, "Hardware emulation building blocks for real-time simulation of large-scale power grids," *IEEE Trans. Ind. Inf.,* vol. 10, no. 1, pp. 373-381, Feb. 2014.

[52] W. Wang, Z. Shen and V. Dinavahi, "Physics-based device-level power electronic circuit hardware emulation on FPGA," *IEEE Trans. Ind. Inf.,* vol. 10, no. 4, pp. 2166-2179, Nov. 2014.

[53] K. Vipin and S. A. Fahmy, "ZyCAP: efficient partial reconfiguration management on the Xilinx Zynq," *IEEE Embedded Syst. Lett.,* vol. 6, no. 3, pp. 41-44, Sept. 2014.

[54] M. A. Akbar et al., "An empirical study for pca- and lda-based feature reduction for gas identification," *IEEE Sensors J.,* vol. 16, no. 14, pp. 5734-5746, July 2016.

[55] G. Zhong, S. Niar, A. Prakash and T. Mitra, "Design of multiple-target tracking system on heterogeneous system-on-chip devices," *IEEE Trans. Veh. Technol.,* vol. 65, no. 6, pp. 4802-4812, June 2016.

[56] P. Govindan, B. Wang, P. Ravi and J. Saniie, "Hardware and software architectures for computationally efficient three-dimensional ultrasonic data compression," *IET Circuits Devices Syst.,* vol. 10, no. 1, pp. 54-61, 1 2016.

[57] M. Abeydeera, M. Karunaratne, G. Karunaratne, K. De Silva and A. Pasqual, "4K real-time HEVC decoder on an FPGA," *IEEE Trans. Circuits Syst. Video Technol.,* vol. 26, no. 1, pp. 236-249, Jan. 2016.

[58] Q. Liu, Z. Xu and Y. Yuan, "High throughput and secure advanced encryption standard on field programmable gate array with fine pipelining and enhanced key expansion," *IET Comput. Digital Tech.,* vol. 9, no. 3, pp. 175-184, 5 2015.

[59] H. Tabkhi, M. Sabbagh and G. Schirner, "Power-efficient real-time solution for adaptive vision algorithms," *IET Comput. Digital Tech.,* vol. 9, no. 1, pp. 16-26, 1 2015.

[60] K. Narendra and P. Gallman, "An iterative method for the identification of nonlinear systems using a Hammerstein model," *IEEE Trans. Autom. Control,* vol. 11, no. 3, pp. 546-550, July 1966.

[61] T. L. Chia, P. C. Chow and H. J. Chizeck, "Recursive parameter identification of constrained systems: an application to electrically stimulated muscle," *IEEE Trans. Biomed. Eng.,* vol. 38, no. 5, pp. 429-442, May 1991.

[62] F. Alonge, F. D'Ippolito and T. Cangemi, "Identification and robust control of dc/dc converter Hammerstein model," *IEEE Trans. Power Electron.,* vol. 23, no. 6, pp. 2990-3003, Nov. 2008.

[63] F. Alonge, F. D'Ippolito, F. M. Raimondi and S. Tumminaro, "Nonlinear modeling of dc/dc converters using the Hammerstein's approach," *IEEE Trans. Power Electron.,* vol. 22, no. 4, pp. 1210-1221, July 2007.

[64] F. Alonge, R. Rabbeni, M. Pucci and G. Vitale, "Identification and robust control of a quadratic dc/dc boost converter by Hammerstein model," *IEEE Trans. Ind. Appl.,* vol. 51, no. 5, pp. 3975-3985, Sept.-Oct. 2015.

[65] F. Mkadem and S. Boumaiza, "Extended Hammerstein behavioral model using artificial neural networks," *IEEE Trans. Microw. Theory Tech.,* vol. 57, no. 4, pp. 745-751, Apr. 2009.

[66] X. Ren and X. Lv, "Identification of extended Hammerstein systems using dynamic self-optimizing neural networks," *IEEE Trans. Neural Netw.,* vol. 23, no. 6, pp. 2990-3003, Nov. 2008.

[67] J. Pan and C. H. Cheng, "Wiener–Hammerstein model based electrical equalizer for optical communication systems," *J. Lightwave Technol.,* vol. 29, no. 16, pp. 2454-2459, Aug. 2011.

[68] F. Taringou, O. Hammi, B. Srinivasan, R. Malhame and F. M. Ghannouchi, "Behaviour modelling of wideband RF transmitters using Hammerstein-Wiener models," *IET Circuits Devices Syst.,* vol. 4, no. 4, pp. 282-290, July 2010.

[69] D. Zmarzly and P. Fracz, "Nonlinear modeling of streaming electrification measured in swinging cylinder system," *IEEE Trans. Dielectr. Electr. Insul.,* vol. 23, no. 1, pp. 174-182, Feb. 2016.

[70] H. W. Dommel, "Digital computer solution of electromagnetic transients in single- and multiphase networks," *IEEE Trans. App. Syst.,* vol. PAS-88, no. 4, pp. 388-399, Apr. 1969.

[71] S. Y. R. Hui and K. K. Fung, "Fast decoupled simulation of large power electronic systems using new two-port companion link models," *IEEE Trans. Power Electron.,* vol. 12, no. 3, pp. 462-473, May 1997.

[72] J. Dong et al., "The 100-kJ modular pulsed power units for railgun," *IEEE Trans. Plasma Sci.,* vol. 39, no. 1, pp. 275-278, Jan. 2011.

[73] P. Lehmann, H. Peter, F. Jamet and V. Wegner, "Some remarks concerning the optimization of a railgun system," *IEEE Trans. Magn.,* vol. 31, no. 1, pp. 546-551, Jan. 1995.

[74] T. Coradeschi et al., "52 megajoule electric gun test facility," *IEEE Trans. Magn.,* vol. 29, no. 1, pp. 923-928, Jan. 1993.

[75] A. N. Smith, B. T. McGlasson and J. S. Bernardes, "Heat generation during the firing of a capacitor-based railgun system," *IEEE Trans. Magn.,* vol. 43, no. 1, pp. 190-193, Jan. 2007.

[76] "SaberRD® datasheet: desktop design of power systems and multi-domain physical systems." [Online].

[77] "Technical information, ABB® IGBT modules 5SNA 1500E330305." [Online].

[78] "Technical information, ABB® phase control thyristor 5STP 52U5200." [Online].

[79] "Technical information, 3300V HiPak2 modules with enhanced trench (TSPT+) IGBTs and field charge extraction diodes rated up to 1800A." [Online].

[80] "Technical information, hybrid marine electric propulsion system with super-capacitors energy storage." [Online].

[81] B. J. Wojtas, "Developments on British railways traction and rolling stock," *Power Eng. J,* vol. 3, no. 2, pp. 95-102, Mar. 1989.

[82] D. Ronanki, S. A. Singh and S. S. Williamson, "Comprehensive topological overview of rolling stock architectures and recent trends in electric railway traction systems," *IEEE Trans. Transport. Electrific.,* vol. 3, no. 3, pp. 724-738, Sep. 2017.

[83] M. Winkelnkemper, A. Korn and P. Steimer, "A modular direct converter for transformerless rail interties," *2010 IEEE International Symposium on Industrial Electronics,* Bari, pp. 562-567.

[84] S. Kouro et al., "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.,* vol. 57, no. 8, pp. 2553-2580, Aug. 2010.

[85] A. G. Exposito, J. M. Mauricio and J. M. M. Ortega, "VSC-based MVDC railway electrification system," *IEEE Trans. Power Delivery,* vol. 29, no. 1, pp. 422-431, Feb. 2014.

[86] D. Ronanki and S. S. Williamson, "Evolution of power converter topologies and technical considerations of power electronic transformer-based rolling stock architectures," *IEEE Trans. Transport. Electrific.,* vol. 4, no. 1, pp. 211-219, Mar. 2018.

[87] D. Ronanki and S. S. Williamson, "Modular multilevel converters for transportation electrification: challenges and opportunities," *IEEE Trans. Transport. Electrific.,* vol. PP, no. 99, pp. 1-1, Jan. 2018.

[88] G. Zhang, Z. Liu, S. Yao, Y. Liao and C. Xiang, "Suppression of low-frequency oscillation in traction network of high-speed railway based on auto-disturbance rejection control," *IEEE Trans. Transport. Electrific.,* vol. 2, no. 2, pp. 244-255, Jun. 2016.

[89] W. Song, S. Jiao, Y. W. Li, J. Wang and J. Huang, "High-frequency harmonic resonance suppression in high-speed railway through single-phase traction converter with LCL filter," *IEEE Trans. Transport. Electrific.,* vol. 2, no. 3, pp. 347-356, Sep. 2016.

[90] G. Zhang, Z. Liu, S. Yao, Y. Liao and C. Xiang, "Energy storage on board of railway vehicles," *2005 European Conference on Power Electronics and Applications,* Dresden, pp. 1-10.

[91] S. M. Lukic, J. Cao, R. C. Bansal, F. Rodriguez and A. Emadi, "Energy storage systems for automotive applications," *IEEE Trans. Ind. Electron.,* vol. 55, no. 6, pp. 2258-2267, Jun. 2008.

[92] D. Iannuzzi and P. Tricoli, "Speed-based state-of-charge tracking control for metro trains with onboard supercapacitors," *IEEE Trans. Power Electron.,* vol. 27, no. 4, pp. 2129-2140, Apr. 2012.

[93] M. M. Steurer, K. Schoder, O. Faruque, D. Soto, M. Bosworth, M. Sloderbeck, F. Bogdan, J. Hauer, M. Winkelnkemper, L. Schwager, P. Blaszczyk, "Multifunctional megawatt-scale medium voltage DC test bed based on modular multilevel converter technology," *IEEE Trans. Transport. Electrific.,* vol. 2, no. 4, pp. 597-606, Dec. 2016.

[94] K. Huang, Z. Liu, F. Zhu, Y. Cheng, H. Wang, Z. Zheng, Y. Wang, "A systematic EMTP impedance modeling scheme aimed at train body in high-speed railway," *IEEE Trans. Transport. Electrific,* vol. 3, no. 1, pp. 272-283, Mar. 2017.

[95] N. R. Tavana and V. Dinavahi, "Real-time nonlinear magnetic equivalent circuit model of induction machine on FPGA for hardware-in-the-loop simulation," *IEEE Trans. Energy Convers.,* vol. 31, no. 2, pp. 520-530, Jun. 2016.

[96] G. Zhong, S. Niar, A. Prakash and T. Mitra, "Design of multiple-target tracking system on heterogeneous system-on-chip devices," *IEEE Trans. Veh. Technol.,* vol. 65, no. 6, pp. 4802-4812, Jun. 2016.

[97] M. Abeydeera, M. Karunaratne, G. Karunaratne, K. De Silva and A. Pasqual, "4K real-time HEVC decoder on an FPGA," *IEEE Trans. Circuits Syst. Video Technol.,* vol. 26, no. 1, pp. 236-249, Jan. 2016.

[98] J. Liu and V. Dinavahi, "A real-time nonlinear hysteretic power transformer transient model on FPGA," *IEEE Trans. Ind. Electron.,* vol. 61, no. 7, pp. 3587-3597, Jul. 2014.

[99] J. Carr, D. Das, J. Li, J. Pan, S. Ebner and O. Apeldoorn, "Modular multilevel converter for direct MVDC connection of offshore wind farms," *2015 IEEE Energy Conversion Congress and Exposition (ECCE),* Montreal, QC, pp. 976-982.

[100] J. Hu, P. Joebges and R. W. De Doncker, "Maximum power point tracking control of a high power dc-dc converter for PV integration in MVDC distribution grids," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC),* Tampa, FL, pp. 1259-1266.

[101] R. Mo, R. Li and H. Li, "Isolated modular multilevel (IMM) DC/DC converter with energy storage and active filter function for shipboard MVDC system applications," *2015 IEEE Electric Ship Technologies Symposium (ESTS),* Alexandria, VA, pp. 113-117.

[102] T. Liang and V. Dinavahi, "Real-Time System-on-Chip Emulation of Electrothermal Models for Power Electronic Devices via Hammerstein Configuration," *IEEE Trans. Emerg. Sel. Topics Power Electron.,* vol. 6, no. 1, pp. 203-218, Mar. 2018

[103] H. Liu, K. Ma and F. Blaabjerg, "Device loading and efficiency of modular multilevel converter under various modulation strategies," *IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG),* Vancouver, BC, 2016, pp. 1-7.

[104] T. Uzuka, "Faster than a speeding bullet: an overview of Japanese high-speed rail technology and electrification," *IEEE Electrific. Mag.,* vol. 1, no. 1, pp. 11-20, Sept. 2013.

[105] B. Xie et al., "A compensation system for cophase high-speed electric railways by reactive power generation of SHC&SAC," *IEEE Trans. Ind. Electron.,* vol. 65, no. 4, pp. 2956-2966, Apr. 2018.

[106] Z. Liu, G. Zhang and Y. Liao, "Stability research of high-speed railway EMUs and traction network cascade system considering impedance matching," *IEEE Trans. Ind. Appl.,* vol. 52, no. 5, pp. 4315-4326, Sept.-Oct. 2016.

[107] F. Ma, A. Luo, X. Xu, H. Xiao, C. Wu and W. Wang, "A simplified power conditioner based on half-bridge converter for high-speed railway system," *IEEE Trans. Ind. Electron.,* vol. 60, no. 2, pp. 728-738, Feb. 2013.

[108] F. Ma, Z. He, Q. Xu, A. Luo, L. Zhou and M. Li, "Multilevel power conditioner and its model predictive control for railway traction systems," *IEEE Trans. Ind. Electron.,* vol. 63, no. 11, pp. 7275-7285, Nov. 2016.

[109] J. H. Kim et al., "Development of 1-MW inductive power transfer system for a high-speed train," *IEEE Trans. Ind. Electron.,* vol. 62, no. 10, pp. 6242-6250, Oct. 2015.

[110] A. Facchinetti and M. Mauri, "Hardware-in-the-loop overhead line emulator for active pantograph testing," *IEEE Trans. Ind. Electron.,* vol. 56, no. 10, pp. 4071-4078, Oct. 2009.

[111] A. Siemens, "High-speed electric railway experiments on the Marienfelde-Zossen line," *J. Inst. Electric. Eng.,* vol. 33, no. 168, pp. 894-923, Aug. 1904.

[112] X. She, A. Q. Huang, Ó. Lucía and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.,* vol. 64, no. 10, pp. 8193-8205, Oct. 2017.

[113] K. Narendra and P. Gallman, "An iterative method for the identification of nonlinear systems using a Hammerstein model," *IEEE Trans. Autom. Control,* vol. 11, no. 3, pp. 546-550, July 1966.

[114] F. Chang and R. Luus, "A noniterative method for identification using Hammerstein model," *IEEE Trans. Autom. Control,* vol. 16, no. 5, pp. 464-468, Oct 1971.

[115] E. Bai and M. Fu, "A blind approach to Hammerstein model identification," *IEEE Trans. Signal Process.,* vol. 50, no. 7, pp. 1610-1619, July 2002.

[116] Y. Bao, L. Y. Wang, C. Wang and Y. Wang, "Hammerstein models and real-time system identification of load dynamics for voltage management," *IEEE Access,* vol. 6, pp. 34598-34607, 2018.

[117] J. T. Hsu and K. D. T. Ngo, "A Hammerstein-based dynamic model for hysteresis phenomenon," *IEEE Trans. Power Electron.,* vol. 12, no. 3, pp. 406-413, May 1997.

[118] X. Gao, X. Ren, C. Zhu and C. Zhang, "Identification and control for Hammerstein systems with hysteresis non-linearity," in *IET Control Theory Appl.,* vol. 9, no. 13, pp. 1935-1947, Aug. 2015.

[119] B. D. S. Pês, E. Oroski, J. G. Guimaraes and M. J. C. Bonfim, "A Hammerstein–Wiener model for single-electron transistors," *IEEE Trans. Electron Devices,* vol. 66, no. 2, pp. 1092-1099, Feb. 2019.

[120] A. Balestrino, A. Landi, M. Ould-Zmirli and L. Sani, "Automatic nonlinear autotuning method for Hammerstein modeling of electrical drives," *IEEE Trans. Ind. Electron.,* vol. 48, no. 3, pp. 645-655, June 2001.

[121] B. Li, S. Zhou, D. Xu, S. J. Finney and B. W. Williams, "A hybrid modular multilevel converter for medium-voltage variable-speed motor drives," *IEEE Trans. Power Electron.,* vol. 32, no. 6, pp. 4619-4630, June 2017.

[122] S. Du, B. Wu and N. Zargari, "A control strategy for star-channel modular multilevel converter in variable-speed motor drive application," *IEEE Trans. Ind. Electron.,* vol. 66, no. 7, pp. 5094-5101, July 2019.

[123] M. Z. Youssef, K. Woronowicz, K. Aditya, N. A. Azeez and S. S. Williamson, "Design and development of an efficient multilevel DC/AC traction inverter for railway transportation electrification" *IEEE Trans. Power Electron.,* vol. 31, no. 4, pp. 3036-3042, Apr. 2016.

[124] A. Choudhury, P. Pillay and S. S. Williamson, "Comparative analysis between two-level and three-level DC/AC electric vehicle traction inverters using a novel DC-link voltage balancing algorithm," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 2, no. 3, pp. 529-540, Sep. 2014.

[125] A. Verdicchio, P. Ladoux, H. Caron and C. Courtois, "New medium-voltage DC railway electrification system," *IEEE Trans. Transport. Electrific.,* vol. 4, no. 2, pp. 591-604, June 2018.

[126] E. Pons, R. Tommasini and P. Colella, "Fault current detection and dangerous voltages in DC urban rail traction systems," *IEEE Trans. Ind. Appl.,* vol. 53, no. 4, pp. 4109-4115, July-Aug. 2017.

[127] W. S. Mcculloch, "The brain computing machine," *Electr. Eng.,* vol. 68, no. 6, pp. 492-497, Jun. 1949.

[128] M. H. Hassoun, "Fundamentals of artificial neural networks," MIT Press, Cambridge, MA, 1995.

[129] S. O. Haykin, "Neural networks and learning machines," Prentice Hall/Pearson, New York, 2009.

[130] Z. Huang and V. Dinavahi, "A fast and stable method for modeling generalized nonlinearities in power electronic circuit simulation and its real-time implementation," *IEEE Trans. Power Electron.,* doi: 10.1109/TPEL.2018.2851570

A

Parameters for Case Studies

A.1 Parameters in Chapter 5

Table A.1: Parameters of Hybrid SiC IGBT module

L_{E1},L_{E2}	10 nH
L_{C1},L_{C2}	20 nH
L_S	100 nH
$C_{oes(V_R)}$	1.17 nF
R_{eq}	1.5 Ω
$Q_c(1/2module)$	2.5 μC
I_{rr}	100 A

A.2 Parameters in Chapter 6

Table A.2: Parameters of traction power system

DC bus voltage	3 kV
DC bus capacitor	10 mF
Carrier frequency	2000 Hz
Z_C	0.119+j0.752 Ω/km
Z_F	0.204+j0.885 Ω/km
Z_R	0.162+j0.671 Ω/km
Z_{CR}	0.057+j0.388 Ω/km
Z_{CF}	0.057+j0.395 Ω/km
Z_{RF}	0.057+j0.341 Ω/km
C_{CF}	0.000504 $\mu F/km$
C_{CR}	0.002057 $\mu F/km$
C_{FR}	0.003262 $\mu F/km$
$K_{P(PR)}$	0.7
$K_{R(PR)}$	0.4

Table A.3: Parameters of DC traction inverter

DC bus voltage	3 kV
DC bus capacitor	10 mF
Carrier frequency	1800 Hz

Table A.4: Parameters of PMSM

Nominal apparent power	3.65 MVA
Nominal voltage	4 kV
Rated frequency	60 Hz
Stator resistance (r_s)	0.0482 Ω
d-axis inductance (L_d)	8.01 mH
q-axis inductance (L_q)	8.01 mH
Magnet flux linkage (F_{rm})	8.66 $V \cdot s$
Rotational inertia (J)	51.36 $kg \cdot m^2$
Damping coefficient (B)	0.0005 $Nm/rad/s$
Load torque (T_{L})	9682$N \cdot m$