Digitally Enhanced SNR Optimized CMOS Optical Receiver

by

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A thesis submitted in partial fulfillment of the requirements for the degree of

Master of Science

in

Integrated Circuit and Systems

Department of Electrical and Computer Engineering

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Abstract

The continuing exponential increase in functionalities of integrated circuits demands high data rate intra-chip and inter-chip communication. However, high speed communications inside silicon chips are often bottlenecked by capacitive drain of the channels. Therefore, as the functionalities of integrated circuits get increasingly sophisticated, achieving the required high bandwidth operations becomes increasingly challenging. Photonic integrated circuits (PIC) are considered as a potential solution, where electronic signals are converted into optical signals and transmitted through waveguide structures. The optical signals are converted back to the electronic domain by photodiodes at the receiving end and then processed by optical receivers. In order to maintain the high data rate operation of the system, the optical receivers must be optimized to perform at high bandwidth. This thesis focuses on enhancing the SNR performance of optical receivers.

The first work of the thesis describes a high gain-bandwidth transimpedance amplifier (TIA) with optimized SNR. The design uses a common gate TIA as the first stage and then the gain and bandwidth is enhanced in the subsequent stages using various techniques. The design is implemented in ST 28-nm FDSOI CMOS technology; it achieves a transimpedance gain of 55 dBΩ and 3dB bandwidth of 32 GHz. The second work of the thesis focuses on designing an energy efficient inter symbol interference (ISI) equalizer. It proposes an Analog to Sequence Converter (ASC) based Maximum A Posteriori (MAP) decoding equalizer. The concept was implemented in 0.13 μm CMOS technology. The implemented prototype is capable of compensating 35+ dB loss at 10 Gb/s data rate with better than 10 pJ/bit energy efficiency.

Acknowledgements

First and foremost, I would like to convey my sincerest gratitude toward Dr. Masum Hossain for his extraordinary guidance, support, and patience throughout my degree. The materials covered in his undergraduate “Integrated Circuits Design” course is actually what grabbed my interest in this field. Subsequently I had the pleasure of expanding my knowledge of this field while working under his guidance.

I would also like to thank Dr. Mani Vaidyanathan, Dr. Vien Van, Dr. Mrinal Mandal and Dr. Xihua Wang for taking the time out of their busy schedules to serve in my final exam committee.

I would like to extend my appreciation towards Aurangozeb and Shovon Dey for their constant support and advice throughout my degree. I would also like to Thank Carson, Alberto, Behdad and Shakib for making the lab an enjoyable work environment.

Lastly, I would like to thank my parents for their endless support and guidance.

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List of Abbreviations

ACS	Add-Compare-Select
ADC	Analog-to-Digital Converter
ASC	Analog to Sequence Converter
BER	Bit-Error-rate
BM	Branch Metrics
CG	Common Gate
CS	Common Source
DSP	Digital Signal Processor
FFE	Feedforward Equalization
FoM	Figure of Merit
HPF	High Pass Filter
ISI	Inter Symbol Interference
MLSD	Maximum Likelihood Sequence Detector
MAP	Maximum A Posteriori
PD	Photodiode
PIC	Photonic Integrated Circuit
RGC	Regulated Cascode
S-FB	Shunt Feedback
SBR	Single Bit Response
SNR	Signal-to-Noise Ratio
TIA	Transimpedance Amplifier
VGA	Variable Gain Amplifier

Chapter 1

Introduction

1.1 Background

Silicon is the material of choice for the semiconductor industry in today's technology. The matured silicon processing technology is likely to dominate the semiconductor industry for the foreseeable future. Continued demand on increased speed and functionality in silicon integrated circuits has been driving the International Technology Roadmap for Semiconductors (ITRS) roadmap [1] towards ambitious and challenging targets in terms of device dimensions and circuit density. On-chip data communication rate has reached impressive peaks with gate dimensions in sub 10 nm domain. However, higher speed electronic operations inside a silicon chip are bottlenecked by capacitive drain during intra-chip data communications. Achieving high bandwidth operations at nominal chip dimensions is a design challenge for highspeed high-functionality circuits.

Silicon based photonics is considered as a potential solution for achieving high bandwidth intra-chip operations [2] [3]. In a photonic integrated circuit (PIC), a laser-modulator module is used to convert electronic signal into optical signal for on-chip transmission through waveguide structures and thereby eliminating the capacitive drain effects on electrical signals [4]-[6]. The optical signal is received by a P-I-N photodiode (PD) circuit for its conversion to electronic signal to be applicable on device level logic. Photonic applications can also be used for inter-chip communications involving fiber-optical coupling between individual chips. Apart from the emerging trends of inter and intra chip optical applications, detection of optical signal at high

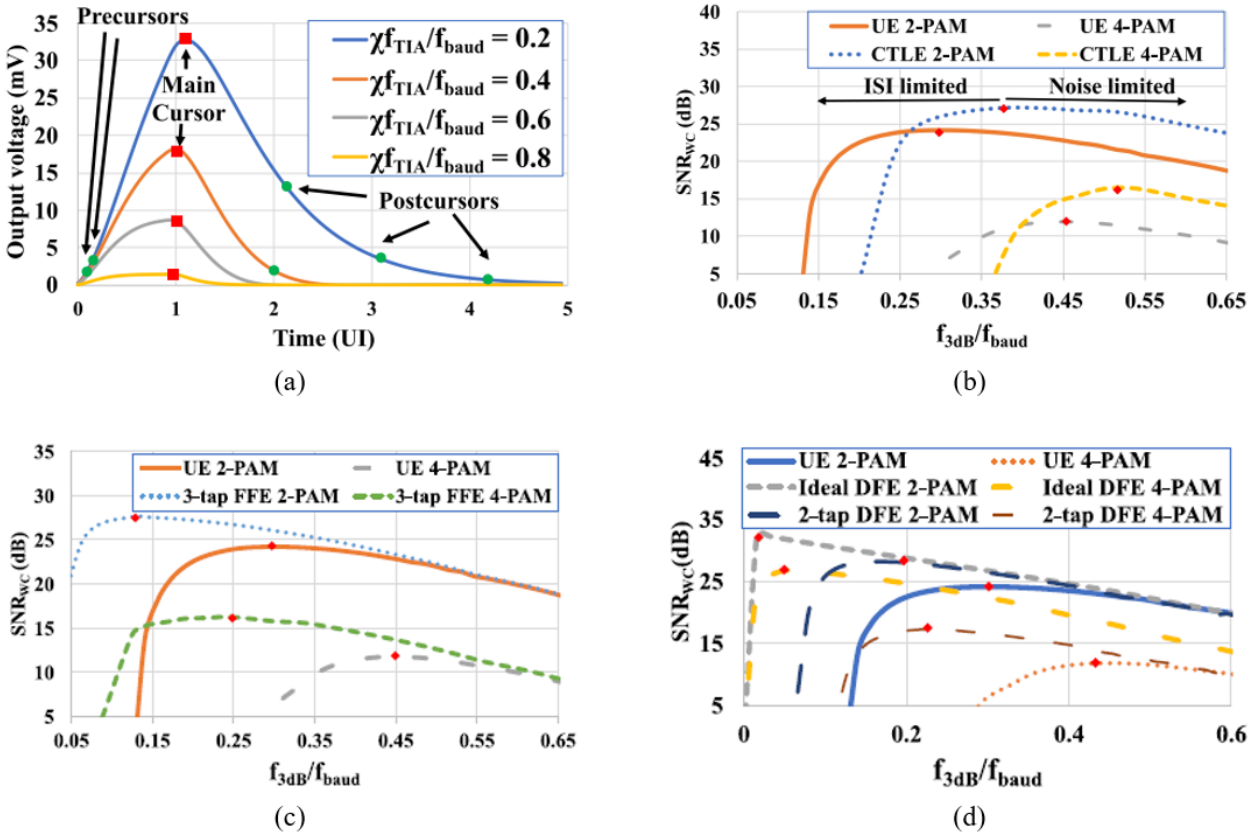


Figure 1.1: (a) Single bit response of receiver with different gains and bandwidths. SNR Comparison of unequalized (UE) to equalized implementations as a function of bandwidth/baud-rate – (b) continuous-time linear equalization (CTLE), (c) feed-forward equalization (FFE), and (d) decision feedback equalizer (DFE). [8]

bandwidth has been an active area of research for many years since the deployment of optical fibers for high bandwidth long distance transatlantic communications [7]. Demands for high bandwidth data communications from corporate, business, community, and individual levels has further led to extensive expansion of optical-fiber networks over cities and industrial complexes.

Transimpedance amplifiers (TIA), where the current signal received from the PD is converted into voltage signal, are the first stage of optical receivers. In order to optimize the signal-to-noise ratio (SNR) of the optical receiver, the gain of the TIA can be increased by intentionally limiting the bandwidth. However, this would introduce inter symbol interference (ISI) as illustrated by the

single bit response plots with various gains in Figure 1.1(a) [8]. The plot illustrates that as the gain is increased while limiting the bandwidth, there is more spreading of the signal to the neighboring symbols, hence causing more interference. However, this issue can be addressed by using an ISI equalizer. As shown in Figures 1.1(b)-(d), which compare unequalized (UE) implementation to equalized implementations, superior SNR performance can be achieved by using an ISI equalizer in conjunction with a TIA with limited bandwidth.

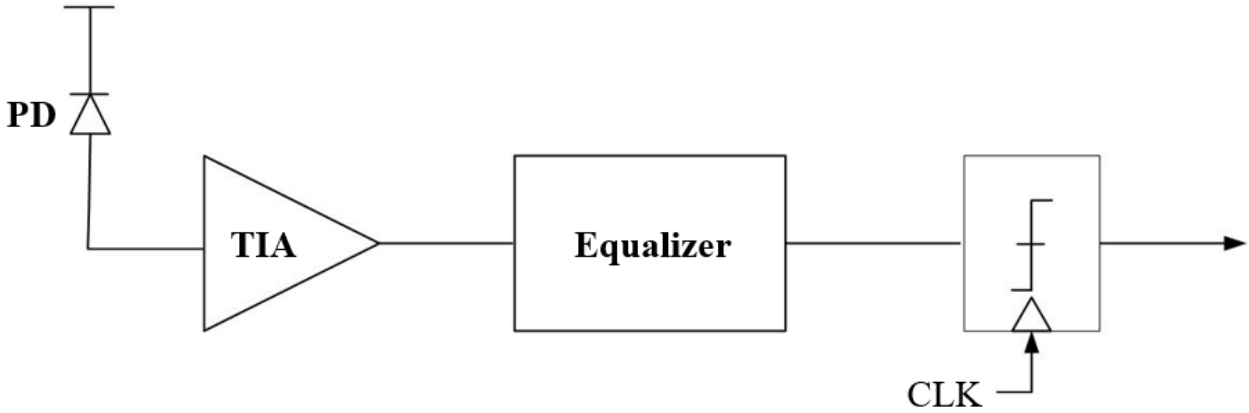


Figure 1.2: Architecture of a general mixed signal optical receiver

Figure 1.2 shows a general architecture of optical amplifiers. In this structure, the ISI equalization is done in the analog domain using continuous-time linear equalization (CTLE). In CTLE, ISI equalization is performed by simply boosting the amplitude of the high frequency components of the signal, effectively extending the bandwidth. However, in the process of boosting the high frequency signal components, the high frequency noise amplitude is unintentionally boosted as well. As a result, CLTE usually causes significant degradation of the SNR. On the contrary, FFE-DFE based systems allow for much superior SNR performance, as illustrated by Figures 1.1(b)-(d) [8]. Therefore, performing the equalization in the mixed-digital domain is more desirable as it allows FFE-DFE implementation. The ADC-DSP based architecture, shown in Figure 1.3, allows the equalization to be performed digitally in the DSP (digital signal processing) unit. A typical

ADC – DSP based optical receiver comprises of a front-end, consisting of a transimpedance amplifier (TIA) and a variable gain amplifier (VGA), followed by an analog to digital converter (ADC) unit and a DSP unit. The photocurrent generated by the P-I-N PD structure is converted into voltage signal in the TIA unit and subsequently the ISI equalization is usually done in the ADC – DSP units.

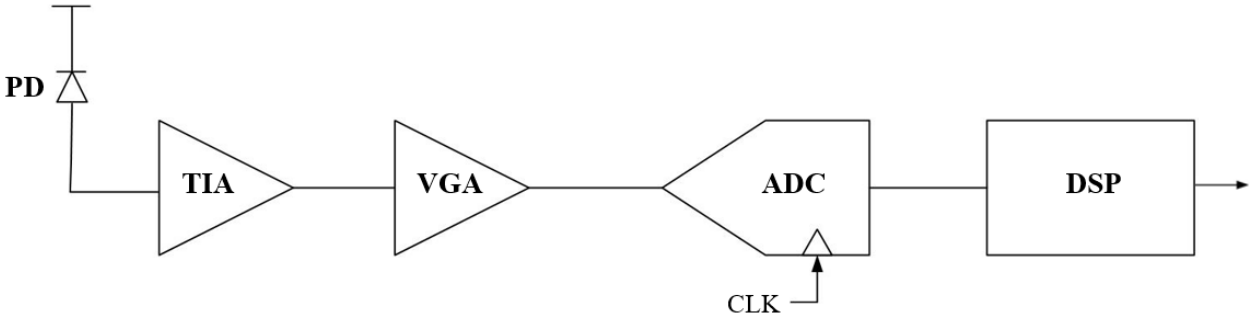


Figure 1.3: Architecture of an ADC-DSP based optical receiver.

Owing to process technology scaling, the density of transistors in chips has been doubling every two years in accordance with Moore's law [9] [10]. This has allowed significant enhancement in performance and functionalities of the chips over the years. However, as process technology scales down, power density of the chips increases. Usually when high performance chips, such as optical receivers with high gain and bandwidth, are being designed, power consumption presents itself as a major trade-off. Therefore, in order to meet the desired low power consumption requirements, energy efficient devices must be designed without sacrificing the performance. As mentioned earlier, ADC-DSP based equalizers are more desirable over the analog-based equalizers as they yield better equalization performance. However, as shown in Figure 1.4, ADC-DSP based equalizers consume more power than the analog based ones [11] – [25]. As a result, increasing the energy efficiency of ADC-DSP equalizers is of great interest.

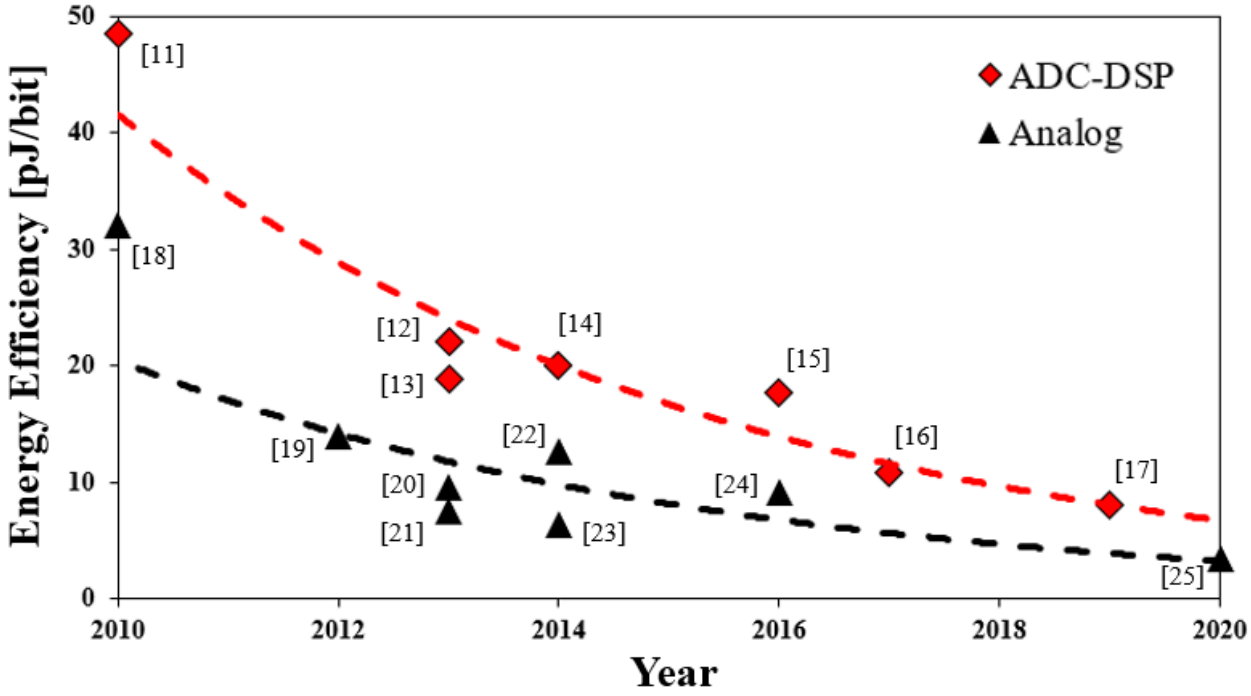


Figure 1.4: Energy efficiency trend of analog based and ADC-DSP based equalizers in the past decade.

1.2 Thesis Contributions

This thesis focuses on enhancing the performance of TIA and equalizer based optical receivers. The first contribution focuses on designing a high gain-bandwidth TIA with optimized SNR and the second contribution discusses an energy efficient ISI equalizer.

Since TIAs are the first stage of optical receivers, the performance of the TIA unit is crucial to the overall performance of the receiver. If the gain, bandwidth and noise of the TIA unit is not optimized, it bottlenecks the performance of the subsequent units. As shown in Figure 1.2, the input of the TIA unit is connected to a P-I-N PD, which has high capacitance in the range of 100fF – 500fF [26]; therefore, in order to keep the input pole from becoming the dominant pole, the TIA

must be designed to have low input resistance. There are various topologies of TIAs such as Common Gate [27] [28], Regulated Cascode [29]-[36], and Shunt Feedback [28] [37] [38]; each topology has performance trade-offs that needs to be carefully considered. The Common Gate (CG) TIA has a very simple design and consumes low power. The input pole and input referred noise of this topology are associated with the transconductance (g_m) value of the input device. However, increasing the g_m requires either increasing the size of the device or increasing the bias current, both of which indirectly compromises the bandwidth, noise, or voltage headroom. The regulated cascode (RGC) topology uses an extra amplifier stage to boost the g_m of the input device, hence improving the noise and input pole without compromising the performance as the CG TIA. However, because of the extra amplifier stage, this topology has relatively higher power consumption. In the Shunt feedback (S-FB) topology, negative feedback is provided across an amplifier through a resistor, R_F; this type of feedback lowers both the input and output resistance. However, in this topology, the transimpedance gain is proportionally dependant on R_F, while the bandwidth and noise are inversely proportional to R_F; as a result, this topology showcases major trade-offs between gain, noise and bandwidth. Aside from choosing the proper topology, the gain, bandwidth, and SNR of the TIA can be further boosted by using various techniques. The first contribution of the thesis describes a multi-stage design to enhance the performance of the TIA.

Since ISI is dependent on the neighbouring data, it includes signal components from the prior (pre-cursor) and post (post-cursor) received signals. Various techniques exist in literature and practice that can be utilized to perform the ISI equalization. From implementation standpoint, some techniques require transmitter and receiver (TxRx-eq) based implementation, while others involve only the receiver (Rx-eq). To adapt the transmitter side equalizer tap values, information regarding

the quality of the eye or link margin that are available at the sampler input on the receiver side are needed. As a result, TxRx-eq requires a back channel and link wakeup protocol, which raises Tx-Rx compatibility concerns for the equipment manufactures. Therefore, receiver-only based equalization techniques are more desirable as they provide the flexibility to the equipment manufacturers to use IPs from different vendors without requiring compatibility. Latest trend in ADC based solutions provide that flexibility [17] [39]. Fundamentally, there are two main approaches to execute ISI equalization – symbol detection and sequence detection. In symbol detection, each symbol decision is made after correcting and compensating the ISI effect of neighboring symbols. However, this approach exhibits a significant attenuation in the amplitude of the received signal causing degradation in signal-to-noise ratio (SNR). This signal attenuation can be averted by using the sequence detection approach, where the entire sequence is considered instead of a single symbol. In this approach, equalization is done by comparing the received signals to different ISI combinations and decoding based on an algorithm known as Maximum Likelihood Sequence Detector (MLSD). In this algorithm, uncorrelated random noise has less impact on the accumulated error compared to single symbol detection. The ISI is also used in a constructive way, which allows us to avoid amplitude of the signal. Both of these factors allow for a better SNR performance compared to the symbol detection approach. In the MLSD algorithm the signal is usually converted to digital domain using ADC and then the distance from the received signal to the pre-defined constellation points are calculated; the decision is subsequently made based on the distance from each constellation point. However, because of the ADC and all the digital computations, power consumption becomes a major concern in this algorithm. To address this issue, a simplified approach known as Viterbi algorithm is used, where the complexity is reduced by only retaining the two most likely transitions [40] [41]. Finding the two survivors requires

accumulating the path metric and then comparing to select using an add-compare-select (ACS) unit. However, the complexity of the Viterbi decoders increases exponentially with the number of states. Even though they can be made more affordable by adopting feedforward equalization (FFE), the energy efficiency still remains a concern. To address this, the second contribution proposes an Analog to Sequence Converter (ASC) based Maximum A Posteriori (MAP) decoding that provides several advantages over Viterbi decoding. This work has been published in the MWSCAS 2019 conference: Z. Huda, S. Dey, A. Monai, Aurangozeb and M. Hossain, "Affordable Sequence Decoding Techniques for High Speed SerDes," *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2019, pp. 1053-1056.

1.3 Thesis Organization

Chapter 2 of the thesis focuses on designing a high gain-bandwidth TIA. In order to optimize the performance, the chapter first explores the advantages and disadvantages of different TIA topologies. It then proposes a multi-stage TIA design that employs various techniques to enhance the performance. The proposed TIA design can achieve a transimpedance gain of 55 dB and 3dB bandwidth of 32 GHz.

Chapter 3 discusses an energy efficient ISI equalizer design that can operate at high data rates. The chapter first describes different ISI equalization techniques that can be employed, both from theoretical and implementation standpoint; it discusses the benefits and challenges each approach exhibit. Then the chapter proposes an Analog to Sequence Converter based Maximum A Posteriori ISI equalization technique. The implemented prototype is capable of compensating 35+ dB loss at 10 Gb/s data rate with better than 10 pJ/bit energy efficiency.

Lastly, chapter 4 summarizes the contribution of this thesis towards designing high performance optical receivers and discusses further progresses that can be made in the future.

Chapter 2

High Gain-Bandwidth Transimpedance Amplifier

2.1 Introduction

Transimpedance amplifiers (TIA) are used in optical receivers to convert the photocurrent signal from the P-I-N photodiodes (PD) to voltage signal. As TIAs are the first module of optical receivers, their performance heavily impacts the performances of the successive units. Therefore, optimizing the performance of the TIA unit is of great interest. There are various topologies of TIAs such as Common Gate [27] [28], Regulated Cascode [29]-[36], and Shunt Feedback [28] [37] [38]. Each topology has its own trade-offs between gain, bandwidth, noise, and/or power consumption. Therefore, the advantages and disadvantages of the topologies need to be compared carefully when designing a high-performance TIA. Aside from using the proper topology, the performance can also be enhanced by employing various techniques in the subsequent stages of the TIA.

This chapter first explores and compares the benefits and challenges of using each topology in section 2.2. It then describes the proposed TIA design with enhanced performance in section 2.3. Lastly, Section 2.4 discusses the implementation of the proposed design and compares its performance with other existing designs.

2.2 Transimpedance Amplifier Topologies

When designing a multi-stage transimpedance amplifier (TIA), the performance of the first stage is crucial to the overall performance of the amplifier. Minimizing the noise of the first stage is critical since the noise signal gets amplified by the subsequent stages. If the gain of the first stage is low, the noise contributed by the following stages become significant as well, affecting the overall signal-to-noise ratio (SNR) of the amplifier. Since the TIA is connected to a photodiode, which has high capacitance in the range of 100-500fF [26], the pole at the input node can become the dominant pole, which would limit the overall bandwidth of the TIA. Therefore, the input pole of the first stage needs to be maximized as much as possible in order to isolate the effect of the large capacitance of the photodiode. This section examines the performances of three TIA topologies – Common Gate, Regulated Cascode, and Shunt Feedback. The trade-offs between gain, noise, and bandwidth for each of these topologies is explored in this section. The data of the three topologies are compared to each other as well to determine which one yields the best performance. In order to properly compare the noise of the different topologies – with different gains and bandwidths – input referred noise density values are utilized.

A. Common Gate Transimpedance Amplifier

In this section, performance of the Common Gate (CG) topology is discussed. The schematic and the small signal model of a Common Gate Transimpedance Amplifier are shown in Figure 2.1. As illustrated in Figure 2.1(a), the input current signal (I_{in}) is supplied at the source node of the M_1 device and the output voltage signal (V_{out}) is taken at the drain node of the device, making it a common gate amplifier; M_2 is used as a current source. C_{in} is the sum of all the capacitance at the

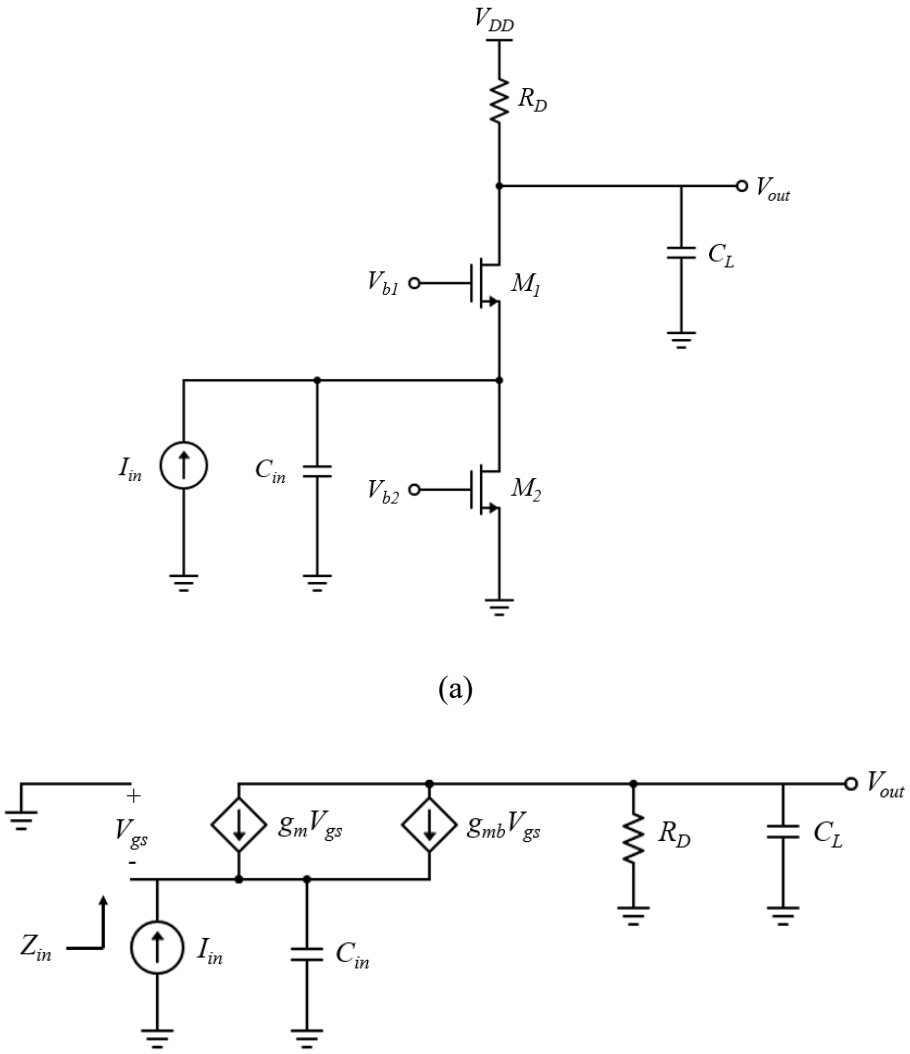


Figure 2.1: (a) Schematic of CG TIA. (b) Small signal model of CG TIA.

input node which includes the photodiode capacitance, wiring capacitance and the device parasitic capacitances at that node (C_{GS1}, C_{SB1}, C_{GD2}, C_{DB2}). C_L is the total output capacitance which consists of C_{GD1}, C_{DB1} and the capacitance from the next stage. The resistor R_D is connected between the drain node and the power supply V_{DD}. Devices M_1 and M_2 are biased using V_{b1} and V_{b2}, respectively.

In order to derive the transfer function, the small signal model of the circuit in Figure 2.1(b) is utilized. Taking into account that the resistance seen at the source node of a MOSFET is $(g_m + g_{mb})^{-1}$, the input impedance Z_{in} is,

$$Z_{in} = \frac{1}{g_m + g_{mb}} \,||\, \frac{1}{sC_{in}} \tag{2.1}$$

Using equation (2.1) the voltage at the source node V_s can be derived,

$$V_s = I_{in} \times Z_{in} \tag{2.2}$$

$$V_s = I_{in}\left(\frac{1}{g_m + g_{mb}} \,||\, \frac{1}{sC_{in}}\right) \tag{2.3}$$

Considering that the gate node is connected to AC ground, the gate-source voltage is $V_{gs} = -V_s$. Therefore, an expression for V_s can also be derived at the output node by applying KCL at the output node and then solving for V_s

$$V_{out} = V_s(g_m + g_{mb})\left(R_D \,||\, \frac{1}{sC_L}\right) \tag{2.4}$$

$$V_s = \frac{V_{out}}{(g_m + g_{mb})\left(R_D \,||\, \frac{1}{sC_L}\right)} \tag{2.5}$$

The transfer function Z_T is obtained by equating (2.3) and (2.5), then solving for $\frac{V_{out}}{I_{in}}$

$$I_{in}\left(\frac{1}{g_m + g_{mb}} \,||\, \frac{1}{sC_{in}}\right) = \frac{V_{out}}{(g_m + g_{mb})\left(R_D \,||\, \frac{1}{sC_L}\right)} \tag{2.6}$$

$$Z_T(s) = \frac{V_{out}}{I_{in}} = (g_m + g_{mb})\left(R_D \,||\, \frac{1}{sC_L}\right)\left(\frac{1}{g_m + g_{mb}} \,||\, \frac{1}{sC_{in}}\right) \tag{2.7}$$

Thus,

$$Z_T(s) = \frac{R_D}{\left(1 + s\frac{C_{in}}{g_m + g_{mb}}\right)(1 + sC_L R_D)} \tag{2.8}$$

The transfer function in equation (2.8) reveals that the DC gain of a CG TIA is equal to R_D and the input pole is $(g_m + g_{mb})/C_{in}$.

In order to analyze the noise performance of the amplifier, the noise sources are added to the circuit as illustrated in Figure 2.2(a). $\overline{I_{n,RD}^2} = 4kT/R_D$ represents the thermal noise contributed from R_D, where k is the Boltzmann's constant and T is the temperature in Kelvin; the thermal noise contributed from M_1 and M_2 are depicted by $\overline{I_{n,M1}^2} = 4kT\gamma g_{m1}$ and $\overline{I_{n,M2}^2} = 4kT\gamma g_{m2}$ respectively, where γ is the excess noise coefficient. $\overline{V_{n,out}^2}$ is the total noise at the output node contributed by all the noise sources.

The small signal model in Figure 2.2(b) is employed to perform the noise analysis. Initially, KCL is applied at the source node noting that $V_{gs} = -V_s$; then, the equation is manipulated to isolate V_s,

$$sC_{in}V_s + I_{n,M2} = I_{n,M1} - (g_m + g_{mb})V_s \tag{2.9}$$

$$V_s = \frac{I_{n,M1} - I_{n,M2}}{g_m + g_{mb} + sC_{in}} \tag{2.10}$$

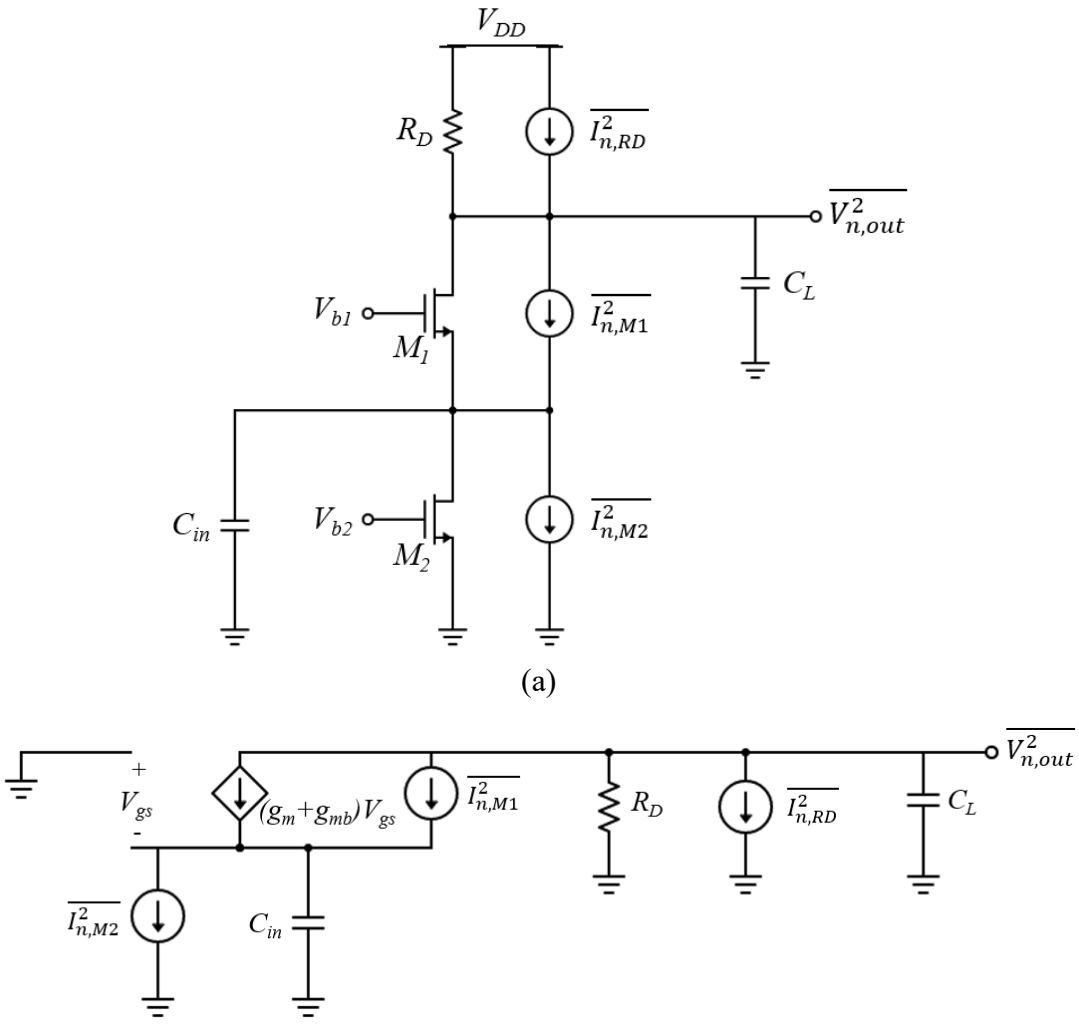


Figure 2.2: (a) Schematic of CG TIA with noise sources. (b) Small signal model of CG TIA with noise sources.

Furthermore, the following equations are derived by applying similar procedure at the output node and taking (2.9) into account

$$-\frac{V_{n,out}}{R_D+\frac{1}{sC_I}}+I_{n,RD}=I_{n,M1}-(g_m+g_{mb})V_s \tag{2.11}$$

$$=sC_{in}V_s+I_{n,M2} \tag{2.12}$$

$$V_s=\frac{-V_{n,out}\left(sC_L+\frac{1}{R_D}\right)+I_{n,RD}-I_{n,M2}}{sC_{in}} \tag{2.13}$$

The output noise expression is derived by equating (2.10) to (2.13)

$$\frac{-V_{n,out}\left(sC_L+\frac{1}{R_D}\right)+I_{n,RD}-I_{n,M2}}{sC_{in}}=\frac{I_{n,M1}-I_{n,M2}}{g_m+g_{mb}+sC_{in}} \tag{2.14}$$

Hence,

$$V_{n,out}=\frac{R_D I_{n,RD}}{1+sC_L R_D}-\frac{R_D sC_{in} I_{n,M1}}{(g_m+g_{mb}+sC_{in})(1+sC_L R_D)} + \frac{(g_m+g_{mb})R_D I_{n,M2}}{(g_m+g_{mb}+sC_{in})(1+sC_L R_D)} \tag{2.15}$$

The expression for input referred noise current is obtained by dividing (2.15) by the transimpedance gain in (2.8),

$$I_{n,in}(s)=\frac{(g_m+g_{mb}+sC_{in})I_{n,RD}}{g_m+g_{mb}}-\frac{sC_{in}I_{n,M1}}{g_m+g_{mb}}+I_{n,M2} \tag{2.16}$$

Thus, the input referred noise spectrum, $\overline{I_{n,in}^2}(f)=\left|I_{n,in}(s)\right|^2$, with the expressions for the noise current sources Substituted in is,

$$\overline{I_{n,in}^2}(f)=\underbrace{\left(1+\left(\frac{2\pi C_{in}f}{g_{m1}+g_{mb1}}\right)^2\right)\frac{4kT}{R_D}}_{\textbf{Noise from } R_D}+\underbrace{\left(\frac{2\pi C_{in}f}{g_{m1}+g_{mb1}}\right)^2 4kT\gamma g_{m1}}_{\textbf{Noise from } M_1}+\underbrace{4kT\gamma g_{m2}}_{\textbf{Noise from } M_2} \tag{2.17}$$

Observing equation (2.17) closely reveals that the input referred noise can be reduced by increasing the g_{m1}. Furthermore, provided that the input pole is equal to $(g_{m1}+g_{mb1})/C_{in}$, the bandwidth can also be enhanced by increasing the g_{m1}. The value of g_{m1} can be increased by increasing the width of M_1 or by increasing the bias current. The change in input noise density and bandwidth with respect to the bias current is illustrated in Figure 2.3. This demonstrates that maximizing the

g_m would yield to enhancing the performance of the CG TIA. However, increasing the size of M_1 increases the parasitic capacitance more rapidly than g_{m1}, which in turn increases C_{in}; that reduces the input pole and also increases the noise contribution from M_1 and R_D at higher frequency. Increasing the bias current increases the voltage drop across R_D and the minimum allowable drain-source voltage of M_2; accommodating that requires a greater voltage headroom to keep all the devices biased properly. The minimum allowable drain-source voltage of M_2 can be minimized by increasing the size of M_2; however, that would increase the g_{m2} and C_{in}, causing the noise to increase and bandwidth to drop. R_D can also be reduced to allow for greater bias current and less voltage drop across R_D. However, reducing R_D also decreases the gain of the TIA and increases the noise contribution from R_D. Therefore, it is challenging to maximize the g_m of the CG TIA without indirectly compromising the bandwidth, noise, or voltage headroom [31] [36].

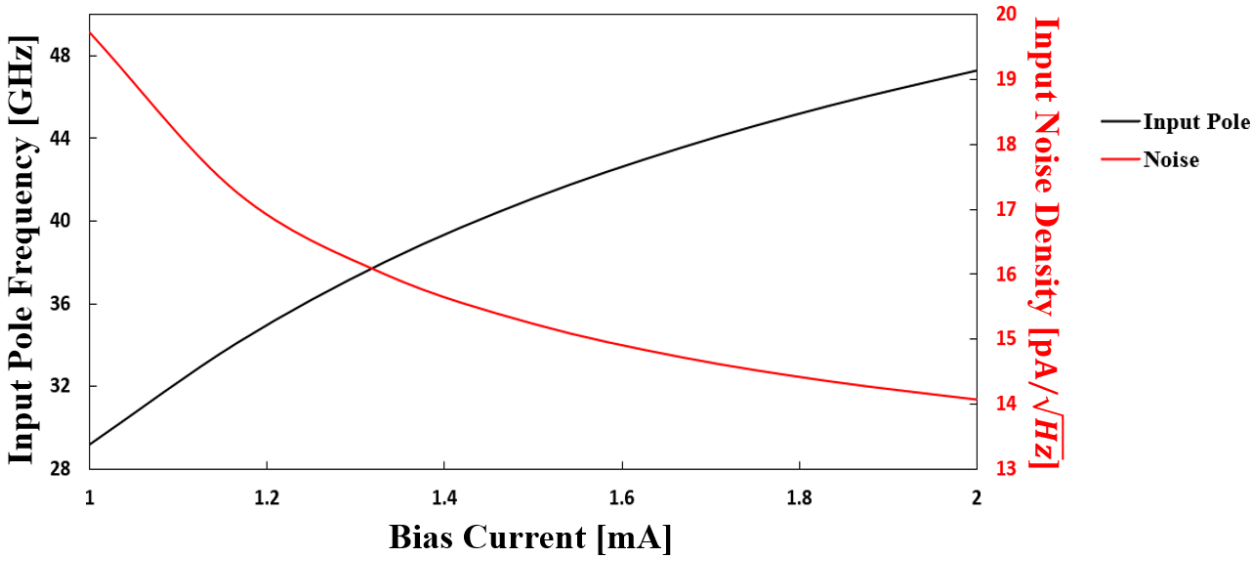


Figure 2.3: Change in input pole frequency and input noise density with respect to bias current.

B. Regulated Cascode Transimpedance Amplifier

As discussed in section A, increasing the g_m yields to better noise and bandwidth performance of the TIA. In this section, the Regulated Cascode (RGC) topology is explored, which allows the boost of g_m without the trade-offs as in the CG TIA case [29] [32]. In the RGC topology, a voltage amplifier with a finite gain of $-A_v$ is connected between the source node and the gate node of M_1, as shown in Figure 2.4(a), to boost the effective g_m.

Since the gate node is connected to the source node through the $-A_v$ amplifier as shown in the small signal model in Figure 2.4(b), the gate voltage is $V_g = -A_v V_s$, which causes the gate-source voltage to be $V_{gs} = -(1+A_v)V_s$. As a result, the input resistance seen at the source node is $((g_m + g_{mb})(1+A_v))^{-1}$. Therefore, the input impedance for the amplifier is

$$Z_{in} = \frac{1}{(g_m + g_{mb})(1 + A_v)} \,||\, \frac{1}{sC_{in}} \tag{2.18}$$

Using equation (2.18) the voltage at the source node V_s is derived,

$$V_s = I_{in}\left(\frac{1}{(g_m + g_{mb})(1 + A_v)} \,||\, \frac{1}{sC_{in}}\right) \tag{2.19}$$

Applying KCL at the output node and solving for V_s yields

$$V_s = \frac{V_{out}}{(g_m + g_{mb})(1 + A_v)\left(R_D \,||\, \frac{1}{sC_L}\right)} \tag{2.20}$$

Equating (2.19) and (2.20) yields

$$I_{in}\left(\frac{1}{(g_m + g_{mb})(1 + A_v)} \,||\, \frac{1}{sC_{in}}\right) = \frac{V_{out}}{(g_m + g_{mb})(1 + A_v)\left(R_D \,||\, \frac{1}{sC_L}\right)} \tag{2.21}$$

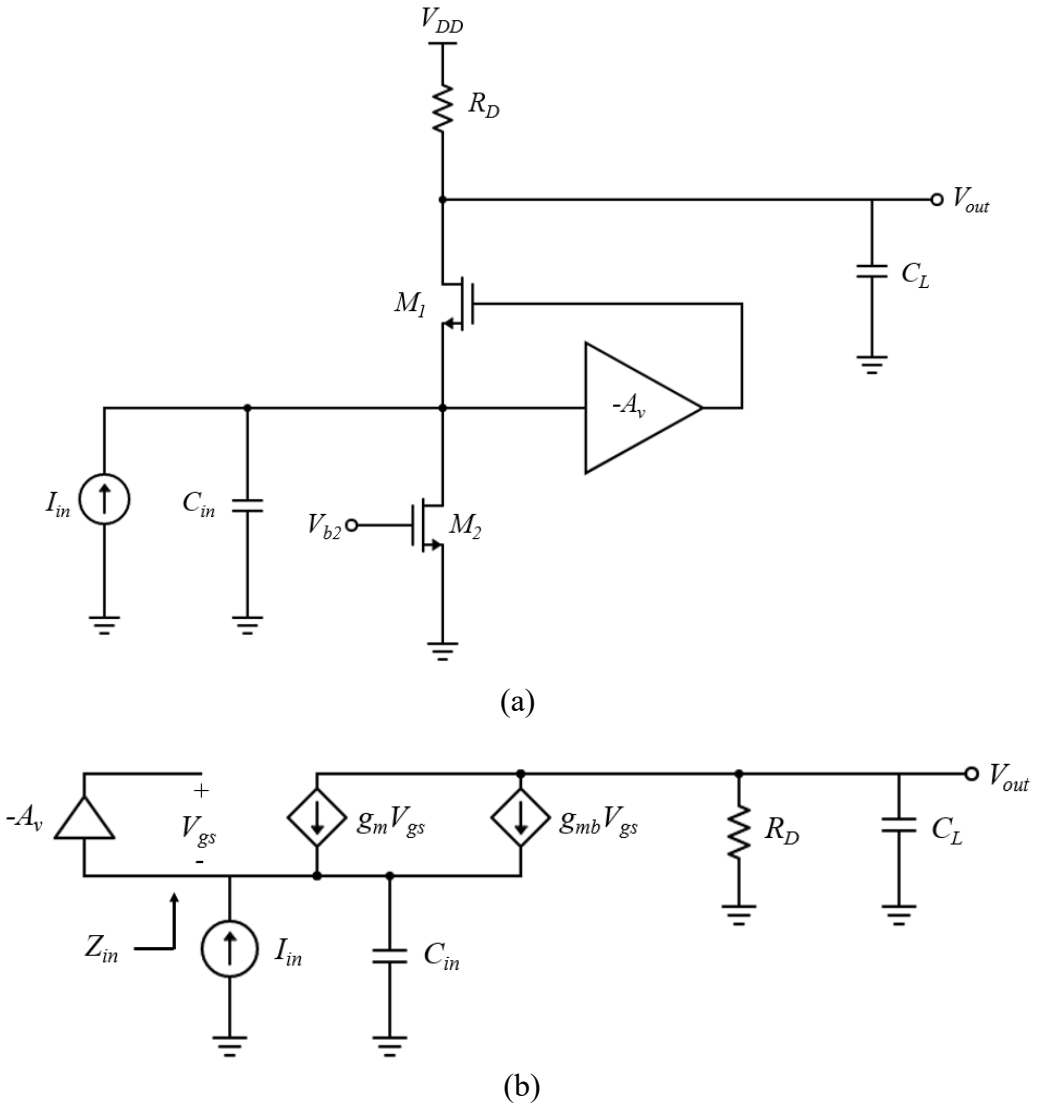


Figure 2.4: (a) Schematic and (b) Small signal model of RGC TIA.

Thus,

$$Z_T(s) = \frac{R_D}{\left(1 + s\frac{C_{in}}{(g_m + g_{mb})(1 + A_v)}\right)(1 + sC_L R_D)} \qquad 2.22$$

(2.22) reveals that the midband transimpedance gain of the RGC topology is the same as the CG topology; however, the input pole of the of the RGC TIA is $(1 + A_v)(g_m + g_{mb})/C_{in}$, a factor of $(1 + A_v)$ greater than the CG TIA.

The thermal noise sources of R_D, M_1 and M_2 are added to the RGC TIA schematic, as shown in Figure 2.5, to analyze the noise performance of the circuit. Provided that $V_{gs} = -(1 + A_v)V_s$, the following expression is formulated by applying KCL at the source node

$$V_s = \frac{I_{n,M1} - I_{n,M2}}{(g_m + g_{mb})(1 + A_v) + sC_{in}} \tag{2.23}$$

Noting that $I_{n,M1} + (g_m + g_{mb})V_{gs} = sC_{in}V_s + I_{n,M2}$, an expression for V_s is also acquired at the drain node

$$V_s = \frac{-V_{n,out}\left(sC_L + \frac{1}{R_D}\right) + I_{n,RD} - I_{n,M2}}{sC_{in}} \tag{2.24}$$

The output noise voltage is then derived by equating (2.23) to (2.24)

$$\frac{-V_{n,out}\left(sC_L + \frac{1}{R_D}\right) + I_{n,RD} - I_{n,M2}}{sC_{in}} = \frac{I_{n,M1} - I_{n,M2}}{(g_m + g_{mb})(1 + A_v) + sC_{in}} \tag{2.25}$$

Thus,

$$V_{n,out} = \frac{R_D I_{n,RD}}{1 + sC_L R_D} - \frac{R_D sC_{in} I_{n,M1}}{\left((g_m + g_{mb})(1 + A_v) + sC_{in}\right)(1 + sC_L R_D)} + \frac{(g_m + g_{mb})(1 + A_v) R_D I_{n,M2}}{\left((g_m + g_{mb})(1 + A_v) + sC_{in}\right)(1 + sC_L R_D)} \tag{2.26}$$

The input referred noise current is obtained by dividing (2.26) by the transimpedance gain in (2.22)

$$I_{n,in}(s) = \frac{\left((g_m + g_{mb})(1 + A_v) + sC_{in}\right) I_{n,RD}}{(g_m + g_{mb})(1 + A_v)} - \frac{sC_{in} I_{n,M1}}{(g_m + g_{mb})(1 + A_v)} + I_{n,M2} \tag{2.27}$$

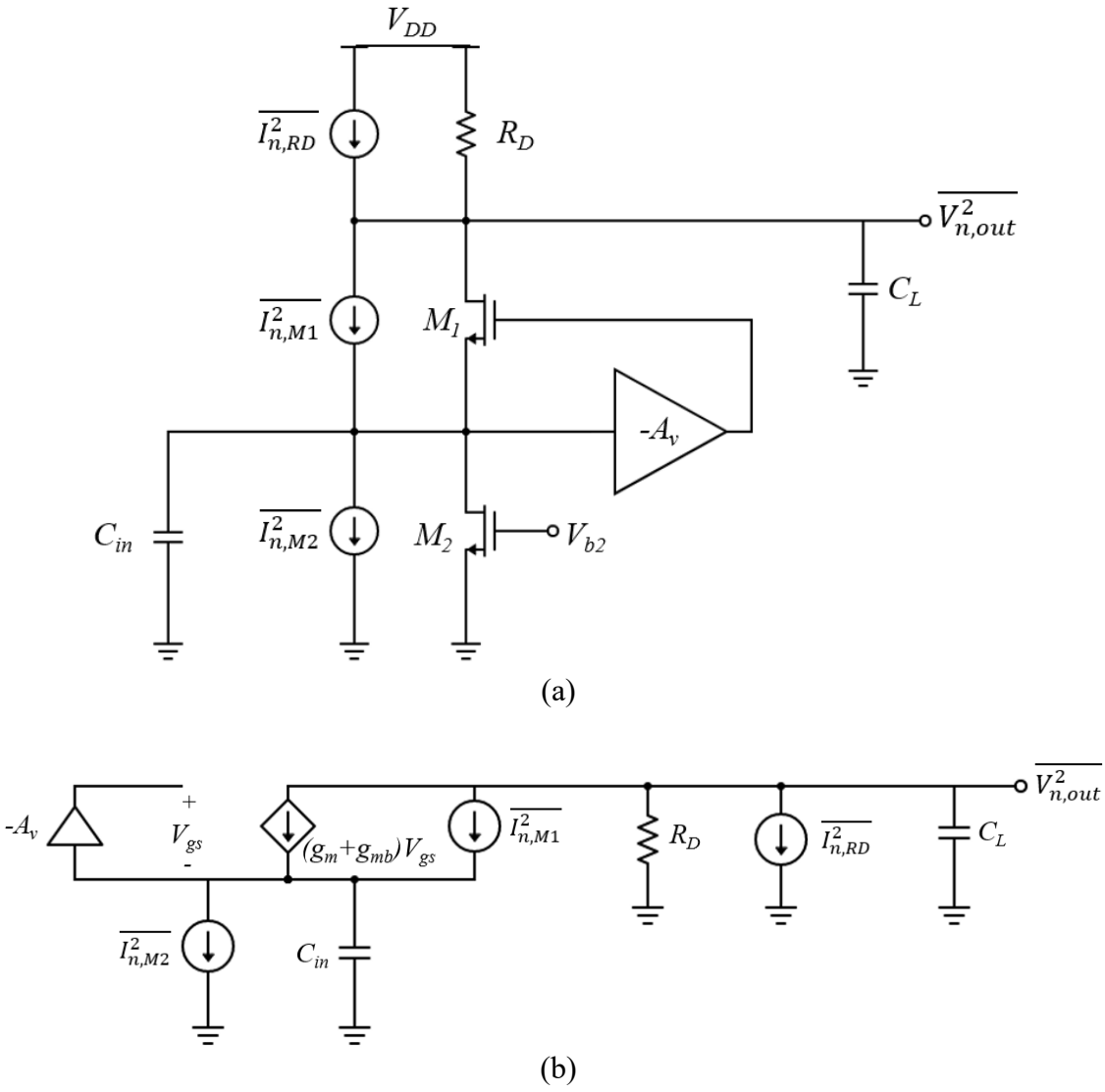


Figure 2.5: (a) Schematic and (b) Small signal model of RGC TIA with noise sources.

Thus, the input referred noise spectrum with the expressions for the noise current sources Substituted in is,

$$\overbrace{\overline{I_{n,in}^2}(f) = \left(1 + \left(\frac{2\pi C_{in} f}{(g_m + g_{mb})(1 + A_v)}\right)^2\right)\frac{4kT}{R_D}}^{\textbf{Noise from } R_D} + \overbrace{\left(\frac{2\pi C_{in} f}{(g_m + g_{mb})(1 + A_v)}\right)^2 4kT\gamma g_{m1}}^{\textbf{Noise from } M_1}$$

$$\underbrace{+ 4kT\gamma g_{m2}}_{\textbf{Noise from } M_2} \qquad 2.28$$

By comparing the transfer function and input referred noise of the RGC TIA to that of the CG TIA, it can be observed that the effective g_m seen by the circuit is boosted by a factor of $(1 + A_v)$. The noise and bandwidth performance of the RGC TIA compared to the CG TIA is shown in Figure 2.6; the dotted plots illustrate the improved performance of the RGC topology. The bias current value in the x-axis is the bias current of the M_1 device. As expected, the RGC topology yields higher input pole frequency and lower input referred noise for the same M_1 device size and bias current since it sees a higher effective g_m. Therefore, this topology can better maximize the effective g_m without indirectly compromising the noise, bandwidth, or voltage headroom. However, because of the extra voltage amplifier stage, the RGC TIA draws more power than the CG TIA. Also, in addition to the M_1 and M_2 devices, the devices in the $-A_v$ amplifier also need to be kept biased properly; that might add extra constraints to the bias current of the CG stage.

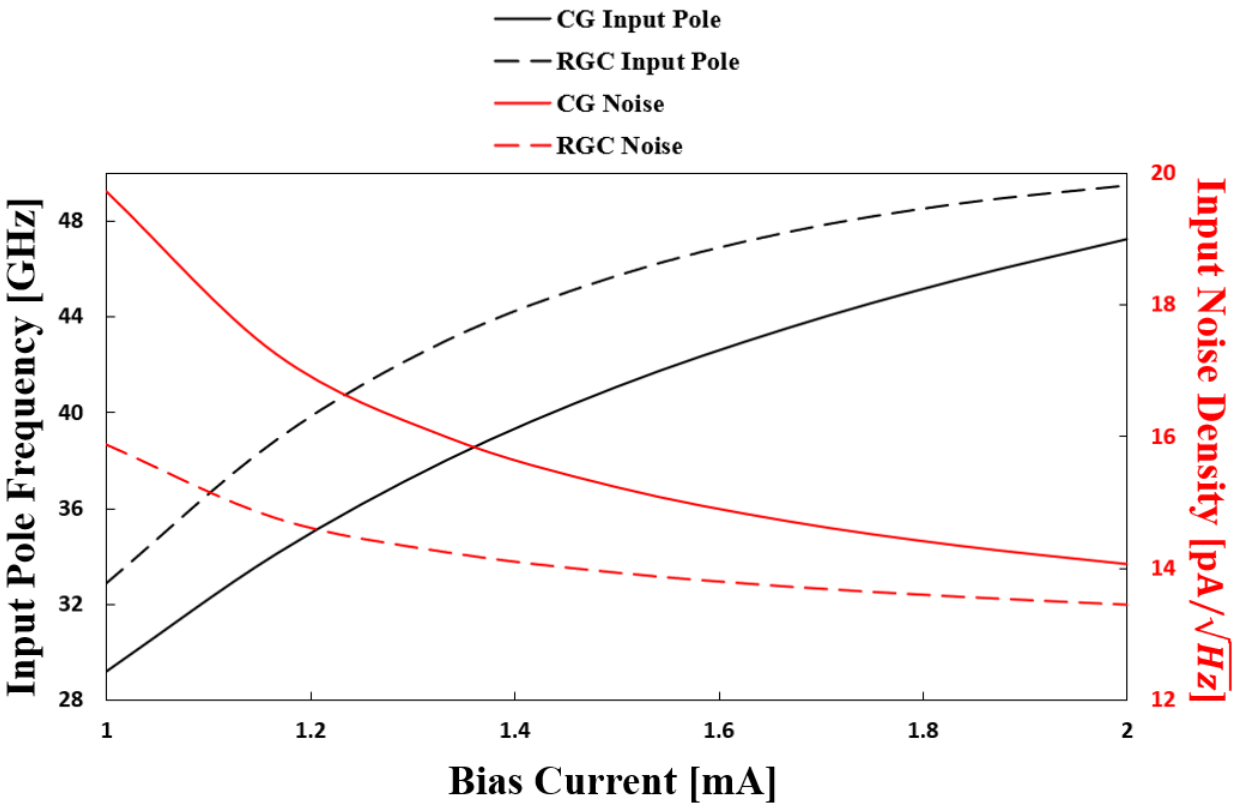


Figure 2.6: Noise and bandwidth performance of CG and RGC topologies with respect to bias current.

The performance for the CG topology and the RGC topology can also be enhanced by replacing the M_2 device with a source resistor, R_S. Replacing M_2 with R_S reduces the C_{in} and also decreases the input resistance, hence enhancing the input pole; the input poles of the CG and RGC topologies become $(1 + (g_m + g_{mb})R_S)/(C_{in}R_S)$ and $(1 + (1 + A_v)(g_m + g_{mb})R_S)/(C_{in}R_S)$, respectively. The noise current of R_S is usually lower than the noise current of M_2. Therefore, Replacing M_2 with R_S can also reduce the noise.

The $-A_v$ amplifier can be implemented with a Common Source (CS) amplifier as shown in Figure 2.7. The CS stage consists of the M_3 device and the R_1 resistor; the input of this stage is at the gate node of M_3 and the output is taken at the drain node. Meaning, the CS stage receives the signal

from the source node of M_1 and feeds the amplified signal to the gate node, making this design consistent with Figure 2.4. Given that the voltage gain of an CS amplifier is $-g_m R$, the design in Figure 2.7 boosts the g_m of the CG stage by a factor of $(1 + g_{m3} R_1)$.

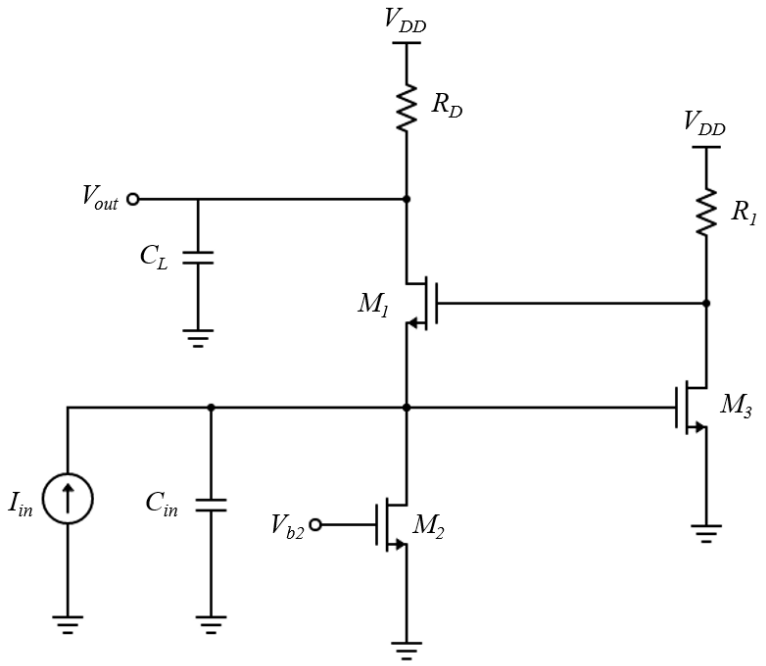


Figure 2.7: Schematic of RGC TIA with CS amplifier.

C. Shunt Feedback Transimpedance Amplifier

In this section, the Shunt feedback (S-FB) TIA topology is explored, where negative feedback is provided from the output to the input; this type of feedback lowers both the input and output resistance [37]. An S-FB TIA is designed by connecting a resistor between the output and input nodes an amplifier with a gain of -A_v, as illustrated in Figure 2.8; R_F provides voltage-current feedback around the voltage amplifier. The parasitic capacitances of the devices in the amplifier at the input and output nodes is included in C_{in} and C_L, respectively.

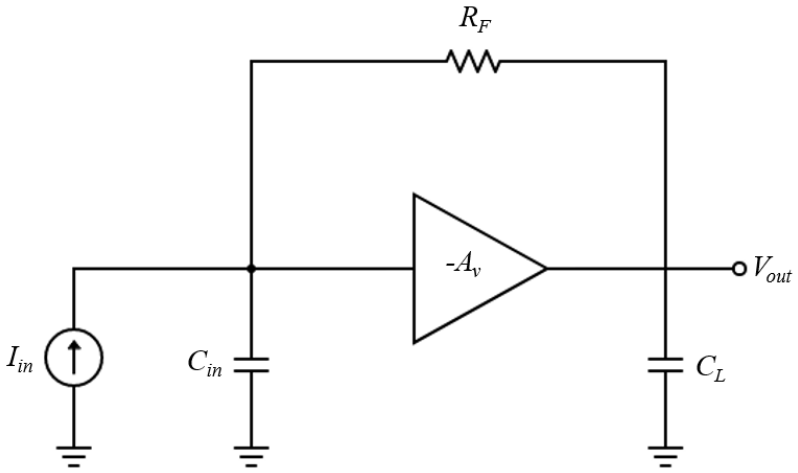


Figure 2.8: Schematic of S-FB TIA.

Noting that $V_{in} = V_{out}/(-A_v)$, the midband transimpedance gain of the S-FB TIA can be derived by applying KCL at the input node

$$I_{in} = \frac{V_{in} - V_{out}}{R_F} \tag{2.29}$$

$$= -\frac{\frac{V_{out}}{A_v} + V_{out}}{R_F} \tag{2.30}$$

Thus,

$$\frac{V_{out}}{I_{in}} = -\frac{A_v}{1 + A_v} R_F \tag{2.31}$$

Furthermore, the resistance seen at the input and output nodes is also derived by applying similar procedures,

$$R_{in} = \frac{R_F}{1 + A_v} \tag{2.32}$$

$$R_{out} = \frac{A_v R_F}{1 + A_v} \tag{2.33}$$

The transfer function is obtained using (2.31), (2.32), and (2.33)

$$Z_T(s) = -\frac{A_v}{1+A_v}\frac{R_F}{\left(1+s\frac{R_F C_{in}}{1+A_v}\right)\left(1+s\frac{A_v R_F C_L}{1+A_v}\right)} \tag{2.34}$$

Since $A_v \gg 1$, the midband gain is approximately equal to R_F and the input pole is approximately equal to $A_v/(R_F C_{in})$.

The voltage amplifier and the feedback resistor are the noise contributors in the S-FB topology. Their thermal noise contributions are modeled by series voltage sources, as shown in Figure 2.9; $\overline{V_{n,RF}^2} = 4kTR_F$ models the resistor noise and $\overline{V_{n,Av}^2}$ models the input referred noise of the amplifier. Since the effect of the load capacitor cancels out when dividing the output noise by the transfer function to acquire the input referred noise, the load capacitor is disregarded for the noise calculations.

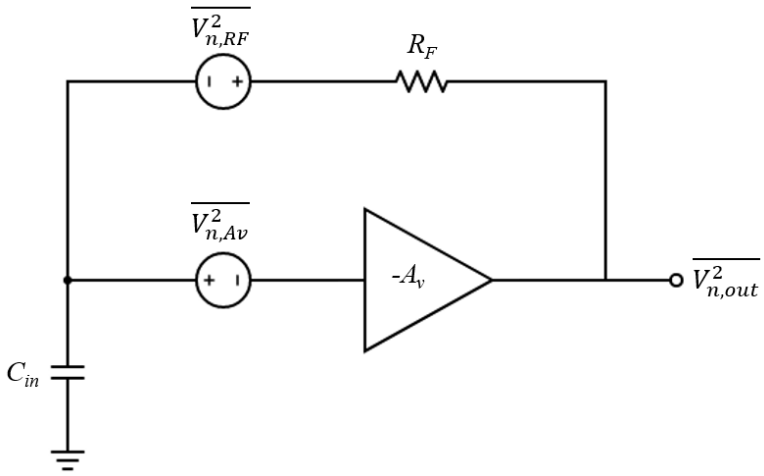


Figure 2.9: Schematic of S-FB TIA with noise sources.

Recognizing that $V_{n,in} = V_{n,out}/(-A_v) + V_{n,Av}$, applying KCL at the input node yields

$$\frac{V_{n,out} - \left(V_{n,in} + V_{n,RF}\right)}{R_F} = sC_{in}V_{n,in} \tag{2.35}$$

$$\frac{V_{n,out} + \frac{V_{n,out}}{A_v} - V_{n,Av} - V_{n,RF}}{R_F} = sC_{in}\left(\frac{V_{n,out}}{-A_v} + V_{n,Av}\right) \tag{2.36}$$

Thus,

$$V_{n,out} = \frac{A_v}{1 + A_v}\frac{V_{n,RF} + (1 + sR_FC_{in})V_{n,Av}}{1 + s\frac{R_FC_{in}}{1 + A_v}} \tag{2.37}$$

The input referred noise current is obtained by dividing (2.37) by (2.34), disregarding C_L

$$I_{n,in}(s) = \frac{V_{n,RF} + (1 + sR_FC_{in})V_{n,Av}}{R_F} \tag{2.38}$$

Therefore, the input referred noise spectrum is

$$\overline{I_{n,in}^2}(f) = \underbrace{\frac{4kT}{R_F}}_{\text{Noise from } R_F} + \underbrace{\left(\frac{1}{R_F^2} + (2\pi C_{in}f)^2\right)\overline{V_{n,Av}^2}}_{\text{Noise from Amplifier}} \tag{2.39}$$

Equation (2.39) reveals that the input referred noise decreases as R_F is increased. Also, the transfer function in (2.34) reveals that the transimpedance gain increases with increasing R_F as well. However, given that the input pole is approximately equal to $A_v/(R_FC_{in})$, increasing R_F limits the bandwidth. As a result, the trade-off between noise/gain and bandwidth needs to be considered when designing the circuit. The trade-off between the noise and bandwidth with respect to R_F is illustrated in Figure 2.10.

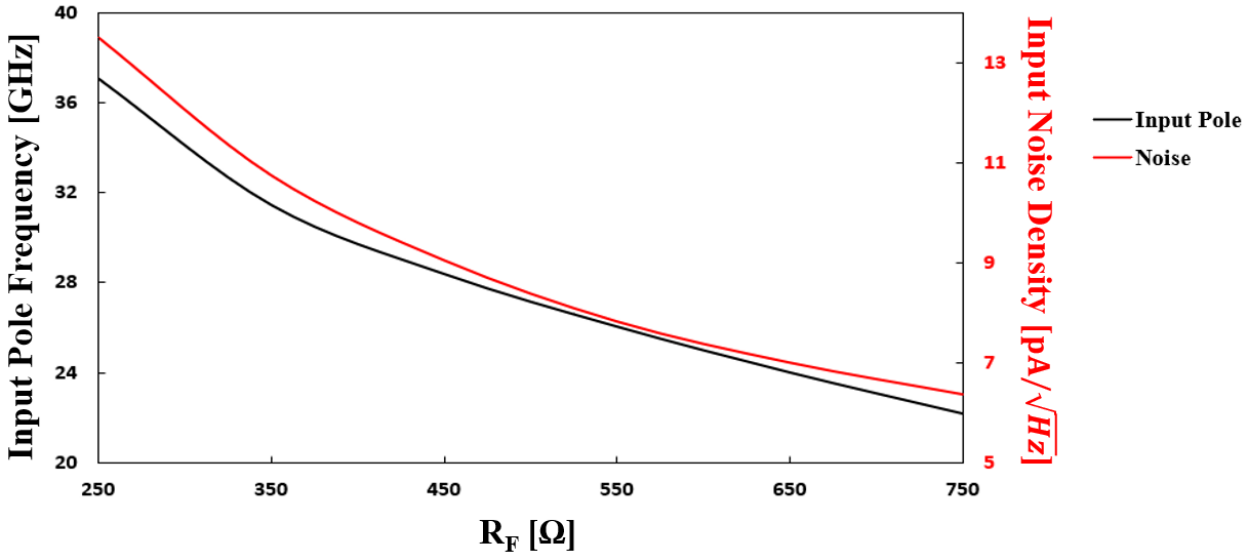


Figure 2.10: Noise and bandwidth performance of S-FB TIA with respect to R_F.

The S-FB TIA is implemented by using a CMOS inverter as the voltage amplifier, which consists of a PMOS device, M_p, and an NMOS device, M_n; the gate nodes and the drain nodes of the two devices are shorted to each other, as shown in Figure 2.11. R_F provides feedback from the output at the source node to the input at the gate node. The gain of a CMOS amplifier is $-G_m R_o$, where $G_m = g_{m.n} + g_{m,p}$ is the summation of the transconductances of the two devices and $R_o = r_{o,n}||r_{o,p}$ is the combined on-resistance of the devices. The output noise of a CMOS inverter amplifier is $\overline{V_{n,Av,out}^2} = 4kT\gamma G_m R_o^2$. Thus, the input referred noise of the amplifier is $\overline{V_{n,Av,}^2} = 4kT\gamma/G_m$. Therefore, noting that $A_v \gg 1$, the approximate transfer function and input referred noise spectrum of the S-FB TIA implementation in Figure 2.11 is

$$Z_T(s) \approx -\frac{R_F}{\left(1 + s\frac{R_F C_{in}}{G_m R_o}\right)(1 + sR_F C_L)} \qquad 2.40$$

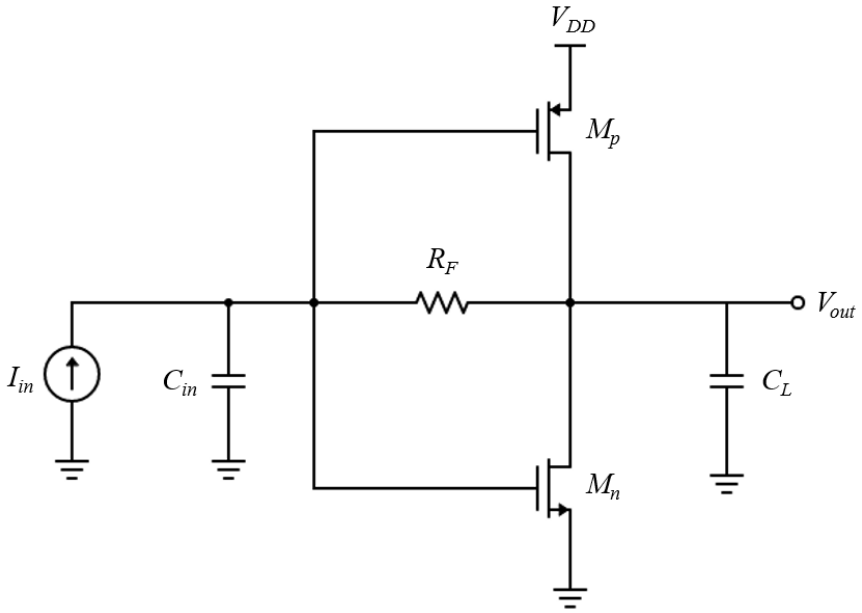


Figure 2.11: Schematic of S-FB TIA implemented with CMOS inverter amplifier.

$$\overline{I_{n,in}^2}(f) = \underbrace{\frac{4kT}{R_F}}_{\text{Noise from } R_F} + \underbrace{\left(\frac{1}{R_F^2} + (2\pi C_{in} f)^2\right)\frac{4kT\gamma}{G_m}}_{\text{Noise from Amplifier}} \qquad 2.41$$

Equations (2.40) and (2.41) reveal that increasing the G_m will extend the bandwidth and reduce noise. However, increasing G_m also increases C_{in}, which eventually limits the bandwidth and causes greater noise contribution from the amplifier at higher frequencies. Also, increasing the G_m increases the bias current which causes higher power consumption.

D. Performance Comparison

Table 2.1 compares the simulated bandwidth, noise, and power consumption performances of the three topologies at the same transimpedance gain. The CG and RGC topologies were simulated using a source resistor instead of the M_2 device in order to enhance their performances. As

expected, the RGC topology yields higher bandwidth and lower noise than the CG topology; it also yields better performances than the S-FB TIA. However, it consumes the most power out of the three topologies because of the extra CS stage. The CG TIA also generates a higher input pole than the S-FB TIA; it consumes significantly less power than the other two topologies as well.

Table 2.1: Performance comparison of the topologies.

	CG TIA	**RGC TIA**	**S-FB TIA**
Transimpedance Gain	48 dBΩ	48 dBΩ	48 dBΩ
Input Pole Frequency	41 GHz	46 GHz	34 GHz
Input Referred Noise Density	12.33 pA/$\sqrt{Hz}$	12.04 pA/$\sqrt{Hz}$	12.33 pA/$\sqrt{Hz}$
Power Consumption	1.2 mW	2.8 mW	2.5 mW

2.3 Proposed TIA Design

As explored in section 2.2, the input pole of the first stage can be extended using various techniques such that it does not become the dominant pole of the entire TIA. However, the output pole of that stage still remains fairly limited and therefore needs to be extended in the subsequent stages without sacrificing the gain and SNR performance.

Photodiode works in the principle of generating electron-hole pairs through absorption of photons followed by their conversion into photocurrents in presence of junction electric field. At higher optical signal strength, the photocurrent density shows saturation effects due to space charge

limitations. The photocurrent saturation effect in a PD negatively impacts its responsivity. Saturation level of a PD can be increased by increasing the surface area, but increases in surface area increases junction capacitance thereby reducing input pole of the receiver. To overcome the saturation effect and maintain large responsivity while optimizing the junction capacitance, optical signal can be split into multiple PDs and then the signal can be added to form the combined response [42-45].

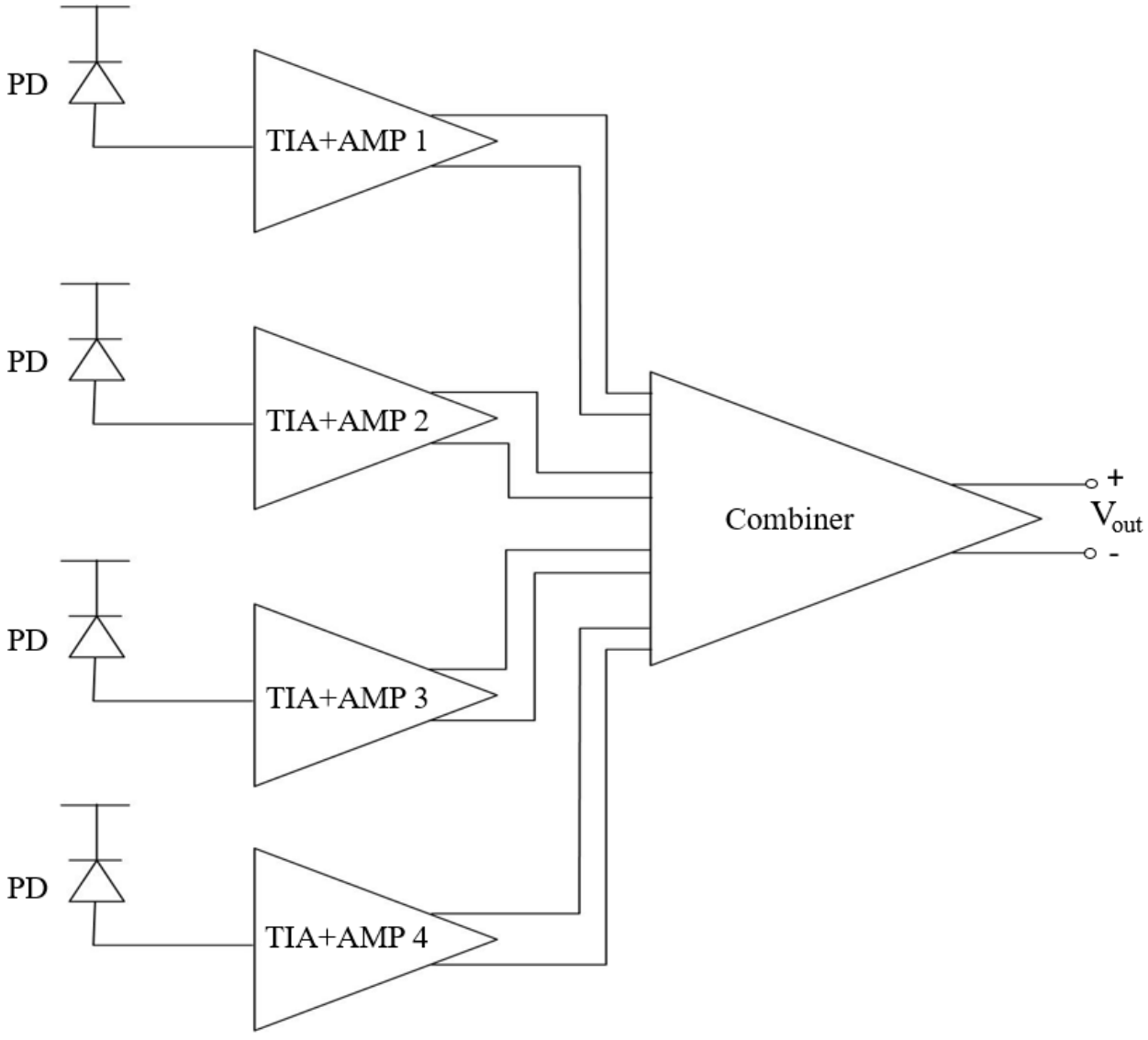


Figure 2.12: Architecture of proposed TIA design.

In this work, a receiver system consisting of four PDs is proposed. Signal from the original optical fiber can be split four-ways through beam splitters to feed the signal to an array of four PDs. This would allow higher effective responsivity without increasing the PD capacitance. The proposed TIA design has four identical TIA plus amplifier (TIA + AMP) units with differential outputs, which are then accumulated using a combiner unit as shown in Figure 2.12. The bandwidth is extended in each of the four TIA + AMP units; the gain and bandwidth are then further enhanced

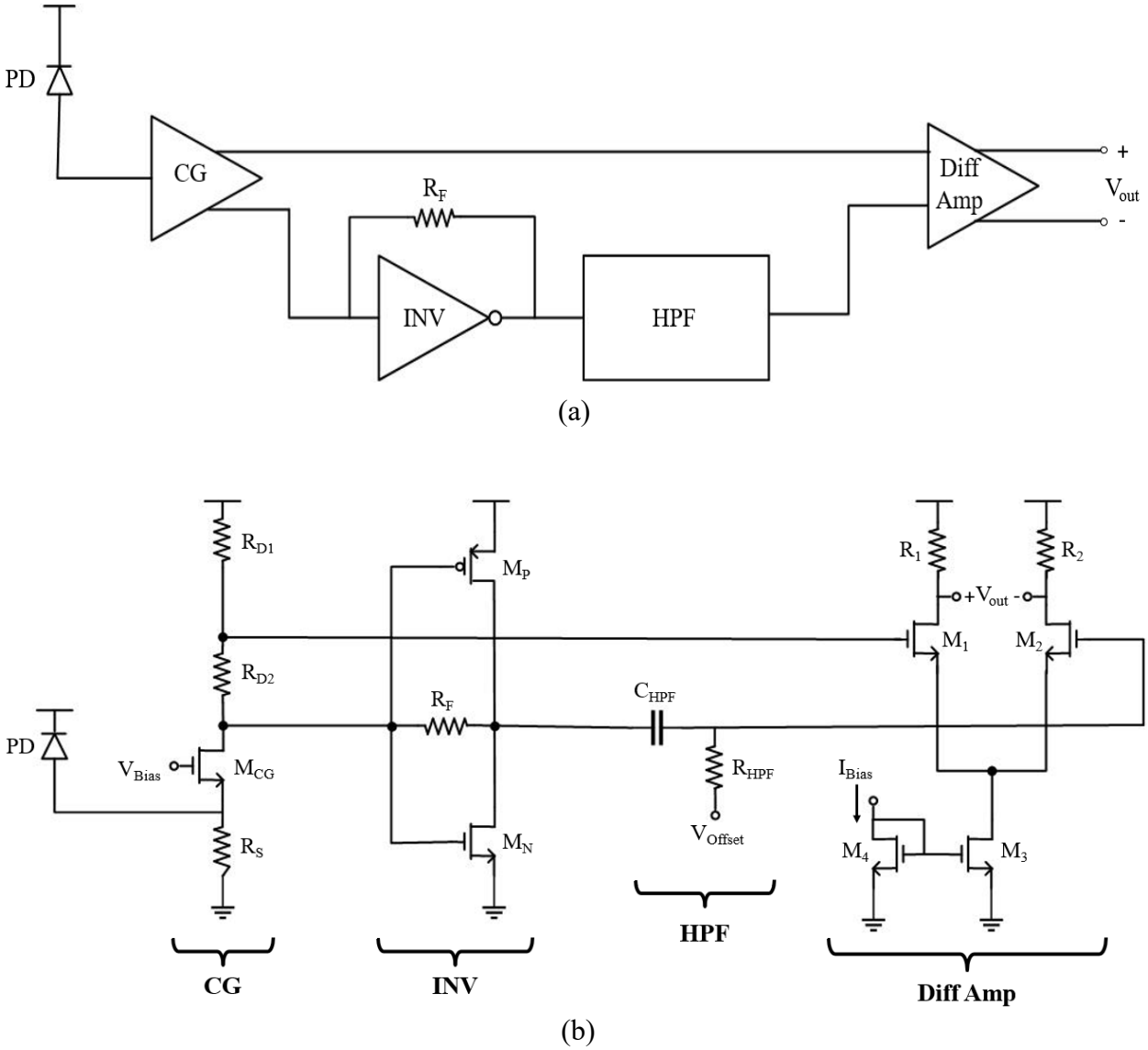
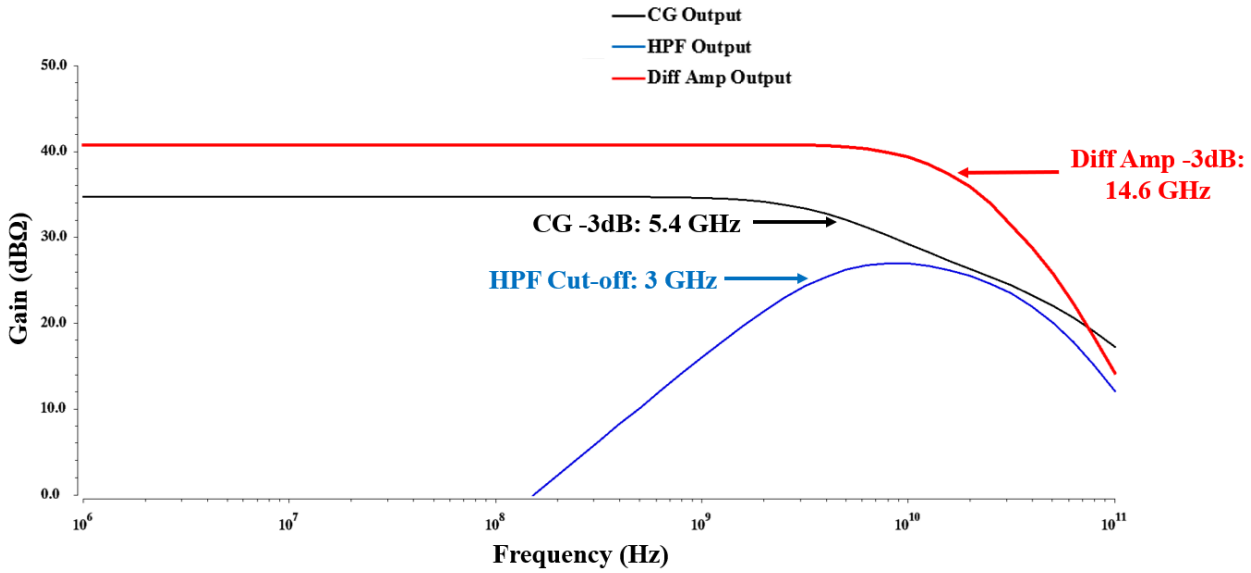


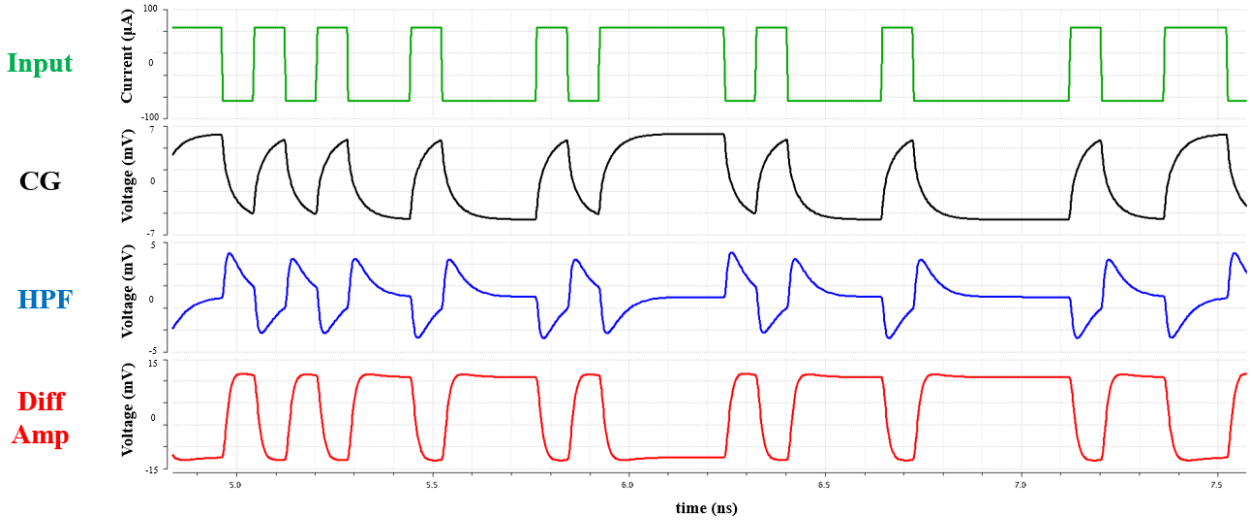
Figure 2.13: (a) Architecture and (b) schematic of the TIA + AMP unit.

in the combiner unit. Having this architecture with four PDs also enhances the SNR value as the signal increases linearly when accumulated at the combiner unit while the noise increases as RMS.

The architecture and schematic of the individual TIA + AMP units is shown in Figure 2.13. As illustrated in Figure 2.13, two outputs are taken from the CG stage, one of which is inverted by



(a)



(b)

Figure 2.14: Bandwidth extension illustration in (a) frequency domain and (b) time domain.

feeding it through a CMOS inverter with negative feedback. The inverted signal is then passed though a high pass filter (HPF). The high pass filter is designed such that the cut off frequency is around the same as the 3dB output pole frequency of the CG stage. The positive CG output signal and the inverted signal from the HPF are fed to the differential amplifier. When the differential amplifier subtracts the two signals, the signal remains unaffected from 0 Hz to the CG pole frequency since the cut off frequency of the HPF is the same as the 3dB pole frequency of the CG output. However, after the 3dB pole frequency, when the CG output signal starts attenuating, the inverted signal from the HPF comes in effect. As a result, when subtracting the two signals, the signal becomes amplified after the 3dB pole frequency. This causes the bandwidth to extend at the output of the differential amplifier. This bandwidth extension technique is shown in Figure 2.14; Figure 2.14(a) illustrates it in the frequency domain and Figure 2.14(b) illustrates it through transient waveforms. As shown in Figure 2.14(a), the output pole frequency of the CG stage is 5.4 GHz and the HPF has a cut off frequency of 3 GHz; therefore, when the two signals are subtracted by the differential amplifier, the bandwidth gets extended to 14.6 GHz. In Figure 2.14(b), it can be seen that when the input signal frequency is increased, the CG output signal starts to get distorted. However, the HPF output signal has higher magnitudes at those high frequency regions. Therefore, the subtracted signal at the differential amplifier output recovers the distorted signal. Figure 2.15 shows the PAM4 eye diagrams of the CG output signal and the differential amplifier output signal at 33 Gb/s data rate. As expected, the eye diagram improves significantly once passed through the differential amplifier.

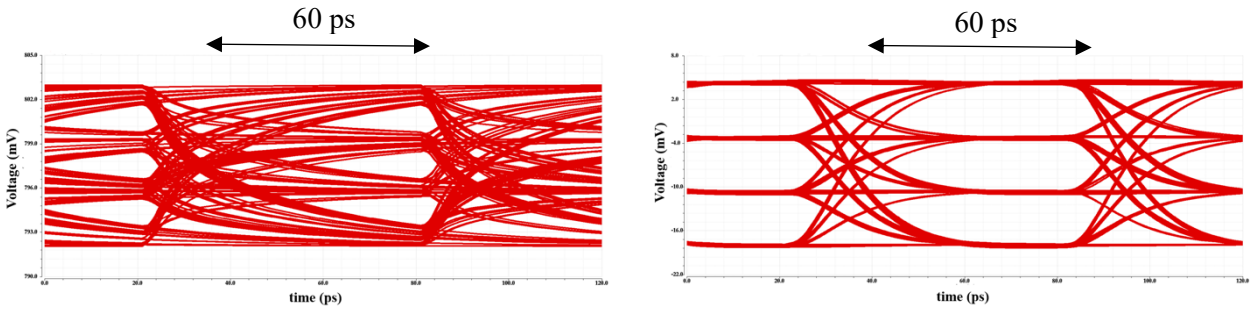


Figure 2.15: Eye diagrams of output signals of (a) CG stage and (b) diff amp stage at 33 Gb/s

The gain and bandwidth are further extended in the combiner unit. As shown in Figure 2.16, the combiner unit consists of four differential pairs, the drain nodes of which are connected together; this sums up the signals from the four differential pairs at the drain nodes. The inputs of the differential pairs are connected to the differential outputs of the TIA + AMP units, which increases the gain by a factor of four. M_{17} and M_{18} are used as dummy devices to reduce the capacitance at the output node. Shunt inductor peaking is employed to enhance the bandwidth; a symmetric inductor is used in order to save area and increase the quality factor of the inductor. This stage enhances the gain and bandwidth to 55.3 dBΩ and 32 GHz.

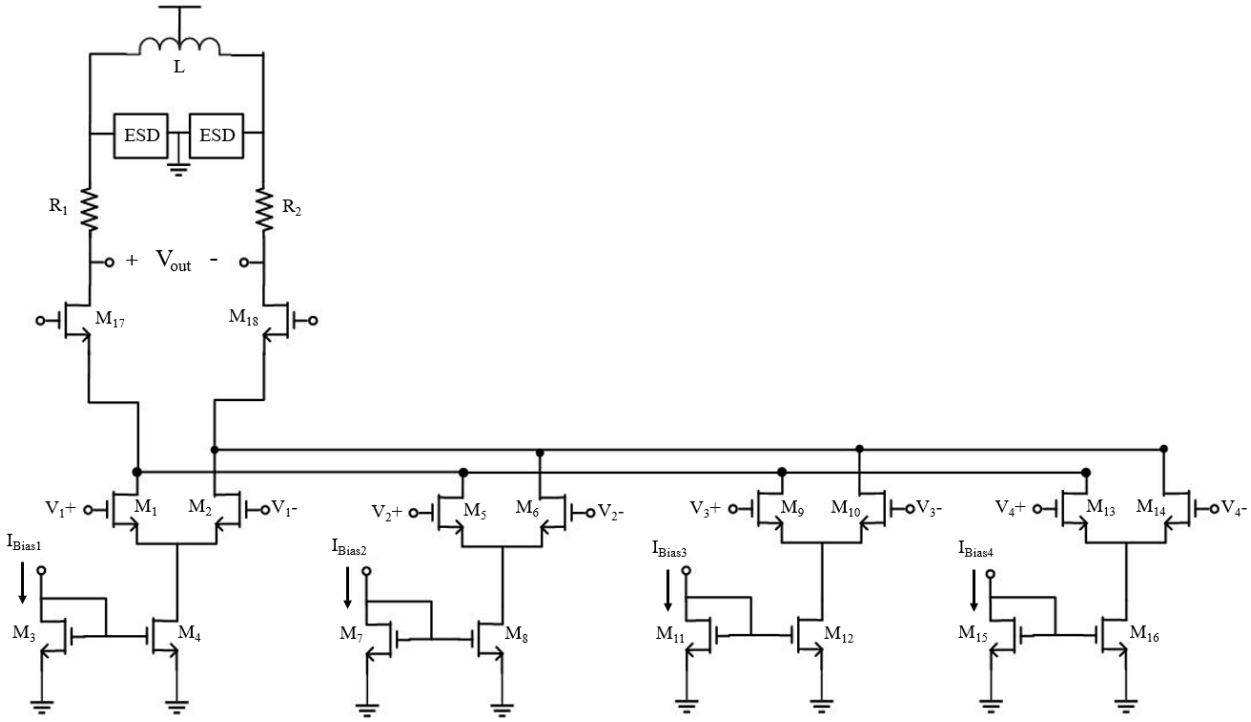


Figure 2.16: Schematic of the Combiner

2.4 Implementation and Results

The TIA is implemented in ST 28-nm FDSOI CMOS technology as shown in Figure 2.17. The chip contains probe pads in order to allow for probe testing as it yields better results. The TIA design consumes 200 μm X 300 μm area. As illustrated in the figure, the inductor consumes majority of the area; using a symmetry inductor allows us to use one inductor instead of two, therefore saving significant amount of space.

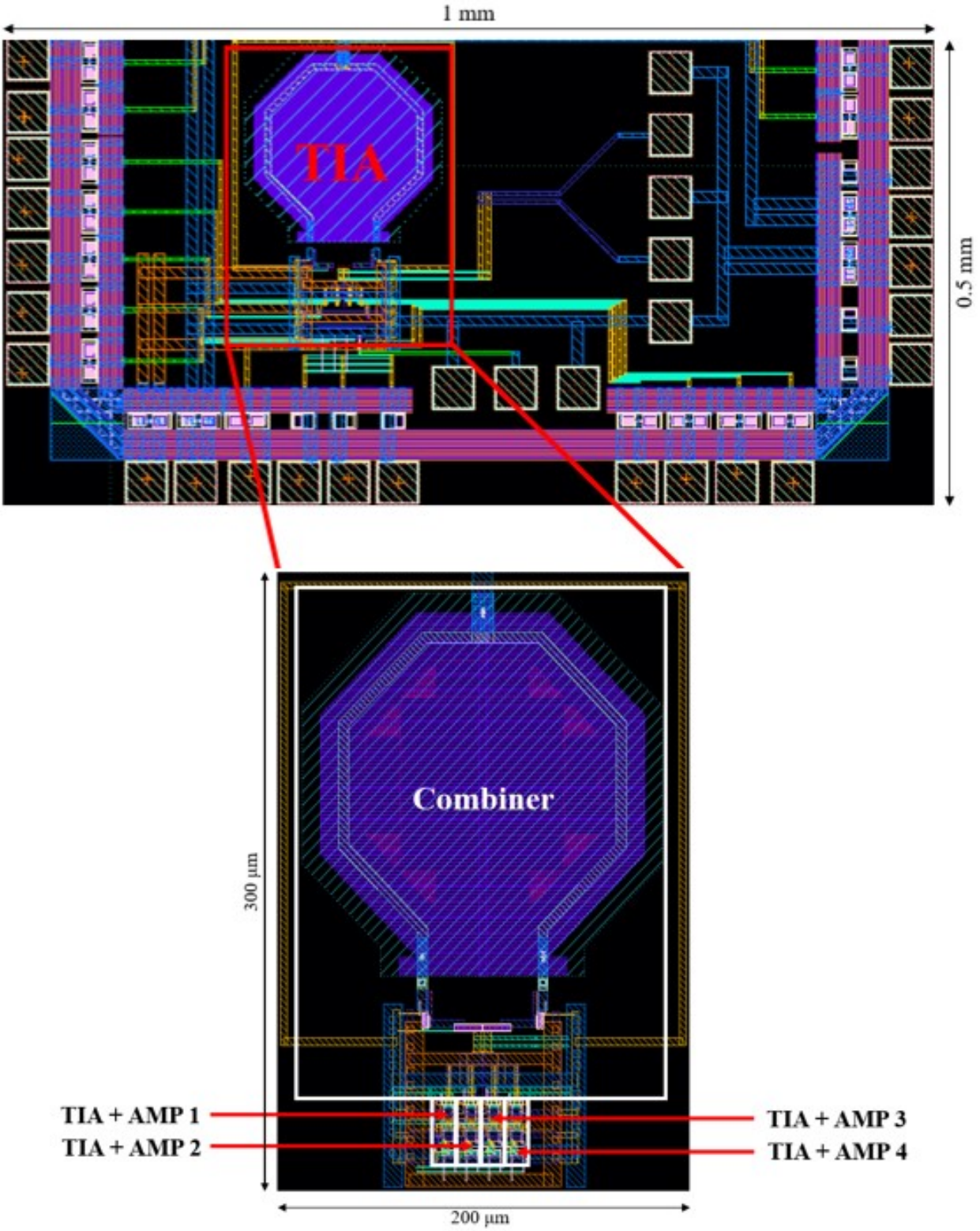


Figure 2.17: Implemented TIA in 28nm FDSOI CMOS technology.

The eye diagrams for this work were generated using PRBS31 pattern input current signal with 200 µA peak-to-peak amplitude. The circuit simulation and post-layout PAM4 eye diagrams at various data rates are shown in Figures 2.18 and 2.19, respectively. The eye diagrams achieve peak-to-peak amplitude of 130 mV; as illustrated in Figure 2.18, this design can operate at 100Gb/s data rate.

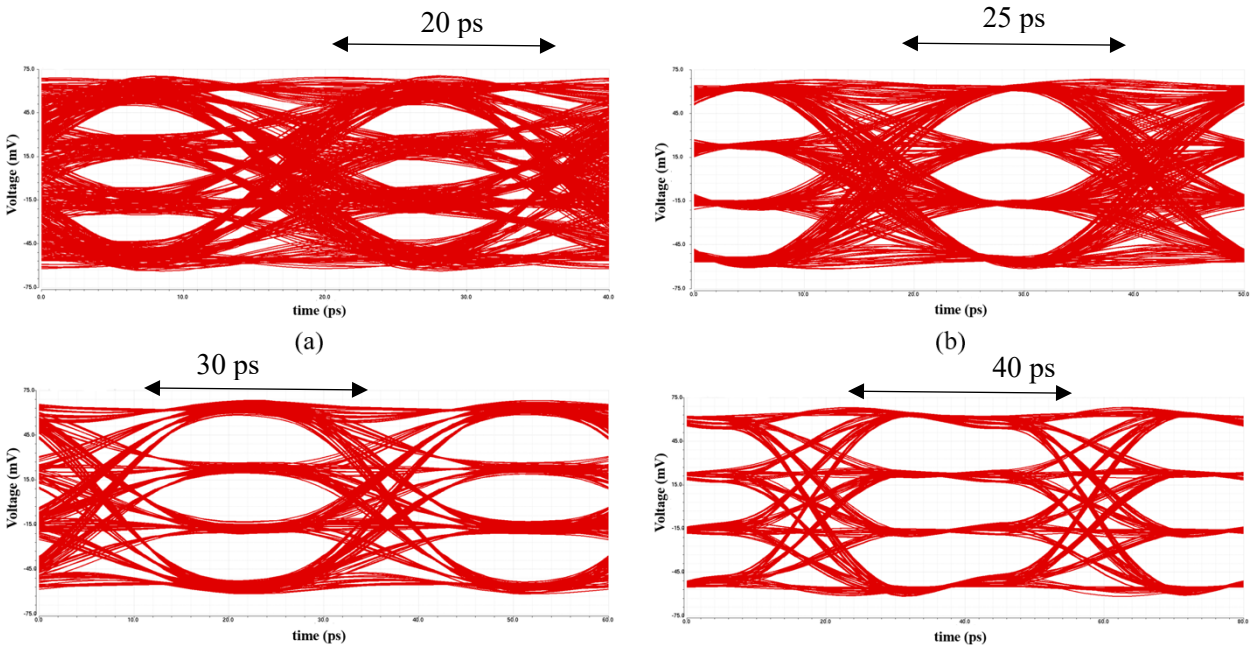


Figure 2.18: Simulated PAM4 eye diagram with data-rate of (a) 100 Gb/s, (b) 80 Gb/s, (c) 67 Gb/s, and (d) 50 Gb/s.

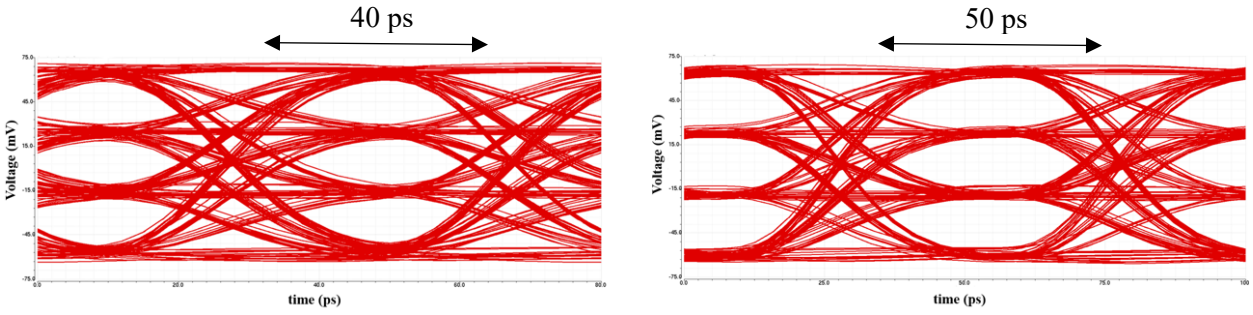


Figure 2.19: Post-layout PAM4 eye diagram with data-rate of (a) 50 Gb/s and (b) 40 Gb/s.

The simulations for this work were done using photodiode capacitance of 100fF. This design achieves a transimpedance gain of 55 dBΩ and 3dB bandwidth of 32 GHz while generating 25 $pA/\sqrt{Hz}$ average input referred noise density. It consumes 101 mW power at 100 Gb/s data rate. The performance of the proposed design is compared to other TIA designs with similar gain and bandwidth in Table 2.2. The other designs in the table – [46] [47] [49] – require multiple inductors to achieve similar gain and bandwidth performance; as a result, they consume significantly more area. The proposed design yields a significantly better Figure of Merit (FoM) – which takes gain, bandwidth, power, noise, and area into consideration – compared to the other designs.

Table 2.2: Performance of the proposed TIA design.

Specification	**[46]**	**[47]**	**[48]**	**[49]**	**This Work**
C_{PD} (fF)	50	50	300	–	100
Gain (dBΩ)	50	51	54	60	55
Bandwidth (GHz)	29	30.5	28	22	32
Power (mW)	45.7	60.1	110	75	101
Average Input Referred Noise Density ($pA/\sqrt{Hz}$)	51.8	55.7	36.5	22	25
Active Area (mm^2)	0.4	0.54	0.07	0.56	0.06
FoM $\left(\frac{dB\Omega \cdot GHz}{mW \cdot mm^2 \cdot pA/\sqrt{Hz}}\right)$	1.53	0.86	5.38	1.43	11.62

Chapter 3

ISI Equalizer for High-Speed Communication

3.1 Introduction

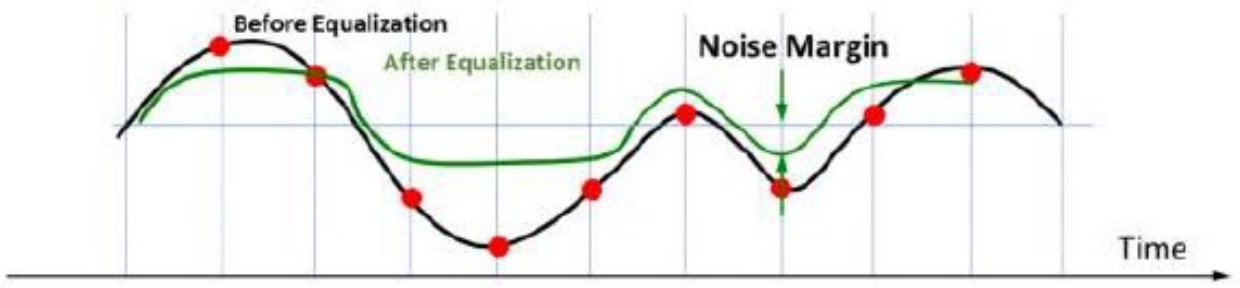
Vast expansion of IoT and recent introduction of the AI usage at the edge of the IoT has created additional bandwidth demand in data centers. Use of optical fibers has become a solution to meet the high bandwidth demand. Higher data rate is associated with the increased channel loss. This frequency dependent loss manifests itself in the form of inter-symbol-interference also known as ISI. In simple words, ISI is the spreading of the symbol on its neighboring symbols. Usually an equalization technique is employed at the receiver to correct the frequency dependant interference, i.e., to remove or reduce all of the ISI components from the received signal. The ISI is generally data dependent and can include signal components with contributions based on prior (pre-cursor) and post (post-cursor) received signals. Various techniques exist, both in the literature and practice, to address pre-cursor and post-cursor ISI known as equalization. From implementation point of view, we can partition the equalization functionality on both transmitter and receiver (TxRx-eq) or only on the receiver side (Rx-eq). To adapt the transmitter side equalizer tap values, we often need the information about the quality of the eye or link margin that are available at the sampler input on the receiver side. Therefore, TxRx-eq requires a back channel and link wakeup protocol that are often part of the standard. A more desirable solution is receiver only equalization that also provides flexibility to the equipment manufacturer to use IPs from different vendors without requiring compatibility. Fortunately, latest trend in ADC based solutions does provide that flexibility [17]-[39].

This chapter first reviews the symbol vs sequence decoding in section 3.2. Section 3.3 describes the hardware challenges associated with Maximum Likelihood Sequence Detector (MLSD) implementation. Section 3.4 introduces the proposed sequence decoder followed by implementation and measured results in section 3.5.

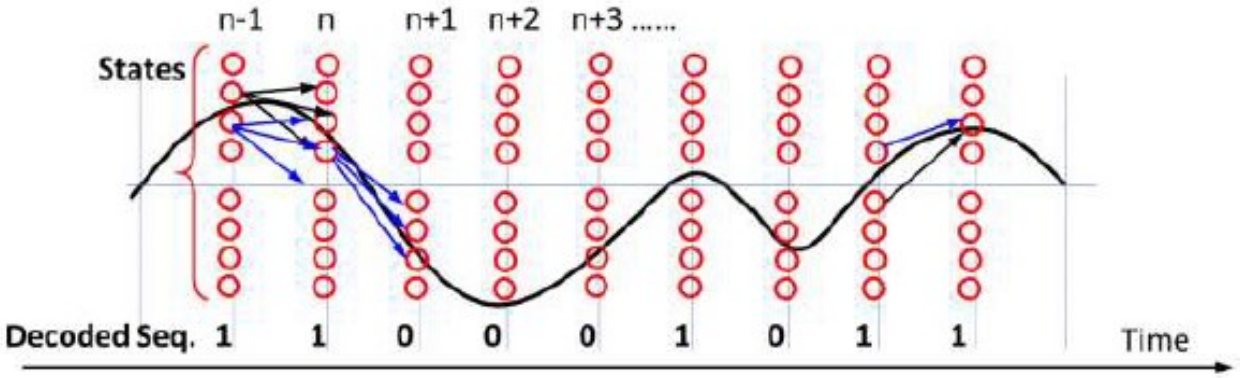
3.2 Symbol Vs Sequence Detection

Fundamentally, the two main approaches to equalization can be classified as symbol detection and sequence detection. In symbol detection, each symbol decision is made after correcting and compensating the ISI effect of neighboring symbols. While, subtracting the ISI, the received signal amplitude also experiences significant attenuation causing degradation in SNR. A simple example shown in Figure 3.1(a) explains the SNR degradation from the trellis diagram. After equalizing the received signal, equalized '1' and '0' comes very close to the threshold. An alternative approach to equalization is to consider the entire sequence instead of a symbol. Therefore, instead of cancelling the ISI we compare the received signals to different ISI combinations, referred to in this chapter as constellation. Each received sample value, r_K, can be compared to the constellation points defined as $\sum_{X=1}^{N} S_X h_X$. Here, h is the impulse response of the channel and S is the transmitted symbol and N reflects number of taps in the channel impulse response function. Ideally in a noise less case, received sample would fall on one of those constellation points. But in the presence of 'noise' and residue ISI, received samples are deviated from those constellation points as shown in Fig. 3.1(b). This deviation is measured as branch metrics (BM).

$$b_L(K) = \left| r_K - \sum_{X=1}^{N} S_X h_X \right|^2 \qquad 3.1$$



(a)



(b)

Figure 3.1: Two different approach to equalization (a) Symbol by Symbol detection (b) Sequence Detection.

Such branch matrices are calculated for different trellises and accumulated over an entire sequence:

$$e(K) = e(K-1) + b_L(K) \tag{3.2}$$

Once the accumulated errors are computed, we can calculate and compare relative likelihood of each sequence, $e_i \geq e_j$. Usually, this comparison is done once the trellis converges to a unique state. By successively comparing all possibilities we can select the one that has the lowest accumulated error. In simple words, most likely sequence is the one that has the least mean square error and therefore, decoding based on this algorithm is known as Maximum Likelihood Sequence Detector (MLSD). The main advantages of such decoding process are first, uncorrelated random noise has less impact on the accumulated error compared to single symbol detection. Second, ISI

is used in a constructive way and therefore, we do not need to pay the penalty for amplitude reduction. Both factors contribute to the SNR benefits that is often advertised. Practical implementation of this decoding is computationally intensive. Therefore, a simplified version, known as Viterbi algorithm, is often implemented [16][40][41][50][51].

3.3 Hardware Challenges in MLSD Implementation

The algorithm described in the previous section is usually implemented using an analog to digital converter (ADC), in which the signal is converted to digital domain and then the distance from the received signal to the constellation points are calculated described as BM in the previous section. A major challenge in this approach is that the power consumption is very high because of the ADC and also because of the digital computations, e.g., the computation of distance to each constellation point, and then the computation required to determine the minimum distance in a set of distances. In addition, the quantization error of the ADC affects the signal-to-noise ratio (SNR) and minimum achievable bit-error-rate (BER). Therefore, to reduce the complexity, we often limit the possibilities by retaining the two most likely transitions as described in Viterbi implementations [40] [41].

Finding the two survivors requires one to accumulate the path metric and then compare to select. These add-compare-select (ACS) units have an inherent feedback that is difficult to close at higher speed. Several techniques have been explored in literature to overcome the computational and highspeed challenge associated with the Viterbi decoding. First, note that complexity of the Viterbi decoder increases exponentially with number of states. By adopting feedforward equalization (FFE) we can limit the residue ISI and make Viterbi decoder more affordable [40], but the power

efficiency still greatly exceeds the 10 pJ/bit target. Computational efficiency can be improved by moving the ACS unit in analog domain as suggested in [50] taking advantage of superior analog performance offered by BiCMOS process. However, analog performance in nano-meter CMOS limits the adaptation of such techniques. While the digital implementation scales more gracefully with technology, full blown implementation still consumes prohibitive power [41]. Therefore, more practical implementations use several simplifications. First, the absolute value instead of the square in equation (3.1) still provides reasonable results without significant performance penalty. Pre-computing of the path metric to parallel process the ACS operation also relaxes the performance as described in [16]. Finally, combining the above techniques with reduced state and resolution has achieved higher speed [51]. However, it is not clear with these simplifications how much performance benefit remains in sequence decoding over symbol detection. Therefore, most popular ADC based solutions still remains FFE-DFE based [17] [39].

3.4 Analog to Sequence Based Maximum A Posteriori (MAP) Decoder

Similar to the Viterbi decoder, computational complexity of the MAP decoder often resorted to analog-mixed signal processing [52]. In this work we are proposing Analog to Sequence Converter (ASC) based MAP decoding that provides several advantages over Viterbi decoding. In contrast to flash type ADCs, the comparator thresholds are not uniformly spread out in the voltage range. Instead, the comparator thresholds are strategically set based on different combinations of the main (h_0), pre-cursor (h_{-1}) and post-cursors (h_{+1}) components. Specifically, these thresholds are chosen so that the entire signal space is subdivided into a set of regions. Front-end linear equalizer response is chosen such that at the output the ISI should be limited to 4 taps only. Therefore, there

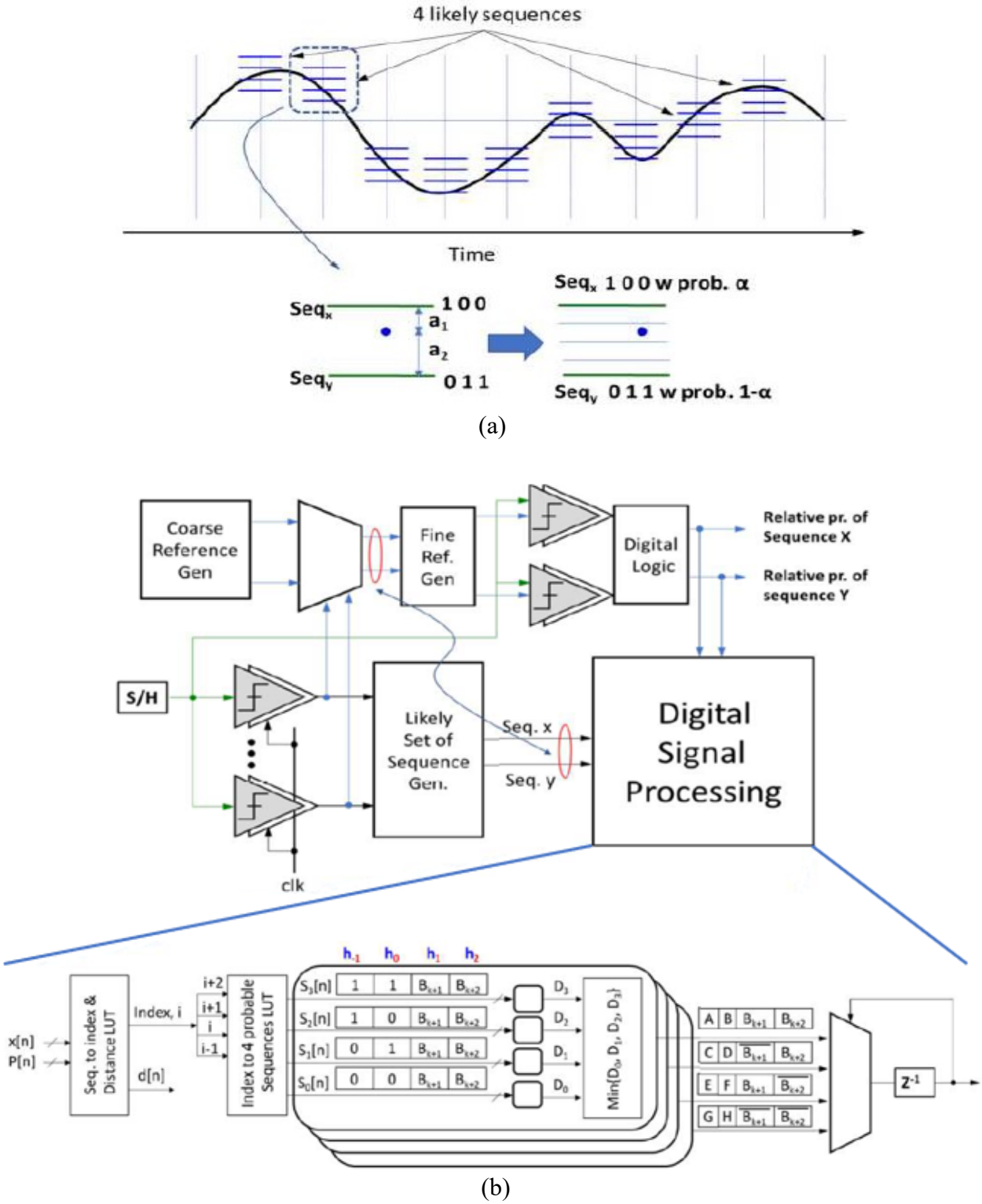


Figure 3.2: Analog to sequence converter based MAP decoder implementation. (a) The conceptual decoding process. (b) The Analog to sequence hardware and the MAP decoding digital signal processing (DSP) hardware.

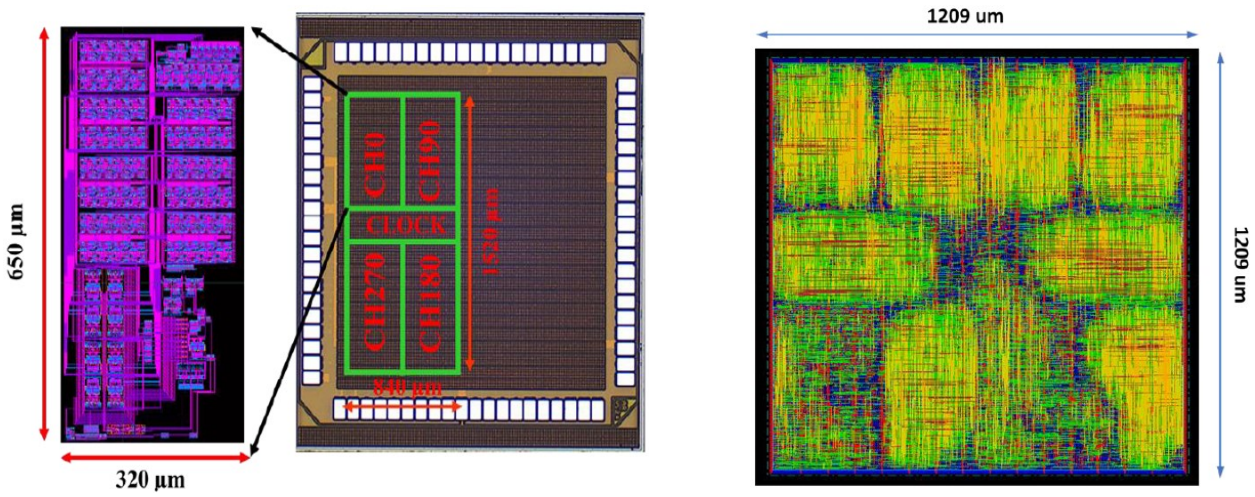
are 16 possible sequences:

$$Seq_{0\rightarrow 15} = \pm h_0 \ \pm h_1 \ \pm h_{-1} \ \pm h_2 \tag{3.3}$$

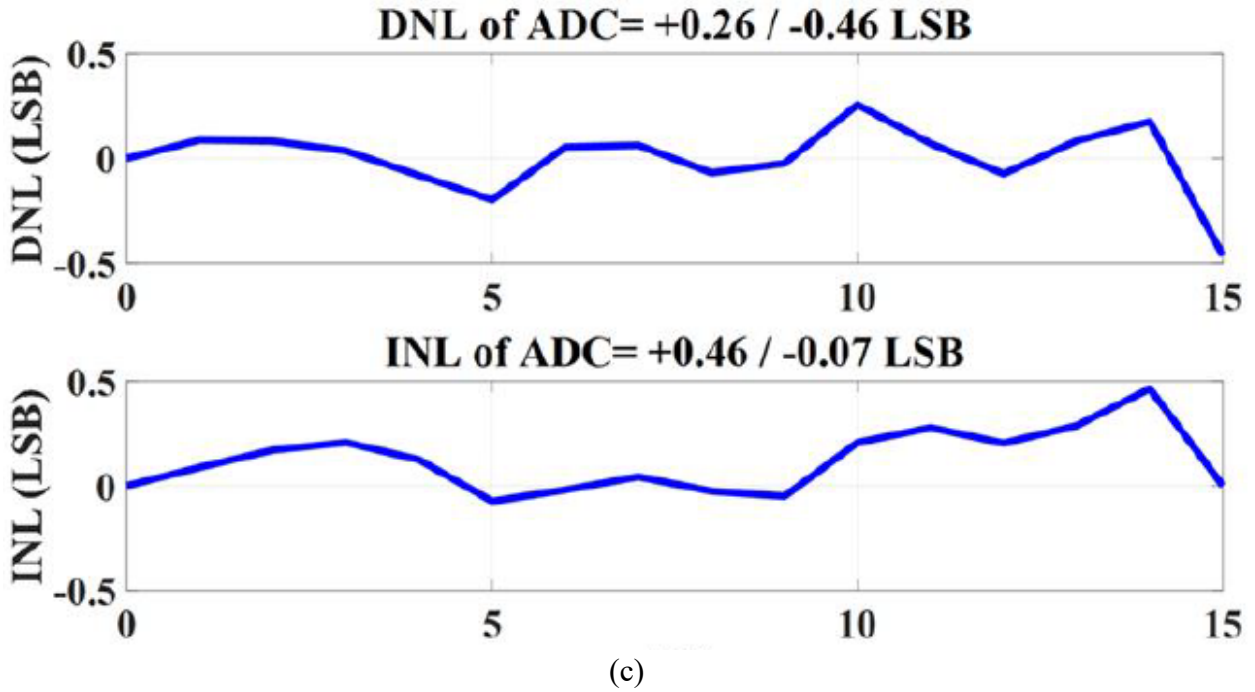
16 References are then calculated based on consecutive sequences:

$$Vth_i = \frac{Seq_i + Seq_{i+1}}{2} \tag{3.4}$$

Based on the comparator outputs, received signal is then mapped to the signal space. Non-binary relationship between the tap values translate to nonuniform separation and stresses the resolution requirement of the comparators in addition to comparator offset. But unlike ADC the comparator output does not directly translate to the multi-bit digital value. Instead, these comparator values are mapped to a set of possible sequences. From this set of possible sequences, the most likely sequence is selected based on likelihood as well as the previously decoded symbols. Therefore, single comparator error is often tolerable and does not translate to symbol error. The conversion process works in two steps - at first, we find the set of sequences that are closest to the received sample and then we place comparators with fine resolution to measure the distance between the received sample to the sequences (Figure 3.2). In other words, Analog to sequence converter find the list of the sequences in ascending order and also quantifies how likely these sequences are. Therefore, we can directly estimate the probability of each sequence, no digital processing is needed. This advantage in the computational efficiency allows for a different sequence decoding algorithm. The proposed sequence selection process works as follows: for an N-tap channel we consider N consecutive UI for decoding. Assuming we have *L* pre-cursors and *M* post cursors, $N = L + M + 1$. After decoding 4 likely sequences, for each sequence, we calculate the probability of L previous and M following compatible sequences. Then we calculate the combined



(a) (b)



(c)

Figure 3.3: Implemented prototype in 0.13 um CMOS (a) Analog to sequence converter die photo, (b) synthesized DSP, and (c) INL/DNL of the analog to sequence converter.

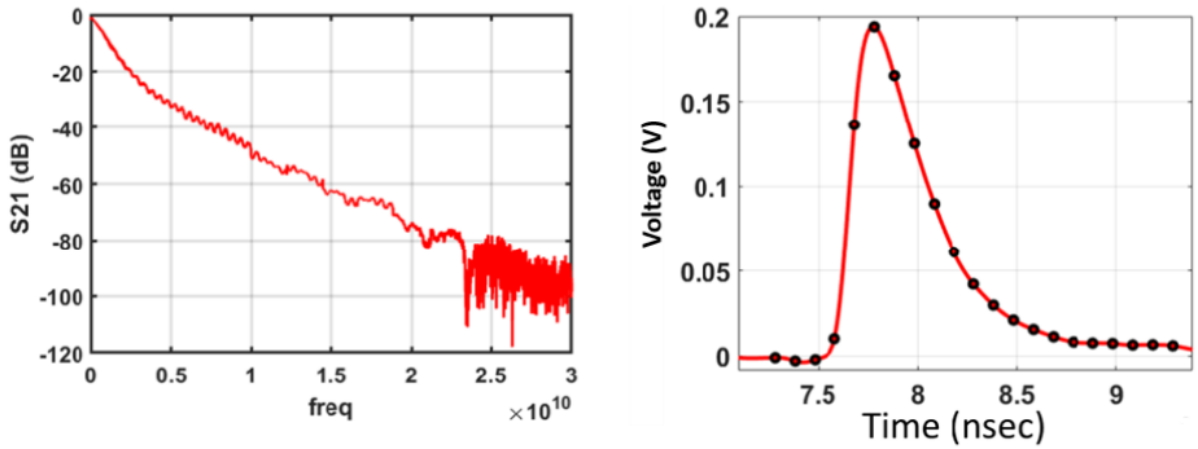
probability by scaling them with the corresponding tap weight.

$$P_K = \frac{\sum_{i=-1}^{-L} \frac{h_i}{d_i} + \frac{h_0}{d_0} + \sum_{i=1}^{M} \frac{h_i}{d_i}}{\sum_{n=1}^{N} h_n}, K = 1, 2 \ldots 2^{N-L} \quad 3.5$$

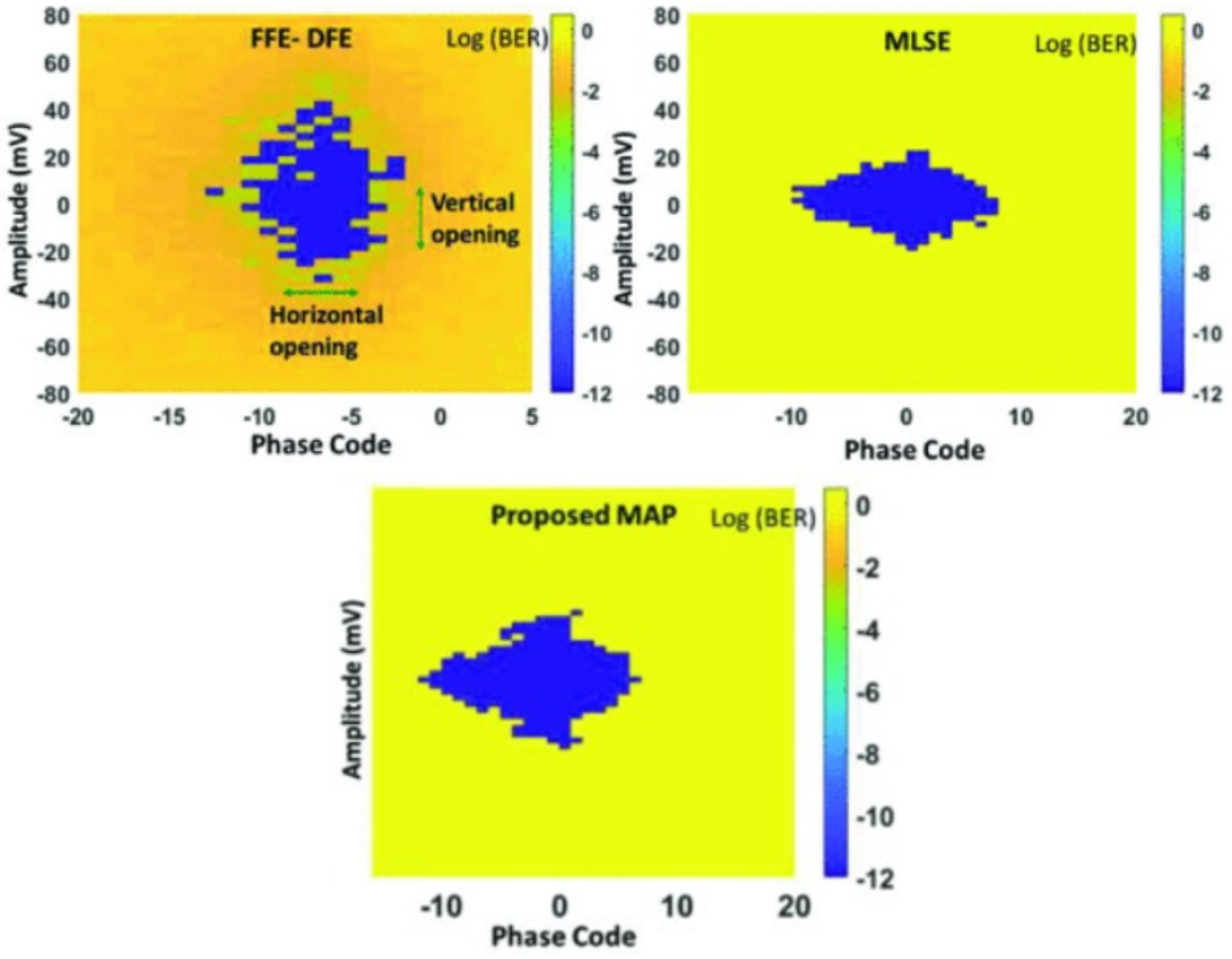
Here we are selecting 2^{N-L} number of sequences based on how likely these sequences are. Final sequence is selected based on M previous decision as shown in Figure 3.2. Note that the distances, d_i, are directly calculated and then scaled by the tap weight, h_i. Therefore, this computation can be most efficiently executed using lookup table. Also, the denominator is common when comparing the probability for different sequences, therefore can be ignored for comparison purpose. Note that the distance between sequences are known based on the tap values. Therefore, these distances are stored with 6-bit resolution. 1.5 bit probability quantization effectively translates to scale 6-bit distance vector into two distance vectors. This significantly improves the resolution without increasing analog to sequence converter power.

3.5 Implementation and Performance Comparison

For proof of concept a prototype is implemented in 0.13 μm CMOS. Analog to sequence converter is implemented in custom integrated circuit whereas the MAP algorithm is tested using FPGA (Figure 3.3). For realistic estimation of power and area, synthesized layout is shown in Figure 3.3(b). We compared the performance of this sequence decoding algorithm with Viterbi and conventional FFE solution for a long reach channel at 10Gb/s NRZ in Figure 3.4. To keep the complexity and power consumption within limit, we use channel shortening filter partially equalize within 4 taps. As expected, the sequence decoding algorithm outperforms the symbol detection algorithm such as FFE. Between two sequence decoding algorithms, MAP decoding outperforms Viterbi simply due



(a)



(c)

Figure 3.4: Performance comparison of the different digital equalization at 10Gb/s. (a) Frequency response and single bit response (SBR). (b) The BER plot as function of voltage and time for FFE, MLSE and proposed MAP decoding.

to the fact that we keep all four possibilities instead of truncating to two. These additional options allow us to make correct decision even in the presence of higher noise. Although computational complexity increases when we keep additional options, but accumulation is limited to 4 UI instead of longer sequence as would be needed in Viterbi. However, as the precursor value decreases, the benefit of MAP decoding also diminishes. This is consistent with the eqn. (3.5) that suggests the weighting factor of the pre-cursor term. Due to the advantage of the Analog to sequence converter it still remains affordable for the given power, area constrain and is expected to improve as we scale to advanced CMOS nodes. The performance summary of the implemented prototype is shown in Table 3.1.

Table 3.1: Performance summary of implemented prototype.

Specification	**This Work**
Architecture	4 X Flash
Technology	130nm CMOS
Supply Voltage	1.2
Sampling Rate (GS/s)	10
Resolution (bit)	4
Probability Resolution (bit)	1.5
Sampling Cap (pF)	0.250
ENOB (bit)	3.2
SNDR/SFDR @Nyquist	21/25
Power (mW)	105
FOM (pJ/Conv.-step)	1.14
Active Area (mm^2)	1.23

Chapter 5

Conclusion

5.1 Thesis Summary

Sustaining the exponentially increasing trend in functionality of integrated circuits requires high bandwidth intra-chip and inter-chip communication. However, higher speed communications inside silicon chips are often bottlenecked by capacitive drain of the channels. Therefore, as the functionalities of integrated circuits get increasingly sophisticated, achieving the required high bandwidth operations becomes increasingly challenging. Photonic integrated circuits (PIC) are considered as a potential solution, where laser-modulator modules are used to convert electronic signals into optical signals for transmission through waveguide structures and then the signals are converted back to the electronic domain by P-I-N photodiodes in the receiving end. Apart from the emerging trends of inter and intra chip optical applications, optical signals are also utilized in optical-fiber networks to meet the high bandwidth data communications demands from data centers, communities, and businesses. In order to process the high data rate optical signals, the performance of the optical receivers must be optimized as well. The focus of this thesis was to enhance the SNR performance of optical receivers. In order to optimize the SNR performance, the gain was boosted at the Transimpedance Amplifier stage by limiting the bandwidth. Subsequently, an equalizer was utilized to equalize the inter symbol interference (ISI) caused by the bandwidth limitation.

Transimpedance Amplifiers (TIA) are the first stage of optical receivers; they convert the photocurrent from the P-I-N photodiodes to voltage signals to be processed by the subsequent stages. As they are the first stage, the performance of the TIA units is vital to the overall performance of the optical receivers. Chapter 2 of the thesis focused on enhancing the performance of TIA units. The chapter first explored and compared the performances and trade-offs of three different TIA topologies – Common Gate, Regulated Cascode, and Shunt Feedback; the transimpedance gain, bandwidth, noise, and power consumption performances were all taken into account. The chapter then proposed a TIA design that uses various techniques to enhance the transimpedance gain, bandwidth, and SNR. The design was implemented in ST 28-nm FDSOI CMOS technology; it achieved a transimpedance gain of 55 dBΩ and 3dB bandwidth of 32 GHz.

Chromatic dispersion in the optical signal being passed through the optical-fibers or waveguide structures causes inter symbol interference (ISI), which distorts the waveform. Therefore, optical receivers must also employ an ISI equalizer. There are various ISI equalization techniques; some are transmitter and receiver based (TxRx-eq) and some are only receiver based (Rx-eq). Since TxRx-eq equalizers raises transmitter-receiver compatibility concerns, Rx-eq equalizers are more desirable for manufacturers. Chapter 3 of the thesis was dedicated towards designing an optimized Rx-eq ISI equalizer. The chapter first discussed the advantages of taking the sequence detection approach over the symbol detection approach. It then discussed the benefits and challenges of different equalization techniques such as feedforward equalization (FFE), Maximum Likelihood Sequence Detector (MLSD) and Viterbi algorithm. The chapter then proposed an Analog to Sequence Converter (ASC) based Maximum A Posteriori (MAP) decoding equalizer. The concept was implemented in 0.13 μm CMOS technology. The implemented prototype is capable of

compensating 35+ dB loss at 10 Gb/s data rate with better than 10 pJ/bit energy efficiency. The work described in the chapter was published in MWSCAS 2019.

5.2 Future Work

The goal of this thesis was to propose ways to enhance the performances of optical receivers to be used at high data rates. This was done by optimizing the performances of individual units of optical receiver – chapter 2 proposed a high gain-bandwidth TIA and chapter 3 proposed an energy efficient ISI equalizer. The next step would be to combine the two designs and optimize the performance of the optical receiver as a whole. The TIA design proposed in chapter 2 uses the CG topology as the first stage; it then employs various techniques to enhance the performance in the subsequent stages. The proposed design can also be implemented using the RGC and S-FB topologies as the first stage. Also, the latest advanced process technologies such as the 10-nm finFET and 14-nm finFET provide superior performances compared to the older technologies. The designs discussed in this thesis can be implemented in the more advanced technologies, which will yield much improved performances.

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