Open-Source Radiation Testing Apparatus and
Electrical Power Supply Design for CubeSat Missions

by

Stefan Eric Damkjar

A thesis submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

in

Integrated Circuits and Systems

Department of Electrical and Computer Engineering
University of Alberta

Abstract

The continuing miniaturization of computing technology and the increasing popularity of CubeSats among a growing market of modest-budget developers have revolutionized the space industry by enabling cost-effective access to space. However, ensuring reliability remains a paramount concern. This thesis describes research that addresses two critical reliability drivers for CubeSat missions: radiation effects and power system design.

Characterizing the sensitivity of commercial off-the-shelf (COTS) components to ionizing radiation can be challenging for inexperienced CubeSat developers. To bridge this gap, an open-source, versatile radiation testing platform is investigated and implemented. This automated platform leverages a modular design, allowing rapid testing of up to 24 devices in a particle accelerator beamline during a single testing session, thereby enhancing data collection efficiency and lowering costs. Experimental results demonstrate the feasibility of this approach for estimating error rates in low Earth orbit.

On any spacecraft, the Electrical Power Supply (EPS) is a mission-critical subsystem, and its reliability is crucial. An innovative open-source EPS design is proposed with fault tolerance features and novel attributes including adaptive single-event latchup detection, a battery charge inhibit scheme for low temperatures, and a power-saving

control scheme. A complete hardware prototype is built and tested, demonstrating promising efficiency, fault tolerance, and overall functionality, that matches or exceeds the performance of COTS EPSs.

Both the software and hardware for both projects are intended to be open-source, contributing to the CubeSat community by providing accessible design resources for enhancing reliability. By offering economical radiation testing and an adaptable and feature-rich EPS solution, the result of this research project should accelerate the development of cost-effective CubeSat missions, empowering researchers to focus on mission-specific scientific payloads and novel contributions to space exploration.

Preface

Chapter 3 of this thesis is intended to be published as S. E. Damkjar, I. R. Mann, B. F. Cockburn, and D. G. Elliott "An Automated Modular Platform for Simplified Particle-Accelerator Testing of Microelectronics." The manuscript was based entirely on my own original work, under the guidance and supervision of Professors I. R. Mann, B. F. Cockburn and D. G. Elliott

Chapter 4 of this thesis has been published as S. E. Damkjar, I. R. Mann, and D. G. Elliott "Proton-beam testing of SEU sensitivity of M430FR5989SRGCREP, EFM32GG11B820F2048, AT32UC3C0512C, and M2S010 microcontrollers in low Earth orbit," in *Proceedings of the 2020 IEEE Radiation Effects Data Workshop (in conjunction with 2020 NSREC)*, 2020, pp. 1–5. The manuscript was based entirely on my own original work, under the guidance and supervision of Professors I. R. Mann and D. G. Elliott

Chapter 7 of this thesis is intended to be published as S. E. Damkjar, B. F. Cockburn, and D. G. Elliott "Open-Source CubeSat Electrical Power Supply." The manuscript was based entirely on my own original work, under the guidance and supervision of Professors B. F. Cockburn and D. G. Elliott

Appendix B has been published as S. E. Damkjar, "openRadiationTesting: Preliminary Release," Aug. 2023. [Online]. Available: https://doi.org/10.5281/zenodo.8260186, licensed under Apache License 2.0 (https://www.apache.org/licenses/LICENSE-2.0).

Appendix C and D have been published as S. E. Damkjar, "openEPS: Preliminary Release," Aug. 2023. [Online]. Available: https://doi.org/10.5281/zenodo.8253813, licensed under Apache License 2.0 (https://www.apache.org/licenses/LICENSE-2.0).

All other parts of this thesis are the original work of Stefan Damkjar, and have not been previously published.

Acknowledgments

I would like to express my deepest gratitude to the many individuals and organizations who have played a significant role in the completion of my doctoral thesis

I am immensely thankful to my supervisors, Dr. Duncan Elliott, Dr. Bruce Cockburn and Dr. Ian Mann for their guidance throughout the research process. I'm also grateful to the AlbertaSat team as well as my fellow researchers, including Junqzhi Zhu, Brendan Bruner, Jorge Marin and Dr. David Miles for their support and encouragement of my work over the years.

I would also like to thank the Faculty of Engineering, the Department of Electrical and Computer Engineering and the Department of Physics at the University of Alberta, the Canadian Space Agency, the Natural Sciences and Engineering Research Council of Canada and CMC Microsystems for supporting this research.

I am enormously grateful of my family and loved ones for their patience and support without which I could not have achieved this milestone.

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List of Acronyms

BL2C TRIUMF Beamline 2C

CANbus Controller Area Network Bus

CMOS Complementary Metal-Oxide-Semiconductor

COTS Commercial Off-the-Shelf

CRC Cyclic Redundancy Check

DAC Digital-to-Analog Converter

DUT Device Under Test

FWHM Full-Width Half-Maximum

GCR Galactic Cosmic Rays

GPS Global Positioning System

I2C Inter-Integrated Circuit

IC Integrated Circuit

ISS International Space Station

LEO   Low Earth Orbit

LEP   Low-Energy Proton

LET   Linear Energy Transfer

LIB   Lithium-Ion Batteries

LSB   Least-Significant Bit

LTAN Local-Time of the Ascending Node

MCU Microcontroller

MPPT Maximum Power Point Tracking

MPSoC Microprocessor System-on-a-Chip

MTBF Mean Time Between Failures

NRCSD NanoRacks CubeSat Deployer

OOSR On-orbit Single Event Upset Rate

RBF   Remove-Before-Flight

RTC   Real-Time Clock

SCR   Silicon-Controlled Rectifier

SEB   Single-Event Burnout

SEE   Single-Event Effects

SEFI Single-Event Functional Interrupt

SEGR Single-Event Gate Rupture

SEL Single-Event Latch-up

SET Single-Event Transient

SEU Single-Event Upset

SPENVIS Space Environment, Effects, and Education System

SPI Serial Peripheral Interface

SRAM Static Random-Access Memory

SRIM The Stopping and Range of Ions in Matter

STK Systems Tool Kit

TID Total Ionizing Dose

TRIUMF TRI-University Meson Facility

TRIUMF TRI-University Meson Facility

TRL Technology Readiness Level

U One 10×10×10 cm CubeSat Volume Unit

1. Introduction

1.1. Thesis Overview

This thesis investigates two of the leading reliability drivers for spacecraft developers: radiations effects and power system design.

Radiation Effects   Traditionally, spacecraft have used purpose-built radiation hardened computing technology to mitigate faults caused by ionizing radiation. Unfortunately such "space grade" components are prohibitively expensive for most university CubeSat projects. The alternative approach, proposed in [15], is to use standard *commercial off-the-shelf* (COTS) components, with critical components having had some assessment of vulnerability to radiation. However, meaningful characterization of radiation sensitivity for modern devices is complicated and costly for inexperienced developers, such as university groups building their first CubeSat. In this work, an automated and versatile open-source device testing platform is proposed, implemented, and tested. The testing platform is intended to provide an efficient tool for placing the *device under test* (DUT) in a particle accelerator beam and log meaningful test data that can used to access reliability in orbit. The testing platform is intended for either discrete components, such as microcontrollers, or entire CubeSat subsystems. One of

the primary design considerations is efficiency of testing, to get the most radiation sensitivity data out of the necessarily limited testing time.

The contributions of this work are:

- Development of an innovative, modular, and open-source testing platform designed for characterizing radiation sensitivity in electronic components or systems used in intense radiation environments.

- A modular design that improves versatility and simplifies the preparation of devices for testing.

- Automated DUT swapping allowing rapid testing of up to 24 devices without the need for human intervention in the radiation test chamber.

- A testing platform tailored to the specific challenges faced by CubeSat developers, including budget constraints and the need for rapid development cycles

- Release of software and hardware design files under an open-source license, aiming to alleviate trial-and-error challenges faced by CubeSat developers during radiation testing, ultimately simplifying the process of designing more reliable and cost-effective spacecraft components

- A discussion of low-energy proton effects and testing strategies including detailed simulations showing the relevant effects of degrading materials.

Part I focuses on the proposed open-source radiation testing apparatus, shown in Fig. 1.1. Chapter 2 provides a review of the literature and background information. Chapter 3 presents the design and implementation of a hardware prototype of the testing apparatus, outlining the technical capabilities and design considerations. In Chapter 4, the developed prototype is used to evaluate the radiation sensitivity of four different types of microcontrollers. A total of 20 devices were tested, and the data

collected, shown in Table 1.1, is evaluated to estimate *single-event upset* (SEU) error rates and the corresponding *mean-time between failures* (MTBF) in *low Earth orbit* (LEO). Chapter 5 discusses the emergence of smaller technology-node devices that are now sensitive to direct ionization from low-energy protons. The contribution of low-energy protons to soft-error rates on CubeSats operating in LEO and the implications on ground-based testing methods are discussed.
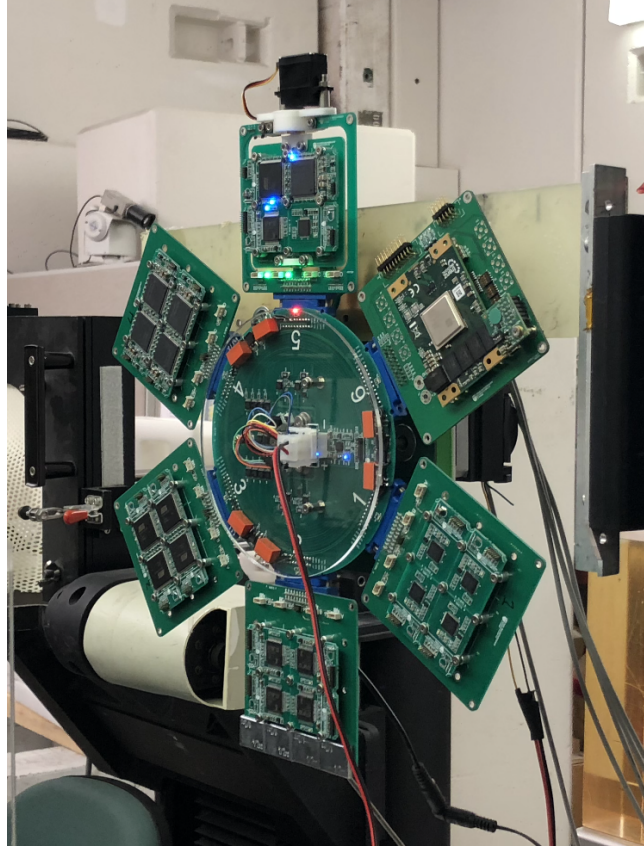
Figure 1.1.: Test equipment installed at TRIUMF.

Table 1.1.: Calculated in-orbit SEU rates for the devices tested.

Manufacturer Part No.	SEU Rate (/bit/day)	MTBF per Device
M430FR5989SRGCREP	0.90×10^{-7}	16661 hours
EFM32GG11B820F2048	5.53×10^{-7}	11 hours
AT32UC3C0512C-ALZR	1.38×10^{-7}	339 hours
M2S010-TQG144I	2.52×10^{-7}	186 hours

CubeSat Electrical Power Supply The power system is suspected to be the single largest cause of all spacecraft failures [16] and therefore, EPS design is a key driver in reliability assurance. Development of a power system that is capable and reliable enough to support all operations of a given mission for the entire mission life is a challenge for most university CubeSat groups, which are relatively inexperienced in developing mission critical subsystems. Instead, most CubeSat missions rely on COTS power systems, which are costly, sometimes difficult to procure, and not necessarily optimized for the given mission. In this work, an open-source EPS for CubeSats is proposed, with several novel features that enhance reliability.

The contributions of this work are:

- An innovative open-source EPS design for the CubeSat community that offers similar or better capabilities than popular COTS EPSs.

- A fail-safe solar panel power control feature that activates when recovering from a fully-discharged battery state.

- A charge/discharge inhibit mechanism allowing battery discharge and heating in low-temperature conditions. It also can be used to optimize battery heater use during eclipse, minimizing unnecessary heating when solar power is unavailable.

- A transistor-based power inhibit circuit for power-off before satellite deployment,

reducing conduction losses and simplifying wiring harness design.

- Intelligent low power sensors that quickly decouple power during over-current events and monitor critical parameters, minimizing power consumption without constant polling.

- A jumper matrix to supply regulated or unregulated bus voltage to 18 output channels, with a synchronized fault response feature for codependent channels.

- Adaptive over-current fault detection compensating for gradual leakage current increase due to accumulated total-ionizing dose effects over the mission's duration.

Part II focuses on the proposed open-source EPS, starting with a review of the literature and background information in Chapter 6. In Chapter 7, the design and testing of a finished hardware prototype, shown in Fig. 1.2, are presented. In future work, this design will be implemented as a technology demonstration payload on a future CubeSat project led by the AlbertaSat team at the University of Alberta [5]. The objective of this project is to provide an affordable EPS option for university CubeSat groups that offers a similar or better level of reliability and sophistication as state-of-the-art COTS EPS products, while also benefiting from collaborative open-source development.

Open-Source Development The two projects presented in this thesis have been developed with the intention of being published under open-source licenses. The motivation for this initiative is to contribute to the community of university CubeSat groups by providing a freely available resource to accelerate their own development efforts. With a shorter path to inexpensive and reliable mission-critical subsystems and testing infrastructure, CubeSat groups can then focus more on the development
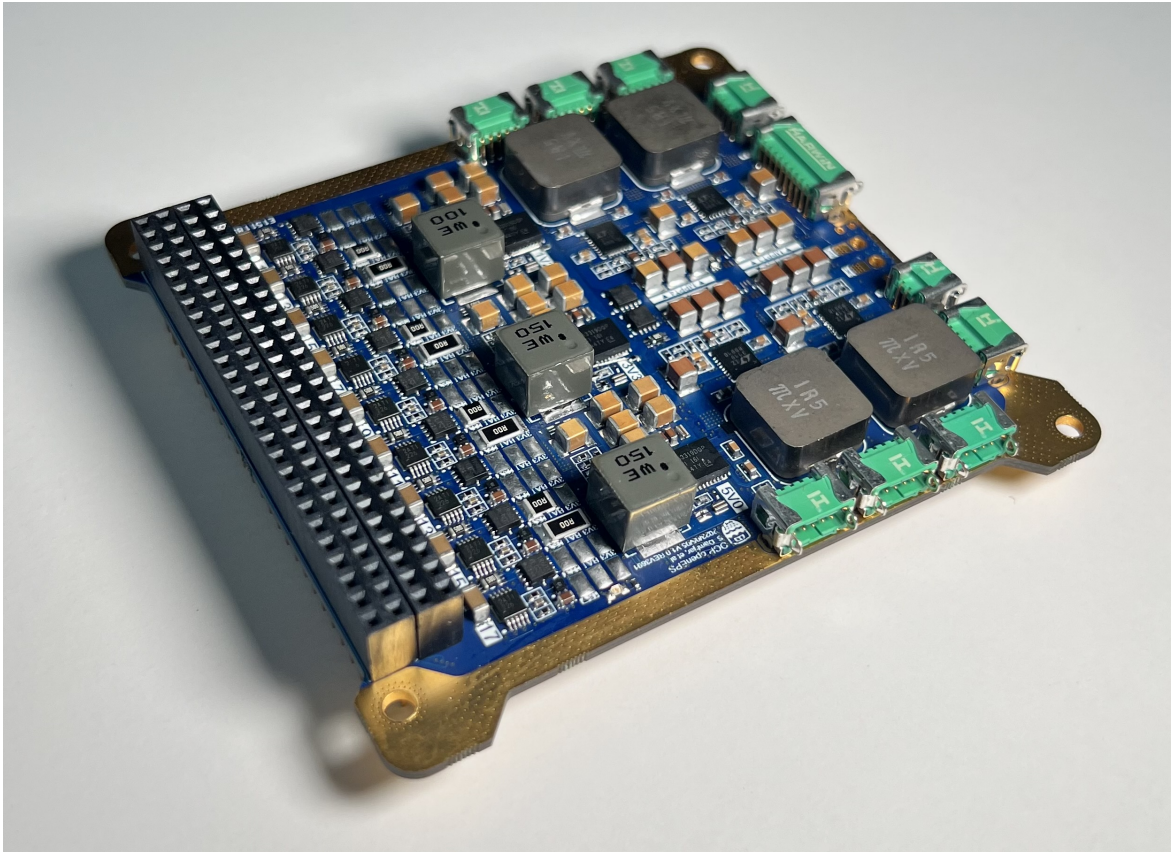
Figure 1.2.: Photograph showing a fully implemented prototype of the proposed open-source EPS design. The design is compatible with the stackable PC104-like physical form-factor, that is used on most CubeSats [2].

of their scientific payloads and on novel contributions to the space community.

1.2. CubeSats – Background Information

The rapid development and miniaturization of computing technology continuously redefines what is possible. As computing technology has evolved to achieve more with less, so too has the space industry. Small satellite technology is a rapidly growing presence in the modern space sector that has greatly lowered the barrier of entry to access space [17]. Among the increasingly diverse classifications of "small satel-

lites", the *CubeSat* has emerged as an effective form factor for academic research and technology demonstrations. The CubeSat standard originated in 1999 from the collaborative effort of California Polytechnic State University and Stanford University's Space Systems Development Laboratory [15]. Since then, over 1800 CubeSats have been launched into space [18]. CubeSats are classified based on units of volume as shown in Fig. 1.3, where each *unit* (U) is a $10 \times 10 \times 10$ cm cube [19]. Fig. 1.4 shows the sizes and developer categories for CubeSat missions launched in 2022.
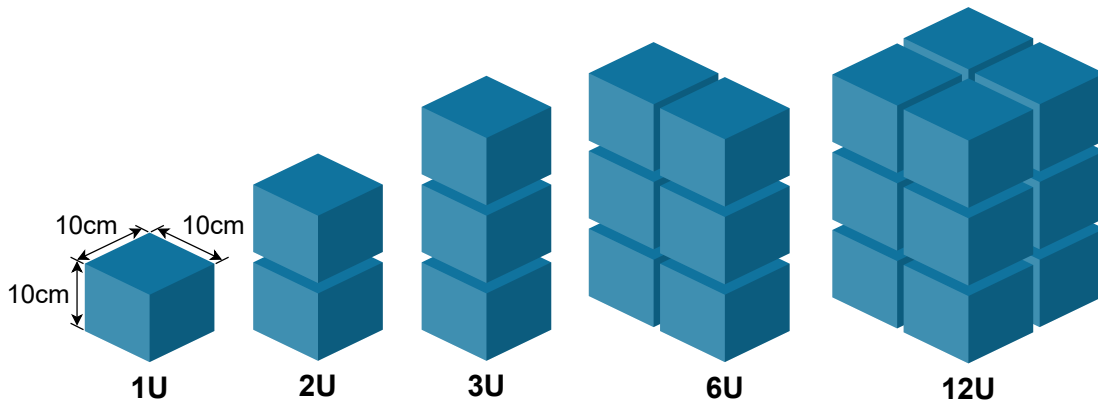
Figure 1.3.: Different CubeSat size classifications, based on the number of $10 \times 10 \times 10$ cm cubes.
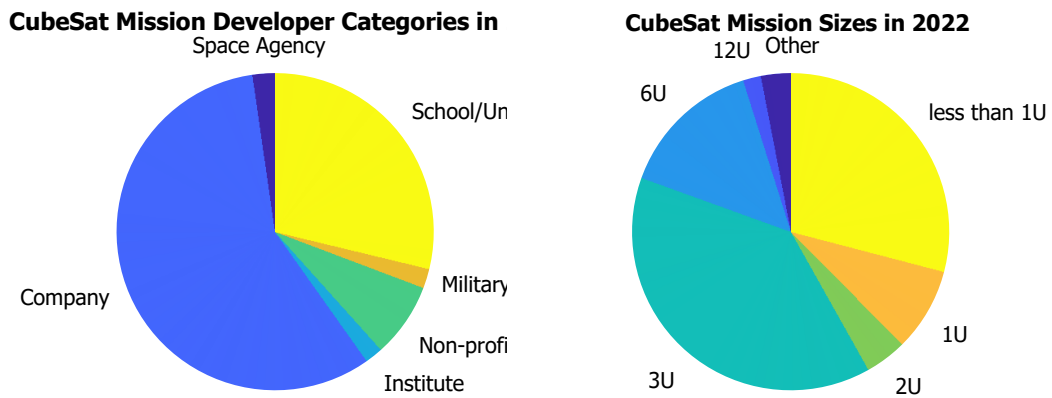
Figure 1.4.: Statistics for CubeSat missions launched in 2022, using data from [3].

A key advantage of CubeSat missions, compared with larger spacecraft projects, is

significantly lower launch costs and shorter development time. These characteristics expand the pool of potential developers and lower the stakes, allowing some risk mitigation efforts to be relaxed. However, reliability is still a critical factor when designing any system intended to operate in a harsh remote environment such as space, where physical access is nearly impossible. As CubeSat developers aim to add even more capabilities to their platforms, new design solutions are needed to optimize the tradeoff of lower costs and mission reliability.

AlbertaSat

The initial motivation for this thesis was the CubeSat development efforts of the AlbertaSat team at the University of Alberta. Fig. 1.5 shows renderings of the Ex-Alta 1 and Ex-Alta 2 CubeSats, developed by the AlbertaSat team, and launched into orbit from the *NanoRacks CubeSat Deployer* (NRCSD) on the *International Space Station* (ISS) in 2017 and 2023, respectively. The developments efforts and lessons learned from these and other AlbertaSat projects have motivated the topics chosen for this thesis and it is my hope that this work will be an asset to future AlbertaSat projects.
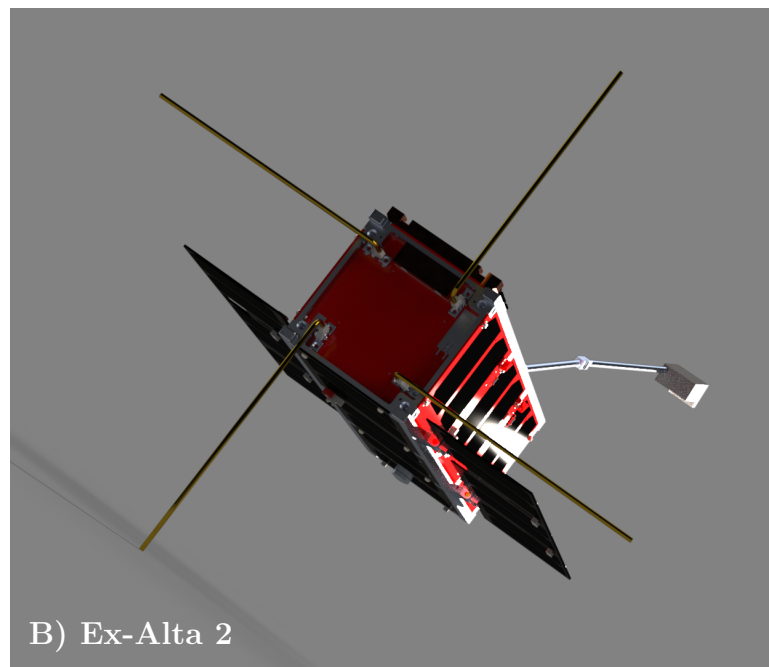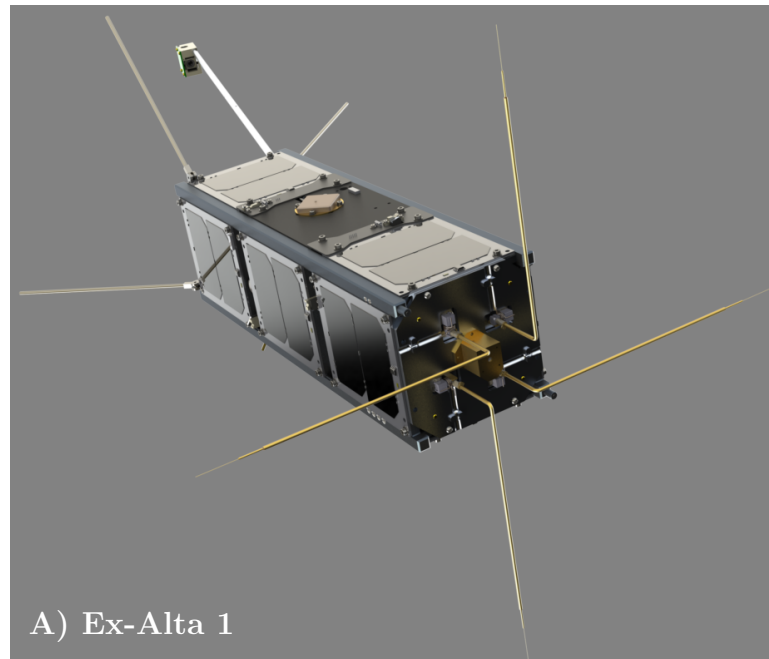
Figure 1.5.: Renderings of the A) Ex-Alta 1 [4] and B) Ex-Alta 2 [5] CubeSats, developed by the AlbertaSat team at the University of Alberta.

Part I.

Radiation Testing

2. Background – Radiation Testing of Electronics to be used in Space

Ordinary COTS electronic components, rather than higher-reliability radiationhardened components, are often used with acceptable success on LEO CubeSat missions [20]. But intense radiation levels do occur in LEO conditions, particularly at the South Atlantic Anomaly [21], and CubeSats with COTS components routinely encounter reliability issues caused by radiation [22]. Some of those issues can be effectively mitigated using error-tolerance strategies. Also, some COTS components are likely to be more vulnerable to radiation effects than others. By screening COTS components based on their sensitivity to radiation effects, components that are particularly vulnerable can be avoided. This method is sometimes referred to as the *"careful-COTS"* approach [23].

Particle accelerator testing is a standard method used by in the aerospace industry to characterize the radiation sensitivity of a component, but it is often too costly and complex for CubeSat missions, particularly in budget-constrained academic projects. The main objective of this work is to develop an inexpensive and straightforward test method to effectively evaluate the radiation tolerance of devices while maximizing the efficiency of costly particle accelerator test time. This work thus aims to develop a

new cost-effective method of testing that will be more accessible to groups developing CubeSat subsystems within a limited budget.

System Design using a "Careful COTS" Approach

Semiconductors in microelectronic devices are sensitive to changes in electrical and material properties caused by ionizing radiation. Solar protons and galactic cosmic rays pass through semiconductor devices, causing soft errors or damage. Thanks to shielding provided by the Earth's magnetic field, faults in devices on the Earth's surface are rare enough that they are not typically a major concern. However, in applications requiring high reliability, such as implantable medical devices [24] or critical data infrastructure, and in applications involving highly radioactive environments, such as nuclear facilities or aerospace applications [25], careful consideration should be given to mitigate faults caused by ionizing radiation.

To ensure reliability for satellite missions, semiconductor components in conventional spacecraft are typically *radiation-hardened*, meaning specialised fabrication processes and/or *integrated circuit* (IC) layout techniques have been used to mitigate ionizing radiation effects. Those components come with higher cost, larger size, increased power consumption, limited performance, and supply chain constraints that often make them unsuitable for low-cost CubeSat missions.

2.1. Sources of Ionizing Radiation in Space

Solar Energetic Particles (Solar Flares)

It is well known that the sun releases harmful ionizing radiation in the form of solar energetic particles, particularly during solar flares and coronal mass ejections [26]. This solar radiation is usually in the form of high-energy protons (ionized hydrogen), smaller quantities of helium ions, electrons and (during solar flare activity) X-ray radiation [27]. Solar energetic particles are usually on the order of 10 to 100 MeV and rarely reach Earth's surface because they are deflected by the Earth's magnetic field, as illustrated in Fig. 2.1, but still pose a threat to orbiting spacecraft [28]. Occasionally, solar radiation levels will peak during events known as geomagnetic storms. X-rays are also generally stopped by Earth's atmosphere but occasionally interfere with radio communications and Global Positioning System (GPS) measurements [29].
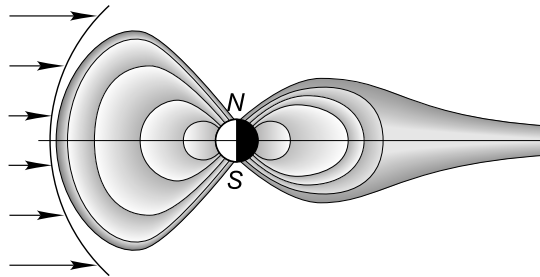
Figure 2.1.: Illustration of solar energetic particles interacting with Earth's magnetic field [6].

Planetary Radiation Belts

As solar energetic particles pass the Earth, high-energy electrons and protons are captured by the Earth's magnetic field and trapped in what are referred to as the Van

Allen radiation belts [30], as shown in Fig. 2.2. The Earth's inner radiation belt exists just above low Earth orbit between 1000 and 6000 km with proton energies exceeding 100 MeV. Because most spacecraft operating in low Earth orbit operate below these altitudes, this is not a major concern. However, there is one region where high radiation levels exist at lower altitudes. This phenomena is called the South Atlantic Anomaly and is known to wreak havoc on spacecraft in low Earth orbit [21].
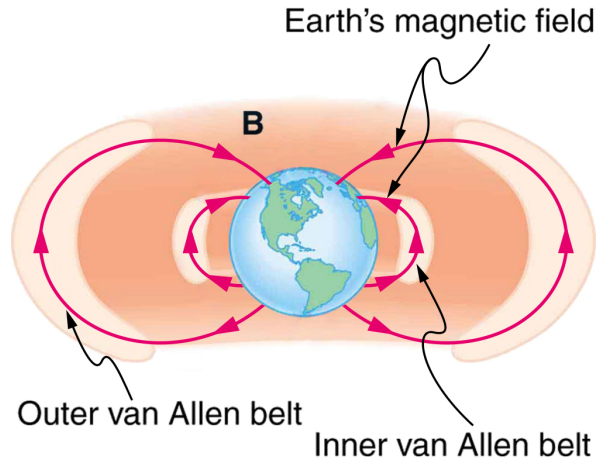
Figure 2.2.: Illustration of the van Allen radiation belts around Earth [7].

Galactic Cosmic Rays

Galactic cosmic rays (GCRs) are believed to originate from the remnants of supernovas elsewhere in the galaxy [31], with a wide distribution of energies sometimes exceeding 10^{19} eV [32]. GCRs react with Earth's atmosphere, producing complex cascades of secondary particles. The most important of those secondary particle for SEEs is neutrons [33] because of the ability neutrons to penetrate materials and produce isotopes [34]. These events will occasionally interfere with or damage digital infrastructure. Most users would prefer to endure rebooting their computer ever few years rather than pay for expensive radiation testing campaigns. But in applications that demand very high

reliability, this becomes an important consideration that requires thorough testing and mitigation strategies known as radiation hardening. This has become an increasingly important issue as more and more aspects of everyday life become dependent on embedded systems and ever shrinking feature size makes semiconductor devices more vulnerable to radiation effects. Radiation hardening is generally reserved for military, medical and aerospace applications [24, 25]; however, it has become a growing concern for automotive applications [35] and critical data infrastructure such as internet nodes, and banking systems.

2.2. Radiation-Induced Fault Types

Radiation effects in semiconductor devices can be classified as either *total ionizing dose* (TID) effects or *single-event effects* (SEEs). SEEs are the result of a single energetic particle [36] while TID refers to gradual parametric changes caused by an absorbed radiation dose over time [37].

2.2.1. Soft Errors

A *soft error* can occur when an energetic ion passes through the depletion region of an N+/P junction. The charged particle creates a funnel-shaped distribution of higher charge carrier density along its trajectory. This *ionization track* momentarily extends the depletion region into the substrate, resulting in a brief pulse of drift current (I_{drift}) across the junction, reducing the voltage on the node. This interaction, shown in Fig. 2.3, occurs within several picoseconds before the charge carriers diffuse back into the substrate [38]. The most significant naturally occurring cause of soft errors in

semiconductor devices are alpha particles emitted from high energy particle collisions or isotopic decay in the device materials [38].
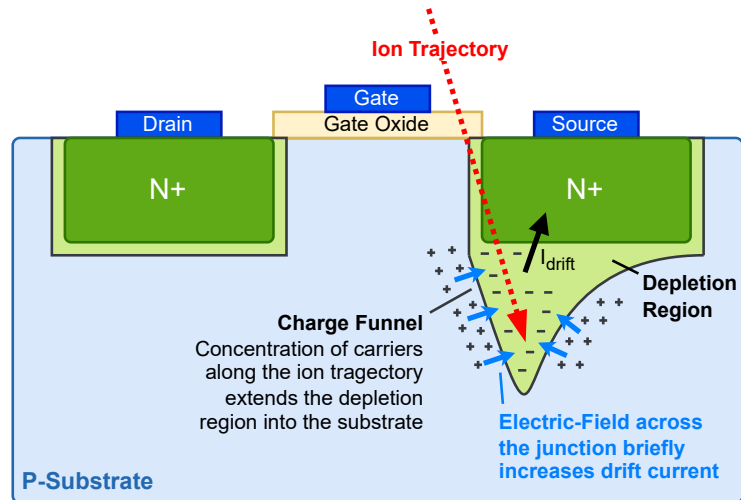
Figure 2.3.: Ionization along the trajectory of a charged particle through a pn-junction momentarily extends the depletion region creating a pulse of increased drift current.

Single-Event Transient (SET)

When a soft error occurs at a driven node, the node voltage is temporarily reduced. Any faulty behaviour resulting from this transient effect is called a *single-event transient* (SET) fault [36].

Single-Event Upset (SEU)

An *single-event upset* (SEU) occurs when a soft error occurs on a floating node (causing a static voltage change) or when an SET fault results in a change to a static logic value (such as the state of a memory bit) [36].

Single-Event Functional Interrupt (SEFI)

A *single-event functional interrupt* (SEFI) fault occurs when a soft error, such as an SEU fault in a configuration register, causes a device to malfunction in a detectable way. A SEFI can be resolved with a soft reset of the configuration registers and does not result in permanent damage to the device [39].

2.2.2. Hard Faults

Single-Event Gate Rupture (SEGR)

An ion passing directly through the gate oxide of a transistor can create a filament of plasma along the ionization track. The resulting electric field can be strong enough to cause a breakdown of the oxide layer. This fault is called a *single-event gate rupture* (SEGR) [40].

Single-Event Latchup (SEL)

A *single-event latch-up* (SEL) fault occurs when a self-sustaining parasitic silicon controlled rectifier (SCR) latch structure, is activated within a *complementary metal-oxide semiconductor* (CMOS) structure, as shown in Fig. 2.4. Similar to burnout, this is due to the movement of charge caused by the ionization track of heavy ions passing through the device. SEL faults result in high current between the V_{DD} and V_{SS} terminals of the CMOS transistor. Generally, this can be detected by constant current monitoring and then halted by cycling the power.
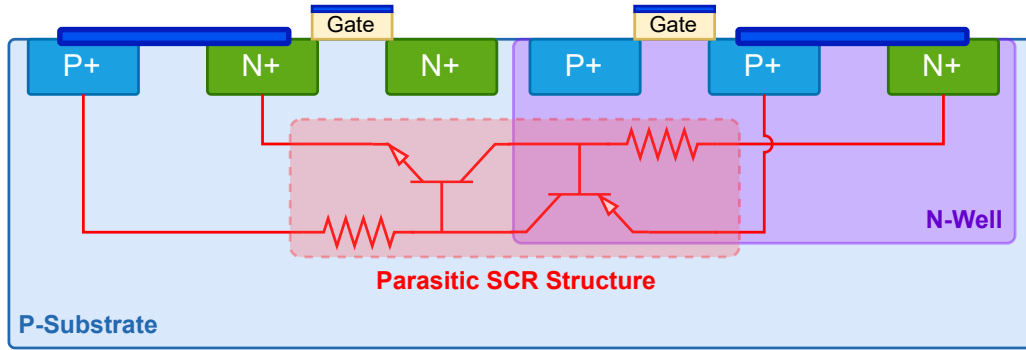
Figure 2.4.: Illustration of a self-sustaining parasitic SCR latch structure within a CMOS structure causing an SEL fault.

Single-Event Burnout (SEB)

An ion passing through a transistor in the off state, which is isolating the signal node from a high drain-source voltage, can activate a parasitic bipolar transistor structure between the n+ source, the p-body, and the epitaxial layer [41]. If enough current is available to the source terminal, the resulting positive feedback mechanism could cause a failure. This fault is called a *single-event burnout* (SEB).

2.3. Radiation Testing Methods

Proton Testing

Proton testing is an effective testing method that is used to emulate the effects of solar radiation, and is the method chosen for this work. *Linear energy transfer* (LET) refers to the increment of energy transfer per unit length along the trajectory of the ionizing particle incident through the device under test and is typically expressed in units of $MeV\,cm^2/mg$ [9]. Protons passing through silicon have a relatively low LET of only $0.54\,MeV\,cm^2/mg$ or less which is often not sufficient to cause SEEs. However, collisions

between protons and nuclei within the DUT, such as silicon, aluminum, copper, or gold, can generate nuclear reaction products with LET as high as $15\,\mathrm{MeV\,cm^2/mg}$, and are therefore representative of a large fraction of the LET spectrum encountered in LEO [23, 42]. This makes protons suitable for SEE testing of LEO spacecraft.

Heavy Ion Testing

Heavy ion testing is an effective and versatile method for evaluating the sensitivity of devices to ionizing radiation [36]. For this method, a particle accelerator facility is used to fire heavy ions at the DUT. This method allows control of the LET between the ionizing radiation and the device under test (including very high LET values) by changing the ion species [43]. Because this method allows the LET to be varied, it can provide insights into radiation effects mechanisms that other testing methods can not. However, the effects of high LET are not truly representative of the proton-rich environment in LEO that exists in the Van Allen Belts [9]. Also, heavy ion testing is generally more costly and facility availability is limited [23, 44].

Total Dose Testing

TID is the *total absorbed dose* deposited in a device substrate by ionizing radiation. In electronic devices the accumulation of TID causes permanent parametric degradation in the device and can lead to functional failure [45, 46]. There are many approaches for performing TID testing, some of which are less expensive and more accessible than particle accelerator testing. Some examples are gamma ray sources, such as cobalt-60, and X-ray sources [47]. These testing methods are attractive because they are relatively inexpensive and generally more accessible than other forms of radiation testing. Due to the very low LET of gamma rays and X-rays incident through silicon, this type

of testing does not cause SEEs so it is only useful for total dose testing. Although this method is a cost-effective way to evaluate lifetime dose effects of COTS devices, it neglects some failure modes that are seen with charged, strongly ionizing, particles such as protons or heavy ions.

In-Orbit Testing

All of the methods discussed above are intended to assess how devices will perform in their operational environment. For the purposes of this work, that operational environment is integrated within a CubeSat in LEO. The mechanisms of radiation effects that cause SEEs and parametric degradation in electronic devices are complex; using ground-based testing to predict and quantify error rates in LEO is not straightforward. Hence, a clear solution is to complement ground-based testing by evaluating device performance in orbit [48]. Such missions have been attempted to study how well classical error rate prediction models based on ground-based testing estimate in orbit performance, particularly in emerging technologies, where new failure mechanisms exist [20, 48].

2.4. Trends in Emerging Semiconductor Technology

Effects of Technology Scaling

As the feature size in modern integrated circuits gets smaller, devices are becoming more vulnerable to radiation-induced faults [35]. This is due to a reduction in the minimum amount of charge needed to disrupt an individual transistor, commonly referred to as the *critical charge*. The critical charge needed to cause faults has steadily

decreased due to reductions in supply voltage, gate oxide thickness and transistor dimensions [49].

Radiation Effects in State-of-the-Art FinFET Devices

In semiconductor technology beyond 22 nm, three-dimensional FinFET transistor structures have become an attractive option because of improvements in channel effects and reduced leakage [50]. Along with their many other advantages, FinFET structures have shown a remarkable reduction in sensitivity to ionizing radiation with 5 to 10 times improvement compared with previous technology nodes [51]. This is due to an improved isolation between the charge collected in the substrate, and the charge collected in the drain and source regions of the transistor.

3. An Automated Platform for Testing Microelectronics

3.1. Introduction

Microelectronic devices continue to evolve rapidly. Keeping up with the latest technology improvements poses a particular challenge to the space industry because of the rigorous and time-consuming quality control measures that are required to develop reliable spacecraft components. This precaution causes a lag in the use of cutting edge computing technology. The development of CubeSats and inexpensive access to space has enabled a new market segment of satellite developers who are able to accept greater risk. Thanks to their small size, low cost, relatively quick development, and the abundance of inexpensive launch opportunities, CubeSats have become popular for increasingly complex missions in *low Earth orbit* (LEO) [3]. The low cost of CubeSats justifies relaxed quality assurance and reliability constraints, enabling a more rapid development cycle and more aggressive adoption of new component technologies. To get the most out of this balancing act of lower cost and relaxed reliability requirements, innovative testing approaches are needed to maximize the operational lifetime and expand the utility of CubeSat missions while still preserving their low cost advantage.

CubeSat projects increasingly use *commercial off-the-shelf* (COTS) microelectronic components, as opposed to the *radiation-hardened* components traditionally used on spacecraft, because of more stringent budget, volume, and power constraints [23, 42, 52]. Radiation-hardened refers to components that have been specifically designed and manufactured to withstand high-radiation environments, and are typically several orders of magnitude more expensive than other high-reliability classes of components such as automotive-grade. COTS components are often used on CubeSats despite lacking characterization data indicating their sensitivity to radiation effects. While such components can be, and often are, used with success, many developers of past CubeSat missions, which failed within the first 6 months after launch, have blamed radiation effects [53]. To ensure sufficient mission reliability, the radiation tolerance of COTS components is a major consideration in determining their suitability for use in space. CubeSat developers need a cost-effective and easily implemented method to characterize the radiation sensitivity of non-hardened components and to identify vulnerabilities before they become mission reliability concerns.

The complexity of designing particle beam experiments and the high cost of access to testing facilities are significant hurdles [54] that make it difficult for CubeSat developers to characterize the radiation tolerance of COTS components. The cost of particle accelerator beam testing can often be equally as prohibitive for developers as purchasing radiation-hardened components. The objective of the work reported here was to create a simple and versatile open-source testing platform that is easy to implement and that will maximize the amount of useful data that can be gathered from beam testing during necessarily limited testing time. The goal is to lower the cost of access to radiation testing and to increase the availability of radiation test data for COTS devices in the literature, which would then help guide future CubeSat subsystem design.

Ultimately this should improve the reliability of low-cost CubeSats and accelerate the adoption of cutting edge computing technology in the space industry.

The hardware and software described in this chapter are entirely original work. The modular testing platform described below has six removable and interchangeable testing stages (each supporting up to four device-under-test boards) that can be individually and remotely positioned into the beam-line, allowing the rapid testing of up to 24 devices without requiring personnel to enter the radiation test chamber. After firing the radiation beam, a *cool-down* period is required before personnel can enter the testing chamber, to avoid exposing personnel to high levels of radioactive decay from the short-lived unstable isotopes produced during the testing. This remote device manipulating capability significantly improves the utilization of testing time by avoiding the need to enter the testing chamber until after all of the testing is complete. The particle beam incidence angle can also be varied remotely. The platform was developed for use at TRIUMF, a high-energy particle accelerator facility in Vancouver, Canada [55]. The design and functionality of the testing platform are discussed below. Test data recorded at the TRIUMF *Proton Irradiation Facility* (PIF) is presented and analysis is discussed. Finally, plans for future improvements to the testing platform are proposed.

3.2. Objectives

In this section, we outline the key objectives that drove the development of our testing platform. These objectives include characterizing the radiation sensitivity of electronic components, by providing rapid and cost-effective implementation of testing procedures, and promoting an open-source design approach for collaborative development.

3.2.1. Characterize Sensitivity to Single-Event Effects

A faulty behavior or fault caused by a single ionizing particle is called a *single-event effect* (SEE). The primary purpose of the developed testing platform is to more rapidly and more efficiently measure the statistical cross-section of SEEs caused by ionizing radiation particles. SEEs have many different forms. The most common fault in memory devices is the *single-event upset* (SEU) [56], which is a fault that changes the binary state of a memory cell. Any other soft fault that produces a measurable malfunction and does not require a power cycle to recover is deemed an SEFI [39]. An example of a *single-event functional interrupt* (SEFI) is an SEU fault in a configuration register. A *single-event latchup* (SEL) fault produces a parasitic high current latch structure in the device, which could result in permanent device failure. This work focuses on these three fault types. The testing platform must reliably detect these faults (SEU, SEFI, and SEL) and record relevant data to characterize operational reliability.

3.2.2. Limitations of Existing Approaches

Components on CubeSats are vulnerable to the same radiation reliability concerns as those on large satellites. Unfortunately, the limited resources of small satellite projects are often accompanied by a lack of radiation testing and analysis [57]. The high cost of beam-time and the effort required to develop a test fixture can make particle accelerator testing a very costly endeavor [54]. An alternative approach sometimes used by CubeSat developers is to include DUTs as a payload on a CubeSat mission to investigate the radiation sensitivity of devices in their actual operating environment [48, 58]. The rationale of such experiments is generally that the compact payload

poses less cost than accelerator testing [54]. However, repeatability of this approach is limited compared with particle accelerators and this approach can be unforgiving if limitations of the test fixture become apparent after launch.

3.2.3. Rapid Low-Cost Implementation

Preparing devices for testing should be fast and easy. To make the testing platform versatile with respect to the type of devices that can be tested, a modular solution is used for mounting the *devices under test* (DUTs). This system is designed to hold a 10×10 cm *DUT motherboard*, with four small *DUT daughter cards*, each holding only the DUT and essential circuitry needed for it to operate. These DUT cards, shown in Fig. 3.1, are interchangeable and simple in design, simplifying the test setup. Alternatively, any device with a serial interface that can fit within the 10×10 cm DUT motherboard (including entire CubeSat subsystems) can be directly attached, replacing the small DUT cards.

3.2.4. Minimizing Human Intervention

A common approach in the literature is to use a single fixed board with a single DUT in the beamline and supporting circuitry around it [59]. A key limitation apparent with this approach is the time needed to swap the DUT throughout testing to determine the repeatability of the experiment. Due to high levels of short-lived residual radioactivity, a cool-down period is required after beam irradiation before personnel can re-enter the testing chamber. This required cool-down time is typically on the order of ten minutes to an hour or more, depending on the duration, intensity and energy of the dose, and the materials receiving the dose. These periods of wasted time reduce the time
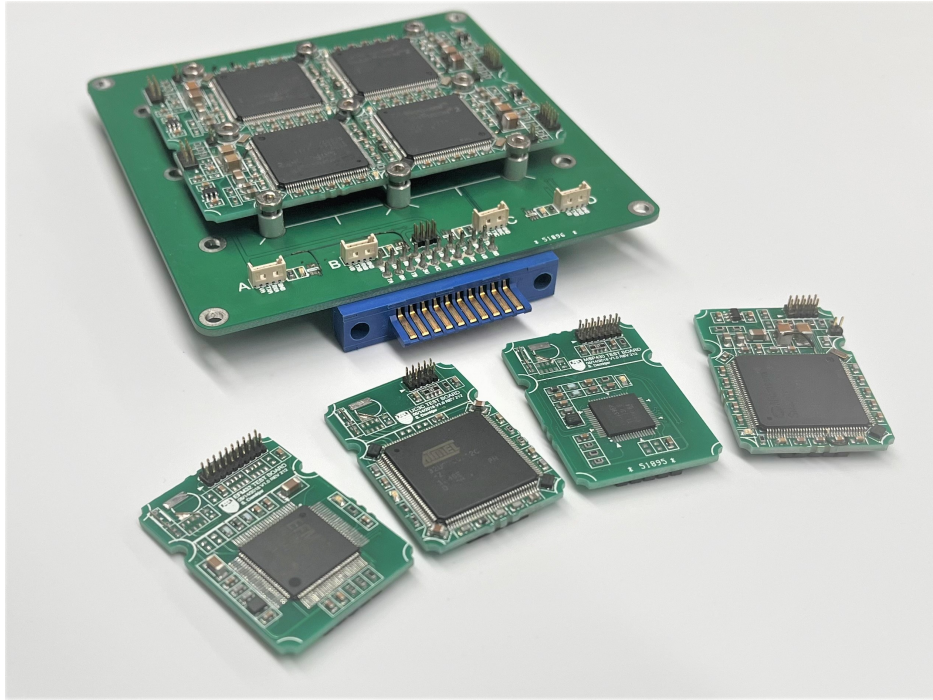
Figure 3.1.: Individual DUT cards for SEE testing.

available for irradiating devices, thus limiting the expensive beam time devoted to actual testing. Automation and remote operation avoid the need for costly cool-down periods during testing and also adequately limiting the safety hazard to personnel.

3.2.5. Open-Source Design

The design files for the software and the electrical and mechanical hardware for this testing platform will be published under an open-source license so that they will be available to other developers. This initiative aims to alleviate trial-and-error challenges faced by CubeSat developers during radiation testing. Moreover, data gathered by different groups using a common testing platform will facilitate the comparison of test results. The total bill of materials cost for this project is under $1000, thus making it accessible to most CubeSat developers.

3.3. Review of Radiation Testing Techniques

The high cost and procurement challenges associated with radiation-hardened devices have driven the growing adoption of COTS devices in satellite components [23, 42, 52]. While this approach offers clear advantages in terms of cost savings and power requirements, it also introduces the potential for unacceptable risks when the radiation effects on these devices are not adequately characterized [60]. The responsibility then lies with the space project engineers to systematically evaluate the sensitivity of these devices to radiation effects [61]. Thus, there is a growing demand for the development of cost-effective radiation testing strategies. In this section, some approaches from the literature are reviewed, which have the potential to be more cost effective than traditional beam-line testing.

3.3.1. Simulation-Based Testing

Various simulation techniques have been proposed to evaluate the SEE sensitivity of devices [62–65]. Additionally, fault-injection simulations are used to verify SEE mitigation techniques, such as logic redundancy [66]. The clear advantage of simulation is that it eliminates the need for expensive radiation facilities and specialized hardware. However, meaningful prediction of SEE rates through simulation generally requires detailed knowledge of the semiconductor layout, which is typically unavailable to the space project engineers.

3.3.2. Pulsed-Laser Testing

Pulsed-laser radiation can effectively emulate the influence of heavy ions and presents several distinct advantages over traditional particle accelerator testing [67–69]. Laser

devices are much more affordable compared with particle beam sources and have fewer safety and ecological concerns [70]. Some other unique advantages of pulsed-laser testing are high reproducibility, precise spatial control to focus on certain elements on a chip and the ability to study dynamic sensitivity in various operational modes [71]. However, the large parameter space of laser testing can make it complex and time-consuming to achieve meaningful predictive results [67]. Additionally, fundamental mechanisms are lacking with laser radiation compared with exposure to radiation from heavy ions, such as ionization of dielectric materials or secondary ion production [70].

3.3.3. Total Ionizing Dose Testing

Total ionizing dose (TID) effects refers to the gradual degradation of a device, such as the ionization of dielectrics. Accumulated TID affects will eventually cause failures and are thus an important factor for mission lifetime requirements [72]. TID testing typically uses radioisotopes such as Cobalt-60 and Cesium-137 or low-energy X-ray generators [73]. Such facilities are relatively low-cost compared with proton and heavy-ion accelerators and have been used to validate CubeSat subsystems [74]. However the significant limitation of this approach is that it provides no information about susceptibility to SEEs.

3.4. Hardware Design

The main elements of the testing platform design are the mechanical mechanism for positioning the DUTs into the beam-line, and the programmable controller for managing the flow of power and data to and from the DUTs. Each of these design elements is discussed in turn in this section.
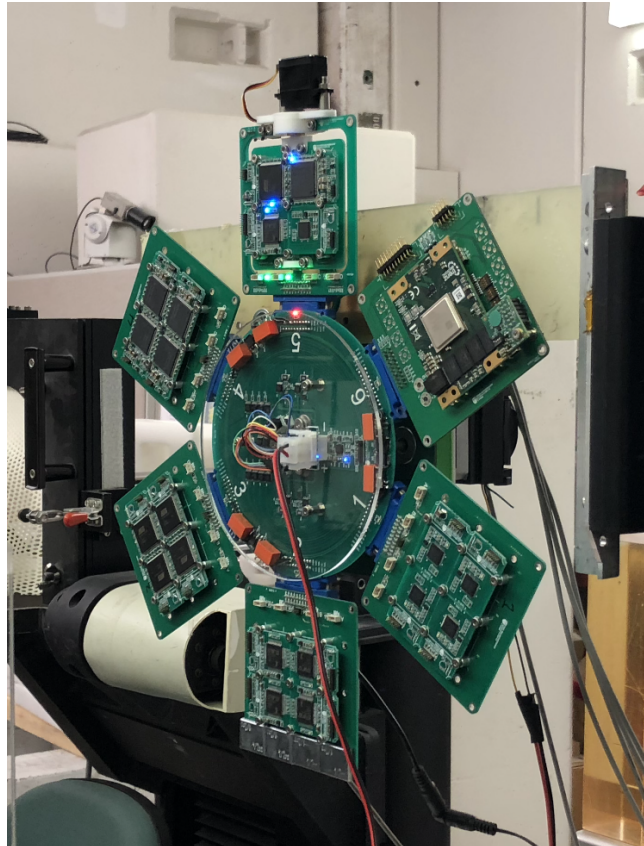
Figure 3.2.: Test equipment installed at TRIUMF.
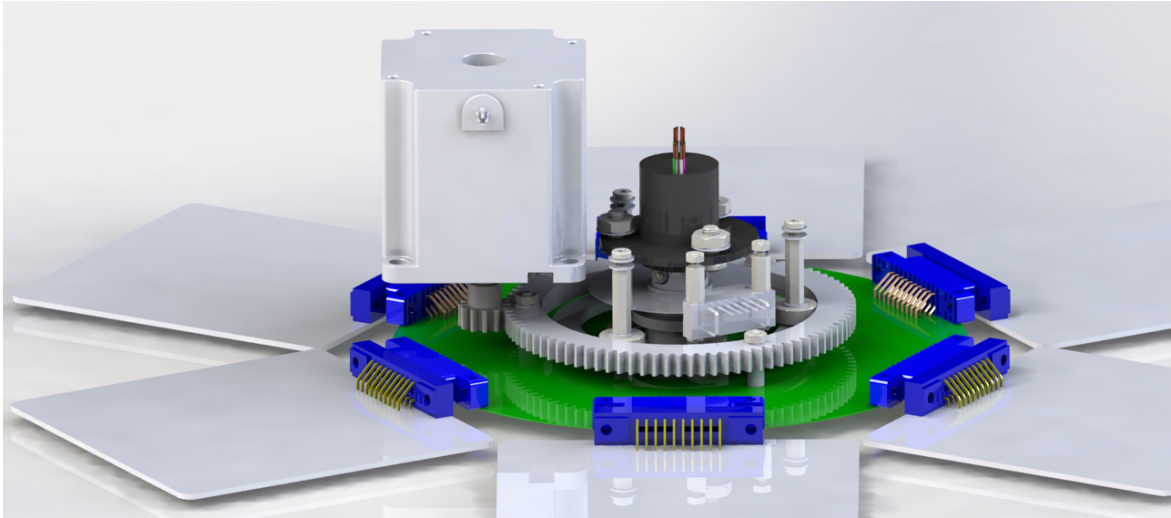
Figure 3.3.: The mechanical rotating mechanism.

3.4.1. DUT Positioner Design

The test platform, shown in Fig. 3.2, was developed for use at the TRIUMF Proton Irradiation Facility [14]. The DUT positioner holds six DUT motherboards and positions them, one at a time, into the beamline, by rotating the assembly.

The rotation is achieved by a stepper motor and gear mechanism, shown in Fig. 3.3. The angular position of the DUT selector is measured with an encoder wheel. Once the DUT selector has been calibrated to the zero position on the encoder wheel, the DUT selected motherboard can be centered in the beamline with an accuracy of ± 0.6 mm. Signals and power are supplied to the DUT motherboards through a central conductive slip ring, which allows for continuous rotation without twisting wires.

3.4.2. DUT Form Factor

The DUT selector holds up to six DUT motherboards. Each DUT motherboard is 10×10 cm in size and is connected to the rotating assembly using a reversible con-

nector and two machine screws. Because the connector is reversible, the DUT motherboard can be positioned to irradiate either face. In this work, a 55×55 mm square beam spot was focused on the center of the DUT motherboard in-line with the beam, meaning that only components within that square region would be irradiated. Each DUT motherboard in this work was designed to hold four DUTs, which were either *microcontrollers* (MCUs) or *microprocessor system-on-a-chips* (MPSoCs). Each DUT was mounted on a 40×27.5 mm DUT card over spring-loaded Pogo-pin contacts with a 27.5×27.5 mm portion positioned within the beam spot. The remaining area on each DUT card is available for supporting circuitry, such as oscillators, and for connectors for loading a test program or data into each DUT. The 10×10 cm size was chosen so that entire assembled CubeSat subsystems could be mounted on the platform, if desired.

3.4.3. Data Logger Design

A system was needed to record data during particle beam testing. This system needed to be reliable and not suffer significantly from the effects of the incoming radiation during the test. At TRIUMF, most of the protons that scatter outside of the beam spot are absorbed in a thick aluminum collimator. Thus, the effects of stray radiation scattering from the beamline are negligible. Therefore, being simply physically out of the path of the beam is usually sufficient to protect the data logger from deleterious effects caused by radiation.

The purpose of the data logger is to reliably perform the following functions:

1. To assign accurate time stamps to each measurement, with millisecond resolution.

2. To detect and record SEL faults by monitoring the current consumption of each

DUT and to power cycle the affected device when a fault occurs, to prevent damage from component overheating (*single-event burnout*).

3. To forward data output from test programs running on the DUTs to the control terminal.

4. To respond to commands sent by the user from the control terminal to multiplex the data and power connections to the intended DUTs.

The terminal side of the data logger has five serial data interfaces. Four of those serial interfaces forward test data that is transmitted from each of the four DUT cards to the terminal. The fifth serial interface receives commands from the terminal and transmits all other data, including current sensor measurements, and time-stamped records of events, such as power cycling a DUT. Fig. 3.4 illustrates the data and power connections.

3.4.4. Incidence Angle Control

The rate of SEEs can vary depending on the angle of incidence between the DUT and the particle beam [75]. The incidence angle of each stage can be adjusted remotely using a servo motor, as shown in Fig. 3.5. The incidence angle can be set between $0°$ and $180°$. Additionally, the stage connectors are reversible so that each stage can be mounted with either the top or the bottom facing towards the particle beam, allowing a full $360°$ range of incidence angles. The current prototype of the testing platform has only one DUT motherboard with a servo motor, but the platform is capable of supporting up to six DUT daughter cards at the same time. Power to the servo motors is kept separate from the DUT power supply lines to avoid disturbing the current consumption measurements.
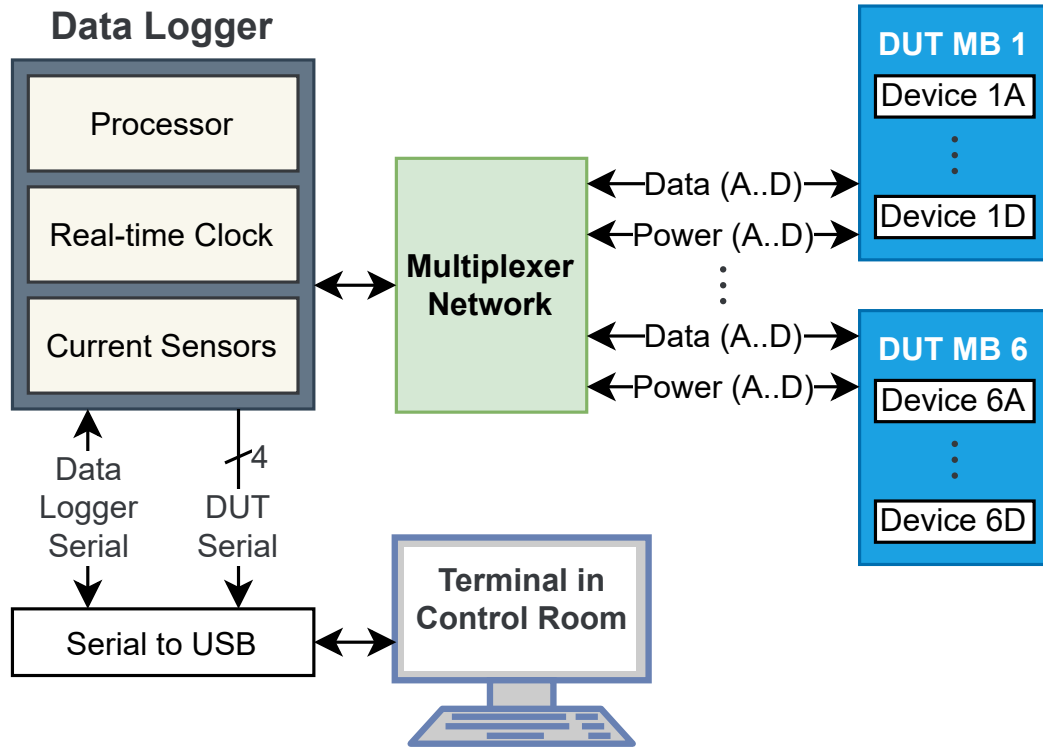
Figure 3.4.: Data logger block diagram.
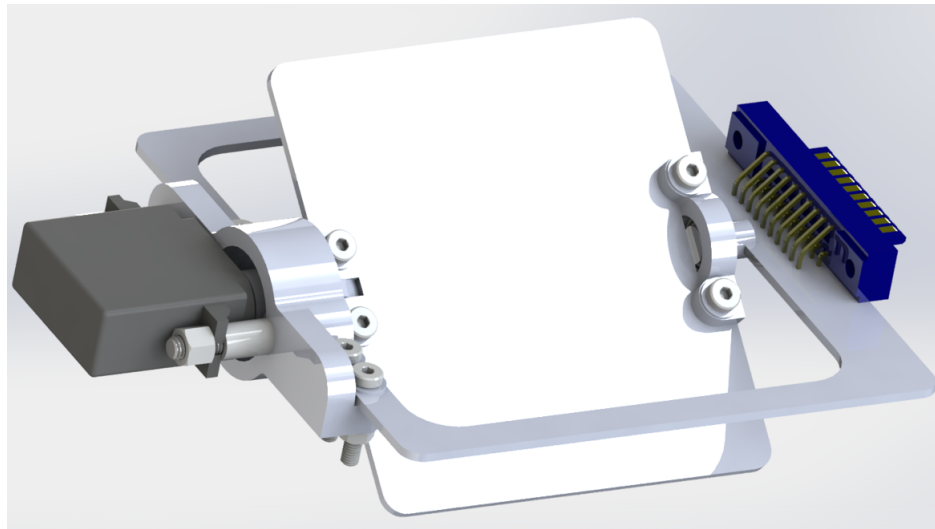
Figure 3.5.: Rendering of the servo-actuated DUT motherboard that allows the beamline incidence angle to be changed.

3.5. Fault Detection

3.5.1. Detecting SEU Faults in SRAM

In this experiment, SEU faults in embedded *static random access memory* (SRAM) subsystems are detected by continuously scanning a large array of data-words for erroneous bits while the DUT is being irradiated. All of the DUTs were either MCUs or MPSoCs that are capable of executing downloaded software. SEU faults in SRAM were detected by continuously writing and then reading back the memory contents a few seconds later. After reading each dataword, it is re-initialized with new data according to the test pattern. The used test pattern alternated with each test between writing and reading back all 1's and all 0's. The newly written value is immediately read to confirm that the write operation was successful. The SEU fault detection algorithm is presented in Fig. 3.6 as pseudo-code. After ten consecutive failed write operations, a SEFI fault is recorded and the affected device is automatically turned off for two seconds to terminate any latching. The number of incident radiation particles per unit area over the duration of the test is called the *fluence*. The fluence values used to determine SEU fault cross-sections must be corrected by subtracting the fluence received during each two-second power off cycle, and during test cycles that coincided with other faulty behaviors.

When an SEU fault is detected, the DUT outputs a single line message that describes the error. The message specifies the time in milliseconds, the type of error (read or write), the value that was read from memory, the value that was expected to be read from memory, and the address of the fault in memory. Fig. 3.7 shows a screenshot of data being recorded on the computer terminal while a DUT is being irradiated.

```
#DEFINE bigarray 99999 // (placeholder value)
typedef unsigned int word; // (placeholder value)
volatile word a[bigarray] = {0};
word previous_write = 0;
word next_write = 0;

ramtest () {
previous_write = next_write;
next_write = next_write^0xffffffff;
  for (j in bigarray) {
    read = a[j];
    if (read != previous_write){
      // Delayed read error
      printf("DR,%0x,%0x,%0x\n",j,
       read,previous_write);
    }
    a[j] = next_write;
    read = a[j];
    if (read != next_write){
      // Instantaneous write error
      printf("IW,%0x,%0x,%0x\n",j,
       read,previous_write);
    }
  }
}
```

Figure 3.6.: Pseudo-code algorithm for SEU fault detection implemented on MCU and MPSOC DUTs during testing. The placeholder value "99999" is replaced later with the appropriate test array size for each DUT (see Table 3.1).

Figure 3.7.: Screenshot of data being recorded during testing.

3.5.2. Detecting SEU Faults in Flash

Additionally, the flash memory of each DUT is monitored for any SEU faults. SEU faults in the non-volatile flash memory of the MCU or MPSoC DUTs are detected by calculating and verifying a 32-bit *cyclic redundancy check* (CRC) in between each iteration of the SRAM test. The start and end times of each memory scan are also recorded.

3.5.3. Detecting SEL Faults

An SEL fault occurs when a parasitic self-sustaining *silicon controlled rectifier* (SCR) latch structure is activated within a bulk *complementary metal-oxide semiconductor* (CMOS) structure due to the movement of charge caused by the ionization track of charged particles passing through the device. SEL faults persist due to feedback paths and can result in potentially damaging high current between the drain and source terminals of the CMOS transistor. The magnitude of the rise in current will depend on the device and the location of the fault within the device. It is very difficult to accurately predict a suitable threshold value for reliable detection of SEL faults for a particular device without experimental testing.

The current consumption of each DUT is monitored with a *least-significant bit* (LSB) resolution of $65\,\mu\text{A}$ and a sampling rate of $50\,\text{samples/s}$. The SEL detection threshold can be configured remotely at any time with a unique value for each device. Fig. 3.8 shows a SEL fault recorded by the current sensors during a proton beam test at TRIUMF. The nominal current consumption of this DUT oscillates around $20\,\text{mA}$ as the memory test cycles. When the SEL fault occurs, the current consumption of the DUT increases sharply to approximately $65\,\text{mA}$ for just over 1 second. This increase
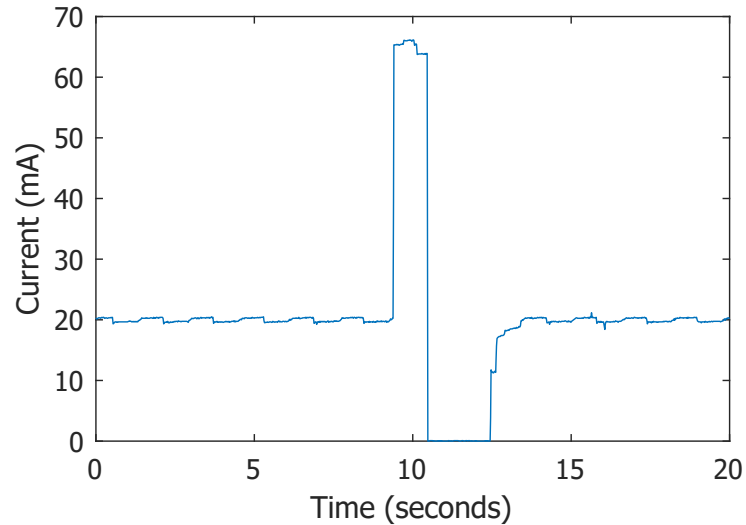
Figure 3.8.: Current consumption produced by an SEL fault measured during proton-beam testing of an EFM32GG11B820F2048 MCU at TRIUMF.

in current is then detected by the current monitor. The time and current measurement values are recorded by the data logger and the power to the device is cycled to prevent damage to the DUT.

During the two-second period when the DUT is off, the SEU fault detection is not functioning. To prevent this off time from skewing the statistical analysis of the data, the turn-off and turn-on times are recorded so that the effective dose contributing to SEU faults can be correctly calculated.

3.5.4. Detecting SEFI Faults

A SEFI fault occurs when a soft error, such as an SEU fault in a configuration register, causes a device to malfunction in a detectable functional way; however, an SEFI fault does not require a power cycle to recover the device, nor does it result in permanent damage [39]. SEFI faults can be corrected by a soft reset of the device. An SEU is a

```
00     00:04:59.626      ,4B,ram
01     00:04:59.773      ,4B,RE:8
02     00:04:59.899      ,4B,nvm
03     00:05:00.025      ,4B,CRC:5df3fc83
04     00:05:00.298      ,4B,end81'ðÀ~ü
05     00:05:00.530      ,4B,boc
06     00:05:00.545      ,4B,2amp
07     üüü|þüüü|üüððüðü|
08     00:05:00.571      ,4B,RE:0
09     00:05:00.572      ,4B,nvmüÿü|üü|üð
10     üü?üðpüð|üþðü||üüðüü
11     ðüüpüü
12     þüüüðüþðüðüð|üððüüðüüüüüðüü
13     ðþüüüü?|üüüðüþðü||üÿðüð|þüþðüpþ
14     00:05:01.269      ,4B,CRC:1144a915
15     00:05:01.643      ,4B,end0þüüpüü|ððü
```

Figure 3.9.: Example of corrupt data recorded from the serial line during testing.

type of SEFI; however, in this work we will distinguish between the two for clarity.

SEFI faults can interfere with the memory test program and the determination of SEU error rates. If the fault persists, then a two-second power cycle is performed on the malfunctioning DUT. Some examples of SEFI faults include:

- The re-initialization of a dataword fails during a memory scan.

- The DUT becomes unresponsive.

- The DUT outputs produce incorrectly formatted data. An example of corrupted data is shown in Fig. 3.9.

The testing method used in this experiment is referred to as *dynamic mode testing*. In *dynamic mode testing*, a continuous write-read sequence is performed during beam exposure [76]. In contrast, during *static mode testing*, the memory is initialized before beam exposure and then read back and the data verified after delivering a particular dose. While static mode testing can simplify data collection by avoiding faulty behavior during exposure, it ignores detecting potential vulnerabilities to SEFI fault modes.

Table 3.1.: Technical details of the tested devices.

	Manufacturer Part No.	Manufacturer	Word Size	SRAM	SRAM Test Array	Flash
A	M430FR5989SRGCREP	Texas Instruments	16-bit	16 kbit	14 kbit	1 Mbit
B	EFM32GG11B820F2048	Silicon Labs	32-bit	4096 kbit	3940 kbit	16 Mbit
C	AT32UC3C0512C-ALZR	Atmel	32-bit	512 kbit	480 kbit	4 Mbit
D	M2S010-TQG144I	MicroSemi	32-bit	512 kbit	448 kbit	2 Mbit

3.6. Testing Results

Some details about the four different DUT types that were tested are summarized in Table 3.1. "SRAM Test Array" indicates the size of the array allocated for the memory scan loop in SRAM. Five copies of each of the four DUT types were tested (20 DUTs in total) at four to six different energies and five different incidence angles. Figs. 3.10 and 3.11 show the SEU cross-section data collected at TRIUMF. This data was obtained during a total of 4 hours of testing time, including setup and tear-down. The testing platform performed well and the results obtained can be analyzed for comparison with other devices or used to predict the SEU sensitivity in known radiation environments.

3.6.1. SEU Cross-sections

Dynamic mode testing is effective for identifying vulnerabilities to SEFI faults. However, those SEFI faults might lead to certain memory test cycles being invalidated. Consequently, the faulty behavior from a SEFI fault could inaccurately influence the count of SEU faults reported within that particular test cycle. Thus, to ensure accurate SEU cross-section calculations, it becomes necessary to subtract the radiation dose delivered during these faulty test cycles from the overall effective dose that contributes to the SEU faults. Intervals when the DUT is powered off must also be subtracted.
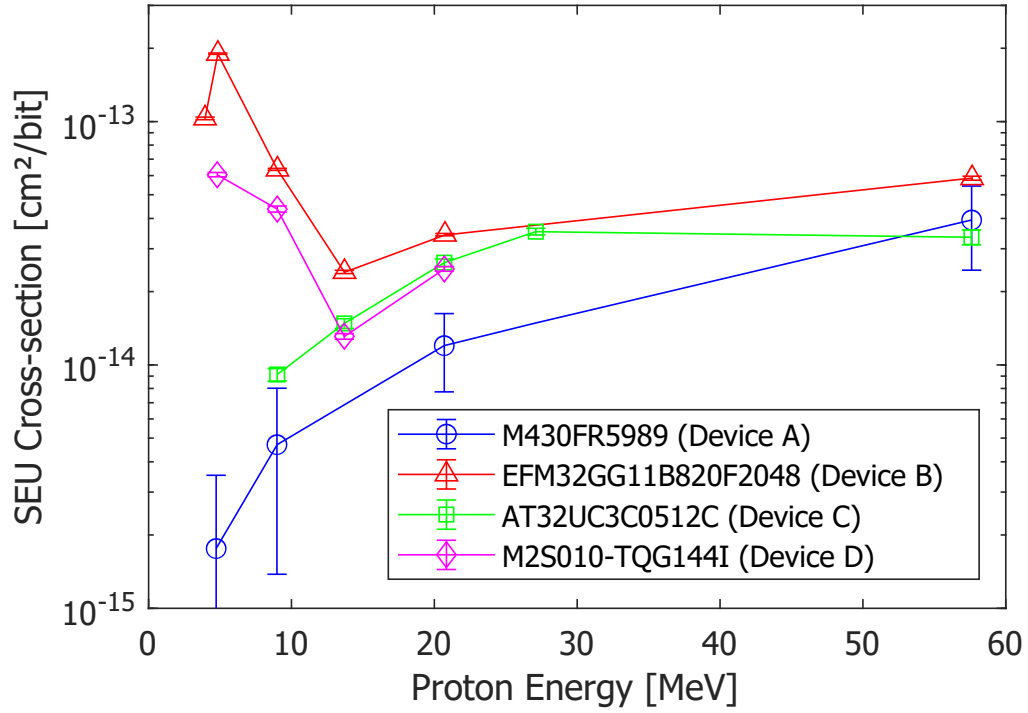
Figure 3.10.: SEU cross-section of the AT32UC3C0512C's SRAM.

Table 3.2.: Classification of fault behaviors recorded during testing.

SEU	SEL	Other Faulty Behaviour	DUT Failed	Occurrences for each DUT				Fault Description
				A	**B**	**C**	**D**	
Yes				18	58547	2772	7064	SRAM SEU
		Yes		0	8	376	361	SEFI
	Yes			0	5	0	0	SEL
	Yes	Yes		0	0	0	3	SEL and SEFI
	Yes		Yes	0	0	3	3	SEL causing Failure

3.6.2. Fault Behavior Classification

The total tallies of different types and combinations of fault behaviors that were observed during normal incidence testing are summarized in Table 3.2. A total of six devices (three M2S010-TQG144I MPSoCs and three M430FR5989SRGCREP MCUs) failed permanently when a SEL fault occurred but did not result in sufficiently high current to trigger the over-current protection circuit.

Any memory test cycle for which the recorded data was invalid in a detectable way (such as invalid syntax or a non-consecutive cycle number) was counted as a SEFI fault. While counting rates of SEU faults is relatively straightforward and directly comparable between devices, recording and classifying SEFI faults can be a significant challenge. SEFI faults can render the DUT completely nonfunctional and different types of SEFIs can exhibit the same symptoms and are thus difficult to classify in a meaningful way [54]. Some of the faulty behaviors that were observed are described below for each type of chip.

3.6.2.1. (Device A) M430 SEFI Behaviors

- The only errors observed were 18 SRAM SEUs.

3.6.2.2. (Device B) EFM32 SEFI Behaviors

- In only one instance a DUT (of any processor variety) this processor stopped responding over the serial line, not attributed to a SEL. The average current consumption decreased until the automatic 2-second watchdog timer automatically triggered a power cycle.

- In 7 instances, the DUTs reported instantaneous write errors for a high percentage of memory addresses until the DUT was power cycled. Each such instance was tallied as one SEFI.

- For one DUT, a single bit became stuck, reporting as a SEU for every memory scan, even when the beamline was turned off. After allowing the test code to continue running for about 15 minutes, the faulty bit appeared to return to normal operation. The SEUs counted for this bit during that period were discounted from the SEU cross-section calculations.

- The rate of SEFI faults increased significantly at lower incidence angles.

3.6.2.3. (Device C) AT32 SEFI Behaviors

- In 373 out of 13253 memory test cycles of all 0's, the first (i.e., at index 0) 32-bit word in the tested memory region was read as 0x66000000.

3.6.2.4. (Device D) M2S SEFI Behaviors

- In 399 out of 7599 memory test cycles of all 0's, the first (i.e., at index 0) 32-bit word in the tested memory region was read as 0x66666666. This behavior is possibly related to the SRAM cell layout, such as when alternate cells have mirrored layouts.

- In 39 instances, bytes sent over the serial line would be corrupted, as shown in Section 3.5.4.

Table 3.3.: Incidence angle testing data.

DUT	Angle	SEU	SEFI	SEL	SEL Cross-section
A	90°	7	0	0	$< 2.08 \times 10^{-11} \text{cm}^2$
A	82.5°	21	0	0	$< 2.91 \times 10^{-11} \text{cm}^2$
A	75°	28	0	0	$< 2.27 \times 10^{-11} \text{cm}^2$
A	67.5°	16	0	0	$< 3.08 \times 10^{-11} \text{cm}^2$
A	45°	9	0	0	$< 3.68 \times 10^{-11} \text{cm}^2$
B	90°	415	192	5	$8.68 \times 10^{-11} \text{cm}^2$
B	82.5°	2332	306	10	$2.91 \times 10^{-10} \text{cm}^2$
B	75°	1449	342	14	$3.17 \times 10^{-10} \text{cm}^2$
B	67.5°	1611	206	12	$3.69 \times 10^{-10} \text{cm}^2$
B	45°	395	144	22	$8.11 \times 10^{-10} \text{cm}^2$
C	90°	22	1	3	$5.21 \times 10^{-11} \text{cm}^2$
C	82.5°	66	0	0	$< 2.91 \times 10^{-11} \text{cm}^2$
C	75°	285	0	0	$< 2.27 \times 10^{-11} \text{cm}^2$
C	67.5°	113	0	0	$< 3.08 \times 10^{-11} \text{cm}^2$

3.6.3. Incidence Angle Testing

With the beamline at a lower incidence angle, the energy deposited by penetrating protons in the sensitive plane of the DUT is higher due to a longer trajectory through this region. Therefore, an increase in SEEs is expected for smaller incidence angles. Indeed, the test results included in Table 3.3 show a significant increase in SEL and SEFI fault rates. Fig. 3.11 shows the calculated SEU cross-section data.

3.7. Future Considerations

Perhaps the most significant complicating factor in the development of this testing platform was the range of unexpected faulty behaviors encountered during irradiation. Even after multiple design iterations, there is still room for improvement to achieve suitable handling of all faulty behaviors. More sophisticated fault classification meth-
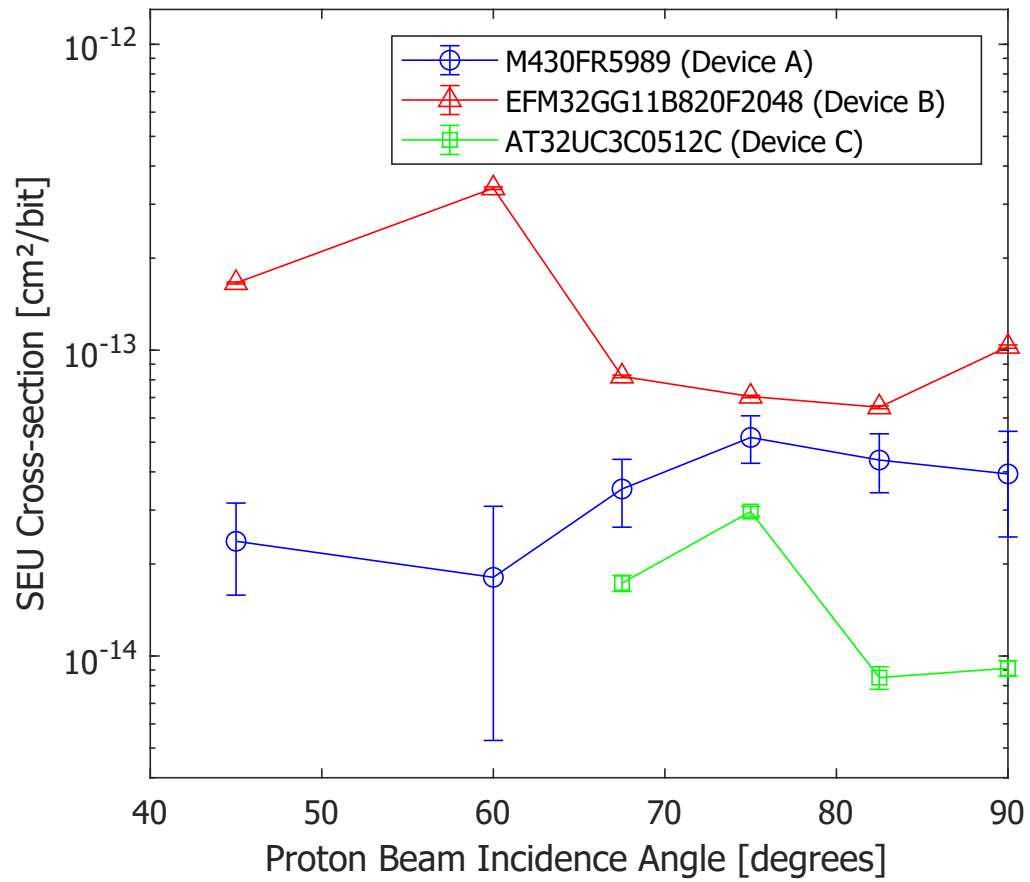
Figure 3.11.: SEU cross-section for 57.6-MeV protons versus different incidence angles.

ods could further improve ease and efficiency of testing. If this open-source design is adopted by other groups, lessons learned from each team of users could contribute to better fault modeling and detection.

During DUT malfunctions or power cycles, the test data output by the DUT may become inaccurate. SEEs tallied during such instances should be omitted, along with the corresponding fluence. This exclusion slightly lowers the effective dose used for calculating SEE cross-sections. In this experiment, we recorded the cumulative total dose at the end of each test. The effective dose used for SEE rate calculations was determined by subtracting the dose received during malfunctions or power cycles. We made the assumption that the fluence rate remained constant throughout each test. However, there were fluctuations in the instantaneous fluence rate during the test, which reduced the accuracy of the calculated SEE. To mitigate this potential source of error, it would be advisable to record the instantaneous fluence rate throughout the test.

In future work, the development of a console-side user interface that offers real-time statistical analysis of recorded data would be highly beneficial. Providing this real-time information would allow the operator to identify optimal radiation energy values based on trends observed in the resulting energy spectrum of measured fault cross-sections. Additionally, enhancing the software interface to enable users to define efficient test schedules would be advantageous. For instance, users could conduct a sweep of various incidence angles with specified time intervals, minimizing downtime in between tests.

3.8. Conclusions

Radiation effects are a significant consideration in the design of electronics for space applications [53]. CubeSats operating in LEO can effectively utilize cost-effective COTS components that have been found to have reasonably good radiation tolerance, instead of using radiation-hardened components that are expensive and difficult to procure. Using traditional methods to evaluate the susceptibility of COTS components to radiation effects is too complex and costly for many groups that are developing CubeSats.

This project aimed to develop a platform that allows efficient, accurate, and cost-effective measurements of SEE rates, including SEU, SEL, and SEFI faults on devices, with minimal complexity for test setup. An automated and remotely controlled, modular testing platform was developed, permitting up to 24 different devices to be tested during a single experiment while minimizing the setup time and the need for human intervention during the testing. The testing platform also allows the incidence angle of the beamline to be adjusted to any angle.

Overall, the final prototype of the testing platform performed well and provided a substantial amount of useful data within a short timeframe. During a four-hour experiment, 20 individual devices were tested at varying energies and incidence angles. A speculative estimate suggests that approximately 20 minutes of cool-down time and 10 minutes of setup time would have been required between each of the five DUT motherboards that were tested. Therefore, this automated testing platform saved approximately two hours of time, or 30 minutes per each of the four different devices. At the time of this writing, TRIUMF's pricing is USD $950 per hour. That amount of cost savings could be substantial relative to the often limited budgets of university CubeSat groups. The collected data can now be used to compare the DUTs to devices

tested in other experiments or to estimate error rates in orbit.

The software and hardware developed for this project are being released under an open source license. Our aim is to significantly reduce the cost, development time and beamline leasing time required for CubeSat developers to assess the radiation sensitivity of devices, especially those lacking published radiation sensitivity characteristics – which is commonly the case for commodity commercial-grade parts. This initiative opens the door for more published test data on more devices, including non-hardened commercial-grade components that are attractive to budget constrained CubeSat developers. Through collaborative open-source development, the testing platform can continue to evolve, incorporating improved automation and advanced fault modeling.

Ultimately the testing platform and methodology outlined in this work should alleviate some of the trial-and-error challenges faced by CubeSat developers during radiation testing. This, in turn, will simplify the process of designing more reliable spacecraft components at a lower cost, thereby expanding the capabilities of the broader space industry.

4. Proton-Beam Testing of Microcontrollers

4.1. Introduction

As CubeSat developers reach for increasing sophistication by integrating newer, high-density *integrated circuits* (ICs) into payloads and avionics, there is a growing need for rapid and inexpensive assessment of radiation effects and in-orbit error rate predictions. To support CubeSat developers in assessing the effects of radiation on component reliability, a versatile open-source radiation effects testing platform was developed to support efficient particle accelerator testing of ICs, such as *microcontrollers* (MCUs). This testing platform uses automation to minimize human interaction in the radiation testing chamber. This allows the tester to maximize testing efficiency, testing more devices in less time. Using that testing platform, five each of four different ICs were tested including MCUs and *microprocessor system-on-a-chips* (MPSoCs). Testing was done at the TRIUMF Proton Irradiation Facility [55] in Vancouver, Canada. The testing platform recorded *single-event effects* (SEEs) including *single-event upsets* (SEUs) in the volatile memories of the *devices under test* (DUTs) as well as *single-event latchups* (SELs) and *single-event function interrupts* (SEFIs). SEU cross-sections were deter-

mined at different energies and at different incidence angles including 90° (normal), 82.5°, 75°, 67.5°, 60°, and 45°. An initially near mono-energetic 65 MeV proton beam was used through a Lucite degrader wheel, shown in Fig. 4.1. The degrader thickness was varied to modulate the mean energy between 3.9 MeV and 57.6 MeV. On-orbit SEE rates of the devices tested were calculated and compared by combining these results with models of the radiation flux in *low Earth orbit* (LEO).

4.2. Experiment Design

4.2.1. Radiation Sources

Testing was done at the TRIUMF Proton Irradiation Facility in Vancouver, Canada [55]. Protons were delivered to the test area with a mean energy of 65 MeV and a *full-width half-maximum* (FWHM) of 1.2 MeV. To produce an accurate estimate of SEU rates in orbit based on data obtained while using the cyclotron, the error rates must be determined over a range of proton energies. While measuring SEE rates at a single proton energy can provide an approximation of on-orbit performance [77], testing over a range of energies should improve the accuracy of the determined on-orbit SEE rate. In this experiment, the proton energy incident on the DUT was varied by inserting a degrader, provided by TRIUMF, inline with the beam. The degrader, shown in Fig. 4.1, was a clear Lucite disk with a wedge cut along the radius of a clear acrylic disk. By rotating the disk, the thickness of material in the beamline was varied to modulate the mean energy of the beam. As the degrader thickness is increased, the mean proton energy incident on the DUT decreased to a minimum of 2.4 MeV with a FWHM of 2.4 MeV. Using the thinnest portion of the degrader, the maximum mean
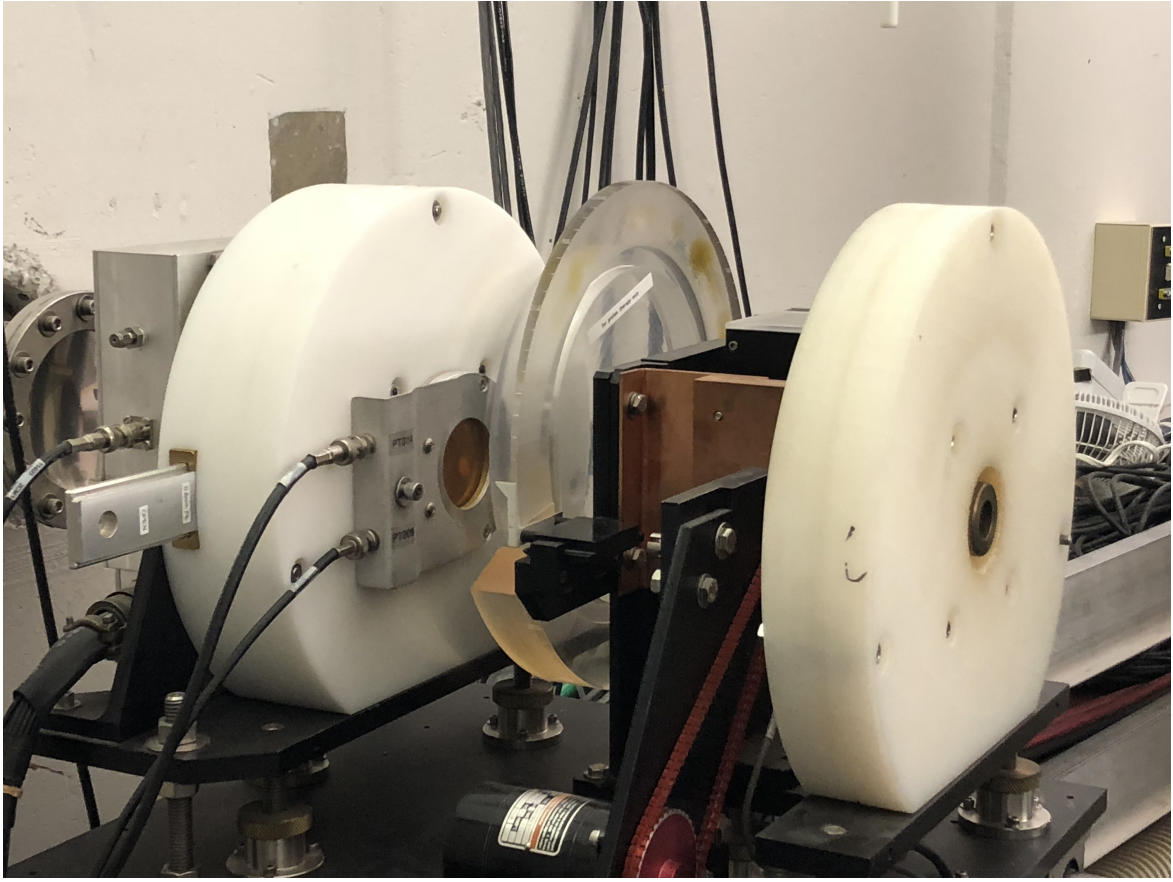
Figure 4.1.: Energy-modulating degrader wheel, provided by TRIUMF at the TRI-
UMF Proton Irradiation Facility. By rotating the clear-acrylic disk, which has a
wedge cut along its radius, the kinetic energy of the beam is modulated.

proton energy was 57.6 MeV with a FWHM of 1.4 MeV.

After passing through the degrader, the proton bean passes through a square aperture

made of thick aluminum. This ensures that only the intended 5×5 cm target is

irradiated. Ambient radiation from the activation of long-lived isotopes in the testing

area exists but is considered negligible in this work.

4.2.2. Test Setup

Testing was done using the remotely controlled robotic testing platform that was presented in Chapter 3. The testing platform, shown in Fig. 4.2, detects and logs SEEs and cycles DUT power if a SEL or a SEFI fault are detected. A stepper motor, in the DUT selector, rotates the assembly to position the DUT motherboards within the 5×5 cm beamline. Each DUT motherboard has four DUT card slots, each with a monitored power supply and a 1-MHz serial interface. On one of the DUT motherboards, the incidence angle is varied using a servo motor. After the initial setup of the testing platform, all manipulation is done remotely or automatically. This solution improves the utilization of costly testing time, maximizing the amount of useful data that can be obtained during the experiment.

The final iteration of the testing platform was successfully implemented at TRIUMF with a total of 20 DUTs arranged with four on each of five DUT motherboards. The sixth DUT motherboard was unused in this experiment. The 20 DUTs included MCUs and MPSoCs which are listed below:

- DUT Board 1: $4 \times$ M430FR5989SRGCREP (Device A)

- DUT Board 2: $4 \times$ EFM32GG11B820F2048 (Device B)

- DUT Board 3: $4 \times$ AT32UC3C0512C-ALZR (Device C)

- DUT Board 4: $4 \times$ M2S010-TQG144I (Device D)

- DUT Board 5: One of each of the above devices

- DUT Board 6: Not populated

The fifth DUT board was used for testing varied incidence angles. Fig. 4.3 illustrates the arrangement of DUTs and Table 4.1 lists some details of each device as tested.

DUT slot

DUT motherboard

**DUT motherboard
with servo motor**

DUT selector

servo motor
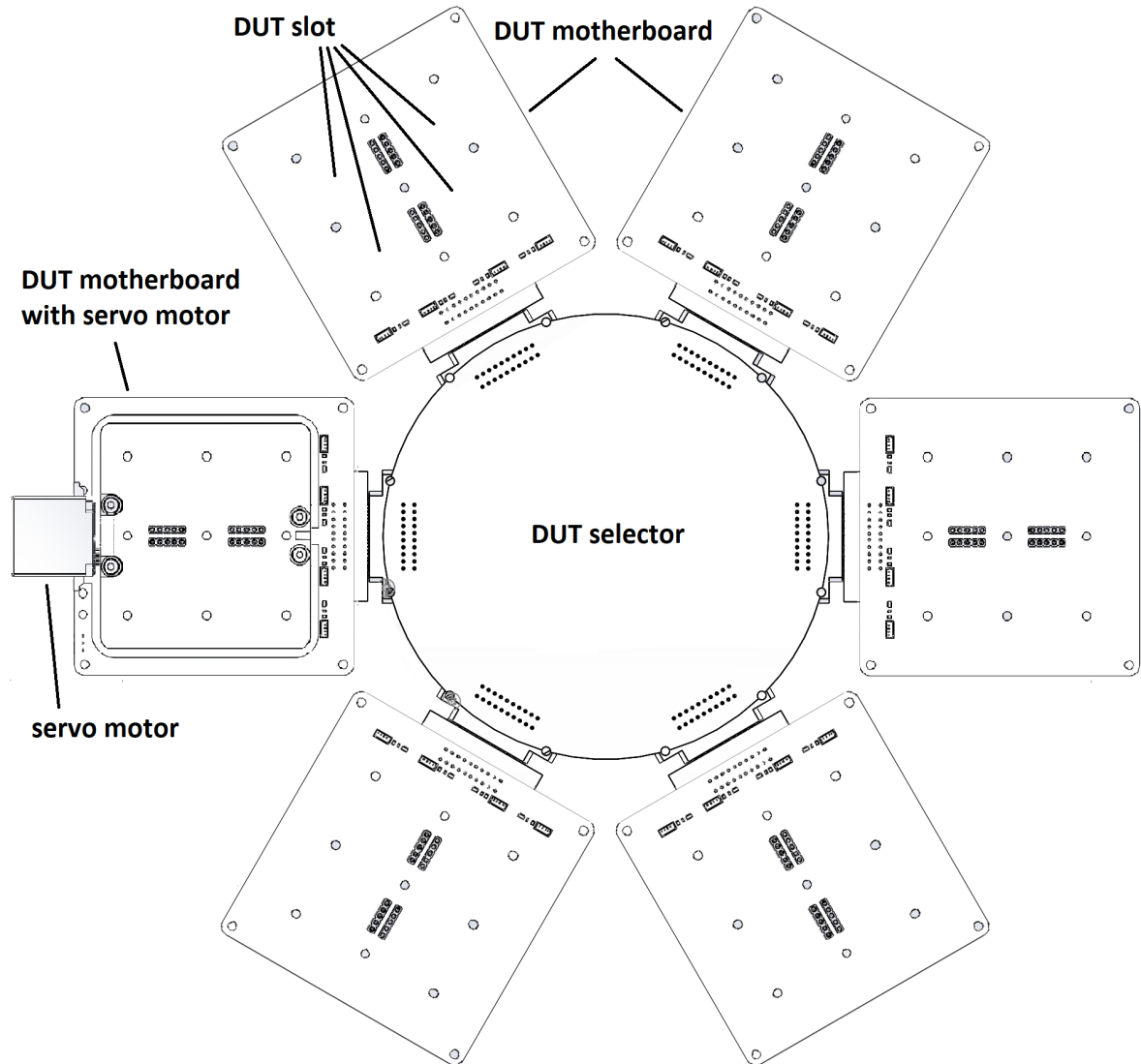
Figure 4.2.: Labelled drawing of the front face (oriented towards the oncoming proton beam) of the rotating testing platform used for positioning the DUTs during testing.

Table 4.1.: Technical details of the four devices.

Manufacturer Part No.	Manufacturer	Word Size	SRAM	Flash	Core Freq.	Process
M430FR5989SRGCREP	Texas Instruments	16-bit	16 kbit	1 Mbit	16 MHz	130 nm [78]
EFM32GG11B820F2048	Silicon Labs	32-bit	4096 kbit	16 Mbit	72 MHz	90 nm [79]
AT32UC3C0512C-ALZR	Atmel	32-bit	512 kbit	4 Mbit	50 MHz	?
M2S010-TQG144I	MicroSemi	32-bit	512 kbit	2 Mbit	166 MHz	65 nm [80]

The sixth DUT board was not used.
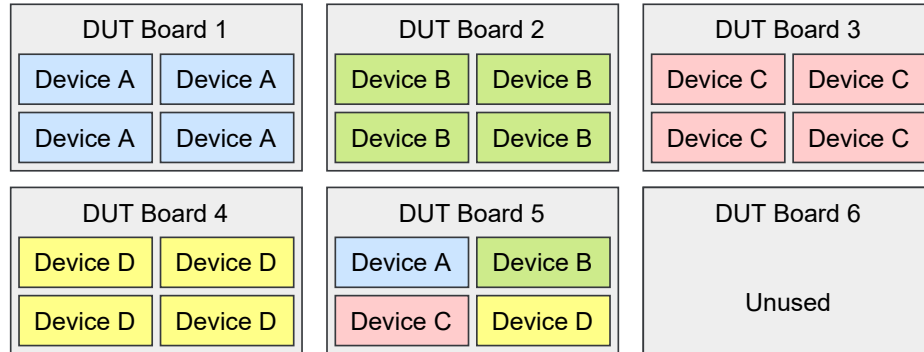
Figure 4.3.: A summary of the arrangement of DUTs during testing.

During the 4-hour experiment, 22 tests were performed on the 20 devices, 4 devices at a time. The proton energy and incidence angle were varied between the tests.

4.2.3. SEE Detection

As the test progresses, SEEs are detected and recorded by the data logger and displayed on the connected terminal in the control room in real-time. The test cycle to detect SEUs begins by initializing a region of memory, alternating between all 1's and all 0's. Immediately after initializing each dataword, the value is read back to ensure that the operation was successful. After initialization is completed, a checksum of the *non-volatile memory* (NVM). is done, providing a brief delay and a method for detecting SEUs in the NVM. After the checksum is completed, the cycle begins again but this

time each data word of the test region is also read before reinitilizing it to check if any bits have unexpectedly changed. When an erroneous bit is detected, the value read, the expected value, and the address of the dataword are recorded along with a timestamp in milliseconds. The sizes of each test region are listed in Table 4.2.

Table 4.2.: Sizes of the test regions being scanned for SEU faults in each DUT.

Manufacturer Part No.	SRAM Test Size
M430FR5989SRGCREP	14 kbits
EFM32GG11B820F2048	3840 kbits
AT32UC3C0512C-ALZR	480 kbits
M2S010-TQG144I	448 kbits

SEL faults are recorded when a DUT sustains current consumption beyond a pre-configured threshold value for 1 second. Current is measured by sense resistor current sensors with a least significant bit resolution of $62\,\mu\text{A}$. When an SEL fault is detected, power to the affected DUT is turned off for 2 seconds before attempting to restart the DUT and re-establish communication. A timestamp is recorded for the fault when the over-current is registered and can be correlated with current sensor data that is sampled at $100\,\text{Hz}$. The measured average current consumption of each type of DUT and the corresponding pre-configured latchup threshold values that were used during testing are listed in Table 4.3.

Table 4.3.: The measured average operating current of each DUT and the pre-configured current threshold used for detection of SEL faults.

Manufacturer Part No.	Average Current	SEL Threshold
M430FR5989SRGCREP	6.4 mA	30 mA
EFM32GG11B820F2048	20.0 mA	50 mA
AT32UC3C0512C-ALZR	62.3 mA	100 mA
M2S010-TQG144I	123.4 mA	150 mA

Any other fault that interrupts the testing in a detectable way is classified as a SEFI fault. Using a static testing method where the system clock is disabled during irradiation and reread after could mitigate SEFI faults during the test but would provide less information about vulnerability of the DUT to SEFI faults. When a malfunction is detected, such as garbled or missing communication or a failure to write content to memory, the affected DUT is turned off for 2 seconds before attempting to restart the DUT and re-establish communication.

4.3. Results

The *SEU cross-section* from each test was calculated as the number of SEUs over the total fluence received minus the fluence that was received while a device was unresponsive or while power to the device was turned off. The resulting fluence value is the *effective fluence.* Where data exists for multiple similar DUTs at the same proton energy and incidence angle, the fluence values and SEU counts are added together such that the resulting SEU cross-section is the weighted average based on the number of SEUs recorded during that test for each similar device. The results recorded during each test are presented in Table 4.4. No changes in checksum values were recorded during the testing indicating that zero SEU faults occurred in the NVM of any DUT.

To evaluate the repeatability of the experiment, Table 4.5 shows the *SEU cross-section* results for each individual EFM32GG11B820F2048 MCU (Device B) at each of the tested energies. The error crossections measured on each individual DUT agreed within 10% of the combined averages. Some sources of error that could affect the repeatability of this experiment are, random shot noise consistent with modeling SEUs as a Poisson process [81], non-uniform flux density of the proton beam and manufacturing variability

Table 4.4.: Summary of SEE data recorded during proton-beam testing at TRIUMF.

Device	Board No.	Proton Energy	Effective Fluence	SEUs	SELs	SEFIs	SEU Cross-section
A	1	4.8 MeV	4.07×10^{10} /cm^2	1	0	0	1.76×10^{-15}cm^2/bit
A	1	9 MeV	3.04×10^{10} /cm^2	2	0	0	4.70×10^{-15}cm^2/bit
A	1	20.7 MeV	4.75×10^{10} /cm^2	8	0	0	1.20×10^{-14}cm^2/bit
A	5	57.6 MeV	1.27×10^{10} /cm^2	7	0	0	3.94×10^{-14}cm^2/bit
B	2	3.9 MeV	1.68×10^{10} /cm^2	6628	0	0	1.03×10^{-13}cm^2/bit
B	2	4.8 MeV	3.47×10^{10} /cm^2	25307	0	0	1.90×10^{-13}cm^2/bit
B	2	9 MeV	4.79×10^{10} /cm^2	11707	1	0	6.36×10^{-14}cm^2/bit
B	2	13.7 MeV	4.43×10^{10} /cm^2	4107	0	0	2.71×10^{-14}cm^2/bit
B	2	20.7 MeV	6.05×10^{10} /cm^2	7986	1	4	3.43×10^{-14}cm^2/bit
B	5	57.6 MeV	1.25×10^{10} /cm^2	2812	1	1	5.85×10^{-14}cm^2/bit
C	3	9 MeV	6.53×10^{10} /cm^2	286	1	1	9.12×10^{-15}cm^2/bit
C	3	13.7 MeV	6.58×10^{10} /cm^2	466	0	0	1.48×10^{-14}cm^2/bit
C	3	20.7 MeV	6.34×10^{10} /cm^2	801	0	0	2.63×10^{-14}cm^2/bit
C	3	27.1 MeV	6.00×10^{10} /cm^2	1015	1	0	3.53×10^{-14}cm^2/bit
C	5	57.6 MeV	1.27×10^{10} /cm^2	204	0	0	3.35×10^{-14}cm^2/bit
D	4	4.8 MeV	8.73×10^{10} /cm^2	2366	1	0	6.05×10^{-14}cm^2/bit
D	4	9 MeV	6.24×10^{10} /cm^2	1222	0	0	4.37×10^{-14}cm^2/bit
D	4	13.7 MeV	24.2×10^{10} /cm^2	1417	1	1	1.31×10^{-14}cm^2/bit
D	4	20.7 MeV	18.5×10^{10} /cm^2	2059	0	0	2.48×10^{-14}cm^2/bit
D	5	57.6 MeV	Device failed due to SEL	-	1	-	-

Table 4.5.: *SEU cross-section* results for each individual EFM32GG11B820F2048 (Device B) MCU at each of the energies tested.

Proton Energy	Device B1	Device B2	Device B3	Device B4	Combined Average
3.9 MeV	1.03×10^{-13}	9.64×10^{-14}	1.07×10^{-13}	1.06×10^{-13}	1.03×10^{-13}
4.8 MeV	1.86×10^{-13}	1.82×10^{-13}	1.97×10^{-13}	1.94×10^{-13}	1.90×10^{-13}
9 MeV	6.22×10^{-14}	5.99×10^{-14}	6.63×10^{-14}	6.59×10^{-14}	6.36×10^{-14}
13.7 MeV	2.69×10^{-14}	2.57×10^{-14}	2.79×10^{-14}	2.79×10^{-14}	2.71×10^{-14}
20.7 MeV	3.55×10^{-14}	3.14×10^{-14}	3.70×10^{-14}	3.32×10^{-14}	3.43×10^{-14}
57.6 MeV	6.00×10^{-14}	5.33×10^{-14}	5.77×10^{-14}	6.30×10^{-14}	5.85×10^{-14}
	cm^2/bit	cm^2/bit	cm^2/bit	cm^2/bit	cm^2/bit

between individual devices.

4.3.1. Single-Event Latchup

Sense-resistor-based current sensors were used to continuously monitor DUT current consumption during testing so that SEL faults could be detected. While testing with a 90° incidence angle, SEL faults were recorded in each type of DUT except the M430FR5989SRGCREP MCUs. Fig. 4.4 shows an example of a SEL fault in a

EFM32GG11B820F2048 MCU. In this case, detection of the SEL by the testing platform was delayed by a few seconds due to latency caused by buffering of the current sensor data. Before and after the SEL fault, the current consumption fluctuates periodically with each test cycle. The number of SEL faults recorded was not sufficient to allow any additional insight. As the incidence angle was decreased, the number of SEL faults recorded in the EFM32GG11B820F2048 MCUs increased significantly. Early in test 1, Device D (a M2S010-TQG144I MPSoC) experienced a latchup event with an average current consumption of around 140 mA and it permanently failed shortly after. This failure is referred to as a *single-event burnout* (SEB) Because this was below the pre-configured threshold, which was set to 150 mA, the SEL detection was not triggered. A total of six devices (three M2S010-TQG144I MPSoCs and three M430FR5989SRGCREP MCUs) failed in this way.
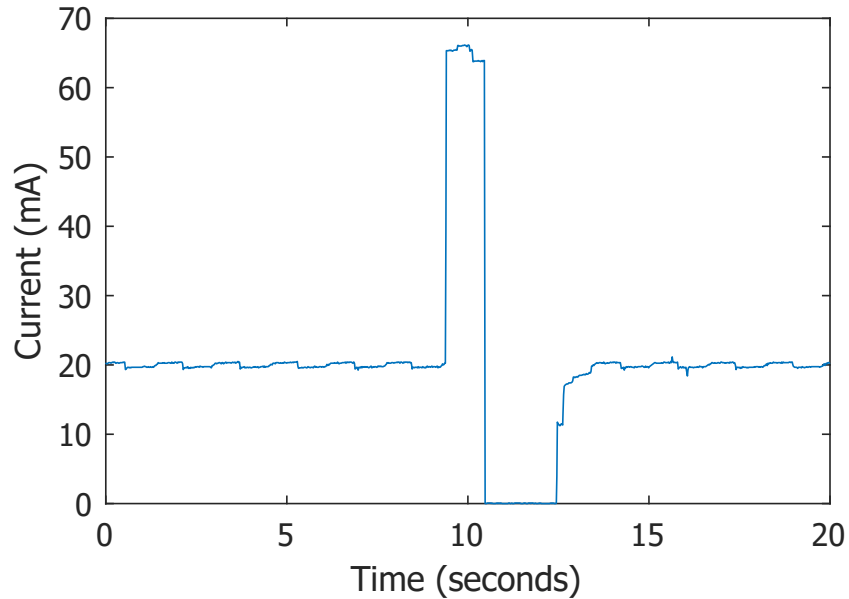
Figure 4.4.: Current consumption recorded during a single-event latchup fault, including overcurrent detection, shutoff, and resume.

4.3.2. Single-Event Functional Interrupts

Several anomalies occurred in the recorded data which were counted as SEFI faults. In most of these cases, serial data transmitted from the DUTs appeared corrupted, as shown in Fig. 4.5. This is caused by SEUs within the working memory of the SEU causing faulty behaviour. In some other cases, which mostly occurred in the EFM32GG11B820F2048 devices, the re-initialization step of the memory test cycle failed such that the value read immediately after attempting to overwrite the memory was not the expected value. In most cases this condition persisted until the DUT was power cycled. While testing with a 90° incidence angle, SEFI faults occurred in each type of DUT except the M430FR5989SRGCREP MCUs.

Table 4.6.: Numbers of SEU, SEL, and SEFI faults recorded with different incidence angles.

Angle	Fluence	SEU			SEL			SEFI		
82.5°	3.43×10^{10} /cm^2	21	8570	140	0	10	0	0	2	0
75°	4.41×10^{10} /cm^2	32	11947	628	0	14	0	0	8	0
67.5°	3.25×10^{10} /cm^2	16	10244	270	0	12	1*	0	3	0
60°	0.79×10^{10} /cm^2	2	10266	-	0	3	-	0	3	-
45°	2.71×10^{10} /cm^2	9	17258	-	0	22	-	0	12	-
Device:		A	B	C	A	B	C	A	B	C

*Failed due to burnout caused by SEL fault with current below threshold

```
00    00:04:59.626    ,4B,ram
01    00:04:59.773    ,4B,RE:8
02    00:04:59.899    ,4B,nvm
03    00:05:00.025    ,4B,CRC:5df3fc83
04    00:05:00.298    ,4B,end81'ðÀ~ü
05    00:05:00.530    ,4B,boc
06    00:05:00.545    ,4B,2amp
07    üüü|þüüü|üüðððüðü|
08    00:05:00.571    ,4B,RE:0
09    00:05:00.572    ,4B,nvmüÿü|üü|üð
10    üü?üðpüð|üþðü||üüðüü
11    ðüüpüü
12    þüüüðüþðüðüð|üððüüðüüüüüðüü
13    ðþüüüü?|üüüðüþðü||üÿðüð|þüþðüpþ
14    00:05:01.269    ,4B,CRC:1144a915
15    00:05:01.643    ,4B,end0þüüpüü|ððü
16    üüðüþüü|ðüü|
17    00:05:01.793    ,4B,boot
18    00:05:02.150    ,4B,ram
19    00:05:02.167    ,4B,RE:0
20    00:05:02.168    ,4B,nvm
21    00:05:02.168    ,4B,CRC:5df3fc83
22    00:05:02.169    ,4B,end0
```

Figure 4.5.: Screenshot of corrupted data being recorded during testing due to a SEFI fault.

4.3.3. Varied Incidence Angles

To test the dependence of SEEs on the incidence angle of incoming radiation, the devices were tested at different angles. A servo motor was used to rotate a DUT board with one of each of the four different devices tested, in the beamline. Testing was done with 57.6-MeV protons at 82.5°, 75°, 67.5°, 60° and 45° incidence angles. Table 4.6 lists the number of SEEs recorded for each device. Because Device D had failed earlier in the experiment, it is not included here. While testing with a 67.5° incidence angle, a SEL fault occurred in Device C (a AT32UC3C0512C-ALZR MCU) at an average current around 80 mA. Because the pre-configured threshold was set to 100 mA for this device, the SEL fault was not detected and the device failed. Fig. 4.6 shows the corresponding SEU cross-sections, calculated using the effective fluence received by each device, which accounts for time when the device was unresponsive or turned off.
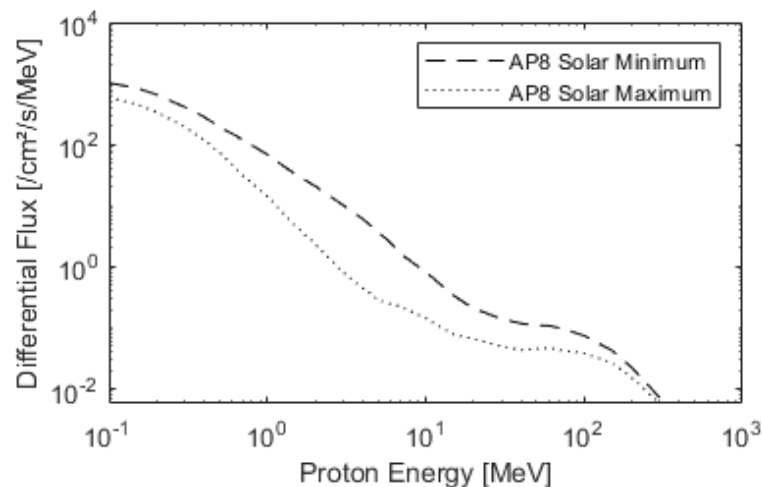
4.4. Predicting SEU Rates in Low Earth Orbit

Figure 4.7.: Average differential proton flux from AP8 model at ISS orbit (400 km, 51.6°) [1, 8].

61
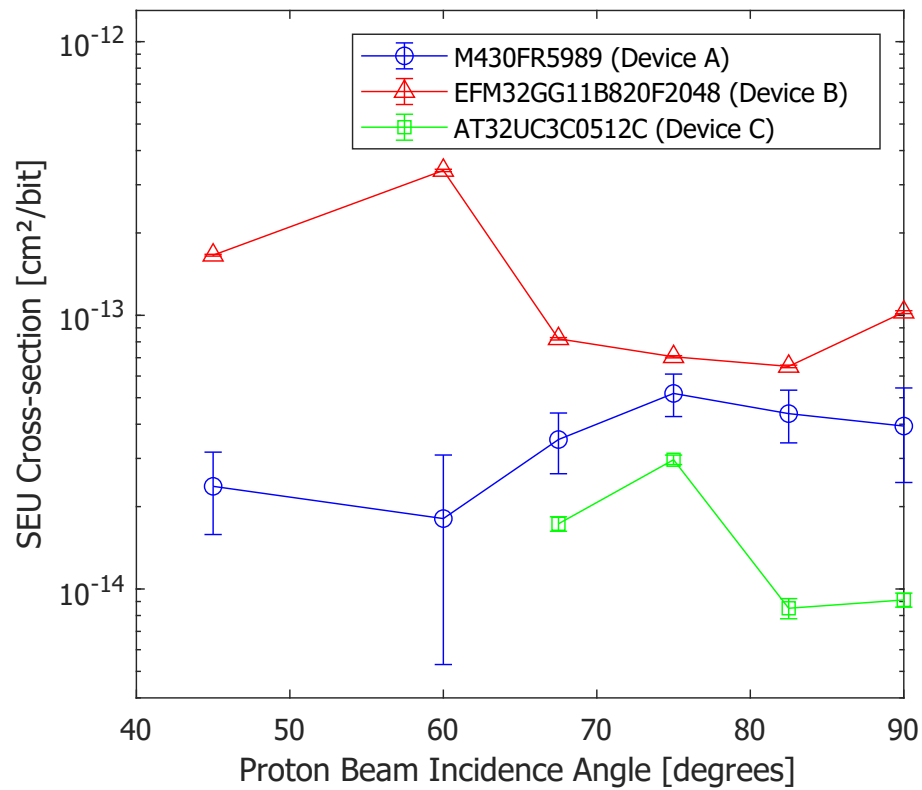
Figure 4.6.: SEU cross-section versus incidence angle in the proton beamline.

When testing the radiation hardness of a component for use in a particular environment, such as space, the tester hopes to accurately predict how the component will behave in that environment. Testing in a particle accelerator gives information on how a component will respond to intense radiation, but such testing most likely produces a radiation spectrum very different from that in the actual operating environment. In this section, the testing results obtained are combined with information about the radiation environment seen by a spacecraft in LEO.

The average SEU rate R_{SEU} in a known radiation environment can be determined as the integral of the product of the SEU cross-section σ_{SEU} and the differential proton flux spectra $d\Phi/dE$ over the energy range [82].

$$R_{SEU} = \int_E \frac{d\Phi}{dE} \sigma_{SEU}(E) \cdot dE \tag{4.1}$$

NASA's radiation belt model, AP8, gives the proton flux spectra down to LEO and is freely available [8]. Fig. 4.7 shows the average differential proton flux spectrum for the ISS orbit with 400 km altitude and 51.6° inclination during both solar minimum and solar maximum in the year 2020. Table 4.7 shows the calculated in-orbit SEU rates and *mean time between failures* (MTBF) for the devices assuming 1 mm of aluminum shielding.

Table 4.7.: Calculated proton induced OOSR for the devices tested, calculated using SPENVIS [1].

Manufacturer Part No.	SEU Rate (/bit/day)	MTBF per Device
M430FR5989SRGCREP	5.09×10^{-8}	1226.9 days
EFM32GG11B820F2048	9.47×10^{-8}	2.6 days
AT32UC3C0512C-ALZR	4.99×10^{-8}	39.1 days
M2S010-TQG144I	6.10×10^{-8}	45.9 days

4.5. Conclusions

Four different types of MCUs or MPSoCs were tested for sensitivity to SEUs using protons between 2.4 MeV and 57.6 MeV. Using the AP8 model for proton flux in Earth orbit, the in-orbit error rates were calculated for each device.

The EFM32GG11B820F2048 MCUs, which has the most features and the highest memory capacity of all of the devices tested, showed the highest sensitivity to SEEs. When the incidence angle was reduced, the number of SEL and SEFI faults in those devices increased significantly. The M430FR5989SRGCREP MCUs, which have the fewest features and the lowest memory capacity, showed by far the lowest sensitivity to SEUs and showed no sensitivity to SEL or SEFI faults during the testing. This result could be due to the higher-density devices having smaller feature sizes for their SRAM cells, thus making them more vulnerable to radiation effects.

The results of this experiment can be used to inform the design and reliability analysis of CubeSat components. The appropriate selection must be made based on a combination of the system requirements and the estimated error rates evaluated against the margin for acceptable risk. For example, although the M430FR5989SRGCREP MCUs had the lowest error rate out of the devices tested, the limited features and memory capacity of this devices may be insufficient for a particular application.

5. Low-Energy Proton Effects

5.1. Introduction

As modern semiconductor technology moves towards smaller and smaller feature sizes, devices have become vulnerable to direct ionization from *low-energy protons* (LEPs) [83–85]. In the past, LEPs could be ignored because the energy imparted by the protons through direct ionization would not cause enough movement of charge in the device to result in a fault. However, in 2006, Rodbell *et al.* [83] observed large *single-event upset* (SEU) cross-sections from LEPs, raising concerns that this new mechanism could significantly increase error rates. Since then, several studies have revealed high SEU cross-sections caused by direct ionization from LEPs in devices with smaller process nodes, 90 nm and below [12, 86–89]. This trend raises concerns that the *on-orbit SEU rate* (OOSR) will be significantly increased [75]. In this chapter, the contribution of LEPs to the OOSR is estimated based on the results presented in Chapter 4. It is shown that even relatively modest shielding can significantly reduce LEP flux for CubeSats operating in LEO.

Beamline testing of LEP effects poses unique challenges due to small-scale effects having a big impact on the outcome of the experiment, such as the beam degrading effects of air, or the encapsulation material used in the *devices under test* (DUTs). Other

studies have used methods such as removing the device encapsulation and irradiating devices in a vacuum to minimize degrading effects [90]. However, these methods are tedious and require specialized facilities. Higher-energy proton sources, which are often used for radiation-effects testing, often rely on degrader blocks to achieve the desired proton energy at the target [91]. When using a high-energy proton source, the degrader must be thicker to reduce the proton energies enough to study direct ionization from LEPs. However, degrader blocks have undesirable effects on the proton beam, such as scattering and beam straggle [12]. *Beam straggle* refers to the widening of the distribution of proton energies in the beamline as it passes through degrader materials. Simulation results showing the extent of beam straggle on a degraded 70-MeV proton beam are shown at the end of this chapter.

5.2. Background

The primary mechanism that produces soft errors in CMOS devices is direct ionization caused by charged particles passing through the sensitive regions of the semiconductor junctions, causing a movement of charge carriers. The minimum movement of charge needed to induce a fault is the *critical charge*. For example, in the case of an SRAM latch with cross-coupled inverters, the critical charge is the minimum charge that must be transferred to one of the two storage nodes that will flip the state of the latch. As feature size becomes smaller, so does the critical charge, thus devices are increasingly vulnerable to radiation effects [92, 93].
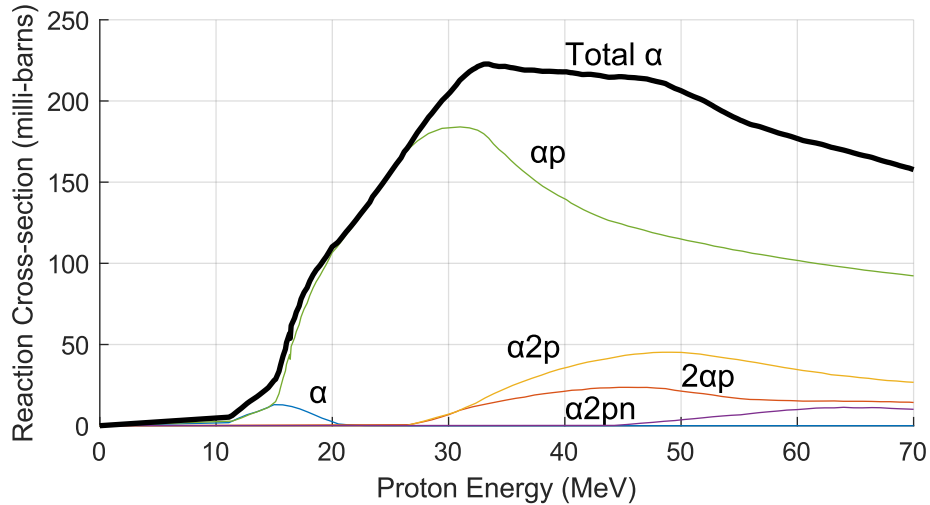
Figure 5.1.: Cross-section of alpha particle production caused by collisions of high-energy protons with silicon atoms (adapted from [9] with permission; see Appendix F).

5.2.1. Alpha Particles Induced Soft Errors

In past technologies, the most significant naturally occurring cause of soft errors has been alpha particles emitted from high-energy particle collisions or isotopic decay in the device materials [38]. The onset of alpha particle production from proton collisions in silicon starts at an incident particle energy of about 10 to 20 MeV, as shown in Fig. 5.1. Previous testing methods with proton beams often focused on using higher proton energies, to determine the worst-case error rates [77].

5.2.2. Direct Ionization from Low-Energy Protons

As the incident particles slow down and come to rest, the rate of their interactions with the surrounding material increases, thus the local energy deposition comes to a maxima called the *Bragg peak* [38]. Fig. 5.2 shows the *linear energy transfer* (LET) of low-energy alpha particles and protons in silicon. The higher mass and charge of
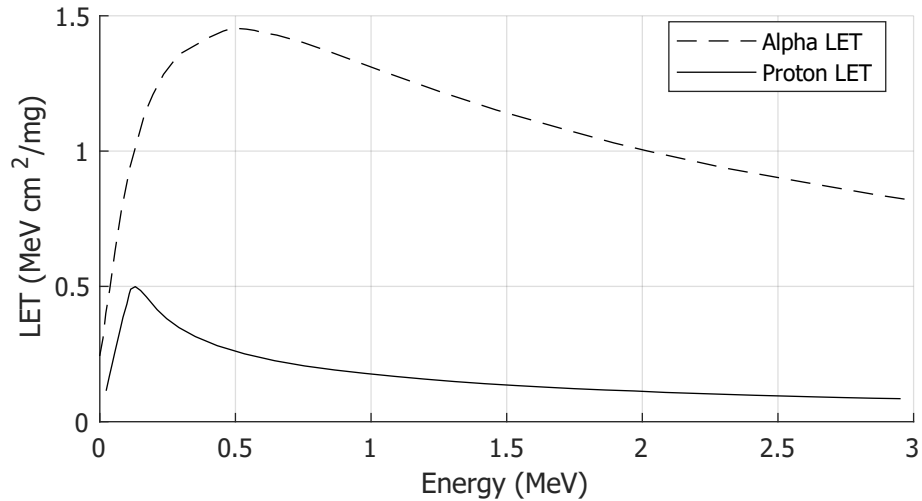
Figure 5.2.: LET of protons and alpha particles in silicon, from simulation data created with SRIM [10].

alpha particles result in much higher LET compared with protons. However, in smaller technology-node devices, the LET of protons around the Bragg peak can be sufficient to cause soft errors, thus introducing a new fault mechanism that requires through consideration and revised testing methods. Some proposed new methods from the literature are discussed below.

5.2.3. Minimally Degraded Beam

Some testing facilities have been specially designed to minimize the perturbing effects, such as beam straggle, caused by degrading materials. The Vanderbilt University School of Engineering's Pelletron accelerator [90] allows testing in a vacuum and uses only thin gold foils in the beamline to minimize scattering. Thus it is an ideal platform for high-fidelity characterization of LEP effects. In [11], Dodds *et al.* present measured proton SEU cross-sections, as shown in Fig. 5.3A. This specialised facility minimizes energy loss, beam straggle, angular scattering, and flux attrition. *Flux attrition* refers

to a reduction in the particle flux reaching the DUT because some of the particles come to a stop in the beamline material. Fig. 5.3B shows that the measured SEU cross-sections correlate with the increased LET of protons in silicon at the Bragg peak.

5.2.4. LEP Testing with High-Energy Protons

High-energy proton sources, such as the TRIUMF Proton-Irradiation Facility [55], are often used to test devices for aerospace applications. In [12] Dodds *et al.* show that the physics of proton energy loss in matter causes the spectrum from high energy proton sources that pass through degrading materials to always converge to a qualitatively similar energy spectrum at low energies (less than 5 MeV). This is demonstrated in their simulated results shown in Fig. 5.4. Thus Dodds *et al.* propose that a degraded 70-MeV beam can be used as a practical test environment to predict the contribution of LEPs on error rates in a space environment. This method can be applied without the need to remove the device encapsulation for testing and without detailed knowledge of the IC design [12].

5.3. Simulated Energy Spectra for TRIUMF BL2C

The experiment presented in Chapter 4 was conducted at beamline 2C (BL2C) at TRIUMF [55]. For this experiment, a 70-MeV proton beam was emitted from the particle accelerator. As the protons travel through the various materials along the beamline, they lose energy. Variations in the paths taken by each individual proton result in a distribution of energies called the *energy spectrum* at the DUT. To determine the energy spectrum the effects of all the various materials along the beamline must be
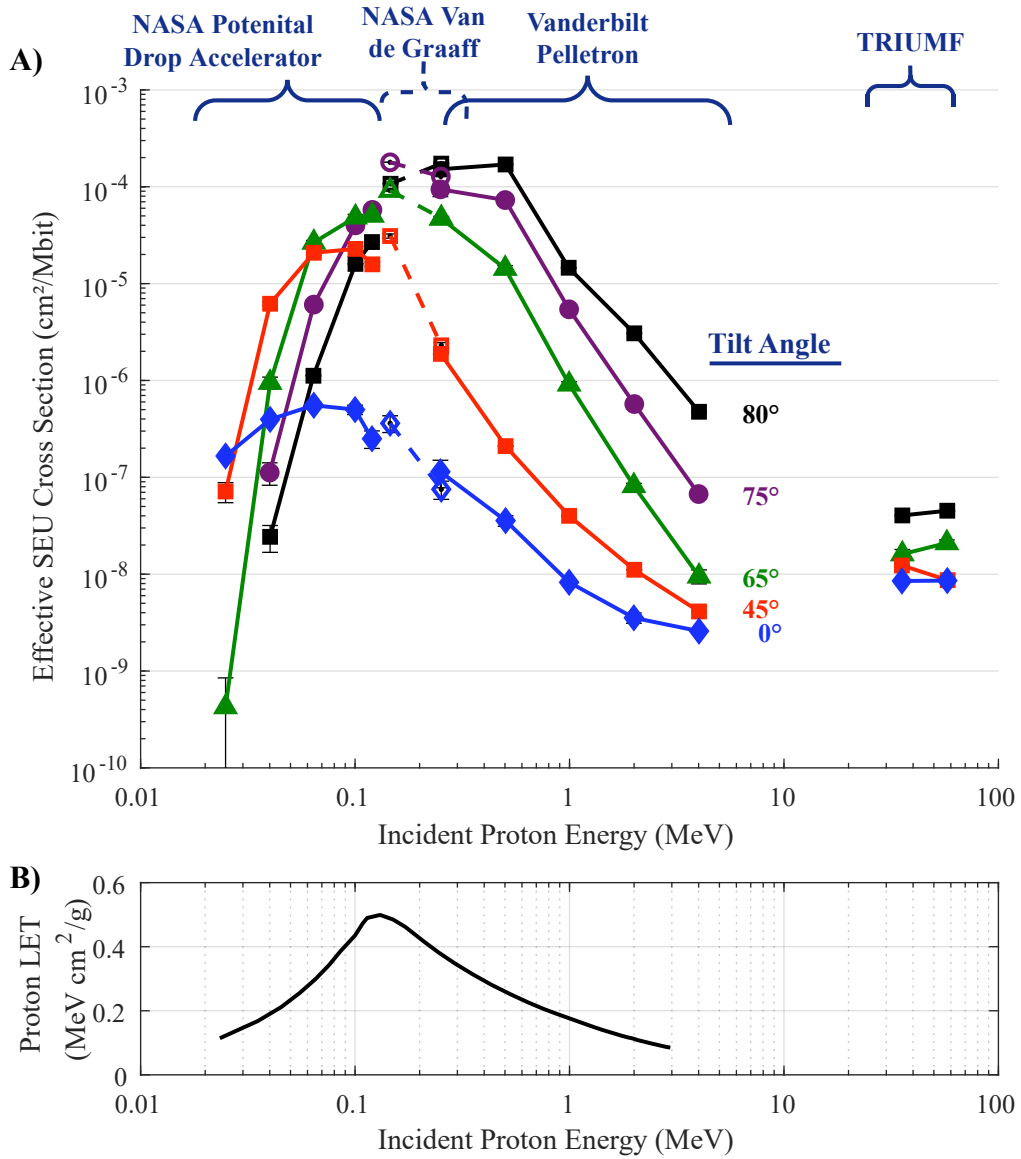
Figure 5.3.: A) Measured proton SEU rates using minimally-degraded LEPs on an SRAM device with its encapsulation material removed (from [11] © 2015 IEEE), and B) LET of protons in silicon, from simulation data created with SRIM [10].
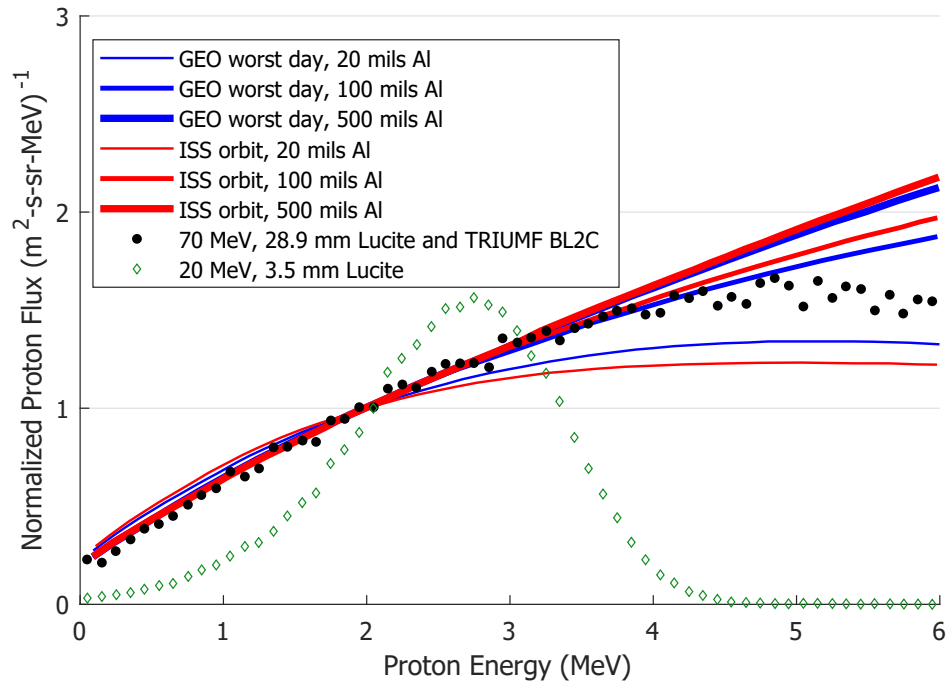
Figure 5.4.: Simulation results showing energy spectra of degraded high-energy proton environments in space and in ground testing, demonstrating that a degraded 70-MeV beam produces a qualitatively similar spectra compared with the LEO and geosynchronous space environments (from [12] © 2014 IEEE).

Figure 5.5.: Energy spectra (simulated in SRIM [10]) of protons reaching the DUT at TRIUMF's BL2C for different degrader thicknesses, with an initial beam energy of 70 MeV. The LET of the protons is indicated by the shaded gradient.

considered. Fig. 5.5 shows the energy spectra of protons reaching the DUT for different degrader thicknesses, simulated with SRIM [10]. A schematic diagram along with a list of the materials and their thicknesses along the simulated beamline is provided in Appendix A. The device encapsulation is modelled as 0.5 mm of epoxy.
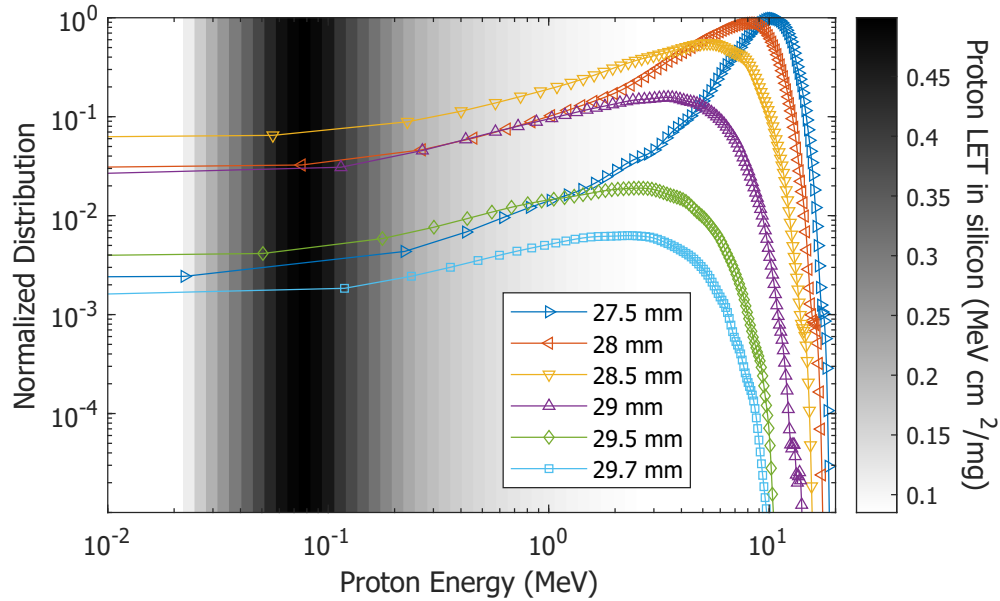
As the degrader thickness is varied, it changes the probability that a proton will reach the sensitive volume of the DUT with its energy within the narrow range of the Bragg peak. Based on the simulated beam spectra, Fig. 5.6A shows the probability that a proton will have an LET greater than $0.2 \, \text{MeV} \, \text{cm}^2/\text{mg}$ when it reaches the DUT. This result suggests that a degrader thickness around 28.5 mm is appropriate to measure SEU rates from LEPs. Fig. 5.6B shows the measured SEU cross-section data, plotted according to the degrader thicknesses used. The result appears slightly shifted compared with the simulation result. Improved modeling of the device encapsulation could
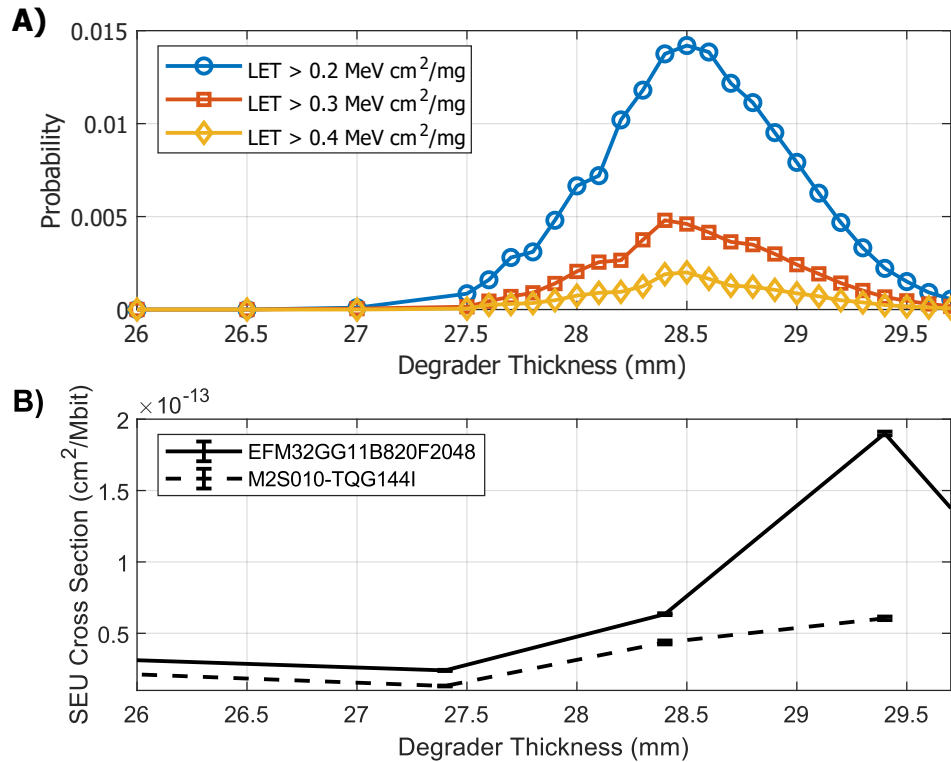
Figure 5.6.: A) probability that a proton will have an LET greater than the given thresholds and B) the measured SEU cross-sections, from Chapter 4, organised by degrader thickness.

possibly improve the accuracy of the simulation.

5.4. Impact of LEPs on Error Rates in LEO

As shown in Fig. 5.7, the measured SEU cross-sections were significantly higher at lower proton energies for two of the DUTs from Chapter 4, indicating greater sensitivity to direct ionization from LEPs:

1. EFM32GG11B820F2048, manufactured with a 90-nm process [78].

2. M2S010-TQG144I, manufactured with a 65-nm process [80].

The most significant contributor of radiation-induced faults on satellites in LEO is

Table 5.1.: Variation in OOSR with four thicknesses of aluminium shielding for the EFM32GG11B820F2048 MCU, calculated using SPENVIS [1].

Aluminium Thickness	Percent Reduction in Average SEU Rate
0 mm	0%
0.370 mm	91.5%
1.853 mm	94.0%
7.410 mm	96.2%

the *South Atlantic Anomaly* (SAA), where the Earth's inner Van-Allen radiation belt comes closest to the Earth's surface [21]. Using shielding materials in this proton-rich environment reduces the LEP flux reaching devices, as shown in Fig. 5.8, because LEPs come to a stop in the shielding material. Radiation belt proton flux is highest during periods of lower solar activity because the slower-moving solar energetic particles are more easily captured in the Van-Allen belts [94]. Thus, Fig. 5.8 considers a *solar minimum* as a worst-case scenario.

Table 5.1 shows the percent reduction in OOSR produced by various thicknesses of aluminium shielding, for the EFM32GG11B820F2048 MCU. This shows that the contribution of LEPs to OOSR can be significantly mitigated by modest shielding, which is generally already provided by the satellite's solar panels and mechanical structure. This result is consistent with the conclusions from the AO-85 CubeSat that was launched in 2015 to a 792-km apogee, 499-km perigee, 65° inclination orbit. The AO-85 CubeSat included a LEP experiment payload to investigate the contribution of LEPs to the OOSR of a commercial SRAM device that was shown to be sensitive to LEPs in ground-based testing [48]. That mission concluded that LEPs did not appear to contribute significantly to the measured OOSR.
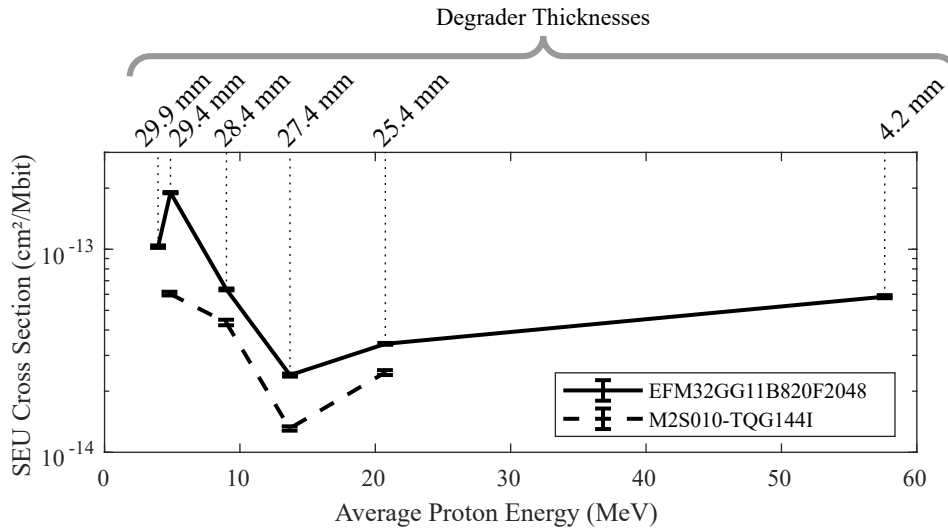
Figure 5.7.: Measured SEU cross-sections of two devices showing sensitivity to direct ionization from LEPs, from the test results presented in Chapter 4. The degrader thicknesses used for each datapoint are shown at the top.
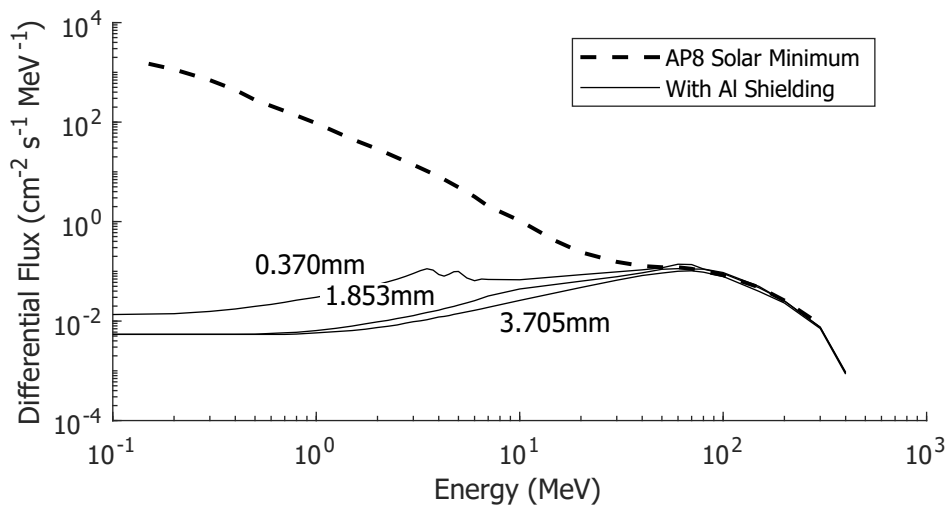

Figure 5.8.: Trapped proton spectra for different aluminium shielding thicknesses at a 400-km altitude during a solar minimum, calculated using SPENVIS [1].

5.5. Conclusions

This chapter focused on investigating the contribution of direct ionization from LEPs on SEU rates in devices with smaller process nodes, particularly in the context of CubeSats operating in LEO. Previous assumptions that LEPs could be ignored are no longer valid for devices with process nodes at 90 nm and below.

Direct ionization from LEPs has been shown to be an important mechanism causing SEUs in new devices [75]. However, for CubeSats operating in LEO, relatively thin shielding can reduce the flux of LEPs that reach the sensitive devices inside by over 90%. This is consistent with the results from Sierawski *et al.* and the LEP payload on their AO-85 CubeSat, which indicated that LEPs did not appear to significantly contribute to the measured OOSR [48].

Testing the effects of LEPs presents challenges due to the significant impact of small-scale effects. Minimizing degrading effects requires specialised facilities. Dodds *et al.* show that the physics of proton energy loss in matter causes degraded high energy proton sources to converge to a qualitatively similar energy spectra at low energies (less than 5 MeV). Thus, a degraded high-energy beamline could be effective as a practical test environment to predict the contribution of LEPs on soft error rates in a space environment [12].

The simulated energy spectra for the TRIUMF BL2C beamline indicate that a degrader thickness of around 28.5 mm is optimal for LEP testing. This thickness results in a higher probability of protons depositing increased energy within the sensitive volume of the DUT. The simulations presented in this study do not account for certain factors, such as variations in ambient air pressure and DUT encapsulation thickness, which could potentially influence the outcomes. Subsequent research could focus on

enhancing the accuracy of these results.

Part II.

Design of a CubeSat Electrical Power Supply

6. Background – CubeSat Electrical Power Supplies

Determination of the electrical power system requirements is a critical element in the design of a spacecraft mission. Nearly all aspects of the mission design impact the power system requirements to some extent. Futhermore, development of the power system is an iterative process which aims to strike a balance between the mission objectives and practical constraints such as size, development time and budget.

The preliminary design process of the power system for a spacecraft generally involves these four high-level steps:

1. **Requirements:** Determine system-level parameters such as average and peak power requirements, mission life, orbital parameters and spacecraft configuration.

2. **Energy source:** Determine the type, size and configuration of the solar array. Most CubeSats use GaAs solar cells [95], and could use deployable or sun tracking arrays to accommodate higher average power requirements .

3. **Energy storage:** Determine the type, size and configuration of the electrical energy storage solution. Most CubeSats use *lithium-ion batteries* (LIBs) [96–98]. Some recent projects have used super-capacitors to accommodate higher peak

power requirements [99–101].

4. **EPS architecture:** Determine the high-level arrangement and interconnections of power system elements, such as converters and distribution elements.

6.1. Power Generation Requirements

The solar array must be sized to satisfy the average power requirements of the various subsystems, throughout the entire mission life. Equation (6.1) can be used to determine how much power the solar array must provide [102]:

$$P_{SA} \geq \frac{\left(\dfrac{P_L T_e}{\eta_e} + \dfrac{P_L T_d}{\eta_d} \right)}{T_d} \qquad (6.1)$$

where, P_{SA} is the power provided from the solar array,

P_L is the total power required for all the various loads in the spacecraft,

T_d and T_e are the daylight and eclipse periods per orbit, respectively,

η_d is the efficiency of the path from the solar arrays, directly to the loads,

η_e is the efficiency of the path from the solar arrays, through the batteries, to the various loads on the spacecraft.
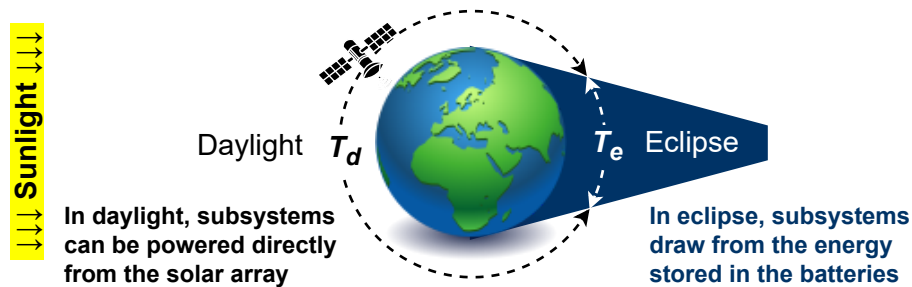

Figure 6.1.: Illustration of the daylight and eclipse periods of a spacecraft orbit
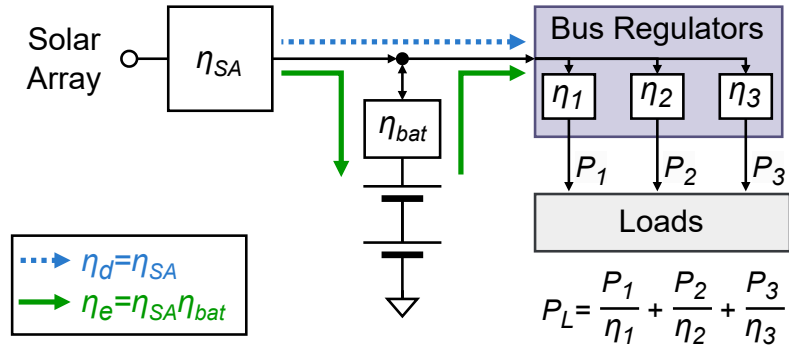
Figure 6.2.: Efficiency elements of the EPS, where η_d is the daylight power efficiency and η_e is the eclipse power efficiency

Bus Regulation Efficiency: The power P_L supplied to the various loads must also account for the efficiencies of the bus regulators (η_1, η_2, η_3) along the power path, as shown in Fig. (6.2). State-of-the art integrated converters can easily achieve efficiencies around 95% or better [41].

Battery Module Efficiency: The battery module efficiency depends on many factors such as temperature, end-of-charge voltage, the charging/discharging current, and overall battery health, which deteriorates throughout the mission. [96–98]. A room temperature battery with a charging/discharging current of 1C has an overall charging/discharging efficiency of around 95 % [103].

Solar Array Efficiency: The solar array efficiency also varies with operating conditions and degrades over time due to ionizing radiation [104, 105]. In LEO, GaAs solar cells degrade at a rate of approximately 2.75 % per year [102]. All of these variables must be considered to guarantee operability throughout the entire mission life.

6.1.1. Solar Power Modeling

The illumination experienced by a solar array in a given orbit varies based on the time of year, the geometry of the spacecraft, and the sun tracking capabilities of the spacecraft. The *Systems Tool Kit* (STK) software environment is a physics-based tool for modeling and simulating complex systems on their operational environment [106].

The EPS design presented in this thesis is intended to be a versatile open-source design that can be applicable to a variety of different CubeSat missions, with only minor modifications. The proposed design is also intended to be included on a technology demonstration payload on the University of Alberta's Ex-Alta 3 CubeSat, currently in development at the time of writing. Thus as a case study for deriving the power handling requirements for the proposed EPS, the Ex-Alta 3 mission will be considered.

6.1.2. Ex-Alta 3 Mission Parameters

The primary payload of the Ex-Alta 3 mission will be a multi-spectral camera and the estimated launch for this mission is in 2025, into a 450 km altitude sun-synchronous orbit [107]. The mission design proposes a 3U CubeSat, possibly including deployed solar panels for additional power capabilities. The most common size for CubeSat missions is 3U [3] and the use of deployable solar panels puts Ex-Alta 3 towards the upper limit of the target audience for the EPS design proposed in this thesis. Thus, considering the power handling requirements of this mission provides a benchmark set of requirements that is likely to be applicable to a large portion of LEO CubeSat missions.

6.1.3. Solar Panel Configuration

Four different solar array designs are considered, as shown in Fig. 6.3. Simulation results from STK (provided by Max Schatz of the AlbertaSat Power System Team) were used to determine the energy generation and the peak power per orbit for each configuration, as shown in Fig. 6.4. The simulations considered a 450-km sun-synchronous orbit, with an orbit period of 90 minutes and the local-time of the ascending node (LTAN) at noon such that the orbit plane intersects the sun, as shown in Fig. 6.5.

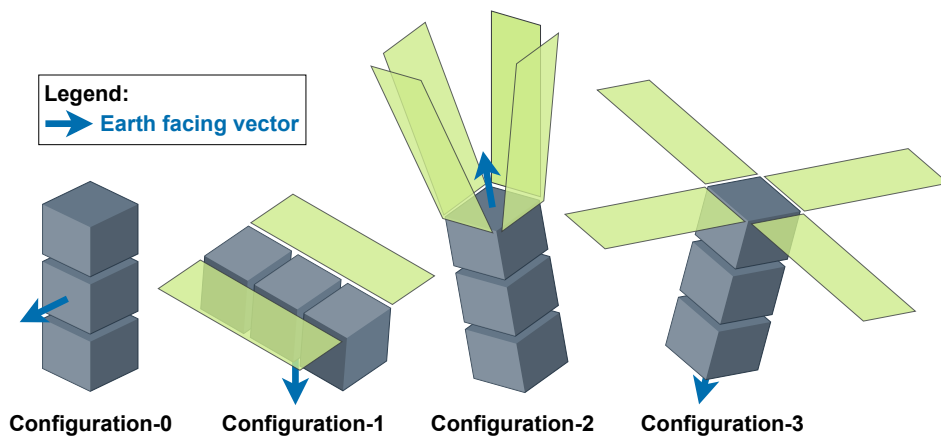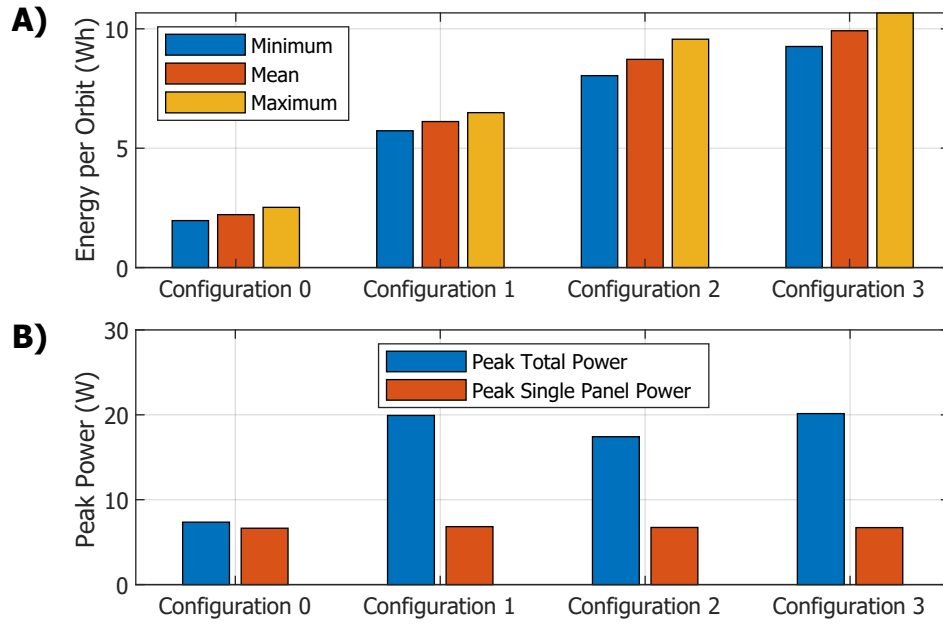**Figure 6.3.:** Different solar array configurations for a 3U CubeSat

Figure 6.4.: A) Energy generation per orbit and B) peak power generation for the different solar array configurations in Fig. 6.3, based on STK simulation data provided by Max Schatz of the AlbertaSat Power System Team
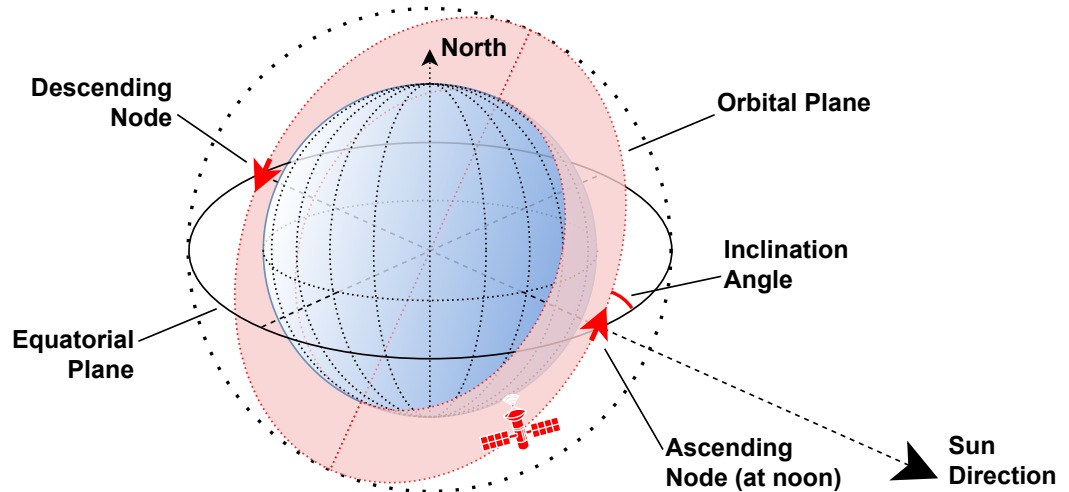

Figure 6.5.: Illustration of the noon-LTAN orbit used for evaluating the different solar array configurations.

The results in Fig. 6.4 show that the highest peak total power generation is approximately 20 W. Adding a 20 % contingency factor shows that a power rating of 24 W for the MPPT converters on the proposed open-source EPS will be applicable to most 3U (or smaller) CubeSat missions.

6.2. Power Budget

Another critical step in satellite power system design is to determine the power consumption requirements of the various subsystems throughout the mission. This iterative process aims to optimize mission success within the constraints of the CubeSat form-factor and the mission parameters, such as size, mass, and cost. This section outlines the key components involved in determining the *power budget* for a CubeSat, focusing on the Ex-Alta 3 mission as an illustrative case study.

Table 6.1 shows the estimated power consumption requirements for the various subsystems on the proposed Ex-Alta 3 CubeSat. A comprehensive power budget analysis must also encompass all other operating modes of the satellite, such as early life commissioning, power safe modes, etc. For brevity, the hypothetical power budget presented here only considers the *science mode* – an operating mode with all payloads and communications are functioning at their intended duty-cycles.

The hypothetical power budget in Table 6.1 shows that the power consumption requirements for the Ex-Alta 3 mission are 34.2 W for total peak power and 20.1 W for average power. These results will provide some context to the power ratings of the bus regulators for the open-source EPS proposed in this thesis.

Table 6.1.: Hypothetical power budget for the proposed Ex-Alta 3 CubeSat mission, based on parameters provided by the AlbertaSat Power System Team

Subsystem	Peak Power	Average Power	Duty Cycle	Energy per Orbit
Command and data handling	2.0	2.0	100	3.00
On-board processing	6.0	6.0	2	0.18
Communications (UHF)	7.9	0.3	100	0.45
Communications (S-Band)	5.0	0.9	10	0.14
Payload-1 (Imager)	8.0	8.0	18	2.16
Payload-2 (Magnetometer)	1.0	1.0	100	1.50
Attitude determination and control	3.5	1.5	18	0.40
GPS module	0.3	0.3	100	0.45
EPS control circuitry	0.5	0.1	100	0.15
Maximum Total System Power	**34.2**	**20.1**	**100**	**8.43**
Units:	(W)	(W)	(%)	(Wh)

7. CubeSat Electrical Power Supply

7.1. Introduction

CubeSat, a class of miniaturized satellite, emerged in the early 2000s as a cost-effective platform for space research [15]. By standardizing a compact form factor, CubeSats provide an affordable and accessible means of conducting scientific research, technology demonstrations and educational activities in a space environment. With an extensive range of potential payloads, CubeSats have proven to be highly versatile. Their relatively low cost has opened up space exploration to a wider range of participants. Despite their small size and reduced robustness, CubeSats can perform substantial and valuable tasks in space at relatively low cost, including roles in lunar expeditions [108].

The development of an efficient, reliable and adaptable *electrical power supply* (EPS) is critical to the successful operation of any space mission. Power system failures are suspected to be the single largest cause of spacecraft failures [53]. Given the stringent size and weight constraints, designing a reliable and efficient power system for a Cube-Sat presents a significant challenge, especially for an inexperienced design team. The effectiveness of the EPS directly impacts overall mission success. This work introduces an innovative, open-source design of an EPS for CubeSats that optimizes reliability,

efficiency and flexibility. The design uses a parallel, multi-channel, *maximum power point tracking* (MPPT) architecture and includes several novel advanced features:

- A conservative solar panel power point control feature that automatically activates when MPPT software is inactive, such as when recovering from a fully-discharged battery state.

- A charge/discharge inhibit mechanism that allows battery discharge and heating when the batteries are too cold for safe charging. Furthermore, this feature could allow for reducing the heater power during eclipse until just before returning to sunlight, thus avoiding unnecessary heating of the batteries while solar power is unavailable.

- A transistor-based power inhibit circuit (for switching off all power before the satellite is deployed) that reduces power wastage by preventing conduction losses, which would typically occur in switch wiring. It also mitigates the magnetic moment created by current-carrying wires that could disrupt the CubeSat's attitude control system and any other magnetometer instruments.

- Intelligent sensors which rapidly decouple power in the event of over current and monitor key parameters, such as current, voltage and temperature, only alert the microcontroller during system-critical conditions like over-current events. This autonomy reduces power consumption by eliminating the need for polling.

- A jumper matrix to supply regulated (e.g.: 5V, 3.3V, 1.2V) or unregulated battery bus voltage to each of the 18 output channels, and a software feature that synchronizes the fault response of codependent channels.

- Adaptive over-current fault detection that compensates for the gradual increase of leakage currents caused by accumulated *total-ionizing dose* (TID) effects over
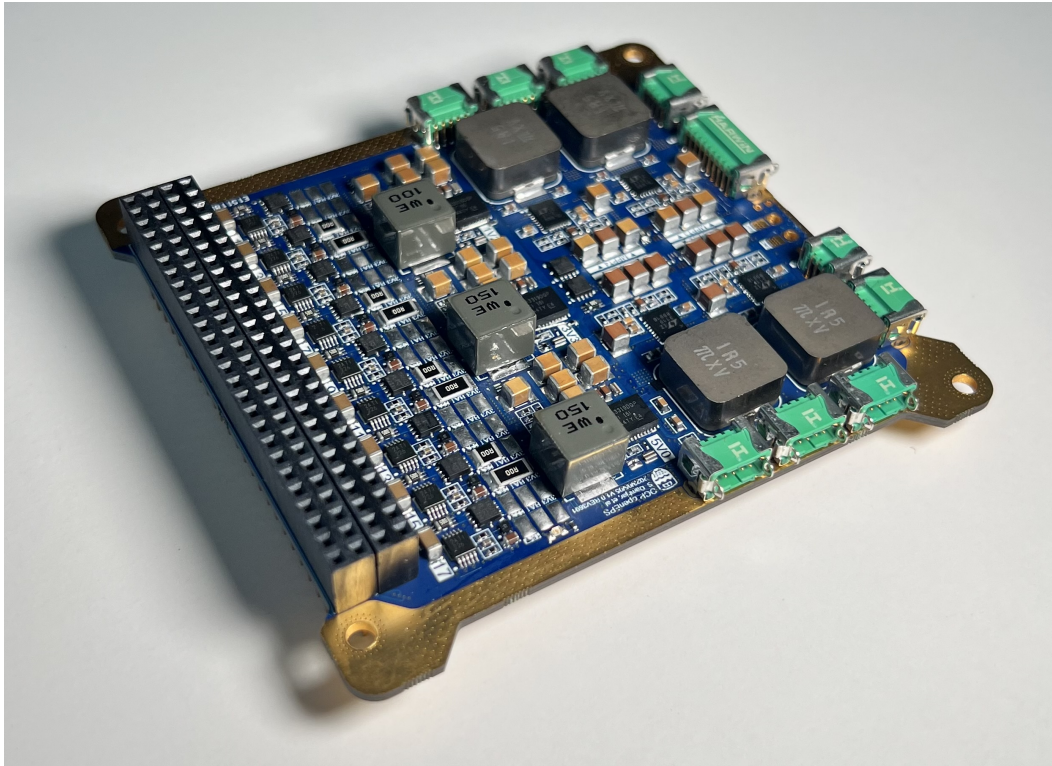
Figure 7.1.: Photograph showing a fully implemented prototype of the proposed open-source EPS design.

the course of the mission.

By leveraging open-source hardware and software, this project is intended to promote collaborative and cost-effective development. A prototype EPS has undergone extensive testing, demonstrating the expected functionality, efficiency, reliability, fault tolerance and thermal management. This chapter presents the proposed EPS design, prototype implementation (shown in Fig. 7.1), and functional test results.

7.2. Motivation

The initial motivation for this work originated from the student-led development of the Ex-Alta 1 CubeSat at the University of Alberta [4]. Like in many other university

CubeSat projects, a *commercial-off-the-shelf* (COTS) power system was purchased. Although successful, the relatively high cost, long procurement time and a lack of access to the proprietary design details of the purchased EPS were significant challenges for the Ex-Alta 1 team. In-house development of a power system would have ensured full control of all the design details to ensure optimal support for the mission. However, developing a reliable power system from scratch is a substantial task, especially for a relatively inexperienced team. The proposed open-source project aims to provide a versatile EPS design that is freely available and that will over time benefit from collaborative development from multiple groups.

7.3. Power System Architecture

The architecture of a satellite power system typically includes: an energy source (such as solar panels), energy storage (such as batteries), and power regulation and distribution. This section presents the design of a partially regulated architecture using:

- parallel multi-channel MPPT solar-array converters for maximizing power production from the solar arrays,

- charge current supplied directly to the battery bus from the solar array converters and

- a versatile hybrid of centralized and distributed power bus regulation.

A recent study comparing MPPT architectures for CubeSats shows that a parallel multi-channel MPPT architecture provides the best overall performance with respect to efficiency, reliability and battery health [109]. The DET architecture proposed in [110] reduces the number of single points of failure with a modest reduction in solar

power utilization, which is mostly compensated for by avoiding converter efficiency losses. However, recent advances have enabled high power density integrated *switching-mode power supply* regulators to achieve very high efficiencies of 95% and above [41], which tips the scales in favor of MPPT. Furthermore, small footprints could allow for multiple redundant converters, improving fault tolerance.

Distributed bus regulation reduces conduction losses [110] and improves thermal distribution [111] but also requires point-of-load regulation, potentially resulting in increased system complexity and mass. A versatile hybrid solution is proposed using a jumper matrix to select regulated or unregulated power independently for each output channel, optimizing both efficiency and reusability, as shown in Fig. 7.2.
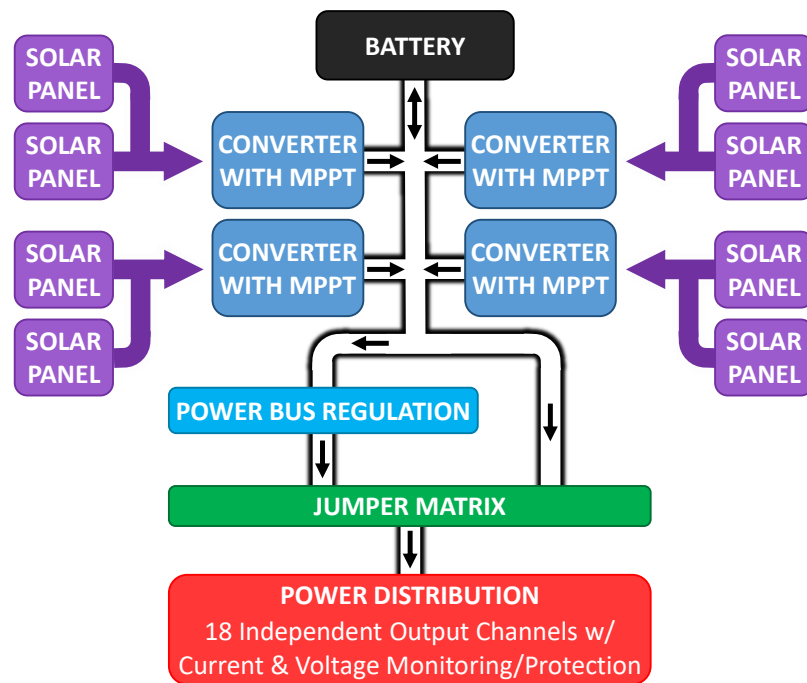

Figure 7.2.: Architecture of the proposed EPS.

Table 7.1.: Comparison of specifications of this work with similar COTS EPS products

	EPS-1 (this work)	EPS-2 [113]	EPS-3 [112]	EPS-4 [114]
Product Name	openEPS	NanoPower P31u	NanoAvionics EPS	iEPS Type A
Solar panel input voltage	3 to 18 V	up to 8.5 V	2.6 to 18 V	3.5 to 15 V
MPPT solar input channels	4	3	4	3
Solar input per channel	up to 3 A	up to 2 A	up to 25 W	up to 2 A
Solar converter efficiency	Up to 97 %	Up to 96 %	Up to 96 %	unpublished
Regulated bus voltages	$1.2, 3.3, 5.0$ V	$3.3, 5.0$ V	$3.3, 5.0, 3 - 12$ V**	$3.3, 5.0$ V
No. of switched outputs	18	10	10****	*
Operating Temperature*****	-40 to 105 °C	-40 to 85 °C	-40 to 85 °C	-40 to 85 °C
Mass	90 g	100 g	190 g***	184 g***
Height	9.8 mm	15.3 mm	19.0 mm***	11.3 mm

* Outputs are always ON and loads are responsible for managing their own connection to the bus.

** An optional resistor programmable buck-boost converter can supply 3 to 12 V.

*** Includes batteries.

**** Expandable to 18 outputs with an optional expansion board.

***** The referenced work also uses LIBs which typically have an operating temperature range of -20 to 60 °C [115]

7.4. Design Overview

One of the defining characteristics of the CubeSat concept is to establish a standard form factor so that reusable subsystems can be developed and shared within a budget-constrained satellite developer community [15]. Many CubeSat subsystems are now available commercially as COTS products, applicable to many CubeSat missions. The proposed EPS design has the same goal, but with the added benefits of collaborative open-source development. Table 7.1 compares the technical specifications of this work with state-of-the-art commercial CubeSat EPSs. The next most capable COTS EPS to this work in its specifications is the NanoAvionics EPS (EPS-3 [**112**]). The proposed EPS is more versatile in terms of output channel configuration (because of the jumper matrix feature) and includes a generous 18 software-controlled and current-protected output channels on a single board. A detailed diagram showing the various hardware components and their interconnections for the proposed EPS is shown in Fig. 7.3 and the design of the novel features is presented below.
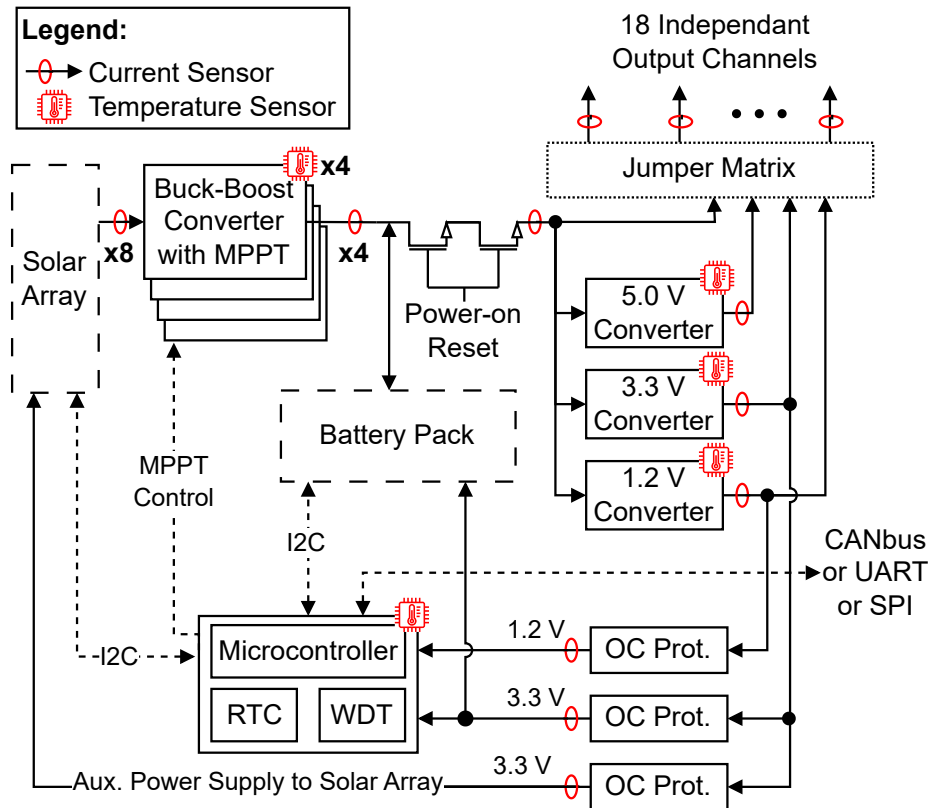
Figure 7.3.: Detailed block diagram showing the elements and interconnections of the proposed EPS design.

7.4.1. Solar Power Regulation

The Linear Technologies LTC3119 buck-boost converter [116] is chosen as the solar power DC-DC converter. Multi-junction GaAs solar cells are commonly used because of their high efficiency and radiation-tolerance. These solar cells typically produce an open-circuit voltage of 2.7 V per cell at room temperature [13] and CubeSats typically have 2 to 6 cells per facet, resulting in an overall voltage range of 5.4 to 16.2 V. The operating range of the LTC3119 converter is 2.5 to 18 V, making it a suitable match. Selection of the LTC3119 converter is also supported by the following factors:

- High efficiency, small footprint and low part count

- Integrated MPPT feature, which regulates the average inductor current and thus the input voltage from the solar array

- Proven space heritage from past missions [117].

To enhance the MPPT capabilities, a novel approach is employed, adding a control circuit with a *digital-to-analog converter* (DAC) that is controlled by a *microcontroller* (MCU) via a *Serial Peripheral Interface* (SPI), as shown in Fig. 7.4. When the battery voltage is sufficient for the DC bus regulators to be active, the DAC circuit allows for software control of the MPPT, resulting in dynamically maximized tracking efficiency. When the battery voltage is insufficient, the DAC control circuit is automatically isolated and the resistor divider (R_1 and R_2 in Fig. 7.4) takes over, providing a conservative fixed power point setting (based on the maximum expected solar cell temperature) to ensure charging can occur while the microcontroller is unpowered.

Selecting the default solar array voltage (V_{R_1,R_2}) programmed by the R_1,R_2 resistor divider is guided by two main criteria:

1. Ensure that solar power extraction is always possible, including at high solar cell
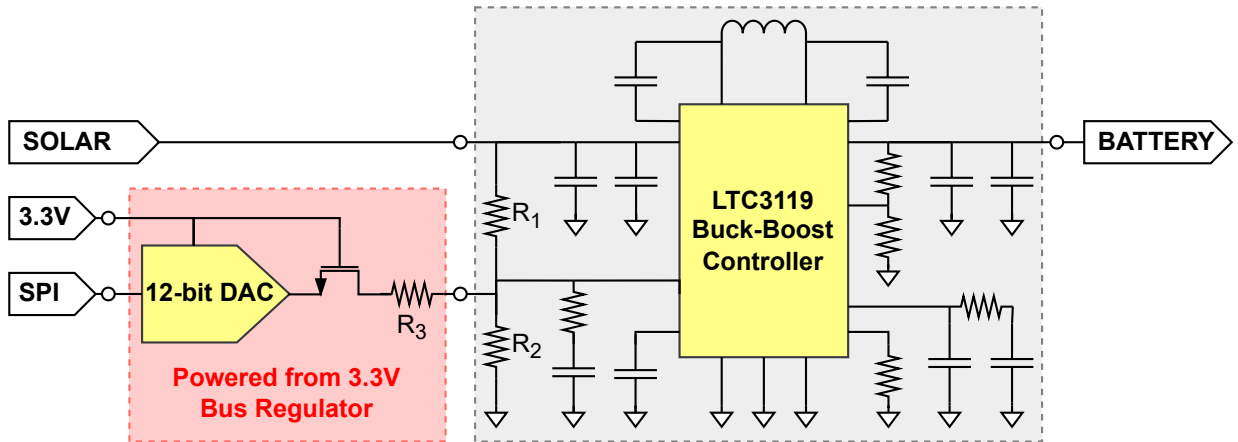
Figure 7.4.: Schematic of solar panel regulator with MPPT control.

temperature, which produces lower input voltage.

2. Maximized power extraction. Maximum power extraction is achieved at the maximum power point (V_{MP}) of the power-voltage curve of the solar array, as shown in Fig. 7.5.

The characteristics of the solar cells vary with environmental conditions such as temperature, as shown in Fig. 7.5. If V_{R_1,R_2} is greater than the open circuit voltage of the solar array, then the solar array voltage will never reach the threshold required by the MPPT control circuit. This will result in zero power generation and is an unrecoverable failure mode. Thus, V_{R_1,R_2} is conservatively chosen to be the maximum power point at the maximum expected temperature, which is about 75 to 94 °C for small satellites in low Earth orbit (LEO) [118].

Maximum Battery Voltage and Current To avoid damage to the batteries, it is important to limit the maximum voltage applied while charging [96]. In case the power demands of the CubeSat are low, the LTC3119 converter will become output-regulated, limiting the voltage applied to the batteries to a safe resistor-programmed
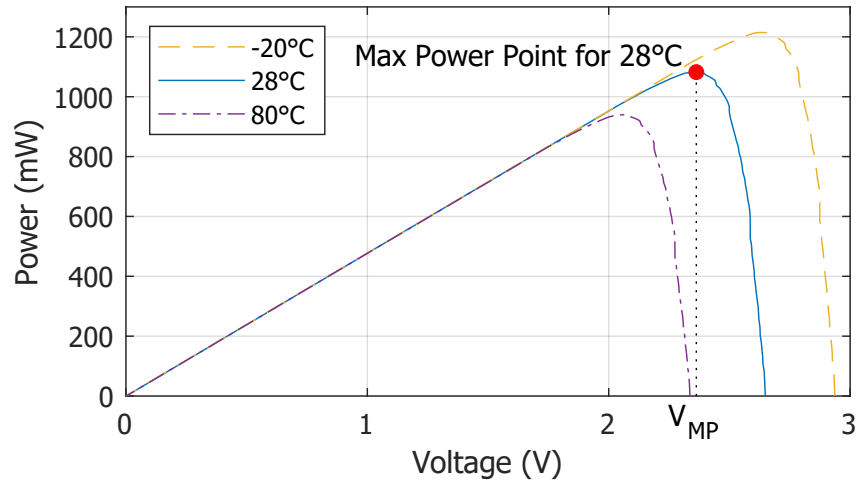
Figure 7.5.: PV curves of a GaAs Solar Cell at different temperatures, with the maximum power point indicated for 28°C [13]

voltage. Battery discharge current is monitored by an overcurrent protection circuit. Output channels can be assigned a priority level and automatically switched off when battery discharge current is too high or when battery voltage is too low. In future work, battery charge current limiting could be achieved by implementing a control scheme that automatically perturbs the operating point of the solar cells away from the maximum power point.

7.4.2. Battery Charge or Discharge Inhibit

Rechargeable *lithium-ion batteries* (LIBs) have emerged as the preferred energy storage solution for CubeSat applications because of their high energy density [100]. A limitation of popular LIB cells reported in the literature is that operating at temperatures below $0\,°C$ sharply diminishes the performance and accelerates aging, reducing the useful life of the cells [119]. This is particularly significant during charging because of irreversible lithium plating of the cell anode that could cause short circuits or even
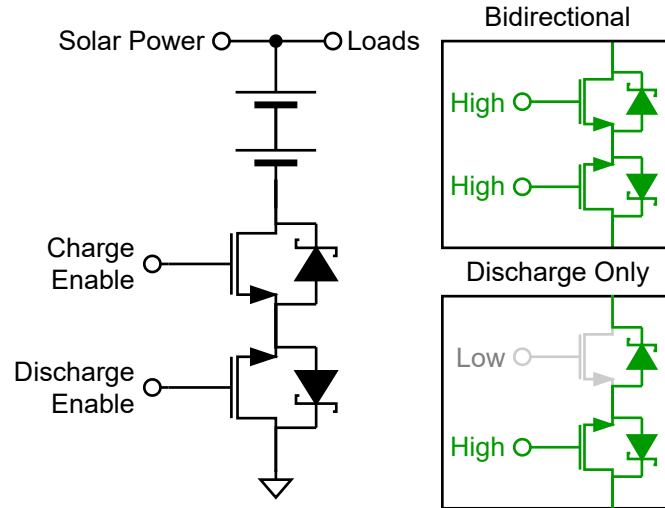
Figure 7.6.: Schematic showing the novel discharge-only mode. When the Charge Enable signal is low, the charge current is blocked, while the discharge current passes through the bypass diode.

battery thermal runaway and explosion [119]. Therefore, the charging current should be blocked when the cell temperature is below $0\,°C$ to protect the cells from damage. Discharge performance, on the other hand, is primarily limited by low ionic conduction, which sharply diminishes below $-20\,°C$ [119]. Therefore, between $-20\,°C$ and $0\,°C$, it is possible to discharge the batteries to operate satellite loads and power the battery heaters to heat the battery cells up to an acceptable charging temperature. In this work, a solution is proposed to selectively inhibit charging and/or discharging using two independently controlled transistors, as shown in Fig. 7.6. When charging is disabled, the discharge current will flow through the bypass diode of the charge enable transistor.

7.4.3. Power Inhibit Switch

CubeSats are typically deployed from spring-loaded rectangular pods, such as the NanoRacks CubeSat Deployer system [120], from the International Space Station. To ensure astronaut safety and to prevent interference with the deployer, CubeSats must be powered off while stowed in the pod. Thus, three independent inhibits are required to disconnect the battery and solar power while the CubeSat is stowed. The advantages of using transistor inhibits are:

- Avoid conduction loses in the alternative high-current switch wiring that would otherwise be required.

- Lower mass and eased mechanical design because of smaller switches and thinner wires.

- Avoid magnetic moments from switched wiring that could interfere with sensors or attitude control.

- Furthermore, this solution provides a power-on reset mechanism that can be triggered to power-cycle the satellite in case of an anomaly.

In this work, a transistor inhibit solution is proposed, as shown in Fig. 7.7. Mechanical switches on the CubeSat external toggle the transistor gates to inhibit the power while the CubeSat is stowed. Several *remove-before-flight* (RBF) jumpers are included to override the inhibits during ground testing. The battery charge or discharge inhibit feature, discussed in the previous section, is also incorporated.
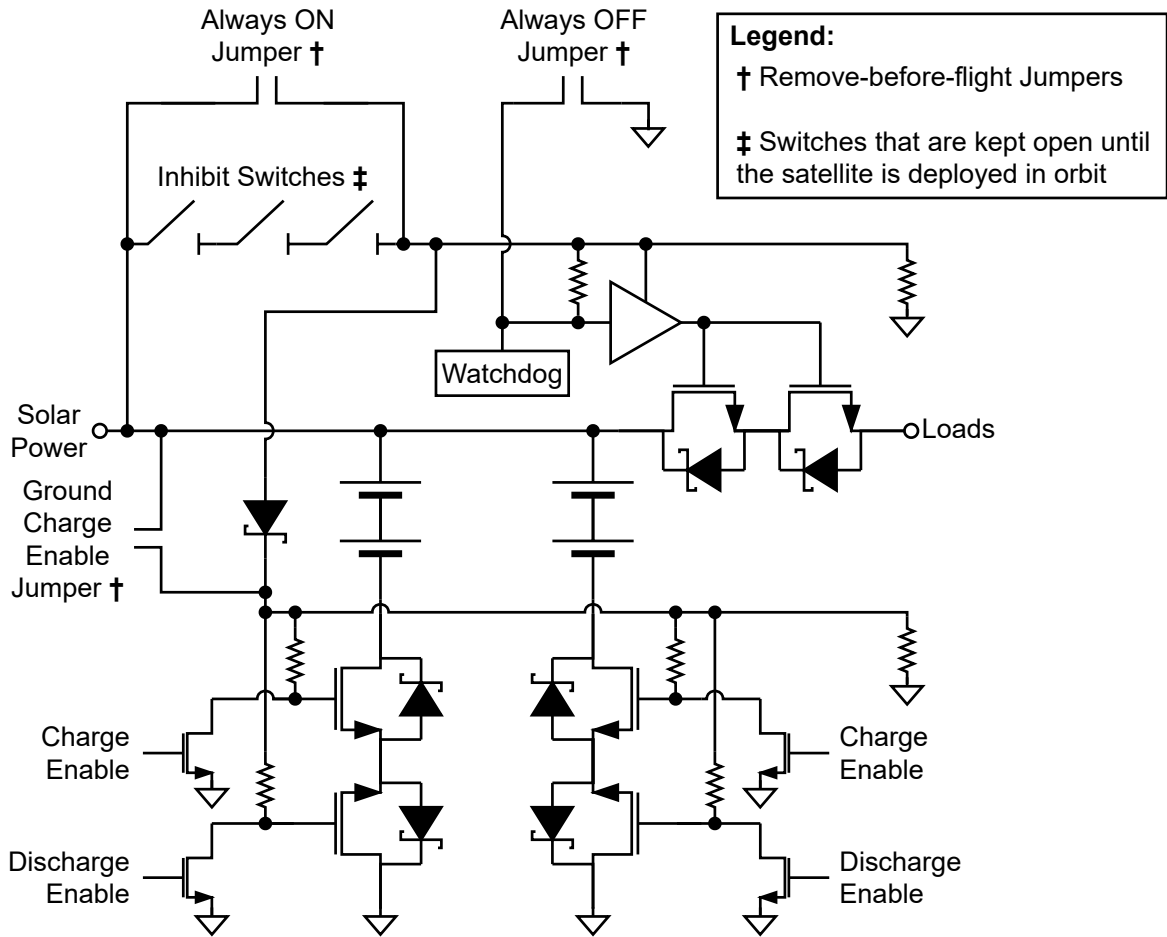
Figure 7.7.: The novel transistor-based power system inhibit switch circuit, supporting separate control over charge and discharge.
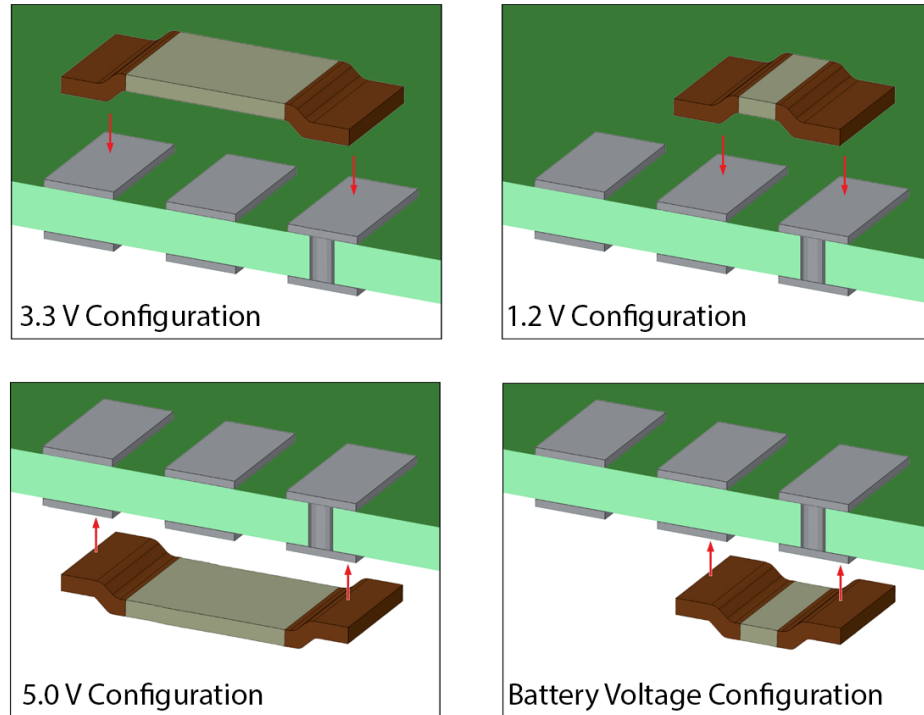
Figure 7.8.: A jumper configuration design that provides four different bus connection options, to maximize flexibility and hence reusability.

7.4.4. Output Configuration Jumpers

Because there is no industry standard on pin assignment, ensuring compatibility of subsystems is a challenge for CubeSat developers. To maximize reusability, the proposed design includes a jumper matrix, shown in Fig 7.8, that allows each of the 18 output channels to be connected to the either the unregulated battery voltage, or to one of three regulated buses. For unused channels, the corresponding output channel components or just the current sense resistor can be left unpopulated to isolate the stack pin from the EPS.

7.4.5. Interfacing and Control

There are two main objectives when designing an EPS subsystem: 1) reliable and capable hardware (discussed above); and 2) an interfacing and control scheme that ensures high availability for the user and that preserves functionality despite anomalies such as partial subsystem failures. This section discusses some of the key features of the interfacing and control scheme developed for the proposed design.

CANbus Interface   The *controller area network bus* (CANbus) is a standard multi-master serial bus that connects multiple nodes together using differential wired-AND signals [121]. A major advantage of this interface for CubeSat applications is that it allows direct bi-directional communication between any two subsystems, without requiring a host computer in-between. Thus in the event of a failure of the on-board computer, the CubeSat would still be operational with the EPS and radio subsystems alone. The EPS also supports control via synchronous or asynchronous serial interfaces.

Power Saving Sensors   To maximize the overall efficiency of the EPS, the power consumption of the control circuits should be minimized. In this work a network of low-power integrated sensors is used, with programmable threshold value registers. During initial startup, the microcontroller initializes all of the sensors with threshold values and then enters a low-power sleep mode, waiting for the next interrupt or timed event. If a threshold value (such as maximum current or voltage) is violated, the sensor immediately turns off the affected channel and sends an interrupt signal to wake up the microcontroller. The microcontroller then logs the event and takes appropriate action, such as attempting to restart the affected channel. Wake-up can also be triggered by the *real-time clock* (RTC) for scheduled events (such as turning a
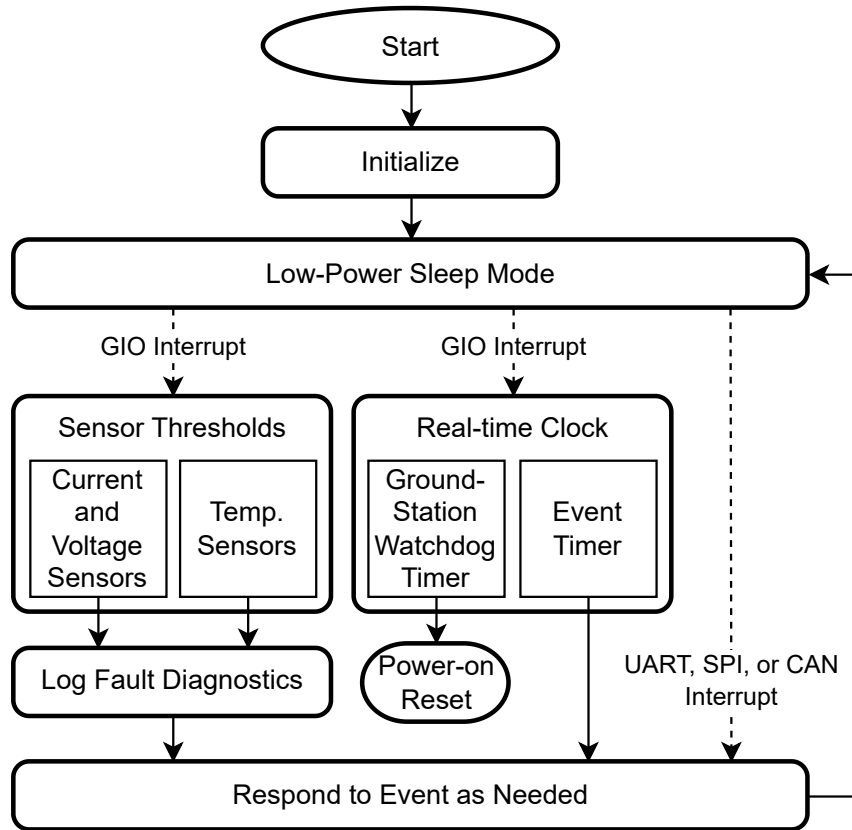
Figure 7.9.: Flow chart showing the different events that can trigger a wake-up.

load on at a specified time) or when commands are received from other subsystems over the serial or CANbus interfaces. Fig. 7.9 summarizes the wake-up interrupts scheme. Additionally, the sensors themselves each have low-power shutdown modes for when not in use, such as when an output channel is switched off.

Output and Bus Monitoring Voltage, current, and temperature sensing and threshold monitoring are achieved using bus monitoring circuits, and temperature sensors. The sensor locations are shown in Fig. 7.3. The temperature sensors are positioned to have thermal contact with the microcontroller and with each of the seven inductors. Each output channel can be configured with a different over-current threshold value.

Battery and Solar Array Interfaces The interfaces of the battery module and solar array include several features. An *inter-integrated circuit* (I2C) interface connected to bus current and voltage monitoring circuits and temperature sensors on the battery module. This I2C interface allows control of the battery charge/discharge inhibit circuit and battery heaters. Additional I2C interfaces to each of the eight solar array connectors (two for each MPPT converter) allow temperature and light sensors to be implemented on each solar panel facet, and also provide an interface to actuate deployment of antennas, instruments, folding solar panels or any other deployable elements.

Software Features The real-time software architecture was developed by Junqi Zhu and is described in detail in his MSc thesis [122]. Some key features that improve operability are:

1. Back-up of persistent configuration data, such as sensor threshold values, to protect the system from data corruption.

2. A software-controlled maximum power point tracking algorithm.

3. Ganged-output channel operation to synchronize control of power distribution to subsystems with multiple bus connections.

7.4.6. Fault-Tolerant Features

Reliability is a major concern for spacecraft developers because of the high cost, harsh operating environment and the lack of physical access after launch. For large non-military spacecraft, long operational lifetimes are required to justify the high development cost. CubeSat missions usually reduce the reliability and operational lifetime

requirements in favor of much lower cost and faster development. Nonetheless, reliability is still a significant concern, and a balance is needed to optimize the trade-off between cost and reliability.

Supervisor Circuit The supervisor watchdog circuit is used to enhance fault tolerance and operational reliability, safeguarding against potential software errors, unexpected behaviors and environmental challenges. The key features are:

- During correct firmware operation, the MCU sends a periodic pulse to the watchdog circuit. If the MCU fails to send a pulse signal to the watchdog timer within the timeout period, the watchdog circuit will automatically trigger a power cycle of the entire satellite, allowing the system to recover from many potential software errors or faulty behaviors caused by radiation. The reset duration is the elapsed time from the moment a reset is triggered until the moment the power is restored to the system. Both the timeout period and reset duration of the watchdog circuit are programmable up to a maximum value of 10 seconds. A reset duration of 5 seconds was used during testing and was consistently sufficient to allow charge stored in capacitors throughout the subsystems to dissipate, to ensure a complete power cycle operation.

- The battery voltage level is continuously monitored by the watchdog circuit and will shut down the satellite subsystems if the battery voltage falls below a resistor-programmable threshold. This limits the degree of discharge, thus extending the operational lifetime of the batteries [96].

- The independent reset input of the watchdog circuit allows other fault detection mechanisms or supervisor circuits in the system, such as over-current sensors, to trigger a power-cycle operation.
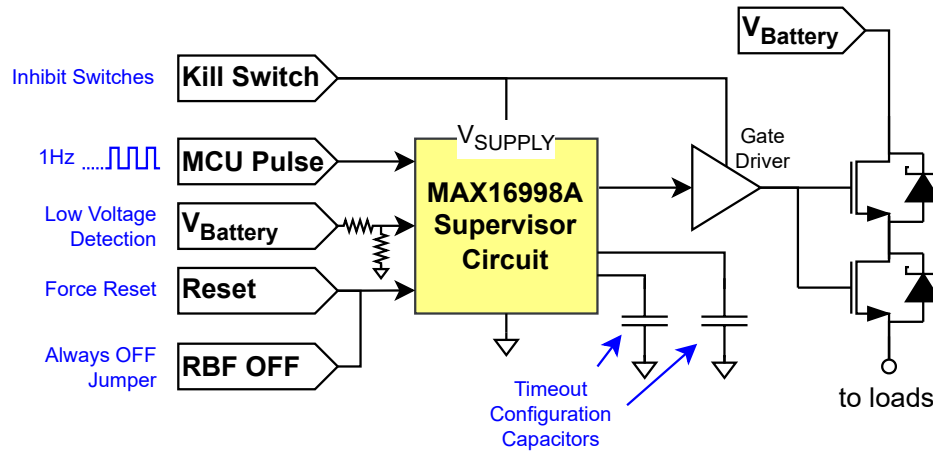
Figure 7.10.: Schematic of the main supervisor circuit, built around the MAX16998A.

- The EPS firmware implements multiple software watchdog timers with configurable timeouts, reset mechanisms, and effects. The effects can be to power cycle a supply channel, a group of supply channels, or (after a longer programmable time-out) power-cycle the entire satellite. In addition to each EPS firmware process being checked by a software watchdog timer, satellite subsystems including the main computer and ground communication subsystem can send messages to reset their respective software watchdog timer in the EPS. One of the software watchdog timers could be reset by a ground station command, ensuring that the satellite would be power cycled if anything were preventing communication with the ground station.

Fault-Tolerant MCU   The proposed EPS uses an MCU from the Hercules TMS570 series [123], which is marketed for safety-critical automotive applications. TMS570 MCUs have been successfully used as a mission-critical component for several spacecraft missions, including NASA's Ingenuity Mars Helicopter [124]. TMS570 MCUs are an appealing option for CubeSats because they include several fault-tolerant fea-

tures, at a much lower cost compared with radiation-hardened devices. Some of those features are listed below:

- Two ARM Cortex-R4 central processor units (CPUs) operate in a redundant lock step architecture. The results of each CPU cycle are compared by the hardware and a disagreement will trigger a power-on reset. The CPUs are physically rotated relative to each other to avoid common mode faults related to silicon layout.

- SRAM and flash memory modules are protected by a CPU-coupled (72,64)-Hamming error correction code (ECC) that will correct single-bit errors or trigger a reset for double-bit errors. This is particularly useful for space applications where high levels of ionizing radiation increase the probability of data corruption.

Adaptive SEL Detection   Another important consideration in intense radiation environments is *single-event latchups* (SELs). An SEL is a potentially destructive fault condition that occurs in *complementary metal-oxide semiconductor* (CMOS) devices when ionizing radiation causes a self-sustaining parasitic silicon-controlled rectifier circuit to form, resulting in a short circuit path and possibly catastrophic damage unless the supply current is quickly switched off [125].

An effective and straightforward method for mitigating permanent electronic component damage from SEL faults is continuous current monitoring with an over-current detection threshold [126]. An SEL fault is presumed when the measured current draw of a channel is in excess of a configured threshold value. The affected channel is switched off for several seconds to allow the SEL to dissipate. However, selecting too low a threshold value could result in normal behavior being mistaken for SEL faults, while too high a value could result in a fault going undetected, resulting in possible

damage. Accurate characterization of SEL fault behavior to determine an appropriate threshold value for a particular device requires modeling with knowledge of the physical layout dimensions [127], or particle accelerator testing which is often too costly for CubeSat projects. To overcome this issue, an adaptive SEL over-current detection threshold algorithm is proposed with the following features:

- The over-current detection threshold can automatically be adjusted upward as the satellite the satellite is exposed to radiation and the current consumption increases. Without this feature, the satellite could get trapped in an over-current protection power-cycling loop where the satellite operator is unable to send a command to adjust the current limit. The static current consumption of CMOS devices increases with accumulated total radiation dose effects that cause a gradual breakdown of gate oxides, resulting in increased leakage currents [37]. Frequent over-current trips on a particular power channel (parameter settable) causes the over-current threshold for that channel to be increased to allow for greater current consumption due to these total radiation dose effects.

- The satellite operator can also adjust the configured threshold values, based on an assessment of diagnostic data. For example, if error reporting indicates that erroneous SEL detection is repeatedly interfering with a normal function, the operator could choose to adjust the threshold accordingly. Each output channel can be configured with a different over-current threshold value.

7.5. Converter Testing

A complete hardware prototype was implemented and tested in a lab setting to assess its performance and verify its functionality. One of each converter design was tested
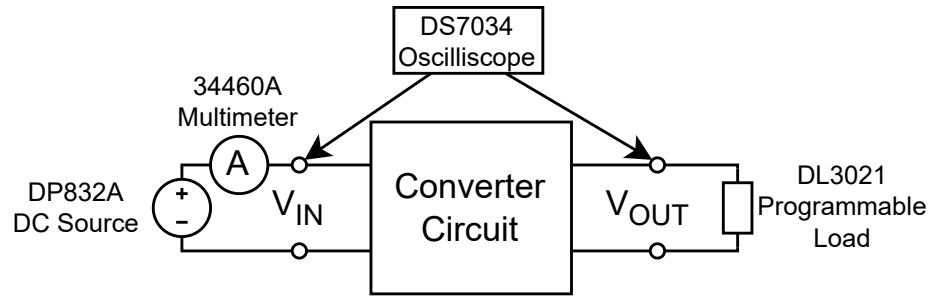
Figure 7.11.: Instrumentation and test setup to measure converter performance.

in isolation to assess the efficiency, output ripple voltage, and load regulation with different constant current loads. The test setup and instrumentation used are shown in Fig. 7.11.

7.5.1. Solar Power MPPT Converter

The solar power MPPT converter (designed using the LTC3119 buck-boost converter controller) was tested in isolation. Fig. 7.12 shows the measured efficiency and ripple voltage versus input current at different input voltages. For lower input voltages, the converter operates in the less efficient "boost" mode. Also, when the output power is low, the converter operates in a "frequency modulating" mode that improves efficiency under light load but significantly increases the ripple voltage [116]. The battery is not significantly impacted by voltage ripple and any large ripple voltage will be largely blocked by the power bus regulators before reaching devices that could be sensitive to the ripple.

The MPPT control operation was tested using two illuminated GaAs solar cells connected in series. Fig. 7.13 shows the input power and input current versus the configured output value of DAC in the MPPT control circuit. The results show the correct characteristic curves of the solar cells, demonstrating the ability of the MPPT control
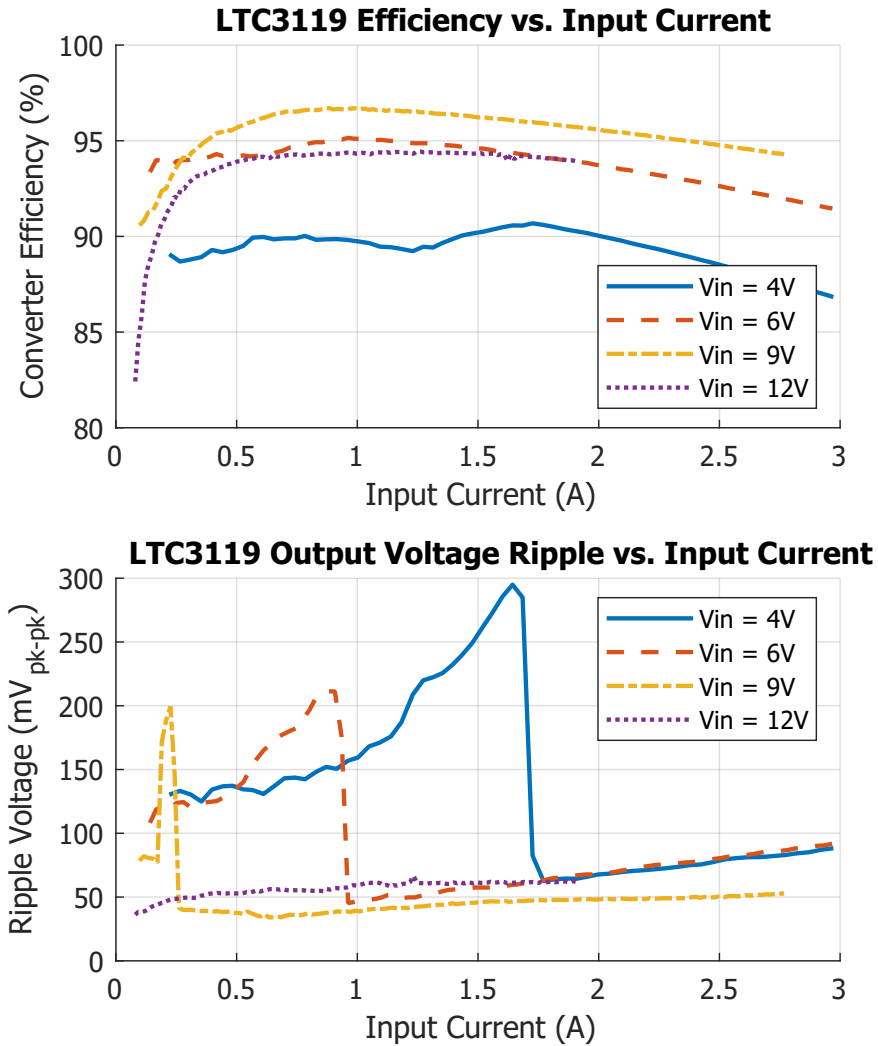
Figure 7.12.: Test results for the solar power LTC3119 converters showing efficiency and output ripple versus the input current.
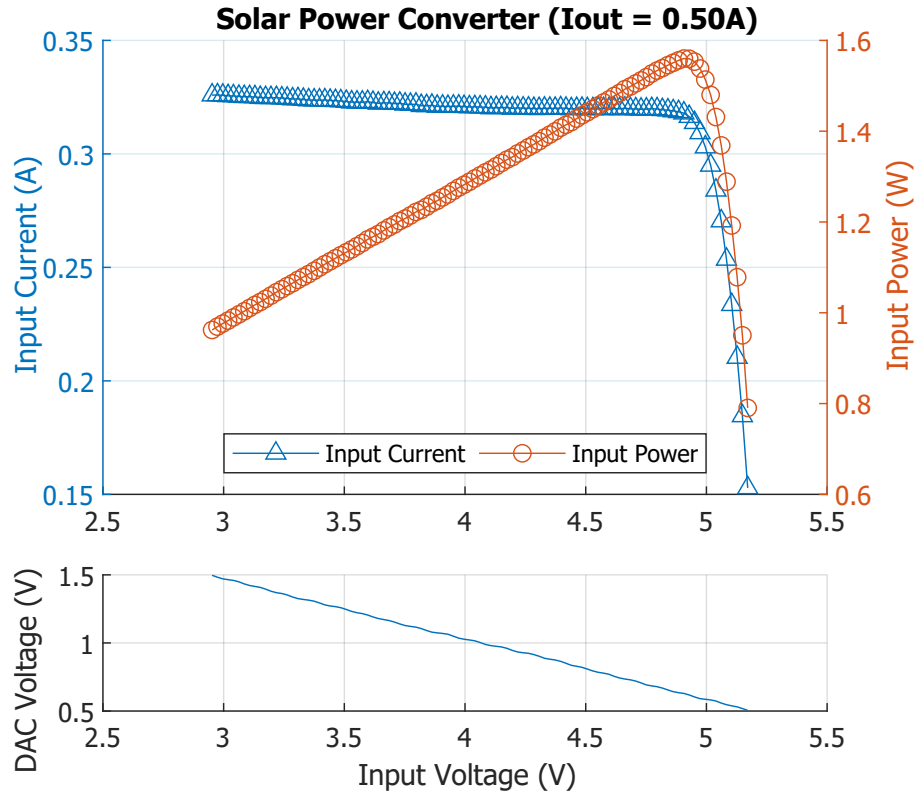
Figure 7.13.: Test results for the LTC3119 converters with a solar panel connected, showing the power point tracking capability using the DAC control circuit.

circuit to linearly control the solar array operating point across the desired operating range. The MPPT control circuit actively regulated the solar input voltage to maintain peak solar cell efficiency under varying loads and illumination. The MPPT algorithm in the firmware uses a perturb-and-observe algorithm to seek the optimal input voltage setting for the current solar cell temperature.

7.5.2. Power Bus Regulators

The regulated bus voltages (1.2 V, 3.3 V, and 5.0 V) are produced using TPS53319 buck converter controllers . Each bus voltage regulator was tested in isolation. For each converter, the measured efficiency and ripple voltage versus input current are

shown in Fig. 7.14 for four different input voltages. When the output power is low, the converter operates in a frequency-modulating mode that improves the efficiency under light load.

7.5.3. Microcontroller Low-Power Mode

The current consumption of the 1.2-V bus to the EPS microcontroller was measured with a 16-MHz oscillator during active mode (153.5 mA), and low-power sleep mode (6.9 mA), confirming a 96% reduction in power consumption.

7.6. Conclusions

An open-source EPS for CubeSats was presented, which has advanced features that improve reliability and versatility. This EPS has been tested to verify its functionality and converter performance. Future testing will include vacuum thermal cycling in a chamber, vibration testing and radiation testing. The primary limitation that determines whether this design is applicable to a particular mission is the magnitude of the power handling requirements. For example, a CubeSat with a very large solar array might produce more power at one time then the converters in this design can handle. Although significant efforts have been made to maximize the versitility of this design, interfacing considerations such as the number of individually controlled outputs and the available bus voltages are also important constraints.

The EPS architecture uses a parallel multi-channel MPPT for solar array power optimization, unregulated battery charging, and a hybrid of centralized and distributed power bus regulation. Each of 18 independently controlled and monitored output chan-
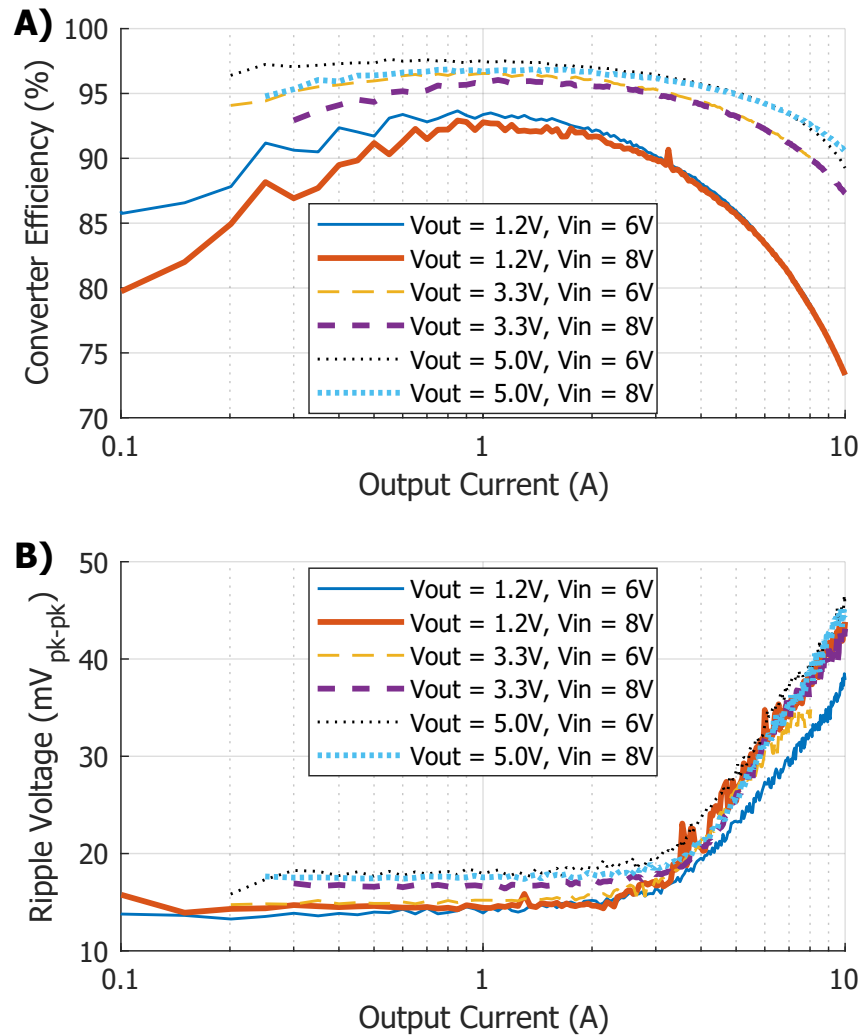
Figure 7.14.: Test results for each of the TPS53319 converters showing A) the efficiency and B) output ripple versus the input current.

nels can be connected to one of three regulated bus voltages, or to the unregulated battery voltage. Separate battery charge and discharge inhibit circuits allows separate temperate ranges and battery heater set points to be defined for safe charging and discharging. A transistor-based power inhibit circuit isolates the EPS while stowed during launch while minimizing magnetic moments and conduction loses. An adaptive SEL detection scheme works to correct the SEL detection threshold as needed throughout the mission. A network of integrated low-power sensors allow the EPS MCU to remain in a low-power sleep mode, minimizing power consumption. Future work will include integration of the battery module and solar array, and further development of the innovative features introduced in this work.

8. Conclusions

The rise of the versatile CubeSat, as an affordable platform for space exploration and research, is a game changer for rapid innovations and democratized access to space. As these satellites become increasingly complex and diverse in their applications, new solutions are needed to improve reliability while maintaining low costs and rapid development time – two characteristics that are fundamental to the concept of CubeSats. This thesis presented a research and development project that produced two new open-source tools that address two important drivers of spacecraft reliability: radiation effects and electrical power supply (EPS) design.

8.1. Radiation Effects

Purpose-built radiation-hardened devices provide the best reliability assurance for space applications, but such devices are expensive, difficult to procure, and generally lag far behind state-of-the-art computing technology. Thus, the creators of the CubeSat concept proposed using COTS components, with some characterization of radiation sensitivity for critical components. This thesis presented the development of an open-source radiation testing platform, which enables efficient and comprehensive radiation testing within particle accelerator facilities. By offering a modular, remotely

controlled setup, this platform simplifies experiment preparation, and maximizes the utility of testing time, thereby promoting data-driven component selection in CubeSat subsystem design. The proposed apparatus can hold up to 24 DUTs – four on each of six stages that are robotically positioned in the beamline. Real-time current consumption and test program data output over a serial interface is logged for each individual DUT. Each stage can be rotated within a $\pm 90°$ range to measure radiation effects with varied incidence angles. The final implemented prototype was used at the TRIUMF Proton Irradiation Facility [55] to evaluate the radiation sensitivity of four different microcontrollers. The data collected was analysed to estimate the on-orbit error rates, as shown in Table 8.1. This result clearly shows that the EFM32GG11B820F2048 MCU has a significantly higher error rate than the other DUTs, and thus is not a very good candidate to use when designing CubeSat subsystems. On the other hand, the M430FR5989SRGCREP MCU shows a significantly lower error rate, potentially making it a good option for CubeSat design.

Table 8.1.: Calculated in-orbit SEU rates for the devices tested

Manufacturer Part No.	SEU Rate (/bit/day)	MTBF per Device	SRAM
M430FR5989SRGCREP	0.90×10^{-7}	16661 hours	16 kbit
EFM32GG11B820F2048	5.53×10^{-7}	11 hours	4096 kbit
AT32UC3C0512C-ALZR	1.38×10^{-7}	339 hours	512 kbit
M2S010-TQG144I	2.52×10^{-7}	186 hours	512 kbit

8.1.1. Future Work

The radiation testing platform presented in Chapter 3 has demonstrated its potential for advancing radiation tolerance evaluation in CubeSat subsystem design. However, there are several avenues for future work that could enhance its capabilities and appli-

cability:

Improved Faulty Behavior Handling   Unexpected faulty behaviors encountered during irradiation highlighted the need for more sophisticated fault handling methods. Further research could focus on developing improved algorithms and software to automatically handle a broader range of faulty behaviors, ultimately leading to a more comprehensive and efficient testing process.

Soft Reset Analysis   While power cycling was effective in restoring normal operation following faulty behaviors, the outcomes of applying soft resets in specific scenarios could provide insights into different categories of faulty behaviors.

Real-Time Statistical Analysis   Developing a console-side user interface that offers real-time statistical analysis of recorded data could significantly enhance the platform's usability. This interface would enable operators to make more informed decisions in-situ about configuring test conditions based on trends in observed error rates.

Instantaneous Flux Rate Recording

The radiation testing experiments presented in this thesis assumed a constant radiation flux rate for each test. In reality, the flux rate varies somewhat over time. To improve accuracy, recording the instantaneous flux rate throughout each test rather than assuming a constant rate could help refine the calculation of Single Event Effects (SEE) rates.

Enhanced Data Analysis   Future efforts could focus on developing more advanced data analysis techniques to extract deeper insights or more accurate fault rate predictions from the collected data.

Additional Testing and Collaborating   Testing more devices with the proposed apparatus will provide a more comprehensive database of radiation sensitivity characteristics for various components, further assisting CubeSat developers in making informed choices. As an open-source project, this radiation testing platform can be expected to continue to evolve, contributing to more reliable and robust CubeSat designs

8.2. CubeSat Electrical Power Supply

An effective and reliable EPS is essential to any spacecraft. COTS EPS subsystems are costly, can be difficult to procure, and the technical support for university groups has proven to be quite poor. CubeSat developers need a more affordable option to acquire a proven power system. The design of an innovative open-source EPS for CubeSats was proposed to meet this demand. Preliminary testing of a hardware prototype demonstrates the performance of the converters and solar panel power point tracking capabilities. The proposed EPS design uses a parallel multi-channel MPPT architecture, and introduces a range of innovative features:

- A fixed solar panel power point control engages automatically in scenarios where MPPT software is unavailable, such as during recovery from a dead battery state.

- A charge/discharge inhibit mechanism facilitates battery heating in excessively cold conditions (between $-20\,^{\circ}\mathrm{C}$ and $0\,^{\circ}\mathrm{C}$).

- A transistor-based power inhibit solution, that guarantees power-off status during launch vehicle stowage, reduces power wastage by preventing conduction losses from switch wiring. This feature also mitigates potential magnetic interference with the CubeSat attitude control system.

- Intelligent sensors autonomously monitor critical parameters like current, voltage, and temperature, alerting the microcontroller only under system-critical circumstances, like over-current events. This self-governing feature reduces power consumption by eliminating constant microcontroller polling.

- A versatile jumper matrix enabling regulated or unregulated bus voltage allocation across 18 output channels, supported by synchronized fault response capabilities for co-dependent channels.

- Adaptive single-event latchup detection compenses for the gradual rise in leakage currents due to accumulated total ionizing dose (TID) effects over the mission's duration.

The proposed EPS design aims to provide similar or better performance and capabilities, compared with state-of-the-art COTS EPS solutions for CubeSats. Thus, this open-source project provides a new resource for CubeSat groups to develop capable, reliable and cost-effective power systems for their missions. In future work, the proposed EPS design will be further verified with environmental testing, and a technology demonstration aboard the Ex Alta 3 CubeSat, being developed by the AlbertaSat team at the University of Alberta [5].

The solutions presented in this thesis have been developed with the intention of being published under an open-source license, thus contributing to the global community of university CubeSat groups. Hopefully, these contributions will bolster CubeSat mission success, and promote collaborative innovation within the space exploration community.

8.2.1. Future Research and Development

Transistor-Based Power Inhibit Solution: Further validation and testing of the transistor-based power inhibit solution, including its integration into the actual deployment process and thorough hazard assessment, would be essential before it can be considered as a reliable alternative to mechanical switches.

Thermal Management Optimization The thermal performance of the EPS, particularly in extreme temperature environments, warrants thorough evaluation and optimization. Conducting detailed thermal simulations and experiments would identify potential hotspots and cold spots within the EPS assembly. Additional measures, such as improved thermal interfaces, could be explored to ensure stable and efficient operation.

Environmental Testing The proposed EPS design should undergo comprehensive environmental testing to validate its robustness and performance under relevant operating conditions. This includes subjecting the EPS to thermal cycling, vibration, and radiation tests to mimic the challenges it would face in space. Testing will help uncover potential weaknesses and allow for necessary adjustments and improvements.

Integration with CubeSat Platforms Integrating the EPS design into an actual CubeSat would provide better insights into its compatibility and performance in real-world scenarios. Feedback from or collaboration with CubeSat mission developers that use the proposed EPS could help identify any challenges or areas for improvement.

Mission-Ready Software Further development and documentation of the real-time software architecture is necessary for mission readiness. Additionally, the EPS software could be further optimized by developing more advanced algorithms for MPPT and SEL fault detection, as well as implementing.

Technology Readiness Level Before the EPS can be considered to be a credible candidate to be a critical subsystem for a CubeSat mission it must undergo thorough validation and demonstrate its long-term reliability in a space environment. By implementing the EPS as a technology demonstration payload on the Ex-Alta 3 CubeSat mission, the EPS design would advance along the technology readiness level (TRL) scale by gaining real-world space environment data and validation. This will help evaluate factors such as hardware performance, software robustness, thermal performance, and fault tolerance.

Documentation and Knowledge Sharing Further developing comprehensive documentation for the EPS design, including detailed specifications, guidelines for integration, and operational procedures would help promote future use of the EPS design for diverse missions.

Battery Module Development The battery module shown in Fig. 8.1, a fundamental component of the electrical power system, is currently still being developed. As a critical energy source for the CubeSat, the battery module requires dedicated efforts. This includes detailed design of the battery charging circuitry, and the necessary monitoring and control circuits. Once the battery module design is complete, it will be tested to ensure it meets the requirements of the NanoRacks CubeSat Deployer System [120].
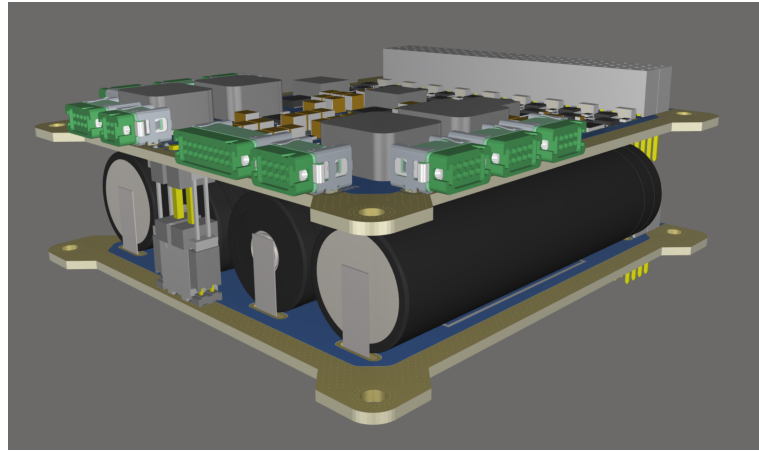
Figure 8.1.: Rendering of the unfinished battery module with four 18650 LIBs, left as future work.

By addressing these areas of future work, the proposed EPS design can evolve from a promising concept to a mature and reliable power system solution for CubeSats. The collaborative efforts of the CubeSat community, along with rigorous testing and real-world mission experience, will contribute to the overall success and advancement of CubeSat technology.

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Appendices

A. TRIUMF BL2C Details for SRIM Simulation
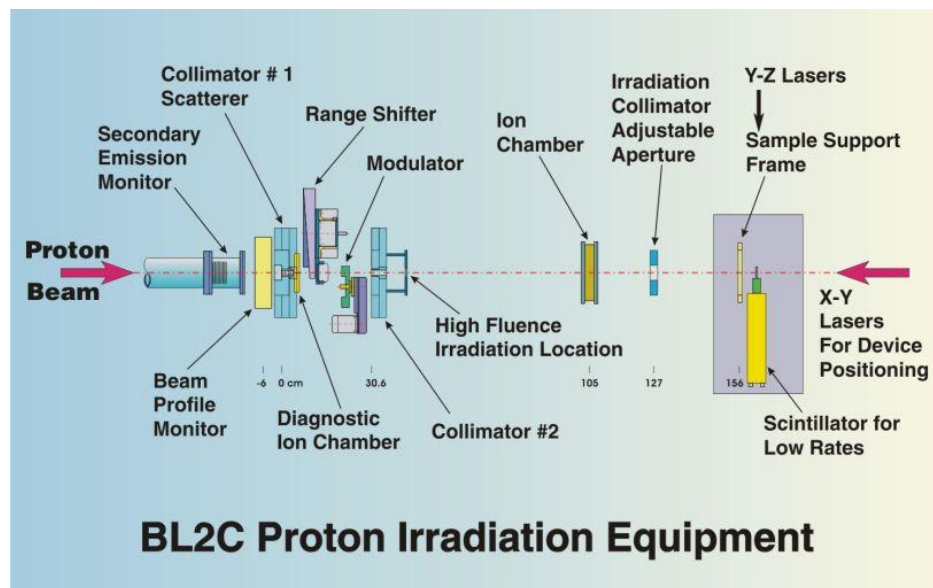
Figure A.1.: Schematic layout of the irradiation equipment in beamline 2C at the TRIUMF proton irradiation facility (image from [14] © 2019 TRIUMF).

Table A.1.: Materials and their thicknesses between the proton beam source and the DUT for the BL2C beamline.

Description	Material	Thickness	Medium to Next Layer	Medium Thickness
Secondary emission monitor	Al	76.2 μm	Vacuum	79.95 mm
Beam exit window	Steel	25.4 μm	Air	152.96 mm
Beam profile monitor	Al	50.8 μm	Air	66.17 mm
Collimator #1 Scatterer	Pb	800 μm	Air	44.95 mm
Diagnostic Ion Chamber	Al	101.6 μm		
Air and degrader wheel*	Air and Lucite	54.95 mm	Air	949.9 mm
Main Ion Chamber	Kapton	203.2 μm	Air	509.9 mm
Approximate DUT Encapsulation	Epoxy	500.0 μm		

* Lucite degrader wheel thickness can be 2.23 mm to 30.44 mm.

B. Open-Source Radiation Testing Platform Schematics

P11 (Header 8): ENC_D0, ENC_D1, ENC_D2, ENC_D3 — pins 1-8, GND

P12 (Header 8): ENC_D4, ENC_D5, ENC_D6, ENC_D7 — pins 1-8, GND

P13 (Header 8): USART0_RX, USART1_RX, USART3_RX, USART2_RX — pins 1-8, GND; TXD, TXA, TXB, TXC

P14 (Header 8): USART4_RX, USART4_TX, I2C2_SCL, I2C2_SDA — pins 1-8, GND

P5 (22112062): USART1_TX, USART1_RX, USART3_TX, USART3_RX, USART2_TX, USART2_RX — pins 1-6; RXA, TXA, RXB, TXB, RXC, TXC

P15 (Header 8): CH_A, CH_B, CH_1, ENC_SEL — pins 1-8, GND

P4 (22112062): USART0_TX, USART0_RX, I2C2_SCL, I2C2_SDA — pins 1-6; RXD, TXD, 3V3, GND

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3V3 R2 1k D2 RED EN4
R20 10k GND GND
GND4 Q2 AOD508

3V3 R4 1k D4 RED EN5
R22 10k GND GND
GND5 Q8 AOD508

3V3 R6 1k D6 RED EN6
R24 10k GND GND
GND6 Q10 AOD508

GND4
P2 EBC10DRAS
TXA4 VA TXB4 PWM VB RXC4 RXD4
RXA4 RXB4 VC PWM TXC4 VD TXD4
3V3 3V3 GND4

GND5
P4 EBC10DRAS
TXA5 VA TXB5 PWM VB RXC5 RXD5
RXA5 RXB5 VC PWM TXC5 VD TXD5
3V3 3V3 GND5

GND6
P6 EBC10DRAS
TXA6 VA TXB6 PWM VB RXC6 RXD6
RXA6 RXB6 VC PWM TXC6 VD TXD6
3V3 3V3 GND6

GND1
P1 EBC10DRAS
TXA1 VA TXB1 PWM VB RXC1 RXD1
RXA1 RXB1 VC PWM TXC1 VD TXD1
3V3 3V3 GND1

GND2
P3 EBC10DRAS
TXA2 VA TXB2 PWM VB RXC2 RXD2
RXA2 RXB2 VC PWM TXC2 VD TXD2
3V3 3V3 GND2

GND3
P5 EBC10DRAS
TXA3 VA TXB3 PWM VB RXC3 RXD3
RXA3 RXB3 VC PWM TXC3 VD TXD3
3V3 3V3 GND3

GND1 Q1 AOD508 GND
R19 10k GND
3V3 R1 1k D1 RED EN1

GND2 Q3 AOD508 GND
R21 10k GND
3V3 R3 1k D3 RED EN2

GND3 Q9 AOD508 GND
R23 10k GND
3V3 R5 1k D5 RED EN3

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EFM32HG110F64G

U16

PA0 1
PB7 5
PB8 6
PB11 8
PB13 10
PB14 11
PC0 3
PC1 4
PC14 17
PC15 18
PD6 13
PD7 14
PE12 23
PE13 24
PF0 19
PF1 20
PF2 21

IOVDD_0 2
IOVDD_5 22
VDD_DREG 15
AVDD_0 12
AVDD_2 9
DECOUPLE 16
#RESET 7
VSS 25

TP1
PWM
LFXIN
HFXIN
SDA
SCL
DBG_SWCLK
DBG_SWDIO
DBG_SWO

R33 10k
VDDD
D7 BLUE

3V3
L1
R34
R32
C20 10µF
GND

VDDA
VDDD
C23 0.1µF
C22 0.1µF
C21 0.1µF
GND

C27 10µF
C26 10000pF
C25 10000pF
GND

C28 1µF
GND

#RESET
C29 0.1µF
GND
GND

RN2D 1k
R35 1k
RN2A 1k
VDDD
C24 0.1µF
GND

P10
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
ARM SWD

R36 10k
GND
GND

RN2B 1k
RN1B 1k
RN1A 1k
RN2C 1k
VDDD

DBG_SWCLK
DBG_SWDIO
DBG_SWO
#RESET

U17
HFXIN 3
VDD
OUT 1
STBY 2
GND
VDD 4
ASDMB 24MHz
VDDD
C30 10000pF
GND

U18
SCL 6
SDA 7
#INT 2
CLKOUT 5
VDD 8
CLKOE 1
NC 3
VSS 4
RTCMK 32.768kHz
LFXIN
VDDD
C31 0.1µF
GND
GND

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Schematic Labels

P7 — 22112042
- 1 RXA
- 2 TXA
- 3 RXB
- 4 TXB

P8 — 22112042
- 1 RXC
- 2 TXC
- 3 RXD
- 4 TXD

P9 — 22112042
- 1 SCL
- 2 SDA
- 3
- 4

3V3

R30 1k — 3V3
R31 1k — 3V3

GND

P11 — Header 2
- 1 3V3
- 2 GND

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C. openEPS Electrical Power Supply Datasheet

openEPS Electrical Power Supply Datasheet

Author: Stefan Damkjar (sdamkjar@ualberta.ca)

Licensing Notice

Acknowledgements

1

System Description

The openEPS Electrical Power Supply (EPS) is intended for mission critical power management on CubeSats. The system includes four independent maximum power point tracking converters, each with two solar panel connectors. Up to four parallel sets of two-cell series strings (up to eight cells in total) of lithium-ion batteries can be connected to the battery module interface. Each of 18 independantly controlled output channels can be connected to any of the regulated bus voltages, or to the unregulated battery voltage. Current, voltage and temperature sensors provide comprehensive system monitoring and threshold limit control. The system was developed as an open source initiative at the University of Alberta in hopes that it will be useful to other groups developing small, low-cost satellites.
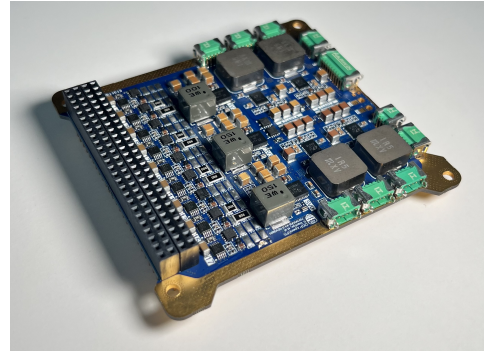
Figure 1: Photograph showing a fully implemented prototype of the openEPS for CubeSats

Highlighted Features

- Four parallel MPPT converters, each with a maximum input power capacity of 24 W, and a maximum input current of 3 A

- Three regulated bus voltages (1.2V, 3.3V, and 5.0V) with independent voltage and current monitoring and protection

- 18 independently controlled power output channels with voltage and current monitoring and both hardware and software controlled over current protection thresholds

- Independently monitored and protected 3.3V power output channel to solar panel interfaces for solar panel mounted sensors or deployment actuation

- Controlled with CANbus, UART, or SPI interface using the CubeSat Space Protocol (CSP) network protocol

- Configurable ground station watchdog timer to recover from failure to connect with a ground station

Open Source Links

https://github.com/sdamkjar/openEPS

Contents

1 Electrical Specifications

1.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings (Table 1) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated throughout the rest of this document is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability and lifetime.

Table 1: Absolute maximum ratings

Parameter	Min	Max	Units
Solar Panel Connectors (P1 to P8)			
Solar panel input V+	−0.3	19.0	V
Solar panel I2C pins	−0.5	7.0	V
3.3V supply to solar panels	−0.3	19.0	V
Inhibit Switch Connector (P9)			
Any inhibit switch connector pin	−0.6	10	V
Flight Preparation Panel (FPP) Connector (P10)			
JTAG inputs: TCK, TMS, TDI, nTRST	−0.5	6.5	V
JTAG outputs: TDO	−0.3	4.6	V
Debug UART (RX, TX)	−0.5	6.5	V
RBF ground charge enable	−12	12	V
RBF always on, always off	−0.6	10	V
RBF deploy disable	−0.3	4.6	V
Battery Module Connector (P11)			
Battery V+	−0.3	19.0	V
Battery module I2C pins	−0.5	7.0	V
3.3V supply to battery module	−0.3	19.0	V
Stack Connector (H1 and H2)			
Stack connector SPI or UART (MISO, MOSI, CLK, nCS, RX, TX)	−0.3	4.6	V
CANbus terminals (CANH, CANL)	−14	14	V
Any power output channel	−0.3	19.0	V

Table 2: Operating environment ratings

Parameter	Test Conditions	Min	Max	Units
Pin Current Ratings				
P1 to P10 current rating per pin			2.0	A
H1,H2 current rating per pin			6.2	A
Temperature Ratings [1]				
Operating temperature	Free-air	−40	105	°C
	Vacuum	−40	TBD	°C
Junction temperature [2]		−40	130	°C
Storage temperature		−40	150	°C

[1] Ratings for EPS module only! (NOT including battery module or solar panels)

[2] Thermal shutdown protection is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

1.2 MPPT Converters

Electrical specifications of the MPPT converters is given in Table 3. The MPPT converters are designed using the LTC3119 buck-boost converter controller. All specifications are at 25 °C unless otherwise specified.

Table 3: MPPT Converter and solar panel interface electrical specifications

Parameter	Test Conditions	Min	Typ	Max	Units
Input voltage (V_{PVIN})		3.0		18.0	V
Input current per converter	$V_{PVIN} = 3.0\,\text{V}$			6.0	A
	$V_{PVIN} = 18.0\,\text{V}$			1.3	A
Input power per converter (P_{PVIN})	$V_{PVIN} > 8.0\,\text{V}$			24	W
Solar panel connector V+ current in				6.0	A
Solar panel connector 3.3V current out				2.0	A
Output ripple voltage	See Fig. 3				
Switching frequency			400		kHz
Output soft-start rise-time			6		ms
Input under-voltage lock-out	Falling (ON to OFF)	2.44	2.50	2.56	V
	Rising (OFF to ON)	2.60	2.70	2.80	V
Output voltage limit		7.92	8.00	8.08	V
Thermal shutdown threshold			165		°C
Converter efficiency	See Fig. 2				
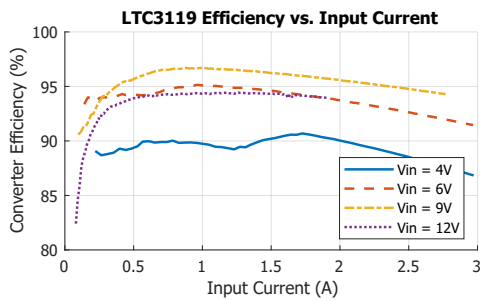
Figure 2: MPPT converter efficiency
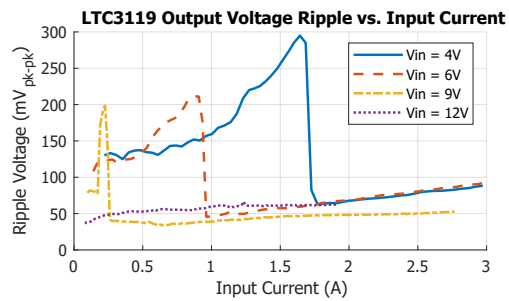
Figure 3: MPPT converter ripple voltage.

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1.3   Bus Regulators

Electrical specifications of the bus regulators is given in Table 4. The bus regulators are designed using the TPS53319 buck converter controller. All specifications are at 25 °C unless otherwise specified.

Table 4: 1.2 V Bus regulator electrical specifications

Parameter	Test Conditions	Min	Typ	Max	Units
Output current				8	A
Output voltage		1.15	1.20	1.21	V
Output ripple voltage	**See Fig.** TBD				
Switching frequency		250	300	350	kHz
Output soft-start rise-time			0.7		ms
Input under-voltage lock-out	Falling (ON to OFF)	4.25	4.45	4.58	V
	Rising (OFF to ON)	4.00	4.20	4.33	V
Output under-voltage protection		0.78	0.84	0.9	V
Output under-voltage protection delay		0.8	1.0	1.2	ms
Output over-voltage protection		1.38	1.44	1.5	V
Output over-voltage protection delay			1		μs
Thermal shutdown threshold			145		°C
Converter efficiency	**See Fig.** TBD				

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Table 5: 3.3 V Bus regulator electrical specifications

Parameter	Test Conditions	Min	Typ	Max	Units
Output current				6	A
Output voltage		3.22	3.30	3.33	V
Output ripple voltage	**See Fig.** TBD				
Switching frequency		250	300	350	kHz
Output soft-start rise-time			0.7		ms
Input under-voltage lock-out	Falling (ON to OFF)	4.25	4.45	4.58	V
	Rising (OFF to ON)	4.00	4.20	4.33	V
Output under-voltage protection		2.15	2.31	2.48	V
Output under-voltage protection delay			0.7		ms
Output over-voltage protection		3.80	3.96	4.13	V
Output over-voltage protection delay			1		μs
Thermal shutdown threshold			145		°C
Converter efficiency	**See Fig.** TBD				

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Table 6: 5.0 V Bus regulator electrical specifications

Parameter	Test Conditions	Min	Typ	Max	Units
Output current				4	A
Output voltage		4.90	5.00	5.05	V
Output ripple voltage	**See Fig.** TBD				
Switching frequency		250	300	350	kHz
Output soft-start rise-time			0.7		ms
Input under-voltage lock-out	Falling (ON to OFF)	4.25	4.45	4.58	V
	Rising (OFF to ON)	4.00	4.20	4.33	V
Output under-voltage protection		3.25	3.50	3.75	V
Output under-voltage protection delay			0.7		ms
Output over-voltage protection		5.75	6.00	6.25	V
Output over-voltage protection delay			1		μs
Thermal shutdown threshold			145		°C
Converter efficiency	**See Fig.** TBD				

2 Mechanical Specifications

Table 7: Mechanical Specifications

Parameter	Test Conditions	Min	Typ	Max	Units
Overall Dimensions			$93.3 \times 87.6 \times 15.3$		mm
Mass	No battery		93.00		g

D. openEPS Schematics and Layout

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VOUT

C76_3 22μF
C75_3 22μF
C74_3 22μF
C73_3 1μF
GND

R93_3 178k
R94_3 20k
GND

C77_3 680pF
R100_3 40.2k
GND

R99_3 200k
GND

GND

C69_3 0.22μF

L4_3 1.5μH MPXV1D1264L1R5

SW2 SW2
BST2
PVOUT
PVOUT
FB
VC
RT
PWM/SYNC
NC
NC
NC
SGND

SW1 SW1
BST1
PVIN
PVIN
VIN
RUN
MPPC
VCC
SVCC
PGOOD
PGND
PGND
PGND
PGND
PGND

LTC3119
U21_3

C68_3 0.22μF

C78_3 4.7μF
GND

GND

R92_3 158k
R98_3 127k
GND

R91_3 470k
R97_3 95.3k
GND

C72_3 1μF
GND

R96_3 1.27k
C79_3 4.7μF

C71_3 1μF
GND

C70_3 22μF
R95_3 28k
GND

VIN

MPPT

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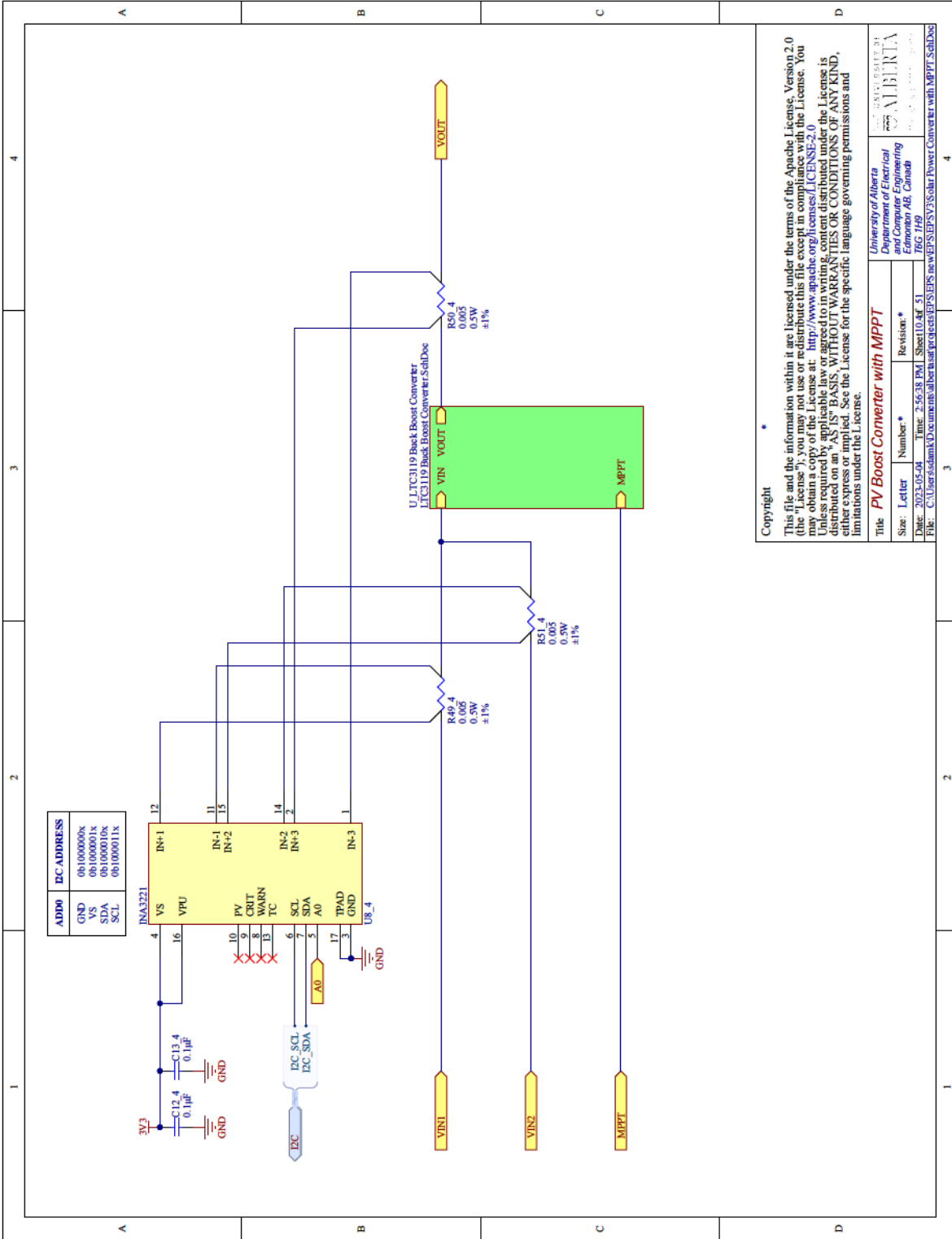Edmonton AB, Canada
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RTCMK_I2C

I2C_SCL
I2C_SDA

I2C

#INT

RTC_CLK

U15
RV-3032-C7

SCL
SDA
#INT
CLKOUT

VDD
EVI
VBU
VSS

6
4
1
5

8
2
3
7

I2C Address: 0b1010001x

3V3

C22
0.1µF
GND

C23
0.1µF
GND

C24
22µF
GND

C25
22µF
GND

C26
22µF
GND

C27
22µF
GND

GND

D2
BAS116
Voltage - Forward (Max): 1.25 V @ 150 Ma
Current - Reverse Leakage: 5 nA @ 75 V

R58
49.9

3V3

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Title RTCMK RTC

Size: Letter | Number:8 | Revision:*

Date: 2023-05-04 | Time: 2:56:38 PM | Sheet8 of 51
File: C:\Users\sdank\Documents\albertasd\projects\EPS\EPSV3\RV-3032-C7RTC.SchDoc

Schematic: PV Boost Converter with MPPT

ADD0	I2C ADDRESS
GND	0b1000000x
VS	0b1000001x
SDA	0b1000010x
SCL	0b1000011x

INA3221

U8_1

VS 4
VPU 16

IN+1 12

IN-1 11
IN+2 15

IN-2 14
IN+3 2

IN-3 1

PV 10
CRIT 9
WARN 8
TC 13

SCL 6
SDA 7
A0 5

TPAD 17
GND 3

C12_1 0.1µF 3V3 GND
C13_1 0.1µF GND

I2C_SCL
I2C_SDA
I2C

A0
GND

R49_1 0.005 0.5W ±1%
R51_1 0.005 0.5W ±1%
R50_1 0.005 0.5W ±1%

U_LTC3119 Buck Boost Converter
LTC3119 Buck Boost Converter.SchDoc
VIN   VOUT

MPPT

VIN1
VIN2
MPPT
VOUT

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Title: PV Boost Converter with MPPT
Size: Letter   Number: *   Revision: *
Date: 2023-05-04   Time: 2:56:38 PM   Sheet 10 of 51
File: C:\Users\adamk\Documents\alberta\sat\projects\EPS\EPS new\EPS\PS V3\Solar Power Converter with MPPT.SchDoc

Title PV Boost Converter with MPPT

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Size: Letter | Number:* | Revision:*
Date: 2023-05-04 | Time: 2:56:38 PM | Sheet10 of 51
File: C:\Users\adamk\Documents\alberta\asf\projects\EPS\EPS.new\EPS\PSV3\Solar Power Converter with MPPT.SchDoc

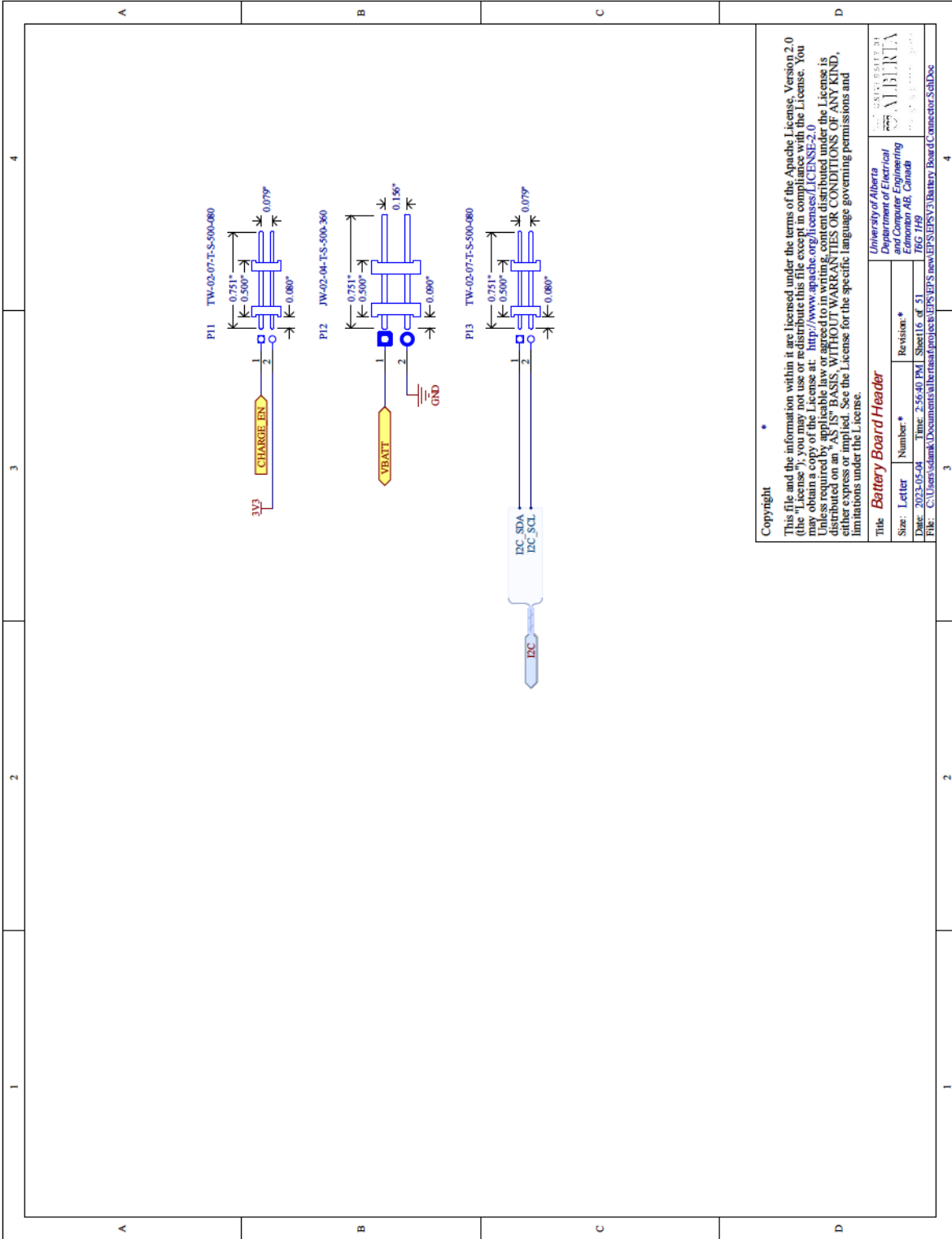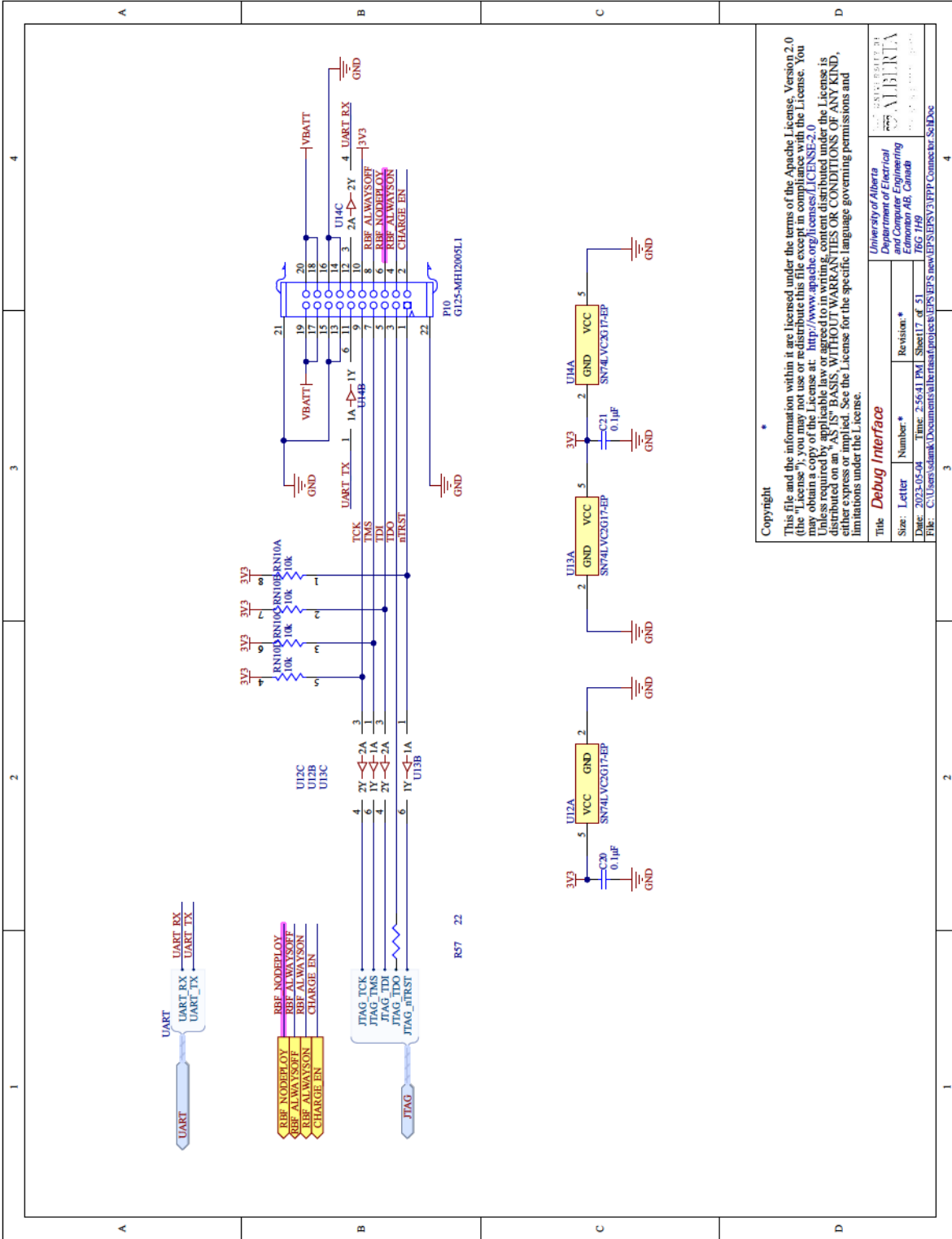| ADD0	I2C ADDRESS
GND	0b1000000x
VS	0b1000001x
SDA	0b1000010x
SCL	0b1000011x

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Title: PV Boost Converter with MPPT

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Size: Letter   Number:*   Revision:*
Date: 2023-05-04   Time: 2:56:38 PM   Sheet10.3of 51
File: C:\Users\adamk\Documents\albertasatforgprojects\EPS\EPS new\EPS\EPS V3\Solar Power Converter with MPPT.SchDoc

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Title PV Boost Converter with MPPT

Size: Letter | Number:* | Revision:*

Date: 2023-05-04 | Time: 2:56:38 PM | Sheet 10.4 f 51

File: C:\Users\adamk\Documents\albertasat\projects\EPS\EPS new\EPS\PS V3\Solar Power Converter with MPPT.SchDoc

U_LTC3119 Buck Boost Converter
LTC3119 Buck Boost Converter.SchDoc

VIN VOUT

MPPT

R50_4
0.005
0.5W
±1%

R51_4
0.005
0.5W
±1%

R49_4
0.005
0.5W
±1%

VOUT

INA3221

ADD0	I2C ADDRESS
GND	0b1000000x
VS	0b1000001x
SDA	0b1000010x
SCL	0b1000011x

VS
VPU

IN+1
IN-1
IN+2
IN-2
IN+3
IN-3

PV
CRIT
WARN
TC

SCL
SDA
A0

TPAD
GND

U8_4

12
11
15
14
2
1

4
16

10
9
8
13

6
7
5

17
3

C13_4
0.1µF

C12_4
0.1µF

3V3

GND

GND

A0

I2C
I2C_SCL
I2C_SDA

GND

VIN1

VIN2

MPPT

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Title   AD5324 Digital-to-Analog Converter
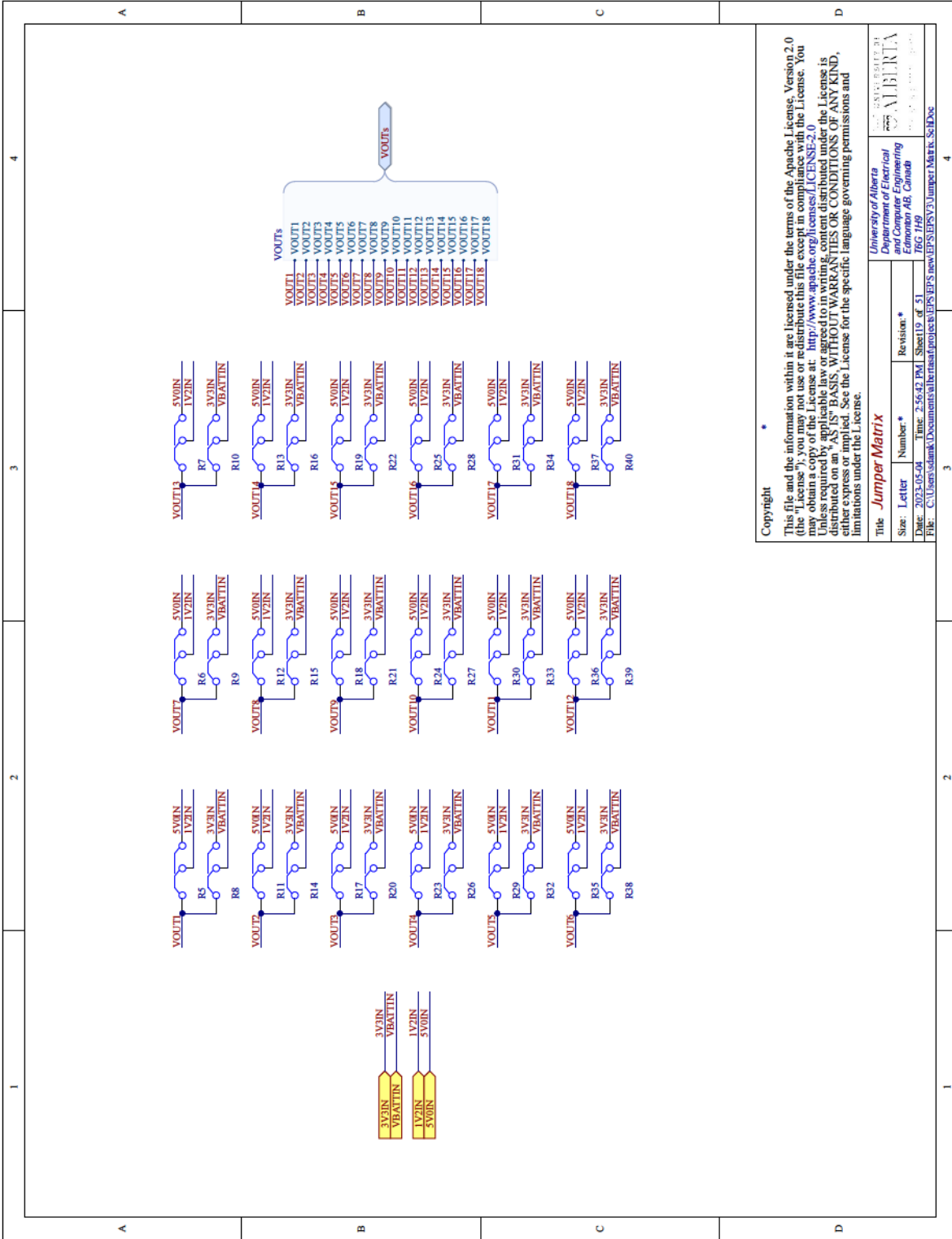
Size: Letter   Number:*   Revision:*

Date: 2023-05-04   Time: 2:56:39 PM   Sheet 12 of 51
File: C:\Users\sdank\Documents\albertasd\projects\EPS\EPS\EPS new\EPS\PSV3\AD5324 Digital-to-Analog Converter.SchDoc

MPPT3

MPPT4

MPPT1

MPPT2

P5 G125-MH11005L1
P6 G125-MH11005L1
P7 G125-MH11005L1
P8 G125-MH11005L1
P1 G125-MH11005L1
P2 G125-MH11005L1
P3 G125-MH11005L1
P4 G125-MH11005L1

PV_3V3
GND

PV SDA3
PV SCL3
PV V+5

PV SDA4
PV SCL4
PV V+6

PV SDA2
PV SCL2
PV V+7

PV SDA1
PV SCL1
PV V+8

PV SDA5
PV SCL5
PV V+1

PV SDA6
PV SCL6
PV V+2

PV SDA7
PV SCL7
PV V+3

PV SDA8
PV SCL8
PV V+4

I2C1 I2C_SCL I2C_SDA
I2C2 I2C_SCL I2C_SDA
I2C3 I2C_SCL I2C_SDA
I2C4 I2C_SCL I2C_SDA
I2C5 I2C_SCL I2C_SDA
I2C6 I2C_SCL I2C_SDA
I2C7 I2C_SCL I2C_SDA
I2C8 I2C_SCL I2C_SDA

PV SDA1 PV SCL1
PV SDA2 PV SCL2
PV SDA3 PV SCL3
PV SDA4 PV SCL4
PV SDA5 PV SCL5
PV SDA6 PV SCL6
PV SDA7 PV SCL7
PV SDA8 PV SCL8

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RESETIN INPUT THRESHOLD VOLTAGE

CONDITION	MIN	TYP	MAX
RESETIN RISING	1.135V	1.255V	1.383V
RESETIN FALLING	1.115V	1.235V	1.363V

ON_RBF

WDT_WDI

Populate R55 after programming MCU

R54 0

OFF_RBF

U9 MAX16998A

C16 1µF

GND

WDI
nEN
nRESET
IN
RESETIN
SRT
SWT
GND
GND

C14 0.1µF
GND

C15 0.22µF
GND

R52 1M

R53 383k
GND

WDT_nRSTIN

U10 MIC5019

R55 1M

GND

VIN

C17 4.7µF
GND

Q4 TPN1R603

Q5 TPN1R603

VOUT

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Title: Watchdog Circuit

Size: Letter | Number: * | Revision: *

Date: 2023-05-04 | Time: 2:56:40 PM | Sheet 15 of 51

File: C:\Users\slamk\Documents\alberta\atf\projects\EPS\EPS new\EPS\EPS V3\MAX16998A Watchdog Circuit.SchDoc

P11   TW-02-07-T-S-500-080
P12   JW-02-04-T-S-500-360
P13   TW-02-07-T-S-500-080

CHARGE_EN
3V3
VBATT
GND
I2C_SDA
I2C_SCL
I2C

0.079"
0.751"
0.500"
0.080"
0.156"
0.090"

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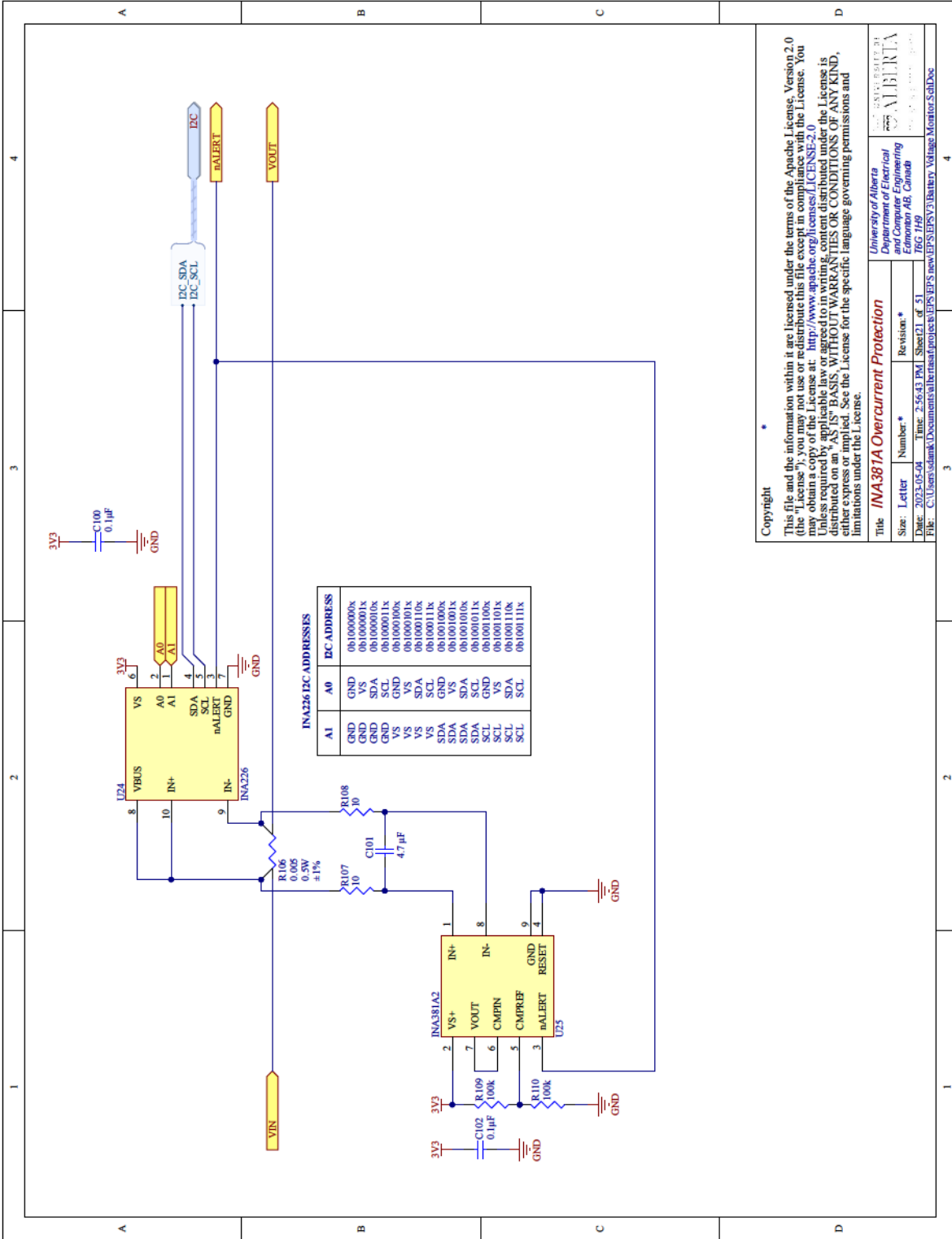UNIVERSITY OF ALBERTA

Title Battery Board Header

Size: Letter   Number: *   Revision: *
Date: 2023-05-04   Time: 2:56:40 PM   Sheet 16 of 51
File: C:\Users\sdamk\Documents\albertasat\projects\EPS\EPS new\EPS\EPS V3\Battery Board Connector.SchDoc

UART
UART_RX — UART RX
UART_TX — UART TX

RBF_NODEPLOY — RBF NODEPLOY
RBF_ALWAYSOFF — RBF ALWAYSOFF
RBF_ALWAYSON — RBF ALWAYSON
CHARGE_EN — CHARGE EN

JTAG
JTAG_TCK — TCK
JTAG_TMS — TMS
JTAG_TDI — TDI
JTAG_TDO — TDO
JTAG_nTRST — nTRST

R57 22

U12C / U2B / U13C
2Y - 2A
1Y - 1A
2Y - 2A
1Y - 1A U13B

RN101 10k
RN100 10k
RN101 10k
RN100 10k
3V3

P10
G125-MH12005L1

UART TX
UART RX
VBATT
VBATT
GND
3V3
GND
TCK
TMS
TDI
TDO
nTRST

1A - 1Y U14B
2A - 2Y U14C
RBF_ALWAYSOFF
RBF_NODEPLOY
RBF_ALWAYSON
CHARGE EN
GND

U12A
VCC GND
SN74LVC2G17-EP
3V3
C20 0.1µF
GND

U13A
GND VCC
SN74LVC2G17-EP
GND

U14A
GND VCC
SN74LVC2G17-EP
3V3
C21 0.1µF
GND
GND

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Title: Debug Interface
Size: Letter   Number: *   Revision: *
Date: 2023-05-04   Time: 2:56:41 PM   Sheet 17 of 51
File: C:\Users\adamk\Documents\alberta\sat\projects\EPS\EPS.new\EPS\EPS\V3\PPP.Connector.SchDoc

TCAN337

U3	
SHDN 5	3 VCC
TXD 1	CANH 7
RXD 4	CANL 6
S 8	2 GND

R41 60.4
R42 60.4
C5 4700pF
GND

3V3
C6 0.1μF
GND

GND

CANH
CANL

CANbus

CAN P
CAN N

SHDN
CAN
S

CAN TX
CAN RX

CAN_TX
CAN_RX

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Title: **Jumper Matrix**

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Size: Letter | Number: * | Revision: *
Date: 2023-05-04 | Time: 2:56:42 PM | Sheet 19 of 51
File: C:\Users\sdank\Documents\altertasafprojects\EPS\EPS\EPS3\Jumper Matrix.SchDoc

VOUTs

VOUT1 VOUT2 VOUT3 VOUT4 VOUT5 VOUT6 VOUT7 VOUT8 VOUT9 VOUT10 VOUT11 VOUT12 VOUT13 VOUT14 VOUT15 VOUT16 VOUT17 VOUT18

3V3IN VBATTIN 1V2IN 5V0IN

HEADER PLACEMENT

TOP SIDE

Pin 1 H1 H2

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Title EPS stack header

Size: Letter   Number: *   Revision: *
Date: 2023-05-04   Time: 2:56:43 PM   Sheet 20 of 51
File: C:\Users\sdamk\Documents\alberta\asf.projects\EPS\EPS\EPS v3\EPS new\EPS\EPS V3\EPS Stack Header.SchDoc
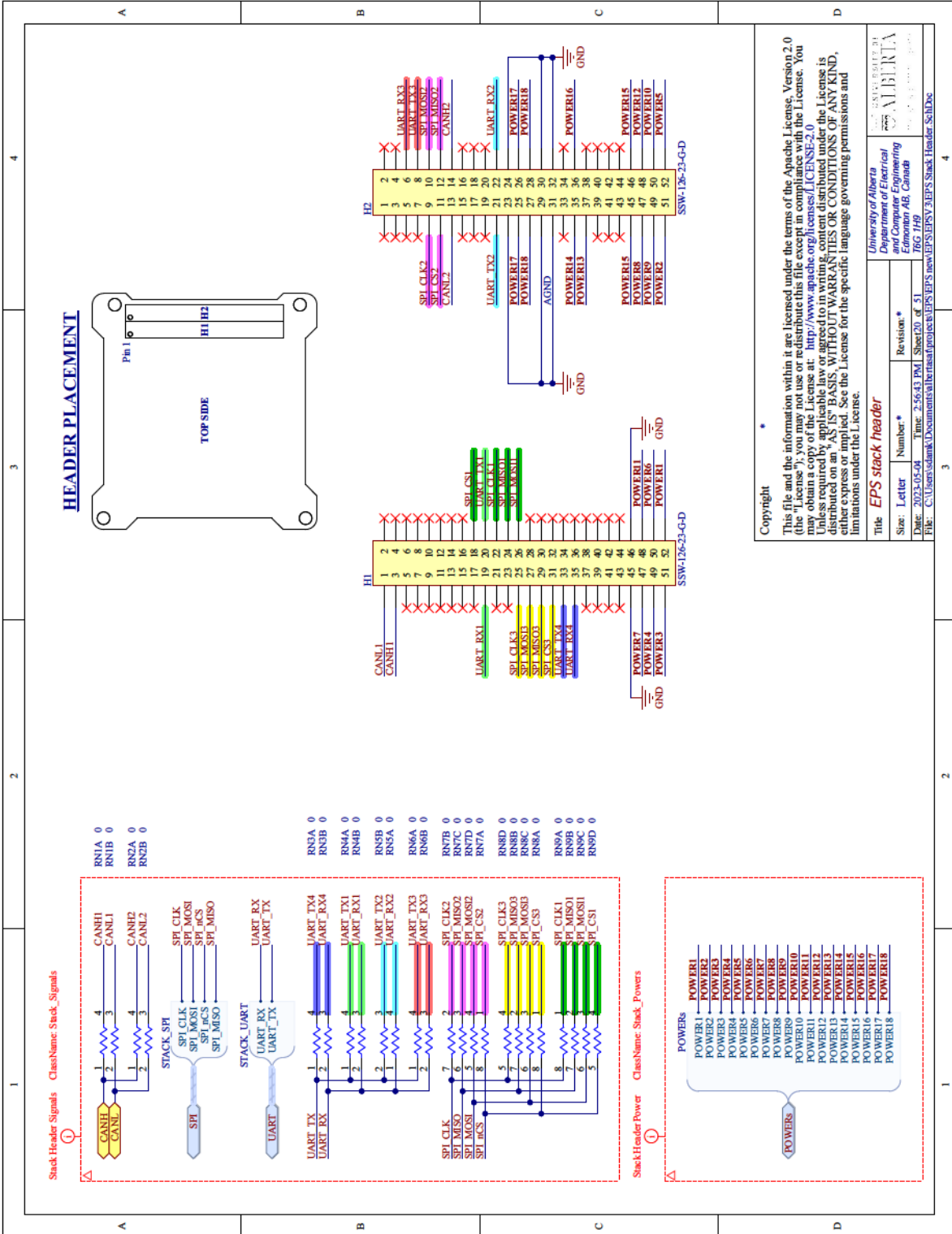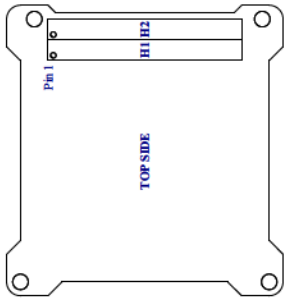
Stack Header Signals   ClassName: Stack_Signals

Stack Header Power   ClassName: Stack_Powers

H1   SSW-126-23-G-D
H2   SSW-126-23-G-D

CANH1
CANL1
CANH2
CANL2

SPI_CLK
SPI_MOSI
SPI_nCS
SPI_MISO

STACK_SPI

UART_RX
UART_TX

STACK_UART

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Title INA381A Overcurrent Protection

Size: Letter | Number:* | Revision:*

Date: 2023-05-04 | Time: 2:56:43 PM | Sheet 21 of 51

File: C:\Users\sdamk\Documents\albertasaf\projects\EPS\EPS new\EPS\EPSV3\Battery Voltage Monitor.SchDoc

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INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

U24 INA226
VBUS
IN+
IN-
VS
A0
A1
SDA
SCL
nALERT
GND

3V3
C100 0.1μF
GND

I2C
I2C_SDA
I2C_SCL
nALERT
VOUT

A0
A1
3V3
GND

R106 0.005 0.5W ±1%
R107 10
R108 10
C101 4.7μF

U25 INA381A2
IN+
IN-
VS+
VOUT
CMPIN
CMPREF
nALERT
GND
RESET

VIN
3V3
C102 0.1μF
GND
R109 100k
R110 100k
GND

188

INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

U19_1 VBUS IN+ IN- VS A0 A1 SDA SCL nALERT GND INA226

INA381A2 IN+ IN- VS+ VOUT CMPIN CMPREF nALERT GND RESET U20_1

R86_1 0.005 0.5W ±1%
R87_1 10
R88_1 10
C66_1 4.7µF
R89_1 100K
R90_1 100K
C67_1 0.1µF
C64_1 0.1µF
C65_1 22µF

3V3 GND VIN VOUT nALERT I2C I2C_SDA I2C_SCL

Title: INA381A Overcurrent Protection
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Edmonton AB, Canada
T6G 1H9
Size: Letter Number:* Revision:*
Date: 2023-05-04 Time: 2:56:44 PM Sheet 21 of 51
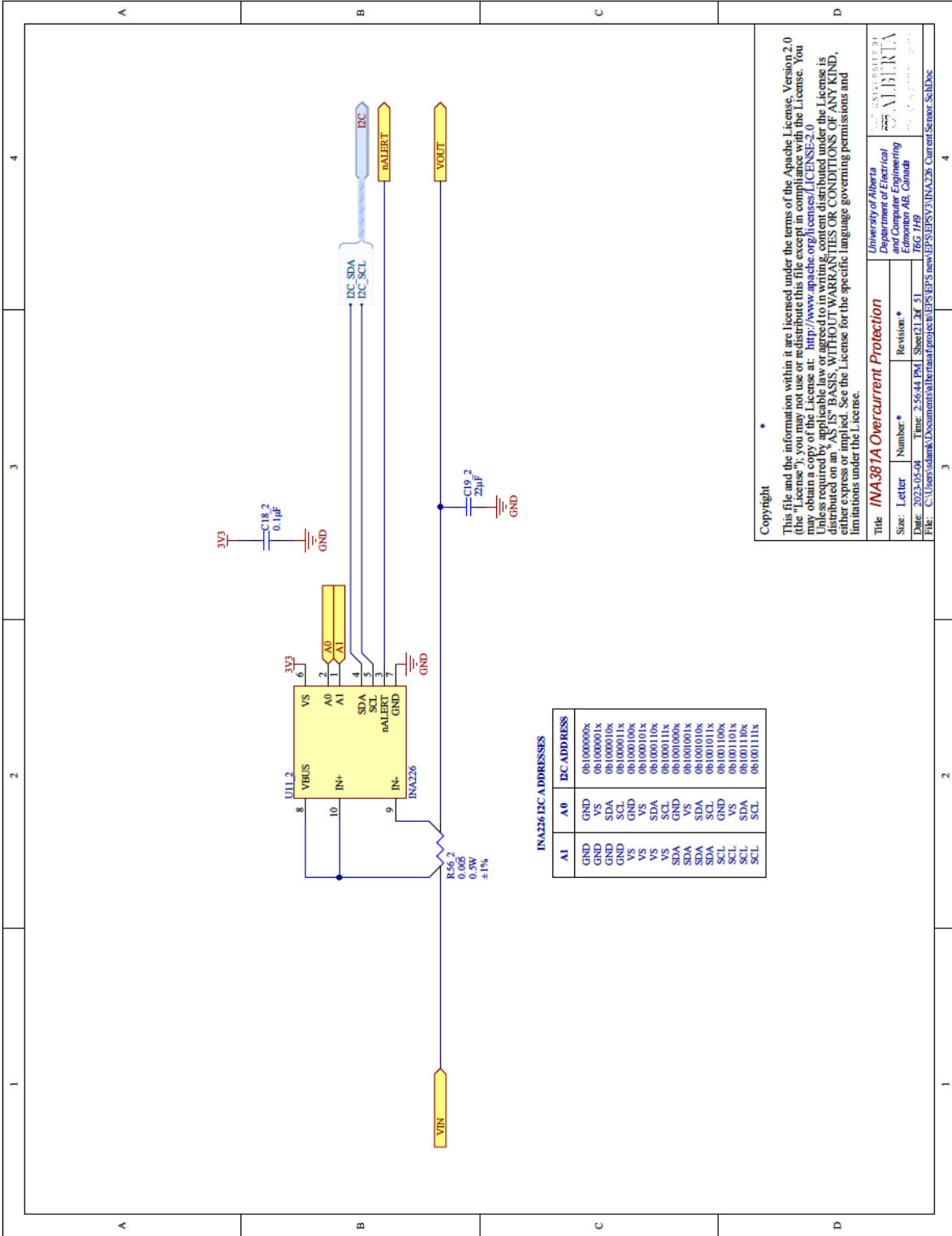File: C:\Users\sdamk\Documents\albertasd\projects\EPS\EPS new\EPS\EPSV3\INA381AOvercurrent Protection.SchDoc
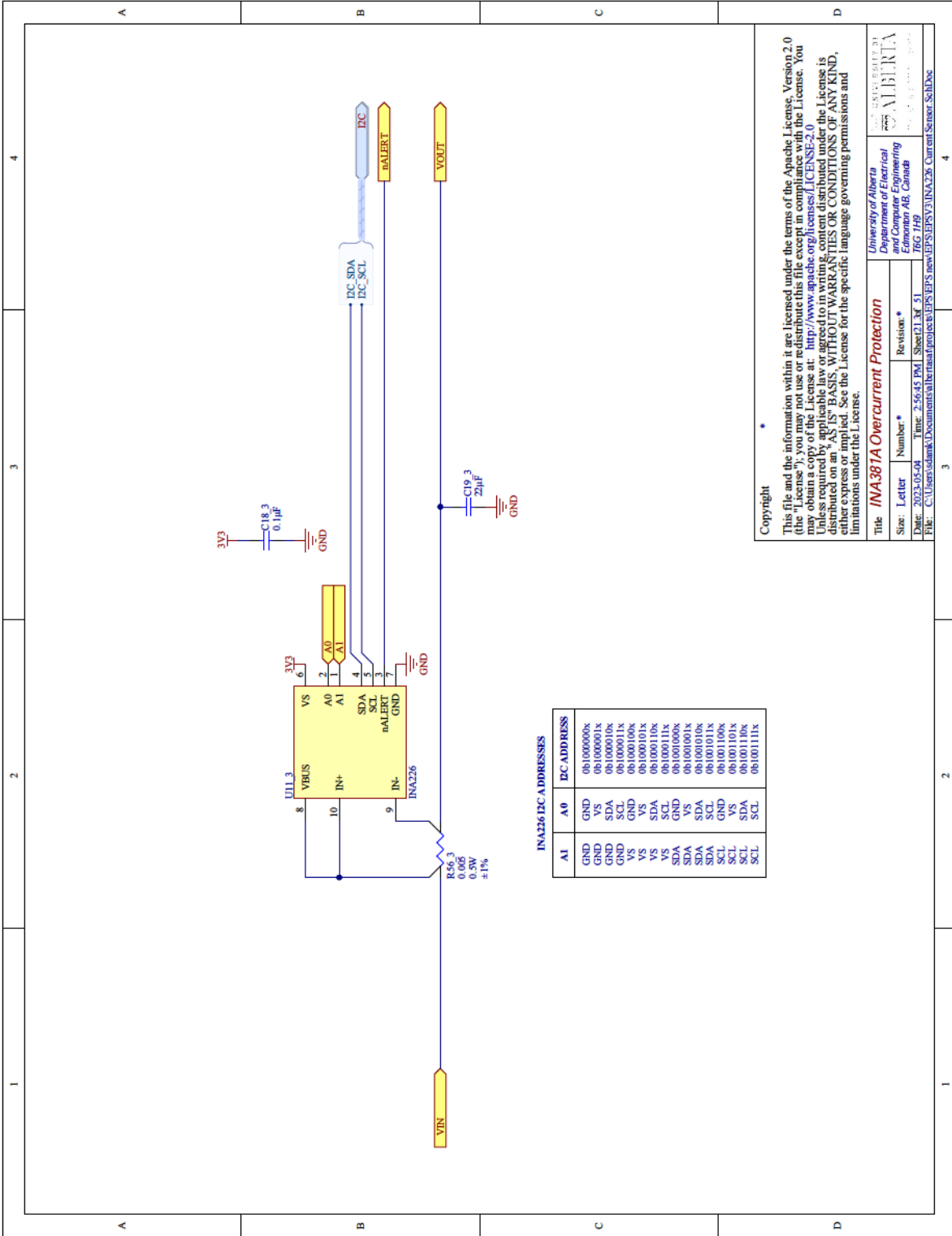
INA381A Overcurrent Protection

U11_1

INA226

VS
A0
A1
SDA
SCL
nALERT
GND
VBUS
IN+
IN-

3V3
A0
A1
GND

I2C
I2C_SDA
I2C_SCL

nALERT
VOUT
VIN

3V3
C18_1
0.1µF
GND

C19_1
22µF
GND

R.56_1
0.005
0.5W
±1%

INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

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Title: INA381A Overcurrent Protection
Size: Letter | Number: * | Revision: *
Date: 2023-05-04 | Time: 2:56:44 PM | Sheet 21 of 51
File: C:\Users\sdamk\Documents\alberta\sd projects\EPS\EPS new\EPS\EPS V3\INA226 Current Sensor.SchDoc

Title   INA381A Overcurrent Protection

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Size: Letter   Number:*   Revision:*
Date: 2023-05-04   Time: 2:56:44 PM   Sheet21 of 51
File: C:\Users\sdamk\Documents\albertas\tf.projects\EPS\EPS\EPS.new\EPS\EPSV3\INA381A Overcurrent Protection.SchDoc

INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

U11_2 — VBUS, IN+, IN−, VS, A0, A1, SDA, SCL, nALERT, GND — INA226

3V3 C18_2 0.1µF GND

3V3 GND

C19_2 22µF GND

R56_2 0.005 0.5W ±1%

I2C I2C_SDA I2C_SCL

nALERT

VOUT

VIN

INA381A Overcurrent Protection

U11_3 — INA226

Pins: VBUS (8), IN+ (10), IN- (9), VS (6, 3V3), A0 (2), A1 (1), SDA (4), SCL (5), nALERT (3), GND (7)

R56_3, 0.005, 0.5W, ±1%

C18_3 0.1µF — 3V3
C19_3 22µF
GND

Ports: VIN, VOUT, nALERT, I2C (I2C_SDA, I2C_SCL)

INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

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Title: INA381A Overcurrent Protection
Size: Letter   Number: *   Revision: *
Date: 2023-05-04   Time: 2:56:45 PM   Sheet 21 of 51
File: C:\Users\adam\Documents\alberta\asd projects\EPS\EPS new\EPS\EPS v3\INA226 Current Sensor.SchDoc

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Title: *Output Channels*

Size: Letter | Number:* | Revision:*

Date: 2023-05-04 | Time: 2:56:45 PM | Sheet22 of 51
File: C:\Users\sdamk\Documents\alberta\asf\projects\EPS\EPS\new\EPS\EPSV3\Output Channels.SchDoc

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Title: INA226 Current Monitor

Size: Letter | Number: * | Revision: *

Date: 2023-05-04 | Time: 2:56:46 PM | Sheet 23 of 51

File: C:\Users\sdamk\Documents\alberta\asf\projects\EPS\EPS new\EPS\PSV3\INA226 Current Monitor.SchDoc

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INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

INA226 Current Monitor schematic

I2C
I2C_SDA
I2C_SCL

VOUT

EN_PU

nALERT

R48_2
1M

C10_2
22µF
GND

U7_2
MIC5019

3V3
A0
A1

3V3
GND

U6_2
VBUS
VS
A0
A1
SDA
SCL
nALERT
GND
IN+
IN-
INA226

R46_2
0.1
±0.5%

3V3
C9_2
0.1µF
GND

3V3
C11_2
4.7µF
GND

GND

Q3_2
TPNIR603

R47_2
10

VIN

INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

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Title: INA226 Current Monitor
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File: C:\Users\sdamk\Documents\alberta\asf\projects\EPS\EPS\new\EPS\EPSV3\INA226 Current Monitor.SchDoc

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Title: INA226 Current Monitor

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File: C:\Users\sdamk\Documents\alberta\sd projects\EPS\EPS new\EPS\EPS V3\INA226 Current Monitor.SchDoc

INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

197

INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

Title: INA226 Current Monitor

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INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

199

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Title: INA226 Current Monitor

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File: C:\Users\adamk\Documents\alberta\asf\projects\EPS\EPS new\EPS\EPS V3\INA226 Current Monitor.SchDoc
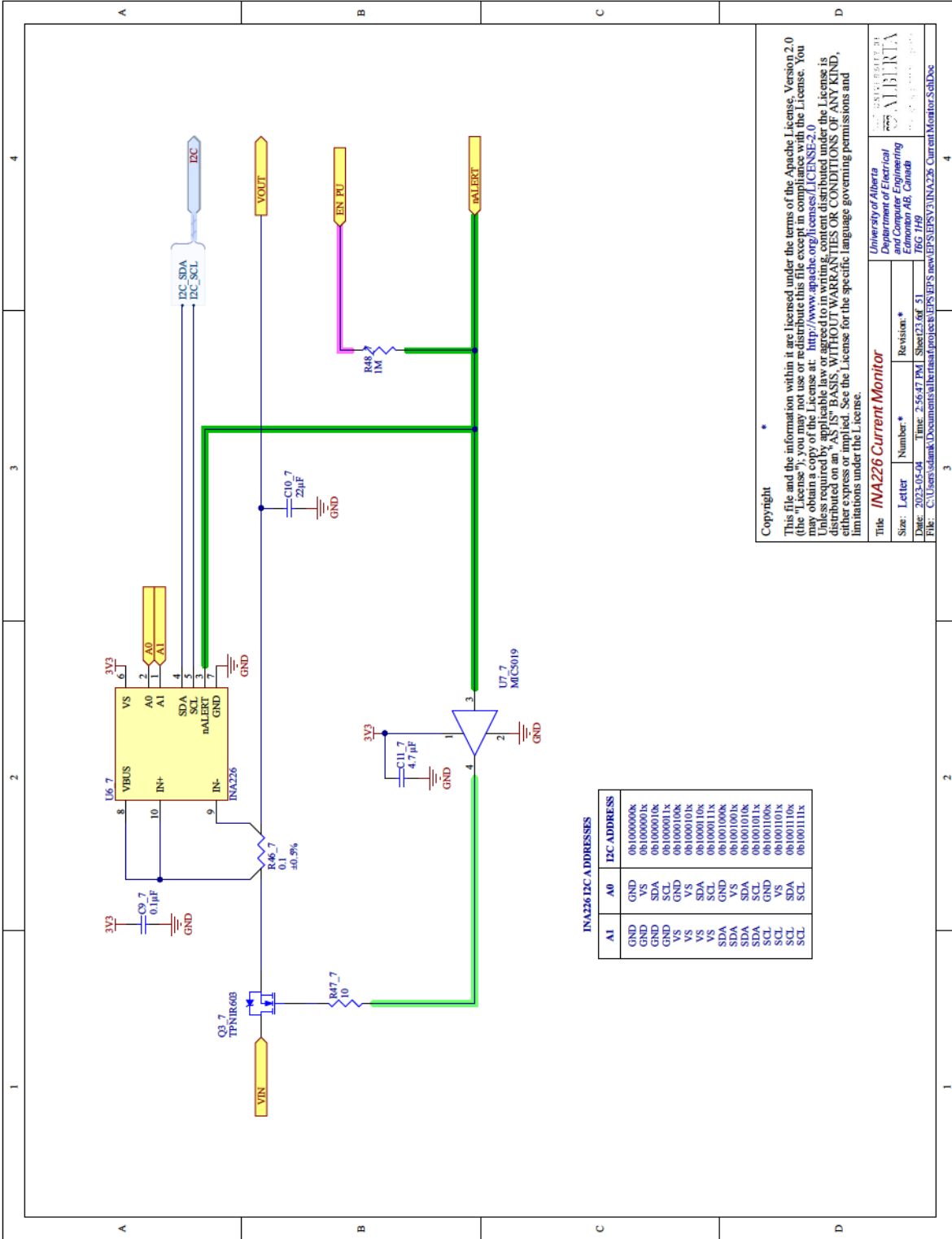
INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

200

INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

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Title: INA226 Current Monitor
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Title: INA226 Current Monitor

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4

I2C

I2C_SDA
I2C_SCL

VOUT

EN_PU

nALERT

R48
1M

C10_8
22µF
GND

3V3
A0
A1

VS
A0
A1
SDA
SCL
nALERT
GND

U6_8
VBUS
IN+
IN-
INA226

GND

U7_8
MIC5019

3

1

2

4

3V3
C11_8
4.7µF
GND

GND

3V3
C9_8
0.1µF
GND

R46_8
0.1
±0.5%

Q3_8
TPN1R603

R47_8
10

VIN

INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

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INA226 Current Monitor

Title: INA226 Current Monitor

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INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

203

INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

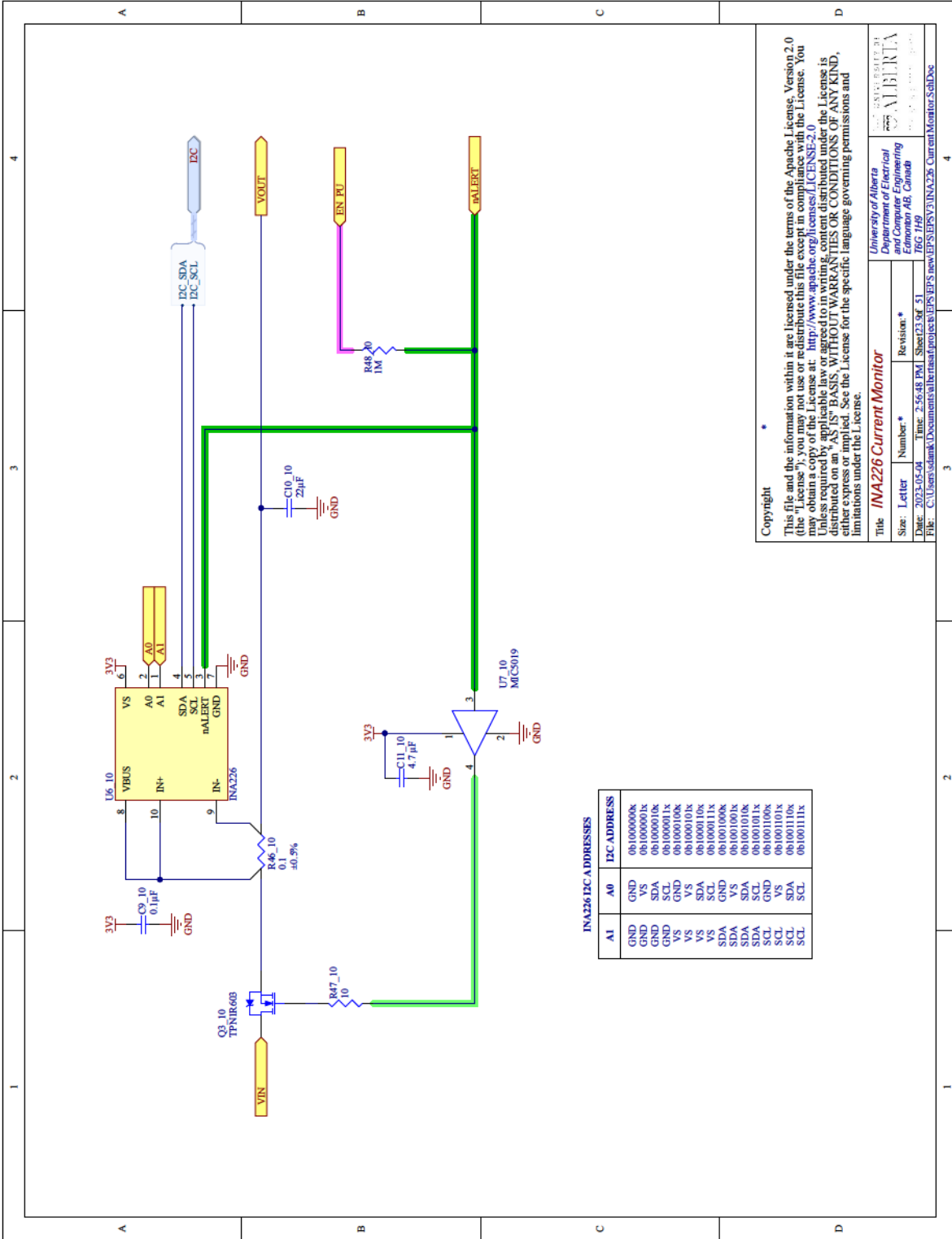Copyright   *

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Title INA226 Current Monitor

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Title: INA226 Current Monitor

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I2C
I2C_SDA
I2C_SCL

VOUT

EN_PU

nALERT

R48_11
1M

C10_11
22µF
GND

U6_11
VBUS
VS
A0
A1
SDA
SCL
nALERT
GND
IN+
IN-
INA226

A0
A1

3V3
GND

R46_11
0.1
±0.5%

C9_11
0.1µF
3V3
GND

Q3_11
TPN1R603

R47_11
10

VIN

U7_11
MIC5019

3V3
C11_11
4.7µF
GND
GND

INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

Title: INA226 Current Monitor

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206

VIN

Q3_13
TPN1R603

R47_13
10

R46_13
0.1
±0.5%

C9_13
0.1μF
3V3
GND

U6_13
VBUS
VS
A0
A1
SDA
SCL
nALERT
GND
IN+
IN-
INA226
8
10
9
3V3
A0
A1
GND

I2C
I2C_SDA
I2C_SCL

VOUT

C10_13
22μF
GND

EN_PU
R48_13
1M

nALERT

U7_13
MIC5019
3V3
C11_13
4.7μF
GND
GND
1
2
3
4

INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

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Title: INA226 Current Monitor
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INA226 Current Monitor

Title   INA226 Current Monitor

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INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

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Title: INA226 Current Monitor
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INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

U6_15
INA226
VBUS
VS
A0
A1
IN+
IN-
SDA
SCL
nALERT
GND

U7_15
MIC5019

R46_15
0.1
±0.5%

R47_15
10

R48_15
1M

C9_15
0.1µF

C10_15
22µF

C11_15
4.7µF

Q3_15
TPN1R603

3V3
GND

VOUT
EN_PU
nALERT
VIN
I2C
I2C_SDA
I2C_SCL
A0
A1

209

INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

Title: INA226 Current Monitor
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Title: INA226 Current Monitor

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INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

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INA226 Current Monitor

Title	INA226 Current Monitor		
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INA226 I2C ADDRESSES

A1	A0	I2C ADDRESS
GND	GND	0b1000000x
GND	VS	0b1000001x
GND	SDA	0b1000010x
GND	SCL	0b1000011x
VS	GND	0b1000100x
VS	VS	0b1000101x
VS	SDA	0b1000110x
VS	SCL	0b1000111x
SDA	GND	0b1001000x
SDA	VS	0b1001001x
SDA	SDA	0b1001010x
SDA	SCL	0b1001011x
SCL	GND	0b1001100x
SCL	VS	0b1001101x
SCL	SDA	0b1001110x
SCL	SCL	0b1001111x

213

TCA9548A

VCC

SDA
SCL

SD0 SC0
SD1 SC1
SD2 SC2
SD3 SC3
SD4 SC4
SD5 SC5
SD6 SC6
SD7 SC7

nRESET
A0
A1
A2

GND
THERMAL PAD

U34

I2C0
I2C1
I2C2
I2C3

I2C_SDA
I2C_SCL

RN16C RN16D 10k
RN16A RN16B 10k
RN15C RN15D 10k
RN15A RN15B 10k

3V3

C105 0.1µF
GND

R111 1M
3V3
nRESET

A0 A1 A2
GND

I2C_SCL
I2C_SDA

I2C_IN

INPUTS			I2C ADDRESS
A2	A1	A0	
GND	GND	GND	0x1110000x
GND	GND	VCC	0x1110001x
GND	VCC	GND	0x1110010x
GND	VCC	VCC	0x1110011x
VCC	GND	GND	0x1110100x
VCC	GND	VCC	0x1110101x
VCC	VCC	GND	0x1110110x
VCC	VCC	VCC	0x1110111x

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Title *

Size: Letter | Number:* | Revision:*
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File: C:\Users\dank\Documents\alberta\asf\projects\EPS\EPS\EPS.new\EPS\EPS.V3\TCA 9548A I2C Multiplexer.SchDoc

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Title *

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TCA9548A

U22

VCC

SDA
SCL

nRESET

A0
A1
A2

GND
THERMAL PAD

SD0 SC0
SD1 SC1
SD2 SC2
SD3 SC3
SD4 SC4
SD5 SC5
SD6 SC6
SD7 SC7

RN11B RN11C RN11D RN12D RN12C RN12B
RN13A RN13B RN13C RN14A RN14C RN14B
10k

PV_3V3

I2C0 I2C1 I2C2 I2C3 I2C4 I2C5 I2C6 I2C7

I2C_SDA
I2C_SCL

I2C_IN

C80 0.1µF
3V3
GND

R101 1M
3V3

nRESET
A0
A1
A2

GND

INPUTS			I2C ADDRESS
A2	A1	A0	
GND	GND	GND	0x1110000x
GND	GND	VCC	0x1110001x
GND	VCC	GND	0x1110010x
GND	VCC	VCC	0x1110011x
VCC	GND	GND	0x1110100x
VCC	GND	VCC	0x1110101x
VCC	VCC	GND	0x1110110x
VCC	VCC	VCC	0x1110111x

215

SENSOR PLACEMENT

⊕ indicates sensor position

BOTTOM SIDE

TMS570 Microcontroller

⑧

TOP SIDE

H1 H2

| ⑦ 5.0V | ⑥ 3.3V | ⑤ 1.2V |

| ① MPPT1 | ② MPPT2 |
| ③ MPPT3 | ④ MPPT4 |

ADD0	I2C ADDRESS
GND	0b1001000x
V+	0b1001001x
SDA	0b1001010x
SCL.	0b1001011x

REGISTER	TYPE	RESET	REGISTER DESCRIPTION
0x00	R	0x8000	Temperature result register
0x01	R/W	0x0220	Configuration register
0x02	R/W	0x6000	Temperature high limit register
0x03	R/W	0x8000	Temperature low limit register
0x04	R/W	0x0000	EEPROM unlock register
0x05	R/W	?	EEPROM1 register
0x06	R/W	?	EEPROM2 register
0x07	R/W	0x0000	Temperature offset register
0x08	R/W	?	EEPROM3 register
0x0F	R	0x0117	Device ID register

Temperature result register
Stores the most recent temperature conversion results in binary two's complement format.
One LSB equals 0.0078125 degC. At reset, the register value (0x8000) represents -256 degC.

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Title   *

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SCL2
SDA2

I2C_SCL
I2C_SDA

I2C2

SCL0
SDA0

I2C_SCL
I2C_SDA

I2C0

U27 TMP117
3V3 — B1 — V+
SDA — A1
SCL — A2
ALRT — C2
ADD0 — C1
GND — B2 — GND

SDA0
SCL0
SCL0

U29 TMP117
3V3 — B1 — V+
SDA — A1
SCL — A2
ALRT — C2
ADD0 — C1
GND — B2 — GND

SDA0
SCL0
3V3

U31 TMP117
3V3 — B1 — V+
SDA — A1
SCL — A2
ALRT — C2
ADD0 — C1
GND — B2 — GND

SDA2
SCL2
SCL2

U33 TMP117
3V3 — B1 — V+
SDA — A1
SCL — A2
ALRT — C2
ADD0 — C1
GND — B2 — GND

SDA2
SCL2
3V3

C104 0.1µF
GND

U26 TMP117
3V3 — B1 — V+
SDA — A1
SCL — A2
ALRT — C2
ADD0 — C1
GND — B2 — GND

SDA0
SCL0
SDA0
GND

U28 TMP117
3V3 — B1 — V+
SDA — A1
SCL — A2
ALRT — C2
ADD0 — C1
GND — B2 — GND

SDA0
SCL0
SDA0

U30 TMP117
3V3 — B1 — V+
SDA — A1
SCL — A2
ALRT — C2
ADD0 — C1
GND — B2 — GND

SDA2
SCL2
SDA2
GND

U32 TMP117
3V3 — B1 — V+
SDA — A1
SCL — A2
ALRT — C2
ADD0 — C1
GND — B2 — GND

SDA2
SCL2
SDA2

C103 0.1µF
GND

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VIN

VOUT

PGOOD

C45 0.1µF   C46 22µF   C47 22µF   C48 4.7µF
GND   GND   GND   GND

C51 1µF
GND

TPS53319

12	VIN
13	VIN
14	VIN
15	VIN
16	VIN
17	VIN
19	VDD
2	EN

6	LL
7	LL
8	LL
9	LL
10	LL
11	LL

4	VBST
1	VFB
5	ROVP
20	MODE
21	TRIP
22	RF

18	VREG
3	PGOOD
23	GND

U17

L2 1.5 µH
MPXV1D8401LIR5

R68 3.0k
C44 0.1µF
C50 1000pF
C49 0.1µF
R69 3.01

C40 3300 pF   C41 22µF   C42 22µF   C43 22µF
GND   GND   GND   GND

R70 453k
R71 453k

R76 100k   R75 100k   R74 100k   R73 105k   R72 0
GND   GND   GND   GND   GND

GND

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TPS53319   U18

VIN 12
VIN 13
VIN 14
VIN 15
VIN 16
VIN 17
VDD 19
EN 2

LL 6
LL 7
LL 8
LL 9
LL 10
LL 11

VBST 4
VFB 1
ROVP 5
MODE 20
TRIP 21
RF 22

VREG 18
PGOOD 3
GND 23

VOUT

C55 22µF
C54 22µF
C53 22µF
C52 3300pF

R79 732k
R80 732k

R85 100k
R84 100k
R83 100k
R82 124k
R81 0

L3 1.5µH MPXV1D0840LIR5
R77 3.01k
C56 0.1µF
C62 1000pF
C61 0.1µF
R78 3.01

VIN
C57 0.1µF
C58 22µF
C59 22µF
C60 4.7µF
C63 1µF

PGOOD

GND

E. openEPS Bill of Materials

As of January 28, 2024, the total bill of materials cost from Digikey is less than $915.50 CAD to populate a single board. This cost improves with higher volumes such as 5 or 100 units. The 6-layer PCB with up to 2 ounce copper and gold plating was $115 CAD each in quantities of 5.

Designator	Manufacturer Part Number	Manufacturer Name	Quantity	Extended Price for 1 board	Extended Price for 5 boards	Extended Price for 100 boards
C1, C2, C3, C6, C8, C9_1, C9_2, C9_3, C9_4, C9_5, C9_6, C9_7, C9_8, C9_9, C9_10, C9_11, C9_12, C9_13, C9_14, C9_15, C9_16, C9_17, C9_18, C9_19, C12_1, C12_2, C12_3, C12_4, C13_1, C13_2, C13_3, C13_4, C14, C18_1, C18_2, C18_3, C20, C21, C22, C23, C64_1, C64_2, C67_1, C67_2, C80, C81, C82, C83, C84, C85, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C100, C102, C103, C104, C105	CGA2B3X7R1H104K050BB	TDK Corporation	66	$ 5.58	$ 22.010	228.95
C4, C7, C11_1, C11_2, C11_3, C11_4, C11_5, C11_6, C11_7, C11_8, C11_9, C11_10, C11_11, C11_12, C11_13, C11_14, C11_15, C11_16, C11_17, C11_18, C11_19, C17, C31, C39, C43, C51, C55, C63, C66_1, C66_2, C78_1, C78_2, C78_3, C78_4, C86, C98, C101	GRM188Z71C475KE21D	Murata Electronics	37	$ 9.10	$ 25.840	336.26
C5	CGA2B2X8R1H472K050BA	TDK Corporation	1	$ 0.24	$ 1.200	7.88
C10_1, C10_2, C10_3, C10_4, C10_5, C10_6, C10_7, C10_8, C10_9, C10_10, C10_11, C10_12, C10_13, C10_14, C10_15, C10_16, C10_17, C10_18, C10_19, C24, C25, C26, C27, C65_1, C65_2	EMK316BB7226ML-T	Taiyo Yuden	25	$ 17.90	$ 58.820	588.28
C15, C68_1, C68_2, C68_3, C68_4, C69_1, C69_2, C69_3, C69_4	CGA3E3X7R1H224K080AB	TDK Corporation	9	$ 2.34	$ 7.520	54.58
C16, C71_1, C71_2, C71_3, C71_4, C72_1, C72_2, C72_3, C72_4, C73_1, C73_2, C73_3, C73_4	UMK107AB7105KA-T	Taiyo Yuden	13	$ 3.07	$ 9.680	98.93
C19_1, C19_2, C19_3, C29, C30, C33, C34, C35, C41, C42, C45, C46, C47, C53, C54, C57, C58, C59, C70_1, C70_2, C70_3, C70_4, C74_1, C74_2, C74_3, C74_4, C75_1, C75_2, C75_3, C75_4, C76_1, C76_2, C76_3, C76_4	C3225X7R1E226M250AB	TDK Corporation	34	$ 51.17	$ 191.220	2218.02
C28, C36, C37, C40, C48, C49, C52, C60, C61	TWK107B7104MVHT	Taiyo Yuden	9	$ 3.96	$ 13.320	126.13
C32, C44, C56	C0402C332K5RAC7867	KEMET	3	$ 0.42	$ 0.800	7.02
C38, C50, C62	CGA2B1C0G2A102J050BC	TDK Corporation	3	$ 1.08	$ 3.440	34.86
C77_1, C77_2, C77_3, C77_4	CGA2B1C0G2A681J050BC	TDK Corporation	4	$ 1.08	$ 3.560	35.88
C79_1, C79_2, C79_3, C79_4	CGA2B2NP01H4R7C050BA	TDK Corporation	4	$ 0.56	$ 1.940	$ 18.28
C99	CGA2B3X8R1H103K050BB	TDK Corporation	1	$ 0.27	$ 1.350	$ 8.49
D1, D2	BAS116LPH4-7B	Diodes Incorporated	2	$ 1.06	$ 3.590	$ 35.06
D3	150060GS75000	Würth Elektronik	1	$ 0.23	$ 1.150	$ 18.52
H1, H2	SSW-126-23-G-D	Samtec Inc.	2	$ 37.22	$ 186.100	$ 3,722.00
L1, L2, L3	MPXV1D0840L1R5	KEMET	3	$ 6.24	$ 26.320	$ 344.50
L4_1, L4_2, L4_3, L4_4	MPXV1D1264L1R5	KEMET	4	$ 14.60	$ 62.040	$ 376.31

P1, P2, P3, P4, P5, P6, P7, P8	G125-MH11005L1P	Harwin Inc.	8	$	115.44	$	519.440	$	7,778.66
P9	G125-MH10605L1P	Harwin Inc.	1	$	12.86	$	64.300	$	1,034.39
P10	G125-MH12005L1P	Harwin Inc.	1	$	18.26	$	91.300	$	1,410.99
P11, P13	TW-02-07-T-S-500-080	Samtec Inc.	2	$	1.36	$	6.800	$	136.00
Q1, Q2	EM6K34T2CR	Rohm Semiconductor	2	$	1.08	$	3.800	$	38.36
Q3_1, Q3_2, Q3_3, Q3_4, Q3_5, Q3_6, Q3_7, Q3_8, Q3_9, Q3_10, Q3_11, Q3_12, Q3_13, Q3_14, Q3_15, Q3_16, Q3_17, Q3_18, Q3_19, Q4, Q5	TPN1R603PL,L1Q	Toshiba	21	$	20.87	$	81.200	$	1,055.59
R1, R2, R3, R4, R45, R48_1, R48_2, R48_3, R48_4, R48_5, R48_6, R48_7, R48_8, R48_9, R48_10, R48_11, R48_12, R48_13, R48_14, R48_15, R48_16, R48_17, R48_18, R48_19, R52, R55, R101, R105, R111	ERJ-2RKF1004X	Panasonic	29	$	1.04	$	2.800	$	32.86
R41, R42	ERA-2AEB60R4X	Panasonic	2	$	0.52	$	1.870	$	26.30
R44, R47_1, R47_2, R47_3, R47_4, R47_5, R47_6, R47_7, R47_8, R47_9, R47_10, R47_11, R47_12, R47_13, R47_14, R47_15, R47_16, R47_17, R47_18, R47_19, R87_1, R87_2, R88_1, R88_2, R107, R108	ERA-2AKD100X	Panasonic	26	$	2.99	$	10.750	$	146.15
R46_1, R46_2, R46_3, R46_4, R46_5, R46_6, R46_7, R46_8, R46_9, R46_10, R46_11, R46_12, R46_13, R46_14, R46_15, R46_16, R46_17, R46_18, R46_19	WSL0805R1000DEA18	Vishay Dale	19	$	42.20	$	186.560	$	1,908.70
R49_1, R49_2, R49_3, R49_4, R50_1, R50_2, R50_3, R50_4, R51_1, R51_2, R51_3, R51_4, R56_1, R56_2, R56_3, R86_1, R86_2, R106	CRF0805-FZ-R005ELF	Bourns Inc.	18	$	10.01	$	29.740	$	244.04
R53	ERJ-2RKF3833X	Panasonic	1	$	0.15	$	0.750	$	1.93
R54, R63, R72, R81	ERJ-2GE0R00X	Panasonic	4	$	0.60	$	0.720	$	4.78
R57	ERJ-2RKF22R0X	Panasonic	1	$	0.15	$	0.750	$	1.93
R58	ERJ-2RKF49R9X	Panasonic	1	$	0.15	$	0.750	$	1.93
R59, R68, R77	CRCW02013K01FKED	Vishay Dale	3	$	0.99	$	2.620	$	30.84
R60, R69, R78	CRCW02013R01FXED	Vishay Dale	3	$	0.63	$	1.660	$	18.90
R61, R62, R65, R66, R67, R74, R75, R76, R83, R84, R85, R89_1, R89_2, R90_1, R90_2, R109, R110	ERJ-2RKF1003X	Panasonic	17	$	0.61	$	1.960	$	19.26
R64	ERJ-2RKF1103X	Panasonic	1	$	0.15	$	0.750	$	1.93
R70, R71	ERJ-2RKF4533X	Panasonic	2	$	0.30	$	0.360	$	3.86
R73	ERJ-2RKF1053X	Panasonic	1	$	0.15	$	0.750	$	1.93
R79, R80	ERJ-2RKF7323X	Panasonic	2	$	0.30	$	0.360	$	3.86
R82	ERJ-2RKF1243X	Panasonic	1	$	0.15	$	0.750	$	1.93
R91_1, R91_2, R91_3, R91_4	MCS0402MD4703BE000	Vishay Dale	4	$	2.00	$	7.320	$	100.80
R92_1, R92_2, R92_3, R92_4	RP73PF1E158KBTD	TE Connectivity	4	$	1.88	$	6.900	$	95.96
R93_1, R93_2, R93_3, R93_4	RP73PF1E178KBTD	TE Connectivity	4	$	1.72	$	6.280	$	87.68
R94_1, R94_2, R94_3, R94_4	RP73PF1E20KBTD	TE Connectivity	4	$	1.72	$	6.340	$	88.48
R95_1, R95_2, R95_3, R95_4	RP73PF1E28KBTD	TE Connectivity	4	$	1.72	$	6.320	$	88.00
R96_1, R96_2, R96_3, R96_4	RP73PF1E1K27BTD	TE Connectivity	4	$	1.76	$	6.580	$	91.88
R97_1, R97_2, R97_3, R97_4	RP73PF1E95K3BTD	TE Connectivity	4	$	1.72	$	6.320	$	88.00
R98_1, R98_2, R98_3, R98_4	RP73PF1E127KBTD	TE Connectivity	4	$	1.88	$	6.860	$	95.60
R99_1, R99_2, R99_3, R99_4	RP73PF1E200KBTD	TE Connectivity	4	$	1.72	$	6.280	$	87.68
R100_1, R100_2, R100_3, R100_4	RP73PF1E40K2BTD	TE Connectivity	4	$	1.72	$	6.280	$	87.68
R102, R103, R104	ERJ-2RKF1002X	Panasonic	3	$	0.45	$	0.540	$	5.79
RN1, RN2, RN3, RN4, RN5, RN6	EXB-24VR000X	Panasonic	6	$	1.08	$	3.300	$	22.68

RN7, RN8, RN9	EXB-28VR000X	Panasonic	3	$	0.45	$	1.800	$	11.35
RN10, RN11, RN12, RN13, RN14, RN15, RN16	EXB-28V103JX	Panasonic	7	$	1.05	$	3.070	$	21.04
U1	TMS5701224CPGEQQ1	Texas Instruments	1	$	33.99	$	169.950	$	2,993.97
U2	REF35160QDBVR	Texas Instruments	1	$	3.16	$	15.800	$	227.98
U3	TCAN330DCNR	Texas Instruments	1	$	4.43	$	22.150	$	320.10
U4, U7_1, U7_2, U7_3, U7_4, U7_5, U7_6, U7_7, U7_8, U7_9, U7_10, U7_11, U7_12, U7_13, U7_14, U7_15, U7_16, U7_17, U7_18, U7_19, U10	MIC5019YFT-TR	Microchip Technology	21	$	32.13	$	127.530	$	2,550.66
U5	AD5324BRMZ	Analog Devices Inc.	1	$	32.08	$	160.400	$	2,489.52
U6_1, U6_2, U6_3, U6_4, U6_5, U6_6, U6_7, U6_8, U6_9, U6_10, U6_11, U6_12, U6_13, U6_14, U6_15, U6_16, U6_17, U6_18, U6_19, U11_1, U11_2, U11_3, U19_1, U19_2, U24	INA226AQDGSRQ1	Texas Instruments	25	$	122.31		529.99	$	7,229.63
U8_1, U8_2, U8_3, U8_4	INA3221AQRGVRQ1	Texas Instruments	4	$	30.24		135.7	$	2,109.52
U9	MAX16998AAUA/V+	Maxim Integrated	1	$	4.75		23.75	$	349.85
U12, U13, U14	SN74LVC2G17MDCKREP	Texas Instruments	3	$	10.71		48.15	$	726.85
U15	RV-3032-C7-32.768KHZ-2.5PPM-TA-QA	Micro Crystal AG	1	$	6.80		34	$	500.27
U16, U17, U18	TPS53319DQPT	Texas Instruments	3	$	35.49		160.24	$	2,111.56
U20_1, U20_2, U25	INA381A2IDSGT	Texas Instruments	3	$	5.37		23.96	$	290.95
U21_1, U21_2, U21_3, U21_4	LTC3119IUFD#PBF	Analog Devices Inc.	4	$	113.88		523.26	$	8,404.53
U22, U34	TCA9548ARGERQ1	Texas Instruments	2	$	6.96		31.22	$	501.70
U23	SG-210STF 24.0000MY0	EPSON	1	$	1.96		9.8	$	142.76
U32, U33	TMP117NAIYBGR	Texas Instruments	8	$	63.28		211.01	$	3,270.54
			COST PER BOARD:	$	915.50	$	786.35	$	573.58

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