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As long as Predators are fighting Aliens
I’m happy.
-Kaston Leung

University of Alberta

MIXED SIGNAL DESIGN OF A HIGH VOLTAGE (HV) CMOS INTEGRATED CIRCUIT FOR MICROFLUIDIC APPLICATIONS

by

Maziyar Khorasani

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of **Master of Science**.

Department of Electrical and Computer Engineering

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Spring 2007

University of Alberta

Faculty of Graduate Studies and Research

The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research for acceptance, a thesis entitled **Mixed Signal Design of a High Voltage (HV) CMOS Integrated Circuit for Microfluidic Applications** submitted by Maziyar Khorasani in partial fulfillment of the requirements for the degree of **Master of Science**.

Dr. Duncan Elliott, Dr. Chris Backhouse
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Dr. Mike MacGregor
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To Foo and Baz
and also my dog Rover

Abstract

Current BioMems, “lab-on-a-chip” (LOC), and microfluidic-based analysis systems suffer from large external power supplies, relays and optics. This reliance on external bulk infrastructures prevents the development of hand-held point-of-care medical devices and miniaturized genetic testing platforms. In this work, we have developed several generations of high-voltage CMOS integrated circuits to replace these external components, offering for the first time, the possibility to reduce size and cost of LOCs and significantly improve integration. The ICs developed accomplish this by generating high-voltage, integrating optical detection circuitry (for sensitive laser induced fluorescence detection) and implementing low-voltage digital control logic and a communication interface, all for the first time on-chip and on the same substrate. Specifically, the high-voltage is generated using an inductive DC-DC boost converter, optical detection is accomplished using photodiodes and associated amplification circuitry, and a successive approximation (SAR) ADC and a serial peripheral interface are responsible for analog-to-digital conversion and communication of control information to and from an off-chip device. We demonstrate successful high-voltage generation up to 150V and current source capability of 60uA (sufficient for millimeter to centimeter microfluidic channel lengths), picowatt optical detector sensitivity, and operation of the integrated ADC. Throughout, we also propose additional methods of optical detection, such as using avalanche photodiodes and phototransistors, and alternative circuit configurations for low-power high-voltage level-shifters - all essential components for future microfluidic controller integrated circuit systems.

Table of Contents

List of Figures

List of Tables

Chapter 1

Introduction

Recent advances in semiconductor and mixed signal integrated circuit (IC) technology has paved the way for the development of standalone life science diagnostic platforms in the form of lab-on-a-chip (LOC), BioMEMS or microfluidic-based total analysis systems (μTAS). These devices offer the advantages of higher speeds, throughput, and portability, while enabling immediate on site analysis at a reduced reagent cost [17–20]. The potential of such systems is rapidly attracting not only academics, but also private commercial ventures. Forecasts ranging from $1 billion to $19 billion [21] have resulted in the formation of numerous companies including Aclara BioSciences, Affymetrix, Caliper, and Orchid BioComputers. Apart from the slew of start-up companies, an abundant number of established chip and instrument makers including 3M, IBM, Intel, Motorola, and PerkinElmer have quickly followed.

Currently though, the majority of LOC systems in development are "microscale devices, coupled to macroscale [and external] infrastructures" [17]. Even as efforts have been made to produce portable systems, many of the devices still rely on conventional and bulky external power supplies and optical detection instruments.

In addition to the benefits of:

- macro- and micro-component integration for increased portability,
- the availability of digital information for increased knowledge transfer and tracking,

- integrated sample preparation and detection for point-of-care,
- direct measurement of a small volume of reactants for increased cost and time savings,
- and quick assay developments,

this research has many potential applications. These applications range from screening and biological assays to genomics and diagnostics. Specifically, testing on fast, sensitive, and automated microfluidic devices can not only facilitate vaccination monitoring efficiency and disease-related genetic abnormality detection, but can also aid in the prevention of health issues such as Adverse Drug Reactions (ADR), the fifth leading cause of death in hospitals in the United States. Current methods of genetic detection for inadvisable prescriptions are too costly to be performed on a per patient basis [22], however, research with microfluidics at the University of Alberta has demonstrated a less expensive and feasible alternative. The human genome project is another great example of the benefits of this work. While the project was initially planned to span over seven years and cost nearly $3 Billion dollars, using DNA sequencers implemented with miniaturized LOC technology, the same feat was accomplished at a tenth of the cost, and in only three years [21].

Though the individual components required for a complete LOC, such as HV CMOS power supplies or CMOS based fluorescence detectors, exist, never before in published works have all of the components been integrated into a complete system, let along for microfluidic applications. Additionally, integrating low-voltage components along side high-voltage components in a mixed LV/HV CMOS process presents significant challenges. In a mature process, accurate modeling and a reliable component set provides a strong foundation for successful design. However, considering the process we are currently using is still young by general standards, the challenges are compounded.

1.1 Thesis Overview

This thesis deals with the design and integration of the individual components required for a complete LOC system with the focus centering on the microelectronics. Once the individual components have been laid out, four (ICKAALOC, ICKAALC2, ICKAALC3 and ICKAALC4) microfluidic integrated circuits, each building on the previous version, will be presented. All four ICs have been fabricated. Along with design, implementation details, and simulation results, testing and verification data will also be presented.

Chapter 2 provides background information on the different types of and the requirements for microfluidic capillary electrophoresis (CE) based systems. In Chapter 3, existing works are reviewed to illustrate not only the accelerated pace at which research is being pursued on such integrated systems, but also to further highlight the novelty of the presented works. Following these, in Chapter 4 through 7, the five critical components that make up the designed ICs are examined. In each chapter, specific requirements, design methodology, and simulation/measured results are presented. The specific components discussed include the optical detection systems (photodiodes and associated amplification circuitry), analog-to-Digital converters, level-Shifters, high voltage generation (through the DC-DC inductive boost converter) and lastly the communication and control interface. Finally in Chapter 8, after a brief description, the four different systems are presented in a back-to-back comparative manner. This thesis ends with Chapter 9 which discusses future works and the closing remarks.

Chapter 2

Background

2.1 Microfluidics

2.1.1 Origin of Microfluidics

Microfluidics is a highly multi-disciplinary field (involving physics, chemistry, engineering, and biotechnology) of science and technology systems that process or manipulate microliter or nanoliter amounts of fluids using channels with micrometer dimensions. Microfluidics is highly applicable to the life sciences, and more specifically to medical diagnostics. Microfluidic systems offer high resolution and sensitive analysis, require small quantities of samples and reagents, and are amenable to portable use.

The field of microfluidics has developed from four key areas [23]:

1. Molecular analysis and microanalytical methods such as Capillary Electrophoresis (CE) coupled with advances in methods of optical (e.g. fluorescence) detection.

2. Biodefense applications and military sources of funding like the Defense Advanced Research Projects Agency (DARPA) of the US Department of Defense. Investments in such initiatives to bring portable microchip and microfluidic based chemical and biological threat detectors into reality has been a driving force behind the interest in such devices in academic research.

3. Molecular diagnostics, like post sequencing of the human genome, and the great benefits associated with knowing specific mutations and genetic pre-dispositions, has triggered the development of inexpensive and portable genetic analysis systems.

4. Microelectronics and microelectromechanical systems (MEMS), where parallels were seen in how the high-throughput fabrication and photolithography technology could be ported to development microfluidic systems.

2.1.2 The Electrokinetic Phenomena

Microfluidic flows can be manipulated by variety of external forces such as electric, magnetic, pressure and capillary forces [24]. However, the most common method for inducing movement either of charged analytes in fluids or the bulk fluid itself in microchip channels is by electrokinetic transport. This process involves two phenomena:

1. Electroosmotic flow (EOF): the bulk movement of a fluid past a solid interface (e.g capillary) due to the formation of an electric double layer (EDL) [25] at the surface under the application of an electric field.

2. Electrophoretic migration: the movement of charged particles in a solution due to the application of an electric field.

For the microfluidic systems discussed in the scope of this thesis, the effects of EOF (i.e. reagent-wall interactions) are minimized, allowing only the use of electrophoretic migration. The two most common methods to reduce EOF are:

1. Permanent coatings of the microchannel surface with a covalently bonded polymer layer.

2. Dynamic coatings by adsorption of a hydrophilic (water-liking) polymer coating to the microchannel wall.

For completeness, EOF has been mentioned, however, since the focus of this thesis is electrophoresis, further detail on EOF is not relevant. With EOF minimized, electrophoresis becomes the dominant method of charged analyte transport.

2.2 Capillary Electrophoresis

To be able to put into perspective the advantages offered by electrophoresis with microfluidics and to examine the origin of microfluidics, it is beneficial to review a commonly used and standard method of separation, capillary electrophoresis (CE).

First highlighted by the work of Jorgenson and Lukacs [26] in the 1980s, CE quickly became a dominant tool in DNA separation, clinical, biomedical and forensic applications, and the analysis of pharmaceuticals. CE describes a family of separation techniques which involve the application of high electric fields across buffer-filled capillaries to achieve separation of a specific sample.

In mainstream and conventional commercial systems, CE involves a capillary about 20-100 cm long and 10-100 μm wide. There are two basic types of CE, one in which the capillary is filled with a solution that does not contain a gel, and the other, a CE in which the capillary is filled with a gel (i.e. a sieving matrix). The two methods are used to achieve different kinds of separation. The first method separates molecules based their different charge-to-mass ratios using EOF (and electrophoresis). The second method, by ensuring molecules have identical (or near identical) charge-to-mass ratios and by using a sieving matrix (i.e. an entanglement of polymers), separates by size. The size-based separation occurs because the larger molecules need to navigate through the "fish-net-like" entanglement, and thus their migration rates are retarded.

Depending on the CE method chosen, both ends of the capillary are then placed in reservoirs (or wells) also filled with the same solution (a.k.a buffer), but in one well, the sample to be analyzed is also added. Application of a high voltage (5-30kV) across the wells causes the analyte (e.g. proteins, DNA) to migrate towards an appropriate electrode (e.g. through electrophoresis). A detector intersects the capillary at its opposite end, and is used to plot the response of the detector (e.g.

the measured fluorescence) with respect to time as samples pass by, thereby generating an electropherogram. A CE system along with a sample electropherogram is illustrated in Fig. 2.1 and Fig. 2.2 respectively.

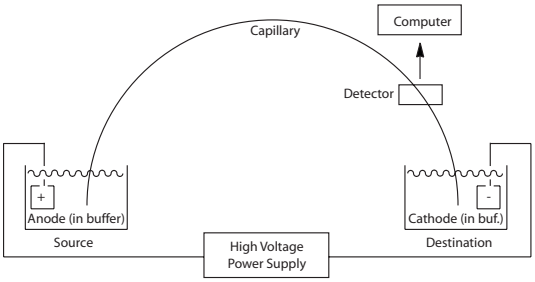

Figure 2.1: A generic CE setup

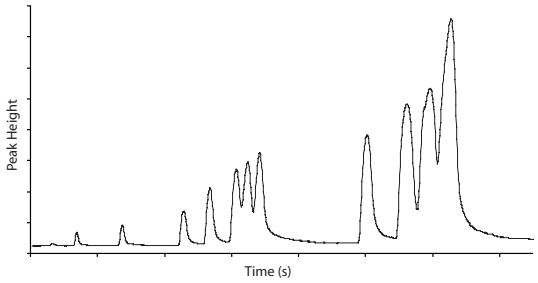

Figure 2.2: A sample electropherogram

The most widely used method of detection in CE is fluorescence. This technique is used for samples that naturally fluoresce or can be chemically modified to be "taggable" with a fluorescent molecule called a fluorophore. In fluorescence detection, a light source (often a laser) of a particular wavelength is focused on the capillary containing flowing fluorescently tagged samples. The light source excites the fluorophore, which then emits a different (usually higher) wavelength. The excitation light (e.g. laser) is filtered and the emission spectrum (from the fluorophore) is collected and plotted with respect to time. Fig. 2.3 illustrates the excitation and emission spectrum of the ROX fluorophore. In this image, the fluorophore is excited with a green laser and the excitation source is filtered with the pigment filter (PSC).

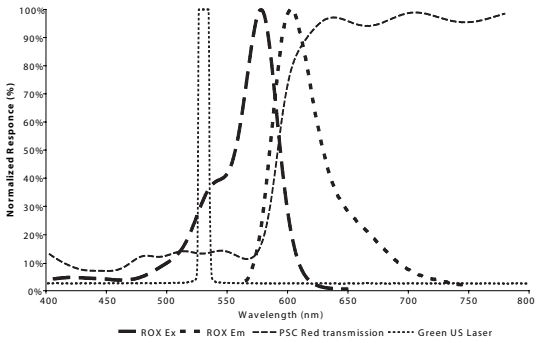

Figure 2.3: ROX fluorophore, and PSC Red paint spectra

2.3 Microfluidic Electrophoresis

It has been shown that no loss of electrophoretic performance occurs in microfluidic channel-based devices compared with those that are capillary-based [27]. From this, electrophoresis using microfluidics can be comparably discussed with respect to standard methods.

A standard design of a microchip capable of injection and separation contains two intersecting channels (illustrated in Fig. 2.4) [28]. The short (a.k.a injection) channel acts to electrophoretically load the sample by applying a negative and positive potential to the sample and sample waste wells respectively. Once a portion of the sample has migrated along the injection channel, by applying a negative and positive potential to the buffer and buffer waste wells respectively (while floating the injection wells), an plug of charged particles with a precisely defined volume is electrophoretically migrated along the longer (a.k.a separation) channel, and separating out along this channel based on the size of the DNA.

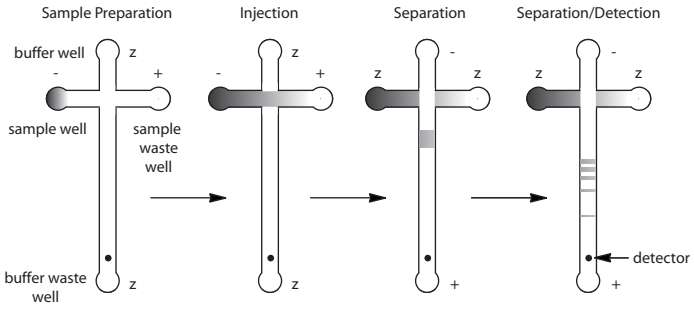

Figure 2.4: Microfluidic channels illustrating sample preparation, injection, separation and detection

Similar to the generic CE setup (Fig. 2.1), a detector is placed near the end of the separation channel and is used to measure the intensity of light emitted by the excited fluorophores. Based on Equ. 2.1 (i.e. for commonly encountered situations):

$$x = \upsilon t \tag{2.1}$$

$$\upsilon = \mu \mathrm{E} \tag{2.2}$$

where x is the distance traveled, υ is the average velocity, and t is the time, the detec-

tor is placed as far away from the intersection channel as possible, maximizing the distance and hence the separation time. However, as can be seen from Equ. 2.1 and 2.2, where μ is the electrophoretic mobility and E is the electric field, the separation time can be decreased by increasing the electric field.

Macro CE separations are normally performed using voltages, and corresponding currents, in the range of 5 – 30 kV and 10 – 100 μA respectively. Higher currents may lead to unstable and irreproducible operating conditions through:

1. Joule heating which can cause changes to the polymer pore sizes resulting in a non-linear separation characteristic.

2. Reduced resolution through heating and convection flow.

Because microfluidic systems have shorter channel lengths, lower voltages can be used while maintaining the same electric fields. For such systems, currents higher than 100 μA have not been reported in literature. In regards to the voltage, if the potential is too high, the DNA becomes completely uncoiled, and regardless of size, orients itself parallel to the field and migrates at the same velocity (a.k.a strongly biased reptation) [29, 30], making mobility based separation infeasible.

Voltage selection is determined during method development in which several factors and variables are considered:

- Resolution and migration velocity are a function of the electric field and the polymers retarding capability. For example, lower electric fields may provide higher resolution but at the cost of much slower speeds (and vice versa). A polymer with smaller pores may result in enhanced resolution in separation but slower speeds (and vice versa).

- The sample and its delta velocity (i.e. difference in rates of travel between varying fragment length samples). Must ensure electric field is a value that allows for maximum resolution.

- Currents should not exceed 100 μA.

Similar to the macro CE setup, the detection mechanism most commonly used is laser-induced fluorescence (LIF) spectroscopy - which will be discussed in more depth in the following section.

Chapter 3

Prior Work

This chapters presents an overview of the recent advancements in microfluidic integration. Specifically, the individual components required in such systems, along with existing systems as a whole are examined.

Complete LOCs require the integration of several different components. These components include reservoirs and fluidic interconnects for sample separation and collection, high voltage generation and distribution networks to power the often demanding bio-analysis tools, detection mechanisms ranging from optical (photodetectors) to chemical detectors, and some form of control/readout and data acquisition circuitry. In the following, the key individual components are examined first, followed by an examination of more complete and integrated systems.

3.1 Components for a Complete LOC System

3.1.1 Fluidic Channels

There are a variety of strategies to fabricate enclosed channels [31–33], the main methods (discussed in [34, 35]) are presented below:

1. Bulk etching with bonding or fusing of the patterned glass, silicon or hard polymer (e.g. polystyrene or polycarbonate).

2. Use of a sacrificial patterned resist under vapor deposited polymers [36].

3. Patterning channels in a polymer and sealing it to a solid substrate. Ex-

amples include PDMS (or polydimethylsiloxane which is a soft conformal polymer) [37] or SU-8.

3.1.2 Power Supply

Recent efforts in academia at the miniaturization of the power supply include a battery-powered, high-voltage power supply with electrochemical (EC) detection and interface circuits designed for microchip capillary electrophoresis (CE) by Jackson *et al.* [1]. The power supply (Fig. 3.1) occupies a space of 7.62 x 10.16 x 2.54 cm^3 and can generate $\pm$1000 V with a maximum output current of 380 μA. Garcia *et al.* developed a battery operated 3-channel high voltage power supply for microchip capillary electrophoresis (CE) with dimensions of 9.5 x 18.4 x 26.4 cm^3 (weighing approximately 3.5 kg) capable of generating a 0 to $\pm$4000 V range for a variety of microchip setups [38]. Most recently, Erickson *et al.* developed a 2.1 x 10 x 2.5 cm^3 device (Fig. 3.2) capable of generating 700 V with a 12 V input voltage [2]. All of these devices rely on off-the-shelf high voltage (HV) DC-DC converters versus custom designing the HV power supplies, lending themselves to larger sizes and higher costs. However, with the increasing demand in applications such high voltage MEMs, automobile parts, medical devices, telecommunication circuits and field-emission displays, and the recent developments in HV semiconductor pro-

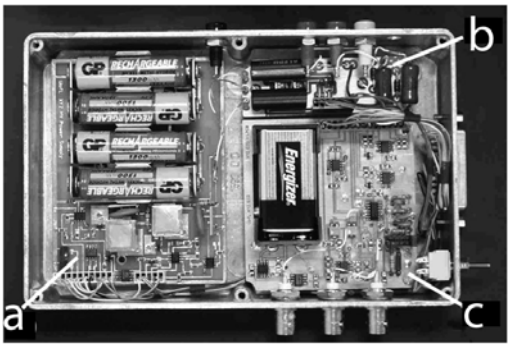

Figure 3.1: The power supply used by Jackson *et al.* [1] including the (a) dual-source high-voltage power supply, (b) interface circuit, and (c) amperometric detection circuit

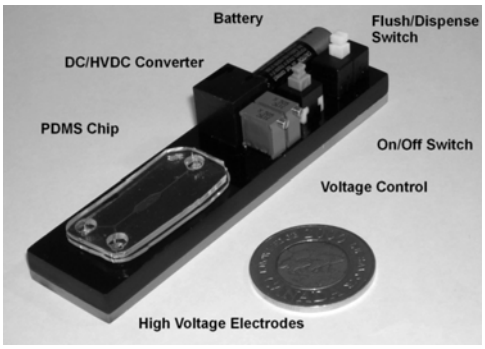

Figure 3.2: Photograph of the power supply used by Erickson *et al.* [2]

cesses, smart power technology [39] (integrated LV and HV) systems offer an excellent alternative to existing bench-top and off-the-shelf power supplies. Current HV CMOS semiconductor foundries like AMS, Atmel, DALSA and X-FAB offer voltages up to 70 V, 40 V, 600 V and 650 V respectively. With such voltages available, high voltage generation for microfluidic applications is not far away. Richards *et al.* [40] reported a high voltage charge pump circuit (integrated in 0.8-μm process) capable of producing 50 V output from a typical 5V input using a 16-stage Pelliconi cascade charge pump (illustrated in Fig. 3.3) along with stacked poly1-metal1-metal2 capacitors. Though still shy of the required high voltage, this design demonstrates the possibilities of HV CMOS processes.

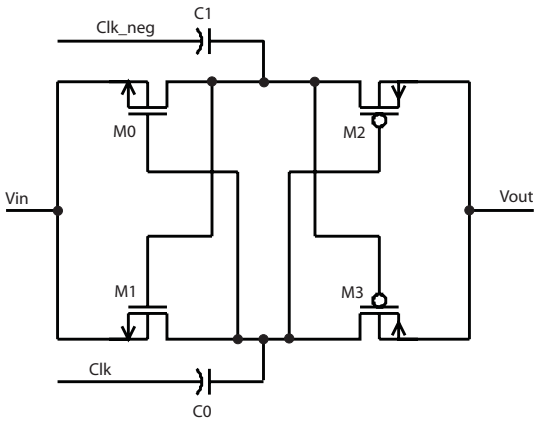

Figure 3.3: Pelliconi cascade charge pump architecture

Besides generating the required high-voltages, switching of the output states is also required. Currently large and expensive off-the-shelf electromechanical switches (e.g. relays) are used for this task. However, with new protocols which take advantage of rapidly switching electric fields (e.g. 10 – 100 Hz) to mimic longer channels in shorter channel systems, relays (with their limited lifetime of about 1 million or so number of fixed operations) pose serious limitations. Solid-state CMOS circuits however overcome this by not only offering orders of magnitude higher lifetime of operation but also direct integration with the high-voltage generation - all on the same substrate.

3.1.3 Optical Detection

In regards to detection methods, most methods of optical detection for compact systems rely on bounded glass substrate technology (for the microfluidics) with an off-chip photomultiplier for laser induced fluorescence detection. However, the large external requirements limit the integration possible. Non-optical detection techniques (e.g. electrochemical) [41] are practical for portable applications, however, fluorescence detection is preferred because it is chemically decoupled from the analysis step, and many of the current biochemistry protocols already incorporate fluorescent labels. Webster *et al.* developed a CE device with integrated fluorescence detector using an external LED and a custom photodiode on a silicon substrate [3]. Though sensitive, the measurement and readout equipment were external. This microfluidic system is shown in Fig. 3.4. A more portable system was developed by Novak et al [4] illustrated in Fig. 3.5. This system, inspired by the DVD pickup head (and similar in size), integrated the optics (filter, mirror, lens, LED, exciter, emitter), detector (photodiode) and the electronics (lock-in amplifier). However, both of these examples still rely on large and bulky external components.

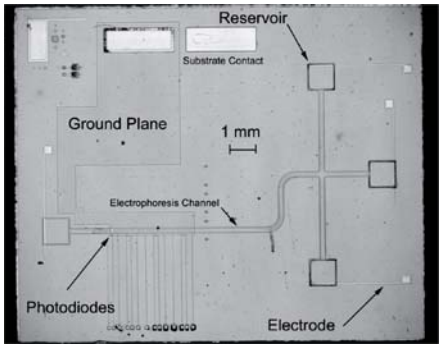

Figure 3.4: Microfluidic system [3]

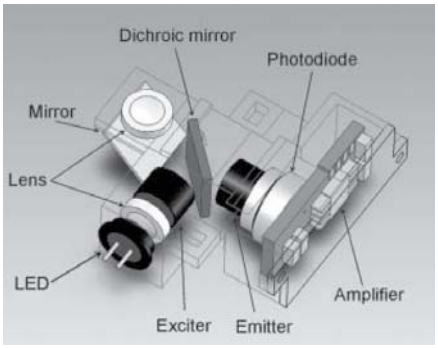

Figure 3.5: Optical system schematic [4]

More recent work has investigated integration in conventional CMOS process. This encourages miniaturization by allowing the optical detectors (e.g. photodiodes) to be on the same substrate as the amplification/detection circuits. Patounakis *et al.* [42] developed an active CMOS biochip (in a 0.25-μm process) with an in-

tegrated pixel array using time-gated (sampling for some specified duration), time-resolved (able to differentiate different sources) detection without the need for optical filters. This was accomplished by using the fact that fluorescence intensity exponentially decays slower than a pulsed laser can be turned off. Hartley *et al.* [7] fabricated a 16-element linear array CMOS sensor chip (in 0.18-μm process) using active pixel sensors [43], correlated double sampling (CDS) [44], and spatial filters. This design was used to perform flow cytometry (a technique used to count, examine and sort microscopic particles in a fluid flowing medium) and is more useful in counting then evaluating optical intensities of marked particles. Manaresi *et al.* [5] introduced a chip (implemented in 0.35-μm CMOS technology) consisting of an active-pixel sensor, 2 x 17 μm photodiode and a readout circuit consisting of a fully differential charge integrator using correlated double sampling.

3.2 Integrated Systems

The following three works, though different in implementation and direct biological application, illustrate excellent examples of CMOS chips integrated along with the microfluidics. The first two methods allow for programmable manipulation of individual particles without fluid flow, the first combining embedded optical detection and transport, and the second without the integrated detection. The third design introduces an active pixel sensor and microfluidics for cytometry on a chip.

Manaresi *et al.* [5] (Fig. 3.6) presented the first device capable of individual particle manipulation without fluid flow. This was accomplished by implementing a moving DEP (dielectrophoresis) cage approach. A DEP cage is created by applying a counterphase sinusoidal voltage to an electrode on the chip and the asscoiated microchamber lid, while at the same time applying an in-phase sinusoidal voltage to the neighboring electrodes. By changing the pattern of voltages applied, cells can be trapped and moved. Each electrode site also contains a readout circuit consisting of a CMOS active pixel sensor with a fully differential charge integrator implementing CDS. This chip is packaged with the microfluidics by gluing a conductive-glass lid with SU-8 walls to the chip to define the microchamber and mounting the die

directly on a printed circuit board.

Lee *et al.* [6] demonstrated an extremely novel method of cell manipulation using magnetic fields. A SiGe chip (which provides a high Q factor) containing an array of microcoils (along with logic), each capable of producing spatially-patterned microscopic magnetic fields was fabricated. A microfluidic channel was then post-processed directly on the SiGe die using PDMS (illustrated in 3.7). Once sealed, the microfluidic channel plus wells are injected with biological samples containing magnetic beads. The magnetic beads are then actuated using the microcoil array. This illustrates an excellent method of cell actuation without the use of electrophoresis forces.

Finally, Hartley *et al.* [7] introduced an active pixel sensor integrated with microfluidics for cytometry on a chip. This paper illustrates a clean and interesting method of integrating the electronics and microfluidics. As shown in Fig. 3.8, the CMOS sensor is solder-reflow flip-chipped bonded to a thin (100 μ) glass patterned with Cr-Ni-Au (50 nm – 50 nm – 1250 nm) which is then permanently bonded to a thicker glass (1.1 mm) which acts as mechanical support and contains the microchannel. Though the design and method of integration are relevant, the target application (cytometry) caters towards cell counting, rather than identification (e.g. via fluorescence) - which is what we are interested in.

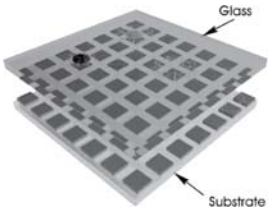

Figure 3.6: Manaresi *et al.* integrated system [5]

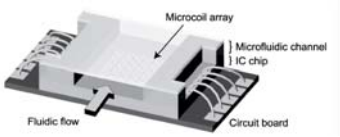

Figure 3.7: Lee *et al.* integrated system [6]

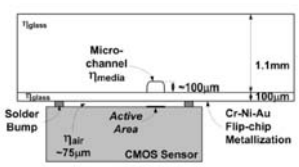

Figure 3.8: Hartley *et al.* integrated system [7]

Chapter 4

Integrated Optical Detection

In this chapter, the requirements for fluorescence based optical detection in CE is first discussed, followed by background information on CMOS optical sensors and their associated circuitry. The methodology and reasoning behind the design, along with simulations is then presented, concluding with actual measured results.

4.1 Motivation

Due to the high excitation powers and low background levels made possible with lasers and dichroic mirror (plus filter) combinations, confocal laser-induced fluorescence (LIF) offers the most sensitive method of detection to date for CE systems [45]. However, many of the current systems (as illustrated in Fig. 4.1) are not conducive for integrated systems, and wafer level fabrication, as they rely on large and bulky external components. Such systems typically include [46]:

- A light source for excitation of the fluorophore (usually a laser)
- A dichroic mirror to reflect the excitation wavelength while allowing the emission wavelength to pass
- A microscope objective to focus the light
- A bandpass filter to reject the scattering of the emitted fluorescence (collected by the objective and passed by the dichroic mirror) [47]
- A pinhole aperture to spatially reject the out-of-plane light

- A detector (e.g. avalanche photodiode or photomultiplier) and associated signal processing to capture and process the image information.

However, by integrating the microfluidics and filter directly on top of the substrate (containing the detector) and minimizing the distance between the sample and detector, the focusing lens along with many of the other macro components can be eliminated. The proposed system is illustrated in Fig. 4.2 and all future presented detector and related circuit designs refer back to this figure.

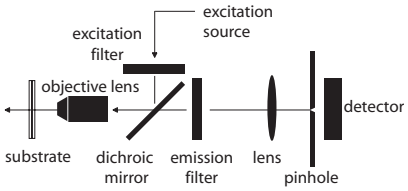

Figure 4.1: Typical confocal LIF system

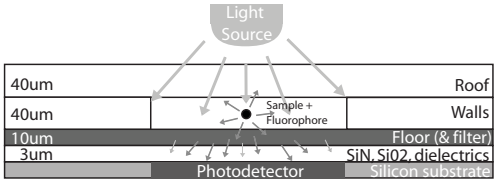

Figure 4.2: Optical system schematic

4.2 Requirements

To design sensors and circuits capable of sensitive optical detection of emitted florescence (as in the system illustrated in Fig. 4.2) first order calculations can be made to determine the optical power reaching the sensor. In this first order approximation, we assume a black box where excitation light(e.g. from a laser), I_0, enters and emitted light (from the fluorophore), $I(z)$, exits after passing through a distance, z. This relationship, illustrated in Fig. 4.3, can be expressed using the absorption (Lambert-Bouguer) law as:

$$I(z) = I_0 e^{-\alpha z} \tag{4.1}$$

Where α, the absorption coefficient (cm^{-1}), is a property of a material that defines the extent to which the material absorbs energy.

Considering though, that the assumed black box consists of a solution mixture of fluorescently tagged analytes, the Beer-Lambert law and the quantum yield of the fluorophore is used to quantify the light energy absorbed and emitted by the

fluorescence. Beer-Lambert's Law (illustrated in Fig. 4.3) states that the incident light, I_0, is absorbed by a given material of thickness T, and concentration C, such that the exiting light is given by:

$$I = I_0 10^{-\varepsilon CT} \tag{4.2}$$

where ε is the extinction coefficient and is a measure of how strongly a chemical species absorbs light ($\text{mol}^{-1}\text{cm}^{-1}$).

Assuming very low concentrations, the amount of light absorbed can then be approximated using the first term in the Maclaurin series (i.e. a Taylor series expansion of a function about 0) as:

$$I_{abs} = I_0 - I \cong \ln 10 \varepsilon CT I_0 \tag{4.3}$$

For fluorescence, the quantum yield, Q, is defined as the ratio of the number of photons emitted to the number of photons absorbed. Using this and the absorbed light energy, we can determine the released light energy as:

$$I_{emitted} = QI_{abs} \cong Q \ln 10 \varepsilon CT I_0 \tag{4.4}$$

From this, we can see that the energy emitted can be increased by increasing the concentration, path length, the incident optical power, or by changing the fluorophore (which affects the quantum yield and extinction coefficient). By increasing the emitted optical power, we require less sensitive detectors and circuits.

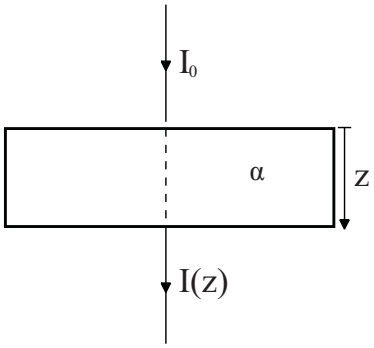

Figure 4.3: Diagram of Beer-Lambert absorption of a beam of light through a material of thickness T

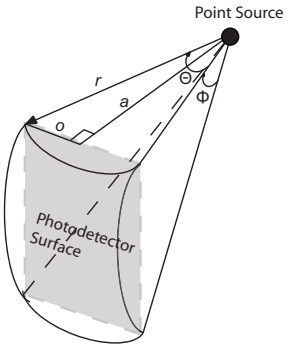

Figure 4.4: Integrating over a sphere cut with dimensions equal that of the photodetector

The second step required is to determine the amount of emitted optical power reaching the sensor. Using Fig. 4.4, by assuming a point source in the middle of the channel and integrating over the area of the sensor (assumed to be a square) divided by the total area of a sphere wrapped around the point source, the light collection efficiency is:

$$\text{collection efficiency} = \frac{4\mathrm{r}^2 \int_0^{tan^{-1}(\frac{o}{a})} \int_0^{tan^{-1}(\frac{o}{a})} \mathrm{d}\phi\mathrm{d}\theta}{4\pi r^2} \tag{4.5}$$

Two additional factors also need to be considered:

1. The fluorophore may be excited at a wavelength other than its maximum. This does not change the shape of the emission spectrum, however, the intensity of the emission is directly dependent on the amount of light the fluorophore absorbs. Thus, using a LED or even laser where the spectral (band) characteristics do not match the fluorescence efficiency (Fig. 2.3) results in reduced (by some $f2$) emission from the dye.

2. The excitation filter attenuates (by some $f2$) the emitted light energy.

With these final factors, the total light collected by the sensor can be expressed as:

$$\text{Total collected Light} = (I_{emitted} \times f1) \times (\text{collection efficiency} \times f2) \tag{4.6}$$

Table 4.1: Parameters for a ROX fluorescent marker and dimensions from Fig. 4.2

Parameters			
Name	Description	Value	Unit
Q	Quantum Yield	70	%
ε	Extinction Coefficient	16.91	nM
C	Fluorophore Concentration	8.2	$\mu m^{-1}M^{-1}$
T	Path Length	40	μm
I_0	Excitation Light Intensity (532 nm)	200	μW
o	Half of the Detector Active Length	75	μm
a	Distance from Sample Point Source to Detector	33	μm
$f1$	Fluorophore Excitation Amount	40	%
$f2$	Emitted Light Transmission through Filter (@600 nm)	10	%

Using the design criteria in Table 4.1 and Equ. 4.6, the total optical power reaching the sensor is determined to be about 30.4 pW. This provides a first-order approximation of the optical power that may reach the detector. However, depending on the peak height, the actual value may be an order larger or smaller.

4.3 Background

The amount of optical power reaching the sensor provides an idea of how sensitive the detector and circuits need to be. In this subsection, background information is presented on the different detectors and the techniques used to meet such low light detection requirements.

4.3.1 Silicon Photodiode Physics

Silicon photodiodes are solid-state devices that convert light energy into electrical energy. The photodiode regions are constructed when a p-type dopant (with acceptor impurities) is brought into contact with an n-type dopant (with donor properties). With no externally applied bias, the concentration gradient formed by the large number of electrons in the n-type semiconductor, and large number of holes in the p-type semiconductor causes the electrons to diffuse into the p-type material and holes to diffuse into the n-type material. When the electrons and holes move to their respective sides, they leave behind immobile (i.e. part of the crystal lattice) positive and negative uncovered (ionized) dopant atoms respectively. An electric field forms between the positive and negative exposed ion regions (forming a built in potential), which quickly sweeps the carriers out, leaving the region depleted of free carriers (i.e. the depletion region).

When a a photon of energy greater than the band gap of silicon 1.12 eV ($\lambda < 1100\,nm$ - the infrared region of the electromagnetic spectrum) falls on the device, an electron-hole pair is created. It is important to note that, with the exception of carrier diffusion, only the light absorbed in the depletion region is used to generate the photocurrent. Furthermore, different energies of light are absorbed at different depths. The higher the wavelength of the photon, the deeper in the device it

is absorbed. This is illustrated in Fig. 4.5 and based on Equ. 4.1. The electron-

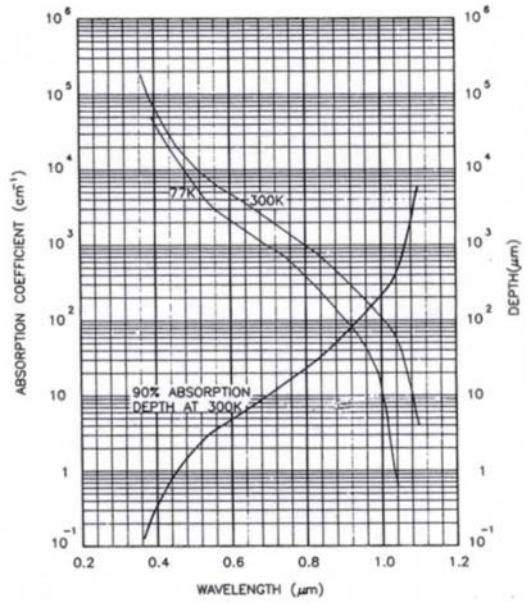

Figure 4.5: Light absorption coefficient, α, as a function of wavelength for silicon [8].

hole pairs generated in the depletion region are swept by the electric field and if the two sides of the p-n junction are electrically contacted, an external current flows. Electron-hole pairs created from photons not absorbed in the depletion region diffuse for average time called the carrier lifetime (determined by the purity of the silicon region), τ. If the carrier lifetime is short, the carriers quickly recombine and do not contribute to the photocurrent. However, if carriers are generated within a diffusion length, L of the depletion region, they are collected and contribute to the photocurrent. The diffusion length is defined by:

$$L = \sqrt{D\tau} \tag{4.7}$$

Where D is the diffusion coefficient defined by the process.

4.3.2 Silicon Photodiode Modes of Operation

There are two modes of operation for silicon photodiodes, photovoltaic (PV) and photoconductive (PC). In photoconductive mode, the diode is reverse biased and

acts like a current source, while in photovoltaic mode, the diode is not biased and exhibits nonlinear characteristics with very bright light conditions or large load resistance. The I-V curve for the two different modes, along with their associated load lines is illustrated in Fig. 4.6. Increase in illumination shifts this curve down, representing an increase in photocurrent. The output current can be expressed by:

$$I_o = I_{ph} - I_S(e^{(\frac{qV}{nkT})} - 1) - I_{shunt} \tag{4.8}$$

and is determined using the equivalent photodiode circuit illustrated in Fig. 4.7. In the above equation, the second term represents the diode current (I_D), I_S is the photodiode reverse saturation current, q is the electron charge, k is Boltzmann's constant, T is the absolute temperature of the photodiode, I_{ph} is the photocurrent under illumination, and I_{shunt} is the current through the shunt resistance (R_{sh}).

If the terminals of the photodiode are shorted, a photocurrent I_{SC} proportional to the light intensity flows from the anode to the cathode, and when the circuit is open, an open circuit voltage, V_{OC} is generated with positive polarity at the anode. The choice of PC or PV mode operation depends on several factors:

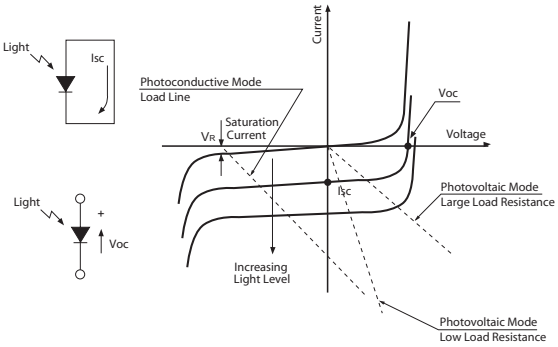

Figure 4.6: I-V characteristic, operating regions (load-lines), and open/short circuit diagram for silicon photodiodes [9].

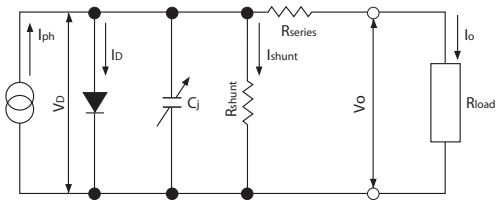

Figure 4.7: The photodiode circuit [9]

- PC mode exhibits a large (higher than nine orders of magnitude) linear range of operation with increasing illumination. PV mode however has a limited linear range of operation (which can be extended by decreasing the load resistance).

- The response time is dependent on the RC time constant defined by the diode capacitance and load resistance. Under the application of a reverse bias (in the PC mode), the depletion width is increased reducing the capacitance and the response time.

- Defects in the silicon crystal lattice result in trap sites in the forbidden energy gap (the region between the valence and conduction bands) and correspondingly act as generation-recombination centers, producing current. This current is generated in the depletion region and is proportional to the junction area and depletion region width. It is this current in combination with the diffusion current (which saturates at I_S under the application of a reverse bias) that results in a so called dark current, which acts to limit the low light sensitivity of PC mode photodiodes. In PV mode, as no bias is applied, the dark current is theoretically zero, allowing for high SNR in low light conditions. It is important to note that there are two other factors, band-to-band tunneling and thermionic emission currents, which also contribute to the dark current. However, as their contributions are small, they are not considered here.

4.3.3 Silicon Photodiode Characteristics

To determine the response of a photodiode to different wavelengths and its lower limit of detection, responsitivity, quantum efficiency, and the noise equivalent power (NEP) are introduced and examined respectively in this subsection.

One of the key parameters when dealing with photodiodes is responsitivity, R, defined as the current (I_o) generated for each received watt of incident optical power (Φ) with units of ampere per watt (A/W). In the ideal case, each incident photon generates an electron-hole pair and [1]:

$$R_{ideal} = \frac{I_o}{\Phi} = \frac{q\lambda}{hc} \tag{4.9}$$

where λ is the wavelength of the incident light, h is Planck's constant, and c is the speed of light. However, as can be seen from Fig. 4.8, the typical responsitivity for

real silicon photodiodes deviates from the ideal case. The initial reduction is due to photons that are reflected from the surface, never penetrating the material and thus never reaching the depletion region. For the case of normal incidence, this reflection coefficient (R) (assuming light passing from air into a material of refractive index, n) can be calculated using Fresnels equation [1]:

$$R = \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^2 \tag{4.10}$$

As illustrated in Fig. 4.9, for silicon, with n $\approx$ 3.5, the reflection coefficient is 31%, leaving only 69% of the light left to penetrate into the detector material.

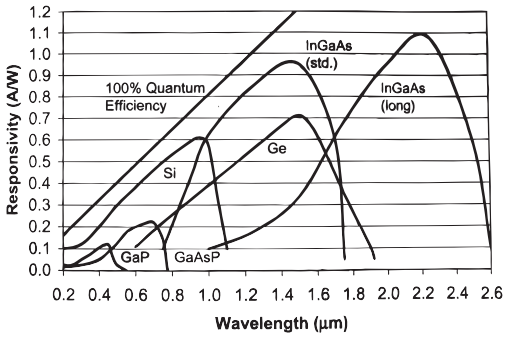

Figure 4.8: Responsitivity of different semiconductor materials with respect to 100% QE [1].

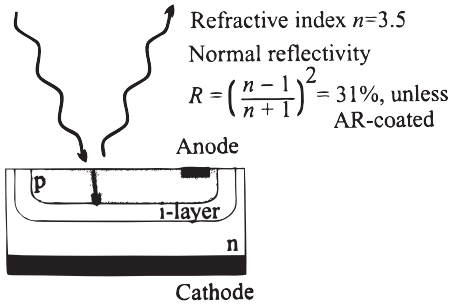

Figure 4.9: High reflectivity of an air/silicon interface (given by Fresnel equations) [1]

This is mirrored in the near 30% reduction of responsitivity from the ideal 100% quantum efficiency case (Fig. 4.8). In addition to this reduction due to the interface, at short wavelengths (i.e. less than 380μm) and at wavelengths greater than 1.1 μm, there is a further minor and steep fall-off of responsitivity respectively. The minor reduction is because the photons are absorbed too near to the surface; this prevents the generated electron-hole pairs from contributing to the photocurrent as they are not near enough to the electric field of the deeper depletion region to be swept in. The steep fall-off on the other hand, is because the photons have insufficient energy to overcome the bandgap of the semiconductor (e.g. 1.12 eV for silicon) and consequently pass through the crystal. Such deviations of the actual from ideal

responsitivity is called quantum efficiency (η) [1]:

$$\eta = \frac{R_actual}{R_ideal} = \frac{I_0 hc}{\Phi\lambda} \tag{4.11}$$

and represents the ratio of the number of electron-hole pairs which contribute to the generated photocurrent, to the number of incident photons.

Responsitivity and quantum efficiency help establish the amount of current that is generated for a given incident light power, however, to quantify the limit of detection, it is useful to examine the noise sources present in a photodiode. There are three main sources of noise in photodiodes, thermal (or Johnson noise, I_J), shot noise (I_S), and flicker noise (I_F). Since these sources are independent of each other, the total noise current can be expressed by [9]:

$$I_N = \sqrt{I_J^2 + I_S^2 + I_F^2} \tag{4.12}$$

The thermal noise is generated by the random thermal motion of electrons and is present in any linear passive resistor. For the photodiode, the thermal noise contribution comes from the shunt resistance (R_{sh}) and is expressed as [9]:

$$\frac{I_J}{\sqrt{B}} = \sqrt{\frac{4kT}{R_{sh}}} \qquad (A/\sqrt{Hz}) \tag{4.13}$$

where k is Boltzmann's constant (1.38×10^{-23} J/K), T is the absolute temperature (K), and B is the noise bandwidth (Hz). Most often, since the thermal noise is independent of frequency, it is expressed in units of $A/\sqrt{Hz}$.

Shot noise is generated by random fluctuations in the normal current flow through a P-N junction. Since the flow carriers is subject to random movements, a noise current is generated. Since it is independent of frequency, similar to thermal noise, it can be expressed in units of $A/\sqrt{Hz}$ and is given by [9]:

$$\frac{I_S}{\sqrt{B}} = \sqrt{2q(I_{ph} + I_{dark})} \qquad (A/\sqrt{Hz}) \tag{4.14}$$

where q is the electron charge.

For Flicker (1/f) noise, the mechanisms behind it are not very well understood, instead, a general equation to represent this type of noise has been determined ex-

perimentally and is given by [9]:

$$\frac{I_F}{\sqrt{B}} = \sqrt{\frac{KI_{dc}}{f}} \qquad (A/\sqrt{Hz}) \tag{4.15}$$

where K is a constant that depends on the type of material and geometry, I_{dc} is the dc junction current and f is the frequency. Flicker noise dominates when the bandwidth of interest contains frequencies less than about 1 kHz.

The lower limit of detection for a photodiode can then be expressed as the intensity of incident light required to generate a current equal to the total noise currents (I_N). This limit is called the Noise Equivalent Power (NEP) and is defined over a frequency of interest by [9]:

$$NEP = \frac{I_N}{R} \tag{4.16}$$

where R is the responsitivity (A/W).

4.3.4 Avalanche Photodiodes

With internal gain, avalanche photodiodes exhibit quantum efficiencies greater than 100%. Thus, in low light conditions, where the noise of the amplifier can exceed the noise of the amplified signal, avalanche photodiodes provide an excellent alternative to standard photodiodes by reducing strict amplifier dependence.

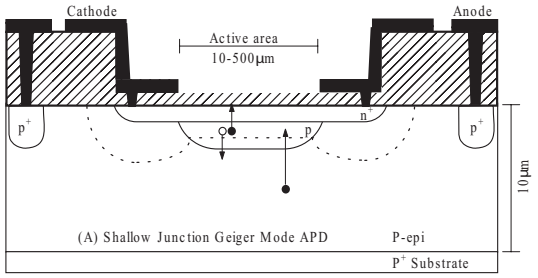

Figure 4.10: Shallow junction Geiger-mode avalanche photodiode [10]

In the linear mode of operation, APDs are operated below their breakdown voltage, and the applied electric field determines a level of internal gain (i.e. the number of electron-hole pairs generated per incident detected photon). Operated in 'Geiger-mode', silicon APDs allow for single-photon detection. Shallow junction Geiger-mode APD detectors have been manufactured with CMOS compatible processing

steps [48], however, their operation requires much higher reverse bias voltages then standard silicon photodiodes operated in PC mode.

A schematic cross-section of a shallow junction APD is illustrated in Fig. 4.10. For Geiger-mode, by applying a reverse bias in excess of the breakdown voltage of the device, a single electron-hole pair created by an incident photon in the depletion layer experiences a self-sustaining avalanche multiplication effect (impact ionization). By reducing the reverse voltage below the breakdown potential, the device can be "quenched," [49] preventing damage due to high power (heating effects), by ending the avalanche event. This is accomplished using either a passive quenched circuit [50] which simply consists of a resistor in series with the APD or an active quenched circuit [51]. Passive quenched circuits are only adequate for low count rates ($< 10^5/\text{s}$) due to the time constant delay (of the quenching resistor and detector capacitance), while active quenched circuits are used for higher count rates (e.g. 6.7 GHz [52]) as the circuits can be optimized to reduce dead-times (i.e. time it takes to place the APD in a reverse bias state after quenching). Fig. 4.11 illustrates an example of an active quenched circuit [11]. The APD anode is biased at a large negative potential ($-\text{V}_{\text{NN}}$) to allow low-voltage components to be used in the quenching circuit.

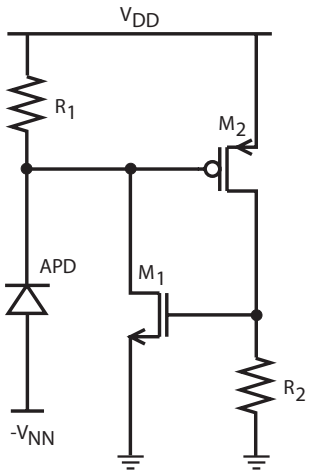

Figure 4.11: A basic active quenched APD circuit [11].

4.3.5 High Voltage Process

The work described in this thesis is designed using DALSA Semiconductor's three metal layer, triple well, dual gate oxide 0.8-μm 5V/HV CMOS/DMOS process. It is smart power technology [39] (i.e. incorporating both low-voltage and high-voltage components on the same substrate) which uses double-Diffused Metal-Oxide Semiconductor (DMOS) transistors in order to obtain high voltage integrated circuits. By defining separate low-voltage and high-voltage regions through deep or high-voltage N-wells, 5 V mixed signal circuits can be isolated from the high-voltage components, which can support source-drain breakdown voltages up to 600V [53].

The multitude of layers available in this process allows us to define different junction depths and structures for avalanche and standard silicon photodiodes. As different wavelengths are absorbed at different depths, by using different junction depths we can cater photodiode responses for specific wavelengths. The different junctions available in this process are illustrated in Fig. 4.12.

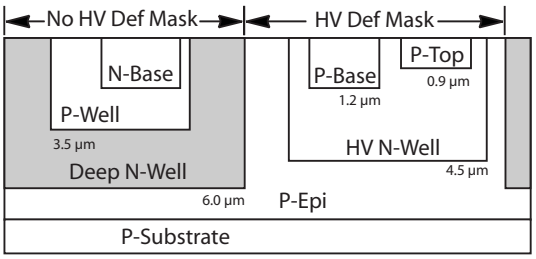

Figure 4.12: Simplified cross section of the 0.8m 5V/High-Voltage process highlighting available junctions and associated depths

4.4 Design and Operation

Using DALSA Semiconductor's 0.8-μm 5V/HV process, five different junction photodiodes and three different avalanche photodiode configurations were designed. In addition, an integrating transimpedance amplifier (TIA) utilizing a 3T active pixel and "lock-in amplifier" approach was designed to convert the photocurrent collected from the photodiodes into an acceptable voltage level for use with an

analog-to-digital converter. An active quenched circuit, coupled to a digital counter was also designed for avalanche photodiodes operating in Geiger-mode.

In the following, the first two subsections discuss the different photodiode and APD structures. The third and fourth subsections present the design of the TIA and the active quenched circuits respectively.

4.4.1 Photodiode Structures

In most classic N-Well CMOS processes, only three photodiode structures are possible (n+/P-sub, N-Well/P-sub, and p+/N-Well [54]), however the large number of layers available in the DALSA process allows us to create many different junction combinations.

Five different photodiode structures were designed on two different chips, ICKAALC2 and ICKAATC1. The five configurations are illustrated in the Fig. 4.14 - 4.18. To understand the choice behind using specific junctions for each design, it is important to reiterate the well known fact that the depletion region extends into the lighter doped region. This can be explained briefly by the relationship between dopant concentration (where N_D and N_A represent the donor and acceptor concentration respectively) and the total uncovered charge (Q) in unbiased P-N junctions [12]:

$$Q_1 = +q(d_1A)N_D \tag{4.17}$$

$$Q_2 = -q(d_2A)N_A \tag{4.18}$$

where q is the charge of the ionized (uncovered) atoms and d represents the width of the depletion region extending into the specific P or N region. Under equilibrium conditions, and assuming the n-type region is more heavily doped (i.e. $N_D >> N_A$), the width of the depletion region (d_1A) extending into the lighter doped (N_A) region must be larger than that of the heavier doped region to maintain overall charge neutrality (i.e. $Q_1 = -Q_2$). This is illustrated below in Fig. 4.13. For the five different designs, the depletion region extending into the lighter doped region is illustrated in Fig. 4.14 - 4.18, through the dashed lines. As the depletion region extends mostly

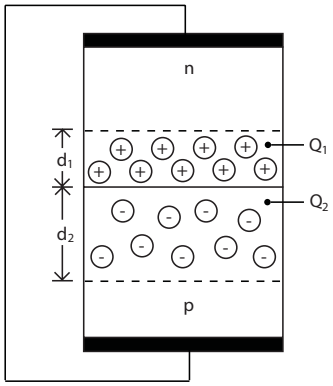

Figure 4.13: A P-N junction under zero bias [12]

into the lighter doped region, the shallower depletion region in the more heavily doped region is not shown in our figures. By knowing in which junction the depletion region predominantly extends, an estimate of its depth can be made.

Each of the five designed devices is discussed briefly below:

1. p+/Deep N-Well Photodiode (PD1): The anode of this photodiode is the p+ diffusion and the cathode is the Deep N-Well. This configuration allows for substrate-isolated optical detectors as it can be placed in its own seperate Deep N-Well. The p+ diffusion is approximately 0.4 μm deep and the N-Well is about 6.0 μm deep. However, since the p+ diffusion has a much larger doping concentration than the Deep N-Well, the depletion region extends into the Deep N-Well. The designed active area is 50 μm $\times$ 50 μm and the N-Well contacts are placed minimum design rule distance away from the p+ diffusion.

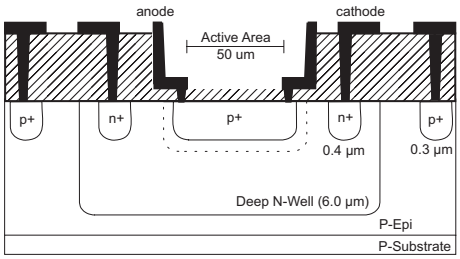

Figure 4.14: PD1: p+ / Deep N-Well with a depletion region around 0.3 μm.

2. P-Well/n+ Photodiode (PD2): The anode of this device is the P-Well and the cathode is the n+ diffusion. This device also allows for isolation since it is in its own P-Well. The P-Well and n+ diffusion have a depth of 3.5 μm and 0.4 μm respectively and the depletion region extends into the lighter doped P-Well. Two different active area sizes were implemented, a 50 μm $\times$ 50 μm photodiode in ICKAALC2 and a 150 μm $\times$ 150 μm photodiode in ICKAATC1.

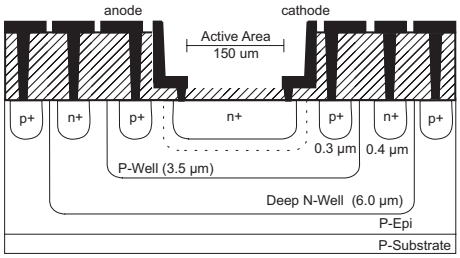

Figure 4.15: PD2: P-Well / n+ with a depletion region around 0.4 μm.

3. P-Epi/Deep N-Well Photodiode (PD3): The anode is the P-Epi layer and the cathode is the Deep N-Well. The deep N-Well extends 6.0 μm deep and the depletion region extends into the lighter doped P-Epi region. A 150 μm $\times$ 150 μm active area photodiode was implemented on ICKAATC1.

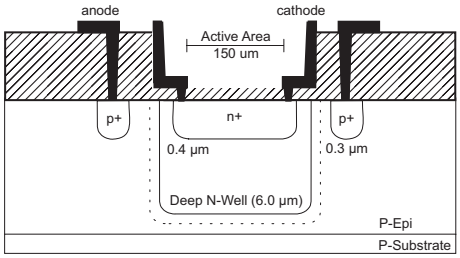

Figure 4.16: PD3: P-Epi / Deep N-Well with a depletion region around 6.0 μm.

4. P-Epi/HV N-Well Photodiode (PD4): Once again, the anode is the P-Epi layer, however in this case the cathode is the HV N-Well. The HV

N-Well is shallower than the Deep N-Well extending only 4.5 μm deep. The depletion region extends once more into the lighter doped p-epitaxial layer. This photodiode was implemented on ICKAATC1 with an active area of 150 μm $\times$ 150 μm.

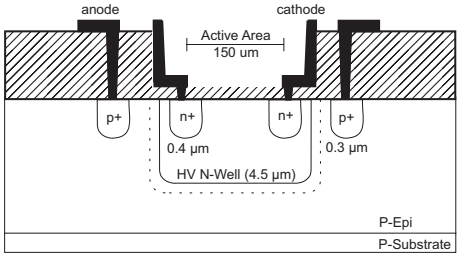

Figure 4.17: PD4: P-Epi / HV N-Well with a depletion region around 4.5 μm.

5. P-Base/HV N-Well Photodiode (PD5): The anode is the P-Base layer and the cathode is the 4.5 μm deep HV N-Well. With the P-base junction depth of 1.2 μm and its higher doping profile, the depletion region extends into the HV N-Well. This photodiode was also implemented on ICKAATC1 with an active area of 150 μm $\times$ 150 μm.

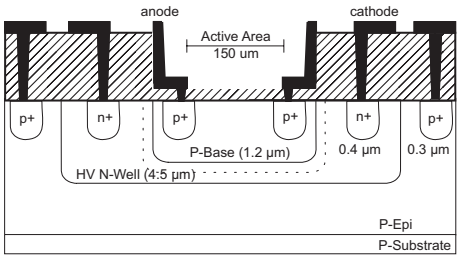

Figure 4.18: PD5: P-Base / HV N-Well with a depletion region around 1.2 μm.

4.4.2 Avalanche Photodiode Structures

Because of the high voltages required for Linear and Geiger Mode APDs, the design of such components is more involved than standard P-N junction photodiodes.

The main issue is the higher electric fields which appear at the junction edges. For proper avalanche operation, the highest electric field should be confined to the center of the diode. However, since:

1. The highest electric field is present at the edges because of the non-planer, spherical geometry of the junction and

2. Breakdown occurs in the region (i.e. edges) where breakdown is first reached

it becomes difficult to contain the highest electric field to the center of the diode as the edges (and hence the junction) breakdown at lower fields first.

The electric field at breakdown for Si at room temperature is defined by [55]:

$$E_m = \frac{4 \times 10^5}{1 - \frac{1}{3}\log_{10}(N/10^{16})} \tag{4.19}$$

When the dopant concentration (N) in a semiconductor changes abruptly from acceptor, N_A, to donor dopants, N_D, you have an abrupt junction. In particular if $N_A \gg N_D$ (or vice versa), you get a one sided abrupt $p^+ - n$ (or $n^+ - p$) junction. Assuming a one-sided abrupt P-N diode, the corresponding breakdown voltage can be determined using [55]:

$$V_{br} = \frac{\varepsilon_s E_m^2}{2qN} \tag{4.20}$$

and the corresponding depletion region width equals [55]:

$$w_{br} = \frac{\varepsilon_s E_m}{2qN} \tag{4.21}$$

It is important to note however that the equations above are given for a one-sided abrupt junction and in reality, linearly graded or diffused junctions with curvature have reduced breakdown voltages [33].

Even though the breakdown voltage is inversely proportional to the doping density, a circuit designer does not have direct control over this property. There are however two common methods of addressing edge breakdown and they include either using periphery guard rings or by using a virtual guard ring:

1. By placing low-doped guard ring regions at the periphery (Fig. 4.19a), premature breakdown of the edges can be suppressed allowing for higher electric fields at the center of the junction.

2. By placing a highly doped region (n-base doping $>$ n-well doping) at the center of the diode (Fig. 4.19b), a lower breakdown voltage region is established, allowing for proper (center breakdown) avalanche operation.

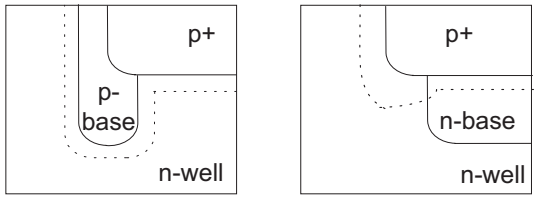

Figure 4.19: Two methods of edge breakdown prevention

These two corresponding methods were used in the design of the four different avalanche photodiode structures illustrated in Fig. 4.20, but the same structures can also be used in the design of zener diodes. The first two designs use lighter doped (higher breakdown voltage) guard rings at the edges of the anode junction. APD1 is in the deep N-Well for low voltage operation while APD2 is implemented in the HV N-Well for higher voltage (and thus superior avalanche) operation. The $p^+/\mathrm{DeepN-Well}$ breakdown voltage is 13 V and the $p^+/\mathrm{HVN-Well}$ is 18 V. If these are the potentials at which the edge breaks down first, then the center of the junction never reaches these voltages. However, since the $\mathrm{P-Well/DeepN-Well}$ and $\mathrm{P-Base/HVN-Well}$ breakdown voltage is 40 V, by adding guard ring structures the the junction periphery, higher electric fields are achieved at the center of the APDs. Similarly, by placing a virtual guard ring at the center of the junction, the depletion region width is extended around the edges allowing for optimal electric fields at the center of APD3 and APD4. The active area of the avalanche photodiodes was matched to the width of the microfluidic channel that would be post-processed overtop of the detector.

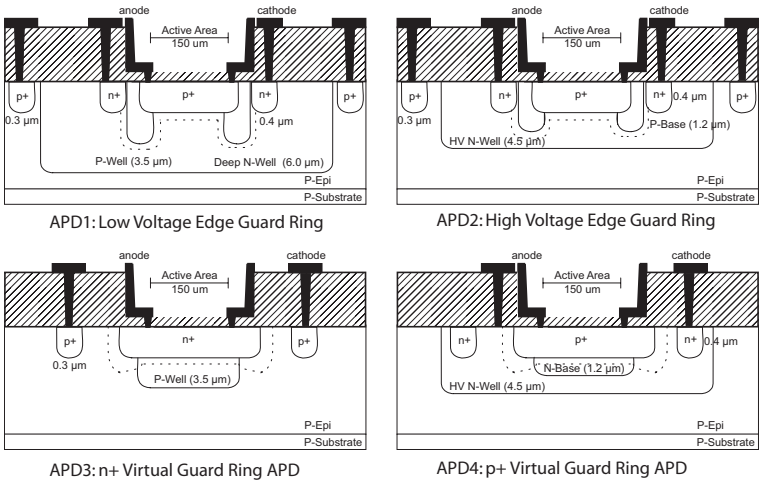

Figure 4.20: The 4 different avalanche photodiode implementations

4.4.3 Photodiode Based Optical Detection Circuit

The design of the silicon photodiode based optical detection circuit involved addressing several problems:

- Low light conditions: the estimated optical power reaching a 150 μm $\times$ 150 μm photodiode (in the proposed optical setup, Fig. 4.2) is about 30.4 pW (calculated in Section 4.2). Such low light conditions translate to very low (picoamp) photocurrents, requiring very sensitive circuits.

- Significantly higher or lower optical powers: designing for a specific range (e.g. based on calculation results) limits the circuit adaptability. Depending on the size of the analyte passing by the detector, the detected light may be an order larger or smaller than the calculated value, requiring wide dynamic range.

- Unavailable photodiode models: the designed photodiodes are a first in this process, and no existing literature reviews their characteristics (e.g. responsitivity, leakage currents or other parameters). Therefore, the detection circuit needs to be as flexible and accommodating as possible.

- Photodiode mode of operation: PV offers low noise operation. PC mode of operation however, theoretically, offers higher quantum efficiencies

(e.g. 9% in Fig. 4.38, due to the larger electric field from the resulting wider depletion region) in exchange for a larger dark current contribution (e.g. 38% - see Fig. 4.39) .

- Noise: 1/f noise dominates at low operating frequencies (Equ. 4.15 and Fig. 4.25).

Based on these requirements, the circuit architecture chosen is illustrated in Fig. 4.21, and is designed using three blocks. The first (pixel) block is responsible for integrating the photodiode photocurrent over time into a voltage then buffering the voltage before it is passed to the next stage. The second stage stores the voltage from two different states, a dark and light state respectively. The third stage subtracts the two (i.e. the dark current contributions from the signal of interest) voltages using the amplifier (illustrated in Fig. 4.23), A1, then stores and holds the final result at the output stage for further processing.

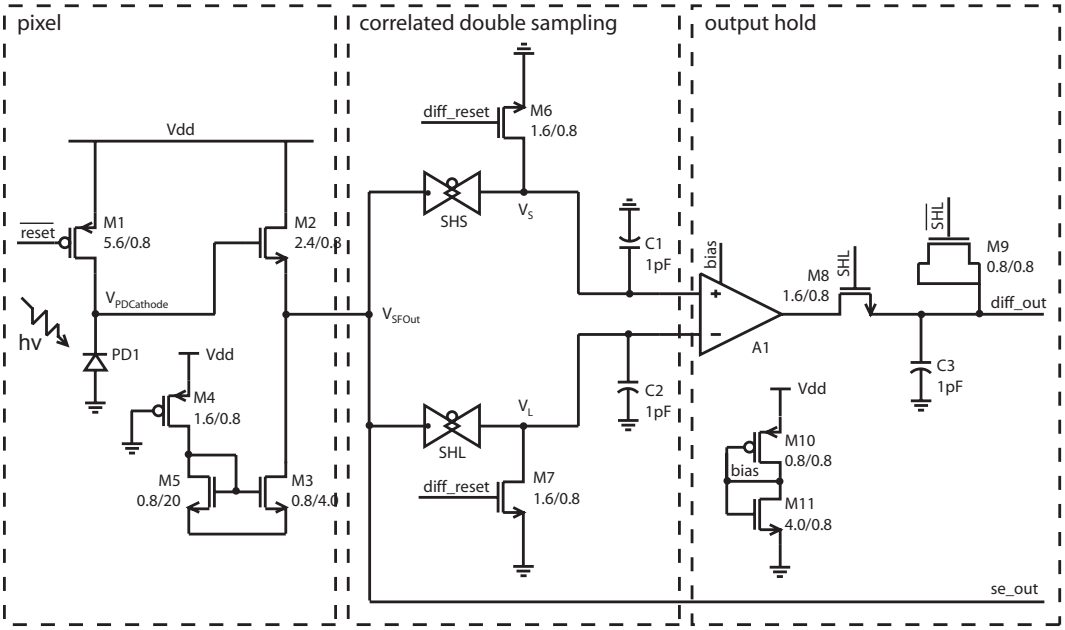

Figure 4.21: Schematic of the three stage optical detection circuit.

The pixel block is composed of three main transistors: a reset (M1), source-follower buffer (M2) and a load transistor (M3), along with support transistors (M4 and M5). On reset, the photodiode voltage is precharged to Vdd by pulsing M1

(designed with a large width). Once reset, as light falls on the photodiode, the $V_{PDCathode}$ node capacitance discharges through the generated photocurrent (leaving the photodiode anode). M2 buffers (with its high input impedance) and "tracks" this discharging node at its output. By ensuring constant current flow through M2 (by limiting the sink capability of M3 with a longer transistor design), the input/output response of the source follower (M2) is made as linear as possible, while ensuring low current draw.

Because the photodiode is operated in PC mode, dark current is a continuously contributing factor (even in the absence of light), discharging $V_{PDCathode}$. Furthermore, ambient background light, present even if there is no fluorescently tagged analyte passing the detector, also acts to skew the measured results. This background ambient light is reduced as much as possible by placing the device in a dark enclosure. By sampling the contributions from the dark current and ambient light sources, and subtracting their combined effect from the actual signal, these additional "noise" sources can be differentially eliminated. This is accomplished by the second (CDS) stage.

Correlated double sampling is a two step operation, first the "dark" (with no excitation source) then the "light" (with emitted light source) value is sampled, then the two are subtracted from each other respectively. This apparently "smart" sampling is possible because the digital control logic for this circuit is also responsible for controlling the excitation light source (e.g., LED or laser).

Referring to the plot in Fig. 4.22, initially with the excitation source on (i.e. LED_Ctrl high), the reset transistor (M1) is pulsed and the "light" current is integrated (through the discharge of $V_{PDCathode}$) over a fixed period of time. At the end of this, the SHS pass-transistor is driven high and the corresponding sampled (V_{SFOut}) value is stored on C1. Directly afterwards, the excitation source turns off, M1 is pulsed, and the "dark" state (with its dark current and ambient light contributions) is integrated for the same amount of time. At the end of this period, the pixel stage output (V_{SFOut}) is sampled by driving SHL high and its value stored on C2. At the same time that SHL is high, M8 in the third stage shunts the differential

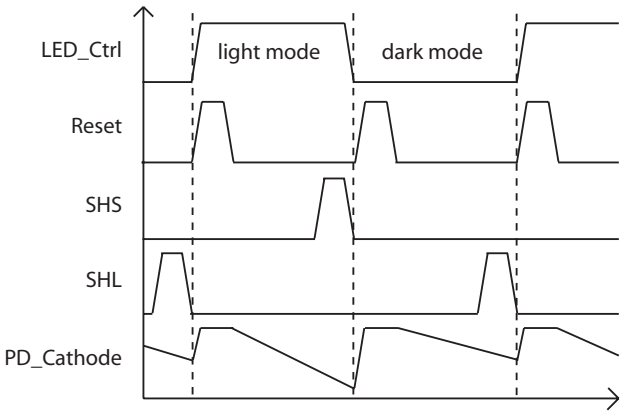

Figure 4.22: Timing diagram for correlated double sampling

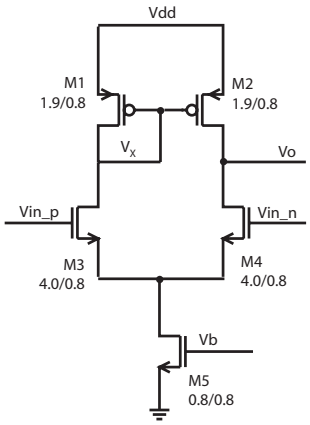

Figure 4.23: Differential amplifier schematic

output of the amplifier to C3 for storage and later processing (e.g. by an ADC).

Additionally, since flicker noise is inversely related to frequency:

$$\overline{V_n^2} = \frac{K}{C_{ox}WL}\frac{1}{f} \tag{4.22}$$

by implementing an integrating transimpedance (versus a non-integrating - high gain) amplifier, we can suppress the effects of flicker noise (Fig. 4.24) by operating at higher frequencies. Using the equation for the 1/f noise corner frequency [13]:

$$f_C = \frac{K}{C_{ox}WL}g_m\frac{3}{8kT} \tag{4.23}$$

we can measure what part of the band is most corrupted by flicker noise and try to remain outside of that range. From Equ. 4.23, with a flicker coefficient for this process of $K = 1.622\,x10^{-}28V^2F$ (determined from the DALSA model files for the kit version cmosp8g V2P5), the corner frequency is calculated to be about 1.43 kHz. Past this point, the flicker noise contribution falls off significantly and the thermal noise determines the noise floor (illustrated in Fig. 4.25). A final design consideration in this circuit is regarding the problem of charge injection and clock feedthrough in the three sampling sub-circuits (i.e. the two pass transistors and M8 along with their associated capacitors).

Charge injection results when the switch turns off, and the charge exiting the collapsing channel (in the inversion layer) is absorbed by the sampling capacitor

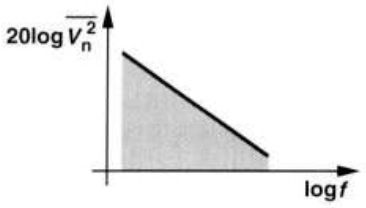

Figure 4.24: The flicker noise spectrum with respect to frequency. [13]

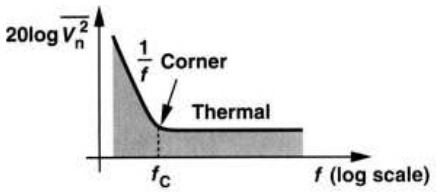

Figure 4.25: Flicker noise reduces below the thermal noise contribution past the corner frequency. [13]

(Fig. 4.26). The total charge in the inversion layer can be expressed by [13]:

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH}) \tag{4.24}$$

This contributes three types of errors on the output voltage, two of which are expressed by [13]:

$$V_{out} = V_{in}\left(1 + \frac{WLC_{ox}}{C_H}\right) - \frac{WLC_{ox}}{C_H}(V_{DD} - V_{TH}) \tag{4.25}$$

where the first term represents a non-unity gain and the second term represents a constant offset voltage. The third error is because of the nonlinear dependence of V_{TH} on V_{in} (body effect) [13].

In the second stage, pass transistors were used because the opposite charge packets injected by the two complementary switches cancel each other out (i.e. when $\Delta q_1 = \Delta q_2$), reducing charge injection. However, this occurs only at one input level (i.e., calculated in this case to be $V_{in} \approx 2.42V$) defined by [13]:

$$W_1L_1C_{ox}(V_{CK} - V_{in} - |V_{THN}|) = W_2L_2C_{ox}(V_{in} - |V_{THP}|) \tag{4.26}$$

The differential nature of the circuit also helps remove the constant offset and lowers the nonlinear component of charge injection [13].

Clock feedthrough introduces an error by coupling the clock transitions to the sampling capacitor through its gate-drain or gate-source overlap capacitance (illustrated in Fig. 4.27). Clock feedthrough error is expressed by the capacitive voltage divider equation given by [13]:

$$\Delta V = V_{CK}\frac{WC_{ov}}{WC_{ov} + C_H} \tag{4.27}$$

and can can be suppressed using a dummy switch with $W_{dummy} = 0.5W_{actual}$ and $L_{dummy} = L_{actual}$ [13]. Furthermore, assuming that half of the charge leaving M8 enters the amplifier and the other half enters the sampling capacitor, C3, the same dummy transistor (as long as it is clocked on the opposite edge) reduces the effects of of charge injection of M8 on C3 by absorbing the injected charge, instead of C3.

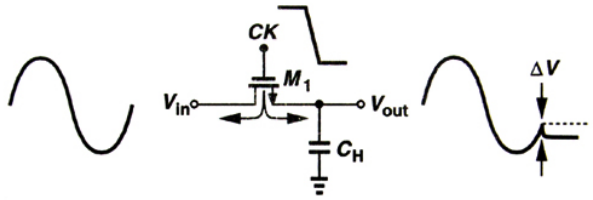

Figure 4.26: Effect of charge injection [13]

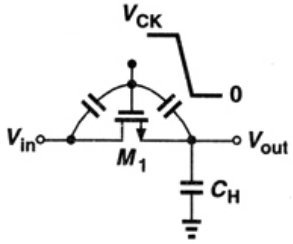

Figure 4.27: Clock feedthrough in a sampling circuit [13]

4.4.4 Photodiode Detection Circuit Simulation Results

This subsection presents the simulation results of the source follower and differential amplifier, and the results of the complete optical detection system under different operating conditions.

From the simulation results of the source follower (Fig. 4.28), it is evident that once M2 turns on ($V_{GS2} > V_{TH2}$), the output response of the source follower is quite linear up to an input voltage of 5 V (with an output of about 3.2 V) due to the constant current through M3. The current through M4/M5 peaks at around 16 μA and the mirrored current (through M3) reaches slightly over 70 μA. However, there is a loss of voltage headroom (i.e. maximum output is around 3.2 V for a 5 V input) because of the buffering of the pixel stage from the CDS stage. Since the current in the "light" mode is simply a superposition of the dark current and current from any additional light sources, the photodiode photocurrent will always be larger in the "light" mode than in the "dark" mode. This higher current translates to a larger discharge of the $V_{PDCathode}$ capacitance and thus a lower voltage at the input of the source follower and hence at the output (than the dark mode). Knowing this, the input to the Vin_p input stage of the amplifier (Fig. 4.23) was chosen to be the lower

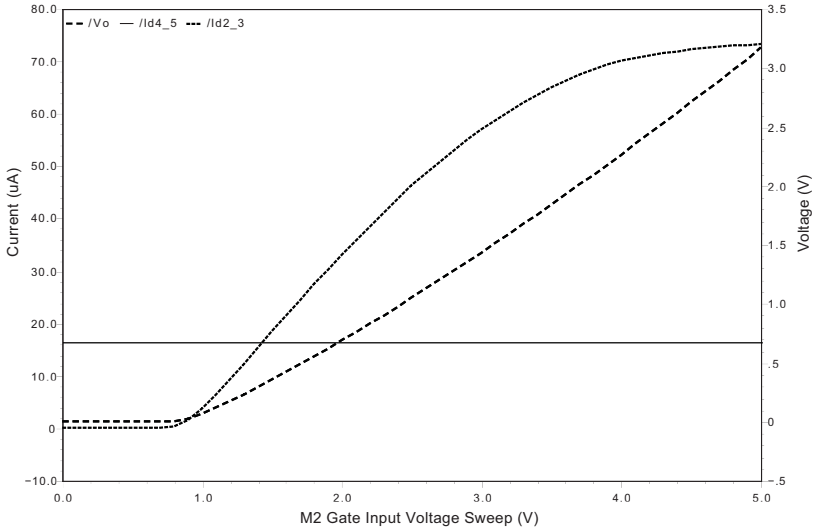

Figure 4.28: Input voltage sweep with output response for M2 (in Fig. 4.21).

("light" mode) voltage and the input to the Vin_n node, the higher ("dark mode") voltage. As illustrated in Fig. 4.31 this generates an exponential behavior for the output voltage (and thus the gain). The benefits of which include:

1. At low currents and small changes (between the "light" and "dark" modes currents), the amplifier exhibits a large gain, but

2. At larger differences in currents, there is a smaller gain, but very linear operation.

Using the Hamamatsu S2387-33R Series photodiode as a reference, with a 5 V reverse bias, the dark current is about 5 pA. At 600 nm, the responsitivity of this photodiode is about 0.35 A/W. With 30.4 pW (calculated earlier) reaching the photodiode, the generated photocurrent is about 10.64 pA. Varying this by a factor of ten times larger or smaller and superimposing this on the dark current, a current range from about 6 pA up to 112 pA is determined. Fig. 4.29 illustrates the response of the circuit to this current range, integrating at 25.2 μs.

In this example, because the integration time is long, the larger currents discharge the PDCathode node more. In the amplifier stages, the large differences between the voltages results in unequal gain (Fig. 4.31). As illustrated by Fig. 4.30,

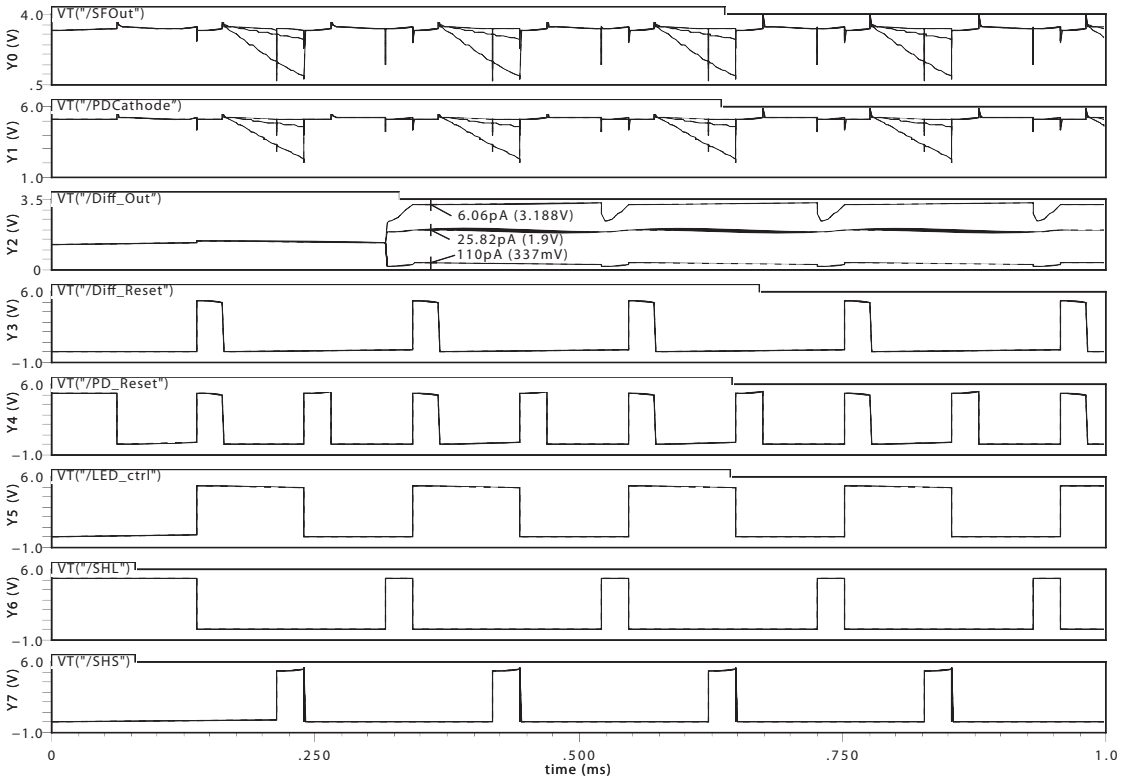

Figure 4.29: TIA response integrating over 25.2 μs for 6.06 pA to 110 pA.

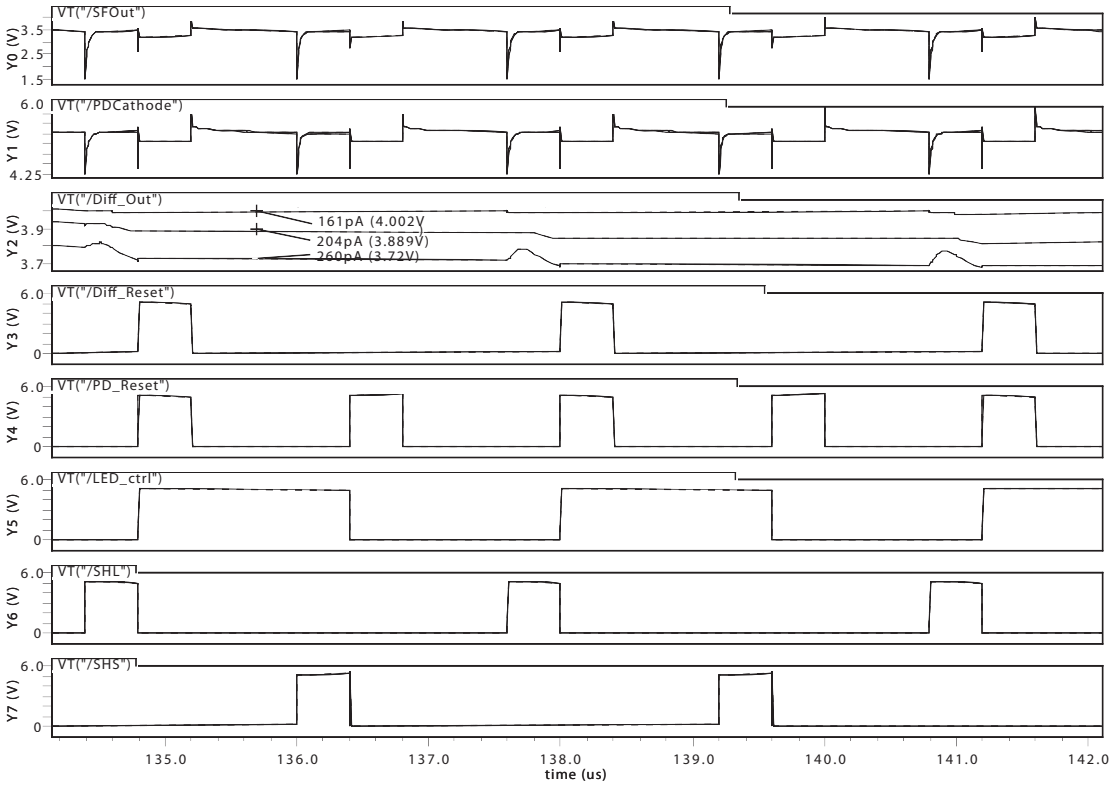

Figure 4.30: TIA response integrating over 0.4 μs for 161 pA to 260 pA.

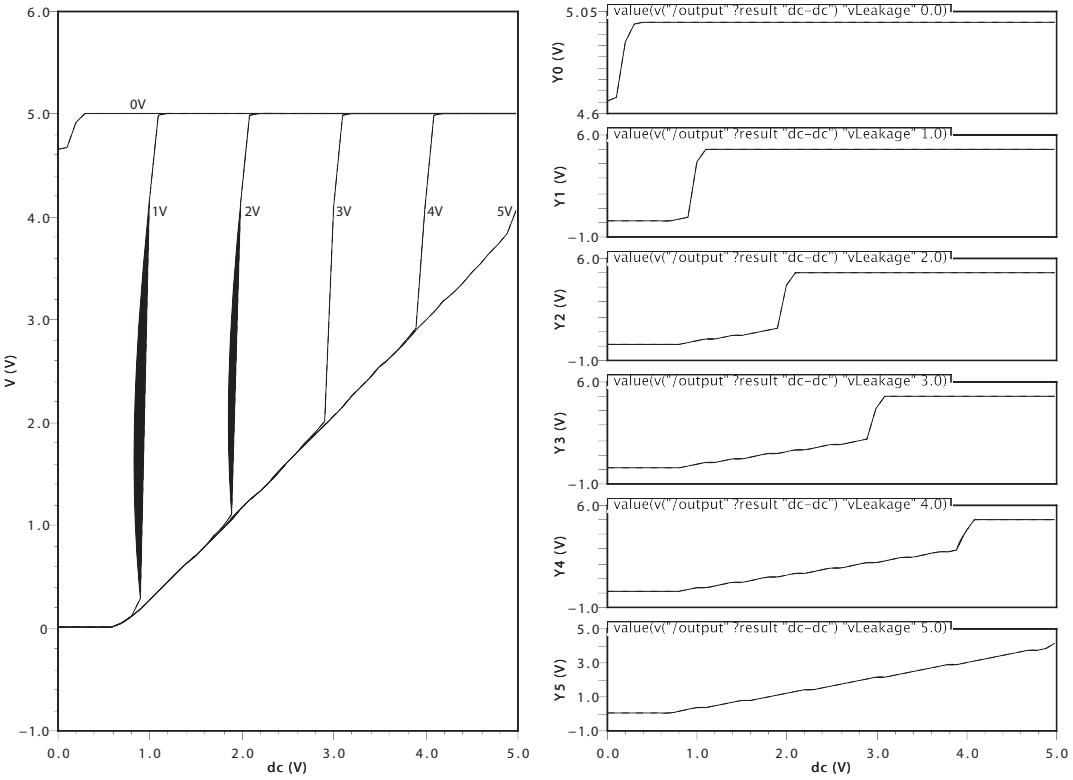

Figure 4.31: Differential amplifier Vin_p sweep for varying Vin_n.

by using a shorter integration time, the resulting closer voltage increments at the source-follower output (SFOut) and higher gain experienced by the amplifier produces more consistent results.

To determine the integrating time for largest gain and to be able to determine which integrating time to use, Fig. 4.32 provides a log-log plot of the gain (V/A) versus the input current from simulation results. Different integration times (with base dark currents) yield different gains, with the lowest currents exhibiting the largest gains because of the larger integration times and because very small incremental changes place the source-follower output voltage in the higher gain region of the amplifier. The operating range for each integration time can also be determined from the figure.

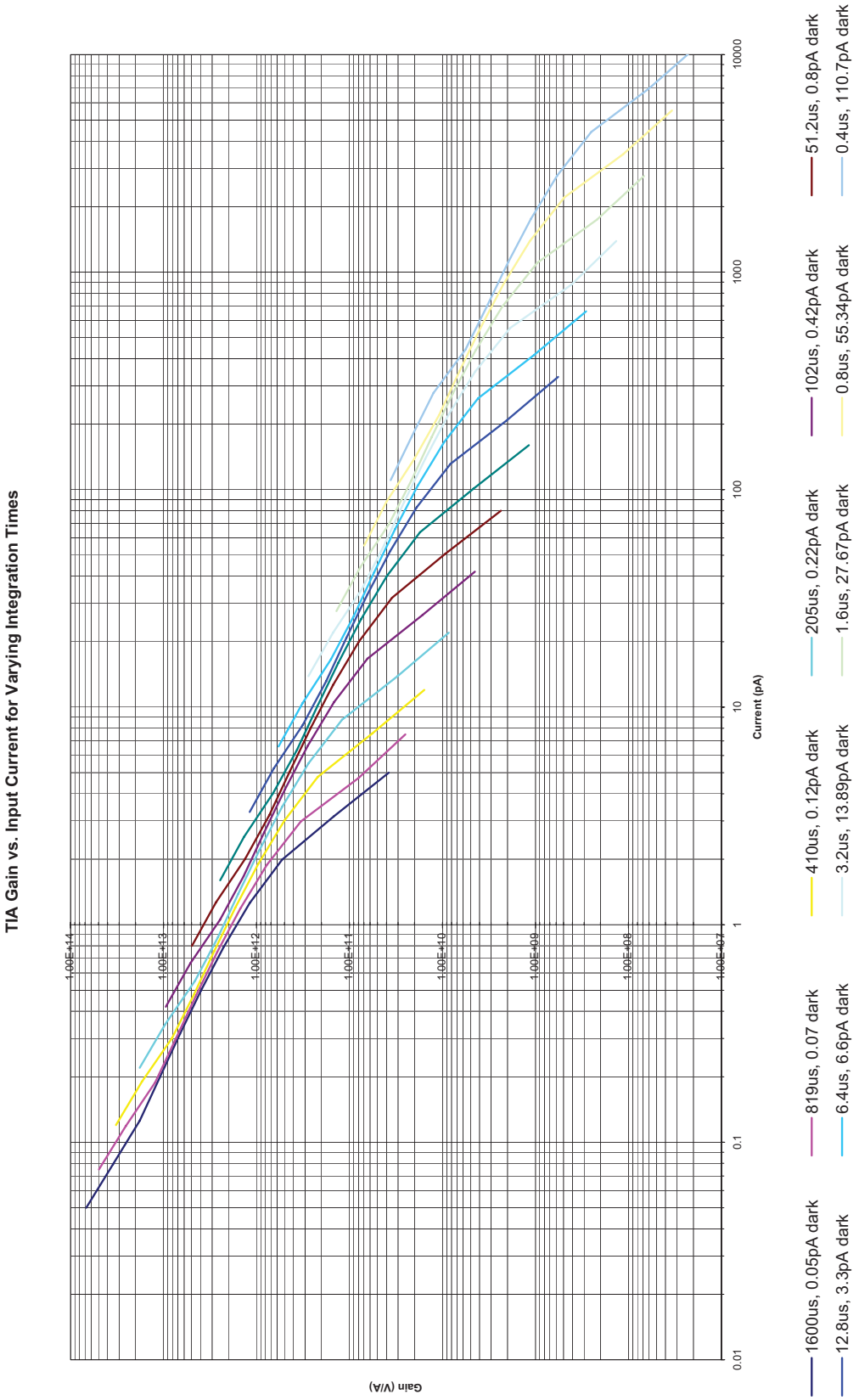

Figure 4.32: Characterization of the gain versus the input current for the TIA.

4.4.5 Avalanche Photodiode Active Quenched Circuit

In this subsection, the design and operation of the active quenched circuit (AQC) for single photon detection is discussed along with simulation results.

For Geiger mode (single photon detection) avalanche photodiode circuits, it is crucial to know what kind of circuit, either an active or passive quenched, to use. Passive quenched circuits offer slower response due to the RC delay from the series resistor and APD capacitance. Therefore, with an expected 30.4 pW of optical power (Φ) arriving at the detector, about 91.8 million photons/sec are calculated to strike the APD (at a wavelength of 600 nm) based on:

$$\text{Number of Photons/sec} = \frac{\Phi\lambda}{hc} \tag{4.28}$$

where h is Planck's constant ($6.626 \times 10^{-34} J \cdot s$) and c is the speed of light. As a result of this high count rate, an active quenched circuit architecture was selected.

To be able to further increase count rate, a smaller (thereby reducing junction capacitance) $50\,\mu$m $\times$ $50\,\mu$m P+/Deep N-Well avalanche photodiode (using the virtual guard ring approach) with an expected breakdown voltage (V_b) of 13 V was designed and used. The junction capacitance (C_d)was calculated to be about 1.7 pA (from the provided diode model file) with a diode (R_d) resistance of about $1.8\,\mu\Omega$.

The designed circuit is illustrated in Fig. 4.33 and consists of a mix of LV digital and HV analog components. The avalanche photodiode model used for simulation is also shown in the same image. The switch (S_1) closes when a photon of light strikes the APD and only opens once the voltage across the APD decreases below its breakdown voltage (V_{bd}).

For single photon (i.e. Geiger mode) detection, the APD is operated at an excess voltage plus the breakdown voltage ($V_e + V_{bd}$). Avalanche breakdown probability increases with increasing excess voltage up to a saturation point, however in most cases an excess voltage of only a few volts is required [48]. Here, an excess voltage of 2 V was selected, yielding a maximum applied voltage of 15 V (to also conjunct with the drain-source breakdown of the PMOS2 used in the circuit).

Because of the high voltage requirements, APD_On is used as on/off logic. With

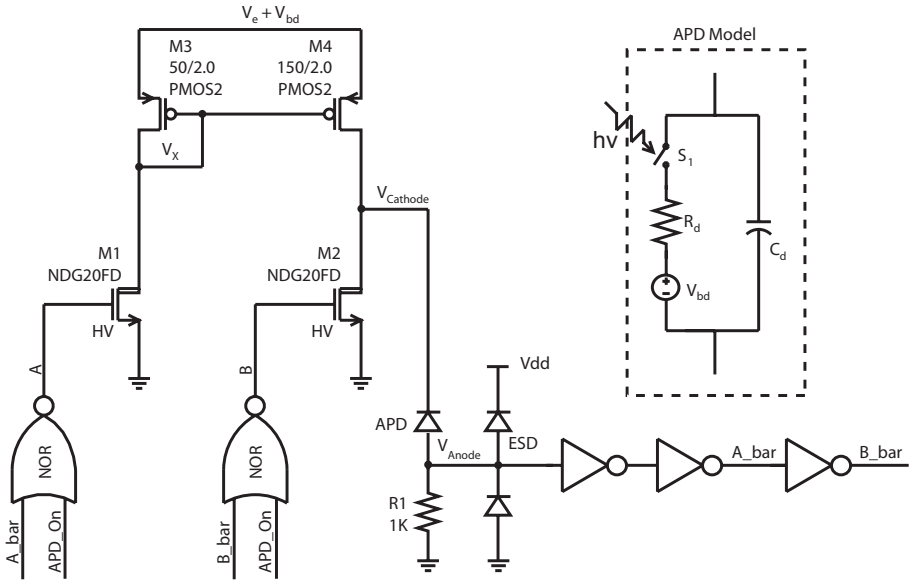

Figure 4.33: Schematic of the APD active quenched circuit and APD model.

APD_On high, both HV LDMOS are off, thus reducing power consumption. In operation, with APD_On driving low, the node A is initially high (and complementary input B is low) since with no photons striking the APD, only a small amount of reverse bias current leaks through the diode, insufficient to pull V_{Anode} high (and A respectively low). This maintains the $V_{Cathode}$ at $V_e + V_{bd}$. Once a photon strikes the APD and avalanche breakdown is triggered, the APD begins to conduct a large amount of current, limited only by amount of current M4 can source (in this case, about 3.5 mA), generating sufficient voltage on R_1 to trigger the series of inverters. This pulse pulls A_Bar high and B_Bar low (and inversely, A low and B high). With M1 off, M4 also turns off, shutting off the supply to the APD. Also, with B high, M2 helps to further drive the $V_{Cathode}$ node low, enabling a rapid quenching of the APD. Once current no longer passes through the APD, A turns on (B off), and with M4 sized with a larger width, the circuit is quickly charged and placed back into its starting state (i.e. APD biased at $V_e + V_{bd}$).

The simulation results are presented in Fig. 4.34 and indicate correct circuit operation to incoming photons (represented by the CLK signal) of light. The dead time is defined as the time during which the APD is not operating in single pho-

ton detection mode (because it is not biased above its breakdown voltage). It is the sum of the quenching plus recharge time (i.e. for the voltage to reach about 99% of the $V_e + V_{bd}$) and it places an upper limit on the operating speeds of the circuit. From simulation, the dead time is measured to be about 10 ns, thus allowing the circuit to operate up to about 100 MHz (meeting the specification of about 91.8 MHz). Finally, this device has been fabricated (ICKAALC4, ICKAATC2) but not yet experimentally verified.

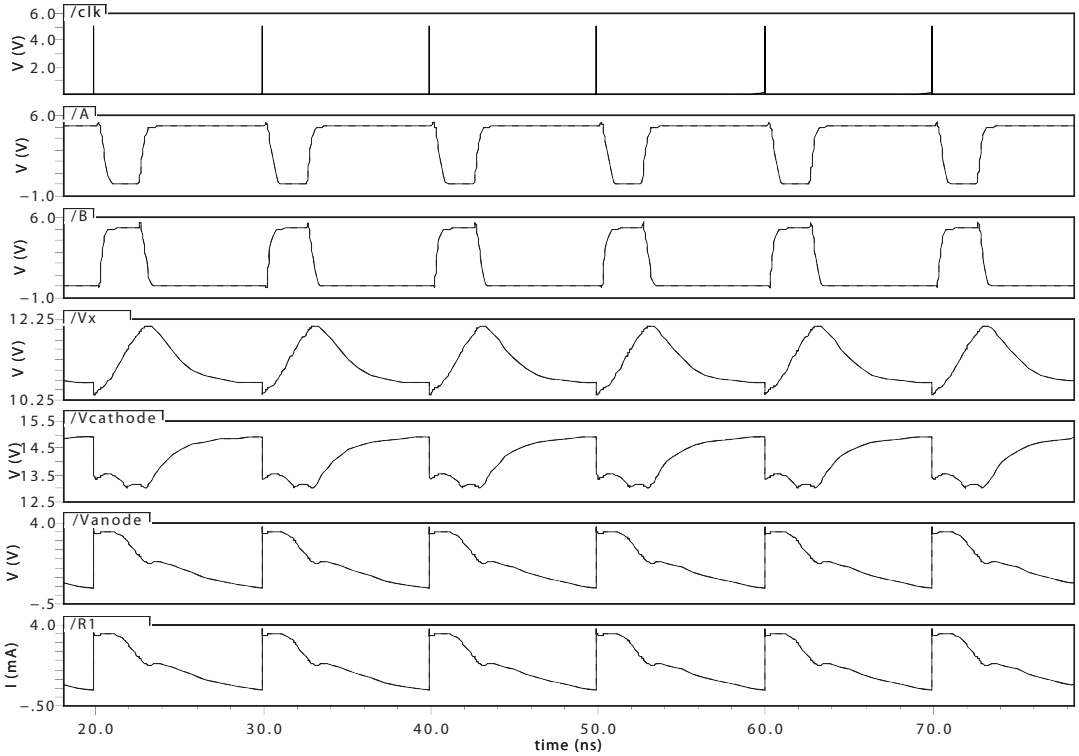

Figure 4.34: Active quenched circuit simulation results.

4.5 Measured Results

In this chapter, measurement and operation results of fabricated devices are analyzed and introduced. The photodiode structures are examined to determine their value as low light and efficient optical detectors followed by a discussion on the presence of parasitic bipolar phototransistors. Finally, the successful operation and low light detection of the first generation transimpedance amplifier coupled with an on-chip photodiode and off-chip ADC is presented.

4.5.1 Photodiodes

Two setups (Fig. 4.35 and 4.36 respectively) were used to characterize the photodiodes, one local at the University of Alberta (System 2 - S2), and the other more complete setup at the University of Sherbrooke (System 1 - S1).

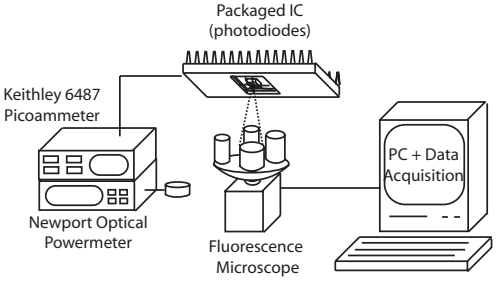

Figure 4.35: Photodiode characterization setup at the University of Alberta.

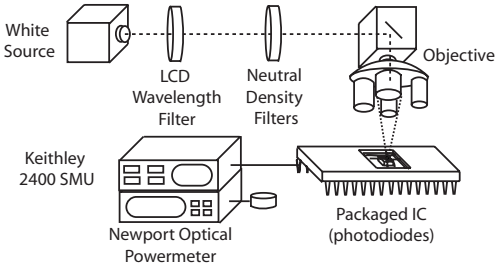

Figure 4.36: Photodiode characterization setup at the University of Sherbrooke.

In the University of Alberta setup, an Axiovert 200M Fluorescence Microscope was used to focus the light of a mercury lamp through varying filter cubes to generate three distinct wavelengths of light, 460 nm, 550 nm and 600 nm. At the highest power objective (63X), the focused spot encompassed the entire photodiode (an area of about 0.0225 mm^2). The Newport 1930F Power Meter was first used to measure the optical power for this spot size, then the different photodiodes were placed under the microscope objective with varying optical intensities and wavelengths, and the photocurrent was measured with the Keithley 6487 Picoammeter.

In the setup at the University of Sherbrooke, a white light source was first passed through a LCD variable wavelength filter (adjustable from 400 nm to 700 nm) then passed through different neutral density filters to vary the attenuation. This light was then focused through a microscope objective to about 80 % of the photodiode active area. Again, a newport optical power meter was used to measure the incident optical power before the photodiode was placed. Once the optical power was measured, the photodiode was placed and the generated photocurrent was measured with a Keithley 2400 SMU to determine the responsitivity (Amperes/Watt). Using this information, the quantum efficiency for the different photodiodes was calculated.(Fig. 4.37).

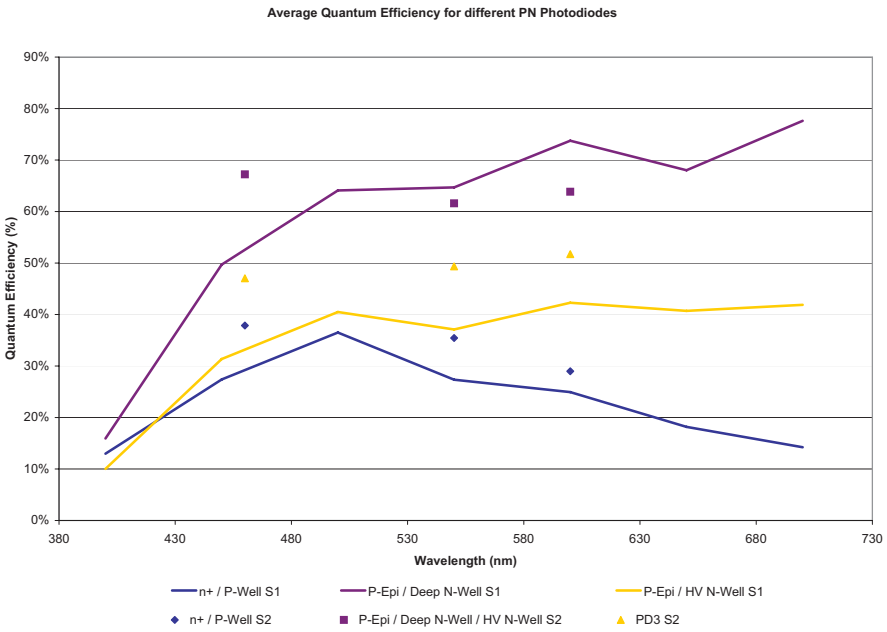

Figure 4.37: Quantum efficiency measurements for three different photodiode configurations under two different setups (S1 and S2).

The varying quantum efficiencies between the three different photodiodes is explained by the penetration depth of light in silicon. Referring to Fig. 4.5, the longest wavelength of light penetrates more to the deepest junction depth. Thus, the P-Epi/Deep N-Well photodiode, with the deepest (about 6.0 μm) depletion region, has the highest QE at the higher wavelengths. The P-Epi/HV N-Well photodiode, which has the next deepest (about 4.5 μm) depletion region has the second highest QE at the higher wavelengths. Finally, the n+/P-Well photodiode, which has the shallowest junction (at about 0.3 μm), respectively also has the lowest QE at the higher wavelengths. Because of electron-hole pair generation at the surface, the lower wavelengths still contribute to the photocurrent. Clearly then, for our fluorescence detection application, with an emission wavelengths of about 600 nm, the deeper junction depth photodiodes provide better response in the region of interest, and conveniently help attenuate the shorter wavelength (excitation) light. One explanation behind the ripple behavior is interference effects (interaction between incident light waves) resulting from the passivation layer (Fig. 4.2). Difference

between results from S1 and S2 can be due to choice and selectivity of filters used.

As expressed earlier, QE can also be enhanced in photoconductive mode under the application of a reverse bias. This improvement (about 9%) for the n+/P-Well photodiode is illustrated in Fig. 4.38 and is because the reverse bias voltage (moderately) improves collection efficiency through the higher electric fields and wider depletion region.

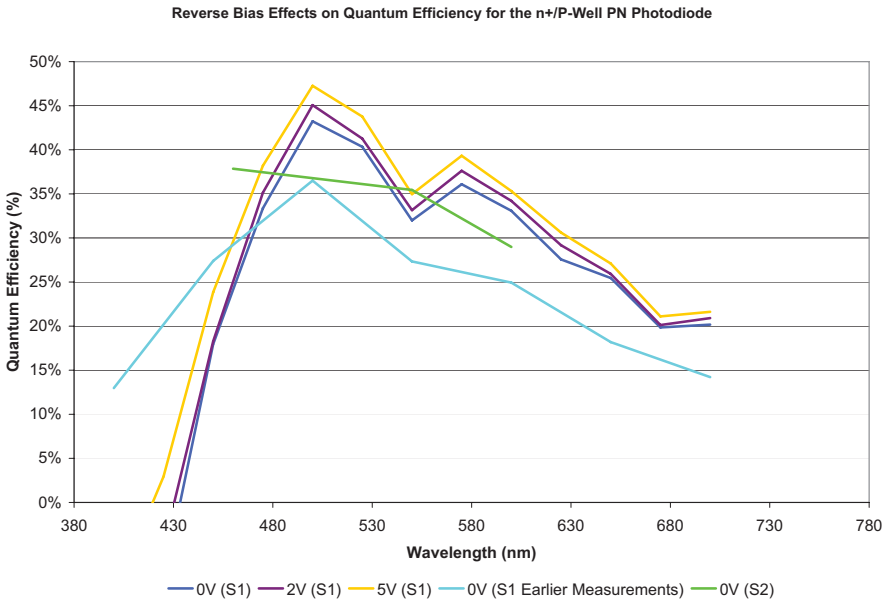

Figure 4.38: Effects of reverse bias on quantum efficiency.

For such low light conditions, the NEP for the different photodiodes was then calculated based on measurements of dark current and shunt resistance. In Fig. 4.39, the dark current (per unit area) of four designed photodiodes is measured with respect to the reverse bias voltage. As expected, the dark current increases with an increase in reverse bias (V_{rb}). This is expressed through:

$$I_{dark} = I_S[e^{(\frac{qV_{rb}}{nkT})} - 1] \tag{4.29}$$

By sampling dark current, it can be subtracted from the signal of interest, however its shot noise contribution cannot be directly reduced (i.e. Equ. 4.14).

The thermal noise contribution stems from the shunt resistance of the photodiode (Equ. 4.13) and KT/C noise of every circuit node that follows. The calculated

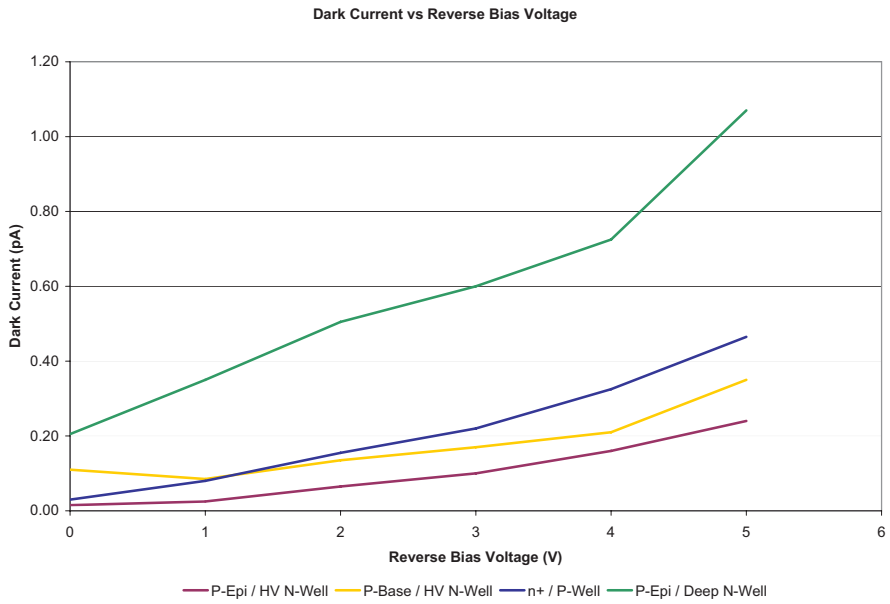

Figure 4.39: Photodiode dark current dependance on reverse bias voltage.

shunt resistance is provided in Table 4.2 and is determined by calculating the change in voltage with respect to the change in current from a -10 mV to 10 mV sweep of the photodiodes (illustrated in Fig. 4.40).

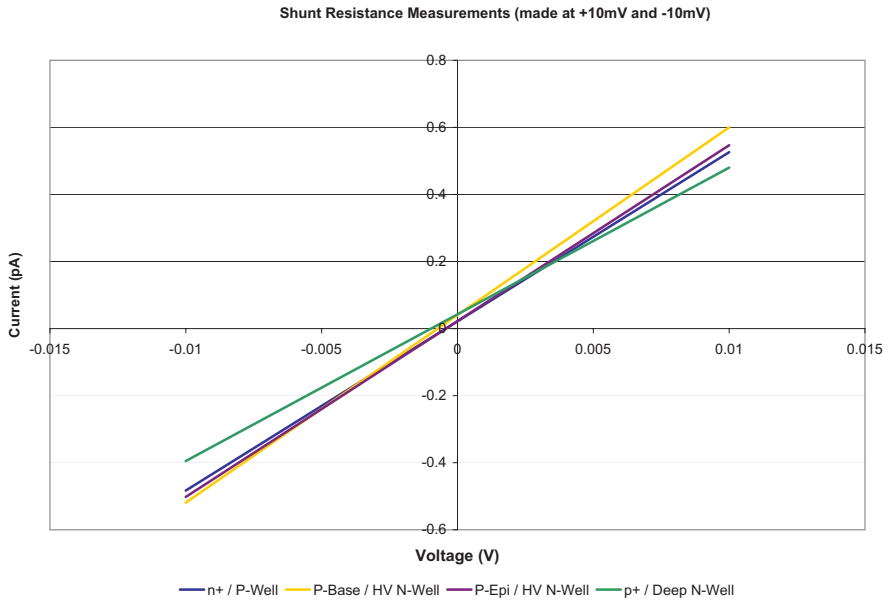

Figure 4.40: Results from shunt resistance measurements.

Table 4.2: Shunt resistance for 4 different (150 μm $\times$ 150 μm) photodiodes

Photodiode Configuration	Shunt Resistance (GΩ)
n+/P-Well	19.82
P-Base/HV N-Well	17.87
P-Epi/HV N-Well	19.07
P-Epi/Deep N-Well	22.86

From the dark current and shunt resistance measurements, the lower limit of detection with varying amounts of optical power (which contribute different amounts of shot noise) is calculated and illustrated in Fig. 4.41. Assuming 30.4 pW of optical power arriving at the detector, at a wavelength of 600 nm, and operating at 1 kHz, the lowest optical power that is detectable by the photodiode (i.e. for a SNR of 1 where the generated photocurrent equals the photodiode noise currents) is calculated (from Equ. 4.16) to be about 7.41 fW.

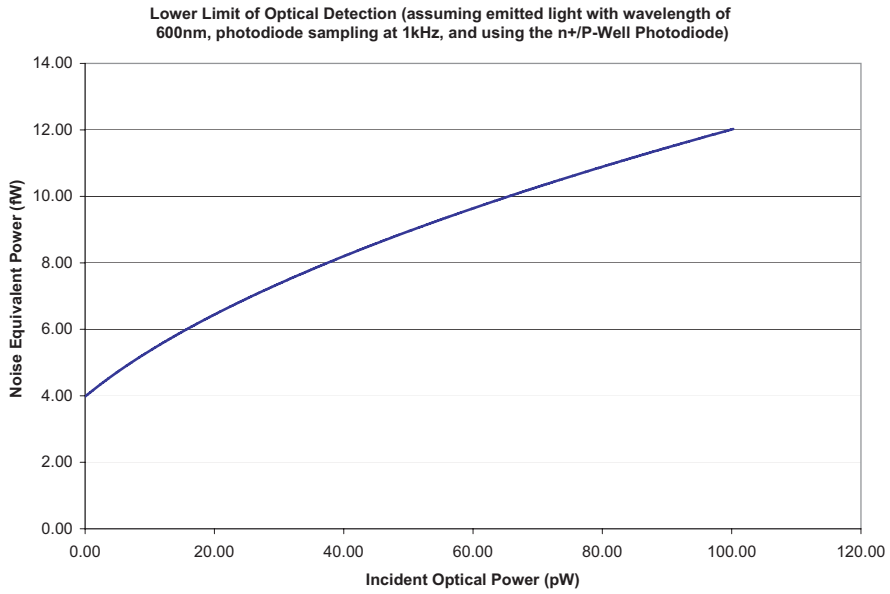

Figure 4.41: Optical power resolvable by the photodiode given noise contributions from incident light (e.g. shot noise).

4.5.2 Phototransistor

Photodiodes, though sensitive and capable of providing linear characteristics, lack internal gain. In very low light applications where the amplifier circuit noise itself is greater than that generated by the photodiode, detection is problematic. In such situations,there is often a transition towards avalanche photodiodes due to their internal gain. However, phototransistors, devices that take advantage of bipolar structures available in CMOS processes, can be used instead to form photodiodes with internal gain [56]. Though this process supports bipolar transistors and the possibility of phototransistors, none had been intentionally designed. However, several parasitic phototransistors where found during testing of the fabricated photodiodes.

Fig. 4.42 highlights several bipolar phototransistors (both PNP and NPN as fabricated in ICKAALC2) found surrounding two of the designed photodiodes. Though both (PNP or NPN) phototransistors can be analyzed, for simplicity sake, the PNP photodiode is examined.

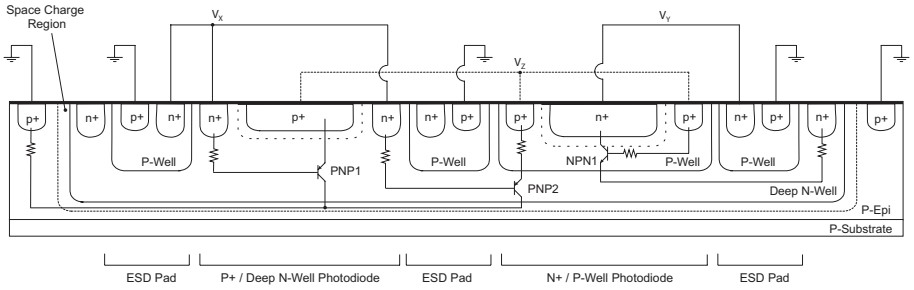

Figure 4.42: Parasitic bipolar phototransistors surrounding designed photodiodes.

There are two PNP phototransistors illustrated, both with a P-Epi collector and Deep N-Well base, however one with a p+ diffusion and the other with a P-Well emitter. The excellent performance of the devices stems from the high gain possible when operated in the active mode of operation whereby the photocurrent (the base current) is amplified by the transistors short circuit current gain factor (β):

$$I_{collector} = \beta I_{ph} \tag{4.30}$$

To this end, the collector is maintained at the lowest potential (ensuring the collector-base junction is reverse biased), the highest potential is applied to the

emitter (forward biasing the emitter-base junction) and the base can be left floating. Under an applied bias and illumination, electron-hole pairs are generated in or near the space charge region (the collector-base interface). The electrons from the photogenerated carriers within a diffusion length or those in this space charge region are collected into it. These electrons are then swept towards the emitter-base junction by its (depletion region) electric field, defining the base (photo) current.

Furthermore, by properly biasing the base, higher gain is possible. Fig. 4.43 illustrates measurements of the gain characteristics of the P-Well PNP parasitic bipolar device with varying base voltage. Fig. 4.44 illustrates the collector current with respect to varying base current.

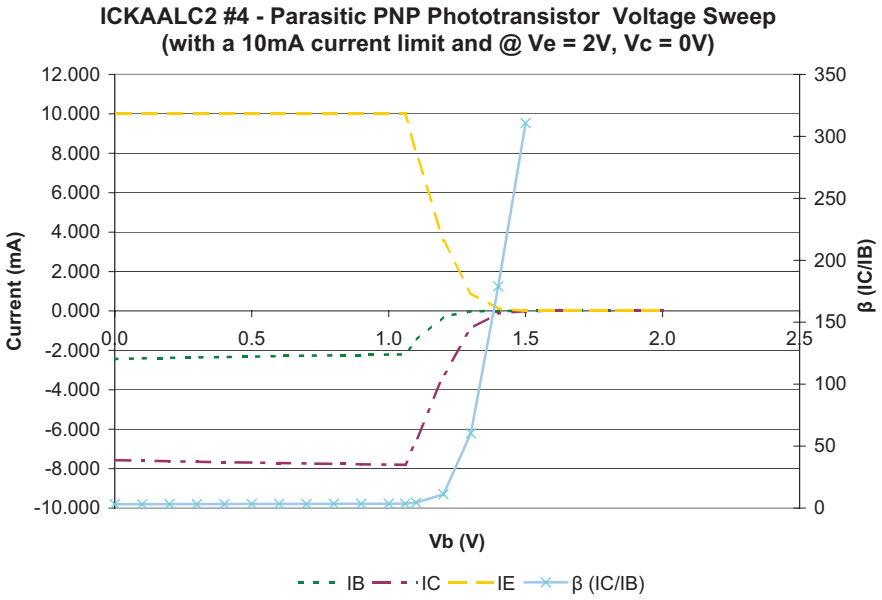

Figure 4.43: Measured gain of the P-Well PNP phototransistor (at $V_{CE} = -2\,V$)).

It is important to note that the p+ diffusion of both photodiode structures is connected in the fabricated design (Fig. 4.42), therefore, it is difficult to ascertain which of the two emitter junctions is the active one. However, the P-Well to Deep N-Well diode has a lower turn-on voltage than the p+ diffusion to Deep N-Well (0.61 V versus 0.73 V respectively), thus we assumed that the emitter region of the characterized PNP bipolar device is the P-Well. This has been verified by using a focused 150 μm $\times$ 150 μm source of light over both, and measuring significantly higher cur-

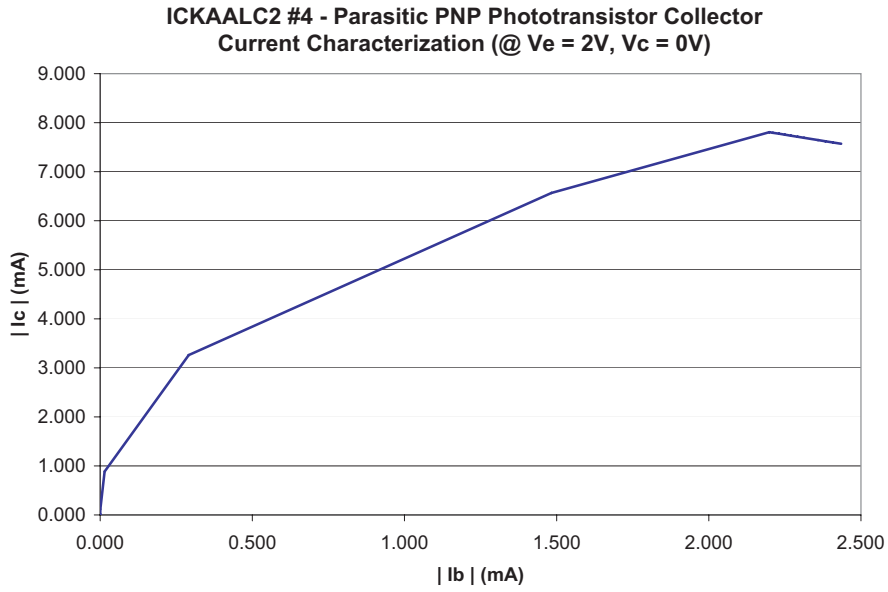

Figure 4.44: Measured I_C with respect to varying I_B (at $V_{CE} = -2\,V$).

rents from the P-Well rather than the p+ diffusion device. Time not permitting, further characterization is left for future investigation.

4.5.3 Transimpedance Amplifier

The photodetector is only one essential component of the entire optical detection system. The transimpedance amplifier stage connected to the detector is just as important as it is responsible for the amplification of the generated photocurrent and its accurate and sensitive current to voltage conversion.

The first transimpedance amplifier designed and fabricated in this process is illustrated in Fig.4.45. The circuit consists of an n+/P-Well photodiode with its anode connected to ground, reset transistor (M1), and a common-source stage. In this circuit, because the anode is directly connect to ground, the photodiode cannot be operated in photovoltaic mode (as the generated photocurrent leaves the diode anode, discharging directly to ground). The photodiode is configured instead for photoconductive mode.

To reduce pin count, the photodiode reset voltage and the gate bias voltage of the common-source PMOS (M2) were connected together (V_b). From simulations,

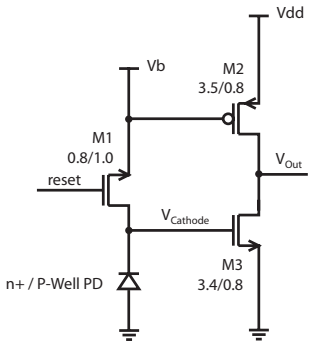

Figure 4.45: Basic transimpedance amplifier circuit with photodiode (ICKAALC3/TC1).

to provide high gain, linear operation and a wide output range, 2 V was selected for the bias voltage. This voltage was verified in the fabriated device through input voltage ($V_{Cathode}$) sweeps of the transimpedance amplifier at different bias voltages. The simulation and measured results (for three separate chips biased at 2 V) is given in Fig. 4.46. It is important to note that the 2 V not only biases the common source load, but is also the voltage at which the photodiode is (reverse) biased at.

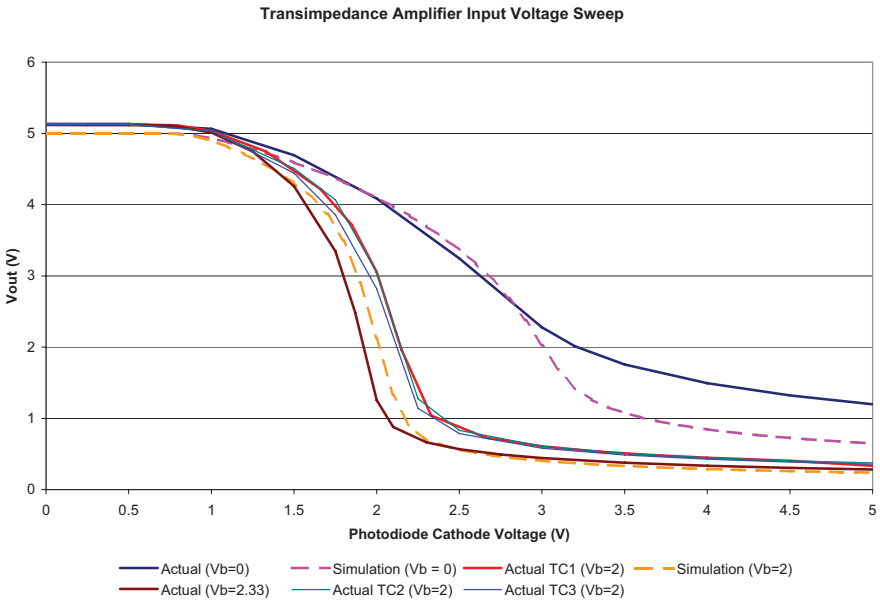

Figure 4.46: Simulation and measured input-output characteristics of the transimpedance amplifier.

From simulation, the capacitance at the $V_{Cathode}$ node is about 4.28 pF (mostly as a result of the photodiode junction capacitance). Using this capacitance, the measured transimpedance amplifier input/output voltage results (Fig. 4.46) and the responsitivity of the photodiode, the response of the circuit to varying amounts of optical power can be estimated. Based on the information in Table 4.3, the transimpedance response with respect to input optical power was calculated. This was compared with the response of the actual circuit.

Table 4.3: Parameters for estimating transimpedance amplifier response

Parameters	Value	Units
Reverse Bias	5	V
Dark Current	0.35	pA
Integration Frequency	1.11	Hz
Input Node Capacitance	4.29	pF
Responsitivity (@600 nm)	0.16	A/W

The actual circuit was tested by applying an increasing ramp function (up to 5 V) to an LED which was used to excite the photodiode. The response of the transimpedance amplifier to the generated photocurrent was then collected using an 8-bit ADC on a PIC 16F877 Microcontroller. A Newport 1930F Single-Channel Power Meters was used to measure the optical power at the varying LED intensities. The actual versus estimated response of the transimpedance amplifier to varying optical power is illustrated in Fig. 4.47. To ensure sufficient resolution between peaks in an electropherogram, a minimum 1 Hz sampling frequency is used. To ensure maximum integration in the transimpedance amplifier, the 1 Hz minimum was used. However, because the transimpedance amplifier reset frequency was 1 Hz at a duty cycle of 10% (i.e. reset every 0.10 s and integrate over 0.90 s), the integration frequency stated is 1.11 Hz.

Because the TIA characterized was on the test chip (ICKAATC1), and the amplifier with integrated photodiode was on a system chip (ICKAALC3), the input/output voltage sweep presented in Fig. 4.46 is not exactly representative of what might be seen on another die. Process variations can easily shift the input/output response of this amplifier (as visible by the simulated vs. actual response in Fig. 4.46).

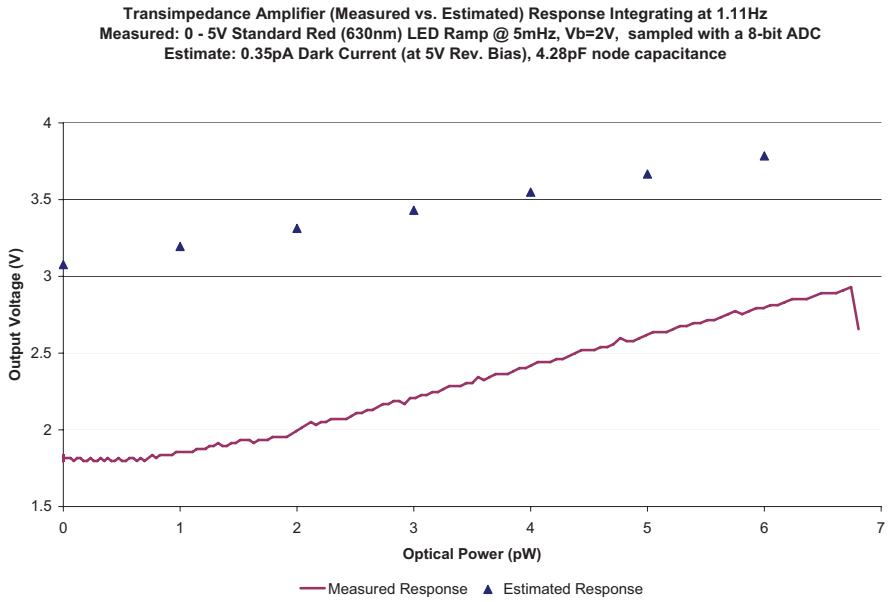

Figure 4.47: Estimated and measured response of the fabricated transimpedance amplifier to varying optical power intensities.

The resolution possible in such a configuration is heavily dependent on the NEP of the photodiode and the resolution of the analog-to-digital converter. The smallest change in optical power ($\Delta\Phi$) that can be detected using the 8-bit ADC can then be determined using Equ. 4.31:

$$\Delta\Phi = \left(Q_{input} - \frac{\Delta V_{output} + Q_{output} - b}{m} \right) \frac{C}{TR} \tag{4.31}$$

In this equation, the input and output bias points of the transimpedance amplifier along with its slope and intercept at this point is given by Q_{input}, Q_{output}, m and b respectively. For an 8-bit ADC with a 5 V reference, the smallest change in output voltage (ΔV_{output}) that is detectable is 0.0195 V (i.e. $5/2^8$). Again, using the parameters in Table 4.3, the smallest change in optical power that is detectable is about 0.17 pW. The analog-to-digital converter can only be increased up to about 12 to 13-bits. Past this point, the NEP of the photodiode (about 7 fW) is reached and the photodiode itself is not sensitive enough to detect changes in optical power (that is, if the noise of the amplifier does not drown out the signal). The relationship between lowest optical power detectable and the ADC resolution is illustrated in Fig. 4.48.

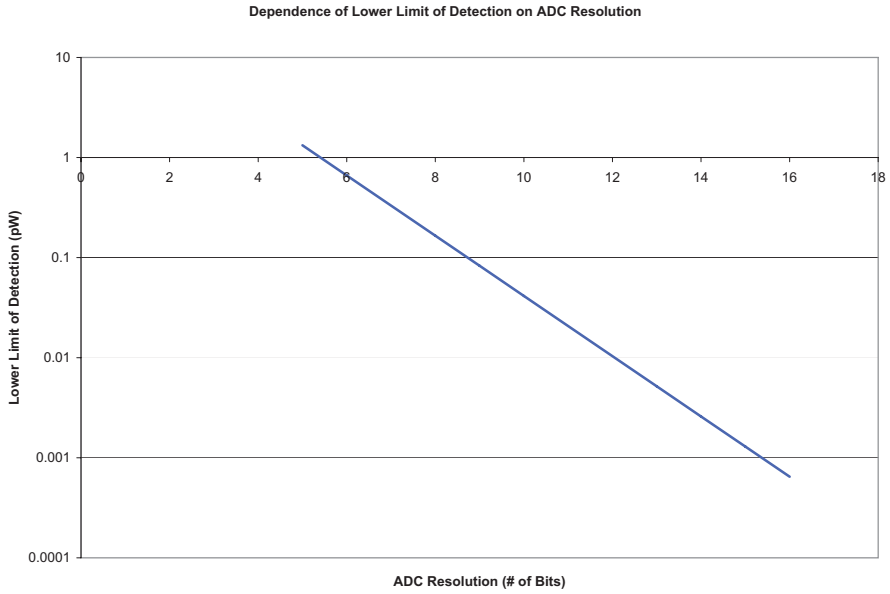

Figure 4.48: Lower limits of detection with different resolution ADC's for the previously discussed transimpedance amplifier.

4.6 Conclusion

Integration of sensitive optical detectors and associated circuitry for microfluidic LOC devices is the precursor to the successful development of miniaturized genetic testing and portable point-of-care diagnostic systems. We have designed, fabricated and tested our own custom photodiode, avalanche photodiode and phototransistor detectors. Extrapolating from experimental measurements, we have demonstrated that our integrating transimpedance amplifier plus photodiode circuit is capable of very low light detection (< 0.1 pW) using ADCs with sufficient ($>$ 8-bit) resolution.

Our optical detection system has the advantage of being integratable with additional HV CMOS compatible components like high-voltage switching and generation and low-voltage analog-to-digital converters, logic and communication circuitry. When combined, an integrated, cost-effective and mass production ready solution is possible. Future work will involve further exploring the use and benefits of avalanche photodiode and phototransistors over conventional photodiodes as detectors and the optimization of the optical detection system.

Chapter 5

Analog-to-Digital Converter

In this section, the requirements for the implemented analog-to-digital converter are first discussed, followed by background on analog-to-digital converters and methods of characterizing them. The following section presents the design, operation and simulation results of the converter and the final section presents the measured performance metrics and analysis of the fabricated device.

5.1 Motivation

While outputs of components like the active quenched APD circuit are already digital and can be directly read out, there are many components in the complete system that require analog-to-digital conversion. These include the photodiode transimpedance amplifier voltage, on-chip current and voltage monitors and potentially even voltages supplied from off-chip that need to be quantized. To accomplish the task of analog-to-digital conversion, two generations of successive approximation analog-to-digital converters were designed and fabricated, an 8-bit (in chip ICKAALC3) and a 12-bit (in chip ICKAALC4), both based around the same platform. However, as multiple design errors were found in the 12-bit ADC, the scope of this thesis only covers the 8-bit variant.

5.2 Requirements

The requirements of the analog-to-digital converter (ADC) are heavily dependent on the specific application. The first generation ADC was designed to sample the voltage outputs of 3 different components, each with its own specifications:

- Transimpedance amplifier: From the simulated input/output relationship of the transimpedance amplifier (biased at Vb = 2 V), an output voltage range from about 2 V to 3 V was expected.

- High-voltage reference monitor: A voltage-divider is used to monitor the high-voltage supply (applied to or generated) in the system by dividing down the voltage to 1 % of its value. The maximum expected supply voltage is 300 V and the minimum is expected to be about 100 V, therefore, establishing an operating range from 1 V to 3 V.

- High-voltage output current monitor: This component measures the current passing through high-voltage output level-shifters. From simulation results, connecting this current to an external (70 kΩ) pull-up resistor biased at 5 V, a current range of 0 - 60 μA can be monitored by measuring a 5 V to 1 V voltage range (respectively).

For the current monitor, 1 μA resolution can be achieved using a 6-bit ADC. For the voltage monitor, an 8-bit ADC with a 5 V reference rail (and 0 - 5 V input range) would be able to resolve 1.95 V changes for the high-voltage (e.g. up to 300 V) supply. Finally, for the previously discussed transimpedance amplifier (Section 4.5.3), using Equ. 4.31, we can determine the different lower limits of detection possible with different resolution ADC's. This is illustrated in Fig. 4.48. From this, an 8-bit ADC provides a resolution of about 0.17 pW and a 12-bit ADC achieves resolution of about 0.01 pW. Finally, to ensure the ADC is synchronized with the bit readout of the serial peripheral interface (SPI), the ADC must be able to operate up to the 5 MHz clock frequency of the SPI.

5.3 Background

Analog-to-digital (ADC) converters and digital-to-analog (DAC) are essential components that provide the interface between the analog and digital world (and vice versa). The first and second subsections below, respectively, will provide background information on DACs and ADCs.

5.3.1 Digital-to-Analog Converters

The output voltage (V_O) of a digital-to-analog converter can be expressed as:

$$V_O = V_{REF} \sum_{i=1}^{N} \frac{b_i}{2^i} \tag{5.1}$$

where b_i represents the ith coefficient and is either 0 or 1, N is the total number of bits in the digital word (i.e. the resolution of the ADC) and V_{REF} is the reference voltage. This is illustrated in Fig. 5.1.

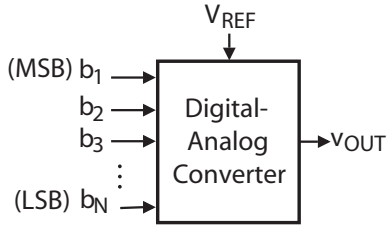

Figure 5.1: Digital-to-analog converter.

As per Fig. 5.2, each digital word of an N-bit DAC has its own unique output voltage, the difference in levels is called the LSB and its value is defined as:

$$LSB = \frac{V_{REF}}{2^N} \tag{5.2}$$

For a DAC with finite resolution, its maximum analog output does not equal V_{REF}, rather the maximum output achievable, called the full scale voltage, is given by:

$$V_{FS} = V_{REF} - LSB = V_{REF}\left(1 - \frac{1}{2^N}\right) \tag{5.3}$$

The fundamental uncertainty in finite precision DACs is called quantization noise, and is represented by the difference between the analog output of an infinite-bit

DAC and the analog output of a finite-bit DAC (Fig. 5.2). The maximum error possible is 1 LSB, but by introducing a vertical shift in the DAC output, an error range of ± 0.5 LSB can be achieved. As the magnitude of the error cannot be reduced below the quantization noise, the accuracy (i.e. the comparison between the actual output and the expected output) is also limited to at most ± 0.5 LSB. The accuracy however can be improved by increasing the resolution (and inversely reducing the quantization noise).

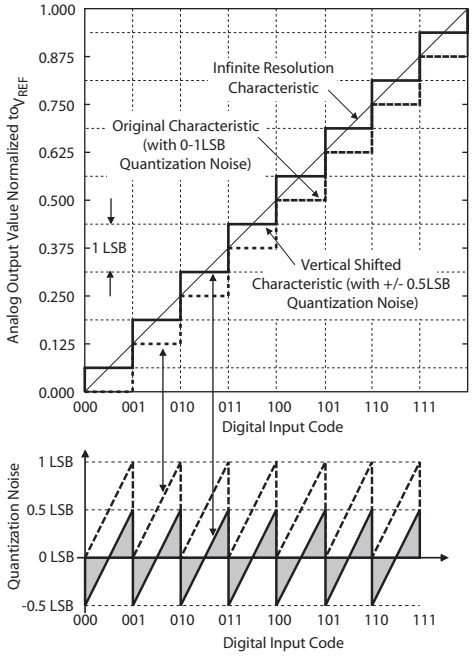

Figure 5.2: Ideal input-output characteristic of a 3-bit DAC [14].

5.3.2 Analog-to-Digital Converters

Analog-to-digital converters convert an analog voltage (with typical values between 0 V and V_{REF}) to a digital code (most often represented by a binary sequence of N-bits). The N-bit sequence (i.e. the resolution) represents how finely an analog voltage can be represented and the accuracy conveys how much of that measurement actually has value. Similar to DACs, the lower limit placed on the accuracy is again limited by the quantization noise and in the ideal case is ± 0.5 LSB.

5.3.3 ADC Architectures

Depending on the specific requirement, there are several different ADC architectures that can be used. Briefly, four of the more commonly used architectures are presented, along with their advantages and disadvantages.

5.3.3.1 Flash

The highest speed analog-to-digital converter is the flash (a.k.a. parallel) analog to digital converter [14]. As illustrated in Fig. 5.3, this architecture uses 2^{N-1} comparators to convert an analog voltage to an N-bit digital value in a single clock cycle. While conversion time remains fixed with an increase in resolution, the number of comparators increases at an exponential rate, and thus with it, so does the die size and power consumption. Additionally, it is difficult to increase the resolution past 8-bits due to limitations placed by component mismatch [57].

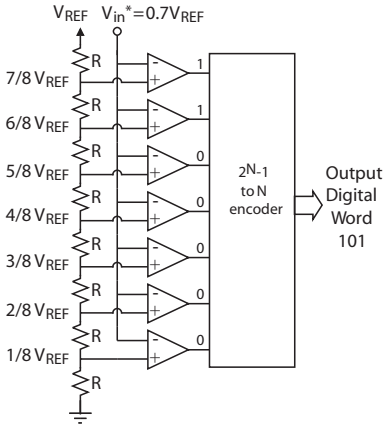

Figure 5.3: A 3-bit flash ADC [14].

5.3.3.2 SAR

Often used in medium to high resolution (8 to 16-bit) and lower speed systems, an N-bit SAR ADC uses a binary search algorithm to sequentially converge to a digital representation of the analog voltage in N-cycles. SAR ADCs (illustrated in Fig. 5.4) consist of three main components: a digital successive-approximation register (SAR), a comparator and a DAC and lend themselves to small areas and low

power consumption. Area, power consumption and conversion time all increase linearly with resolution. However, due to the settling time constraints placed by the DAC and higher frequency requirement of the clock, such architectures generally operate at lower speeds.

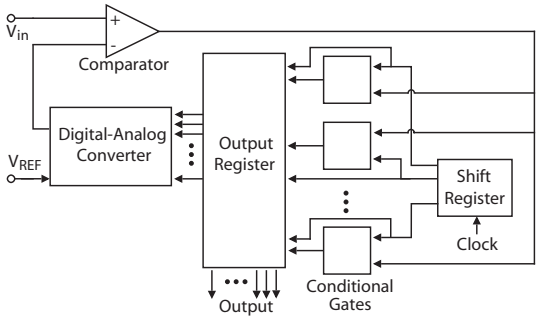

Figure 5.4: Architecture of a SAR ADC [14].

5.3.3.3 Pipelined

For high sampling rates and medium to high (8 to 16-bit) resolution, pipelined ADC architectures present excellent performance. By using multiple stages of lower resolution ADCs and DACs (Fig. 5.5), the analog voltage is resolved into a digital bit sequence from the most significant to the least significant bit (LSB). Both area and conversion time increase linearly and throughput is increased at the expense of latency because of its fundamental multi-stage pipelined structure. Though power consumption is less than in a Flash ADC, both the area and power is still higher than the SAR architecture.

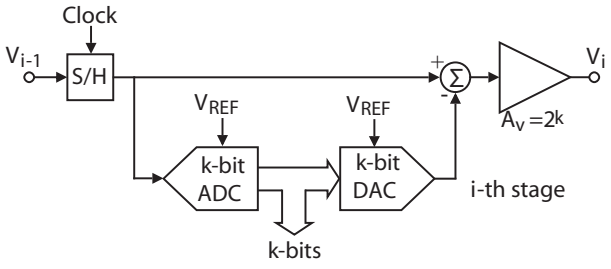

Figure 5.5: Single stage of a pipelined ADC [14].

5.3.3.4 Delta Sigma

While Flash, SAR and Pipelined ADC architectures are referred to as Nyquist rate ADCs (i.e. their sampling rate being equal to the Nyquist rate), Delta Sigma converters (Fig. 5.6) are oversampling ADCs in which a signal is sampled at a sampling frequency significantly (i.e. β times) higher than twice the bandwidth of the signal being sampled. Though this results in low to medium speeds of operation, much higher resolution can be achieved (e.g. 18-bits).

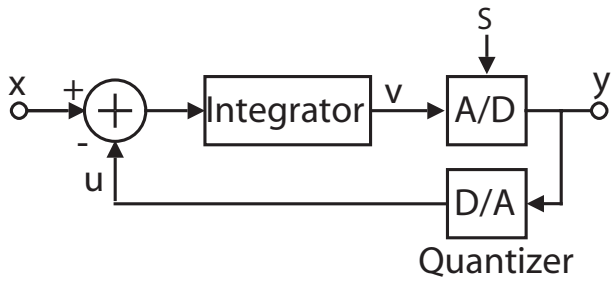

Figure 5.6: Diagram of a first order Delta Sigma ADC [14].

5.3.4 Data Converter Performance Metrics

There are nonidealities inherent in every circuit, some of which are caused by elements like opamps (offset, finite gain, bandwidth), comparators (offset, finite gain), and passive components (mismatch, thermal noise), and others which are caused by more fundamental circuit properties (e.g. parasitic elements, flicker noise, charge injection, clock feedthrough). All of these manifest themselves as static or dynamic and linear or nonlinear errors.

Where the ADC has had time to resolve the input signal, the term static is used to describe such errors, otherwise they are classified as dynamic. Such errors can then either be linear or nonlinear. Linear errors, which include things like offset or gain errors, are of less concern as they can be easily removed. Nonlinear errors, which result from things like random mismatch between equivalent structures (e.g. resistor banks in R-2R ladder DACs), however, cause much more irreversible problems. Examples of static nonlinear errors include differential and integral nonlinearity

(DNL and INL respectively).

When characterizing an ADC, there are several performance metrics in both the static and dynamic domain used, however, as the ADC designed here mostly operates in the static regime (i.e. sampling rate is significantly faster than the rate of change of the input signal), the static error performance metrics are only presented. Metrics that will be discussed include DNL, INL, gain and offset errors, and are generally represented in LSB units (but can also be represented as a percentage of the FSR).

5.3.4.1 Offset and Gain Errors

Offset error is defined as the difference between the nominal and actual offset points and is determined by the step value when the digital output is zero (Fig. 5.7). This error affects all the codes by the same amount and can be subtracted out.

Gain errors relate to the deviation in the slope of the actual versus the ideal transfer function (Fig. 5.8). Once the offset error has been eliminated, the gain error is determined by examining the nominal gain point (i.e. the step value when the digital output is at full scale).

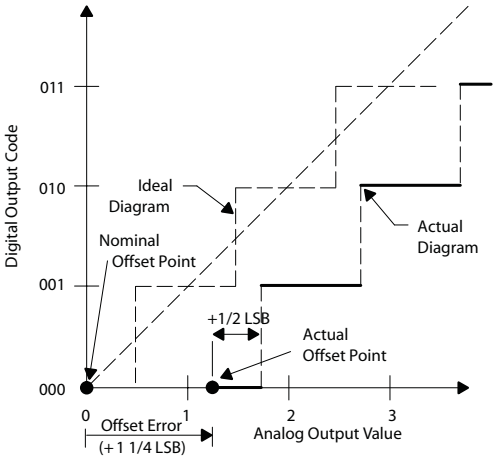

Figure 5.7: Offset error in a 3-bit ADC [15].

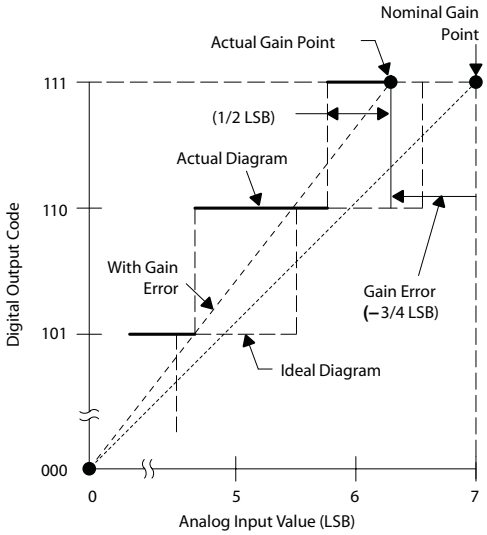

Figure 5.8: Gain error in a 3-bit ADC [15].

5.3.4.2 Differential Nonlinearity (DNL) Error

Differential nonlinearity, illustrated in Fig. 5.9, is the difference between the actual step width and the ideal value of 1 LSB. If the step width is 1 LSB, then the differential nonlinearity error is zero, otherwise, there is the chance that the converter can become monotonic or that there might be missing codes.

5.3.4.3 Integral Nonlinearity (INL) Error

Integral nonlinearity error, illustrated in Fig. 5.10, is the deviation of the values on the actual transfer function from the ideal (the straight line). The deviations are measured at the transitions from one step to the next. The straight line is most often drawn between the end points of the transfer function (once the offset and gain errors have been removed).

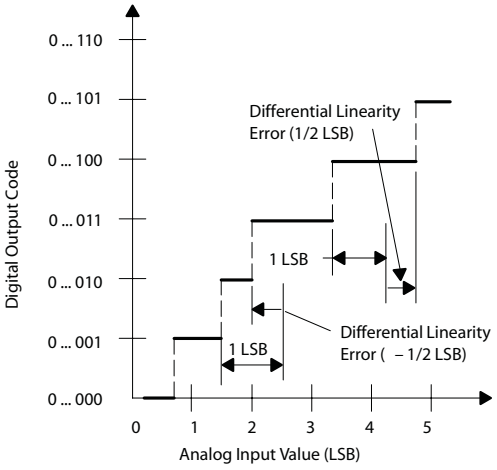

Figure 5.9: Differential nonlinearity error in a 3-bit ADC [15].

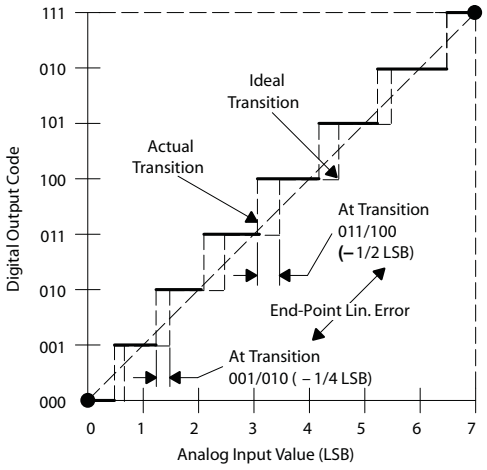

Figure 5.10: Integral nonlinearity error in a 3-bit ADC [15].

5.4 Design and Operation

Due to the requirements of medium resolution (8-bits to 16-bits), moderate operating frequencies (5 Mhz), and the need for smaller area (as required by the 0.8-μm process) and reduced power consumption, the SAR ADC architecture was chosen. By selecting this design, not only are the requirements met, but because of its its

modular nature, it was very easy to modify the designed ADC for higher resolution by simply exchanging the DAC and comparator with devices with higher resolution. The first section presents the design of the 8-bit SAR ADC and its subcomponents, followed by a section on the performance metrics determined from simulation results. The final section discusses the performance metrics of the actual fabricated device.

5.4.1 SAR ADC Top-Level

A top-level schematic of the ADC is illustrated in Fig. 5.11. As described earlier in the background section, the SAR architecture consists of an all digital successive-approximation register (SAR) component, a comparator, and an R-2R ladder DAC. The SAR ADC employs a binary search algorithmic approach to converge to a digital result from an analog voltage input. The digital processing occurs in the SAR which plays the central role between the comparator and DAC. The ADC operation along with a description of the SAR register is provided first, following which, the sample and hold circuit, comparator then DAC operation and results are presented.

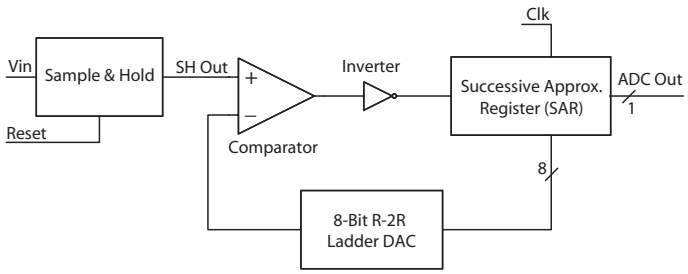

Figure 5.11: A block diagram SAR ADC architecture.

5.4.1.1 Successive-Approximation Register

The successive approximation ADC operates based on the principle of a binary search where by it begins at half of the reference voltage then attempts to successively set (or not set) the N-bits, halving the search range each cycle, and thus also setting a bit each cycle. This operation is illustrated in Fig. 5.12 and an example is

presented in Table. 5.1 for an 8-bit ADC, with a 5 V reference and a 3.21 V input signal.

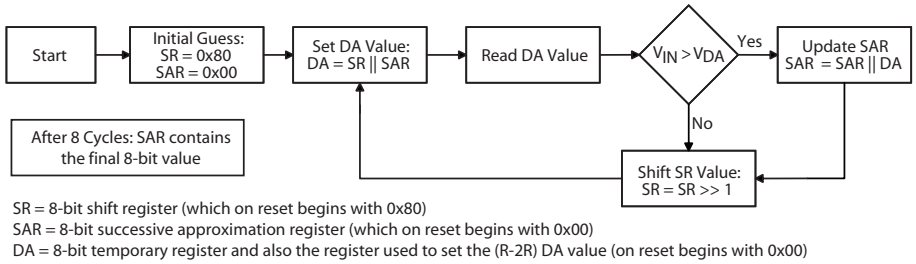

Figure 5.12: ADC operation steps.

Table 5.1: Example of SAR binary search operation

SR Value	SAR Value	DAC In	DAC Out (V)	Comparison Results	
10000000	00000000	10000000	2.5	low	keep bit
01000000	10000000	11000000	3.75	high	drop bit
00100000	10000000	10100000	3.125	low	keep bit
00010000	10100000	10110000	3.4375	high	drop bit
00001000	10100000	10101000	3.28125	high	drop bit
00000100	10100000	10100100	3.203125	low	keep bit
00000010	10101000	10100110	3.2421875	high	drop bit
00000001	10101000	10100101	3.22265625	high	drop bit

The SAR block is illustrated in Fig. 5.13 and is a direct mapping of the flowchart logic in Fig. 5.12. It consists of basic combinational logic and three N-bit registers:

1. The SA register is a shift register that begins with its MSB high and all other bits low. After N-cycles, the single high bit rotates back to the MSB position, preparing the register for the next conversion cycle.

2. The DA register stores the digital input values for the DAC and is at an all zero state on reset.

3. The successive-approximation register (SAR) stores the ongoing and also final results of the ADC conversion.

All of the registers were implemented with Scan D-type flip-flops (i.e. with the additional scan-in and scan-enable inputs) with outputs tied to the D input and new

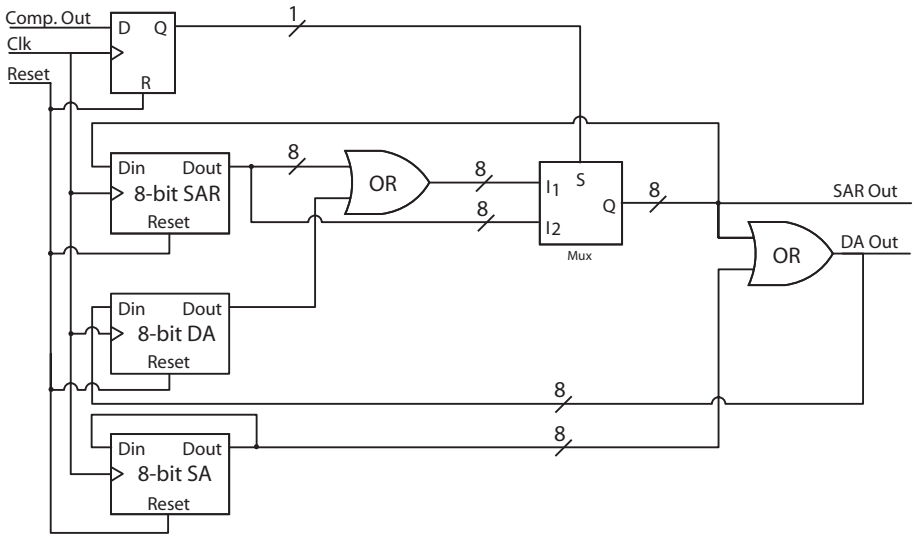

Figure 5.13: SAR register schematic.

inputs arriving at the scan-in port. Though increasing area, by driving scan-enable low and cycling the outputs to the inputs, a constant state is maintained, reducing power consumption from switching states. By increasing the width of each register, the digital logic can easily accommodate higher resolution conversions. Finally, the output digital code does not necessarily need to be read from SAR. Depending on the requirements, either the entire N-bit digital code can be read from the successive-approximation register after N-cycles or one bit per cycle can be derived (from MSB to the LSB) by sampling the inverted output of the comparator, saving one additional read cycle.

5.4.1.2 Sample and Hold

A single transistor-capacitor parallel SH circuit is used. The transistor width is reduced to 2 μm to decrease the effects of charge injection (Equ. 4.24), with a resulting on-resistance (R_{ON}) of about 6.6 kΩ. Assuming all the charge is transferred to the capacitor (in the worse case, where δV is the change in voltage due to charge injection), δV = 628 μV per calculation. Furthermore, because of the V_{TH} drop of the single NMOS transistor, the maximum voltage that can be passed to the ADC is: $V_{OUT_{max}} = V_{IN} - V_{TH} - \delta V$ = 3.916 V. As the maximum input voltage expected

based on requirements is about 3 V, this falls within specifications. A 1 pF capacitor helps reduce charge injection (Equ. 4.24) while still allowing the sampled voltage to remain constant for about 5 ms (from simulation), sufficient for the ADC convergence period (about 1.6 μs).

5.4.1.3 R-2R Ladder DAC

As illustrated in Fig. 5.14, an R-2R ladder DAC is used to implement the ADC. The digital inputs (b_i) range from the MSB ($i = N-1$) to the LSB ($i = 0$) and are switched between either 0 V or V_{REF} (where V_{REF} = 5 V). Operation of the DAC is based on Kirchhoff's current law where the current entering a node must leave by way of two resistors. Thus, the output voltage is determined using V_{REF} and the resistance, which is inversely proportional to the summed binary weight of each digit (Equ. 5.1). The max output voltage is given by Equ. 5.3 and is about 4.98 V.

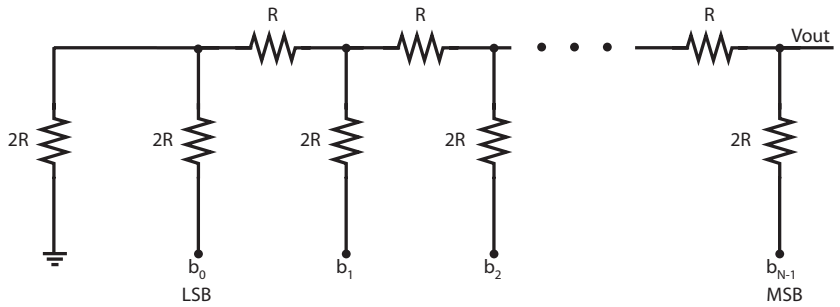

Figure 5.14: N-bit R-2R ladder DAC with .

The R-2R ladder is a very simple and fast (with a fixed output impedance of R) DAC, however the output accuracy is heavily dependent on the resistor matching. For higher resolution implementations, other alternative should be considered.

5.4.1.4 Comparator

For the 8-bit resolution ADC, the open loop (two stage op-amp) comparator illustrated in Fig. 5.15 was used. The resolution of this comparator at different input common mode voltages is illustrated in Fig. 5.16. As for an 8-bit ADC, a resolution of 1 LSB (0.019 V) is required, from this figure it is clear that the comparator operates well within this range from about 0.2 V to 4.5 V.

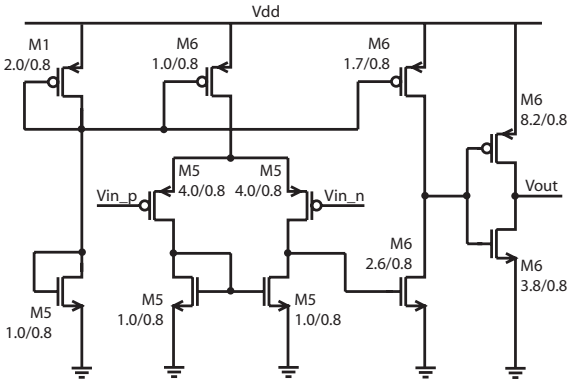

Figure 5.15: Two-stage open loop comparator.

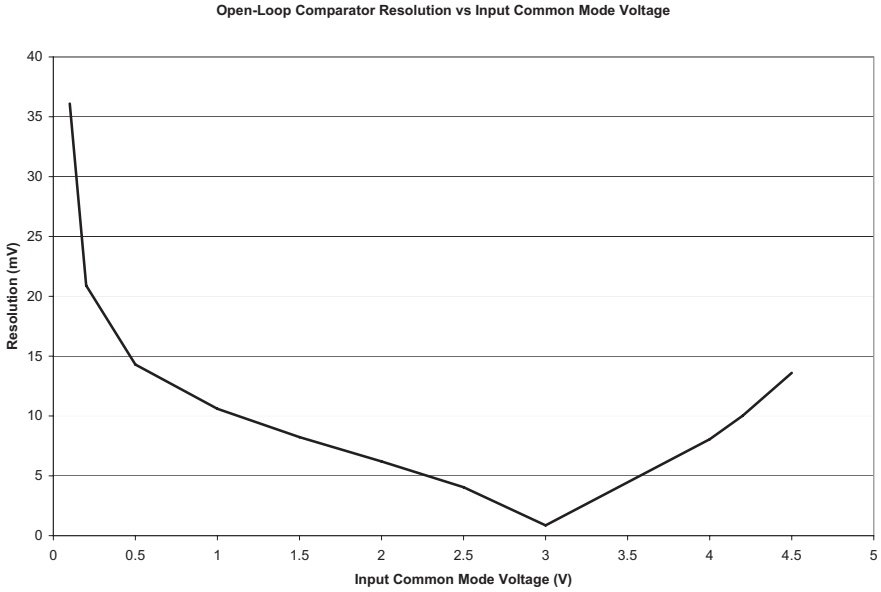

Figure 5.16: Resolution of the open-loop comparator with respect to input common mode voltage.

For the comparator to be able to sample the correct value at its inputs, the outputs of both the SH and the DAC must have settled to a constant value. The settling time for the sample and hold circuit is based on the on-resistance of the switch (R_{ON}) and the sampling capacitance (C_H) and is calculated to be about 14.5 ns. The settling time of the DAC output depends on the output impedance of the ladder network (R) and the input capacitance of the comparator, and is calculated to be about 111 ns. Thus, both sufficiently meet the 200 ns (5 MHz) operating requirement.

5.4.2 Simulation Results and Performance Metrics

To quantify the performance of the ADC, a linear ramp was applied to its input with a step size of 1.22 mV (i.e. $5/2^{12}$) and the resulting output codes were examined. From this, the offset and gain errors were determined to be 2 LSB and 1 LSB respectively up to a full scale range of 197 LSB (i.e. about 3.848 V - as expected from the SH Section 5.4.1.2).

The DNL and INL errors were determined using the histogram method (Fig. 5.17 and Fig. 5.18 respectively) after the offset was subtracted and the gain (slope) error was adjusted for. The maximum and minimum DNL errors were found to be 0.0562 LSB and -0.130 LSB respectively. It is clear from the INL that some form of nonlinearity is present. This could be a result of the comparator performance (nonlinearity is illustrated in Fig. 5.16) or charge injection from the sample and hold circuit (in which V_{TH} exhibits a nonlinear dependence on V_{IN} - see Equ. 4.25). However, both the DNL and INL are minimal and the ADC response is found to be both monotonic (with continually increasing codes) and complete (i.e. no missing codes).

5.5 Measured Results

In characterizing the fabricated ADC, an instrument to generate a precise linear ramp was not readily available so ADC histogram testing was done using a sinusoidal input. For histogram testing, applying a sinusoidal input results in a histogram that is not flat, rather is "bath-tub shaped." This is because at the sinusoid midpoint crossing there are the least number of samples (i.e. dv/dt = max) and at the sinusoid amplitude peaks, there are the highest number of samples (i.e. dv/dt = min). Based on the works of Bossche [58] and Murmann [59], a correction is provided to address this. Using this correction, the DNL and INL of a 500 Hz sinusoidal input (3.5 V_{pk-pk}) sampled at 4800 Hz is given in Fig. 5.20 and Fig. 5.21 respectively. A more intuitive illustration of the deviation is in Fig. 5.19.

From the DNL, short code word lengths (i.e. less than -0.9 LSB) indicate the

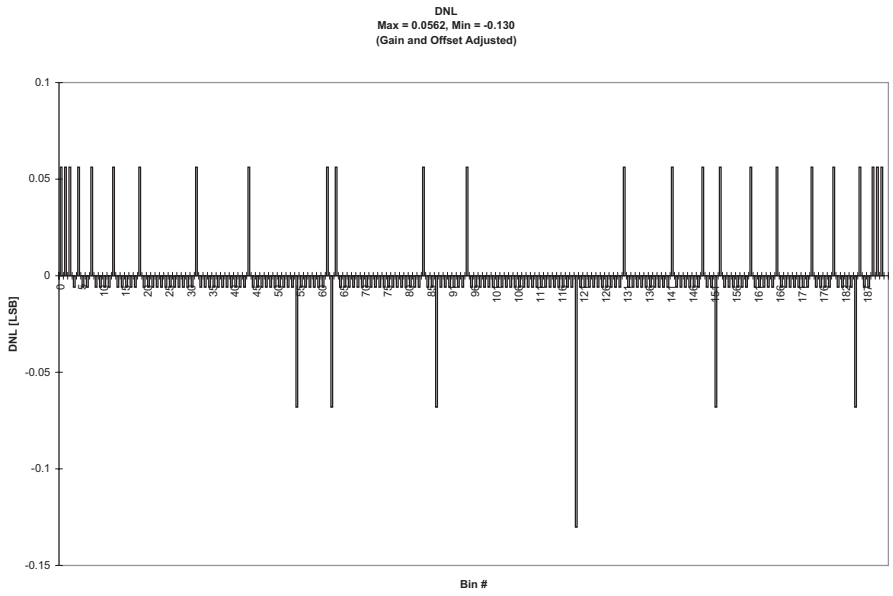

Figure 5.17: DNL results from simulation of the 8-bit ADC with an applied ramp with 4096 steps.

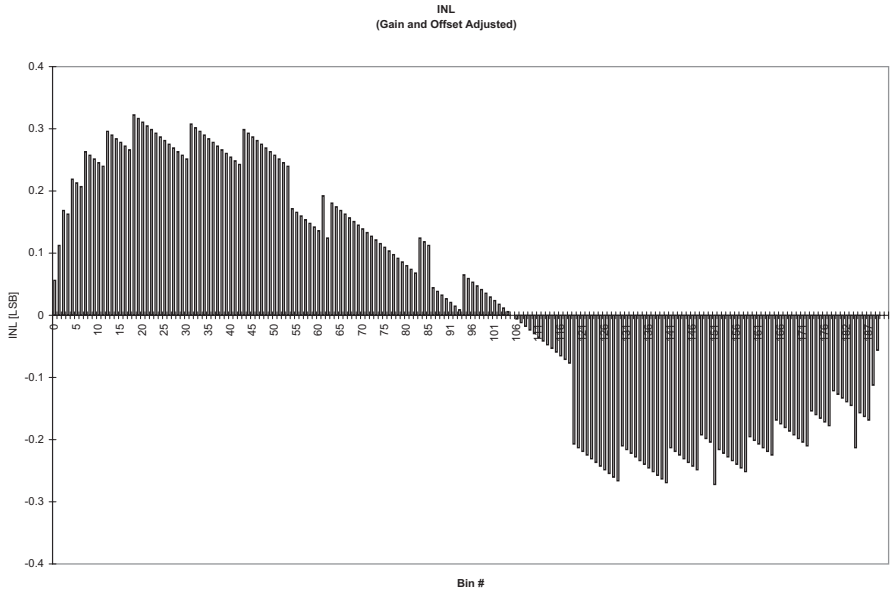

Figure 5.18: INL results from simulation of the 8-bit ADC with an applied linear ramp with 4096 steps.

possibility missing codes [59]. Based on this, there are 15 missing codes based on the actual measurements. Furthermore, from the INL plot we can see that the actual signal begins to deviate from the expected signal at higher input voltages. An explanation behind some of these observed behaviors might again first be due

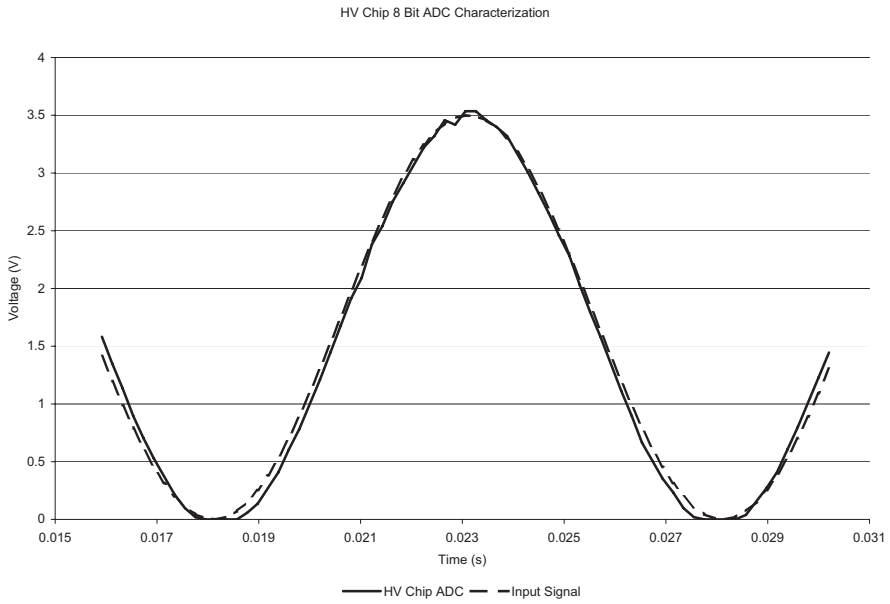

Figure 5.19: Actual versus ideal response of the 8-bit ADC to a 500 Hz sinusoid.

to charge injection and nonlinear performance of the comparator at higher voltage ranges, but also due to the nonlinear performance of the DAC. In simulation, the R-2R ladder DAC performs ideally, however, in reality, accuracy is strongly dependent on matching which may not be ideal. Parasitic sources may also contribute to longer settling times of the DAC output causing other deviations. From these results, the ADC is operating with about a 7-bit resolution, sufficient to meet the initial requirements.

5.6 Conclusion

High-resolution ADCs are essential for sensitive optical detection systems. Additionally, complete LOC systems, which incorporate voltage and current monitoring, require analog-to-digital conversion to be able to communicate analog values off-chip. We have designed an 8-bit and 12-bit successive approximation ADC and successfully demonstrated the operation of the fabricated lower resolution ADC at 7-bits for the 0-3 V target operating range. The performance of the ADC could be improved in future work by replacing the R-2R ladder resistive DAC with a current

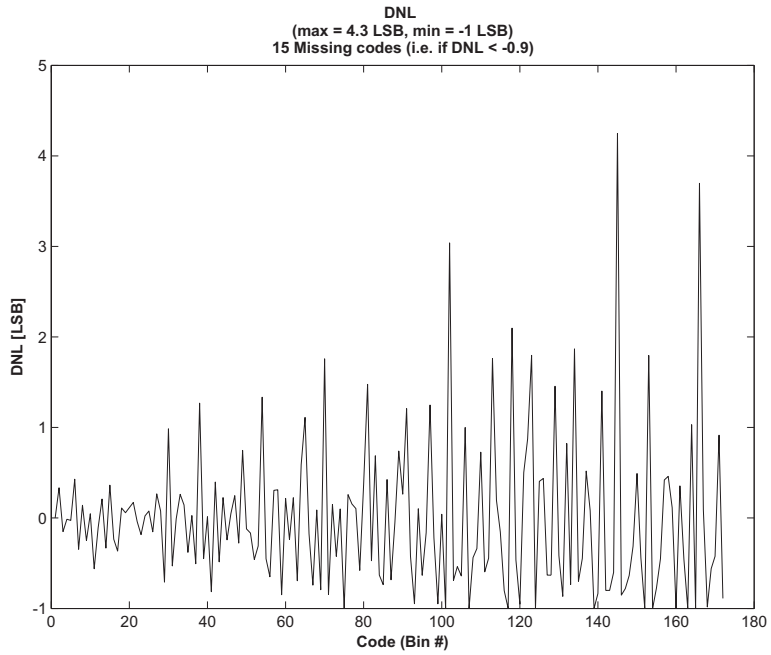

Figure 5.20: DNL results from actual measurements of the 8-bit ADC with an applied 500 Hz sinusoid.

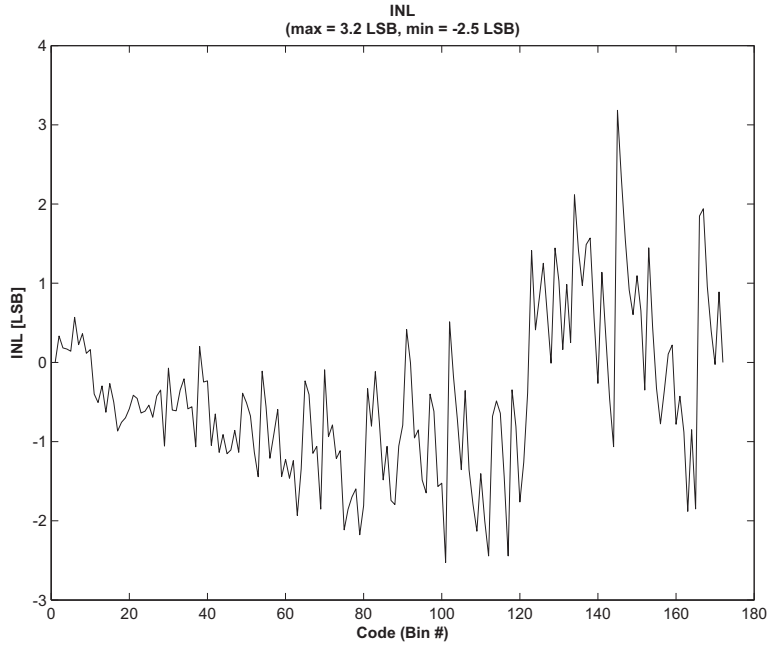

Figure 5.21: INL results from actual measurements of the 8-bit ADC with an applied 500 Hz sinusoid

mode variant, and the comparator with a clocked version that incorporates positive feedback to improve resolution.

Chapter 6

High-Voltage Generation and Output Stages

In this chapter, high-voltage generation through an inductive step-up boost converter is first presented. This is followed by a comparison previously published level-shifter circuits (used to switch the high-voltages required for microfluidic applications) with several proposed designs.

6.1 Motivation

As discussed in earlier chapters, besides the optical detection, the high-voltage power supply and associated switching elements like relays are the next largest external component in electrophoretic based microfluidic systems. So, to create a truly portable solution, the power supply and the switching elements need to be reduced significantly in size.

6.2 Requirement

For millimeter (and potentially even micrometer) channel lengths, sufficient electric fields (e.g. 150 V/cm [60]) for size-based separation of analytes can be achieved with only several hundreds of volts. As the maximum voltage possible across the high-voltage transistors in the DALSA process at the time of this work was 300 V, a target voltage of 300 V was set. Further, as currents in microfluidic systems generally do not reach 100 uA, a target source current capability of 60 uA was also

set.

As presented in the background section, the two most common operations used in our application of microfluidics is an injection step followed by a separation step. These two steps require outputs, which are capable of being placed in a high-voltage, floating (or high-impedance state) and a ground (low) state, with switching frequencies that may range between to 10-100 Hz.

6.3 Inductive DC-DC Step-Up Boost Converter

To reach the high-voltages required, a inductive step-up boost converter is used. Background and its principles of operation are presented first, followed by simulation and measured results.

6.3.1 Principles of Operation

The basic boost converter circuit is illustrated in Fig. 6.1. This circuit steps-up an input voltage to higher voltage at the output. As power must be conserved (Ohms law), the output current is lowered from the source current. In this work, the switch is implemented with LDMOS (laterally diffused high-voltage NMOS) transistors. With the transistor sinking current, a magnetic field forms in the inductor (L) as current passes through it. With the transistor off, as the magnetic field cannot collapse instantaneously, current instead passes through the flyback diode, charging the load capacitor (C). To reach a target voltage, this transistor is switched repeatedly until sufficient charge is stored on the capacitor.

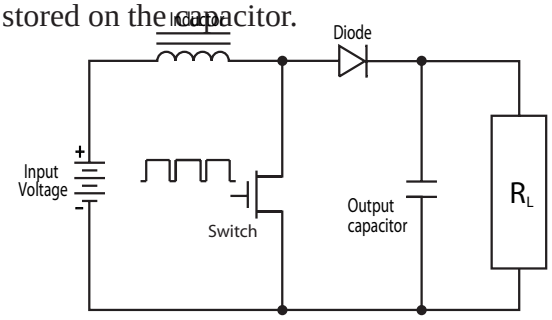

Figure 6.1: Basic inductive DC-DC boost converter circuit.

Depending on the size of the load, the maximum output voltage (and thus gain)

becomes dependent on several factors. A large load limits the gain as it places the boost converter in the continuous regime. In this mode, the gain is dependent only on the duty cycle. However, when the load is sufficiently small (i.e. $I_O/I_I < 0.1$ [16]), the boost converter operates in the discontinuous mode and the gain is dependent on the duty cycle (D), input voltage(V_I), and the output current (I_O) and the gain can generally be higher. Fig. 6.2 illustrates the relationship between gain and the ratio of the output to input current. The two different modes of operation are discussed in more detail below.

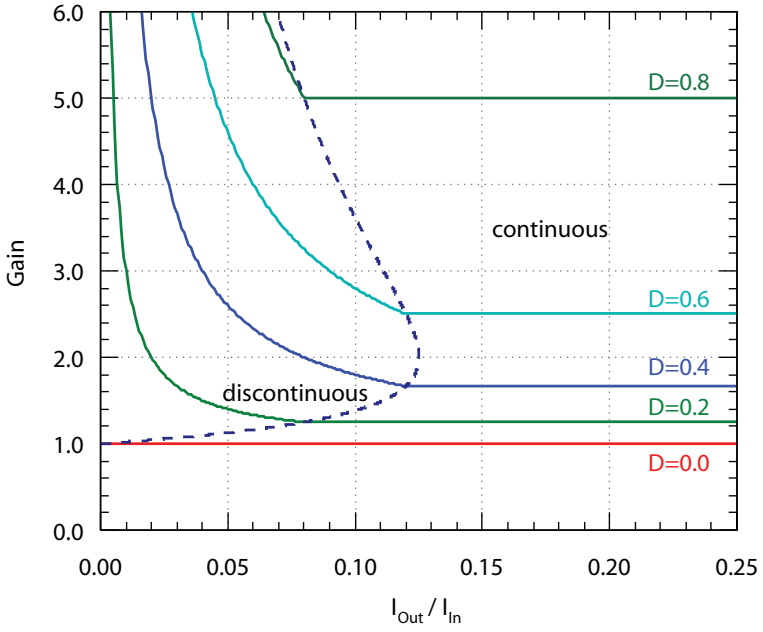

Figure 6.2: Gain dependent on output-input current ratio for the discontinuous and continuous modes of operation. [16]

6.3.1.1 Continuous mode

When the load is small, the boost converter operates in continuous mode and the inductor current (I_L) never falls to zero (Fig. 6.3).

Assuming all of the components are ideal, when the switch (pull-down transistors) is on, the inductor voltage equals the input voltage and a change in current occurs given by:

$$\Delta I_{L_{ON}} = \int_0^{DT} \frac{V_{L_{ON}}}{L} dt = \frac{V_i DT}{L} \tag{6.1}$$

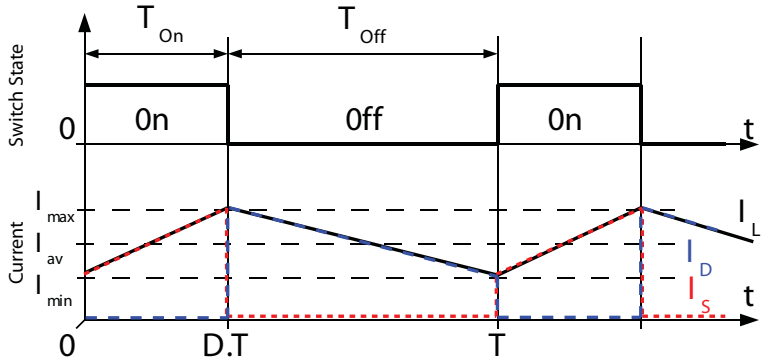

Figure 6.3: Boost converter continuous mode of operation.

Where D is the duty cycle (i.e. on-time) and T is the switching period. Assuming there is no voltage drop across the diode, when the switch turns off, the change in current equals:

$$\Delta I_{L_{OFF}} = \int_0^{(1-D)T} \frac{V_i - V_o}{L} dt = \frac{(V_i - V_o)(1-D)T}{L} \tag{6.2}$$

As energy must be conserved, the change in inductor current during the on cycle must equal that of the off cycle (i.e. $\Delta I_{L_{ON}} = \Delta I_{L_{OFF}}$). This yields:

$$\frac{V_o}{V_i} = \frac{1}{1-D} \tag{6.3}$$

6.3.1.2 Discontinuous mode

During the discontinuous mode of operation, the amount of energy required by the load is small enough that it can be transferred in less then a full duration of the off cycle (i.e. δT). This results in a period of zero inductor current (Fig. 6.4).

When the switch is on, the inductor current is initially zero but reaches a maximum defined by:

$$I_{L_{MAX}} = \frac{V_i DT}{L} \tag{6.4}$$

When the switch is off, as the load requires less energy, the inductor current falls to zero earlier at δT. Furthermore, as the output current (I_o) equals the average inductor current during the off state, the output current can be written as:

$$I_o = \frac{I_{L_{MAX}}}{2}\delta \tag{6.5}$$

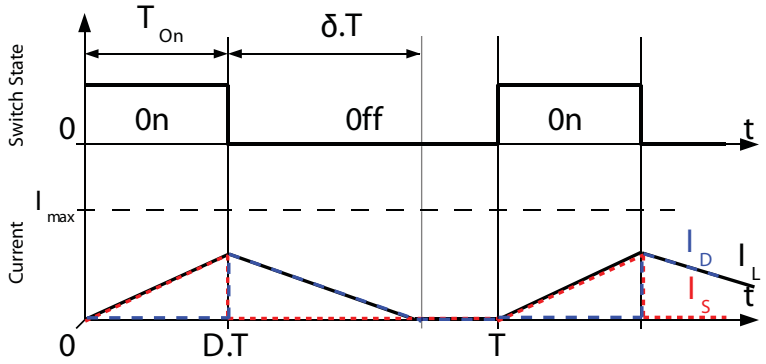

Figure 6.4: Boost converter discontinuous mode of operation.

Knowing again that change in current during the on-time and during the off-time must be equivalent, and solving for:

$$\Delta I_{L_{MAX}} + \frac{(V_i - V_o)(1-D)T}{L} = 0 \tag{6.6}$$

Yields:

$$\delta = \frac{V_i D}{V_o - V_i} \tag{6.7}$$

Using Equ. 6.7 in Equ. 6.5 yields the output voltage gain in discontinuous mode:

$$\frac{V_o}{V_i} = 1 + \frac{V_i D^2 T}{2LI_o} \tag{6.8}$$

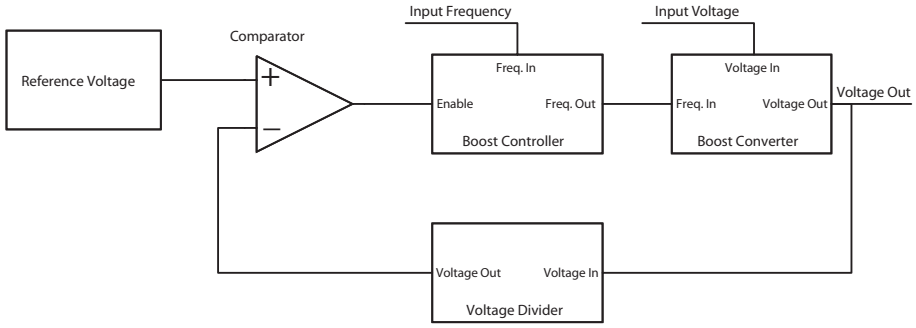

Figure 6.5: This basic controller turns off the input frequency source once the (divided down) output voltage surpasses a reference.

Because the gain can become quite large in discontinuous mode, a control circuit is required to monitor the output voltage and ensure it remains within some

threshold. A basic control scheme is illustrated in Fig. 6.5. In this figure, a scaled output voltage (e.g. 1%) is compared with a reference voltage. If larger than the reference, the off-state is extended, ensuring the output voltage drops.

6.3.2 Simulated and Measured Results

A current controlled oscillator implemented with 31 current starved inverter stages, followed by a divide by 80 stage (which modified the duty cycle to 90%), is used to generate the required frequency and duty cycle for the boost converter operation. Simulation and measured results of the generated boost converter input frequency is illustrated in Fig. 6.6.

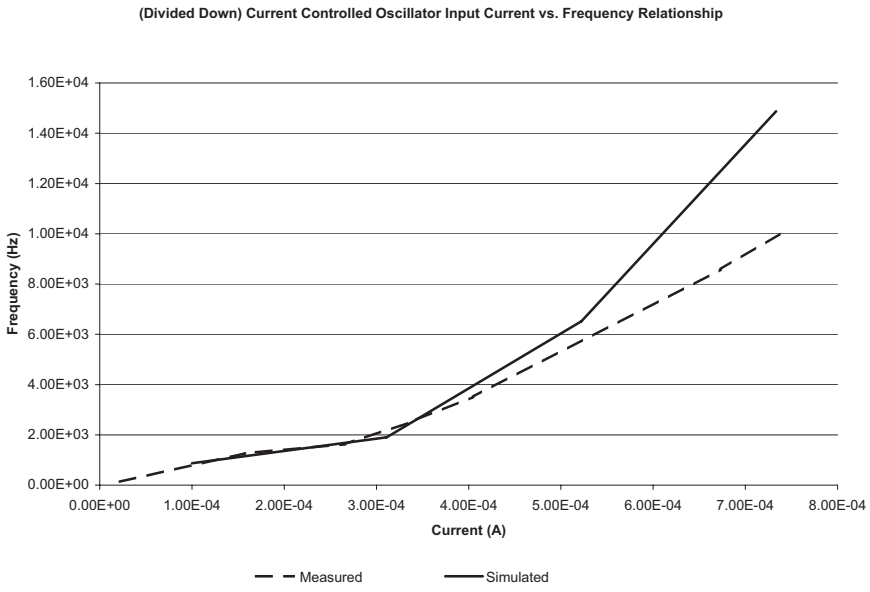

Figure 6.6: Measured and simulated results of the divided down oscillator frequency with respect to input current.

Along with the oscillator, the flyback diode for the boost converter circuit is also implemented on the actual HV CMOS chip using a diode connected extended drain HV PMOS (EDPMOS). However, because of a parasitic bipolar PNP transistor in the layout (Fig. 6.7), a larger amount of the input current (passing through the emitter) is sunk into the (collector) substrate than pushed through to the (base) output. This significantly reduces the efficiency of the boost converter.

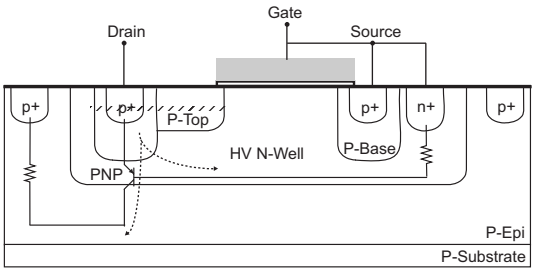

Figure 6.7: Parasitic PNP in the boost converter diode connected transistor.

Both the current lost to the substrate (i.e. through the collector region) and the current that reaches the output (i.e. through the base region) are dependent on the common-emitter current gain (β) as shown in Equ. 6.9 and Equ. 6.10 respectively.

$$i_{substrate} = \frac{\beta}{\beta+1} i_e \tag{6.9}$$

$$i_{out} = \frac{1}{\beta+1} i_e \tag{6.10}$$

Ideally, to maximize current to the output through the base region (and conversely reduce current loss to the substrate), β should be as small as possible. Fig. 6.8 shows the measured β values of the EDPMOS (labeled PEG95EA) and a custom HV diode with a base width of 10 μm. β is influenced inversely by two factors: the width of the base and the relative doping of the base and emitter region. As the doping cannot be altered, the base width can be increased to decrease β. However, as the width can only be increased to a reasonable point, the leakage to the substrate must be tolerated when using an internal diode.

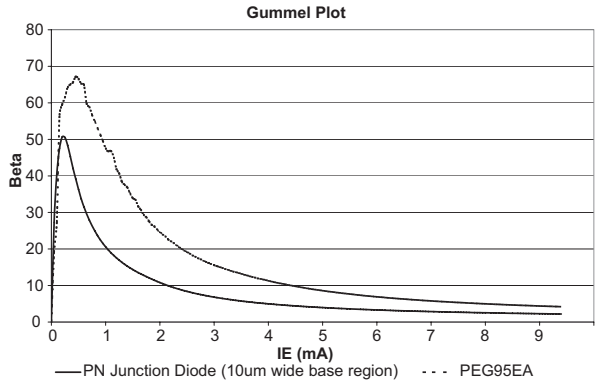

Figure 6.8: Measurement results of gain dependence on input (emitter) current.

To address the leakage to the substrate through the parasitic PNP, an external fast switching diode (Fair child Semiconductor 1N4148 switching diode) with a junction voltage of 620 mV (min) to 720 mV (max) was placed in parallel with the internal diode. As the internal diode junction voltage is about 700 mV, the external diode turns on sooner, limiting the leakage to the substrate. Furthermore, as it was found during testing that the reference voltage used in the boost controller feedback loop was not accurate, the on-chip boost controller did not function. However, the diode, with its breakdown voltage of around 142 V - 150 V (rated to breakdown at 100 V though), helps regulate the voltage at 150 V, but unfortunately does not allow the voltage to reach the target 300 V. For a higher voltage, a fast switching diode with a higher breakdown voltage is required. Final implemented and measured boost converter specifications are listed in Table 6.1 and simulations results are given in Fig. 6.9.

Table 6.1: Boost Converter Specification

Parameter	Value	Unit
V_{IN}	5	V
I_{IN}	7.6	mA
$V_{OUT_{MAX}}$	150	V
$I_{OUT_{MAX}}$*	60	μA
Frequency	2.4	kHz
L	100	mH
C	100	nF
R_L	10	MΩ
*$I_{OUT_{MAX}}$ @ 150 V		

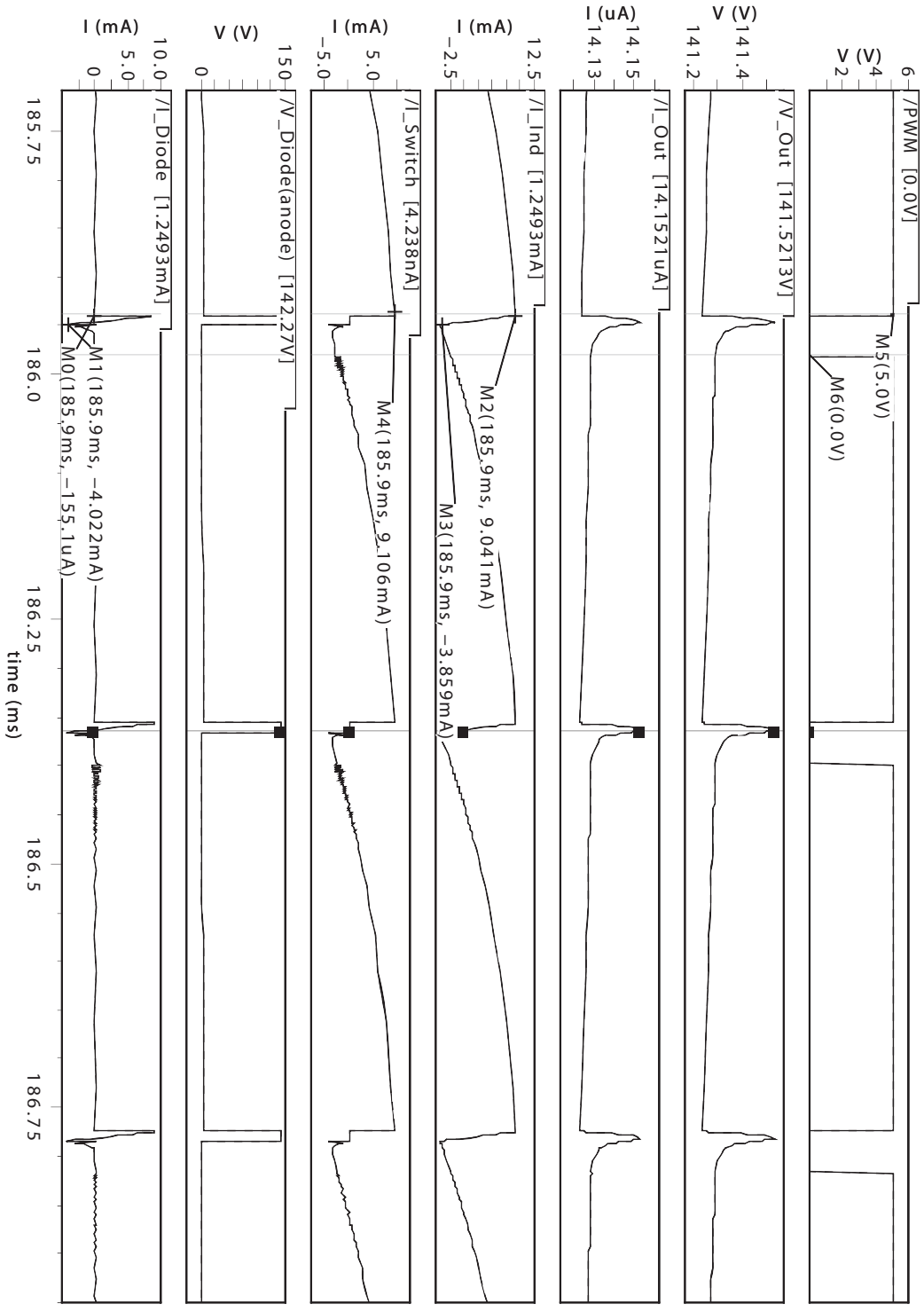

Figure 6.9: Boost converter simulation results.

6.4 Level-Shifter Circuit

In this section, background information on level-shifters will be first provided, followed by description behind the operation of five different level-shifter designs. The final section will discuss the measured and simulation results.

6.4.1 Background

A conventional high-voltage level-shifter (Fig. 6.10) consists of a complementary output stage with independent control of the LDMOS and EDPMOS transistors, M1 and M2. While the LDMOS can be controlled by standard low-voltage (5 V) logic, an appropriate signal ($V_G < V_{PP} - V_{TH}$) must be applied to the gate of the EDPMOS for proper operation. Gate voltage for the EDPMOS and LDMOS to control the outputs is given in Table 6.2. Especially for portable devices, these signal must be provided in an energy efficient manner. To address this, the five designs below employ four static: (1) pseudo-NMOS, (2) pseudo-NMOS with current limit for reduced power (3) full-static cross-coupled (4) resistive pull-up, and one dynamic implementation.

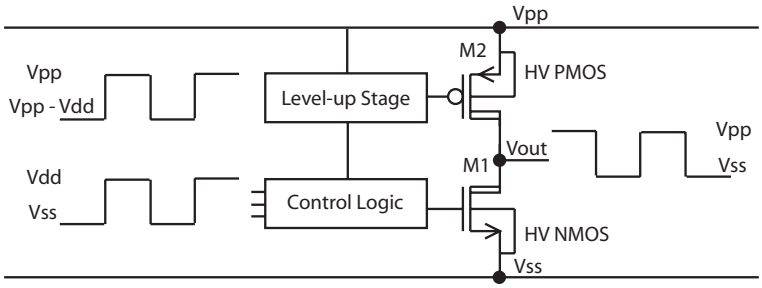

Figure 6.10: Components of a conventional level-shifter circuit.

Table 6.2: Output stage gate voltage and respective outputs.

	HV NMOS		HV PMOS	
Output State	$V_{G_{HVNMOS}}$	state	$V_{G_{HVPMOS}}$	State
High	$< V_{SS} + V_{THN}$	Off	$< V_{PP} - V_{THP}$	On
Float	$< V_{SS} + V_{THN}$	Off	$> V_{PP} - V_{THP}$	Off
Low	$> V_{SS} + V_{THN}$	On	$> V_{PP} - V_{THP}$	Off

6.4.2 Implementation and Operational Detail

Five different level shifters were implemented and fabricated. This section describes the different designs and explains their operation. The circuits discussed below are composed of six different kinds of n- and p-type MOS transistors, all of which are available in some form in most HV CMOS technologies. Illustrated in Fig. 6.11, devices (a) and (b) are standard LV NMOS and PMOS transistors, which can float up to 40 V above the substrate potential, but have a V_{GS} and V_{DS} limited to 5 V. Device (c), (d) and (e) are the high-voltage MOSFETs with source-drain breakdown voltage (V_{BDS}) in excess of 300 V and gate-oxide breakdown voltage (V_{BOX}) of 30 V. Device (c) is a floating HV extended drain PMOS (EDPMOS) while devices (d) and (e) are floating and non-floating lateral diffused HV NMOS (LDMOS) transistors. Device (f) is a thick-oxide medium voltage PMOS (PMOS2) with $V_{BOX} \approx 30\,V$ and $V_{BDS} \approx 15\,V$. Capable of floating in excess of 300 V when placed in its own well, this device serves well as an active load in current mirrors.

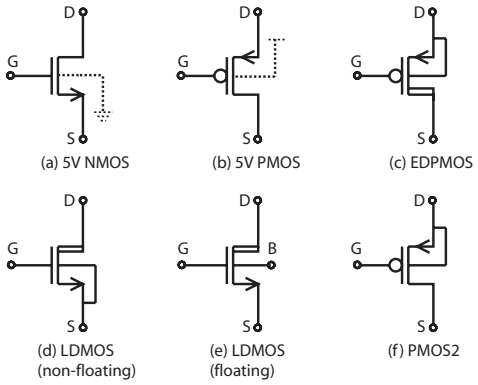

Figure 6.11: The 5 V and high-voltage CMOS devices used.

6.4.2.1 Circuit 1 - Pseudo-NMOS

Presented in [61] and [53], this circuit adopts a conventional cross-coupled level-shifter configuration (Fig. 6.12). Transistors M2 and M3 are used as pull-ups to drive V_{DN6} and V_{DN7} to V_{PP}, and to ensure the output EDPMOS is turned completely off or on. To prevent V_{BOX} when either M6 (V_{IN} high) or M7 (V_{IN} low) are

on, and when the HV supply exceeds 30 V, M1 and M4 are used to limit the voltage drop across V_{DN6} or V_{DN7} to $V_{PP} - V_{DD}$.

The major drawback of this design is the continuous power dissipation in both output high and output low due to the fully-on pseudo-NMOS (LDMOS pulldown and PMOS2 pullup) configuration. From simulation results in Fig. 6.13, a constant 2.69 mA of current flows through the drain terminal of M6 or M7 in either case, which at $V_{PP} = 300$ V results in over 800 mW of quiescent power!

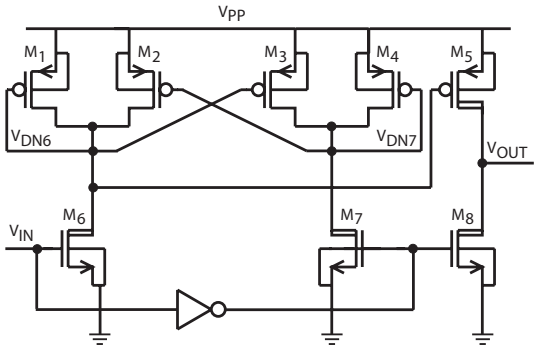

Figure 6.12: Circuit 1: Pseudo-NMOS level-shifter schematic.

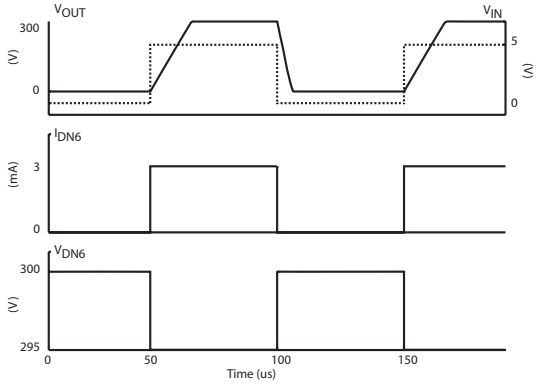

Figure 6.13: Circuit 1: Simulation results.

6.4.2.2 Circuit 2 - Pseudo-NMOS with current limit

To reduce the power consumption of circuit 1, a current limit can be enforced by adding the LV current mirror transistors M10 to M12, and the load transistor M9 (illustrated in Fig. 6.14). As shown in the simulation results of Fig. 6.15, the current

mirror transistors are sized to limit their on-current to about 970 nA (a factor of about 2700 reduction from circuit 1). However, the addition of the LV transistors requires M6 and M7 to be replaced with floating versions, otherwise their source and bulk is connected to the drain of the LV transistors.

While power consumption is significantly reduced with these modifications, the propagation delay increases from the reduced current, and area increases significantly due to the larger floating LDMOS transistors.

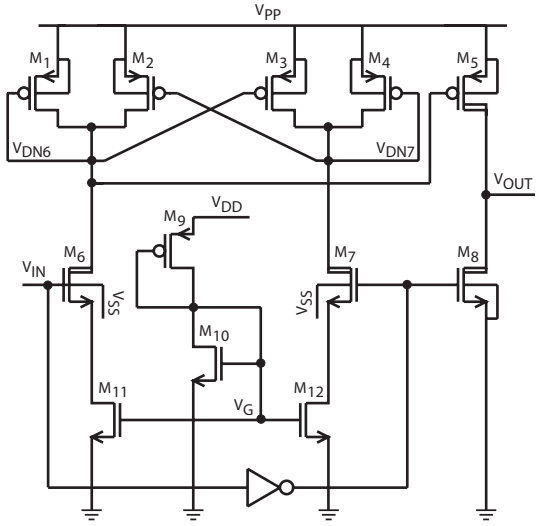

Figure 6.14: Circuit 2: Pseudo-NMOS with current limit level-shifter schematic.

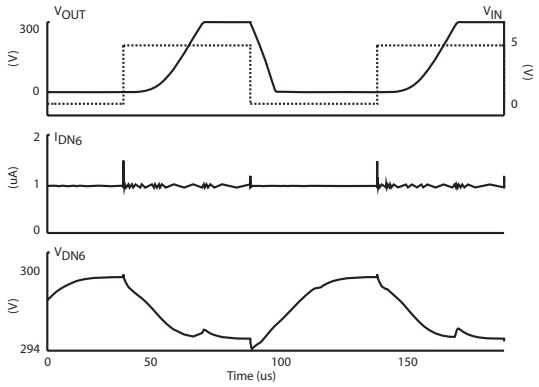

Figure 6.15: Circuit 2: Simulation results.

6.4.2.3 Circuit 3 - 3T resistive load

To reduce power consumption further, a three transistor (3T), full-static level-shifter using a resistive load is presented. The design and the corresponding simulation results are shown in Fig. 6.16 and 6.17.

While a conventional level-shifter may use a PMOS load rather than a resistive one, such a circuit suffers a near threshold drop at the gate of the EDPMOS when M1 is off. Consequently, the output EDPMOS, with a slightly different threshold voltage, is not driven completely off and the output voltage is not an ideal 0 V. By accounting for subthreshold leakage through M1 and appropriately sizing the resistive load, the V_{GS} of M2 can be minimized to ensure it remains off.

By using the current limit concept introduced in circuit 2 in conjunction with a resistive load, not only can a sufficient voltage drop be achieved at the gate of the EDPMOS during output high, but the on-current can also be controlled and reduced. The LV transistors are sized to allow around 450 nA through the drain of M1, reducing the current draw by half compared to circuit 2, but also resulting in an increased propagation delay. For output low, as M1 is completely off, the power dissipation is very small as it is a function only of the (sub-nanoamp) subthreshold leakage.

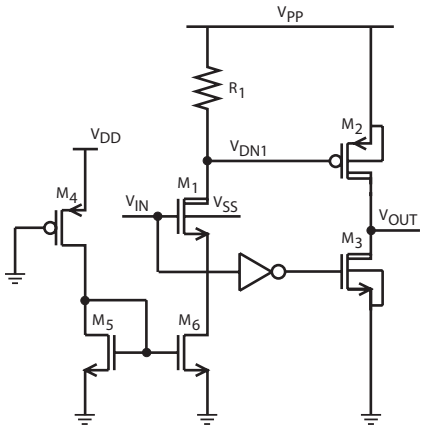

Figure 6.16: Circuit 3: 3T resistive load level-shifter schematic.

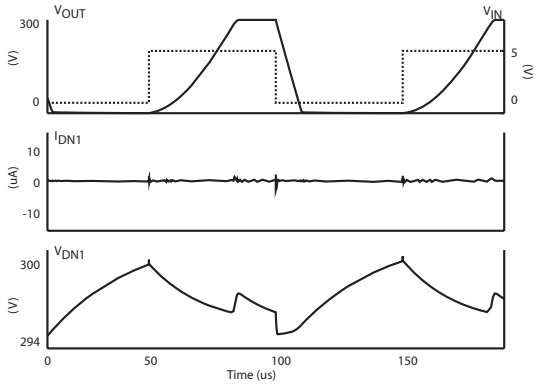

Figure 6.17: Circuit 3: Simulation results.

6.4.2.4 Circuit 4 - Full-static PMOS

To reduce power consumption to an absolute minimum, a full-static level-shifter, similar to circuits in [62], is presented. The design and the corresponding simulation results are shown in Fig. 6.18 and 6.19.

While the first circuit relied on active loads to limit the voltage drop across the cross-coupled PMOS2 transistors, this design uses transistors M3 and M4 biased at $V_{BIAS} > V_{PP} - V_{BOX}$ to limit the voltage-drop and ensure the voltage at the gates of M1, M2 and M5 do not exceed V_{BOX}. Specifically, when the input is either logic high or low, respectively, V_{DP1} or V_{DP2} are pulled low until their voltage drops below $V_{BIAS} + V_{TH}$, at which point M3 or M4 turn off, preventing further voltage drop.

Implemented with the medium voltage PMOS2 transistors, gate-oxide breakdown of M1 and M2 due to subthreshold leakage in M3 and M4, respectively, is prevented by sub-nanoamp drain-bulk (non-permanent) breakdown of M1 and M2 (since $V_{BDS} < V_{BOX}$ for the PMOS2).

As the subthreshold leakage, equivalent to the sub-nanoamp drain-bulk current, is the only continuous current draw, the power consumption of this circuit is significantly reduced compared to the earlier designs. The requirement of a circuit to generate the bias voltage is the main overhead of this design. A voltage divider can be used at the expense of increased area (and power consumption).

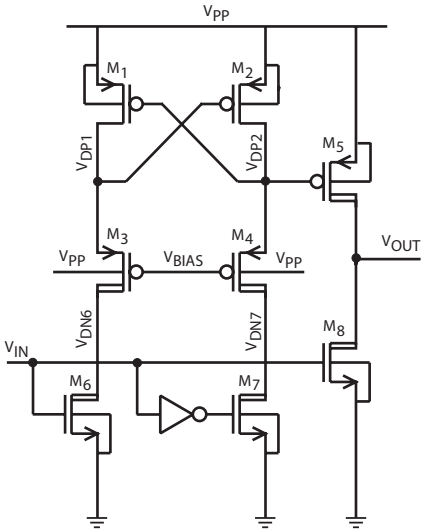

Figure 6.18: Circuit 4: Full-static cross-coupled level-shifter schematic.

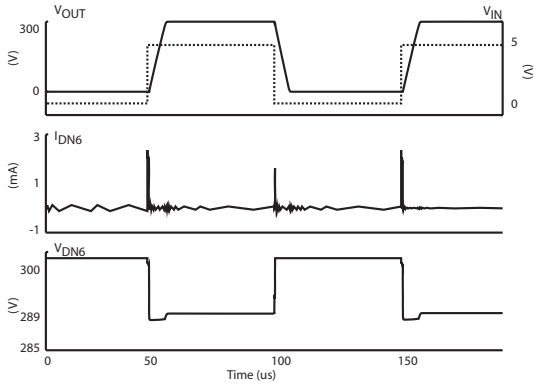

Figure 6.19: Circuit 4: Simulation results.

6.4.2.5 Circuit 5 - Dynamic

In this circuit (adopted from [63]), power consumption is reduced through dynamic control of the charge on the gate of the output EDPMOS transistor. Fig. 6.20 and 6.21 show the circuit and corresponding simulations.

A strobe signal, V_{IN1} controls the operation of the level-shifter. When M2 is off and the strobe signal is high, C1 is discharged and the output EDPMOS is turned off. However, if M2 and the strobe are high at the same time, M2 carries a 750 μA drain current, causing a 5 V drop across the PMOS2 load transistor M5. When the strobe (and V_{IN2}) signal go low, V_{GP6} is isolated and the voltage drop is ideally

retained. However, because of subthreshold leakage through M5, V_{GP6} must be periodically refreshed to maintain the level-shift operation.

Because power is consumed only during the strobe pulses, low average power dissipation is achieved by ensuring the duration of the strobe pulse is small. Also, because of already available dynamic control of input signals, crowbar current at the output stage can be eliminated by ensuring M3 is off before the EDPMOS turns on for output high, and turning the EDPMOS on only after the output stage LDMOS has been turned off for output low. Though not demonstrated here, crowbar current can also be eliminated in the static circuits.

To reduce power dissipation further, an improved design takes advantage of the Zener diode, Z1. With Z1 designed for a breakdown voltage of less than 15 V (to prevent V_{BDS} of the PMOS2 M5), M2 now only needs to be pulsed for output high (rather than also pulsing the strobe signal), thus eliminating the additional current draw through M1.

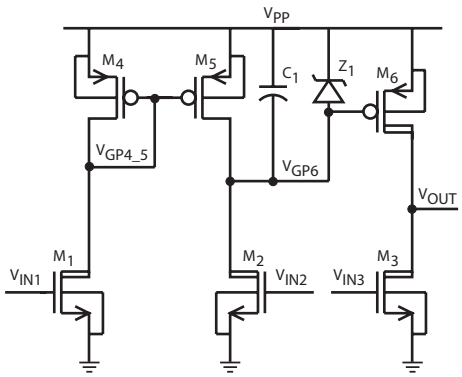

Figure 6.20: Circuit 5: Dynamic level-shifter with proposed zener schematic.

6.4.3 Measured versus Simulated Results

The simulation and measured results are presented in Table 6.3. Only simulation results are currently available for Arch. 4, however the design is fabricated and simply requires testing. The circuits were simulated and tested with a 52 pF capacitor in parallel with a 10 MΩ resistor and verified for a high voltage supply range from 5V to 300 V. Only the 300 V results are presented. Similar to conventional gate

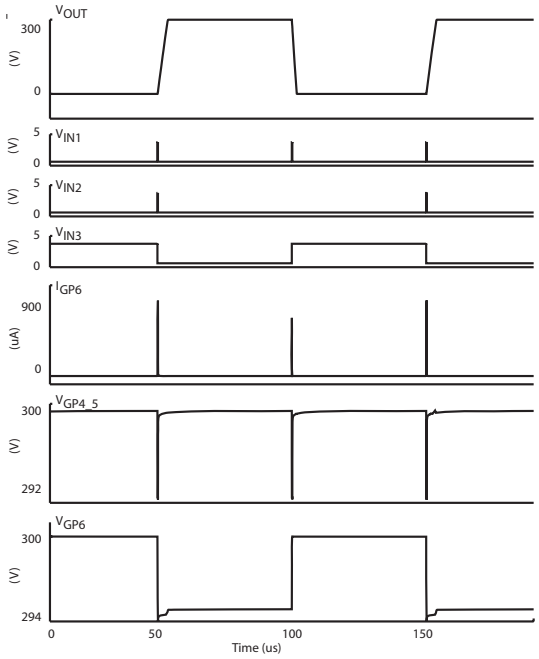

Figure 6.21: Circuit 5: Simulation results.

logic, the propagation delay is measured with respect to its input crossing $V_{DD}/2$ and its output crossing $V_{PP}/2$.

Table 6.3: Level Shifter Comparison at 300 V (52 pF || 10 MΩ Load)

Parameter	Circuit 1		Circuit 2		Circuit 3		Circuit 4		Circuit 5	
	Sim.	Mes.	Sim.	Mes.	Sim.	Mes.	Sim.	Mes.	Sim.	Units
Rise Time (10%-90%)	13.0	14.8	15.7	11.9	23.7	105.1	5.25	9.99	10.25	μs
Fall Time (90%-10%)	4.72	6.95	7.96	6.73	8.15	5.52	4.72	5.82	4.74	μs
Slew Rate (rising)	18.4	15.69	15.2	20.1	10.2	2.3	14.89	24.0	23.6	V/μs
Slew Rate (falling)	50.7	35.4	30.5	39.7	28.9	42.0	50.8	42.0	53.3	V/μs
Tprop (L – H)	8.08	8.97	22.9	9.44	24.2	61.5	3.68	5.89	6.2	μs
Tprop (H – L)	2.91	4.06	5.39	4.57	4.97	3.56	2.80	3.84	3.0	μs
$I_{V_{PPQ}}$ High	2689	2363	1.0	0.450	0.619	1.6	0.040	0.037	0.044	μA
$I_{V_{PPQ}}$ Low	2689	2338	0.976	1.16	0.002	0.009	0.002	0.003	0.030	μA
Min V_{PP}	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	V
Source Current (@V_{OH} = 299V)	-179.4	-150.3	-182.8	-149.9	-179.1	-149.9	-218.1	-149.9	-177.8	μA
Sink Current (@V_{OL} = 1.00V)	401.7	311.5	401.7	353.8	401.7	387.6	401.7	387.6	401.7	μA
Energy (rising edge)	28.0		4.97		4.80		4.80		0.163	μJ
Energy (falling edge)	5.87		4.38		0.049		0.049		0.053	μJ
Area (sum of components)	95,188		163,114		122,049		122,991		133,653	μm2

Circuit 3 also offers low power consumption compared to circuits 1 and 2, however, reduced operating frequency limits its use in high speed applications. The higher rise time is explained by reduced voltage drop across the gate of the EDPMOS due to process variations of the HV resistor in the fabricated device. Circuit 4 achieves the fastest measured rise time because the voltage drop across the gate of the output EDPMOS is larger than the 5 V drop used by the other circuits. Excluding the area and power consumption contributions from the bias generation, circuit

4 also exhibits the lowest area and power dissipation combination among all other designs.

The dynamic level-shifter achieves comparable performance and area with circuit 4, replacing the bias generation with a method of generating control pulses. The higher current consumption in the output high state is a result of the large capacitance seen at the gate of the EDPMOS (illustrated by the additional voltage drop on V_{DP2} in circuit 4 and V_{GP6} in circuit 5 when the input goes high). Though circuit 2 offers reduced power dissipation from circuit 1, an increase in area and reduced operating frequency is the trade-off. Circuit 1 offers the smallest area but at the expense of high power consumption.

6.4.4 Conclusion

Eliminating reliance on large, bulky and external power supplies and relays is a large-step forward towards a compact and portable microfluidic LOC system. We have developed a system capable of generating and switching the high-voltages required for millimeter to centimeter microfluidic operations. We have demonstrated that our DC-DC boost converter system can successfully generate up to 150 V and potentially even 300 V with a sufficient external diode, and that our level-shifter circuits offer the low power consumption required to operate off the low-current source capability of the on-chip power supply. Future work will involve examining alternative ways of generating the bias voltage required for the full-static level-shifters, and pursue dynamic approaches to obtain even lower power consumption while maintaining or even surpassing current performance.

Chapter 7

Communication and Control Interface

The optical detection, high-voltage generation and output switching components of the complete integrated system have already been presented. Furthermore, the analog-to-digital converter, which is capable of converting the information gathered from all of these systems and converting it to a digital code, has also been presented. The remaining component, the communication and control interface (CCI), is the final component that ties all of these units together. Figuratively speaking, the CCI is the brains of the system, capable of controlling the operations of the different components and communicating information to the chip and off the chip. In the first section, motivation behind its presence is discussed, followed by the specific requirements. Background about the serial peripheral interfaces (SPI) (the communication protocol used for communication) is then provided. Finally, the design, simulation and testing results of the fabricated device is presented.

7.1 Motivation

A core is required that is capable of communicating information and commands with an off-chip device. The off-chip device should be able to control the operation of the device and receive information regarding the status of the different components. By placing the control and communication interface on-chip, it allows for minimal off-chip components, furthering the goal towards an integrated solution.

7.2 Requirements

There are several key components that need to be controlled:

- Boost-converter: to be able to control the value of the HV generated on-chip.
- Output level-shifters: to be able to place the level shifters in one of three states (high voltage, float or ground).
- Analog-to-Digital Converter: inputs to the ADC should be selectable (between external voltage, current and voltage monitor and the transimpedance amplifier).
- Transimpedance Amplifier: control of the operating frequency (i.e. integration period) of the transimpedance amplifier.
- Reset: a system wide reset to place the system into a known state.

Therefore, there must be a method to send commands to the chip to perform the specific operation for each component, and there must also be a method of receiving information from the chip regarding the status of the different components (e.g. from the ADC). Finally, because of the limitations placed due to the larger (0.8-μm process) feature size, the digital logic must be as compact as possible to prevent excess area consumption.

7.3 Serial Peripheral Interface Background

Based on the above mentioned requirements, custom control logic was implemented around a serial peripheral interface (SPI). The serial peripheral interface is a synchronous serial data link which requires three control signals: a clock (SCK), a master-out-slave-in (MOSI), and a master-in-slave-out (MISO). Between a master and a slave, the SPI module operates as a large shift register (as illustrated in

Fig. 7.1) where the data leaves the master and is shifted into the slave through the MOSI pin, and data leaves the slave and enters the master through the MISO pin. A common clock (SCK) is used by both the master and the slave and is generated by the master. The slave just sends and receives data, and can only do this when the master generates the necessary clock signal. The master however generates the clock signal only while sending data. Thus, the master has to send data to the slave to read data from the slave. To allow the master device to communicate with multiple devices, an additional active low chip select (CS) signal is used. By setting CS high for a specific slave, the device ignores all incoming commands, only the device with CS low can accept commands or respond.

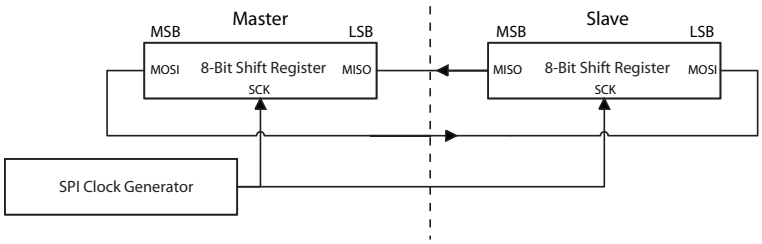

Figure 7.1: The SPI protocol works around one big shift register split between the master and the slave device.

To account for delays that may occur through the communicating channel (e.g. wire) which may cause the data from improperly latching when clocked on the same edge, the data is sent on either the rising or falling edge and is read on the complementary edge. Different devices operate in one of four different SPI modes (Table 7.1) dependent on the setting of two control bits, CKP and CKE [64]. CKP (clock polarity select) determines if the clock idles low or high and CKE (clock edge select) determines when the data is transmitted relative to the clock (SCK).

Table 7.1: SPI Modes of Operation

CKP	CKE	SCK State	Transmit Edge	Read Edge	Mode Name
0	0	Idle low	Rising	Falling	Mode (0,1)
0	1	Idle low	Falling	Rising	Mode (0,0)
1	0	Idle high	Falling	Rising	Mode (1,1)
1	1	Idle high	Rising	Falling	Mode (1,0)

7.4 Design

Because of unavailability of tools, the communication and control interface was custom designed at the gate level but laid out with the tools. Furthermore, of the four modes available, Mode (1,1) was selected because it was compatible with the existing protocols used by other members involved in this project. In the following section, the top-level design followed by the different subsections is discussed.

7.4.1 Top-Level

The communication and control interface is composed of three main components (illustrated in Fig. 7.2):

1. Shift register and decoder logic: which respectively sample and interpret the data.

2. Register file: contains the registers for control over the ADC, HV outputs, HV supply output voltage and the general control register.

3. ADC: contains the successive-approximation ADC and outputs data through the MISO pin on the falling edge to the master device.

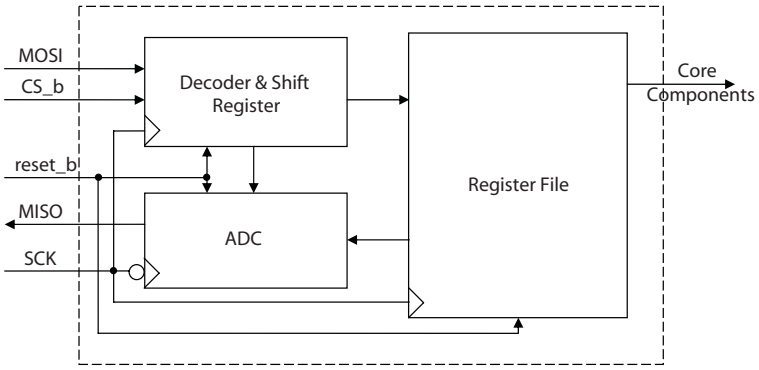

Figure 7.2: High-level overview of the SPI components.

Along with the three main input/output signals (i.e. SCK, MISO, MOSI), two additional signals were added:

1. CS_b: Is an active low chip select signal. When high, the MISO pin is in a high impedance state and the SPI module ignores incoming data. When transitioning to the active low state, it resets the internal counter while maintaining the current state for all the other registers.

2. reset_b: is an active low reset signal. When this signal is low, the internal counter and the registers are cleared, the high voltage outputs are put in a safe (floating) state, and the target Vpp voltage (to be generated) is set to 0 V.

7.4.2 Shift-Register and Decoder Logic

Though data transmission in SPI may involve any number of clock cycles, an 8-bit data packet scheme was chosen to conform with the 8-bit SPI read and write commands of the PIC Microcontroller being used to interface with the HV CMOS chip. Using this convention, the three MSB bits represent an opcode, while the five remaining bits represent the data. The different opcode and data combinations is briefly presented in Table 7.2.

Table 7.2: CCI Valid Opcode and Data Sequence

Opcode	Data	Description
000	XXXXX	NOP
001	UDDDD	Vref control register
010	AAADD	HV outputs control register
011	AAAVO	ADC control register
100	OPTHL	General control register
101	XXXXX	NOP
110	XXXXX	NOP
111	XXXXX	Synchronous reset

Table 7.3: 8-bit Gray code

Decimal	Binary
0	000
1	001
2	011
3	010
4	110
5	111
6	101
7	100

A 3-bit Gray counter is used to keep track of the arriving bits. Illustrated in Table 7.3, a Gray counter takes advantage of the fact that successive values differ in only one digit to reduce the presence of logic glitches (which occurs due to the delay in logic values changing, and momentarily holding a previous value). The Gray counter beings at zero, and once it has been incremented by three, it

indicates the opcodes have arrived. The opcodes are then processed by a basic 3-to-8 decoder. The one (out of eight) output that goes high, sets the respective register in the register file active, and the register in the register file simply shifts in the incoming remaining data bits. The relationship between these components is illustrated in Fig. 7.3.

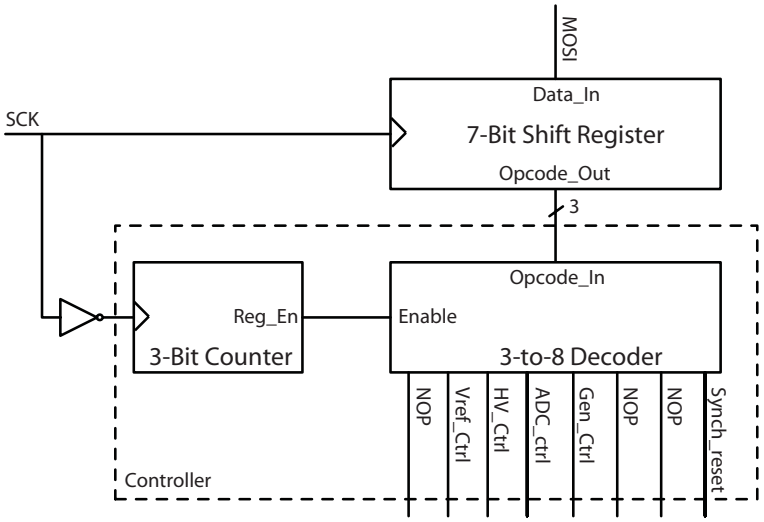

Figure 7.3: SPI Decoder and shifter register logic.

The communication and control interface supports only one read-from-slave command while all other commands write to the device (to perform a specific operation). The only information the CCI can send to the master is the 8-bit digital code from the ADC. The CCI requires one operation (i.e. one 8-bit packet) to turn the ADC on and to select which line the ADC samples from. Immediately following this packet, the slave device begins to output the 8-bit digital code. As per the ADC chapter, one bit is then generated each cycle from the ADC, and this bit is transmitted by the MISO pin on the falling edge. A simulation showing an ADC opcode read, followed by turning on the ADC, sampling the input signal, then the final conversion to the digital code output on the MISO pin is illustrated in Fig. 7.4.

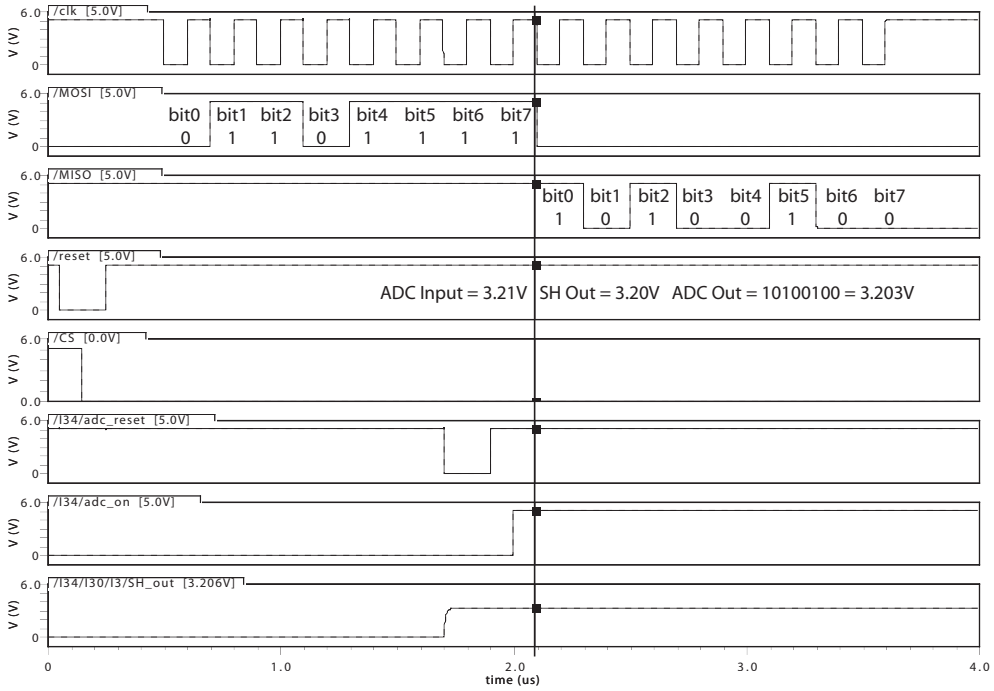

Figure 7.4: ADC operation through the CCI.

7.4.3 Register File

The register file contains all of the registers that control the different components. The registers are activated by the control in the shift-register and decoder logic component and read the bits on the rising edge of the clock. Once the values are written into the register, the respective combinational logic becomes active immediately, making use of the information in the registers. Fig. 7.5 illustrates the different registers available in the register files and their responsibility.

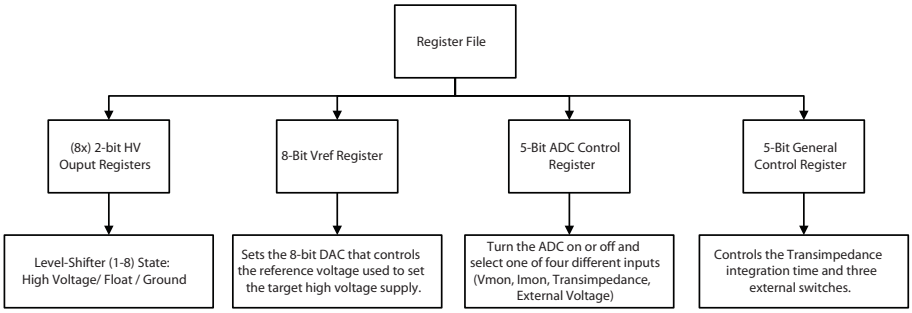

Figure 7.5: The register file contains a register for each component, with each representing a different function.

7.5 Testing

The operation of the communication and control interface was verified on the fabricated chip ICKAALC3. Several different tests were done to ensure complete operation of the CCI. The basic test setup used is illustrated in Fig. 7.6, and the separate tests are highlighted in the subsections below:

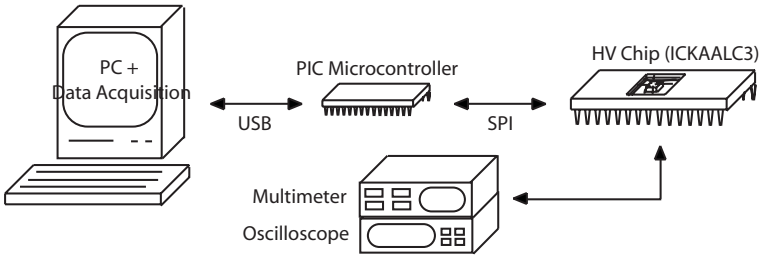

Figure 7.6: The setup used to test ICKAALC3 and verify the CCI operation.

The basic test setup consisted of a computer running hyperterminal interfaced through a USB to an FTDI USB to Serial chip that was then interfaced to a 16F877 PIC Microcontroller. The PIC microcontroller was preloaded with the required compiled commands. On running the program, different opcodes and hence chip operations could be selected. Furthermore, data could also be read from ICKAALC3 through the PIC and captured in hyperterminal for further processing.

7.5.1 Switch Test

Three different digital switches were added to control various external devices including:

1. Heater Switch (opcode: 100XXXHX): a switch to turn on and off an external resistive heater used in PCR (polymerase chain reaction) applications.

2. Valve Switch (opcode: 011XXXVX): a switch to control an external valve or pump used in PCR applications.

3. Light Switch (opcode: 100XXXXL): a switch to control either a laser or LED driver used for fluorescence detection.

Testing these three switches was the easiest method to verify correct functionality. The chip was sent the specific the three above mentioned opcodes and the specific pins were monitored. Toggling indicated correct operation.

7.5.2 High-Voltage Outputs

The control of the high-voltage output registers was tested by applying an external high-voltage and toggling the states of the outputs. Initially 15 V, then up to 300 V was applied while the different outputs were monitored using a 10 MΩ load (i.e. from the multimeter resistance). There are eight separate high-voltage outputs, five of which support high-voltage, float and a ground state (i.e. are tri-state), and three of which support just ground and float state (i.e. are bi-state). All channels were tested and fully functional.

From Table 7.2, the high-voltage outputs register supports three additional address bits and two data bits. The three address bits specify the differen to output channels while the two data bits determine the state of the high-voltage output. For the data bits, the first bit sets whether the channel is on or off (floating) while the second bit determines its high or low value. The address and the corresponding output channel is specified in Table. 7.4 while the data bit and its respective output state is presented in Table. 7.5.

Table 7.4: High-Voltage Output Channel Addressing Scheme

Address	Channel	Type
000	Channel 1	Tri-state
001	Channel 2	Tri-state
010	Channel 3	Tri-state
011	Channel 4	Tri-state
100	Channel 5	Tri-state
101	Channel 6	Bi-state
110	Channel 7	Bi-state
111	Channel 8	Bi-state

Table 7.5: High-Voltage Output Channel State Setting Scheme

Decimal	Binary
00	Floating
01	Floating
10	Ground
11	High-Voltage

7.5.3 General Control Register

Besides the two controls switches (i.e. heater and valve), the general control register contains three other control bits:

1. PWM (opcode: 100XPXXX): Allows the user to select between an internally generated frequency source for the boost converter switch or an externally generated source.

2. Output channel (opcode: 100OXXXX): by toggling this switch, the all of the high-voltage outputs can be turned off or on directly.

3. Transimpedance amplifier clock (opcode: 100XXTXX): by toggling this bit at different frequencies, the transimpedance amplifier integration time can be varied.

All three of these are essential switches for their respective components, and all have been verified individually to ensure their proper operation.

7.5.4 ADC Control Register

The ADC control register allows the ADC to be turned on or off to conserve power. When on, by selecting a specific address, different inputs to the ADC can be selected. The input choices are listed in Table. 7.6. The ADC operation has been

Table 7.6: ADC addressing scheme.

Address	Input Source
000	Voltage monitor
001	Current monitor
010	Transimpedance amplifier output
011	External voltage input
1XX	Undefined

verified using the external input voltage. The results of this are presented in the ADC section and will not be repeated here.

7.6 Conclusion

Though methods of optical detection, analog-to-digital conversion and high-voltage generation are essential for microfluidic operations, a means of communicating controls and data between the LOC and off-chip is crucial. We have developed a compact control logic, which uses the serial peripheral interface protocol to communicate off-chip. We have demonstrated its functionality both through simulation and verification of the fabricated device. This communication and control interface is sufficiently robust to accommodate future commands and data additions with rapid and minimal modification. Not only is the design robust, but by using the SPI protocol, varying clock frequencies (while considering the minimum clock frequency required for the ADC operation) can be used allowing the system to be interfaced to various external controllers. Future versions will offer the ability to read from registers, rather than simply outputting an ADC value, and potentially even allow the device to act as a master, rather than passive slave device, and thus send commands to other devices off-chip devices (or even multiple HV CMOS chips).

Chapter 8

System Chips

In this chapter, the design of four generations of high-voltage CMOS controllers are presented and compared.

8.1 Motivation

There has been much work in both academia and industry towards complete and portable microfluidic platforms. However, to the best of the authors knowledge, there has not yet been a published report of such a complete system capable of integrating the high-voltage generation, optical detection and control circuitry on a single substrate. Building on the components presented in earlier chapters and through the evolution of four generations of HV CMOS microfluidic controller designs, this works aims to present such a solution.

8.2 Requirements

A complete system composed of HV generation, optical detection and control and readout circuitry for microfluidic applications is required. The system must be able to generate and switch up to 300 V and source 60 μA to at least four output channels during which it must also be able to detect low optical powers (i.e. 0.1 pW to 100 pW) emitted from fluorescently marked and excited analytes. The system must be capable of receiving control commands and transmitting information (such as optical power measurements) between itself and an external device (e.g. computer).

8.3 Designs

To accomplish the above goals, four generations of continually improved up HV CMOS chips were designed. The first chip was designed exclusively by Leendert van den Berg and is discussed here for completeness. The second generation chip was designed by Maziyar Khorasani and Leendert van den Berg with additional components designed by Philip A. Marshall. The third chip was designed by Maziyar Khorasani, Mohammad Behnam, Meysam Zargham and Philip A. Marshall and fourth chip was designed by Maziyar Khorasani and Philip A. Marshall.

8.3.1 Generation 1: ICKAALOC

8.3.1.1 Design

The first HV CMOS controller designed was ICKAALOC (Fig. 8.1). The chip specifications are summarized in Table. 8.1. The chip has three tri-state (high-voltage, high-impedance, and ground) outputs and one bi-state output (high-impedance or ground). The level-up stage is illustrated in Fig. 8.2 and relies on pull-up resistors to prevent gate oxide breakdown of the HV PMOS transistors (as described in Section **??**).

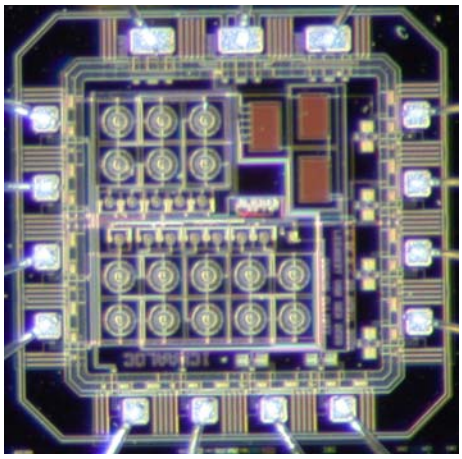

Figure 8.1: Die photo of ICKAALOC

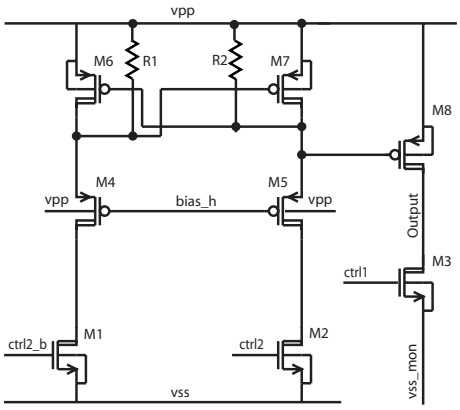

Figure 8.2: ICKAALOC level-shifter with pull-up resistors.

The high-voltage outputs are controlled using three digital input pins. An on-chip voltage-divider is responsible for generating the bias for the level-up stage. An

on-chip boost converter with an internal diode and two pull-down transistors is also present. There is no on-chip oscillator or boost controller, rather must be provided from an external source.

Table 8.1: ICKAALOC Specifications

Specification	Value
Dimensions	2 mm x 2 mm
Pins	15
Control logic	3 digital input pins
Output drivers	3 Tri-state
	1 Bi-state
Level-up stage	Static with resistive pull-ups
Voltage Divider	R_{Total} = 24 MΩ
	R_{Vpp--} = 1.44 MΩ
	R_{Vmon} = 240 kΩ
Boost converter	Internal diode (PEG21FA)
	2 NDG20FD Pull-downs

The simulated total static power consumption is about 1.54 mW (with a 300 V power supply) excluding the boost converter operation. Of this, the digital components contribute an insignificant 3.65 nW (static) with the majority of the current draw due to the voltage-divider. For its operation, the boost converter draws about 5.08 mA from the 5 V supply.

8.3.1.2 Verification

The relationship between the digital logic inputs and the high-voltage outputs has been verified, as has the operation of the voltage-divider used to generate the bias voltage for the level-up stage and the voltage monitor (which should 1% of the high-voltage supply). Fig. 8.3 illustrates the ideal values of the voltage divider versus measured. The visible deviation is not completely unexpected as the DALSA documents suggest possible variation of about $\pm 3\,k\Omega$ in the fabricated result.

8.3.1.3 Experimental Results

Using the setup illustrated in Fig. 8.4, consisting of an external power supply operating at 150 V, and external CCD based optics (discussed in the Appendix X),

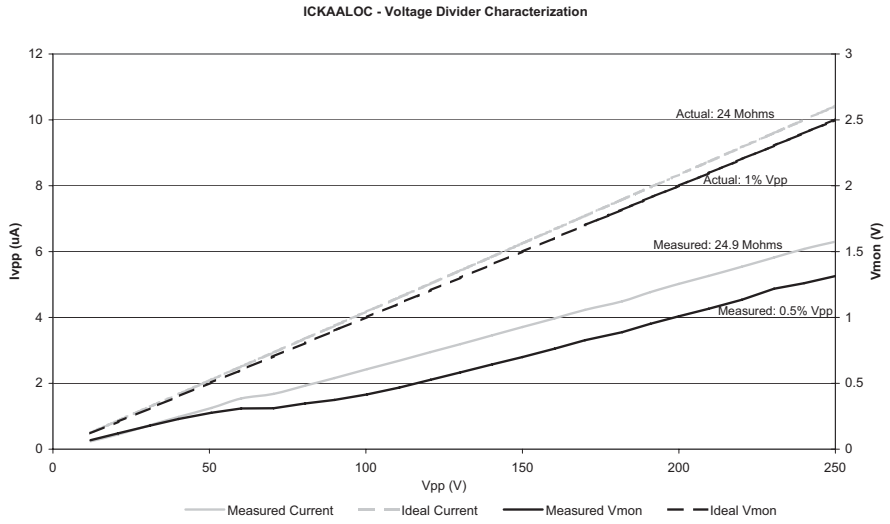

Figure 8.3: ICKAALOC voltage-divider measured versus ideals results.

a electropherogram of a successful microfluidic separation of ALFExpress from Pharmacia is illustrated in Fig. 8.5. ALFExpress is a 50-500 base pair DNA sizer (a sample with known number of base pairs, in this case ten plus one primer peak) used for calibration in genetic analysis and mutation detection.

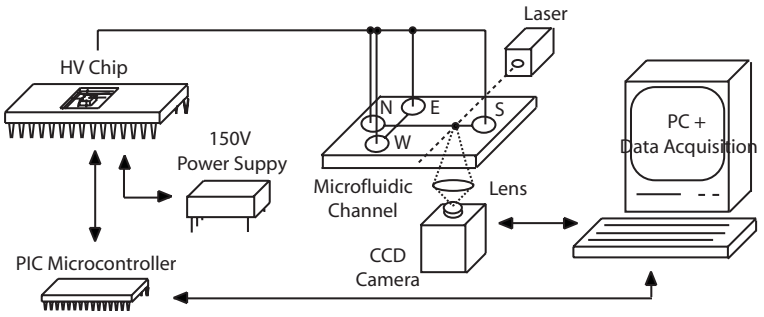

Figure 8.4: Setup for using ICKAALOC for switching the HV required for microfluidic CE of ALFExpress.

8.3.2 Generation 2: ICKAALC2

8.3.2.1 Design

Besides the addition of a control and communication (i.e. SPI) interface, ICKAALC2 (illustrated in Fig. 8.1) makes several improvements over ICKAALOC.

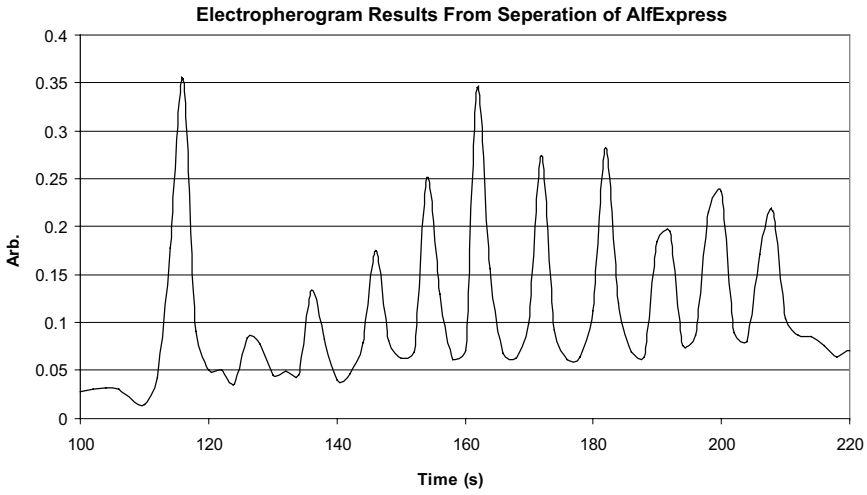

Figure 8.5: Electropherogram results of the separation of AlfExpress at 150 V.

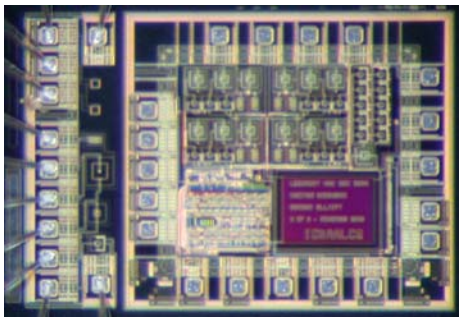

Figure 8.6: Die photo of ICKAALC2

All four outputs are now tri-state, and the resistive pull-up level shifter is replaced with the PMOS2 implementation (Arch. 3 from Section **??**). The voltage-divider resistance is increased as is the number of pull-downs in the boost converter, respectively decreasing current draw and increasing boost converter efficiency. A boost control circuit (discussed in Section 6.3), along with a current controlled oscillator is also added. ICKAALC2 component listing is provided in Table. 8.2.

In regards to testing, there exists some problems between the control logic and level-shifters, preventing further characterization.

Table 8.2: ICKAALC2 Specifications

Specification	Value
Dimensions	2 mm x 2.2 mm
Pins	19
Communication	Serial peripheral interface
Output drivers	4 Tri-state
Level-up stage	Static cross-coupled PMOS
Voltage Divider	R_{Total} = 605 MΩ
	R_{Vpp--} = 21.175 MΩ
	R_{Vmon} = 6.05 MΩ
Boost converter	Internal diode (PEG95EA)
	8 NDG20FD Pull-downs
	Current controlled oscillator
	Boost controller

8.3.3 Generation 3: ICKAALC3

8.3.3.1 Design

The third generation HV CMOS controller, ICKAALC3 (illustrated in Fig. 8.7), has thus fur been the most successful of all of the designed chips. This chip has the improved communication and control interface (CCI) discussed in Chapter 7 along with an 8-bit ADC, five tri-state and three bi-state high-voltage outputs and an integrated photodiode along with transimpedance amplifier. The voltage-divider, voltage monitor current monitor, level shifter circuit, boost converter and boost controller are reused from ICKAALC2, but are now interfaced to the on-chip CCI (and ADC). Table 8.3 summarizes the chip features. The most novel feature is the presence of electrodes on the die for future post processing of the microfluidic channels directly on the chip.

8.3.3.2 Verification

ICKAALC3 has been the most completely characterized chip thus far, and the results have been presented throughout this thesis. The results presented in each chapter regarding the CCI, ADC, transimpedance amplifier with the photodiode and the boost converter (up to 150 V with an external diode) have been derived from this chip and so will not be revisited.

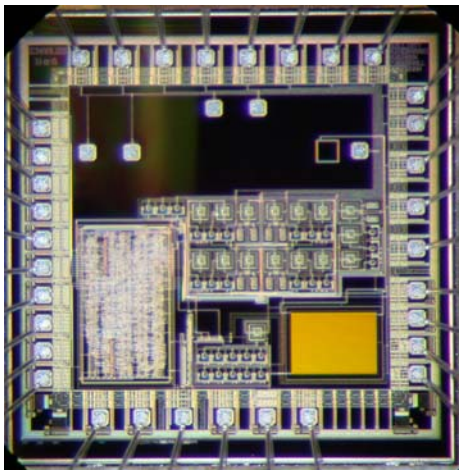

Figure 8.7: Die photo of ICKAALC3

Table 8.3: ICKAALC3 Specifications

Specification	Value
Dimensions	3 mm x 2.9 mm
Pins	33
Communication	Serial peripheral interface
Output drivers	5 Tri-state
	3 Tri-state
Level-up stage	Static cross-coupled PMOS
Voltage Divider	R_{Total} = 605 MΩ
	R_{Vpp--} = 21.175 MΩ
	R_{Vmon} = 6.05 MΩ
Boost converter	Internal diode (PEG95EA)
	8 NDG20FD Pull-downs
	Current controlled oscillator
	Boost controller
Optical detection	150 μm x 150 μm photodiode
	PC transimpedance amplifier
On-chip electrodes	5

8.3.3.3 Experimental Results

Similar to Section 8.3.1.3, microfluidic CE separation has been accomplished using this chip. Unlike the case for ICKAALOC where the chips primary function was to switch the HV outputs, in this experiment, ICKAALC3 not only switched the outputs, but also generated the required (150 V) voltage. The experimental setup is similar to Fig. 8.4 and uses the same ALFExpress sample, except the 150 V power

supply is generated on-chip. The electropherogram result is given in Fig. 8.8.

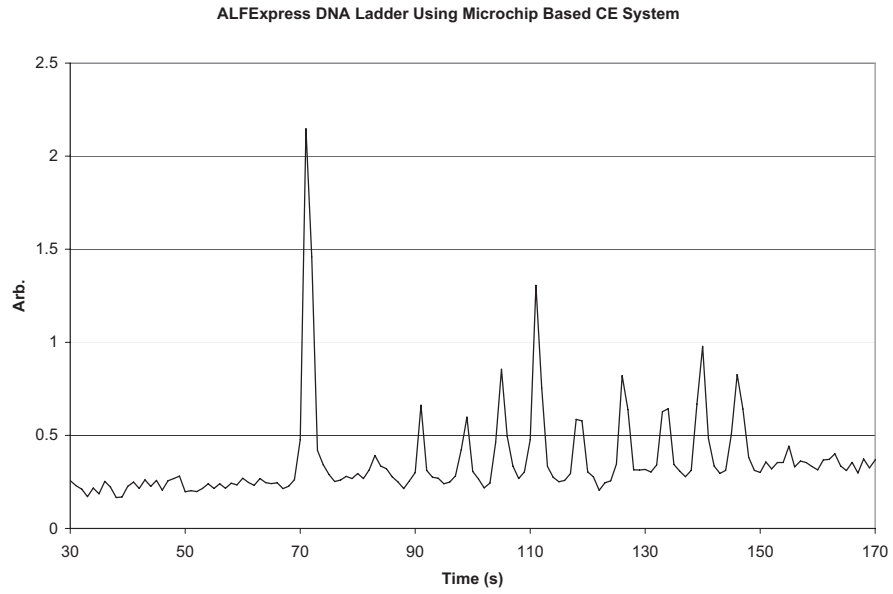

Figure 8.8: Electropherogram results of the separation of AlfExpress at 150 V.

8.3.4 Generation 4: ICKAALC4

8.3.4.1 Design

ICKAALC4 (illustrated in Fig. 8.9) is the largest chip design yet with an improved 12-bit ADC, heater switch capable of switching up to 300 mA (as required by an external platinum heater), and avalanche photodiode detection (and related circuitry). Though still containing five tri-state and three bi-state HV outputs, the static level-up stages have been replaced with dynamic variants (Section **??**) where the logic operates based on a fully synchronous design using the on-chip 10 MHz clock. The on-chip 10 MHz clock is generated using a 15 stage current controlled oscillator (CCO) which allows either an external or internal current control. Finally, the low-voltage digital (e.g. for the CCI) and noise sensitive logic (e.g. ADC), along with the high-voltage components (e.g. boost converter) have been placed in separate wells to provide isolation and reduce noise. In regards to verification however, this design is currently undergoing testing.

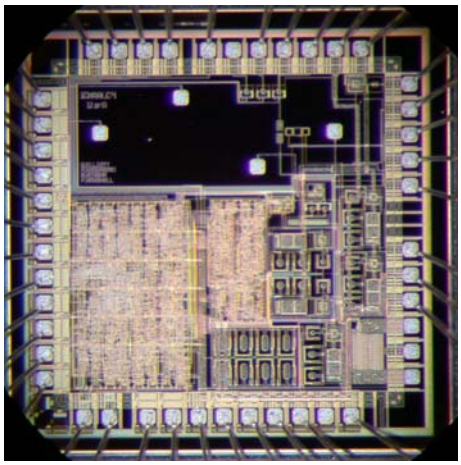

Figure 8.9: Die photo of ICKAALC4

Table 8.4: ICKAALC4 Specifications

Specification	Value
Dimensions	3.22 mm x 3.22 mm
Pins	45
Communication	Serial peripheral interface
Output drivers	5 Tri-state
	3 Tri-state
Level-up stage	Fully dynamic
Boost converter	Internal diode (PEG95EA)
	8 NDG20FD Pull-downs
	Current controlled oscillator
	Boost controller
	3 voltage monitors
Optical detection	150 μm x 150 μm photodiode
	PC transimpedance amplifier
	Avalanche photodiode
	APD active quenching circuit
On-chip electrodes	4
Heater switch	Switch up to 300 mA

8.4 Conclusion

Four generations of microfluidic controller integrated circuits have been designed and presented. Capable of varying levels of integration, from high-voltage generation and optical detection to high-current switching, these systems bring portable and hand-held POC diagnostic systems much closer to reality. The first genera-

tion chip is capable of only high-voltage generation and switching. The second version improved the logic, communication interface and the performance of the entire system. The third version provided a significant advance by integrating optical detection and offering the possibility of post-processing microfluidic channels directly on the die. The fourth version made improvements on the third by using dynamic level-shifters and offering a higher-resolution ADC and provided high-current switching capabilities. In addition, two test chips provided space to characterize components individually, and to explore additional components that might be placed on future chips. Future work will involve the integration of additional components required for complete analysis, such as controls for PCR heaters and microcoils for movement of magnetic beads, as well as optimization of existing designs.

Chapter 9

Conclusion and Future Direction

9.1 Summary

In this thesis, the problem of integration for microfluidic systems has been addressed at both the component level and at the system level. The three main components for a microfluidic controller, including the high-voltage generation, optical detection and control and communication, has been discussed in depth. These components were then integrated in a complete HV CMOS microfluidic controller capable of generating and switching sufficient voltages to accomplish capillary electrophoresis.

Chapters 2 and 3 provided background information and reviewed existing works respectively. Chapter 4 provided an in depth review of CMOS compatible optical detection methods, components and circuits. Chapter 5 delved into analog-to-digital converters and digital-to-analog converters required in processing analog values generated on-chip to allow for off-chip communication. Chapter 6 discussed the method of high-voltage generation and switching and Chapter 7 ended with the communication and control interface, the core required to connect all of these individual components together.

9.2 Future Direction

Currently, capillary electrophoresis separation of analytes on microfluidic channels is only one step in creating a truly complete analysis system. There is preprocess-

ing of the sample through polymerase chain reaction (PCR) that occurs before the analysis. Thus, the initial future objective should be to able to provide the circuitry that can help accommodate PCR on the same platform being currently used. This requires innovative methods of controlling resistive heaters, measuring temperature and controlling valve switches (among many things).

Further, electrophoresis actuation of analytes is not the only means available on a CMOS processes. As mentioned in the literature review chapter, research has explored methods of moving particles using inductor coils to generate magnetic field for actuation of analytes tagged with magnetic beads. Similar research should be done to determine whether the DALSA HV kit can support such techniques.

Improvements in the area of optical detection including avalanche photodiode circuitry and phototransistors, as detectors with internal gain, provides a very attractive solution to current transimpedance amplifier approaches using basic photodiodes.

Finally, besides using boost converter circuits requiring large external inductors, capacitors and diodes, future work should revisit charge pump circuits, which provide on-chip solutions, requiring no external components.

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