Electrothermal Transient Behavioral Modeling of Thyristor-Based Ultrafast Mechatronic Circuit Breaker for Real-Time DC Grid Emulation

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***Abstract*—The accuracy of power electronics simulation relies on the semiconductor switch model employed. Thus, in this paper where an ultrafast mechatronic circuit breaker (UFMCB) is implemented in real-time on the field programmable gate array, a detailed nonlinear thyristor model is proposed for extra device-level information regarding design evaluation. The cascaded thyristors impose a heavy computational burden on the UFMCB simulation, and node elimination is achieved following the proposal of a scalable thyristor model. For the convenience of the circuit breaker's integration into dc grid, a pair of coupled voltage–current sources is inserted as its interface, which achieves a reduction in the dimension of system admittance matrix, and the subsequent proposal of a relaxed scalar Newton–Raphson method further expedites the simulation by decomposing the nodal matrix equation. Meanwhile, the modular multilevel converter as a dc grid terminal adopts half-bridge and clamped double submodule topologies to test system performance in conjunction with the UFMCB. Real-time execution is achieved and the results are validated by ANSYS/Simplorer and PSCAD/EMTDC in device- and system-level, respectively.**

***Index Terms*—Clamped double submodule (CDSM), electrothermal, field programmable gate array (FPGA), hardware-in-loop (HIL), high-voltage direct current (HVdc), hybrid HVdc breaker (HHB), modular multilevel converter (MMC), real-time systems, thyristor model.**

I. Introduction

THE high-voltage direct current (HVdc) system with a meshed or radial network of dc lines is a promising configuration for the power transmission [1]–[3], where the modular multilevel converter (MMC) is favored due to merits, such as high power quality, modularity, and scalability. However, the rapid current rise following the dc side fault is a prominent drawback of the HVdc grid, and a potential power transmission interruption to the receiving terminals requires that the fault be isolated immediately [4], [5].

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Blocking the insulated-gate bipolar transistors (IGBTs) is insufficient to prevent feeding energy to the fault location with the most prevalent half-bridge submodule (HBSM) configuration since the freewheeling diodes still act as a rectifier; neither would that be expected if the station delivers power to other terminals. As a solution, various types of dc circuit breakers are investigated [6]. The hybrid HVdc breaker (HHB) can avert the hazardous impact by dc faults in a few milliseconds with 9 kA being the typical breaking capability [7] and has been intensively studied [8]–[10]. The mechanical breaker [11] and its solid-state counterpart [12] keep evolving to overcome shortcomings such as slow response and high energy consumption during fault interruption. The ultrafast mechatronic circuit breaker (UFMCB) with the fast thyristor as its main power semiconductor switch was also proposed for a lower cost and higher breaking capability, and the development is some steps ahead of most of its counterparts since it is among a few dc circuit breakers that have ever been tested in a high voltage and large current environment [13], [14]. Its system-level design procedures were also specified [15], and in these cases, the dc circuit breaker has only been tested in simple systems. For the design purpose, it is necessary to conduct the real-time simulation to gain a deeper insight into the UFMCB's performance in a more practical and complex electromagnetic environment such as the MMC-based dc grid where a variety of scenarios can be simulated to study the interaction between the dc circuit breaker and other components.

Meanwhile, for the UFMCB's design evaluation, an accurate insight into the status of its components, mainly the thyristors, under various operating conditions is required, e.g., the selection of an appropriate thyristor type with adequate capacity ensures normal operation while lowering the cost. Therefore, a device-level model with electrothermal dynamics [16], [17] is mandatory in the electromagnetic transient (EMT) simulation considering that the prevalent ideal switch with each state having a fixed value is incapable of revealing proper electrothermal dynamics of the silicon controlled rectifier (SCR).

The commercial offline device-level simulators play the aforementioned role in small-scale converters. However, in high-power applications, simulating dozens or even more those highly detailed nonlinear models—as well as the remaining system-level components—with a small time-step poses a huge computational burden on the processors, making the simulation extremely slow. In contrast, real-time hardware-in-loop (HIL)

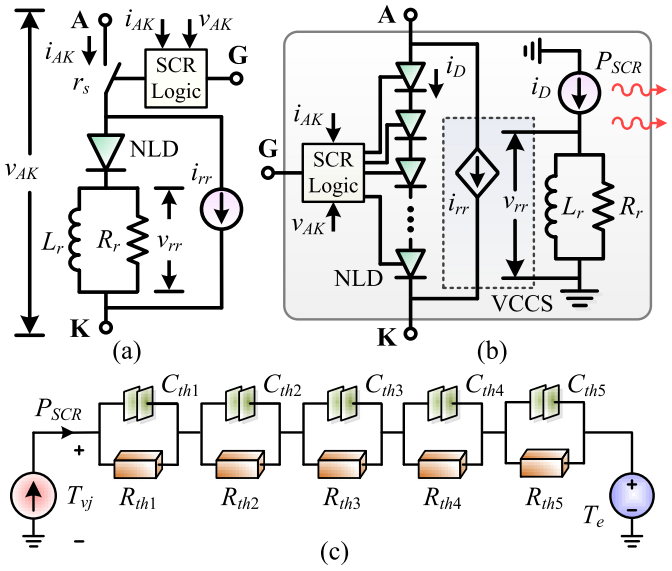

Fig. 1. Nonlinear behavioral thyristor model. (a) Single device. (b) Scalable thyristor model with (c) cascaded R–C network for thermal impedance.

emulation has been widely used due to its parallel hardware architecture and pipelined design [18]–[20], e.g., a full-scale HHB was deployed to the field programmable gate array (FPGA) with a low processing burden attributing to its high symmetry that enables internal circuit partitioning [21]. To simulate dc fault ride through, the MMCs with new submodule (SM) topologies are other option, such as the full-bridge SM[22], and the more economical clamped double submodule (CDSM) [23], [24] for requiring fewer switches per voltage level.

Therefore, this paper proposes a device-level UFMCB based on the nonlinear thyristor model for real-time testing of the HVdc grid on the FPGA, and the electrothermal interaction is established for prototype design guide. While the UFMCB's irregularity prohibits internal partitioning, it is separated from the dc grid for parallel processing; then the relaxed scalar Newton–Raphson (RSNR) method is proposed to avoid the conventional inefficient matrix equation solution.

The paper is organized as follows. Section II elaborates the nonlinear thyristor model. The UFMCB is discussed in Section III where the efficient RSNR solution is also specified. In Section IV, the HVdc grid modeling is introduced, and Section V narrates the hardware design on the FPGA. The HIL implementation results are presented and validated in Section VI, and Section VII provides the conclusions.

II. Nonlinear Device-Level Thyristor Model

The electrothermal model of a power semiconductor switch contains two parts that determine its junction temperature: the electrical part reflecting the total power loss and the transient thermal impedance. The major features taken into consideration in the thyristor electrical model are static I–V characteristics and the reverse recovery phenomenon. Fig. 1(a) shows the nonlinear behavioral model improved from the diode [25], to which an additional part implementing the SCR logic is added for determining its conduction behavior.

A. Basic Device Characteristics

The nonlinear diode NLD reflects the static ON-state characteristics between the thyristor's anode–cathode voltage v_{AK} and the current i_{AK}. It is approximated by the following analytical function:

$$v_{AK} = A + B \cdot i_{AK} + C \cdot \sqrt{i_{AK}} + D \cdot \ln(i_{AK} + 1) \quad (1)$$

where A, B, C, and D are temperature-dependent coefficients, which are either provided by the device manufacturer's datasheet or can be estimated according to the available I–V curves normally under 25 °C and 125 °C. Therefore, the four coefficients as a function of temperature can be linearly interpolated. To enable a low hardware latency, the static I–V characteristic is taken as a purely nonlinear resistor with its conductance determined by the current

$$G_{AK}(i_{AK}) = \frac{i_{AK}}{v_{AK}(i_{AK})}. \quad (2)$$

The SCR logic block distinguishes a thyristor from the diode. It turns ON after a positive pulse is exerted on the gate and a v_{AK} greater than the forward voltage drop V_{To}; it turns-OFF when the current i_{AK} vanishes and v_{AK} keeps below 0 over a period longer than the turn-OFF time t_q. Correspondingly, when the thyristor is under conduction, the controlled switch r_s exhibits a low impedance, otherwise it approaches infinity. Thus, in the model, NLD is enabled to be only in charge of ON-state characteristics.

The current source i_{rr} yields proper reverse recovery current whose value is dependent on the voltage over R_r–L_r pair, which has the following relation:

$$L_r = \frac{R_r}{\ln 10}\left(t_{\mathrm{rr}} - I_{\mathrm{rrm}}\left(\frac{dI_r}{dt}\right)^{-1}\right) \quad (3)$$

where t_{rr} and I_{rrm} are the reverse recovery time and peak current, respectively, and I_r is the reverse recovery current.

B. Scalable Cascaded Thyristor Model

The aforementioned nonlinear behavioral thyristor model contains four nodes. Different from the ideal switch, a device-level model has the mandatory requirement that its voltage and current should not exceed the actual ratings. Therefore, it is always organized in series or parallel to withstand high voltages or large currents, resulting in inefficient circuit solution and a deficiency of simulation hardware/software resource.

Fig. 1(b) presents a computationally efficient model for cascaded thyristors. The R_r–L_r pair is separated by means of a voltage-controlled current source since their values are too small to affect the static feature, and the NLD is merged with the SCR logic part to eliminate internal nodes. The NLD, along with i_{rr}, participates in external circuit solution. Following the acquisition of the diode static current i_D, the voltage over the R_r–L_r

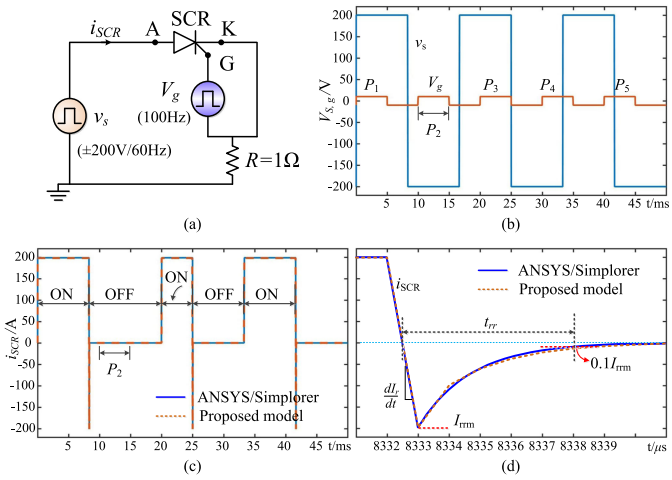

Fig. 2. Thyristor model validation. (a) Test circuit. (b) Source and gate voltages. (c) and (d) Thyristor current.

pair $v_{\rm rr}$ can be calculated, and the reverse recovery current is

$$i_{\rm rr} = K \cdot v_{\rm rr} = K(i_D - I_{L\rm eq})(G_{Lr} + R_r^{-1})^{-1} \tag{4}$$

where K is a coefficient, and G_{Lr} along with $I_{L\rm eq}$ constitutes the companion model of the inductor.

Fig. 2 shows the waveforms of the proposed thyristor model, and they are validated by ANSYS/Simplorer which employs a different detailed physics-based thyristor model. It is noticed that even when the gate voltage V_g is positive at P_2, the SCR keeps OFF since the forward voltage v_s is negative.

C. Dynamic Electrothermal Interaction

In the EMT simulation, the variables are in discrete time-domain. Thus, the SCR power loss of an arbitrary period is discretized using the second-order Trapezoidal rule

$$P_{\rm SCR} = \frac{\int_{T_0}^{T} v_{AK}\, i_{AK}\, dt}{T - T_0} = \frac{\sum_{n=1}^{N_t} \left(v_{AK}^n i_{AK}^n + v_{AK}^{n+1} i_{AK}^{n+1}\right) \Delta t}{2(T - T_0)} \tag{5}$$

where T_0 and T are the time instant when the integration starts and ends, and N_t is the number of discrete sections. To ensure the accuracy, $P_{\rm SCR}$ is calculated in each time-step, and therefore, $T - T_0$ should be the time-step Δt and $N_t = 1$.

The power loss is eventually dissipated in the form of heat, leading to the junction temperature rise. To maintain a compact size as well as a low cost, the external cooling system is not included in the UFMCB. According to the device datasheet [26], the inherent transient thermal impedance of the thyristor is composed of five parts

$$Z_{\rm th} = \sum_{i=1}^{5} R_{{\rm th}(i)} \left(1 - e^{\frac{-t}{\tau_i}}\right) \tag{6}$$

where $R_{{\rm th}(i)}$ is the thermal resistance and τ_i is the time constant. Consequently, the transient thermal impedance can be depicted by five serial R–C pairs, as shown in Fig. 1(c) where the

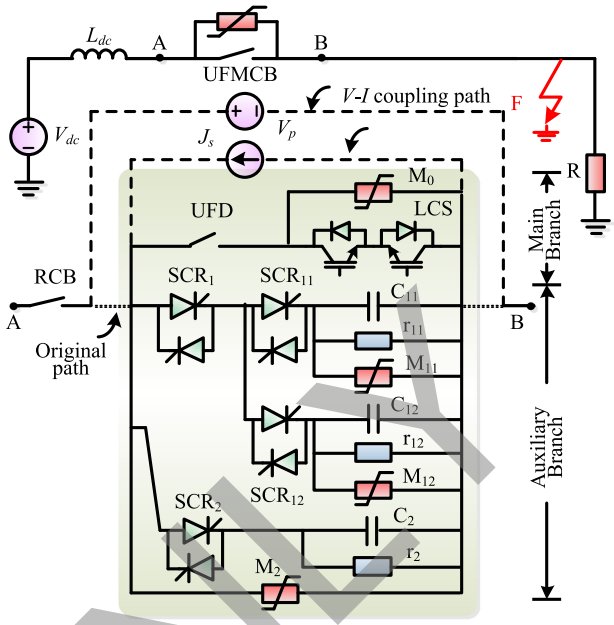

Fig. 3. Bidirectional UFMCB decoupled from transmission path.

capacitor is calculated by

$$C_{{\rm th}(i)} = \tau_i {R_{{\rm th}(i)}}^{-1} \tag{7}$$

and the current source is numerically equal to $P_{\rm SCR}$ since the SCR power loss is diffused through the thermal impedance and causes the junction temperature to rise from initial 25 °C. Meanwhile, the ambient temperature is set $T_e = 25$ °C and, therefore, can be modeled as a constant voltage source. As a result, the instantaneous junction temperature, deemed as the voltage over the input current source, is calculated by

$$T_{vj}(t) = \sum_{i=1}^{5} \frac{P_{\rm SCR}(t) + I_{{\rm his}(i)}(t - \Delta t)}{R_{{\rm th}(i)}^{-1} + G_{C{\rm th}(i)}} \tag{8}$$

where $I_{{\rm his}(i)}$ and $G_{C{\rm th}(i)}$=$2C_{{\rm th}(i)}/\Delta t$ are the history current and the equivalent conductance of the ith capacitor's companion model, respectively. Finally, these temperature-sensitive parameters of the SCR are updated for the next time-step.

III. Ultra-Fast Mechatronic Circuit Breaker

A. UFMCB Model Description

Fig. 3 shows the topology of a bidirectional UFMCB, which is symmetric since all unidirectional components have their counterparts in an opposite direction. In the proposed EMT simulation of the HVdc grid, the source $V_{\rm dc}$ is replaced by an MMC, and therefore, a heavy computational burden is imposed by the device-level UFMCB and the MMC if not simplified. In this paper, the MMC fully detailed model instead of the average value model is preferred since the latter is proved to be less accurate regarding dc fault [27]. Meanwhile, the UFMCB model is anyhow a major source of the computational burden since it contains a large number of nodes and nonlinearities that as a consequence require an iterative computation process

to be completed in a small time-step. Thus, as an independent apparatus, the UFMCB is separated from the dc yard by a pair of coupled voltage–current source. The impact of the UFMCB on dc grid is realized by the voltage source V_p, which means when the dc yard operates without any circuit breaker, its configuration remains the same by setting V_p constant zero. Meanwhile, although all SCRs are connected in an antiparallel manner to accommodate bidirectional power flow, no additional node is induced in the EMT model.

In the main branch (MB), the principle of the dc breaker decides that the load commutation switch (LCS) always turns ON and OFF under a low voltage clamped by the auxiliary branch [15], meaning its primary power loss is induced by normal conduction. Therefore, the switching transients can be ignored and the LCS is taken as a current-dependent resistor, whose conductance G_{LCS}, according to the static I–V characteristics in the manufacturer's datasheet, can be calculated by the terminal voltage divided by the current, as in (2). The IGBT nonlinear I–V characteristics are piecewise linearized with each taking the form of

$$i_C = k_1(T_{vj}) \cdot v_{CE} + k_2(T_{vj}) \tag{9}$$

where k_1 and k_2, such as coefficients in (1), are also temperature-dependent and, consequently, linearly interpolated based on two temperatures, i.e., 25 °C and 125 °C. The two IGBTs with opposite directions in the LCS can be further merged and eventually taken as one resistor.

To lower the voltage and current stresses, each IGBT symbol in the LCS is a 3×3 array of the ABB 5SNA 0650J450300 HiPak modules with inherent cooling mechanism. The analytical function for its transient thermal impedance shares the same form as (6); other than this there are only three cascaded R–C pairs, and the parameters can be found in the datasheet [28].

The metal-oxide varistors (MOVs) denoted as M_0, M_{11}, M_{12}, and M_2 are specifically installed to protect the circuit breaker's components from overvoltage. Its nonlinear I–V characteristics are described by

$$i_v = I_{\text{pref}} \left(\frac{v_v}{kV_{\text{pref}}} \right)^{\alpha} \tag{10}$$

where i_v and v_v are the MOV's current and voltage, and the remaining parameters are constant. The highly nonlinear conductance based on partial derivative between i_v and v_v will hinder real-time emulation as the circuit solution requires too many Newton–Raphson (N–R) iterations. Thus, piecewise linearization is used to divide its entire I–V curve into 11 segments, which are proven to be sufficient to retain a high accuracy by offline simulation, with each having the form of

$$i_v = G_v \cdot v_v + I_0 \tag{11}$$

where I_0 is a constant in the segment, and the conductance G_v is linearly interpolated by the terminal values as

$$G_v = (I_{n+1} - I_n)(V_{n+1} - V_n)^{-1} \tag{12}$$

where (V_{n+1}, I_{n+1}) and (V_n, I_n) represent the two terminals of a piecewise linear segment of the I–V characteristics. Then, the equivalent current of its companion model is

$$I_{v\text{eq}} = i_v - G_v \cdot v_v. \tag{13}$$

The ultrafast disconnector (UFD), on the other hand, is usually taken as an ideal switch with fixed ON- and OFF-state conductances. In this paper, the arc phenomenon is considered by employing the Mayr arc model, which is [29]

$$\frac{d\ln g}{dt} = \frac{1}{\tau_M} \left(\frac{ui}{P_M} - 1 \right) \tag{14}$$

where g is the arc conductance, u and i are the arc voltage and current, respectively, and τ_M as well as P_M represents the time constant and cooling power constant, respectively. Taking the logarithm of arc conductance $\ln g$ as a variable, the above-mentioned transcendental equation can be rewritten in its integrated form as

$$\ln g = \ln g_0 + \frac{1}{\tau_M} \int \left(\frac{i^2}{gP_M} - 1 \right) dt \tag{15}$$

and eventually discretized as

$$g(t + \Delta t) = g_0 \cdot \exp\left(\frac{b}{\tau_M} \left(Z(t) + \left(\frac{i^2}{g(t)P_M} - 1 \right) \Delta t \right) \right) \tag{16}$$

where g_0 is the initial conductance, b is a binary denoting the open or closed status of the UFD, and the iterative $Z(t)$ is

$$Z(t) = Z(t - \Delta t) + \left(\frac{i^2}{g(t - \Delta t)P_M} - 1 \right) \Delta t. \tag{17}$$

For simplicity, the UFD conductance is denoted by G_{UFD}, and whichever model is adopted, its existence induces in the MB an internal node, which can be eliminated by merging with the LCS. Then, the companion model in the form of Norton equivalent circuit with G_{MB} and I_{MBeq} (the conductance and equivalent current, respectively), is expressed by

$$G_{\text{MB}} = \frac{G_{\text{UFD}} \cdot (G_{\text{LCS}} + G_{v0})}{G_{\text{UFD}} + G_{\text{LCS}} + G_{v0}} \tag{18}$$

$$I_{\text{MBeq}} = \frac{G_{\text{MB}}}{G_{\text{LCS}} + G_{v0}} I_{v\text{eq}}. \tag{19}$$

With the breaking period restricted by a relatively slow UFD reaction [15], the UFMCB operation time is mainly determined by the protection voltage of M_2 as a higher rating curtails the duration, and a larger dc current leads to a longer operation period. Their exact relationship can be ascertained with a real-time emulator as part of the design guide.

B. RSNR Method

The N–R iteration is involved in solving the decoupled UFMCB since it contains a number of nonlinearities contributed by the thyristor and MOV. The nodal matrix equation takes the form of

$$\mathbf{U}^k = (\mathbf{G}^{(-1)})^k \cdot \mathbf{J}^k \tag{20}$$

where the subscription k is the iteration number. Following the acquisition of the kth iteration nodal voltage vector $\mathbf{U}^k$, the

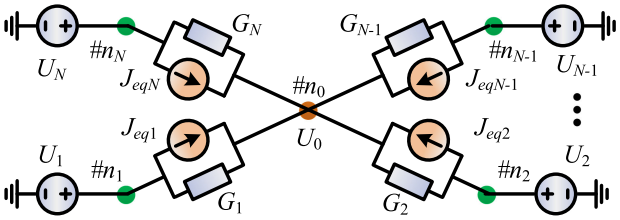

Fig. 4. Equivalent circuit of the proposed RSNR method.

admittance matrix $\mathbf{G}$ and the current vector $\mathbf{J}$ are updated for the next calculation until the results are convergent, i.e.,

$$\left|\frac{\mathbf{U}^{k+1}-\mathbf{U}^{k}}{\mathbf{U}^{k+1}}\right| \leq \epsilon \tag{21}$$

where ϵ is the threshold. To solve (20) with a high dimension and varying admittance matrix, the Gaussian elimination should be applied repeatedly, which is quite inefficient and consequently not used for the five-node UFMCB.

An RSNR method is proposed that decomposes the circuit and consequently avoids calculating the matrix equation. At the kth N–R iteration, the general matrix equation (20) can be expanded and sorted out as

$$\begin{bmatrix} G_{11} & \cdots & G_{1i} & \cdots & G_{1N} \\ G_{21} & \cdots & G_{2i} & \cdots & G_{2N} \\ \vdots & \cdots & \vdots & \cdots & \vdots \\ \underline{G_{i1}} & \cdots & \underline{G_{ii}} & \cdots & \underline{G_{iN}} \\ \vdots & \cdots & \vdots & \cdots & \vdots \\ G_{N1} & \cdots & G_{Ni} & \cdots & G_{NN} \end{bmatrix}^k \begin{bmatrix} U_1 \\ U_2 \\ \vdots \\ \underline{U_i} \\ \vdots \\ U_N \end{bmatrix}^k = \begin{bmatrix} J_{\text{eq}1} \\ J_{\text{eq}2} \\ \vdots \\ \underline{J_{\text{eq}i}} \\ \vdots \\ J_{\text{eq}N} \end{bmatrix}^k. \tag{22}$$

Therefore, at an arbitrary node i, its voltage can be extracted from the ith row which is underlined in (22) as

$$U_i^k = (G_{ii}^k)^{-1} \cdot \left(J_{\text{eq}i}^k - \sum_{j=1, j\neq i}^{N} G_{ij}^k U_j^k \right). \tag{23}$$

To solve the ith nodal voltage U_i^k, voltages at other nodes U_j^k are yet to be known. However, the nodal voltage at the kth iteration can be expressed by the previous calculation, i.e.,

$$U_i^k = (G_{ii}^k)^{-1} \cdot \left(J_{\text{eq}i}^k - \sum_{j=1, j\neq i}^{N} G_{ij}^k \left(U_j^{k-1} + \xi_j \right) \right) \tag{24}$$

where ξ_j denotes the error between two successive iterations at the jth node. It means that the solution of an arbitrary node can be realized without solving the large matrix equation as in (22), which is time-consuming. Compared with the Jacobi method for linear systems [30], the elements $J_{\text{eq}i}$, G_{ii}, and G_{ij} are possibly nonlinear in the RSNR and, therefore, their values should also be updated in every iteration. With the ongoing repetitive process updating nodal voltages, ξ_j decreases until it is smaller than ϵ when the results are deemed convergent.

Fig. 4 describes the RSNR method by an equivalent circuit. The node n_0 to be solved is neighbored by a number of other nodes, denoted as n_1, n_2, etc., and the branches between two nodes are represented by the Norton equivalent circuit $J_{\text{eq}i}$ and G_i ($i = 1, 2, ...$). The potentials at other nodes U_1, U_2, etc., are represented by voltage sources to form a complete circuit. Then, the nodal voltage to be solved can be derived by

$$U_0 = \left(\sum_{i=1}^{N} J_{\text{eq}i} + \sum_{i=1}^{N} G_i U_i \right) \left(\sum_{i=1}^{N} G_i \right)^{-1}. \tag{25}$$

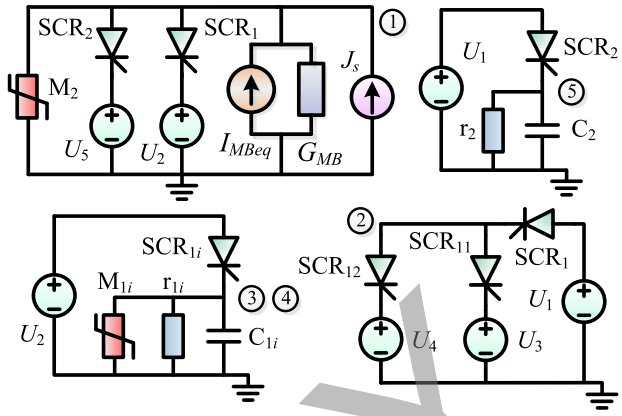

Fig. 5. UFMCB nodal domain decomposition.

Thus, the partitioned five-node UFMCB evolved into five subcircuits as shown in Fig. 5, or from a mathematical point of view, the five-dimensional (5-D) matrix equation is split into five single equations that can be solved in a more efficient parallel manner. For instance, Node 1 is neighbored by Nodes 2 and 5, and therefore, the impact of other components on these two nodes are converted to voltage sources U_2 and U_5, whereas for Node 5 solution the potential U_1 is assumed to be available.

IV. Multiterminal HVdc Grid

A. Modular Multilevel Converter

The HBSM is the most prevalent configuration in the MMC for fewer devices than other topologies. However, its incapability of dc grid protection once dc line faults occur even when all the IGBTs are blocked indicates the necessity of the HVdc breaker, and in some cases, the CDSM shown in Fig. 6 along with the three-phase MMC, since it is able to produce a voltage level as two HBSMs.

It is obvious that the MMC has a large number of nodes regardless of the SM configuration. Merging the arm turns out to be impractical as the status of the diode is more difficult to ascertain than the IGBT. The equivalent circuit based on the analysis of the CDSM operation modes, on the other hand, loses generality since only these desired states are considered. Hence, the partitioning using the transmission-line link model (TLM-link) [31] is adopted, as shown in Fig. 7, where the SMs are separated from their corresponding arms for a decoupled transient solution to ensure real-time execution of the dc grid adopting the joint CDSM-MMC and UFMCB protection.

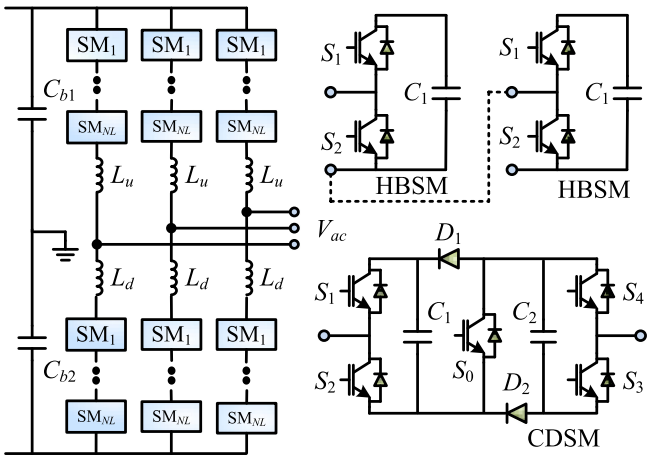

Fig. 6. Three-phase MMC topology and its SM configurations.

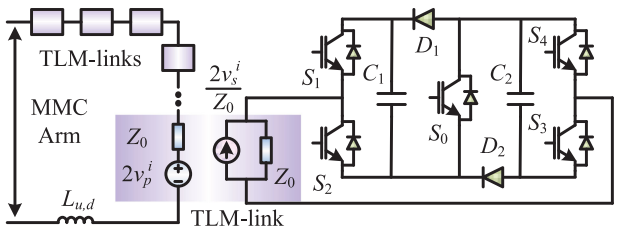

Fig. 7. MMC SM partitioned by TLM-link.

To avoid the introduction of an additional node, the Norton equivalent circuit is adopted on the SM side, whereas on the arm side are the Thévenin equivalent circuits, which are eventually merged and turned into the Norton equivalent circuit, as the companion model takes the form of

$$G_{\text{arm}} = (N_L \cdot Z_0 + Z_{Lu,d})^{-1} \tag{26}$$

$$J_{\text{arm}} = G_{\text{arm}} \cdot \left(2\sum_{i=1}^{N_L} v_p^i + 2v_{Lu,d}^i\right). \tag{27}$$

Once the CDSM-MMC is blocked, the dc side is approximated by a second-order L–C circuit, and due to the discharging of capacitors C_{b1} and C_{b2}, the fault current will rise to the maximum before reducing to 0, as estimated by

$$i_F = e^{\alpha t}[-\alpha\beta C_b V_{\text{dc}}(0^-)\sin(\beta t) + I_{\text{dc}}(0^-)\cos(\beta t)] \tag{28}$$

where $V_{\text{dc}}(0^-)$ and $I_{\text{dc}}(0^-)$ are the dc voltage and current prior to the fault, and

$$\alpha = -\frac{R_p + R_F}{2L_p},\ \beta = \sqrt{\frac{1}{L_p C_b} - \left(\frac{R_p + R_F}{2L_p}\right)^2} \tag{29}$$

are coefficients determined by the fault resistance R_F, the MMC dc bus capacitance C_b, and the fault path resistance and inductance denoted by R_p and L_p, respectively.

B. Four-Terminal DC Grid Test Case

Fig. 8 shows the four-terminal dc grid where the rectifier stations STN_2 and STN_4 employ HBSM-MMCs, whereas the

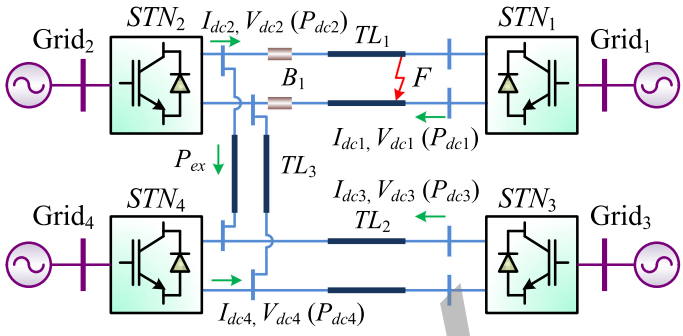

Fig. 8. Four-terminal HVdc grid based on mixed MMC topologies and the UFMCB.

TABLE I
UFMCB PARTS HARDWARE DESIGN SUMMARY

Module	LUT	FF	DSP48	Latency
GauElim (Solver1)	20580	11606	68	242
RSNR (Solver2)	2149	1776	31	49
SCR (×4)	2496	1366	18	10
MB	1205	494	9	12-25
Update	2043	1605	26	5
MOV (×4)	2375	0	0	0
UFMCB (Solver1)	28699 (2.43%)	15071 (0.64%)	121 (1.77%)	**756**
UFMCB (Solver2)	10268 (0.87%)	5241 (0.22%)	84 (1.23%)	**177**
Avaiable	1182240	2364480	6840	–

inverter stations STN_1 and STN_3 are the CDSM-based MMCs, all of which are symmetric monopole with the dc neutral point grounded in a fashion as shown in Fig. 6. Therefore, the UFMCBs should be deployed to the two rectifier stations, while their counterparts do not require it for the fault isolation capability; since the fault is simulated on line TL_1, only the UFMCB B_1 is installed at STN_2. Once the pole-to-pole fault F takes places on that line, all IGBTs of STN_1 are ordered to turn-OFF, whereas on the rectifier side, only the breaker B_1 is ordered to operate so that the power transmission from STN_2 to the remaining healthy system continues.

V. UFMCB HARDWARE DESIGN

The hardware design of the proposed UFMCB integrated into the dc grid is based on the Xilinx UltraScale+ VU9P FPGA, which has total available resources of 1 182 240 LUT blocks, 2 364 480 FFs, and 6840 DSPs. The UFMCB model has five main parts that are designed into corresponding hardware modules by the high-level synthesis tool Vivado HLS enabling the design by C/C++ coding. In Table I, the five types of hardware modules are listed, i.e., the SCR, the MB, the MOV, the solver, and the signal update function (Update). Due to the introduction of the scalable thyristor model, the hardware resource utilization rate is low, less than 3% for all three types. Meanwhile, for the 5-D nodal matrix equation, the original solver using Gaussian elimination requires more resources than that required in the proposed RSNR solver, whereas the main improvement is on the latency that is a key factor for real-time execution. A

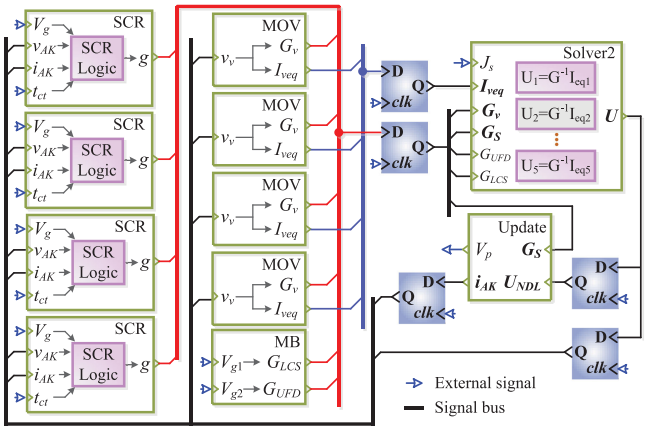

Fig. 9. Synthesized hardware architecture of the UFMCB on the FPGA.

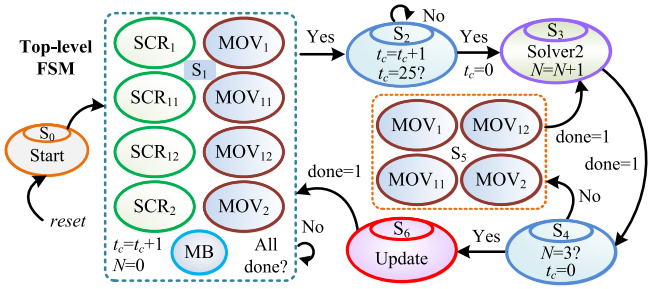

Fig. 10. UFMCB top-level FSM.

time-step around 8 μs required by Solver1 would compromise the resolution, especially considering that device-level results are needed; in contrast, the proposed RSNR enables a four times speedup since the time-step can be set to 2 μs. The fact that the MOV latency remains 0 due to hardware parallelism indicates that the selected time-step will not change even if the MOV piecewise linearization yields more segments.

The synthesized UFMCB hardware architecture is shown in Fig. 9. The four SCR modules receive their individual gate signals from the protection device and then give the conductances to the solver module. Meanwhile, the MOVs and the module MB conduct the companion model calculation and the outcomes are also sent to the solver where the nodal voltages are computed in parallel. It is noticed that the outputs from the SCR, MOV, and MB are not instantly sent to the solver, instead, the D-latch whose clock port is fed by the data valid indicator is always between the outputs and inputs of two hardware modules. Once correct nodal voltages are obtained from Solver2, they are sent to the Update module for calculating the thyristor currents and the voltage coupling V_p. As can be seen, a closed-loop is formed, and the inputs of a module are acquired from its upstream counterparts; however, parallelism is available for most of the blocks, and whenever the output data are valid, it is sent to the downstream modules.

A proper finite-state machine (FSM) is required to coordinate those modules since the involvement of nonlinear elements forces the adoption of the N–R iteration. According to Fig. 10, repetitive operations of the MOV and Solver2 modules are possibly needed. In the beginning, the reset order is issued and the emulation starts from state S_1 when MB and all the SCR and MOV modules are running. Completion of these modules does not indicate an immediate start of circuit solution; instead, Solver2 begins until 25 clock cycles counted since S_1 has passed due to the variable latency of the MB whose maximum latency is 25 clock cycles after taking its arc phenomenon into account. Following the nodal voltage solution is the convergence check. Since a maximum of three iterations is needed, the calculation in each time-step is repeated three times to ensure the results will not be distorted. As can be seen, only the MOV modules are involved in the N–R iteration before entering to the nodal voltage solution module for gathering convergent results in the time domain. Hence, according to the FSM, a simulation time-step involves 3 N–R iterations and the total latency is 177, as provided in Table I.

Therefore, the Xilinx UltraScale+ FPGA providing a virtual primary power system can work as an HIL emulator under either the open-loop mode as in this paper for dc circuit breaker design evaluation and system study or the closed-loop mode by interconnecting external control and protection devices for real-time testing.

VI. Real-Time HIL Emulation Results

The proposed real-time HIL emulation setup provides both device- and system-level information, which are validated by ANSYS/Simplorer and PSCAD/EMTDC, respectively, as the former tool contains electrothermal models of power electronics, whereas the latter is popular for grid-level study.

A. UFMCB Design Evaluation by HIL System

The dc circuit breaker design is validated by tests conducted in the dc system as shown in Fig. 3, where a 120 kV dc voltage is applied to an 80 Ω load via an 100-mH inductor $L_{\rm dc}$ which has a parasitic resistance of 1 Ω and the UFMCB, and each SCR symbol contains 60 serial 5STF 28H2060 thyristors. At $t = 100$ ms, a line-to-ground fault with a resistance of 1 Ω takes place, and the protection is triggered 50 μs later. Fig. 11(a) shows the UFMCB's terminal voltage and current. The current rises in an approximately linear fashion during the breaking period, followed by an opposite trend in fault clearance period when it is eventually quenched to 0 by the MOV M_2, which maintains a protection voltage v_{M2} of around 170 kV. The identical voltage waveforms to offline simulation results validate the proposed MOV model. The insights peculiar to a device-level SCR model are given and compared with the ideal model in PSCAD/EMTDC. It is noticed in Fig. 11(b) that the currents of proposed thyristor model are identical to those from ANSYS/Simplorer, while PSCAD/EMTDC leads to some differences in two of them even though the waveforms are in system-level. In Fig. 11(c) and (d), the power losses of $\rm SCR_1$ and $\rm SCR_2$ from different tools are compared to demonstrate the importance of a device-level model. The HIL emulation results give definitive values at different time instants, while for PSCAD/EMTDC, a small ON-state resistance should be given to

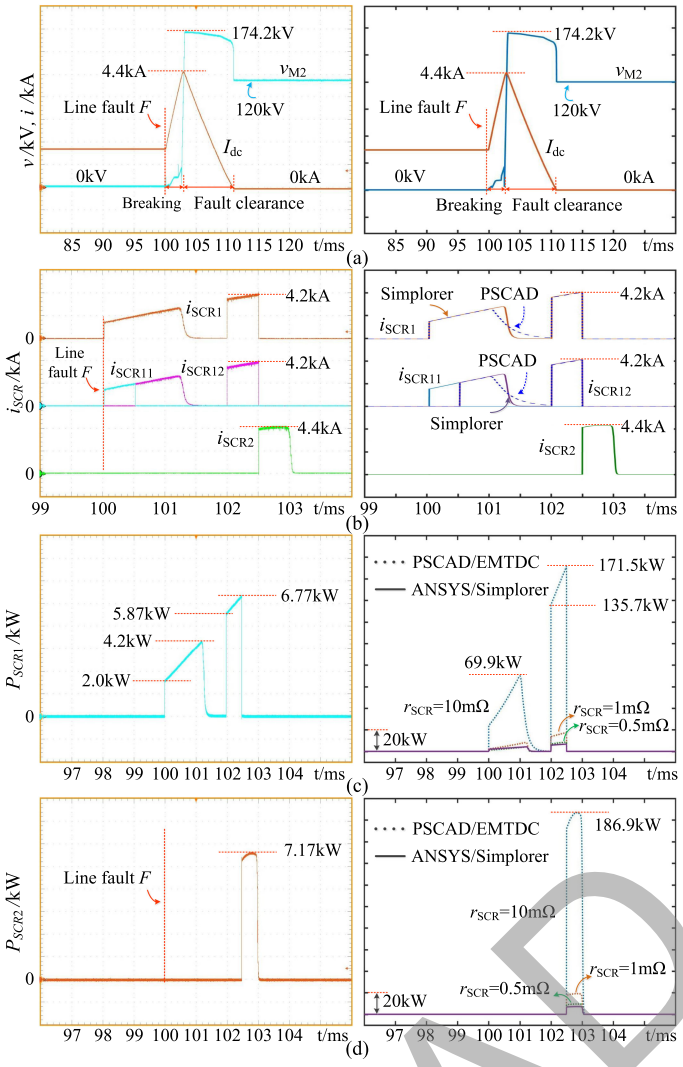

Fig. 11. UFMCB real-time emulation oscilloscope results (left) validated by ANSYS/Simplorer and PSCAD/EMTDC (right). (a) Protection waveforms. (b) SCR currents. (c) SCR_1 power consumption. (d) SCR_2 power consumption.

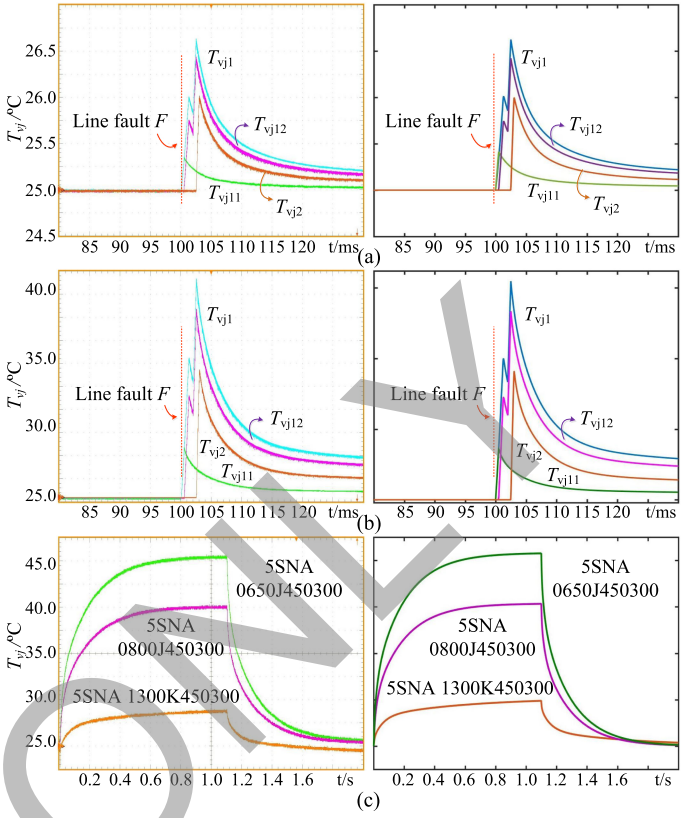

Fig. 12. UFMCB power switch junction temperatures during protection from real-time HIL emulation (left) and ANSYS/Simplorer (right). (a) 5STF 28H2060. (b) 5STF 05D2425. (c) 3 IGBT types for LCS.

the ideal thyristor before simulation, and its various values yield distinct power losses that will be misleading if adopted for the design evaluation. The bidirectional current breaking capability of the UFMCB is also confirmed in the test and all the results under reverse operation are absolutely identical to those shown earlier.

Based on the power loss, the selection of an appropriate type of thyristor can be conducted by judging the junction temperature. With 5STF 28H2060, which has a peak nonrepetitive surge current I_{TSM} of 46.5 kA, the highest junction temperature appears in SCR_1, and it is merely around 27 °C as shown in Fig. 12(a), meaning the capacity of the thyristor is not fully utilized. The 5STF 05D2425 thyristor with $I_{TSM} = 7.0$ kA and a lower cost yields the maximum temperature at 41 °C as shown in Fig. 12(b). Therefore, the latter type is more suitable while an adequate capacity margin is maintained. The 5SNA 0650J450300 IGBT is selected for the LCS, according to Fig. 12(c), because even with a smaller capacity than its counterparts, the junction temperature during normal operation will not exceed 50 °C. The above-mentioned results are validated by identical waveforms on the right side from ANSYS/Simplorer, which is among popular device-level EMT simulation tools referred to for power electronic apparatus design guide before the equipment is galvanized and tested.

In Fig. 13, the two thyristor types are compared regarding the power loss and junction temperature when the UFMCB is closed to establish the normal power transmission. Only SCR_1 and SCR_{11} conduct during the process and therefore their device-level information is revealed. Although the 5STF 05D2425 with a smaller capacity yields a higher junction temperature due to larger power loss, it is only 30 °C—lower than the opening process. Therefore, this thyristor type is preferred over 5STF 28H2060 for constructing the UFMCB for applications with a similar voltage and power ratings to the tested dc system, and the proposed HIL platform can always be referred to when the system changes.

The impact of three sets of UFD parameters on the dc circuit breaker, mainly the thyristors SCR_1 and SCR_{12}, are demonstrated in Fig. 14. The currents of SCR_1 are given as an example in Fig. 14(a). UFD_2, which has a cooling power constant of 1000 kW, leads to the SCR current i_{SCR1} virtually identical to that of the ideal switch model UFD_1; in contrast, when the UFD_3 has a longer arc duration, i.e., the cooling power constant

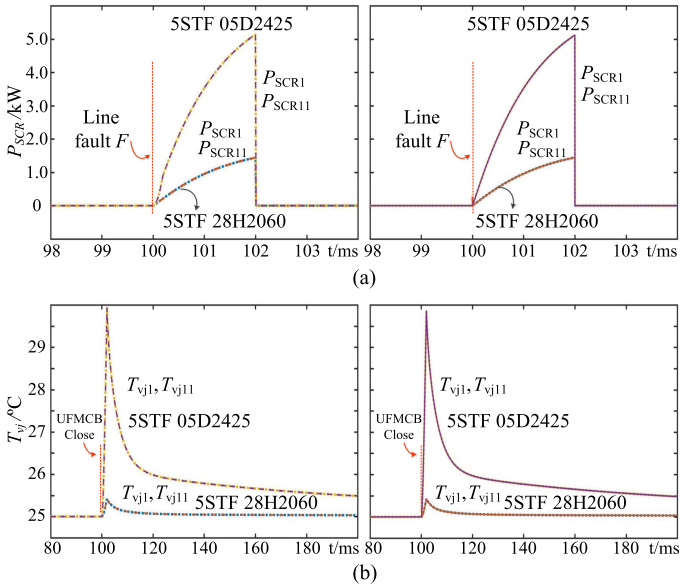

Fig. 13. UFMCB thyristor device-level results during closing from real-time HIL emulation (left) and ANSYS/Simplorer (right). (a) Power loss. (b) Junction temperature.

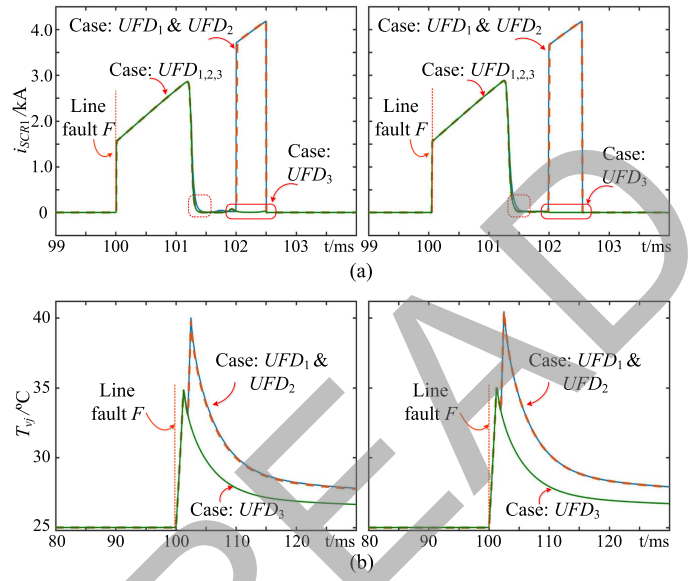

Fig. 14. Impact of UFD arc on the UFMCB thyristors from real-time HIL emulation (left) and ANSYS/Simplorer (right). (a) SCR currents. (b) Junction temperature.

reduces to 100 kW, it can be seen that between 102 and 102.5 ms, the current i_{SCR1} is 0 as it is diverted to the UFD-M_0 path in the MB. The junction temperatures of SCR_1 in Fig. 14(b) are a direct reflection of the current: the thyristor junction temperature rises to over 40 °C when the UFD model is ideal and $P = 1000$ kW, whereas it is only 35 °C if $P = 100$ kW.

B. UFMCB in HVdc Grid

The four-terminal dc grid in Fig. 8 is taken as the test-bench for studying the system's performance under the joint protection scheme of the self-protective CDSM-MMC and the

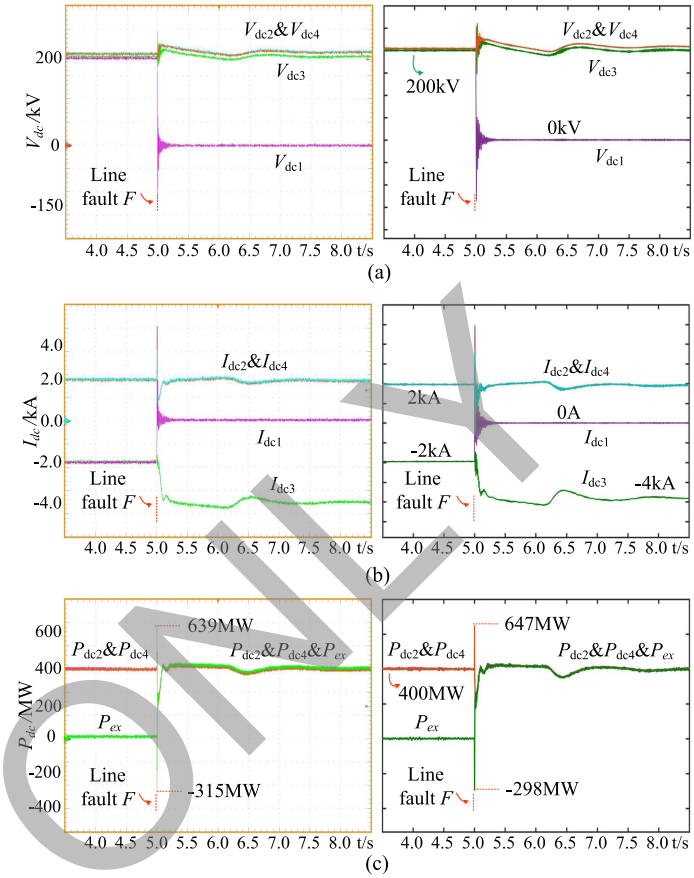

Fig. 15. Real-time MTDC grid dc line fault emulation results (left) and PSCAD/EMTDC validation (right). (a) DC voltages. (b) DC currents. (c) Power.

external apparatus UFMCB. As shown in Fig. 15, initially, all dc currents at the four terminals are around ±2 kA, and their dc voltages are approximately 200 kV, with the rectifier side having a slight margin, meaning each rectifier is delivering 400 MW power solely to the corresponding inverter, which accounts for no power flow between the two HVdc links as $P_{ex} = 0$. At $t = 5$ s, the pole-to-pole fault takes place near STN_1, followed by protections from both the UFMCB and the station itself. Due to the CDSM-MMC's blocking capability, the dc voltage on STN_1 side V_{dc1} plummets to 0, and so is its current I_{dc1} with a short period of oscillations. On the other hand, the prompt response of the UFMCB exempts STN_2 from blocking and its power P_{dc2} is able to restore immediately. Consequently, P_{ex} increases to 400 MW and the power STN_3 received is doubled to about 800 MW, as it can be seen that its dc current I_{dc3} rises from 2 kA to around 4 kA whereas its dc voltage V_{dc3} is still 200 kV.

In Fig. 16, the dc grid protection performance of the CDSM-MMC and UFMCB are given. In Fig. 16(a), after the permanent fault, all IGBT gate signals in the SM are retrieved, and the SM capacitor is slightly charged and maintained around 4 kV for the 51-level MMC even though at the dc side its voltage V_{dc1} has become 0, and due to the high impedance of the SMs, the arm current drops to 0. As an important property of dc

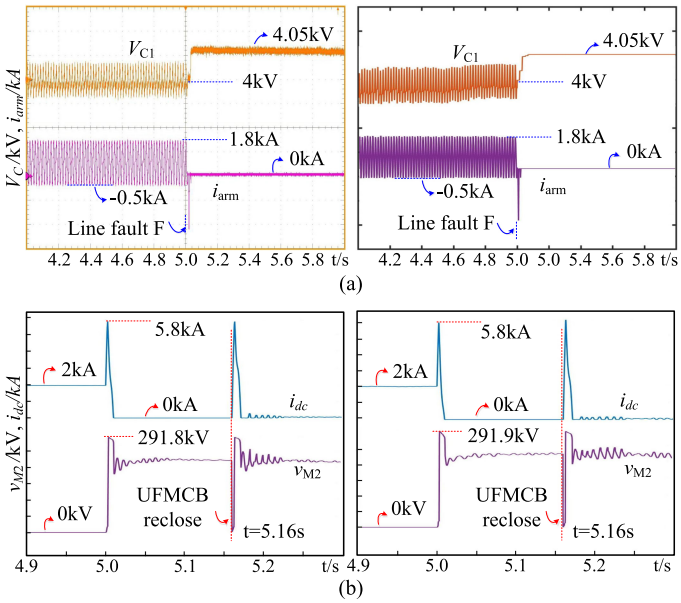

Fig. 16. Real-time HIL emulation results (left) and PSCAD/EMTDC validation (right) of protections initiated by (a) CDSM-MMC and (b) UFMCB with reclosure.

circuit breakers, the UFMCB reclosing function is tested in Fig. 16(b). After the fault, the dc current keeps rising when it is commutating from one branch to another in the circuit breaker and decreases to 0 after all SCRs are turned-OFF so M_2 maintains a voltage of nearly 290 kV—higher than the rated 200 kV dc yard voltage—to extinguish the current; a reclosure is attempted 160 ms later to restore the power transmission, but since the fault still exists, another interruption is witnessed.

VII. Conclusion

A detailed UFMCB with device-level nonlinear electrothermal thyristor model was proposed in this paper for the twofold purposes of circuit breaker design evaluation and the dc grid real-time HIL emulation. The SCR model was deemed as a superimposition of the static I–V characteristics and the reverse recovery phenomenon, and a scalable model representing the cascaded devices was obtained for node number reduction. Due to a slow current changing rate enabled by the smoothing inductor, the UFMCB can be separated from the dc grid by a pair of coupled voltage–current sources. The RSNR method avoids solving circuit matrix equations normally conducted in the EMT simulation, and the subsequent parallelism leads to a remarkable improvement on the FPGA hardware latency for real-time execution with high fidelity. The joint protection scheme combining the CDSM-MMC and UFMCB was tested on the HIL setup, and the results were validated in both device- and system-level by commercial EMT simulation tools. The proposed device-level modeling method is also applicable to other types of HVdc circuit breakers for less computational burden regardless of their regularity, and the designed emulator can be used for real-time testing of actual converter controllers by establishing a power HIL setup once the exact parameters of other primary system components such as transmission lines and cables are acquired.

Appendix

The four-terminal dc grid parameters: MMC level 51, $C_{\rm SM}$ = 5 mF, $L_{u,d}$ = 50 mH, $L_{\rm dc}$ = 100 mH, $C_{b1,2}$ = 100 μF, MMC ac side V_g = 135 kV/60 Hz, $V_{\rm dc}$ = $\pm$100 kV; UFMCB parameters: r_{11} = 50 Ω, r_{12} = 100 Ω, r_2 = 4 kΩ, C_{11} = 300 μF, C_{12} = 114 μF, C_2 = 7.8 μF, V_{M_0} = 18.33 kV, $V_{M_{11}}$ = 11.67 kV, $V_{M_{12}}$ = 133.33 kV, V_{M_2} = 300 kV; UFD arc model: τ_M = 0.6 μs, P_M = 100–1000 kW.

ABB 5STF 05D2425 parameters: V_{To} = 2.551 V, t_q = 25 μs, $\frac{dI_r}{dt}$ = 800 A/μs, $I_{\rm rrm}$ = 110 A, K = 21.06, $\tau_{1\text{–}5}$ = 0.4857, 0.2162, 0.0762, 0.0043, 0.0006 s, $R_{1\text{–}5}$ = 13.07, 8.03, 8.20, 2.57, 0.13 K/kW; At 25 °C/125 °C: A = 4.3/1.96, $B = 7\times10^{-5}/4\times10^{-4}$, $C = 7\times10^{-5}/5\times10^{-4}$, $D = 2\times10^{-4}/0.08$, I_L = 1500 mA/1000 mA.

ABB 5STF 28H2060 parameters: V_{To} = 1.198 V, I_L = 500 mA (25 °C)/300 mA (125 °C), t_q = 60 μs, $\frac{dI_r}{dt}$ = 800 A/μs, $I_{\rm rrm}$ = 315 A, K = 21.06, $\tau_{1\text{–}5}$ = 0.4871, 0.1468, 0.0677, 0.0079, 0.0021 s, $R_{1\text{–}5}$ = 6.73, 1.44, 0.65, 0.84, 0.32 K/kW; At 25 °C: A = 0.57536, $B = 8\times10^{-5}$, $C = 1.94\times10^{-3}$, D = 0.06964.

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