High Speed Digital Sampling and Its Applications in PLLs

by

Jinghang Liang

A thesis submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

in

Integrated Circuits and Systems

Department of Electrical and Computer Engineering
University of Alberta

ABSTRACT

Sampling, employed as a special type of mixing, allows using a low local frequency to down-convert the high-frequency RF signal. Existing work of sampling is limited to analog sampling. If a high-speed digital sampler is directly applied to sample the RF signal, the generated output will be the 1-bit digitized alias signal corresponding to the RF input. We show in simulation that a digital sampler, implemented with a sense amplifier such as a StrongARM latch or a current mode logic (CML) latch, can greatly extend the operating frequency when compared to static digital dividers implemented with the same circuit (i.e., through 130 GHz for circuit implemented in TSMC 40nm bulk CMOS process).

In a traditional high-frequency PLL implementation, analog frequency dividers that typically use inductors are needed when exceeding the frequency operation range of digital dividers. Unfortunately, these analog dividers not only cost in power consumption and large silicon areas but also suffer from limited frequency ranges. To solve this problem, another circuit architecture, named the alias-locked loop (ALL), which utilizes the advantage of digital sampler and applies it in the feedback path to replace the dividers, was proposed [15]. An ALL has several advantages including wide frequency range of operation, saving silicon area and design cost, but suffers from several drawbacks, including spurs and the need for two reference clocks.

One significant drawback of an ALL is that the feedback signal to the PFD (phase frequency detector) may not be single-tone periodic in most cases, which therefore introduces periodic spurs. To solve this problem, another circuit architecture, named coresidual alias-locked loop (C-

ALL), which uses a digital circuit and the sampling clock to synthesize the reference signal, is proposed. By predicting the expected pattern of 1's and 0's and providing this signal to the phase detector, a C-ALL can mitigate the periodic PFD pattern that generates frequency spurs in an ALL output (by as much as 27.7 dB in simulation). In addition, a C-ALL does not require a second reference clock.

The C-ALL control loop has a “dead zone” in lock when the phases are close, but no net charge pump signal is generated. This dead zone results in only a coarse phase lock and no effective suppression of phase noise. To solve this problem, we propose a new type of locking mechanism and a new type of circuit architecture we call a Phase Shift Coresidual Alias-Locked Loop (PS-CALL), which guarantees feedback at every active edge of the alias signal, thus eliminating the dead zone and achieves fine phase lock. Our simulations show that a PS-CALL can not only achieve phase lock but also reduces the spur level by 16.2 dB compared to a normal C-ALL.

We propose another circuit architecture named the differential alias-locked loop (D-ALL) to avoid the second reference clock required by an ALL. In a D-ALL, two feedback signals are generated from two samplers clocked at different sampling frequencies (divided down from a common clock), and the sampled signals fed into the phase frequency detector (PFD). Spectre post-layout extracted circuit simulations have verified the proposed design can achieve lock at programmable frequencies in the range of 21–23.3 GHz.

In addition to digital sampling and its applications in high-speed PLLs, other issues in PLLs are also discussed in this thesis. The capacitor in the loop filter is either an off-chip discrete component preventing full integration, or on-chip consuming significant silicon area. Moreover, the voltage ripples on the loop filter output can result in large spurs at the VCO output. To

address these two issues, a new circuit architecture is presented with a VCO-based integrator to replace the charge pump and loop filter. Instead of using a charge pump and capacitor as the integrator, a VCO is used to implement the integrator with the phase being the output in the proposed PLL architecture. To ensure loop stability, a voltage-controlled delay line (VCDL) is developed to introduce a zero in the loop transfer function. Spectre simulation has verified the proposed design with a VCO-based integrator can successfully synthesize the targeting frequency at 3 GHz with 39% of total silicon area saving at a cost of 109% increase in total power consumption, without compromising on phase noise performance.

PREFACE

This thesis is an original work by Jinghang Liang under the supervision of Prof. Duncan Elliott. Some parts of the thesis have been published as described below.

Some parts of Chapter 2 and Chapter 3 have been published as:

- [16] J. Liang, Z. Zhou, J. Han, D. G. Elliott. "A 6.0–13.5 GHz Alias-Locked Loop Frequency Synthesizer in 130 nm CMOS", IEEE Transactions on Circuits and Systems I, vol. 60, no. 1, pp. 108-115, 2013

I was responsible for the system design, simulation, analysis as well as the manuscript composition. Dr. Duncan Elliott was the supervisory author and was involved with technical guidance throughout. Zhiying Zhou and Dr. Jie Han helped in chip design and manuscript preparation.

Some parts of Chapter 5, Chapter 7 and Chapter 8 have been published as:

- [63] J. Liang and D. G. Elliott, "Coresidual alias-locked loops," IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, 2016, pp. 9-12.
- [93] J. Liang and D. G. Elliott, "Frequency Synthesis Based on A Novel Differential Locking Mechanism," IEEE International Symposium on Circuits and Systems (ISCAS), Florence, May 28 - 31, 2018.
- [110] J. Liang and D. G. Elliott, "VCO-based integrator PLL [Technical Program]," IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, 2016, pp. 1-4. doi: 10.1109/ISCAS. 2016. 7720798

I was responsible for the system design, simulation, analysis as well as the manuscript composition. Dr. Duncan Elliott was the supervisory author and was involved with technical guidance throughout. Chapter 5 had assistance in chip design and manuscript preparation from David Sloan and Dr. Masum Hossain.

ACKNOWLEDGEMENTS

The work presented in this thesis could not have happened without the help of many people.

First of all, I would like to show my deepest appreciation to my supervisor, Dr. Duncan Elliott, not only for his professional guidance to my research but also for his full support during my study. Dr. Elliott is the most knowledgeable person I've ever met and discussing with him can always generate sparkling ideas. Moreover, Dr. Elliott's support throughout my study, especially for the period when I have to take my responsibility as a father and a son, is priceless. I would also like to thank Dr. Masum Hossain for his insightful advice to this research, thank Dr. Kambiz Moez for his wonderful lectures in ECE403 and valuable discussions throughout the course and research.

The VLSI lab is always a place with hardworking students and supportive lab mates. I would like to thank David Sloan who has always provided wonderful feedbacks, ideas, and friendship. I would like to thank Khaled Al-Amoodi, Waleed El-Halwagy and other lab mates for always being ready to help and share. I wish to acknowledge the help provided by Tai-chun Lee, Nancy Minderman and all the other technical and support staff.

Edmonton is undoubtedly my second hometown. I would also like to thank Hao Chen, Zhiyin Zhou, David Sloan, Russel Dodd and all my other friends that I have met in here. I will treasure the friendship and all the memories forever.

During my graduate study, I met my wife, married her and had our little princess. Love and support from my wife are always a constant source of encouragement throughout the duration of

this thesis. I also wish to thank my mother, my aunt Sophia Lu, my uncle Robert Wu and other family members, for their love and support.

Finally, I would also like to thank the Natural Sciences and Engineering Research Council, Alberta Innovates, and CMC Microsystems for the support of this work.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1. Introduction

With the fast development of radio frequency and millimetric wave applications such as communications and radars, high-frequency synthesizers become increasingly more important in recent years. A phase-locked loop (PLL), which can be applied as a frequency synthesizer, is a critical component in many circuits and systems as it provides the timing basis for functions such as clock control, data recovery, and synchronization.

1.1. Background and Motivation

1.1.1. High frequency dividers

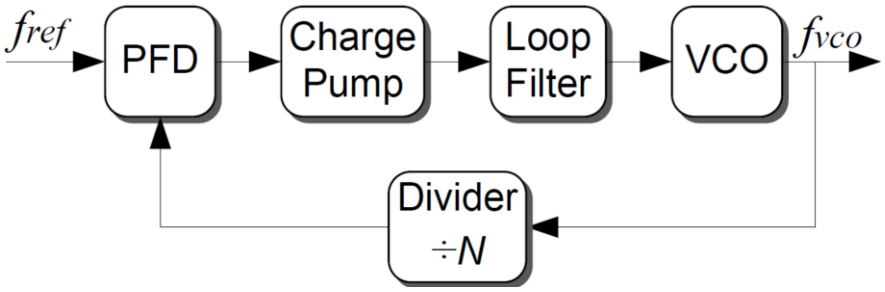


Figure 1: A traditional PLL implementation. For high-speed PLLs, only the VCO and the first few stages in the divider chain work at high frequency.

In a traditional PLL implementation as shown in Figure 1, a divider in the feedback path converts higher frequencies to lower frequencies. A traditional digital divider is based on flip-flops, whose highest speed is limited by the setup time plus propagation time clock-Q. For a given process, these two parameters are mainly determined by the process itself. The voltage-controlled oscillators (VCOs) can be greatly optimized for a given process and can obtain a very high frequency, i.e. a 410 GHz VCO implemented in 45 nm digital CMOS process in [1], a 540 GHz LC-VCO implemented in a 40 nm bulk CMOS in [2], a 432 GHz push-push oscillator in a 65 nm CMOS process in [3] and a 553-GHz quadruple-push oscillator in 45 nm ULP CMOS in [4]. However, dividers based on flip-flops will not work at such high frequencies. Designers usually resort to regenerative dividers [5][6][7] or injection-locked frequency divider (ILFD) [8][9][10][11][12] to extend the operating frequency of their devices. Unfortunately, regenerative

dividers and ILFDs usually contain inductors that not only cost large silicon areas but also result in narrow frequency range of operations. In Chapter 2, we will review the principles of these dividers and explain these limitations.

1.1.2. Charge pumps and loop filters

A charge pump and a loop filter are widely used in a modern PLL implementation as shown in Figure 1. The loop filter is usually implemented with a resistor and a capacitor. For a certain bandwidth requirement, there is a trade-off between choosing the resistance and the capacitance. Implementing a chosen time constant with a smaller capacitor and larger resistor will exhibit higher thermal noise. Additionally, a smaller resistor and a large capacitor usually require a large silicon area or off-chip implementation.

There have been various approaches proposed to address this issue. For instance, instead of using only one charge pump, two charge pumps were used to separate the integral path and the proportional path [13]. An equivalent capacitance, which was controlled by both a small capacitor and the charge pump current, was created in the phase domain. A large equivalent capacitance can be achieved by tuning the corresponding charge pump currents without using a physically large capacitor [13]. Another example is the so-called capacitance multiplication technique, which uses active circuits to 'amplify' a small capacitance [14]. However, extra power consumption and extra noise from the operational amplifier directly impacts the noise performance.

1.2. Goals and Thesis Outline

In this dissertation, we focus on different techniques in frequency synthesis. First analog sampling circuits are examined, digital sampling circuits are analyzed, and input referred noise is simulated and discussed. Simulation has shown that a digital sampler, implemented with a sense amplifier or a CML latch, can greatly extend the operating frequency when compared to static digital dividers implemented with the same circuit architecture (i.e., through 130 GHz for circuit implemented in TSMC 40nm bulk CMOS process). Based on previous work of alias-locked loops (ALLs) that uses digital sampling to replace dividers [15], novel frequency synthesizer circuit architectures named coresidual alias-locked loop (C-ALL), phase shift coresidual alias-

locked loop (PS-CALL) and differential alias-locked loop (D-ALL) are newly proposed. A C-ALL digitally produces the anticipated sampler output to reduce spurs, a PS-CALL guarantees feedback provided at every active edge of the alias signal to achieve fine phase lock, and a D-ALL locks on positive and negative alias frequencies to save the extra reference clock. In addition to the sampler-based circuit architectures, a PLL with a VCO-based integrator is proposed to replace the area-intensive charge pump with an integrator.

The thesis proceeds as follows. Chapter 2 reviews the previous work, including traditional high frequency synthesis using PLLs and ALLs. Chapter 3 presents the analysis, implementations, and applications of digital sampling. Chapter 4 and Chapter 5 presents the proposed C-ALL and D-ALL architecture. Chapter 6 presents the PLL architecture with a VCO-based integrator. Chapter 7 concludes the thesis.

CHAPTER 2. Previous Work

2.1. Review of Previous Work

Dividers play an important role in PLLs by bringing the high VCO frequencies down to around reference clock frequencies. For high-speed PLLs, different approaches can be implemented to design high-frequency VCOs, while designing digital dividers that operate at the VCO frequency is usually challenging. For instance, a 410 GHz VCO was implemented in 45 nm digital CMOS process in [1], and dividers for such high frequencies are currently infeasible. To alleviate this problem, a new frequency synthesizer architecture, named the alias-locked loop (ALL), was proposed in [15]. In this Chapter, recent developments in high-speed PLLs using high-speed dividers, subsampling PLLs and ALLs are all reviewed.

2.1.1. High-speed dividers

High-speed PLLs usually resort to injection-locked frequency dividers (ILFDs) or regenerative frequency dividers in the feedback path. The inductors in these high-speed dividers not only cost a large silicon area but also limit the frequency range of operation.

2.1.1.1. Injection-locked frequency dividers

An ILFD usually consists of an oscillator with one or more terminals for input signal injection [17]. In a PLL, the VCO output is usually used as the input signal of the ILFD. If no input signal is injected, i.e., only DC signal is applied as the input signal, the ILFD operates like a free-running oscillator. If the input signal is injected, however, the ILFD output frequency will be sub-multiple of the input frequency and the phase of the ILFD output signal is locked to the input phase. Due to the limited oscillation frequency range, an ILFD can only lock to the input signal within a certain frequency range.

Different types of oscillators result in different topologies of ILFDs. For instance, an ILFD based on a five-stage RC-type ring oscillator was demonstrated in [18], another ILFD based on a three-stage ring of NMOS inverters with PMOS active load was proposed in [19]. Unfortunately, both abovementioned types of dividers can only provide a limited low operation frequency and are not as suitable for millimeter wave applications as LC ILFDs.

Figure 2 shows an LC-oscillator based divide-by-2 ILFD that was proposed in [20]. The working mechanism of this ILFD is similar to other types of ILFDs. The input signal is injected to the gate terminal of an NMOS M_4. When the positive peaks of the input signal arrive, M_4 will be turned on and then the two outputs are shorted. Therefore, the positive peaks of the input signal will result in zero-crossing points of the differential outputs (two zero crossings per ILFD cycle). By carefully designing the free-running oscillating frequency of the ILFD to be around half of the input frequency, the ILFD implements a division ratio of two. However, due to the high-quality-factor of the LC oscillator in ILFD, the locking range is quite narrow, i.e., only a 3% tuning range is obtained at a 50 GHz center operating frequency for the proposed ILFD reported in [20].

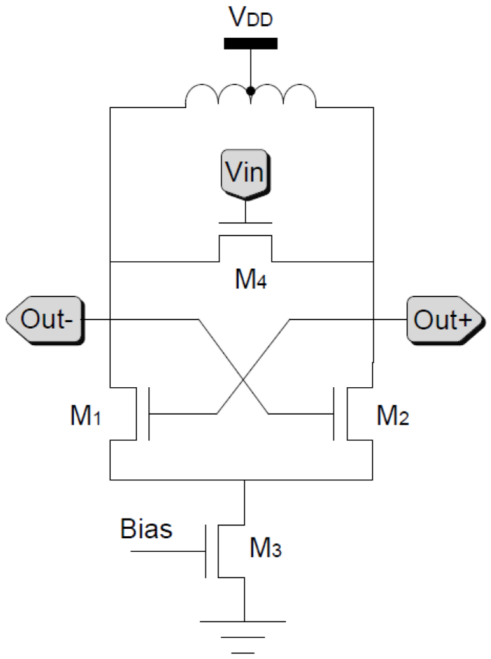


Figure 2: A divide-by-2 ILFD [19].

This narrow tuning range has resulted in difficulties in PLL designs. Intuitively, an ILFD with a working range as wide as the VCO tuning range can satisfy and ensure proper locking. However, for millimeter-wave circuits, even the routing parasitic can lead to significant frequency shifting. Take the ILFD in [21] as an example, it is observed that a 20 um routing path of metal4 corresponds to 1-2 fF parasitic capacitance, which would cause the center frequency of the ILFD to drift by 300-500 MHz. Therefore, in order to ensure proper locking along the loop for all

process, voltage and temperature (PVT) corners, it is desirable to keep about two times of margin of the frequency operation range, which will require more design effort to overcome the abovementioned inherent narrow tuning range of ILFDs. ILFDs with switched capacitor banks can widen frequency ranges, but this requires additional efforts in matching frequency harmonics of ILFDs and VCOs.

2.1.1.2. Regenerative dividers

Originally proposed by Miller in 1939, the regenerative divider is also called Miller divider or dynamic divider. Basically, the regenerative divider is based on mixing the output with the input and filtering out higher frequencies in the result [22], as shown in Figure 3.

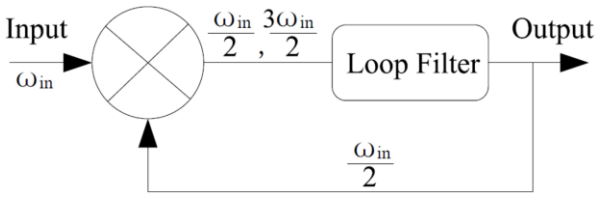


Figure 3: General structure of a regenerative divider that consists of a mixer and a filter.

By carefully adjusting phase and gain conditions, the component at half of the input frequency survives and circulates around the loop. Since both the device capacitances and the parasitic capacitances can be absorbed in the low-pass filter, a regenerative divider can achieve a very high speed and is widely used in bipolar, GaAs and millimeter-wave CMOS designs. However, mathematical calculations have shown that proper operation of the regenerative divider requires either sufficient broadband phase shift around the loop or enough suppression of the third harmonic (or a combination of both) [22]. Bandpass loads that contain inductors are usually used to suppress the third harmonic in a CMOS regenerative divider. Similar to ILFDs, regenerative dividers also consume large areas and have limited frequency ranges due to the inductors.

2.1.1.3. Example of a 75 GHz PLL

In [21], a 75 GHz PLL was demonstrated in 90 nm CMOS technology. To design a PLL at such high frequencies, a robust VCO together with carefully designed dividers are highly desirable. More significantly, operation locking ranges of the dividers need to be carefully optimized along the divider chain to ensure functionality. As previously mentioned, any unexpected device

parasitic or routing parasitic capacitance will result in significant frequency shift in the VCO and dividers. Therefore, it is much more challenging when connecting these blocks with perfect frequency alignment inside a loop than designing them individually.

To implement a PLL at such a high frequency, design tradeoffs between the operating frequency and the frequency range were carefully considered. Specially, different types of dividers were employed in [21] along the divider chain. An ILFD was applied right after the VCO as the first-stage divider because ILFDs can achieve the highest operation frequency albeit with a limited narrow working range. Then regenerative divider, which can be viewed as a compromise between locking range and working range, was applied as the second-stage divider. With the above two stages of dividers, millimeter-wave frequency was converted to relatively low frequency that is suitable for static CMOS dividers based on flip-flops. The block diagram of the divider chain is shown in Figure 4.

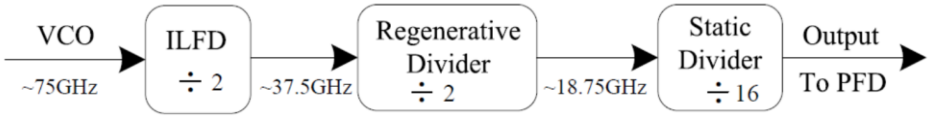


Figure 4: Divider implementations in a 75 GHz PLL [21]. A strategy of first ILFD, then regenerative divider and finally static divider is used in the divider chain design.

To conclude, high-speed dividers, including both ILFDs and regenerative dividers, usually resort to inductors and thus operates within a limited frequency range and take large silicon areas. Therefore, novel designs that function at wide frequency range, take small area and low design cost, are desirable.

2.1.2. Subsampling PLLs

To save the divider, dividerless PLL architectures have been extensively studied in the past decade. For example, PLL with an aperture phase detector (APD) was proposed in [23], injection-locked PLLs have been reported in [24][25]. Among all these dividerless PLL architectures, subsampling PLLs (SSPLLs) have attracted attention because of the superior in-band phase noise performance. In this section, integer-N SSPLLs are reviewed, and then recent progress on fractional-N SSPLLs, mm-wave SSPLLs and digital SSPLLs are discussed.

2.1.2.1. Integer-N SSPLLs

As shown in Figure 5 (a), an SSPLL uses a sampling PD that sub-samples the high frequency VCO output with the reference clock. Since the subsampling process cannot distinguish between the targeting frequency Nf_{ref} and other harmonics of f_{ref}, a frequency locked-loop (FLL) is typically used to pull in the VCO to the correct frequency before switching to the SSPLL to achieve phase lock. After locking, the FLL can be powered off to save power and avoid noise contributions to the output. A linear phase domain model for the SSPLL is shown in Figure 5 (b). As illustrated in Figure 5 (a) (b), there is no classical divide-by-N divider in the feedback path in both circuit implementation and phase domain transfer function. A virtual frequency multiplier "N", however, is present on the reference clock path in phase domain as illustrated in Figure 5 (b). Since the phase noise of CP and PD is not multiplied by N^2 when transferred to the output, the SSPLL has been reported to achieve state-of-the-art FoMs in the last decade [26][27][28][29][30].

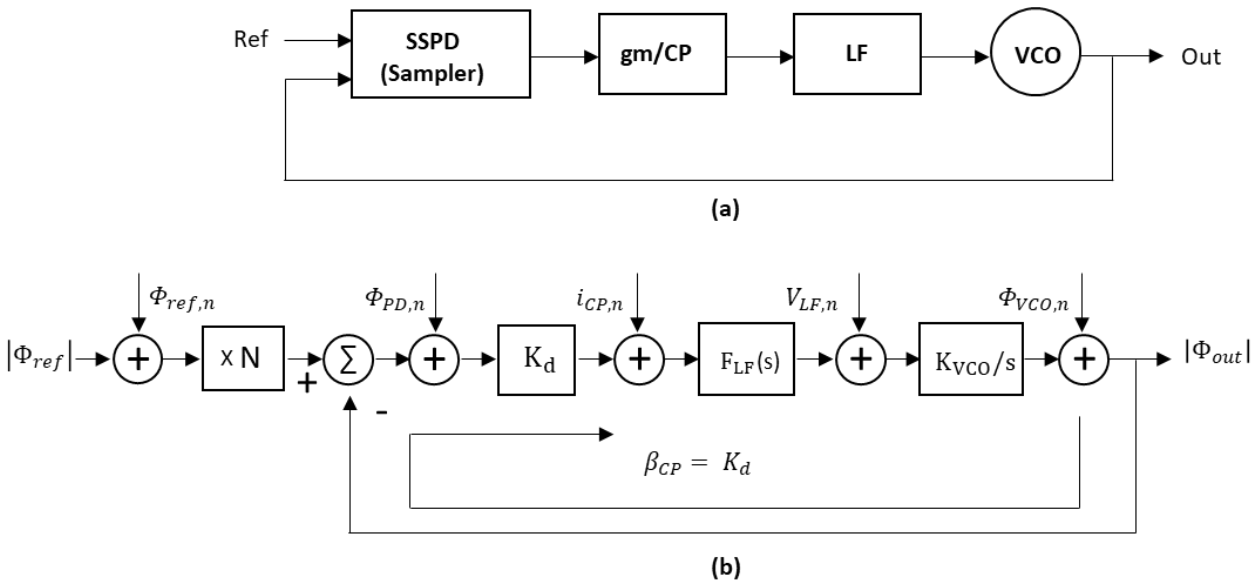


Figure 5: SSPLL (a) architecture, (b) phase domain model, where $\emptyset_{ref,n}$, $\emptyset_{PD,n}$, $\emptyset_{VCO,n}$, $i_{CP,n}$, $V_{LF,n}$ represent the noise contributions of the reference clock, phase detector, VCO, charge pump and loop filter, respectively [26].

2.1.2.2. Fractional-N SSPLLs

The original SSPLLs only function in integer-N mode and therefore cannot synthesize fractional-N frequencies. To solve this problem, researchers have proposed different circuit architectures to synthesize new frequencies by constantly rotating the phase of either the reference clock or the feedback from the VCO.

In [31], a digital-to-time converter (DTC) is used to repeatedly updated the reference clock phase to align the sampling clock edge (and thus the VCO zero-crossing when in lock) to achieve fractional-N behavior. However, the DTC is usually challenging since it needs to not only cover one entire VCO cycle but also perform with high resolution. A 10-bit high-resolution DTC is used to delay the reference clock edge to ensure a near-zero-crossing detection of the VCO output in [32][33]. Additionally, the nonidealities of the DTC limit the performance of the SSPLL. To solve this problem, N. Markulic et al. proposed to calibrate the nonidealities including DTC gain and nonlinearity in background and achieved an FOM of −246.6 dB in fractional mode in [34].

Instead of adjusting the rising edge of the reference clock using a DTC, another approach is proposed where the feedback signal fed into the SSPD is derived from the VCO, with an adjusted frequency through applying a constantly updated phase. For instance, phase interpolation (PI) techniques have been shown to efficiently create multiple phases of the VCO signal and achieve low in-band phase noise in fractional mode. For instance, D. Liao et al. proposed to use a capacitive phase interpolation network to generate 16-phase variants of the VCO output, which could adjust a PFD feedback signal to a different frequency from the VCO and achieved a FOM of -239 dB in fractional-N mode in [35]. A. Tharayil Narayanan et al. proposed a circuit architecture to combine the advantage of both DTC and PI, which allows a lower resolution in both the DTC and the phase-interpolator [36]. For instance, a −249.5 dB FoM is achieved with a 5-bit DTC and a 5-bit pipelined PI [36].

Current implementations of the SS-PLL, no matter in integer-N mode or fractional-N mode, have the limitation that, in lock, at the sampler, the sampled input frequency must be an integer multiple of the sampling clock (although each signal may be optionally processed through some frequency adjustment).

2.1.2.3. mm-Wave SSPLLs

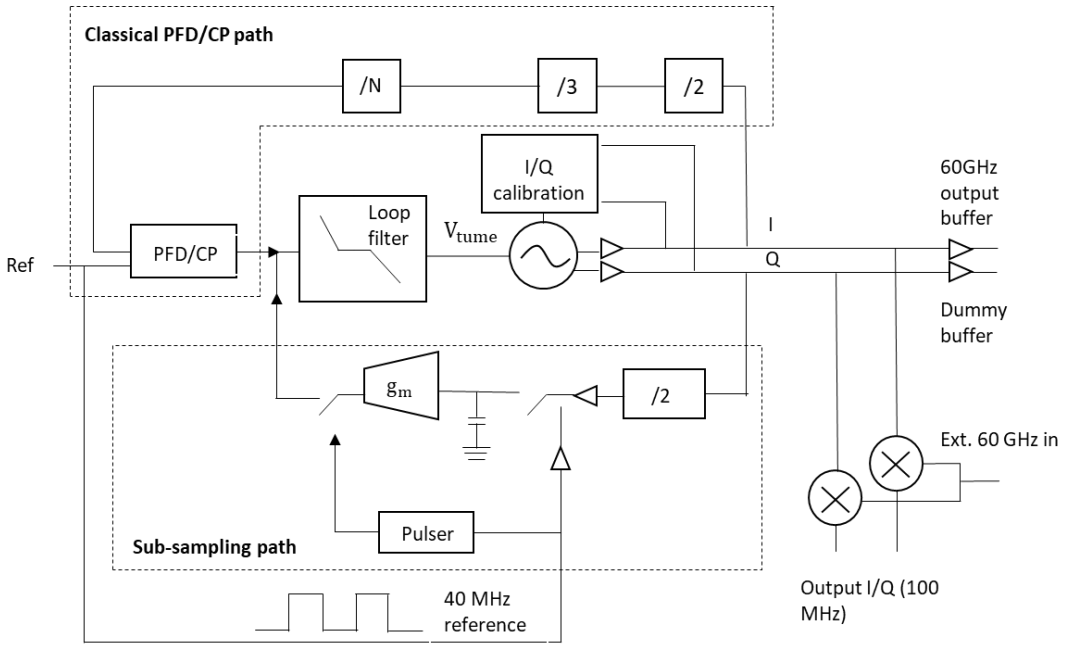


Figure 6: A 60 GHz mm-wave SSPLL [40].

As mentioned above, an SSPLL has the advantage of not multiplying the PFD and charge pump phase noise by N^2 (where N is the ratio of the targeting VCO frequency and the reference frequency). The millimeter wave (mm-Wave) VCO usually demonstrates poor phase noise performance due to the lower quality factor of the LC tank. This makes SSPLL more attractive in mm-Wave frequency synthesis. Additionally, the sampling PD can work at a much higher frequency compared to the conventional PFD, and it benefits more as technology scales down to more advanced nodes. Because of these advantages, SSPLLs are very popular in mm-Wave applications in recent years.

In [37], an SSPLL has been demonstrated to synthesize a VCO output up to 104.8GHz using a cascaded PLL circuit architecture, where a fractional-N PLL is applied to increase the sampling clock frequency to ~2.75 GHz first. Other researchers, however, prefer to divide a mm-wave VCO frequency before the subsampling phase detector (SSPD) instead of direct subsampling. In [38], J. Kim et al. suggest that directly subsampling is not suitable for mm-wave frequency synthesizing due to the limited capture range of the sampling operation. For instance, a 28.0-31.0 GHz frequency was synthesized in [39] using injection locked frequency multiplication with a

3.3-4.3 GHz frequency generated by an SSPLL. In another example, a 60 GHz SSPLL was built with an inductively-peaked static divider and a SSPD running at 30 GHz [40]. With the exception of [37], usually researchers don't use direct analog subsampling to synthesize frequencies much over 30 GHz [40][41][42]. Figure 6 shows an example 60GHz SSPLL design from [40]. The VCO is firstly divided by 2 before being sampled by the SSPD.

2.1.2.4. Digital SSPLLs

Digital PLLs are popular in recent years since traditional analog PLLs become more problematic as process scales down. After the first publication of SSPLL in [26], researchers have proposed various implementations of digital SSPLLs.

In a traditional SSPLL, the subsampled voltage signal is first converted to current using an analog gm-cell and then processed by an analog loop filter. In [43], Z. Chen et al. proposed a digital SSPLL that first uses an ADC (analog-to-digital converter) to digitalize the subsampled voltage to digital codes and then processes the digital signals in the digital domain. The chip was implemented with an 8b ENOB (Effective Number of Bits) SAR-ADC in 65 nm CMOS technology and a state-of-the-art FoM of -241.8dB was achieved [43]. Instead of using a multiple-bit ADC or TDC (time-to-digital converter), D. Tasca et al. proposed a simplified circuit architecture to use a bang-bang PD to implement a digital SSPLL [44]. A single D-flip-flop, as a 1-bit TDC, was used to digitalize whether the VCO lead or lagged the active edge of the reference clock. Also fabricated in 65 nm CMOS process, the tested chip was measured to have a state-of-the-art FoM of –238.3dB.

2.1.3. Alias-Locked Loop (ALL)

To address the issues of narrow tuning range and additional inductors (with their large areas) found in high frequency PLLs as discussed in section 2.1.1, a new type of frequency synthesizer, named the alias-locked loop (ALL), was proposed in [15].

2.1.3.1. General Structure of an ALL

An ALL used a digital sampler as the first stage of a divider, avoiding ILFDs or regenerative dividers, and the additional area-intensive inductors that these circuits bring. Previous

subsampling based PLLs resort to analog samplers and are aimed at better power and noise performance. For instance, an 896 MHz - 902 MHz analog subsampler was proposed to replace the prescaler in [45] and a 2.2 GHz analog subsampler was used as phase detector in [26][27]. In the ALL architecture proposed in [15][16], the traditional divider was replaced by an aliasing divider, implemented with a high-speed digital sampling latch, although a D flip-flop (D-FF) can be used. This sampling circuit used a stable reference clock to sample the voltage-controlled oscillator (VCO) signal. Since the sampling frequency was significantly lower than the sampled signal, the VCO signal was subsampled, creating an alias frequency. In this way the high frequency of the output signal of the VCO can be lowered, which in turn can be fed into a CMOS divider or directly to a conventional phase-frequency detector (PFD). Similar to a PLL with a fractional-N divider or a bang-bang phase detector, the ALL structure gained a lower cost in area and power consumption compared to a traditional PLL.

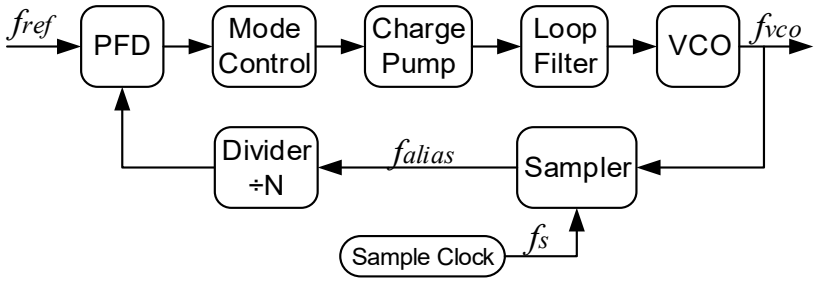


Figure 7: A general block diagram of an ALL [15]. Instead of using high cost ILFDs or regenerative dividers, an ALL employs a digital sampler in the feedback path.

Figure 7 shows a general structure of an ALL. Most of the modules in an ALL are the same as in a traditional PLL. A PFD compares the phase (frequency) of the reference clock with the feedback signal and then generates a control signal for a charge pump. The charge pump converts the phase difference to current that controls the charging or discharging operation of the capacitor in the loop filter, thereby the control voltage of the VCO is tuned. Different from a traditional PLL, however, the divider-by-N between the VCO and the PFD is replaced by a high-speed sampling circuit. In addition, a divider is applied after the sampling circuit. Adding a module named Mode-Control that inverts the sense of the PFD as required when the alias frequency is negative, an ALL is a continuously negative feedback loop and therefore able to

lock the targeting frequency. Details of the Mode-Control module will be discussed in Section 3.4.

The frequency relationship in an ALL can be written as:

$$f_{alias} = f_{RF} - f_s \times round\left(\frac{f_{RF}}{f_s}\right), \tag{2.1}$$

where the function *round(·)* rounds to the nearest integer value.

The phase difference of the divided alias signal and the reference signal is detected by a PFD. Since the frequencies of both signals are not high, a conventional PFD is sufficient. When the loop is locked, the absolute value of the divided alias frequency $f_{alias}/_N$ will be equal to the reference frequency f_{ref}, i.e.,

$$\frac{|f_{alias}|}{N} = f_{ref}. \tag{2.2}$$

Equations (2.1) and (2.2) lead to the following equation:

$$f_{VCO} = \begin{cases} M \times f_S + N \times f_{ref}, \ for\ f_{alias} \geq 0, \\ M \times f_S - N \times f_{ref}, \ for\ f_{alias} < 0, \end{cases} \tag{2.3}$$

where M can be any positive integer.

Once the loop is locked, the frequency determined by Equation (2.3) is synthesized. Multiple values of M can, however, satisfy Equation (2.3). Therefore, for a given reference signal and a constant sampling signal, there exist a number of VCO frequencies that can meet all the requirements and finally make the loop locked. This is different from a traditional PLL that can lock at one single frequency. As different initial conditions of the control voltage of VCO result in different M, and thus result in different output frequencies, careful considerations should be taken on choosing initial conditions of the VCO in an ALL. Designers can initialize the charge pump with a digital-to-analog converter (DAC) fed from a lookup table (LUT), so the ALL will start out and lock in the correct frequency range (correct value of M).

2.1.3.2. Discussion of an ALL

Figure 8 illustrates frequency regions produced by the aliasing divider. It can be observed that the sampling frequency directly determines the number of regions. If a lower frequency signal is applied as the sampling clock, then there will be more Region 0's and Region 1's within the VCO tuning range, which requires a high-resolution DAC fed from a lookup table to initialize the VCO into the correct frequency range. If a higher frequency sampling clock is applied instead, however, there will be fewer Region 0's and Region 1's, therefore easing the requirement of the DAC resolution. Compared to in a traditional PLL that the target frequency is controlled by the user by programming the division ratio, in an ALL the user selects the target frequency by controlling the DAC during frequency acquisition, and during phase lock the Mode-Control and the programmable divider.

Another drawback of a lower sampling frequency is that it will result in more special frequencies that require an alternate sampling frequency f_S to achieve lock. These frequencies are multiples of one half of the sampling frequency. As analyzed in Chapter 3, the alias frequency for these signals is 0. Take a sampling frequency of 1 GHz for example. If a 13 GHz (or 13.5 GHz) signal is desired to be synthesized, it can be seen in Figure 8 that the loop is not a negative feedback loop around the target frequency for either mode. Hence, the sampling frequency of 1 GHz cannot be used to synthesize this frequency. As a result, for these frequencies, a different sampling frequency has to be utilized.

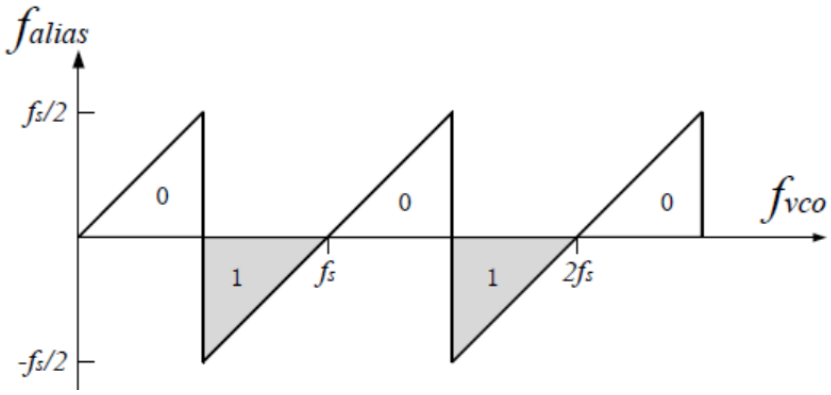


Figure 8: Frequencies produced by the aliasing divider.

2.2. Contribution of This Work

In this thesis, digital samplers in high-speed circuits are presented and their applications in phase-locked loops (PLLs) are demonstrated.

First, digital sampling circuits are analyzed, and the characterization methodologies are discussed. Simulation has shown that a digital sampler, no matter implemented by a sense amplifier or a current mode logic (CML) circuit, can greatly extend the operating frequency when compared to static digital dividers implemented with the same circuit architecture (i.e., through 130 GHz for circuit implemented in TSMC 40nm bulk CMOS process).

Second, we propose novel circuit architectures that we have named coresidual alias-locked loop (C-ALL), phase shift coresidual alias-locked loop (PS-CALL) and differential alias-locked loop (D-ALL), which employ digital sampling circuits instead of dividers. A C-ALL digitally produces the anticipated sampler output to reduce spurs (i.e., by as much as 27.7 dB in simulation), a PS-CALL guarantees feedback provided at every active edge of the alias signal to achieve fine phase lock, and a D-ALL locks on positive and negative alias frequencies to save the extra reference clock. These proposed circuits greatly extend the applications of SSPLLs, since previous work always has the limitation that, in lock, at the sampler, the sampled input frequency must be an integer multiple of the sampling clock (although each signal may be optionally processed through some frequency adjustment).

Additionally, we propose a new type of PLL circuit architecture with a VCO-based integrator to replace the charge pump and loop filter. This can avoid the large on-chip capacitor in a loop filter, and also mitigate the VCO output spurs resulted from the voltage ripples on the loop filter output.

CHAPTER 3. Digital Sampling

Mixers are ubiquitous in modern radio frequency (RF) transceivers. Mixing plays important roles in modern RF applications ranging from telecommunications to radio astronomy and biological sensing. A mixer, which by definition is a nonlinear electrical circuit that can produce continuous sum and difference frequencies of two or more input signals, is usually implemented with an analog multiplier and requires local frequencies to be close to or as high as the RF frequencies. As a special type of mixing, sampling allows using a low local frequency to down-convert the high-frequency RF signal. While a traditional multiplier-based mixer produces the sum and the difference of the two input frequencies, a sampler-based mixer produces the alias frequency instead. Existing work of RF sampling is dominated by analog sampling. In this chapter, digital sampling is analyzed and discussed.

3.1. Introduction of Sampling

According to Nyquist criterion, for a band-limited signal, as long as the sampling frequency is larger than two times of the signal bandwidth, there will be no information loss during the sampling process. Since RF signal usually has a very limited bandwidth, a much lower frequency, which only needs to be at least two times larger than the bandwidth, can be used to sample it. As the sampling frequency is much lower than the RF signal frequency, this kind of sampling is always referred to as subsampling. In this thesis, sampling and subsampling can be used interchangeably unless otherwise noted. Theoretically, the signal obtained from sampling can be used to restore the original information without any loss.

Assume the RF signal is represented by $x(t)$ in the time-domain and by $X(f)$ in the frequency domain. The sampling of the RF signal can be mathematically described by multiplying of $x(t)$ with Dirac impulses in the time-domain. The output of the sampling $x_s(t)$ can be written as:

$$x_s(t) = x(t) \cdot \sum_{k=-\infty}^{\infty} \delta(t - k \cdot T_s), \tag{3.1}$$

where $T_s = 1/f_s$ is the period of the sampling clock. The frequency domain representation is as follow:

$$X_s(f) = X(f) \cdot f_s \cdot \sum_{k=-\infty}^{\infty} \delta(f - k \cdot f_s) = f_s \cdot \sum_{k=-\infty}^{\infty} X(f - k \cdot f_s). \qquad (3.2)$$

Therefore, the input RF signal is aliased to frequencies spaced f_s apart from each other.

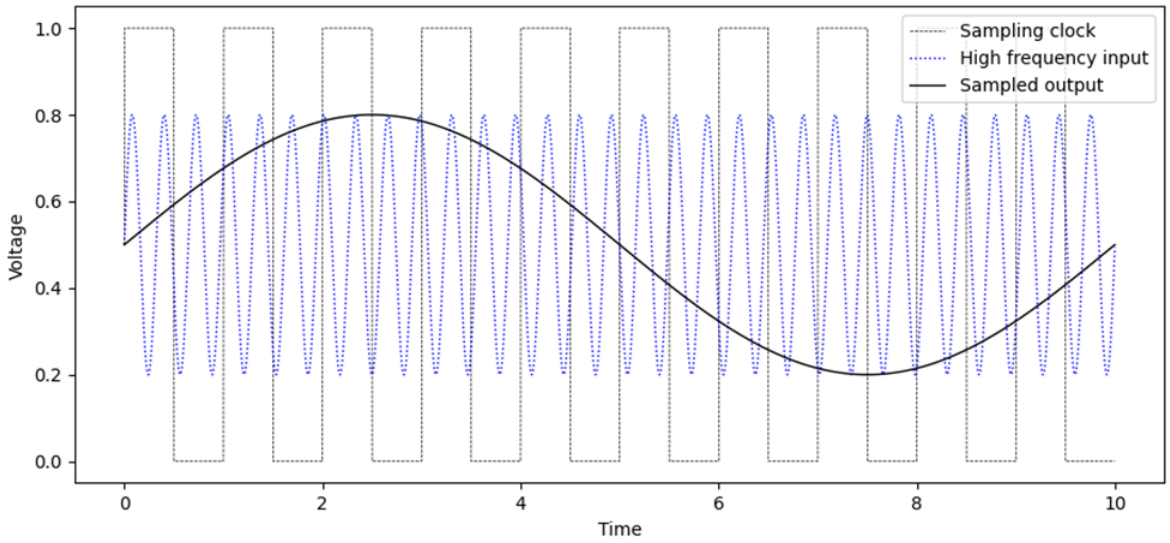


Figure 9: Illustration of sampling. Highlighted dark dots represent the operation of sampling, and the solid line represents the output signal after sampling [46].

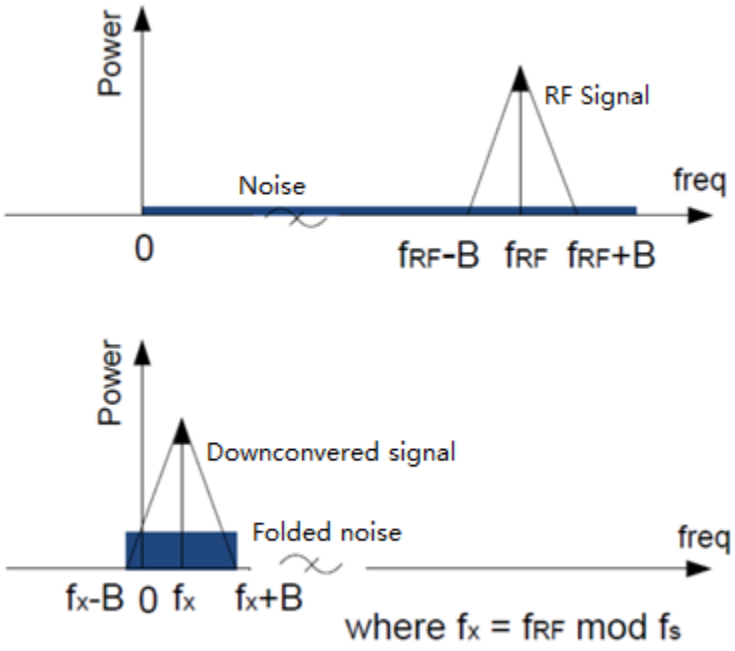


Figure 10: Sampling operation as down-conversion in frequency domain. Not only the high-frequency signal but also the noise within the sampling bandwidth is down-converted to baseband by sampling. Noise within the sampling bandwidth is folded and therefore degrades the SNR.

As is shown in Figure 9, the high frequency signal (represented by the solid line) is sampled at the instants indicated by the highlighted dark dots, and the output signal is shown as the lower frequency reconstruction (represented by the dash line). This is a down-conversion process. Figure 10 shows this down-conversion process in frequency domain. The band-limited RF signal is linearly moved to baseband with sampling frequency f_S. Meanwhile, the noise and interferers within the sampling bandwidth, both inside and outside of the signal bandwidth, are all sampled and eventually fall into the baseband. This phenomenon is known as noise-folding [46], which greatly degrades the signal-to-noise ratio (SNR) and limits the applications of sampling. Although this is not a problem in sampling-based PLLs because of the large amplitude of VCO signal, scenarios in a receiver where the signal amplitude is relatively small such as a radar is totally different. To alleviate noise-folding, bandpass filtering is usually proved to be an efficient technique. However, off-chip surface acoustic wave (SAW) filters are expensive while on-chip LC bandpass filters suffer from limited Q (quality factor) of the inductors.

3.2. Traditional Sampling Mixer

Track-and-hold circuits based on high-quality CMOS switches have been playing key roles in modern ICs. For instance, there are track-and-hold circuits in most ADCs. As can be seen from the following example, a properly designed track-and-hold circuit behaves as a sampling mixer.

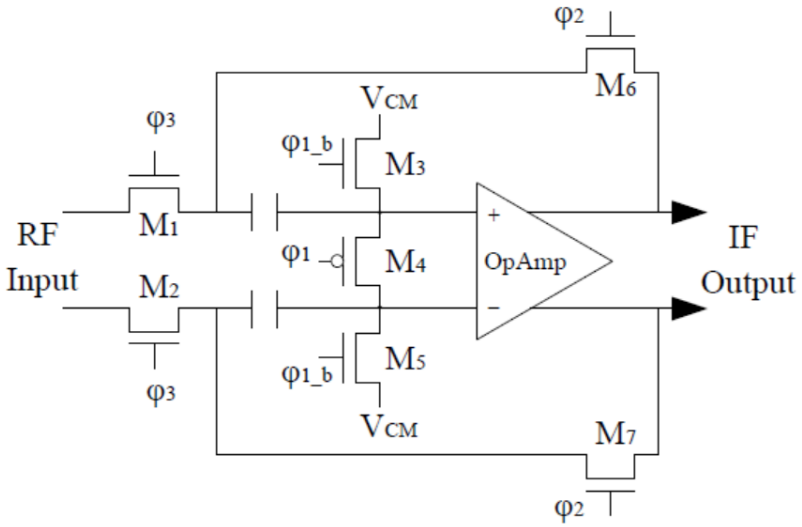


Figure 11: Simplified schematic of a track-and-hold sampling mixer [47].

A sampling mixer based on track-and-hold circuit was proposed in [47] as illustrated in Figure 11. In the track mode, M_1 - M_5 are all turned on while M_6 and M_7 are off. The right-hand plates of the sampling capacitors are equal to the common mode voltage, while the left-hand plates are used to sample the RF inputs at this instant. Since M_6 and M_7 are open, the operational amplifier doesn't impact the track mode operation, the tracking bandwidth is only limited by the RC time constant formed by the switch resistances and all the capacitances (sampling capacitances and also parasitic capacitances). Very high tracking bandwidth can therefore be achieved. In the hold mode, all the switches are reversed and then only M_6 and M_7 are turned on. A pair of charged capacitors feeding back around the operational amplifier is formed, and the sampled voltages in the track mode are held as the outputs in this mode. Although the bandwidth of the circuit is greatly reduced due to the feedback of the operational amplifier, the settling time only needs to be small compared to the sampling period no matter how high the RF input frequency is. Because of the inherent advantage of sampling, the proposed mixer provides a highly linear performance.

Despite of the great simplicity and high performance, sampling mixers are not widely used mainly due to two reasons.

Firstly, although the sampler is clocked at a relatively low sampling frequency, the sampling clock must provide very precise time resolution or else wrong instants will be sampled. This requires low jitters for the sampling clocks, which usually should be no more than a tiny fraction of the RF input signal periods. In case of high frequency RF signals, such as those in millimeter-wave range, the absolute jitter requirement is extremely high.

Secondly, the operation of sampling can result in noise-folding. As is discussed in the previous section and concluded in the textbook [46], great care needs to be taken if sampling is applied.

3.3. Digital Sampling

Different from sample-and-hold analog sampling, digital sampling can also be directly applied to sample the RF signal. The generated output will be the digital alias signal corresponding to the RF input. The digital sampler, in this case, can be viewed as a combination of an analog sampler

and a 1-bit analog-to-digital converter (ADC), thereby saving the normal ADCs with a sacrifice of precision.

3.3.1. Background

With the fast scaling down of CMOS technology, performance of digital blocks undoubtedly benefit more than analog blocks. On one hand, parasitics are lower, transistor speeds are increased and therefore higher timing resolution can be obtained. On the other hand, voltage resolution is substantially decreased due to the decreasing of the power supply voltage, and accurately modeling of MOS transistors has been increasingly more difficult. In addition, larger process variation results in decreased reliability and more severe aging effects are all degrading analog circuits [48].

As a result, increasingly more functional blocks that were historically implemented in analog modules are now being implemented digitally instead, resulting in increased flexibility and decreased cost. In wireless transceivers, advances in data converters have been pushing the border between analog and digital processing domain closer to the antenna [49]. As discussed previously, sampling techniques can provide an attractive alternative to traditional circuit architectures. Especially in recent years, RF sampling was proposed as a solution for SDR (software-defined radio) [50]. Several high-speed 1-bit digital receiver circuit architectures have been proposed, e.g. in [51][52]. However, these proposed implementations are either limited to theoretical discussions or suitable for circuit architectures based on simple modulation methods. Operating frequencies of these implementations are generally in Ultra-Wideband (UWB), which are lower than millimeter-wave frequencies. Moreover, less robustness against interferers limits the applications of these transceivers.

As can be shown in the following discussion, RF sampling and directly digitizing for high frequency such as millimeter-wave is desired, and the digital sampler can be modeled as an analog sampler and a 1-bit ADC. A digital sampler is also equivalent to a threshold (comparator) feeding a digital input latch. In a realistic scenario, non-ideals include input-referred noise, delay, DC offset, hysteresis and etc.

3.3.2. Digital sampler architecture

In this section, two different types of circuit architecture, one based on sense-amplifier latch and the other based on current mode logic (CML) latch, are presented and discussed.

3.3.2.1 Sampler based on sense-amplifier latch

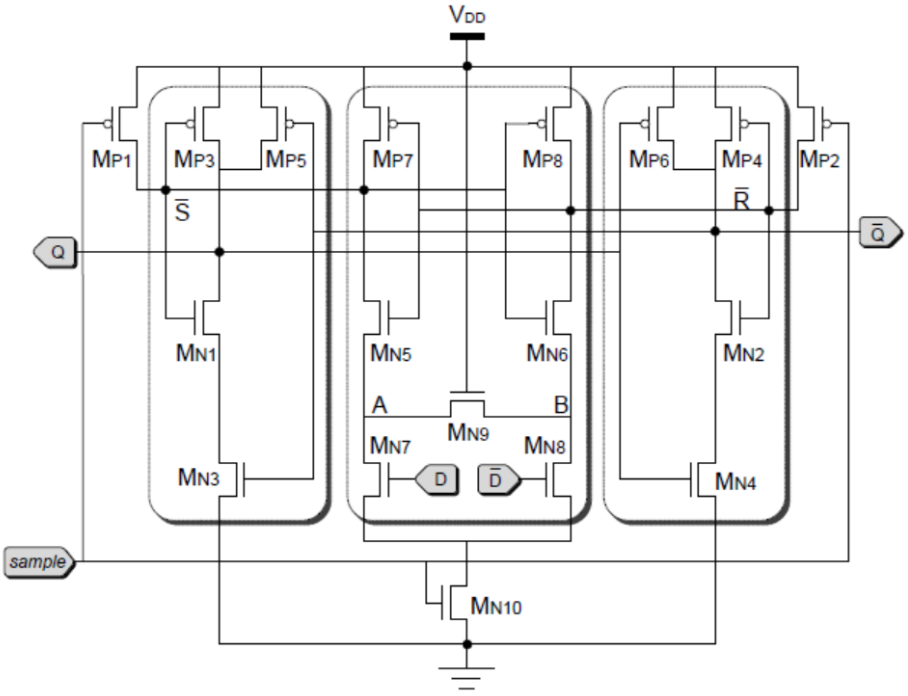


Figure 12: Sense-amplifier sampling circuit [54], commonly referred to as a StrongARM latch [55]. The first stage (in the center) senses a differential input, while the second stage (on both sides) provides a full-swing output signal.

The original idea of a high-speed digital sampler is based on a sense-amplifying latch [53][54]. A sense-amplifier flip-flop (SAFF) is produced by adding an SR latch to the output of the sense amp, which produces a rising edge triggered flip-flop with an output that is valid except in transition. One of the most commonly used SAFF is the so-called StrongARM latch which is shown in Figure 12. A sense amplifier is typically applied in the dynamic random-access memory (DRAM) and static random-access memory (SRAM) implementations because it can detect a subtle voltage difference. Combined with CMOS differential logic, sense-amplifying

structures can significantly improve performance (i.e. delay reduction) and cost (size and power reduction).

We observe that most latches and flip-flops can successfully sample higher input frequencies (at the D inputs) than the maximum frequency at their clock inputs. For this reason, latches and flip-flops can be used at higher frequencies as aliasing dividers than as conventional dividers. Generally, the highest frequency at which the SAFF can function properly is determined by the precharge period. When applied as a flip-flop, the precharge phase of the SAFF is determined by the input signal because it should recognize every single edge of the input. This is different when a SAFF is applied as a digital sampler, where the precharge phase in an SAFF is determined by the sampling frequency instead of the input signal. As discussed in Chapter 4, it is the SAFF structure that makes it possible to reach as high as 130 GHz input frequency in the proposed digital sampler design, compared to a highest operating frequency of less than 20 GHz for the same SAFF circuit used in a static divider under the same condition in the same 40 nm CMOS process.

As shown in Figure 12, the circuit of the digital sampler is composed of two cascaded latches. The sense-amplifying master latch consists of M_{P7-8} and M_{N5-9} with dynamic logic. The dynamic logic requires two phases: precharge phase when the clock signal is low and evaluation phase when it is high. During precharge phase, M_{P1} and M_{P2} turn on and M_{N10} turns off. Since M_{N9} always turns on at this phase, nodes $\overline{S}$, $\overline{R}$, A and B are all charged to high. In the evaluation phase, M_{P1} and M_{P2} turn off and M_{N10} turns on. The differential input voltage of D and $\overline{D}$ determines that A and B have different voltages before they are completely discharged. During this tiny discharge time delay on M_{N9}, the state of the input is latched. The cross transistor, M_{N9}, forces the whole differential tree precharge and discharge rapidly in every clock cycle, regardless of the state of input data [54]. Therefore, the delay of M_{N9} will affect the speed of latching. With any input offset error less than the RF input signal for the sampler, the f_{alias} signal will continue to be produced, albeit with an asymmetric duty cycle. Observing the active (e.g. rising) edge of the output of the sampler, the asymmetric duty cycle would be observed as a constant phase offset compared to an ideal sampler, which would not affect the loop behavior.

3.3.2.2. Sampler based on CML latch

Similar to the sampler based on a sense-amplifying latch, a sampler based on CML latch also consists of two stages. Since the restoring latch as the second stage is the same as the one shown in Figure 12, Figure 13 only illustrates the first stage. The sense-amplifying master latch consists of R_{1-2} and M_{N1-7}. Note that peaking inductors $L_{1-2}$are optional and can be applied to increase the bandwidth for high frequency applications. The sampler requires two phases: sensing phase when 'CLK' is high and evaluation phase when 'CLKb' is high. Operation of a CML based sampler is similar to a sense-amplifier based sampler, so this will not be discussed again in this thesis.

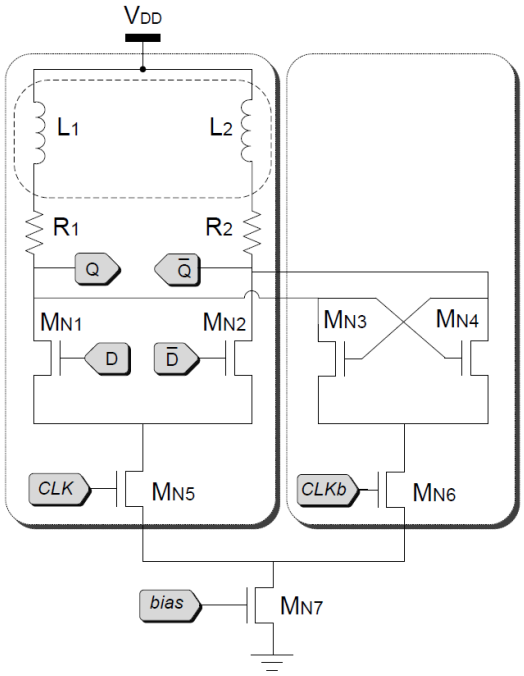


Figure 13: Sampler based on a CML latch.

3.3.3. Behavior of the digital sampler

Assume the RF input with a frequency of f_{RF} is sampled with a pulse clock, whose frequency f_S is much lower than f_{RF}. Since sampling occurs at the rising edge of the sample clock, only the residue frequency is reflected into the output of the sampler (by dividing the RF frequency f_{RF} by the sampling frequency f_s). The output of the sampling circuit is a so-called alias signal of the

RF input. The frequency of the alias signal f_{alias} is determined by both f_{RF} and f_S, as shown in Figure 14. We describe f_{alias} as being negative, if when f_{RF} increases, f_{alias} decreases, or vice versa.

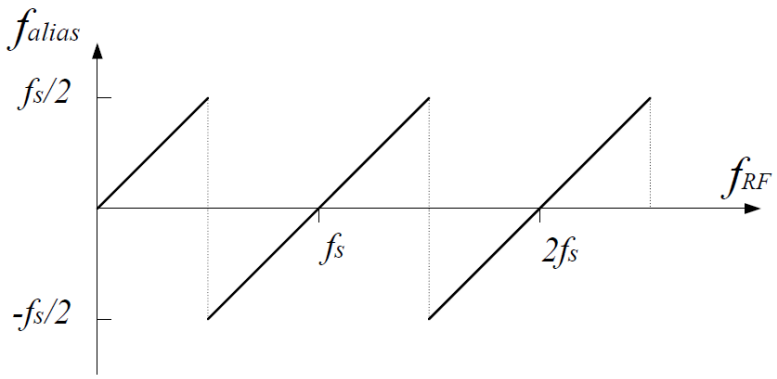


Figure 14: Alias frequency produced by the digital sampler. f_{RF} represents the RF input frequency, f_S represents the sampling frequency and f_{alias} represents the output alias frequency.

Therefore, the frequency can be calculated as:

$$f_{alias} = f_{RF} - f_s \times round\left(\frac{f_{RF}}{f_s}\right), \tag{3.5}$$

where $round(\cdot)$ rounds to the nearest integer value.

3.3.4. Mathematical explanation

Still assume that f_{RF} is the RF signal frequency, and f_s is the sampling frequency,

$$f_{RF} = x \times f_s, \tag{3.6}$$

where x is a positive fraction.

Let

$$x = L + r, \tag{3.7}$$

where L is a non-negative integer, r is a fraction and $0 \leq r < 1$. Further assume

$$r = \frac{P}{Q}, \tag{3.8}$$

where both P and Q are positive integers, and $0 \leq P < Q$. Applying Equations (3.7) and (3.8) into (3.6), we obtain

$$f_{RF} = L \times f_s + \frac{P}{Q} \times f_s. \tag{3.9}$$

Noting that the period $T = \frac{1}{f}$, Equation (3.9) implies

$$Q \times T_s = Q \times L \times T_{RF} + P \times T_{RF}. \tag{3.10}$$

Equation (3.10) shows that during a time of $Q \times T_s$, the sampler gets Q samples of the inputs. Among the Q samples, the outputs get the same voltage value ('0' or '1') for P times, while for the other $Q - P$ times, the other voltage state ('1' or '0') is sampled. So when $P < \frac{Q}{2}$, the sampled output voltage flips P times; when $P > \frac{Q}{2}$, the sampled output voltage flips $Q - P$ times. This means that with a total of Q samples within each $Q \times T_s$ time period, the sampled output voltages flips $min\ (P, Q - P)$ times. Therefore, the average period of output signal, $\overline{T_{out}}$, is

$$\overline{T_{out}} = \frac{Q \times T_s}{min\ (P,Q-P)}. \tag{3.11}$$

Thus, the average frequency of output, $\overline{f_{out}}$, is

$$\overline{f_{out}} = \frac{min\ (P,Q-P)}{Q \times T_s} \times f_s. \tag{3.12}$$

However, it should be noted that when $P > \frac{Q}{2}$, if the frequency of the input of the sampler increases, the output of the sampler is lowered instead of being increased, which is different from the condition when $P < \frac{Q}{2}$. This is the reason that some of the alias frequencies are negative, as will be shown in Figure 25. It should also be noted that Equation (3.12) has also mathematically demonstrated the residue operation of a digital sampler.

3.3.5. Non-ideality discussions

Previous discussions assume ideal behavior of digital samplers. In real implementations, however, there are various types of non-idealities, including DC-offset, hysteresis and different type of noise sources. In this subsection, the impact of these non-ideal properties will be discussed.

3.3.5.1. DC offset

During an evaluation phase, the correct operation of a sense amplifier will be impacted by numerous factors, such as the mismatch in the cross-coupled transistors and the load capacitance difference. These effects are the same as the comparator offset, which was extensively studied decades ago because of the wide applications of comparators in random-access memories (RAMs). It has been shown that these impacts during fabrication can be modeled by an equivalent input signal source, as shown in Figure 15 [56][57].

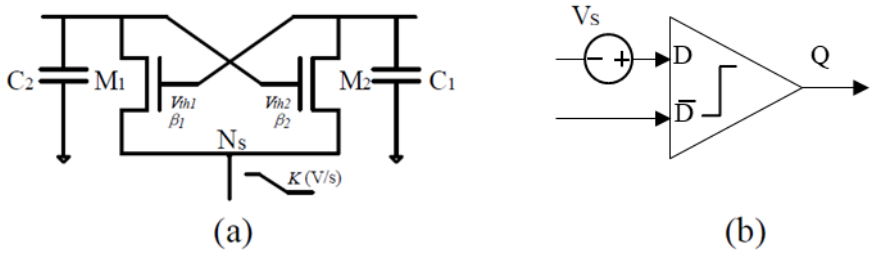


Figure 15: Modeling of offset in a comparator. (a) Simplified model of a comparator. (b) Equivalent model of the offset as an input source [56].

The following equation is proposed in [57] for calculating V_S:

$$V_S = A\sqrt{\frac{CK}{\beta}}\left(\frac{\Delta C}{C} + \frac{\Delta\beta}{\beta}\right) + \Delta V_{th}, \tag{3.13}$$

where

K: voltage decrease speed coefficient at N_S *(Unit: V/S)*,

A: proportional constant, approximately 0.5,

β: channel conductance, equals to $\mu C_{ox}\frac{W}{L}$,

C: load capacitor,

$\Delta V_{th} = V_{th1} - V_{th2}$,

$\Delta\beta = \beta_1 - \beta_2$,

$\Delta C = C_2 - C_1$,

$\beta = \frac{1}{2}(\beta_1 + \beta_2)$,

$C = \frac{1}{2}(C_2 + C_1)$.

It has been verified that Equation (3.3) closely matches simulated results over a wide operation range. Therefore, the impact of offset can be intuitively evaluated as shown in Figure 16 for different scenarios.

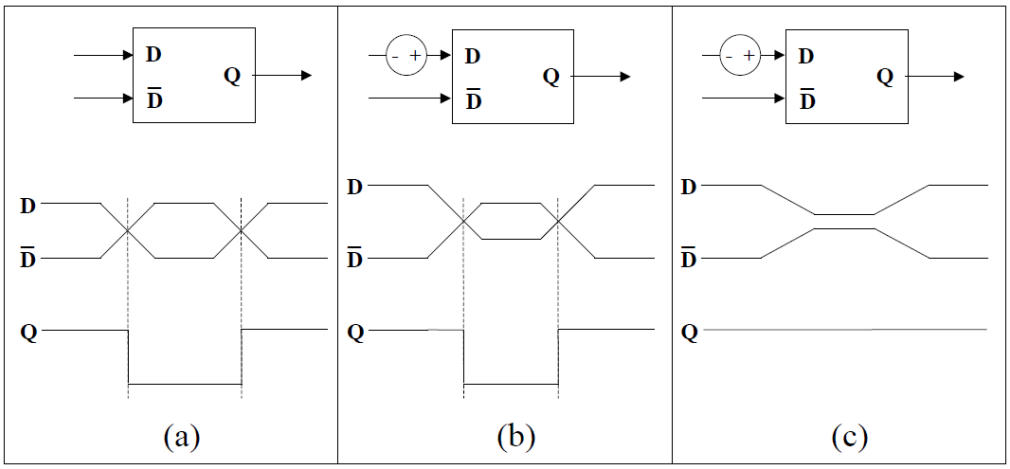


Figure 16: Impact of offset in digital sampler. Equivalent model of an offset and the output for: (a) no offset; (b) a small offset compared to sampled signal amplitude, where the offset only impacts on phase but not frequency, such as in an ALL. (c) a large offset compared to sampled signal amplitude, where the sampled signal will be lost, such as in a RF frontend.

If V_S is much less than the input signal amplitude, the sampler could still be functional depending on the applications. Take an ALL as an example, the alias output signal will continue to be produced, albeit with an asymmetric duty cycle, as shown in Figure 16 (b). Observing the active (e.g. rising) edge of the output of the sampler, the asymmetric duty cycle would be observed as a

constant phase offset compared to an ideal sampler, which would not affect f_{alias} and therefore would not affect the loop behavior.

However, for the applications with a weak input signal, such as in a RF frontend like a radar, if V_S is larger than the signal amplitude, the SAFF output will be unchanging and not functional as a sampler (as illustrated in Figure. 3.6(c)). Therefore, when applied in these scenarios, the equivalent value of V_S should be as small as possible, or at least, much smaller compared to the RF signal amplitude.

Since the causes of offset, such as the process variations and layout mismatches, are usually within a small limited range. With some further mathematical analysis on Equation (3.3), $|V_S|$ can theoretically be minimized to 0 by tuning load capacitances (Figure 17).

Based on the above observations, calibrations of the load capacitances should be provided for the applications such as RF frontends. Figure 17 shows a possible method resorting to two binary-weighted capacitor banks and digital control logic. It should be mentioned that this calibration method is at the cost of sacrificing the speed of the sampler due to the increasing of the load capacitances. However, the speed can be further optimized using the proposed multiple-stage sampler even when the load capacitances are larger.

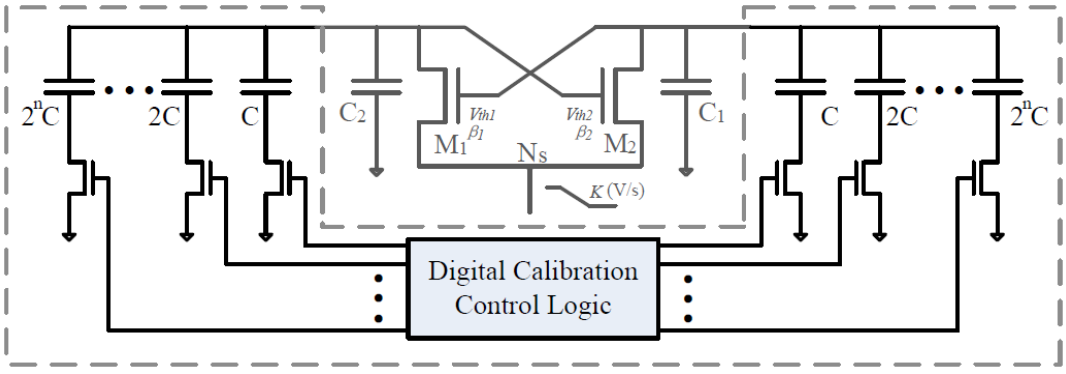


Figure 17: One possible calibration method of digital sampler. The calibration circuits, which resorts to two capacitor banks and digital control logic, is highlighted in the dashed box.

3.3.5.2. Power supply noise

Power supply could be a significant contributor of noise in integrated systems. Power supply noise comes from various sources and impacts the integrated systems in multiple ways. The following part presents two main sources of power supply noise and discusses the impact on the sampler, as illustrated in Figure 18.

Firstly, the power supply itself, no matter a DC-DC converter or a linear regulator, is noisy. The noise may come from the switching noise and incompletely filtered switching ripple for a DC-DC converter, or from the amplifier noise in the output and reference stages for a linear regulator [58].

Secondly, the digital switching can be coupled to the power supply and ground, and therefore impact the other analog or mixed-signal circuits. This is especially common for mixed-mode applications.

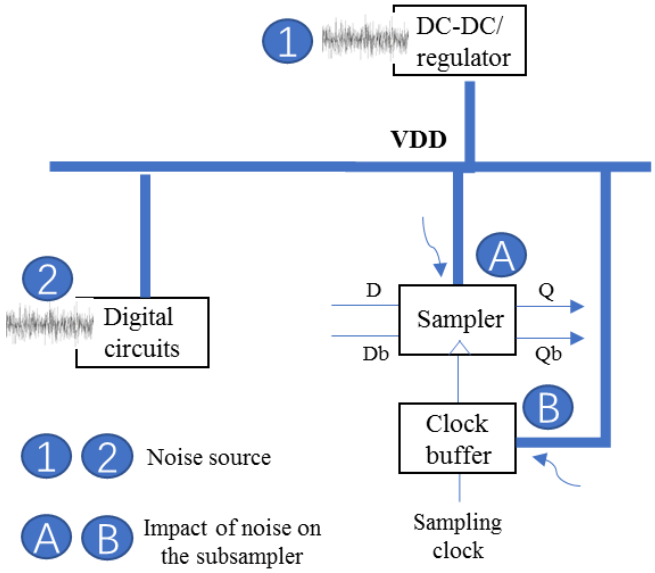


Figure 18: Power supply noise. Two main sources of the power supply noise are the power supply itself and the digital circuits. The generated power supply noise impacts the sampler through both the sampler itself and the sampling clock buffer.

The power supply noise can affect the performance of the sampler mainly in two ways as discussed below.

One is by impacting the operation of the sampler itself. Since the power supply noise is usually a common-mode noise, the impact of power supply noise can therefore be rejected by the symmetric and differential circuit architecture of a sampler. However, when taking the transistor mismatch into considerations, there would be an equivalent input-referred power supply noise at the input of the sampler. The output will be eventually determined by the sum of the input signal and the input referred power supply noise.

The other is by impacting the rising edge of the sampling clock via the clock buffer. The noise conducted through the power supply converts into phase noise in the output clock. The power supply noise can directly affect the zero-crossing of the clock buffer, and therefore cause a change in the rising edge of the sampling clock. An incorrect rising edge of the sampling clock will result in sampling the input signal at the incorrect instant, leading to an incorrect output. As will be discussed in Chapter 4, the phase noise or jitter in the sampling clock will be amplified by the sampler with a multiplication of the sampling ratio. Therefore, the power supply noise for the sampling clock buffer must be carefully designed and optimized.

To minimize the impact the power supply noise, several design techniques can be implemented:

i. Carefully design the DC-DC converter or the regulator by taking the load into considerations. Optimize the filters of the VDD distribution as well. This can minimize the noise generated by the power supply.
ii. Use separate VDD and GND lines for different modules. It is extremely important to isolate the sampler VDD from the noisy digital VDD. Put the digital sampler into a triple-well is also a useful technique if process permits, which can further alleviate the substrate coupled noise. Guarding rings could be an effective technique.
iii. Using non-overlapping clocks for the digital circuits and the sampler can effectively reduce the substrate noise, and also minimize the impact of the digital switching on the sampler.
iv. Optimize the layout of the sampler for the best symmetry. As mentioned above, with a symmetric circuit and layout, the power supply noise will be rejected as a common mode noise.

When take all the above-mentioned techniques in circuit implementations, power supply noise can usually be minimized, and the impact can be neglected.

3.3.5.3. Hysteresis

For static comparators, if the NMOS is turned on in the previous clock cycle, some charges will be left in the gate oxide traps, therefore impacts the threshold voltage of NMOS in this clock cycle; Similarly, if the PMOS is turned on in the previous clock cycle, some charges will be left in the gate oxide traps, therefore impact the threshold voltage of PMOS in this clock cycle. This property of dependence of the state of a system on its history is well-known as hysteresis. Hysteresis is widely applied in a lot of applications such as hysteresis comparators. However, in the proposed sampler that is based on dynamic logic, all the NMOS and PMOS transistors in the sense-amplifier are reset in the precharge mode within every clock cycle, therefore hysteresis is greatly decreased and usually negligible. Therefore, hysteresis is ignored in our analysis.

3.3.5.4. Transistor noise

Different from hysteresis, noise always exists and permanently impacts the operation of the sampler. There are multiple noise phenomenon within a transistor, including thermal noise, shot noise, flicker noise, and etc. Analytical modelling of the noise within the sampler is complicated, especially when taking all types of noise from all the transistors into consideration. In this section, impact of transistor noise will be analyzed through simulations.

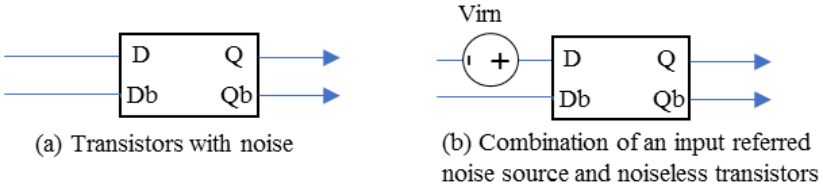
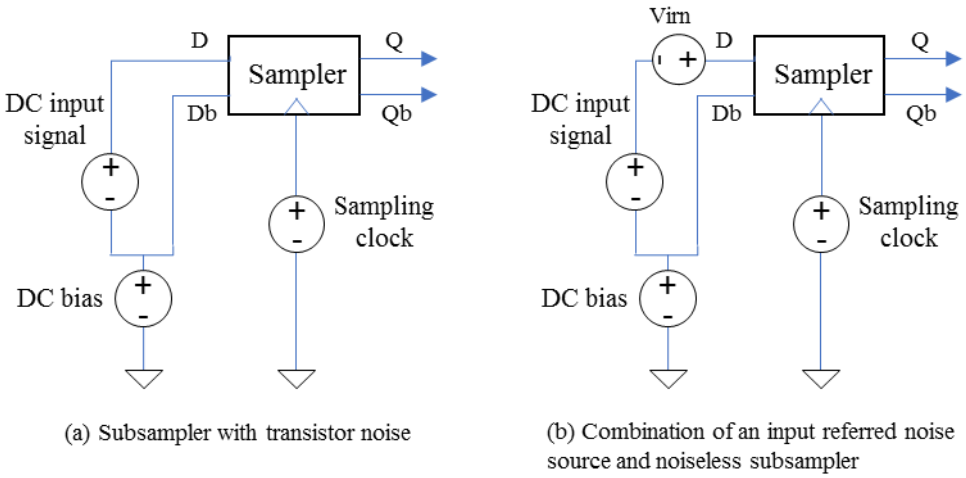


Figure 19: Noise within the whole sampler can be modeled as an input referred noise source. (a) A sampler with noisy transistors (b) the equivalent model of the sampler with noise-free transistors and an input referred noise source V_{irn}.

As discussed in [59], noise within a sense-amplifier can be modeled as an input referred noise source. An equivalent model of the sampler can be simplified as a sampler with noise-free

transistors and an input referred noise source, as is illustrated in Figure 19. In the following subsections, the distribution of the input referred noise will be studied through simulations.

The first simulation is setup as illustrated in Figure 20 (a). A DC bias, which equals to VDD/2, is applied as the common mode bias for the differential input. Another DC voltage is applied as the input signal. Since the sampler can be modeled as a combination of a noiseless sampler and an input referred noise source, the simulation setup can be equivalent as shown in Figure 20 (b). When the rising edge of the sampling clock arrives, the output is determined by the sum of the input-referred noise source $\boldsymbol{V_{irn}}$ and the DC input signal.



(a) Subsampler with transistor noise

(b) Combination of an input referred noise source and noiseless subsampler

Figure 20: Simulation setup of input referred noise distribution. A 1 GHz square wave (0 to VDD) is used as the sampling clock, a DC voltage of VDD/2 is used as the DC bias, and another DC signal is applied as the input. When the rising edge of the sampling clock arrives, the output is determined by the sum of the DC input signal and the input referred noise. Therefore, by observing the output distribution for a fixed DC input signal, the input referred noise can be analyzed.

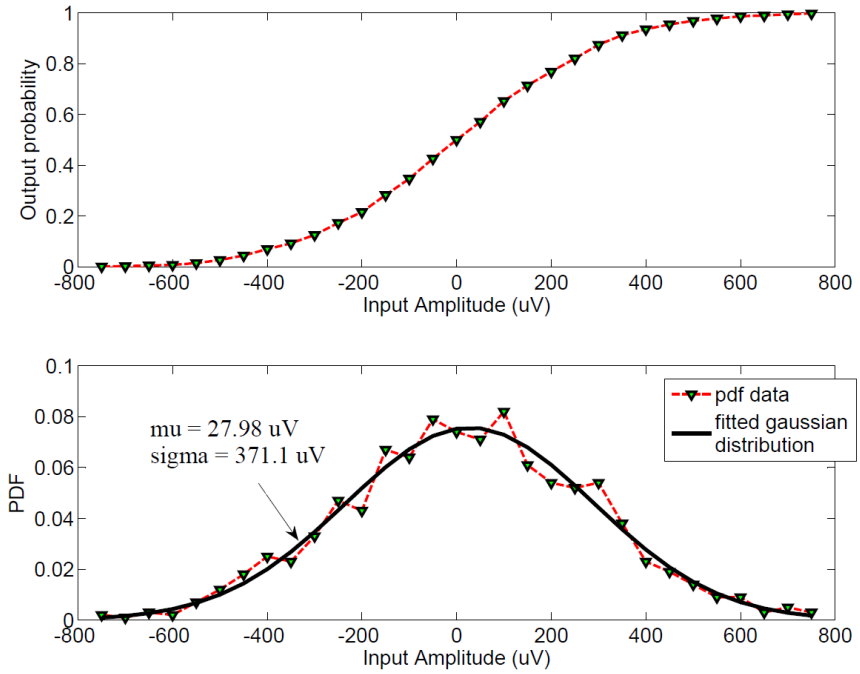


Figure 21: Simulation results for the input referred noise distribution.

The DC input signal is swept from -800 mV to 800 mV with a step size of 50 mV. For each voltage of the DC input signal, 1000 sampling cycles are collected for analysis. When DC input signal is below 0 (assume the DC voltage is $\boldsymbol{V_{DC}}$, where $\boldsymbol{V_{DC}}$<0), the output should always be 0 for a noiseless scenario. When take the input referred noise into consideration, however, the output equals to 0 with a certain probability. This probability corresponds to the probability that the input referred noise voltage is smaller than $-\boldsymbol{V_{DC}}$. In this way, the distribution of the input referred noise can be obtained as shown in Figure 21. The input referred noise follows a gaussian distribution. For a sense-amplifier based sampler built in GlobalFoundries 130nm Bulk CMOS process, the standard deviation is ~371 μV, which is consistent with [60]. In [60], the authors have calculated that the standard deviation of input-referred noise of the comparator σ is around hundreds of μV for both 90 nm and 65 nm CMOS process.

The second simulation is setup as illustrated in Figure 22. Transient noise from DC to 1 THz is applied, the sampling clock frequency is set to be 2 GHz and a differential RF signal with frequency around 77 GHz is used in Cadence Spectre simulations. Note that the output of the sampler will be uniquely determined by the 77GHz differential RF signal if the sampler is noise free. In the noisy scenario, however, the output will be determined by both the 77GHz

differential RF signal and the input referred noise. Therefore, the output of the noisy scenario can help to analyze the input referred noise.

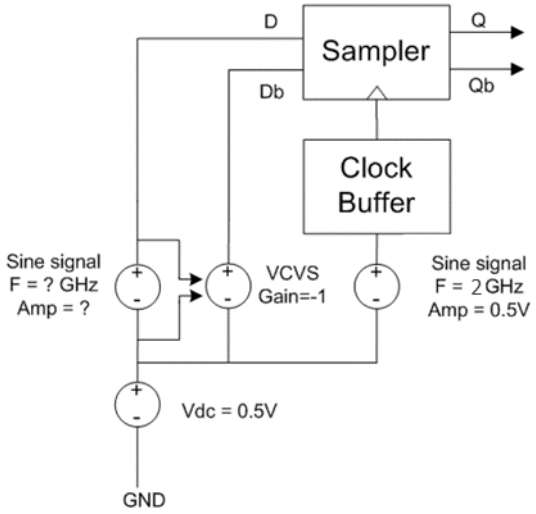


Figure 22: Simulation testbench setup. Transient noise from DC to 1 THz is applied, the sampling clock frequency is set to be 2 GHz and a differential RF signal with frequency around 77 GHz is used in Cadence Spectre simulations.

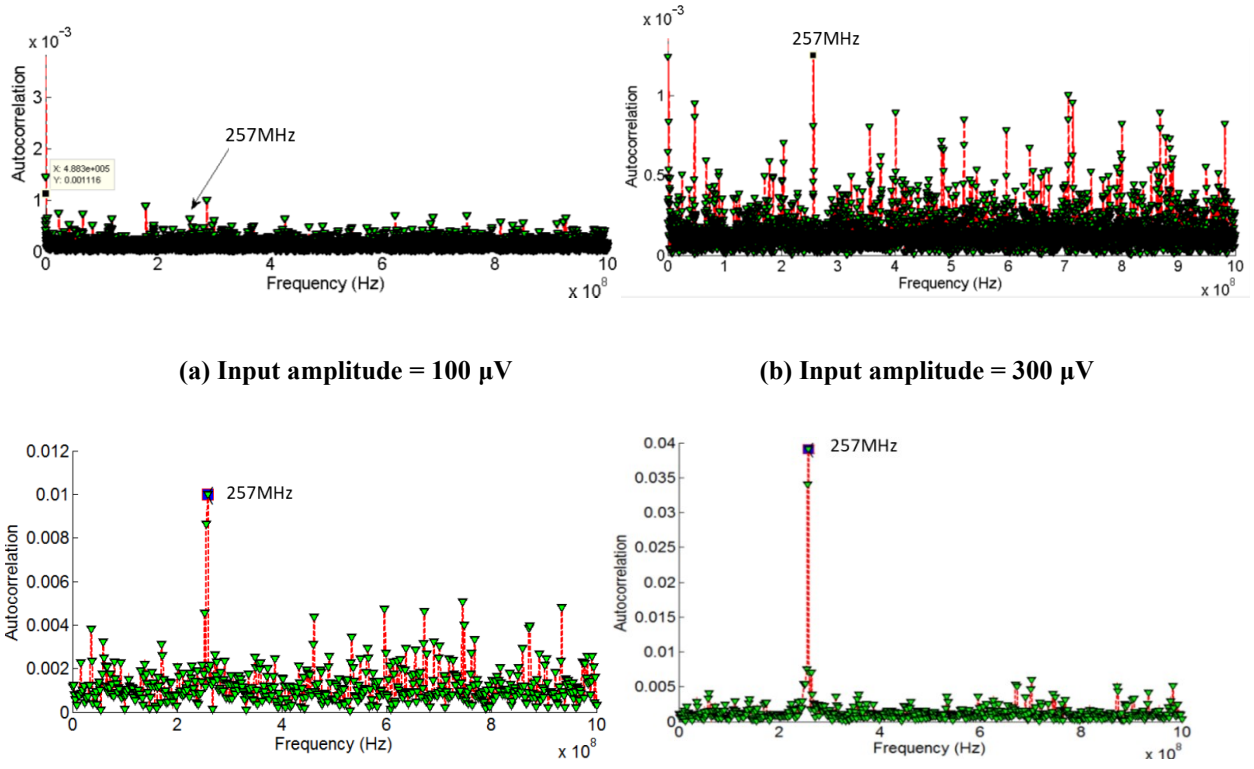
To verify the function of the sampler, frequency domain analysis is proceeded. For a time-invariant (also known as stationary) random process, the autocorrelation function (R) is defined as:

$$\mathrm{R}(\tau) = E\left[v_{out,Q}(t + \tau/2) \cdot v_{out,Q}(t - \tau/2)\right], \tag{3.14}$$

where $v_{out,Q}(t)$ represents the output of the sampler, τ represents the separation of the two noise samples in time and $E[\cdot]$ represents the expected value of the random process. By calculating the Fourier transform of the autocorrelation, we can then obtain the power spectral density (PSD) of the output signal.

The signal frequency is randomly selected to be 77.743 GHz. With a sampling clock frequency of 2 GHz, the sampler output is expected to be 257 MHz. If weak RF signal (i.e. amplitude = 100 μV) is directly sampled, the output would be heavily impacted by the input referred noise, and therefore the circuit cannot perform the expected alias function, as illustrated in Figure 23 (a).

As the input signal amplitude increases to 300 µV, it can be observed that the expected alias frequency is larger than the other noise frequencies, as shown in Figure 23 (b). When the input signal amplitude increases to 500 µV and 1 mV, the expected alias frequency demonstrates increasingly more power density than any other frequencies.



(a) Input amplitude = 100 µV

(b) Input amplitude = 300 µV

(c) Input amplitude = 500 µV

(d) Input amplitude = 1 mV

Figure 23: Simulation results for different RF input amplitudes with a RF frequency of 77.743 GHz and a sampling clock frequency of 2 GHz. As the signal amplitude increasing, output is determined more by the signal than the random noise. When the amplitude increases from 300 µV to 1 mV, the expected alias frequency can be observed with an increasingly larger power density. Simulation time is set to be 3 µs and therefore 6000 sampling cycles are simulated for each input amplitude.

Assume the power density at the expected alias frequency is P_1, and the largest power density at those undesired frequencies is P_2. By computing P_1/P_2, we can analyze the operation of sampler for different input RF signal amplitude. Here we define the Relative Power Density (RPD) function as:

$$\mathrm{RPD}(A_{in}) = 10\log(P_1(A_{in})/P_2(A_{in})), \tag{3.15}$$

where "A_{in}" represents the amplitude of the input RF signal.

Figure 24 presents how the calculated RPD changes for different input signal amplitudes A_{in}. It can be observed that when A_{in} is around or below 300 µV, RPD is below 0 dBc, which means the expected alias frequency is buried under the noise. As A_{in} increases, RPD becomes positive. When A_{in} reaches 500 µV and 1 mV, the RPD is 3.1 dBc and 6.9 dBc, respectively.

This is consistent with our analysis of the input referred noise distribution shown in Figure 21. When A_{in} is below or around the standard deviation (371 µV), the RPD is below or around 0, which means the output is heavily impacted by the input referred noise. When the input amplitude is much larger than the standard deviation, the RPD is larger than 0, which means the output is determined by the input signal. Usually, an RPD of 3dBc or larger can suffice for RF applications. For this specific sampler that is designed in GlobalFoundries 130nm Bulk CMOS process, the signal amplitude should be above 500 µV to obtain an RPD of more than 3dBc.

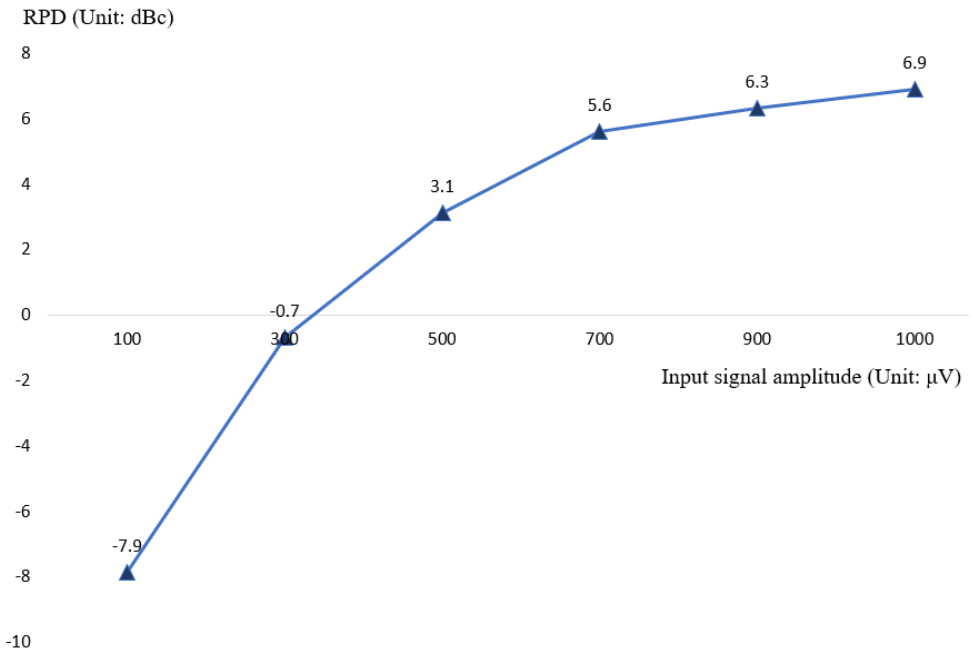


Figure 24: The RPD (Relative Power Density) changes for different input signal amplitudes.

3.4. Digital Sampler inside a PLL

Assuming a digital sampler is applied to sample a high-frequency signal, i.e. the VCO signal as in the case of an ALL, Figure 25 (a) illustrates the output frequencies produced by the aliasing divider. For the positive alias frequencies (Region '0' in Figure 25 (a)), the ALL becomes a negative feedback loop. This means that the loop is stable and can synthesize the targeting frequencies. However, if the alias frequencies are negative (Region '1' in Figure 25 (a)), the loop is a positive feedback loop and cannot achieve lock.

To solve this problem, a module named Mode-Control was added between the PFD and the charge pump to control the loop polarity as shown in Figure 5. This module inverts the sense of the PFD output (swaps the two PFD outputs: 'UP' and 'DOWN') for Region 1's in Figure 25 (a), restoring stable, negative feedback control. Figure 25 (b) shows the equivalent frequencies produced when Mode-Control is applied.

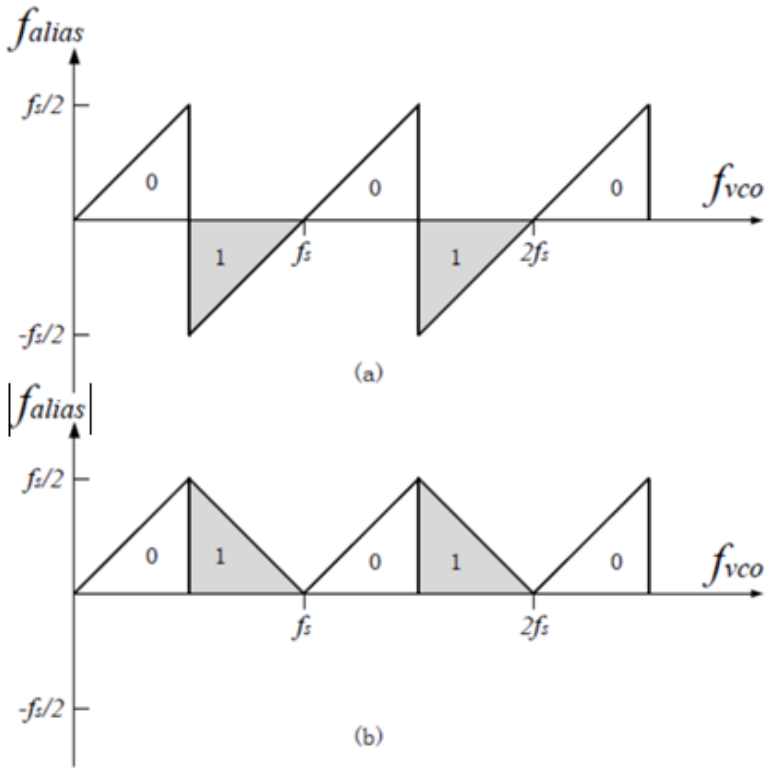


Figure 25: (a) Frequencies produced by the aliasing divider without Mode-Control. (b) Equivalent frequencies produced with Mode-Control.

3.5. Summary

This chapter reviews the traditional analog sampling and the applications of sampling as a mixer in wireless communications. Noise-folding phenomena is discussed as a main limitation of sampling. Then digital sampling is proposed and two possible digital sampler circuits are discussed. Implementations of digital sampling and mathematical explanations are also provided. Non-ideal properties including DC-offset and noise are discussed in practical implementations. Additionally, a module named Mode-Control is proposed to ensure the loop negative feedback and can therefore synthesize targeting frequencies.

CHAPTER 4. Characterization of Digital Samplers

Digital samplers have been widely used in modern circuits and systems. For instance, digital latches and flip-flops in digital systems, sense amplifiers in memories, clocked comparators in A/D converters, and regenerative amplifiers in high-speed I/O receivers can all be classified as digital samplers since they all sample the input voltage at certain time points such as the rising edge of the sampling clock. An ideal digital sampler would have the perfect sampling aperture, i.e. sampling the input voltage at exactly one point in time. A realistic digital sampler, however, captures a weighted average of the input voltage over a certain time window instead of a certain time point, and then makes the digital decision by the voltage below or above a threshold voltage.

For digital applications such as latches and sense amplifiers, digital samplers are usually characterized by setup and hold times together with the latch propagation delay. For analog applications such as clocked comparators, digital samplers are characterized by their sensitivity and bandwidth. The so-called impulse sensitivity function (ISF) has been developed to characterize many of the important characteristics of these circuits listed above. Under these scenarios, an ISF may be useful for predicting the sampled output for either a regular or irregular input at the latching speed, but it does not capture effects of device noise, which is a key limitation of subsampling to recover phase information for high-frequency recurring signals, as we intend to use it. For analog applications such as aliasing dividers inside PLLs or subsamplers in RF communication circuits where the signal is recurring, we want to know how device noise affects the accuracy of the sampled signal, and therefore we propose the sampling probability function (SPF) in this chapter.

4.1. Impulse Sensitivity Functions

In analog applications such as in serial link receivers, a digital sampler functions as a latch, and it can be viewed as a noisy nonlinear filter followed by an ideal sampler and slicer (comparator) as shown in Figure 26.

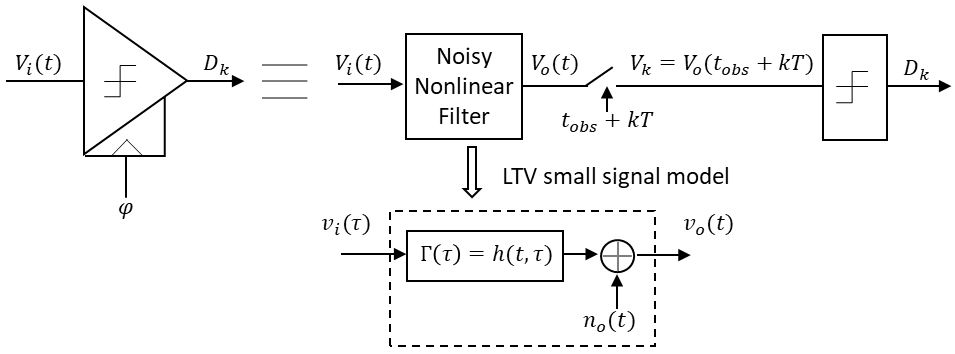


Figure 26: Linear Time-Variant Model of a digital sampler as a clocked comparator [60].

The small-signal comparator response can be modeled using an impulse sensitivity function (ISF):

$$\Gamma(\tau) = h(t,\tau) \tag{4.1}$$

The comparator ISF is a subset of a time-varying impulse response $h(t,\tau)$ for a linear time-variant (LTV) system, which can be expressed as:

$$y(t) = \int_{-\infty}^{\infty} h(t,\tau)\ x(\tau)\, d\tau \tag{4.2}$$

where $h(t,\tau)$ is the system response at t to a unit impulse arriving at τ. Output voltage of a comparator can be expressed as:

$$V_o(t_{obs}) = \int_{-\infty}^{\infty} V_i(\tau)\ \Gamma(\tau) d\tau \tag{4.3}$$

and the comparator decision can be calculated as:

$$D_K = sgn(V_K) = sgn\big(V_o(t_{obs} + KT)\big) = sgn\Big(\int_{-\infty}^{\infty} V_i(\tau)\ \Gamma(\tau) d\tau\Big) \tag{4.4}$$

Because of the effectiveness and efficiency, ISFs are the dominant way to characterize latches, and different methodologies have been developed to obtain them [60][61][62]. Based on the definition of ISF, T. Toifl et al. [61] proposed to simulate the ISF directly by sweeping different time offsets and carefully searching the corresponding pulse amplitude for each specific time offset (which are detailed in Appendix A). The searching of the pulse amplitude for a certain time

offset either consumes a lot of simulation time or requires smart searching algorithms, which limits the use of this methodology. Furthermore, simulating the effects of tiny impulses on large-signal waveforms is likely to suffer from numerical inaccuracies. To solve this problem, different methods have been proposed. For instance, researchers in [62] utilized the efficient periodic AC simulation and the periodic time-varying analysis to characterize the ISF. A more practical methodology was proposed in [60] and are detailed in Appendix A. A small step signal is applied to the comparator at time offset τ compared to the rising edge of the sample clock with a small offset voltage, $V_{ms}(\tau)$. Compared to previous methodologies, the main difference is that the metastable point is found statistically by counting the occurrences of the output bit being 0 or 1 over multiple measurements. Following the same simulation setups in [60], we have the following simulation results for the SAFF-based digital sampler as shown in Figure 27 and Figure 28.

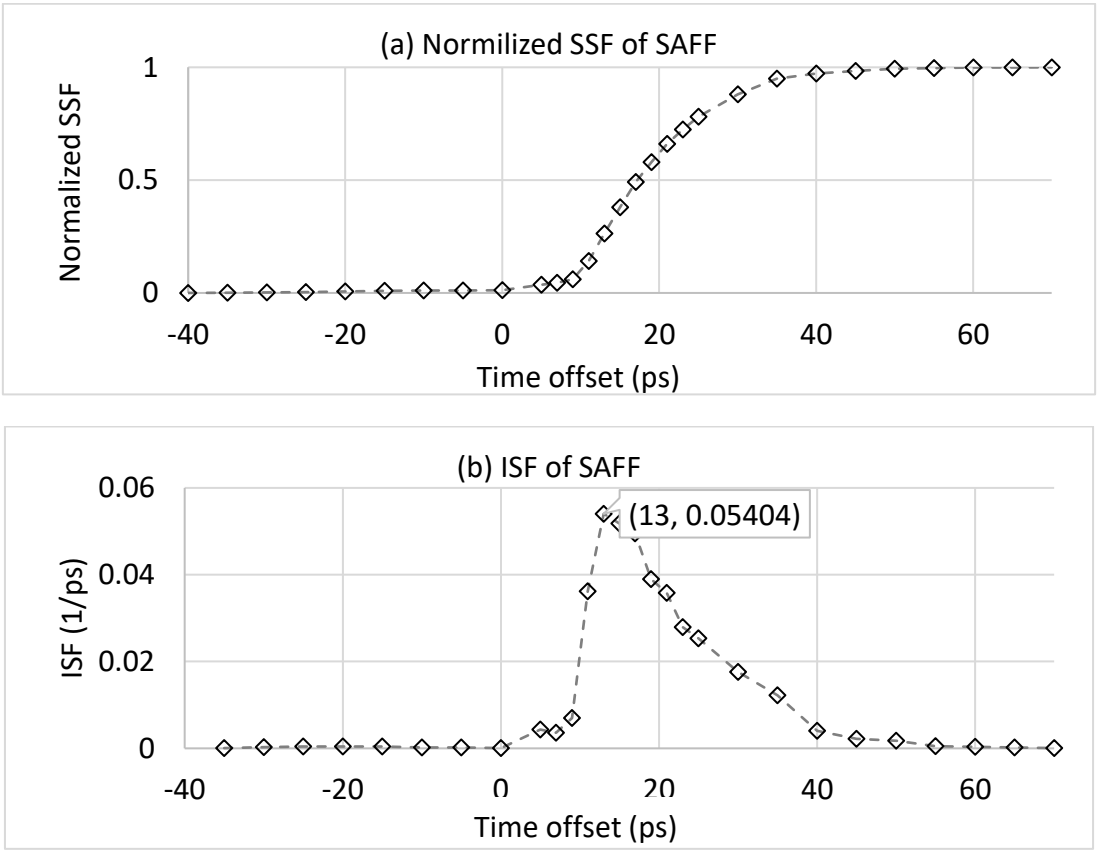


Figure 27: ISF simulations of SAFF. (a). Normalized Step Sensitivity Function (SSF) for time offset τ between -40ps to 70ps. (b). ISF derived from the normalized SSF.

Similarly, we can obtain the ISF of the CML as shown in Figure 28.

By comparing Figure 27 and Figure 28, we can have the following observations:

1) The sampling gain of the CML sampler is 18.6 dB (= 20*log(0.06662/ 0.06094)) higher than the gain of the sense amplifier based sampler.
2) By defining the sampling aperture time as the width that contains 80% of sensitivity, we can obtain the sampling apertures of SAFF and CML to be 24 ps and 18 ps, respectively. This means the CML has a smaller sampling aperture, or a higher sampling time resolution, by 6 ps.

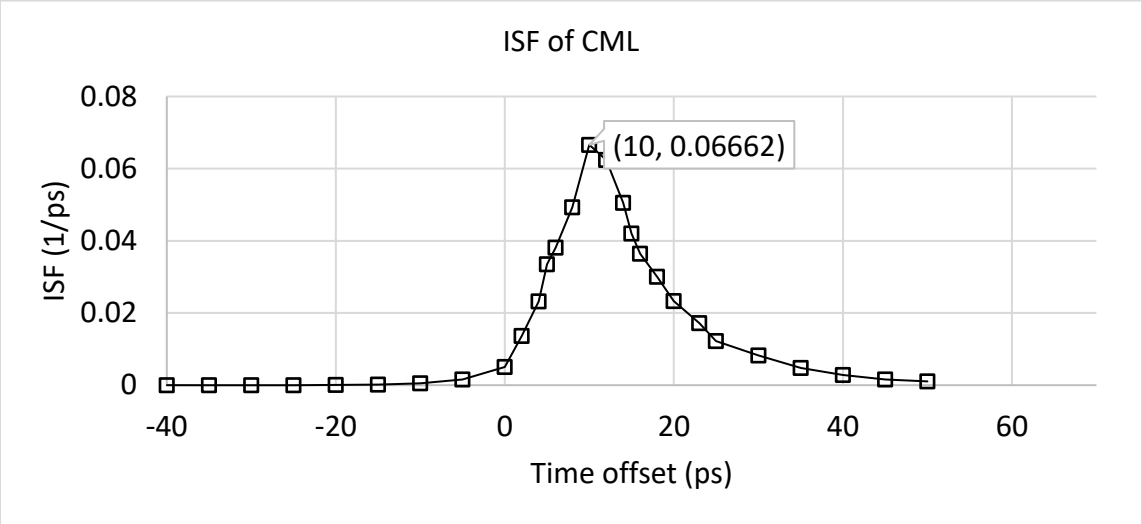


Figure 28: ISF of CML.

4.2. Sampling Probabilities and Sampling Errors

As discussed above, ISF can be used to characterize the performance of digital sampler functioning as a latch, a clocked comparator or a regenerative amplifier. Under these scenarios, an ISF may be useful for predicting the sampled output for either a regular or irregular input at the latching speed, but it does not capture effects of device noise, which is a key limitation of subsampling to recover phase information for high-frequency recurring signals, as we intend to use it. For high-frequency applications, such as an aliasing divider inside a PLL where the input is a largely periodic input like a VCO or a narrow-band received signal, the input is at a much higher frequency and the output is determined by multiple periods of input signal within the

sampling aperture, which makes the scenario more complicated than a single step function or an impulse function for a clocked comparator. Under these scenarios, we want to know how device noise affects the accuracy of the sampled signal, and therefore we propose the sampling probability function (SPF).

For a digital sampler, when applied as a down-conversion mixer, the output is determined by both the input signal within the sampling aperture (characterized by the ISF) and the noise. For an input signal with a certain frequency, if we change the phase offset of the input signal compared to the rising edge of the sampling clock, the digital output will be different because of the different input phases within the sampling aperture. More importantly, when the impact of noise is present, the output frequency of occurrence of 1's and 0's will be probabilistic. We name this the sampling probability function (SPF), which characterizes the impact combination of both the digital sampler ISF and the noise as the phase offset of the input signal changes for a certain input frequency.

To obtain the SPF of a digital sampler, we have developed the following simulation procedure:

- Assume a sinusoid wave with a frequency f_x is the input signal of the digital sampler. Sweep f_x for the below simulations to measure performance at discrete operating frequencies.
    - Run simulations by sweeping φ from -180 degree to +180 degree. Here we assume the phase offset of the zero-crossing is φ away from the rising edge of the sample clock.
        - For each φ, run the simulations for two clock cycles and repeat for multiple times (for instance, *N* times):
            - In the first cycle of the sample clock, reset the digital sampler output to be zero.
            - In the second cycle of the sample clock, apply the high-frequency sine wave with a frequency f_x as the input signal of the digital sampler and monitor the digital output being 1 or 0 when stable.
        - Post processing: For the above φ, calculate the probability, P(φ), of

output occurrence being 1's within the *N* times simulations.

- Post processing: At frequency f_x, the probability P(φ) can be obtained as a function of the phase offset φ for each φ between ± 180 degree. Then we can obtain the SPF vs. phase offset at frequency f_x.
- Post processing: Calculate the time delay τ corresponding to each φ by using the following equation $\tau = \frac{1}{f_x} \cdot \frac{\varphi}{360^\circ}$. With the probabilities from (b), we can obtain the SPF vs. time offset at frequency f_x.

- Post processing: For each f_x, shift the phase offset by calling phase at which the 50% sampling probability occurs the zero phase offset or zero timing offset. Then the relationship of how SPF changes as phase offset and time offset changes for multiple f_x can be obtained.

Figure 29: Pseudo code of sampling probability simulations for different input signal frequencies.

Following the above pseudo code in Figure 29, we can simulate and calculate the sampling probabilities of the SAFF-based sampler and the CML-based sampler. Both the SAFF-based sampler and the CML-based samplers are designed in TSMC 40 nm ULP bulk CMOS process with normal threshold transistors and a VDD of 1 V. The sampling clock is a rail-to-rail digital pulse clock with a 1 GHz frequency and 10 ps rising/falling trapezoidal edge, and input signal is a differential sinusoid wave with each signal of the pair having an AC amplitude of ±200 mV at a DC voltage of 0.6 V.

Because each simulation event only produces a "1" or "0", multiple simulation runs are needed to measure the sampling probabilities. Choosing the number of runs *N*, requires considerations of both simulation complexity and result accuracy. On one side, the accuracy of sampling probability is proportional to $\frac{1}{\sqrt{N}}$, and a higher accuracy requires a larger *N*. On the other side, simulation complexity, i.e., simulation time, increases proportionally as the number of runs increases. Figure 30 shows how sampling probability changes as *N* increases for a certain phase offset of -84.4 degree (or equivalent to a relative phase offset of 0.03 degree in Figure 31) for a 10 GHz input frequency. Firstly, starting from *N*=50, 10 sets of runs have been simulated with each set consisting of *N* simulations. Specifically, the same random seed is used within each set

of simulations, while different random seeds are used for different sets of simulations. With the calculated sampling probabilities, statistics analysis shows the mean value, μ, is 0.55, and the standard deviation, σ, is 8.30%. Then we change the number of runs *N* and expect to see that as *N* increases, the standard deviation, σ, changes proportionally to $\frac{1}{\sqrt{N}}$. Four more groups of simulations have been proceeded with *N* increasing from 100, 200, 500 to 1000, and results are summarized in Figure 30. From Figure 30, the sampling probability converges as number of runs increases from 50, 100, 200, 500 to 1000. For *N*=1000, the statistic standard deviation is 0.34%, which is acceptable in terms of accuracy while also takes affordable simulation time. Therefore, *N* is set to be 1000 in later simulations if not otherwise mentioned.

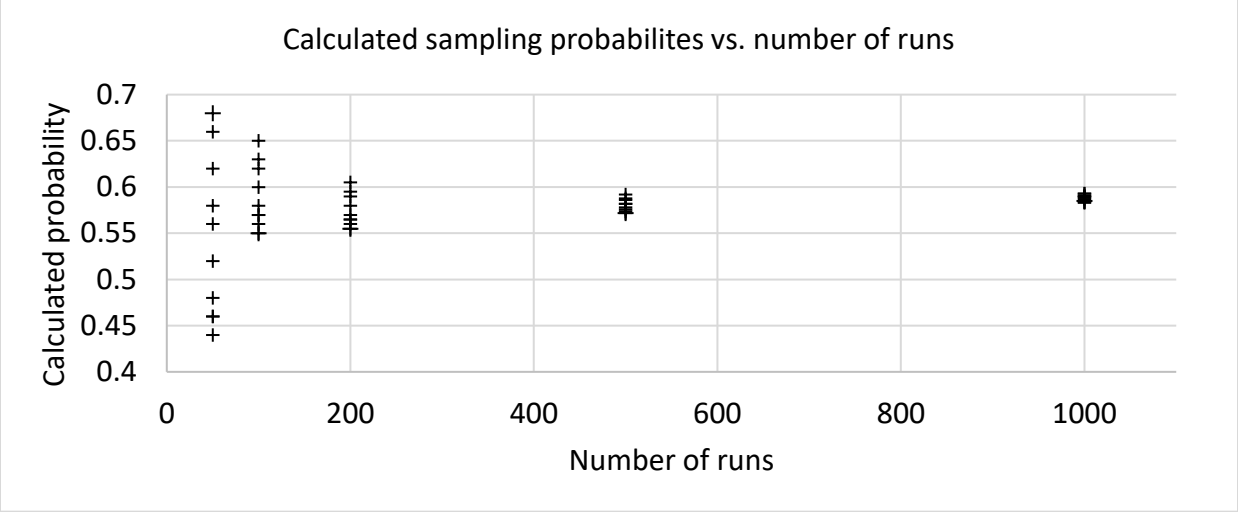


Figure 30: Sampling probability converges as number of runs increases from 50, 100, 200, 500 to 1000. For each number of runs, 10 sets of runs have been simulated and the mean value μ and standard deviation σ are therefore calculated. For N=50, μ=0.55, standard deviation σ=8.30%; For N=100, μ=0.59, σ=3.34%; For N=200, μ=0.57, σ=1.67%; For N=500, μ=0.58, σ=1.66%; For N=1,000, μ=0.59, σ=0.34%.

We first use a VCO frequency of 10 GHz ($f_x = 10\,\mathrm{GHz}$) as an example to illustrate the relationship. Following the simulation procedures as described in Figure 29, we have obtained the relationship between the sampling probabilities and the relative phase offsets as shown in Figure 31 (a). As the relative phase offset increases from -3 degree to +3 degree, the weighted average of the signal amplitude falling into the sampling aperture increases, and therefore the sampling probability increases from 0 to 1. By calculating the finite difference of the sampling probabilities, we have obtained the relationship between the probability density and the relative

phase offset, as shown in Figure 31 (b). The probability density function fits well to a Gaussian distribution with a mean value of 0 degree ($\mu = 0$) and a standard deviation of 0.79 degree ($\sigma = 0.79$). Since the probability within [-σ, +σ] is 65.3% for a Gaussian distribution, here we can use the standard deviation σ of the fitted curve to characterize the average phase error produced by device noise, thus we name σ to be the sampling phase error. A small sampling phase error means only a small phase offset can lead to the same [-σ, +σ] interval, which further means the sampling probability changes more steeply as phase offset changes. Therefore, the sampling phase error can be used to characterize the sampling accuracy.

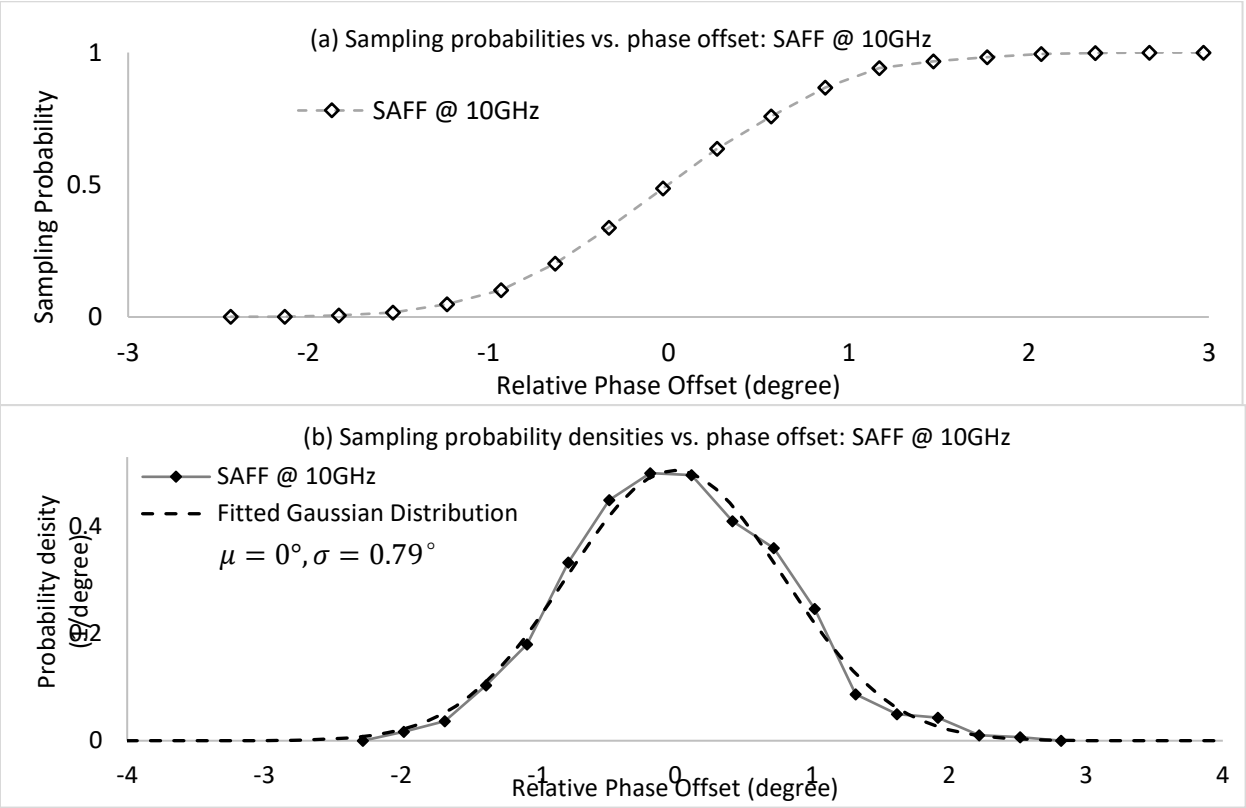


Figure 31: Sampling probabilities of SAFF-based digital sampler for a 10GHz input signal. (a) Sampling probabilities vs. relative phase offset. (b) Sampling probability densities vs. relative phase offset, and the fitted Gaussian distribution where $\mu = 0$ degree, $\sigma = 0.79$ degree.

The relationship between the sampling probability and the relative phase offset characterizes how the sampling probability changes with phase. The phase offset, however, is frequency dependent in terms of absolute time delay. To characterize how the sampling probability changes with absolute time offset, with the same group of simulation data we can further obtain the

relationship by converting phase offset to time offset at the 10 GHz frequency. By calculating the finite difference of the sampling probabilities, we can obtain the relationship between the probability density and the time offset, as shown in Figure 32 (b). The probability density function fits to be a Gaussian distribution with a mean value μ of 0 ps and standard deviation σ of 0.2175 ps. Similarly as the above definition of sampling phase error, here we define the standard deviation σ of the fitted curve to be the *sampling time error*, which characterizes the probability density distribution of sampling errors. A small sampling time error σ means only a small time offset can lead to the same 65.3% probability, which further means the sampling probability changes more steeply as time offset changes.

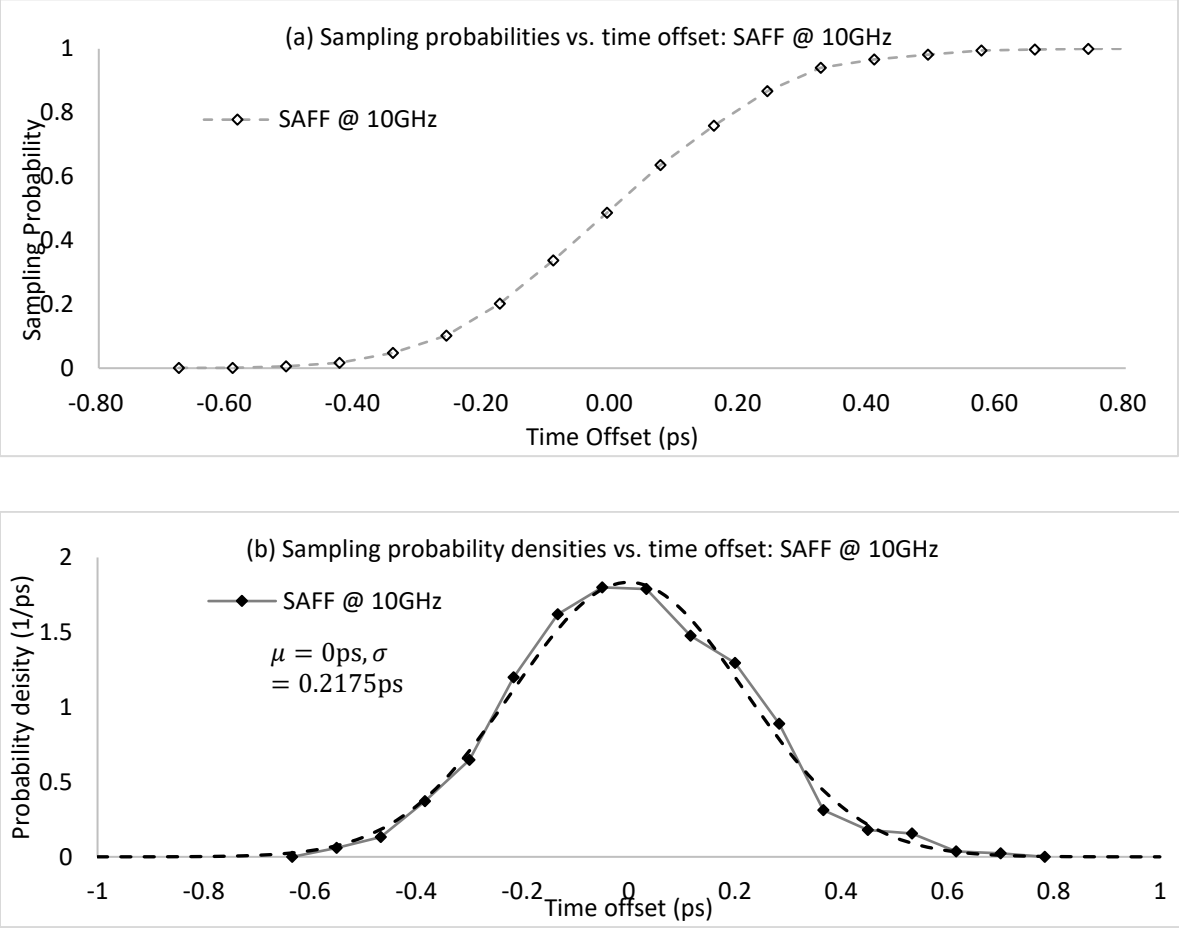


Figure 32: Sampling probabilities of SAFF-based digital sampler for a 10GHz input signal. (a). Sampling probabilities vs. time offset. (b). Sampling probability densities vs. time offset, and the fitted Gaussian distribution where $\boldsymbol{\mu = 0ps}$, $\boldsymbol{\sigma = 0.2175ps}$.

As we vary the VCO frequency through 10GHz, 30GHz, 50GHz, 70GHz, 90GHz and 110GHz, we obtain the sampling probabilities vs. phase as shown in Figure 33.

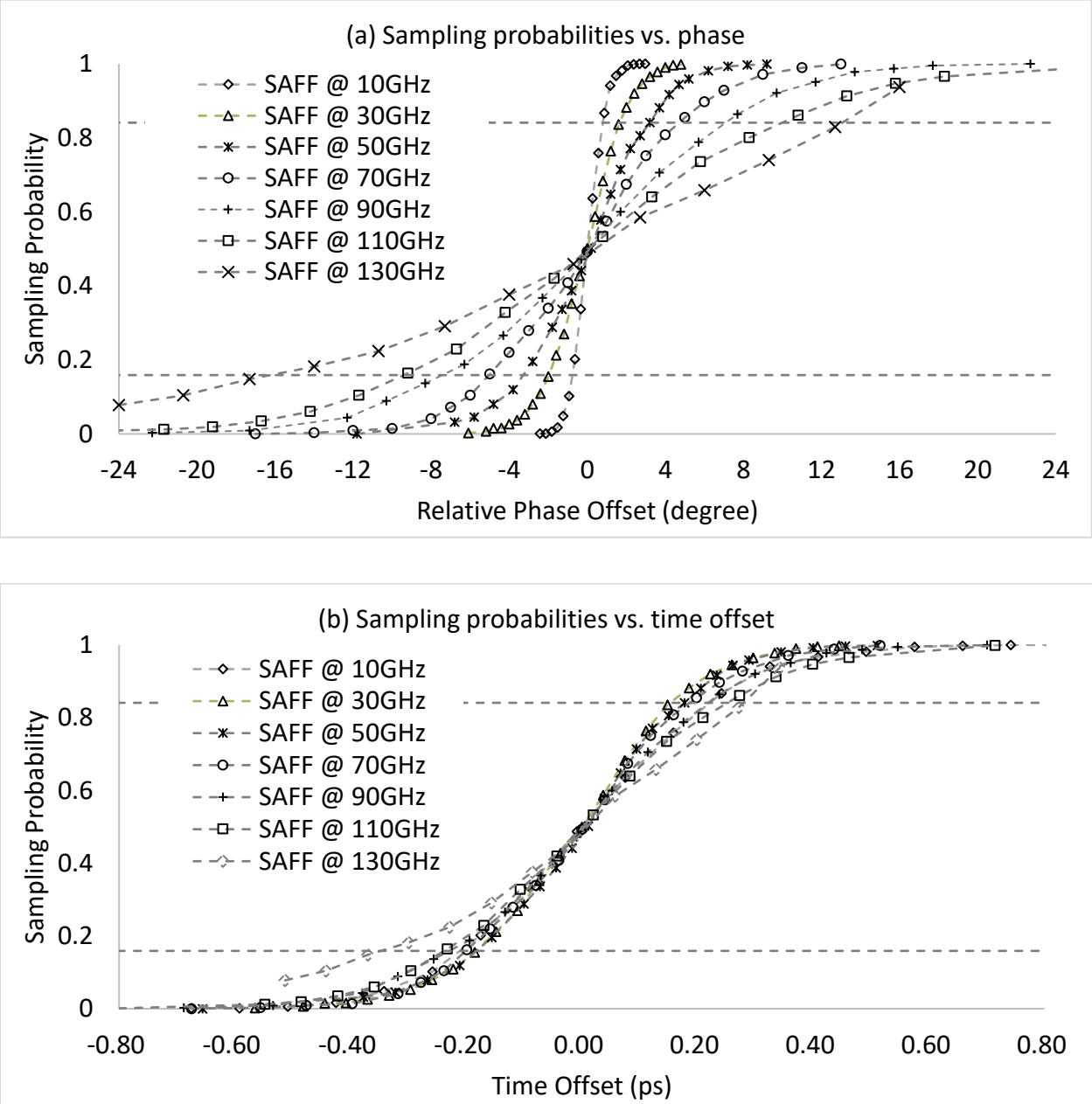
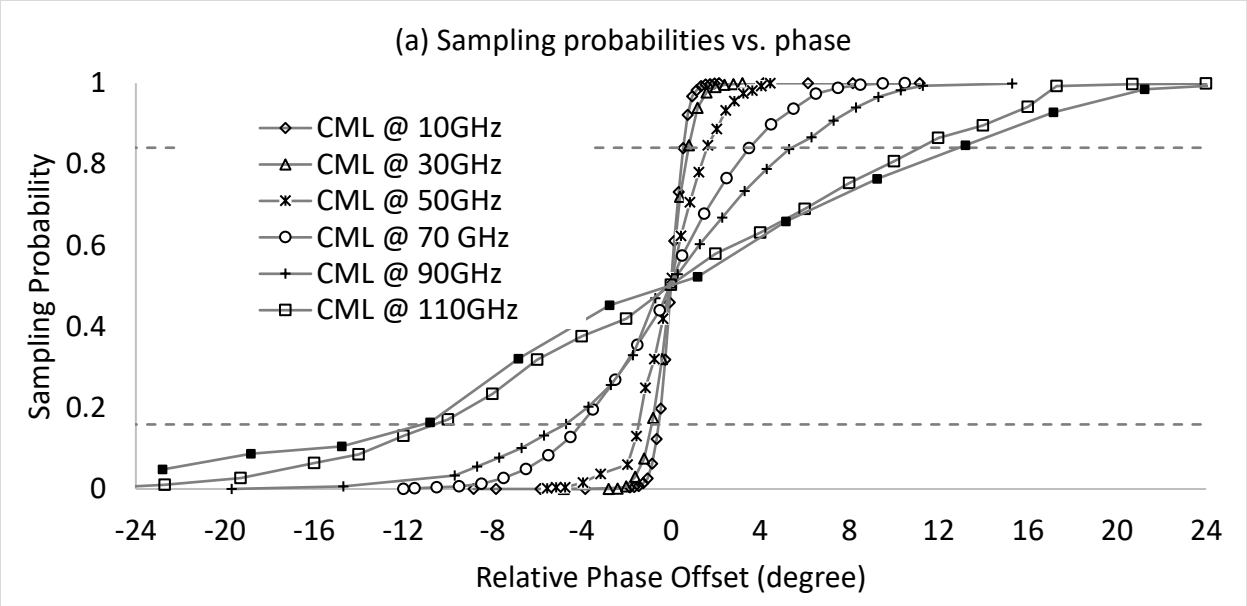


Figure 33: Sampling probabilities of SAFF-based digital sampler for input signals with different frequencies. (a) Sampling probabilities vs. phase offset. (b) Sampling probabilities vs. time offset.

Similarly, we can obtain the relationship between the sampling probabilities and the phase/time offset for a CML-based digital sampler as shown in Figure 34.



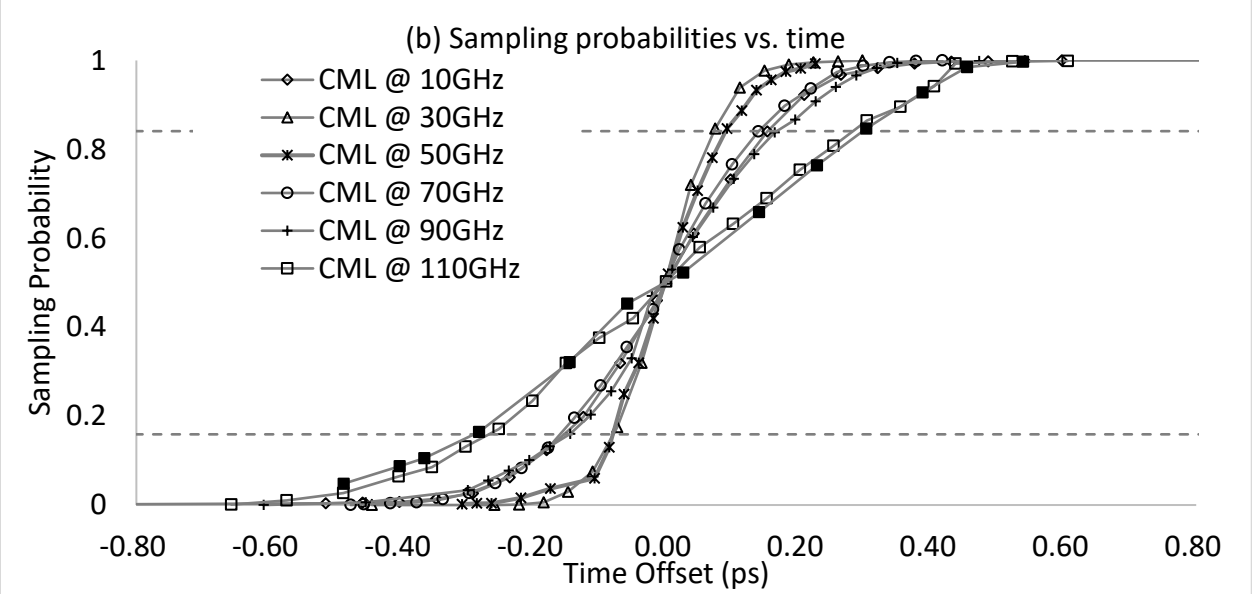
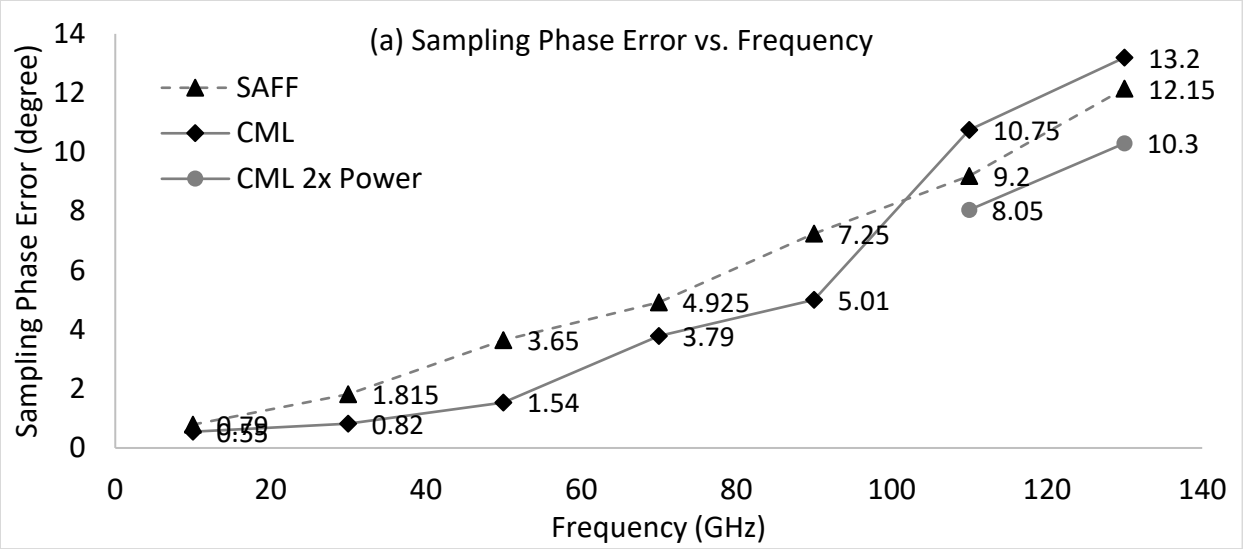


Figure 34: Sampling probabilities of CML-based digital sampler for input signals with different frequencies. (a). Sampling probabilities vs. phase offset. (b). Sampling probabilities vs. time offset.

Similar as shown in Figure 33 (b) and Figure 34 (b), the sampling phase errors and sampling time errors can also be calculated for both the SAFF-based digital sampler and CML-based digital sampler at all frequencies from 10 GHz to 110 GHz, as shown in Figure 35.



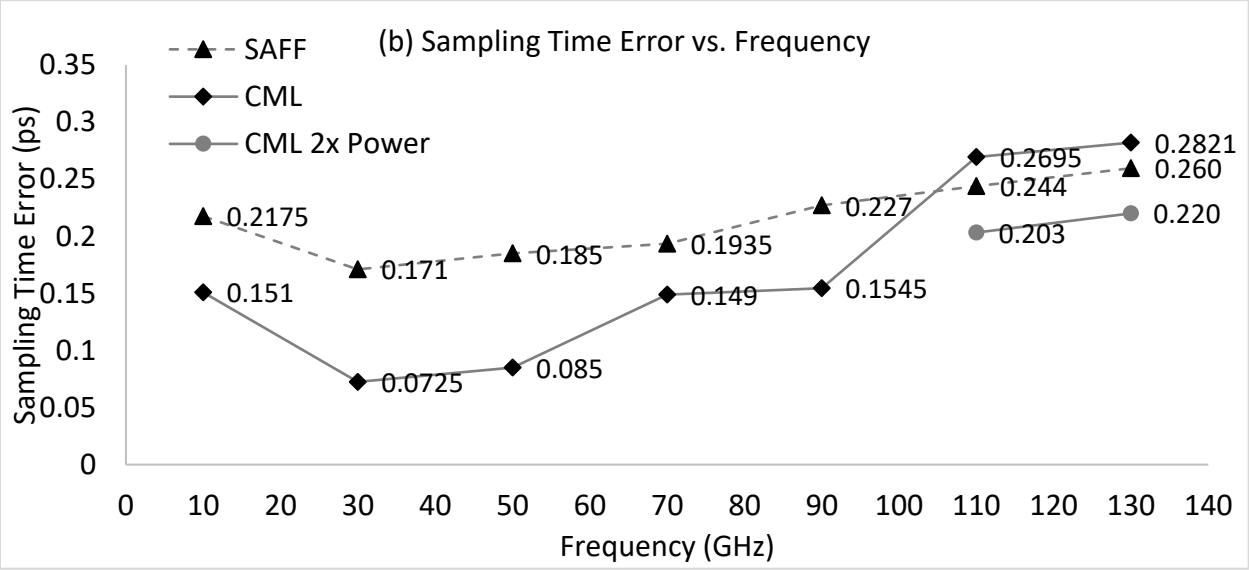


Figure 35: Sampling phase/time errors vs. frequencies for both SAFF-based digital sampler and CML-based digital sampler (a). Sampling phase errors vs. frequencies. (b). Sampling time errors vs. frequencies. Noticing that a new CML circuit architecture, denoted as "CML 2x power", which is implemented with two times of transistor sizes (and thus two times of power) and half of load resistance of the original CML, has been simulated for 110 GHz and 130 GHz and demonstrated smaller sampling phase/time errors.

From Figure 35, it can be observed that:

a) For both the CML-based digital sampler and the SAFF-based digital sampler, as the frequency of the sampled input increases, a greater range of input voltages are averaged into

the same sampling aperture (as characterized by its ISF) for the same input phase offset. Therefore, the slope of the sampling probability function will be reduced and the sampling errors will monotonically increase as input signal frequency increases.

b) Based on discussions in Chapter 3, the output of the digital sampler will be determined by both the input signal and the circuit noise. The slew rates of input signals are low at lower frequencies (such as around or below 10GHz), and the signal changes little within the sampling aperture (i.e., sampling apertures of SAFF and CML are 24 ps and 18 ps from Section 4.1, respectively) at these frequencies for both the two types of digital sampler circuits. Therefore, the digital sampler output will be dominated by circuit noise which could be modeled as additive noise at the input or input-referred noise.

c) It can be observed in Figure 35 that there is a local minimum at around 30 GHz. As frequency increases from 10 GHz to around 30 GHz, the slew rate will also be increased and the signal amplitude within the sampling aperture becomes larger, which therefore mitigates the sampling time errors. As the frequency further increases to 50 GHz or even higher, more of a cycle or more than one cycle fit in the sampling aperture, reducing the net signal, thus increasing the influence of circuit noise.

d) For frequencies below 110 GHz, a CML-based digital sampler achieves smaller sampling errors (both sampling phase errors and sampling time errors) than an SAFF-based digital sampler. It can be observed that the CML-based sampler has a higher gain compared to the SAFF-based sampler according to the previous ISF analysis in Figure 27 and Figure 28, and this has resulted in the smaller sampling errors for the CML-based sampler. For frequencies at 110 GHz or higher, the sampling errors of the CML-based digital sampler are larger than the SAFF-based digital sampler, which is due to the limited bandwidth of the CML circuit design, i.e., designed load resistance and parasitic capacitance and the input-referred noise. By reducing the load resistance while increasing the CML biasing current, designers can reduce the transistor noise and therefore mitigate the sampling errors at higher frequencies. For instance, Figure 35 also shows the sampling phase/time errors for a CML circuit architecture with two times of transistor sizes (and thus two times of power) and half of load resistance (denoted as “CML 2x power” in Figure 35). It can be observed that for a 130 GHz signal, the sampling phase (time) error has been reduced from 13.2 degree (0.2821 ps) in the original CML circuit architecture to 10.3 degree (0.220 ps) in “CML 2x power”. More

importantly, simulation has shown that the sampling phase error and sampling time error of "CML 2x power" are smaller than the sampling error of the SAFF circuit architecture, which shows more design flexibility in a CML circuit architecture.

Based on the above analysis, a CML-based digital sampler is a better candidate in high-frequency applications such as inside a high-frequency PLL.

4.3. Summary

Digital samplers are usually characterized by setup and hold times together with the latch delay when using in digital applications such as latches and sense amplifiers. Impulse sensitivity function (ISF) is the dominant tool to characterize the performance of a digital sampler in these applications. Under these scenarios, an ISF may be useful for predicting the sampled output for either a regular or irregular input at the latching speed, but it does not capture effects of device noise, which is a key limitation of subsampling to recover phase information for high-frequency recurring signals.

For high-frequency applications, such as an aliasing divider inside a PLL where the input is a largely periodic input like a VCO, we have proposed the sampling probability function (SPF) to characterize the performance the digital sampler in the presence of circuit noise. Simulation has shown that a digital sampler, no matter implemented by a sense amplifier or a CML, can greatly extend the operating frequency when compared to static digital dividers implemented with the same circuit architecture. For instance, in simulation using the TSMC 40 nm Bulk CMOS process, when this sense amplifier is applied as a digital sampler, it can successfully subsample a 130 GHz input with an error of 12.15 degree or 0.260 ps. When this same CMOS sense amplifier is connected as a static divider, however, it fails before reaching 20 GHz.

Simulation has also shown that a CML-based digital sampler can perform a steeper SPF and smaller sampling errors than a SAFF-based digital sampler for as high as 90 GHz, which means a CML-based digital sampler is a better candidate when used as an aliasing divider. Simulation has also shown that the operation range of CML-based digital sampler can be extended to as high as 130GHz by increasing the CML bias current and therefore reduce the circuit noise.

CHAPTER 5. Coresidual Alias-Locked Loop

An alias-locked loop (ALL) is similar to a phase-locked loop but uses digital sampling to produce a lower frequency alias signal from the VCO output. This digital aliased signal, when in lock, is a recurring sequence of 1's and 0's at an average frequency of the reference clock. The lack of alignment of this bitstream to the reference clock can produce a pattern of phase lead and lag indication by the phase frequency detector (PFD), which in turn produce spurs on the VCO output. A coresidual alias-locked loop (C-ALL) is a circuit architecture to reduce spurs in the voltage-controlled oscillator (VCO) output of an ALL by predicting the expected pattern of 1's and 0's and providing this signal to the PFD. The expected pattern is generated in the digital domain as the reference signal to the PFD, therefore a C-ALL implements a coresidual function. Spectre post-layout simulations have verified that the proposed design can not only achieve lock and synthesize the targeting frequency but also reduce synthesizer output frequency spurs by 27.7 dB.

5.1. Introduction

Phase-Locked Loops (PLLs) play an increasingly important role in modern electronic systems. With the rapid advancements in high-frequency communications in recent years, synthesizers working at radio frequency and millimeter wave range have become more important and many approaches have been taken to solve the challenge of measuring the VCO output, typically done with a divider. A 0.56 THz CMOS PLL with two stages of injection locking frequency dividers (ILFDs) has already been demonstrated [64]. In a classic integer-N PLL-based frequency synthesizer [65], the frequency resolution is determined by the reference frequency, which therefore results in a large division ratio requiring a narrower loop bandwidth and the close-in phase-noise is dominated by the charge pump and phase detector. To solve this problem, researchers proposed the so-called fractional-N PLL. Typically, a ΣΔ modulator is applied to shape the quantization noise to high frequency, and then the shaped noise is low-pass filtered by the loop [66][67]. Additionally, novel techniques based on phase interpolator [68], phase-domain

---

This Chapter is based on a conference paper presented at ISCAS 2016 [63].

averaging [69], and mixer in the feedback path [70] were all proposed to suppress the phase noise. In [70], a PLL with very fast settling, high-frequency resolution and spectral purity is achieved by using a mixer in the feedback path, where the VCO frequency is down-converted with an external direct digital frequency synthesis (DDFS) signal. With a single-sideband (SSB) mixer and a second PLL providing the carrier signal for the mixer, a dual-loop synthesizer circuit architecture is proposed in [71][72][73]. The VCO signal is first down-converted by the mixer and fed into the divider chains, and then fed into the phase detector. Since the division ratio in the published dual-loop architecture is greatly reduced compared to a conventional PLL, the phase noise contributed from phase detector and charge pump is greatly reduced. Due to the requirement of the SSB mixer, however, both loops should provide similarly high frequencies. Since an analog sampler inherently is a down-conversion mixer, an analog sample-and-hold circuit is used to replace the SSB mixer in the feedback path [45][47]. A low-pass filter is further applied to restore the down-converted signal. The phase noise performance of the loop is directly impacted by the order of the filter. Furthermore, DDFS is usually used to generate variable reference frequencies instead of a fixed reference clock. Both the filter and DDFS increase the cost of these architectures.

A subsampling PLL (SSPLL) has the advantage (similar to an ALL as discussed later in Section 5.4) of not multiplying the power of PFD and charge pump phase noise by N^2 (where N is the ratio of the targeting VCO frequency and the reference frequency) [74]. In [37], an SSPLL has been demonstrated to synthesize a VCO output up to 104.8GHz using a cascaded PLL circuit architecture, where a fractional-N PLL is applied to increase the sampling clock frequency to ~2.75 GHz first. Other researchers, however, prefer to divide a mm-wave VCO frequency before the subsampling phase detector (SSPD) instead of direct subsampling. In [38], J. Kim et al. suggest that direct subsampling is not suitable for mm-wave frequency synthesizing due to the limited capture range of the sampling operation. For instance, a 28.0-31.0 GHz frequency was synthesized in [38] using injection locked frequency multiplication with a 3.3-4.3 GHz frequency generated by an SSPLL. In another example, a 60 GHz SSPLL was built with an inductively-peaked static divider and a SSPD running at 30 GHz [39]. Usually researchers don't use direct subsampling to synthesize frequencies much over 30 GHz [40][41][42][75][76].

In order to develop architectures suitable for high-speed frequency synthesis, a new type of

circuit architecture, named an Alias-Locked Loop is proposed in [15] (further described in Section 5.2). A digital (regenerative) latch can amplify a small input signal, and its fundamental speed limit is the sampling clock frequency, allowing the f_{VCO} to be much higher in an ALL. For instance, sense-amplifier latch in TSMC 40nm bulk CMOS process can operate effectively beyond 130 GHz as a digital sampler in an ALL, while the same circuit cannot operate beyond 20 GHz as a divider. In this paper, we'll evaluate the performance of an ALL, and propose an improved architecture we've named a Coresidual Alias-Locked Loop (C-ALL).

This Chapter is organized as follows. Review of ALLs is first provided in Section 5.2. Based on review and discussions of an ALL, a C-ALL is proposed as an improved architecture in Section 5.3. To analyze the phase noise performance, phase domain models for an ALL and a C-ALL are both created respectively in Section 5.4. Discussions are provided in Section 5.5. Design and simulation results are included in Section 5.6. Section 5.7 goes to the conclusion.

5.2. Review of Alias-Locked Loops

In the ALL architecture, a digital sampler, which could be implemented with a regenerative latch (one with positive feedback) [77] is used as an aliasing divider to replace the traditional divider. A stable reference clock, which is usually with significantly lower frequency than the VCO signal, is applied in the digital sampler to sample the VCO signal. The VCO signal will be subsampled, therefore creating an alias frequency. As the latch is clocked by the slower reference clock and not the VCO output, it can support higher VCO frequencies than a traditional digital divider. It should be mentioned that although the regenerative latch has arbitrarily high gain, it is limited by input referred noise. The ALL is tolerant of latch input offset error, so long as high and low are sensed and the output changes [78]. High speed sense-amp latches or current-mode logic (CML) latches are well suited to this application. As discussed in [15][16], the sampling latch in a digital sampler makes a sampling "decision" at the sample clock rate. This is different from a divider, since a divider is clocked at the VCO rate and it is, by design, usually much higher than the sample clock rate. This advantage allows the sampling latch to operate at a much higher frequency than in a divider. The generated alias signal, whose frequency is significantly lower than the VCO signal, can be fed into a CMOS static divider, or be fed directly to a PFD.

As illustrated in Figure 36, components within an ALL are mostly the same as or similar to in a

traditional PLL. A PFD is applied to compare the phase (frequency) of the reference clock with the feedback signal and generate a control signal for a charge pump accordingly. By converting the phase to current and controlling the charging and discharging the capacitor within the loop filter, the charge pump thereby tunes the VCO frequency. The difference from a conventional PLL, however, is the sampler creating a lower alias frequency of the VCO replacing the higher frequency stages (or all stages) of the divider in a PLL. An optional programmable divider can be added to the ALL for further division of the alias signal as in a conventional PLL for finer frequency control.

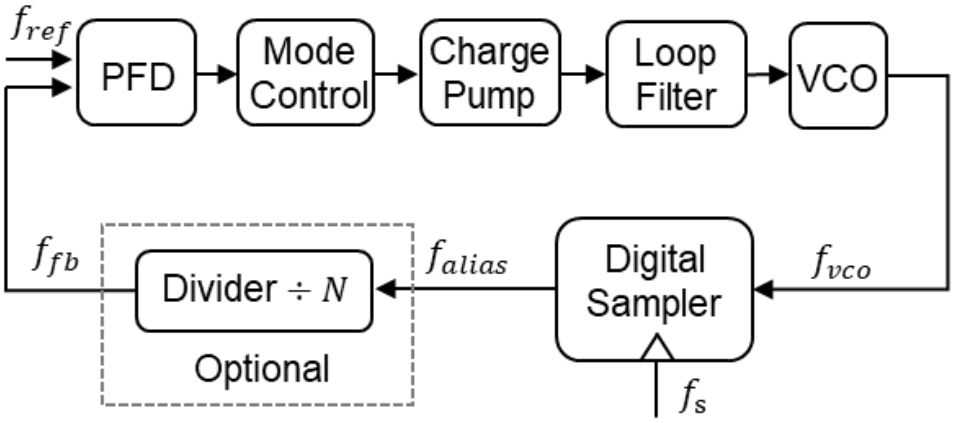


Figure 36: An Alias-Locked Loop (ALL) architecture [16]. The divider is optional and the division ratio is assumed to be 1 in further mathematical calculation unless otherwise specified. Noting that $f_{vco} = Kf_s + f_{alias}$, where K is the subsampling ratio which will be defined in Section 5.4. As illustrated in Figure 39, a digital sampler senses the analog inputs and digitizes the output to be 1's or 0's.

Since a change of the VCO frequency can lead to a change in sign of the alias frequency, the loop can change from negative feedback mode to positive feedback mode, therefore making the loop unstable. To ensure negative feedback in the loop over the whole range of the targeting frequencies, a mode-control module, which can be implemented by multiplexers, inverts the sense of the PFD output as needed [16]. Nonlinear dynamics of an ALL was also analyzed based on numerical investigations to examine the lock-in behavior [79]. The alias frequency is the difference of the VCO frequency and the integer multiple of the sampling clock frequency, and thus one alias frequency could map to multiple VCO frequencies. To solve this disambiguation, one can either initialize the loop filter with a digital-to-analog converter (DAC) to directly bring the VCO to the targeting frequency range, or using two different sampling frequencies to

generate the corresponding alias frequencies, and therefore the VCO frequency is uniquely determined [80].

5.3. Coresidual Alias-Locked Loops

5.3.1. Limitations of a conventional ALL

Based on the observation that the alias signal frequency is always lower than a half of the sampling clock, DDFS or frequency dividers controlled by the sampling clock can be used as the reference signal in an ALL. The feedback signal, as can be observed in Figure 38 (a)-(b), in most cases is not single-tone periodic, and therefore results in periodic spurs. Figure 38 (a) shows an example of a 300 MHz alias signal sampled from a 1 GHz sampling clock. When this 300 MHz alias signal and a 300 MHz square wave reference clock (Figure 38 (b)) are both fed into a PFD, short pulses will be generated in every 10 ns and eventually result in spurs even when the loop is locked. Spectrum of the ALL in Figure 48 (a) has shown the spurs when in lock.

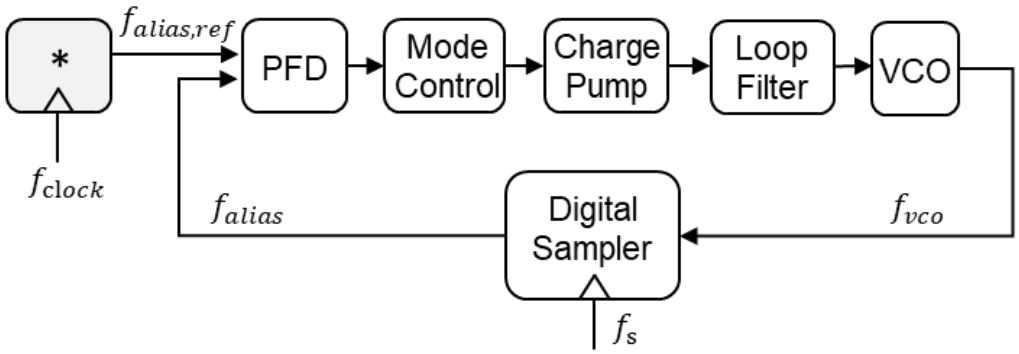


Figure 37: Block diagram of the architecture with the reference alias signal generated by a "*" block, which we develop as the "alias-generator" in Figure 41.

To address this problem, designers can either filter out or eliminate these spurs. ΔΣ modulators have been introduced in fractional-N PLLs to shape the quantization noise, which will be low-pass filtered by the loop. ΔΣ modulators, however, cannot be directly applied in ALLs. Therefore, a different technique is required.

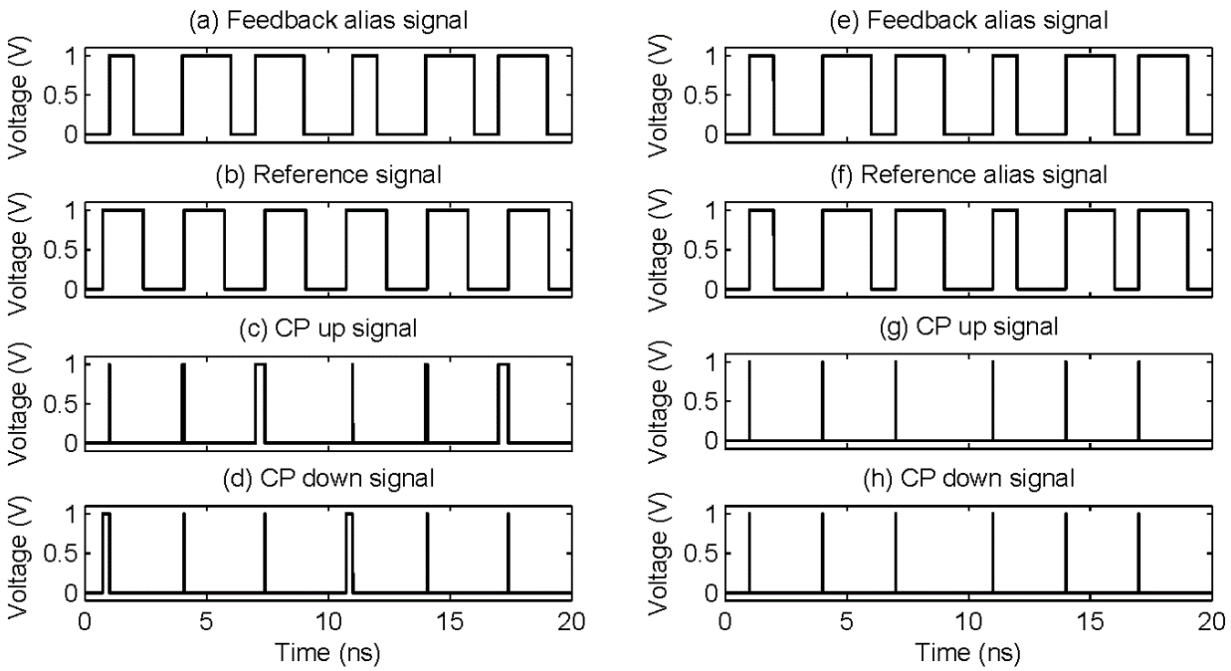


Figure 38: Charge pump output comparisons of a conventional ALL and the proposed C-ALL when in lock. As illustrated in (a)~(d), short pulses will be generated for the charge pump (CP) in every 10 ns by the PFD even when the loop is locked in an ALL. These pulses eventually result in spurs in the ALL output spectrum. In these simulations, the C-ALL has eliminated the erratic pulse width changes in the CP up and CP down signals as illustrated in (e)~(h) that are responsible for the spurs [63]. The output spectrums for both circuit architecture approaches are shown in Figure 48.

5.3.2. Coresidual Alias-Locked Loops

5.3.2.1. Eliminating frequency spurs by changing the reference signals

A method of solving this problem uses a different reference signal. Assuming a VCO signal with a targeting frequency of f_{VCO} is to be synthesized by an ALL. For a sampling frequency f_s, the alias frequency would be f_{alias}. Instead of using a single tone frequency reference signal f_{ref} in a conventional ALL, as illustrated in Figure 37, assume another signal $f_{alias,ref}$ which is identical to the feedback alias signal f_{alias} is available as the reference (as shown in Figure 38 (f)), then the two signals feeding into the PFD will synchronize in both frequency and phase when the loop achieves lock. Therefore, the frequency spurs in a conventional ALL will be eliminated in the newly proposed architecture. In the following sections, we are going to discuss how to generate the reference signal $f_{alias,ref}$.

5.3.2.2. Reference signal generations

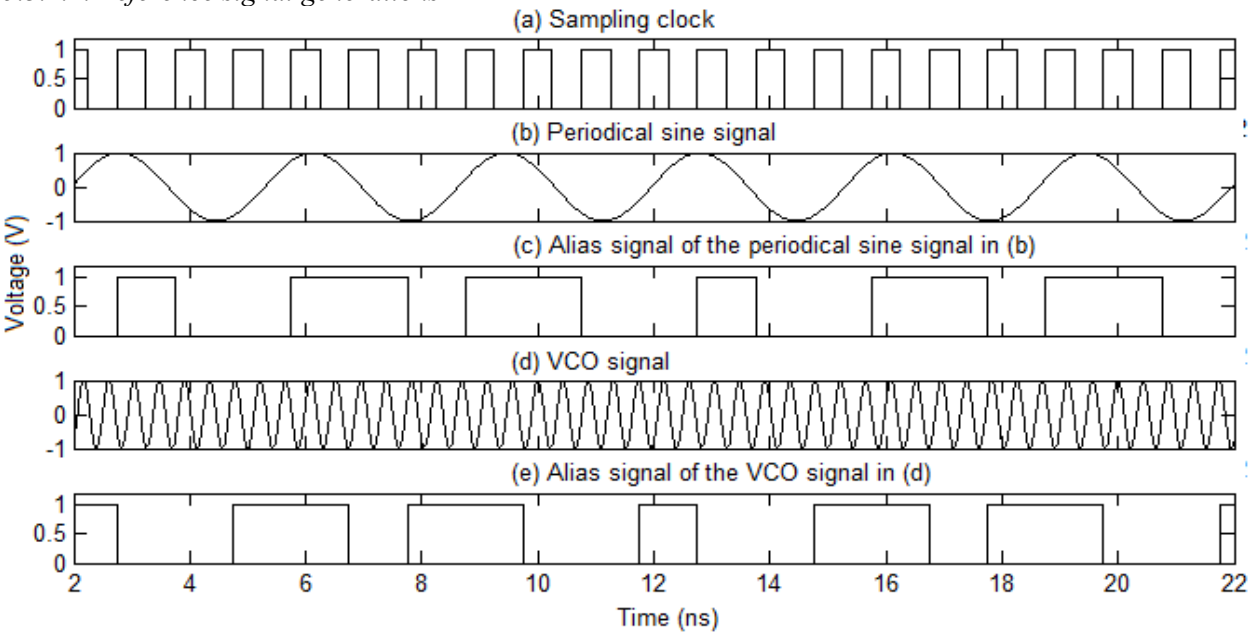


Figure 39: For signals whose frequencies can be represented by $Kf_s + f_{alias}$, the alias signals are the same sequence of bits for different K if sampled by the same sampling frequency f_s. (a). The sampling clock with a sampling frequency f_s. Sampling occurs at the rising edge of the sampling clock. (b). Sine wave with a frequency of f_{alias} ('K=0' for '$Kf_s + f_{alias}$') for illustration purpose (does not exist in circuit). (c). Alias signal of sine wave in (b) generated digitally in circuit from a sampling clock in (a). (d). Sine wave with a frequency of $2f_s + f_{alias}$ ('K=2' for '$Kf_s + f_{alias}$'). (e). Alias signal of sine wave in (d). We observe that the alias signal in (c) is the same sequence of bits as the alias signal in (e) (with a phase shift).

Given

$$f_{vco} = Kf_s + f_{alias}, \tag{5.1}$$

where K is a non-negative integer. Based on the observation that the digital subsampling is mathematically a residue operation, the generated digital alias signals for any value of K will produce the same digital sequence of bits. To conceptualize the technique, assume there is a periodical sine wave with frequency equal to f_{alias} available. Using the sampling clock f_s to digitally sample this signal, the output signal is therefore the digital alias signal corresponding to K=0. Figure 39 has shown that for different K ('K=0' and 'K=2'), the alias signals are the same sequence of bits with phase shifted. Therefore, for any other K as in a targeting frequency $f_{vco} = Kf_s + f_{alias}$, the alias signal corresponding to K=0 as illustrated in Figure 39 (c) can be used as the reference alias signal in Figure 38 (f).

The relationship between the sampling clock and the alias signal corresponding to K=0 can be predetermined, therefore the alias signal corresponding to K=0 can be generated by digital logic.

```
// f_alias is the desired alias signal frequency
// f_s is the sampling frequency
// Out is the expected alias digital signal output
// Δt is a time unit
For j = 1:∞
    if cos (2πf_S(j − 1) ∗ Δt) <0 AND cos (2πf_S j ∗ Δt) >=0
// the rising edge of the sampling clock
        if cos (2πf_alias j ∗ Δt)>0
          Out[j] =1;
        Else
          Out[j] =0;
    else
        Out[j] = Out[j-1];
    end
end
```

Figure 40: Pseudo code of alias-generator for generating the reference alias signal.

Figure 40 shows pseudo code for generating the reference alias signal. The module is named as the alias-generator, which is a synthesizable digital block clocked by the sampling clock f_s to generate the reference clock signal.

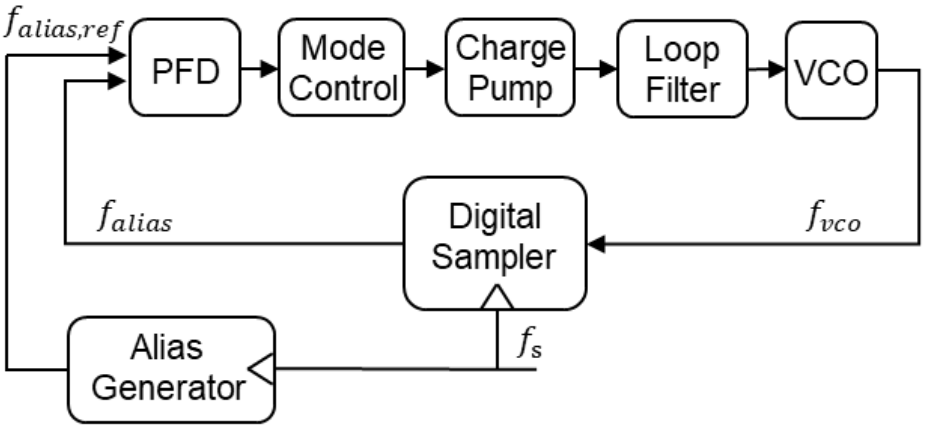


Figure 41: The proposed Coresidual Alias-Locked Loop (C-ALL) architecture [63].

By feeding the output of the alias-generator to the PFD as the reference, both the frequency and

the phase of the feedback alias signal will be compared with the reference alias signal. This type of circuit architecture is named a C-ALL, since the loop mathematically implements a coresidual function when in lock as illustrated in Figure 41. Simulation has verified that a C-ALL can not only lock in frequency but also lock in phase as illustrated in Figure 38 (e-h). Therefore, the periodical spurs which exist in an ALL are eliminated in a C-ALL.

5.4. Phase-Domain Model and Noise Analysis

Phase noise is one of the most important measures of merit to evaluate the performance of a PLL. To analyze the phase noise of an ALL and a C-ALL, the following phase domain models are therefore proposed. To our knowledge, no linear phase analysis has been attempted, either in a component level for a digital sampler, or in the system level for an ALL or a C-ALL. The importance of this phase analysis comes when optimizing the loop phase noise performance by choosing loop bandwidth or sampling clock frequency etc.

5.4.1. Phase-domain model of a digital sampler

Figure 42 has shown a phase domain model of a digital sampler. A digital sampler consists of two parts: an analog sampler with an interpolation filter, and a 1-bit quantizer.

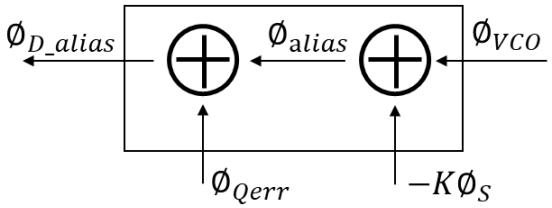


Figure 42: Phase domain model of a digital sampler, which consists of an analog sampler, an interpolation filter and a 1-bit quantizer.

An analog sampler with an interpolation filter can mathematically result in the residue operation:

$$\emptyset_{alias} = mod(\emptyset_{VCO}, \emptyset_S) = \emptyset_{VCO} - K\emptyset_S, \tag{5.2}$$

where $\emptyset_{VCO}$, $\emptyset_S$ and $\emptyset_{alias}$ represent the phases of the VCO signal, the sampling clock and the analog sampler output, respectively. Here $K = \text{round}\left(\emptyset_{VCO}/\emptyset_S\right) \approx \text{round}\left(\text{f}_{VCO}/\text{f}_S\right)$ is a non-

negative integer, which is defined as the subsampling ratio.

Digital sampling is a one-bit quantization of analog sampling. Therefore, the final output of a digital sampler can be represented as:

$$\emptyset_{D\_alias} = \emptyset_{alias} + Q_{err} = \emptyset_{VCO} - K\emptyset_S + Q_{err}. \tag{5.3}$$

Figure 42 shows the phase domain model of a digital sampler.

5.4.2. Phase-domain analysis of an ALL

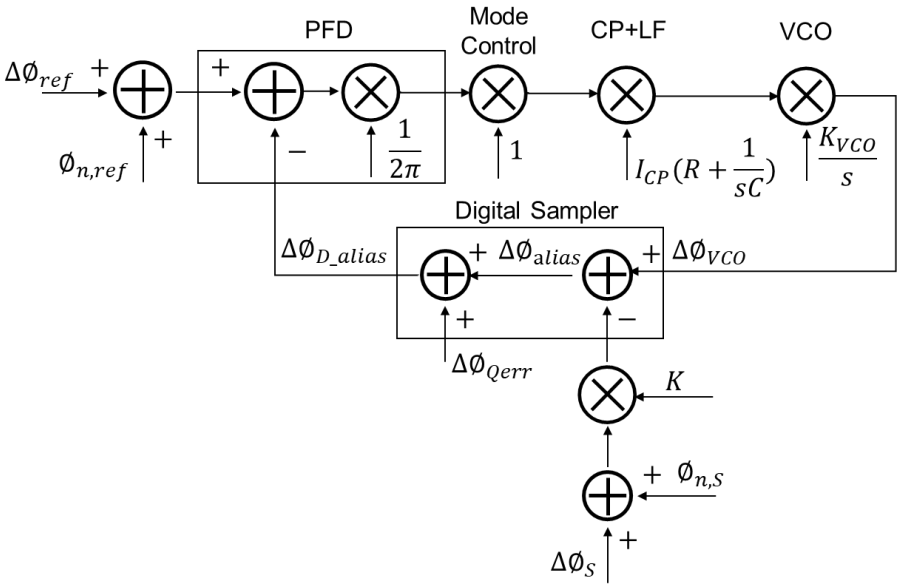


Figure 43. Phase domain model of an ALL, with noise sources from the sampling clock and the reference clocks.

Figure 43 has illustrated the phase domain model of an ALL. Phase noise contributions from sampling clock noise, reference clock noise, PFD/CP noise and the digital sampler quantization error are analyzed in the following.

5.4.2.1. Phase noise contributions from quantization errors

The quantization errors from digital sampling result in phase errors in the PFD, which appear as phase noise at the output spectrum. Based on Equation (5.3), the transfer function can be described as:

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{Qerr}}\right)_{ALL} = \frac{Forward\ Gain}{1 + Loop\ Gain} = \frac{1}{\frac{1}{\frac{1}{2\pi} I_{cp}(R + \frac{1}{sC})\frac{K_{vco}}{s}} + 1}. \quad (5.4)$$

Thus, the quantization error resulting from digital sampling is low-pass filtered by the loop filter and contributes to the total output phase noise.

5.4.2.2. Phase noise contributions from sampling clock phase noise

Similarly, the transfer function from the sampling clock phase noise to the output phase noise can be calculated as

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{n,s}}\right)_{ALL} = \frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{D\_alias}} \frac{\Delta\emptyset_{D\_alias}}{\Delta\emptyset_{n,s}}. \quad (5.5)$$

Applying Equation (5.3), we find the $\Delta\emptyset_{D\_alias}$ is K times dependence on $\Delta\emptyset_{n,s}$:

$$\frac{\Delta\emptyset_{D\_alias}}{\Delta\emptyset_{n,s}} = K. \quad (5.6)$$

Combing Equations (5.5) and (5.6), we have:

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{n,s}}\right)_{ALL} = \frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{D\_alias}} \frac{\Delta\emptyset_{D\_alias}}{\Delta\emptyset_{n,s}} = K \frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{D\_alias}} = \frac{K}{\frac{1}{\frac{1}{2\pi} I_{cp}(R + \frac{1}{sC})\frac{K_{vco}}{s}} + 1}. \quad (5.7)$$

Therefore, the phase noise of the sampling clock is first multiplied by the subsampling ratio K and then low-pass filtered by the loop.

5.4.2.3. Phase noise contributions from reference clock phase noise

The transfer function from the reference clock phase noise to the output phase noise can be calculated as

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{n,ref}}\right)_{ALL} = \frac{Forward\ Gain}{1 + Loop\ Gain} = \frac{1}{1 + \frac{1}{\frac{1}{2\pi} I_{cp}(R + \frac{1}{sC})\frac{K_{vco}}{s}}}. \quad (5.8)$$

Similar to a conventional PLL, the reference clock phase noise is low-pass filtered by the loop. Within the loop bandwidth, Equation (5.8) can be approximated as:

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{n,ref}}\right)_{ALL} \approx \frac{\frac{1}{2\pi} I_{cp}\left(R + \frac{1}{sC}\right)\frac{K_{vco}}{s}}{\frac{1}{2\pi} I_{cp}\left(R + \frac{1}{sC}\right)\frac{K_{vco}}{s}} = 1, \quad (5.9)$$

In a PLL, the transfer function from the reference clock phase noise to the output phase noise can be written as follows:

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{n,ref}}\right)_{PLL} = \frac{\frac{1}{2\pi} I_{cp}\left(R + \frac{1}{sC}\right)\frac{K_{vco}}{s}}{1 + \frac{1}{2\pi} I_{cp}\left(R + \frac{1}{sC}\right)\frac{K_{vco}}{s}\frac{1}{N}} \approx \frac{\frac{1}{2\pi} I_{cp}\left(R + \frac{1}{sC}\right)\frac{K_{vco}}{s}}{\frac{1}{2\pi} I_{cp}\left(R + \frac{1}{sC}\right)\frac{K_{vco}}{s}\frac{1}{N}} = N, \quad (5.10)$$

where N is the division ratio in a PLL.

In a subsampling PLL, an analog subsampler functions as a phase detector in [80][81], the transfer function from the reference clock phase noise to the output phase noise can be written as follows:

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{n,ref}}\right)_{SSPLL} = \frac{A_{SSPD} I_{cp}\left(R + \frac{1}{sC}\right)\frac{K_{vco}}{s}}{1 + A_{SSPD} I_{cp}\left(R + \frac{1}{sC}\right)\frac{K_{vco}}{s}\frac{1}{N}} \approx \frac{A_{SSPD} I_{cp}\left(R + \frac{1}{sC}\right)\frac{K_{vco}}{s}}{A_{SSPD} I_{cp}\left(R + \frac{1}{sC}\right)\frac{K_{vco}}{s}\frac{1}{N}} = N, \quad (5.11)$$

where N is the division ratio between the targeting VCO frequency and the reference clock frequency, A_{SSPD} represents the gain of the sampling PD. By comparing Equations (5.9) and (5.10), we observe that the phase noise power contribution from the reference clock is N^2 smaller in an ALL compared to in a conventional PLL and in an SSPLL.

5.4.2.4. Phase noise contributions from PFD/CP noise

In an ALL, by calculating the phase noise transfer function, we can obtain the output phase noise

contributed from the PFD and CP.

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{n,PFD}}\right)_{ALL} = \frac{I_{cp}(R+\frac{1}{sC})\frac{K_{vco}}{s}}{1+\frac{1}{2\pi}I_{cp}(R+\frac{1}{sC})\frac{K_{vco}}{s}}. \quad (5.12)$$

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta I_{n,CP}}\right)_{ALL} = \frac{(R+\frac{1}{sC})\frac{K_{vco}}{s}}{1+\frac{1}{2\pi}I_{cp}(R+\frac{1}{sC})\frac{K_{vco}}{s}}. \quad (5.13)$$

Similar to a conventional PLL, the PFD and CP noise is low-pass filtered by the loop. Within the loop bandwidth, Equations (5.11) and (5.12) can be approximated as:

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{n,PFD}}\right)_{ALL} = \frac{I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}}{1+\frac{1}{2\pi}I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}} \approx \frac{I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}}{\frac{1}{2\pi}I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}} = 2\pi. \quad (5.14)$$

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta I_{n,CP}}\right)_{ALL} = \frac{\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}}{1+\frac{1}{2\pi}I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}} \approx \frac{\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}}{\frac{1}{2\pi}I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}} = \frac{2\pi}{I_{cp}}. \quad (5.15)$$

For a PLL, the transfer function can be written as follows:

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{n,PFD}}\right)_{PLL} = \frac{I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}}{1+\frac{1}{2\pi}I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}\frac{1}{N}} \approx \frac{I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}}{\frac{1}{2\pi}I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}\frac{1}{N}} = 2\pi N, \quad (5.16)$$

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta I_{n,CP}}\right)_{PLL} = \frac{\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}}{1+\frac{1}{2\pi}I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}\frac{1}{N}} \approx \frac{\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}}{\frac{1}{2\pi}I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}\frac{1}{N}} = \frac{2\pi}{I_{cp}}N, \quad (5.17)$$

where N is the division ratio in a PLL.

For an SSPLL, the transfer function at low frequencies can be written as follows:

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{n,PD}}\right)_{SSPLL} \approx \frac{I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}}{A_{SSPD}I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}} = \frac{1}{A_{SSPD}}, \tag{5.18}$$

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta I_{n,CP}}\right)_{SSPLL} \approx \frac{\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}}{A_{SSPD}I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}} = \frac{1}{A_{SSPD}I_{cp}}. \tag{5.19}$$

By comparing Equations (5.14) to (5.18), Equations (5.14) and (5.16), the power of the phase noise contributed from PFD and CP is N^2 smaller in an ALL compared to in a conventional PLL.

From all the above analysis and calculations, the noise contributions to the VCO output of loop components are summarized below and in Table 1:

Table 1: Comparison of Phase noise Contribution from loop components

Phase noise multiplication factors	Circuit architectures		
	PLL	SSPLL	ALL/CALL
Reference/Sampling clock	N^2	N^2	K^2
PFD	N^2	*1*	*1*
CP	N^2	*1*	*1*

1) Reference or sampling clock: In a PLL/SSPLL/ALL /CALL, the reference clock/sampling clock phase noise will be multiplied by N^2 or K^2, respectively, where N is the division ratio of a conventional PLL or a SSPLL, and K is the subsampling ratio in an ALL or a CALL.
2) PFD/CP phase noise contributions: In an ALL or an SSPLL, the phase noise contribution from the PFD/CP is not multiplied by the subsampling ratio K or the division ratio N, while it is multiplied by the division ratio N in a conventional PLL.

5.4.3. Phase-domain analysis of a C-ALL

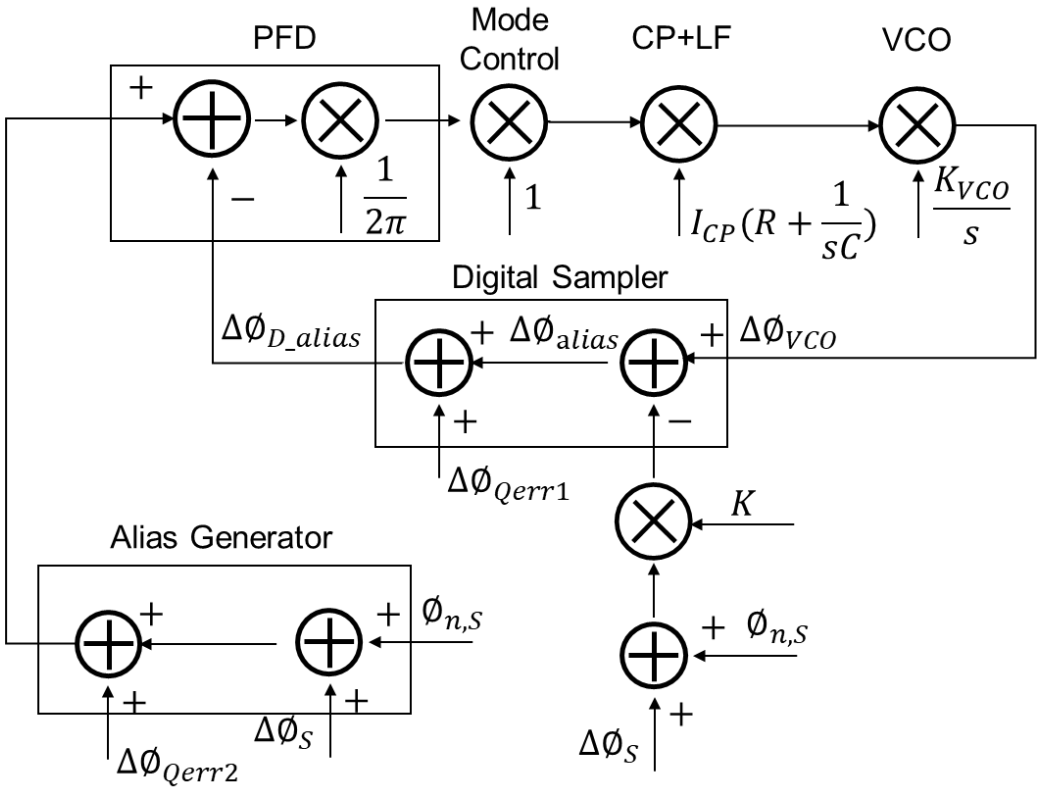


Figure 44: Phase domain model of a C-ALL. Here we only consider noise from the sampling clock and the quantization error.

As a synthesizable digital block clocked only by the sampling clock f_s, the alias-generator assumes an ideal noiseless reference clock sampled by the sampling clock and quantized by the sampler. Because of the 1-bit quantization, quantization error is also introduced and the phase domain model of a C-ALL is shown in Figure 44.

In an ALL, a reference clock is used as the input of the PFD and therefore contributes to the output phase noise. In a C-ALL, however, the reference signal $\emptyset_{ref}$ as illustrated Figure 44 is assumed to be noiseless. By calculating the transfer function, the phase noise contribution of the quantization error Q_{err2} to the output can be determined by:

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{Qerr2}}\right)_{C-ALL} = \frac{\frac{1}{2\pi}I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}}{1+\frac{1}{2\pi}I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}} = \left(\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{Qerr1}}\right)_{C-ALL}. \quad (5.17)$$

Therefore, compared to the reference clock contributing to output phase noise in an ALL, there is no reference clock contribution in a C-ALL. Meanwhile, the phase noise contribution of quantization error from the alias-generator is newly introduced in a C-ALL. Since both input signals of the PFD are generated by the same sampling clock, the two signals can be synchronized by the sampling clock before feeding into the PFD and thereby remove the accumulated jitter.

5.4.4. Spur calculation of ALL and C-ALL

While conventional integer-N charge-pump-based PLLs can approach zero phase error in lock (theoretically in the absence of noise, etc.), ALLs, like fractional-N PLLs and bang-bang PLLs, continuously produce non-zero phase error feedback, even in lock in most scenarios. Fractional-N frequency synthesizers generate spurs at the output of VCO because of the programmable feedback divider that switches between two different integer division ratios in order to get a fractional one. The VCO output is impacted by this alternating signaling, producing frequency spurs in the VCO output spectrum. Similarly, bang-bang PLLs produce significant up and down signaling when in lock, which generate unwanted spurs at the output of VCO due to the nonlinearity of the bang-bang phase detector. Similar to the fractional-N PLLs and bang-bang PLLs, the ALL has alternating up/down signaling in lock (as shown in Figure 38 (a-d)) that produces frequency spurs in its output spectrum (as shown in Figure 48 (a)).

In order to understand how severely these spurs affect the spectrum of VCO in an ALL, the analysis is performed below.

Take Figure 38 (a-d) as an example, the charge pump current of the ALL is given by:

$$I_{CP}(x) = \begin{cases} -I_0, & nT \le x < nT + \tau_1, \\ I_0, & nT + \frac{2}{3}T - \tau_2 \le x < nT + \frac{2}{3}T, \\ 0, & others, \end{cases} \tag{5.18}$$

where I_0 represents the amplitude of the charge pump current , T represents the period of the charge pump, τ_1 and τ_2 represent the duration of the charge pump currents in the down path and

the up path, respectively. For this analysis, we assume there is no mismatch between the up and down path.

The control voltage of the VCO can be calculated as:

$$V_{ctrl}(t)_{ALL} = V_0 + \frac{\int_0^t I_{cp}\, dx}{C_{filter}}. \tag{5.19}$$

Let $A = V_0 - \frac{I_0\tau_1}{C_{filter}}$, $\tau = \frac{2}{3}T - \tau_1 - \tau_2$, $\omega = \frac{2\pi}{T}$, and with Fourier series expansion,

$$V_{ctrl}(t)_{ALL} \approx \frac{A\tau}{T}\sum_{n=-\infty}^{\infty} sinc\left(\frac{n\omega\tau}{2}\right) e^{j\omega nt}, \tag{5.20}$$

Based on the control voltage, the VCO signal can be obtained as:

$$V_{vco}(t) = V_A\, cos\left(\omega_0 t + 2\pi K_{vco}\int_0^t V_{ctrl}(x)_{ALL}\, dx\right)$$

$$= V_A\, cos\left(\omega_0 t + 2\pi K_{vco}\frac{A\tau}{\omega T}\sum_{n=-\infty}^{\infty}\frac{1}{n}Sa\left(\frac{n\omega\tau}{2}\right) sin\, n\omega t\right)$$

$$= V_A\, cos\left(\omega_0 t + \alpha_n\sum_{n=-\infty}^{\infty} sin\, n\omega t\right)$$

$$= V_A\mathcal{R}\left\{e^{j\omega_0 t}\prod\nolimits_{n=1}^{\infty} e^{j\alpha_n sin\, n\omega t}\right\} = V_A\mathcal{R}\left\{e^{j\omega_0 t}\prod_{n=1}^{\infty}\left(\sum_{m=-\infty}^{\infty} J_m(\alpha_n)e^{jm\omega t}\right)\right\}, \tag{5.21}$$

where $\alpha_n = 2\pi K_{vco}\frac{A\tau}{\omega T}\frac{1}{n}sinc\left(\frac{n\omega\tau}{2}\right)$, and $J_i(\cdot)$ is the i-th order Bessel function of the first kind. The magnitude of each spur at different frequency can be determined from Equation (5.21).

From Equations (5.21) we conclude that each harmonic at the control line of a VCO will generate an infinite number of spurs at multiple frequencies around the carrier frequency of the VCO; In this case of an ALL, there will be infinite number of spurs at frequency offset of multiple of 100MHz, as will be illustrated in Figure 48 (a).

The largest spur is at 100 MHz offset, and the magnitude of spur can be calculated as:

$$Spur_{@100MHz} = \frac{V_A \mathcal{R}\left\{e^{j\omega_0 t}\prod_{n=1}^{\infty}\left(J_m(\alpha_n)e^{jm\omega t}{}_{|m=1}\right)\right\}}{V_A \mathcal{R}\left\{e^{j\omega_0 t}\prod_{n=1}^{\infty}\left(J_m(\alpha_n)e^{jm\omega t}{}_{|m=0}\right)\right\}}$$

$$= \frac{\mathcal{R}\left\{e^{j(\omega_0+\omega)t}\prod_{n=1}^{\infty}\left(J_1\left(2\pi K_{vco}\frac{A\tau}{\omega T}\frac{1}{n}sinc\left(\frac{n\omega\tau}{2}\right)\right)\right)\right\}}{\mathcal{R}\left\{e^{j\omega_0 t}\prod_{n=1}^{\infty}\left(J_0\left(2\pi K_{vco}\frac{A\tau}{\omega T}\frac{1}{n}sinc\left(\frac{n\omega\tau}{2}\right)\right)\right)\right\}}, \quad (5.22)$$

In the implementation, I_0 is $100\mu A$ representing the charge pump current amplitude, T is 10ns representing the period of spur, τ_1 and τ_2 are approximately 0.3ns and 0.4ns representing the duration of the charge pump currents in the down path and the up path, respectively.

Solving the Bessel functions numerically using Matlab we get the estimate,

$$Spur_{@100MHz} \approx -51dBc. \quad (5.23)$$

Note that Equations (5.20) and (5.23) contain approximations and this model does not include other sources of spur such as sampling clock feedthrough. As illustrated in Figure 48 (a), the spur level at 100MHz offset from the post-layout simulation result is -44.4dBc, which is within 7dB, showing this technique is accurate in frequency and has strong predictive value of the spur magnitude for design work. We will show in Section 5.6 that the C-ALL further suppresses the spurs by 27 dB.

5.5. Discussion

5.5.1. Continuous-time approximation

To satisfy the continuous-time approximation requirement in a PFD-based PLL, the loop filter time constant needs to be significantly larger than the PFD updating period, therefore we have:

$$\omega_{-3dB} \ll 2\pi f_{PFD}, \tag{5.24}$$

where ω_{-3dB} is the loop bandwidth and f_{PFD} represents the PFD updating frequency.

For a certain range of desired frequencies, f_{PFD} varies for different f_{vco}. To meet the requirement of Equation (5.24), the loop bandwidth is set to satisfy:

$$\omega_{-3dB} \leq \frac{1}{10} * 2\pi f_{PFD,min}. \tag{5.25}$$

A larger allowed loop bandwidth ω_{-3dB}, which corresponds to a higher PFD updating frequency $f_{PFD,min}$ (defined as the minimum f_{PFD} for all targeting frequencies), allows the selection of a higher loop bandwidth which leads to better VCO noise suppression.

For a conventional PLL, no matter an integer-N one or a fractional-N one, the PFD updating frequency $f_{PFD,min}$ is equal to the reference frequency:

$$(f_{PFD,min})_{PLL} = f_{ref} = \frac{f_{VCO}}{N}. \tag{5.26}$$

For a C-ALL, however, the PFD updating frequency f_{PFD} is equal to the alias frequency f_{alias}, which varies for different targeting frequencies.

$$(f_{PFD,min})_{C-ALL} = f_{alias,min}. \tag{5.27}$$

Assume a targeting frequency range of $\{f_a, f_a + \Delta f, f_a + 2\Delta f, \dots, f_b\}$ to be synthesized with different types of circuit architectures. For simplicity purpose, further assume f_a is a multiple of Δf.

For an integer-N PLL, the reference frequency f_{ref} need to be set as Δf, hence we have:

$$(f_{PFD,min})_{integer-N\ PLL} = (f_{ref})_{integer-N\ PLL} = \Delta f. \quad (5.28)$$

For a fractional-N PLL, however, the reference frequency f_{ref} can be set to be much higher than Δf, which is usually determined by the order of the ΔΣ modulator. Take frequency synthesizers for Bluetooth application {2.402 GHz, 2.403 GHz, … , 2.48 GHz} as an example, a 1 MHz reference frequency, which is equal to the frequency resolution, was used inside an integer-N PLL in [82] while a 40 MHz reference frequency was used inside a fractional-N PLL in [83]. Therefore, we have:

$$(f_{PFD,min})_{factional-N\ PLL} = (f_{ref})_{frational-N\ PLL} \gg \Delta f. \quad (5.29)$$

For a C-ALL, the alias frequency f_{alias} is determined by the sampling frequency.

Assume a sampling frequency f_s is applied, the generated alias frequencies could be $\{f_x + \Delta f, f_x + 2\Delta f, \dots\}$, where $f_x = mod(f_a, f_s)$. Then we have:

$$\left(f_{PFD,min}\right)_{C-ALL} = \min\{f_x + \Delta f, f_x + 2\Delta f, \dots\} = f_x + \Delta f. \quad (5.30)$$

In the case where f_s is a integer fraction of f_a, f_x will therefore be 0 and $\left(f_{PFD,min}\right)_{C-ALL}$ is Δf. Still take the abovementioned Bluetooth application as an example, $\left(f_{PFD,min}\right)_{C-ALL}$ will be 2 MHz and 402MHz if f_s is set to be 200 MHz and 1 GHz, respectively.

Based on Equations (5.28) (5.29) and (5.30), for the same targeting frequencies, the PFD updating frequency of an integer-N PLL is smaller, and in most cases much smaller, compared to a fractional-N PLL or a C-ALL. By carefully choosing the sampling frequency, it can bring larger flexibility for a C-ALL in choosing the loop bandwidth compared to an integer-N PLL.

5.5.2. Bandwidth of the loop

As discussed in Section 5.5.1, the loop bandwidth is constrained by Equation (5.27) in a C-ALL because of the continuous time approximation. Furthermore, based on the analysis in Section 5.4, the VCO phase noise is high-pass filtered by the loop while the quantization errors and phase noises from the other components are low-pass filtered by the loop. Therefore, similar to the loop

bandwidth of a conventional PLL, the loop bandwidth of a C-ALL (and also an ALL) determines the output phase noise contributions from each component and hence impacts on the total phase noise performance of the loop.

5.5.3. Sampling clock and quantization error

In addition to removing the frequency spurs produced by the ALL, a C-ALL has another advantage of eliminating the reference clock. As illustrated in Figure 36, an ALL circuit architecture requires one sampling clock and one reference clock. By using the alias generator module clocked by the sampling clock, only one clock is therefore needed in a C-ALL as illustrated in Figure 41.

Quantization error is introduced when the analog alias signal is digitized to be 0's and 1's by the digital sampler. The difference in phase, or the difference in rising edge between actual alias signal and the digital alias signal, is defined as the quantization error. As discussed in Section 5.4, quantization error in an ALL or a C-ALL is low-pass filtered by the loop and therefore directly impacts the output phase noise performance. C-ALLs, and all other digital sampling-based frequency synthesizers such as ALLs, are all similar to bang-bang PLLs [84][85], where phase detectors provide digital bang-bang output to the charge pump regardless of the amplitude of the phase difference. This is different from conventional PLLs, where a PFD provides time-domain or voltage-domain analog continuous feedback that is proportional to the phase difference.

Basically, the high frequency sampling clock is used as 'ruler' to quantize the analog alias signal. The higher the sampling clock frequency, the smaller the quantization error will be (at the cost of creating higher frequency digital circuits and the corresponding power consumption).

Current implementations of the SS-PLL, no matter in integer-N mode [86][28][29] or fractional-N mode [34][36], have the limitation that, in lock, at the sampler, the sampled input frequency must be an integer multiple of the sampling clock (although each signal may be optionally processed through some frequency adjustment). The ALL and C-ALL have a different limitation in that when in lock, the VCO frequency cannot be close to an integer multiple of half the sampling clock frequency, but outside of this, provides greater tuning range. For a given

sampling clock f_{s1}, any targeting frequencies that are close to or equal to $M * \frac{f_{s1}}{2}$ (where M is any positive integer) to be synthesized by an ALL or a C-ALL need to switch to a new sampling frequency f_{s2} [16]. Hence, for the SS-PLL, ALL and C-ALL, the reference or sample clock can be adjusted in order to provide a broad tuning range.

5.6. Design and Simulation Results

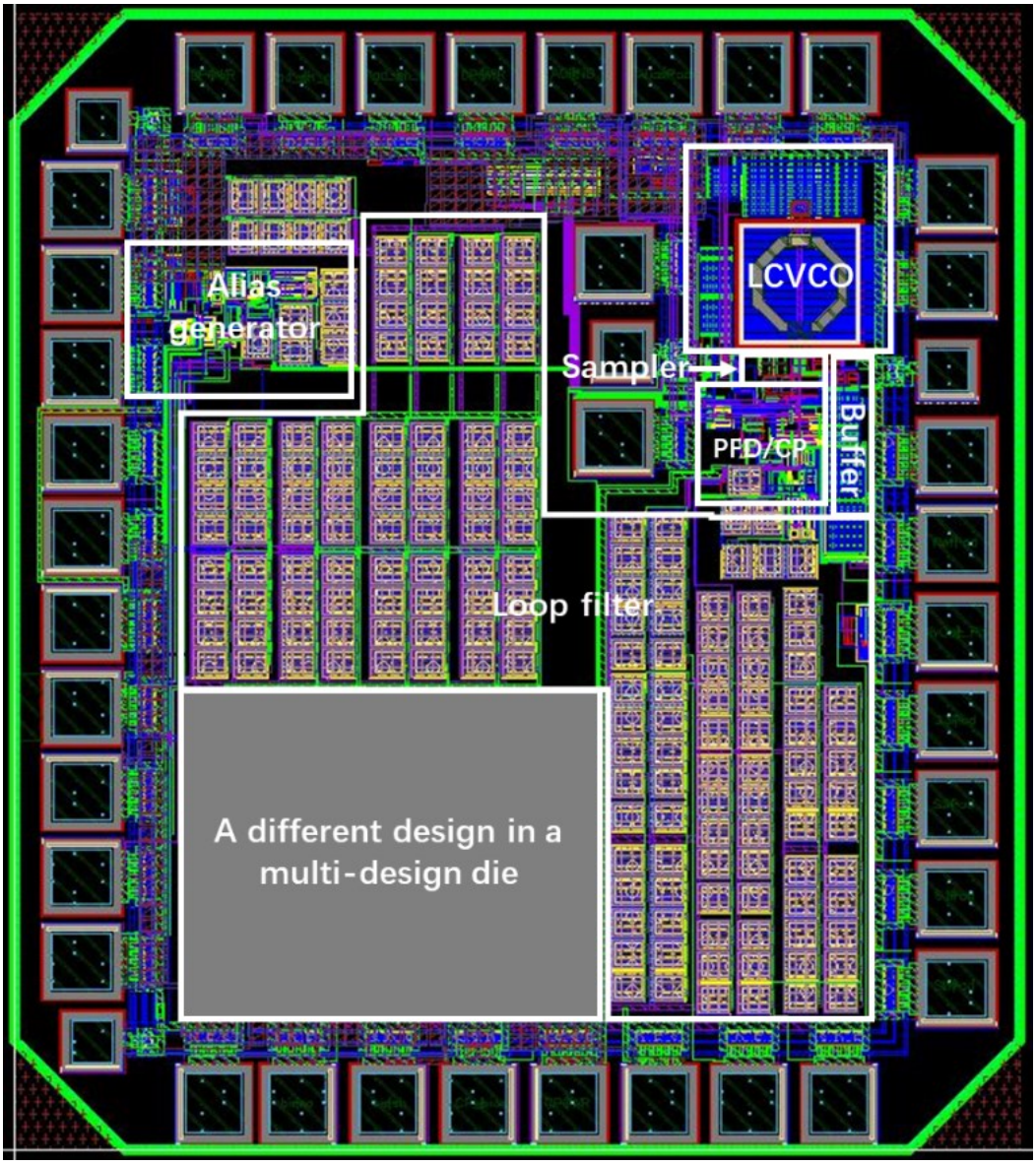


Figure 45: Layout containing the 21GHz - 23.3 GHz C-ALL.

To verify the proposed architecture as shown in Figure 41, a 21-23.3 GHz C-ALL was designed

using GlobalFoundries 130 nm Bulk CMOS process and post-layout extracted circuit simulations were performed in Cadence Spectre. The layout of the key components, including LC VCO, sampler, loop components (PFD and charge pump), loop filter and output buffers are shown in Figure 45.

5.6.1. LC VCO

A 21-23.3 GHz LC VCO is designed. The VCO is tuned with varactors and two binary-weighted switched capacitors, which extend the tuning rage (21GHz - 23.3 GHz) without increasing the K_{VCO} of the VCO (~614MHz/V in the middle range). For the inductor, both the parameterized model from GlobalFoundries process kit and the extracted model generated from ADS Momentum were used in Spectre simulations, and there is only ~1% of frequency change between the two simulation methods. Post-layout simulation results are shown in Figure 46.

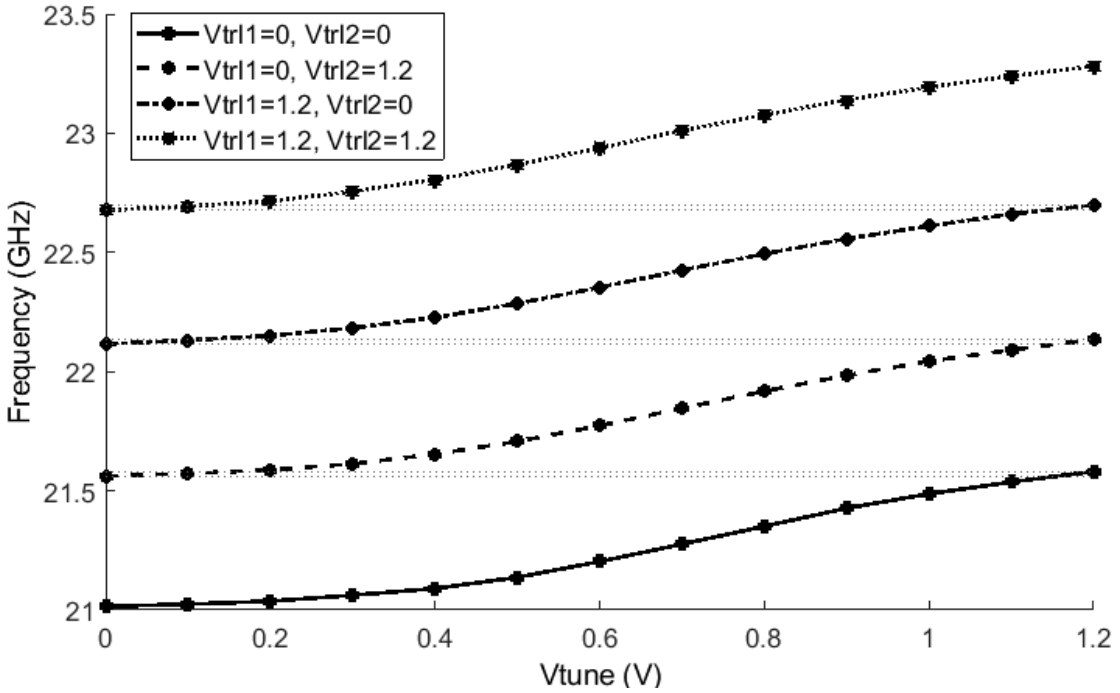


Figure 46: Post-layout simulation results of the VCO. By using a 2-bit switchable MIM capacitor bank, the VCO achieves a wide tuning range from 21 GHz to 23.3 GHz.

5.6.2. Sampler

A CML (current mode logic) latch is used to sample the 21-23.3 GHz VCO, with a sampling

clock tested up to 1GHz. To reduce the effects of the act of sampling from loading the VCO, buffers are inserted between the VCO and sampler. There are various types of non-idealities such as DC offset, which could be caused by process variations or layout mismatches. So long as any DC offset is reasonable and the sampler records 1's and 0's, the impact of DC offset is usually only on phase but not frequency, and therefore can be neglected. If DC offset were an issue, a DC offset cancellation input on the sampler could be implemented, informed by a counter on the output, in order to approach an equal population of sampled 1's and 0's [78].

5.6.3. Sampling clock buffer

The rising edge of the sampling clock is highly critical for low noise sampling, while the falling edge is not relevant to the sampling. A buffer similar to [74] is designed to ensure the rising edge clean. By re-positioning the triggered edges for the NMOS and the PMOS, short-circuit current can be avoided and a clean sharp rising edge can be therefore obtained.

5.6.4. Other modules

Based on the pseudo code provided in Figure 40, the alias-generator module is designed using VHDL and synthesized with digital standard cells. The PFD is implemented with the conventional architecture, and a fully differential topology has been used in the charge pump design to reduce the effect of the non-idealities of the charge pump transistors. A module named mode-control is designed to invert the sense of lead and lag to ensure the loop always negative feedback. Loop filter, and therefore loop bandwidth, is optimized for the best phase noise performance when the in-band phase noise is equal to the out-of-band phase noise.

5.6.5. Simulations

The C-ALL was verified through a post-layout simulation using Cadence. Both the ALL and C-ALL are simulated synthesizing 19 different frequencies with similar results. Simulations are run with full transistor noise models at 27℃. By using a reference alias signal generated by the alias-generator, Figure 47 has shown that the C-ALL can achieve lock and synthesize the desired 21.7 GHz signal.

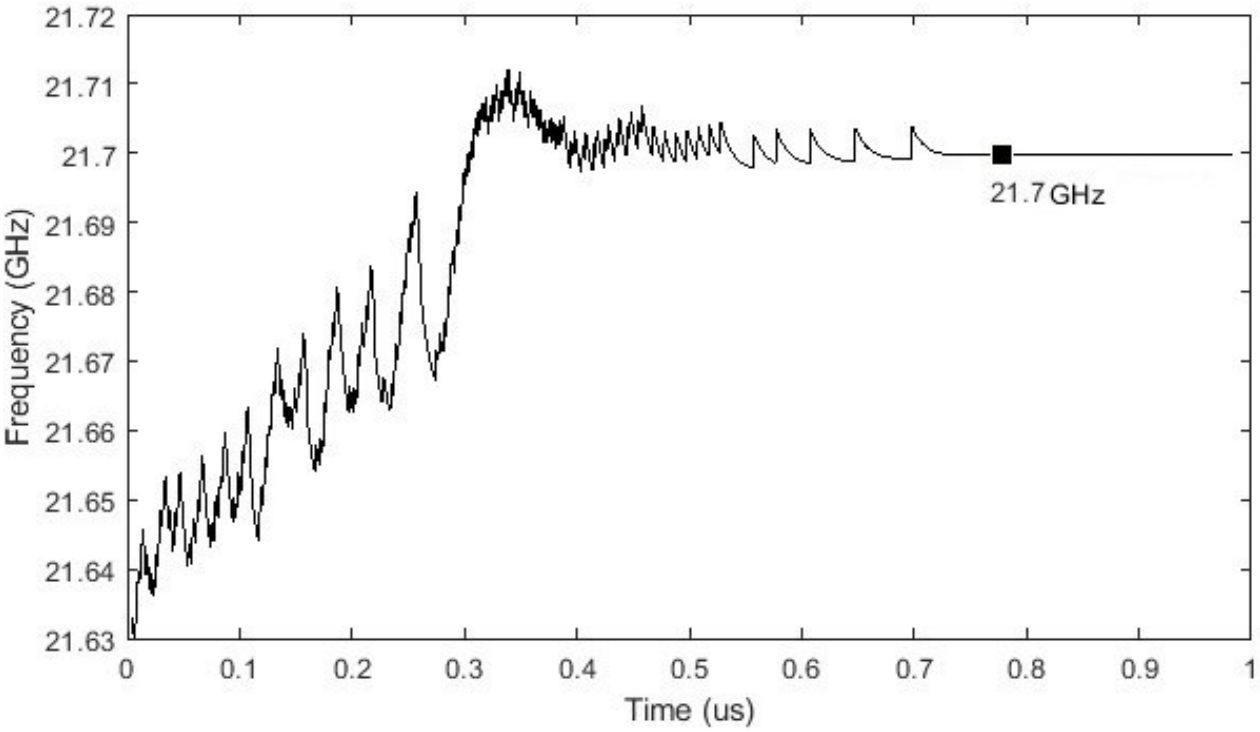


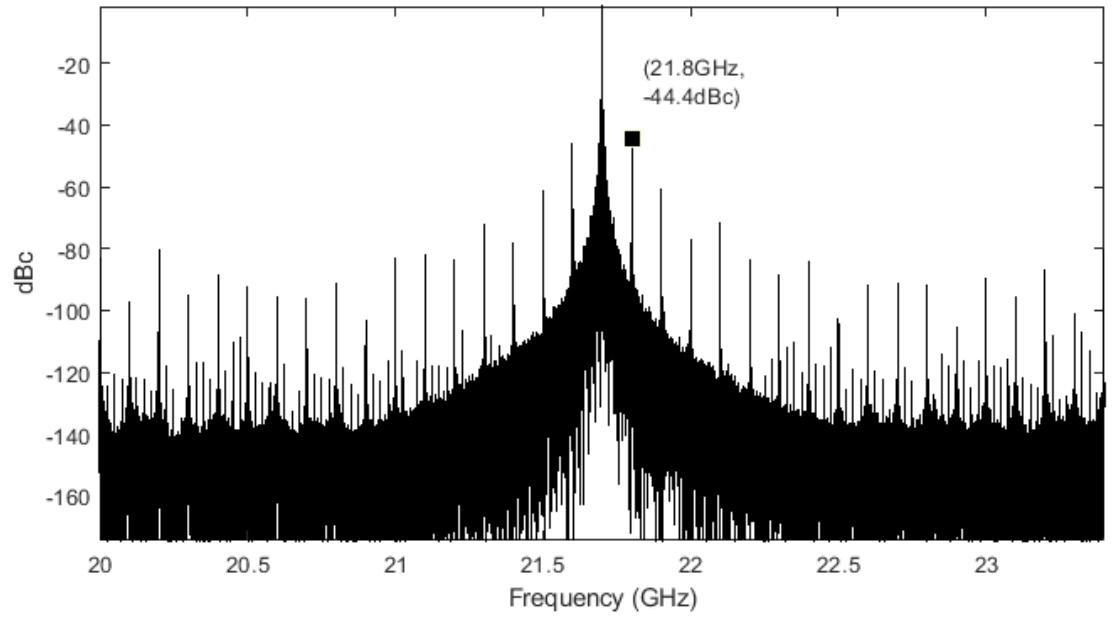
Figure 47: Post layout simulation results of the C-ALL. The design can achieve lock at the desired 21.7 GHz frequency.

Figure 48 has shown the frequency spectrums of the output signals synthesized by the ALL and the C-ALL, respectively. With a 300 MHz square wave as the reference, the VCO output of the ALL has periodic spurs when in lock as expected. As shown in Figure 38 (a), the ALL has a 10 ns periodic behavior producing the spur with a 100 MHz offset. This offset is the greatest common factor of the 300 MHz reference clock and the 1 GHz sampling clock. The magnitude of the largest frequency spur is -44.4 dBc at 100 MHz offset as shown in Figure 48 (a). With the alias generator set to generate a frequency of 300 MHz, the largest spur of the VCO output in the C-ALL (-72.1 dBc at 500 MHz offset as shown in Figure 48 (b)) is due to sampling. Comparing Figure 48 (a) and Figure 48 (b) shows that the proposed C-ALL architecture has reduced the spur level by 27.7 dB.

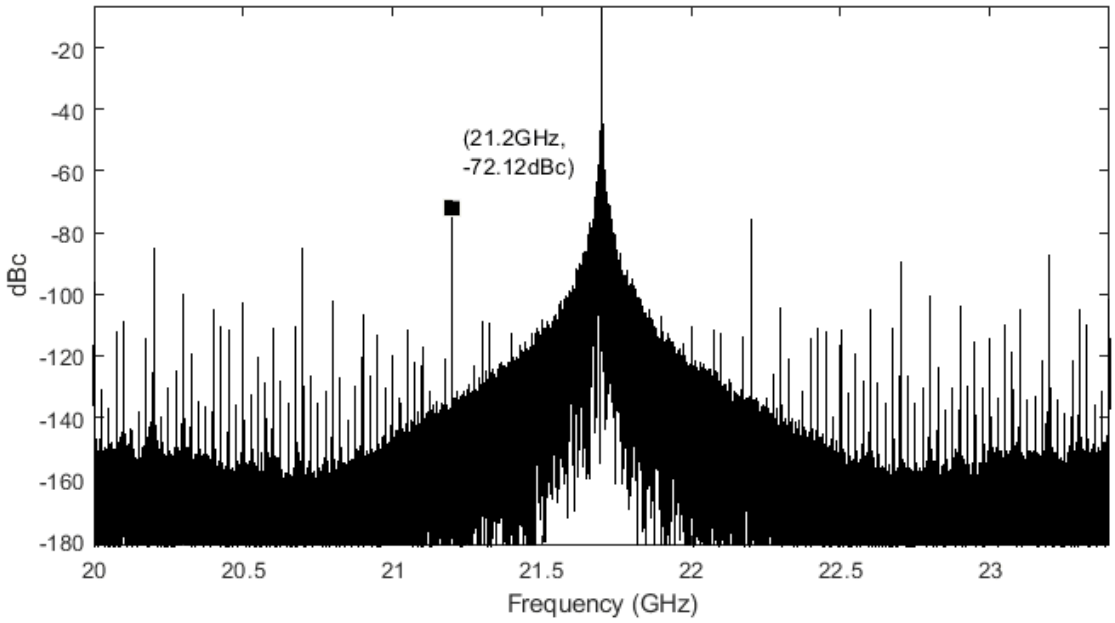
5.6.6. Comparisons with state-of-the-art frequency synthesizers

Comparisons with state-of-the-art frequency synthesizers are shown in Table 2. The total current consumption of the loop is ~11.8mA, including 8mA from the VCO, 2mA from the CML sampler, and ~1.8mA from other loop components. Comparisons have not only shown that the C-

ALL effectively reduces the spur level compared to ALL (from -44.4 dBc to -72.1 dBc), but also shows that the spur level of -72.1 dBc in a C-ALL achieves state-of-the-art results compared to other recent work (-67 dBc in [87], -58 dBc in [88] and -80 dBc in [86]).



(a)



(b)

Figure 48: Output spectrum of the ALL and C-ALL when in lock employing identical loop filters. (a) The ALL's largest spur is -44.4 dBc at 100 MHz offset as expected. (b) The C-ALL's largest spur is -72.12 dBc at 500 MHz offset due to sampling at $f_s = 1$ GHz.

Table 2: Comparison of C-ALL with state-of-the-art frequency synthesizers

	This work		Gao [86] JSSC'10	Sharma [87] JSSC'19	Cherniak [88] JSSC'18	Kim 2006 [89]	Lin 2011 [90]	Cheng 2014 [91]	Luo 2015 [92]
Architecture	ALL	C-ALL	Type-II SS-PLL with spur cancellation	Reference sampling PLL	Digital Bangbang PLL	PLL with half-duty sampled-feedforward loop filter	PLL with 3rd order loop filter	PLL with 3rd order loop filter	PLL with tail feed-back VCO
Feedback module	Digital sampler		Subsampling PD	Static divider	CML Prescaler	ILD	ILD	ILD	CML
Output freq.	21-23.3GHz		2.21GHz	2.05-2.55GHz	20.4-24.6 GHz	17.6-19.4 GHz	20.80-23.37 GHz	19.2-20.6 GHz	24.1-28.2 GHz
Ref. spur	-44.4 dBc	-72.1 dBc	-80 dBc	-67 dBc	-58 dBc	-44 dBc	-45 ~ -50 dBc	-58 dBc	-52 dBc
Reference clock	1GHz		55MHz	50MHz	52MHz	550-606MHz	362MHz	100MHz	108MHz
RMS jitter	0.642ps		0.3ps	0.11ps	0.213ps	0.652ps	0.601ps	0.723ps	0.5856ps
Phase noise	-79.9 dBc/Hz @ 100 kHz, -90.0 dBc/Hz @1 MHz, -109 dBc/Hz @10 MHz		-121 dBc/Hz @ 200 kHz	-122.8 dBc/Hz @ 200 kHz, -125.2 dBc/Hz @1 MHz	−100 dBc/Hz @ 1 MHz	-85.6 dBc/Hz 100 kHz, -101.2 dBc/Hz @1 MHz, -113.5 dBc/Hz @10 MHz	-85 dBc/Hz @1MHz, -122.2 dBc/Hz @ 10 MHz	-75.8 dBc/Hz @ 1MHz, -110 dBc/Hz @ 10 MHz	-84.05-dBc/Hz @ 100 kHz, -92.18 dBc/Hz @1 MHz, -110.08 dBc/Hz @10 MHz
Jitter FoM	-232.33 dB		-244.66 dB	-253.49 dB	-240.49 dB	-230.72 dB	-229.68 dB	-227.02 dB	-230.50 dB
DC power (VCO+loop)	14.2mW (11.8mA@1.2 V)		3.8mW	3.7mW	19.7mW	19.94mW	29.8mW	38mW	26mW
Process	130nm		180nm	65nm	65nm	130nm	180nm	180nm	90nm
Active area	0.25mm²		0.20mm²	0.36mm²	0.42mm²	0.75mm²	0.27mm²	0.46mm²	0.49mm²
$* \ FoM = 10\log\left(\frac{Jitter}{1s}\right)^2 + 10\log\left(\frac{Power}{1mW}\right)$									

In [86], a subsampling delay-locked loop (SSDLL) was introduced outside the SSPLL to align the reference sampling edge with the zero-crossing of the VCO. This can avoid the charge sharing, variation of VCO capacitive load and charge injection during sampling, and therefore reduce the sampling spur. Spur level was reduced from -46 dBc in prior art [74] to -80 dBc in [86].

Another technique called the reference sampling PLL (RS-PLL) was proposed in [87] to reduce the spur level to -67 dBc. Instead of sampling the VCO signal with the sampling clock, an RS-PLL used a VCO square wave to sample the reference sine wave. In [88] the fractional spur was reduced to -58 dBc by pre-distorting the digital-to-time converter (DTC) with digital pre-distortion (DPD).

Among similar frequencies synthesizers (over 17 GHz) in Table 2, [88] has the best FoM of -240.49 dB, with this work following next with a simulated FOM of -232.33 dB. This work, however, has a different set of advantages including lower design complexity and lower spur level. Additionally, the simplicity of digital sampler allows the lowest power consumption for a synthesizer at similar frequencies.

5.6. Conclusion

A coresidual alias-locked loop (C-ALL) circuit architecture is proposed that saves one reference clock and reduces the frequency spurs when compared to the alias-locked loop (ALL) output. Instead of comparing the feedback signal with an external reference clock, an alias signal is generated in the digital domain and used as the reference signal. Therefore, a C-ALL implements a coresidual function.

Phase domain models of both an ALL and a C-ALL are proposed and the phase noise transfer functions are computed. The phase noise contributions from loop components such as PFD, charge pump and reference clock in an ALL is N^2 smaller compared to a conventional PLL, with the cost of additional phase noise from sampling clock and digital sampler quantization error. In a C-ALL, the phase noise contributed by the reference clock is eliminated, the phase noise due to quantization error is increased by 3 dB compared to an ALL.

A 21 – 23.3 GHz C-ALL architecture was designed in GlobalFoundries 130nm Bulk CMOS process and post-layout simulations were performed using Cadence Spectre. Simulation has verified the proposed design can not only achieve lock at the desired frequencies but also significantly reduce output spurs by 27.7 dB.

CHAPTER 6. Phase Shift Coresidual Alias-Locked Loops

In a C-ALL, the high-frequency VCO signal is quantized or digitized by the lower-frequency sampling clock, which produces quantization errors. In phase domain, the quantization errors lead to discontinuities and dead zone in the phase transfer function between the VCO signal and the alias output. The control system, no matter for a C-ALL, provides zero feedback when the VCO signal changes within the dead zone and therefore only achieves coarse phase lock and cannot effectively suppress phase noise. In this chapter, we will propose a new type of locking mechanism and a new type of circuit architecture we call a Phase Shift Alias-Locked Loops (PS-CALLs) that guarantees feedback is provided at every active edge of the alias signal so fine phase lock is achieved.

6.1. Quantization error and dead zone

As discussed in Section 3.3, a digital sampler can be applied as a down-conversion mixer, and the frequency relationship between the RF signal, the sampling clock and the generated alias signal can be characterized by Equation (3.5). When a digital sampler is applied inside the feedback path within a PLL, the phase transfer function of the sampler directly determines the characteristics of the whole loop. In this section, the phase relationship between the VCO signal and the digital alias signal, and corresponding phase transfer function will be discussed.

Revisiting Section 5.4.1 and Equation (5.2), the phase relationship between the VCO signal and the digital alias signal in an ALL or a C-ALL can be modeled as:

$$\emptyset_{alias} = mod(\emptyset_{VCO}, \emptyset_S) = \emptyset_{VCO} - K\emptyset_S, \tag{6.1}$$

where $\emptyset_{VCO}$, $\emptyset_S$ and $\emptyset_{alias}$ represent the phases of the VCO signal, the sampling clock and the analog sampler output, respectively. Here $K = \text{round}\left({}^{\emptyset_{VCO}}/_{\emptyset_S}\right) \approx \text{round}\left({}^{\text{f}_{VCO}}/_{\text{f}_S}\right)$ is a non-negative integer, which is defined as the *subsampling ratio*.

Digital sampling is a one-bit quantization of analog sampling. Therefore, the digital alias signal,

as the final output of a digital sampler, can be represented as:

$$\emptyset_{D,alias} = \emptyset_{alias} + Q_{err} = \emptyset_{VCO} - K\emptyset_S + Q_{err}. \quad (6.2)$$

Due to the quantization error Q_{err} generated from the digital sampling, the phase relationship between the VCO $\emptyset_{VCO}$ and the alias signal $\emptyset_{D,alias}$ is non-linear.

```
φ0 = np.arange(φ_init, φ_end, (φ_end − φ_init)/scan)
// 'scan' represents the number of groups, "φ0" is an array that represents all the possible phases to scan.
interval = range(1, round(time/step)) // 'time' represents simulation time, and 'step' represents the size of each step.
t = np.arange(0, time, step)
φ_S = 2πf_s *t //Phase of the sampling clock.
y_s = sign(sin(φ_s)) //sample clock output.
for j in range(scan):  // scan all the groups.
    φ_j = 2πf_vco*t + φ0[j]   // define φ_j as the VCO phase to be sampled.
    y_vco[j] = sin(φ_j)
    for i in interval:  // for each group, calculate the alias signal for the time interval.
        if y_s[i] > 0 and y_s[i-1] <= 0:
            y_alias [j, i] = sign(y_vco[j, i])
        else:  y_alias [j, i] = y_alias [j, i-1]
    end
end
```

Figure 49: Pseudo code of the behavior-level simulation to verify the phase relationship between the VCO and the digital alias output.

To verify the above analysis, a group of behavior-level simulations (written in Python) has been proceeded to analyze the phase relationship. In the initial simulation setup, a sinusoid signal with the frequency of f_{VCO} and initial phase of 0 is applied as the input VCO signal of the digital sampler, a pulse wave with frequency of f_S and initial phase of 0 is used as the sampling clock of the digital sampler. Sample the VCO signal with the sampling clock and generate a digital alias

signal X_0. Then keep the frequency f_S and initial phase of the sampling clock and the frequency of the VCO f_{VCO} unchanged, and then increase the VCO initial phase gradually. The phase step size is set to be $2\pi/N$, where N is the number of groups that we are going to simulate. The generated digital alias signal is X_1. Repeat the above simulation for another (N-1) times, with each time increasing the initial phase by $2\pi/N$ and keeping all the other parameters unchanged. Specifically, for the i_{th} step, the initial phase of the VCO would be $2\pi * (i-1)/N$ and the generated digital alias signal is X_{i-1}. Simulation pseudo codes are shown as Figure 49.

Phase relationships between the N different phases of VCO and the corresponding generated alias signals can be obtained following the procedures as described in Figure 49. We use the following parameters as an example: $f_{VCO} = 10.1\text{GHz}$, $f_S = 1\text{GHz}$ and N=50. According to Chapter 3, the alias signal has a frequency, f_{alias}, to be 0.1 GHz, which corresponds to a pulse with a period of 10 ns, or 10 sampling periods. Figure 50 shows the simulation results of the phase relationship. Specifically, instead of showing all the alias signals for the 50 different phases, the identical digital alias signals are combined and only the 10 different alias signal patterns have been illustrated. Take the VCO phase between 0 and π/5 for instance, simulations have shown that the first 5 groups (VCO phases: 0, 2π/50, 2*2π/50, 3*2π/50, 4*2π/50) falling into this range correspond to the same alias signal pattern, as illustrated in Figure 50 (b). Similarly, we can obtain the other 9 groups of results as illustrated in Figure 50 (c)~(k).

Assuming the reference alias signal is identical to the alias signal in Figure 50 (b), which means the PFD output is 0 when the VCO phase is any value between 0 and π/5. Similarly, we can plot the PFD output as VCO phases changes from -π to π, as illustrated in Figure 51. From Figure 51, we can have the following observations:

1) The relationship between the PFD output and the VCO phase is quantized linear, which is consistent with the mathematical relationship in Equation (6.2).
2) Because of quantization error, when the VCO phase changes within a certain region, the digital alias output will keep the same phase without any change, and thus the PFD output will stay unchanged. For instance, when the VCO phase changes from 1.2π/5 to 1.3π/5, as long as the phase stays within the interval of (π/5, 2π/5), the PFD output pulse duration will keep as T_S unchanged, where T_S is the sampling clock period.

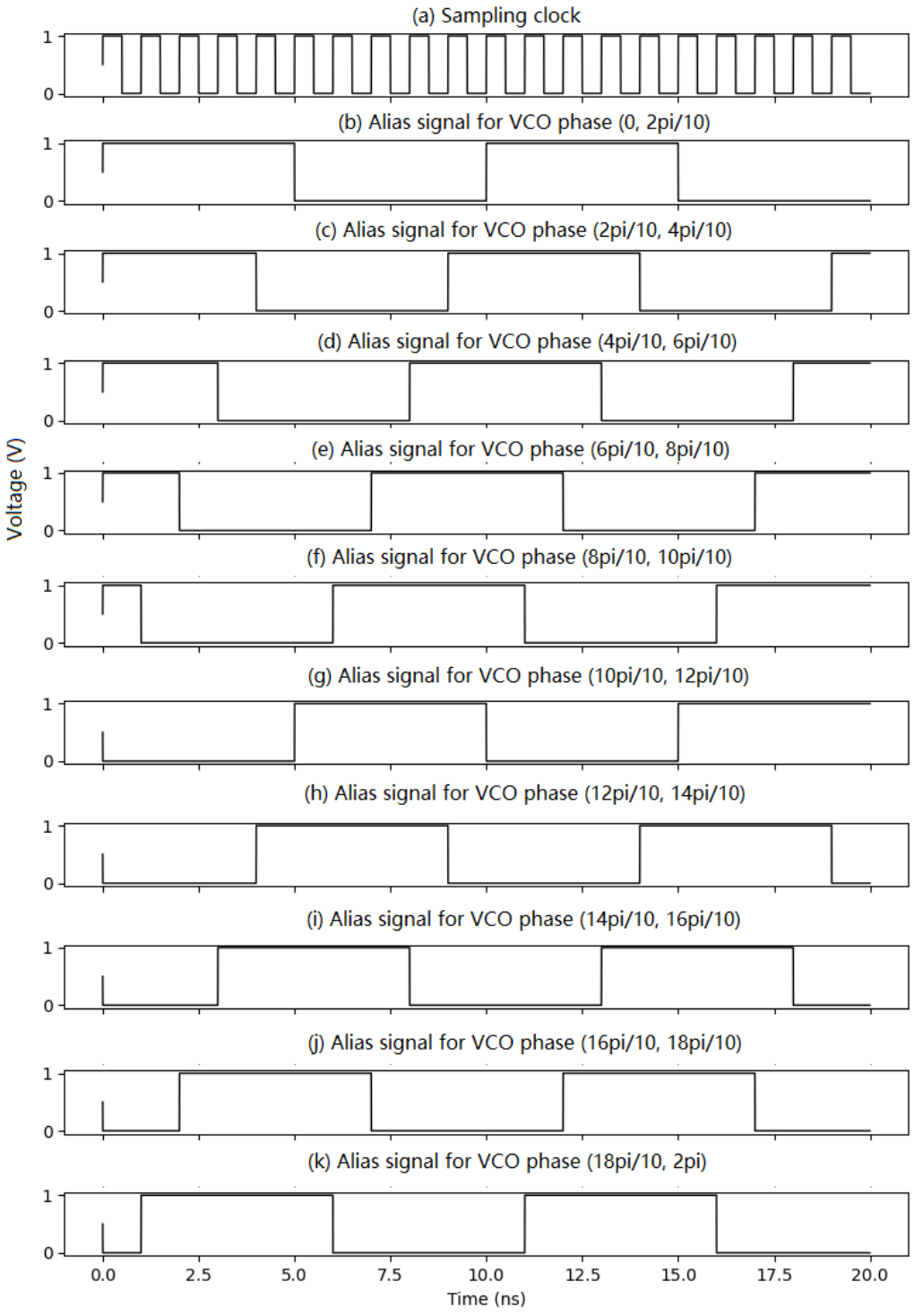


Figure 50: Digital alias signals corresponding to different VCO phases, with $f_{VCO} = 10.1$GHz, $f_S = 1$GHz and N=50. (a) 1GHz Sampling clock. Digital alias signals for VCO phases ranging (b) from 0 to π/5. (c) from π/5 to 2π/5. (d) from 2π/5 to 3π/5. (e) from 3π/5 to 4π/5. (f) from 4π/5 to π. (g) from π to 6π/5. (h) from 6π/5 to 7π/5. (i) from 7π/5 to 8π/5. (j) from 8π/5 to 9π/5. (k) from 9π/5 to 2π.

We define a dead zone to be an input region that the control system provides zero feedback when the input changes. As illustrated in Figure 51, the VCO phase interval (0, π/5) is a dead zone since the PFD output stays at zero and provides no feedback control as VCO phase changes within this region. Take a C-ALL as an example, when inside a dead zone for a VCO, both PFD inputs change at the sampling clock and thus can produce a tie which indicate neither up nor down signal from the charge pump. Additionally, we define the VCO phases 0, ±π/5, ±2π/5, ±3π/5, ±4π/5 and ±π to be quantization thresholds as the digital alias phase as well as the PFD output changes steeply when crossing these points. In next section we will see that these quantization thresholds play important roles to solve the dead zone related problems.

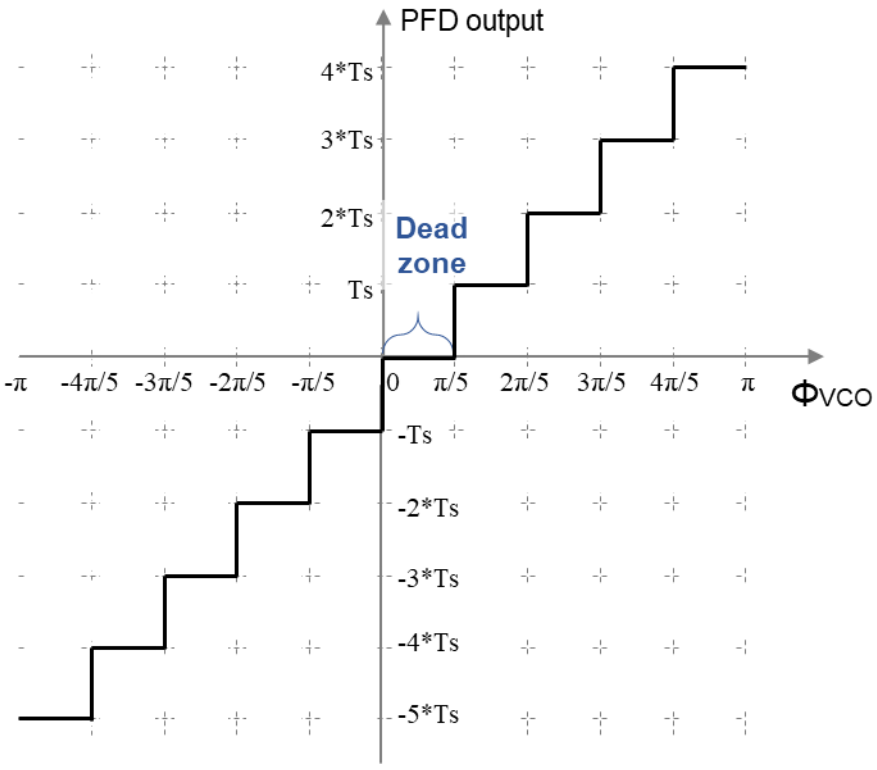


Figure 51: Phase relationship between the PFD output and the VCO phase of a C-ALL, with f_{VCO} = 10.1GHz and f_S = 1GHz. VCO phase region (0, π/5) is a dead zone since the loop has zero feedback when VCO phase changes.

6.2. Phase Shift C-ALL (PS-CALL)

In a C-ALL, based on the discussions above, the loop cannot effectively supress the phase error

or phase noise due to the dead zones. This has limited the applications of the circuit architecture. Here in this section, we will propose a different phase locking mechanism and corresponding circuit architecture to address these problems.

6.2.1. New locking mechanism

As discussed in Section 6.1, Figure 51 reflects the phase relationship of a C-ALL. In a C-ALL, when the VCO phase is smaller than 0, the PFD will provide constant feedback control (which is equal to charge pump current multiplied by the time duration of a sampling clock period) to increase the VCO phase until it is larger than 0; when the VCO phase is larger than 0, however, the PFD provides 0 feedback because of the dead zone and the VCO is therefore free-running until VCO phase is larger than π/5 or smaller than 0.

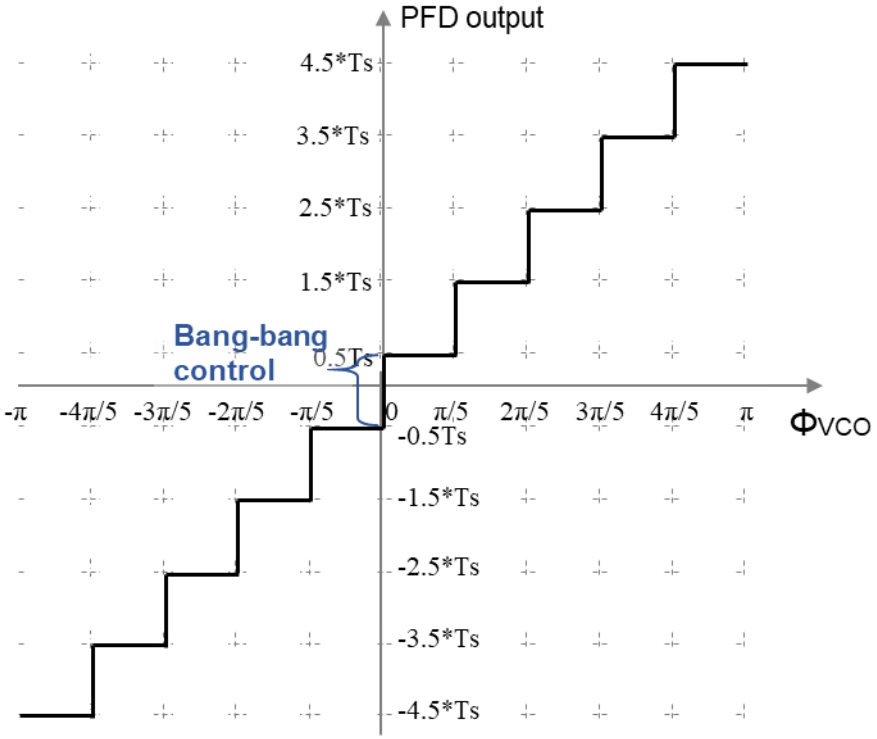


Figure 52: A new locking mechanism with phase relationship between the PFD output and the VCO phase. For VCO phases between –π and π, the relationship between the PFD output and the VCO phase is quantized linear. For VCO phases at or around 0, it has behavior similar to bang-bang control.

To achieve fine phase lock and effectively suppress phase noise, we need to lock the loop output

to some phases that the digital sampler can effectively sense and detect. As discussed in the previous section, a small change in VCO phase at or around the so-called quantization thresholds can lead to a large change in the phase of digital alias signal and therefore creates a PFD output with a duration of T_S, where T_S is the sampling clock period. Motivated by the bang-bang PLL which never achieves zero phase error at the PFD output, here we propose a new locking mechanism as illustrated in Figure 52. For VCO phases between $-\pi$ and π, the relationship between the PFD output and the VCO phase is quantized linear, which is the same as in Figure 51. For VCO phases at or around 0 (or any other quantization thresholds), however, the relationship is non-linear and provides bang-bang control between larger than and smaller than 0 (or any other quantization thresholds) in Figure 52. When the VCO phase is smaller than 0, the PFD will provide constant feedback control to increase the VCO phase until it is larger than 0, and when the VCO phase is larger than 0, the PFD will provide constant feedback control to decrease the VCO phase until it is smaller than 0. In this way, the loop keeps on toggling the VCO phase between larger and smaller than 0, which provides bang-bang behavior and achieves phase lock. This is the essential difference compared to a C-ALL, where there is a dead zone around 0 (or any other quantization thresholds) and no feedback controls are provided within these regions.

6.2.2. Circuit architecture of a PS-CALL

In order to implement the circuit architecture of the newly proposed locking mechanism, one possible way (as illustrated in Figure 53) is to use a different reference alias signal by observing that all the adjacent digital alias signals are shifted by one sampling clock period. For instance, if the reference alias signal can be shifted by half of the sampling clock period, then the digital alias signal will always be lead or lag compared to the reference alias signal, which therefore provides bang-bang control of the loop.

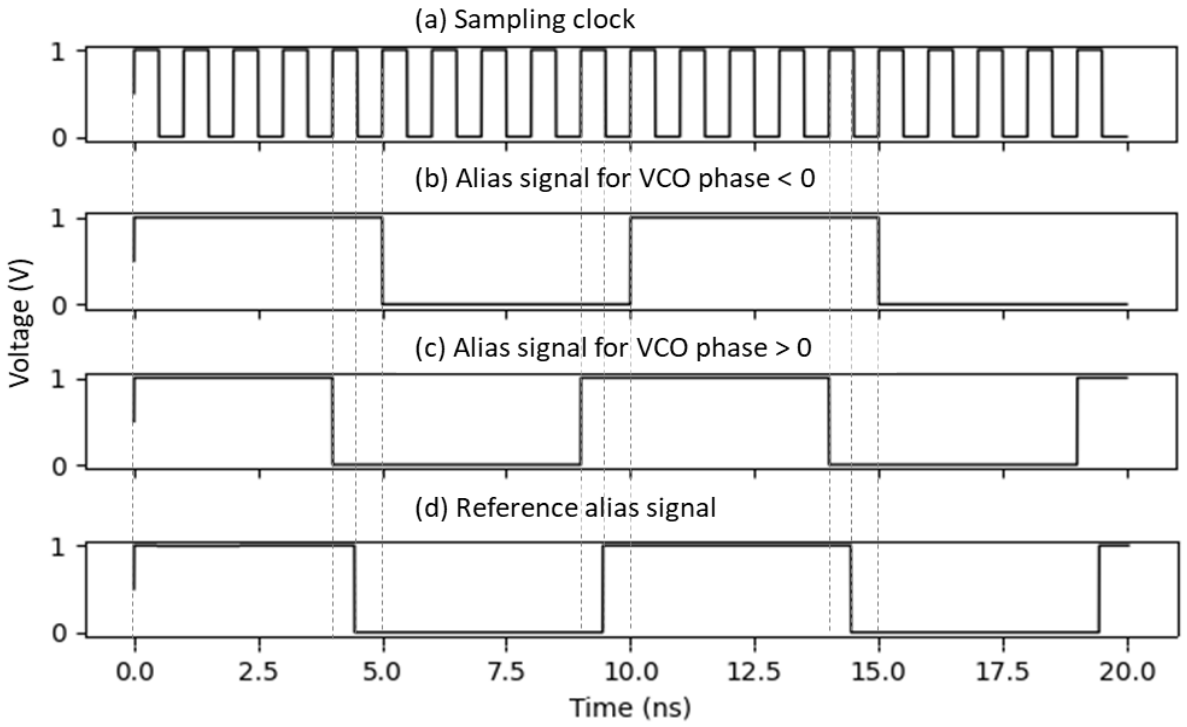


Figure 53: Timing diagram of the proposed PS-CALL (a) Sampling clock. (b) Alias signal for VCO phase < 0. (c) Alias signal for VCO phase > 0. (d) Generated reference alias signal which is shifted by half of the sampling clock period compared to the feedback alias signal.

Figure 53 shows the timing diagram of related signals for the proposed locking mechanism. Figure 53 (a) shows the sample clock, which is set to be 1 ns for simplicity of illustration purpose. Figure 53 (b) and Figure 53 (c) correspond to the alias signals for VCO phases smaller than 0 (or more exactly, smaller than 0 and larger than $-\pi/5$) and larger than 0 (or more exactly, larger than 0 and smaller than $\pi/5$) for a 100MHz alias signal, respectively. These two alias signals share the same signal pattern of 1's and 0's with a delay of 1 sampling clock period. If the reference alias signal, as illustrated in Figure 53 (d), is with the same pattern of 1's and 0's, but with an offset of half sampling clock period from the other two signals, then this reference alias signal can be used as the PFD input and be compared with the feedback alias signal. Similar to a bang-bang PLL, the VCO output will toggle between VCO phases smaller than 0 (as shown in Figure 53 (b)) and larger than 0 (as shown in Figure 53 (c)), which eventually achieve lock at 0. Since the loop and the timing diagram are still based on a C-ALL circuit architecture, and the phase of the reference alias signal has been shifted by half of the sampling period compared to in a C-ALL, this type of circuit architecture is called a Phase Shift C-ALL (PS-CALL).

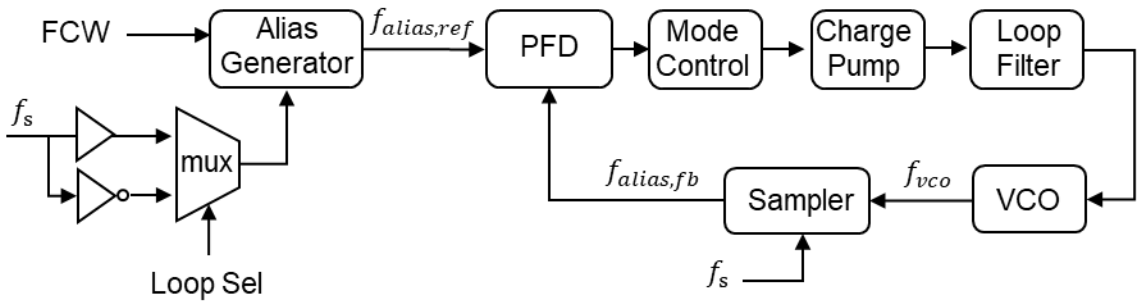


Figure 54: One circuit implementation of the PS-CALL. The only difference between a C-ALL and a PS-CALL is the clock of the Alias Generator. The loop is first configured as a C-ALL to pull in by using the sample clock as the clock of the Alias Generator, and then configured as a PS-CALL to achieve phase lock by using the inversion of the sample clock as the clock of the Alias Generator. Note that "FCW" means "Frequency Control Word" module.

The circuit block diagram can be illustrated as shown in Figure 54. Compared to a C-ALL as illustrated in Figure 41, the only difference is the digital clock of the Alias Generator. In a C-ALL, the clock of the Alias Generator is simply the sample clock, while in a PS-CALL the clock of the Alias Generator is the inversion of the sample clock. Normally we would use a C-ALL for pull-in, and a PS-CALL for phase lock. Therefore, the clock of the Alias Generator is multiplexed between the sample clock and the inversion of the sample clock as illustrated in Figure 54. During Phase I, the loop is configured as a normal C-ALL with the sample clock as the input of the Alias Generator. As discussed in Chapter 5, the C-ALL can pull into the targeting frequency region, and the reference alias signal are aligned in phase with the feedback alias signal when the loop achieves lock. In Phase II, the loop is configured as a PS-CALL with the inversion of the sample clock used as the input of the Alias Generator. Since the reference alias signal will be half of sampling clock offset as illustrated in Figure 53 (d), the PS-CALL is enabled to achieve phase lock through the bang-bang feedback control.

6.2.3. Simulation results

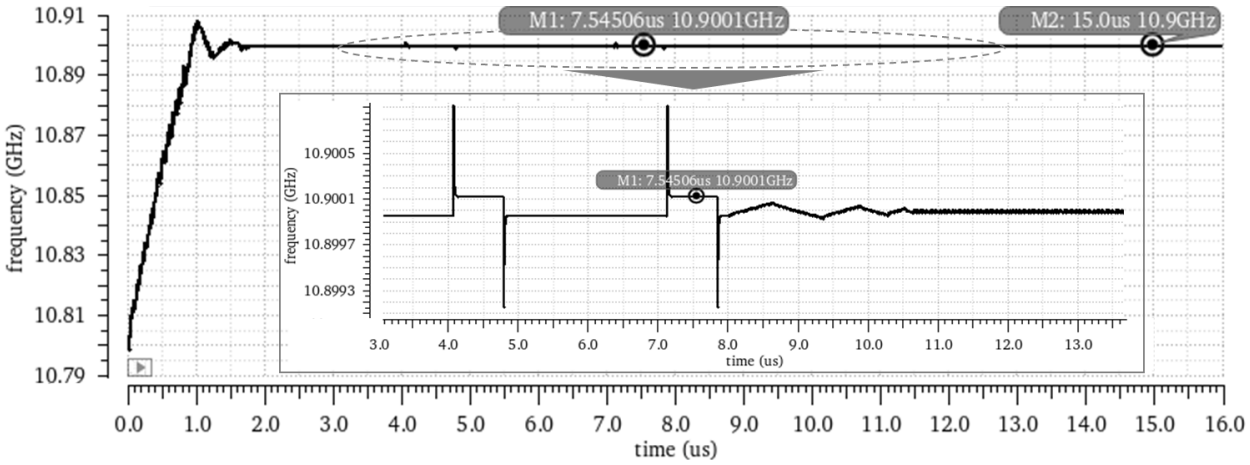


Figure 55: Spectre simulations verifying the proposed PS-CALL circuit architecture. "Loop Sel" is set to be 0 from 0-8 μs as Phase I, where the loop functions as a conventional C-ALL to pull in the desired frequency range. Then "Loop Sel" is set to be 1 from 8-16 μs as Phase II, where the PS-CALL is enabled to achieve phase lock at the targeting 10.9 GHz frequency.

Spectre circuit simulations validate the functionality of the PS-CALL. Behavior level model has been built using VerilogA with the following parameters: a VCO with a center frequency of 10.5 GHz and a gain of 1.0 GHz/V, a sample clock with a frequency of 1 GHz, a charge pump current of 200 μA at Phase I and 4 μA at Phase II, and a loop filter with a 50 Ω resistor, a 1 nF main capacitor and a 150 pF second capacitor. The two operating phases are controlled by the multiplexer and the corresponding control signal "Loop Sel" as illustrated in Figure 54. "Loop Sel" signal is set to be 0 from 0 μs to 8 μs as Phase I and be 1 from 8 μs to 16 μs as Phase II. Note that we intentionally extend the Phase I (C-ALL) time to be long to observe the dead zone and also to compare the frequency spectrum of C-ALL with PS-ALL. Alias Generator is set to generate a 100 MHz signal by change the Frequency Control Word (FCW). By correctly setting up the control mode of the "Mode Control" module, the loop is expected to synthesize a targeting frequency of 10.9 GHz. Figure 55 has illustrated the transient simulation results. It can be observed that the loop achieves certain range of frequency lock at Phase I, and locks to the targeting frequency of 10.9 GHz at Phase II.

To verify the loop performance in frequency domain, Fourier transform has been carried out to

analyze the output power spectrum in Phase I as a C-ALL and Phase II as a PS-CALL as shown in Figure 56. It can be observed that the noise level of at Phase II has been greatly reduced compared to Phase I. Take the largest spur of Figure 56 (b) as an example, the power spectrum is -126.5 dBc at 8.9 GHz for a PS-CALL, while the power spectrum is -109.3 dBc at 8.9 GHz for a C-ALL. The PS-CALL has suppressed the power spectrum of the largest spur by 16.2 dBc.

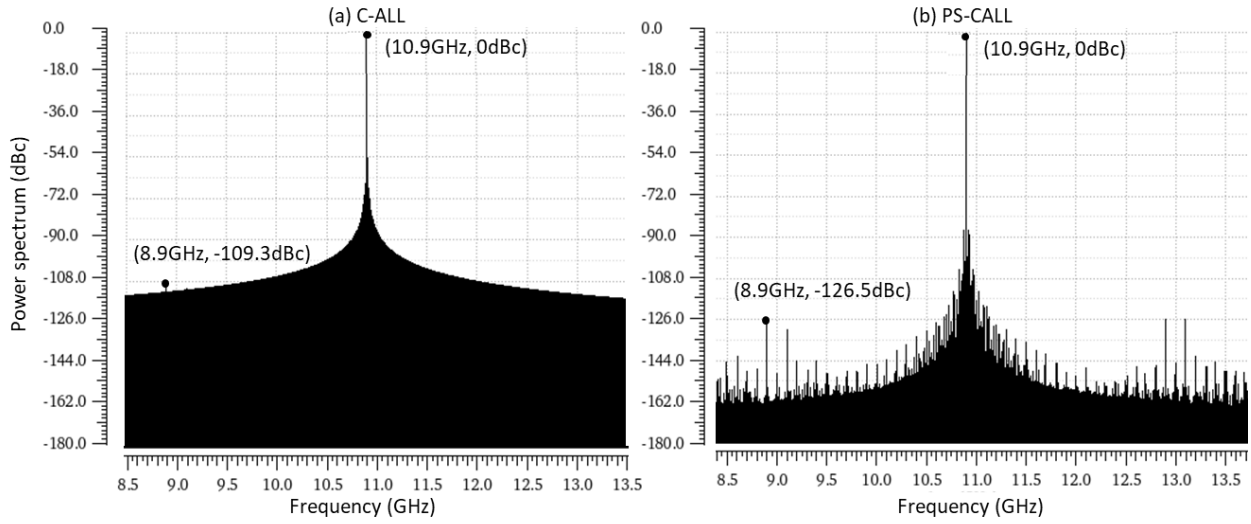
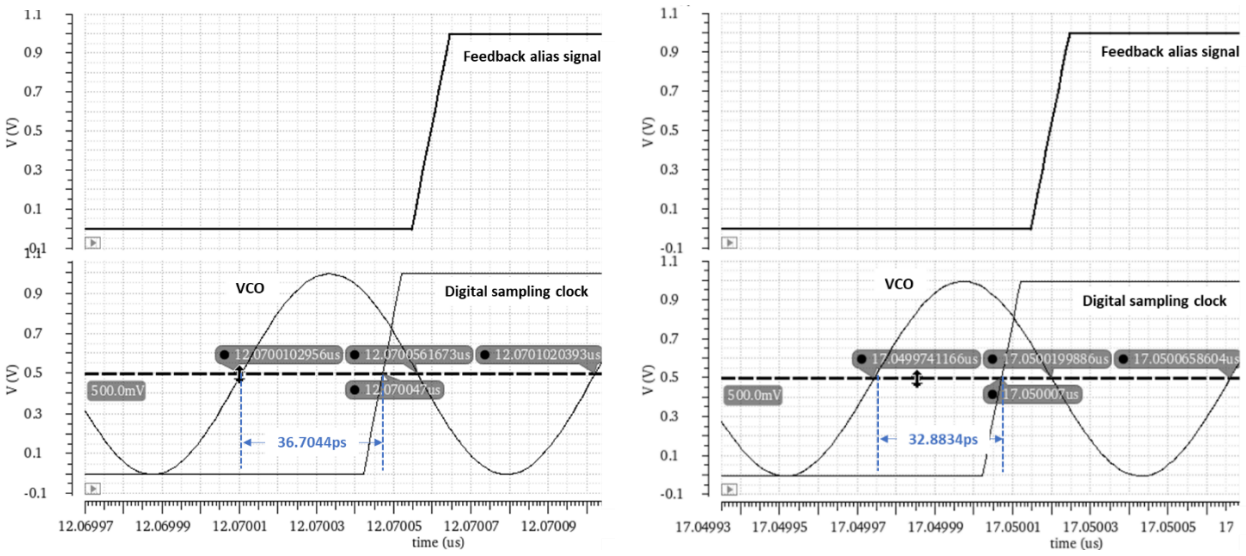


Figure 56: Power spectrum comparisons of C-ALL and PS-CALL simulations when in lock. (a) C-ALL in lock synthesizing the targeting 10.9 GHz output. (b) PS-CALL in lock synthesizing the targeting 10.9 GHz output, which greatly reduces the noise spectrum and the largest spur level by 16.2 dB.

To demonstrate that the PS-CALL achieves phase lock, in simulations, we change the sample clock and observe the phase of the VCO clock change to match it. If a loop achieves phase lock, then the phase relationship between the synthesized VCO output and the sampling clock should be fixed. Based on this observation, assuming at some point a loop achieves lock, and the relationship between the VCO and the sampling clock is φ_1, then an abrupt phase perturbation (i.e. a fixed delay) is added to the sampling clock. The loop will be out of lock and then gradually go back to lock. Assume the relationship between the VCO output in lock and the perturbed sample clock is φ_2, then we should have $\varphi_2 = \varphi_1$ if a loop achieves phase lock or otherwise $\varphi_2 \neq \varphi_1$ if not phase lock. Still take the 10.9 GHz targeting frequency and 1 GHz sample clock as an example, since the period is around 100 ps, a delay of 40 ps is applied to the sample clock as an abrupt phase perturbation to clearly verify the results.



(a) **(b)**

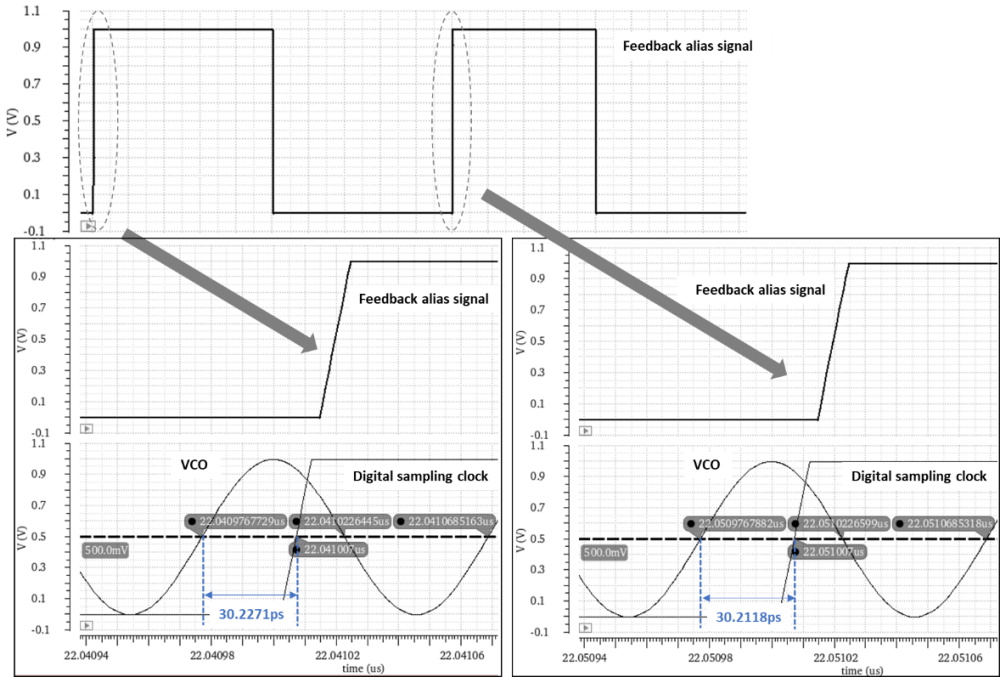
Figure 57: C-ALL phase relationship before and after sample clock perturbation. (a) Phase relationship between VCO and sample clock before sample clock perturbation. (b) Phase relationship between VCO and sample clock after a 40 ps perturbation in the sample clock.

For a C-ALL, Figure 57 has illustrated the phase relationships between the sample clock and the VCO before and after perturbing the sample clock. When there is a rising edge of the digital alias signal, assume φ_{delay} represents the phase delay between the rising edge of VCO signal and rising edge of digital sample clock that result in this rising edge of alias signal. By comparing phase relationships between the VCO and the sample clock before and after perturbation, we can see that the phase relationship changes by 3.882 ps (= $\left|\varphi_{delay,w/o\ pert} - \varphi_{delay,with\ pert}\right|$, where $\varphi_{delay,w/o\ pert} = 36.7044$ ps and $\varphi_{delay,with\ pert} = 32.8824$ ps represent the phase relationship before and after perturbation, respectively). If compared with the VCO output period, the phase change will be $\left|\varphi_{delay,w/o\ pert} - \varphi_{delay,with\ pert}\right|/T_{VCO}$ = 4.17% for the alias signal rising edge. This means that the same phase relationship between the VCO and the sample clock does not hold before and after the sample clock phase perturbation, which further means a C-ALL only achieves coarse phase lock within the bounds of the dead zone and cannot effectively suppress phase noise. The PS-CALL, however as shown below, achieves fine phase lock and holds the same phase relationship between the VCO signal and sample clock before and after perturbation.

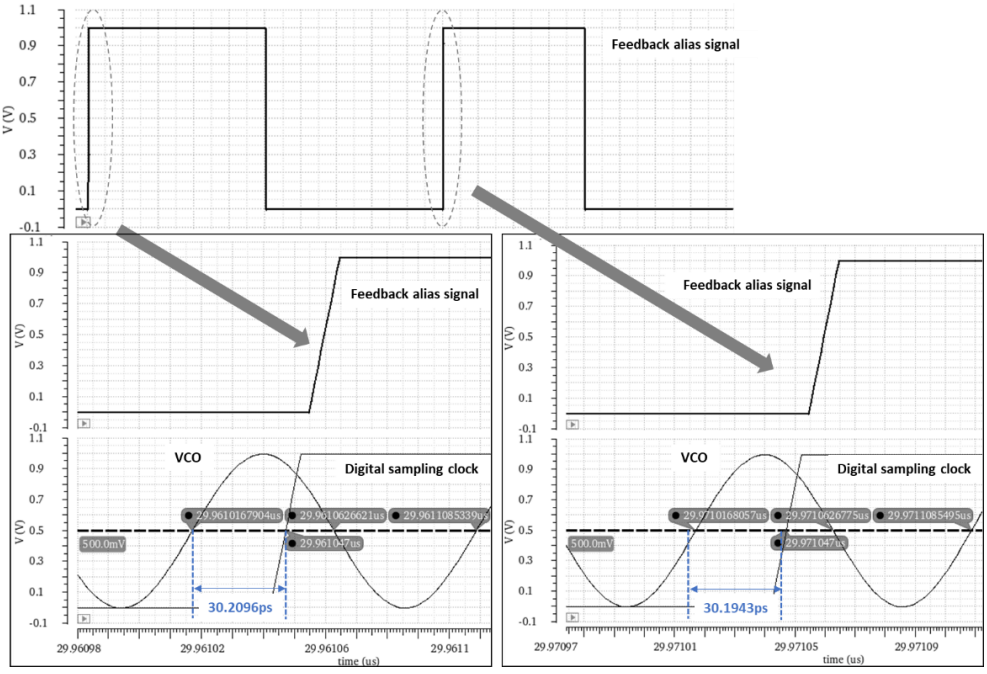
While a C-ALL has the limitation of only achieving coarse phase lock, a PS-CALL has the benefit of fine phase lock as discussed below. For a PS-CALL, Figure 58 has illustrated the phase relationships between the sample clock and the VCO before and after sample clock perturbation. It should be noted that the phase toggles between lead and lag when in lock because of the bang-bang control. By comparing phase relationships between the VCO and the sample clock before and after perturbation, we can see that the phase relationship changes by 17.5 fs (= $\left|\varphi_{delay,lead,w/o\ pert} - \varphi_{delay,lead,with\ pert}\right|$, where $\varphi_{delay,lead,w/o\ pert} = 30.2271$ ps and $\varphi_{delay,lag,with\ pert} = 30.2096$ ps represent the phase relationship for the lead phase before and after perturbation, respectively) and 17.5 fs (= $\left|\varphi_{delay,lag,w/o\ pert} - \varphi_{delay,lag,with\ pert}\right|$, where $\varphi_{delay,lag,w/o\ pert} = 30.2118$ ps and $\varphi_{delay,lag,with\ pert} = 30.1943$ ps represent the phase relationship for the lag phase before and after perturbation, respectively) for the two bang-bang alias signal rising edges, respectively. If compared with the VCO output period, the phase change will be $(\left|\varphi_{delay,lead,\frac{w}{o}pert} - \varphi_{delay,lead,with\ pert}\right| + \left|\varphi_{delay,lag,w/o\ pert} - \varphi_{delay,lag,with\ pert}\right|)/2*T_{VCO}$ = 0.019% for the alias signal rising edges. This means that the same phase relationship between the VCO and the sample clock holds when the PS-CALL achieves lock again after a phase perturbation, which further indicates that a PS-CALL does achieve phase lock and tracks phase changes of the sample clock which provides the reference. Additional analysis with 20 consecutive periods of before & after perturbation of analysis shows a standard deviation of 305 fs, or 0.33% compared to the period of the 10.9 GHz signal, which further verifies the phase lock of the PS-CALL.

6.2.4. Further discussions

In this section, we are going to discuss an improved circuit implementation of a PS-CALL. As an example, Figure 54 has illustrated one possible circuit implementation of a PS-CALL, where a C-ALL is firstly used to pull in the targeting frequency range and then a PS-CALL is enabled to achieve phase lock. As illustrated in Figure 52, the relationship between the PFD output and the VCO phase is quantized linear for VCO phases between –π and π, which is the same as a C-ALL. This means that a PS-CALL itself can not only be used for phase lock but also to pull in the targeting frequency range similar as a C-ALL. The circuit implementation is shown in Figure 59.



(a)



(b)

Figure 58: PS-CALL phase relationship before and after sample clock perturbation. (a) Phase relationship between VCO and sample clock before perturbing the sample clock. (b) Phase relationship between VCO and sample clock after a 40 ps perturbation in the sample clock.

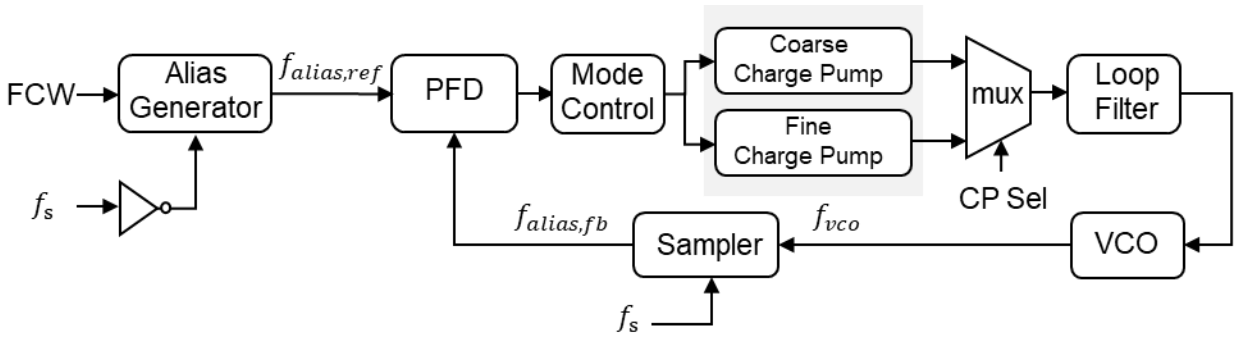


Figure 59: Another circuit implementation of the PS-CALL, where "FCW" represents the frequency control word. The same loop is used for both coarse tuning during pull in with a large charge pump current and fine tuning during phase lock with a small charge pump current.

Following the same simulation setup as Figure 59, we have verified the functionality of a PS-CALL using Spectre transient simulation as illustrated in Figure 60. The same loop is used for frequency synthesis with a charge pump current of 200 µA from 0 µs to 5 µs and 4 µA from 5 µs to 9 µs. We can observe from the simulation results that the PS-CALL can be used for both pull in and phase lock.

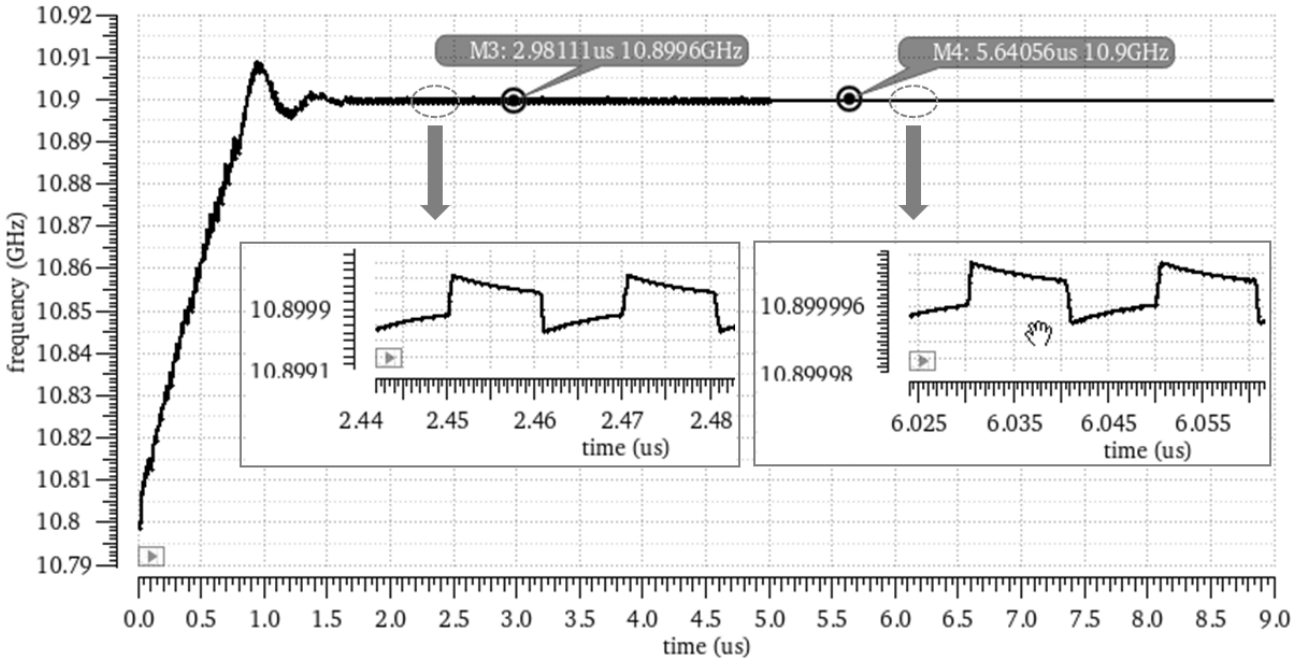


Figure 60: Transient simulation results of the PS-CALL circuit proposed in Figure 59, showing a coarse charge pump setting useful for pull-in and a fine charge pump setting useful for lock. Using the coarse charge pump setting of 200 µA (simulated from 0 µs to 5 µs), phase lock is quickly achieved at 10.9 GHz ±400 KHz.

Using the fine charge pump setting of 4 µA (simulated above from 5 µs to 9 µs) phase lock is maintained with less error at 10.9 GHz ± 7 KHz.

6.3. Summary

In a C-ALL, digital sampling leads to quantization and ties, which in turn result in discontinuities and dead zones respectively in the phase transfer function. In this chapter, a new type of circuit architecture, named as Phase Shift Coresidual Alias-Locked Loop (PS-CALL), has been proposed to implement a new locking mechanism, in which a quantized linear control in wide phase range and bang-bang control in the fine phase range to achieve phase lock. A PS-CALL inherently avoids the dead zone issue in a C-ALL. Circuit implementations have been discussed and simulations have been carried out to verify the functions of the loop. Simulations have shown that a PS-CALL can not only achieve phase lock but also reduce the spur level by 16.2 dB compared to a normal C-ALL.

CHAPTER 7. Differential Alias-Locked Loop

Existing Alias-Locked Loops (ALLs) use digital samplers in the feedback path to achieve a wide frequency lock range for high-speed frequency synthesis, at the cost of one additional reference clock, compared to a Phase-Locked Loop (PLL). In this paper, we propose the differential alias-locked loop (D-ALL) circuit architecture which uses only one reference clock input. In this D-ALL synthesizer architecture, two frequencies are derived from the voltage-controlled oscillator (VCO) output and are compared as the two inputs to the phase frequency detector (PFD). In contrast, a PLL or an ALL has a reference clock as one PFD input and a frequency derived from the VCO output as the other PFD input. Additionally, finer tuning of sampling clock division ratios allows wider frequency acquisition range, better phase noise performance, and more design freedom in choosing loop bandwidth compared to [93]. Phase domain models show that a D-ALL avoids the N^2 times multiplications of the phase noise from the charge pump (CP) and the PFD, that is present in a conventional integer-N or fractional-N PLL. Spectre circuit simulations verify that the proposed design achieves lock at multiple programmable frequencies in the range of 21–23.3 GHz.

7.1. Introduction

Phase-Locked Loops (PLLs) play an important role in modern integrated circuits (ICs) such as frequency synthesis. In an integer-N PLL, the frequency resolution, or the synthesized frequency channel spacing, is equal to the reference frequency. For applications with high frequency resolution requirement such as RF communications, an integer-N PLL usually means a large division ratio and/or a small reference frequency, which leads to limited loop bandwidth and larger phase noise from loop components (multiplied by N^2, where N is the division ratio) as demonstrated in [74]. To solve this problem, researchers proposed the fractional-N PLL architecture where a ΔΣ modulator is applied in the feedback path to shape the quantization noise [94][95][96]. Additionally, novel techniques such as fractional-N counters based on phase interpolator or phase-noise-filtering based on phase-domain averaging were proposed in [97][98].

This Chapter is based on a conference paper presented at ISCAS 2018 [93].

In order to build PLLs where the VCO frequency is higher than the maximum frequency of a counter, several techniques have been employed. Instead of using a divider to divide the high-frequency voltage-controlled oscillator (VCO) signal to low frequency, another solution is to use a mixer in the feedback path to down-convert the VCO signal before feeding into the PFD. For instance, a dual loop architecture was proposed with a single sideband (SSB) mixer [72][73] in the feedback path. Based on the observation that an analog sample-and-hold circuit is inherently a down conversion mixer [47], researchers have proposed another circuit architecture using an analog subsample-and-hold circuit in the feedback path [45]. In all of these abovementioned mixer-based solutions, additional filters are usually required to filter out the undesired tones and this increases the complexity, adds additional cost, and reduces frequency range. For instance, a 6th-order Butterworth low-pass filter is used in [45] to filter out the harmonics. In the dual-loop architecture, however, the unwanted sidebands or harmonics due to mismatches and non-linearities of the SSB mixer can be filtered out by the low-pass loop filter [72][73].

The alias-locked loop (ALL) circuit architecture, which uses a digital sampler in the feedback path, was proposed in [15]. Compared to all the analog mixers, a digital sampler can directly down-convert and digitize the VCO signal without the need for filters. We show, in simulation, that a digital sampler can directly sample the VCO signal at frequencies through 130 GHz in TSMC 40nm CMOS process, without using any injection-locked frequency dividers or mixers. An ALL has the advantages of wide frequency range of operation and cost-savings in design effort, at the cost of one extra reference clock compared to a conventional PLL. To solve this problem in an ALL, an improved circuit architecture we call the coresidual alias-locked loop (C-ALL) was proposed in [63]. In a C-ALL, the desired reference signal is generated by digital circuit modules clocked by the sampling clock instead of directly provided by an external reference clock. In this paper, another novel circuit architecture named the differential alias-locked loop (D-ALL) is proposed that also saves the second reference clock required by an ALL.

In this chapter, we review the ALL architecture in Section 7.2, propose the D-ALL architecture in Section 7.3, discuss several key issues including frequency acquisition and loop bandwidth in a D-ALL in Section 7.4, and present the simulation results in Section 7.5.

7.2. Review of Alias-Locked Loops

In a traditional PLL, the divider is usually the only module that runs the same high frequency as the VCO. Design of a divider can be challenging for high frequencies and the area cost can be large. One common example is an LC-based injection-locked frequency divider. The passive inductor usually takes a large silicon area. To solve this problem, the ALL was proposed to use a digital sampler to replace the divider in a PLL. The sampler is clocked by a sampling clock whose frequency is much lower than the VCO frequency. The VCO signal will be subsampled and an alias frequency is therefore created. In this way the high frequency of the VCO signal is converted to the lower frequency of the alias signal, which in turn can be fed into a CMOS static divider or directly to a conventional PFD. One advantage of a sampler over a divider is that the sampler simultaneously allows a high operation frequency and a wide frequency range. A non-obvious advantage of the sampling latch is that it must make a sampling "decision" at the sampling clock rate, which is usually much lower than the VCO rate. This is different from a divider which is always clocking at the VCO rate. A regenerative sampling circuit (including essentially all static latches) has unlimited DC gain (but finite input-referred noise) for discriminating between a 1 or 0 on the analog VCO output. The ALL and D-ALL architectures are robust in the presence of fixed input offset error and delay (even a delay of multiple sampling clock periods). Our preferred digital samplers are differential current mode logic (CML) latches and CMOS differential sense amplifier latches [16].

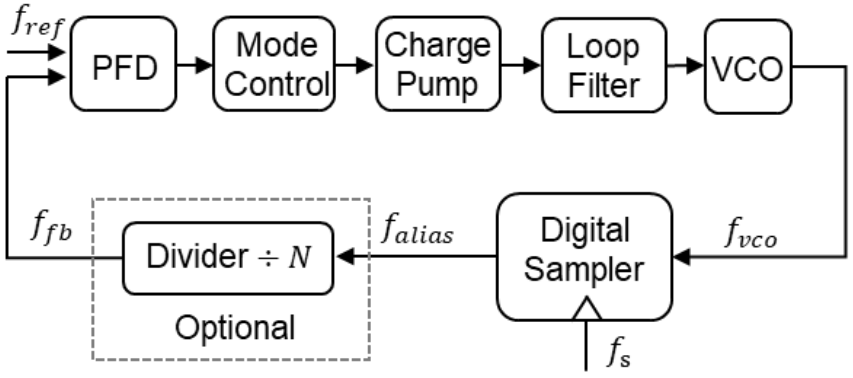


Figure 61: An Alias-Locked Loop (ALL) architecture. The divider is optional and the division ratio is assumed to be 1 in further mathematical calculation unless otherwise specified. Noting that $f_{vco} = Kf_s + f_{alias}$, where K is the subsampling ratio [16].

Figure 61 shows a general block diagram of an ALL. Observe that most of the modules in an ALL are the same as in a PLL. The phase/frequency information of the reference clock and the feedback signal is compared in the PFD. The generated phase difference of the PFD is converted to current charging and discharging operation of the CP, and therefore controls the voltage of the capacitor in the loop filter (LF) and eventually adjusts the tuning voltage of the VCO. Different from a traditional PLL where a traditional divider is applied in the feedback path, a digital sampler, which uses a stable clock to sample the VCO signal, is utilized to convert the high frequency VCO signal to lower frequency in an ALL. As mentioned above and also in [16], there could be various circuit implementations of the digital sampler, including a sense-amplifier style differential latch or a CML latch. An optional divider can be applied after the sampler to provide additional programmability or to further lower the feedback signal frequency. The frequency difference at the PFD could respond positively or negatively to an increase in the VCO frequency. The mode-control block can selectively invert the sense of the PFD output and is used to keep the feedback loop gain negative [16].

As shown in Figure 61, an ALL requires two clocks with one as the reference clock (same usage as a PLL) and the other as the sampling clock which leads to extra cost. By using differential phase detection, the need for the second clock is eliminated as we will describe.

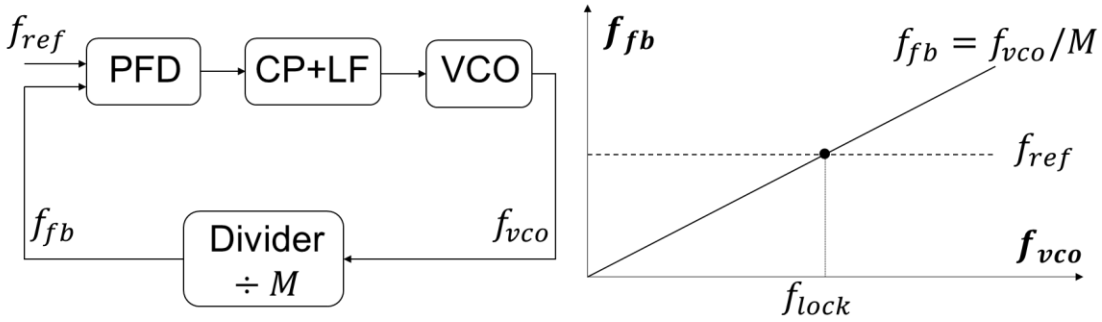
7.3. Differential Alias-Locked Loops

7.3.1. Locking Mechanisms Comparison

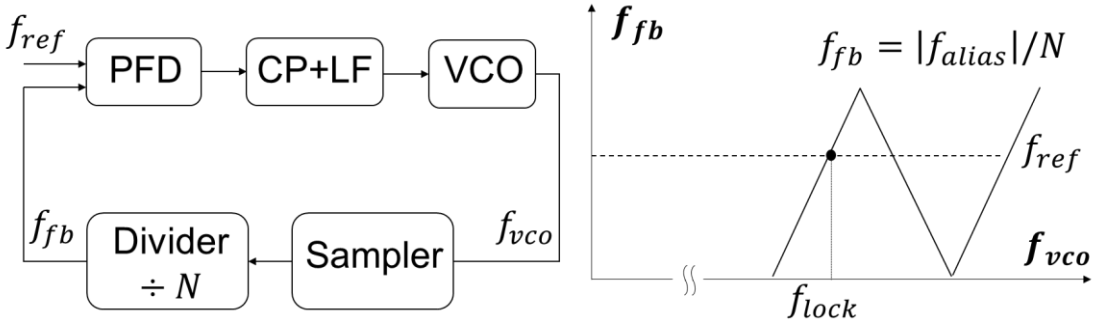
In a PLL or an ALL, the feedback signal is compared with the fixed reference clock in phase domain. In this section, locking mechanisms of PLLs and ALLs will be discussed, and a new different locking mechanism will be proposed.

The feedback signal in a PLL is a divided VCO signal, while the feedback signal in an ALL is the alias signal generated from down-conversion or digital sampling of the VCO. When the feedback signals are equivalent to the fixed reference signal in both frequency and phase, the loops achieve lock and the targeting frequencies are synthesized as shown in Figure 62 (a) (b). Within a certain frequency range, the frequency and phase of the feedback signal can be treated as a linear function of the VCO frequency and phase. The slope of this linear function within a

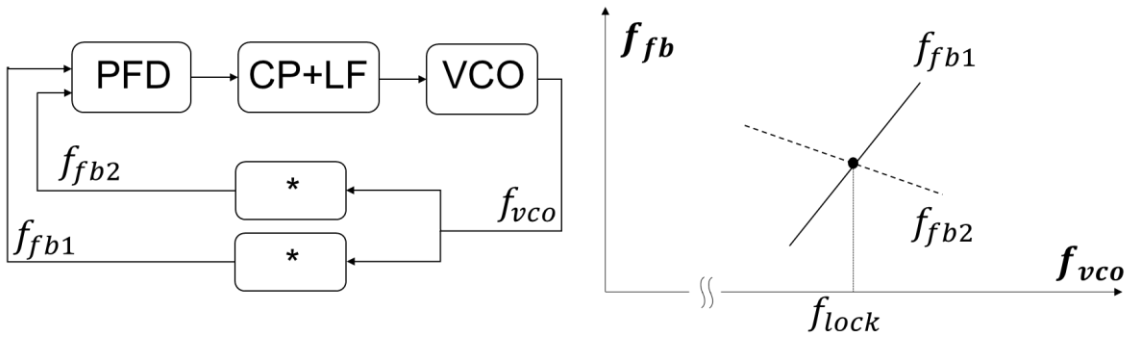
PLL is $1/M$, where M is the division ratio of the feedback divider of a PLL, while the slope of this linear function within an ALL is $\pm 1/N$, where N is the division ratio of the feedback divider between the sampler and the PFD. Because of the inherent property of digital aliasing, multiple VCO frequencies map to the same alias frequency in an ALL. This disambiguation of an ALL can be resolved by multiple methods. One possible solution is to use a digital-to-analog converter (DAC) fed from a lookup table to initialize the CP. Another solution is to use two different sampling frequencies to produce two corresponding alias frequencies to uniquely determine the targeting frequency [16].



(a): Locking mechanism of a PLL, with a divided VCO signal $f_{fb} = f_{vco}/M$ and a fixed reference f_{ref} feeding into a PFD. 'M' is the division ratio of the feedback divider. When a PLL achieves lock, $f_{fb} = f_{ref}$, and the VCO frequency $f_{lock} = Mf_{ref}$ is the desired synthesized frequency.



(b): Locking mechanism of an ALL, with a subsampled VCO signal $f_{fb} = f_{alias}/N$ and a fixed reference f_{ref} feeding into a PFD. 'N' is the division ratio of the feedback divider. When an ALL achieves lock, $f_{fb} = f_{ref}$, and the VCO frequency $f_{lock} = Kf_S + Nf_{ref}$ is the desired synthesized frequency, where f_S is the sampling frequency and K can be any non-negative integer.



(c): The proposed locking mechanism, where two feedback signals f_{fb1} and f_{fb2} are fed into a PFD. Both the two feedback signal frequencies f_{fb1} and f_{fb2} are certain functions (represented by the two '*' blocks) of the VCO frequency f_{vco}. If the two functions are linear and with different slopes, then the loop can achieve lock at a certain VCO frequency that satisfies $f_{fb1} = f_{fb2}$, and the VCO frequency f_{lock} is the desired synthesized frequency.

Figure 62: Locking mechanisms of (a) a PLL, (b) an ALL and (c) the proposed loop [93].

Instead of comparing a feedback signal with a fixed reference signal, we propose to use two function blocks (represented by the two '*' blocks in Figure 62 (c)) to generate two feedback signals with different slopes. By feeding the two feedback signals into a PFD and comparing the phase information with each other, a negative feedback of the loop is ensured and the loop can therefore be applied to synthesize targeting frequencies as illustrated in Figure 62 (c). It should be mentioned that although a positive slope and a negative slope are illustrated in Figure 62 (c), any two unequal slopes (i.e. two unequal positive slopes, two unequal negative slopes, or one positive slope and one negative slope) could be used to achieve lock. In the following sections, the feedback functional blocks represented by '*' will be discussed and one possible implementation will be proposed and demonstrated.

7.3.2. Mathematical Preparations

Assuming a target VCO frequency $f_{vco} = Rf_S$ is to be synthesized, where R is an arbitrary positive rational number and f_S is the sampling clock frequency. R can always be represented by the sum of a non-negative integer K and a non-negative proper fraction s; therefore we have,

$$R = K + s. \tag{7.1}$$

It is easy to prove that there must exist a non-negative integer k_1 that can satisfy:

$$1-\frac{1}{2^{k_1}} \le s < 1-\frac{1}{2^{k_1+1}}. \tag{7.2}$$

Actually, if Equation (7.2) is not true, then for all the non-negative integers k_1, the following expression is correct:

$$s < 1-\frac{1}{2^{k_1}} \text{ or } s \ge 1-\frac{1}{2^{k_1+1}}. \tag{7.3}$$

Take $k_1 = 0$ for example, then we can obtain

$$s < 0 \text{ or } s \ge \frac{1}{2}. \tag{7.4}$$

Apparently $s = \frac{1}{4}$ doesn't satisfy Equation (7.4), which proves the correctness of Equation (7.2).

Similarly, we can prove that there must exist a non-negative integer k_2 that can satisfy

$$\frac{1}{2^{k_2+1}} < s \le \frac{1}{2^{k_2}}. \tag{7.5}$$

It should be noted that s cannot be zero in Equation (7.5).

Given the VCO frequency is f_{vco} and the sampling frequency is f_s, let $f_{vco}/f_s = R$; then with Equations (7.1) and (7.2), there exists a non-negative integer k_1 that satisfies

$$\left(1-\frac{1}{2^{k_1}}\right) f_s \le f_{vco} - Kf_s < \left(1-\frac{1}{2^{k_1+1}}\right) f_s. \tag{7.6}$$

With simple algebraic manipulation, Equation (7.6) can be transformed to the following expression:

$$(2^{k_1}(K+1)-1)\frac{f_s}{2^{k_1}} \le f_{vco} < (2^{k_1}(K+1)-1)\frac{f_s}{2^{k_1}} + \frac{1}{2}\frac{f_s}{2^{k_1}}. \tag{7.7}$$

From Equation (7.7), if a sampling frequency $f_s/2^{k_1}$ is used instead of f_s, then the generated alias frequency is non-negative.

There must exist an integer D_1 that is no larger than 2^{k_1} that can satisfy the following relationship:

$$(D_1(K+1)-1)\frac{f_s}{D_1} \le f_{vco} < (D_1(K+1)-1)\frac{f_s}{D_1} + \frac{1}{2}\frac{f_s}{D_1}. \tag{7.8}$$

Similarly, from Equations (7.1) and (7.5), there must exist a non-negative integer k_2 that can satisfy

$$(2^{k_2}K+1)\frac{f_s}{2^{k_2}} - \frac{1}{2}\frac{f_s}{2^{k_2}} < f_{vco} \le (2^{k_2}K+1)\frac{f_s}{2^{k_2}}. \tag{7.9}$$

From Equation (7.9), if a sampling frequency $f_s/2^{k_2}$ is used instead of f_s, then the generated alias frequency is non-positive.

There must exist another integer D_2 that is no larger than 2^{k_2} that can satisfy the following relationship:

$$(D_2K+1)\frac{f_s}{D_2} - \frac{1}{2}\frac{f_s}{D_2} < f_{vco} \le (D_2K+1)\frac{f_s}{D_2}. \tag{7.10}$$

If two derived frequencies intersect at a VCO frequency, then these can be used to control a negative feedback loop. As we will show in Section 7.3.3, for the alias frequencies we are generating, such intersections will only occur if one alias frequency is positive and one alias frequency is negative. Note that we define the alias frequency to be negative when the alias frequency decreases as the VCO frequency increases. Since these numbers such as 2^{k_1}, 2^{k_2}, D_1, and D_2, are used to determine the division ratios of the sampling clocks, they are named sampling clock division ratios.

7.3.3. Differential Alias-Locked Loops

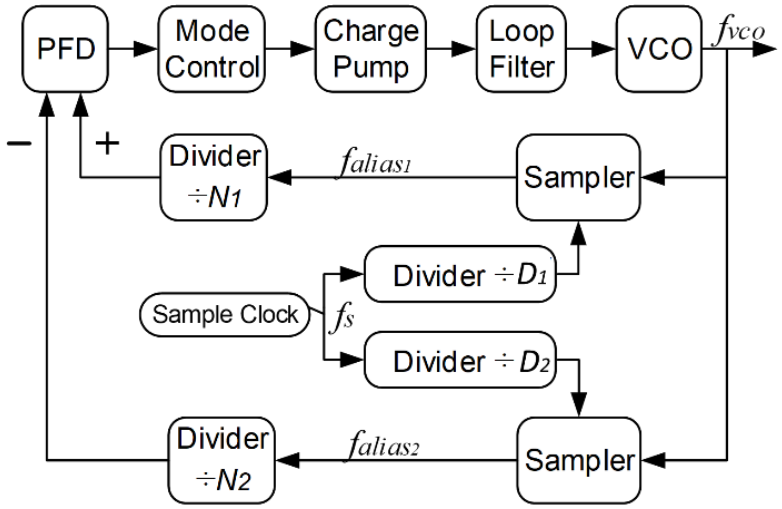


Figure 63: The proposed D-ALL architecture. Instead of using only one sampler in an ALL, a D-ALL has two sampling paths and the generated alias frequencies are fed in a PFD. One of the two alias frequencies must be negative while the other must be positive.

For a targeted VCO frequency f_{vco}, by properly selecting the sampling clock division ratios (D_1 and D_2), two different alias frequencies, with one positive and the other negative, can be generated simultaneously with two samplers from Section 7.3.2. Based on the observation in Section 7.3.1 and the locking mechanism proposed in Figure 62 (c), a PFD can be applied to compare the phase information of the two divided alias signals and eventually bring the loop into lock. Since the two divided alias signals feeding into the PFD are equal in absolute frequency (aligned in phase), but opposite in polarity when in lock, this architecture is named a differential alias-locked loop (D-ALL). One possible implementation of a D-ALL is illustrated in Figure 63.

// f_{alias1} is the alias signal frequency of the 1st sampler that is sampling the VCO signal
// f_{alias2} is the alias signal frequency of the 2nd sampler that is sampling the VCO signal
// f_{vco} is the targeted VCO signal frequency

D_1 = 1; // Fix D_1 to be 1, and calculate f_{alias1}
D_2 = 2;
While (f_{alias1}*f_{alias2}>=0)
    D_2 = D_2 + 1;
// Adjust D_2, until f_{alias1}*f_{alias2}<0.

$f_x = \mathrm{GCD}(|f_{alias1}|, |f_{alias2}|)$;
//GCD is the greatest common divisor function.
$N_1 = \left|\frac{f_{alias1}}{f_x}\right|$; $N_2 = \left|\frac{f_{alias2}}{f_x}\right|$;

If (Feedback polarity is positive)
$X_{\mathrm{mode\_control}}$ = NOT ($X_{\mathrm{mode\_control}}$);
// Adjust loop polarity to ensure loop negative feedback.

Figure 64: Pseudo code for choosing parameters of a D-ALL.

Similar to the function of an ALL architecture, a change in the VCO frequency could cause a change in sign of the digital alias frequency, and therefore the loop feedback could switch from negative to positive. The mode-control module, which is usually implemented with multiplexers, can selectively invert the sense of the PFD output as needed to ensure the loop negative feedback over the whole range of D-ALL frequencies of operation. Therefore, a D-ALL will be functional only with the correct selection of:

1) Sampling clock division ratios of D_1 and D_2;

2) Alias divider ratios of N_1 and N_2;

3) Loop polarity by controlling the mode-control module.

The design procedures can be summarized as follows in Figure 64.

Take, for example, a targeted frequency of $f_{vco} = 21.8$ GHz and a sampling frequency of $f_s = 1$ GHz:

1) First set D_1 = 1, and use $f_s = 1$ GHz directly as the first sampling clock; thus the targeting alias frequency is $f_{alias1} = -200$ MHz;

2) Starting from 2, keep increasing D_2 by 1 each time, until $f_{alias2} > 0$. In this example, when $D_2 = 2$, we have $f_{s2} = 0.5$ GHz and $f_{alias2} = -200$ MHz which cannot satisfy the

relationship; when $D_2 = 3$, we have $f_{s2} = 0.333$ GHz and $f_{alias2} = +133$ MHz which can satisfy the relationship;

3) By choosing $N_1 = 3$ and $N_2 = 2$, the relationship of $\left|\frac{f_{alias1}}{N_1}\right| = \left|\frac{f_{alias2}}{N_2}\right|$ can be satisfied;

4) Determine the value of $X_{\text{mode\_control}}$ by examining the loop polarity.

7.3.4. Improved architecture of a D-ALL

One potential issue in Figure 63 is the need for two separate digital samplers, which will possibly lead to different outputs when sample the same VCO signal when this signal is near the zero crossing, resulting in erroneous phase differences as seen at the PFD. An improved circuit architecture, which uses only one common sampler to provide consistent decisions, is proposed in this subsection.

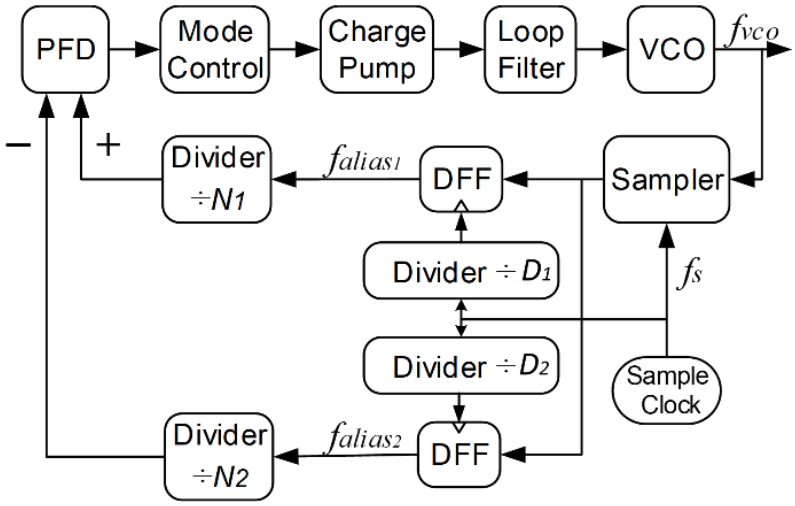


Figure 65: The implementation of a D-ALL. Only one digital sampler clocking at f_s is required instead of two samplers shown in Figure 63. The two signals f_{alias1} and f_{alias2}, are generated by re-sampling of f_{alias} with two D flip-flops (DFFs) clocking at $\frac{f_s}{D_1}$ and $\frac{f_s}{D_2}$, respectively. This implementation is equivalent to that shown in Figure 63 but with only one digital sampler.

Figure 65 presents one possible implementation that only uses one digital sampler clocking at f_s to generate the digital alias signal with a frequency of f_{alias}. By using two additional DFFs

clocked at $\frac{f_S}{D_1}$ and $\frac{f_S}{D_2}$ to resample the digital alias signal respectively, the two differential signals f_{alias1} and f_{alias2} are therefore generated.

The architecture shown in Figure 65 is mathematically equivalent to that shown in Figure 63, but with the advantage of using only one high-speed digital sampler instead of two, and therefore can save area, power consumption, and matching requirements. The digital sampler, as mentioned earlier, can be implemented with a sense-amplifier style differential latch or a CML latch, which can save silicon area compared to an LC-oscillator-based injection locked frequency divider in a conventional high-frequency PLL [21].

In [93], we showed that sampling clock division ratios could be powers of 2, i.e. 2^{k_1}, 2^{k_2} and lock can be achieved. Again, take a targeted frequency of $f_{vco} = 21.8$ GHz and a sampling frequency of $f_s = 1$ GHz as an example, the proposed architecture as shown in Figure 63 allows lower sampling clock division ratios of $D_1 = 1$ and $D_2 = 3$, compared to sampling clock division ratios of $2^{k_1} = 1$ and $2^{k_2} = 4$ using the architecture in [93]. Using these less constrained integer values means smaller sampling clock division ratios, which leads to higher PFD update rates and results in several advantages, including more flexibility in choosing loop bandwidth, and therefore more freedom to optimize total phase noise of the loop. Another advantage of smaller sampling clock division ratios is that higher sampling frequencies are generated, and therefore covers a wider frequency acquisition range without switching to other sampling frequencies.

7.4. Analysis and Discussions

7.4.1. Frequency acquisitions

Figure 66 shows the alias frequencies produced by a D-ALL. If the desired VCO frequency is within 'Region1' (or 'Region2'), then by setting $D_1 = 1$ and $D_2 = 2$ (or $D_1 = 2$ and $D_2 = 1$), we can have a positive alias frequency f_{alias_a} (or f_{alias_b}) and a negative alias frequency f_{alias_b} (or f_{alias_a}). Similarly, if the desired VCO frequency is within 'Region3' (or 'Region4'), then by setting $D_1 = 2$ and $D_2 = 4$ (or $D_1 = 4$ and $D_2 = 2$), we can have a positive alias frequency f_{alias_b} (or f_{alias_c}) and a negative alias frequency f_{alias_c} (or f_{alias_b}). If the desired VCO frequency is within 'Region5', in order to generate a positive alias frequency and a negative alias

frequency, then larger D_1 and D_2 values need to be selected to provide different sampling frequencies.

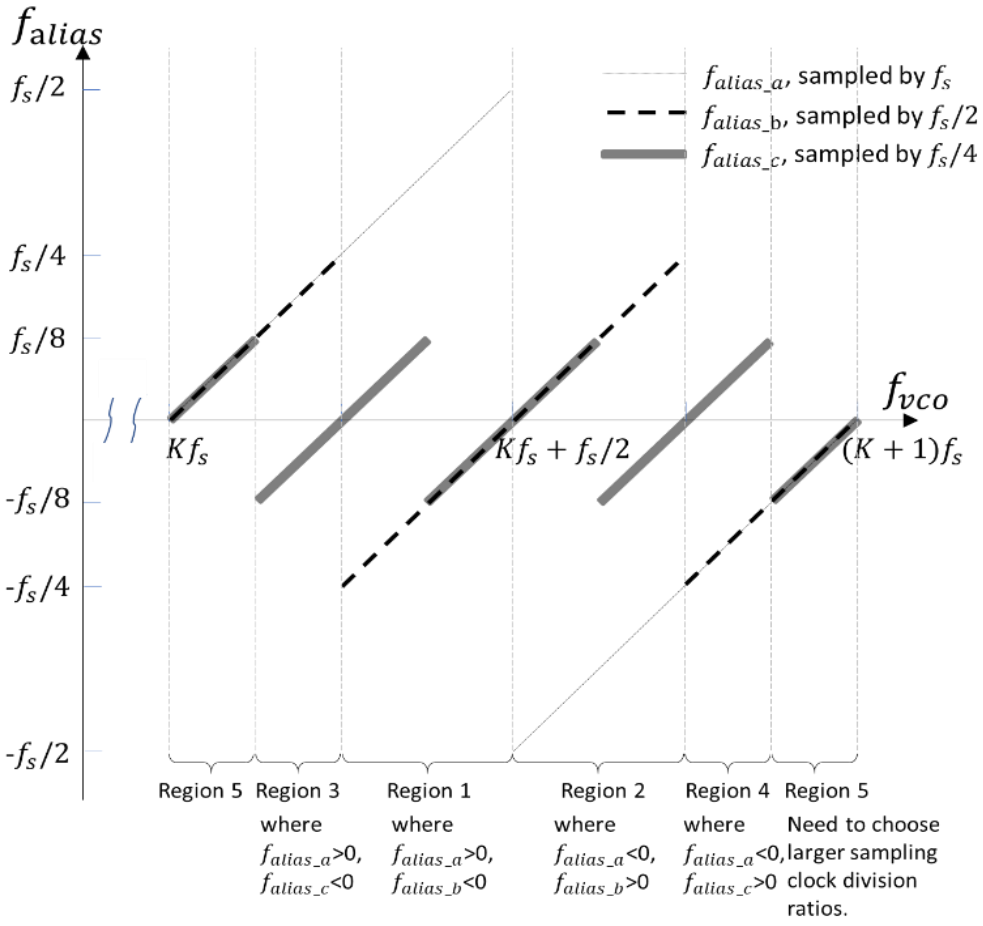
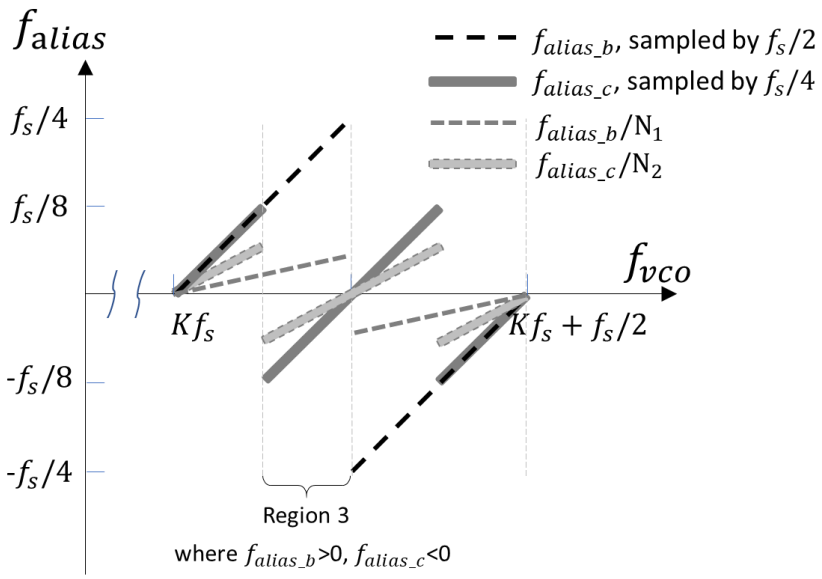


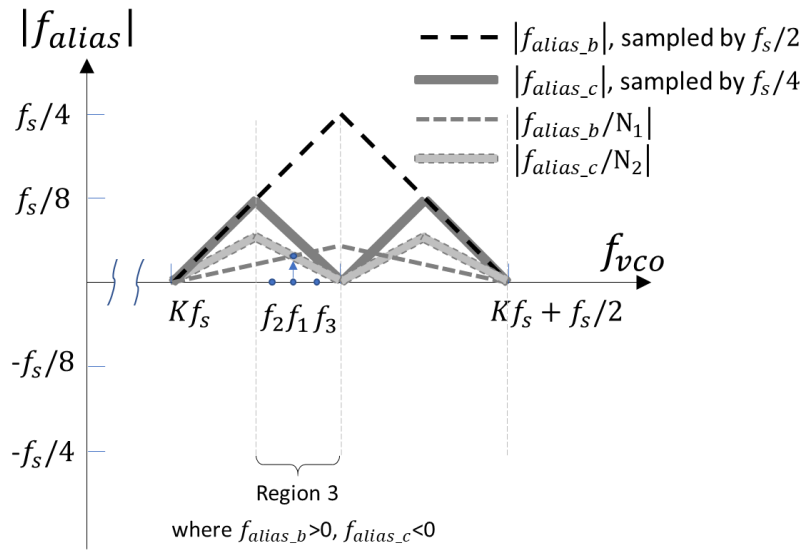
Figure 66: Alias frequencies produced by a D-ALL. f_{VCO} represents the VCO input frequency, f_s represents the input sampling frequency, f_{alias_a} , f_{alias_b} and f_{alias_c} represent the output alias frequencies corresponding to the sampling frequencies of f_s, $f_s/2$, and $f_s/4$ respectively.

The acquisition and lock operation is illustrated in Figure 67. Assume f_1, f_2, and f_3 are three frequencies in the same region (i.e. 'Region3' in Figure 67), where f_1 is the desired frequency, f_2 is smaller than f_1, and f_3 is larger than f_1. Since $f_{vco} = f_1$ is the desired output frequency, the division ratios $N_1$and N_2 are set to satisfy the following equation when $f_{vco} = f_1$:

$$\left|\frac{f_{alias\_b}}{N_1}\right| = \left|\frac{f_{alias\_c}}{N_2}\right|. \tag{7.11}$$



(a)



(b)

Figure 67: Operation of a D-ALL. (a) alias frequencies. (b) absolute value of alias frequencies. f_a is the desired frequency, f_2 is smaller than f_1, and f_3 is larger than f_1. When f_{VCO} is larger (or smaller) than f_1, $\left|\frac{f_{alias\_b}}{N_1}\right|$ will be larger (or smaller) than $\left|\frac{f_{alias\_c}}{N_2}\right|$, and the loop will decrease (or increase) f_{VCO} until $f_{VCO} = f_1$.

According to Figure 67, in 'Region3' f_{alias_b} is positive while f_{alias_c} is negative. Assume the VCO frequency is initialized to be f_2 by additional modules such as a frequency-locked loop

(FLL) or a digital-to-analog converter (DAC). It can be seen from Figure 67 that $\left|f_{alias\_b}/N_1\right| < \left|f_{alias\_c}/N_2\right|$ when $f_{vco} = f_2$. The frequency difference is compared by a PFD and then the LF voltage is tuned by the CP to increase the VCO frequency. Similarly, if the initialized frequency is $f_{vco} = f_3$, then $\left|f_{alias\_b}/N_1\right| > \left|f_{alias\_c}/N_2\right|$, which will decrease the VCO frequency.

The D-ALL is a negative feedback loop in 'Region3' and will eventually achieve lock at $f_{vco} = f_1$ by satisfying $\left|f_{alias\_b}/N_1\right| = \left|f_{alias\_c}/N_2\right|$. By switching the values of D_1 and D_2, or simply changing the loop polarity with the mode-control module shown in Figure 63, the same analysis will result in a negative feedback loop for the D-ALL in a different region (i. e. 'Region4' in Figure 66) and another targeting frequency in 'Region4' can be synthesized.

It can also be observed from Figure 65 that with sampling clock division ratios (i.e., D_1 and D_2) increasing, the corresponding frequency acquisition range (i.e., 'Region1', 'Region2', 'Region3' and 'Region4') is becoming smaller. As discussed in Section 7.3, this imposes more stringent requirements of the other modules, such as a higher-resolution DAC to initialize the VCO into the correct frequency range. Therefore, although infinite pairs of $(D_1,\ D_2)$ are available to satisfy the D-ALL requirement, minimum possible values of $(D_1,\ D_2)_{max}$ are preferred in a D-ALL.

7.4.2. Frequency resolution

Similar to a PLL, frequency resolution is defined as the minimum frequency spacing that a D-ALL can achieve. For a D-ALL, as long as $f_{alias\_b} * f_{alias\_c} < 0$ and $\left|\frac{f_{alias\_b}}{N_1}\right| = \left|\frac{f_{alias\_c}}{N_2}\right|$ can be satisfied, the loop can be locked by properly choosing N_1 and N_2.

Therefore, a D-ALL can achieve arbitrarily small frequency resolutions by programming the divider ratios N_1 and N_2 theoretically. Unfortunately, N_1 and N_2 cannot be arbitrarily large as discussed below.

In a traditional PLL, the bandwidth of the loop is usually determined by minimizing the total phase noise, which is the frequency offset for which the in-band phase noise equals the out-of-band phase noise. In a D-ALL, when N_1 and N_2 are large, $\left|\frac{f_{alias\_b}}{N_1}\right|$ (and also $\left|\frac{f_{alias\_c}}{N_2}\right|$) will be

small and the output of the PFD will be at a low frequency. To satisfy the continuous loop approximation requirement, the bandwidth of the loop should be around or smaller than $\frac{1}{10}\left|\frac{f_{alias\_b}}{N_1}\right|$, and therefore cannot be the optimal bandwidth at which the phase noise is minimized.

7.4.3. Number of reference clocks

One limitation of the ALL architecture lies in the requirement of one additional clock. Instead of using only one reference clock in a conventional PLL, two clocks are required in an ALL, with one for sampling and the other as a reference clock. Based on the proposed differential locking mechanism, a D-ALL has solved this problem by eliminating the reference clock as illustrated in Figure 63 and Figure 65.

One potential issue is that the sampling clock usually needs to have a high frequency, i.e. 1 GHz. However, a 1 GHz sampling clock is usually not directly available from a crystal oscillator. Fortunately, there are various low-cost architectures to achieve a 1 GHz signal with low jitter (i.e., an RMS jitter less than 3 ps). In addition to the conventional PLLs, multiple low-cost low-phase noise approaches have been proposed in the last decade, including the multiplying delay-locked loop (MDLL) [100][101], injection-locked LC-VCO [102], subsampling PLL (SSPLL) [33][40][74][97][102][104] and injection-locked ring oscillator (ILRO) [105][106][107][108]. Take the ILRO as an example. With a simple architecture, ILRO can low-pass filter the noise from the injection clock and high-pass filter the noise from the ring oscillator, which functions similar to a conventional PLL [107][108]. Measurements have shown that for a targeted 2.5 GHz signal, the RMS jitter is smaller than 5 ps in most cases and can be smaller than 1.5 ps when tuning the bandwidth of the ILRO [107].

7.4.4. Loop bandwidth

The conventional PFD operates in discrete-time, and the continuous-time approximation requires that the loop time constant be much longer than the input period [63]; therefore, we have:

$$\omega_{-3dB,D-ALL} \ll \frac{2\pi f_{alias1}}{N_1}, \tag{7.12}$$

where ω_{-3dB} is the loop bandwidth.

For a certain range of desired frequencies, f_{alias1}/N_1 varies for different f_{vco}. To meet the requirement of Equation (7.12), the loop bandwidth is set to satisfy:

$$\omega_{-3dB,D-ALL} \leq \frac{1}{10}\left(\frac{2\pi f_{alias1}}{N_1}\right)_{min}. \tag{7.13}$$

It should be noted that the relationship in Equation (7.13) is much different from the relationship of a conventional PLL,

$$\omega_{-3dB,PLL} \leq \frac{1}{10}(2\pi f_{ref}) = \frac{1}{10}\left(\frac{2\pi f_{VCO}}{N'}\right), \tag{7.14}$$

where $\frac{2\pi f_{VCO}}{N'}$ is usually determined by the frequency resolution in an integer-N PLL.

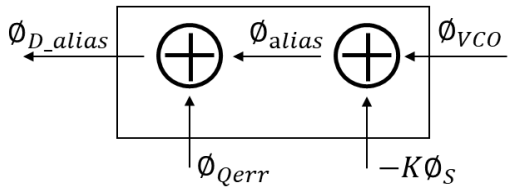


Figure 68: Phase domain model of a digital sampler, which consists of an analog sampler, an interpolation filter and a 1-bit quantizer [63].

Assume a targeting frequency range of 21.6–21.9 GHz to be synthesized with a frequency step of 100 MHz (21.6 GHz, 21.7 GHz, 21.8 GHz and 21.9 GHz) with a sampling frequency of 1 GHz.

For 21.9 GHz, we can set $D_1 = 1$ to have a 1 GHz sampling clock and $f_{alias1} = -100$ MHz, $D_2 = 6$ to have a 166.7 MHz sampling clock and $f_{alias2} = 66.7$ MHz, and then we can set $N_1 = 3$ and $N_2 = 2$ to satisfy Equation (7.11).

For 21.8 GHz, we can set $D_1 = 1$ to have a 1 GHz sampling clock and $f_{alias1} = -200$ MHz, $D_2 = 3$ to have a 333.3 MHz sampling clock and $f_{alias2} = 133.4$ MHz, and then we can set $N_1 = 3$ and $N_2 = 2$ to satisfy Equation (7.11).

For 21.7 GHz, we can set $D_1 = 1$ to have a 1 GHz sampling clock and $f_{alias1} = -300$ MHz, $D_2 = 2$ to have a 500 MHz sampling clock and $f_{alias2} = 200$ MHz, and then we can set $N_1 = 3$ and $N_2 = 2$ to satisfy Equation (7.11).

For 21.6 GHz, we can set $D_1 = 1$ to have a 1 GHz sampling clock and $f_{alias1} = -400$ MHz, $D_2 = 2$ to have a 500 MHz sampling clock and $f_{alias2} = 100$ MHz, and then we can set $N_1 = 4$ and $N_2 = 1$ to satisfy Equation (7.11).

$$\omega_{-3dB,D-ALL} \leq \frac{1}{10}\left(\frac{2\pi f_{alias1}}{N_1}\right)_{min} = \frac{2\pi}{10} * Min(33.3, 66.6, 100, 100)\ \text{MHz}$$

$$= 2\pi * 3.3\ \text{MHz}. \tag{7.15}$$

For an integer-N PLL with a reference frequency of 100 MHz,

$$\omega_{-3dB,PLL} \leq \frac{1}{10}\left(2\pi f_{ref}\right) = 2\pi * 10\ \text{MHz}. \tag{7.16}$$

Therefore, the largest allowed loop bandwidth of a D-ALL is smaller than that of an integer-N PLL.

7.4.5. Phase noise

A phase domain model of a digital sampler was proposed in [63]. Digital subsampling is a one-bit quantization of analog subsampling as shown in Figure 68, therefore, the final output of a digital sampler can be expressed as:

$$\emptyset_{D\_alias} = \emptyset_{alias} + \emptyset_{Qerr} = \emptyset_{VCO} - K\emptyset_S + \emptyset_{Qerr}. \tag{7.17}$$

Based on the phase domain model of a digital sampler, the phase domain model for a D-ALL corresponding to Figure 67 can be built as shown in Figure 69.

7.4.5.1. Phase noise contributions from quantization errors

The quantization error generated from digital subsampling can lead to the output phase error, which appears as phase noise at the output spectrum. The transfer function can be described as:

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{Qerr}}\right)_{D-ALL} = \frac{Forward\ Gain}{1 + Loop\ Gain} = \frac{1}{\frac{1}{\frac{1}{2\pi} I_{cp}\left(R + \frac{1}{sC}\right)\frac{K_{vco}}{s}\left(\frac{1}{N_1} + \frac{1}{N_2}\right)} + 1}. \quad (7.18)$$

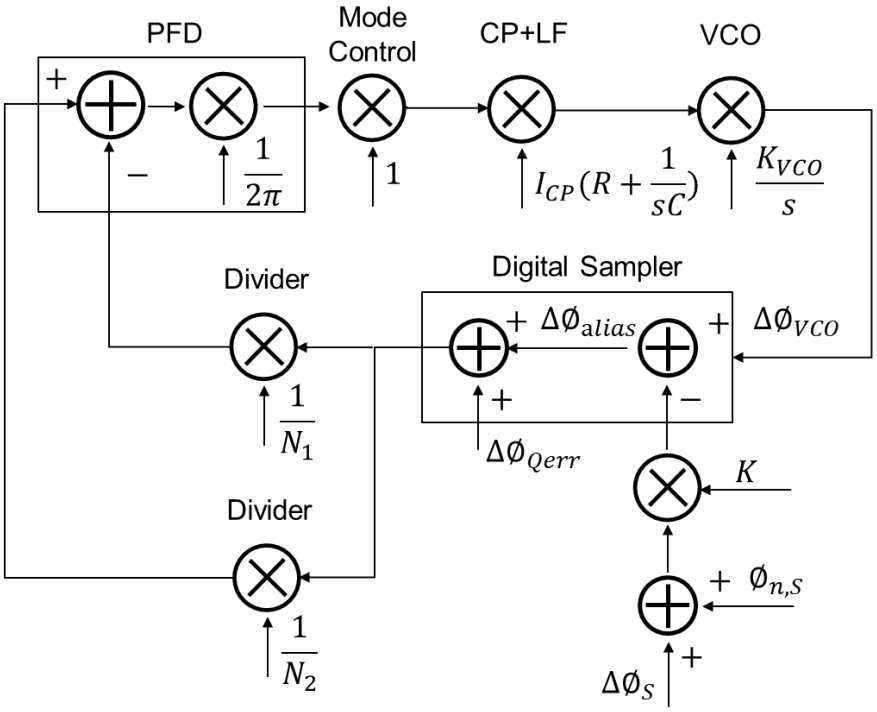


Figure 69: Phase domain model of a D-ALL.

Recall from [63], the phase noise transfer function of an ALL is:

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{Qerr}}\right)_{ALL} = \frac{1}{\frac{1}{\frac{1}{2\pi} I_{cp}(R + \frac{1}{sC})\frac{K_{vco}}{s}\frac{1}{N}} + 1}. \quad (7.19)$$

Compared to an ALL, the phase noise contributed by the reference clock is eliminated since there is no need for reference clock, and the phase noise contributed from quantization error is also decreased for the same divider ratio. Furthermore, since both input signals of the PFD can be synchronized with the sampling clock, the jitter accumulated from the samplers and the dividers can be removed.

7.4.5.2. Phase noise contributions from sampling clock phase noise

The transfer function from the sampling clock phase noise to the output phase noise can be calculated as

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{n,s}}\right)_{D-ALL} = \frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{D_{alias}}}\frac{\Delta\emptyset_{D_{alias}}}{\Delta\emptyset_{n,s}} = K\frac{\Delta\emptyset_{VCO}}{\Delta\emptyset_{D_{alias}}}$$

$$= \frac{K}{\frac{1}{\frac{1}{2\pi}I_{cp}(R+\frac{1}{sC})\frac{K_{vco}}{s}\left(\frac{1}{N_1}+\frac{1}{N_2}\right)}+1}. \qquad (7.20)$$

Therefore, the phase noise of the sampling clock is first multiplied by the subsampling ratio K and then low-pass filtered by the loop.

7.4.5.3. Phase noise contributions from CP

In a D-ALL, the phase noise contribution from the CP noise can be calculated as

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta I_{n,CP}}\right)_{D-ALL} = \frac{Forward\ Gain}{1+Loop\ Gain} = \frac{\frac{2\pi}{I_{cp}}}{\frac{1}{\frac{1}{2\pi}I_{cp}(R+\frac{1}{sC})\frac{K_{vco}}{s}\left(\frac{1}{N_1}+\frac{1}{N_2}\right)}+1}. \qquad (7.21)$$

Similar to a conventional PLL, the CP noise is low-pass filtered by the loop. Within the loop bandwidth, Equation (7.21) can be approximated as

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta I_{n,CP}}\right)_{C-ALL} = \frac{\frac{2\pi}{I_{cp}}}{\frac{1}{\frac{1}{2\pi}I_{cp}(R+\frac{1}{sC})\frac{K_{vco}}{s}\left(\frac{1}{N_1}+\frac{1}{N_2}\right)}+1} \approx \frac{2\pi}{I_{cp}}. \qquad (7.22)$$

In a conventional PLL, the phase noise contribution from CP to output can be calculated as

$$\left(\frac{\Delta\emptyset_{VCO}}{\Delta I_{n,CP}}\right)_{PLL} = \frac{\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}}{1+\frac{1}{2\pi}I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}\frac{1}{N}} \approx \frac{\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}}{\frac{1}{2\pi}I_{cp}\left(R+\frac{1}{sC}\right)\frac{K_{vco}}{s}\frac{1}{N}} = \frac{2\pi}{I_{cp}}N. \qquad (7.23)$$

By comparing Equations (7.22) and (7.23), we observe that the power of the phase noise contributed from CP is N^2 smaller in a D-ALL compared to in a conventional PLL. This is consistent with the subsampling PLL discussed in [74]. The analog subsampler functions as a phase detector in [74] while the digital sampler functions as an aliasing divider in this work.

7.5. Design and Simulation Results

To verify the proposed architecture as shown in Figure 65, a 21–23.3 GHz D-ALL was designed using GlobalFoundries 130 nm Bulk CMOS process and post-layout extracted circuit simulations were performed in Cadence Spectre.

7.5.1. LC VCO

A 21–23.3 GHz LC VCO is designed. The VCO is tuned with varactors and two binary-weighted switched capacitors, which extend the tuning rage (21GHz – 23.3 GHz) without increasing the K_{VCO} of the VCO (K_{VCO} is ~614MHz/V in the middle range).

7.5.2. Sampler

A CML latch is used to sample the 21–23.3 GHz VCO, and buffers are inserted between the VCO and sampler to reduce the effects of the act of sampling from loading the VCO.

7.5.3. Sampling clock buffer

A buffer similar to [74] is designed to ensure the rising edge clean. By re-positioning the triggered edges for the NMOS and the PMOS, short-circuit current can be avoided and a clean sharp rising edge can be therefore achieved.

7.5.4. Digital blocks

The digital blocks contain the re-sampling DFFs, the programmable dividers for alias signals, and the programmable dividers for the sampling clocks, and the block is synthesized by standard digital synthesis.

7.5.5. Other modules

The PFD is implemented with the conventional architecture, and a fully differential topology has been used in the CP design to reduce the effect of the non-idealities of the CP transistors. The mode-control module is designed to selectively invert the sense of lead and lag to ensure the loop always negative feedback.

7.5.6. Layout considerations

Multiple power domains have been used to reduce the noise coupled from the power and ground signal lines. Additionally, the sampler is placed in a triple-well to reduce the substrate coupled noise from the other modules.

7.5.7. Simulations

The D-ALL was verified through a post-layout extracted circuit simulation using Cadence. D-ALL synthesizer pull-in and lock were demonstrated at 6 frequencies (21.6 GHz, 21.7 GHz, 21.8 GHz, 21.9 GHz, 22.3 GHz, and 22.4 GHz) throughout the VCO range of 21–23.3 GHz. Simulations are run with full transistor noise models at 27 ℃. Assume a 21.6 GHz output signal is desired to be synthesized and a $f_s = 1$ GHz signal is available as the sampling clock. By setting the sampling clock division ratios to be $D_1 = 1$, $D_2 = 2$, and alias divider ratios to be $N_1 = 4$ and $N_2 = 1$, then the sampling clock for the first sampler is 1 GHz and the corresponding alias frequency when the loop is in lock is $f_{alias1} = -400$ MHz, while the sampling clock for the second sampler is 500 MHz and the corresponding alias frequency when the loop is in lock is $f_{alias2} = +100$ MHz. Then the divided frequencies feeding into the PFD are $\frac{f_{alias1}}{N_1} = \frac{-400\ MHz}{4} = -100$ MHz and $\frac{f_{alias2}}{N_2} = \frac{+100}{1} = +100$ MHz respectively, which can therefore maintain the lock.

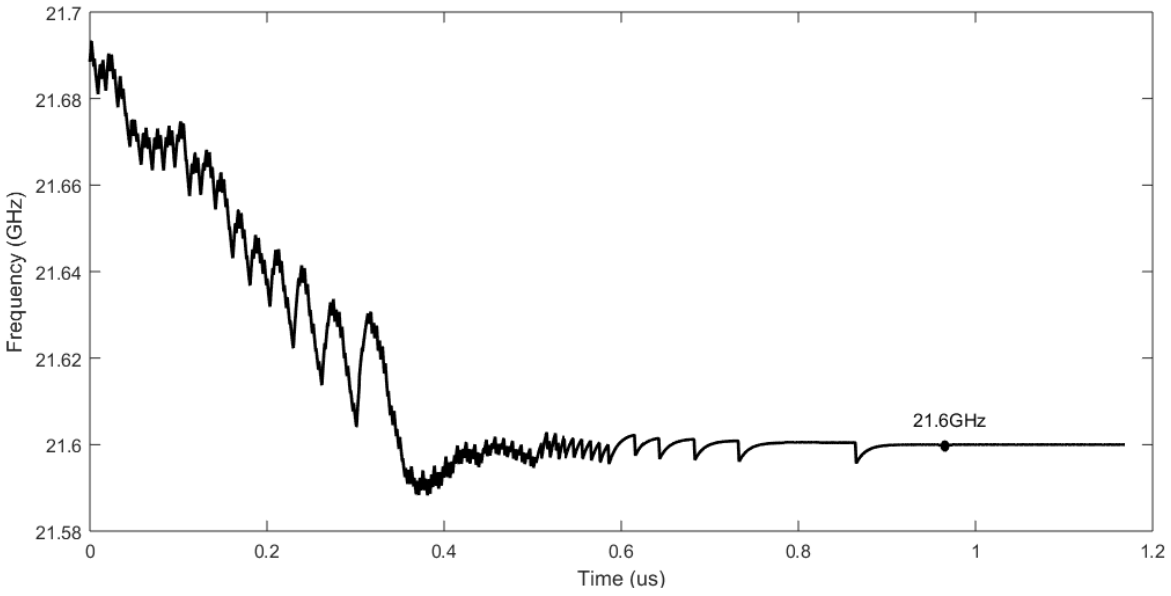


Figure 70: Transient simulations of a D-ALL synthesizing a 21.6 GHz signal. A $f_s = 1$ GHz signal is used as the sampling clock, and the parameters are set as $D_1 = 1$, $D_2 = 2$, $N_1 = 4$ and $N_2 = 1$.

Assume the initialized VCO frequency is 21.7 GHz. With the above settings, the alias frequencies are $f_{alias1} = -300$ MHz, $f_{alias2} = +200$ MHz and $\frac{f_{alias1}}{N_1} = \frac{-300}{4} = -75$ MHz, $\frac{f_{alias2}}{N_2} = \frac{+200}{1} = +200$ MHz. Feeding the -75 MHz signal and the $+200$ MHz signal into the PFD will decrease the VCO frequency until the loop is in lock.

The D-ALL was verified through a post-layout extracted circuit simulation using Cadence Spectre. A 1 GHz square wave is used as the sampling clock. Simulation has shown that the designed D-ALL can synthesize multiple targeted frequencies. Transient simulation results of synthesizing the targeted 21.6 GHz signal are illustrated in Figure 70.

In a conventional high-frequency PLL, dividers are usually the most power-hungry modules since multiple stages are required and DC bias is needed in each of the first few high-speed stages. For instance, in [109], a PLL with a 21 GHz maximum operating frequency was implemented in 130 nm Bulk CMOS process. The total power consumption is 22.5 mW, of which 9 mW is dissipated by the divider chain including the CML prescaler. In the proposed D-ALL architecture, however, the total power consumption is 15.4 mW, of which only 2.9 mW is dissipated by the digital sampler, which is 67.8% less compared to the divider in [109]. The

active area of the conventional PLL in [109] is 0.28 mm^2 , while in the case of the D-ALL in this work, the active area is 0.21 mm^2 .

Table 3: Comparison of D-ALL with conventional PLLs

	This work	Ding [109] JSSC'07
Architecture	Differential Alias-Locked Loop (D-ALL)	Conventional PLL
Oscillator	LC	LC
Output freq.	21–23.3 GHz	20.05–21 GHz
Total power (VCO + loop)	15.4 mW	22.5 mW
Divider/sampler power consumption	2.9 mW	9 mW
Process	130 nm	130 nm
Active area	0.21 mm^2	0.28 mm^2

As mentioned previously, another advantage of a sampler over a divider is that the sampler simultaneously allows a high operation frequency and a wide frequency range. Although the D-ALL is verified to synthesize a frequency range of 21–23.3 GHz in this work, additional simulation has shown that the digital sampler can function for frequencies as high as 40 GHz and a range from almost DC to 40 GHz. This is different from the conventional dividers since a digital sampler only needs to make a sampling "decision" at the 1 GHz sampling clock rate, while a divider has to be clocked at the 40 GHz VCO rate.

7.6. Future Work

Similar to a C-ALL, a D-ALL also has the so-called "dead zone" problem even when in lock. This dead zone results in only a coarse phase lock and no effective suppression of phase noise. As part of future work, to achieve fine phase lock, we can propose another circuit architecture named phase shift differential alias-locked loop (PS-DALL) to always provide non-zero feedback and guarantee lock at every active edge of the alias signal.

7.7. Conclusion

We have introduced the differential alias-locked loop (D-ALL) circuit architecture and the algorithm to choose loop parameters used for frequency synthesis. A D-ALL has the advantage of wide frequency range of operation compared to a traditional high-frequency PLL.

Instead of comparing the feedback signal with a reference clock in a PLL or an ALL, a D-ALL feeds two digital alias signals generated from two digital samplers clocked at different sampling frequencies into a PFD. The D-ALL eliminates the second reference clock required in an ALL. Additionally, by finer tuning the sampling clock division ratios, better phase noise performance, wider frequency acquisition range, and more freedom in choosing loop bandwidth can be achieved compared to [93]. Spectre post-layout extracted circuit simulations have verified the proposed design can achieve lock at programmable frequencies in the range of 21–23.3 GHz.

CHAPTER 8. VCO-integrator Based PLLs

Charge-pump-based PLLs are widely used in modern ICs because of their superior performance. This well-known circuit architecture, however, poses several disadvantages including large loop filter implemented either as an off-chip discrete component, or on-chip consuming significant silicon area, and large frequency spur at the VCO output because of the voltage ripples on the loop filter. To address these issues, we propose a novel PLL circuit architecture with VCO implemented as an integrator instead of an integrator based on a charge pump and loop filter. To ensure loop stability, a voltage-controlled delay line is developed to introduce a zero in the loop transfer function. A phase domain model is developed for this novel class of circuits that includes the VCO-based integrator. Spectre simulation has verified the proposed design with a VCO-based integrator can successfully synthesize the targeting frequency at 3 GHz with 39% of total silicon area saving at a cost of 109% increase in total power consumption without compromising on phase noise performance.

8.1. Introduction

Phase-Locked Loops (PLLs) are fundamental blocks of modern integrated circuits (ICs). Among different types of PLLs, type-II PLLs are widely used because of their superior performance. Although Type-I PLLs have shorter settling times, the Type-II PLLs' second pole allows them to theoretically converge to zero phase error. A type-II PLL, which usually contains a charge pump and a loop filter, not only achieves frequency lock but also achieves phase alignment owing to the two poles at origin in phase domain [111].

For a given loop bandwidth of a PLL, which means the time constant of the loop filter is determined, the resistance and capacitance consisting the loop filter needs to be carefully designed and optimized. A designer needs to compromise between smaller noise and smaller silicon area when choosing the resistance and capacitance in the loop filter. For instance, a large resistor can result in large thermal noise, while a large capacitor requires large silicon area or off-

---

This Chapter is based on a conference paper presented at ISCAS 2016 [110].

-chip implementation. Different approaches have been proposed to address this issue. Instead of using only one charge pump in a conventional implementation, an integral path and a proportional path have been implemented separately by using two charge pumps in [112]. As another alternative to a large capacitor, a low frequency pole can be achieved with a smaller capacitor and an opamp [113]. In addition to the extra power consumption from the operational amplifier, the extra noise from these components and kT/C noise from the smaller capacitor directly impact the loop noise performance, which limits the application of this technique.

Another issue in a type-II PLL is the undesired frequency spur at the voltage-controlled oscillator (VCO) output. In a type-II PLL, voltage pulses are generated by PFD even during lock, charge pump current pulses are therefore generated, and a second capacitor is usually added in parallel with the loop filter to reduce the periodic voltage ripples [111]. The choice of this second capacitor's value is a compromise between reducing the PFD-generated voltage ripple at the VCO input and minimizing the impact on the loop transfer function as designed. As a result, the capacitance is around 10% ~ 20% of the main capacitor. Different techniques have been proposed to minimize frequency spurs. Noticing that the resistor in the loop filter is to introduce a zero to stabilize the loop, different stabilization techniques were proposed to replace the resistor, and the main capacitor can be used to filter the voltage and therefore minimize the voltage ripple. An alternative approach to generate the zero is to insert a voltage-controlled phase shifter (VCPS), which is implemented by a voltage-controlled delay-line (VCDL) between the phase detector (PD) and the reference clock in [114][115][116]. Similar to the resistor in the conventional PLL architecture, the VCPS introduces a zero in the open-loop phase domain transfer function and thus ensures stabilization. Since there is no resistor in the loop filter, the voltage ripple can be directly attenuated and minimized by the main capacitor. Digital PLLs, which have attracted a lot of research attention in the last decade, can inherently solve the large area capacitor by eliminating it and the voltage ripple problem by resorting to digital loop filters, but at a cost of design complexities in time-to-digital converters (TDCs) and quantization errors in the digital-to-analog converters (DACs) or the digitally controlled oscillators (DCOs) [117][118][119].

Our use of a VCO as an integrator in a PLL was inspired by previous similar use in analog integrators for other applications. Analog integrators are key building blocks in many analog

signal processing circuits including PLLs, ADCs and filters. Conventional analog integrators usually resort to opamp-RC or Gm-C implementations, which are limited by the performance of the operational transconductance amplifiers (OTAs) [120]. For instance, the DC gain of these integrators is limited by the gain of OTAs used. As IC process scales down and transistor output resistance reduces, OTA and thus integrator performance is further exacerbated [121]. To address these issues, researchers have proposed VCO-based integrators in ADCs [122][123][124][125][126], analog filters [120][121] and regulators [127]. A ring oscillator-based integrator was proposed in [128][129] to implement the integral control path together with a conventional analog proportional path within a PLL, as illustrated in Figure 71.

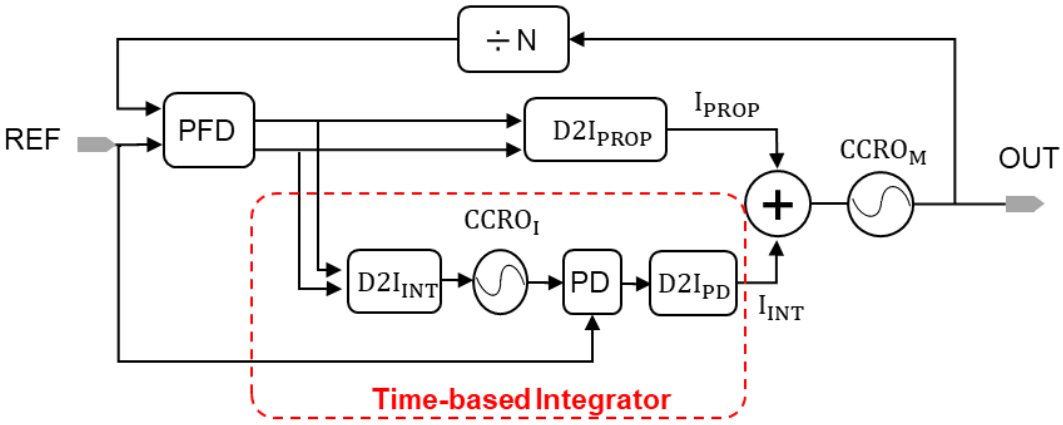


Figure 71: Block diagram of the PLL with time-based integrator in the integral control path [128].

Building on these VCO-based integrator innovations, in this chapter, we propose a new type of PLL with a VCO working in the phase domain as an integrator, as illustrated in Figure 72. Instead of using a combination of charge pump and RC filter as an integrator in a conventional type-II PLL, time-based integral path and time-based proportional path are proposed using a combination of VCO, PD and VCDL. Similar to the PLL with smallest reported active area of only 0.0021 mm^2 in [128], the proposed architecture in this work also demonstrates a small active area, and moreover reduces the voltage ripple at the loop filter while maintaining low power consumption.

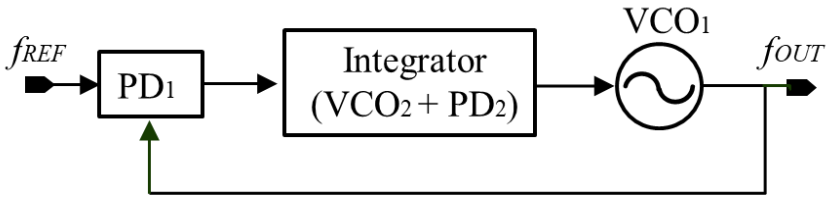


Figure 72: Proposed PLL with a VCO as an integrator [110].

In this chapter, Section 8.2 introduces the proposed circuit architecture that uses VCOs as integrators in PLLs and discusses stabilization techniques, Section 8.3 discusses the circuit design consideration and the phase-domain models, Section 8.4 and Section 8.5 provide discussions and simulation results, and Section 8.6 is the conclusion.

8.2. VCO as an Integrator in PLLs

8.2.1. VCO as an integrator in a PLL

Figure 73 (a) illustrates the block diagram of the VCO-based integrator. The integrator consists of two identical VCOs and a PD. To distinguish the two type of VCOs inside the proposed PLL architecture, the VCO used inside the integrator is referred to as the I-VCO (integrator VCO), which can be implemented as a normal ring oscillator. Similarly, the PD within this integrator is named as I-PD (integrator PD). Both of the two input signals, V_{in1} and V_{in2}, are applied as the control signals of the two I-VCOs. The two I-VCOs, which have a gain of K_{I-VCO}, are then fed into the I-PD which has a gain of K_{I-PD}. According to the equivalent phase domain linear mathematical model illustrated in Figure 73 (b), we can have the following equation:

$$V_{out} = [(K_{I-VCO} \cdot \mathrm{s}^{-1} \cdot V_{in1}) - (K_{I-VCO} \cdot \mathrm{s}^{-1} \cdot V_{in2})] \cdot K_{I-PD} = K_{I-VCO}K_{I-PD}(V_{in1} - V_{in2})\mathrm{s}^{-1}. \quad (8.1)$$

Equation (8.1) verifies the proposed architecture behaves as an integrator.

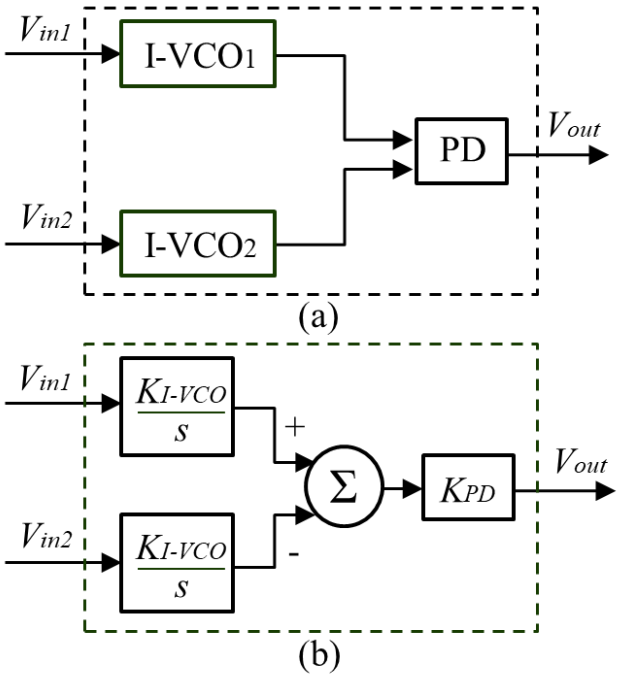


Figure 73: Proposed architecture using a VCO as an integrator: (a). block diagram (b). phase domain model.

As shown in Figure 72, a VCO-based integrator is proposed to replace the combination of charge pump and loop filter. However, charge pump PLL usually requires a resistor in the loop filter to stabilize the loop. Stabilization techniques of the newly proposed PLL with a VCO based integrator will be discussed in the following section.

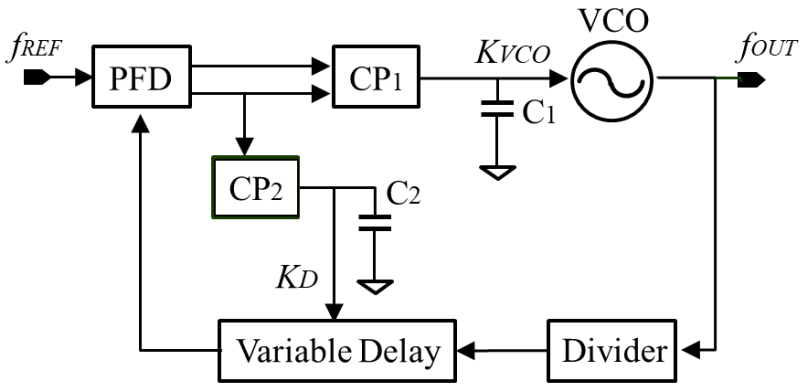
8.2.2. Stabilization technique

Type-II PLLs contain two poles at the origin in the phase domain, which makes the loop unstable. To solve this problem, an additional resistor is added to introduce a zero to stabilize the loop [111]. According to Equation (8.1), the proposed architecture in Figure 73 (a) behaves as an integrator at DC, thereby resulting in instabilities. To stabilize the proposed architecture, zeros should be added to the phase domain model. Several other techniques were proposed.

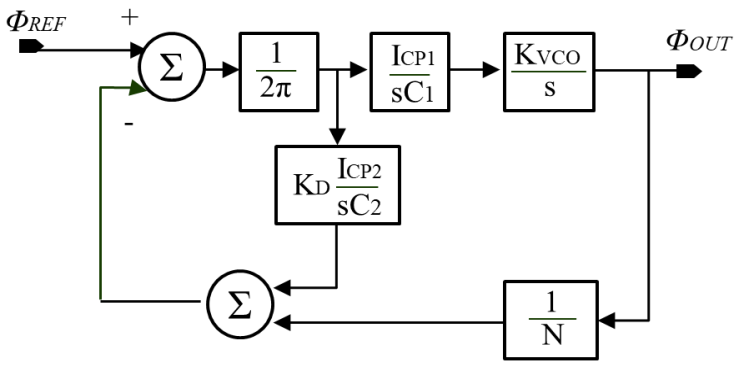
As illustrated in Figure 74 (a), a VCDL between the feedback signal and the PD is included [110]. The corresponding phase domain model is illustrated in Figure 74 (b). Assume the VCDL has a sensitivity of K_D, then the open-loop transfer function is given by:

$$T_{open-loop} = \frac{I_{cp1}}{2\pi}\frac{1}{sC_1}\left(\frac{K_{VCO}}{s}\frac{1}{N} + \frac{I_{cp2}}{I_{cp1}}\frac{C_1}{C_2}K_D\right), \tag{8.2}$$

where $I_{cp1}$and I_{cp2} represent the two charge pump currents respectively. From Equation (8.2), a stabilizing zero is obtained without adding a resistor in series with C_1. The control signal is very sensitive, which could be impacted by the large signal swings in a VCDL. To avoid kickback noise, a unit gain buffer is applied between the control signal and the VCDL.



(a)



(b)

Figure 74: A stabilization technique with a VCDL inserted between the feedback signal and the PD. (a) Block diagram as presented in [110]. (b). The corresponding phase domain model.

In the proposed architecture, a VCDL is incorporated following each I-VCO as illustrated in Figure 75 (a) instead of adding the VCDL between feedback and PD in [110]. According to the

equivalent phase domain model illustrated in Figure 75 (b), we can have the following equation:

$$V_{out} = [(K_{I-VCO} \cdot \mathrm{s}^{-1} \cdot V_{in1} + K_D \cdot V_{in1}) - (K_{I-VCO} \cdot \mathrm{s}^{-1} \cdot V_{in2} + K_D \cdot V_{in1})] \cdot K_{I-PD}$$

$$= (K_{I-VCO}K_{I-PD} \cdot \mathrm{s}^{-1} + K_D K_{I-PD})(V_{in1} - V_{in2}). \quad (8.3)$$

Compared to Equation (8.1), (8.3) shows that the proposed stabilization technique has created a zero in phase domain by using VCDLs.

8.2.3. Comparison with a charge pump and loop filter

In a conventional charge-pump-based type-II PLL, as illustrated in Figure 76, the transfer function of the combination of charge pump and loop filter can be expressed as (4) below:

$$V_{out} = \frac{1}{2\pi} I_{cp} \cdot ((\mathrm{sC})^{-1} + R) \cdot (V_{in1} - V_{in2}) = \frac{1}{2\pi} \left(I_{cp}(\mathrm{sC})^{-1} + I_{cp}R\right)(V_{in1} - V_{in2}), \quad (8.4)$$

where V_{in1} and V_{in2} represent the outputs from a PFD (or V_{up} and V_{dn} in a conventional representation). Equations (8.3) and (8.4) incorporate similar functions in phase domain. Furthermore, if Equations (8.5) and (8.6) can be satisfied, then Equations (8.3) and (8.4) are equal, and the proposed architecture in Figure 75 (a) implements exactly the same function as a combination of charge pump and loop filter.

$$I_{cp}(\mathrm{sC})^{-1} = K_{I-VCO}K_{I-PD} \cdot \mathrm{s}^{-1} \quad (8.5)$$
$$I_{cp}R = K_D K_{I-PD} \quad (8.6)$$

or

$$I_{cp}\mathrm{C}^{-1} = K_{I-VCO}K_{I-PD} \quad (8.5)$$
$$I_{cp}R = K_D K_{I-PD} \quad (8.6)$$

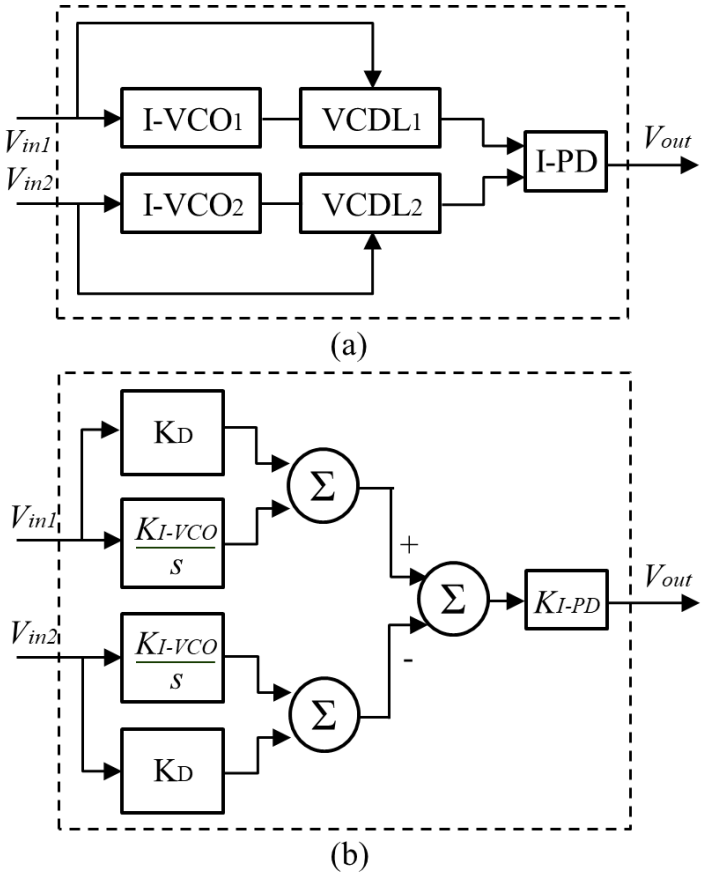


Figure 75: A VCDL is added to each I-VCO to introduce a zero: (a). block diagram (b). phase domain model.

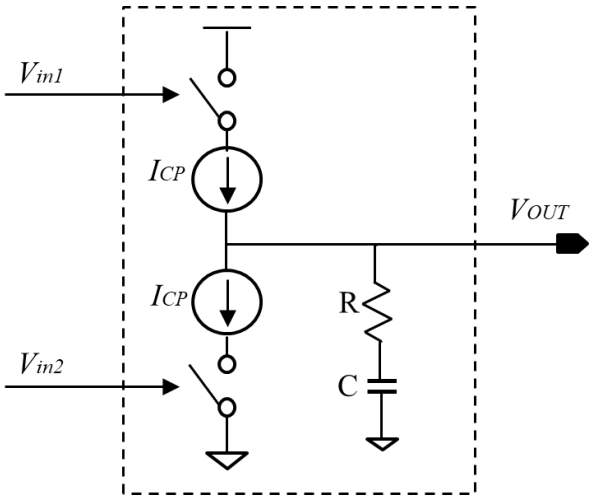


Figure 76: Charge pump and loop filter in a conventional type-II PLL. Note that the second capacitor, which is usually less than 20% of *C* to minimize the voltage ripple in a type-II PLL, is not illustrated here for simplicity purpose [111].

8.3. Type-II PLL with VCO-Based Integrator

To distinguish from the I-PD, we call the PD in the main loop of the type-II PLL as the main PD (Similarly, we call the VCO in the main loop of the type-II PLL as the main VCO). The following section discusses possible implementations of the I-PD and the main PD.

8.3.1. I-PD

The output of the I-PD is directly used to control the main VCO so an analog I-PD output is desired. A sampling PD can directly provide an analog output as the control signal V_{tune} for the main VCO and therefore is a good candidate among all the existing PD topologies. One main limitation of the sampling PD is the limited frequency acquisition range. A sampling PD can be functional as long as the two input frequencies of the I-PD are close to each other, which is not difficult since the layouts of the two I-VCOs will be identical.

Employing a sampling I-PD, the gain is:

$$K_{I-PD} = \frac{A_{I-VCO} \times \sin(\Delta\emptyset)}{\Delta\emptyset} \approx A_{I-VCO} \approx 0.5V_{DD}, \tag{8.7}$$

where A_{I-VCO} is the amplitude of the I-VCO, and V_{DD} is the power supply voltage of the I-VCO. The last 'approximately equal' holds if the I-VCO is implemented with a ring VCO, which is the most common scenario. It should be noticed that a sampling PD is used as the I-PD in our proposed circuit architecture where a ring VCO output is expected, a PFD is used as the PD in the VCO-based integrator in [128] where a pulse output is expected.

8.3.2. Main PD

In this subsection, two possible architectures of the main PD, including the conventional PFD and the subsampling PD, are discussed and compared.

8.3.2.1. PFD as a main PD

As discussed in [111], for a conventional charge-pump-based type-II PLL where a PFD is applied as the main PD, we define the natural frequency and damping factor of the loop and have the

following equations:

$$\omega_n = \sqrt{\frac{I_{cp}K_{VCO}}{2\pi CN}}, \tag{8.8}$$

$$\zeta = \frac{RC}{2}\omega_n, \tag{8.9}$$

where ω_n represents the natural frequency, ζ is the damping factor, I_{cp} is the charge pump current, K_{VCO} is the gain of the main VCO, N is the division ratio, R and C are the resistor and capacitor in the loop filter respectively. Usually, ω_n is a parameter that a designer can choose to optimize the phase noise performance, and ζ is set to be 1 in most cases.

Assuming a PFD is applied as the main PD of the proposed PLL with VCO based integrator, we have the following equations by combining Equations (8.5) - (8.9):

$$K_{I-VCO} = \frac{2\pi N{\omega_n}^2}{K_{VCO}\,A_{I-VCO}}, \tag{8.10}$$

$$K_D = \frac{4\pi N\zeta\omega_n}{K_{VCO}\,A_{I-VCO}}. \tag{8.11}$$

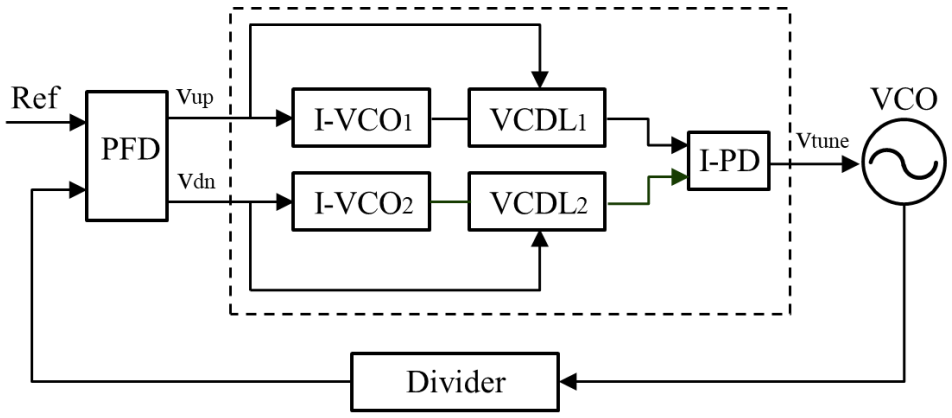


Figure 77: Concept of a PLL with a PFD based on the proposed integrator as a step towards the proposed circuit [110].

Equations (8.10) and (8.11) show that K_{I-VCO} and K_D can be uniquely determined if all the other parameters are known. As illustrated in Figure 77, two I-VCOs and two VCDLs are required in the proposed architecture based on a conventional PFD. The dead zone problem exists in this

architecture, where small differences in phase will not result in change of main VCO frequency because short digital pulses from the PFD cannot effectively control the I-VCOs and VCDLs. To avoid dead zones in the PFD transfer function, we follow the common practice to briefly assert both 'up' and 'down' pulses simultaneously in every reset operation in a type-II PLL [111].

8.3.2.1. Subsampling PD as a main PD

The subsampling PD has attracted interest by researchers in recent years because of the suppression of the in-band phase noise [74] and high-speed operation [15][16]. Motivated by [74], we propose to use a subsampling PD as the main PD as illustrated in Figure 8.8. Instead of using two I-VCOs and two VCDLs as illustrated in Figure 77, only one I-VCO and one VCDL are used as the integrator, and the reference clock is applied as the other input of the I-PD.

The phase domain model of the proposed SSPLL is shown in Figure 79, where T_{ref} represents the period of the reference clock and τ_{pulse} represents the duration of the pulse. A multiplexer, together with the pulse generator, as shown in the following calculations, function as a loop gain controller. As will be discussed in Section 8.4, the gain controller introduces an additional degree of freedom in design implementation.

The open loop transfer function of the proposed PLL can therefore be determined by:

$$T_{open-loop} = K_{PD}\frac{\tau_{pulse}}{T_{ref}}(K_{I-VCO}\mathrm{s}^{-1} + K_D)K_{I-PD}K_{VCO}\mathrm{s}^{-1}. \tag{8.12}$$

The closed loop function is:

$$T_{closed-loop} = \frac{\Phi_{out}}{\Phi_{ref}} = \frac{T_{forward}}{1+T_{open-loop}}. \tag{8.13}$$

Based on the observation that, $K_{PD} = A_{VCO}, T_{forward} = T_{open-loop}$, and combing with (8.12) and (8.13), we have:

$$\omega_n = \sqrt{K_{I-VCO}K_{VCO}A_{VCO}\frac{\tau_{pulse}}{T_{ref}}}, \tag{8.14}$$

$$\zeta = \frac{K_D}{2}\sqrt{\frac{K_{VCO}A_{VCO}}{K_{I-VCO}}\frac{\tau_{pulse}}{T_{ref}}}, \tag{8.15}$$

where ω_n and ζ are the same as defined as in (8.8) and (8.9). With some basic mathematical manipulations, we have

$$K_{I-VCO} = \frac{{\omega_n}^2}{K_{VCO}A_{VCO}\frac{\tau_{pulse}}{T_{ref}}}, \tag{8.16}$$

$$K_D = \frac{2\zeta\omega_n}{K_{VCO}A_{VCO}\frac{\tau_{pulse}}{T_{ref}}}. \tag{8.17}$$

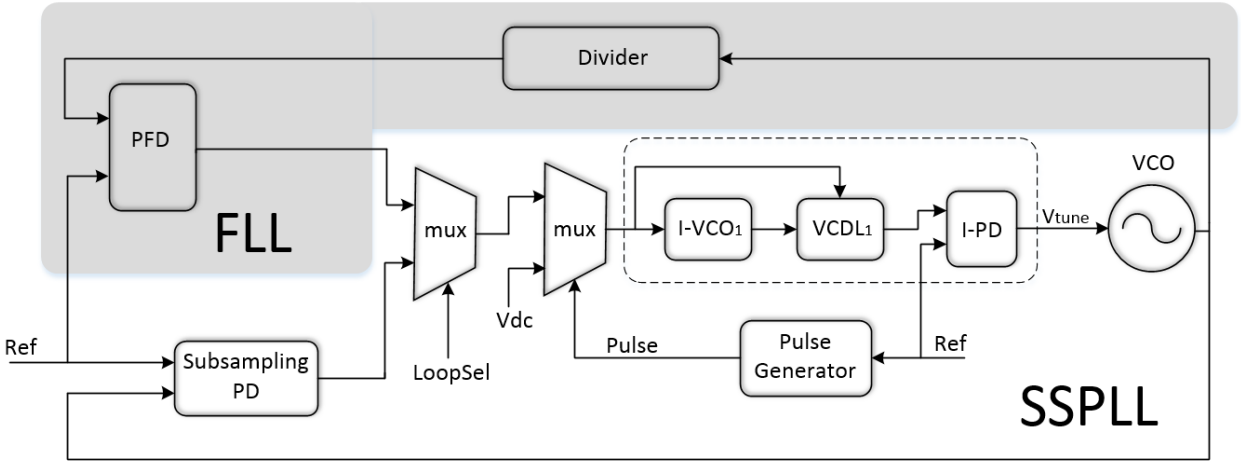


Figure 78: Proposed subsampling PLL (SSPLL) with a sampling PD as the I-PD. A frequency locked loop (FLL) is applied to bring the main VCO frequency to the desired range and achieve frequency lock [110].

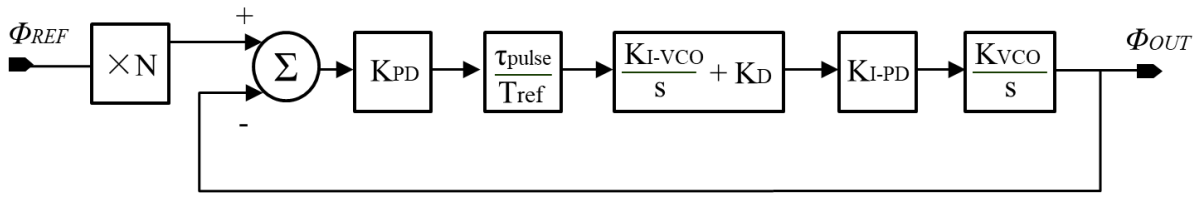


Figure 79: Phase domain model of the proposed SSPLL with a sampling PD as the I-PD [110].

By comparing Equations (8.16) and (8.17) with (8.10) and (8.11), we can see that the two parameters K_{I-VCO} and K_D are determined by one more parameter $\frac{\tau_{pulse}}{T_{ref}}$ in addition to ω_n and ζ,

which means by controlling the pulse duration τ_{pulse}, K_{I-VCO} and K_D can be adjusted to a more feasible region.

Due to the inherent limited acquisition frequency range of the subsampling PD, an additional frequency-locked loop (FLL) is needed to bring the main VCO into the desired frequency region as illustrated in Figure 8.8. Since the FLL is only required to bring the main VCO into the desired frequency region, the dead zone problem is not present and therefore only one I-VCO and one VCDL are sufficient. The loop mode is controlled by another multiplexer to switch between the FLL and the SSPLL.

8.4. Discussion

A PLL with a VCO-based integrator is different from a conventional PLL in many aspects. s-domain models are created, and discussed, including degrees of design freedom, loop stabilization techniques, phase-domain modeling and phase noise analysis in the section below based on this s-domain analysis. Specially, comparisons will show the trade-offs between power and phase noise performance in a PLL with a VCO-based integrator.

8.4.1. Degree of design freedom

As discussed in Section 8.4, using a conventional PFD in the proposed PLL architecture, the relationship of Equations (8.8) and (8.9) could be obtained. The two key parameters of the proposed architecture K_{I-VCO} and K_D are uniquely determined if ω_n and ζ are given. This is different from the charge-pump-based type-II PLLs, where three parameters ($I_{cp}, R\ and\ C$) are determined by only two equations (i.e., two degrees of freedom in the phase domain behavior, but three degrees of freedom in the design implementation). The third degree of freedom in the design implementation is in choosing parameters of $I_{cp}, R\ and\ C$, and allows designers to make trade-offs between area and phase noise [111].

We create an analogous third degree of design implementation freedom in the VCO-integrator architecture by introducing a pulse generator-based loop gain controller. Recall from (8.5) and (8.6), although there are both three unknowns on the left side (I_{cp}, C and R) and on the right side (K_{I-VCO}, K_{I-PD} and K_D), the I-PD is limited to a few known PD topologies and therefore K_{I-PD}

is fixed in most cases. As a result, there are only two unknowns on the right side (K_{I-VCO}, K_D). Therefore, if we apply a certain I-PD in the proposed PLL architecture, we lose one degree of freedom of design implementation when choosing the parameter (K_{I-VCO}, K_D) values. This can result in some unfeasible values for an I-VCO or a VCDL. Take a 100MHz I-VCO as an example, $K_{I-VCO} = 10GHz/V$ or $K_{I-VCO} = 10\,Hz/V$ are impractical to implement.

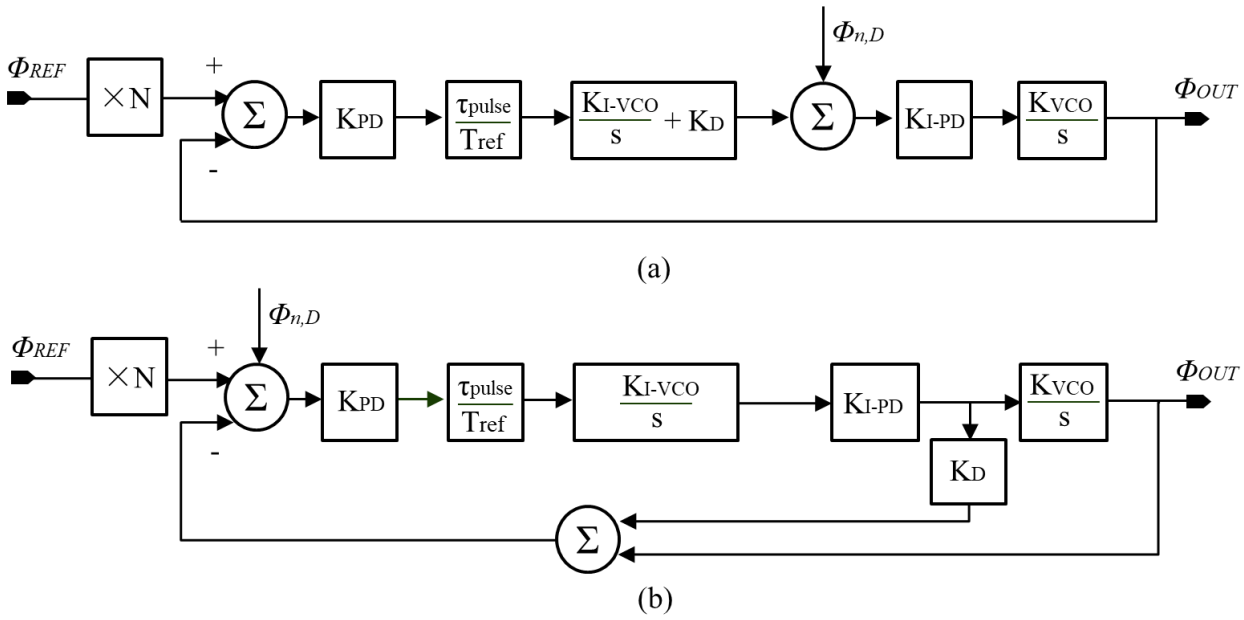


Figure 80: Phase domain model of the proposed subsampling PLL (SSPLL) with a sampling PD based on the proposed integrator. A VCDL is applied to stabilize the loop with noise contribution considered. (a) the VCDL is applied to the I-VCO signal. (b) the VCDL is applied to the feedback signal.

As shown in Figure 8.8, by introducing an additional degree of freedom in the design implementation from a gain controller into loop, the loop gain can be continuously adjusted with another parameter $\frac{\tau_{pulse}}{T_{ref}}$. As is shown in Equations (8.16) and (8.17), designers can always tune the duration of the pulse to optimize the values of K_{I-VCO} and K_D. Hence, we have the same degrees of freedom in design implementation as a charge-pump-based type-II PLL.

8.4.2. Different stabilization technique

Although using a VCDL as a stabilization technique is motivated by [114][115], the VCDL in our proposed architecture is applied to the I-VCO signal instead of the reference or the feedback

signal in [114][115]. This inherently eliminates the unit-gain buffer, which is used to reduce the kick-back noise in [114][115]. This not only reduces the power consumption and the silicon area, but also reduces the phase noise contribution of the VCDL as calculated below.

Figure 80 illustrates the phase domain model of the different scenarios. The open loop transfer functions of Figure 80 (a) has been calculated in Equation (8.12). The open loop transfer functions of Figure 80 (a) and Figure 80 (b) can be calculated as below:

$$T_{open-loop,a} = \mathrm{Y}(K_{I-VCO}\mathrm{s}^{-1} + K_D)K_{VCO}\mathrm{s}^{-1}, \tag{8.18}$$

$$T_{open-loop,b} = YK_{I-VCO}\mathrm{s}^{-1}(K_{VCO}\mathrm{s}^{-1} + K_D), \tag{8.19}$$

where $Y = K_{PD}\frac{\tau_{pulse}}{T_{ref}}K_{I-PD}$ is a constant number.

The difference between the two open loop transfer functions, by comparing Equations (8.18) with (8.19), can be obtained as $YK_D(K_{VCO} - K_{I-VCO})\mathrm{s}^{-1}$.

When apply a VCDL to the feedback signal as shown in Figure 80 (b), the phase noise transfer function can be calculated as:

$$\frac{\Phi_{n,out,b}}{\Phi_{n,VCDL}} = \frac{T_{forward}}{1 + T_{open-loop,b}} = \frac{K_{PD}\frac{\tau_{pulse}}{T_{ref}}K_{I-VCO}\mathrm{s}^{-1}K_{I-PD}K_{VCO}\mathrm{s}^{-1}}{1 + T_{open-loop,b}}$$

$$= \frac{YK_{I-VCO}\mathrm{s}^{-1}K_{VCO}\mathrm{s}^{-1}}{1+YK_{I-VCO}\mathrm{s}^{-1}(K_{VCO}\mathrm{s}^{-1}+K_D)}, \tag{8.20}$$

while the phase noise transfer function of Figure 80 (a) can be calculated as:

$$\frac{\Phi_{n,out,a}}{\Phi_{n,VCDL}} = \frac{T_{forward}}{1+T_{open-loop,a}} = \frac{K_{I-PD}K_{VCO}\mathrm{s}^{-1}}{1+T_{open-loop,a}} = \frac{K_{I-PD}K_{VCO}\mathrm{s}^{-1}}{1+Y(K_{I-VCO}\mathrm{s}^{-1}+K_D)K_{VCO}\mathrm{s}^{-1}}. \tag{8.21}$$

By comparing Equations (8.20) with (8.21), we can observe that the phase noise contribution from the VCDL is amplified by $K_{PD}\frac{\tau_{pulse}}{T_{ref}}K_{I-VCO}\mathrm{s}^{-1}\frac{1+T_{open-loop,a}}{1+T_{open-loop,b}}$ times if we use the VCDL at

the feedback signal instead of the I-VCO signal. It can also be observed that the transfer function in Equation (8.20) is band-pass in frequency domain, while the corresponding transfer function in Equation (8.21) for Figure 80 (b) has a low-pass response. Therefore, the VCDL in Figure 80 (a) has contributed less for the in-band phase noise because of the band-pass filtering property of the loop.

8.4.3. Comparisons with previous work

Researchers have proposed the use of a ring oscillator-based integrator inside a PLL in [128][129]. Instead of using a combination of charge pump and loop filter, this ring oscillator-based integrator was applied to implement the integral control path together with a conventional analog proportional path within a PLL. By combining the advantages of no quantization error of analog PLLs and small area of digital PLLs, the prototype PLL occupied the smallest reported active area of only 0.0021 mm^2 [128].

One main limitation of the proposed circuit architecture in [128][129] (as illustrated in Figure 71) is the spurious tones due to frequency offset between reference frequency and free-running frequency of the current controlled ring oscillator within the integral path ($CCRO_I$). If the free-running frequency of $CCRO_I$ is not equal to reference frequency, the loop will constantly sense the frequency difference and provide adequate control until the $CCRO_I$ frequency equals to the reference frequency. A non-zero I_{CCROI} in steady state requires non-zero PFD output, which means there has to be a constant phase offset when in lock. The constant phase offset, however, will result in modulation of $CCRO_M$ through proportional path and eventually lead to reference spur in frequency domain. Take a reference frequency of 275 MHz as an example, a 1% error in $CCRO_I$ free-running frequency translates to a reference spur of -27 dB, or a jitter of 12.9 ps for an output frequency of 2.2 GHz.

In our proposed circuit architecture, however, even the free-running frequency of the I-VCO is not equal to the reference frequency, the I-PD will constantly sense the frequency difference and a constant feedback need to be generated by the main PD. Different from [128][129] where a separate proportional path constantly modulates the $CCRO_M$, the VCDL is cascaded with the VCO-based integrator in our proposed circuit architecture and therefore no spurious tones will be

generated even in case of frequency offset between reference frequency and free-running frequency of the I-VCO.

It should also be mentioned that the spur generated from sampling behavior can be attenuated by adding an additional buffer between sampling PD and VCO, or adding another dummy sampling PD in parallel with the sampling PD to make the load of the VCO unchanged.

8.4.4. Phase noise compared to a charge-pump-based SSPLL

A major concern of the PLL is the phase noise performance. From the above discussion, the phase noise contribution from VCDL is bandpass filtered, which has improved the limited phase noise performance of the VCDL.

The phase noise performance is determined by both the in-band phase noise and the out-of-band phase noise. The in-band phase noise is usually determined by the loop components while the out-of-band phase noise is usually determined by the VCO. Since the most attractive property of a subsampling PLL is the reduced in-band phase noise performance, the bandwidth of a subsampling PLL is usually wide, i.e. around 3~5 MHz in [74]. In the following, we compare the phase noise performance of the subsampling PLL with a charge pump proposed in [74] and the subsampling PLL with a VCO-based integrator. To provide a fair comparison, we assume the same open loop transfer functions, the same loop bandwidth, and all the other modules inside the two loops (VCO, subsampling PD, FLL etc.) are identical. Since the open loop transfer functions are the same and the VCOs are identical, the out-of-band phase noise performance should also be the same. Therefore, we are going to limit our discussion to the in-band phase noise performance in the following subsections.

First, we calculate the open loop transfer functions of the two loops and set them to be equal, then we calculate the phase noise contributions from the charge pump and the VCO-based integrator, respectively. The phase noise contributed from the charge pump has a low-pass transfer function, while the phase noise contributed from the VCO-based integrator has a band-pass transfer function. If the phase noise contribution from the VCO-based integrator can be equal to the charge pump, then the in-band phase noise contribution of the VCO-based integrator will be smaller than that of the CP in the SSPLL because of the band-pass filtering property.

8.4.4.1. Open loop transfer functions

To provide a fair comparison, the open loop transfer functions of the two implementations should be the same, which means:

$$T_{open-loop,a} = T_{open-loop,SSPLL}. \tag{8.22}$$

Therefore, we have

$$\left(K_{PD}\frac{\tau_{pulse}}{T_{ref}}K_{I-PD}(K_{I-VCO}\mathrm{s}^{-1}+K_D)K_{VCO}\mathrm{s}^{-1}\right)_a = \left(K_{PD}\frac{\tau_{pulse}}{T_{ref}}I_{CP}(R+(\mathrm{sC})^{-1})K_{VCO}\mathrm{s}^{-1}\right)_{SSPLL}. \tag{8.23}$$

By using the same VCO and the same subsampling PD, Equation (8.23) can be simplified as:

$$\left(\frac{\tau_{pulse}}{T_{ref}}K_{I-PD}(K_{I-VCO}\mathrm{s}^{-1}+K_D)\right)_a = \left(\frac{\tau_{pulse}}{T_{ref}}I_{CP}(R+(\mathrm{sC})^{-1})\right)_{SSPLL} \tag{8.24}$$

From (8.24), we have:

$$\left(\frac{\tau_{pulse}}{T_{ref}}K_{I-PD}K_D\right)_a = \left(\frac{\tau_{pulse}}{T_{ref}}I_{CP}R\right)_{SSPLL}. \tag{8.25}$$

$$\left(\frac{\tau_{pulse}}{T_{ref}}K_{I-PD}K_{I-VCO}\right)_a = \left(\frac{\tau_{pulse}}{T_{ref}}\frac{I_{CP}}{C}\right)_{SSPLL}. \tag{8.26}$$

The phase noise contribution from a VCO-based integrator can be calculated as:

$$\frac{\Phi_{n,out,a}}{\Phi_{n,I-VCO}} = \frac{T_{forward}}{1+T_{open-loop}} = \frac{K_{I-PD}K_{VCO}\mathrm{s}^{-1}}{1+T_{open-loop}}, \tag{8.27}$$

A simple transformation can result in the following equation:

$$\Phi_{n,out,a} = \frac{K_{VCO}\mathrm{s}^{-1}}{1+T_{open-loop,a}}\,\Phi_{n,I-VCO}K_{I-PD} = \frac{K_{VCO}\mathrm{s}^{-1}}{1+T_{open-loop,a}}\,\frac{\Phi_{n,I-VCO}}{K_{I-VCO}}K_{I-VCO}K_{I-PD}. \tag{8.28}$$

Whereas the phase noise contribution from a charge pump can be calculated as:

$$\frac{\Phi_{n,out,SSPLL}}{I_{n,CP}} = \frac{T_{forward}}{1+T_{open-loop,SSPLL}} = \frac{\frac{\tau_{pulse}}{T_{ref}}(R+(\mathrm{sC})^{-1})K_{I-VCO}\mathrm{s}^{-1}}{1+T_{open-loop,SSPLL}}. \quad (8.29)$$

A simple transformation can result in the following equation:

$$\Phi_{n,out,SSPLL} = \frac{K_{VCO}\mathrm{s}^{-1}}{1+T_{open-loop,SSPLL}} I_{n,CP}(R+(\mathrm{sC})^{-1}) \frac{\left(\tau_{pulse}\right)_{SSPLL}}{T_{ref}}$$

$$= \frac{K_{VCO}\mathrm{s}^{-1}}{1+T_{open-loop,SSPLL}} \frac{I_{n,CP}}{I_{CP}} \left(I_{CP}R + \frac{I_{CP}}{sC}\right) \frac{\left(\tau_{pulse}\right)_{SSPLL}}{T_{ref}}. \quad (8.30)$$

Equation (8.28) has shown the phase noise contribution from the VCO-based integrator is band-pass filtered while (8.30) has shown the phase noise from the charge pump is low-pass filtered, as illustrated in Figure 81.

8.4.4.2. Phase noise @ 3dB bandwidth offset

Using the 3dB bandwidth from [74] of ω_{-3dB}= 5 M rad/s, we only need to compare the phase noise performance at 3dB bandwidth offset. As discussed above, the in-band phase noise contribution of the VCO integrator will be smaller than the CP in the SSPLL because of the band-pass filtering property, if the phase noise for the VCO-based integrator architecture is setup to be equal to the SSPLL.

For a frequency offset close to the loop bandwidth, from Equations (8.28) and (8.30), we only need to compare $\frac{I_{n,CP}}{I_{CP}}$ and $\frac{\Phi_{n,I-VCO}}{K_{I-VCO}}$.

Due to the superior CP noise suppression of the SSPLL circuit architecture, a small charge pump current $I_{CP} = 30\ \mu A$ was used in [74]. For a white noise current PSD normalized to the CP current, there is a general estimation in [130]:

$$\frac{I_{n,CP}}{I_{CP}} = 6 \times 10^{-19} \frac{A}{Hz}, \quad (8.31)$$

In [130], the phase noise of a ring oscillator can be calculated as:

$$L(f) = \frac{2kT}{I}\left(\frac{1}{V_{DD}-V_t}(\gamma_N + \gamma_P) + \frac{1}{V_{DD}}\right)\left(\frac{f_0}{f}\right)^2. \quad (8.32)$$

Take the simulation in Section 8.4.4 as an example, a 100MHz ring oscillator with a $K_{I-VCO} \approx 1$ MHz/V is used.

The pulse is set to be $\frac{\tau_{pulse}}{T_{ref}} = 0.05$ and V_{DD} is set to be 1.2V.

$$\frac{\Phi_{n,I-VCO}}{K_{I-VCO}} \approx \frac{\Phi_{n,I-VCO}}{1\times10^6} = \frac{2\times1.38\times10^{-23}}{1\times10^6 \times I}\left(\frac{4}{3}\times\frac{1}{1.2-0.4}+\frac{1}{1.2}\right)\left(\frac{100\text{ M}}{1\text{M}}\right)^2 = \frac{6.9\times10^{-23}}{I_{single-stage}}. \quad (8.33)$$

where $I_{single-stage}$ is the average current consumption of each stage of the I-VCO. For a similar phase noise performance at 5 MHz offset, by comparing Equations (8.31) and (8.33) we have the following result:

$$I = \frac{6.9\times10^{-23}}{6\times10^{-19}}\times\frac{1}{0.05} = 2.3\ mA. \quad (8.34)$$

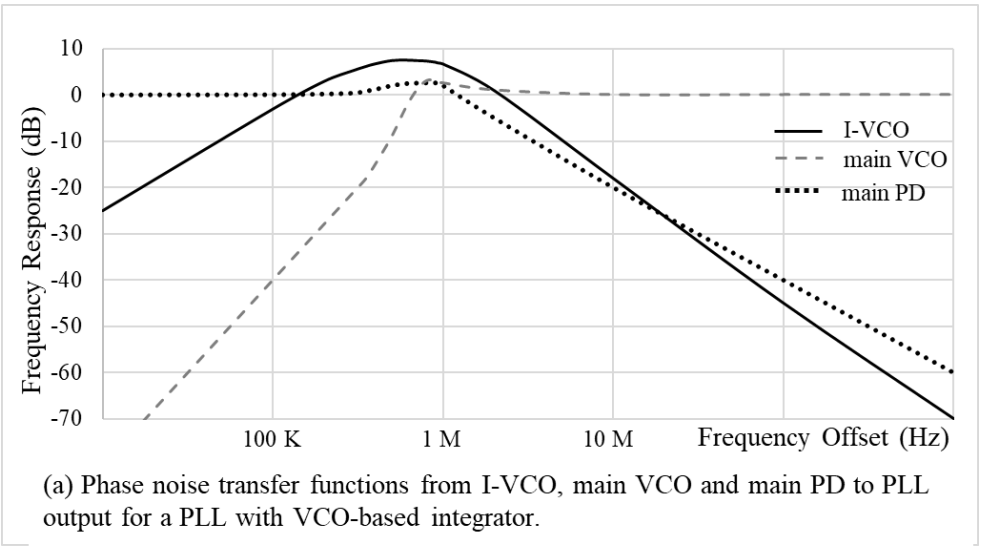
Take a 3-stage ring oscillator as an example, the total current consumption is

$$I_{total} = 6.9\ mA. \quad (8.35)$$

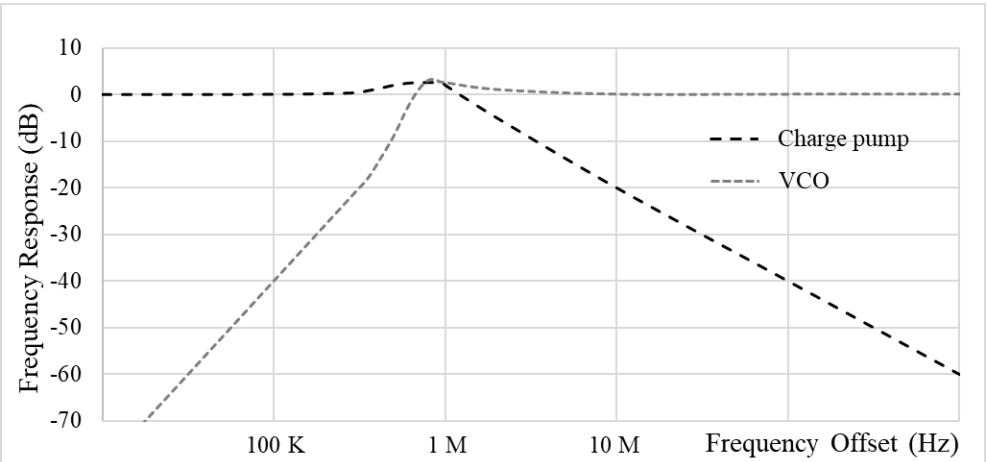
And the power consumption is

$$P_{total} = V_{DD} * I_{total} = 1.2\ V * 6.9\ mA = 8.3\ mW \quad (8.36)$$

For a frequency offset, which is much smaller than the loop bandwidth, the VCO-based integrator contributes a much smaller phase noise due to the band-pass transfer function shown in Figure 81 (a).



(a) Phase noise transfer functions from I-VCO, main VCO and main PD to PLL output for a PLL with VCO-based integrator.



(b) Phase noise transfer functions from charge pump and VCO to PLL output for a conventional Type-II PLL.

Figure 81: Phase noise transfer functions. (a) Phase noise transfer functions from I-VCO, main VCO and main PD to PLL output for a PLL with VCO-based integrator. (b) Phase noise transfer functions from charge pump and VCO to PLL output for a conventional Type-II PLL. It can be observed that the transfer function for the I-VCO is band-pass while the transfer function for the charge pump is low-pass in frequency domain.

For area comparison, a VCO-based integrator consists of an I-VCO, a VCDL and an I-PD, and the total area is less than 500 μm^2 in our proposed design in 130 nm process (from a full layout design of previous work). In the same process, the area of the corresponding charge pump is ~300μm^2 (not including capacitors of the loop filter).

Table 4: Comparison of a SSPLL with a VCO-based integrator and a charge-pump-based SSPLL (Note here the phase noise is set to be equal at $\omega_{offset} \approx \omega_{-3dB}$).

Architecture	**SSPLL with a VCO-based integrator [this work]**	**Charge-pump-based SSPLL [74]**
Phase noise at frequency offset equal to ω_{-3dB}	Set to be equal	
Phase noise at frequency offset smaller than ω_{-3dB}	Small	Medium
Power of integrator	Medium (8.3 mW)	Negligible ($30\ \mu A * 1.8V = 54\mu W$)
Total power (including integrator and other loop components)	16 mW	7.6 mW
Area of integrator (scaling to 130 nm CMOS process)	Negligible (~ 500 μm^2 for ring VCO-based integrators)	Large (~ 23,000 μm^2, adding 64% to the other active chip area in [155])

However, the loop filter in the charge-pump-based SSPLL takes much more area as shown in Table. 1. In [74] where a 180 nm process is used, the active area of the whole chip is 0.11 mm^2. Of that, the combined area of the PD, charge pump and reference buffer (measured on published die photo) is ~9,000 μm^2, the FLL takes ~5,000 μm^2, the VCO takes ~54,000 μm^2, while the loop filter area (dominated by two capacitors) is ~44,000 μm^2, which means the on-chip loop filter adds 64% to the total active chip area. If scaled to 130 nm process, the area of loop filter would be $\sim 44{,}000\ \mu m^2 * \left(\frac{130\text{nm}}{180\text{nm}}\right)^2 = 22{,}951\ \mu m^2$.

Existing FoM (Figure of Merit) evaluates tradeoff between power and phase noise. The proposed circuit architecture, however, is trading area for power, or vice versa. Table 4 summarizes the above discussion.

8.4.5. Phase noise compared to a conventional charge-pump-based PLL

In a conventional charge-pump-based PLL with a divider and PFD, loop noise, which is contributed from reference clock, PFD, charge pump, loop filter and divider, is low-pass filtered and dominant the in-band phase noise of the output. Among all these components, PFD and charge pump usually are major loop noise sources and the contributed noise is further amplified by N^2, where N is the division ratio. An SSPLL can avoid the multiplication of N^2 because the

divider is eliminated in phase domain for charge pump and PFD [74]. Note that N equals to 40 in [74] and 30 in the simulation illustrated below, this corresponds to 30~32dB increase of noise contributed from PFD and charge pump by calculating $10log\ (N^2)$.

From Equation (8.22), phase noise of I-VCO is proportional to $\frac{1}{I_{single-stage}}$. Therefore, to obtain the same phase noise performance compared to a conventional charge-pump-based PLL, the power consumption of the I-VCO can be greatly reduced by N^2 times lower.

$$I_{total,2} = \frac{I_{total}}{N^2} = \frac{6.9\ mA}{30^2} = 7.7\ \mu A. \tag{8.37}$$

The I-VCO power consumption is

$$P_{total} = V_{DD} * I_{total,2} = 1.2\ V * 7.7\ \mu A = 9.2\ \mu W, \tag{8.38}$$

which is negligible. In a conventional charge-pump-based PLL, the charge pump is turned on only at a small percentage of duty cycle and therefore the power consumption is also negligible.

Similar to a SSPLL with a VCO-based integrator, the transfer function of the VCO-based integrator to the output is band-pass filtered. Therefore, for a frequency offset that is much smaller than the loop bandwidth, the VCO-based integrator contributes a much smaller in-band phase noise. Furthermore, the in-band phase noise contribution from the PFD is different because the phase noise contribution from the PFD is not amplified by N^2 in the PLL with a VCO-based integrator.

Table 5: Comparison of a PLL with a VCO-based integrator vs. a conventional charge-pump-based PLL (Note here the phase noise is set to be equal when $\omega_{offset} \approx \omega_{-3dB}$).

Architecture	**PLL with a VCO-based integrator**	**Conventional charge-pump-based PLL**
Phase noise at frequency offset equal to ω_{-3dB}	Set to be equal	
Phase noise at frequency offset smaller than ω_{-3dB}	Small	Medium

Power of integrator	Negligible (9.2 µW)	Negligible
Area of integrator (scaling to 130 nm CMOS process)	Negligible (~ 500 μm^2 for ring VCO-based integrators)	Large (~ 680,000 μm^2 in [131])

For area comparison, as discussed previously, a VCO-based integrator consists of an I-VCO, a VCDL and an I-PD, with a total area is less than 500 μm^2 in our proposed circuit architecture in 130 nm process. For a conventional charge-pump-based PLL, the area of a charge pump and loop filter will be large. For instance, the loop filter takes ~170,000 μm^2 in 65 nm CMOS process (or ~680,000 μm^2 in 130 nm CMOS process) in [131]. Table 5 summarizes the above discussion.

8.5. Simulations

The SSPLL with a VCO-based integrator has been verified through a mixed analog simulation incorporating both VerilogA and transistor-level circuit models for key components with transistor noise modeled using Cadence Spectre. Schematic implementations of the FLL components were designed in the GlobalFoundries 130nm (formerly IBM 130nm) bulk CMOS process. The main VCO has a center frequency of 2.99 GHz and an equivalent gain of ~500 MHz/V by using a 4-bit digitally switched capacitor bank (VCO gain for a selected capacitor band of 50 MHz/V). A 100 MHz signal is used as the reference clock and the division ratio in the FLL is therefore set to be 30.

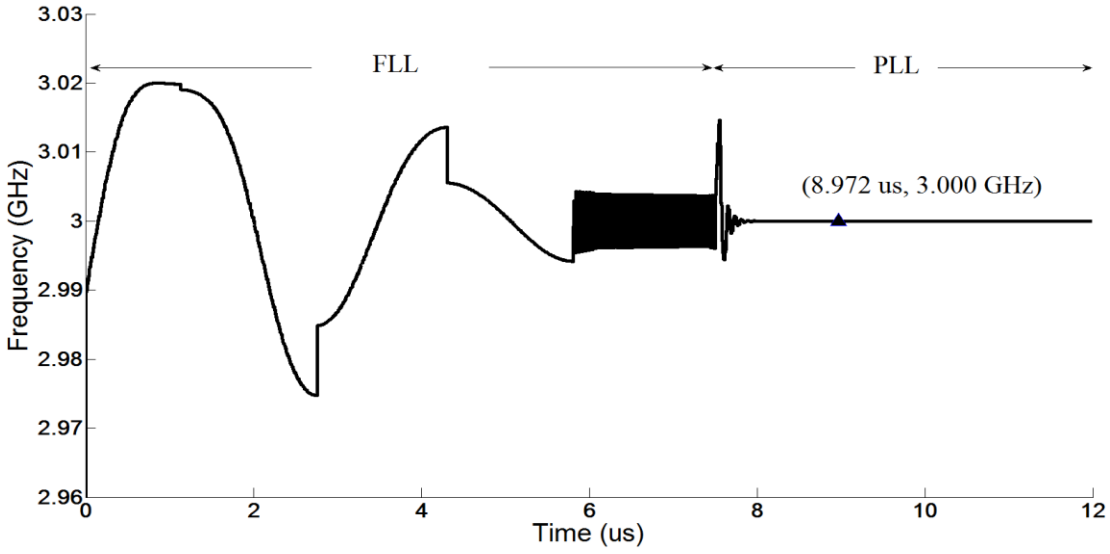


Figure 82: Spectre simulation shows the proposed SSPLL achieves lock at the desired frequency of 3.0 GHz [110].

Setting the loop bandwidth ω_{-3dB}= 5 M rad/s and ζ =1, we can have ω_n=$\frac{\omega_{-3dB}}{2.5} = 2\ \mathrm{Mrad/s}$. Compared to the reference clock period of 10 ns, the pulse width is set to be 500 ps, which results in a $\frac{\tau_{pulse}}{T_{ref}} = 0.05$. Then using Equations (8.16) and (8.17), we can obtain the values $K_{I-VCO} \approx 1\ \mathrm{MHz/V}$ and $K_D \approx 0.5\ rad/\mathrm{V}$. As shown in Figure 82, from 0 to 7.5 μs, the FLL is enabled and bring the loop into the desired state; while after t = 7.5 μs, the SSPLL is enabled and eventually the SSPLL achieves lock at the desired 3.0 GHz.

The area taken by the VCO-based integrator is ~ 500 μm^2 in GlobalFoundries 130 nm Bulk CMOS process, which is negligible compared to a relatively large area in a charge-pump-based SSPLL. For instance, the loop filter added 64% more of the total PLL active chip area in [74].

The area savings from the I-VCO architecture is at the cost of larger power consumption. To have a similar phase noise contribution at the 3dB bandwidth offset compared to a charge-pump-based SSPLL, a 100 MHz I-VCO with a power consumption of 8.3 mW should be selected, compared to a negligible power consumption of 54 μW in the charge pump and 7.6 mW in other loop components in [131]. Therefore, compared to a charge-pump-based SSPLL, an SSPLL with a VCO-based integrator saves the total area by 39% at a cost of 109% increase in total power consumption.

8.6. Conclusions

This proposed novel PLL circuit architecture employs a VCO as an integrator to replace the conventional charge pump and loop filter combination. Phase domain models are developed for analysis. To obtain one more degree of freedom in design implementation, a gain controller based on a pulse generator is developed to adjust the loop gain. Criteria for choosing the parameters are presented and the proposed architecture was simulated using Cadence Spectre.

Both the charge-pump-based SSPLL in [74] and charge-pump-based conventional PLL in [131]

are used as benchmarks of low phase noise performance and normal phase noise performance, respectively. An integrated loop filter in a charge-pump-based SSPLL can add 64% to the area of the active circuits (calculated for [74]). The proposed architecture saves the total area by 39% at a cost of 109% increase in total power consumption compared to a charge-pump-based SSPLL at similar phase noise performance. Compared to the loop filter taking ~680,000 μm^2 in 130 nm CMOS process for a charge-pump-based conventional PLL, the proposed architecture provides lower in-band phase noise with the filter taking less than 500 μm^2. The proposed circuit architecture has shown the possibility of trading power and phase noise for area (or vice versa), compared work that optimizes traditional power – phase noise FOM tradeoffs.

CHAPTER 9. Conclusions

In this chapter we summarize the contributions of this dissertation. The contributions of this dissertation are mainly to propose and discuss the digital sampling, improve the performance and cost of an ALL, and improve the performance and cost of a conventional PLL.

9.1. Contributions

9.1.1. Digital sampling

Analog RF subsampling, before being proposed to apply in frequency synthesis in 1999 [45], has mainly been used as mixing in applications such as wireless communications [132][133][134][135]. In this thesis dissertation we have proposed to directly digital sample the VCO signal for a frequency synthesizer. Digital sampling circuits have been analyzed, and characterization methodologies have been created. Simulation has shown that a digital sampler, implemented with a sense amplifier or a current mode logic (CML), can greatly extend the operating frequency when compared to static digital dividers implemented with the same circuit (i.e., through 130 GHz for circuit implemented in TSMC 40nm bulk CMOS process).

9.1.2. C-ALL, PS-CALL and D-ALL

We have proposed novel circuit architectures that we have named coresidual alias-locked loop (C-ALL), phase shift coresidual alias-locked loop (PS-CALL) and differential alias-locked loop (D-ALL), which employ digital sampling circuits instead of dividers. A C-ALL digitally produces the anticipated sampler output to reduce spurs (i.e., by as high as 27.7 dB in simulation), a PS-CALL guarantees feedback provided at every active edge of the alias signal to achieve fine phase lock, and a D-ALL locks on positive and negative alias frequencies to save the extra reference clock. These proposed circuits greatly extend the applications of SSPLLs, since previous work always has the limitation that, in lock, at the sampler, the sampled input frequency must be an integer multiple of the sampling clock (although each signal may be optionally processed through some frequency adjustment).

9.1.2.1. Coresidual Alias-Locked Loop

One significant drawback of an ALL is that the feedback signal may not be single-tone periodic in most cases, which introduces frequency spurs. To solve this problem, another circuit architecture that uses a digital circuit and the sampling clock to synthesize the reference signal is proposed. In the proposed circuit architecture, a digital alias signal is generated in the digital domain as the reference signal to replace the reference clock. The new circuit architecture implements a coresidual function and is therefore named as a coresidual alias-locked loop (C-ALL). By predicting the expected pattern of 1's and 0's and providing this signal to the phase detector, a C-ALL can significantly reduce the frequency spurs (e.g. by 27.7 dB in Chapter 5) compared to an ALL output. In addition, a C-ALL can also avoid of using the second reference clock.

9.1.2.2. Phase-Shift Coresidual Alias-Locked Loop

In a C-ALL, the high-frequency VCO signal is quantized or digitized by the lower-frequency sampling clock, which produces quantization errors. The C-ALL control loop has a "dead zone" in lock when the phases are close, but no net charge pump signal is generated. This dead zone results in only a coarse phase lock and no effective suppression of phase noise. To solve this problem, we propose a new type of locking mechanism and a new type of circuit architecture we call a Phase Shift Coresidual Alias-Locked Loop (PS-CALL), which guarantees feedback at every active edge of the alias signal, thus it eliminates the dead zone and achieves fine phase lock.

9.1.2.3. Differential Alias-Locked Loop

As mentioned, one drawback of an ALL is the requirement for one extra reference clock compared to a conventional PLL. A conventional PLL usually has only one clock that is used as the reference, while an ALL requires two clocks with one as the reference and the other as the sampling clock. We propose another circuit architecture named the differential alias-locked loop (D-ALL) to avoid the second reference clock. In a D-ALL, two feedback signals are generated from two samplers clocked at different sampling frequencies, and they are feeding into the phase frequency detector (PFD) and comparing with each other. As the sampling frequencies can be generated from the same clock signal, only one clock is needed in a D-ALL.

9.1.3. PLLs with VCO-based integrators

Additionally, we propose a new type of PLL circuit architecture with a VCO-based integrator to replace the charge pump and loop filter. This can avoid the large on-chip capacitor in loop filter, and also mitigate the VCO output spurs resulted from the voltage ripples on the loop filter output.

In a conventional PLL, the capacitor in the loop filter is usually large that is implemented either as an off-chip discrete component, or on-chip consuming significant silicon area. Both implementations increase the system cost. Moreover, the voltage ripples on the loop filter output can result in large spurs at the VCO output. To address these two issues, a new PLL circuit architecture is presented by using VCOs as integrators. Instead of using a charge pump and capacitor as the integrator, a VCO is used to implement the integrator with the phase being the output in the proposed PLL architecture. To ensure loop stability, a voltage-controlled delay line is developed to introduce a zero in the loop transfer function. The proposed circuit architecture saves silicon area without comprising power consumption or phase noise performance. For instance, a VCO-based integrator consisting of an I-VCO, a VCDL and an I-PD, takes a total area of less than 500 μm^2 in 130 nm process, compared to a loop filter area of ~170,000 μm^2 in 65 nm CMOS process or equivalently ~680,000 μm^2 in 130 nm CMOS process in [14].

9.2. Future work

First, since the high-frequency VCO signal is quantized by the digital sample clock in a PS-CALL, all the signals along the loop are digitized by the period or one-half period of the digital sample clock. Therefore, a PS-CALL is inherently friendly to be implemented as an all-digital circuit architecture. Figure 83 shows one possible circuit implementation of a digital PS-CALL.

Second, this work has discussed the basics of digital sampling and demonstrated the applications of digital sampling in PLLs. A digital sampler can be viewed as a combination of an analog sampler and a 1-bit ADC, thereby saving the normal ADCs with a sacrifice of precision. This kind of precision loss is suitable for many applications including continuous wave frequency modulated (CWFM) radars and frequency/phase modulation (FM/PM) communications.

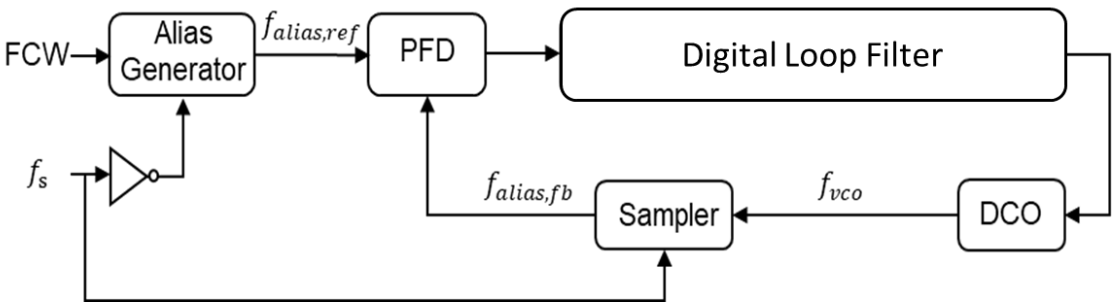


Figure 83: One possible implementation of a digital PS-CALL.

Third, VCOs have been used as integrators in ADCs, amplifiers and regulators in the past few years, and this dissertation has expanded its applications into PLLs. There could be potentially many more applications suitable for VCO-based integrators.

BIBLIOGRAPHY

[1] E. Seok, C. Cao, D. Shim, D. J. Arenas, D. B. Tanner, C. Hung, and K. K. O, "A 410GHz CMOS push-push oscillator with an on-chip patch antenna", IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), pp. 472-629, Feb. 2008.

[2] W. Steyaert and P. Reynaert, "A 0.54 THz Signal Generator in 40 nm Bulk CMOS With 22 GHz Tuning Range and Integrated Planar Antenna," in IEEE Journal of Solid-State Circuits, vol. 49, no. 7, pp. 1617-1626, July 2014, doi: 10.1109/JSSC.2014.2319251.

[3] T. D. Nguyen and J. Hong, "A High Fundamental Frequency Sub-THz CMOS Oscillator With a Capacitive Load Reduction Circuit," in IEEE Transactions on Microwave Theory and Techniques, vol. 68, no. 7, pp. 2655-2667, July 2020, doi: 10.1109/TMTT.2020.2987783.

[4] D. Shim, D. Koukis, D. J. Arenas, D. B. Tanner and K. O. Kenneth, "553-GHz signal generation in CMOS using a quadruple-push oscillator," IEEE Symposium on VLSI Circuits - Digest of Technical Papers, 2011, pp. 154-155.

[5] J. Chien and L. Lu, "40GHz wide-locking-range regenerative frequency divider and low-phase-noise balanced VCO in 0.18 um CMOS", IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), pp. 544-621, Feb. 2007.

[6] Y. Lin, C. Wu, C. Huang, C. Lu and Y. Wang, "Ultra-Wide Locking Range Regenerative Frequency Dividers With Quadrature-Injection Current-Mode-Logic Loop Divider," in IEEE Microwave and Wireless Components Letters, vol. 24, no. 3, pp. 179-181, March 2014, doi: 10.1109/LMWC.2013.2291864.

[7] C. -H. Shieh, K. -C. Tseng and T. -H. Huang, "Dual-Band 60-/24-GHz Signal Generator Using a Regenerative Miller Frequency Dividing System," 2018 Asia-Pacific Microwave Conference (APMC), 2018, pp. 138-140, doi: 10.23919/APMC.2018.8617198.

[8] K. Yamamoto and M. Fujishima, "70GHz CMOS harmonic injection-locked divider", IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), pp. 2472-2481, Feb. 2006.

[9] H. Chang, W. Chen, H. Yeh and I. Y. Shen, "A V-Band CMOS Low-DC-Power Wide-Locking-Range Divide-by-6 Injection-Locked Frequency Divider Using Transformer Coupling," in IEEE Microwave and Wireless Components Letters, vol. 30, no. 6, pp. 593-

596, June 2020, doi: 10.1109/LMWC.2020.2992107.

[10] A. Garghetti, A. L. Lacaita and S. Levantino, "A Novel Single-Inductor Injection-Locked Frequency Divider by Three With Dual-Injection Secondary Locking," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 5, pp. 1737-1745, May 2019, doi: 10.1109/TCSI.2018.2871178.

[11] B. Hong and A. Hajimiri, "A General Theory of Injection Locking and Pulling in Electrical Oscillators—Part II: Amplitude Modulation in LC Oscillators, Transient Behavior, and Frequency Division," in IEEE Journal of Solid-State Circuits, vol. 54, no. 8, pp. 2122-2139, Aug. 2019, doi: 10.1109/JSSC.2019.2908763.

[12] A. Garghetti, A. L. Lacaita, D. Seebacher, M. Bassi and S. Levantino, "A 13.6-69.1GHz 5.6mW Ring-Type Injection-Locked Frequency Divider by Five with >20% Continuous Locking Range and Operation up to 101.6GHz in 28nm CMOS," IEEE Custom Integrated Circuits Conference (CICC), 2021, pp. 1-2, doi: 10.1109/CICC51472.2021.9431565.

[13] Sadhu, B., et.al, "A linearized, low-phase-noise VCO-based 25-GHz PLL with autonomic biasing" in IEEE Journal of Solid-State Circuits, May, 2013, pp.1138-1150

[14] C. Lee, L. Kabalican, Y. Ge, H. Kwantono, G. Unruh, M. Chambers and I. Fujimori, "A 2.7GHz to 7GHz Fractional-N LCPLL Utilizing Multimetal Layer SoC Technology in 28nm CMOS" IEEE Symposium on VLSI Circuits, Digest of Technical Papers, pp. 71-72, 2014.

[15] L. van den Berg and D. G. Elliott, "An alias-locked loop frequency synthesis architecture", IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1536-1539, 18-21 May. 2008.

[16] J. Liang, Z. Zhou, J. Han and D. G. Elliott, “A 6.0-13.5 GHz Alias-Locked Loop Frequency Synthesizer in 130 nm CMOS,” IEEE Transactions on Circuits and Systems I, vol. 60, no. 1, pp. 108-115, 2013

[17] S. Cheng, H. Tong, J. Silva-Martinez and A. I. Karsilayan, "A fully differential low-power divide-by-8 injection-locked frequency divider up to 18 GHz", IEEE Journal of Solid-State Circuits, pp. 583-591, vol.42, no.3. 2007.

[18] R. J. Betancourt-Zamora, V. Shwetabh and T. H. Lee, "1-GHz and 2.8-GHz CMOS injection-locked ring oscillator prescalers", IEEE Symposium on VLSI Circuits, Digest of Technical Papers., pp. 47-50, Jun. 2001.

[19] K. Yamamoto and M. Fujishima, "A 44 mW 4.3-GHz injection-locked frequency divider

with 2.3-GHz locking range", IEEE Journal of Solid-State Circuits, vol.40, no.3, pp.671,677, March 2005.

[20] M. Tiebout, "A CMOS direct injection-locked oscillator topology as high-frequency low-power frequency divider", IEEE Journal of Solid-State Circuits, pp. 1170-1174, vol.39, no.7. July 2004.

[21] J. Lee, M. Liu and H. Wang, "A 75-GHz Phase-Locked Loop in 90-nm CMOS Technology", IEEE Journal of Solid-State Circuits, pp. 1414-1426, vol.43, no.6, June 2008.

[22] J. Lee, and B. Razavi, "A 40-GHz frequency divider in 0.18 um CMOS technology", IEEE Journal of Solid-State Circuits, pp. 594-601, vol.39, no.4, April 2004.

[23] A. R. Shahani et al., "Low-power dividerless frequency synthesis using aperture phase detection," in IEEE Journal of Solid-State Circuits, vol. 33, no. 12, pp. 2232-2239, Dec. 1998. doi: 10.1109/4.735707

[24] I.-T. Lee, et al., “A Dividerless Sub-Harmonically Injection-Locked PLL with Self-Adjusted Injection Timing,” ISSCC Dig. Tech. Papers, pp. 414-415, Feb. 2013.

[25] H. Yang, I. Y. Shen and H. Chang, "A K-band CMOS Low-Phase-Noise Sub-harmonically Injection-Locked QVCO with Divider-less Frequency-tracking Loop," 2019 IEEE MTT-S International Microwave Symposium (IMS), 2019, pp. 377-380, doi: 10.1109/MWSYM.2019.8700923.

[26] X. Gao, E. A. M. Klumperink, M. Bohsali and B. Nauta, "A 2.2GHz 7.6mW sub-sampling PLL with -126dBc/Hz in-band phase noise and 0.15ps rms jitter in 0.18 um CMOS", IEEE International Solid-State Circuits Conference - Digest of Technical Papers (ISSCC), pp.392-393,393a, 8-12 Feb. 2009.

[27] X. Gao, E. A. M. Klumperink, G. Socci, M. Bohsali and B. Nauta, "Spur-reduction techniques for PLLs using sub-sampling phase detection", IEEE International Solid-State Circuits Conference - Digest of Technical Papers (ISSCC), pp.474-475, 7-11 Feb. 2010.

[28] Q. Shi, K. Bunsen, N. Markulic and J. Craninckx, "A Self-Calibrated 16GHz Subsampling-PLL-Based 30s Fast Chirp FMCW Modulator with 1.5GHz Bandwidth and 100kHz rms Error," IEEE International Solid-State Circuits Conference - Digest of Technical Papers (ISSCC), 2019, pp. 408-410, doi: 10.1109/ISSCC.2019.8662348.

[29] H. Ting and T. Lee, "A 5.25GHz Subsampling PLL with a VCO-Phase-Noise Suppression Technique," IEEE International Solid-State Circuits Conference - Digest of Technical Papers

(ISSCC), 2020, pp. 390-392, doi: 10.1109/ISSCC19947.2020.9063009.

[30] Y. Lim et al., "A 170MHz-Lock-In-Range and −253dB-FoMjitter 12-to-14.5GHz Subsampling PLL with a 150μW Frequency-Disturbance-Correcting Loop Using a Low-Power Unevenly Spaced Edge Generator," IEEE International Solid-State Circuits Conference - Digest of Technical Papers (ISSCC), 2020, pp. 280-282, doi: 10.1109/ISSCC19947.2020.9062921.

[31] P. Huang, W. Chang and T. Lee, "A 2.3GHz fractional-N dividerless phase-locked loop with −112dBc/Hz in-band phase noise," IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014, pp. 362-363, doi: 10.1109/ISSCC.2014.6757470.

[32] Q. Shi, K. Bunsen, N. Markulic and J. Craninckx, "A Self-Calibrated 16GHz Subsampling-PLL-Based 30s Fast Chirp FMCW Modulator with 1.5GHz Bandwidth and 100kHz rms Error," IEEE Journal of Solid-State Circuits, vol. 54, no. 12, pp. 3503-3512, Dec. 2019, doi: 10.1109/JSSC.2019.2941113.

[33] K. Raczkowski, et al, "A 9.2–12.7 GHz Wideband Fractional-N Subsampling PLL in 28 nm CMOS with 280 fs RMS Jitter," IEEE Journal of Solid-State Circuits, vol. 50, no. 5, pp. 1203-1213, May 2015.

[34] N. Markulic et al., "A DTC-Based Subsampling PLL Capable of Self-Calibrated Fractional Synthesis and Two-Point Modulation," in IEEE Journal of Solid-State Circuits, vol. 51, no. 12, pp. 3078-3092, Dec. 2016, doi: 10.1109/JSSC.2016.2596766.

[35] D. Liao, F. F. Dai, B. Nauta and E. Klumperink, "Multi-phase sub-sampling fractional-N PLL with soft loop switching for fast robust locking," IEEE Custom Integrated Circuits Conference (CICC), 2017, pp. 1-4, doi: 10.1109/CICC.2017.7993633.

[36] A. Tharayil Narayanan et al., "A Fractional-N Sub-Sampling PLL using a Pipelined Phase-Interpolator with an FoM of -250dB," IEEE Journal of Solid-State Circuits, vol. 51, no. 7, pp. 1630-1640, July 2016.

[37] X. Yi et al., "A 93.4–104.8-GHz 57-mW Fractional-N Cascaded PLL With True In-Phase Injection-Coupled QVCO in 65-nm CMOS Technology," in IEEE Transactions on Microwave Theory and Techniques, vol. 67, no. 6, pp. 2370-2381, June 2019, doi: 10.1109/TMTT.2019.2906614.

[38] J. Kim et al., "A 76fsrms Jitter and –40dBc Integrated-Phase-Noise 28-to-31GHz Frequency Synthesizer Based on Digital Sub-Sampling PLL Using Optimally Spaced Voltage

Comparators and Background Loop-Gain Optimization," IEEE International Solid-State Circuits Conference - Digest of Technical Papers (ISSCC), San Francisco, CA, USA, 2019, pp. 258-260, doi: 10.1109/ISSCC.2019.8662532.

[39] V. Szortyka, Q. Shi, K. Raczkowski, B. Parvais, M. Kuijk and P. Wambacq, "A 42 mW 200 fs-Jitter 60 GHz Sub-Sampling PLL in 40 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 50, no. 9, pp. 2025-2036, Sept. 2015, doi: 10.1109/JSSC.2015.2442998.

[40] T. Siriburanon et al., "A 60-GHz sub-sampling frequency synthesizer using sub-harmonic injection-locked quadrature oscillators," IEEE Radio Frequency Integrated Circuits Symposium, Tampa, FL, USA, 2014, pp. 105-108, doi: 10.1109/RFIC.2014.6851670.

[41] T. Siriburanon et al., "A Low-Power Low-Noise mm-Wave Subsampling PLL Using Dual-Step-Mixing ILFD and Tail-Coupling Quadrature Injection-Locked Oscillator for IEEE 802.11ad," in IEEE Journal of Solid-State Circuits, vol. 51, no. 5, pp. 1246-1260, May 2016, doi: 10.1109/JSSC.2016.2529004.

[42] V. Szortyka, Q. Shi, K. Raczkowski, B. Parvais, M. Kuijk and P. Wambacq, "A 42 mW 200 fs-Jitter 60 GHz Sub-Sampling PLL in 40 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 50, no. 9, pp. 2025-2036, Sept. 2015, doi: 10.1109/JSSC.2015.2442998.

[43] Z. -Z. Chen et al., "Sub-sampling all-digital fractional-N frequency synthesizer with −111dBc/Hz in-band phase noise and an FOM of −242dB," IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, 2015, pp. 1-3, doi: 10.1109/ISSCC.2015.7063029.

[44] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori and A. L. Lacaita, "A 2.9-to-4.0GHz fractional-N digital PLL with bang-bang phase detector and 560fsrms integrated jitter at 4.5mW power," IEEE International Solid-State Circuits Conference - Digest of Technical Papers (ISSCC), 2011, pp. 88-90, doi: 10.1109/ISSCC.2011.5746231.

[45] A. N. Hafez and M. I. Elmasry, "A low power monolithic sampled phase-locked loop architecture for wireless transceivers", IEEE International Symposium on Circuits and Systems (ISCAS), pp. 549-552 vol.2, Jul. 1999.

[46] T. H. Lee, "The design of CMOS radio-frequency integrated circuits", Cambridge University press, 2004.

[47] P. Y. Chan, A. Rofougaran, K. A. Ahmed and A. A. Abidi, "A highly linear 1-GHz CMOS downconversion mixer", Nineteenth European Solid-State Circuits Conference (ESSCIRC),

pp. 210-213, Sep. 1993.

[48] B. Murmann, "Digitally assisted analog circuits", IEEE Micro, pp. 38-47, vol.26, no.2, 2006.

[49] M. Skolnik, "Radar handbook, Third Edition", McGraw-Hill Professional, Janauary 2008.

[50] H. J. Kim, J. U. Kim, J. H. Kim, H. Wangand I. S. Lee, "The design method and performance analysis of RF sampling frontend for SDR/CR receivers", IEEE Transactions on Industrial Electronics, pp. 1518-1525, vol.57, no.5, 2010.

[51] L. Smaini and D. Helal, "RF Digital Transceiver for Impulse Radio Ultra Wide Band Communications", European Solid-State Circuits Conference (ESSCIRC), September, Leuven, Belgium, 2004.

[52] S. Hoyos, B. M. Sadler and R. A. Gonzalo, "Monobit digital receivers for ultra-wideband communications", IEEE Transactions on Wireless Communications, pp. 1337-1344, vol.4, no.4, 2005.

[53] M. Matsui, H. Hara, Y. Uetani, L. Kim, T. Nagamatsu, Y. Watanabe, A. Chiba, K. Matsuda and T. Sakurai, "A 200 MHz 13 mm^2 2-D DCT macrocell using sense-amplifying pipeline ip-op scheme", IEEE Journal of Solid-State Circuits, vol. 29, no. 12, pp. 1482-1490, Dec. 1994.

[54] B. Nikolic, V. G. Oklobdzija,V. Stojanovic, W. Jia, J. Chiu and M. Leung, "Improved sense-amplier-based flip-flop: design and measurements", IEEE Journal of Solid-State Circuits, vol. 35, no. 6, pp. 876-884, JUN. 2000.

[55] B. Razavi, "The StrongARM Latch [A Circuit for All Seasons]," in IEEE Solid-State Circuits Magazine, vol. 7, no. 2, pp. 12-17, Spring 2015, doi: 10.1109/MSSC.2015.2418155.

[56] S. Suzuki and M. Hirata, "Threshold Difference Compensated Sense Amplifier", IEEE Journal of Solid-State Circuits, vol. 14, no. 6, pp. 1066-1070, Jun. 1979.

[57] N. Ieda, Y. Ohmori, K. Takeya and T. Yano, "Single Transistor MOS RAM Using a Short-Channel MOS Transistor", IEEE Journal of Solid-State Circuits, vol. 13, no. 2, pp.218-224, Feb. 1978.

[58] Brijesh A Shah, "Power Supply Noise and Clock Generator", Cypress Semiconductor White Paper

[59] P. Nuzzo, F. De Bernardinis, P. Terreni and G. Van der Plas, "Noise Analysis of Regenerative Comparators for Reconfigurable ADC Architectures," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 55, no. 6, pp. 1441-1454, July 2008.

[60] M. Jeeradit et al., "Characterizing sampling aperture of clocked comparators," IEEE Symposium on VLSI Circuits, Digest of Technical Papers, HI, USA, 2008, pp. 68-69, doi: 10.1109/VLSIC.2008.4585955.

[61] T. Toifl et al., "A 22-Gb/s PAM-4 receiver in 90-nm CMOS SOI technology," in IEEE Journal of Solid-State Circuits, vol. 41, no. 4, pp. 954-965, April 2006, doi: 10.1109/JSSC.2006.870898.

[62] J. Kim, B. S. Leibowitz and M. Jeeradit, "Impulse sensitivity function analysis of periodic circuits," IEEE/ACM International Conference on Computer-Aided Design, 2008, pp. 386-391, doi: 10.1109/ICCAD.2008.4681602.

[63] J. Liang and D. G. Elliott, "Coresidual alias-locked loops," IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, 2016, pp. 9-12.

[64] Y. Zhao et al., "A 0.56 THz Phase-Locked Frequency Synthesizer in 65 nm CMOS Technology," in IEEE Journal of Solid-State Circuits, vol. 51, no. 12, pp. 3005-3019, Dec. 2016.

[65] L. Kong and B. Razavi, "A 2.4 GHz 4 mW Integer-N Inductorless RF Synthesizer," in IEEE Journal of Solid-State Circuits, vol. 51, no. 3, pp. 626-635, March 2016.

[66] T. Riley, M. Copeland, T. Kwasniewski, "Delta-sigma modulation in fractional-N frequency synthesis", IEEE Journal of Solid-State Circuits, vol. 28, no. 5, pp. 553-559, May 1993.

[67] E. Familier and I. Galton, "Second and Third-Order Noise Shaping Digital Quantizers for Low Phase Noise and Nonlinearity-Induced Spurious Tones in Fractional-N PLLs," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 6, pp. 836-847, June 2016.

[68] Y. H. Choi, B. Kim, J. Y. Sim and H. J. Park, "A Phase-Interpolator-Based Fractional Counter for All-Digital Fractional-N Phase-Locked Loop," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 3, pp. 249-253, March 2017.

[69] A. Li; Y. Chao; X. Chen; L. Wu; H. C. Luong, "A Spur-and-Phase-Noise-Filtering Technique for Inductor-Less Fractional-N Injection-Locked PLLs," in IEEE Journal of Solid-State Circuits, vol.PP, no.99, pp.1-13, April 2017

[70] A. Bonfanti, F. Amorosa, C. Samori and A. L. Lacaita, "A DDS-based PLL for 2.4-GHz frequency synthesis," in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 50, no. 12, pp. 1007-1010, Dec. 2003.

[71] Kan, T.K.K.; Leung, G.C.T.; Luong, H.C., "A 2 V 1.8 GHz fully integrated CMOS dual-loop frequency synthesizer," IEEE Journal of Solid-State Circuits, vol.37, no.8, pp.1012,1020, Aug 2002

[72] W. S. T. Yan and H. C. Luong, "A 2-V 900-MHz Monolithic CMOS Dual-Loop Frequency Synthesizer for GSM Receivers," IEEE Journal of Solid-State Circuits, vol. 36, no. 2, pp. 204-216, Feb. 2001.

[73] Zhinian Shu, Ka Lok Lee and B. H. Leung, "A 2.4-GHz ring-oscillator-based CMOS frequency synthesizer with a fractional divider dual-PLL architecture," in IEEE Journal of Solid-State Circuits, vol. 39, no. 3, pp. 452-462, March 2004.

[74] X. Gao, E. A. M. Klumperink, M. Bohsali and B. Nauta, "A Low Noise Sub-Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is Not Multiplied by N^2," in IEEE Journal of Solid-State Circuits, vol. 44, no. 12, pp. 3253-3263, Dec. 2009.

[75] B. Jiang and H. C. Luong, "A 23-mW 60-GHz Differential Sub-Sampling PLL with an NMOS-Only Differential-Inductively-Tuned VCO," IEEE Asian Solid-State Circuits Conference (A-SSCC), Macau, Macao, 2019, pp. 279-282, doi: 10.1109/A-SSCC47793.2019.9056968.

[76] X. Liu and H. C. Luong, "A Fully Integrated 0.27-THz Injection-Locked Frequency Synthesizer With Frequency-Tracking Loop in 65-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 55, no. 4, pp. 1051-1063, April 2020, doi: 10.1109/JSSC.2019.2954232.

[77] A. Abidi and H. Xu, "Understanding the regenerative comparator circuit," Proceedings of the IEEE Custom Integrated Circuits Conference (CICC), San Jose, CA, 2014, pp. 1-8.

[78] L. van den Berg, "A High-Speed Alias-Locked Loop Frequency Synthesis Architecture" Master Thesis, University of Alberta, 2008.

[79] Bi, Chuang, and Orla Feely. "Nonlinear dynamics of alias-locked loop." European Conference on Circuit Theory and Design, 2009: 343-346.

[80] X. Gao, E. Klumperink and B. Nauta, "Sub-sampling PLL techniques," IEEE Custom Integrated Circuits Conference (CICC), San Jose, CA, 2015, pp. 1-8.

[81] N. Markulic et al., "A self-calibrated 10MB/S phase modulator with -37.4dB EVM based on a 10.1-to-12.4GHz, -246.6dB-FoM, fractional-N subsampling PLL," 2016 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2016, pp. 176-177.

[82] A. Paidimarri, N. Ickes and A. P. Chandrakasan, "A 0.68V 0.68mW 2.4GHz PLL for ultra-low power RF systems," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Phoenix, AZ, 2015, pp. 397-400, doi: 10.1109/RFIC.2015.7337789.

[83] N. Pourmousavian, F. Kuo, T. Siriburanon, M. Babaie and R. B. Staszewski, "A 0.5-V 1.6-mW 2.4-GHz Fractional-N All-Digital PLL for Bluetooth LE With PVT-Insensitive TDC Using Switched-Capacitor Doubler in 28-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 53, no. 9, pp. 2572-2583, Sept. 2018, doi: 10.1109/JSSC.2018.2843337.

[84] T. Kuan and S. Liu, "A Bang Bang Phase-Locked Loop Using Automatic Loop Gain Control and Loop Latency Reduction Techniques," in IEEE Journal of Solid-State Circuits, vol. 51, no. 4, pp. 821-831, April 2016.

[85] D. Cherniak et al., "A 15.6-18.2 GHz Digital Bang-Bang PLL with −63dBc in-Band Fractional Spur," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Philadelphia, PA, 2018, pp. 36-39

[86] X. Gao, E. A. M. Klumperink, G. Socci, M. Bohsali, and B. Nauta,“Spur reduction techniques for phase-locked loops exploiting a subsampling phase detector,” IEEE Journal of Solid-State Circuits, vol. 45, no. 9, pp. 1809–1820, Sep. 2010.

[87] J. Sharma and H. Krishnaswamy, "A 2.4-GHz Reference-Sampling Phase-Locked Loop That Simultaneously Achieves Low-Noise and Low-Spur Performance," in IEEE Journal of Solid-State Circuits, vol. 54, no. 5, pp. 1407-1424, May 2019.

[88] D. Cherniak, L. Grimaldi, L. Bertulessi, R. Nonis, C. Samori and S. Levantino, "A 23-GHz Low-Phase-Noise Digital Bang–Bang PLL for Fast Triangular and Sawtooth Chirp Modulation," in IEEE Journal of Solid-State Circuits, vol. 53, no. 12, pp. 3565-3575, Dec. 2018.

[89] Jaeha Kim, Jeong-Kyoum Kim, Bong-Joon Lee, Namhoon Kim, Deog-Kyoon Jeong and W. Kim, "A 20-GHz phase-locked loop for 40-gb/s serializing transmitter in 0.13um CMOS," in IEEE Journal of Solid-State Circuits, vol. 41, no. 4, pp. 899-908, April 2006, doi: 10.1109/JSSC.2006.870766.

[90] Y. Lin, J. Tsai, Y. Kuo and T. Huang, "An ultra low-power 24 GHz Phase-lock-loop with low phase-noise VCO embedded in 0.18 μm CMOS process," Asia-Pacific Microwave Conference, 2011, pp. 1630-1633.

[91] J. Cheng, M. Wu, H. Huang, Y. Wu, J. Tsai and T. Huang, "A K-band phase-locked loop in

0.18 μm CMOS technology for vital sign detection radar," IEEE MTT-S International Microwave Workshop Series on RF and Wireless Technologies for Biomedical and Healthcare Applications (IMWS-Bio2014), 2014, pp. 1-3, doi: 10.1109/IMWS-BIO.2014.7032400.

[92] J. Luo, L. Zhang, L. Zhang, Y. Wang and Z. Yu, "A 24GHz low power and low phase noise PLL frequency synthesizer with constant KVCO for 60GHz wireless applications," IEEE International Symposium on Circuits and Systems (ISCAS), 2015, pp. 2840-2543, doi: 10.1109/ISCAS.2015.7169278.

[93] J. Liang and D. G. Elliott, "Frequency Synthesis Based on A Novel Differential Locking Mechanism," IEEE International Symposium on Circuits and Systems (ISCAS), Florence, May 28 - 31, 2018.

[94] T. Riley, M. Copeland, T. Kwasniewski, "Delta-sigma modulation in fractional-N frequency synthesis", IEEE Journal of Solid-State Circuits, vol. 28, no. 5, pp. 553-559, May 1993.

[95] E. Familier and I. Galton, "Second and Third-Order Noise Shaping Digital Quantizers for Low Phase Noise and Nonlinearity-Induced Spurious Tones in Fractional-N PLLs," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 6, pp. 836-847, June 2016.

[96] Z. Zong, P. Chen and R. B. Staszewski, "A Low-Noise Fractional-N Digital Frequency Synthesizer With Implicit Frequency Tripling for mm-Wave Applications," in IEEE Journal of Solid-State Circuits, vol. 54, no. 3, pp. 755-767, March 2019.

[97] Y. H. Choi, B. Kim, J. Y. Sim and H. J. Park, "A Phase-Interpolator-Based Fractional Counter for All-Digital Fractional-N Phase-Locked Loop," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 3, pp. 249-253, March 2017.

[98] A. Li; Y. Chao; X. Chen; L. Wu; H. C. Luong, "A Spur-and-Phase-Noise-Filtering Technique for Inductor-Less Fractional-N Injection-Locked PLLs," in IEEE Journal of Solid-State Circuits, vol.PP, no.99, pp.1-13, April 2017

[99] “ 5G Spectrum Recommendations” August 2015, Online access: http://www.4gamericas.org/files/6514/3930/9262/4G_Americas_5G_Spectrum_Recommendations_White_Paper.pdf

[100] Farjadrad R, Dally W J, Ng H, et al. "A low-power multiplying DLL for low-jitter multigigahertz clock generation in highly integrated digital chips". IEEE Journal of Solid-

state Circuits, 2002, 37(12): 1804-1812.

[101] Elshazly A, Inti R, Young B, et al. “Clock Multiplication Techniques Using Digital Multiplying Delay-Locked Loops”. IEEE Journal of Solid-state Circuits, 2013, 48(6): 1416-1428.

[102] Zhang X, Zhou X, Daryoush A S, et al. "A theoretical and experimental study of the noise behavior of subharmonically injection locked local oscillators". IEEE Transactions on Microwave Theory and Techniques, 1992, 40(5): 895-902.

[103] J. Cheng, N. Qi, P. Chiang and A. Natarajan, “A 1.3mW 0.6V WBAN-Compatible Sub-Sampling PSK Receiver in 65nm CMOS", IEEE International Solid-State Circuits Conference - Digest of Technical Papers (ISSCC), pp.168-169, 8-12 Feb. 2014.

[104] W. Wu et al., "A 28-nm 75-fsrms Analog Fractional-N Sampling PLL With a Highly Linear DTC Incorporating Background DTC Gain Calibration and Reference Clock Duty Cycle Correction," in IEEE Journal of Solid-State Circuits, vol. 54, no. 5, pp. 1254-1265, May 2019.

[105] Chien J, Lu L. "Analysis and Design of Wideband Injection-Locked Ring Oscillators With Multiple-Input Injection". IEEE Journal of Solid-state Circuits, 2007, 42(9): 1906-1915.

[106] Mesgarzadeh B, Alvandpour A. "First-Harmonic Injection-Locked Ring Oscillators". IEEE Custom Integrated Circuits Conference (CICC), 2006: 733-736.

[107] K. Hu, T. Jiang, J. Wang, F. O`Mahony and P. Chiang, “A 0.6 mW per Gb/s, 6.4-7.2 Gb/s Serial Link Receiver Using Local Injection-Locked Ring Oscillators in 90 nm CMOS”, IEEE Journal of Solid-State Circuits, vol. 45, no. 4, pp. 899-908, Apr. 2010.

[108] Jang S, Chuang Y, Lee S H, et al. “An Integrated 5–2.5-GHz Direct-Injection Locked Quadrature LC-VCO”. IEEE Microwave and Wireless Components Letters, 2007, 17(2): 142-144 .

[109] Y. Ding and K. K. O, "A 21-GHz 8-Modulus Prescaler and a 20-GHz Phase-Locked Loop Fabricated in 130-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 42, no. 6, pp. 1240-1249, June 2007.

[110] J. Liang and D. G. Elliott, "VCO-based integrator PLL [Technical Program]," IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, 2016, pp. 1-4. doi: 10.1109/ISCAS. 2016. 7720798

[111] Behzad Razavi, “Design of Analog CMOS Integrated Circuits 1st Edition”, McGraw-Hill

Education, 2nd Edition.

[112] Sadhu, B., et.al, "A linearized, low-phase-noise VCO-based 25-GHz PLL with autonomic biasing" IEEE Journal of Solid-State Circuits, May, 2013, pp.1138-1150

[113] C. Lee, L. Kabalican, Y. Ge, H. Kwantono, G. Unruh, M. Chambers and I. Fujimori, "A 2.7 GHz to 7 GHz Fractional-N LC-PLL Utilizing Multimetal Layer SoC Technology in 28nm CMOS" IEEE Symposium on VLSI Circuits, Digest of Technical Papers, 2014, pp. 71-72.

[114] Thomas H. Lee, and John F. Bulzacchelli, "A 155-MHz Clock Recovery Delay- and Phase-Locked Loop" IEEE Journal of Solid-State Circuits, vol. 27, no. 12, pp. 1736-1746, December, 1992

[115] Alireza Zolfaghari, Andrew Chan, Behzad Razavi, “A 2.4GHz 34mW CMOS Transceiver for Frequency Hopping and Direct-Sequence Applications” IEEE International Solid-State Circuits Conference - Digest of Technical Papers (ISSCC), 2001

[116] Tai-Cheng Lee; Razavi, B., "A stabilization technique for phase-locked frequency synthesizers," IEEE Journal of Solid-State Circuits, vol.38, no.6, pp.888-894, June 2003

[117] C. Hsu, M. Z. Straayer and M. H. Perrott, "A Low-Noise Wide-BW 3.6-GHz Digital ΔΣ Fractional-N Frequency Synthesizer With a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation," in IEEE Journal of Solid-State Circuits, vol. 43, no. 12, pp. 2776-2786, Dec. 2008, doi: 10.1109/JSSC.2008.2005704.

[118] Minjae Lee; Heidari, M.E.; Abidi, A.A., "A Low-Noise Wideband Digital Phase-Locked Loop Based on a Coarse–Fine Time-to-Digital Converter With Subpicosecond Resolution," in IEEE Journal of Solid-State Circuits, vol.44, no.10, pp.2808,2816, Oct. 2009

[119] Wei Liu; Wei Li; Peng Ren; Chinglong Lin; Shengdong Zhang; Yangyuan Wang, "A PVT Tolerant 10 to 500 MHz All-Digital Phase-Locked Loop With Coupled TDC and DCO," in IEEE Journal of Solid-State Circuits, vol.45, no.2, pp.314,321, Feb. 2010

[120] B. Drost, M. Talegaonkar and P. K. Hanumolu, "A 0.55V 61dB-SNR 67dB-SFDR 7MHz 4th-order Butterworth filter using ring-oscillator-based integrators in 90nm CMOS," IEEE International Solid-State Circuits Conference - Digest of Technical Papers (ISSCC), San Francisco, CA, 2012, pp. 360-362.

[121] B. Drost, M. Talegaonkar and P. K. Hanumolu, "Analog Filter Design Using Ring Oscillator Integrators," in IEEE Journal of Solid-State Circuits, vol. 47, no. 12, pp. 3120-

3129, Dec. 2012.

[122] Park, M.; Perrott, M.H. “A 78 dB SNDR 87 mW 20 MHz Bandwidth Continuous-Time ΔΣ ADC With VCO-Based Integrator and Quantizer Implemented in 0.13 μm CMOS” IEEE Journal of Solid-State Circuits, Dec. 2009

[123] Straayer, M.Z.; Perrott, M.H., "A 10-bit 20MHz 38mW 950MHz CT ΣΔ ADC with a 5-bit noise-shaping VCO-based quantizer and DEM circuit in 0.13 μm cmos," IEEE Symposium on VLSI Circuits, Digest of Technical Papers, vol., no., pp.246,247, 14-16 June 2007

[124] Naiknaware, R.; Haiming Tang; Fiez, T.S., "Time-referenced single-path multi-bit ΔΣ ADC using a VCO-based quantizer," Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on, vol.47, no.7, pp.596,602, Jul 2000

[125] J. Hamilton, S. Yan, T. R. Viswanathan, "A Discrete-Time Input ΔΣADC Architecture Using a Dual-VCO-Based Integrator", IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 57, Issue 11, Nov. 2010

[126] Peng Zhu ; Xinpeng Xing ; Georges Gielen, "A 40-MHz Bandwidth 0–2 MASH VCO-Based Delta-Sigma ADC With 35-fJ/Step FoM", IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 62, Issue 10, Oct. 2015

[127] Z. Dai, S. Gupta, S. Kalani and P. R. Kinget "3.7μW 0.8V VCO-integrator-based high-efficiency capacitor-free low-dropout voltage regulator" IEEE International Symposium on Circuits and Systems (ISCAS), 22-25 May 2016

[128] J. Zhu, R. K. Nandwana, G. Shu, A. Elkholy, S. J. Kim and P. K. Hanumolu, "A 0.0021 mm^2 1.82 mW 2.2 GHz PLL Using Time-Based Integral Control in 65 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 52, no. 1, pp. 8-20, Jan. 2017, doi: 10.1109/JSSC.2016.2598768.

[129] J. Chuang and H. Krishnaswamy, "A 0.0049 mm^2 2.3GHz sub-sampling ring-oscillator PLL with time-based loop filter achieving −236.2dB jitter-FOM," IEEE International Solid-State Circuits Conference - Digest of Technical Papers (ISSCC), San Francisco, CA, 2017, pp. 328-329, doi: 10.1109/ISSCC.2017.7870394.

[130] Abidi, A.A., "Phase Noise and Jitter in CMOS Ring Oscillators," in IEEE Journal of Solid-State Circuits, vol.41, no.8, pp.1803-1816, Aug. 2006 doi: 10.1109/JSSC.2006.876206

[131] R. Nandwana, T. Anand, S. Saxena, S. Kim, M. Talegaonkar, A. Elkholy, W. Choi, A.

Elshazly, P. Hanumolu "A 4.25GHz-4.75GHz Calibration-free Fractional-N Ring PLL Using Hybrid Phase/Current-mode Phase Interpolator With 13.2dB Phase noise Improvement" IEEE Symposium on VLSI Circuits, Digest of Technical Papers, Honolulu, HI, 2014, pp. 1-2.

[132] S. Karvonen, T. Riley and J. Kostamovaara, "A low noise quadrature subsampling mixer," IEEE International Symposium on Circuits and Systems (ISCAS), 2001, pp. 790-793 vol. 4, doi: 10.1109/ISCAS.2001.922356.

[133] E. Cijvat, P. Eriksson, Nianxiong Tan and H. Tenhunen, "A 1.8 GHz subsampling CMOS downconversion circuit for integrated radio circuits," IEEE International Symposium on Circuits and Systems (ISCAS), 1998, pp. 65-68 vol.2, doi: 10.1109/ISCAS.1998.706842.

[134] T. Vasseaux, B. Huyart, P. Loumeau and J. F. Naviner, "A track&hold-mixer for direct-conversion by subsampling," IEEE International Symposium on Circuits and Systems (ISCAS), 1999, pp. 584-587 vol.4, doi: 10.1109/ISCAS.1999.780072.

[135] T. Vasseaux, B. Huyart and P. Loumecu, "A track&hold-AGC suitable for downconversion by subsampling," 6th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 1999, pp. 1527-1530 vol.3, doi: 10.1109/ICECS.1999.814461.

APPENDIX A: Simulation procedure for Impulse Sensitivity Functions

The original simulation procedure of ISF can be described as below [61]:

a) In the first sampling clock cycle, reset the latch to be zero.
b) In the second sampling clock cycle, apply a short probe voltage pulse to mimic the impulse stimuli to the latch. Assume the pulse is τ (denoted as the time offset with respect to the latch clock) away from the rising edge of the sampling clock.
c) For a certain τ, adjust the pulse amplitude until the latch output crosses the mid-rail voltage before the required time in the third cycle, which therefore means the latch detects the pulse signal correctly.
d) For different time offset τ, repeat the abovementioned steps and the corresponding amplitude of each pulse can therefore be obtained.

However, this method needs carefully tuning of the pulse amplitude, which either consumes a lot of simulation time or requires smart searching algorithms. Furthermore, it's challenging to simulate the effects of tiny impulses on large-signal waveforms due to numerical inaccuracies. To solve this problem, different methods have been proposed. For instance, researchers in [62] utilized the efficient periodic AC simulation and the periodic time-varying analysis to obtain the ISF. A more practical methodology was proposed in [60] and is discussed below.

First apply a small step signal to the comparator at time τ with a small offset voltage $V_{ms}(\tau)$. Compared to previous methodologies, the main difference is that the metastable point is found statistically by counting the occurrences of the output bit being 0 or 1 over multiple measurements. In other words, $V_{ms}(\tau)$ is defined as the step offset V_{os} that yields the equal probabilities of ones and zeros. With the help of a simple servo loop to keep the comparator metastable, the offset voltage can then be generated. Sweep various time τ and measure the corresponding $V_{metastable}$, the step sensitivity function SSF(τ) will then be obtained. ISF can finally be obtained by calculating the derivative of the SSF.