Gaussian pulse generator circuit for UWB systems by discrete switches and integrated circuit

by

Mahdi Alesheikh

A thesis submitted in partial fulfillment of the requirements for the degree of

Master of Science

in

Electromagnetics and Microwaves

Department of Electrical and computer engineering
University of Alberta

Abstract

A Gaussian pulse generator circuit is a component of an ultra-wideband transceiver (transmitter and receiver) circuit that generates a narrow pulse for imaging, detecting, and various other applications. In UWB transceivers Gaussian pulse is always converted to a Monopulse to be DC-free and more compatible for transmission via an antenna. This Monopulse is created using Avalanche transistors as discrete switches and a differential CMOS transistor in 65 nm technology as an integrated circuit. Discrete switches generate high amplitude voltage with a moderate pulse width, improving the detection range in UWB transceivers. However, using a 65 nm integrated circuit (IC) instead of a discrete circuit can capture a sharper pulse with less pulse width, increasing the range resolution. The first design is consists of three-stage Avalanche transistors, to increase the amplitude of Gaussian pulse by a factor of three. The final Monopulse is created by a balun that subtracted two Gaussian pulses, which have different phases. In this design, the final Monopulse is connected to the antenna and sent by the transmitter circuit. After receiving the transmitted signal and analyzing the data by the computer, the buried object in 45 cm depth is detected and separated from the sand. The second design consists of a differential pair circuit that generates a sharp pulse due to the voltage difference between its two inputs. The desired Monopulse is formed by sharpening this pulse using an inverter chain and mixing three pulses with different phases. These Gaussian pulse generator systems can be utilized in different applications, such as detecting buried objects, underwater imaging,

through-wall imaging, diagnosing cancer glands without using harmful methods like an X-ray beam, etc.

Preface

This thesis is an original work by Mahdi Alesheikh. The first part of this manuscript, Chapter 5-1, has been submitted to the IEEE sensor journal. I was responsible for the fabrication and analysis of the circuit as well as the manuscript composition. Dr. Feghhi, who collaborated in the design of the circuit and contributed to manuscript corrections, aided finish Chapter 3 to 5-1-3. Ms. Modarres and Mr.Karimov assisted in imaging and collecting data. Mr. Karimov assists in designing a monopulse shaping network in Chapter 5-1-4, and Ms. Modarres is primarily responsible for Chapter 5-1-5. Prof. Karumudi and Prof. Hossain were the supervisory author and were involved with concept development and manuscript composition. Chapter 5-2 is related to the second project. I was responsible for designing the circuit and optimizing that with the help of Dr.Feghhi. Dr. Feghhi proposed the circuit idea, and we worked together to complete chapters 5-2-2-1 through 5-2-2-6. In addition, I was responsible of developing the initial version of the circuit's Layout as well as simulating the first Layout and worst-case scenarios. As a result, I completed chapters 5-2-3 and 5-2-4 on my own.

This Thesis is Proudly Dedicated To:

my mother, Mansoureh,

And my sweet sister, Melika.

Acknowledgment

First and foremost, I would like to thank my supervisors, Dr. Rambabu Karumudi and Dr.Masum Hossain, who has supervised me throughout my MSc program. Their help and consideration made the completion of this thesis possible. Furthermore, I appreciate Dr. Feghi's guidance, who helped me with his circuit designing skills. Also, I am grateful to my Lab group, Fateme, Adil, Kapil, and Shakib, for making a friendly group to pursue our purposes. I am incredibly thankful to my mother, who helped me a lot; she is an associate professor and encourages me in achieving my goals of continuing my study at the MSc level. She is the best source of love; without her help, today, I am not here to defend my thesis.

Mahdi Alesheikh

September 2021

Contents

List of tables

List of figures

1- Introduction

Sending and receiving data wirelessly and remotely is one of the most commonly used communication technologies these days. To send and receive data, the transmitter and receiver structure are required. There are different types of transceivers, such as cellphone transceivers, radar transceivers, radio transceivers, etc. One kind of transceiver is an ultra-wideband radar transceiver. Ultra-wideband is a radio technology capable of using very low energy over a significant fraction of the radio spectrum for short-range, high-bandwidth communications [1]. The extremely wide frequency bandwidth brings a high amount of signal energy to be transmitted without interfering with the carrier waves in the same frequency range [2]. Thanks to their low energy consumption and high bandwidth, ultrawideband radars have attracted much attention for different applications, such as designing portable devices to measure distances between cars and detect and position Objects approaching the vehicle [3]. Moreover, ultra-wideband systems' manufacturing cost tends to be low compared to other radar systems [4].

Most transmitters use a low noise amplifier (LNA) at the receiver's input to amplify the received signal attenuated by the medium and a power amplifier (PA) at the transmitter's front end to amplify the transmitted signal. A mixer is also used to up-convert the signal's frequency, reducing the effect of noise on

the transmitted signal. However, on the receiver side, the signal's frequency is decreased for ease of analysis. With the oscillator's help, the mixer multiplies a pure sinusoidal signal produced by the oscillator in the signal and decreases or increases signal frequency. Finally, the receiver and transmitter use the antenna to send or receive data. All transmitters operate in a similar manner, although their configurations and types varies based on the type of application and function of the circuit. In the short-range radar transmitters, there is a simpler structure in the transmitter section. In this structure, a pulse generator produces a narrow pulse for radar application. Then it is only amplified with the help of an ultra-wideband power amplifier and transmitted via an antenna [5]. The receiver has an antenna to get the returned signal which is attenuated by the medium. Finally, the necessary signals are taken to the digital part, and the results are extracted from them with the help of computer analysis.

There are many radio broadcasting methods like frequency modulation (FM) [6], frequency-shift keying (FSK) [7], using squire pulses, and using Gaussian pulses. The Gaussian pulses are sharp signals that can be used for ultra-wideband short-range radar imaging, where range resolution is required for detection [8]. Gaussian pulses are usually produced by using discrete elements like Avalanche transistors [9] and step recovery diode (SRD) [10] or using CMOS technology in an integrated circuit (IC) [11], or through the digital configurations [12]. Integrated circuits are significantly faster than discrete

circuits [13]. This faster feature gives the ability that can get a sharper signal with lower pulse width. In ultra wideband radar imaging systems, the Gaussian pulse characteristics such as amplitude, ringing, and pulse width significantly influence imaging performance. The radar system's range resolution is determined by Gaussian pulse width [14], therefore using an IC instead of discrete circuits enhances the range resolution. The Gaussian pulse amplitude and power determined the detection range. Because IC's power is remarkably lower than discrete circuits, it can only be used for short-range detection, such as detecting cancer glands with a biomedical instrument attached to the body. The focus of this thesis is on the pulse generator, which is a component of these transceivers. Two distinct methods for generating the Gaussian pulse signal are presented. In the first design, a Gaussian pulse generator was created with discrete elements. This structure is a Marx Avalanche transistor circuit, which increases the amplitude of the Gaussian pulse by using three Avalanche transistors stages [15]. Also, an output stage is designed for this structure which improves the quality of these transmitters' output pulses. This circuit is used to locate a buried object at a depth of 45cm and for underwater imaging. The images demonstrate this design's high performance. In the second design, a Gaussian pulse generator in 65nm technology has been proposed. This circuit is used only for short-range but high-accuracy applications due to its low power. The technique used to generate this pulse is an enhanced method that improved the

output pulse characterisitcs. In addition, an external output voltage can adjust the pulse width of the circuit. It means that the range resolution of this circuit can be changed and that it can be used with varying degrees of accuracy for various applications.

2- Ultra-wideband transceivers

The basis of each communication device is its transceivers blocks that are used for sending and receiving data. There are different types of transceivers based on the type and methods of sending and receiving data. One type of transceiver is an ultra-wideband radar transceiver. Currently, ultra-wideband (UWB) radars are widely used in real-time short-range location systems, such as biomedical instruments, wireless network sensors, industrial machines [11],[16]-[19].

Ultrawideband radar systems use a specific signal to send and receive by the transceiver to find an object. It can use a square pulse, sine wave, Gaussian pulse, etc. Gaussian pulse is one of the most common pulses that are used in these transceivers [20]. However, in ultrawideband radar systems, The Gaussian pulse constantly changed to the Monopulse to be DC-free [21]. The Monopulse shaping network is used instead of a Gaussian pulse generator to omit the antenna's input DC voltage. There are various methods for converting a Gaussian pulse to a Monopulse, including subtracting two Gaussian pulses or deriving the Gaussian pulse [21], [22]. Following the creation of a Monopulse, the derivative of that is formed in the antenna for transmission to the target.

3- Gaussian pulse

Gaussian pulse is used in high spatial resolution radar systems and ranging capability for wireless sensor network terminals. A Gaussian pulse has a relatively low duty cycle. This low duty cycle results in low power dissipation, which extends the battery life of radio systems. These unique features make it superior to other pulses, and nowadays, Gaussian pulse is commonly used in ultrawideband radar systems[23]. Gaussian pulse characteristics are well-suited to different imaging applications, such as through-wall imaging, ground penetration radar imaging, buried objects imaging, etc. [24],[25].

Typically, Gaussian pulses are generated using discrete elements like Avalanche transistors or step recovery diode or combined circuits like CMOS transistors in integrated circuits (IC), making a sharper Gaussian pulse compared to the discrete switches.

3-1 Gaussian pulse characteristics

Gaussian pulse has important characteristics like amplitude, rise and fall time, ringing, and pulse width, significantly influencing imaging performance [22]. Ringing is one of the most important attributes of the Gaussian pulse. Ringing determines the signal-to-noise ratio (SNR) of systems; a better SNR makes a shorter imaging processing time [26], [27]. Also, the ringing has essential

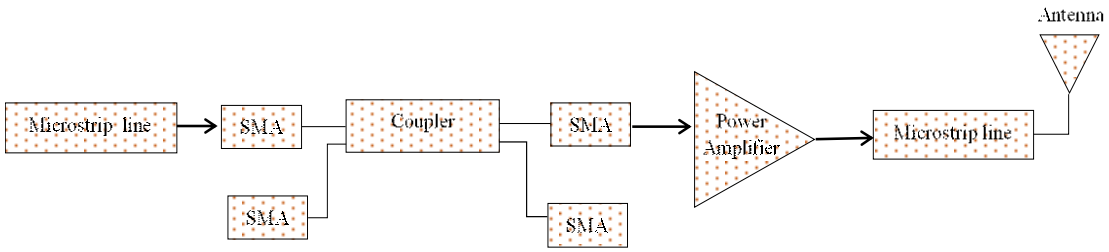


Fig.1 Gaussian pulse transmitter

effects on total harmonic distortion (THD). In a sense, which distorts the rising and falling edges of the Gaussian pulse [28].

3-2 Effect of ringing and discontinuity

As shown in Fig. 1, a typical transmitter architecture was chosen to investigate the effect of ringing. All the transmitter elements such as microstrip transmission lines, coupler, Sub Miniature Version A (SMA), antenna, and the air gap formed at interconnection zones are designed to find their influence on the characteristics of the Gaussian pulse. There are many interconnections in the Gaussian pulse transmitter like Sub Miniature Version A, junctions, microstrip transmission lines, etc. These interconnections may have some impact on the Gaussian pulse.

Two conditions were investigated and compared to the mathematical state to find the effect of discontinuity and ringing. One time the effect of SMA and transmission lines interconnections was ignored to have an ideal configuration, and in another time, it was considered a real configuration. The correlation

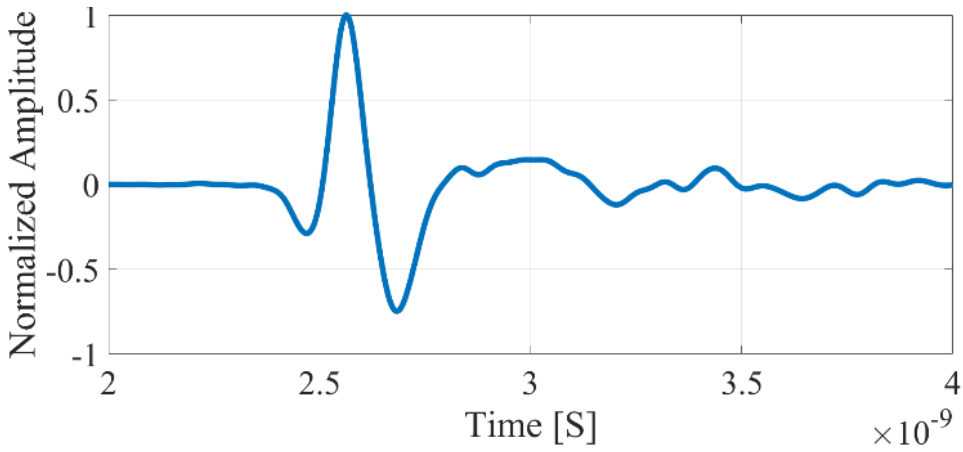


Fig. 2. The output of the real configuration

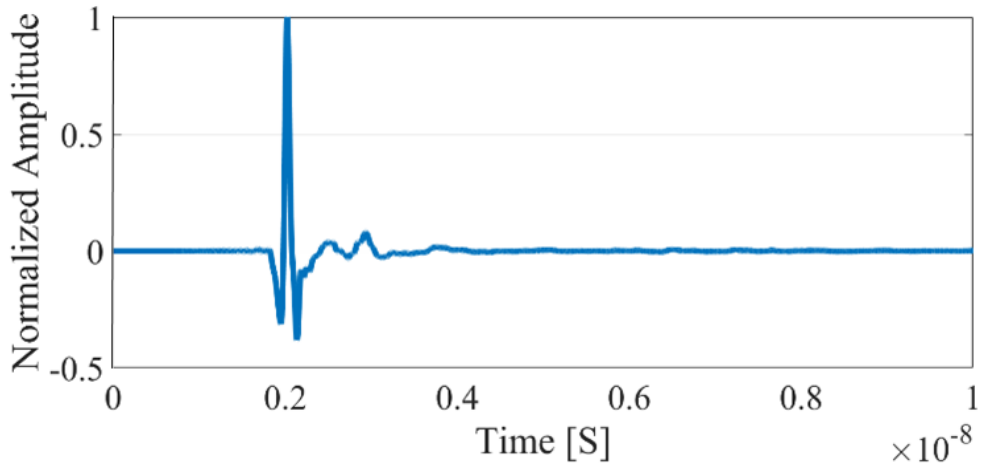


Fig. 3. The output of the ideal design

between these two configurations was 86%. It shows that 14% of the signal loss, through distortions factors. Also, The ringing of the real circuit is 20 percent of the total amplitude and 12.2 percent more than the ideal circuit.

The correlation between the mathematical configuration with these two configurations is 46 and 58 percent, respectively. The output of this situation is shown in Fig. 2, 3, and 4. Because the mathematical circuit is distortion and

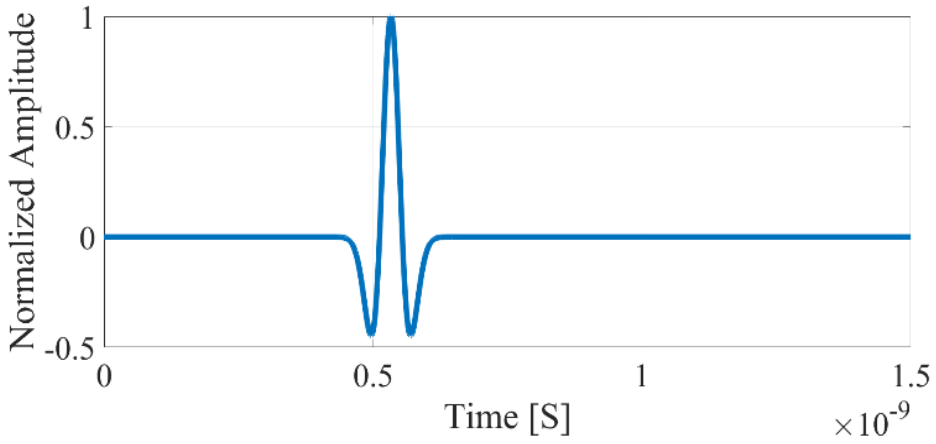


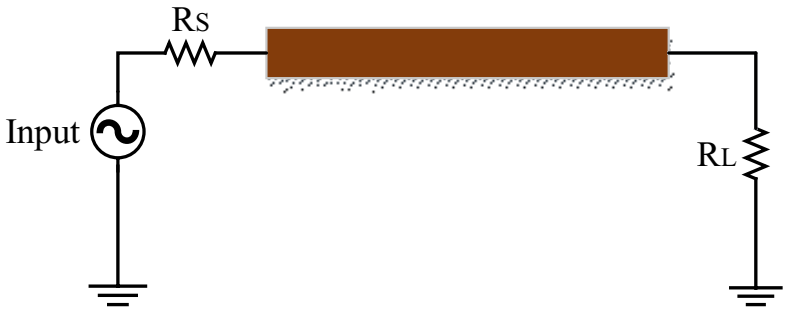
Fig. 4. The output of the mathematical configuration

ringing-free, the result of mathematical configuration is not achievable in a practical circuit; hence we get a very low correlation compared to the other two states.

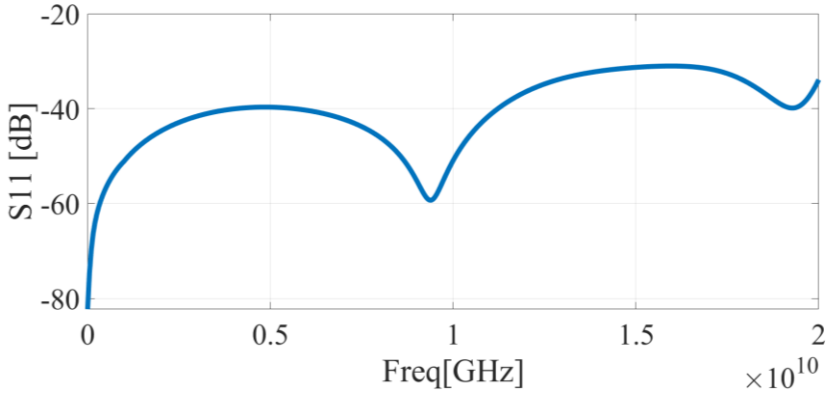
3-3 Gaussian pulse transmitter

In the transmitter selected to find the ringing and discontinuity effects, microstrip transmission lines with 50 Ω characteristic impedance connect the components. The 50 Ω microstrip transmission lines cause a phase difference to the signals without decreasing the amplitude. The phase difference created by the microstrip line is different for each frequency. Also, the 90-degree coupler differentiates the Gaussian pulse to make a Monopulse [29]. And there is a power amplifier (PA) before the Vivaldi antenna to amplify the Monopulse and increase the signal-to-noise ratio. All of the components are designed and

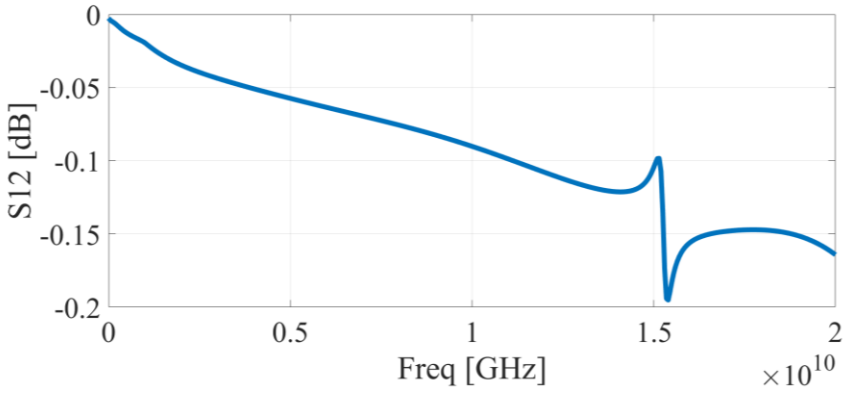
simulated in HFSS software to determine the interconnection effect, and the S parameters of each are shown in Fig. 5, 6, and 7.



(a)

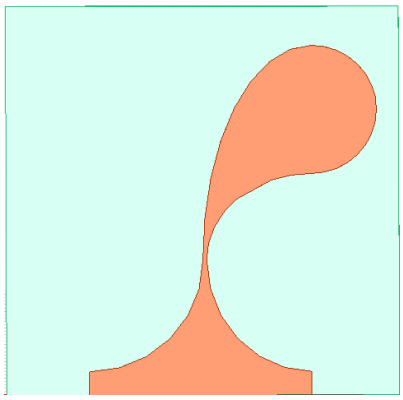


(b)

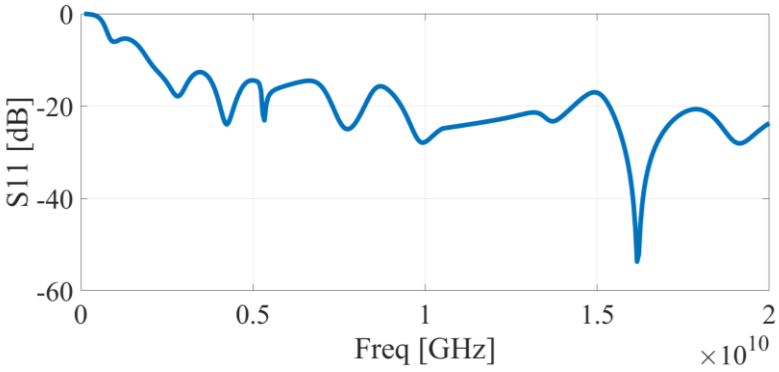


(c)

Fig. 5. a) Designing the microstrip b) S11 parameters c) S12parameters



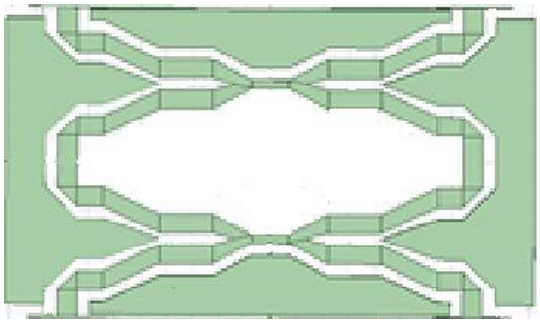
(a)



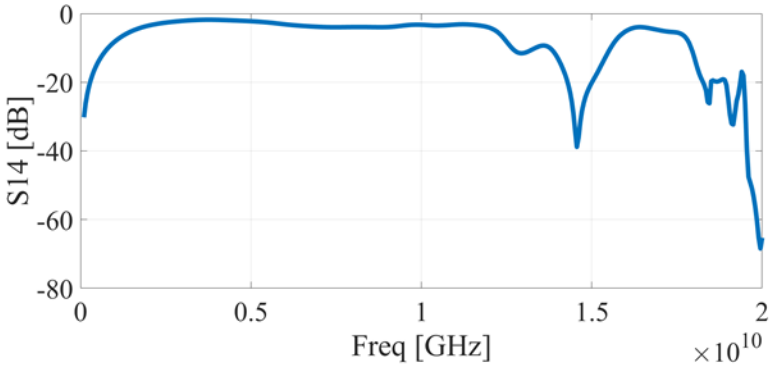
(b)

Fig. 6. a) Designing the Vivaldi antenna b) S11 parameters

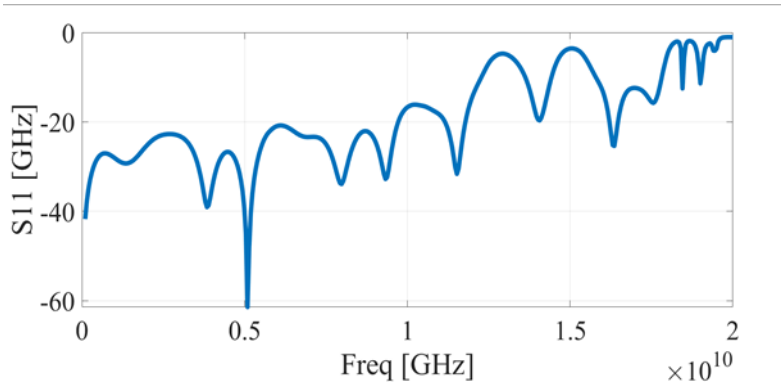
The microstrip line S_{11} parameter is periodic, which is repeated each 10 GHz. The S_{11} bandwidth is related to the length of the microstrip. *S* parameters of the coupler shown that it has a -10 dB bandwidth from 1 to 12.5GHz. Based on the Vivaldi antenna's s parameter, the signal frequency component that the antenna can radiate is from 1.5 to 15 GHz. The S parameters of SMA are significant since this is a region where there may be a gap between its connections, resulting in a discontinuity.



(a)



(b)

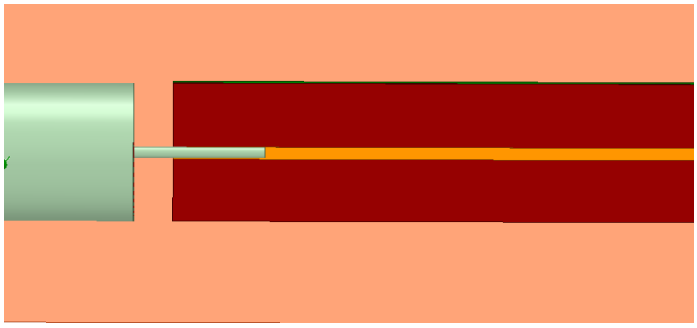


(c)

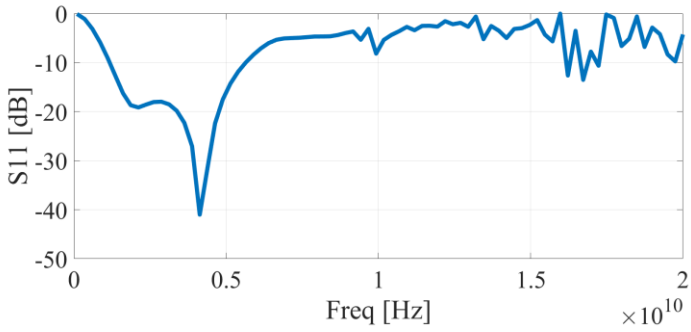
Fi.g 7. a) Designing the 90-degree b) S12 paramters c) S11 paramters

3-4 De-embedding procedure

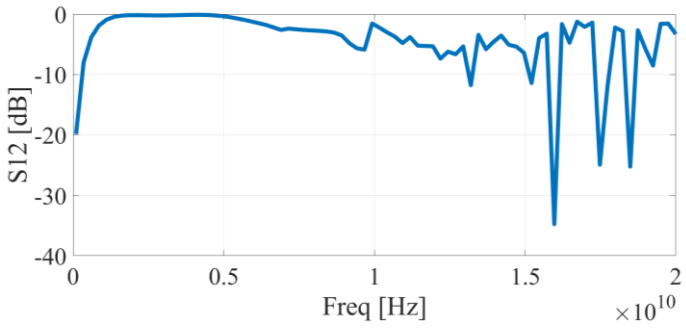
The gap between SMA and transmission lines is an essential component that influences output. To find The SMA effects, a model of that is designed in Fig.8.



(a)



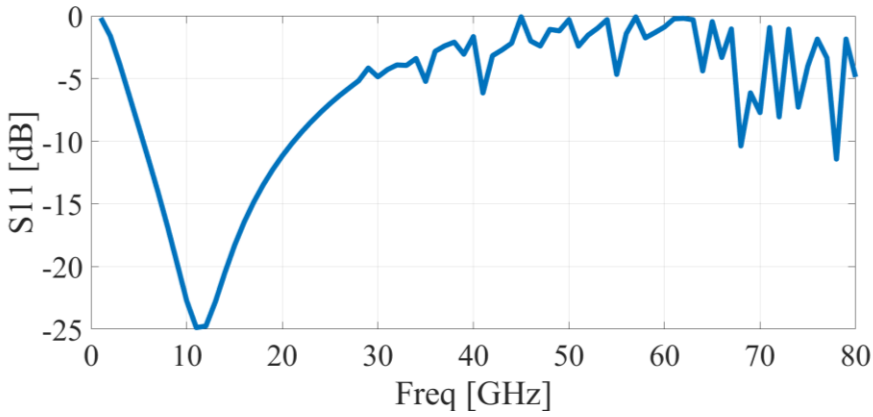
(b)



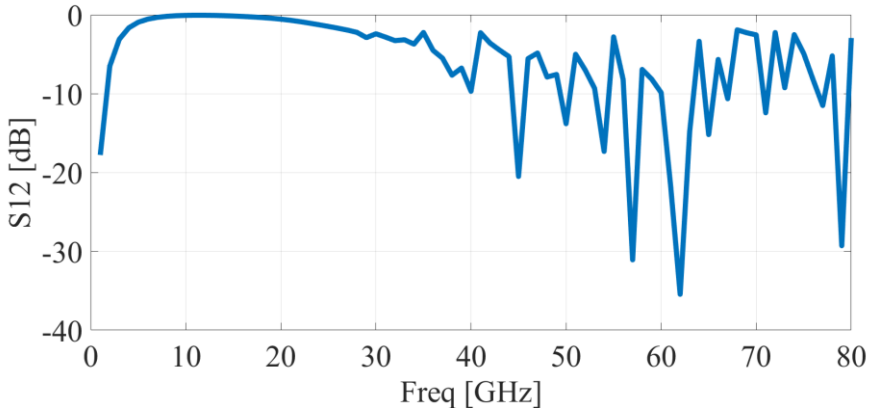
(c)

Fig. 8. a) Designing the connection structure b) S_{11} parameters c) S_{12} parameters

It is shown in Fig. 8 that the SMA is connected to the microstrip line with considering an air gap between the connection. The S parameters of this setup are depicted in Figures 8 (b) and (c) (c). To calculate the S parameters of the air gap, we used the T parameters of the overall circuit and detaching elements in Matlab to find the S parameters of the gap. The S parameters of the gap can be shown in Fig. 9.



(a)



(b)

Fig. 9. S parameters of the gap a) S_{11} b) S_{12}

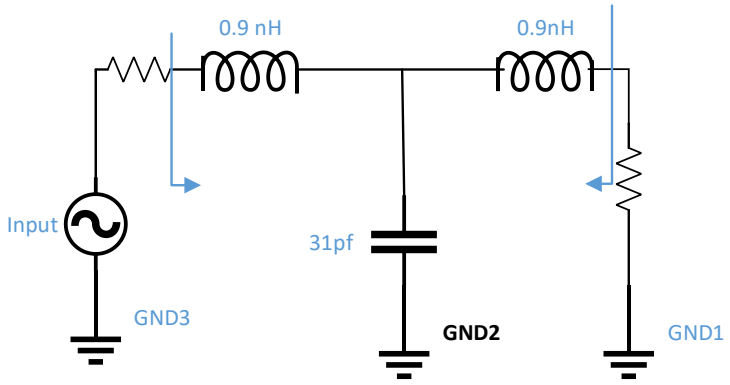


Fig. 10. Model for the gap

With the help of the Advanced designing system (ADS) software, using the gap's S-parameters, the gap can be modeled by three passive elements. The model that is given for the gap is shown in Fig. 10.

3-5 Relation between input pulse width and ringing

The output result of the fabricated circuit is investigated as a function of the pulse width. In doing so, the pulse width from 50 to 300 ps is studied. The results are categorized into five different regions based on the correlation between real configuration and ideal configuration. The first region start from 50 to 100 ps, shows a correlation of around 86 %.

The second region started from 100 to 150 ps, represent a closed behavior between the two experiences. As a result of this experience, the correlation is between 88% to 89%. For the rest of the experience, incremental behavior is

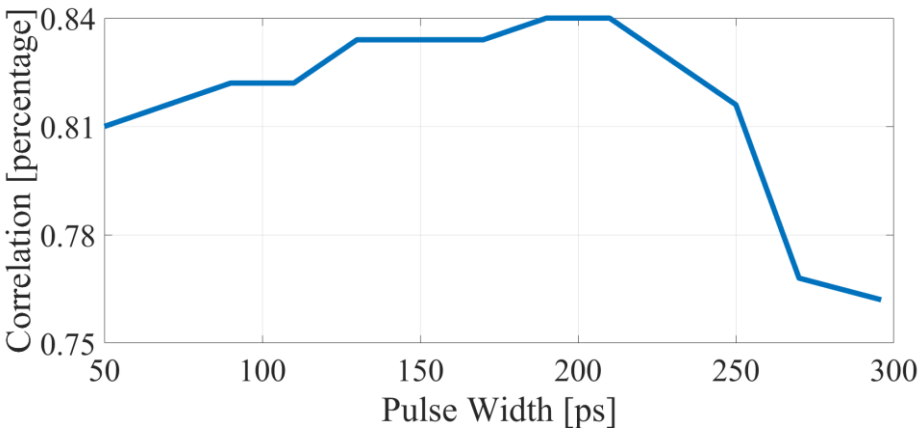


Fig. 11. correlation of ideal and real configurations as a function of pulse width

achieved. However, after the 250 ps, the correlation decreased to 78% because it couldn't pass low-frequency bands. The diagram of a correlation between real configuration and ideal configuration as a function of pulse width is shown in Fig. 11.

3-6 Coupler Bandwidth effect

There is a 42 ps Gaussian pulse at the coupler input, as is shown in Fig 12. This Gaussian pulse passes through the 90-degree coupler to convert to Monopulse [30]. The coupler bandwidth is a significant factor in the output signal shape. Four 90 degrees couplers with different bandwidths have been investigated. The frequency behavior of couplers with 5, 10, 15, and 40 GHz bandwidth with the input frequency behavior is shown in Fig. 13. It shows that the coupler with higher bandwidth can pass more frequency spectrums.

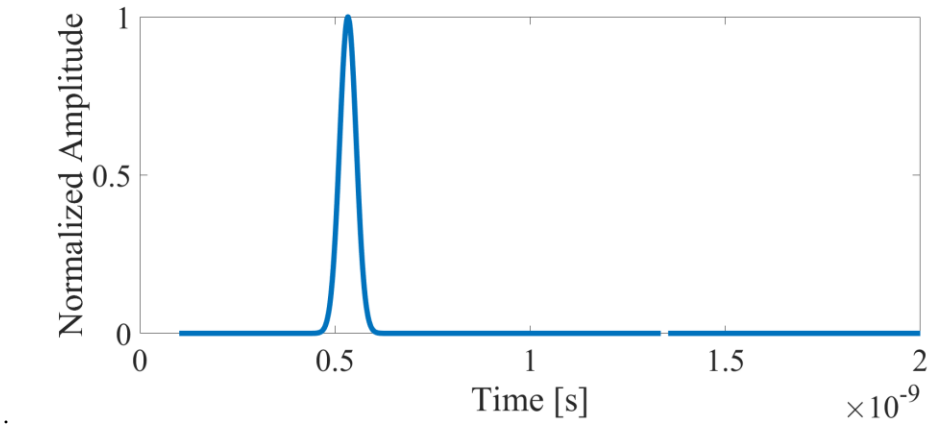


Fig. 12. Input signal

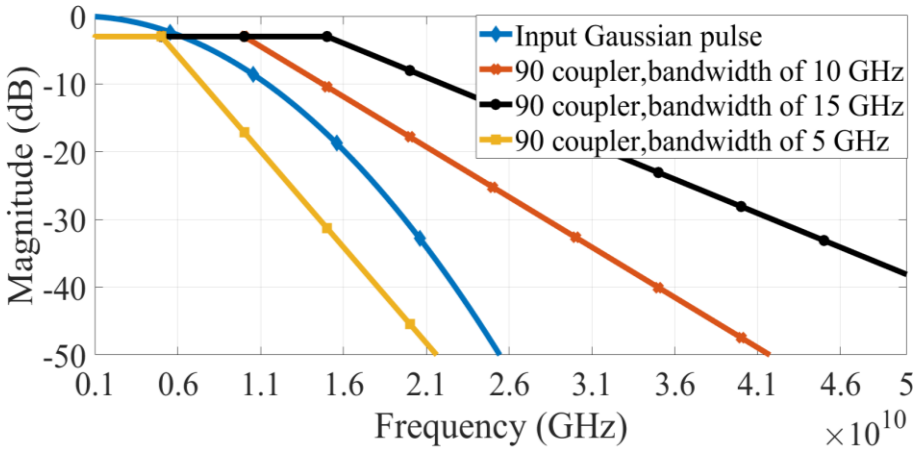


Fig. 13. Coupler bandwidth

The output Monopulses of these couplers and their frequency spectrum are shown in Fig. 14 and Fig. 15, showing different pulse characteristics.

The comparison of the various Monopulses is shown in table 1. It shows that increasing the coupler bandwidth decreased both positive and negative pulse width. Also, by obtaining the correlation between each Monopulse and the ideal

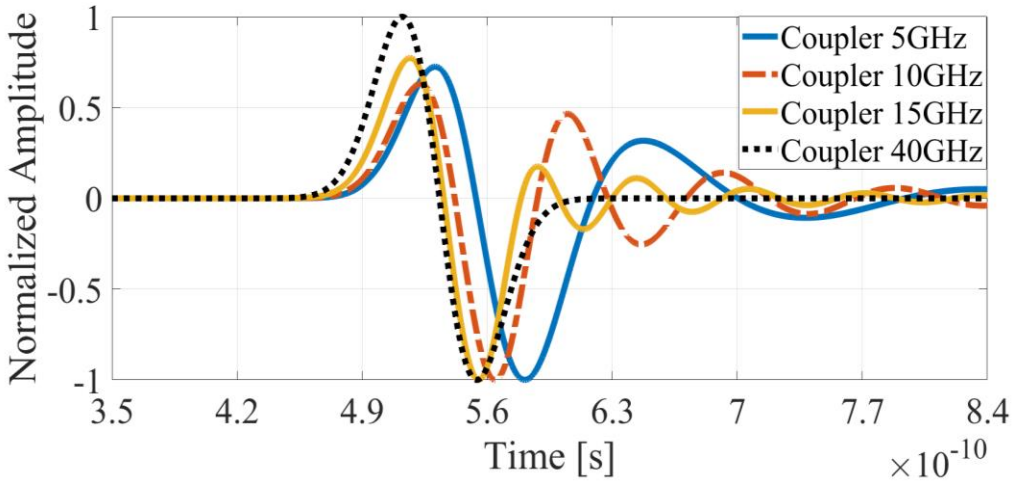


Fig. 14. Output Monopulse

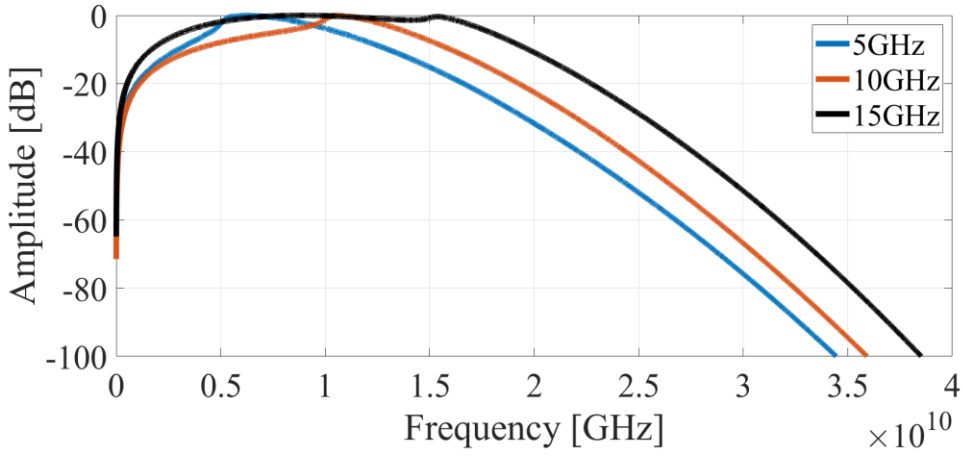


Fig. 15. frequency spectrum for each output monopulse

Monopulse received by the 40 GHz bandwidth coupler, it is discovered that the results of 15 and 10 GHz coupler bandwidth are very close to the ideal Monopulse. However, the 5GHz coupler output is far from the ideal output because of the unnecessary increase in pulse width. The ringing amplitude is

determined by the percentage of the signal's overall magnitude. It has been shown that only the 15 GHz coupler output has a low ringing.

Table 1. Monopulse characteristics of each coupler

	5GHz	10GHz	15GHz
correlation	0.57%	0.88%	0.98%
ringing	24%	28%	5%
Positive Pulse width	36ps	32ps	32ps
Negative Pulse width	40ps	28ps	27ps

4- Literature review

Discrete elements or integrated circuits can generate Gaussian pulses, which are used in UWB systems. Different discrete switching devices like SRD diodes and Avalanche transistors can produce a Gaussian pulse [10]. SRD diodes are fast switching devices used for fabricating a Gaussian pulse system. These diodes are suitable for generating narrow pulses with a few nanosecond pulse widths. Fig. 16 depicts a typical SRD structure for generating a Gaussian pulse [10]. When the input alternating current source is negative, two SRD diodes operate as low impedance devices, and the output is connected to the ground. Once the voltage rises and is positive, the SRD_1 switches to the off-state, causing the output to follow the positive input sharply. Then, SRD_2 switches to the off-state with a slight delay caused by the load resistor in the SRD_2 path. Because of this switching, the output is sharply connected to the ground, and a Gaussian pulse appears at the output. Despite the fact that this structure generates a low ringing Gaussian pulse, its amplitude is lower than other discrete switching devices.

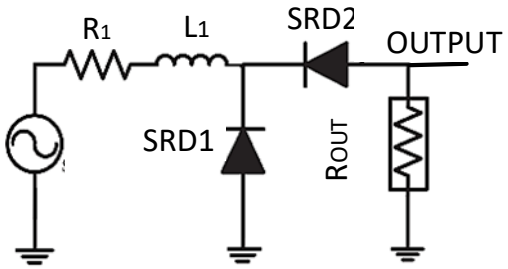


Fig. 16. Gaussian pulse generator by using SRD diodes [10]

Avalanche transistors can also be used to create a Gaussian pulse. Switching transistors from on to off is a possible way of producing a semi-Gaussian pulse with a moderate amplitude. A transistor operating point is adjusted to place a transistor in three typical regions, including saturation, linear, and cut-off regions. A conventional transistor with a high *dc* biasing voltage can be damaged because of the Avalanche phenomenon. However, Avalanche transistors are developed to work in the Avalanche region. These transistors need high biasing voltages but low current to switch to the Avalanche region. This high biasing voltage and low current can be produced by converting a low amplitude voltage signal to high amplitude and low current voltage using a booster circuit [31]. A single Avalanche transistor generates a Gaussian pulse shown in Fig. 17 [9]. The Avalanche transistor is initially turned off in this design, and the output is connected to the ground. When the triggering signal

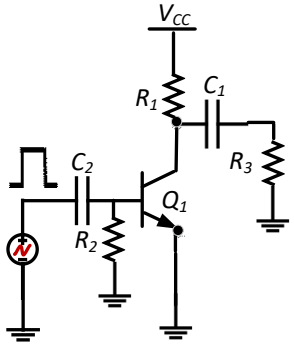


Fig. 17. Gaussian pulse generator by Avalanche transistor [9]

arrives, the transistor switches on, causing the capacitor, which was charged by V_{CC} connected to the ground, to discharge. The Avalanche transistor's quick

switching causes the output to fall sharply to the minus value. Then the output capacitor is discharged by the time constant of $\tau = R_{OUT} \times C$, and as a result, the output returns to zero, resulting in a Gaussian pulse at the output. This circuit used only one Avalanche transistor stage to generate a Gaussian pulse. In our design, to achieve better pulse width and amplitude, a Marx structure composed of three Avalanche transistor stages is used to increases the amplitude by three times.

Despite the discrete switches, integrated circuits can generate a Gaussian pulse with a narrower pulse width due to the high speed of Mosfet transistors. A straightforward way to generate a Gaussian pulse is using an oscillator. The oscillator oscillates constantly and produces a sinusoidal signal at its output. It is possible to obtain the desired Gaussian pulse by using a filter after the oscillator. In one study [32] shown in Fig. 18, by using a glitch pulse generator, an oscillator, and a pulse-shaping filter, the Monopulse was created. The activation time of the ring oscillator is controlled by an on/off switch; when the switch is turned off, transistors enter a sub-threshold region, and the entire circuit turns off. Following the oscillator, a buffer is used to separate the first and second stages to eliminate the effects of first and second stages on each other. .

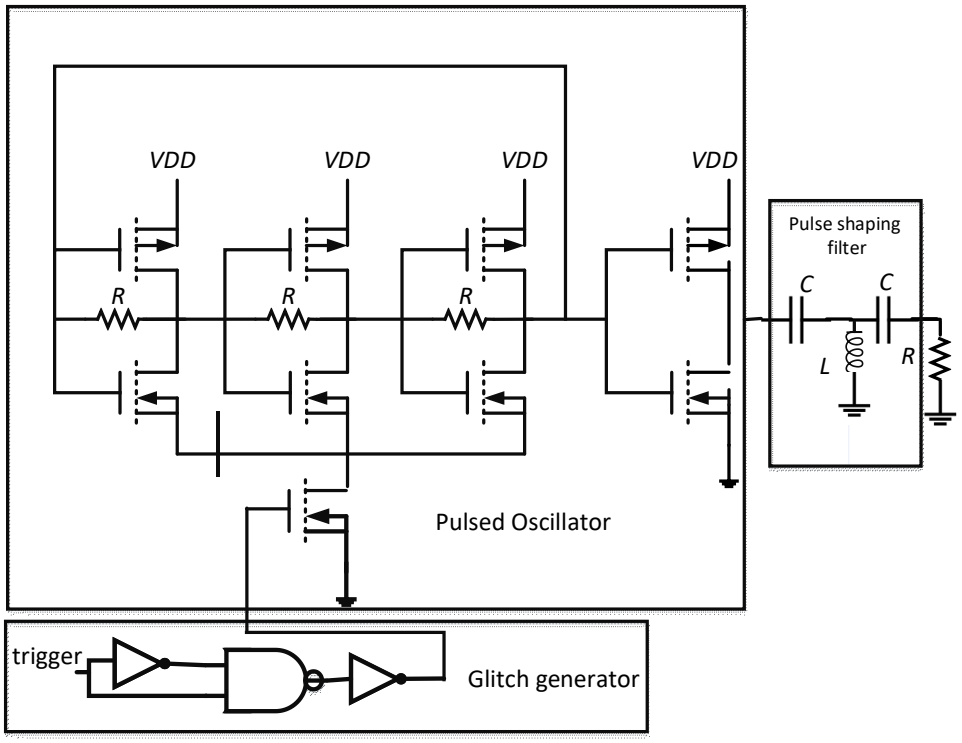


Fig. 18. Gaussian pulse generator by using an oscillator [32]

By using feedback in a ring oscillator, a frequency ban receives a 360-degree phase shift and is added to the input to amplify again, causing the oscillator to oscillate constantly. One limitation of these structures is that they require a filter to remove some frequency components in order to shape the desired Monopulse signal. Ringing is another issue that arises when using oscillators. The oscillators do not turn off quickly and continue to oscillate after the switch is turned off. This time is significant for oscillator designers because this ringing distorts the Gaussian pulse shape and reduces the imaging performance. As a result, more simulations are required to eliminate the effect of ringing on

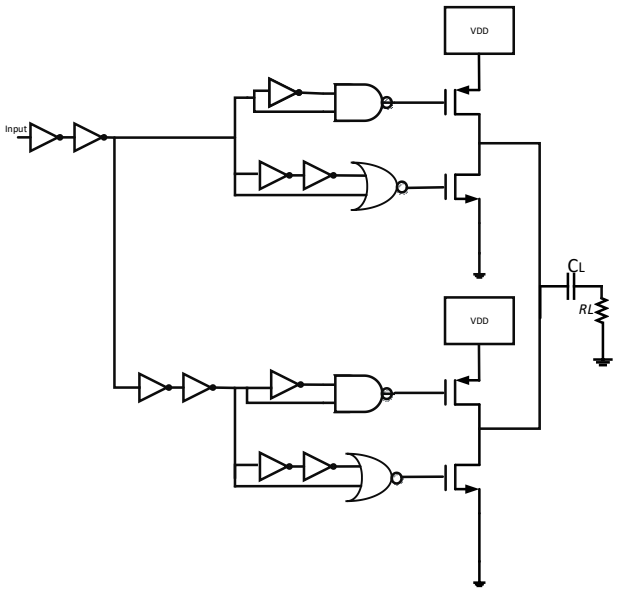


Fig. 19. the digital triangular pulse generator [33]

imaging. Despite having a proper pulse width and amplitude, this design has a significant ringing problem.

A digital circuit can also be used to generate a Gaussian pulse [33]. The advantage of using a digital circuit is that it consumes low power. In this system, depicted in Fig. 19, an inverter branch sharpens the input pulse generator signal. Then there are two identical pathways to create a Monopulse. The pulse generator's *C* and *D* outputs are the same as its *A* and *B* outputs. *C* and *D* outputs only have two more inverters to delay the output and create the Monopulse's second period. Output *A* is formed by AND operation of the input and inverted of that. The AND operation of the input and inverted of that is always zero; nevertheless, due to inverter delay, a sudden condition is generated in which

both AND inputs are high voltage, leading the output to reach peak value in a short period of time. Because the AND output is high voltage for a brief period of time, it produces an extremely sharp signal with a fast rising time. Output *B* is the inverse of output *A*. It means that its inputs are always high voltage, and in a short time, they change to zero, causing the output to change to zero as well. Both *A* and *B* have a NOT gate at the end of their paths, which is used to inverse their outputs. When the voltage at output *B* is high, the transistor M_2 turns on and abruptly connects the final output to the ground. In addition, if output *A* is negative, the transistor M_1 activated, and the final output is connected to V_{DD}. The same thing happened with outputs *C* and *D*, as well as transistors M_3 and M_4. The *C* and *D* are added to the final output by a delay to make a derivative of the Monopulse. The pulse width is proportional to the inverter delay, which can be adjusted by changing the size of the inverters. In addition, this design used a capacitor before connecting to an antenna to match 50 ohms.

Because just one transistor of the final stage is in the *ON* state at any given time, this method consumes less power. This is a basic construction that consumes low power and produces a Monopulse with narrow pulse width. Still, in our transmitter, because an antenna derives the input signal, only one Monopulse is needed at the antenna's input, not a derivative of that. It means that the *C* and *D* paths are ineffective for our imaging system.

Another study in Fig. 20 makes the fifth Derivative Gaussian pulse generator for the UWB breast cancer detection system [17]. This design consists of a squire waveform former circuit, delay circuits, Phase Detector Circuits (PDC), and Pulse Shaping Circuit (PSC).

The squire waveform circuit is responsible for matching the circuit's input to 50 ohms, and it has a capacitive filter for rejecting low-frequency bands. Like other designs, there is an inverter chain to achieve rise or fall time as low as possible. Then there is a delay circuit to generate a signal with different phases to use in the phase detector. If the phase detector circuit detects a phase difference between its two inputs, it will generate a sharp signal at the output. The phase detector output is related to the input circuit's previous and new states. The entire conditions of its inputs are shown in table 2. When the phase detector receives

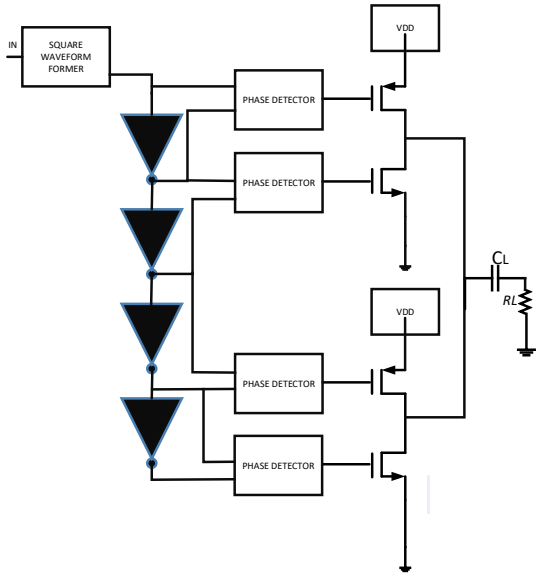


Fig. 20. Gaussian pulse generator [17]

two different inputs, as shown in Fig. 21, the output abruptly changes its state and displays a phase difference. The output voltage level will be low if both input signals are low . However, when the ln1 input leads to the ln2 input, the output voltage goes up to a high voltage. Finally, the output voltage level is zero when both input signals are high voltage.

This design's pulse width and power are not better than the previous design; it merely demonstrates a new way to generate the Gaussian pulse by a phase detector.

In another method [34], an all-digital reconfigurable IR-UWB pulse generator using BPSK modulation in the 130nm RF-CMOS process is explained. This circuit in Fig. 22 consists of four main blocks: a DE multiplex circuit block,

Table 2. phase detector's states

In1, In2	V1	V2	Vout
0,0	1	X	X
1,0	1	0	1
1,1	0	1	0
0,1	1	1	0
0,0	1	1	0

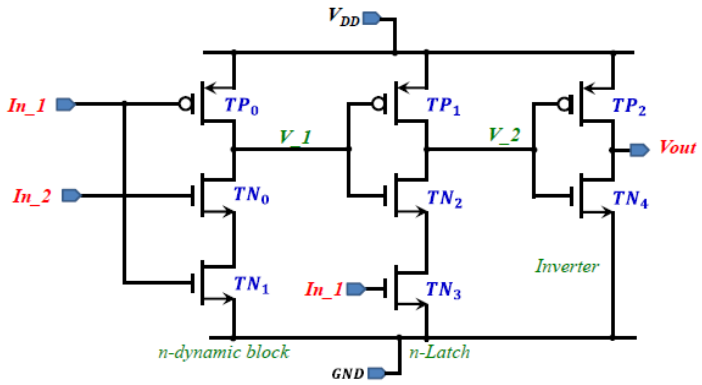
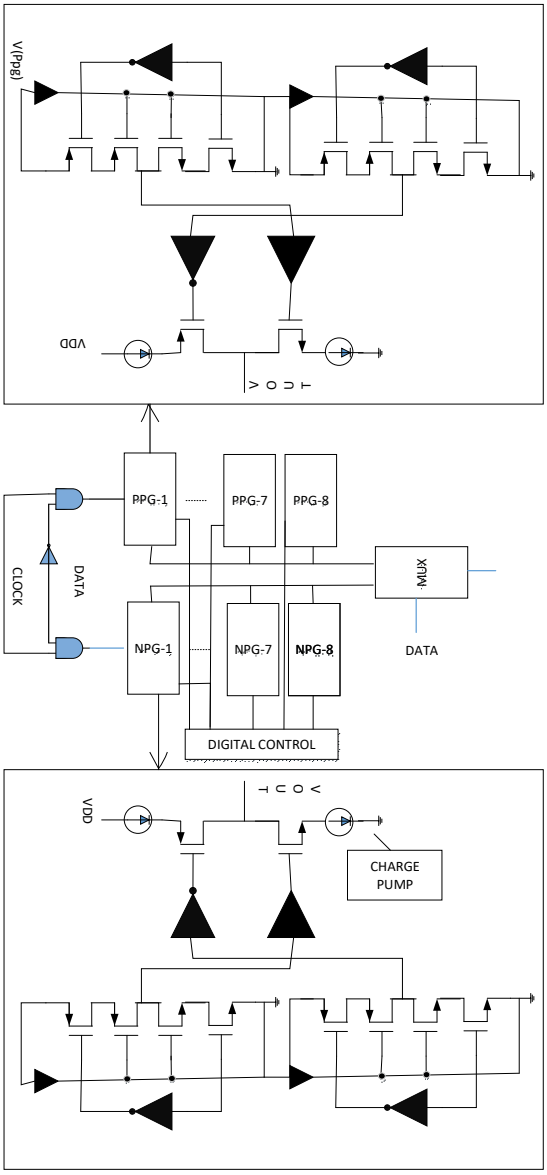


Fig. 21. Phase detector circuits [17]

negative and positive pulse Generator blocks (NPG/PPG), modulator, and output buffer circuits. DE multiplex (DEMUX) circuit using two static CMOS NAND blocks and an inverter circuit to select the output gates. When the input data is "1," the AND gate output is a high voltage, and the negative pulse generator blocks are activated, resulting in an output waveform with a "0" degree phase. Also, when the data signal is "0," an inverter activates the AND gate and positive pulse generator blocks, producing an output waveform with a "180" degree phase. The negative or positive pulse generator combines edge combiner circuits, buffer, inverter buffer circuits, and charge pump circuits. The edge combiner circuit is the main component that generates a waveform from the phase difference between the signals at the inputs. The designer creates a delay, as in previous methods, by using a static inverter to generate a pulse with a phase detector. In this design, because of the different current levels, the



charge pump's transistor cannot directly connect to signal V(c). Thus, buffers are used to gradually increase the driving capability of the charge pump's transistor.

In this design, a multiplexer selects the positive pulse generator or negative pulse generator as an output; meanwhile, it matches the output to 50 ohms.

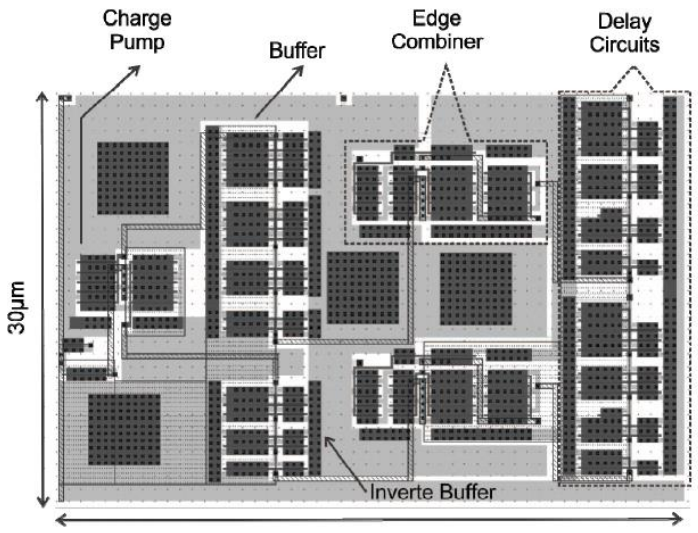


Fig. 23. Fabricated IC [34]

There is no difference between positive and negative pulses in imaging applications, and providing both only complicates the circuit. As a result, this circuit is unsuitable for imaging applications.

Previous researches have shown that voltage control oscillators (VCO) can also produce a Gaussian pulse. However, the Gaussian pulse's starting stage is arbitrary because the differential component of the noise at the VCO core determines the oscillation starting point. In another paper [35], asymmetrical topology is employed by traditional cross-coupled VCOs instead of the past simple symmetric oscillator. In asymmetric VCO, the deterministic differential DC component at the VCO core sets the starting point of oscillation. Therefore, the radiated impulsion phase is locked to the arrival time of the trigger signal. This design comprises a digital buffer, a cross-coupled asymmetric VCO, a

power amplifier, and broadband bowtie antennas, as shown in Fig. 24. In this design, the CMOS buffer input is fed to the trigger signal. The buffer input impedance is measured to be 50 ohms to minimize the reflection and ringing of the trigger signal. The buffer sharpens the control signals and regulates the asymmetric cross-coupled VCO's current source. Two voltage control capacitors are used at the center of the oscillator to adjust the frequency of oscillation. A single-stub shunt-matching network is inserted before the on-chip bowtie antennas at the collector node of power amplifier transistors. An impedance matching network provides the necessary oscillation inductance and enables maximum power transmission from the VCO to the power amplifier. At the end of the transmitter, the on-chip bowtie antennas are intended for the wideband operation to transmit the signal. Despite the fact that this design has

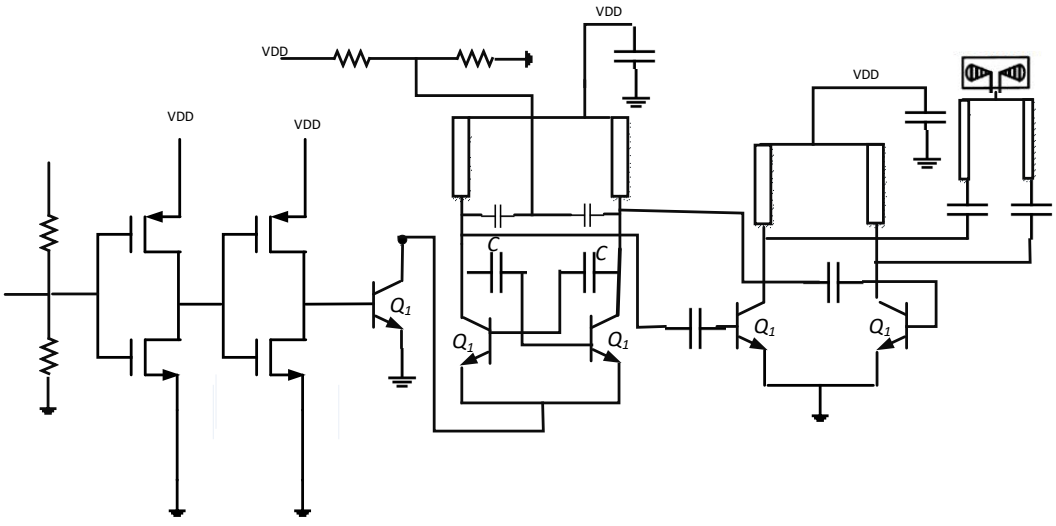


Fig.24 Gaussian pulse generator with Asymmetric VCO [35]

a narrow pulse width Gaussian pulse, the ringing level is high due to the use of an oscillator. As previously stated, the ringing is undesirable for imaging applications.

5- This Work

Gaussian pulse can be made by a discrete device or an integrated circuit. In this research, two different circuit structures are simulated and designed to generate a Gaussian pulse. The first design is a high-power Gaussian pulse generator system with discrete switches, and the second one is an integrated circuit in 65nm technology which makes a narrow Gaussian pulse with a few picosecond pulse widths. Both structures show a successful result for Gaussian pulse transmitters, and can be employed in different ultra-wideband devices for various applications.

5-1 Making Gaussian pulse system by Avalanche transistor

In this design, a Gaussian pulse system is designed by three Avalanche transistor stages. The Gaussian pulse width of 481 ps with 51V amplitude is achieved at the output. This Gaussian pulse is converted to a Monopulse by a Balun to be more compatible with an antenna for UWB transmitter systems.

5-1-1 Avalanche transistor

Despite the conventional transistors, which break down with high collector-emitter voltage, some transistors are developed to work as a switch in their Avalanche region by means of a high voltage level. These transistors are called Avalanche transistors which are appropriate for high voltage applications. The Avalanche

voltages of the typical transistors are in the range of several volts to a few hundred volts. The collector-emitter junction of an Avalanche transistor in the *OFF* state can be connected by applying a voltage of more than the Avalanche voltage.

Figure 25 depicts the measured piecewise output characteristics of this design's Avalanche transistor. When the voltage is applied to the negative ramp, it acts as a negative resistor, indicating that the voltage polarity differs from the current polarity. This situation is analogous to an unstable condition that functions as positive feedback. According to Fig. 25, a transistor in the cut-off region excited by a high collector-emitter voltage, BVCEO, can provide an almost short circuit path between its collector and emitter pads with a capability of passing high current. This phenomenon comes from a strong electric field appearing at the transistor collector, which produces electron-hole pairs [36]. The electric field will increase the electron-hole pairs then an abrupt current flows through the collector-emitter path because of the Avalanche multiplication effect [37]. As shown in Fig. 25, the

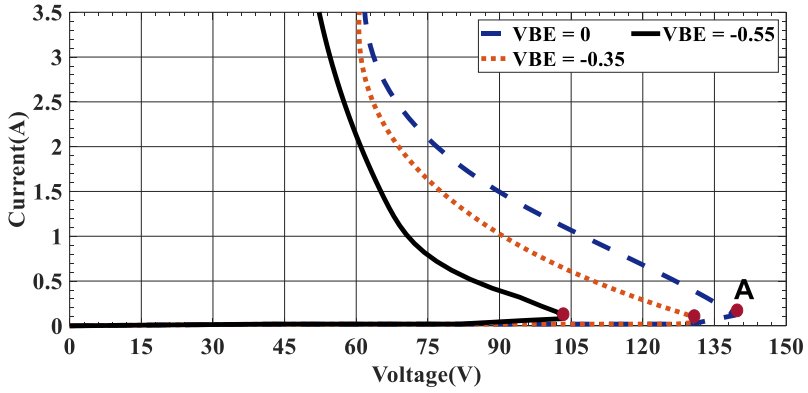


Fig. 25.Avalanche operation work

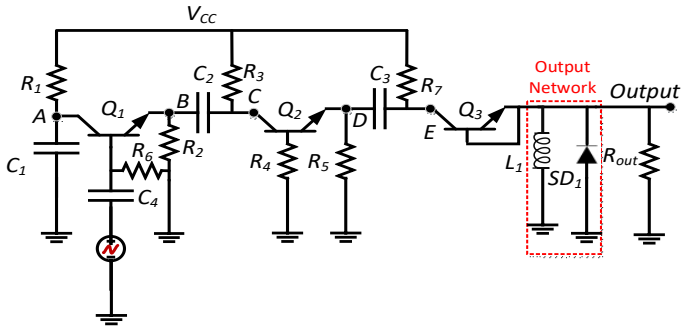
breakdown knee point of *"A"* can be moved to higher/lower voltages by using different V_{BE} and corresponding I_B. In other words, for an NPN transistor, the Avalanche multiplication effect can be produced by either an excessive electric field when V_{BE} is equal or less than zero or a lower electric field and a positive V_{BE}.

There are different kinds of Avalanche transistors like 2N4014, FMMT417, etc. the breakdown voltage of these models is different from 40 v to 350v. In this design, 2N4014 is used, which has an Avalanche breakdown voltage of more than 80 V.

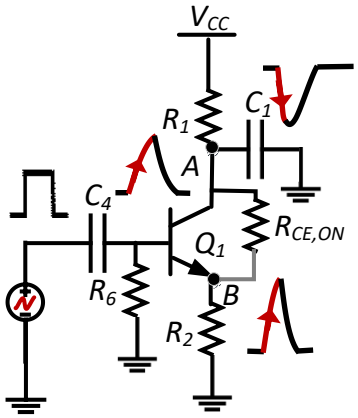
5-1-2 Three-stage Marx Avalanche transistor circuit

In this design, a Gaussian pulse is generated by using a series of Avalanche transistors. This series structure is known as the Marx structure, which can increase the output pulse amplitude [15]. This structure is shown in Fig. 26 (a). Each transistor stage is used to develop a Gaussian pulse by charging and discharging a capacitor which is switched by the Avalanche transistor. Three transistor stages can increase the amplitude of the Gaussian pulse by a factor of three. However, there is a trade-off between the pulse width and amplitude of the Gaussian output pulse. In other words, a significant part of the output amplitude is sacrificed to achieve a proper pulse width. In this design, each stage produces an amplitude of around V_{CC}. Then the outputs will be added up to each

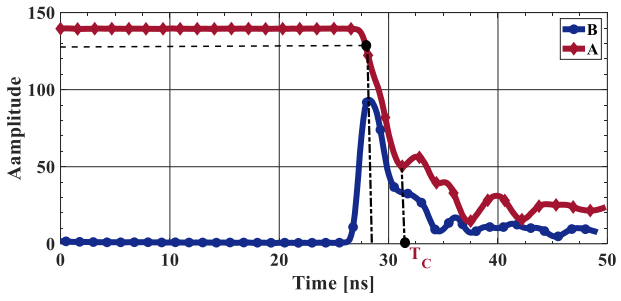
other, and a voltage equal to almost three times bigger than the V_{CC} is produced



a)



- b)



c)

- Fig. 26.a) Three-stage Marx Avalanche transistor b) First stage Of Marx circuit c) (c) measuring R_{CEON}

at the output of the design. For the stages, the produced output Gaussian pulses result from the fact that the voltage of V_{CC} is charged on the capacitors of $C_{1\text{-}3}$, then transistors are switched on and discharge the voltages of the capacitors using resistors R_2, R_5, R_{OUT}.

Fig. 26(b) shows the first stage of the design. C_1 is charged by the maximum value of V_{CC}, through R_1 with a time constant of $\tau_1 = C_1 \times R_1$. The developed voltage on C_1 will be transferred to the right side through the transistor collector-emitter path when the trigger pulse excites the base of the transistor. During this time, the collector-emitter path represents a resistive behavior, $R_{CE,ON}$, which can, in turn, degrade the output amplitude. The amplitude at point B is calculated as follows.

$$V_B = V_A \times \frac{R_2}{R_2 + R_{CE,ON}} \tag{1}$$

Fig. 26(c) shows the pulses of points A and B. As can be seen from Fig. 26(c), the charges on C_1 will be discharged through the collector-emitter of Q_1 and $R_{1,2}$ by a fall time of almost equal to $(((R_2+R_{CE,ON})\|R_1)\times C_1)$, which is slow in the range of 4.3ns; however, the measured 10 to 90 percent rise time of point B is fast, at around 360 ps. Note that, all the time, a low DC current flows from V_{CC} through R_1 to charge C_1, irrespective of the state of Q_1. As can be seen from Fig. 26(c), the expected intersection point of these two graphs is around 108 V. However, the $R_{CE,ON}$ of Q_1 pushes the real point to just below 97 V. According

to (1) and considering the difference between the voltages of points A and B, $R_{CE,ON}$ of 14Ω, is calculated. The transferred voltage at point B is discharged through R_2 with a time constant of $\tau_2 = C_1 \times (R_{CE,ON} + R_2)$. Besides, R_2 provides a path for the capacitor C_2 to be charged to the maximum amplitude of V_{CC} with a current function of $I_{(t)}$, as follows.

$$I(t) = \frac{V_{CC}}{R_3+R_2} e^{-\frac{t}{(R_2+R_3)\times C_2}} \quad (2)$$

By the passage of time, the current of $I_{(t)}$ tends to get to zero before applying the trigger pulse. At that time, the voltage dropping at point B is zero; therefore, the voltage of V_C is equal to the charged voltage of C_2, which is V_{CC}. The charged voltage on C_2 creates a high electric field on the collector-emitter junction of Q_2, and it is not enough to shorten the collector-emitter path of Q_2. However, by applying the trigger pulse, the dropping voltage at V_A is transferred to V_B abruptly. The voltage level of V_B is added to the previous voltage of V_C immediately. Therefore, the collector voltage of Q_2 jumps to a value of more than the breakdown voltage of the transistor. The electric field of the transistor rises; meanwhile, electrons combine with holes, and a short-circuit happens for the collector-emitter junction. So, the collector-emitter of Q_2 will be connected, and the V_C is transferred to V_D; however, part of this voltage drops on the $R_{CE,ON}$ of Q_2. Also, a fraction of this voltage is discharged through R_5. The third stage will follow this trend. The output voltage would be a summation of $V_A + V_C +$

V_E, which is discharged through R_{out}. Note that the R_2 and R_5 should be high enough not to discharge their whole voltages before R_{out}.

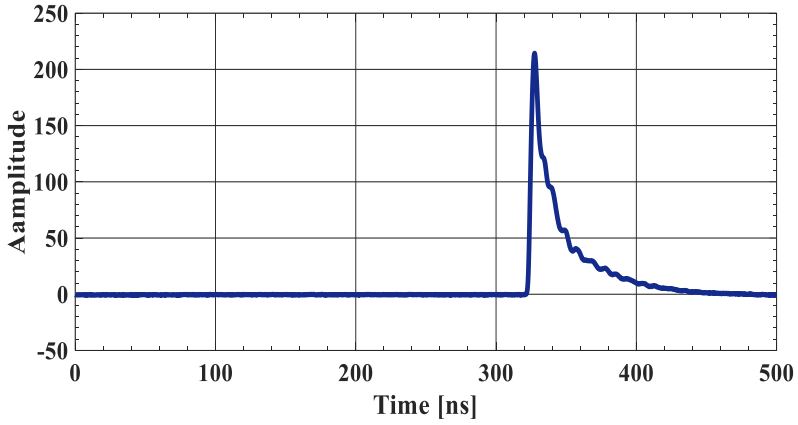


Fig.27 Marx Avalanche transistors output

5-1-3 Enhanced Marx Gaussian pulse generator circuit

Fig. 27 shows a measured output Gaussian pulse of around 214 Volt. The pulse width of this output is as wide as several nanoseconds, which is not suitable for imaging applications. One possible way to reduce the pulse width is to decrease the capacitance values of C_1, C_2, C_3. Following this procedure, a pulse of narrower width at the cost of lower amplitude will be achieved. By reducing the capacitances of $C_{1\text{-}3}$, a better pulse width of around 700 ps and amplitude around 100 V is achieved.

At the output of Fig. 26, an output network consisting of a parallel L1 and SD1 is accommodated for optimal pulse width. The inductor of L_1 is used to reduce

the pulse width. In other words, L_1 accompanied by the resistance seen at the output point, V_{OUT}, acts like a high pass filter that blocks low-frequency components of the Gaussian output pulse. As the result of using the filter, the output pulse of narrow pulse width with a lower amplitude is extracted. This output pulse has a positive polarity which suffers from a negative part. The fast Schottky diode of SD_1 is used to eliminate the negative part of the output pulse. Thanks to the high-frequency Schottky diode of BAT 62-03W, the output ringing level of the Gaussian output pulse will be less than 6 percent which is negligible. Fig. 28 shows the Gaussian output pulse with a pulse width of around 480 ps and amplitude of just above 50 V.

5-1-4 Monopulse shaping network

A conventional procedure to convert a Gaussian pulse to a Monopulse is to use a broadband differentiator at the proposed Gaussian pulse network output [4].

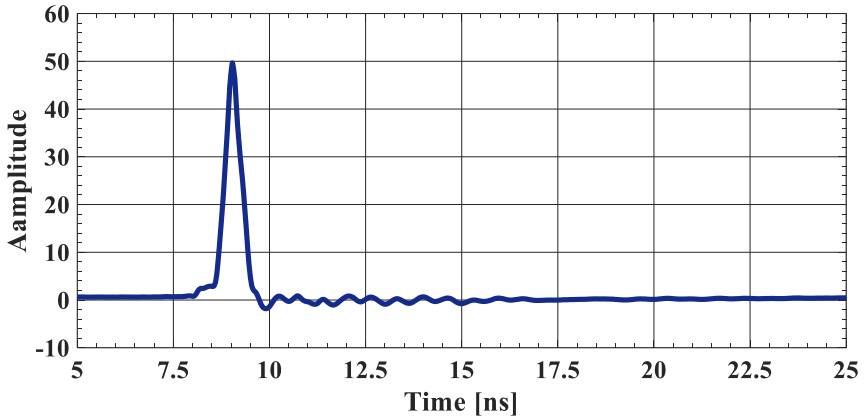


Fig. 28. Enhanced Gaussian pulse

However, designing a differentiator is challenging, but having a high-quality Monopulse with a significant amplitude at the system's output is also cumbersome. An alternative way of producing a Monopulse out of a Gaussian pulse is to provide two branches of Gaussian pulse shaping networks then

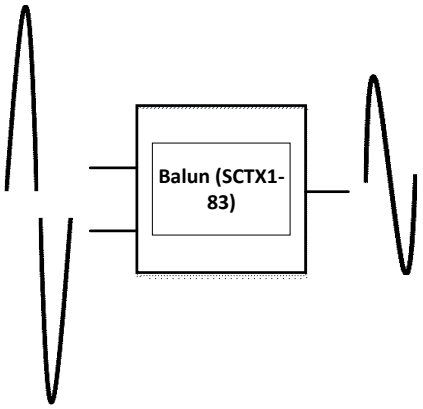


Fig. 29. Monopulse generation method

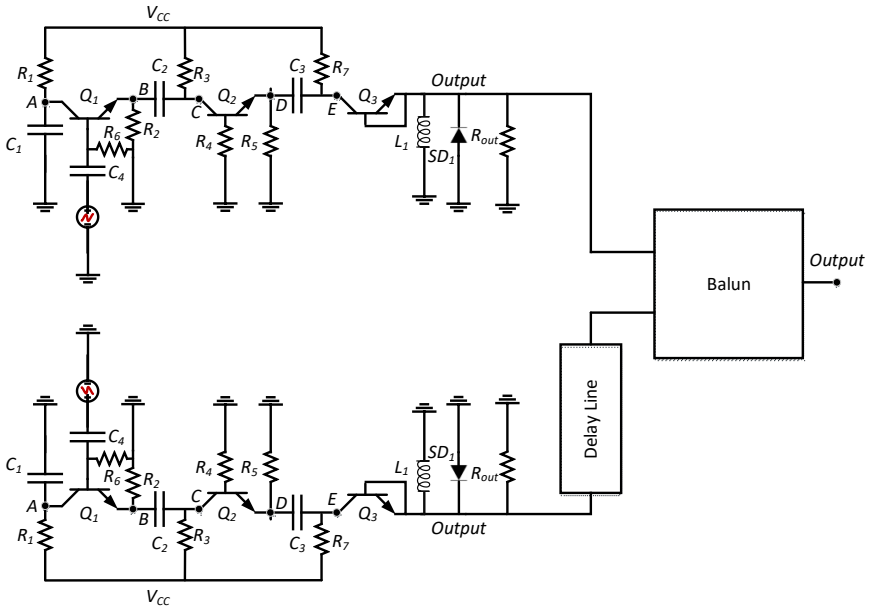


Fig. 30. Monopulse generator schematic

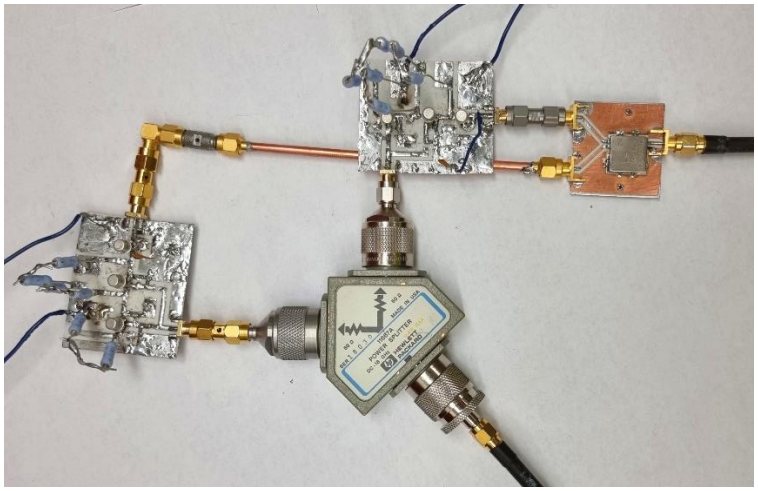


Fig. 31.fabricated circuit

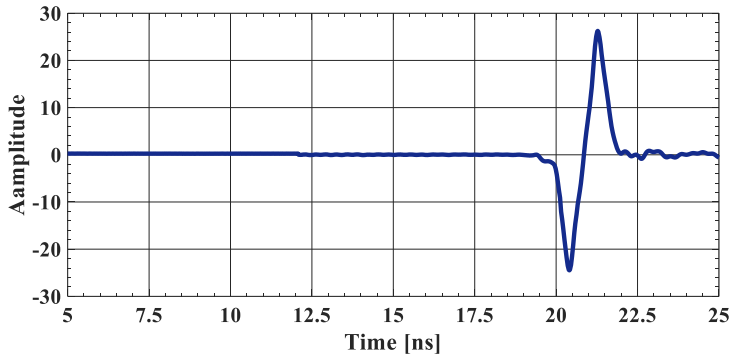


Fig 32. fabricated circuit output

subtract the output pulses. Fig. 29 shows this method. In doing so, an extra delay for one of the branches is provided. Then a subtractor is used to mix up the outputs. Fig. 30 shows a schematic of the design, and Fig 31 shows the fabricated circuit. A balun, model SCTX1-83, is exploited to subtract the output pulses. The empirical coupling voltage rate between the input and output ports of the balun is just above 51 percent. This value demonstrates that balun

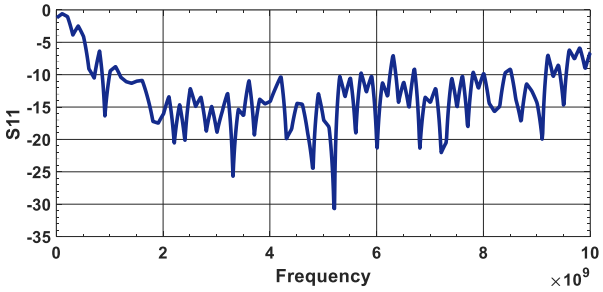
provides a more efficient rate to convert a Gaussian pulse to a Monopulse as compared to a differentiator-based pulse shaping network. The output Monopulse of this design shown in Fig. 32 reveals a Monopulse of 483 ps and 51 V of pulse width and peak to peak amplitude, respectively. The output peak power of this Monopulse is around 12.5 Watt, which is suitable for a high penetration depth application.

A Vivaldi antenna shown in Fig. 33(a) is used to propagate the pulse. S_{11} of the antenna is shown in Fig. 33(b). The -10 dB bandwidth of this antenna is from around 0.8 to 9 GHz. Another same antenna is placed 20 cm apart from the transmitter to receive the radiating pulse. The received pulse is a second derivative Gaussian pulse, which is shown in Fig. 33(c). The pulse has a pulse width of 478 ps. Moreover, the normalized spectrum of the second derivative Gaussian pulse, shown in Fig. 33(c), is depicted in Fig. 33(d). According to Fig. 33(d), the -10 dB bandwidth of the pulse is from 0.2 GHz to 1.05 GHz.

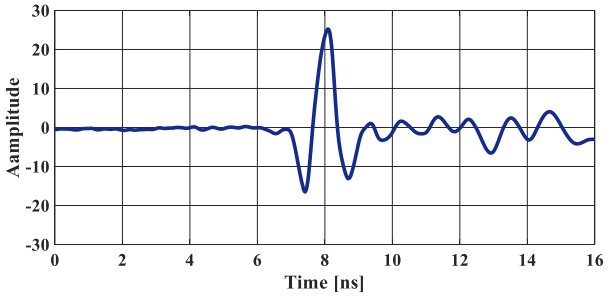
5-1-5 imaging

The proposed high-power Gaussian transmitter is useful for the detection and imaging of underground structures. The experimental setup includes a cubic sandbox that emulates the ground, two Vivaldi antennas (transceiver), and an automated measurement system, as illustrated in Fig. 34 (a). The synthetic aperture radar (SAR) technique is exploited to increase the cross-range resolution [22].

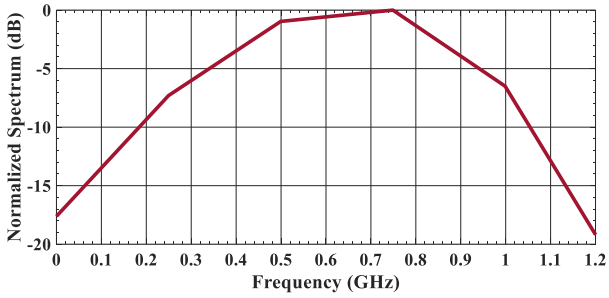
a)



b)



c)



d)

Fig 33. Vivaldi antenna b) antenna's S11 c) received signal from 20 cm distance d) output spectrum of the second derivative Gaussian pulse of Fig. 5(c).

The data acquisition is completed in the XY plane, with a 2 cm increment in each direction and a total aperture length of 48 cm. The target is copper ore, as shown in Fig. 34 (b). The target has been buried in a depth of 45 cm. Two sets of measurements are performed: one as the target scene with the absence of the buried target, including measurement fixtures, sandbox, surrounding objects (Ambient signal), and one the target scene with the presence of the buried ore. The calibration process is performed as follows:

$$s_{calibrated} = s_{Raw} - s_{Ambient} \quad [3]$$

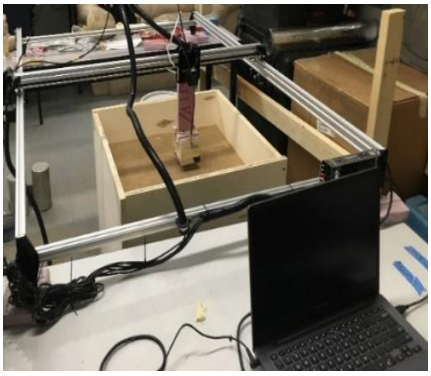


Fig. a)

Fig. b)

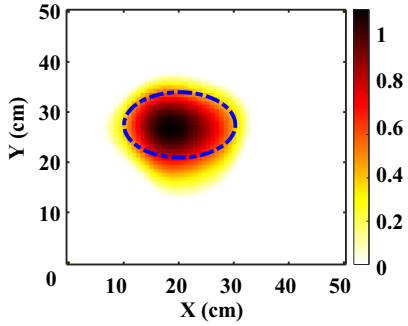


Fig. c)

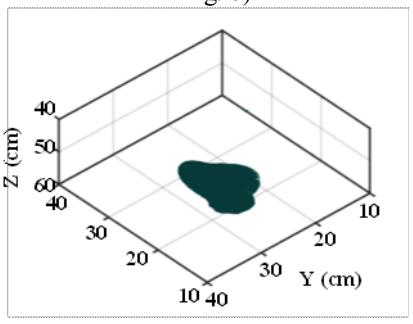


Fig. d)

Fig. 34. a) Experimental setup b) target c) 2D cross-section of reconstructed image d) 3D isosurface image

Fig. a)

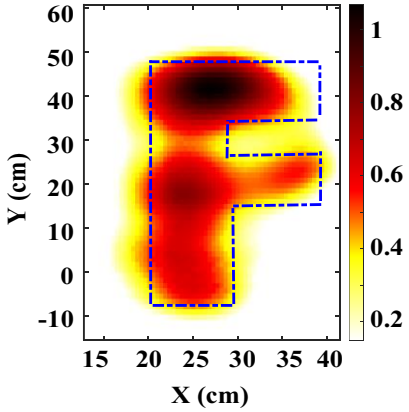


Fig. b)

Fig. 35. a) Experimental setup b) 2D cross-section of reconstructed

Where $s_{calibrated}$, s_{Raw}, and $s_{Ambient}$ are the calibrated signal, the measured signal with the buried target, and the ambient signal, respectively. The time-space measured data is transformed to a 3D image using time-domain global back projection (TD-GBP) [38]. The 2D cross-section and 3D isosurface of the images are illustrated in Fig. 34 (c) and (d). As can be seen, the designed transmitter is prosperous in high-depth microwave imaging due to its high-power property.

Then, a metal object in the shape of the letter "F," as shown in Fig. 35, has been buried in the depth of 12 cm of sand. The same data acquisition and calibration procedure are performed, and the 2D reconstructed image in $z = 12\,cm$ is illustrated in Fig. 35. Furthermore, the designed high-power transmitter is tested for underwater imaging experiments. A container with the dimension of 40x60 cm^2 is filled with water and a metal object (14x14 cm^2) is submerged in depth of 25 cm. The 2D cross-section image and 3D isosurface image are illustrated in Fig. 36. As

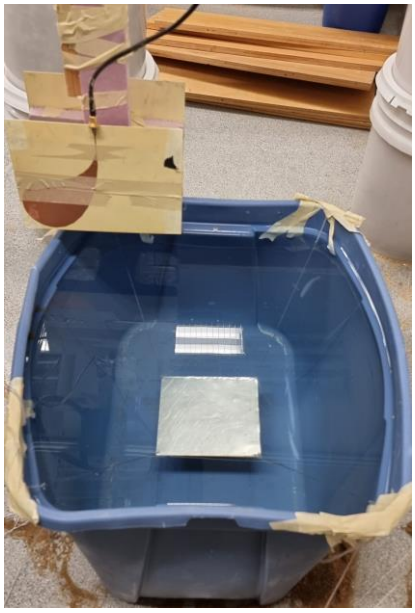


Fig. a)

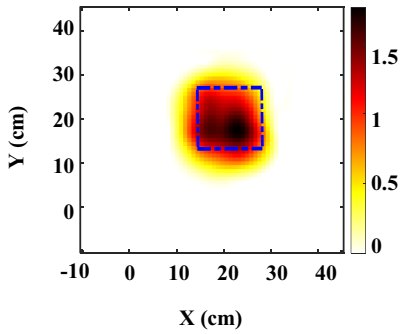


Fig. b)

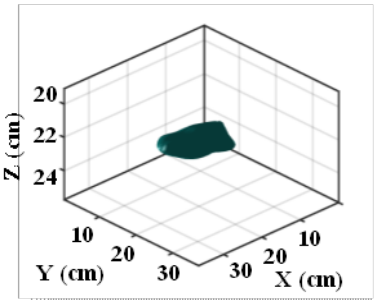


Fig. c)

Fig. 36. a) Experimental setup b) 2D cross-section of reconstructed image c) 3D isosurface image

can be seen, the designed transmitter is successful for underwater imaging even in the lossy medium such as water.

5-1-6 comparison to other designs

The output Monopulse of this system represents a high-quality pulse suited for the high penetration imaging system. A criterion of comparison is useful for comparing the proposed design to the other published papers. Papers with Marx's structures are chosen to ensure fairness in the comparison. For a Monopulse, some specifications such as amplitude, pulse width, ringing, number of transistors, and dc supply need to be evaluated. However, instead of

TABLE 3

comparison between Gaussian pulse generators

Ref	Amplitude (V)	pulse width (ns)	Ringing (%)	Efficiency (%)	Number of transistor	FOM
[9]	470	~1	~10	36	5	2.11
[42]	7000	17	~7.1	~55	36	0.45
[39]	5200	7	~28.4	46	37	0.23
[40]	1800	4	~31	~46.8	12	0.37
[41]	4000	20	~28.2	37	36	0.06
[43]	1100	1.3	~31	8.7	8	0.21
This Work	50	0.48	6	15	3	5.2

focusing on the output Monopulse, the overwhelming majority of the published papers related to the Avalanche transistors have reported the Gaussian output pulse. Hence, a figure of merit is presented for this work for the Gaussian output pulse. Obviously, for having a high-quality pulse, high amplitude, narrow pulse width, low ringing level, and high efficiency are of interest. The efficiency of the Avalanche-based pulse generators is calculated as follows.

$$\text{Efficiency} = \frac{output\ peak\ voltage\ of\ the\ generator}{maximum\ theoretical\ output\ voltage} \tag{4}$$

Where maximum theoretical output voltage can be found as the number of stages multiplied by the charging voltage, the proposed FOM is recommended to cover all the pulse specifications as follows.

$$FOM = \frac{Efficiency}{Pulse\ width \times Ringing} \tag{5}$$

Note that because efficiency covers up amplitude and number of transistors, these parameters are not accommodated in the above equation.

Table 3 has elaborated the specification of some published papers and evaluated the superiority of this work upon the others. In [9], a typical Avalanche Marx structure was presented with a FOM of more than 2. However, their design suffers from the floating ground. In other words, the design of [9] utilizes two separated ground; one for the input trigger pulse and the other for the entire configuration. Papers of [39] and [40] represent a high-efficiency factor, but their ringing levels are too much for imaging purposes. In [41], the design has a high amplitude output signal but increased pulse width. [42] depicts a low ringing level Gaussian pulse with high pulse width. [43] offers a low efficiency and high ringing pulse, which causes low FOM. The proposed work represents a medium amplitude Gaussian pulse with a suitable pulse width, acceptable efficiency, and high FOM. The design is suitable for a detection range of up to 2 meters in dry sand, with a decent range resolution.

5-2 An enhanced method for Gaussian pulse generator in integrated circuit

This chapter proposes an enhanced method for generating a Gaussian pulse utilizing a differential pair circuit in 65nm technology. This design is an integrated circuit (IC) that is faster and has a better pulse width than the discrete

switches. The circuit has the special feature of having changeable output pulse width. Because the output pulse width is changeable, it is possible to get different range resolutions for various applications without designing a new circuit.

5-2-1 IC design

An integrated circuit, often known as an IC, is made up of a sequence of a series of electronic circuits on a flat thin semiconductor material [13]. Integrating large numbers of small Mosfets into a small chip result in faster and cheaper circuits than those constructed of discrete components [44]. The technical developments in the manufacturing of semiconductor metal-oxide-silicon devices have made integrated circuits practical. The performance of ICs is much better than discrete systems. Also, packaged ICs use much less material than discrete systems and have high efficiency due to their low size and proximity, which enables them to switch rapidly and use considerably lower power [45]. Integrated circuits are fabricated with different technologies and classified into analog, digital, and mixed signals consisting of analog and digital signals together. In this design, 65nm technology is used for a mixed-signal integrated circuit. ICs are manufactured in a planar process involving photolithography, deposition, and etching as three main process steps [45], [46]. There are nine distinct interconnection layers on our circuit. By a layer of dielectric, each level of

interconnection is isolated from the other. Vias are used to render vertical connections between interconnections at various levels. The thickest and widest metal layers of the upper layers of a chip cause the wires on those layers to have the least resistance and the shortest constant *RC* time, so they are being used for power and clock supply chains. Also, there are thin and short wires on the lower part metal layers of the chip, closest to the transistors, only for local interconnection.

5-2-1-1 Cadence Software

In this circuit, Cadence software is used to design the IC. Cadence Design Systems is software published by a US company for electrical engineering and has been used for 30 years to fabricate integrated circuits, printed circuit boards, chip systems, hardware, and silicon structures. Cadence has several fully custom integrated circuit design tools, includes Schematic simulation, Layout simulation, and post-layout simulation. Cadence is mainly used for designing analog, mixed-signal, radiofrequency, and digital circuits. For developing a circuit, first of all, the circuit must be simulated in Schematic. There are several different simulations in the Schematic section to investigate the operation of the circuits, such as DC simulation, AC simulation, transient simulation, etc. In this design, DC simulation is used to find the DC voltage of each node and check that the circuit biasing is suitable. The AC simulation is used to find which

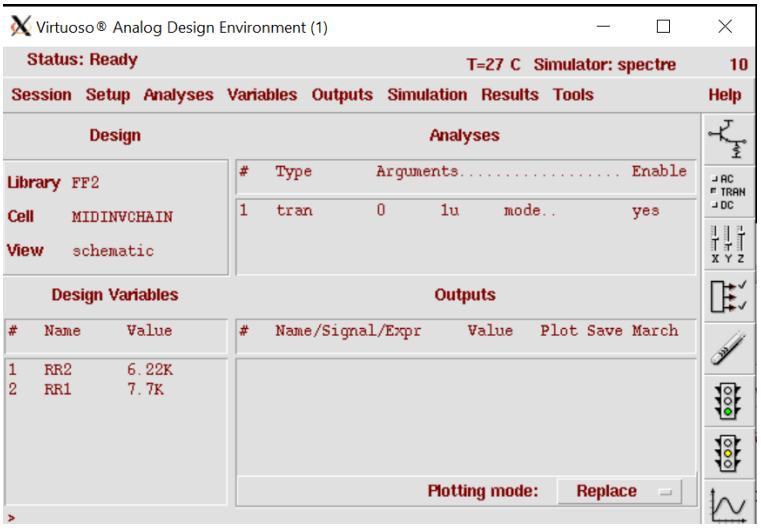


Fig.37 transient simulation setup

frequency band our circuit works, and transient simulation is utilized to find the circuit's output as a function of time and investigate the output Monpulse characteristics.

Monte Carlo simulation is also used to simulate the circuit in worse conditions that may be happened after fabrication. After designing and simulating the circuit in the Schematic part, the circuit must be developed in the Layout part before fabricating by the TSMC company. In Layout, the physical parts of each device are shown in 9 layers of the IC. The Layout designer must connect all devices without interfering with each other by considering the TSMC Layout rules. Three simulation checklists must be run after creating the identical circuit in the Schematic and Layout to ensure the validity of the circuit design before sending it to fabrication. First, it must be checked for Physical Design Rule

Check (DRC) errors. In this simulation, it matched the device for all layout rules. Some critical errors that must be corrected are:

".s" errors related to the minimum distance or space between each device.

".w" errors related to the maximum/minimum width of each line.

"*.A" errors related to the area of each device.

"G.*" errors: related to the grid that is the minimum resolution can be manufactured. Each length must not be less than the grid resolution.

".DN" errors related to the density. Specific metal and oxide densities are required for fabrication.

Following the DRC verification, the Layout Versus Schematic (LVS) simulation must be run to ensure that the Schematic and Layout similarity. Without complete similarity between Schematic and Layout, it is impossible to simulate the final version of the circuit. Finally, the Parasitic Extraction (PEX) simulation adds all parasitic elements to the circuit to act like an actual model. It adds all parasitic capacitors and resistors to the circuit to check that the circuit will work in real condition or not. After passing these simulations in Cadence the circuit is ready to send for fabrication.

5-2-1-2 High-frequency structure simulator(HFSS)

In this design, high-frequency structure simulator (HFSS) software is used to find the S parameters of each element. HFSS is software for investigating electromagnetic structures and is a commercial finite element method solver. This application is one of the commercial techniques used for designing antennas and designing complex electronic circuit elements for radio frequencies. In this Thesis it is used to generate the S parameters of each component that show the element's frequency response.

5-2-2 Methodology of Gaussian pulse generator

5-2-2-1 Schematic

The first component of this design is an inverter chain, which is used to sharpen the input triggering pulse. If the inverter's input voltage exceeds a certain threshold, the output is connected to VCC; otherwise, it is always connected to ground. Because the inverter output has only two modes, zero and one, the output pulse changes drastically, causing the input pulse to become sharper and reducing its rise or fall time. Also, the size of inverting transistors increased gradually in the inverter chain to have the minimum possible rise or fall time.

In this design, the Gaussian pulse is made by a differential pair circuit. The differential pair circuit has the benefit in the gain and linearity; moreover, it doesn't have common-mode noise because it subtracted the noise between two inputs. In this circuit, the *DC* voltage difference between the two inputs causes

the transistor to turn on and make a sharp pulse at its output. The differential pair circuit has two inputs, one of them is connected to the variable *DC* voltage, and another is connected to the sharp signal made by an inverter chain. When one of the inputs is excited by a sharp signal, the Mosfet transistor suddenly turns on and makes a low rise time pulse at the output. Another input connected to the DC voltage can change the transistor's starting point, which makes a sharp signal at the output. By changing the *DC* voltage of the other transistor (second input), the first transistor's emitter voltage which is responsible for making the output, is changed. As a result, the output pulse is created with a different time shift.

The final Monopulse is formed by combining two sharp ascending pulses and one sharp descending pulse. One of the pulses is a fixed signal, and the other two pulses can shift to have different pulse widths. An inverter chain makes the first fixed pulse, and two differential pair circuits create the other two pulses. These three pulses are added by a combination of NAND and NOR gates in the output stage. Pads outside the IC determine the voltage of one input of the differential pair circuit. By changing this voltage, the two unfixed signals that make the Monopulse shifted, and as a result, the final signal pulse width and amplitude will be changed. It means that the circuit range resolution can be changed, and different ranges resolution can be used for each application.

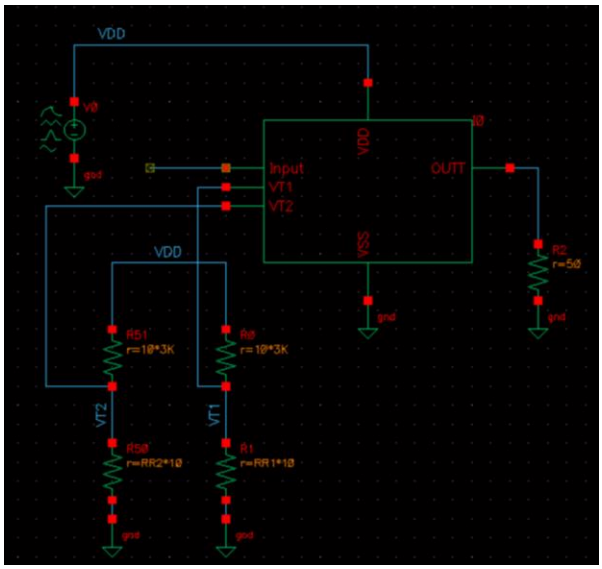


Fig. 38. Connection of IC

Finally, the antenna sends this signal to the target for detection. This circuit must be the same as the antenna input resistor, which is 50 ohms, in order to not lose power through the antenna. For this reason, a simple matching circuit that consisting of two capacitors is used. As a result, the adder circuit combines these three signals while also being matched to 50 ohms by a simple matching circuit. The Cadence-designed integrated circuit is depicted as a Cellview in Fig. 38. It shows that out of the IC, a 50-ohm resistor (antenna resistor) models the antenna's effect that will be connected to the circuit after fabrication. A *DC* power supply produces an output V_{DD} voltage (1V DC) to brings the circuit's power and turn on the transistors. Also, this voltage is divided by variable resistors to tune the circuit and connected to the differential pairs inputs. Variable resistance is changed by changing the ratio of the resistors inside of it.

The input signal of the circuit is connected to the pulse generator to get the input squire wave signal. The input squire wave signal has a period of 100 ns with a 50 ns pulse width. This pulse's rise and fall time are five ns and are defined by the pulse generator. The IC consists of 5 different sections: first falling edge circuit, first rising edge circuit, second falling edge circuit, two differential pairs, and the output circuit shown in Fig. 39.

5-2-2-2 inverter

All falling and rising edge circuits are consisting a series of inverters. The inverter's delay is attributed to the capacitive load at the output node and the logic gate's limited current. A differential equation representing the output voltage as a function of time must be solved to determine the propagation delay

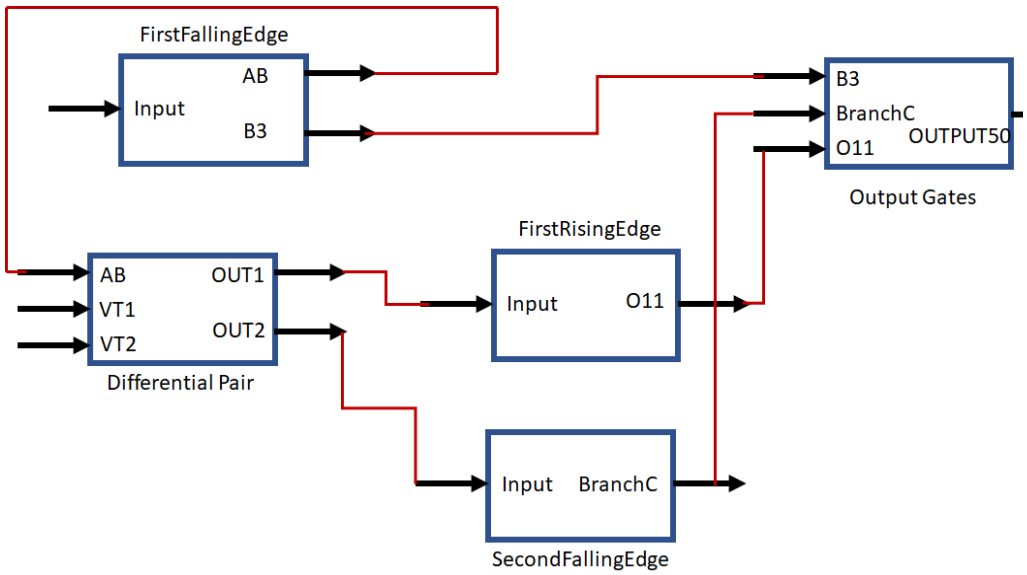


Fig. 39. IC components

that can be defined as the time when the output exceeds $\frac{VDD}{2}$. For the delay calculation, charging and discharging of the load capacitor is essential.

It is possible to model the inverter as a two-port network shown in Fig. 40 [47]. The inverter input capacitance is the summation of two intrinsic Mosfet gate capacitances, whereas the output capacitance is the summation of the Mosfet drain capacitances.

The inverter's delay can be written as a summation of rising and falling time delays [48].

$$T_{delay} = t_{risetimedelay} + t_{falltimedelay} \quad [6]$$

The delay time of each period is calculated by multiplexing the effective resistor to the capacitor.

$$T_{delay} = t_{risetimedelay} + t_{falltimedelay} = R_{effpmos}C_D + R_{effnmos}C_G \quad [7]$$

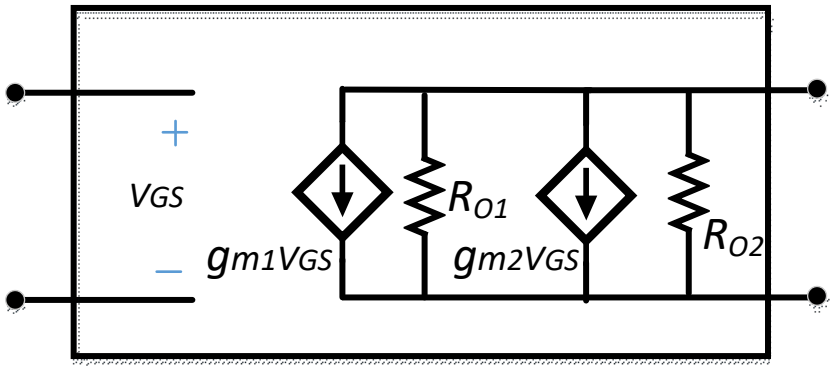


Fig. 40. Inverter two-port network model

This equation shows that delay is related to the size of the transistors; however, if the inverter connects to the circuit, which has an x branch-like Fig. 41, the average delay is calculated by the following equation [47], [48].

$$T_{delay} = \frac{T_{risetimedelay} + T_{falltimedelay}}{2} = CG \times \left(\frac{R_{effpmos} + R_{effnmos}}{2}\right) \times \left(\left(\frac{CD}{CG}\right) + x\right)$$

[8]

In this equation, R_{eff} is related to the ratio of length to width $\left(\frac{L}{W}\right)$ of a transistor and CG related to multiplying of length by width (WL), so by changing the size of inverters, it is possible to set the desired delays. Because N-channel devices have higher electron mobility, they have a higher driving capability. If we module the PMOS transistor k times wider than NMOS transistor and set R_{eff} and CG for NMOS transistor model, for Pmos delay, we have $\frac{\mu Reff}{k}$ and $k \times CG$ as its characteristics for its model where μ models the higher driving capability

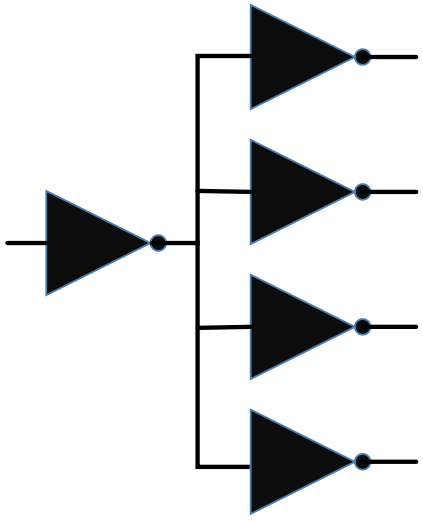


Fig. 41. An inverter connected to multiple branch circuit

of the N-channel devices. By these assumptions, the total delay will be as equation 9.

$$T_{delay} = Reff \times CG \times (1+\frac{\mu}{k}) \times (1+k) \times (\frac{CD}{CG}+1) \quad [9]$$

The minimum k for the inverter pair delay is $\sqrt{u}$ which is easily proven by equating the derivative of the last equation to zero. As a result of derivation, the PMOS must be broadened by a factor of $\sqrt{u}$ to minimize the average delay. Typically set the PMOS three times wider than NMOS to get the minimum delay.

In our circuit, we have an inverter chain like Fig. 42, whose delay will be the summation of each inverter.

$$T_{delay} = t_{delayinv1} + t_{delayinv2} + \ldots + t_{delayinvN}. \quad [10]$$

By the formula that we got before the total delay will be:

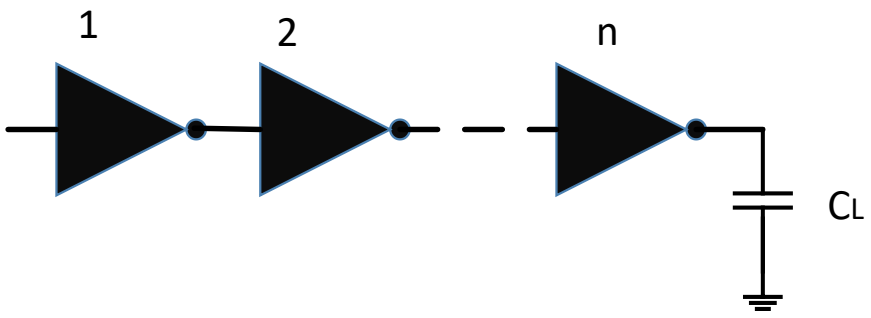


Fig. 42. Inverter Chain

$$T_{delay} = Reff \times CG1 \times (1+ \frac{\mu}{k}) \times (1+k) \times (\frac{CGin(2)}{CGin(1)} +1) + Reff \times CG2 \times (1+ \frac{\mu}{k}) \times (1+k) \times (\frac{CGin(3)}{CGin(2)} +1) +.....+ Reff \times CG(N-1) \times (1+ \frac{\mu}{k}) \times (1+k) \times (\frac{CL}{CGin(N-1)} +1) = \sum_1^N Reff \times CGi \times (1 + \frac{\mu}{k}) \times (1 + k) \times (\frac{CGin(i+1)}{CGin(i)} + 1)$$

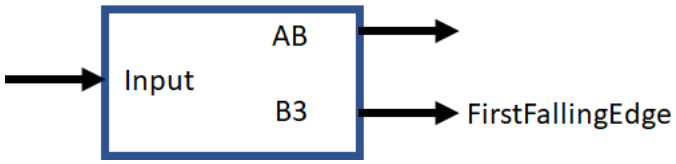
[11]

To minimize this total delay by getting the derivate of the equation and set it to zero ($\frac{\partial t}{\partial CG} = 0$) we get this $\frac{CG(i+1)}{CG(i)} = \frac{CG(i)}{CG(i-1)}$ proportion as a result. This proportion shows the *CG(i)* should be set to $\sqrt{CG(i+1) \times CG(i-1)}$ to minimize the total delay. It means that each *CG(i)* must be the geometric mean of before and after stage capacitors. Therefore, in order to get the minimum delay, each stage invertor's size must be multiplexed by the same amount. This fixed number measure as an $F = \sqrt[N]{\frac{CL}{CG1}}$. *F* is calculated by the Nth roots of the ratio of the last load capacitor to the first input capacitor, in which the N is the number of stages.

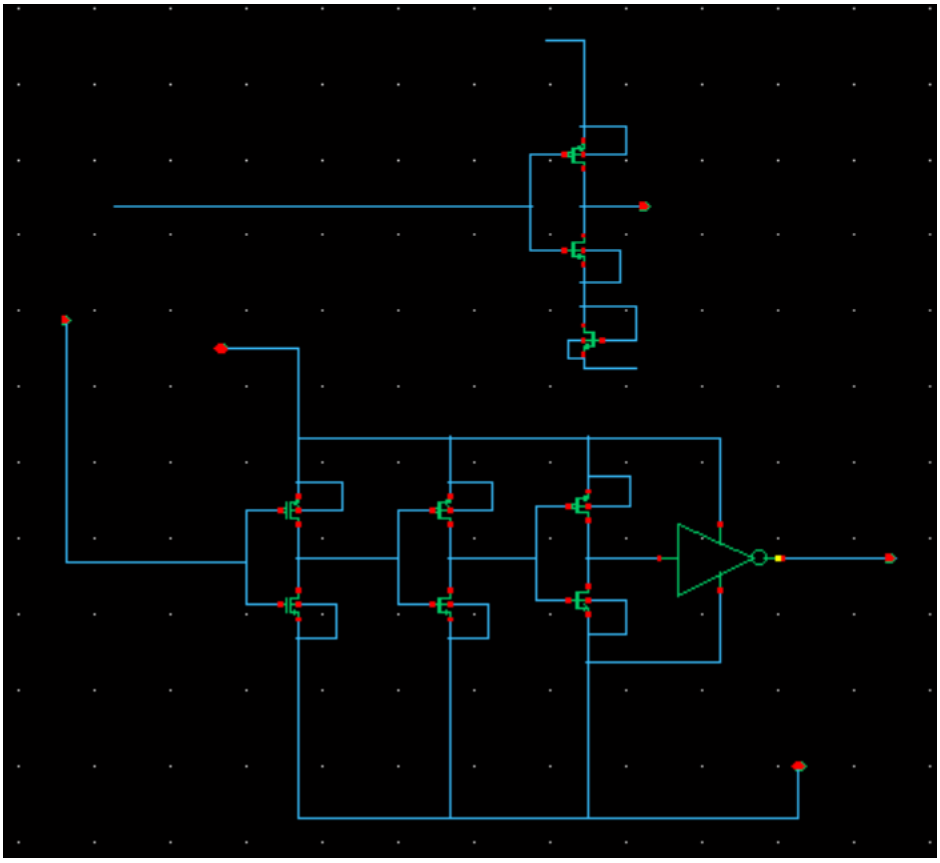
5-2-2-3 First Falling Edge circuit

The first falling edge circuit is the combining of multiple inverters that are shown in Fig. 43. The circuit's input is the squire wave signal made out of the IC by the pulse generator. The input peak-to-peak voltage is 1V, and the rise and fall times are five ns, as illustrated in Fig. 44. The frequency of the triggering pulse is 10 MHz it means the period of the signal is 100 ns. The *AB*

is the inverter chain output connected to the input of differential pairs to compare with the other differential pair input. The comparison between these inputs makes a sharp signal at the differential pair output. The first inverter chain is responsible for sharpening the squire waive and send it to the differential pair.



a)



b)

Fig. 43 a) First falling edge input and outputs b) First falling edge structure

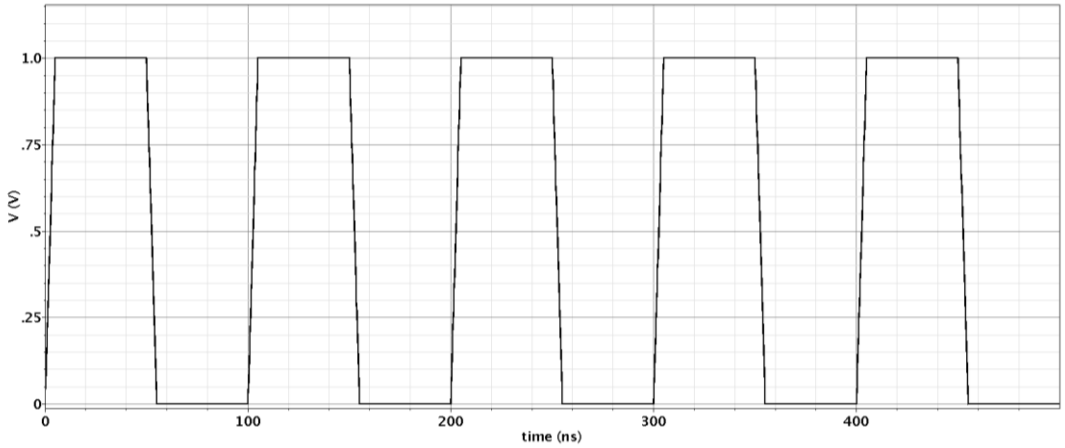


Fig 44. First falling edge input

The output of this inverter chain (*AB*) is shown in Fig. 45. the static power of the *AB* generator circuit is 0.12 Mw, and the average power is 0.72 Mw.

A different circuit makes the *B3* output consists of an inverter chain and three separate inverters. The *B3* is shown in Fig. 46. This sharp signal is connected to an adder to make the Monopulse with two other sharp signals made by differential pairs. *B3* Output peak-to-peak voltage is 1 volt, and its frequency,

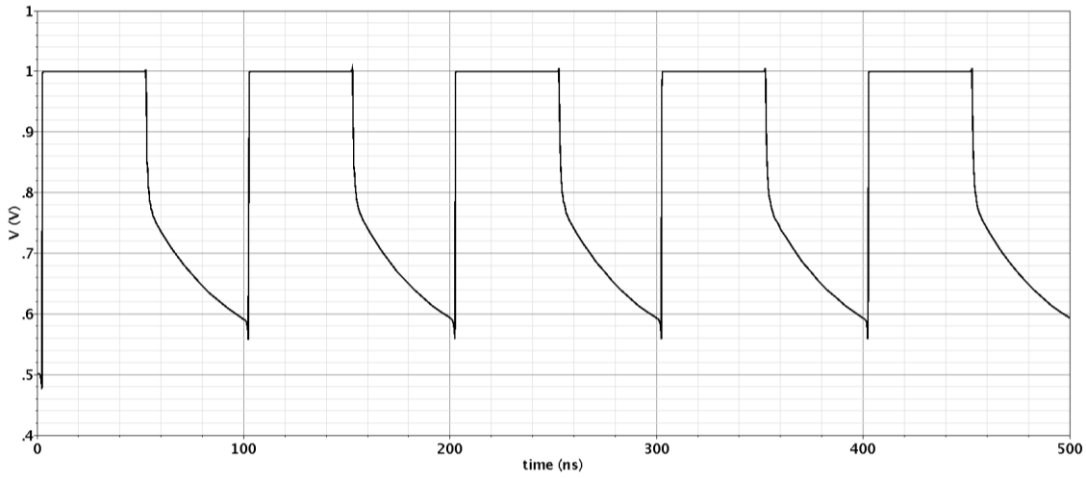


Fig. 45. The AB output

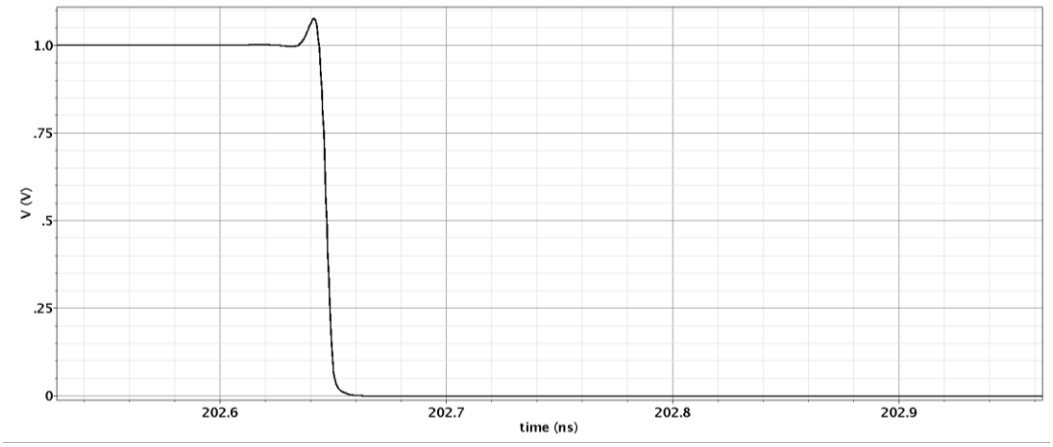


Fig. 46. The B3 output

same as the input, is 10 MHz (100 ns period). Only the rise and fall times decreased to 8 ps compared to the other output. This inverter chain is capable of sharpening pulses from less than 1 kHz to more than 1GHz frequency. However, for frequencies more than 1GHz, the period is less than 1ns; thus, a signal with a rise and fall time of less than 100 ps was required. This rise and fall time cannot be produced by lab equipment. So for the input signal, we can use pulses

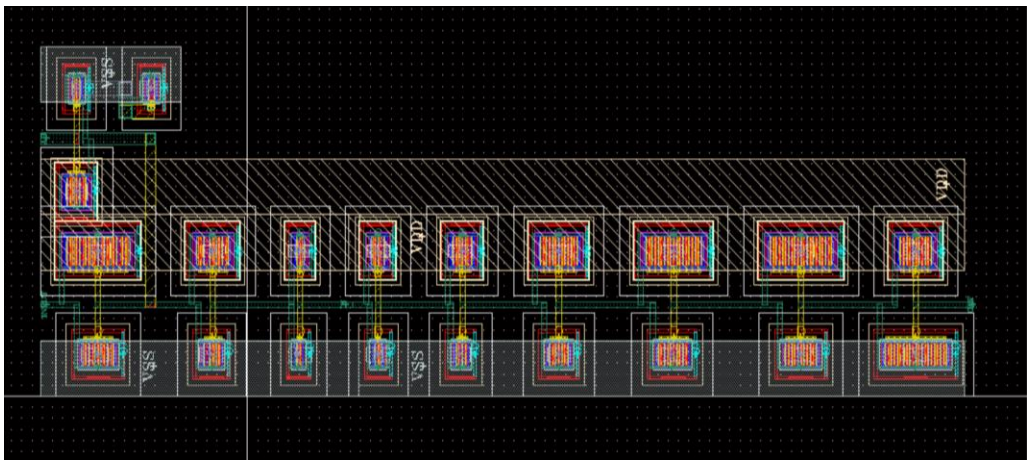
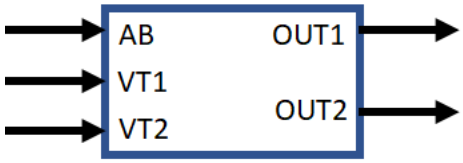


Fig. 47. First falling edge layout

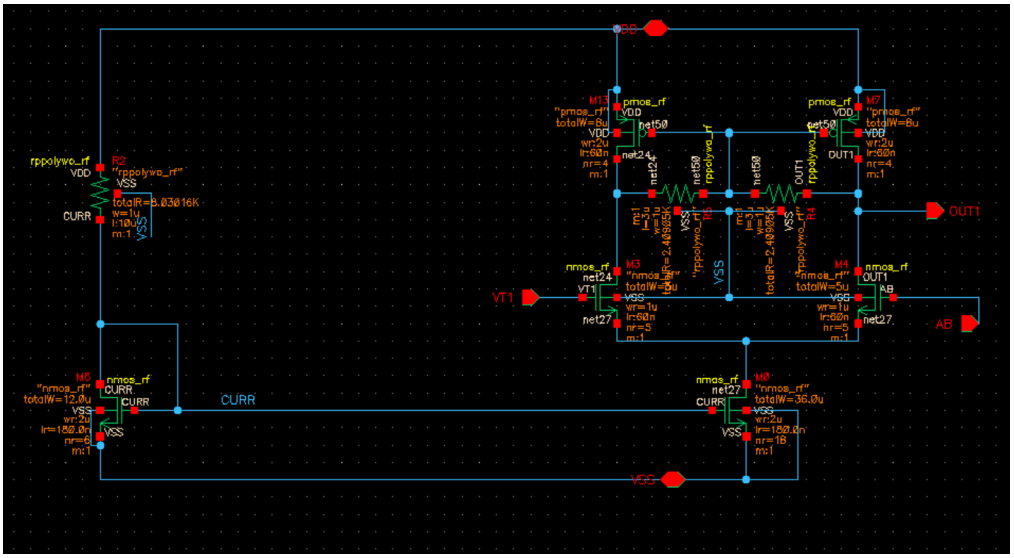
with a frequency of less than 1 kHz to around 1GHz. The physical model of the circuit is designed in the Layout section that is shown in Fig. 47.

5-2-2-4 Differential pair

The second part of the circuit provides a sharp rising edge signal for creating the Monopulse. This design consists of two differential pair circuits and a biasing circuit that determines the current level. As shown in Fig. 48, two resistors are added to the differential pair as common-mode feedback to stabilize



a)



b)

Fig 48. a) First falling edge input and outputs b) First falling edge structure

the output voltage. The circuit has two inputs, one is an *AB* signal that comes from the first falling edge circuit, and the other is a *DC* voltage determined by the tuning voltage out of the IC. The tuning voltage is divided into two branches, VT_1 and VT_2, in order to tune both differential pair circuits separately.

The output of this configuration is shown in Fig. 49. The first differential pair output is routed to the first rising edge circuit and the second falling edge circuit, producing two of the three signals comprising the final Monopulse. Differential pair configuration has static power of 0.46 mW and average power of 0.79 mW.

The final output pulse width for both positive and negative parts was investigated as a tuning voltage to test the circuit's tenability, as shown in Fig. 50. Vn/Vp denotes negative/positive amplitude, and Pp/Pn denotes

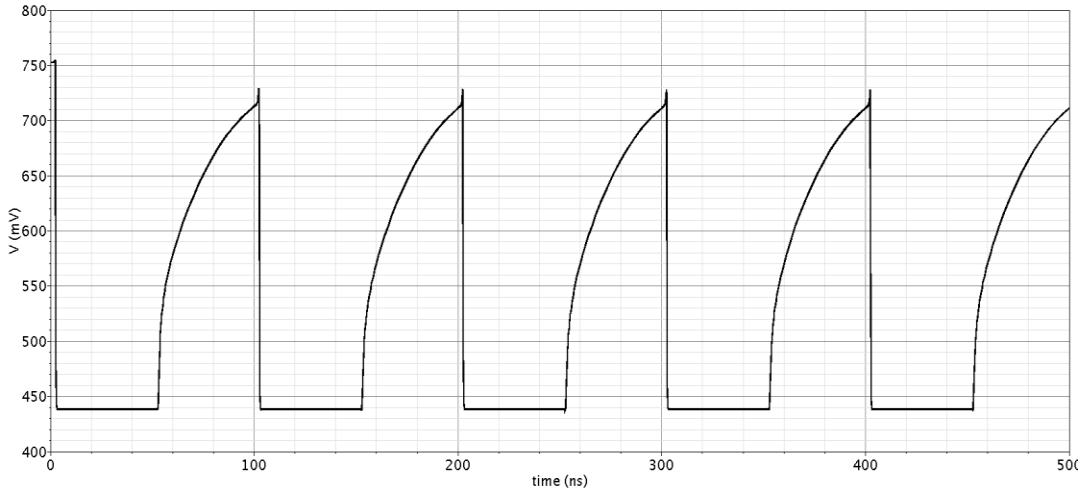
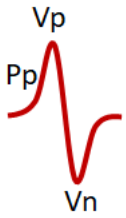


Fig. 49. Differential pair circuit output

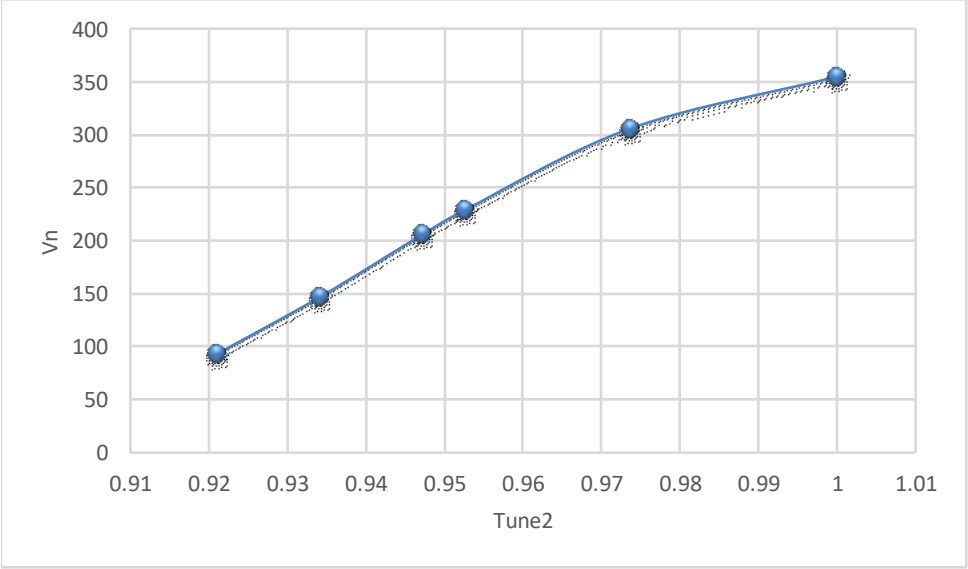
positive/negative pulse width. This graph depicts the circuit's ability to work in extensive range resolution.

5-2-2-5 First rising and second falling edge inverter chains

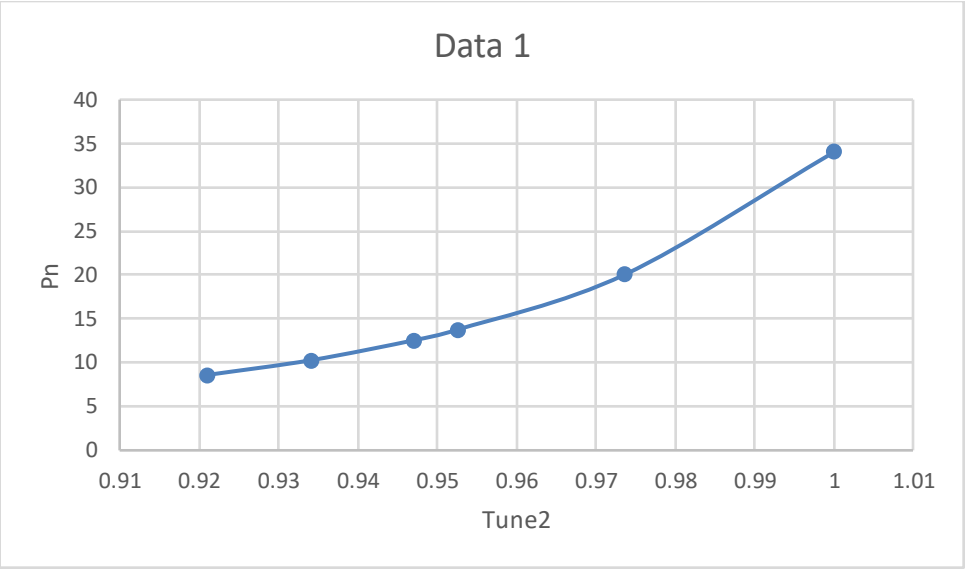
Following the differential pairs, two inverter chains reduce the signal's rising and falling time. The output of the differential pairs, *BranchC* and *O11*, is connected to the rising and falling edge inverter chains, which are then combined with the output of the first falling edge circuits, *B3*, to form the final Monopulse signal. The rising edge circuit consists of six inverter circuits, shown



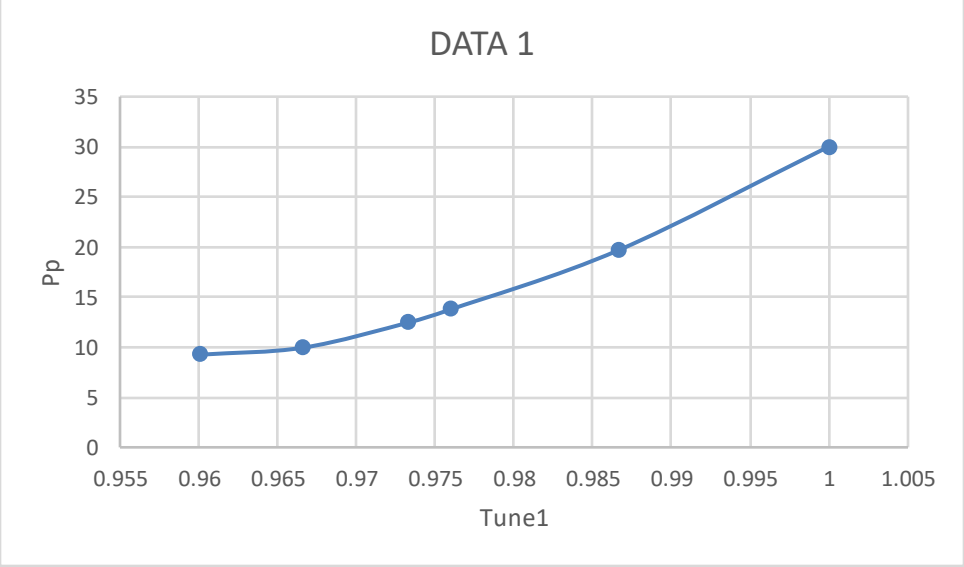
a)



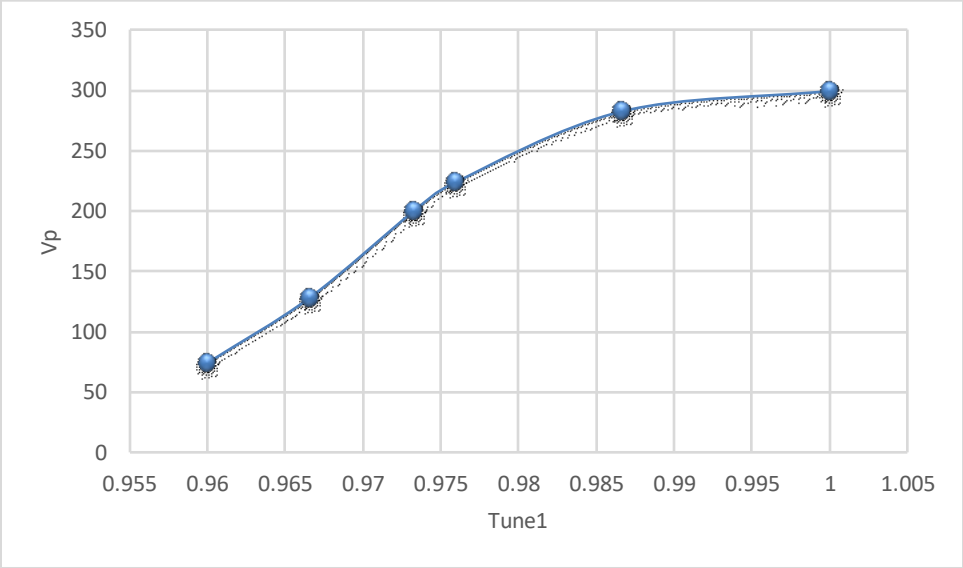
b)


Data 1
Pn
40
35
30
25
20
15
10
5
0
0.91
0.92
0.93
0.94
0.95
0.96
0.97
0.98
0.99
1
1.01
Tune2

c)


DATA 1
Pp
35
30
25
20
15
10
5
0
0.955
0.96
0.965
0.97
0.975
0.98
0.985
0.99
0.995
1
1.005
Tune1

d)



e)

Fig. 50. a) Monopulse characteristic b) negative amplitude as a function of tuning voltage c) negative pulse width as a function of tuning voltage d) positive pulse width as a function of tuning voltage e) positive amplitude as a function of the tuning voltage

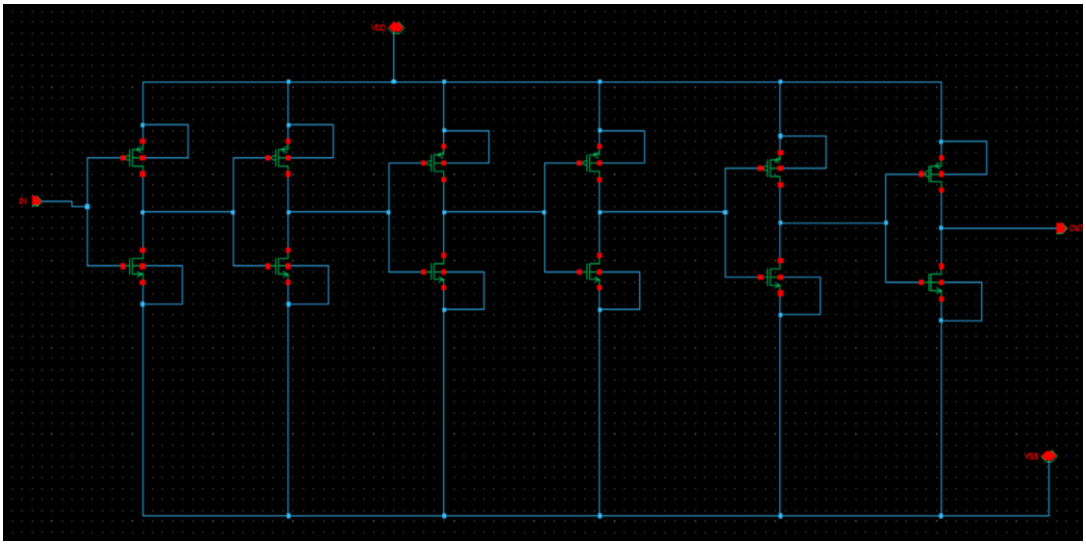
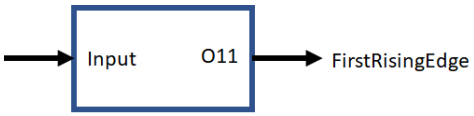
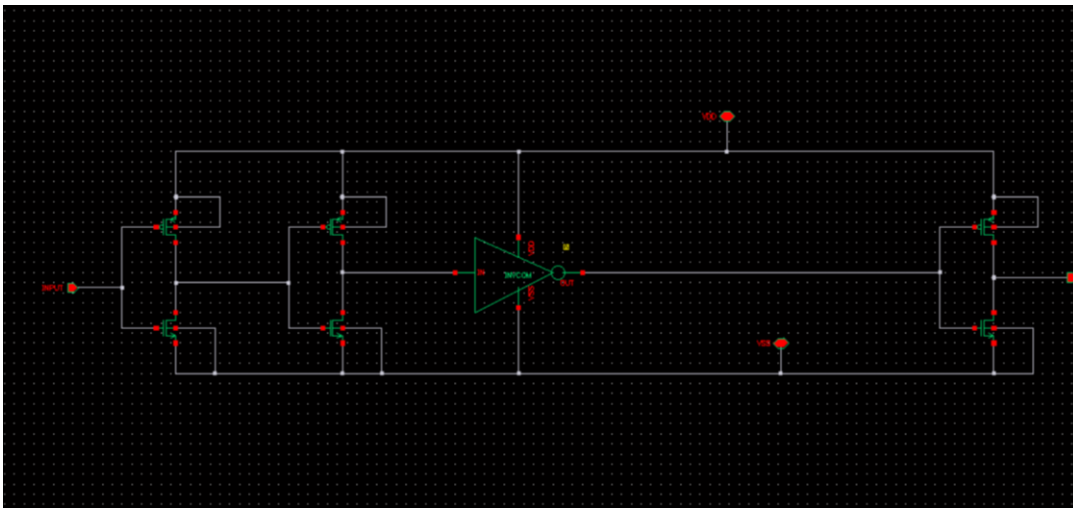


Fig. 51. Same Inverter chain



a)



b)

Fig. 52. a) First rising edge circuit input and output ports b) First rising edge schematic

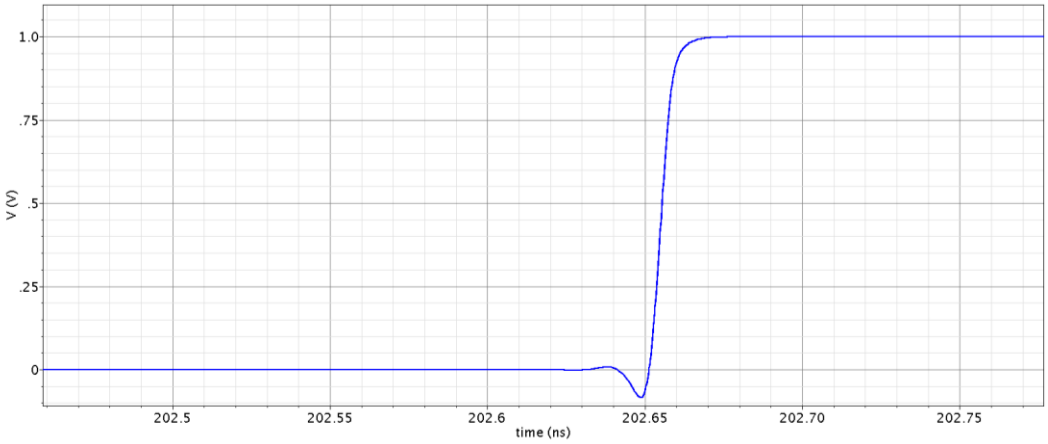


Fig. 53. a) First rising edge circuit output

in Fig. 51, which are placed in the middle of three separated inverters shown in

Fig. 52. The first rising edge circuit output and Layout are shown in Fig. 53 and 54, respectively.

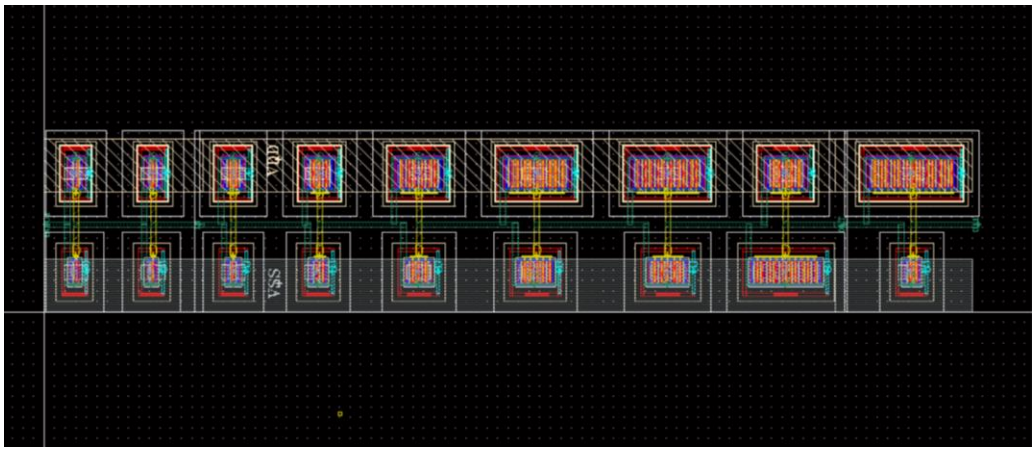
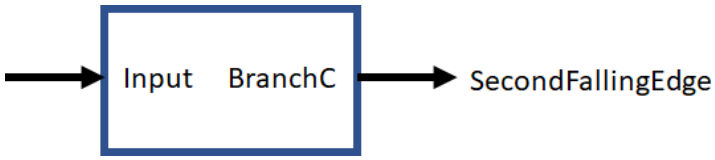
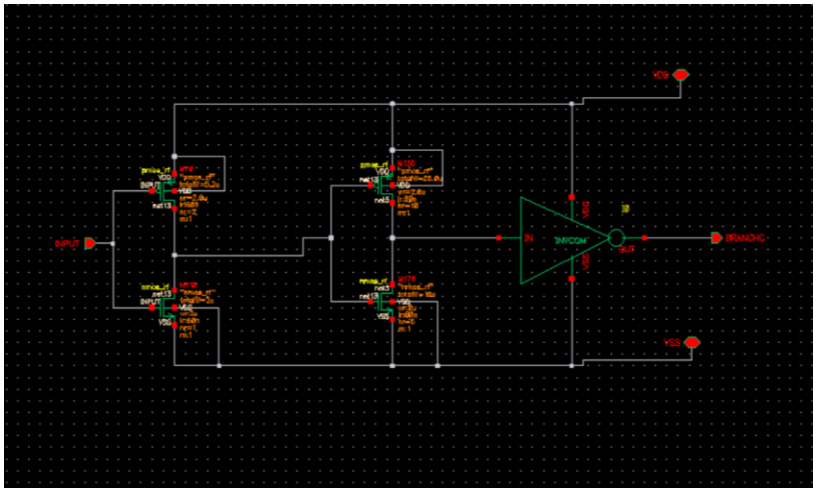


Fig. 54. a) First rising edge circuit Layout



a)



b)

Fig. 55. a) Second falling edge diagram b) Second falling edge diagram schematic

The second falling edge circuit includes the same six inverters as the first rising edge circuit, as well as two distinct inverters at its input. This circuit's Schematic, output, and Layout are depicted in Figs. 55, 56, and 57, respectively.

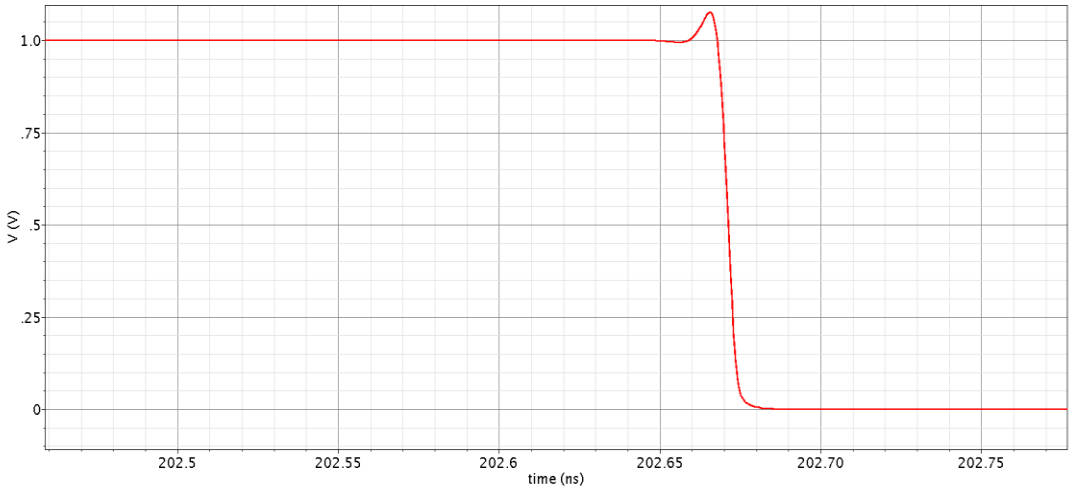


Fig. 56. Second falling edge output

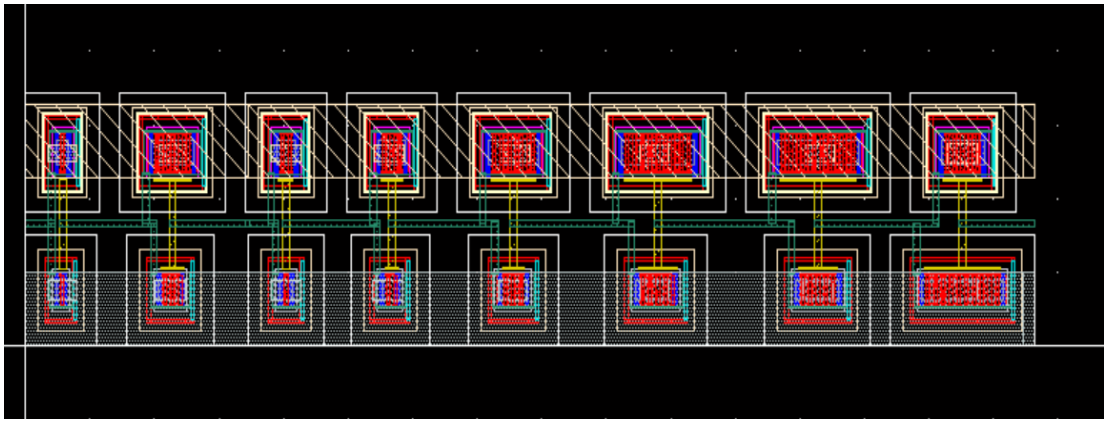
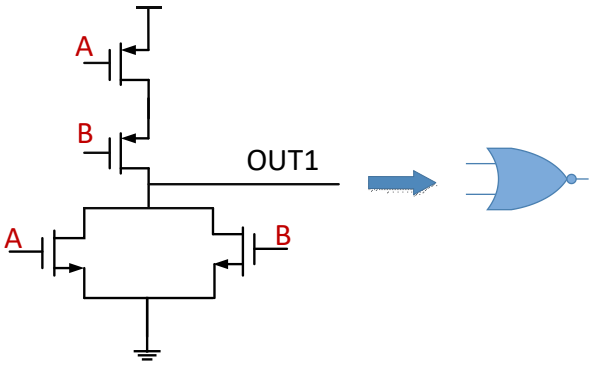


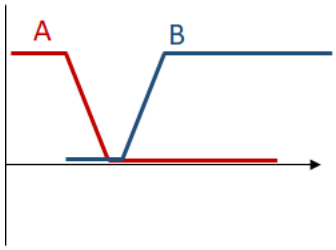
Fig. 57. Second falling edge Layout

5-2-2-6 Output stage

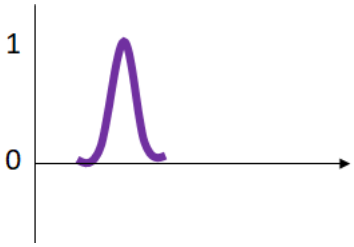
The output stage functions similarly to the NOR and NAND gates depicted in Figs. 58 and 59. When one of the NOR gate input signals (*A* or *B*) is a high voltage, one of the differential pair transistors turns on. In contrast, another turns



a)



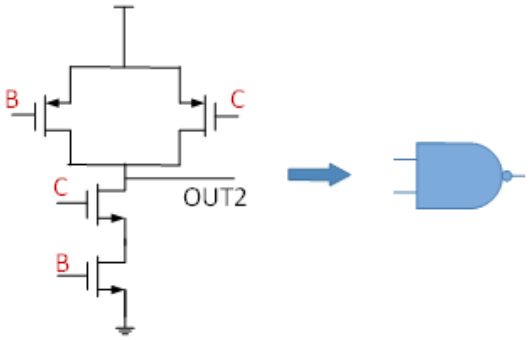
b)



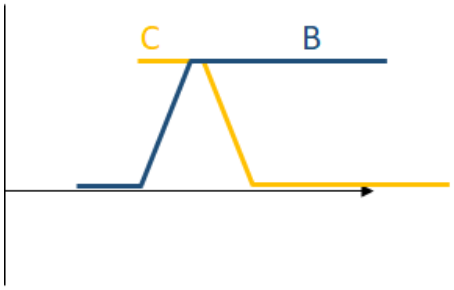
c)

Fig 58. a) The output up stage b) The output up stage inputs c) and output

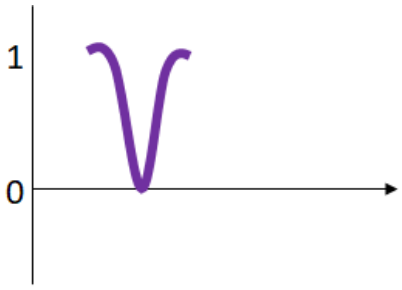
off, resulting in the output being connected to the ground and receiving the zero pulse. When both inputs are zero, the differential pair is disconnected, and the upside cascade circuit is activated, resulting in the output being abruptly connected to V_{CC}. The output circuit's down part functions similarly to a NAND



a)



b)



c)

Fig 59. a) The output downstage b) The output downstage inputs c) and output

gate. When one of the B or C inputs is zero, one of the differential pair's transistors is turned on, and the output is connected to V_{CC}. In addition, if both are zero, the output is connected to V_{CC}. However, when B and C are both high voltages, the differential pair is disconnected, and the cascade is activated. By quickly connecting the output to the ground, the cascade circuit creates the Gaussian pulse's downside. The desired Monopulse can be obtained by combining these upside and downside signals, as shown in Fig 60.

The Schematic, Layout, and output stage results are shown in Fig. 61 and 63, and 62. Two capacitors remove the DC voltage and deliver the pure monopulse to the antenna following the output stage. These two capacitors function

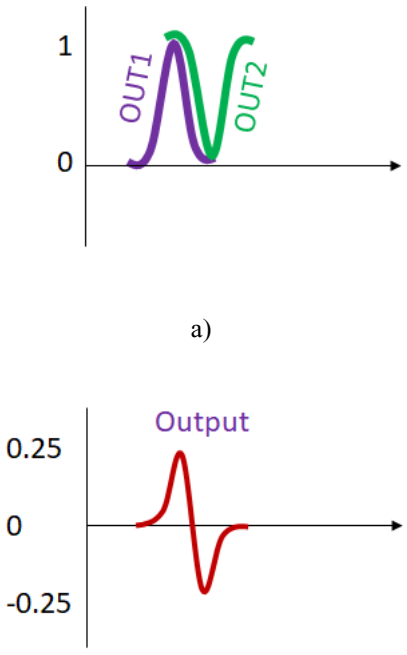
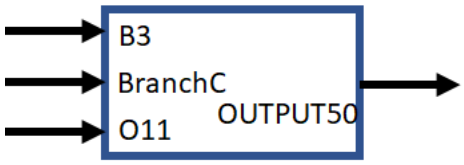
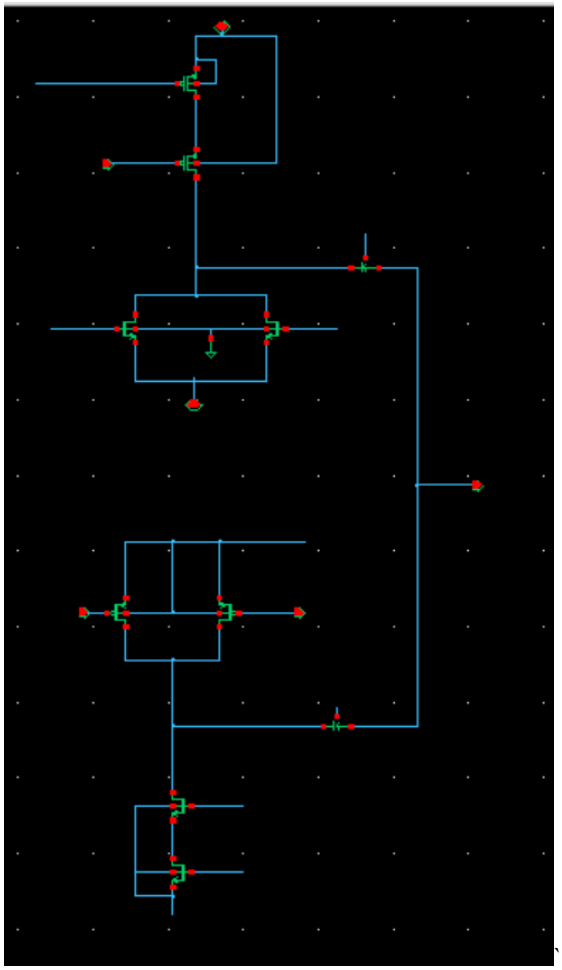


Fig. 60. a) each output of last stage b) final output



a)

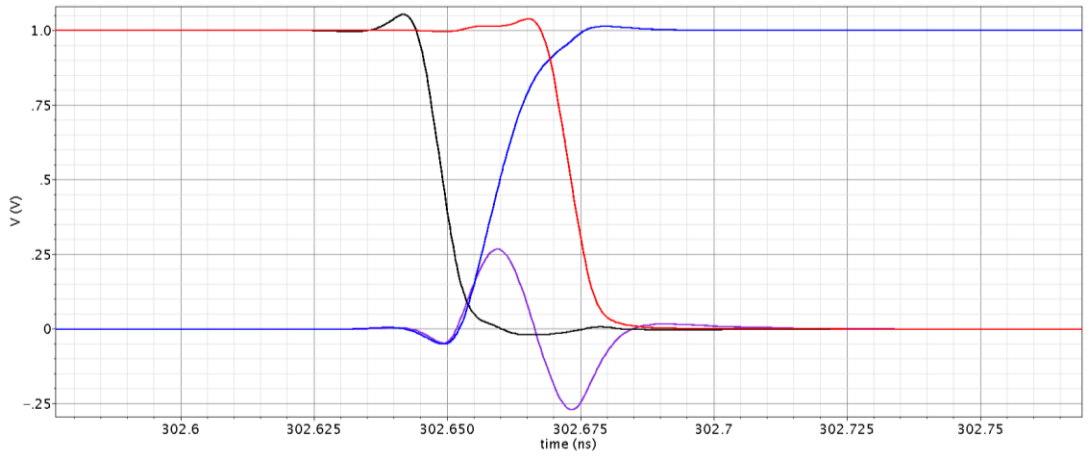


b)

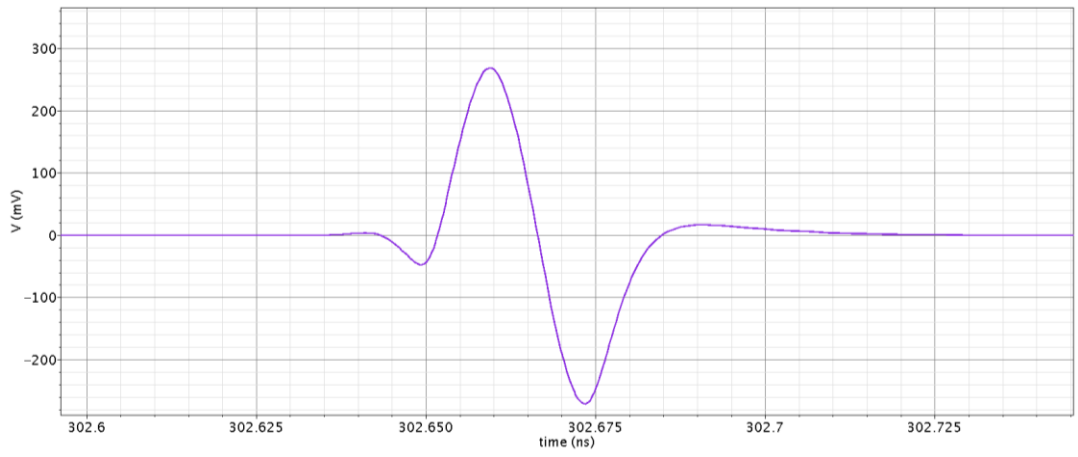
Fig. 61. A) Last stage ports b) and schematic

similarly to a simple matching circuit, lowering the deriving resistors to match 50 ohms and transmit more power to the antenna. Finally, after the fabrication

of IC by the TSMC company, the Monopulse signal will be connected to the antenna for sending to the target.



a)



b)

Fig. 62. A) each Last stage outputs b) and final output

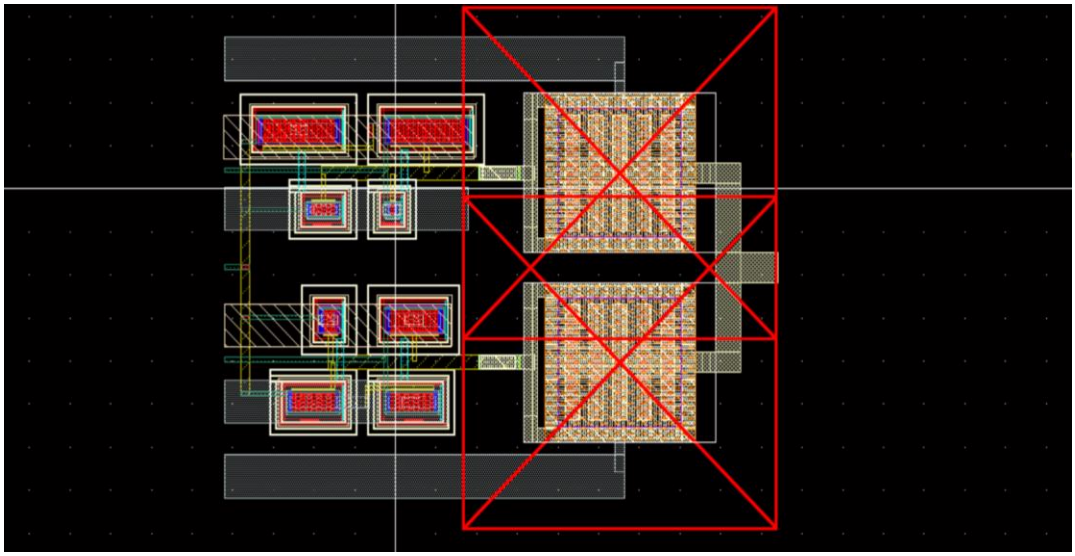


Fig. 63. Layout of the last stage

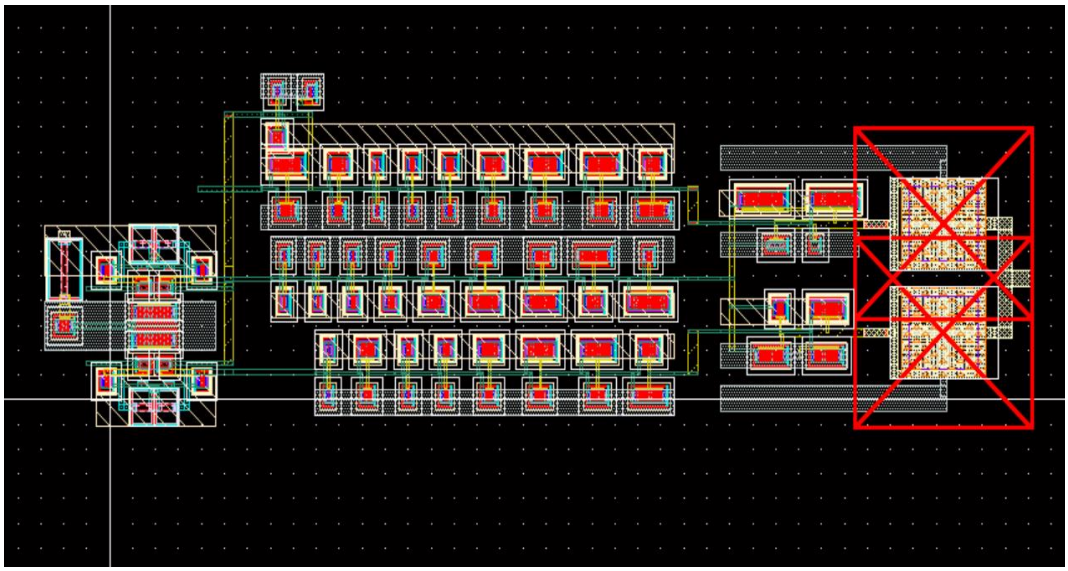


Fig. 64. Layout of the total circuit

5-2-3 Layout Results

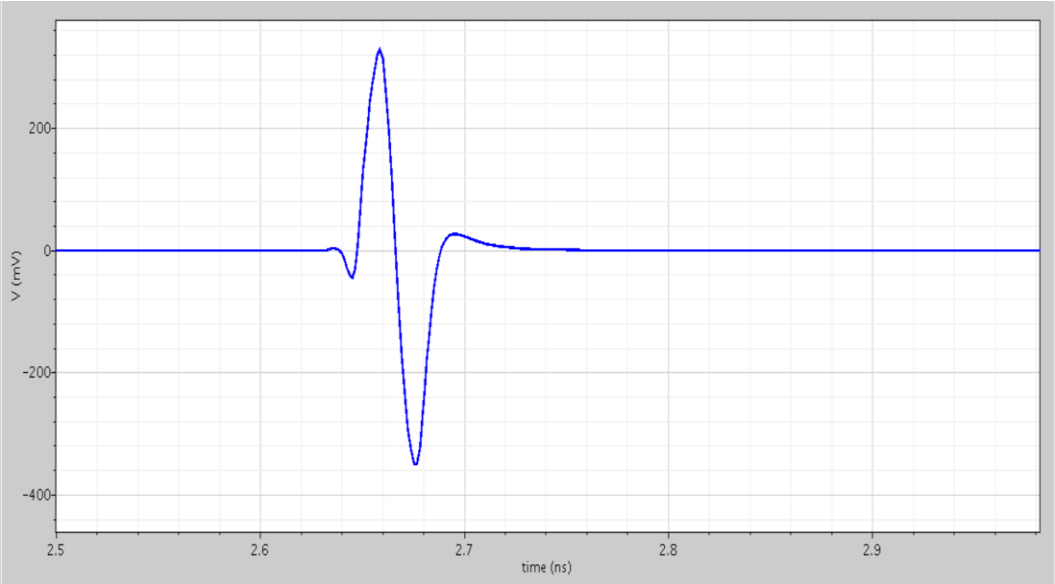


Fig. 65. the final Layout output

Each block has its own Layout, which must pass all Layout tests (DRC, LVS PEX) before connecting to other blocks. The final Layout connects all of the layout blocks depicted in Fig. 64. The final outcome is a 12.5 ps symmetric Monopulse with an amplitude of 345 mV shown in Fig. 65. After obtaining the Layout result, a Vivaldi antenna is modeled with ADS software and connected to the circuit to determine its effect. By connecting this antenna, the second derivate of Monopulse with a pulse width of around 12 ps is obtained, as shown in Fig. 66.

5-2-4 Post layout Results

After layout design, post-layout simulation must be performed to add all parasitic elements to the circuit and investigate circuit operation in an actual

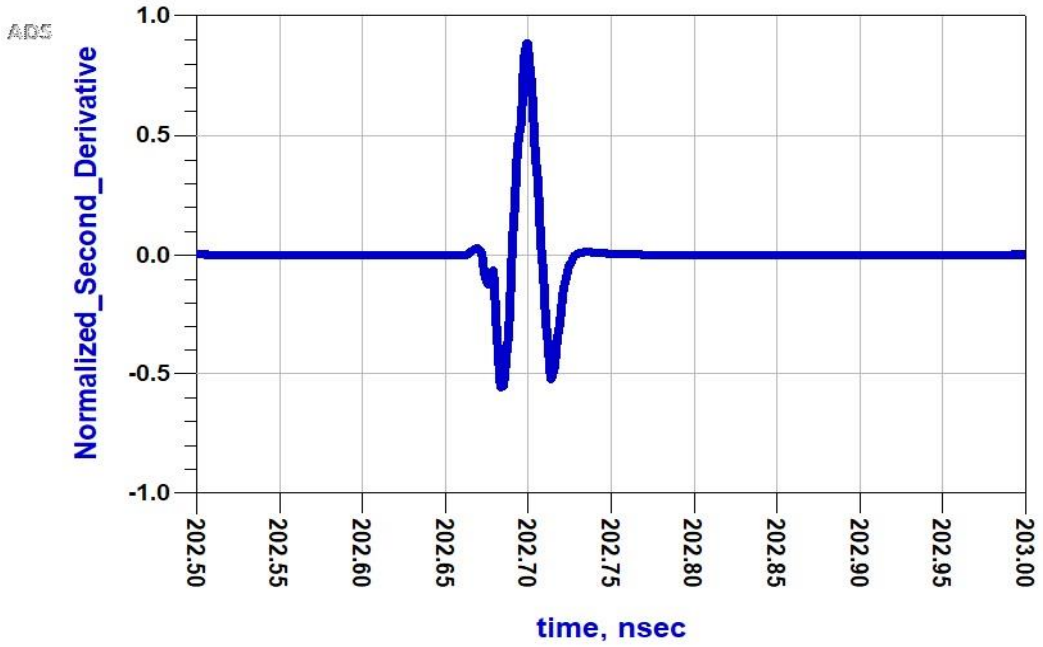


Fig. 66. Output of antenna

situation. Two post layouts are created: post layout one contains all parasitic capacitors and posts Layout two, including all parasitic capacitors and resistors. The first post layout output, which includes parasitic capacitors, is shown in Fig. 67; the output pulse width is 16 ps, and the amplitude is 308 mV. Note that the positive and negative pulse widths have roughly 1 to 2 ps difference for some simulations, so their average pulse width is mentioned in this design. Also, the typical voltage between 260 to 300 mV is reported for each case; however, it is possible to increase or decrease amplitude by using the tunable resistors, leading to worse or better pulse width, respectively. Finally, the IC will connect to the Pads to connect the antenna out of the IC. These Pads contain capacitors and resistors that can affect the output pulse characteristics. As a result, the Pads

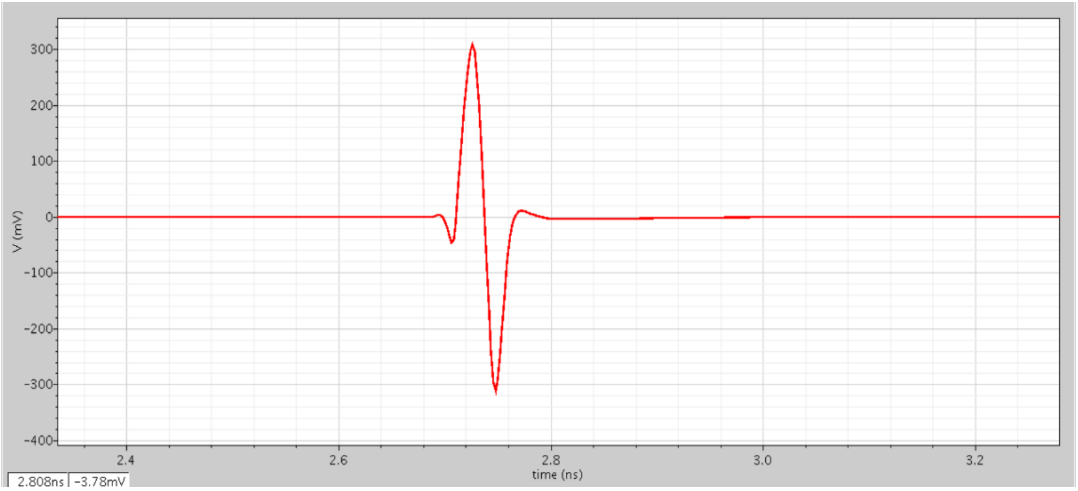


Fig. 67. Post layout one output

effects on the output of post layout one considered using the Pads model. Fig. 68 shows the output pulse with a pulse width of 16.5 ps and an amplitude of 257 mV when the pads effect is taken into account. It demonstrates that the pads reduce the amplitude by 50 mV.

Fig. 69 depicts the output of the second post layout, which incorporates all of the parasitic capacitors and resistors; the output pulse width is 17.5 ps, and the amplitude is 273 mV. These results show that the second post-layout simulation is more accurate than the first because it takes into account all parasitic resistor and capacitor effects, which increase the pulse width and decrease the amplitude of the final Monopulse. Pads are added to the second post-layout in the same way they were in the first to account for their effect. The output with pads effects is shown in Fig. 70, with a pulse width of 18.5 ps and an amplitude of 219 mV.

It demonstrates that the pads have the same effect on the output as was investigated in the first post layout.

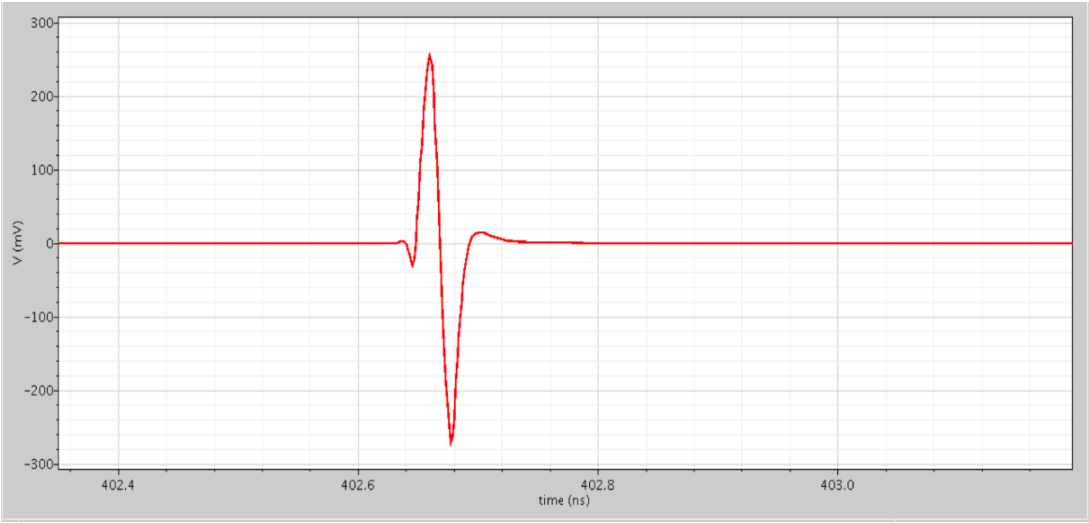


Fig. 68. Post layout one output with Pad effect

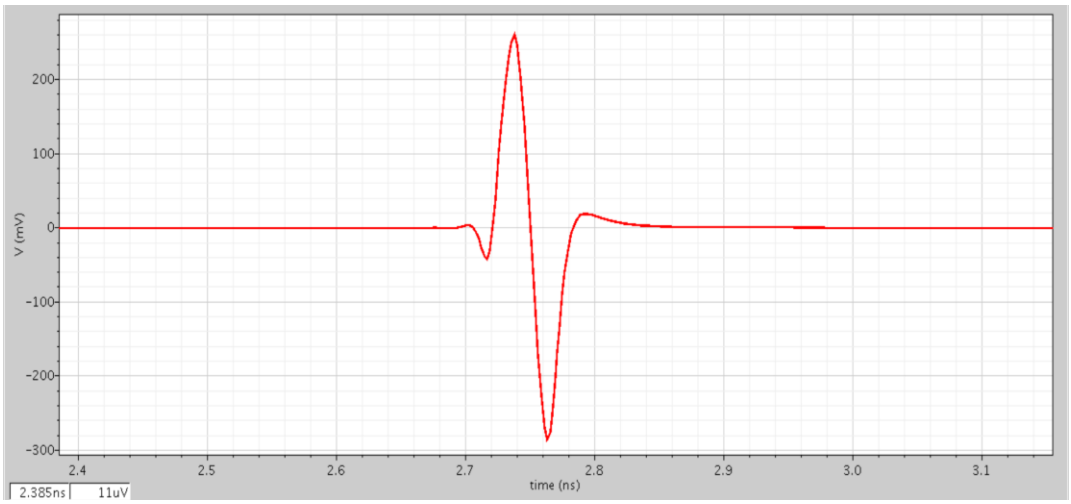


Fig. 69. Post layout two output without Pad effect

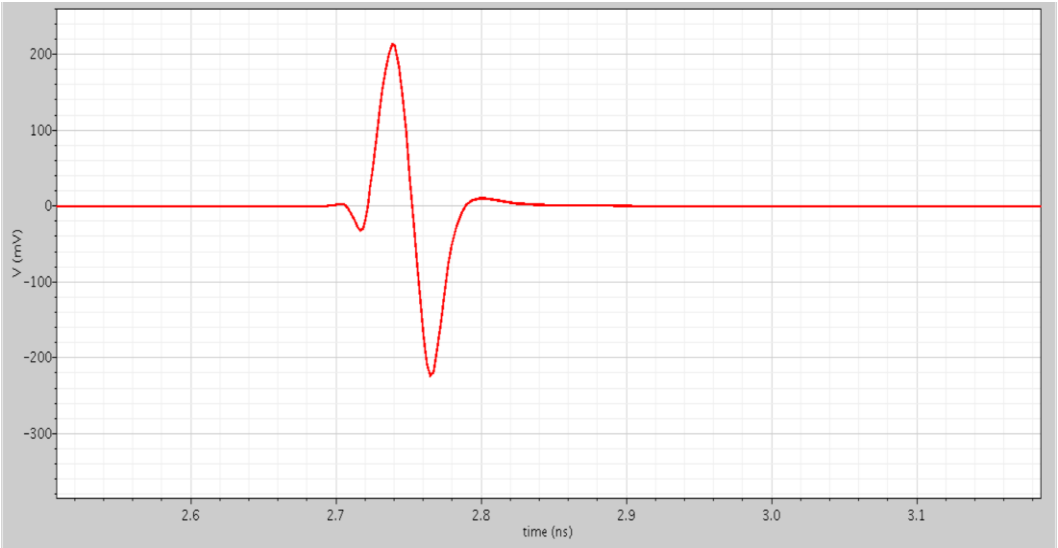


Fig. 70. Post layout two output with Pad effect

The desired Monopulse is obtained in all four post-layout simulations by adjusting the tunable resistors. Table 4 compares all of the post-layout results. Positive and negative pulse widths increased by only 1.5 ps in the second post layout, while amplitude decreased by 36 mV. Furthermore, it was discovered that PAD does not affect pulse width; it only reduces amplitude by 40 mV.

Table 4. comparison results of each post layout

	Amplitude	Pulse width
Post layout 1	308 mv	16 ps
Post layout 1 with pad	257 mv	16.5 ps
Post layout 2	273 mv	17.5 ps
Post layout 2 with pad	219 mv	18.5 ps

5-2-4-1 Post layout simulation of the worst-case scenario (in corners)

Some simulations depict the circuit's operation in the worst-case scenarios that could have occurred after manufacturing ICIn these simulations, the speed of each transistor is increased or decreased to create a situation in which each transistor does not work at its regular speed. These simulations were performed on the second post layout of our design, which contains all parasitic capacitors and parasitic resistors.

5-2-4-2 Changing Speed

The following four conditions are being investigated:

1- (Slow, Slow mode) : By changing the speed of NMOS and PMOS transistors and decreasing their speed, we obtain the Monopulse with 22 ps pulse width and 258 mV amplitude shown in Fig 71.

2- (Slow, Fast mode) : By decreasing the speed of NMOS and increasing PMOS transistors, we obtain the pulse with 16.5 ps pulse width and 250 mV amplitude shown in Fig 71.

3- (Fast, slow mode) : By increasing the speed of NMOS and decreasing PMOS, we obtain the 19.5 ps pulse width and 293 mV amplitude. The output is shown in Fig 71.

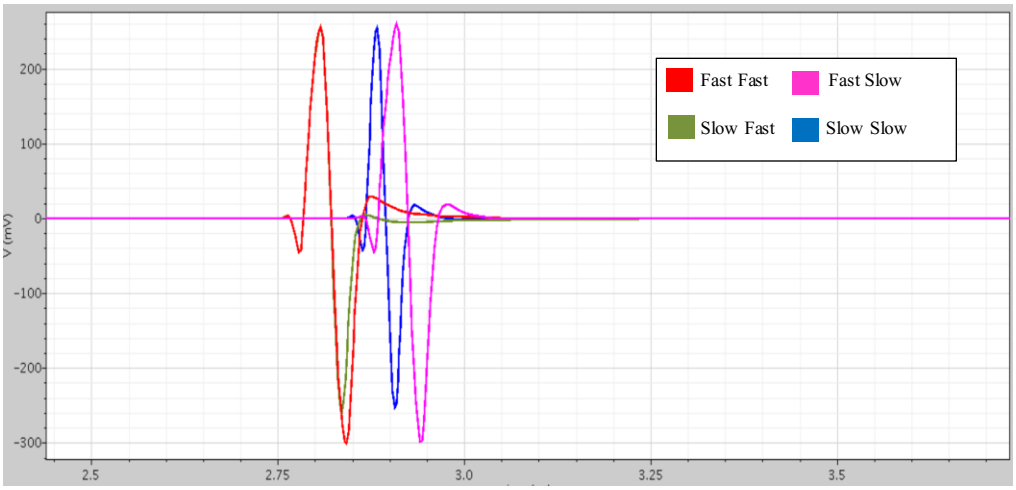


Fig. 71. Worst case situation outputs

4- (Fast, Fast mode) : By changing the speed of NMOS and PMOS and increase their speed, we obtain the 18.5 ps pulse width and 300 mV amplitude. The output is shown in Fig 71.

The adverse effects of the transistors' functionality in these four situations are absorbed into the tunability of the design. As a result, for all scenarios, the output Monopulse is redeemed by input tuning voltages. According to the graphs, these conditions only affect the pulse width and do not affect the output Monopulse shape. Furthermore, these results demonstrate that Slow Slow mode is the worst possible condition for our circuit. However, the desired pulse characteristics are achieved even in this mode.

5-2-4-3 Changing temperature

Temperature fluctuations are another worst situation that can happen to a circuit. In this design, temperature simulation is performed, and the circuit temperature ranges from 27 to 70 degrees Celsius. The result of this simulation is shown in Fig. 75, which shows the circuit will work at higher temperatures. The output Monopulse has a pulse width of 20 ps and an amplitude of 281 mV.

5-2-4-4 All worst cases together

A specific simulation is performed to ensure that this design works after fabrication, covering all of the worst conditions, including speed and temperature. To cover all of the worst conditions after fabrication, the temperature changes in the Slow mode condition, which is the worst situation

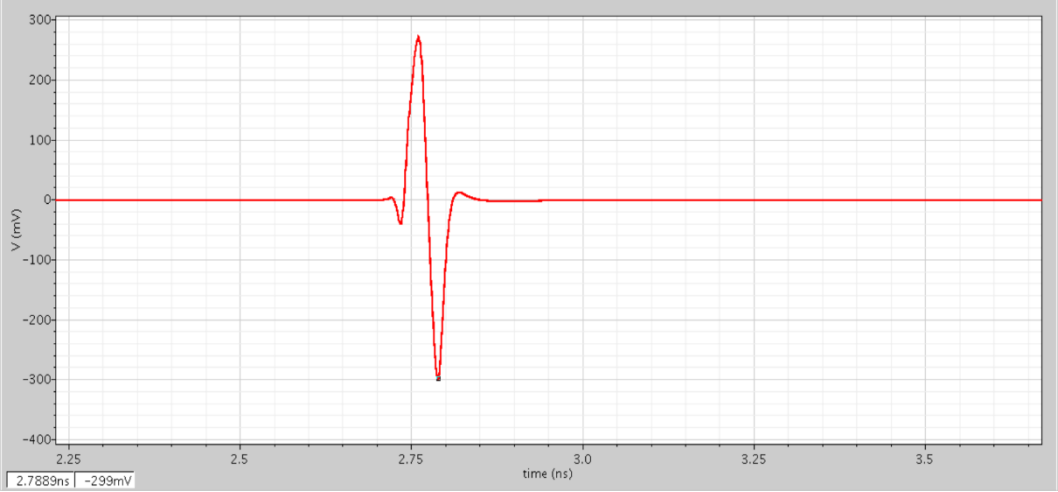


Fig. 72. Circuit output in 70-degree Celsius

we had before. Fig. 76 depicts the outcome of this situation. The worst-case simulation output includes pulse widths of 22 ps and amplitudes of 257 mV, proving that the IC will work in any scenario following fabrication.

All of the worst-case situations are compared in Table 5.

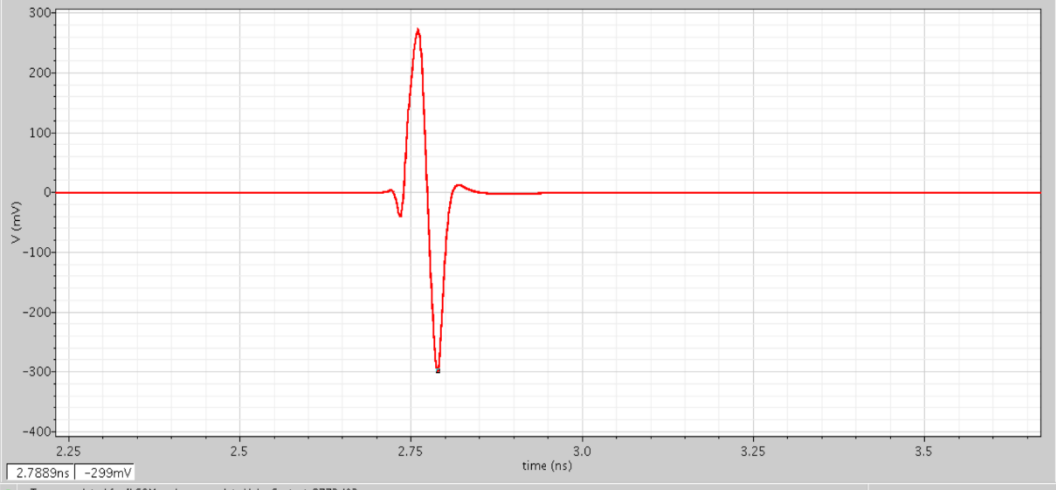


Fig. 73. Circuit output with all worse condition

Table 5. output comparison of each worse case

	Amplitude	Pulse width
SLOW-SLOW Mode	258 mv	22 ps
SLOW-FAST Mode	250 mv	16.5 ps
FAST-SLOW Mode	273 mv	19.5 ps
FAST-FAST Mode	300 mv	18.5 ps
70-degree temperature	281 mv	20 ps
All worst case	257 mv	22 ps

5-2-5 Comparison

This design is compared with some other published papers, which are listed in Table 6. The important properties of the output monopulse were compared, as well as their circuit properties. It should be noted that the pulse width is specified as the full width at half maximum (FWHM) of the output pulses. These designs incorporated a variety of technologies, resulting in a unique power supply for each of them. These circuits' ringing is expressed as a percentage of the ringing amplitude to the maximum signal amplitude.

Table 6. the comparison between integrated circuits

	Pulse width	Amplitude (Vpp)	Technology	Power Consumption	ringing
[17]	40 ps	115.2 mV	180 nm	0.2mW	75%
[32]	500 ps	673 mV	180 nm	1.38 mW	100%
[49]	150 ps	200mV	90 nm	0.1 mW	7%
[50]	20 ps	160 mV	45 nm SOI CMOS	0.04 mW	10%
This work	18 ps	438 mV	65nm	5.9mW	5%

6- Conclusion

Two methods for making a Gaussian pulse generator are presented by using discrete switches and integrated circuits. The first circuit generates a high-power Gaussian pulse with a three-stage Avalanche transistor, which improves detection range. This circuit is used for underwater imaging and detecting buried objects in a sandbox at a depth of 45cm. The second design, on the other hand generates a narrow pulse width Gaussian pulse with 65 nm technology that can be used in short-range but high-resolution applications. In this design, differential pair circuits, with the help of inverter chains, generates a Gaussian pulse. Compared to other studies, the first design has a higher figure of merit, and the second one has a very low pulse width and tunable ports, giving us the feature of the variable pulse width. Our results show that these circuits are suitable for UWB radar applications.

Resources

[1] Hyunseok Kim and Youngjoong Joo, "Fifth-derivative Gaussian pulse generator for UWB system," *2005 IEEE Radio Frequency integrated Circuits (RFIC) Symposium - Digest of Papers*, Long Beach, CA, USA, 2005, pp. 671-674, doi: 10.1109/RFIC.2005.1489903.

[2] J. Han and C. Nguyen, "Ultra-wideband electronically tunable pulse generators," IEEE Trans. Microw. Wireless Compon. Lett., vol. 14, pp. 112-114, 2004.

[3] L. Yang et al., "Ultra-Wideband communication-an idea whose time has come", *IEEE Signal Processing Magazine*, vol. 21, no. 6, pp. 26-54, Nov. 2004.

[4] R. Feghhi, D. Oloumi and K. Rambabu, "Design and Development of an Inexpensive Sub-Nanosecond Gaussian Pulse Transmitter," in IEEE Transactions on Microwave Theory and Techniques, vol. 67, no. 9, pp. 3773-3782, Sept. 2019.

[5] R. K. Dokania et al., "A 6μW, 100Kbps, 3–5GHz, UWB impulse radio transmitter," Proc. ACM/IEEE Int. Symp. Low-Power Electronics and Design (ISLPED), pp.91–94, 2010.

[6] Yeonghwan Ju, Youngseok Jin and Jonghun Lee, "Design and implementation of a 24 GHz FMCW radar system for automotive applications," 2014 International Radar Conference, 2014, pp. 1-4, doi: 10.1109/RADAR.2014.7060385.

[7] H. Zhou, C. Gao, X. Xu, F. Shen and Z. Guo, "A detection and tracking method based on monopulse radar in FSK mode applied in smart transportation systems," TENCON 2017 - 2017 IEEE Region 10 Conference, 2017, pp. 366-368, doi: 10.1109/TENCON.2017.8227891.

[8] J. Han and C. Nguyen, "A new ultra-wideband, ultra-short monocycle pulse generator with reduced ringing," IEEE Trans. Microw. Wireless Compon. Lett., vol. 12, pp. 206-208, 2002.

[9] Dongxiao Li and X. Yang, "Parameters analysis of Gaussian pulse circuit based on avalanche transistors," 2015 IEEE 6th International Symposium on Microwave, Antenna, Propagation, and EMC Technologies (MAPE), 2015, pp. 764-768, doi: 10.1109/MAPE.2015.7510428.

[10] D. Oloumi and E. Fear, "A Picosecond Pulse generator Using SRD diodes: Design, Analysis, and Measurements," *2018 USNC-URSI Radio Science Meeting (Joint with AP-S Symposium)*, 2018, pp. 159-160, doi: 10.1109/USNC-URSI.2018.8602738.

[11] O. Ramos Sparrow et al., "High rate UWB CMOS transceiver chipset for WBAN and biomedical applications, "Analog Integrated Circuits and Signal Processing, Volume 81, Issue 1, 2014.

[12] R. Vauche et al., "A 100 MHz PRF IR-UWB CMOS Transceiver With Pulse Shaping Capabilities and Peak Voltage Detector," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 6, pp. 1612-1625, June 2017.

[13] Weste, NH and Harris, D.M., 2011. Integrated circuit design. Boston: Pearson.

[14] P. P. Mercier, D. C. Daly, A. P. Chandrakasan, "An Energy-Efficient All-Digital UWB Transmitter Employing Dual Capacitively-Coupled Pulse-Shaping Drivers, "IEEE Journal of Solid-State Circuits, vol.44, no.6, pp.1679–1688, 2009.

[15] Z. Huang, Q. Fu, P. Chen, H. Yang, and X. Yang, "High power pulse generator based on avalanche transistor Marx circuit," in

Communication Problem-Solving, 2014 © IEEE Int. Conf., pp. 315-317.

[16] Sheng, H, Orlik, P., Haimovich, A.M., Cimini, L.J., Zhang, J.: `On the spectral and power requirements for ultra-wideband transmission', IEEE Int. Conf. on Communications, March 2003, Anchorage, AL, USA, 1, p. 738–742.

[17] S. H. Ignácio Barboza, J. A. Amaya Palacio, E. Pontes and S. T. Kofuji, "Fifth derivative Gaussian pulse generator for UWB Breast Cancer Detection System," *2014 IEEE International Conference on Ultra-WideBand (ICUWB)*, Paris, 2014, pp. 269-273, doi: 10.1109/ICUWB.2014.6958991.

[18] E. C. Fear, S. C. Hagness, P. M. Meaney, M. Okoniewski and M. A. Stuchly, "Enhancing Breast Tumor Detection with Near-Field Imaging," IEEE Microwave Magazine, vol. 3, pp. 48-56, March 2002

[19] W. Hung, C. Chang and T. Lee, "Real-Time and Noncontact Impulse Radio Radar System for μm Movement Accuracy and Vital-Sign Monitoring Applications," in *IEEE Sensors Journal*, vol. 17, no. 8, pp. 2349-2358, 15 April15, 2017.

[20] Z. Zhang, Y. Li, G. Wang, Y. Lian, "The Design of an EnergyEfficient IR-UWB Transmitter With Wide-Output Swing and SubMicrowatt Leakage Current, "IEEE Transactions on Circuits and Systems II: Express Briefs, vol.65, no.10, pp.1485–1489, 2018

[21] R. Feghhi, D. Oloumi and K. Rambabu, "Tunable Subnanosecond Gaussian Pulse Radar Transmitter: Theory and Analysis," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 9, pp. 3823-3833, Sept. 2020, doi: 10.1109/TMTT.2020.2983161.

[22] D. Oloumi, J.-W. Ting, and K. Rambabu, "Design of pulse characteristics for near-field UWB-SAR imaging," *IEEE Trans. Microw. Theory Techn.*, vol. 64, pp. 2684-2693, 2016.

[23] J. R. Andrews, "Picosecond pulse generation techniques and pulser capabilities," Applicat. Note AN-19, 2008.

[24] L. Li, A. E.-C. Tan, K. Jhamb, and K. Rambabu, "Buried object characterization using ultra-wideband ground penetrating radar," IEEE Trans. Microw. Theory Techn., vol. 60, no. 8, pp. 2654–2664, Aug. 2012

[25] J. Li, Z. Zeng, J. Sun and F. Liu, "Through-Wall Detection of Human Being's Movement by UWB Radar," in IEEE Geoscience and Remote Sensing Letters, vol. 9, no. 6, pp. 1079-1083, Nov. 2012, doi: 10.1109/LGRS.2012.2190707.

[26] K. Rambabu, AEC. Tan, K.K.M. Chan and MYW. Chia, "Estimation of Antenna effect on UWB pulse shape in transmission and reception," IEEE Trans. on Electromagnetic Compatibility, Vol.51, No. 3, Aug. 2009, pp. 604-610.

[27] AEC. Tan, M.Y.W. Chia, K.K.M. Chan, and K. Rambabu, "Modeling the transient radiated and received pulses of ultra-wideband antennas", IEEE Trans. Antennas Propag., Vol.61, No.1, Jan. 2013, pp. 338-345.

[28] Pozar, D.M., 2011. Microwave engineering. John wiley & sons.

[29] C.-W. Hsue, L.-C. Tsai, and K.-L. Chen, "Implementation of first-order and second-order microwave differentiators," IEEE Trans. Microw. Theory Techn., vol. 52, pp. 1443-1448, 2004.

[30] M. Chudzik, I. Arnedo, A. Lujambio, I. Arregui, I. Gardeta, F. Teberio, et al., "Design of Transmission-Type Nth-Order Differentiators in Planar Microwave Technology," IEEE Trans. Microw. Theory Techn., vol. 60, pp. 3384-3394, 2012.

[31] S. Fan et al., "A Cross-Coupled Active Rectifier-Booster Regulator Integrated Circuit for Broadband Wireless Energy Harvesting System," 2020 IEEE MTT-S International Wireless Symposium (IWS), 2020, pp. 1-3, doi: 10.1109/IWS49314.2020.9359959.

[32] S. Sim, D. Kim and S. Hong, "A CMOS UWB Pulse Generator for 6–10 GHz Applications," in *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 2, pp. 83-85, Feb. 2009, doi: 10.1109/LMWC.2008.2011318.

[33] Kim, H.; Park, D.; Joo, Y.: 'All-digital low-power CMOS pulse generator for UWB system', Electronics Letters, 2004, 40, (24), p. 1534-1535, DOI: 10.1049/el:20046923 IET Digital Library

[34] L. C. Moreira, J. F. Neto, T. Ferauche, G. A. Silva Novaes and E. T. Rios, "All-digital reconfigurable IR-UWB pulse generator using BPSK modulation in 130nm RF-CMOS process," *2017 IEEE 8th Latin American Symposium on Circuits & Systems (LASCAS)*, Bariloche, 2017, pp. 1-4, doi: 10.1109/LASCAS.2017.7948096

[35] P. Chen and A. Babakhani, "A 30GHz impulse radiator with on-chip antennas for high-resolution 3D imaging," 2015 IEEE Radio and Wireless Symposium (RWS), San Diego, CA, 2015, pp. 32-34, doi: 10.1109/RWS.2015.7129717.

[36] J. Tan, Z. Zhong, Y. Liu, D. Zeng and J. Tan, "Research on high-repetition high-voltage nanosecond rectangular pulse generator based on avalanche transistor," 2015 7th Asia-Pacific Conference on Environmental Electromagnetics (CEEM), 2015, pp. 73-76, doi: 10.1109/CEEM.2015.7368632

[37] N. Beev, J. Keller, and T. E. Mehlstäubler, "Note: An avalanche transistor-based nanosecond pulse generator with 25 MHz repetition rate," Review of Scientific Instruments, vol. 88, p. 126105, 2017.

[38] Ozdemir, Caner & Demirci, Şevket & Yigit, Enes & Yılmaz, Baran. (2014). A Review on Migration Methods in B-Scan Ground Penetrating Radar Imaging. Mathematical Problems in Engineering. 2014. 1-16. 10.1155/2014/280738.

[39] Inokuchi, M. et al. "Development of Miniature Marx Generator using BJT." 2009 IEEE Pulsed Power Conference (2009): 57-60.

[40] T. Heeren, T. Ueno, Douyan Wang, T. Namihira, S. Katsuki and H. Akiyama, "Novel dual Marx Generator for microplasma applications," in IEEE Transactions on Plasma Science, vol. 33, no. 4, pp. 1205-1209, Aug. 2005, doi: 10.1109/TPS.2005.852433.

[41] J. Yan, S. Shen and W. Ding, "High-Power Nanosecond Pulse Generators With Improved Reliability by Adopting Auxiliary Triggering Topology," in IEEE Transactions on Power Electronics, vol. 35, no. 2, pp. 1353-1364, Feb. 2020, doi: 10.1109/TPEL.2019.2922360.

[42] Yan J, Shen S, Wang Y, Zhang S, Cheng L, Ding W (2018) A novel trigger for pseudospark switch with high repetition rate, low jitter, and compact structure. Rev Sci Instrum 89:065102

[43] P. Krishnaswamy, A. Kuthi, P. T. Vernier and M. A. Gundersen, "Compact Subnanosecond Pulse Generator Using Avalanche Transistors for Cell Electroperturbation Studies," in IEEE Transactions on Dielectrics and Electrical Insulation, vol. 14, no. 4, pp. 873-877, Aug. 2007, doi: 10.1109/TDEI.2007.4286518.

[44] Horowitz, P., Hill, W. and Robinson, I., 1989. The art of electronics (Vol. 2, p. 658). Cambridge: Cambridge university press.

[45] Basu, Joydeep (9 October 2019). "From Design to Tape-out in SCL 180 nm CMOS Integrated Circuit Fabrication Technology". IETE Journal of Education. 60 (2): 51–64. arXiv:1908.10674

[46] 1998. Kim, Yong-Bin; Chen, Tom W. (15 May 1996). Assessing Merged DRAM/Logic Technology. 1996 IEEE International Symposium on Circuits and Systems. Circuits and Systems Connecting the World. Atlanta, USA. pp. 133–36. doi:10.1109/ISCAS.1996.541917.

[47] Weste NH, Harris D. CMOS VLSI design: a circuits and systems perspective. Pearson Education India; 2015.

[48] R. H. Stern, "MicroLaw," in *IEEE Micro*, vol. 5, no. 4, pp. 90-92, Aug. 1985, doi: 10.1109/MM.1985.304489.

[49] Bo Qin, X. Wang, A. Wang, Hongyi Chen and Bin Zhao, "A programmable 1.8pJ/pulse Gaussian pulse generator for impulse UWB transceiver in 90nm CMOS," 2009 IEEE Radio and Wireless Symposium, 2009, pp. 498-501, doi: 10.1109/RWS.2009.4957397.

[50] X. An, J. Wagner and F. Ellinger, "A 7th Derivative Gaussian Pulse Generator for IR-UWB Radar Applications in Pedestrian Detection," *2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2018, pp. 317-320, doi: 10.1109/ICECS.2018.8617898.