Real-Time System-on-Chip Emulation of Electrothermal Models for Power Electronic Devices via Hammerstein Configuration

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***Abstract*— Real-time emulation of device-level power electronics plays an essential role in many industrial applications for design and hardware-in-the-loop testing of system components and controllers. Due to the complexity and heavy computational burden of the real-time hardware implementation of the analytical and the numerical models, this paper proposes dynamic electrothermal behavioral models for diode, thyristor, and insulated-gate bipolar transistor based on the Hammerstein configuration. The power electronic device model parameters are extracted from the known device datasheets and implemented in Zynq System-on-Chip platform with accelerated processing for real-time application. An electromagnetic rail gun system has been employed as the study case to compare the performance of the proposed electrothermal behavioral models with that of off-line simulation models on SaberRD software.**

***Index Terms*— Behavioral model, diode, electrothermal, Hammerstein configuration, hardware-in-the-loop (HIL), insulated-gate bipolar transistor (IGBT), real-time systems, sliding mode control (SMC), system-on-chip (SoC), thyristor.**

NOMENCLATURE

CC	Charging circuit.
EMRG	Electromagnetic rail gun.
PFN	Pulse forming network.
PFU	Pulse forming unit.
PL	Programmable logic.
PS	Processing system.
SoC	System-on-chip.
HIL	Hardware-in-the-loop.
TSSM	Two-state switch model.
HCM	Hammerstein configuration model.
TLM	Transmission line modeling.

I. INTRODUCTION

REAL-TIME HIL technology plays a pivotal role in the design and development of power electronic system for many applications. There is a need for accurate device-level modeling in real-time HIL simulation, especially under the extreme and extensive range conditions. With the help of HIL technology, the newly designed power switch, protection circuit and algorithm, power converter and controller can be repeatedly evaluated for design optimizing and tuning in a nondestructive emulation environment [1], [2]. Field programmable gate arrays (FPGAs) are gaining preferred status in real-time modeling of various power apparatus and systems [3]–[12]. Rapid evolution of integrated circuit technology has led to the availability of commercial SoC platform with a large capacity of computational resources such as ARM-based multicore processors and FPGA on the same device, enabling the real-time implementation for complex industrial application [13]–[19].

Recently, various system-level and device-level power electronic models have been utilized in modeling and simulation of power converters and network behavior [20]. The performance of the models has been a vital issue for selecting the appropriate model for a specific application. The system-level power electronic model can be mainly categorized into three types: 1) ideal model [22]; 2) switching function model [23]; and 3) averaged model [24]. The ideal model employs ON- and OFF-state resistances for simulation. The switching function model describes the behavior of the converter by controlled voltage and current sources. The averaged model considers the average behavior of the system while ignoring the switching behavior. In general, the averaged model consumes less compute power than the rest with less accuracy, whereas the ideal model costs the most compute power with higher precision.

In this paper, the following device-level power electronic models have been utilized in circuit simulation: 1) analytical model [25]–[30]; 2) behavioral model [31]–[37]; 3) numerical model [38], [39]; and 4) hybrid model [40]. The analytical model that could accurately describe the device steady state and transient operation is based on device physics. The behavioral model provides a good prediction of the device performance, while ignoring the detailed physical characteristics. The numerical model can simulate the device's electrical, thermal, and optical characteristics by using the finite element method without fabricating the physical device; however, it is prohibitively time consuming. The hybrid model combines the accelerated physics-based calculation of the analytical model, low-computational consumption of the behavioral model, and the accurate geometrical properties of the numerical model. In general, behavioral models are the fastest and require

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least computation resources, while the rest of the models are expected to be both resource and execution time intensive.

Behavioral models can utilize the device datasheet to achieve a comprehensive device-level simulation. However, the analytical, numerical, and hybrid models require specific dimensions and fabrication description to extract the dedicated physical parameters. In general, the device datasheet does not provide such detailed manufacturer design specifications, which makes modeling of the general device arduous. Some physical parameters inside the power semiconductor are not able to be measured or estimated unless there is an extensive cooperation with the semiconductor manufacturer. High-order nonlinear equations, convergence problems, sensitivity to initial conditions, which may result in incomplete or inaccurate simulation, are also some of the main challenges in these models.

The choice of the modeling approach depends on the required accuracy, compute resource, convergence properties, validity range, and time consumption of the application. The analytical, numerical, and hybrid models consume a significant amount of compute resource, thereby making them inappropriate for the real-time simulation at least in the near future. Though the system-level model is simplified enough to achieve real-time execution, it cannot represent the detailed switching transient of the power electronic device. It should be noted that accuracy of the model is highly related to the modeling complexity. Therefore, it is reasonable to choose a device-level power electronic behavioral model for the real-time hardware emulation with acceptable accuracy and low-compute resource consumption.

The Hammerstein and the Wiener models are two of the common behavioral models, which separate the static and dynamic characteristics of general physical systems. The Hammerstein model consists of a nonlinear static block in the front of a linear time-invariant dynamic block, while the Wiener model consists of a linear time-invariant dynamic block followed by a nonlinear static block. From the perspective of power electronic device model identification, the Hammerstein model is more user-friendly than the Wiener model since dynamic changes happen after applied conditions. The earliest literature of the Hammerstein model can be dated back to 1966 [41]. With generations of development in nonlinear system identification theory, the Hammerstein-based models have been applied in a variety of areas, such as model identification [42], [43], biomedical engineering [44], hysteresis phenomena [45], [46], power electronics [47]–[49], electrical drives [50], neural networks [51], [52], communication systems [53], [54], and mechanical engineering [55]. Applying the Hammerstein configuration technique for behavioral modeling can indeed reduce the complexity of hardware implementation of power electronic device models. The modeling of insulated-gate bipolar transistor (IGBT) by Hammerstein configuration was illustrated in [31] with detailed circuit experiments, however, no dynamic electrothermal physical behavior could be predicted by the model and the highly nonlinear model equations may require iterative computation. Though the nonlinear part of the Hammerstein model can be optimized by introducing the Taylor Series technique, the requirement of iteration process is still cumbersome due to the nonlinear nature of model. If the nonlinear part of the Hammerstein model can be separated into linear parts in the equation or equivalent linear electrical element, computation burden can be significantly reduced by either circumventing iterations entirely or using only a few iteration in real-time implementation.

TABLE I
UTILIZATION OF DATASHEET PLOTS IN THE MODELING PROCEDURE FOR VARIOUS DEVICE

Device	Static electrical model	Dynamic electrical model	Transient power loss model	Thermal network calculation
Diode	I_F-V_F	Q_{rr}- I_F, I_{rr}- I_F, Q_{rr}- di/dt, I_{rr}- di/dt	E_{rec}- I_F, E_{rec}- di/dt	Z^{Diode}_{thjc}-t
Thyristor	I_T-V_T	Q_{rr}-di/dt, I_{rr}-di/dt	W_{on}- I_{TRM}, W_{off}- V_0	Z^{Thy}_{thjc}-t
IGBT	I_C-V_{CE}	$t_{d,on}$- I_C, t_r- I_C, $t_{d,off}$- I_C, t_f- I_C, $t_{d,on}$- R_G, t_r- R_G, $t_{d,off}$- R_G, t_f- R_G	E^{IGBT}_{on}-I_C, E^{IGBT}_{off}-I_C, E^{IGBT}_{on}-R_G, E^{IGBT}_{off}-R_G,	Z^{IGBT}_{thjc}-t

This paper proposes dynamic electrothermal nonlinear behavioral models for the diode, thyristor, and IGBT using the Hammerstein configuration with the equivalent electrical component representation for real-time emulation of device-level behavior. The parameters of the Hammerstein models are extracted from the dedicated device datasheet. The performance of the proposed models is tested and validated in the EMRG system. This paper is organized as follows. Section II describes the construction of the Hammerstein configurations for diode, thyristor, and IGBT. Section III gives a brief introduction to the Zynq SoC platform and explains the details of the case study implementation. Section IV shows the real-time emulation results and verification using SaberRD software, which provides device-level experimentally verified static and dynamic performance features. Section V gives the conclusion of this paper.

II. CONSTRUCTION OF DEVICE-LEVEL DYNAMIC ELECTROTHERMAL MODEL VIA HAMMERSTEIN CONFIGURATION

This section introduces the detailed behavioral modeling method via the Hammerstein configuration. Section II-A describes the difference between the Hammerstein model and the Hammerstein configuration. In Section II-B–II-E, the static electrical model, the dynamic electrical model, the transient power loss model, and the thermal network will be discussed individually for the devices. Table I shows the necessary plots from the datasheet [64], [65] for the power device behavioral modeling via the Hammerstein configuration. The information requirements for each device are classified into four modeling procedures.

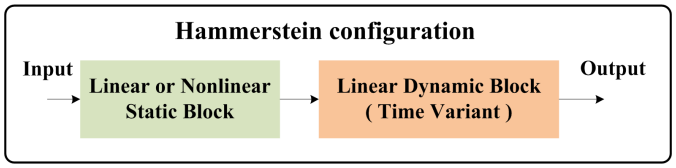

Fig. 1. Block diagram of the Hammerstein configuration.

A. Hammerstein Model Versus Hammerstein Configuration

The Hammerstein model consists of a nonlinear static block followed by a linear time-invariant (LTI) block, while the Hammerstein configuration encapsulates the idea of separating the static block from the dynamic block. The static block in the configuration can be a linear or nonlinear block. The dynamic block in the configuration is a linear time-variant (LTV) system. The block diagram of Hammerstein configuration is shown in Fig. 1.

Iterative solution becomes necessary when the Hammerstein model is applied for system simulation due to the nonlinear static block inside the model. Hammerstein configuration provides a way to simplify the nonlinear static blocks into linear static blocks in order to reduce the calculation burden. For the dynamic block, the configuration could utilize a LTV system instead of the LTI one if the time-varying parameters have a small impact on the system simulation results.

B. Device Static Electrical Model

The static characteristics of the power electronic devices (diode, thyristor, and IGBT) are similar (shown in Fig. 2) and are made up of a temperature-dependent conductance $g_{\rm ON}(T_{\rm vj})$ with a paralleled temperature-dependent voltage controlled current source (VCCS) $i_{\rm ON}(T_{\rm vj})$. The VCCS is a Thévenin equivalent expression of the $v_{\rm ON}(T_{\rm vj})$. During the ON-state, the model shows high conductance with a paralleled VCCS, while under OFF-state the model exhibits low conductance with the paralleled zero-value VCCS. The linear interpolation method has been utilized to estimate $g_{\rm ON}(T_{\rm vj})$ and $v_{\rm ON}(T_{\rm vj})$ at the operating temperatures between T_{125° and T_{25°, given as

$$g_{\rm ON}(T_{\rm vj}) = \frac{T_{\rm vj} - T_{25^\circ}}{T_{25^\circ} - T_{125^\circ}}\left(g_{\rm ON}^{T_{25^\circ}} - g_{\rm ON}^{T_{125^\circ}}\right) + g_{\rm ON}^{T_{25^\circ}} \quad (1)$$

$$v_{\rm ON}(T_{\rm vj}) = \frac{T_{\rm vj} - T_{25^\circ}}{T_{25^\circ} - T_{125^\circ}}\left(v_{\rm ON}^{T_{25^\circ}} - v_{\rm ON}^{T_{125^\circ}}\right) + v_{\rm ON}^{T_{25^\circ}} \quad (2)$$

$$i_{\rm ON}(T_{\rm vj}) = v_{\rm ON}(T_{\rm vj}) \cdot g_{\rm ON}(T_{\rm vj}). \quad (3)$$

C. Device Dynamic Electrical Model

The dynamic characteristic of power electronic devices varies from device to device due to the differences in physical structure and the manufacturing process. The device models of dynamic behavior will be introduced separately in this section. The dynamic characteristic curves for the three devices are shown in Fig. 3.

These dynamic characteristics can be described as a transient phenomena of an RC circuit which is a first-order delay circuit. The input and output of the dynamic part in Hammerstein configuration (shown in Fig. 4) are either the values of VCCSs or the conductances, which depend on the selected device and conditions. The first-order delay circuit can be represented in discrete time by applying the bilinear transformation as follows:

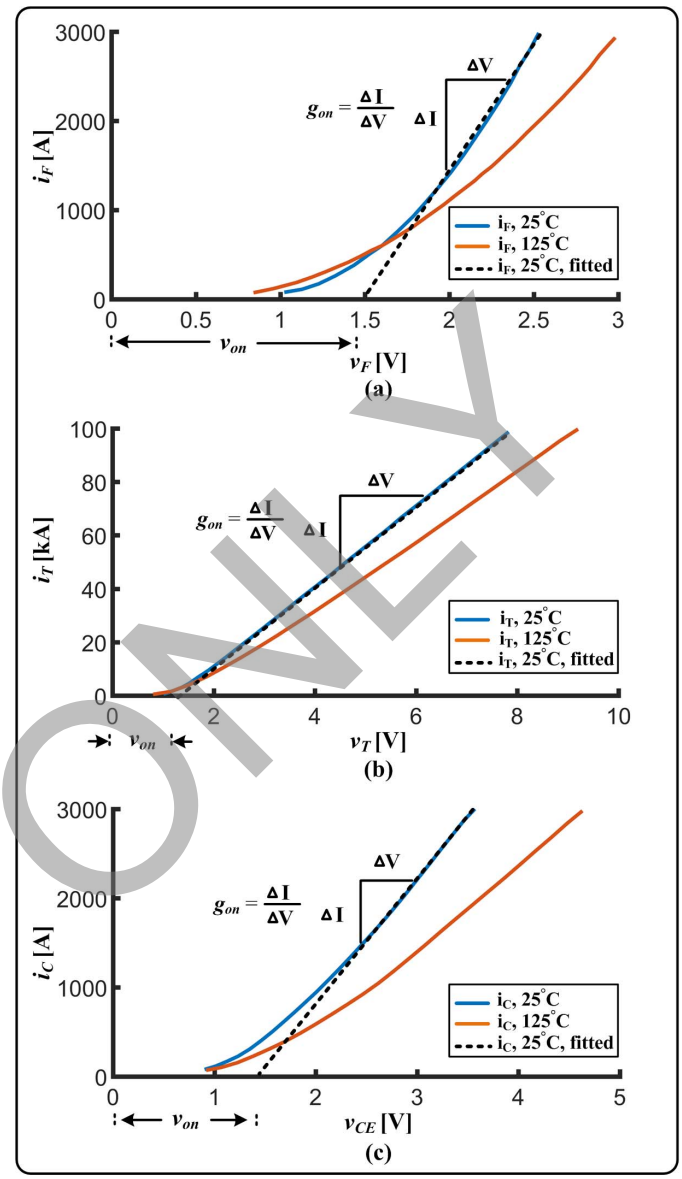

Fig. 2. Static characteristics. (a) Diode. (b) Thyristor. (c) IGBT.

$$\frac{U_o}{U_i} = \frac{\frac{1}{CS}}{R + \frac{1}{CS}} = \frac{1}{RCS + 1} \quad (4)$$

$$S = \frac{2}{\Delta t_{\rm elect}} \cdot \frac{1 - z^{-1}}{1 + z^{-1}} \quad (5)$$

$$\tau = R \cdot C \quad (6)$$

$$\frac{U_o}{U_i} = \frac{\Delta t_{\rm elect} + \Delta t_{\rm elect} z^{-1}}{\Delta t_{\rm elect} + 2\tau + (\Delta t_{\rm elect} - 2\tau) z^{-1}} \quad (7)$$

where $\Delta t_{\rm elect}$ is the electrical circuit simulation time step; R and C are the first-order delay circuit parameters; and τ is the time constant. The real values of R and C are not critical to the simulation. The product of R and C influences on the dynamic calculation significantly. Table II shows the time-based transient value of the first-order delay circuit.

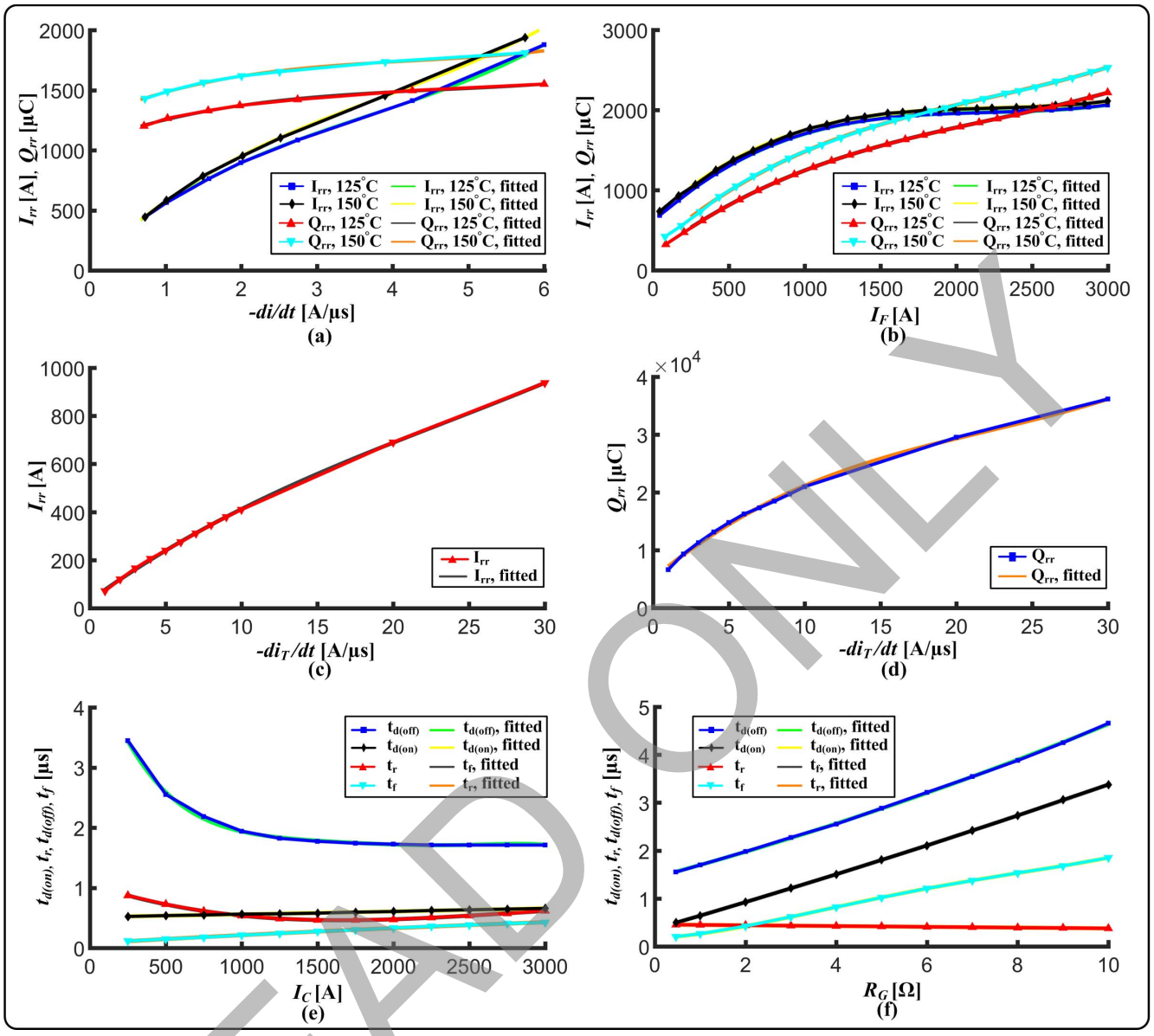

Fig. 3. Dynamic characteristics. (a) Diode Q_{rr}- di/dt, I_{rr}- di/dt curves. (b) Diode Q_{rr}- I_F, I_{rr}- I_F curves. (c) Thyristor I_{rr}-di/dt curves. (d) Thyristor Q_{rr}-di/dt curves. (e) IGBT $t_{d,\mathrm{ON}}$- I_c, t_r- I_c, $t_{d,\mathrm{OFF}}$- I_c, t_f- I_c curves. (f) IGBT $t_{d,\mathrm{ON}}$- R_G, t_r- R_G, $t_{d,\mathrm{OFF}}$- R_G, t_f- R_G curves.

TABLE II
TRANSIENT PERCENTAGE VALUE OF THE FIRST-ORDER DELAY CIRCUIT

Time	Value
0.105τ	90.03%
1.386τ	25.01%
2.302τ	10.01%

1) Diode and Thyristor: The dynamic behavior of diode and thyristor are focused on the reverse recovery phenomenon during the turn-OFF time. Compared with the turn-OFF period, the turn-OFF energy loss and the forward recovery phenomenon are negligible. The uncontrolled and half-controlled devices such as diode and thyristor cannot be turned OFF by the gate signal. When the devices meet turn-OFF conditions, the VCCS $i_{\mathrm{ON}}(T_{\mathrm{vj}})$ inside the static block of the Hammerstein configuration plays a dominant role in the behavioral modeling, while the value of the $g_{\mathrm{ON}}(T_{\mathrm{vj}})$ inside the static block is set to the standard blocking state. The reverse recovery period can be separated into three periods for transient behavior as follows: 1) static state before turn-off; 2) linear decrease of reverse recovery current; and 3) static state decay of reverse recovery current. Fig. 5 shows the detailed separation of the reverse recovery period. During the Stage 1 period, the output of the static block will bypass the dynamic block and be directly linked to the output of the Hammerstein configuration.

During the turn-OFF transient, the value of di/dt is determined by the default gate resistor. The reverse recovering time t_{rr} is estimated by the following equation:

$$t_{\mathrm{rr}} = \frac{2Q_{\mathrm{rr}}}{I_{\mathrm{rr}}}. \tag{8}$$

Thus, the complete Hammerstein configuration for either the diode or thyristor can be depicted as in Fig. 4(a).

2) Insulated-Gate Bipolar Transistor: The main dynamic characteristics of IGBT are the rise time (during turn-ON period) and the fall time (during turn-OFF period) of the

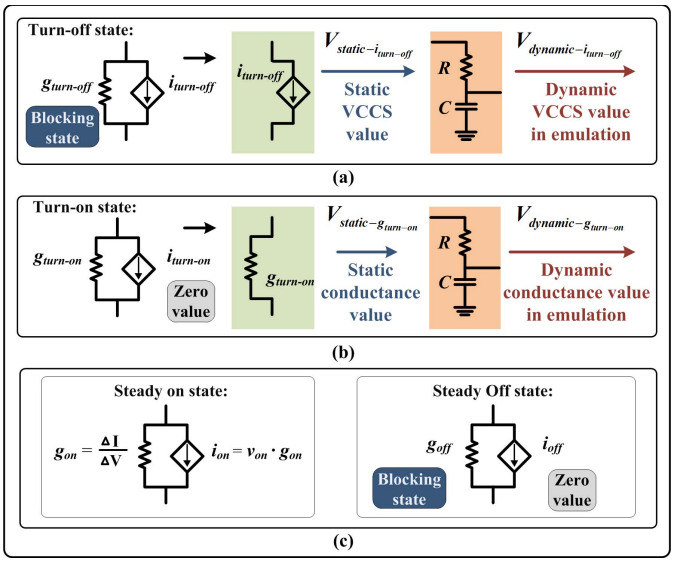

Fig. 4. Hammerstein configuration. (a) VCCS-based representation during turn-OFF. (b) Conductance-based representation during turn-ON. (c) Steady-state ON and OFF representation.

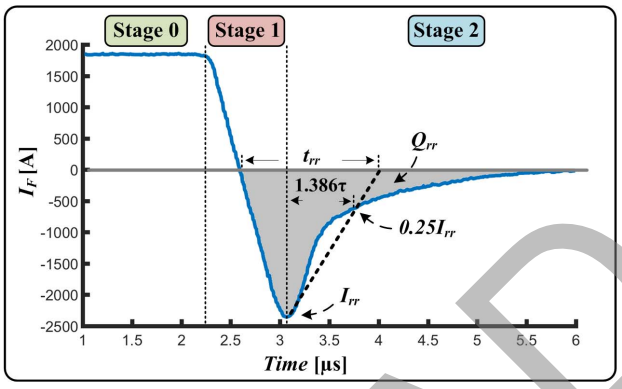

Fig. 5. Reverse recovery phenomenon of diode.

collector current. Fig. 3(e) and (f) shows the collector current-dependent and the gate resistance-dependent curves for turn-ON delay time $t_d(\text{ON})$, turn-OFF delay time $t_d(\text{OFF})$, rise time t_r, and fall time t_f.

The definition of the IGBT rise and fall time is the period from 10% to 90% and 90% to 10% of the collector current, respectively. So the rise and fall time of IGBT is equal to the normalized time 2.197τ in terms of the first-order delay circuit. By calculating τ, the dynamic part of the Hammerstein model can be determined.

In the full-controlled type devices such as the IGBT, the peak value of turn-ON current cannot be predicted until the circuit matrix equation is solved. During the turn-ON time, the VCCS $i_{\text{ON}}(T_{\text{vj}})$ in the static block will be set to zero while the value of the conductance $g_{\text{ON}}(T_{\text{vj}})$ in the static block will be set from the standard blocking state to the ON-state. During the turn-OFF time, the value of VCCS $i_{\text{ON}}(T_{\text{vj}})$ will be set to zero, while the conductance $g_{\text{ON}}(T_{\text{vj}})$ will be set from the ON-state to the standard blocking state. Thus, the complete Hammerstein configuration for the IGBT can be shown as in Fig. 4(a) for turn-OFF condition and Fig. 4(b) for turn-ON condition. Fig. 4(c) shows the steady-state representation for ON- and OFF-state.

D. Device Transient Power Loss Model

The transient power loss model is based on a normalized turn-ON or turn-OFF waveforms. By extracting the parameters from the datasheet, a transient power loss waveform model can be established with approximate timing and shape as shown in Fig. 6. The transient power loss model is separated into two periods, given as

$$\begin{aligned} E_{\text{loss}} &= E_{\text{loss-linear}} + E_{\text{loss-fod}} \\ &= \frac{1}{2} \cdot t_{\text{linear}} \cdot P_{\text{peak}} + \int_0^{\infty} P_{\text{peak}} \cdot e^{\frac{-t}{\tau_{\text{fod}}}} dt \\ &= \left(\frac{t_{\text{linear}}}{2} + \tau_{\text{fod}} \right) \cdot P_{\text{peak}} \end{aligned} \tag{9}$$

$$P_{\text{peak}} = \frac{E_{\text{loss}}}{\frac{t_{\text{linear}}}{2} + \tau_{\text{fod}}} \tag{10}$$

where E_{loss} is the total power loss during the turn-ON or the turn-OFF period, mentioned in Table I; $E_{\text{loss-linear}}$ is the power loss in the linear period; $E_{\text{loss-fod}}$ is the power loss during the first-order delay approximation time; t_{linear} is the time of linear region; P_{peak} is the peak value of transient power; τ_{fod} is the timing variable of the first-order delay approximation, and estimated according to the reference time given in Fig. 6.

In electromagnetic transient simulation [56] of power circuits, all components and devices are modeled as a discrete-time companion models consisting of current sources and resistors. The drawback of the proposed Hammerstein configuration is that the node voltage may not represent the real device nodes due to its behavioral nature. The transient power loss model works as a supplement for the proposed device Hammerstein configuration.

E. Device Thermal Network Calculation

The thermal network of the individual device is shown in Fig. 7. The power loss consumption becomes a VCCS inside this network. Cascaded combination of resistor and capacitor pairs has been utilized to compute the junction temperature, given as

$$T_{\text{vj}}(t) = P_{\text{loss}}(t) \cdot (Z_{\text{thjc}} + Z_{\text{thch}} + Z_{\text{thha}}) + T_{\text{amb}} \tag{11}$$

where $P_{\text{loss}}(t)$ is the power loss for the individual device; T_{amb} is the ambient temperature; and Z_{thjc}, Z_{thch}, and Z_{thha} are the thermal impedance from junction to case, case to heat sink, and heat sink to ambient, respectively. In this paper, each individual device is considered to be mounted on a 10-K/kW water-cooled heat sink. The thermal impedances of the devices [64], [65], are shown in Table III. τ_{th}^i is the multiplication product of R_{th}^i and C_{th}^i.

Higher resistance value in Z_{thjc} represents lower heat emission efficiency inside the device. Higher τ_{th}^i value in Z_{thjc} indicates longer delay for the temperature rising and falling. The thermal parameters of the selected thyristor show the best heat emission efficiency, while the ones of the diode present the worst. The calculation for the junction temperature of the

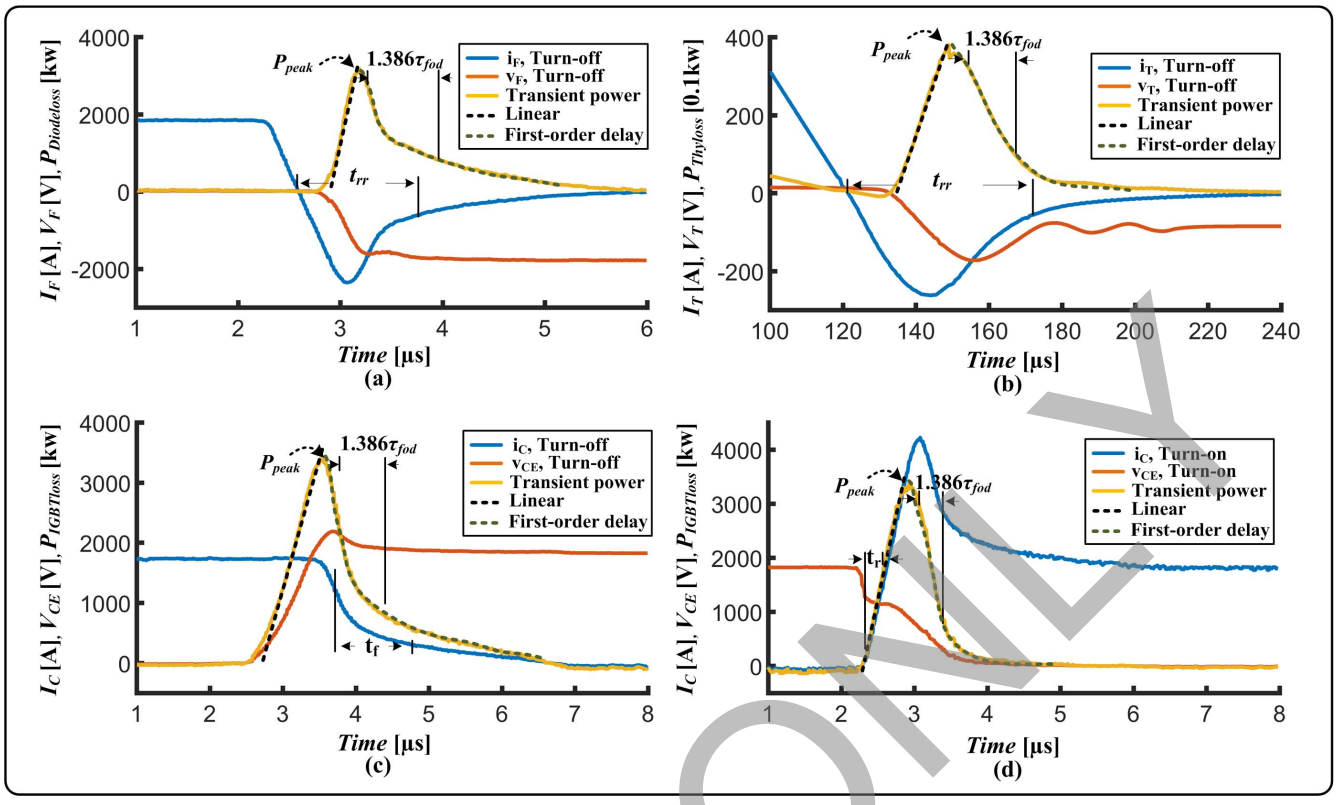

Fig. 6. Transient power loss curves. (a) Diode turn-OFF curves. (b) Thyristor turn-OFF curves. (c) IGBT turn-OFF curves. (d) IGBT turn-ON curves.

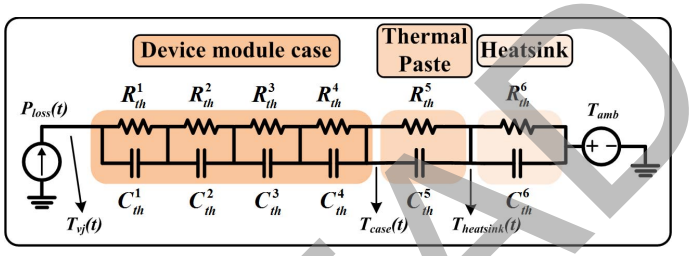

Fig. 7. Thermal calculation circuit of the power electronic device.

device is given as

$$T_{\mathrm{vj}}(t) = \sum_{i=1}^{6} \Delta T^i_{\mathrm{th}}(t) + T_{\mathrm{amb}} = \sum_{i=1}^{6} \left(\frac{R^i_{\mathrm{th}} \cdot \Delta t_{\mathrm{thm}}}{2\tau^i_{\mathrm{th}} + \Delta t_{\mathrm{thm}}} (P_{\mathrm{loss}}(t) + P_{\mathrm{loss}}(t - \Delta t_{\mathrm{thm}})) + \frac{2\tau^i_{\mathrm{th}} - \Delta t_{\mathrm{thm}}}{2\tau^i_{\mathrm{th}} + \Delta t_{\mathrm{thm}}} \Delta T^i_{\mathrm{th}}(t - \Delta t_{\mathrm{thm}}) \right) + T_{\mathrm{amb}} \tag{12}$$

where Δt_{thm} is the thermal time step.

III. Study Case: EMRG System in Real-Time SoC Platform

This section briefly introduces the Zynq SoC platform. Then it presents the details of the test circuit and its real-time implementation.

TABLE III
THERMAL IMPEDANCES FOR THERMAL NETWORK

Thermal impedance	Z_{thjc}				Z_{thch}	Z_{thha}
	i=1	i=2	i=3	i=4	i=5	i=6
$R^{i,IGBT}_{th}[K/kw]$	5.854	1.375	0.641	0.632	9	10
$\tau^{i,IGBT}_{th}[ms]$	207.4	30.1	7.55	1.57	3000	45000
$R^{i,Diode}_{th}[K/kw]$	11.54	2.887	1.229	1.295	18	10
$\tau^{i,Diode}_{th}[ms]$	203.6	30.1	7.53	1.57	3000	45000
$R^{i,Thy}_{th}[K/kw]$	2.701	0.816	0.326	0.160	1.6	10
$\tau^{i,Thy}_{th}[ms]$	947.8	124.9	14.6	3.2	3000	45000

A. Zynq SoC Platform

The Zynq-7000 All Programmable SoC [62], shown in Fig. 8, consists of a dual-core ARM-based PS and 28-nm FPGA-based PL in a single device, which enables the integration of hardware acceleration using parallelism and high-frequency clocking sequential computation.

The PS contains a dual-core processor, snoop control unit, Level-2 cache, on-chip memory, direct memory access, NEON, floating point unit engine, and the peripheral devices. The NEON engine is a general purpose single instruction multiple data processing structure. Each ARM core in the PS has a 128 b width NEON engine. The engine can process four floating type data or eight integer type data simultaneously by one instruction. With the help of this engine, the parallel and repetitive operations can be significantly accelerated on large data sets.

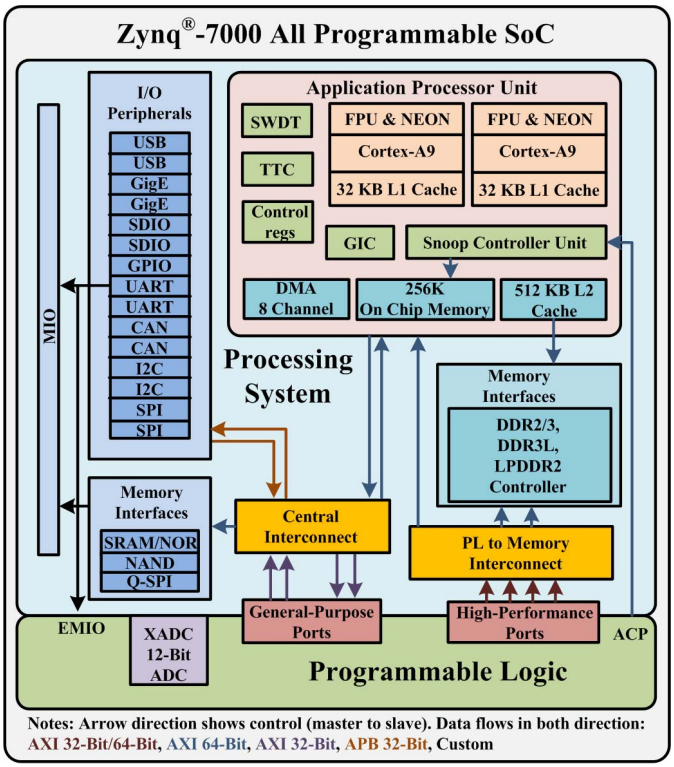

Fig. 8. Zynq-7000 All Programmable SoC schematic.

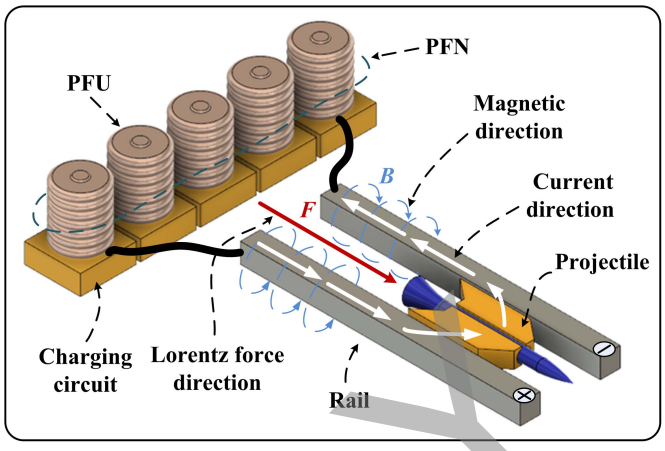

Fig. 9. EMRG system.

The communication between the PS and the PL plays a vital role in the hardware and software codesign process used in this paper. Advanced eXtensible Interface (AXI) is a high-performance communication standard for SoC designs. There are three types of AXI for PS–PL communication: AXI-ACP for coherency; AXI-GP for general purpose; and AXI-HP for high performance. For a large data set, the technical bandwidth of AXI standard varies from 2400 to 9600 MB/s.

B. Test Circuit Topology

The EMRG [58]–[61], shown in Fig. 9, has been chosen as the study case to demonstrate the efficacy of the proposed behavioral modeling via the Hammerstein configuration. In the EMRG, two circuit topologies are implemented in the SoC. The smaller network topology is the CC for the capacitors inside the PFN, which consists of the IGBT and diode. The larger network topology is the paralleled PFUs consisting of diodes and thyristors as the energy source for the EMRG.

The CC, shown in Fig. 10(a), is recommended by ABB document [67]. The inductor and the capacitor can be considered as a single component. Thus, the equivalent is a one node circuit.

The PFN circuit, shown in Fig. 10(b), consists of five PFUs and an equivalent inductor and a resistor for the rail. Each PFU is triggered by an optical switch in the rail. The TLM method [57] has been applied to separate the circuit topology for parallel execution. The inductor in the PFU is considered as a lossless transmission line, and the node current expressions are given as

$$I_m(t-\tau) = I_k(t-2\tau) + \frac{2}{Z_L}V_k(t-\tau)) \tag{13}$$

$$I_k(t-\tau) = I_m(t-2\tau)) + \frac{2}{Z_L}V_m(t-\tau)) \tag{14}$$

$$Z_L = \frac{L}{\Delta t_{\text{elect}}} \tag{15}$$

where Z_L is the equivalent TLM expression of cable inductance in discrete time; $I_m(t-\tau)$ and $I_k(t-\tau)$ represent the past history currents of the cable. Δt_{elect} is the electrical simulation time step.

C. Control System

The circuit control diagrams are shown in Fig. 11. The control method of the CC is the sliding mode control (SMC) where the charging current can be maintained in a stable range. When the voltage of the capacitor reaches the expected value, the CC will stop working.

The control method of the PFN is based on the projectile location in the rail. The optical switches are located at the specific point. When the projectile passes the optical switch, the corresponding thyristor will be triggered. The design objective of the trigger point is to maintain a stable current for the generation of the Lorentz force during the acceleration process.

D. Implementation Method

The CC can be considered as one node circuit after the combination of the inductor and capacitor component. The node voltage calculation for solving the CC is sequential. The PFN circuit utilizes the TLM method to separate the circuit topology consisting of a large circuit matrix into several parallel circuit submatrices.

A performance comparison of PS and PL for both charging and PFN circuit is demonstrated to decide the suitable compute hardware for each circuit. For this purpose, all the power electronic devices are considered as a VCCS in parallel with a resistor under the static thermal state. It should be noted

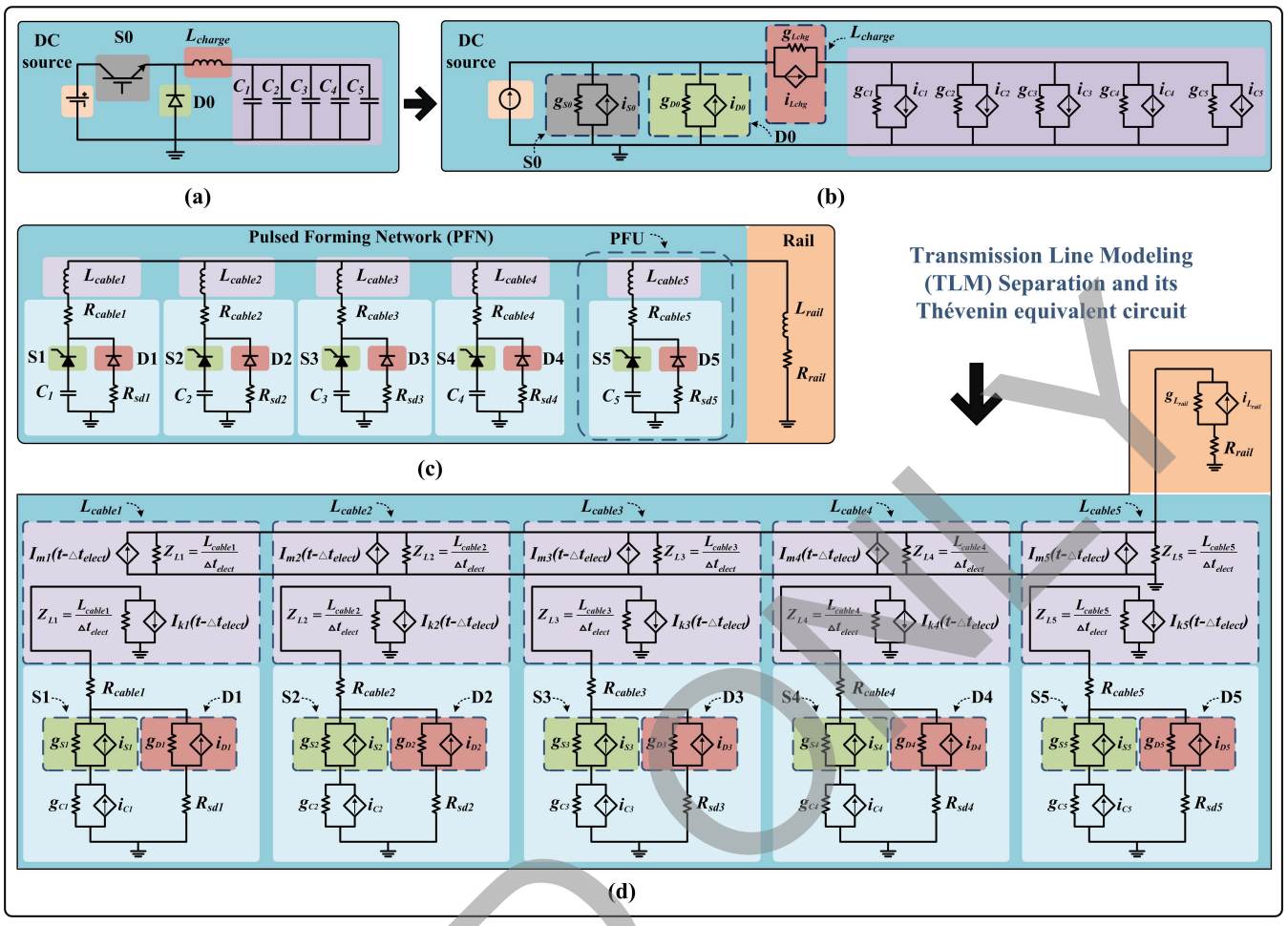

Fig. 10. EMRG circuit topologies and their Hammerstein-based Thévenin equivalents. (a) CC. (b) Thévenin equivalents for the CC. (c) PFN. (d) Thévenin equivalents for the PFN.

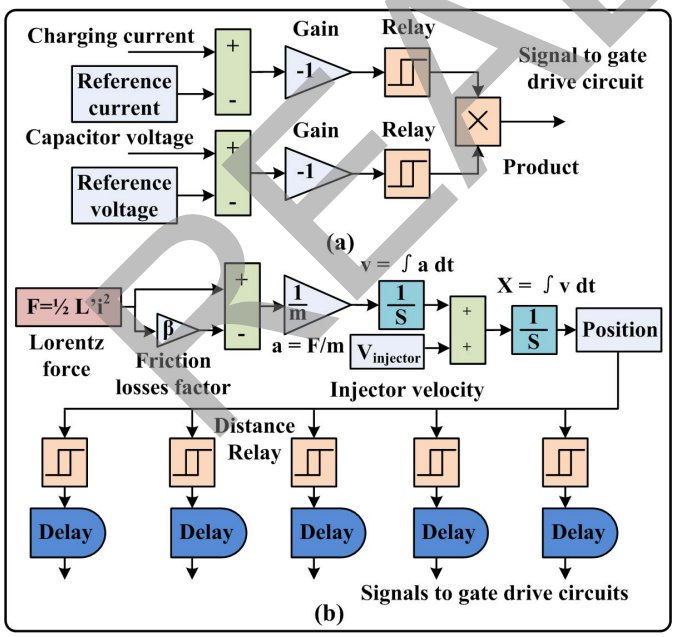

Fig. 11. EMRG control diagram. (a) CC and (b) PFN.

that the no device-level behavioral calculations are included in the comparison because the fundamental EMTP circuit calculation cannot be optimized much while the device-level behavioral calculation varies from algorithm to algorithm. After the performance test, the results proved that the PS was suitable for the CC with NEON acceleration, while the PL was appropriate for PFN.

In this case, it is reasonable to implement the CC in Cortex A9 Core 0 of the PS and PFN into the PL. The device thermal circuit was implemented in the Cortex A9 Core 1 of the PS. CC and its thermal circuit are communicated by the global signal inside the PS, while PFN and its thermal counterpart are communicated by the AXI standard between PS and PL. The simulation time step for CC is 100 ns, while the time step for PFN one is 2.5 μs. The thermal circuits for both circuits are calculated at a 10-μs time step.

E. State Charts

Fig. 12 shows the calculation procedure of the CC and the PFN. The cooperation between Cortex A9 cores and the PS–PL is also indicated in the state charts.

The dashed green states show the initialization of the electrical circuits or the thermal circuits calculation. The dotted blue and the solid red states indicate the repetitive calculation for the electrical and thermal circuit, respectively. The background colors of the state chart specify the compute hardware resource type: either the cores of the PS or the PL.

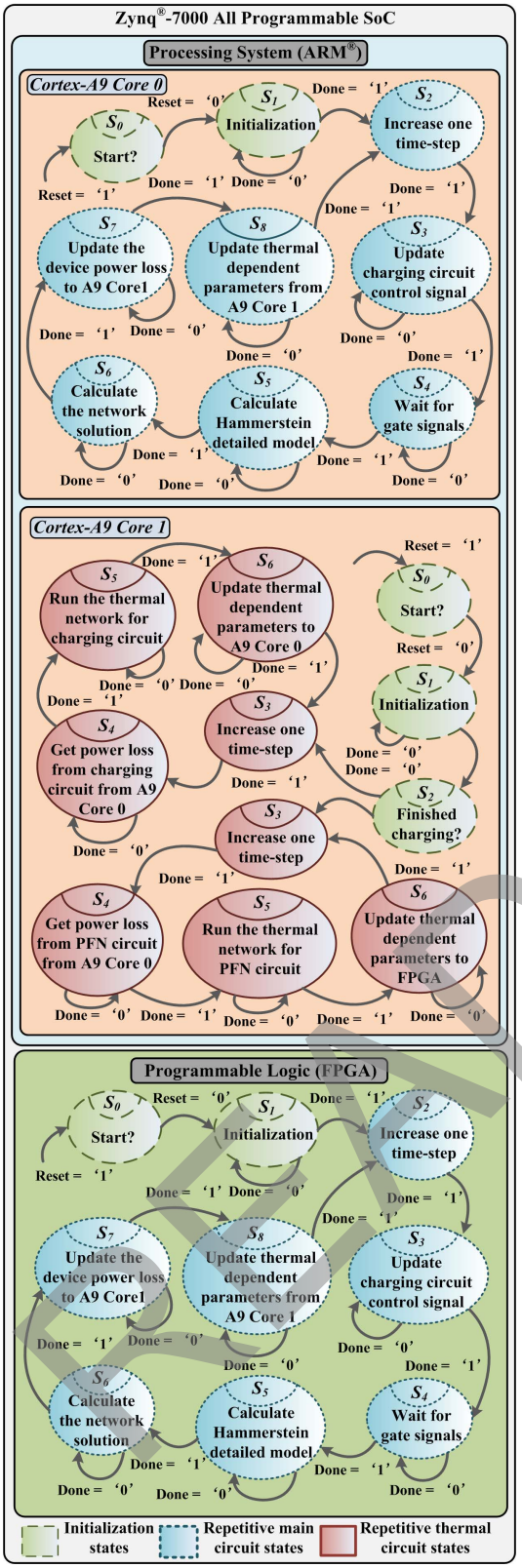

Fig. 12. State chart of EMRG system on the Zynq SoC platform.

The Cortex-A9 Core 1 execute the thermal circuit and temperature-dependent parameters calculation. After the initialization, the state chart splits into two calculation loops. The loop selection depends on the charging state of the EMRG system. If the capacitor voltage reaches the desired value and the EMRG system is ready to launch the projectile, the state chart will go into the PFN thermal loop or it will go to the CC thermal loop.

The Cortex A9 Core 0 and PL execute the CC and the PFN circuit, respectively, which will also update the power loss to the Core 0 and get respective parameters for the next step electrical calculation.

TABLE IV
EXECUTION TIME COMPARISON PER TIME STEP FOR CC AND PFN

Hardware time cost	Core 0 O0 $0.8GHz$	Core 0 O1 $0.8GHz$	Core 0 O2 $0.8GHz$	Core 0 O3 $0.8GHz$	PL HLS $0.1GHz$
CC (ns)	330	170	7.5	7.5	580
PFN (ns)	7845	3765	3590	2510	1870

TABLE V
PL RESOURCE UTILIZATION FOR CC AND PFN

Circuit type	BRAM	DSP	FF	LUT
CC	768 (70%)	17 (1%)	9654 (2%)	47895 (21%)
PFN	314 (28%)	220 (24%)	46044 (10%)	75509 (34%)

IV. REAL-TIME SOC EMULATION RESULTS AND DISCUSSION

A. Compute Hardware Resource Selection and Performance

Table IV shows the performance comparison for both the CC and the PFN circuit. The hardware configurations are indicated at the top of Table IV. The number of the Ox is the optimization level of the NEON engine. Level-3 (O3) is the highest level of NEON instruction optimization by the compiler in Xilinx software development kit. The NEON engine can theoretically accelerate the execution speed up to four times faster in floating type data processing. In the PL, high-level synthesis (HLS) is utilized to optimize the corresponding code to reduce the overall latency. In Table IV, the execution speed under different applied condition are shown for both CC and PFN. The Level-3 optimization achieves the shortest computation delay in the Core 0 of PS. However, the execution time of PL for PFN is 34% shorter than the one in PS. This is because the PFN consists of six paralleled subcircuit, which fits the highly parallel FPGA execution architecture. CC is a sequential topology which can utilize the advantage of high-sequential clocking computation feature in Core 0 of PS. The execution time of CC in Core 0 is 77.3 times faster than the one in PL. In this case, it can be concluded that CC is suitable for PS while PFN is appropriate for PL.

Table V illustrates the PL resource utilization in the performance comparison. Compared with the CC, the PFN circuit consumes relatively higher computational resource due to larger sized circuit topology. The thermal calculation is implemented on the other core of the PS. The proposed implementation method will be validated in the next section.

B. Results of Full Circuit Implementation

Figs. 13–15 show the real-time implementation results of the full circuit topology. Fig. 13(a) demonstrates the diode

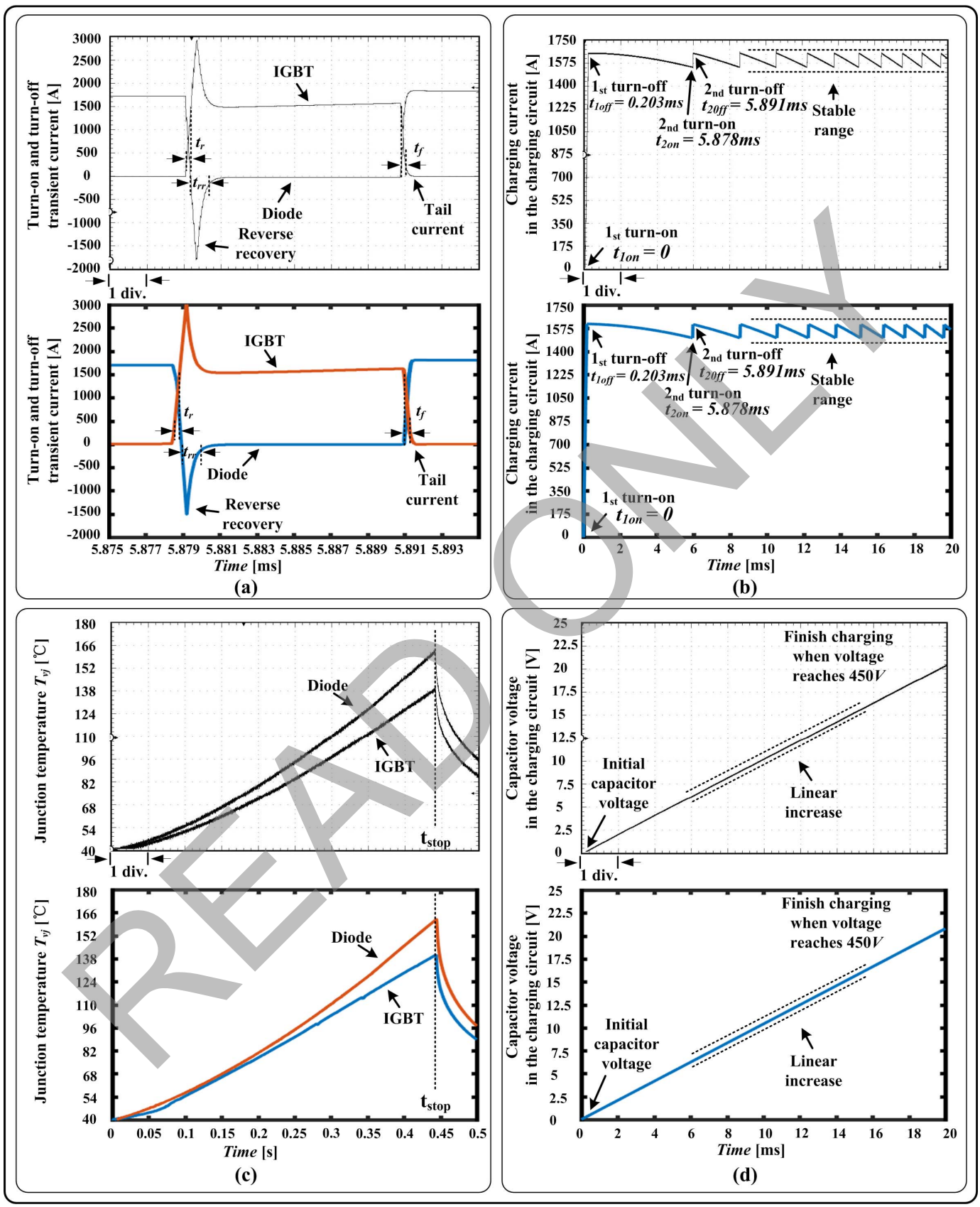

Fig. 13. System-level and device-level results for CC and PFN from real-time hardware emulation (top subfigure) and off-line simulation by SaberRD software (bottom subfigure). (a) IGBT and diode turn-ON and turn-OFF transient current. (b) Charging current in the CC. (c) Junction temperature for IGBT and diode. (d) Capacitor voltage in the CC. Scale: (a) x-axis: 0.002 ms/div; (b) and (d) x-axis: 2 ms/div; and (c) x-axis: 50 ms/div.

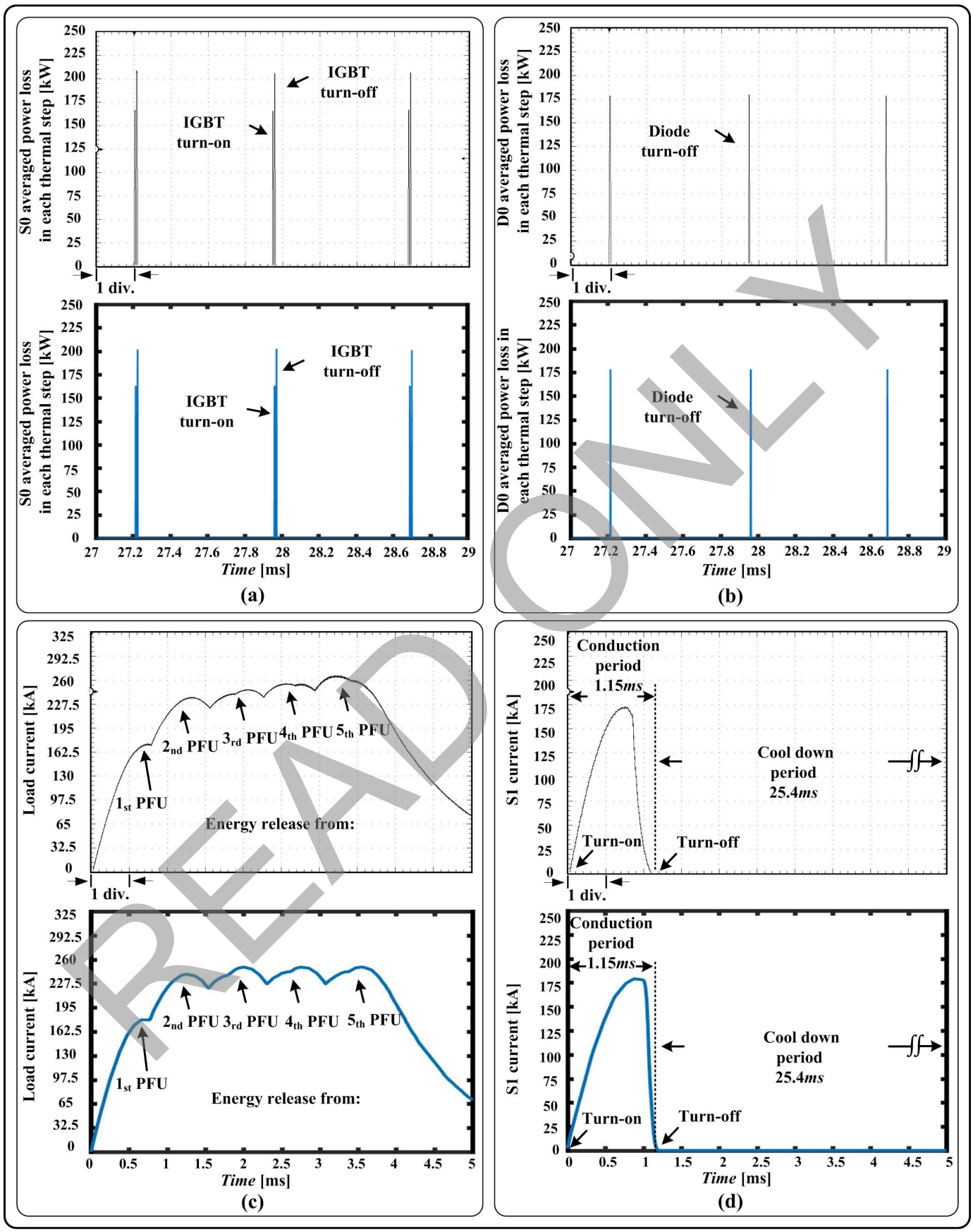

Fig. 14. System-level and device-level results for CC and PFN from real-time hardware emulation (top subfigure) and off-line simulation by SaberRD software (bottom subfigure). (a) S0 averaged power loss in each thermal step for the CC. (b) D0 averaged power loss in each thermal step for the CC. (c) Load current in the PFN. (d) S1 current in the PFN. Scale: (a) and (b) x-axis: 0.2 ms/div; (c) and (d) x-axis: 0.5 ms/div.

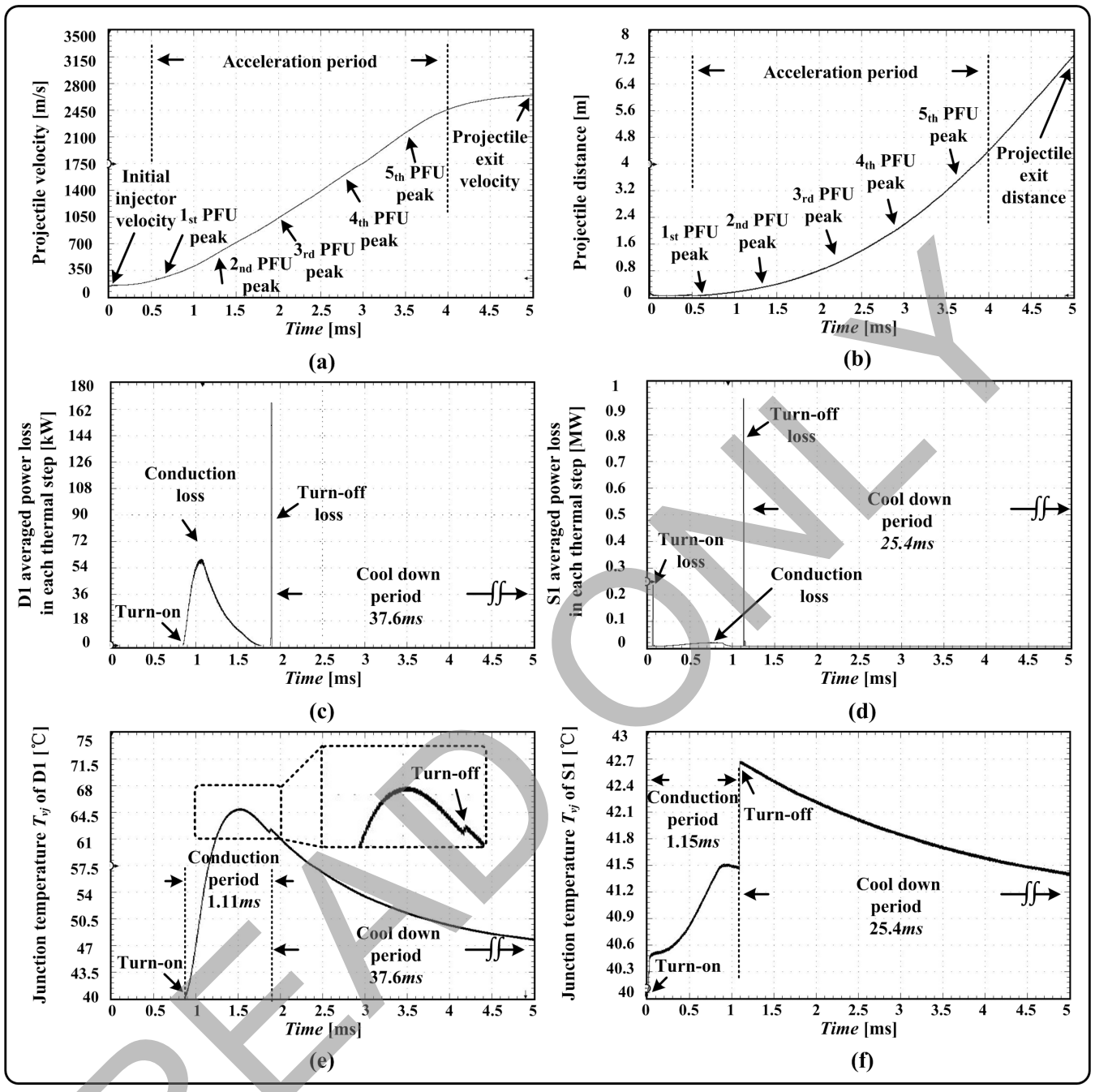

Fig. 15. System-level and device-level results for the PFN from real-time hardware emulation. (a) Projectile velocity. (b) Projectile distance. (c) D1 averaged power loss in each thermal step. (d) S1 averaged power loss in each thermal step. (e) Junction temperature of D1. (f) Junction temperature of S1. Scale: (a)–(f) x-axis: 0.5 ms/div.

and IGBT turn-ON and turn-OFF transient waveform. When turned ON, IGBT shows overshoot phenomenon which is mainly introduced by the reverse recovery of diode inside the circuit topology. When turned OFF, IGBT shows tail current in the transient due to the recombination of minority carriers. Fig. 13(b) and (d) demonstrates the charging current and capacitor voltage, respectively. The sawtooth shape of charging current is due to the SMC, which intend to maintain the charging current at a stable range. With a stable charging current, the voltage of the capacitor shows a linear increase, which is regarded as a safe strategy for the device. Fig. 13(c) shows the temperature variation during the charging period. CC stopped charging at t_{stop} when the capacitor voltage reached 450 V. Fig. 14(a) and (b) shows the averaged power loss of diode and IGBT in each thermal time step Δt_{thm}, respectively. Both turn-ON and turn-OFF average power loss in each thermal time step are considered in IGBT thermal network while only turn-OFF is included for the diode. In Fig. 14(c), the envelop of the projectile indicated different PFU energy release time in EMRG system. Fig. 14(d) shows S1 current in the PFN circuit. The small difference between the results can be considered as the consequence of the extreme application

TABLE VI

LATENCIES OF CC WITH DEVICE-LEVEL BEHAVIORAL (CORE 0) AND THERMAL (CORE 1) CALCULATION AND ITS CORE–CORE COMMUNICATION

Core 0 O3 $0.8GHz$	Core 1 O3 $0.8GHz$	Core 0 -Core 1 $0.8GHz$	Core 1 -Core 0 $0.8GHz$	Average delay per time-step
$87.5ns$	$1540ns$	$115ns$	$52.5ns$	$89.175ns$

TABLE VII

LATENCIES OF PFN WITH DEVICE-LEVEL BEHAVIORAL (PL) AND THERMAL (PS-CORE 1) CALCULATION AND PS–PL COMMUNICATION

PL HLS $100MHz$ (4 time-steps)	PS - Core 1 O3 $0.8GHz$	PL - PS	PS - PL	Average delay per time-step
$2280ns$	$875ns$	$2115ns$	$1525ns$	$1698.75ns$

condition whose physical parameters may not be precisely described in the datasheet. After releasing the energy, S1 takes a relatively long time to cool down. In Fig. 15(a) and (b), the velocity and distance of the projectile are shown, respectively, with the peak indication of each PFU energy release. The initial injector velocity is 140 m/s and projectile exit velocity is 2615.4 m/s after the acceleration period. The projectile exit length is 7.23 m. Fig. 15(c) and (d) shows the diode's averaged power loss and the junction temperature, respectively, in each thermal time step. The temperature jumped over 20 °C in less than 1 ms, which indicates that the heat emission efficiency is relatively low. In Fig. 15(e) and (f), the thyristor's averaged power loss and the junction temperature, respectively, in each thermal time step are shown. Compared with the diode, the thyristor shows relatively higher heat emission efficiency regarding temperature variation range.

Table VI explains the latencies of the CC with device-level behavioral and thermal calculation. The emulation time step of the CC is 100 ns, while the time step of its thermal calculation is 10 μs. A shorter time step in thermal calculation do not improve the accuracy in the thermal dynamic. The electrical circuit (Core 0) will update the power loss to the thermal circuit (Core 1) every 100 times. With fewer Core–Core data transmission, the emulation of both thermal and electrical side can be accelerated and the accuracy of both sides remains the same under the circumstance. The thermal circuit (Core 1) update the temperature-dependent parameters to the electrical circuit (Core 0) in the next time step. These temperature-dependent parameters are critical in the calculation of the equivalent electrical model in the equations and figures in Section II. The latency of the electrical circuit (Core 0), the thermal circuit (Core 1), electrical to thermal circuit communication (Core 0–Core 1), and thermal to electrical circuit communication (Core 1–Core 0) are 87.5, 1540, 115, and 52.5 ns, respectively. The averaged delay per time step is less than the required time step 100 ns.

Table VII shows the latencies of the PFN circuit with device-level behavioral and thermal calculation. The emulation

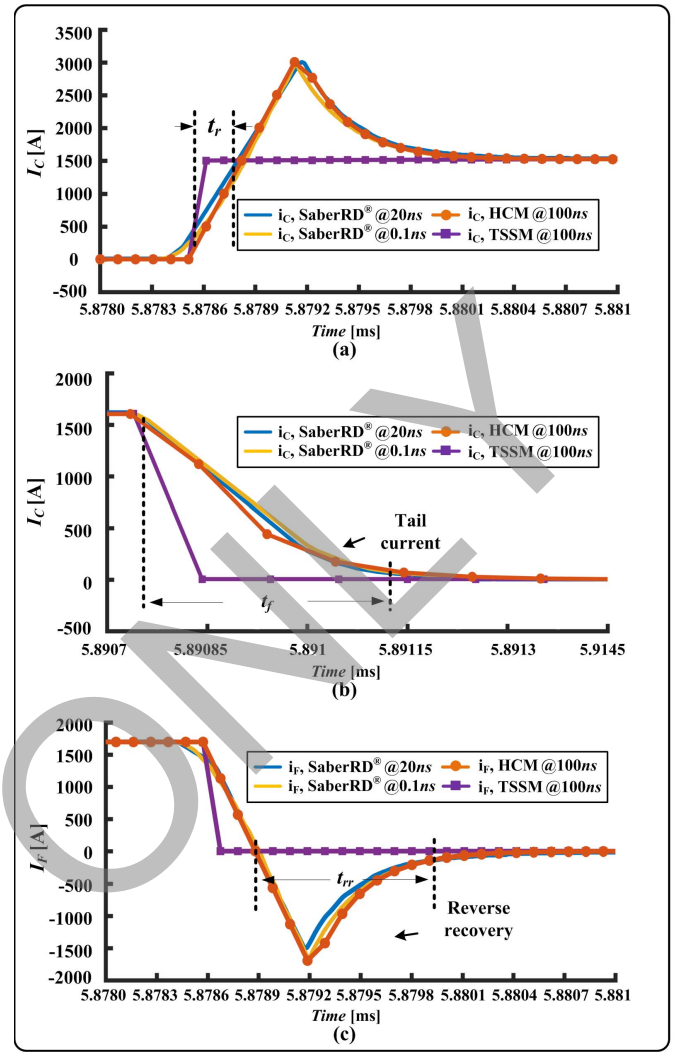

Fig. 16. Accuracy comparison of TSSM, HCM models with SaberRD. (a) IGBT turn-ON. (b) IGBT turn-OFF. (c) Diode turn-OFF.

time step of the PFN is 2.5 μs, while the time step of its thermal calculation is 10 μs. By applying smaller time step, the accuracy of the thermal dynamic will not be improved but the execution time can be enlarged enormously. The electrical circuit (PL) of the PFN updates the power loss to the thermal circuit (Core 1) every four steps. The thermal circuit (Core 1) updates the temperature-dependent parameters to the electrical circuit (PL) in the next time step. These temperature-dependent parameters have been applied in the Hammerstein configuration modeling in Section II. The latency of the electrical circuit (PL) of four time steps, thermal circuit (Core 1), electrical to thermal circuit communication, and thermal to electrical circuit communication are 2280, 875, 2115, and 1525 ns, respectively. Although the communication delay between the PS and PL is 20 times larger than the Core–Core one, the thermal and electrical circuits of PFN still run in real-time with the proper allocation of computation hardware resource. The averaged delay per time step is less than the required time step 2500 ns. The PL is controlled by Core 1 and works as a hardware accelerator for the electrical circuit to compute the results of four time steps.

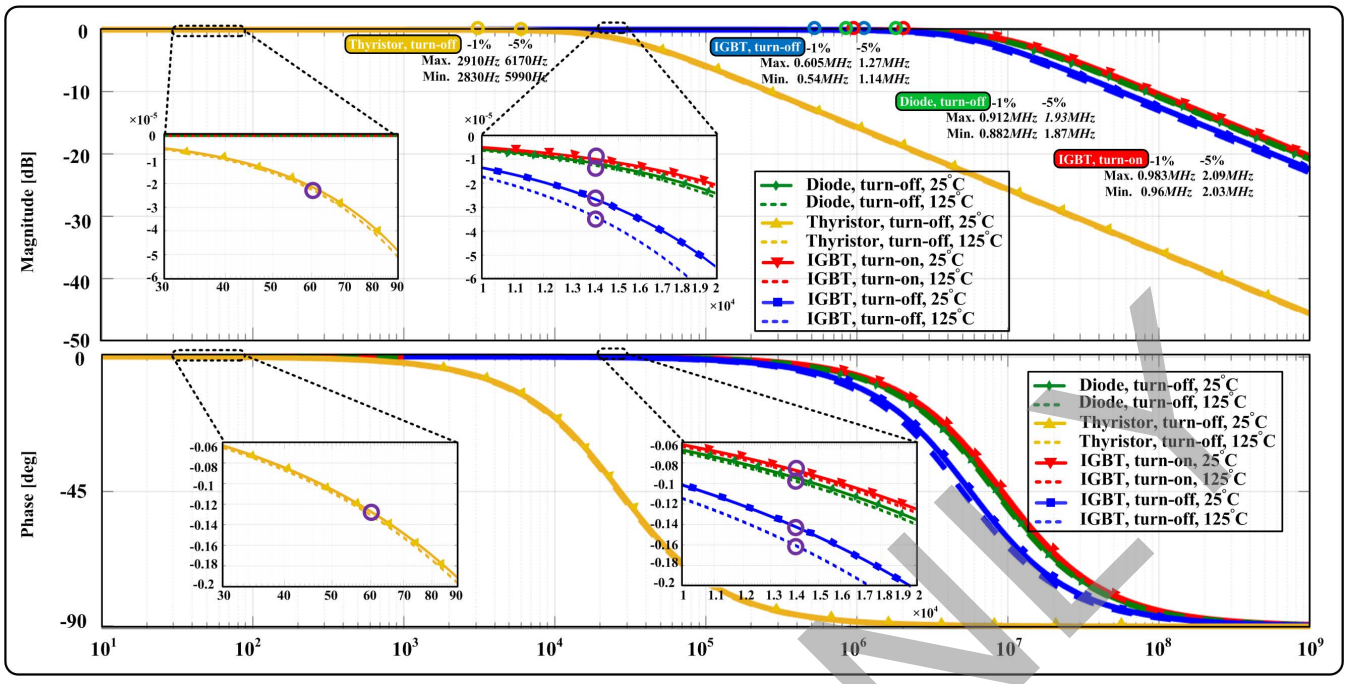

Fig. 17. Frequency response of proposed Hammerstein configuration for diode, thyristor, and IGBT.

TABLE VIII
PL RESOURCE UTILIZATION FOR THE PFN CIRCUIT WITH DEVICE-LEVEL BEHAVIORAL CALCULATIONS

BRAM	DSP	FF	LUT
68 (6%)	390 (43%)	93418 (21%)	159979 (73%)

TABLE IX
COMPARISON OF DEVICE SWITCHING TIMES AND AVERAGE POWER DISSIPATION

	SaberRD®	SoC	Error (%)
CC switching at $14kHz$			
t_r(IGBT)	$248.5ns$	$242.6ns$	2.37
t_f(IGBT)	$392.2ns$	$405.6ns$	3.42
t_{rr}(Diode)	$1041ns$	$1027ns$	1.34
P_{on}(IGBT)	$22.7kW$	$23.5kW$	3.52
P_{off}(IGBT)	$28.9kW$	$29.9kW$	3.46
P_{cond}(IGBT)	$0.38kW$	$0.40kW$	5.26
P_{rr}(Diode)	$25.2kW$	$25.3kW$	0.47
P_{cond}(Diode)	$0.16kW$	$0.17kW$	6.25
PFU energy release in $5ms$			
t_{rr}(Thyristor)	$62.3\mu s$	$63.7\mu s$	2.25
P_{rr}(Diode)	$0.33kW$	$0.34kW$	3.03
P_{cond}(Diode)	$5.41kW$	$5.47kW$	1.11
P_{rr}(Thyristor)	$18.64kW$	$18.51kW$	0.69
P_{cond}(Thyristor)	$3.67kW$	$3.81kW$	3.81

Table VIII presents the PL resource utilization of the PFN circuit. It is clear that the higher computation resource consumption is required due to the higher complexity of the device-level transient behavioral calculation.

In Fig. 16, the accuracy comparison of TSSM, the proposed HCM, and SaberRD has been demonstrated. TSSM and HCM are implemented in the real-time SoC platform with a 100-ns time step. The execution times for the TSSM are shown in Table IV, while the execution times for HCM are shown in Tables VI and VII. The SaberRD model is demonstrated in 0.1 and 20 ns time step. The SaberRD model cannot converge at the 100-ns time step and the accuracy of the 20-ns result gets worse in the simulation, especially during the IGBT turn-ON and diode turn-OFF periods. SaberRD takes 1.5 h with a 0.1-ns time step and 92 s with a 20-ns time step for a 10-ms simulation.

In Fig. 17, the frequency response of the proposed Hammerstein behavioral models for the diode, thyristor, and IGBT are shown. The expanded windows show the normal operating frequency (circled). The highest switching frequency applied in this paper for diode and IGBT is 14 kHz. Although the thyristor is not switching at 60 Hz (circled) in this paper, it can be considered as the reference for normal phase control switching frequency. The temperature variation has little impact on the frequency response. The operating range for the proposed diode, thyristor, and IGBT model are 0–0.882 MHz, 0–2830 Hz, and 0–0.54 MHz, respectively, within 1% error.

In Table IX, the switching times and average power dissipation of diode, thyristor, and IGBT are compared from off-line SaberRD simulation and real-time SoC emulation under two conditions. The first condition is that the CC is switching at a steady frequency at 14 kHz. The second condition is during the energy release period of a single PFU. The time step for SaberRD and SoC emulation is 0.1 and 100 ns, respectively. As can be seen, there is good agreement of the results.

V. CONCLUSION

This paper proposed and emulated the real-time device-level dynamic electrothermal models for diode, thyristor, and IGBT

based on Hammerstein configuration on a SoC-based hardware and software codesign platform for the application of EMRG system. The Hammerstein configuration modeling procedures reduce the complexity of building accurate device-level power electronic models. The modeling procedure of the static and dynamic electrical models, transient power loss model, and thermal network calculation is given based on the dedicated device datasheet. The proposed models have been validated in two circuits of the EMRG system and compared with the result from the off-line device-level software SaberRD. Based on the different topology of the CC and the PFN circuit inside the EMRG system, the hardware compute performance comparison, selection, and acceleration have enabled the goal of real-time execution. Future work is planned for the application of the Hammerstein-based nonlinear modeling for more complex power converter systems for industrial applications.

APPENDIX

Parameters for EMRG test circuits are as follows:

A. CC: $L_{\text{charge}} = 200\ \mu\text{H}$, $V_{\text{DC}} = 1800$ V.

B. PFN: $L' = 0.327\ \mu\text{H/m}$, $R_{\text{rail}} = 0.38\text{m}\ \Omega$, $L_{\text{rail}} = 0.30\ \mu\text{H}$, $C_i = 0.3$ F, $R_{\text{cablei}} = 50\ \mu\Omega$, $L_{\text{cablei}} = 1\ \mu\text{H}$, $R_{\text{sdi}} = 8\ \mu\Omega$, where $i = 1, 2, 3, 4, 5$.

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