The Applicability of Ferroelectrics for Analog and Digital Transistor Applications

by

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Abstract

As transistors scale to ever smaller dimensions, power density becomes an increasingly important issue in integrated circuit (IC) design. Recently, negative-capacitance field-effect transistors (NCFETs), realized by stacking ferroelectric material on top of conventional gate oxides, have been proposed to reduce power consumption in modern aggressively scaled devices. The negative capacitance of these ferroelectric materials provide voltage amplification to the transistor in order to reduce the subthreshold-swing (SS), which would reduce the active power consumption of the device via a reduction of the supply voltage. Beyond reduction of power consumption for individual transistors, the unique negative capacitance behavior in these ferroelectric materials also offers a vast array of options in modern IC design. As a result, ferroelectric materials are an exciting area of research.

The current state-of-the-art modeling approach for the dynamics of ferroelectric materials is via the Landau-Khalatnikov (LK) equation. In this work, we implement a multi-domain improvement upon the LK equation and combine it with Cadence circuit simulations to model and predict the characteristics of NCFETs and other ferroelectric devices.

In the first stage of this work, we calibrate our multi-domain LK model to experimental results to show a very strong match. Using this calibrated model, we examine the potential speed limitations of NCFETs and identify the requirement on the viscosity

parameter of the ferroelectric materials to provide sub-picosecond rise time required for modern transistors.

In the second stage, we propose a new measurement technique for extracting the LK parameters of a ferroelectric material. We demonstrate via Cadence circuit simulation that this new measurement technique is able to accurately extract all LK parameters, including the viscosity parameter, which is difficult to extract using standard techniques.

In the third stage, we propose a new application for ferroelectric materials to increase the unity-current-gain frequency f_T of a transistor. By placing the ferroelectric in parallel with the FET gate, the negative capacitance of the ferroelectric cancels the positive gate capacitance of the FET, which in turn increases the f_T. This new application of ferroelectrics opens new possibilities for IC design.

Overall, this work improves the understanding of ferroelectric materials pertaining to their applications in IC design, providing critical information for the electron device community as it continues to explore methods to advance the performance of nanoscale electronics into the 2030s and beyond, the current horizon of the International Roadmap for Devices and Systems.

Preface

Versions of chapters 2, 3, and 4 in this thesis were published in *IEEE Transactions on Electron Devices* as

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- Z. C. Yuan *et al.*, "Feedback stabilization of a negative-capacitance ferroelectric and its application to improve the f_T of a MOSFET," *IEEE Trans. Electron Devices*, vol. 68, no. 10, pp. 5101-5107, Oct. 2021.

In all these published works, I was the primary researcher, responsible for writing software source code that implements ferroelectric physics and integrating it into a circuit simulator, as well as data analysis and manuscript composition.

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Chapter 1

Introduction

1.1 Overview

The performance improvement of electronic devices has been driven by the exponentially increasing transistor density in modern chips. This trend, known as Moore's law, requires transistors to scale to ever-smaller dimensions, and the electronics industry is becoming increasingly concerned with managing the power density in large digital chips [1], [2]. One way to reduce power density is to use transistors with a low subthreshold swing (SS). However, conventional transistors are fundamentally limited to SS $\geq$ 60 mV/dec by Boltzmann mechanics. Negative-capacitance field-effect transistors (NCFETs) realized by stacking ferroelectric material on top of conventional gate oxides have recently been proposed as a potential way to break the 60 mV/dec limit [3]-[6].

Since the negative capacitance effect originates from a physical phenomenon of ions physically displacing in a distorted crystal lattice, it may not be able to respond at the speed required for modern electronic integrated circuits. We use numerical simulations based on a phenomenological model of the ferroelectric material to explore the potential speed limitation of NCFETs. In addition, we use this phenomenological model to simulate a prospective measurement method to determine if a ferroelectric material is suitable for NCFETs. Finally, we explore a novel application for ferroelectrics in high-f_T (high unity-current-gain frequency) applications by placing a ferroelectric in parallel with a MOSFET gate. Each of these studies are explored in detail in Chapters 2, 3, and 4, respectively.

1.2 Background

1.2.1 What is Negative Capacitance?

In ferroelectric materials, the crystal lattice assumes a tetragonal unit cell rather than a cubic cell, where one of the cell dimensions is longer than the other two; the ions in this unit cell are pinned to asymmetrical positions in the direction of the elongated side, which makes the overall polarization of the crystal non-zero at steady state. Thus, a capacitor using a ferroelectric material as the oxide is stable at a state that exhibits non-zero spontaneous polarization. This capacitor can be flipped to an equal but opposite polarization by applying an electric field to deform the crystal to a state with the opposite polarization [7], [8]. Fig. 1.1 depicts a diagram of a ferroelectric crystal lattice, specifically that of lead zirconium oxide (PZT).

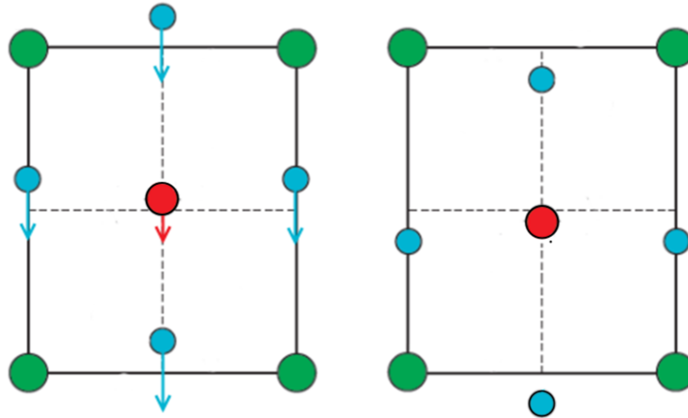

Fig. 1.1. Visual example of a ferroelectric lattice with the ions displaced to an off-center position. An externally applied electric field can push the ions to the mirror-opposite off-center position. The arrows represent the direction the ions move to reach the mirror position.

From understanding the physical origin of the ferroelectric material's negative capacitance, we can derive a phenomenological model for the ferroelectric material. First, due to the bi-stable nature of the ferroelectric crystal, we can assume it has a double-welled potential energy landscape as shown in Fig. 1.2.

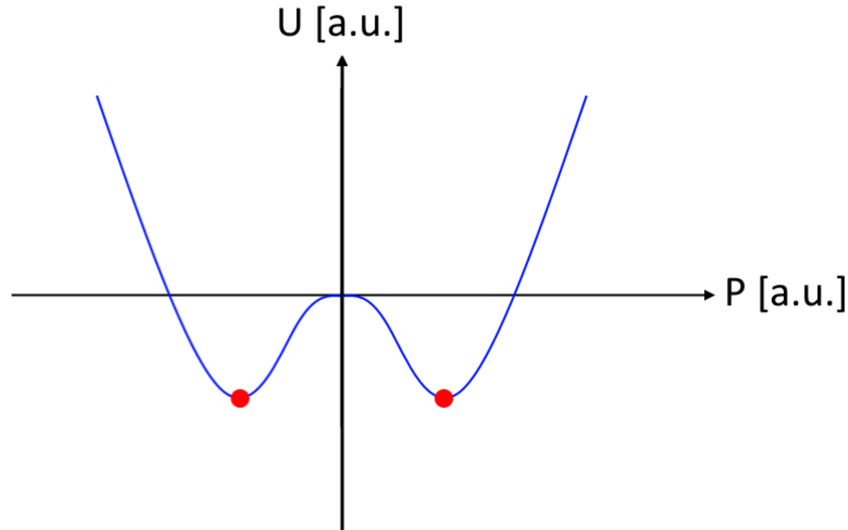

Fig. 1.2. Potential energy of a ferroelectric material as a function of its polarization. The two red dots located at the minima represent the two stable configurations of the ferroelectric ions.

For simplicity, we also assume that the potential energy landscape is an even function in P; i.e., we assume the potential energy of the ferroelectric material is the same when the ions within the crystal lattice are in each of the opposite mirrored positions. From these assumptions, we can derive a Taylor series polynomial describing the ferroelectric material's potential energy, which we will truncate to the sixth order:

$$U(P) = \alpha P^2 + \beta P^4 + \gamma P^6 \tag{1.1}$$

where the terms α, β, and γ are the Taylor coefficients. A capacitor using ferroelectric materials as the oxide material can be described by a superposition of the polarization of the ferroelectric material and the direct electrostatic interaction between the capacitor plates, as described by the well-known Maxwell's equation:

$$Q = \int \varepsilon_0 E + P \, dA \tag{1.2}$$

This description of the behavior of ferroelectric material easily lends itself to a phenomenological circuit model of a ferroelectric capacitor, as shown in Fig. 1.3. The ferroelectric capacitor is modeled by two capacitors each representing the direct electrostatic interaction of the capacitor plates and the charge accumulated on the capacitor

plates due to the polarization of the ferroelectric material, respectively. The polarization of the ferroelectric material has been modeled as a lossy capacitor for completeness. The capacitor representing direct electrostatic interaction has a charge of

$$Q_{\text{vac}} = \int \varepsilon_0 E \, dA = \varepsilon_0 \frac{V_{\text{FE}}}{t_{\text{FE}}} A \tag{1.3}$$

where we have taken the simplifying assumption that the capacitor has uniform charge distribution across its plates and experiences uniform electric field. The capacitor representing the direct electrostatic interaction of the capacitor plates has a capacitance equal to a vacuum capacitor of the same size $C_{\text{vac}} = \varepsilon_0 A / t_{\text{FE}}$. The capacitance of the model capacitor representing only the contribution of the ferroelectric polarization can be derived from (1.1) by the standard capacitor relation:

$$\frac{1}{C_P} = \frac{d^2 U}{d {Q_p}^2} \tag{1.4}$$

where C_P is the instantaneous capacitance of this model capacitor and Q_p is the charge accumulated on the ferroelectric capacitor due to only the polarization of the ferroelectric material:

$$Q_p = \int P \, dA = PA \tag{1.5}$$

where we have again assumed that the capacitor has uniform charge distribution across its plates. The sum of the charge on both model capacitors is the charge accumulated on the actual ferroelectric capacitor $Q_{\text{vac}} + Q_p = Q$.

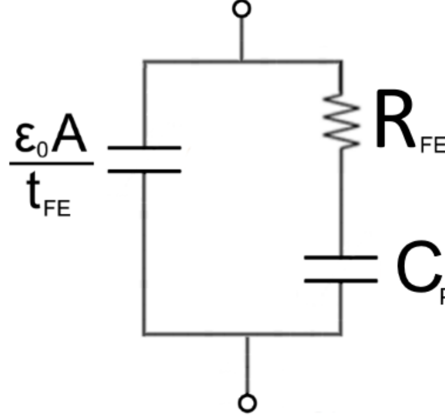

Fig. 1.3. Circuit model of a ferroelectric capacitor. $\varepsilon_0 A/t_{\mathrm{FE}}$ represents the direct electrostatic interaction between capacitor plates, R_{FE} represents the internal losses within the ferroelectric material, and C_P is the instantaneous capacitance due to the polarization of the ferroelectric material.

At this point, we have derived a model for the ferroelectric capacitor using only the understanding of the bi-stable nature of the ferroelectric crystal and making a simplifying assumption that the potential energy of a particular configuration of the ion positions within the crystal must be equal to its mirror opposite. It is important to note that this model is not only a simple representation of the most important properties of the ferroelectric capacitor, but is mathematically equivalent to the state-of-the-art modeling approach for the dynamics of the ferroelectric capacitor via the Landau-Khalatnikov (LK) equation [9], [10]:

$$\rho \frac{dP(t)}{dt} = E(t) - 2\alpha P(t) - 4\beta P^3(t) - 6\gamma P^5(t) \tag{1.6}$$

where ρ is the kinetic coefficient modeling the ion's resistance to movement within the ferroelectric crystal and is related to R_{FE} in our circuit model by $R_{\mathrm{FE}} = \rho t_{\mathrm{FE}}/A$, and α, β, and γ are the Landau parameters modeling material properties of the ferroelectric material and are equivalent to the same parameters in (1.1). By differentiating the potential energy (1.1) of the ferroelectric capacitor with respect to charge, we can plot the V-Q relation in Fig. 1.4.

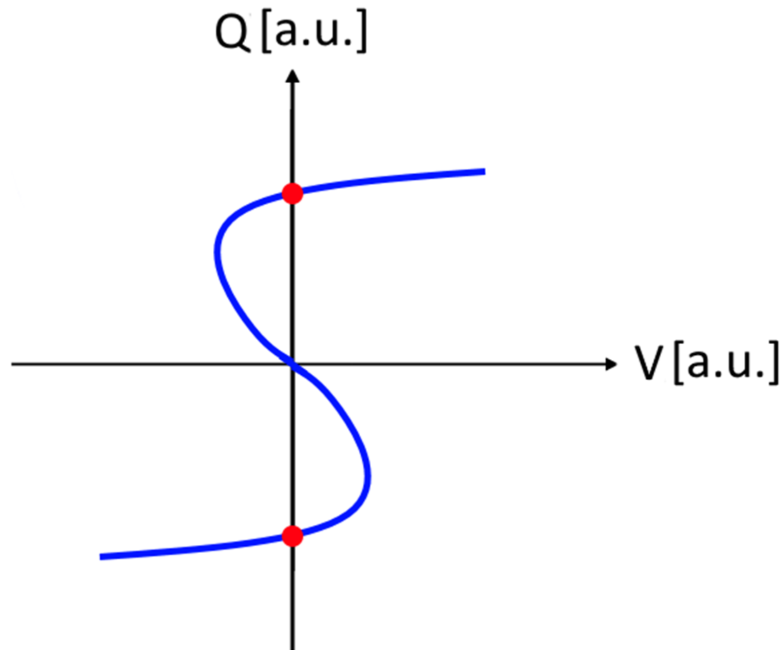

Fig. 1.4. Hypothetical V-Q curve of a ferroelectric capacitor. The two red dots represent the two stable configurations of the ferroelectric crystal.

The slope of a capacitor's V-Q plot at any point is its instantaneous capacitance at that point. As show in Fig. 1.4, there is a portion of the ferroelectric capacitor's V-Q plot which predicts that it will exhibit negative instantaneous capacitance. This phenomenon has been proposed as a potential way to break the 60 mV/dec limit imposed upon conventional transistors by Boltzmann mechanics [3]-[6].

1.2.2 Application of Ferroelectric Materials for Reduced Subthreshold Slope in NCFETs

The negative capacitance exhibited by ferroelectric capacitors can be exploited for "voltage amplification," by making the voltage across a second capacitor placed in series with a ferroelectric capacitor larger than that applied to the series combination. This voltage amplification can be exploited in the gate stack of a transistor to achieve SS < 60 mV/dec [3]. Consider two capacitors in series, a ferroelectric capacitor and a linear positive capacitor, where the latter will be used to represent the MOSFET gate, as shown in Fig. 1.5.

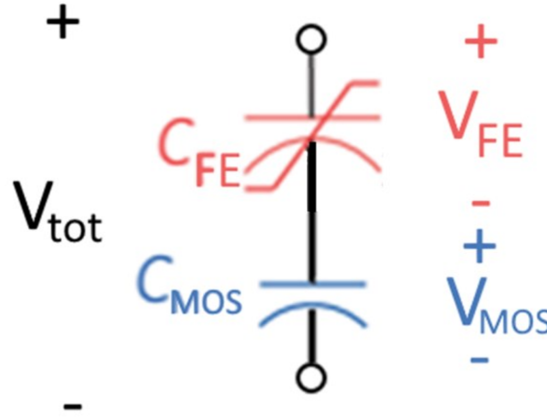

Fig. 1.5. Ferroelectric capacitor C_{FE} and linear positive capacitor C_{MOS} in series.

The voltage across the "MOSFET" capacitor can be found through capacitance division:

$$V_{\mathrm{MOS}} = \frac{C_{\mathrm{MOS}} C_{\mathrm{FE}}}{C_{\mathrm{MOS}} + C_{\mathrm{FE}}} V_{\mathrm{tot}} \tag{1.7}$$

From equation (1.7) we can see that V_{MOS} is greater than V_{tot} when the ratio $C_{\mathrm{MOS}} C_{\mathrm{FE}} / (C_{\mathrm{MOS}} + C_{\mathrm{FE}})$ is greater than 1, which will be true if C_{FE} is negative and $C_{\mathrm{MOS}} < |C_{\mathrm{FE}}|$. By exploiting this "voltage amplification," the SS of a NCFET can be lowered to below 60 mV/dec even though the underlying MOSFET is still constrained by Boltzmann mechanics. The SS of a MOSFET is defined as the incremental gate voltage needed to increase drain current by one decade, as represented by the formula

$$SS_{\mathrm{MOS}} = \frac{\delta V_{\mathrm{MOS}}}{\delta(\log_{10} I)} \tag{1.8}$$

where V_{MOS} is the gate voltage of the MOSFET and I is the drain current. In the case of an NCFET, i.e., a device in which a ferroelectric capacitor has been added in series with the MOSFET gate, the SS can be represented by

$$SS_{\mathrm{NC}} = \frac{\delta V_{\mathrm{tot}}}{\delta(\log_{10} I)} = \frac{\delta V_{\mathrm{tot}}}{\delta V_{\mathrm{MOS}}} \frac{\delta V_{\mathrm{MOS}}}{\delta(\log_{10} I)} = \frac{\delta V_{\mathrm{tot}}}{\delta V_{\mathrm{MOS}}} SS_{\mathrm{MOS}} \tag{1.9}$$

where V_{tot} is the gate voltage of the NCFET, and V_{MOS} now represents the internal node between the ferroelectric capacitor and the MOSFET. Clearly, SS_{NC} can be less than 60 mV/dec even while SS_{MOS} is greater than 60 mV/dec as long as $\frac{\delta V_{\text{tot}}}{\delta V_{\text{MOS}}} < 1$, or in other words, $\frac{\delta V_{\text{MOS}}}{\delta V_{\text{tot}}} > 1$.

An alternative way of representing the benefit of using NCFETs is by looking at the potential energy landscape of the ferroelectric capacitor, the MOSFET, and the NCFET as a function of the charge accumulated on the capacitor plates or the gate, respectively. For this comparison, the MOSFET gate capacitance will again be approximated as a constant and thus the potential energy of the MOSFET gate will simply be the parabolic potential energy of a linear dielectric capacitor. The potential energy of the NCFET gate can be found by simply adding together the potential energy of the ferroelectric capacitor and the MOSFET gate for the same charge.

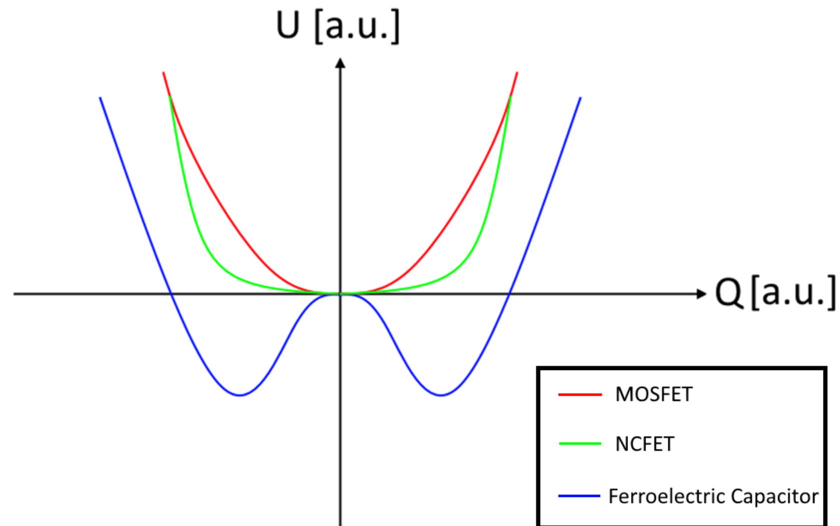

Fig. 1.6. Hypothetical potential energy of a MOSFET gate (red), and a NCFET gate (green), and a ferroelectric capacitor (blue).

As shown in Fig. 1.6, the amount of energy required to push the same amount of charge onto the NCFET gate is lower than that of the MOSFET gate, or alternatively the same amount of energy can push more charge onto the NCFET gate than the MOSFET gate.

1.2.3 Recent Progress

Despite decades of research into ferroelectric materials, whether ferroelectric materials can be applied to FET devices is still unknown. The actual existence of negative capacitance has not been experimentally measured until very recently. As can be seen in Fig. 1.4, in order to measure the full S-shaped curve of the ferroelectric V-Q relation, the voltage applied must be reversed twice within a single traversal of the curve; i.e., in order go from the negatively charged stable state to the positively charged stable state, the voltage applied must be increased to the tip of the ‘S’, then decreased past 0 to the negative tip of the ‘S’, then increased back up to 0 again. Unfortunately, this form of excitation is not practical and instead most experiments can only apply a monotonic signal to the ferroelectric capacitor within the time of a single switch, resulting in a measured curve similar to that shown in Fig. 1.7. This boxy shaped curve is known as the hysteresis curve of the ferroelectric capacitor.

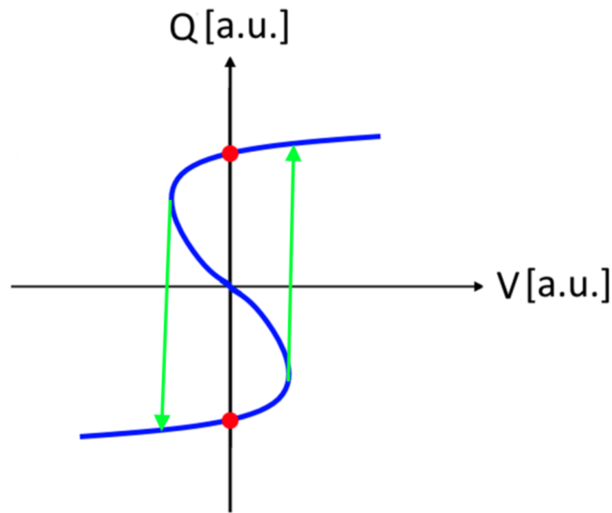

Fig. 1.7. Hypothetical V-Q curve of a ferroelectric capacitor with green arrows representing the path actually traversed in measurement.

The excess voltage provided must then be dissipated by some combination of the dissipative elements within the testing circuit and losses within the ferroelectric capacitor itself. In a landmark 2014 Nature publication, A. Khan et al. experimentally demonstrated for the first-time negative capacitance within a ferroelectric capacitor [11]. They did so by adding a large resistor in series with a ferroelectric capacitor. By calculating the voltage

drop across this large resistor and using it to find the voltage across the ferroelectric capacitor, the study showed a transient portion of the ferroelectric capacitor switching that exhibited negative differential capacitance, where the differential voltage change across the capacitor was negative compared to the differential charge accumulation. However, this study still was not able to measure the S-shaped curve as predicted by the LK equation. More recently in 2018, M.Hoffmann et al. were able to measure a S-shaped curve by applying pulsed signals to reach each point on the curve [12], measuring a scatter plot which nevertheless clearly traced out the expected shape as predicted by the LK model. Though the LK model of the ferroelectric capacitor seems all but confirmed, there has technically still been no experimental measurement of an actual traversal of the S-shaped curve, thus leaving room for improvement in measurement techniques.

In attempting to measure NCFETs with SS < 60 mV/dec, experimental results from NCFETs from Global Foundries have shown reduced (and hence improved) SS compared to standard FETs [13], but they were not able to achieve SS < 60 mV/dec. Other experimental results have shown SS < 60 mV/dec but were achieved with devices having hysteretic current-voltage characteristics [14], which are not suitable for integration into modern chips. Some theories even predict that the fabrication of NCFETs with stabilized negative capacitance is not possible [15]. As understanding of NCFETs continue to improve, the ferroelectric community has shifted from a focus of attaining sub-thermionic (<60 mV/dec at room temperature) SS to simply improving the SS of existing FETs and enhancing on-current [16]. Another shift in focus for ferroelectrics is their use as back-end-of-line (BEOL) elements, which has been flagged as likely being the first commercial use of negative-capacitance ferroelectrics in modern ICs, as recently discussed in DRC 2021 [18].

In addition to the development of NCFETs, ferroelectric materials have been proposed for use in non-volatile non-destructive memory [17]. These ferroelectric FETs (FeFETs) differ from NCFETs because the negative capacitance aspect of the ferroelectric material is not exploited. Instead, the bi-stability of the ferroelectric material is used to store information as a binary bit.

With all the currently known applications of ferroelectric materials in modern devices, the ferroelectric community can benefit greatly from having ways to predict and analyze the potential performance of ferroelectrics for enhancing transistor operations in IC design.

1.3 This Work

This work focuses on using a phenomenological model of ferroelectric materials combined with measurements taken of bulk ferroelectric material to predict the benefit of integrating ferroelectric materials into modern transistors. The specific aims of the research are to utilize numerical models and simulations to accomplish the following tasks:

1. Determine how strongly speed limitations in ferroelectric materials could impact NCFET and FeFET performance.
2. Develop a method for characterization of ferroelectric materials under radio-frequency (RF) excitation to allow extraction of all parameters needed to predict the performance of transistors incorporating ferroelectrics.
3. Investigate new applications of ferroelectric capacitors in RF analog applications using a novel parallel-NCFET (P-NCFET) design and demonstrate an improvement in f_T compared to conventional MOSFETs.

These tasks naturally partition this Ph.D. research into three stages. These three stages are complete and have led to three publications [19], [20], [21], all in *IEEE Transactions on Electron Devices*.

1.4 Overview of Stages

For the convenience of the reader, we have provided below a summary of each of the three stages of work, as well as a description of the key points. Please note that full details are available in later chapters.

1.4.1 Switching-Speed Limitations of Ferroelectric Negative-Capacitance Field-Effect Transistors

Summary:

Negative-capacitance field-effect transistors (NCFETs) have been proposed to reduce power consumption in modern aggressively scaled devices. Although negative capacitance phenomena have been studied in various forms [22]-[28], the idea to use ferroelectric materials to create NCFETs, in which voltage amplification from negative capacitance is utilized to realize SS < 60 mV/dec, came to prominence only very recently as a result of the work of Salahuddin and Datta [3]. As a result, all experimental work done until this study on NCFETs only considered static (dc) device behavior, rather than dynamic (transient switching) behavior. The goal of this study is to predict potential NCFET speed limitations using a numerical simulation where the ferroelectric material is calibrated to transient measurements of the bulk material.

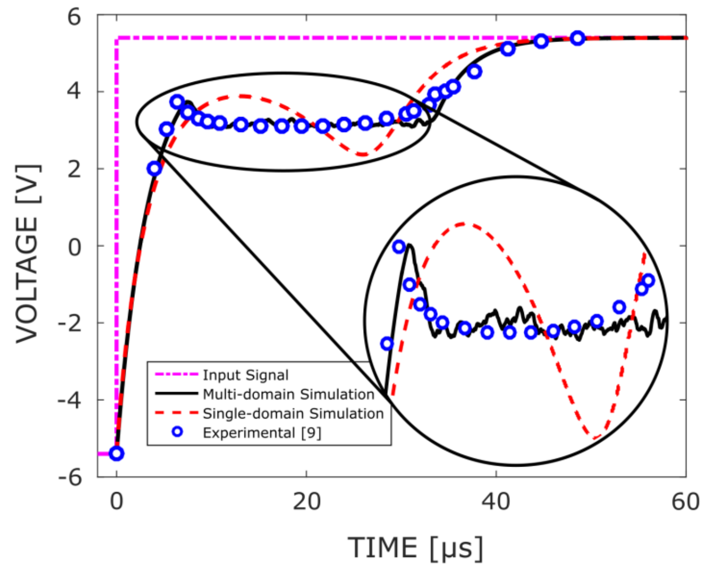

Fig. 1.8. Validation of our simulation methodology via a comparison with the experimental curves in [11]. Circles show experimentally measured values for the voltage v_{FE} across the ferroelectric capacitor. Solid line shows the result of our modified equation, which exhibits a strong match to experiment. Dashed line shows the result of an unmodified equation. The input voltage is also shown as a dash-dotted line.

The ferroelectric model we use is the Landau-Khalatnikov (LK) equation [9], [10] used to describe the bulk ferroelectric material, which has been modified to account for non-uniform polarization:

$$\rho \frac{dP_i(t)}{dt} = \frac{v_{\text{FE}}(t)}{t_{\text{FE}}} + k\left[\sum_j \left(P_j(t) - P_i(t)\right)\right] - 2\alpha_i P_i(t) - 4\beta_i P_i^{\,3}(t) - 6\gamma_i P_i^{\,5}(t) \tag{1.10}$$

where we discretize the ferroelectric oxide into a square lattice and consider the area A_i centered around each lattice point i to have a uniform polarization $P_i(t)$. k is the interaction factor that describes the strength of the coupling between nearest neighbor lattice points, and the sum over j is the sum over all neighbors of i. α_i, β_i, and γ_i are the distinct Landau parameters assigned to each lattice point i. The parameters in (1.10) are found by fitting it to experimental results [11]. Fig. 1.8 shows both the close agreement to measurement of (1.10) [shown by the solid line], as well as the vast improvement (1.10) has over the unmodified equation [shown by the dashed line].

After the ferroelectric material parameters have been correctly calibrated, we model a digital inverter-inverter configuration at the 28-nm node to obtain an understanding of the impact of ferroelectric materials in high-speed digital circuits. Each MOSFET is enhanced by a ferroelectric capacitor in series with its gate, the combination thus yielding an NCFET, as depicted in Fig. 1.9. The ferroelectric capacitor has dimensions $t_{\text{FE}} = 6$ nm and $A = 90$ nm^2. The conventional NMOS and PMOS transistors are modeled as voltage-dependent gate capacitances $C_{\text{GS}}(v_{\text{GS}}, v_{\text{DS}},)$ and $C_{\text{DS}}(v_{\text{GS}}, v_{\text{DS}},)$, combined with a voltage-dependent current source $i_{\text{DS}}(v_{\text{GS}}, v_{\text{DS}},)$, where $v_{\text{GS}}(t)$ and $v_{\text{DS}}(t)$ are the gate-source and drain-source voltages, respectively, both dependent on time t. Both NMOS devices have gate dimensions of 30 nm × 30 nm. The PMOS devices have double the channel width as the NMOS devices, with dimensions of 60 nm × 30 nm, in order to reach a similar on current of approximately 20 μA as the NMOS devices. The supply voltage V_{DD} is taken to be 1 V. We consider the transient behavior of this inverter pair at frequencies varying from 5 MHz to 500 MHz.

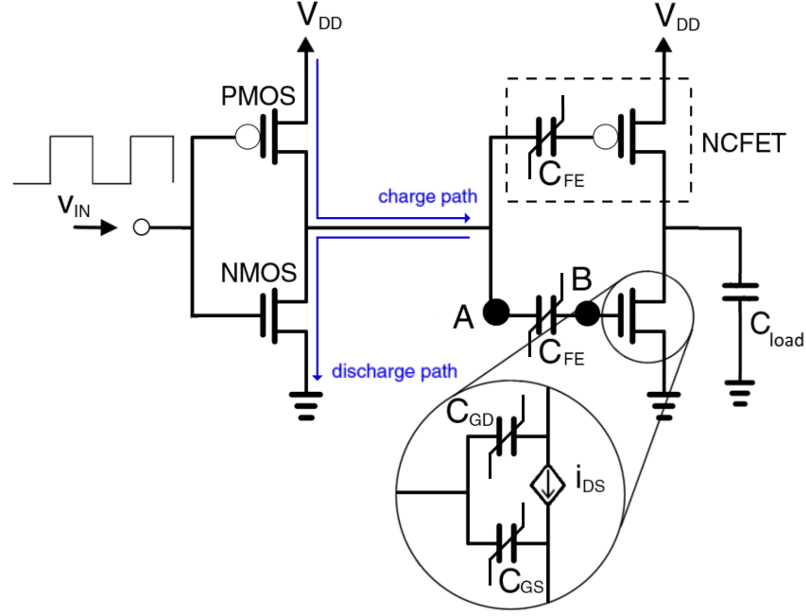

Fig. 1.9. The simulation set-up corresponding to a high-speed digital inverter-inverter model.

The reduction in NCFET performance at high frequencies is illustrated explicitly in Fig. 1.10. As shown, the voltage amplification, defined as the peak voltage at node B divided by the peak voltage at node A in Fig. 1.9, steadily decreases as the frequency increases. It is worth adding that at very high frequencies, the insertion of the ferroelectric material can lead to an attenuation of the voltage at B with respect to A.

This analysis was performed on a specific ferroelectric material and there is no obvious extension to other ferroelectric materials. However, using (1.10) with simple approximations for an NCFET, as explained in Chapter 2 and Appendix A, we can calculate the minimum possible rise time required to achieve voltage amplification to be

$$\tau_{\text{min}} = \frac{\rho t_{\text{FE}}}{2}\left(\frac{C_{\text{MOS}}}{A}\right) \tag{1.11}$$

where C_{MOS} is the gate capacitance of the MOSFET without the ferroelectric oxide. The rise time for the inverter-inverter circuit in Fig. 1.9 using usual MOSFETs is approximately $\tau_{\text{min}} = 1$ ps, i.e., the rise time representative of modern and future processors working in the GHz to THz range. From (1.11), an upper bound on the minimum ρ required for a particular ferroelectric material to achieve this value of rise time with NCFETs is 0.1 Ω·m.

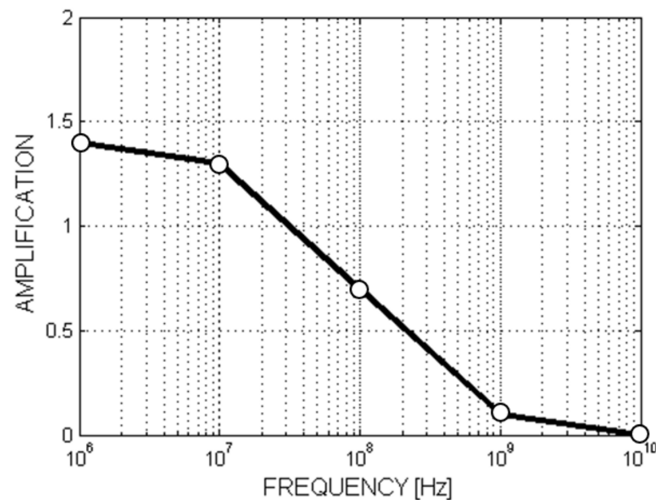

Fig. 1.10. Dependence of voltage amplification in the circuit of Fig. 1.9 on frequency, as described in the text.

Key Points:

The specific contributions from the first stage, "Switching-Speed Limitations of Ferroelectric Negative-Capacitance Field-Effect Transistors," are summarized as follows:

1. Current studies on NCFETs focus on static measurements of subthreshold slope. We have identified an additional parameter ρ that strongly influences the high-frequency response of ferroelectric materials.
2. Our transient switching simulation results show that while ferroelectrics do have the potential to provide voltage amplification and hence an enhanced response to gate voltages in the MHz range, they will cease to provide this advantage in the GHz to THz range.
3. Ferroelectric materials must have a viscosity coefficient ρ less than 0.1 $\Omega\cdot$m to achieve voltage amplification with a 1-ps rise time.

1.4.2 Toward Microwave S- and X-Parameter Approaches for the Characterization of Ferroelectrics for Applications in FeFETs and NCFETs

Summary:

As applications of ferroelectrics continue to be proposed, such as in memory [29], [30], including non-destructive non-volatile memory utilizing FeFETs [31], and negative differential resistance FETs [32], the search to identify the best ferroelectrics and the best material composition for all these emerging devices continues to be a topic of great interest. Measurement approaches to facilitate such identification are highly desirable to move the related technologies toward realization. While the previous study extracted a value for ρ by fitting (1.10) to experiment, this value, of course, cannot be extended to all ferroelectrics. In addition, common ferroelectric characterization techniques such as using the Sawyer-Tower (ST) circuit [33], [34], are heavily impacted by non-idealities such as parasitics from cabling and oscilloscope probes [35], [36]. In particular, extraction of the loss parameter ρ will depend on unknown parasitics [36]. In this study, we offer "X-parameters" and "S-parameters" as two frequency-domain electrical alternatives to conventional time-domain electrical measurement approaches to accurately de-embed the parasitics and reveal the intrinsic ferroelectric behavior, from which the LK parameters can then be reliably extracted. S-parameters are well known in microwave approaches [37]. X-parameters are a large-signal generalization of S-parameters, with the distinction being that S-parameters are limited to purely linear networks whereas X-parameters can be used to characterize *non*linear networks [38], [39]. X-parameters also offer the ability to measure systems with memory, which is especially applicable to the ferroelectric response [40].

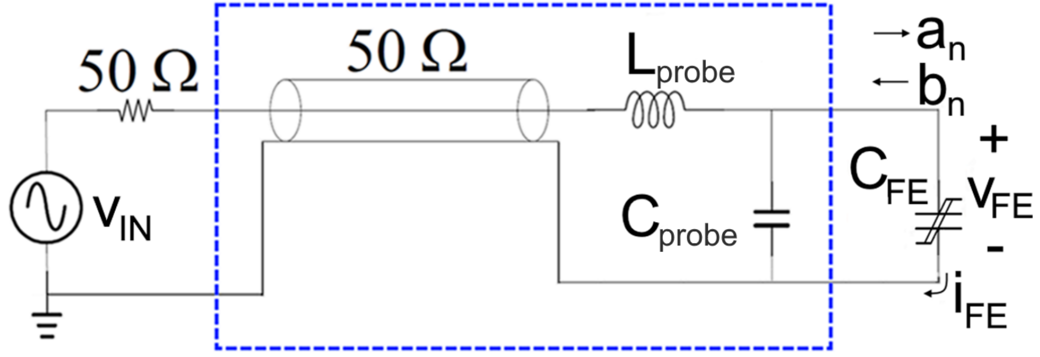

Fig. 1.11. Proposed X-parameter test circuit to measure ferroelectric parameters and switching speed at high frequencies. The boxed subcircuit shows the cabling and parasitics, all of which comprise a linear network that can be de-embedded to accurately isolate the required signals around the ferroelectric at the fundamental (driving) and harmonic frequencies.

Fig. 1.11 shows a model of the test circuit with cabling and parasitics used to simulate a realistic ferroelectric measurement with X-parameters. The ferroelectric is driven by a large-signal sinusoidal source v_{IN} at a fundamental frequency ω_0, and the incident and reflected power waves a_n and b_n around the ferroelectric are determined at all harmonic frequencies $n\omega_0$, where $n = 1$ corresponds to the fundamental, and where the harmonics for $n \neq 1$ result from the highly nonlinear nature of ferroelectric switching. In doing so, we assume the passive network of cable and contact parasitics (shown boxed in Fig. 1.11) that couples the source to the ferroelectric capacitor remains linear even with a large input signal, so that standard calibration methods [37] involving open, short, and through loads (in place of the ferroelectric) can be used to de-embed this network at the fundamental and all harmonic frequencies of interest, thus enabling the accurate determination of a_n and b_n for all n. The voltage and current harmonics can be converted to time-dependent waveforms using Fourier series:

$$v_{\mathrm{FE}}(t) = \sum_{n=1}^{N} v_n \cos\left(n\omega_0 t + \phi_{v,n}\right) \tag{1.12a}$$

$$i_{\mathrm{FE}}(t) = \sum_{n=1}^{N} i_n \cos\left(n\omega_0 t + \phi_{i,n}\right) \tag{1.12b}$$

where N is the highest harmonic that can be accurately measured, t is time, $v_{\mathrm{FE}}(t)$ is the

voltage across the ferroelectric, and $i_{\mathrm{FE}}(t)$ is the current through the ferroelectric. These waveforms can then be used to systematically extract the LK parameters.

To illustrate the merit of our proposed X-parameter approach, we have simulated the X-parameter measurement and the resultant waveforms are plotted in Fig. 1.12. We use Si-doped HfO_2 for the ferroelectric capacitor C_{FE}, and we presume a surface area of $A = 1000$ nm × 1000 nm, discretized into a 100 by 100 lattice, and a thickness of $t_{\mathrm{FE}} = 10$ nm. For regular lattice sites, we assign values of the lossless parameters $\alpha(\mathbf{r})$, $\beta(\mathbf{r})$, and $\gamma(\mathbf{r})$ to be those extracted from a fit of experimental results [41], and the loss parameter ρ is set to 1.8 mΩ·m [42]. To model multidomain effects, we add defect sites to the ferroelectric by assigning parameter values $\alpha(\mathbf{r})$, $\beta(\mathbf{r})$, and $\gamma(\mathbf{r})$ at random lattice points so that they must stay in one of the two stable states without any possibility of switching. We assume values of parasitic inductance and capacitance $L_{\mathrm{probe}} = 50$ pH and $C_{\mathrm{probe}} = 50$ fF.

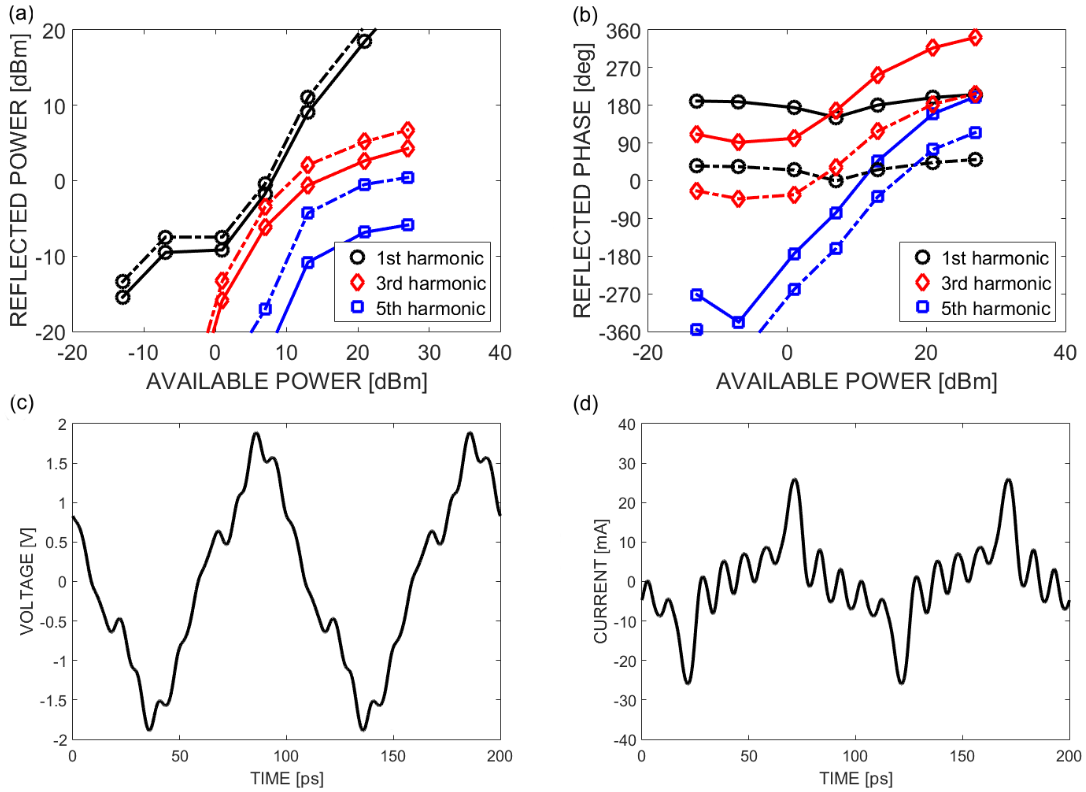

Fig. 1.12. Reflected power b_{n} and time-domain waveforms $v_{\mathrm{FE}}(t)$ and $i_{\mathrm{FE}}(t)$ for the circuit in Fig. 1.11, found using the X-parameter approach described in the text. (a) Magnitude of the first three odd harmonics of b_n before calibration (solid lines) and after calibration (dashed lines); (b) phase of the first three odd harmonics of b_n before calibration (solid lines) and after calibration (dashed lines); (c) voltage waveform $v_{\mathrm{FE}}(t)$; (d) current waveform $i_{\mathrm{FE}}(t)$.

The variable ρ can be extracted from the simulated measurement by noting that, at steady state and over an entire period T, the ferroelectric returns to its initial potential energy. Thus, the variable ρ which parameterizes the power loss of the ferroelectric material can be found by equating the energy supplied to the energy dissipated by the ferroelectric. Values for the parameters α, β, and γ can be extracted using a chi-squared polynomial regression of order five to fit a parameterized plot of $v_{\mathrm{FE}}(t)$ and $q_{\mathrm{FE}}(t)$, where $q_{\mathrm{FE}}(t)$ is the charge on the ferroelectric capacitor plates and is found by integrating $i_{\mathrm{FE}}(t)$. Once the other variables are known, k can then be found from the measured current and voltage through the use of a self-consistent numerical solution. A detailed accounting of the mathematical formulae required to extract these parameters are presented in Chapter 3.

Table 1.1 summarizes the extracted and expected values of ferroelectric parameters from our suggested extraction procedure. To further simulate realistic measurement uncertainties, the extracted values were obtained assuming the calibration had an error of 0.2 dB, and only harmonics within 40 dB of the fundamental were used to plot the $P(t)$ vs. $E(t)$ hysteresis curve. As shown, there is good agreement even with the assumed uncertainties, demonstrating the viability of our approach, i.e., the use of harmonic (X-parameter) information available from the switching of a ferroelectric to first find the de-embedded $P(t)$ vs. $E(t)$ curve, and to then use that curve to systematically isolate its LK parameters.

TABLE 1.1
ASSIGNED VS. EXTRACTED FERROELECTRIC PARAMETERS

Parameter	Assigned	Extracted
ρ	1.80 mΩ·m	2.20 mΩ·m
α	-3.60×10^{8} V·m/C	-3.18×10^{8} V·m/C
β	2.25×10^{10} V·m^5/C^3	2.29×10^{10} V·m^5/C^3
γ	1.67×10^{9} V·m^9/C^5	1.05×10^{9} V·m^9/C^5
k	3.00×10^{-8} V·m^3/C	3.60×10^{-8} V·m^3/C

For the specific case of characterizing ferroelectrics in NCFETs targeted for low-power logic applications, a highly simplified S-parameter approach can be used. This method

retains the advantage of de-embedding techniques inherent to frequency-domain measurements but requires a balanced ferroelectric-dielectric capacitor stack that is hysteresis free; such a balanced stack emulates the gate of an NCFET [3], with the linear capacitor replacing the gate capacitance of the MOSFET.

In a balanced structure, the ferroelectric stabilizes in the middle of the two spontaneous polarizations [3]. Upon application of a small-signal voltage, the stack can hence be expected to behave as shown in Fig. 1.13, where the boxed portion shows a first-order representation of the ferroelectric based on a linearization of the LK equation, with $C_N = A/2\alpha t_{\mathrm{FE}}$ representing the small-signal negative capacitance of the ferroelectric and C_{DE} representing the series dielectric. As shown in Table 1.2, the extraction correctly reveals the expected (assigned) values.

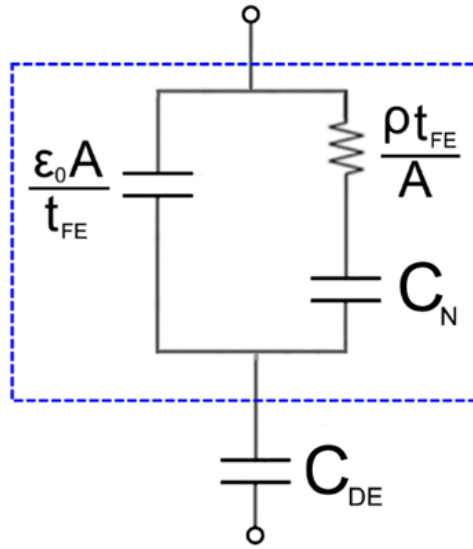

Fig. 1.13. Equivalent circuit model of a ferroelectric capacitor in series with a linear capacitor in a balanced capacitor stack. The boxed subcircuit is the circuit representation of the ferroelectric, found by linearizing the LK equation.

TABLE 1.2
ASSIGNED VS. EXTRACTED FERROELECTRIC PARAMETERS

Parameter	Assigned	Extracted
ρ	1.80 mΩ·m	1.93 mΩ·m
α	-3.60 × 10^8 V·m/C	-3.70 × 10^8 V·m/C

Key Points:

The specific contributions from the second stage, "Toward Microwave S- and X-Parameter Approaches for the Characterization of Ferroelectrics for Applications in FeFETs and NCFETs," are summarized as follows

1. The large-signal X-parameter technique, in which a ferroelectric is excited by a large input sinusoid and the resulting harmonics from the highly nonlinear ferroelectric switching are measured, can be used to trace the intrinsic polarization vs. electric-field curve for the ferroelectric, from which all the LK parameters can be derived; these include the lossless LK parameters, α, β, and γ, and the loss parameter ρ.
2. The viability of the X-parameter approach is demonstrated through simulations of a measurement setup. The suggested procedure to extract values for the LK parameters from the simulated measurement data yields results that closely match the expected values.
3. A simplified small-signal S-parameter approach using a balanced capacitor stack to emulate the gate structure of an NCFET targeted for low-power logic applications can be used to extract the loss parameter ρ and the lossless parameter α, but cannot reveal the other LK parameters.

1.4.3 Feedback Stabilization of a Negative-Capacitance Ferroelectric and its Application to Improve the f_T of a MOSFET

Summary:

In this study, we propose a *parallel* NCFET structure (P-NCFET) that reduces the input capacitance and consequently achieves higher unity-current-gain frequency f_T in comparison to a conventional MOSFET. This increase in f_T makes the P-NCFET an attractive choice for application in RF integrated circuits. The key to our approach is the use of active feedback in addition to capacitance matching to stably hold the ferroelectric in its negative-capacitance regime, and thus achieve the capacitance cancellation required to reduce the input capacitance.

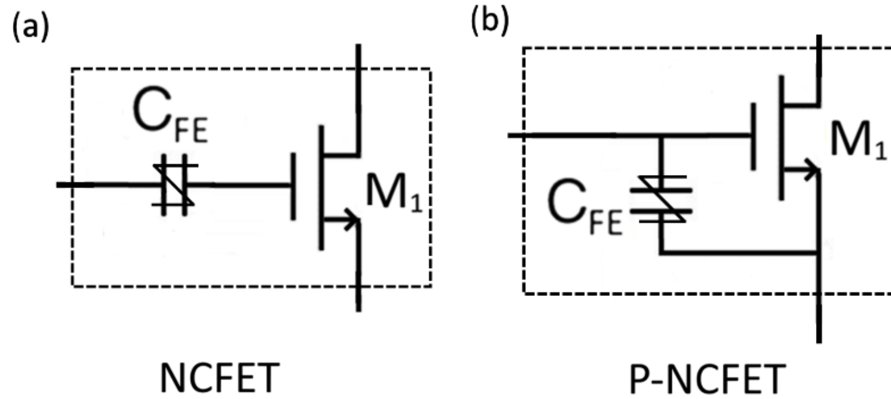

Fig. 1.14. (a) NCFET vs. (b) proposed P-NCFET.

A comparison of a P-NCFET with a conventional NCFET is shown in Fig. 1.14. The proposed P-NCFET structure in Fig. 1.14(b) has a lower gate-source capacitance than the MOSFET M_1 due to partial cancellation of the gate capacitance of M_1 by the parallel negative capacitance of the ferroelectric. The NCFET with the *series* ferroelectric is balanced by the gate capacitance of the MOSFET; however, the proposed P-NCFET structure with the ferroelectric in *parallel* with the gate and source terminals of the MOSFET is inherently unstable [43]. We thus propose a simple feedback technique to stabilize the P-NCFET structure, and demonstrate the stability using Nyquist criteria.

Fig. 1.15(a) shows a simple current mirror used to bias a conventional MOSFET, where two extra resistors R_1 and R_2 are shown, and in Fig. 1.15(b), the mirror of Fig. 1.15(a) has been redrawn to show it can be viewed from a feedback perspective, with the gate-source capacitances C_{gs1} and C_{gs2} of M_1 and M_2, respectively, shown outside the devices themselves, where for ease of the present discussion, C_{gs} is the only component of gate capacitance considered for each MOSFET. In Fig. 1.15(b), the low-pass filtering action of C_{gs2} and C_{gs1} with R_2 and R_1, respectively, can be seen to block a high-frequency ac signal v_{sig} applied at the gate of M_1 from circulating in the feedback loop.

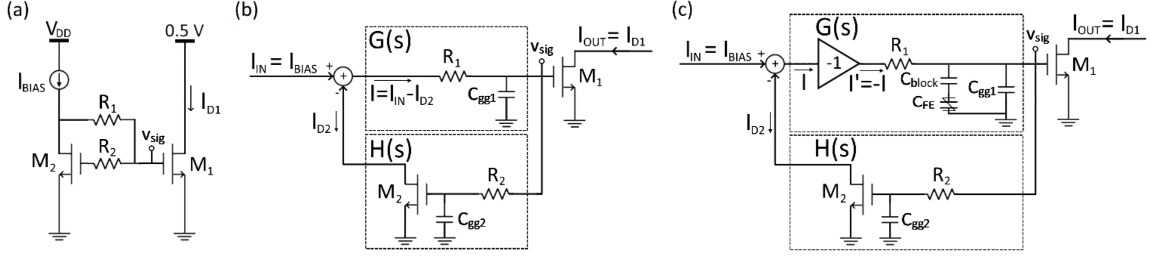

Fig. 1.15. (a) Biasing of a MOSFET M_1 using a current mirror. (b) Negative-feedback visualization of the biasing scheme in (a). (c) Biasing of a P-NCFET using the approach of (b) but with the addition of a negative unity-gain current amplifier for proper polarity.

Fig. 1.15(c) shows the configuration when M_1 is replaced by a P-NCFET consisting of M_1 in parallel with a ferroelectric offering a capacitance C_{FE}, but where a large blocking capacitor C_{block} is added in series with C_{FE} to maintain dc separation between the gate of M_1 and the ferroelectric, and noting the ferroelectric must be biased at 0 V to realize a negative value for C_{FE} while M_1 must be biased in saturation with V_{GS1}~0.5 V. The feedback operation is the same as for the circuit of Fig. 1.15(b), except a negative unity-gain current amplifier ($I' = -I$) is required in the feedback path since the gate capacitance of the P-NCFET $C_{\text{FE}} + C_{\text{gs1}}$ is designed to be *negative* for stable operation, thus requiring the opposite polarity of net restorative charge.

A circuit realization of the feedback stabilization approach of Fig. 1.15(c) is shown in Fig. 1.16, where the current mirror formed by identically sized M_3 and M_4 implements the negative unity-gain current amplifier. The main transistor M_1 was chosen to have a gate length $L = 60$ nm and a gate width $W = 3.3$ µm per finger × 30 fingers, with the latter chosen so that 10 mA of drain current corresponds to a gate-source voltage of ~0.5 V and a drain-source voltage of 0.5 V for a rated supply voltage of 1V. With these design parameters, the gate-source capacitance of M_1 is $C_{\text{gs1}} \approx 60$ fF. The ferroelectric has an area $A_{\text{FE}} = 0.9$ µm^2 and a thickness $t_{\text{FE}} = 10$ nm, resulting in an approximate capacitance $C_{\text{FE}} \approx -130$ fF in the zero-polarization state. The other elements are chosen to minimize parasitic loading and minimize impact on the high-frequency operation of the P-NCFET, and to maintain feedback stability as explained below.

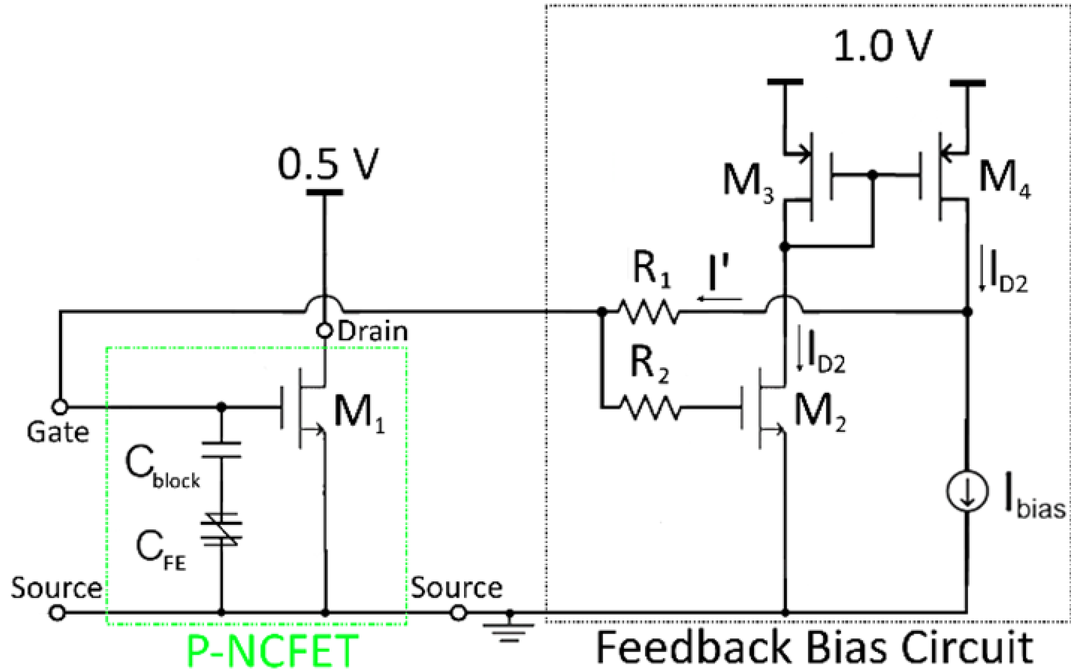

Fig. 1.16. Circuit implementation of the approach illustrated in Fig. 1.15(c). The current mirror formed by identically sized M_3 and M_4 implements the negative unity-gain current amplifier. The labeled gate and source on the left on the left of M_1, and drain and source above and to the right of M_1, indicate the usual small-signal input and output ports, respectively, of the P-NCFET.

It is well-known that a feedback system is stable if the *closed-loop* transfer function has no right half-plane (RHP) poles, and that by the Nyquist criterion, the number of RHP poles in the closed-loop transfer function equals $P_{\text{GH}} - N_{\text{CCW}}$, where P_{GH} is the number of RHP poles in the *open-loop* transfer function and N_{CCW} is the number of counterclockwise encirclements of -1 in the Nyquist plot, where the latter plot is a locus of the *open-loop* transfer function in the complex plane as the frequency is swept [44]. A simplified expression for the open-loop transfer function of the P-NCFET feedback circuit in Fig. 1.16 can be found by making a few assumptions consistent with the final circuit design goals. The negative unity-gain current amplifier implemented by the current mirror formed by M_3 and M_4 can be assumed to have infinite bandwidth and a gain of exactly one. We also assume the poles in the open-loop transfer function are significantly separated, by approximating R_1 as much larger than both R_2 and the output resistance r_{o4} of M_4. With these approximations, the open-loop transfer function from Fig. 1.16 can be expressed as

$$G(s)H(s) = \frac{-g_{m2}r_{o4}}{[1 + sR_1(C_{\text{gs1}} + C_{\text{FE}})][1 + sR_2C_{\text{gs2}}][1 + sr_{\text{o4}}C_{\text{d4}}]} \quad (1.13)$$

where $G(s)$ is the transfer function of the forward block [shown explicitly in Fig. 1.15(c)], $H(s)$ is the transfer function of the feedback block, $C_{\text{gs1}} + C_{\text{FE}}$ is the equivalent gate-source capacitance of the P-NCFET, with values chosen such that the total capacitance is negative, and $g_{\text{m}i}$, r_{oi}, $C_{\text{gs}i}$, and $C_{\text{d}i}$ are the transconductance, output resistance, gate-source capacitance, and total drain capacitance of the i-th transistor M_i, respectively.

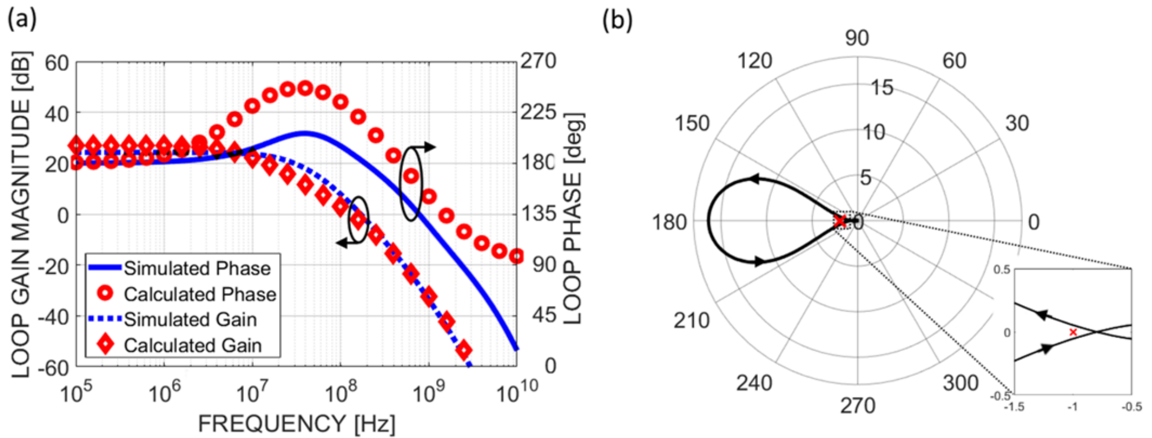

Fig. 1.17. (a) Magnitude and phase of the open-loop transfer function for the feedback stabilized P-NCFET circuit, calculated from (1.13) and from full circuit simulation. (b) Nyquist plot of the open-loop transfer function with 'x' denoting the -1 point. The inset shows a zoomed view around the -1 point. The Nyquist plot makes a single counterclockwise encirclement around -1.

Fig. 1.17(a) shows a bode plot of the open-loop transfer function from full simulation of the feedback circuit in Fig. 1.16. The bode plot shows a 20 dB/dec drop in magnitude around 10 MHz accompanied by a $+45°/\text{dec}$ phase shift over 2 decades, which confirms the presence of a single RHP pole, i.e., $P_{\text{GH}} = 1$, as expected from (1.13). Fig. 1.17(b) shows a Nyquist plot of the same open-loop transfer function which has one counterclockwise encirclement of -1, i.e., $N_{\text{CCW}} = 1$, also as expected from (1.13). Therefore, $P_{\text{GH}} - N_{\text{CCW}} = 0$ and the feedback circuit of Fig. 1.16, as implemented, is indeed stable.

As already discussed, a negative ferroelectric capacitance C_{FE} is used to partially cancel the gate capacitance of M_1 in Fig. 1.16, reducing the input capacitance applicable to the P-

NCFET and hence increasing its f_T in comparison to that of the conventional MOSFET M_1. Since the gate of the P-NCFET is also the gate of M_1, the transconductance of the P-NCFET is equal to that of M_1. If the gate capacitance is the only parasitic determining f_T, then the expected improvement can be expressed as

$$f_{\mathrm{T,P-NCFET}} \approx \left|\frac{g_{\mathrm{m1}}}{2\pi(C_{\mathrm{gg1}} + C_{\mathrm{FE}})}\right| = \left|\frac{C_{\mathrm{gg1}}}{C_{\mathrm{gg1}} + C_{\mathrm{FE}}}\right| f_{\mathrm{T,MOS}} \tag{1.14}$$

where g_{m1} is the transconductance of M_1 and the P-NCFET, $f_{\mathrm{T,P-NCFET}}$ is the unity-current-gain frequency of the P-NCFET, and $f_{\mathrm{T,MOS}}$ is the unity-current-gain frequency of the MOSFET. The design parameters of M_1 yield a gate capacitance $C_{\mathrm{gg1}} \approx 85$ fF and the size of the ferroelectric was chosen so that $C_{\mathrm{FE}} \approx -130$ fF, which was done to achieve a reduction of approximately 50% in gate capacitance. From (1.14), the maximum f_T improvement of the P-NCFET over the MOSFET M_1 in our circuit of Fig. 1.16 is thus a factor of approximately two.

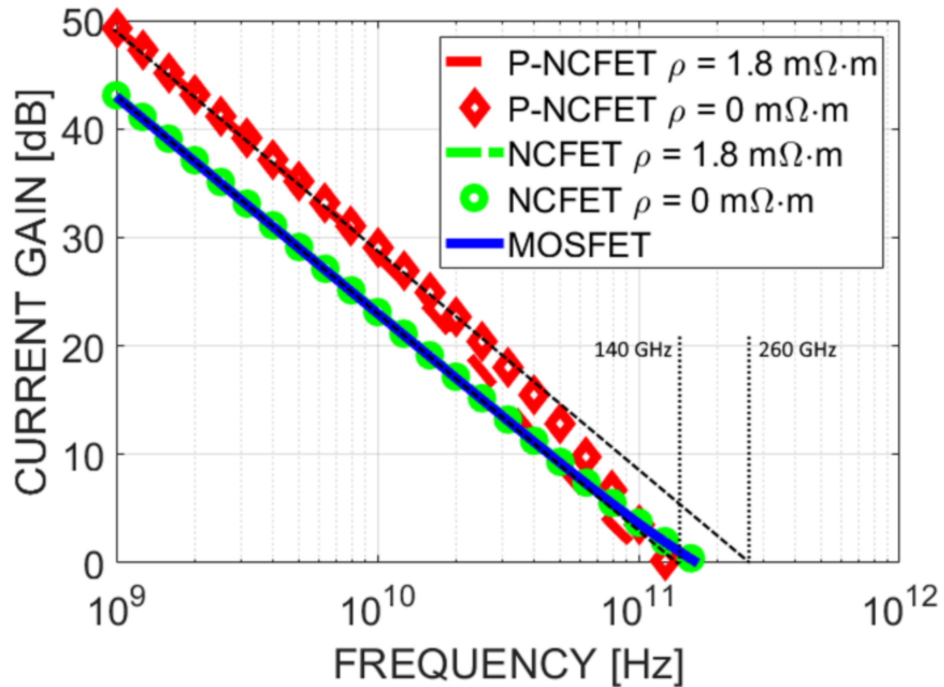

Fig. 1.18. Simulated current gain of the P-NCFET, the NCFET, and the standard MOSFET. All devices are biased at 10 mA of drain current. The current gain of the NCFET is identical to the standard MOSFET, as expected.

The magnitude of the short-circuit current gain $|h_{21}|$ is extracted for all devices, with the result displayed in Fig. 1.18. The extrapolated f_T of the P-NCFET is 260 GHz, approximately double that of the conventional MOSFET at 140 GHz, an outcome of the implemented capacitance cancellation, while the f_T values of the NCFET and MOSFET are identical, all independent of ρ, as expected.

Key Points:

The specific contributions from the third stage, "Feedback Stabilization of a Negative-Capacitance Ferroelectric and its Application to Improve the f_T of a MOSFET," are summarized as follows

1. Instead of a conventional series configuration used in an NCFET, a ferroelectric can be placed in *parallel* with the usual gate capacitance of a MOSFET, yielding a new P-NCFET structure [Fig. 1.14]. The sum of the negative capacitance and traditional MOSFET gate capacitance is lower in magnitude than that of the MOSFET itself, offering the possibility of improved high-frequency performance and demonstrating the idea of capacitance cancellation.
2. For the capacitance cancellation to work, an active feedback circuit is designed to stabilize the ferroelectric in its negative-capacitance region [Fig. 1.15(c) and Fig. 1.16], and the stability of the feedback circuit is demonstrated through classical stability analysis and the Nyquist criterion [Fig. 1.17].
3. The short-circuit current gain of the biased and stabilized P-NCFET viewed as a two-port vs. that of the traditional MOSFET show that the extrapolated f_T for the P-NCFET is significantly higher than that for the traditional MOSFET [Fig. 1.18].

Chapter 2

Switching-Speed Limitations of Ferroelectric Negative-Capacitance Field-Effect Transistors[1]

2.1 Introduction

As Moore's law continues and transistors scale to ever-smaller dimensions, the electronics industry is becoming increasingly concerned with managing the power density in large digital chips [1], [2]. One way to reduce this power density is to use transistors with a steep slope, i.e., a low subthreshold swing (SS). However, conventional transistors are fundamentally limited to SS ≥ 60 mV/dec by Boltzmann mechanics. Recently, the exploitation of ferroelectric materials has gained much attention as a potential way to break this 60 mV/dec limit [3]-[6].

In ferroelectric materials, the crystal lattice is stable at a state that exhibits a spontaneous polarization, which can be flipped by applying an electric field to deform the crystal to the opposite state [7], [8]. A capacitor made with such a ferroelectric material can exhibit "negative capacitance," where the stored charge in a stable state is negative with respect to the applied voltage. Such negative capacitance can be exploited for "voltage amplification," by making the voltage across a second capacitor placed in series with a ferroelectric larger than that applied to the series combination. This voltage amplification can be exploited in the gate stack of a transistor in order to achieve SS < 60 mV/dec [3].

[1] A version of this chapter has been published [17].

Although negative-capacitance phenomena have been studied in various forms [22]-[28], the idea to use ferroelectrics to create "negative-capacitance field-effect transistors" (NCFETs), in which voltage amplification from negative capacitance is utilized to realize SS < 60 mV/dec, came to prominence only very recently, as a result of the work of Salahuddin and Datta [3]. Subsequently, negative capacitance in lead zirconium titanate (PZT) was experimentally validated [11], and soon thereafter, NCFETs using ferroelectrics were demonstrated experimentally [14], [39], [46], with SS values of 42 mV/dec [45] and 8.5 mV/dec [14]. However, all experimental work done thus far on NCFETs has considered only static (dc) device behavior, rather than dynamic (transient switching) behavior. While a few studies have experimentally measured the transient response of isolated ferroelectric capacitors [11], [47], the dynamic response of NCFETs incorporating ferroelectrics thus remains relatively unexplored, especially for operation at frequencies relevant in present-day, high-speed digital electronics.

In this study, we present a multi-domain simulation methodology based on the Landau-Khalatnikov equation to probe the dynamic behavior of NCFETs. With the parameters of the ferroelectric material calibrated to the experimental data presented in [11], we simulate a digital inverter-inverter configuration and show that, given the ferroelectric materials currently known, NCFETs may lose their advantage over conventional FETs when operating at frequencies in the GHz range.

2.2 Methodology

2.2.1 Simulated Circuits

We perform two switching simulations in order to investigate the ferroelectric described in section 2.2.2. The first set-up, depicted in Fig. 2.1, emulates the experimental measurement in [11]. An input voltage source v_{IN} stepping between -5.4 V and +5.4 V, with a period of 120 μs, is placed in series with a 50-kΩ resistor and a ferroelectric (thickness t_{FE}= 60 nm and area A = 30 μm × 30 μm). An oscilloscope, represented as a 60-pF capacitor C_{OSC}, appears in parallel with the ferroelectric capacitor C_{FE}.

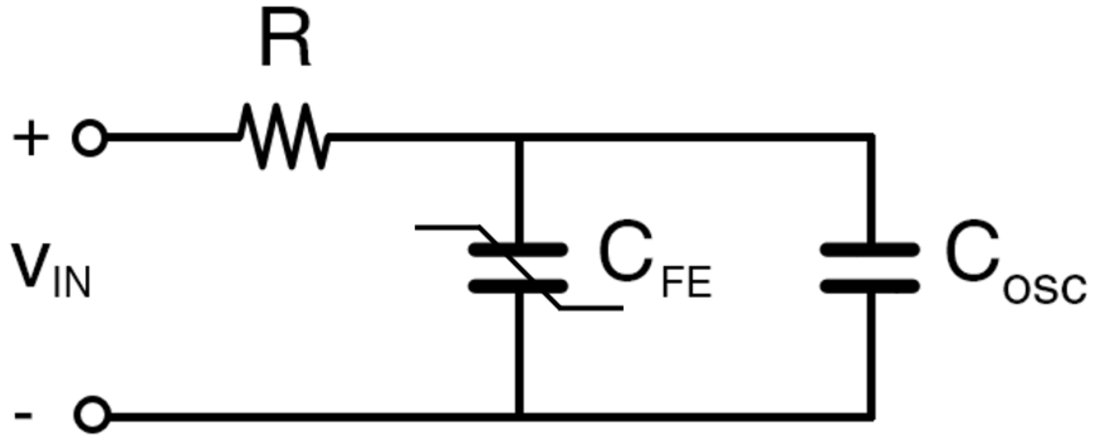

Fig. 2.1. The first simulation set-up, corresponding to the experimental measurement in [11].

The second set-up, shown in Fig. 2.2, is constructed to obtain an understanding of the impact of ferroelectrics in high-speed digital circuits. We model a digital inverter-inverter configuration at the 28-nm node, with each MOSFET enhanced by a ferroelectric capacitor in series with its gate, the combination thus yielding an NCFET, as depicted in Fig. 2.2. Here, the ferroelectric capacitor has dimensions t_{FE} = 6 nm and A = 90 nm^2, with the thickness and area chosen for capacitance matching with the MOSFET in order to maximize voltage amplification [3], [48]. The conventional NMOS and PMOS transistors are modeled as voltage-dependent gate capacitances $C_{\mathrm{GS}}(v_{\mathrm{GS}}, v_{\mathrm{DS}},)$ and $C_{\mathrm{DS}}(v_{\mathrm{GS}}, v_{\mathrm{DS}},)$, combined with a voltage-dependent current source $i_{\mathrm{DS}}(v_{\mathrm{GS}}, v_{\mathrm{DS}},)$, where $v_{\mathrm{GS}}(t)$ and $v_{\mathrm{DS}}(t)$ are the gate-source and drain-source voltages, respectively, both dependent on time t. The voltage dependencies, shown in Fig. 2.3, were determined using Cadence Spectre simulations [44]. Both NMOS devices have gate dimensions of 30 nm × 30 nm. The PMOS devices have double the channel width as the NMOS devices, with dimensions of 60 nm × 30 nm, in order to reach a similar on current as the NMOS devices of approximately 20 μA. The supply voltage V_{DD} is taken to be 1 V. We consider the transient behavior of this inverter pair at frequencies varying from 5 MHz to 500 MHz. In the first half of the cycle, the input to the second stage charges to V_{DD} through the PMOS of the first inverter, while in the second half of the cycle, it discharges to ground through the NMOS of the first inverter. In both cases, we use the voltage-dependent current and capacitance data obtained from Cadence Spectre [49], shown in Fig. 2.3, to determine the circuit response through numerical simulation.

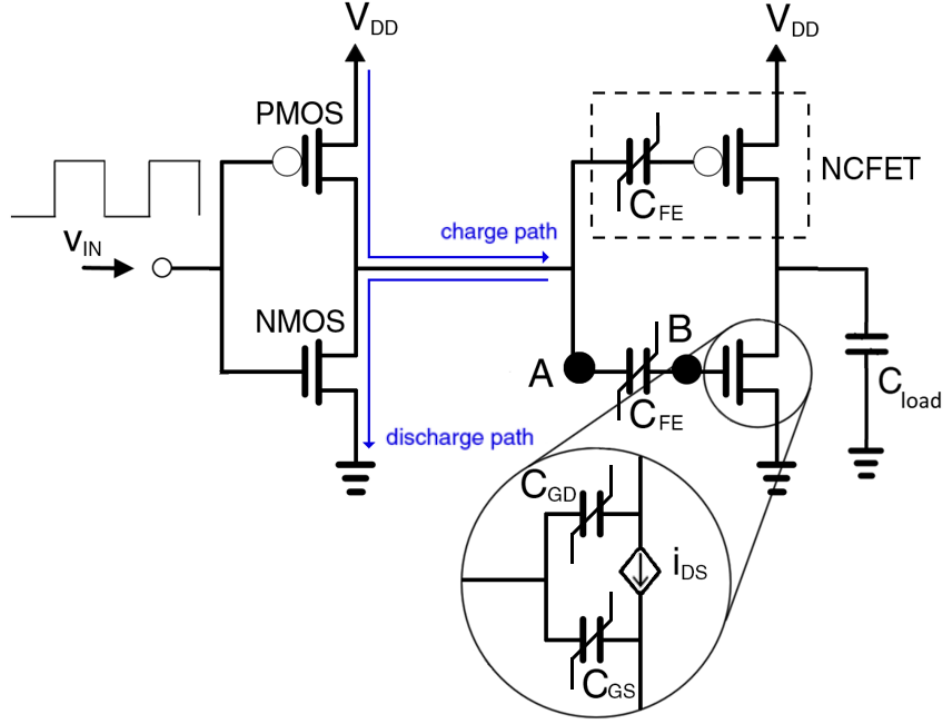

Fig. 2.2. The second simulation set-up, corresponding to a high-speed digital inverter-inverter model.

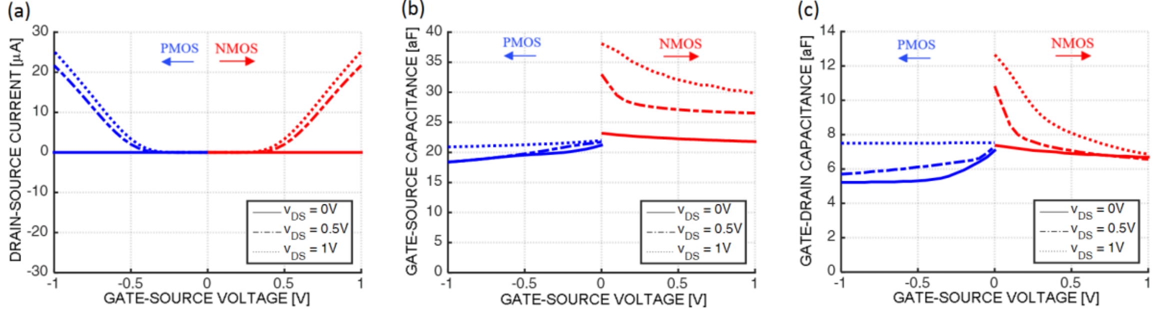

Fig. 2.3. Cadence Spectre [44] simulation results for a 28-nm FET: (a) $i_{DS}(v_{GS}, v_{DS})$ curves of NMOS and PMOS, (b) $C_{GS}(v_{GS}, v_{DS})$ curves for NMOS and PMOS, and (c) $C_{GD}(v_{GS}, v_{DS})$ curves for NMOS (red online) and PMOS (blue online).

2.2.2 Modeling the Ferroelectric

Our simulation methodology is based on the Landau-Khalatnikov (LK) equation [9], [10] for a ferroelectric capacitor (C_{FE} in Figs. 2.1 and 2.2):

$$\rho \frac{dP(t)}{dt} + \frac{dG}{dP} = 0 \tag{2.1}$$

where $P(t)$ is the polarization, G is the Gibb's free energy, and ρ is the viscosity.
The viscosity ρ in (2.1) accounts for the resistance of the ferroelectric to deformation, which is the mechanism for polarization switching, and hence ρ accounts for the finite time required for switching to occur. The expression for the Gibb's free energy appearing in (2.1) is

$$G = \alpha P^2(t) + \beta P^4(t) + \gamma P^6(t) - E(t)P(t) \tag{2.2}$$

where α, β and γ are material coefficients specific to a chosen ferroelectric [50], and where

$$E(t) = \frac{v_{\mathrm{FE}}(t)}{t_{\mathrm{FE}}} \tag{2.3}$$

is the electric field across the ferroelectric, with $v_{\mathrm{FE}}(t)$ being the voltage across it.

Equations (2.1) - (2.3) apply to a ferroelectric crystal with a uniform polarization; in order to capture the effect of multiple domains and the resulting nonuniform polarization, we discretize the ferroelectric into a square lattice and consider the area A_i centered around each lattice point i to have a uniform polarization $P_i(t)$. A linear interaction factor ties together all neighboring lattice points [51], [52]. We thus modify equations (2.1) and (2.2) to apply to a non-uniform polarization, finally obtaining

$$\rho \frac{dP_i(t)}{dt} = \frac{v_{\mathrm{FE}}(t)}{t_{\mathrm{FE}}} + k\left[\sum_j \left(P_j(t) - P_i(t)\right)\right] - 2\alpha_i P_i(t) - 4\beta_i {P_i}^3(t) - 6\gamma_i {P_i}^5(t) \tag{2.4}$$

where k is the interaction factor that describes the strength of the coupling between nearest neighbor lattice points, the sum over j is the sum over all neighbors of i, and we assume the entire ferroelectric crystal experiences a uniform electric field specified by (2.3). Finally, the charge on the ferroelectric capacitor is given by

$$Q(t) = \sum_i \left[\varepsilon_0 \frac{v_{\mathrm{FE}}(t)}{t_{\mathrm{FE}}} + P_i(t) \right] A_i. \tag{2.5}$$

Under these assumptions, equations (2.4) and (2.5) specify the nonlinear, time-dependent, charge-voltage (Q - v_{FE}) relation for each element C_{FE}, and they can be used with the corresponding current dQ/dt through each element, and Kirchoff's laws, to determine the transient responses of the circuits in Figs. 2.1 and 2.2. The time-domain integration is performed using Euler's method with adaptive time step.

2.2.3 Device Parameters

For the ferroelectric, we consider $PbZr_{1-x}Ti_xO_3$, where $x = 0.8$ for the overall crystal. However, in order to capture variations within the ferroelectric, we assume that the material exhibits a random spread, with x uniformly distributed between 0.6 and 1.0; the resulting coefficients α_i, β_i and γ_i in (2.4) can then be obtained using the expressions found in [50]. ρ is fitted at 2 Ω·m to produce a good agreement with the experimental result. The validity of our model and the underlying assumptions are verified by strong agreement with experiment, as shown in section 2.3.1.

2.3 Results and Discussion

2.3.1 Calibration with Experiment

As shown in the exploded view of Fig. 2.4, our simulated transient response aligns very well with the experimental curves in [11], including the sharp peak followed by a rapid decay and subsequent rise. Note that this signature behavior, and particularly the peaking, cannot be properly captured by a simulation that assumes uniform polarization, i.e., a single domain (cf., [11, Fig. 4b]). A multi-domain model [specified by our (2.4) and (2.5)] is needed to account for non-uniform polarization. We found that, for the purposes of this calibration to experiment, a square lattice with 100 points in each direction was adequate for reproducing the experimental curves. As the voltage across the ferroelectric v_{FE} climbs, it reaches the threshold required to cause the polarization at one lattice point of the ferroelectric crystal to flip, which, in turn, causes a cascading effect: the flipped

polarization at one lattice point spreads to neighboring lattice points via the interaction factor k (modeling the shifting of domain walls), which results in a sharp drop in the electric field and hence v_{FE}. This drop then slows as the region of flipped domains spreads to cover a greater proportion of the crystal, and v_{FE} resumes its steady climb, driven by the input signal, and the electric field thereby rises sufficiently to help flip the lattice points most resistant to a change in polarization. Clearly, capturing such behavior requires a non-uniform (multi-domain) polarization approach.

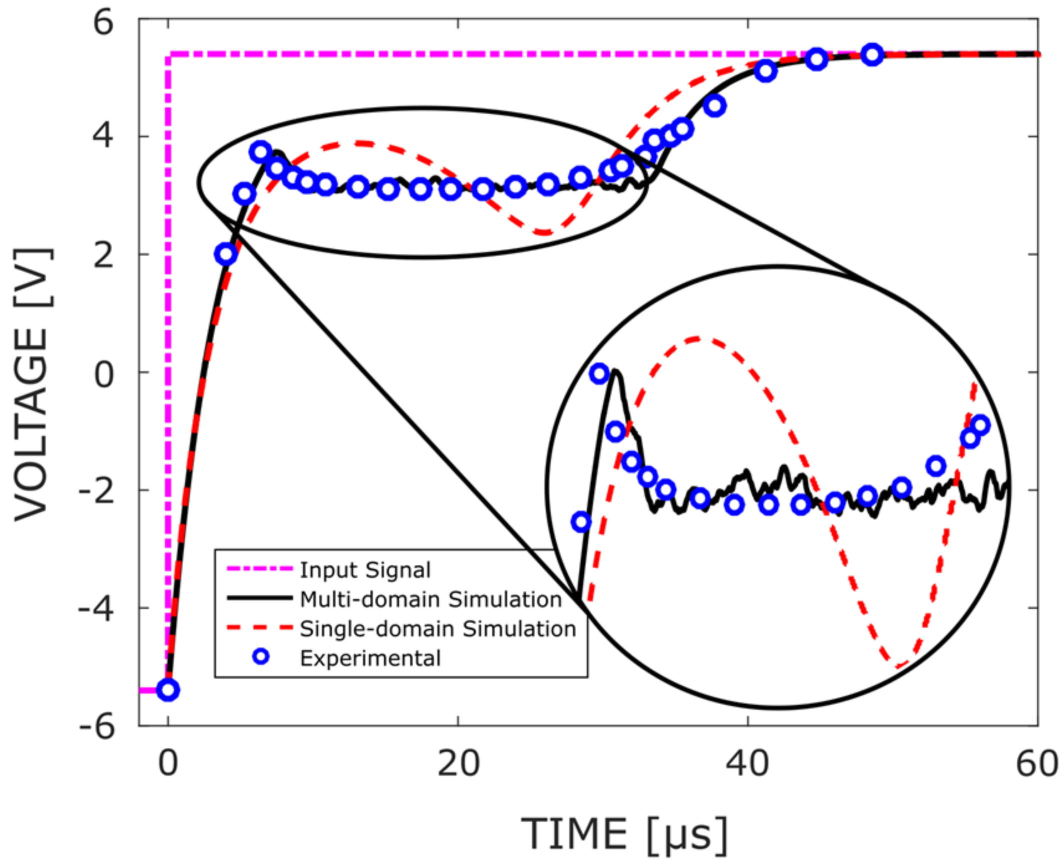

Fig. 2.4. Validation of our simulation methodology via a comparison with the experimental curves in [11]. Circles show experimentally measured values for the voltage v_{FE} across the ferroelectric. Solid line shows the result of our multi-domain simulation, which exhibits a strong match to experiment. Dashed line shows the result of a single-domain simulation. The input voltage is also shown as a dash-dotted line.

2.3.2 Dynamic Behavior at Low Frequencies

Having calibrated our simulation to experiment, we now examine the switching behavior of an inverter (Fig. 2.2) in order to assess the viability of digital circuits using

PZT NCFETs. We first consider operation at a frequency of 5 MHz. As seen in Fig. 2.5, our simulation confirms the voltage amplification effect of the ferroelectric at 5 MHz. The voltage at the internal node B (Fig. 2.2) (between the ferroelectric capacitor and the gate of the MOSFET) is 1.4 times greater than that of node A (to the left of the ferroelectric capacitor), which demonstrates a voltage boosting effect created by the ferroelectric capacitor. This boost will allow for an effective SS lower than 60mV/dec [3].

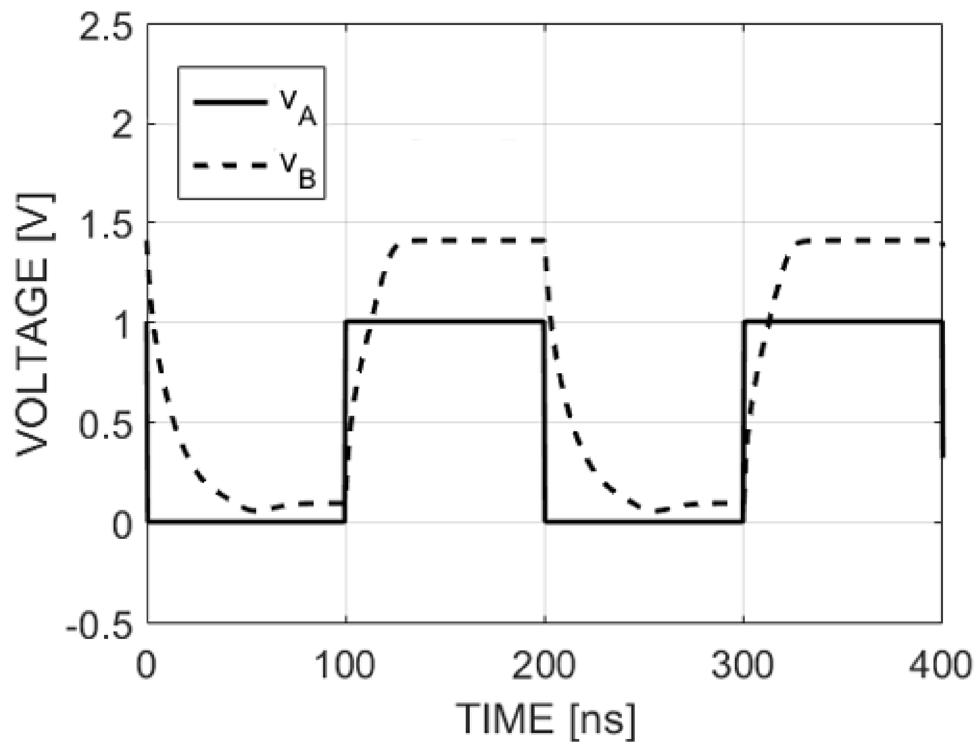

Fig. 2.5. Dynamic simulation of the circuit of Fig. 2.2 with an input signal at 5 MHz, showing verification of the voltage amplification effect.

2.3.3 Dynamic Behavior at High Frequencies

We then consider operation of this circuit at a frequency of 500 MHz. As shown in Fig. 2.6, at this frequency, the voltage amplification is lost, and the voltage at the internal node B in Fig. 2.2, i.e., between the ferroelectric capacitor and the gate of the MOSFET, is always lower than the voltage at node A to the left of the ferroelectric. We will now examine the reason for this result.

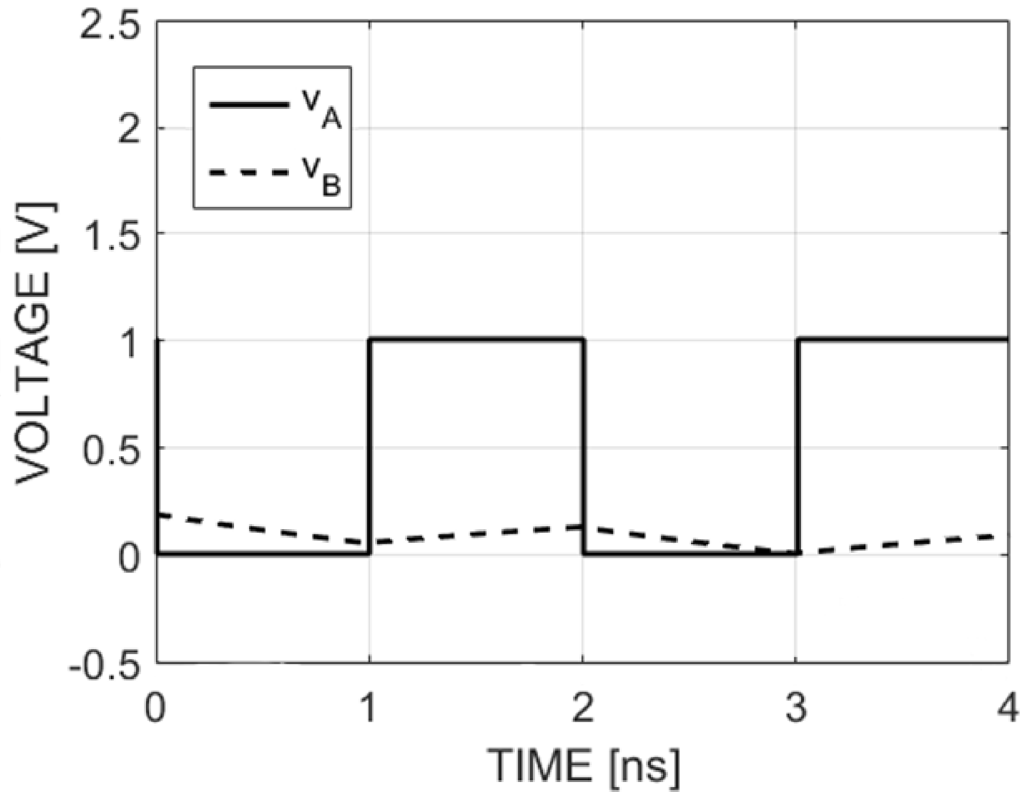

Fig. 2.6. Dynamic simulation of the circuit of Fig. 2.2, with an input signal at 500 MHz, showing loss of voltage amplification, i.e., showing $v_{\mathrm{B}} < v_{\mathrm{A}}$, at a higher frequency (vs. that for Fig. 2.5).

2.3.4 Connection to *P*-*E* Hysteresis Curves

The reason for a lack of negative capacitance and hence voltage amplification at high frequencies (Fig. 2.6) can be understood by considering the P-E hysteresis curves of a ferroelectric. Since the ferroelectric crystal must physically distort in order to switch polarization states, there is a small but finite delay between a voltage input and the resulting response in polarization – a delay modeled through the viscosity ρ in our LK approach. It then follows that for an input at high frequencies, the polarization cannot keep pace, and therefore remains in a fixed state. This gives rise to a symmetry breaking effect at high frequencies [53], [54], as shown in the simulated P-E hysteresis curves in Fig. 2.7, where for illustration, we take E to be the electric field across a single-domain ferroelectric. For frequencies up to 1 GHz, the ferroelectric is able to reach both positive and negative polarization. However, as the frequency increases further, and certainly by 10 GHz, the

electric field changes too quickly for the ferroelectric to respond, and the polarization remains trapped in one of the two stable states. Due to this trapped polarization state, the ferroelectric capacitor cannot exhibit negative capacitance, and hence voltage amplification cannot occur. These results are consistent with experimental data for the switching kinetics of PZT; measured rise times are approximately 200 ps [47], suggesting an operating-frequency limit of about 2.5 GHz.

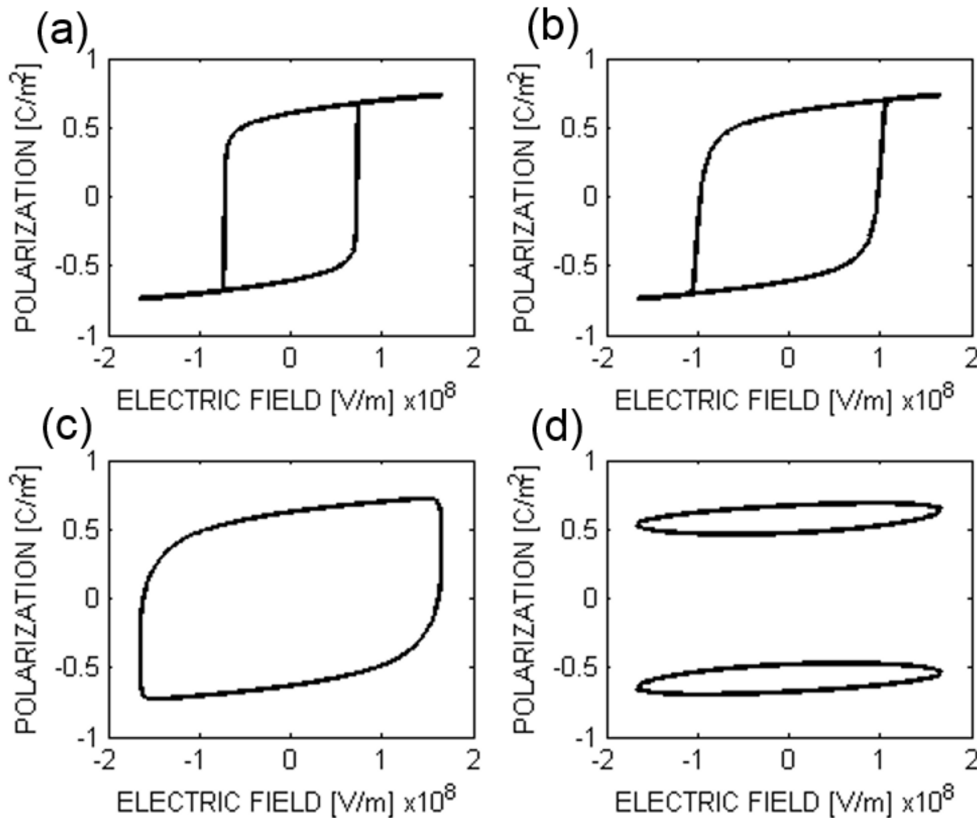

Fig. 2.7. Hysteresis curves at frequencies of (a) 10MHz, (b) 100MHz, (c) 1GHz, (d) 10GHz, showing the symmetry breaking phenomenon at high frequencies.

2.3.5 Frequency Effects on Voltage Amplification

The impact of symmetry breaking at high frequencies is illustrated explicitly in Fig. 2.8. As shown, the voltage amplification, defined as the peak voltage at node B divided by the peak voltage at node A in Fig. 2.2, steadily decreases as the frequency increases and as symmetry breaking inhibits polarization switching and the negative-capacitance effect. It is worth adding that at very high frequencies, the insertion of the ferroelectric can actually

lead to an attenuation of the voltage at B with respect to A. This phenomenon can be understood by considering the physical implications of the symmetry breaking of ferroelectric materials. At high frequencies, once symmetry breaking occurs [Fig. 2.7(d)], the ferroelectric is trapped in one of two polarization loops. In this case, the magnitude of the polarization change is small, i.e., the contribution of the term involving $P_i(t)$ in (2.5) to the dynamic response is negligible at high frequencies; the ferroelectric behaves essentially as a linear capacitance $\sim\varepsilon_0 A/t_{\mathrm{FE}}$ that is small compared to the gate capacitance $\varepsilon_{\mathrm{ox}}\varepsilon_0 A/t_{\mathrm{ox}}$ of the MOSFET, where $\varepsilon_{\mathrm{ox}}$ is the relative permittivity of silicon and $t_{\mathrm{ox}}$is its thickness, leading to the voltage attenuation visible in Fig. 2.8 at high frequencies.

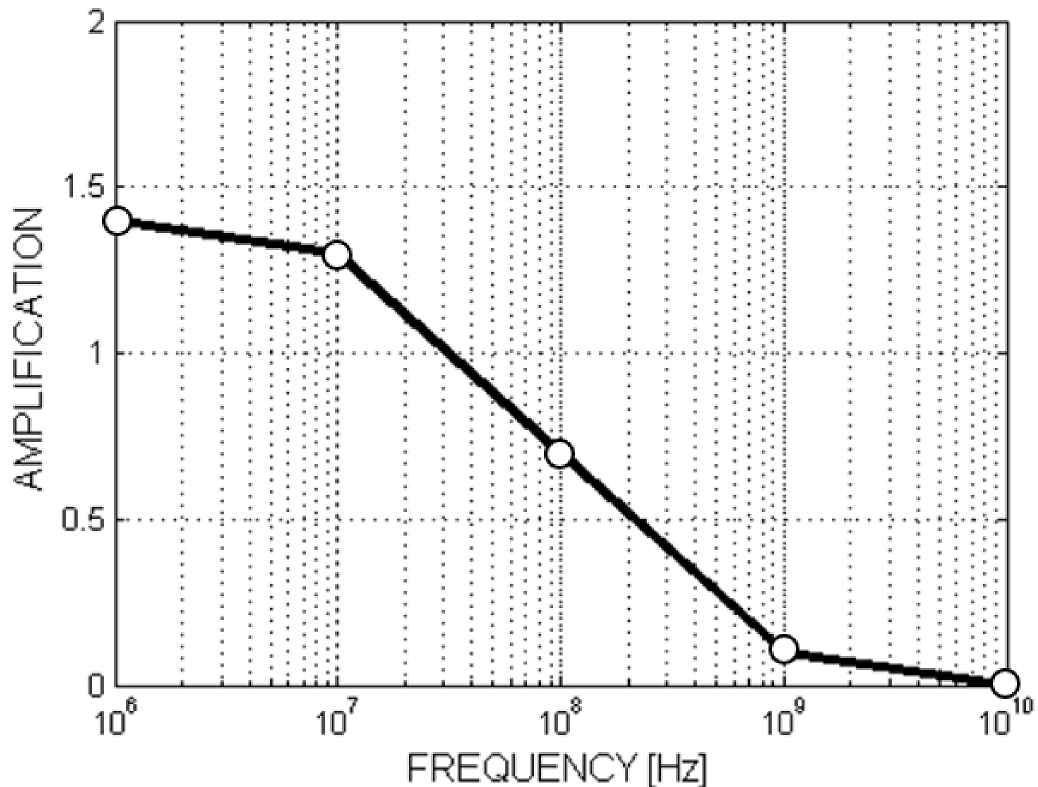

Fig. 2.8. Dependence of voltage amplification in the circuit of Fig. 2.2 on frequency, as described in the text.

2.3.6 Generalization to Other Ferroelectric Materials

The previous analysis was performed on a specific composition of PZT and there is no obvious extension to other ferroelectric materials. However, with an RC circuit approximation of a switching NCFET, we show in Appendix A that the minimum possible time required to achieve voltage amplification within an NCFET configuration is

$$\tau_{\min} = \frac{\rho t_{\mathrm{FE}}}{2}\left(\frac{C_{\mathrm{MOS}}}{A}\right) \tag{2.6}$$

where C_{MOS}/A is the usual capacitance per unit area of the gate.

With this expression, we can determine a bound for ρ to obtain $\tau_{\min} = 1$ ps, where 1 ps corresponds to the rise time of the inverter-inverter circuit in Fig. 2.2 in the absence of a ferroelectric material, i.e., the rise time with usual MOSFETs as opposed to NCFETs, and hence the rise time representative of modern and future processors working in the GHz to THz range.

A lower bound on the thickness for ferroelectrics is $t_{\mathrm{FE}} = 1$ nm, a value that can be found by accounting for the typical dimensions of a unit cell in ferroelectrics [50], and a reasonable minimum per-unit-area capacitance value for modern MOSFETs is $C_{\mathrm{MOS}}/A \sim$ 30 fF/μm^2, which can be deduced from the Cadence Spectre [49] simulation results shown in Fig. 2.3. With these values, to obtain $\tau_{\min} = 1$ ps, we find from (2.6) that ρ must be less than about 0.1 Ω·m, independent of other material properties, a value considerably lower than the $\rho = 2$ Ω·m value we used to match experiments for PZT in Fig. 2.4. In fact, for PZT, using the same α, β, and γ material coefficients as we did for Fig. 2.4, we find ρ must be reduced to 0.1 mΩ·m to achieve voltage amplification with a 1-ps rise time, as shown in Fig. 2.9. Note that the required ρ of 0.1 mΩ·m is actually 1000 times lower than the value of 0.1 Ω·m we found from (2.6), emphasizing that the latter value represents an *upper bound* on ρ, i.e., a *necessary* condition for any ferroelectric material to provide voltage amplification under high-speed operation.

2.4 Conclusions

The following conclusions can be drawn from this study examining NCFETs operating under high-speed switching conditions.

1. Current studies on NCFETs focus on static measurements of subthreshold slope. We have identified an additional parameter ρ that strongly influences the high-frequency response of ferroelectric materials.
2. The transient switching simulation results presented in this study show that while

ferroelectrics do have the potential to provide voltage amplification and hence an enhanced response to gate voltages in the MHz range, they will cease to provide this advantage in the GHz to THz range.

3. Ferroelectric materials must have a viscosity coefficient ρ less than 0.1 Ω·m to achieve voltage amplification with a 1-ps rise time.

While the requirement for a very low ρ may make NCFETs unsuitable for high-speed processors, they may still find application in low-speed applications, such as low-power sensors or low-power embedded systems, where polarization switching, negative capacitance, and voltage amplification will still occur. For high-speed applications, work is required to find a material with a suitably low ρ (below 0.1 Ω·m)

Chapter 3

Toward Microwave S- and X-Parameter Approaches for the Characterization of Ferroelectrics for Applications in FeFETs and NCFETs[2]

3.1 Introduction

Ferroelectric negative-capacitance field-effect transistors (NCFETs) realized by stacking ferroelectric material on top of conventional gate oxides have recently emerged as strong candidates to continue supply-voltage scaling as transistors approach their physical scaling limit [3], [45]. The use of ferroelectrics enables NCFETs to break the subthreshold slope (SS) barrier of 60 mV/decade set by Boltzmann statistics and to provide a high on-current I_{ON} [46]. Other applications of ferroelectrics, such as in memory [29], [30], including non-destructive non-volatile memory utilizing ferroelectric FETs (FeFETs) [28], and negative differential resistance FETs [32], are rapidly emerging. HfO_2 is currently the most prominent material being considered for use as a ferroelectric due to its compatibility with current integrated-circuit (IC) process flows, and research is underway into the engineering of HfO2 for use in NCFETs. For example, the negative capacitance behavior of HfO_2 has been shown to depend on crystal granularity [56], physical strain [56], [57], and orientation [57]. Furthermore, silicon [58], yttrium [59], and zirconium [60] all cause different negative capacitance behaviors when used to dope HfO_2. Recently, Global

[2] A version of this chapter has been published [20].

Foundries has successfully fabricated an NCFET ring oscillator using HfO_2 that operates at up to 40 GHz [13], with each individual device in the ring having a reduced subthreshold slope compared to standard FETs. Motivated by such results, work continues in the area of optimizing FeFETs and NCFETs, not only in silicon but also in a variety of other materials (e.g., [61], [62], and [63]), and the search to identify the best ferroelectrics and the best material composition (e.g., thickness, crystal orientation, and physical strain) for all these emerging devices continues to be a topic of great interest. Measurement approaches to facilitate such identification are highly desirable to move the related technologies toward realization.

The Sawyer-Tower (ST) circuit is a well-known method to characterize ferroelectrics [33], [34]. However, while such an approach can be used to obtain the lossless Landau-Khalatnikov (LK) parameters α, β, and γ, it cannot be used to determine the loss parameter ρ due to the impact of parasitics in the measurement approach, such as parasitics from the cabling and oscilloscope probes [32]. Since the ST circuit relies on tracking signals in the time domain, the dynamic switching portion of the polarization vs. electric-field hysteresis trace, which must be known accurately to predict ρ, will depend on the unknown parasitics [36, Sec. IV]. Knowledge of ρ is important to accurately predict the switching speed of NCFETs [19], [42], [64], [65]. Direct measurements of ferroelectric switching speed using time-domain measurements have also been attempted, but only speeds up to 100 MHz were successfully measured [66].

Optical methods have been used to determine ρ. For example, by utilizing a form of the LK equation that is second order in time and fitting its parameter values to resonance patterns from measurements of the absorbance at different wavelengths of light, a value of ρ can be deduced and used to predict NCFET switching speed [42]. However, as we will show, a first-order equation along with direct electrical excitation is sufficient for the accurate extraction of ρ at speeds relevant to today's devices. Electrical methods offer the advantage of being familiar to the electron-device community, involving conventional electrical measurement tools (e.g., network analyzers) and approaches (e.g., de-embedding of parasitics), and of stimulating the ferroelectric in a manner consistent with its use in circuit applications.

Recently, a single-domain LK equation was used to fit a variety of experimental data, with the suggestion that the loss parameter ρ is not a constant, as typically assumed, but must vary with polarization [67]. While a variable-ρ approach provides a good fit to the experimental results in [11], [65], [68] – [71], a multidomain LK equation has also been shown to provide an accurate fit to experimental polarization vs. electric-field curves [19]. Though both these approaches can provide an excellent fit to the measurement data currently available, characterization of ferroelectrics via time-domain measurements [11], [65], [68] – [71] may not reveal the intrinsic polarization vs. electric-field curve, i.e., the curve with fully de-embedded parasitics, including an accurate portrayal of the switching portions. As a result, irrespective of the modeling approach, it is desirable to have an alternative to conventional time-domain measurement approaches that can accurately reveal the intrinsic[3] ferroelectric behavior, from which the LK parameters can then be reliably extracted.

In this study, we take a step toward this goal, by offering two such electrical methods that can be used to characterize ferroelectrics. In section 3.2, we propose and demonstrate the viability of a technique to probe ferroelectrics under the general condition of complete switching between the two stable states, based on the use of X-parameters [40], which are a large-signal generalization of the well-known small-signal S-parameters. The key feature of this new approach is to exploit the highly nonlinear nature of ferroelectric switching, which has been demonstrated outside of electron-device applications [72], [73], by exciting the ferroelectric with a large input signal and utilizing the resulting harmonic response to precisely reconstruct the intrinsic polarization vs. electric-field hysteresis curve of the ferroelectric, thereby allowing an accurate determination of all the LK parameters, including the loss parameter ρ. In section 3.3, we offer a simplified approach to probe balanced ferroelectric-dielectric stacks, emulating the structure required for low-power logic NCFET operation. Forgoing the exact measurement of the lossless nonlinear LK parameters β, and γ, which can be determined by other means, we focus on the small-signal

[3] In this study, we define "intrinsic" as describing the characteristics seen across the terminals of *only* the device in question. In contrast, "extrinsic" would describe characteristics seen across the combination of the device in question and connected components such as probe or cable parasitics.

linear negative-capacitance region of a ferroelectric's polarization vs. electric-field behavior, which is the region most relevant for a balanced structure used in low-power logic, and we show how the loss parameter ρ and the lossless linear parameter α can be obtained via conventional S-parameter measurements. Both our approaches are frequency-domain approaches, relying on large-signal harmonic information (X-parameters) or steady-state small-signal sinusoidal information (S-parameters); as we will show, parasitics can hence be de-embedded in both cases and are not a limiting factor as they are in time-domain approaches [74], such as with the ST circuit. Overall, this chapter thus presents two frequency-domain electrical techniques that can help accelerate the realization of NCFET circuit applications utilizing the unique properties of ferroelectrics. The conclusions of this study is presented in section 3.4.

3.2 X-parameter Technique

3.2.1 $P(t)$ vs. $E(t)$ Curve from Harmonic Information

X-parameters are a large-signal generalization of the well-known S-parameters, with the distinction being that S-parameters are limited to purely linear networks whereas X-parameters can be used to characterize *non*linear networks [38], [39]. X-parameters also offer the ability to measure systems with memory, which is especially applicable to the ferroelectric response [40]. Our approach with X-parameters exploits the highly nonlinear nature of ferroelectric switching. When driven by a large sinusoidal signal, the ferroelectric can be made to switch between its two stable states, with each switching transition creating harmonic information that can be measured and exploited to reveal the intrinsic $P(t)$ vs. $E(t)$ curve, from which all the LK parameters can be found.

As shown in Fig. 3.1, the ferroelectric is driven by a large-signal sinusoidal source v_{IN} at a fundamental frequency ω_0, and the incident and reflected power waves a_n and b_n around the ferroelectric are determined at all harmonic frequencies $n\omega_0$, where $n = 1$ corresponds to the fundamental, and where the harmonics for $n \neq 1$ result from the highly nonlinear nature of ferroelectric switching. In doing so, we assume the passive network of cable and contact parasitics (shown boxed in Fig. 3.1) that couple the source to the ferroelectric capacitor remains linear even with a large input signal, so that standard calibration methods [37] involving open, short, and through loads (in place of the

ferroelectric) can be used to de-embed this network at the fundamental and all harmonic frequencies of interest, thus enabling the accurate determination of a_n and b_n for all n.

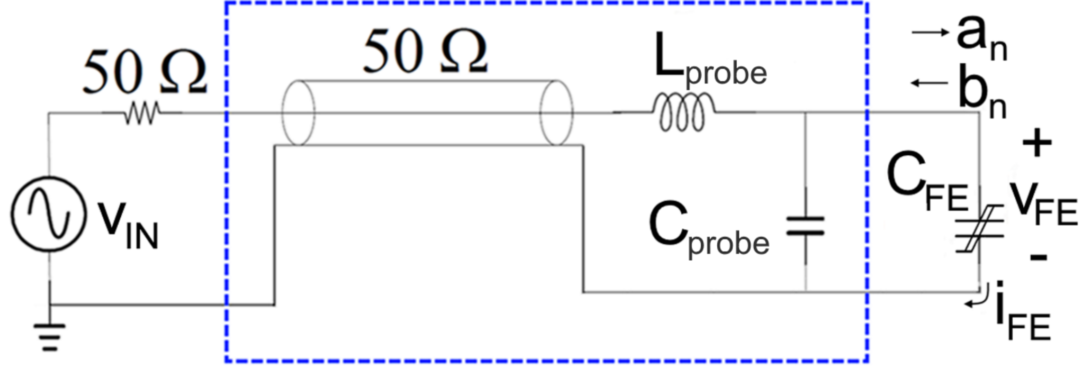

Fig. 3.1. Proposed X-parameter test circuit to measure ferroelectric parameters and switching speed at high frequencies. The boxed subcircuit shows the cabling and parasitics, all of which comprise a linear network that can be de-embedded to accurately isolate the required signals around the ferroelectric at the fundamental (driving) and harmonic frequencies.

The power signals at each harmonic can be converted into voltage and current waveforms around the ferroelectric using the same procedure as with S-parameters [37]. The complex voltage harmonics are specified by

$$v_n e^{j\phi_{v,n}} = \sqrt{Z_0}(a_n + b_n) \tag{3.1}$$

where v_n and $\phi_{v,n}$ are the magnitude and phase of the nth voltage harmonic and Z_0 is the reference impedance, and the current harmonics are specified by

$$i_n e^{j\phi_{i,n}} = (a_n - b_n)/\sqrt{Z_0} \tag{3.2}$$

where i_n and $\phi_{i,n}$ are the magnitude and phase of the nth current harmonic. The voltage and current harmonics can be converted to time-dependent waveforms using Fourier series:

$$v_{\mathrm{FE}}(t) = \sum_{n=1}^{N} v_n \cos(n\omega_0 t + \phi_{v,n}) \tag{3.3a}$$

$$i_{\mathrm{FE}}(t) = \sum_{n=1}^{N} i_n \cos(n\omega_0 t + \phi_{i,n}) \tag{3.3b}$$

where N is the highest harmonic that can be accurately measured, t is time, $v_{\mathrm{FE}}(t)$ is the voltage across the ferroelectric, and $i_{\mathrm{FE}}(t)$ is the current through the ferroelectric.
The electric field can be calculated by assuming it is uniform across the ferroelectric:

$$E(t) = v_{\mathrm{FE}}(t)/t_{\mathrm{FE}} \tag{3.4}$$

where t_{FE} is the thickness of the ferroelectric. The polarization then follows from Maxwell's equation:

$$P(t) = Q(t)/A - \varepsilon_0 E(t) \tag{3.5}$$

with $E(t)$ available from (3.4) and $Q(t)$ found by simply integrating $i_{\mathrm{FE}}(t)$ in (3.3b).

3.2.2 Second-Order vs. First-Order LK Equation

The simplest way to describe the $P(t)$ vs. $E(t)$ hysteresis behavior of a ferroelectric is by using the single-domain Landau-Khalatnikov (LK) model [7]:

$$\rho \frac{dP(t)}{dt} = E(t) - 2\alpha P(t) - 4\beta P^3(t) - 6\gamma P^5(t) \tag{3.6}$$

where the material constants α, β, γ, and ρ must be chosen to match the measured $P(t)$ vs. $E(t)$ behavior.

Here, in (3.6), we do not use the LK equation that is second-order in time, suggested in [42] and also used in [75], which includes an additional term $l\ [d^2P(t)/dt^2]$ on the left side, where l is an inertial parameter. Our choice of the first-order equation can be justified by examining the resonance frequency of the experimental results fitted to the second-order equation in [42], which is 10 THz. At excitation frequencies significantly lower than that of the resonance frequency, the second-order equation converges back to the first-order equation, and differences between the two are negligible. To illustrate how the two equations compare at speeds significantly below 10 THz, in Fig. 3.2, we show results from the second-order LK equation presented in [42] to those from the first-order LK equation,

where the first-order equation is obtained simply by setting the term that is second-order in time to zero. We chose the LK parameters calibrated to hafnium dioxide, as done in [42]; the relevant values of ρ, α, β, and γ are listed in the first column of Table 3.1, and l is calibrated to 47 amu per dipole. Fig. 3.2 shows that the second-order equation predicts no significant difference in the time response of the ferroelectric when excited by a square pulse with 10-ps pulse width, 100-fs rise time, and amplitude as shown in the legend. Therefore, even though the addition of a second-order term provides a more accurate model for the ferroelectric dynamic behavior at higher frequencies, in this study we will use the first-order version (augmented for multidomain effects as described in section 3.2.3 below). It is also worth adding that the first-order LK equation is the most commonly used approach to describe dynamical ferroelectric behavior [3], [64], [65], [67], and that while we choose the first-order version, the extraction procedure used in [42] to find l could be incorporated if a second-order equation was chosen.

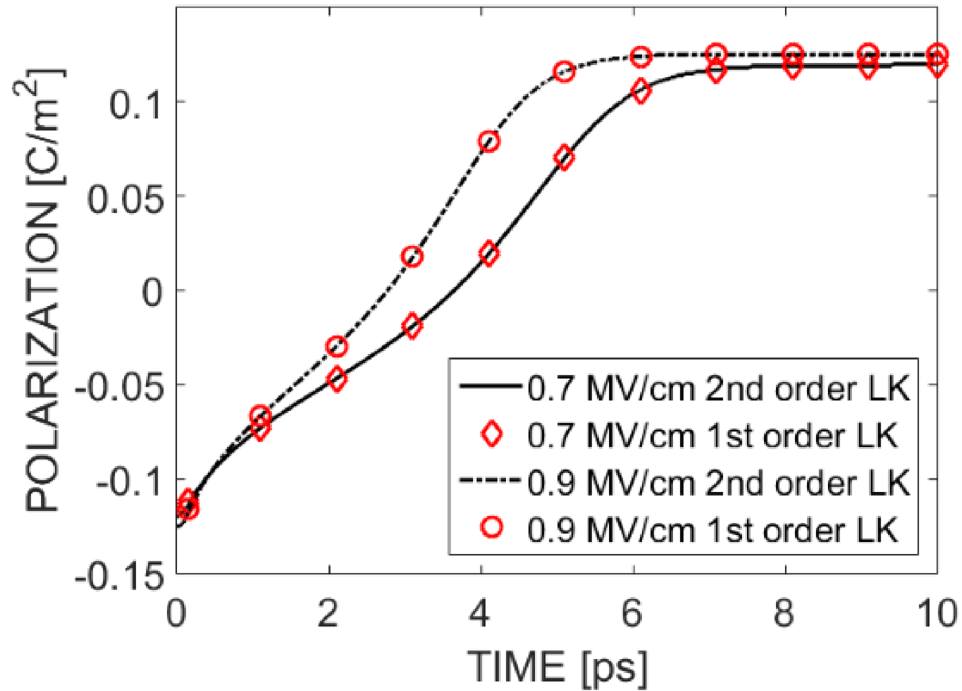

Fig. 3.2. Reproduction of the simulation found in [39], with the first-order LK equation (symbols) and second-order LK equation (lines).

3.2.3 Multidomain LK Equation

We can modify (3.6) to consider multidomain effects during ferroelectric switching by defining a local polarization $P(t, \mathbf{r})$, where $\mathbf{r}$ refers to a vector position in the ferroelectric. By assuming variation only along the plane of the ferroelectric (not along its thickness), $P(t, \mathbf{r})$ can be related to the macroscopic (area-averaged) polarization $P(t)$:

$$P(t) = \int P(t, \mathbf{r})\, d\mathbf{r}/A \tag{3.7}$$

where A is the surface area and $d\mathbf{r}$ is a differential area element. We then replace the macroscopic polarization in (3.6) with the local polarization, and add a local interaction term that depends on a coupling coefficient k between local dipoles at $\mathbf{r}$ and $\mathbf{r} + d\mathbf{r}$, which yields a modified LK model that has been shown to accurately reproduce the response of PZT [19] and zirconium-doped HfO_2 [69], and is consistent with the energy function for a ferroelectric with non-uniform polarization [76], [77]:

$$\rho \frac{dP(t, \mathbf{r})}{dt} = E(t) - 2\alpha(\mathbf{r})P(t, \mathbf{r}) - 4\beta(\mathbf{r})P^3(t, \mathbf{r}) - 6\gamma(\mathbf{r})P^5(t, \mathbf{r}) + k\nabla^2 P(t, \mathbf{r}) \tag{3.8}$$

3.2.4 Illustration of the Experimental Method

To illustrate the merit of our proposed X-parameter approach, we have simulated the measurement scheme of Fig. 3.1, with the ferroelectric described by (3.8). We use Si-doped HfO_2 for the ferroelectric capacitor C_{FE}, and we presume a surface area of $A = 1000$ nm $\times$ 1000 nm, discretized into a 100 by 100 lattice, and a thickness of $t_{\mathrm{FE}} = 10$ nm. For regular lattice sites, we assign values of the lossless parameters $\alpha(\mathbf{r})$, $\beta(\mathbf{r})$, and $\gamma(\mathbf{r})$ to be those extracted from a fit of experimental results [41], and the loss parameter ρ is set to 1.8 mΩ·m [42]. To model multidomain effects, we add defect sites to the ferroelectric by assigning parameter values $\alpha(\mathbf{r})$, $\beta(\mathbf{r})$, and $\gamma(\mathbf{r})$ at random lattice points so that they must stay in one of the two stable states without any possibility of switching. This approach has been shown to replicate multidomain behavior in a previous study [78]. In our own simulations, we choose an even number of defects with half in each of the two stable polarizations to maintain symmetry. In [78], 15 defects were used, and in our study, the

results reported are found using 10 defects. We assume values of parasitic inductance and capacitance $L_{\text{probe}} = 50$ pH and $C_{\text{probe}} = 50$ fF.

We set v_{IN} to have a fundamental frequency ω_0 of 10 GHz, and a spread of input power is used to obtain results for the reflected power. The first three odd harmonics prior to the de-embedding of parasitics (solid line) and after the de-embedding of parasitics (dashed line) are shown in Fig. 3.3(a) and 3.3(b), which are plotted following the convention for X-parameter data used in [79]. Note that only odd harmonics are plotted because we have modeled the ferroelectric to have symmetrical response, so the even harmonics are negligibly small, and the de-embedded a_n harmonics are left out to avoid visual clutter, as they follow the same trend as the b_n values. Fig. 3.3(a) demonstrates a clear signature of the effect of the ferroelectric's threshold behavior on the reflected-power harmonics: at low input power, the ferroelectric does not respond, and the higher-order ($n > 1$) harmonic power levels are negligible; starting at an input power of 0 dBm up to 13 dBm, power is increasingly scattered into the higher harmonics, as the ferroelectric begins to respond; increasing the input power past 13 dBm does not significantly increase the reflected power of higher harmonics. This behavior is the power equivalent of the well-known ferroelectric threshold electric-field behavior: when an applied electric-field is below the coercive field, there is no significant polarization response; if the applied field only slightly exceeds the coercive field, the ferroelectric polarization begins to-respond but does not fully traverse between the two stable states within a period of the signal; once the field is sufficiently strong for complete switching, increasing it further does not significantly increase the polarization response. For illustrative purposes, we use an input power of 13 dBm, which is the lowest power at which the ferroelectric fully responds, to calculate the voltage and current waveforms around the ferroelectric; in practice, this choice is also recommended to minimize errors, since the relative magnitude of the higher harmonics vs. the fundamental continually decreases for higher input powers. Furthermore, to emulate measurement limitations, we use only the harmonics within 40 dB of the fundamental. The resulting voltage and current waveforms are shown in Figs. 3.3(c) and 3.3(d), respectively. These waveforms are used to trace out the $P(t)$ vs. $E(t)$ hysteresis shown by the solid curve in Fig. 3.4, as described in section 3.2.1.

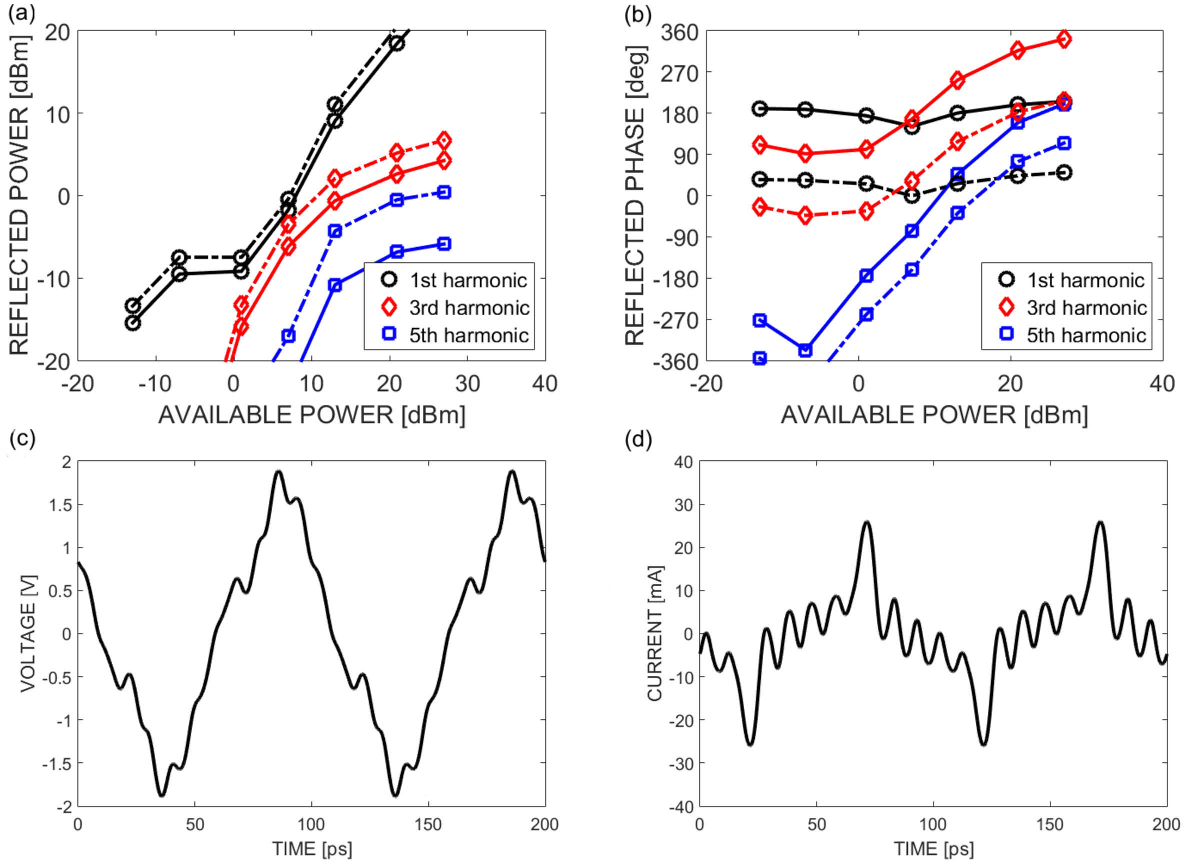

Fig. 3.3. Reflected power b_{n} and time-domain waveforms $v_{\mathrm{FE}}(t)$ and $i_{\mathrm{FE}}(t)$ for the circuit in Fig. 3.1, found using the X-parameter approach described in the text. (a) Magnitude of the first three odd harmonics of b_n before calibration (solid lines) and after calibration (dashed lines); (b) phase of the first three odd harmonics of b_n before calibration (solid lines) and after calibration (dashed lines); (c) voltage waveform $v_{\mathrm{FE}}(t)$; (d) current waveform $i_{\mathrm{FE}}(t)$.

3.2.5 Extraction of ρ

To demonstrate how the ferroelectric parameters can be extracted from a measured $P(t)$ vs. $E(t)$ hysteresis curve, such as that in Fig. 3.4, we first note that at steady state and over an entire period T, the ferroelectric returns to its initial potential energy. Thus, any energy supplied must be equal to the energy dissipated by the ferroelectric:

$$\int_{t_1}^{t_1+T} E(t)\, dP(t) = \int_{t_1}^{t_1+T} \rho \frac{dP(t)}{dt} dP(t) \tag{3.9}$$

where the left and right integrals represent the energy supplied and energy dissipated by the ferroelectric, respectively, both per unit volume. The loss parameter ρ is then found by simply rearranging (3.9) to demand that

$$\int_{t_1}^{t_1+T} \left[E(t) - \rho \frac{dP(t)}{dt} \right] dP(t) = 0 \tag{3.10}$$

or, equivalently,

$$\int_{t_1}^{t_1+T} E_{\text{int}}(t)\, dP(t) = 0 \tag{3.11}$$

where, for the sake of discussion, we define

$$E_{\text{int}}(t) \equiv E(t) - \rho \frac{dP(t)}{dt} \tag{3.12}$$

as an internal electric field that would occur if the ferroelectric was lossless: $E_{\text{int}}(t) = E(t)$ when $\rho = 0$. Since the left side of (3.10) is a monotonic function in ρ, the required value of ρ can be found by solving (3.10) with standard numerical techniques (*e.g.*, binary search) and with $E(t)$, $P(t)$, and $dP(t)/dt$ obtained from (3.4) and (3.5), *i.e.*, from the simulated measurement results illustrated in Fig. 3.4.

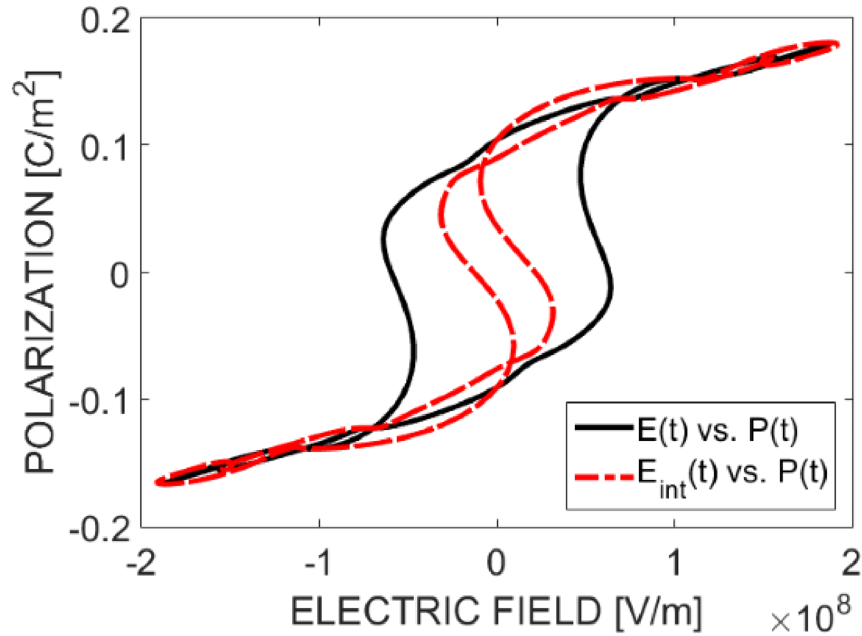

Fig. 3.4. Polarization vs. electric field hysteresis plots found from the X-parameter approach with the circuit of Fig. 3.1, as described in section 3.2. For $E_{\text{int}}(t)$ vs. $P(t)$, $E_{\text{int}}(t)$ is specified by (3.12) with ρ chosen so that the integral of $E_{\text{int}}(t)$ over a full period is zero.

3.2.6 Extraction of α, β, γ

Taking the area integral of both sides of (3.8) reveals

$$E_{\text{int}}(t) = \frac{1}{A}\int [2\alpha(\mathbf{r})P(t,\mathbf{r}) + 4\beta(\mathbf{r})P^3(t,\mathbf{r}) + 6\gamma(\mathbf{r})P^5(t,\mathbf{r})]\, d\mathbf{r} \tag{3.13}$$

where the term $\int k\nabla^2 P(t,\mathbf{r})d\mathbf{r}$ collapses to zero due to the use of Neumann boundary conditions. The integrand in (3.13) can be interpreted as describing a lossless "S" curve for a local electric field $E_{\text{int}}(t,\mathbf{r})$ vs. local polarization $P(t,\mathbf{r})$ at each location $\mathbf{r}$, and $E_{\text{int}}(t)$ can then be viewed as an area-averaged quantity over all such local fields for the multidomain ferroelectric. A plot of this area-averaged (macroscopic) $E_{\text{int}}(t)$ vs. the area-averaged (macroscopic) polarization $P(t)$ need not follow a classical "S" shape, as illustrated in Fig. 3.4, but need only be consistent with zero loss as prescribed by (3.11). Despite the lack of a classical "S" shape, we can still extract nominal values of α, β, γ by fitting an overall "S" curve that passes through the origin and the non-switching portions of the $E_{\text{int}}(t)$ vs. $P(t)$ curve, *i.e.*, those portions of our simulated measurements in Fig. 3.4 for which $E_{\text{int}}(t) \approx E(t)$ and the origin. This process can be seen in Fig. 3.5, where the relevant portions used for fitting are shown as empty circles.

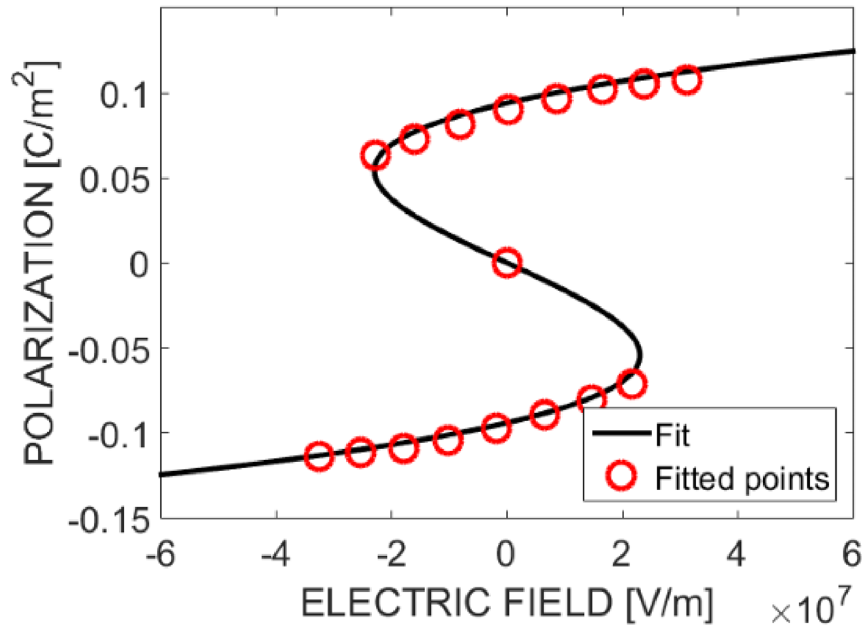

Fig. 3.5. Chi-squared fit for an "S" curve that passes through the origin and the stable (non-switching) regions [over which $E_{\text{int}}(t) \approx E(t)$] of the curves in Fig. 3.4.

Values for the parameters α, β, and γ can thus be extracted using a chi-squared polynomial regression of order five to fit an "S"-shaped lossless trace to the empty circles:

$$E_{\text{fit}}(P) = c_0 + c_1 P + c_2 P^2 + c_3 P^3 + c_4 P^4 + c_5 P^5 + \cdots \tag{3.14a}$$

$$\chi^2 = \sum \frac{[E_{\text{int}}(P) - E_{\text{fit}}(P)]^2}{E_{\text{fit}}(P)} \tag{3.14b}$$

where $c_1 = 2\alpha$, $c_3 = 4\beta$, and $c_5 = 6\gamma$ are the LK coefficients. Here, for generality, we include the even coefficients c_0, c_2, and c_4, which are intrinsically zero for a perfectly symmetrical ferroelectric, but which can be made nonzero to describe asymmetry, a phenomenon that has been observed in fabricated ferroelectric structures [11], [69].

Table 3.1 summarizes the extracted and expected values of ferroelectric parameters from our suggested extraction procedure. To further simulate realistic measurement uncertainties, the extracted values were obtained assuming the calibration had an error of 0.2 dB, and only harmonics within 40 dB of the fundamental were used to plot the $P(t)$ vs. $E(t)$ hysteresis curve. As shown, there is good agreement even with the assumed uncertainties, demonstrating the viability of our approach, *i.e.*, the use of harmonic (X-parameter) information available from the switching of a ferroelectric to first find the de-embedded $P(t)$ vs. $E(t)$ curve, and to then use that curve to systematically isolate its LK parameters.

TABLE 3.1
ASSIGNED VS. EXTRACTED FERROELECTRIC PARAMETERS

Parameter	Assigned	Extracted
ρ	1.80 mΩ·m	2.20 mΩ·m
α	-3.60×10^{8} V·m/C	-3.18×10^{8} V·m/C
β	2.25×10^{10} V·m^5/C^3	2.29×10^{10} V·m^5/C^3
γ	1.67×10^{9} V·m^9/C^5	1.05×10^{9} V·m^9/C^5
k	3.00×10^{-8} V·m^3/C	3.60×10^{-8} V·m^3/C

3.2.7 Extraction for More Sophisticated Models

The basic LK parameters α, β, γ, and ρ can be used as constants in a simple single-domain model to approximate ferroelectric behavior. However, adjustments to this model may be necessary to more accurately fit experimental results. One approach is to extract a multidomain parameter k, and another is to use a variable ρ [67]. We will show that suitable values can be extracted for either approach from X-parameter data.

In order to fit to the multidomain LK model, we assume the ferroelectric has a small number of defects, which is consistent with earlier work [78]. This approach is also consistent with our finding that the exact number of defects should have no significant impact on the measured voltage and current, and hence the measured $P(t)$ vs. $E(t)$ response, which we confirmed by varying the defects between 6 and 1,000 in our 10,000-point grid and finding no significant changes to the simulated measurement results in Figs. 3.3 and 3.4. k can then be found from the measured current and voltage directly around the ferroelectric through the use of a self-consistent numerical solution. The already extracted α, β, γ, and ρ parameters along with an initial guess for k would be used to simulate the current response $i_{\mathrm{FE}}(t)$ arising from $v_{\mathrm{FE}}(t)$, via an equation of the form (3.8), and with the exact number of defects unimportant, as just mentioned. A larger k will cause the ferroelectric to switch faster due to faster domain wall propagation, causing an increase in peak current during the transients, and vice versa. This unidirectional relationship between k and peak current can then be used to modify k in the solution until the measured current transient $i_{FE}(t)$ corresponding to the direct excitation $v_{FE}(t)$ is found. Table 3.1 shows our extracted k with this approach is very close to the initially assigned k value.

Given that finding k for a multidomain model requires a self-consistent numerical solution, a simpler alternative may be the use of a variable ρ [67]. To extract a variable ρ, multiple $P(t)$ vs. $E(t)$ curves are required (*e.g.*, found by changing the input signal frequency or power). A fixed value of polarization P_1 occurring at a time t_1 is selected for each curve, along with the corresponding values $E(t_1)$ and $dP(t_1)/dt$ are recorded. A linear line-of-best-fit is fitted to these $E(t)$ vs. $dP(t)/dt$ points to find $\rho(P_1)$, as shown in [67]. This procedure is then repeated for each P_1 within the range of measured $P(t)$ to find the overall $\rho(P)$. Using the X-parameter data measured at different input powers shown

in Fig. 3.3(a) and Fig. 3.3(b), the derived ρ varies from 1 – 3 mΩ·m. In comparison, the value of ρ extracted by the multidomain model was 2.2 mΩ·m.

3.3 S-parameter Technique

For the specific case of characterizing ferroelectrics in NCFETs targeted for low-power logic applications, a highly simplified S-parameter approach can be used. This method retains the advantage of de-embedding techniques inherent to frequency-domain measurements but requires a balanced ferroelectric-dielectric capacitor stack that is hysteresis free; such a balanced stack emulates the gate of an NCFET [3], with the linear capacitor replacing the gate capacitance of the MOSFET. Applying a small-signal S-parameter measurement to this structure allows the extraction of the loss parameter ρ and the linear LK parameter α, but cannot extract the nonlinear LK parameters β and γ, nor the multidomain parameter k. Although not all LK parameters can be extracted using this method, the knowledge of ρ is important for predicting the switching speed [19], [42], [64], [65], as already mentioned in Section 3.1, and the knowledge of α can be used to make first-order predictions on metrics such as SS, $I_{\mathrm{on}}/I_{\mathrm{off}}$, and reduced source-drain conductance in NCFETs [80].

In a balanced structure, the ferroelectric stabilizes in the middle of the two spontaneous polarizations [3]. Upon application of a small-signal voltage, the stack can hence be expected to behave as shown in Fig. 3.6, where the boxed portion shows a first-order representation of the ferroelectric based on a linearization of the LK equations (3.4) – (3.6), with $C_N = A/2\alpha t_{\mathrm{FE}}$ representing the small-signal negative capacitance of the ferroelectric and C_{DE} representing the series dielectric.

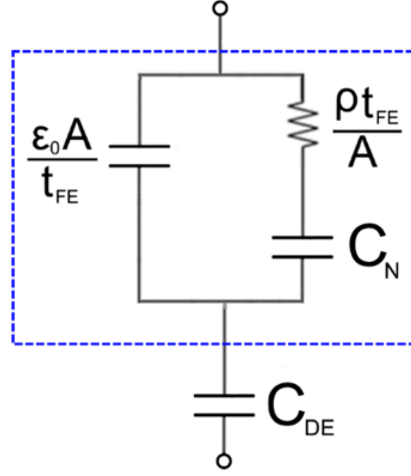

Fig. 3.6. Equivalent circuit model of a ferroelectric capacitor in series with a linear capacitor in a balanced capacitor stack. The boxed subcircuit is the circuit representation of the ferroelectric, found by linearizing the single-domain LK equations (3.4) – (3.6).

The approach uses the measurement circuit of Fig. 3.1, but with the capacitor stack replacing the isolated ferroelectric as the device under test (DUT). With standard de-embedding techniques, a measured value for S_{11} in such a configuration can be related to the load impedance offered by the DUT [81],

$$Z_L = \frac{1+S_{11}}{1-S_{11}} Z_0 \tag{3.15}$$

which must equal that indicated by the model in Fig. 3.6,

$$Z_L = \frac{1}{\frac{j\omega\varepsilon_0 A}{t_{\mathrm{FE}}} + \frac{1}{\frac{\rho t_{\mathrm{FE}}}{A} + \frac{1}{j\omega C_N}}} + \frac{1}{j\omega C_{\mathrm{DE}}}. \tag{3.16}$$

By equating the real and imaginary parts of (3.15) and (3.16), two equations can be obtained to isolate values for ρ and C_N, and hence also $\alpha = A/2t_{\mathrm{FE}}C_N$, where we assume the other parameter values for the stack, *i.e.*, t_{FE}, A, and C_{DE}, are known.

To simulate the behavior of a realistic stack, we use the same multidomain model and parameter values for the ferroelectric as in section 3.2, including the defects. We also use the same values of parasitic inductance and capacitance ($L_{\mathrm{probe}} = 50$ pH and $C_{\mathrm{probe}} = 50$

fF), again with an error of 0.2 dB in calibration. Fig. 3.7 shows the S-parameters from the simulated measurement for a frequency range of $1 - 20$ GHz, both with and without the parasitics de-embedded. The S-parameters for the DUT with parasitics de-embedded shows an approximately constant real component of the impedance, which is consistent with (3.16) at the frequencies of interest, where the vacuum-capacitance term $j\omega\varepsilon_0 A/t_{\mathrm{FE}}$ is negligible. We extract values of ρ and α using v_{IN} with an amplitude of 100 mV and a fundamental frequency ω_0 of 10 GHz. As shown in Table 3.2, the extraction correctly reveals the expected (assigned) values.

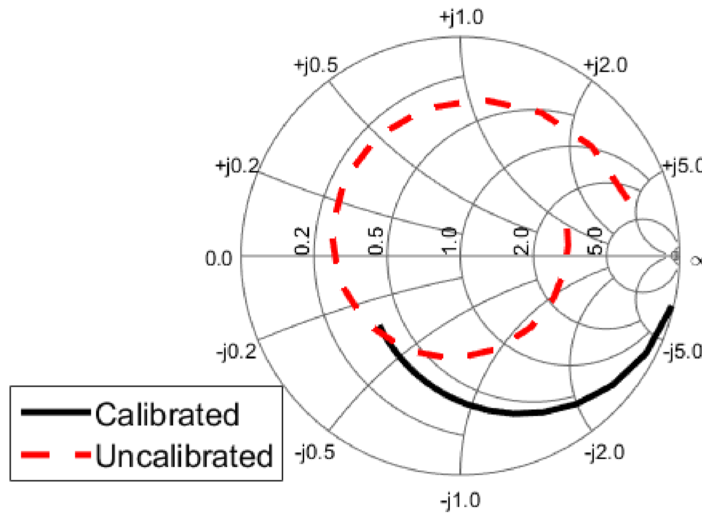

Fig. 3.7. S-parameter values with the input signal ranging from 1 – 20 GHz, with and without parasitics de-embedded.

TABLE 3.2
ASSIGNED VS. EXTRACTED FERROELECTRIC PARAMETERS

Parameter	Assigned	Extracted
ρ	1.80 mΩ·m	1.93 mΩ·m
α	-3.60×10^{8} V·m/C	-3.70×10^{8} V·m/C

3.4 Conclusions

The following conclusions can be drawn from this study of microwave S- and X-parameter techniques for the characterization of ferroelectrics for applications in FeFETs and NCFETs.

1. The large-signal X-parameter technique, in which a ferroelectric is excited by a large input sinusoid and the resulting harmonics from the highly nonlinear ferroelectric switching are measured, can be used to trace the intrinsic polarization vs. electric-field curve for the ferroelectric, from which all the LK parameters can be derived; these include the lossless LK parameters, α, β, and γ, and the loss parameter ρ.
2. The viability of the X-parameter approach is demonstrated through simulations of a measurement setup. The suggested procedure to extract values for the LK parameters from the simulated measurement data yields results that closely match the expected values.
3. A simplified small-signal S-parameter approach using a balanced capacitor stack to emulate the gate structure of an NCFET targeted for low-power logic applications can be used to extract the loss parameter ρ and the lossless parameter α, but cannot reveal the other LK parameters.

The full X-parameter technique we propose will reconstruct the entire voltage and current transients around the ferroelectric, which in turn allows an accurate reconstruction of the intrinsic polarization vs. electric-field behavior, and hence an accurate determination of all the ferroelectric parameters. On the other hand, the S-parameter approach has the advantage of greatly simplifying the measurement process but cannot reconstruct the polarization vs. electric-field behavior or reveal all the ferroelectric parameters, and it requires a balanced capacitor stack. Both methods are based on frequency-domain electrical measurements, which are familiar to the electron-device and microwave communities, and which can readily de-embed the impact of parasitics and avoid the limitations of time-domain approaches. As such, the methods described in this chapter offer useful and viable alternatives to other techniques to help speed the characterization and understanding of ferroelectrics for use in FeFET and NCFET technologies.

Chapter 4

Feedback Stabilization of a Negative-Capacitance Ferroelectric and its Application to Improve the f_T of a MOSFET[4]

4.1 Introduction

Ferroelectrics have recently received significant attention from the electron device community due to their application in negative-capacitance, field-effect transistors (NCFETs), which have emerged as a possible candidate for breaking the 60mV/decade subthreshold slope barrier and operating at low supply voltages [3], [13], [41], [82], [84]. A conventional NCFET consists of a ferroelectric in *series* with the gate of a MOSFET. Though normally unstable, the negative capacitance C_{FE} of the ferroelectric is stabilized in a conventional NCFET when the equivalent series capacitance looking into the gate is a positive value, i.e., $C_{\mathrm{gg}}C_{\mathrm{FE}}/(C_{\mathrm{gg}}+C_{\mathrm{FE}}) > 0$, where C_{gg} is the usual MOSFET gate capacitance [3]. Although the conventional NCFET structure offers voltage amplification due to the negative capacitance of the ferroelectric [19], it exhibits an increase in input capacitance [80], [84] and no improvement in unity-current-gain frequency f_T [85].

In this study, we propose a *parallel* NCFET structure (P-NCFET) that reduces the input capacitance and consequently achieves higher f_T in comparison to a conventional MOSFET. This increase makes the P-NCFET an attractive choice for application in radio-frequency (RF) integrated circuits. The key to our approach is the use of active feedback

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[4] A version of this chapter has been published [21].

in addition to capacitance matching to stably hold the ferroelectric in its negative-capacitance regime, and thus achieve the capacitance cancellation required to reduce the input capacitance. In addition to a variety of capacitance-cancellation applications, a feedback stabilization technique also directly addresses ferroelectric leakage issues, such as those identified in normal NCFETs [86]. Furthermore, since the technique allows for a discrete ferroelectric in parallel with the usual MOSFET gate, as opposed to a ferroelectric integrated into a usual MOSFET gate, there can be advantages in fabrication, with the ferroelectric introduced as a back-end-of-line (BEOL) instead of front-end-of-line (FEOL) element.

In Section 4.2, we describe the P-NCFET structure and demonstrate the viability of our method of stabilization using simple feedback. In Section 4.3, we show such a stabilized P-NCFET can achieve a significant increase in f_T compared to a conventional MOSFET. For completeness, we also consider the maximum oscillation frequency $f_{\max}$ and the $g_m f_T / I_D$ metric [85], [87], where g_m is the transconductance and I_D is the dc bias current, and we also compare the P-NCFET to a regular NCFET in addition to a conventional MOSFET. The conclusions of this study are presented in Section 4.4.

4.2 P-NCFET Structure and Feedback Stabilization

A comparison of a P-NCFET with a conventional NCFET is shown in Fig. 4.1. The proposed P-NCFET structure in Fig. 4.1(b) has a lower gate-source capacitance than the MOSFET M_1 due to partial cancellation of the gate capacitance of M_1 by the parallel negative capacitance of the ferroelectric. It is well-known that the series ferroelectric in an NCFET facilitates a voltage gain; similarly, the parallel ferroelectric in a P-NCFET facilitates a current gain that can be leveraged to increase the cutoff frequency. The NCFET with the *series* ferroelectric is balanced by the gate capacitance of the MOSFET; however, the proposed P-NCFET structure with the ferroelectric in *parallel* with the gate and source terminals of the MOSFET is inherently unstable [42]. We thus propose a simple feedback technique to stabilize the P-NCFET structure, demonstrate the stability using Nyquist criteria, and present a start-up circuit required to initialize the ferroelectric into its zero-polarization, negative-capacitance region.

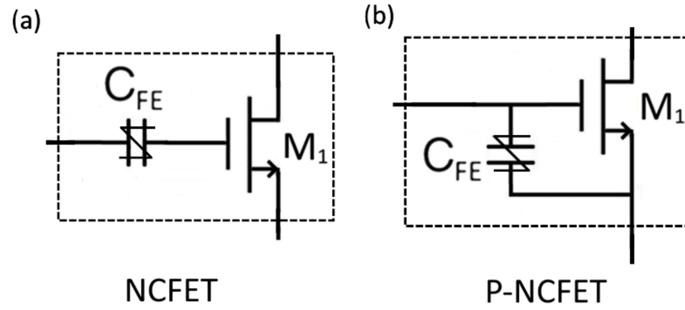

Fig. 4.1. (a) NCFET vs. (b) proposed P-NCFET.

4.2.1 Stabilizing a P-NCFET Using Feedback

Fig. 4.2(a) shows a simple current mirror used to bias a conventional MOSFET, where two extra resistors R_1 and R_2 are shown, and in Fig. 4.2(b), the mirror of Fig. 4.2(a) has been redrawn to show it can be viewed from a feedback perspective, with the gate-source capacitances C_{gs1} and C_{gs2} of M_1 and M_2, respectively, shown outside the devices themselves, where for ease of the present discussion, C_{gs} is the only component of gate capacitance considered for each MOSFET, a simplification that is removed in Section 4.2.3. In Fig. 4.2(b), the low-pass filtering action of C_{gs2} and C_{gs1} with R_2 and R_1, respectively, can be seen to block a high-frequency ac signal v_{sig} applied at the gate of M_1 from circulating in the feedback loop. The feedback operation itself can be visualized as follows, noting that all devices in a current mirror are in saturation and nominally controlled by the gate-source voltage V_{GS}: any bias deviation in the current $I_{\text{OUT}} = I_{\text{D1}}$ will be reflected as a deviation in V_{GS1} across C_{gs1} and hence in V_{GS2} across C_{gs2}, and hence finally in I_{D2}; the resulting difference (nominally zero) between $I_{\text{IN}} = I_{\text{BIAS}}$ and I_{D2} then creates the nonzero current $I = I_{\text{IN}} - I_{\text{D2}}$, which charges C_{gs1} to restore V_{GS1} and hence $I_{\text{OUT}} = I_{\text{D1}}$.

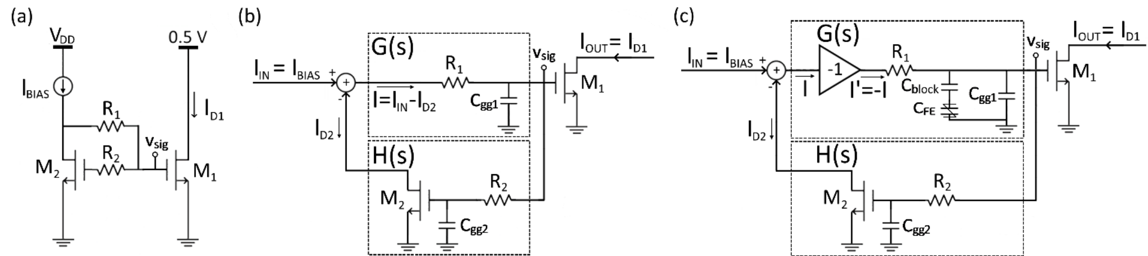

Fig. 4.2. (a) Biasing of a MOSFET M_1 using a current mirror. (b) Negative-feedback visualization of the biasing scheme in (a). (c) Biasing of a P-NCFET using the approach of (b) but with the addition of a negative unity-gain current amplifier for proper polarity.

Fig. 4.2(c) shows the configuration when M_1 is replaced by a P-NCFET, where a large blocking capacitor C_{block} is added in series with the ferroelectric to maintain dc separation between the gate of M_1 and the ferroelectric, and noting the ferroelectric must be biased at 0 V to realize a negative value for C_{FE} while M_1 must be biased in saturation with V_{GS1}~0.5 V. The feedback operation is the same as for the circuit of Fig. 4.2(b), except a negative unity-gain current amplifier ($I' = -I$) is required in the feedback path since the gate capacitance of the P-NCFET $C_{\text{FE}} + C_{\text{gs1}}$ is designed to be *negative* for stable operation, as explained in Section 4.2.2, thus requiring the opposite polarity of net restorative charge.

4.2.2 Stability and Loop Gain

4.2.2.1 Circuit Realization

A circuit realization of the feedback stabilization approach of Fig. 4.2(c) is shown in Fig. 4.3, where the current mirror formed by identically sized M_3 and M_4 implements the negative unity-gain current amplifier.

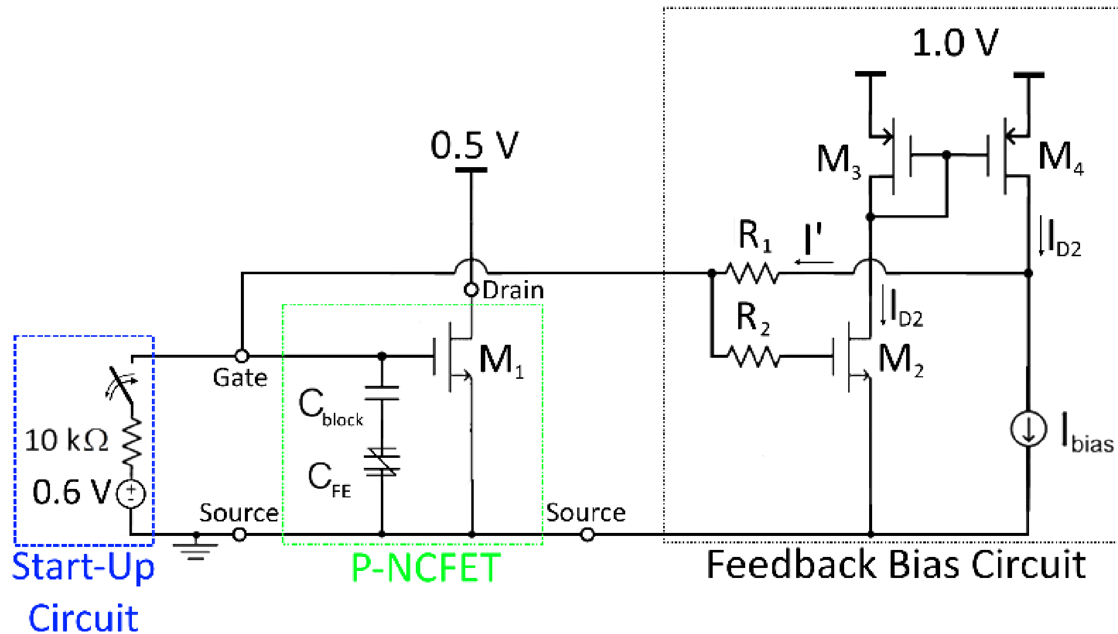

Fig. 4.3. Circuit implementation of the approach illustrated in Fig. 4.2(c). The current mirror formed by identically sized M_3 and M_4 implements the negative unity-gain current amplifier. The labeled gate and source on the left on the left of M_1, and drain and source above and to the right of M_1, indicate the usual small-signal input and output ports, respectively, of the P-NCFET.

To demonstrate the viability of the approach, the circuit was implemented using a 65-nm CMOS TSMC process design kit (PDK) and the Landau-Khalatnikov (LK) [9], [10] ferroelectric model, and the relevant operation verified. The main transistor M_1 was chosen to have a gate length $L = 60$ nm (minimum for the PDK) and a gate width $W =$ 3.3 μm per finger $\times$ 30 fingers, with the latter chosen so that 10 mA of drain current corresponds to a gate-source voltage of ~0.5 V and a drain-source voltage of 0.5 V for a rated supply voltage of 1V. With these design parameters, the gate-source capacitance of M_1 is $C_{\mathrm{gs1}} \approx 60$ fF. For the ferroelectric, the full nonlinear, time-dependent, hysteretic behavior indicated by the LK model was implemented, with the following ferroelectric parameters of HfO_2: S-curve coefficients $\alpha = -3.60 \times 10^8$ V·m/C, $\beta = 2.25 \times 10^{10}$ V·m^5/C^3, and $\gamma = 1.67 \times 10^9$ V·m^9/C^5 [41], and a loss coefficient ρ of 1.8 mΩ·m extracted from experimental results [42]. The ferroelectric has an area $A_{\mathrm{FE}} = 0.9$ μm^2 and a thickness $t_{\mathrm{FE}} = 10$ nm, resulting in an approximate capacitance $C_{\mathrm{FE}} \approx -130$ fF in the zero-polarization state, a desired value substantiated in Section 4.3. Since studies show that a single domain is important for the realization of NC effects [88], [89], we assume a ferroelectric obeying single-domain LK dynamics. Given the ferroelectric in a P-NCFET is not a part of the FET gate stack like in an NCFET, but is a BEOL element, single-domain behavior can be achieved by techniques applicable to a standalone nanostructure [90], [91].

The bias transistors M_2-M_4, resistors R_1, R_2 and the dc blocking capacitor C_{block} are chosen to minimize parasitic loading and minimize impact on the high-frequency operation of the P-NCFET. Transistor M_2 has $L = 60$ nm and $W = 3.3$ μm per finger $\times$ 3 fingers to facilitate a ratio $I_{\mathrm{D1}}/I_{\mathrm{BIAS}} = 1/10$, and transistors M_3 and M_4 have $L = 180$ nm and $W =$ 5.2 μm per finger $\times$ 15 fingers to minimize channel-length modulation effects on the current mirror [92]. R_1 and R_2 were set to 500 kΩ and 100 kΩ, respectively, so that R_2 is sufficiently smaller than R_1 to maintain feedback stability as explained in Section 4.2.2.2. C_{block} was set to approximately 20 times $|C_{\mathrm{FE}}|$ to enable dc blocking without affecting ac performance.

4.2.2.2 Feedback Stability

It is well-known that a feedback system is stable if the *closed-loop* transfer function has no right half-plane (RHP) poles, and that by the Nyquist criterion, the number of RHP poles in the closed-loop transfer function equals $P_{\mathrm{GH}} - N_{\mathrm{CCW}}$, where P_{GH} is the number of RHP poles in the *open-loop* transfer function and N_{CCW} is the number of counterclockwise encirclements of -1 in the Nyquist plot, where the latter plot is a locus of the *open-loop* transfer function in the complex plane as the frequency is swept [44].

A simplified expression for the open-loop transfer function of the P-NCFET feedback circuit in Fig. 4.3 can be found by making a few assumptions consistent with the final circuit design goals. The negative unity-gain current amplifier implemented by the current mirror formed by M_3 and M_4 can be assumed to have infinite bandwidth and a gain of exactly one. We also assume the poles in the open-loop transfer function are significantly separated, by approximating R_1 as much larger than both R_2 and the output resistance r_{o4} of M_4. With these approximations, the open-loop transfer function from Fig. 4.3 can be expressed as

$$G(s)H(s) = \frac{-g_{m2}r_{o4}}{[1 + sR_1(C_{\mathrm{gs1}} + C_{\mathrm{FE}})][1 + sR_2C_{\mathrm{gs2}}][1 + sr_{\mathrm{o4}}C_{\mathrm{d4}}]} \tag{4.1}$$

where $G(s)$ is the transfer function of the forward block [shown explicitly in Fig. 4.2(c)], $H(s)$ is the transfer function of the feedback block, $C_{\mathrm{gs1}} + C_{\mathrm{FE}}$ is the equivalent gate-source capacitance of the P-NCFET, and $g_{\mathrm{m}i}$, r_{oi}, $C_{\mathrm{gs}i}$, and $C_{\mathrm{d}i}$ are the transconductance, output resistance, gate-source capacitance, and total drain capacitance of the i-th transistor M_i, respectively. We emphasize that the simplified form (4.1) is used only to provide insight, with all our final results here and in Section 4.3 based on full circuit simulations.

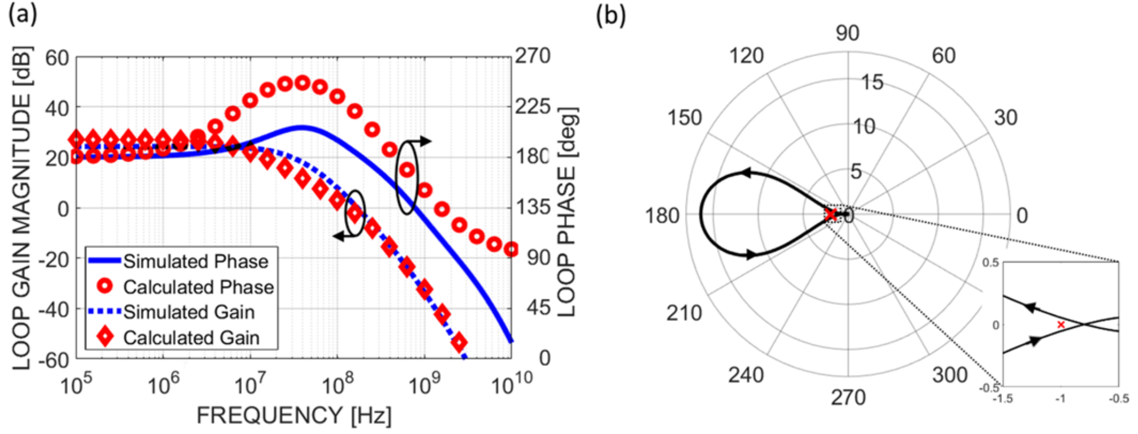

Fig. 4.4. (a) Magnitude and phase of the open-loop transfer function for the feedback stabilized P-NCFET circuit, calculated from (4.1) and from full circuit simulation. (b) Nyquist plot of the open-loop transfer function with 'x' denoting the -1 point. The inset shows a zoomed view around the -1 point. The Nyquist plot makes a single counterclockwise encirclement around -1.

We first choose $C_{\mathrm{gs1}} + C_{\mathrm{FE}}$ to be negative, so that (4.1) indicates the open-loop transfer function $G(s)H(s)$ has two poles (involving $R_2 C_{\mathrm{gs2}}$ and $r_{o4} C_{d4}$) in the left half-plane (LHP) and one pole [involving $R_1(C_{gs1} + C_{FE})$] in the RHP. We further choose R_1 to be much larger than R_2 and r_{o4}, consistent with how (4.1) is obtained, and the magnitude of the dc gain $g_{m2} r_{o4}$ is set to be greater than unity.

To demonstrate how these choices are sufficient to achieve stability, consider the limiting case where the RHP pole at $-1/[R_1 (C_{\mathrm{gs1}} + C_{\mathrm{FE}})]$ is much lower than ω_{GH}, where ω_{GH} is the frequency at which the open-loop gain $|G(s)H(s)| = 0$ dB, and where the two LHP poles (involving R_2 and r_{o4}) are much higher than ω_{GH} and can hence be neglected.

A bode plot of $G(s)H(s)$ would then show the phase beginning at 180° and a magnitude greater than unity, and the phase increasing due to the $-1/[R_1 (C_{\mathrm{gs1}} + C_{\mathrm{FE}})]$ pole toward a value of 270° at ω_{GH}, where the magnitude would be exactly one.

It then follows that the Nyquist plot of this $G(s)H(s)$ must show a lower half loop with a counterclockwise encirclement of -1, and the full Nyquist plot would show a complete counterclockwise encirclement of -1. Since the open-loop transfer function has one RHP pole, i.e., $P_{\mathrm{GH}} = 1$, and the Nyquist plot has one counterclockwise encirclement of -1, i.e.,

$N_{\text{CCW}} = 1$, then $P_{\text{GH}} - N_{\text{CCW}} = 0$ and the feedback circuit must be stable. Simulation confirms this approach, with the choices $R_1 = 5R_2$ and $g_{m2}r_{o4} = 16.4$ sufficient for stability, as demonstrated in Fig 4.4.

Fig. 4.4(a) shows a bode plot of the open-loop transfer function from full simulation of the feedback circuit in Fig. 4.3. The bode plot shows a 20 dB/dec drop in magnitude around 10 MHz accompanied by a $+45°/\text{dec}$ phase shift over 2 decades, which confirms the presence of a single RHP pole, i.e., $P_{\text{GH}} = 1$, as expected from (4.1). Fig. 4.4(b) shows a Nyquist plot of the same open-loop transfer function which has one counterclockwise encirclement of -1, i.e., $N_{\text{CCW}} = 1$, also as expected from (4.1). Therefore, $P_{\text{GH}} - N_{\text{CCW}} = 0$ and the feedback circuit of Fig. 4.3, as implemented, is indeed stable.

4.2.2.3 Impact of Other Elements on Stability

The previous analysis and the derivation of (4.1) assumed only the gate-source component C_{gs} of the total effective gate capacitance C_{gg} of the MOSFETs impact the feedback stability; however, more generally, the gate-drain component C_{gd} could also play a role and should be considered.

For example, if the C_{gd} components of M_1 and M_2 are non-negligible, the capacitances C_{gs1} and C_{gs2} in (4.1) must be modified to represent the total effective capacitance from the gate node to the source node of each FET. C_{gs1} in (4.1) would be replaced with $C_{\text{gs1}} + C_{\text{gd1}}$, and C_{gs2} in (4.1) would be replaced with $C_{\text{gs2}} + C_{\text{M2}}$, where C_{M2} is the Miller capacitance of M_2 [93].

In a practical application of the P-NCFET as an amplifier where a signal source and load are connected to the gate and drain of M_1, respectively, both the Miller capacitance of M_1 and the output impedance of the signal source must be considered in calculating the total effective capacitance from the gate node to the source node of M_1.

As explained in Section 4.2.2.2 above, the feedback circuit will be stable when there is one RHP in the open-loop transfer function at a frequency much lower than all the LHP poles. If we assume any additional parasitic elements, e.g., the gate, source, and drain resistances, or the ρ of the ferroelectric, are non-negligible, then the only impact on the

feedback stability would be either to add LHP poles or move existing poles; in such cases, it is sufficient to simply increase the magnitude of C_{FE} or R_1 to maintain a low RHP pole and ensure stability in the manner already discussed.

4.2.3 Startup Circuit

The previous analysis demonstrated stability of the feedback portion of Fig. 4.3 with the ferroelectric already balanced around its zero-polarization point, shown in Fig. 4.5(a) as point **D** in the lossless 'S'-shaped charge vs. voltage (Q_{FE} vs. V_{FE}) curve, where $Q_{\mathrm{FE}} = (\varepsilon_0 E_{\mathrm{FE}} + P_{\mathrm{FE}})A_{\mathrm{FE}}$ is the charge, with $E_{\mathrm{FE}} = V_{\mathrm{FE}}/t_{\mathrm{FE}}$ and P_{FE} being the electric field and polarization, respectively, for the ferroelectric. However, a start-up circuit to push the ferroelectric to this point is necessary if the ferroelectric begins in a different polarization, e.g., in one of the usual stable states **A** or **A'**. To design this start-up circuit, we must understand how the feedback circuit responds to a ferroelectric with nonzero polarization.

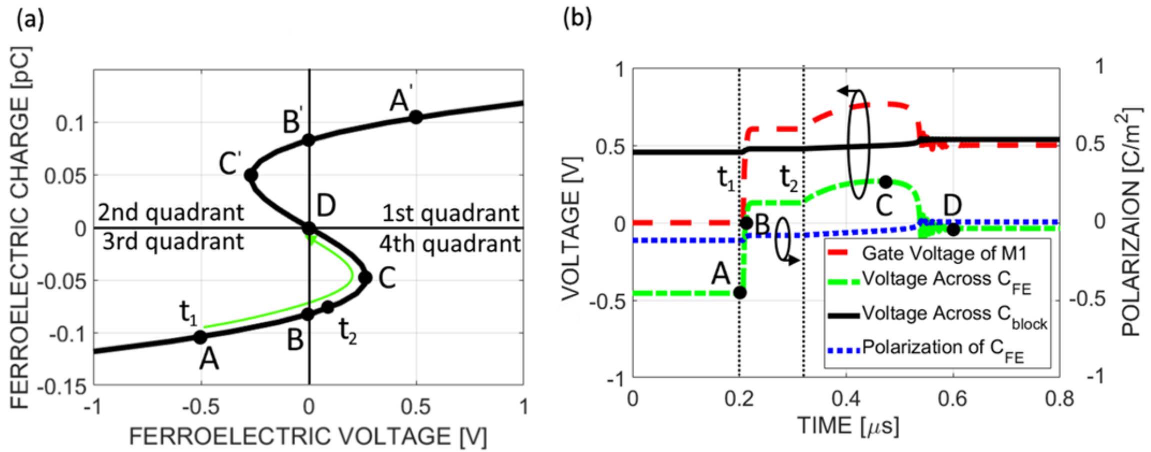

Fig. 4.5. (a) 'S'-shaped polarization curve of the ferroelectric, including a trajectory discussed in Section 4.2.3. (b) transient gate voltage (red), ferroelectric voltage (green), blocking capacitor voltage (black), and polarization (blue). Corresponding ferroelectric states and when they occur during transient are marked on both plots.

We first note that with the chosen parameters of our circuit, the desired bias value of I_{D1} corresponds to a voltage of $\sim$0.5 V at the gate node of M_1, and the blocking capacitor will dc shift that voltage by -0.5 V such that the dc voltage across the ferroelectric is approximately 0 V, positioning it at state **D** in Fig. 4.5(a). Thus, the feedback circuit is

designed to restore charge to move the ferroelectric back toward **D** if it deviates into the 2nd or 4th quadrant, i.e., *to reduce charge if the ferroelectric voltage is negative and to increase charge if the ferroelectric voltage is positive.*

If we then assume the ferroelectric is initially in state **A** in Fig. 4.5(a), with a voltage $V_{\mathrm{FE}} = -0.5$ V, corresponding to the lower power rail of the feedback circuit, and with the gate voltage of M_1 then being 0 V, then the feedback circuit will continue to rail and hold the ferroelectric in state **A**. To push the ferroelectric into state **D**, an external voltage source of 0.6 V (shown on the far left of Fig. 4.3) is momentarily connected to the circuit to push the ferroelectric into region **BC** in the 4th quadrant. When this external voltage source is then disconnected, the feedback circuit will cause the charge on the ferroelectric to increase until it reaches state **D**.

To demonstrate this process, we simulate the circuit in Fig. 4.3 with the ferroelectric polarization initially set to state **A** and the external voltage source of 0.6 V connected at time t_1 and disconnected at time t_2. When the external voltage source is disconnected, the feedback circuit continually pushes charge onto the ferroelectric until it reaches approximately 0 C/m^2 polarization. The corresponding trajectory on the 'S' curve, with timestamps t_1 and t_2, are also shown in Fig. 4.5(a); similarly, the labeled ferroelectric states (**A** through **D**) traversed over the course of the start-up transient are marked in Fig. 4.5(b). We note in this traversal that the ferroelectric capacitance in region **BC** is positive, and by extension the capacitance $C_{\mathrm{gs1}} + C_{\mathrm{FE}}$ to ground from the gate of M_1 is positive; therefore, the additional charge pushed onto the ferroelectric by the feedback circuit during the excursion from **B** to **C** causes the gate voltage of M_1 to temporarily increase and overshoot the start-up circuit drive voltage of 0.6 V. This overshoot continues until the system reaches state **C** at approximately 0.5 μs. Beyond this point, when the ferroelectric enters region **CD**, the total gate capacitance $C_{\mathrm{gs1}} + C_{\mathrm{FE}}$ becomes negative, so that the charge being pushed onto the ferroelectric causes the gate voltage of M_1 to decrease, arriving finally at approximately 0.5 V, as expected.

In the case that the ferroelectric is not initially in state **A**, but at an arbitrary polarization, simply grounding the gate of M_1 will push the ferroelectric into state **A**, after which the start-up circuit can operate as normal.

In addition, although we have used precisely 0.5 V for the value of the dc shift, such an exact value is not essential, and the circuit will operate properly as long as the ferroelectric is in the **CC'** region; in our own simulation, the ferroelectric has a polarization slightly above 0 C/m^2 at steady-state, as shown in Fig. 4.5(b).

Finally, while there is significant polarization change and by extension charge movement throughout the start-up process, the voltage $V_{\mathrm{block}} \approx 0.5$ V across the blocking capacitor does not significantly change, since $C_{\mathrm{block}} \gg |C_{\mathrm{FE}}|$. Thus, the approximation $V_{\mathrm{FE}} \approx V_{\mathrm{GS1}} - 0.5$ V continues to hold throughout the entire start-up transient, as shown in Fig. 4.5(b).

4.3 RF Figures of Merit

The biased and stabilized P-NCFET, shown boxed in Fig. 4.3, can be considered as being in a standard common-source, two-port configuration for small-signal applications. In this section, we show that the resulting unity-current-gain frequency f_T of the P-NCFET can be substantially improved in comparison to that of the MOSFET M_1. For completeness, we also examine an NCFET replacing the P-NCFET in Fig. 4.3, formed simply by placing the same ferroelectric used in the P-NCFET in series with the gate of M_1, rather than in parallel with the gate and source. Finally, for completeness, in addition to f_T, we also consider the maximum oscillation frequency f_{max}, and the metric $g_m f_T / I_D$ [85], [87].

4.3.1 High f_T Benefit of a P-NCFET

As already discussed, a negative ferroelectric capacitance C_{FE} is used to partially cancel the gate capacitance of M_1 in Fig. 4.3, reducing the input capacitance applicable to the P-NCFET and hence increasing its f_T in comparison to that of the conventional MOSFET M_1. Since the gate of the P-NCFET is also the gate of M_1, the transconductance of the P-NCFET is equal to that of M_1. If the gate capacitance is the only parasitic determining f_T, then the expected improvement can be expressed as

$$f_{\mathrm{T,P-NCFET}} \approx \left|\frac{g_{\mathrm{m1}}}{2\pi(C_{\mathrm{gg1}} + C_{\mathrm{FE}})}\right| = \left|\frac{C_{\mathrm{gg1}}}{C_{\mathrm{gg1}} + C_{\mathrm{FE}}}\right| f_{\mathrm{T,MOS}} \tag{4.2}$$

where g_{m1} is the transconductance of M1 and the P-NCFET, $f_{\mathrm{T,P-NCFET}}$ is the unity-current-gain frequency of the P-NCFET, and $f_{\mathrm{T,MOS}}$ is the unity-current-gain frequency of the MOSFET. The design parameters of M_1 yield a gate capacitance $C_{\mathrm{gg1}} \approx 85$ fF. As mentioned in Section 4.2.2.1, the size of the ferroelectric was chosen so that $C_{\mathrm{FE}} \approx -130$ fF, which was done to achieve a reduction of approximately 50% in gate capacitance. Additional cancellation might be possible, but would have to be weighed in any implementation against potential challenges posed by variation of gate-source capacitance over process corners. From (4.2), the maximum f_T improvement of the P-NCFET over the MOSFET M_1 in our circuit of Fig. 4.3 is thus a factor of approximately two.

For the NCFET formed by placing the ferroelectric in series with the gate of M_1, if we again assume the gate capacitance is the only parasitic determining f_T, then f_T is expected to be the same as the f_T of the MOSFET, because both C_{gg} and g_{m} increase by the same factor [85]:

$$g_{\mathrm{m,NCFET}} \approx \frac{C_{\mathrm{FE}}}{C_{\mathrm{gg1}} + C_{\mathrm{FE}}} g_{\mathrm{m1}} \tag{4.3a}$$

$$C_{\mathrm{gg,NCFET}} \approx \frac{C_{\mathrm{FE}}}{C_{\mathrm{gg1}} + C_{\mathrm{FE}}} C_{\mathrm{gg1}} \tag{4.3b}$$

For all devices, we note that the ρ of the ferroelectric does not have a significant impact on f_T. For the NCFET, the ferroelectric appears in series at the input port and is hence immaterial to current gain irrespective of the value of ρ. For the P-NCFET, where the ferroelectric is in parallel at the input port, ρ yields a resistance that is much lower than the impedance of C_{FE} at the frequencies of interest, i.e., those from which f_T is extrapolated, and is hence also immaterial to the f_T, with the main impact of the ferroelectric being capacitance cancellation.

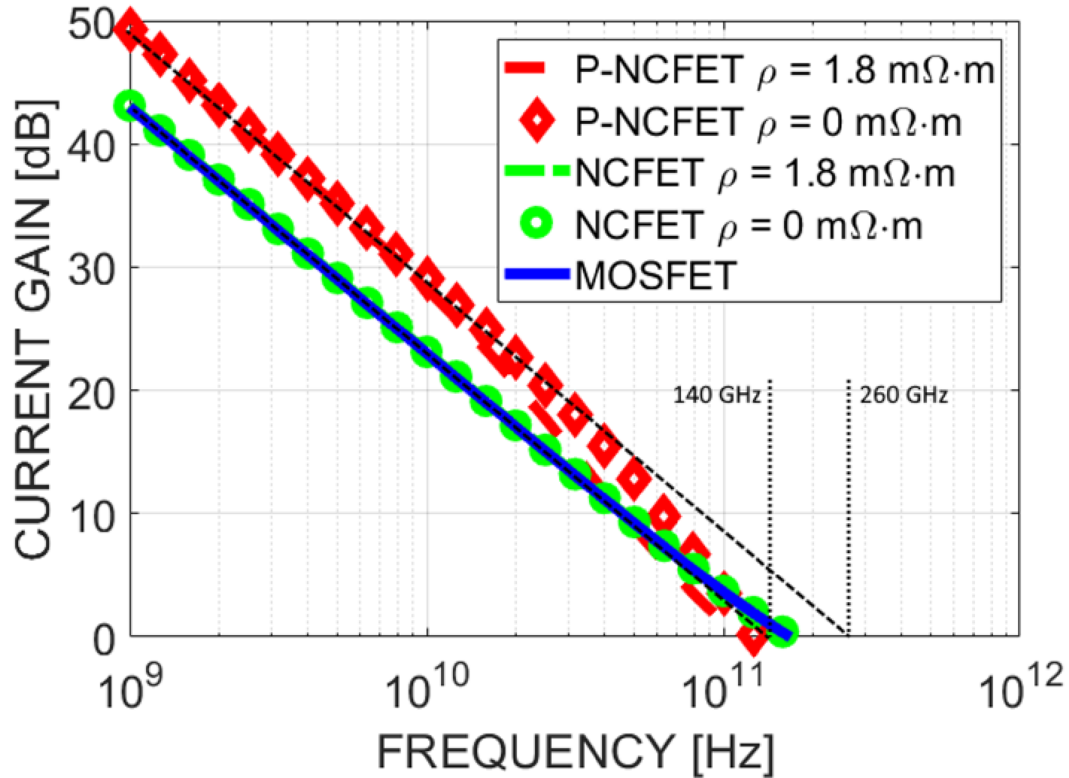

Fig. 4.6. Simulated current gain of the P-NCFET (red), the NCFET (green), and the standard MOSFET (blue). All devices are biased at 10 mA of drain current. The current gain of the NCFET is identical to the standard MOSFET, as expected.

The magnitude of the short-circuit current gain $|h_{21}|$ is extracted for all devices, with the result displayed in Fig. 4.6. The extrapolated f_T of the P-NCFET is 260 GHz, approximately double that of the conventional MOSFET at 140 GHz, an outcome of the implemented capacitance cancellation, while the f_T values of the NCFET and MOSFET are identical, all independent of ρ, as expected.

4.3.2 $f_{\max}$ of a P-NCFET

$f_{\max}$ is extracted from Mason's unilateral power gain U [94] – [96], plotted for all devices in Fig. 4.7, and which can be specified in terms of the two-port h-parameters:

$$U = \frac{|h_{21} + h_{12}|^2}{4[\mathrm{Re}(h_{11})\mathrm{Re}(h_{22}) + \mathrm{Im}(h_{21})\mathrm{Im}(h_{12})]} \tag{4.4}$$

Further insight can be gained by also considering the well-known basic formula for $f_{\max}$ [97], even though more involved expressions (e.g., [Eq. (8), 97]) are available:

$$f_{\max} \approx \sqrt{\frac{f_T}{8\pi R_g C_{\mathrm{gd}}}} \tag{4.5}$$

where R_g is the gate resistance of the FET.

We first consider the case when $\rho = 0$, i.e., when the ferroelectric is lossless. Since Mason's gain U is invariant to the addition of any lossless element (in series or parallel) at the input port [96], then we can expect $f_{\max}$ to be identical for all devices when $\rho = 0$, which is confirmed in Fig. 4.7 (with only small differences in the low-frequency values of U, arising from the impact of biasing on the dc power gain).

When $\rho > 0$, the changes in $f_{\max}$ are best understood through (4.5). For the NCFET, the addition of a lossy series element (the ferroelectric) at the input port effectively increases R_g while f_T remains unaffected, causing a decrease in $f_{\max}$ from the MOSFET case, as illustrated in Fig. 4.7. For the P-NCFET, we would expect that an increase in f_T over the MOSFET would *increase* $f_{\max}$ over the MOSFET; however, despite having the ferroelectric in parallel with the gate-source terminals, R_g for the P-NCFET is even greater than for the NCFET, offsetting the increase in f_T and leading to an overall decrease in $f_{\max}$ in comparison to the MOSFET, with the decrease being on par with that for the NCFET. Here, the extra increase in R_g for the P-NCFET case can be shown to occur due to the presence of a *parallel negative and lossy capacitance* at the input port of the P-NCFET vs. the series connection in the NCFET, which causes a larger increase in R_g looking into the input port of the P-NCFET vs. the NCFET when $\rho > 0$. These results are all borne out in Fig. 4.7, with the following observable values: the extrapolated $f_{\max}$ of the P-NCFET with $\rho = 1.8$ mΩ·m is 74 GHz; the extrapolated $f_{\max}$ of the NCFET with $\rho = 1.8$ mΩ·m is 68 GHz; and the extrapolated $f_{\max}$ of the MOSFET is 119 GHz. The reduction in $f_{\max}$ for both the NCFET and P-NCFET when $\rho > 0$ emphasizes that low-loss ferroelectrics are desirable for RF applications.

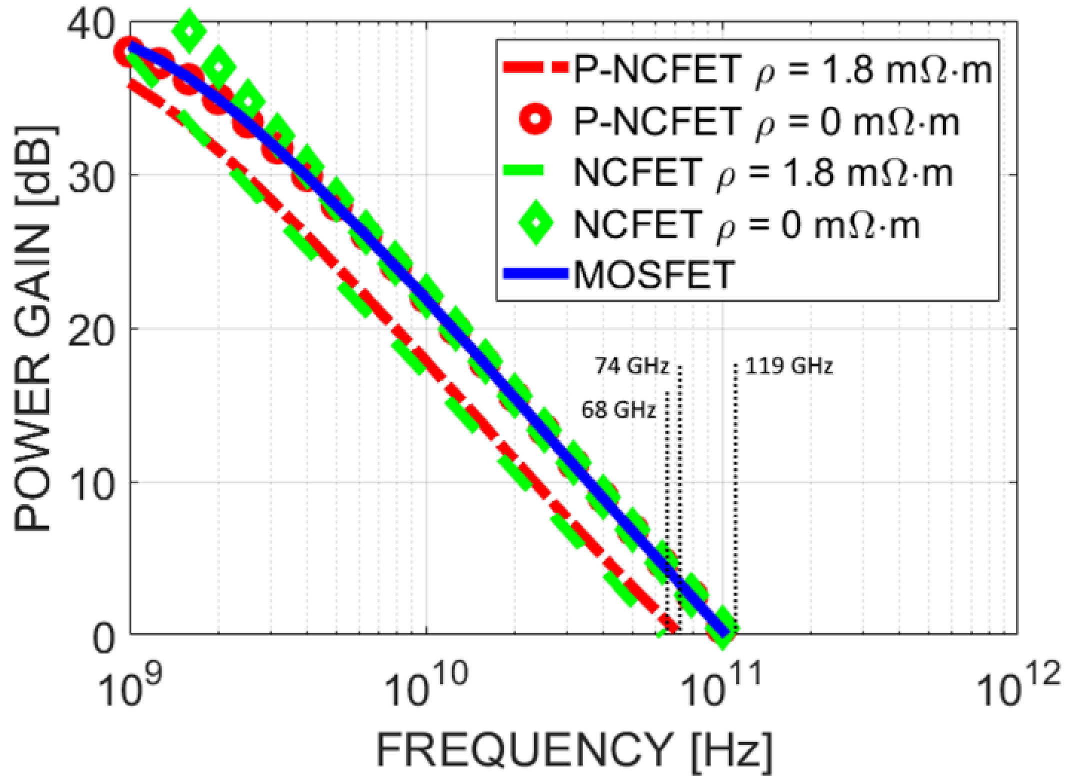

Fig. 4.7. Simulated unilateral power gain of the P-NCFET (red), NCFET (green), and the standard MOSFET (blue). All devices are biased at 10 mA of drain current. The power gain of the P-NCFET and NCFET with $\rho = 0$ mΩ·m is identical to the standard MOSFET as expected.

4.3.3 $g_m f_T / I_D$ of a P-NCFET

As explained in Section 4.3.1, the g_m of the P-NCFET is identical to that of the conventional MOSFET, and the f_T of the P-NCFET is double that of the conventional MOSFET for the capacitance cancellation we have chosen. Thus, the $g_m f_T / I_D$ improvement is also expected to be approximately a factor of two.

From (4.3a), the g_m of the NCFET is three times that of the conventional MOSFET for the values of capacitances we have chosen, while the f_T remains the same as the MOSFET. Thus, the $g_\mathrm{m} f_\mathrm{T} / I_\mathrm{D}$ improvement is also expected to be approximately a factor of three.

Fig. 4.8 shows that the P-NCFET achieves approximately double the $g_m f_T / I_D$ of the MOSFET, while the NCFET achieves approximately triple the $g_m f_T / I_D$ of the MOSFET, as expected.

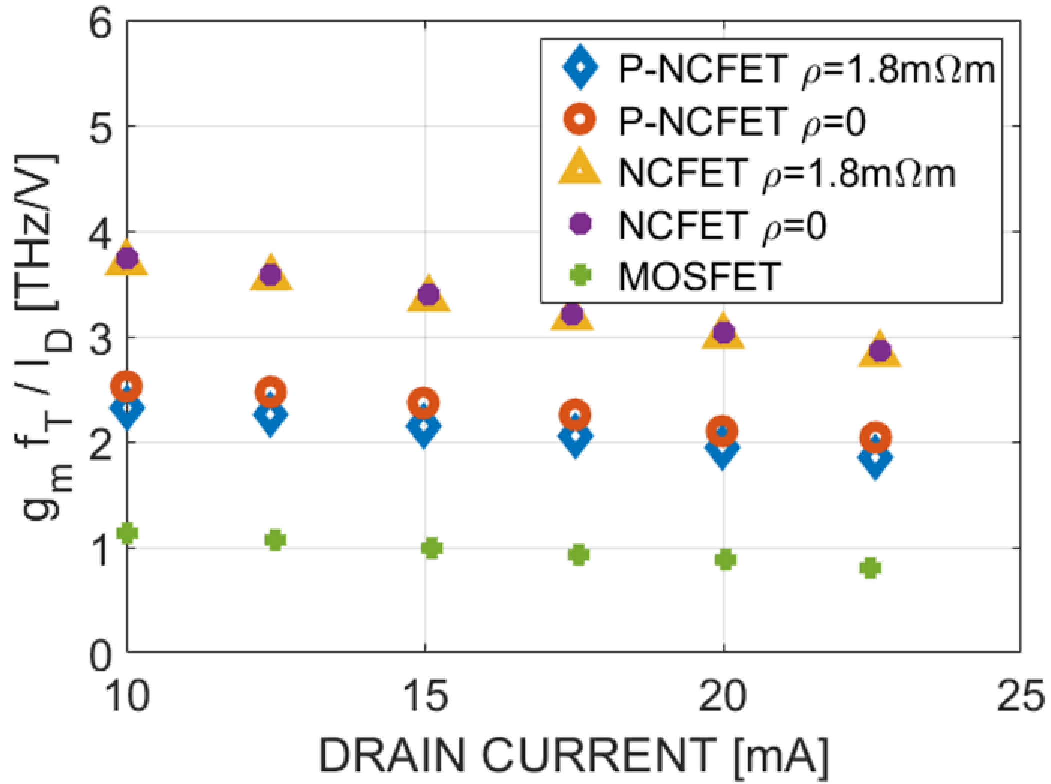

Fig. 4.8. $g_m f_T / I_D$ plotted against dc drain current, with $V_D = 0.5$ V for all devices and the same I_D between devices achieved by adjusting I_{bias}.

4.4 Conclusion

The following conclusions can be drawn from this study on the use of active feedback to stabilize a ferroelectric operating in its negative-capacitance regime and its application to achieve capacitance cancellation.

1. Instead of a conventional series configuration used in an NCFET, a ferroelectric can be placed in *parallel* with the usual gate capacitance of a MOSFET, yielding a new P-NCFET structure [Fig. 4.1(b)]. The sum of the negative capacitance and traditional MOSFET gate capacitance is lower in magnitude than that of the MOSFET itself, offering the possibility of improved high-frequency performance and demonstrating the idea of capacitance cancellation.

2. For the capacitance cancellation to work, an active feedback circuit is designed to stabilize the ferroelectric in its negative-capacitance region [Fig. 4.2(c) and Fig. 4.3].
3. The stability of the feedback circuit is demonstrated through classical stability analysis and the Nyquist criterion [Fig. 4.4].
4. A start-up circuit is proposed to push the ferroelectric into the negative capacitance region from any initial polarization, and the viability of the start-up circuit is demonstrated through transient simulation [Fig. 4.5].
5. The short-circuit current gain of the biased and stabilized P-NCFET viewed as a two-port vs. that of the traditional MOSFET show that the extrapolated f_T for the P-NCFET is significantly higher than that for the traditional MOSFET [Fig. 4.6].
6. While the higher f_T for the P-NCFET is accompanied by a moderate decrease in $f_{\max}$ [Fig. 4.7], the $g_m f_T / I_D$ improves significantly [Fig. 4.8].

Overall, this study shows a possible new way for ferroelectrics to be used for improved performance metrics in IC designs by leveraging their negative capacitance to achieve capacitance cancellation. The approach is illustrated in this study by a new P-NCFET structure with significantly higher f_T and $g_m f_T / I_D$ than a conventional MOSFET, even if the $f_{\max}$ may decrease, as with a regular NCFET, depending on the value of ρ. While the approach requires active feedback to stabilize the ferroelectric in its negative-capacitance region, it is demonstrated to have promise with careful simulations employing a full dynamic model for the ferroelectric based on the LK formalism. Additionally, since the cancellation approach requires a discrete ferroelectric in parallel with the usual MOSFET gate, as opposed to a ferroelectric integrated into a usual MOSFET gate, there can be advantages in fabrication, with the ferroelectric introduced as a BEOL vs. FEOL element. Such introduction and use of negative capacitance may thus open new potential uses for ferroelectrics in the electron-device community.

Chapter 5

Conclusion and Future Work

5.1 Summary of Contributions

In this chapter, we summarize the main contributions from each stage of work. The work leading to the conclusions listed here is detailed in the previous chapters.

5.1.1 Stage 1 (Chapter 2)

The specific contributions from the first stage, "Switching-Speed Limitations of Ferroelectric Negative-Capacitance Field-Effect Transistors," are summarized as follows:

1. Current studies on NCFETs focus on static measurements of subthreshold slope. We have identified an additional parameter ρ that strongly influences the high-frequency response of ferroelectric materials.
2. Our transient switching simulation results show that while ferroelectrics do have the potential to provide voltage amplification and hence an enhanced response to gate voltages in the MHz range, they may cease to provide this advantage in the GHz to THz range, unless the viscosity coefficient ρ is sufficiently low.
3. Ferroelectric materials must have a viscosity coefficient ρ less than 0.1 $\Omega \cdot$m to achieve voltage amplification with a 1-ps rise time.

This work demonstrates a close match between our model to experiment. By illuminating the requirement on ρ (below 0.1 $\Omega \cdot$m) for high-speed applications, we highlight an aspect

of ferroelectric materials that should be considered for GHz to THz operations.

5.1.2 Stage 2 (Chapter 3)

The specific contributions from the second stage, "Toward Microwave S- and X-Parameter Approaches for the Characterization of Ferroelectrics for Applications in FeFETs and NCFETs," are summarized as follows:

1. The large-signal X-parameter technique, in which a ferroelectric is excited by a large input sinusoid and the resulting harmonics from the highly nonlinear ferroelectric switching are measured, can be used to trace the intrinsic polarization vs. electric-field curve for the ferroelectric, from which all the LK parameters can be derived; these include the lossless LK parameters, α, β, and γ, and the loss parameter ρ.
2. The viability of the X-parameter approach is demonstrated through simulations of a measurement setup. The suggested procedure to extract values for the LK parameters from the simulated measurement data yields results that closely match the expected values.
3. A simplified small-signal S-parameter approach using a balanced capacitor stack to emulate the gate structure of an NCFET targeted for low-power logic applications can be used to extract the loss parameter ρ and the lossless parameter α, but cannot reveal the other LK parameters.

The X-parameter and S-parameter techniques we propose are based on frequency-domain electrical measurements, which are familiar to the electron-device and microwave communities, and which can readily de-embed the impact of parasitics and avoid the limitations of time-domain approaches. As such, the methods described in this chapter offer useful techniques to help the characterization and understanding of ferroelectrics.

5.1.3 Stage 3 (Chapter 4)

The specific contributions from the third stage, "Feedback Stabilization of a Negative-Capacitance Ferroelectric and its Application to Improve the f_T of a MOSFET," are summarized as follows:

1. Instead of a conventional series configuration used in an NCFET, a ferroelectric can be placed in *parallel* with the usual gate capacitance of a MOSFET, yielding a new P-NCFET structure. The sum of the negative capacitance and traditional MOSFET gate capacitance is lower in magnitude than that of the MOSFET itself, offering the possibility of improved high-frequency performance and demonstrating the idea of capacitance cancellation.
2. For the capacitance cancellation to work, an active feedback circuit is designed to stabilize the ferroelectric in its negative-capacitance region, and the stability of the feedback circuit is demonstrated through classical stability analysis and the Nyquist criterion.
3. The short-circuit current gain of the biased and stabilized P-NCFET viewed as a two-port vs. that of the traditional MOSFET show that the extrapolated f_T for the P-NCFET is significantly higher than that for the traditional MOSFET.

This study shows a possible new way for ferroelectrics to be used for improved performance metrics in IC designs. The approach is illustrated in this study by a new P-NCFET structure with significantly higher f_T than a conventional MOSFET. Additionally, the use of a discrete ferroelectric in parallel with the usual MOSFET gate, as opposed to a ferroelectric integrated into a usual MOSFET gate, may open new potential uses for ferroelectrics via back-end-of-line (BEOL) integration in the electron-device community.

5.2 Future Work - Evaluation of Ferroelectrics as BEOL Elements in ICs Through a Tuned Oscillator

While the previous study demonstrated a new application for ferroelectrics in a P-NCFET instead of a conventional NCFET, the feedback stability mechanism provides more opportunities for incorporating ferroelectrics into circuit designs, particularly as BEOL elements **[18]**. Our next step towards more advanced circuit applications is to create an oscillator with a BEOL ferroelectric. A standard inductor is much larger than other structures on an IC chip [98], as shown in Fig. 5.1. An oscillator using the negative capacitance of a BEOL ferroelectric would be much smaller than a standard oscillator using inductors. The outcome of this study, like the study done in Chapter 4, will hence be another important step in showing the potential of ferroelectrics as BEOL elements, with many applications that could then be further probed; for example, the use of a BEOL ferroelectric to cancel load capacitance in a digital circuit and improve power-delay performance. As discussed in DRC 2021 [99], BEOL applications are likely to be the first use of negative-capacitance ferroelectrics in modern ICs.

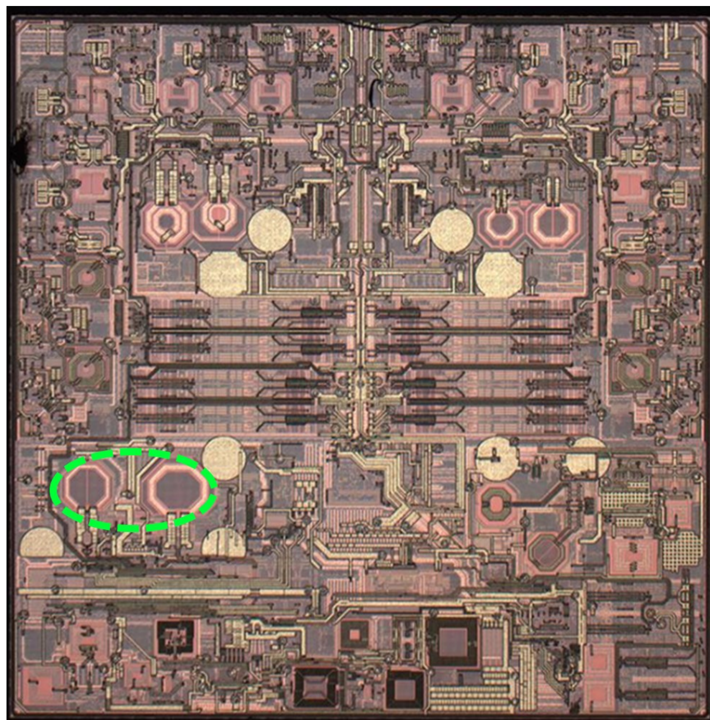

Fig 5.1 Image of 28-nm RF transceiver die [*taken directly* from Fig. 1.7, 98] with inductor coils circled in green.

The feedback circuit we presented in Chapter 4 relies on the negative capacitance of a BEOL ferroelectric at zero polarization to achieve stable negative feedback. By connecting a positive tuned capacitor in parallel with a ferroelectric, the total capacitance can be designed to exhibit a positive capacitance near zero polarization sandwiched by two negative-capacitance regions at higher values of polarization, as shown in Fig. 5.2. Using the negative feedback of Chapter 4, such a capacitive structure cannot achieve stability in the zero-polarization region and hence will oscillate between the two negative capacitance regions. To exploit this feature, the feedback approach of Chapter 4 can again be used with a ferroelectric and tuning capacitor, but with the feedback designed to operate at high frequency (instead of maintaining dc stability) and to facilitate a large tunable frequency range.

One possible approach is to replace the inductor in a cross-coupled LC oscillator with a ferroelectric, as shown in Fig. 5.3(a), a configuration that can be considered as a feedback circuit and can be shown to exhibit the same polarity as the feedback circuit in Chapter 4. Following the same approach as we did in Chapter 3 and Chapter 4, the ferroelectric oscillator will be evaluated against standard LC oscillator circuits and key performance metrics will be extracted using Cadence circuit simulations. Preliminary simulations using the circuit in Fig. 5.3(a) shows that the circuit successfully oscillates and can be tuned by varying the capacitance of the tuning capacitor, as shown in Fig. 5.3(b).

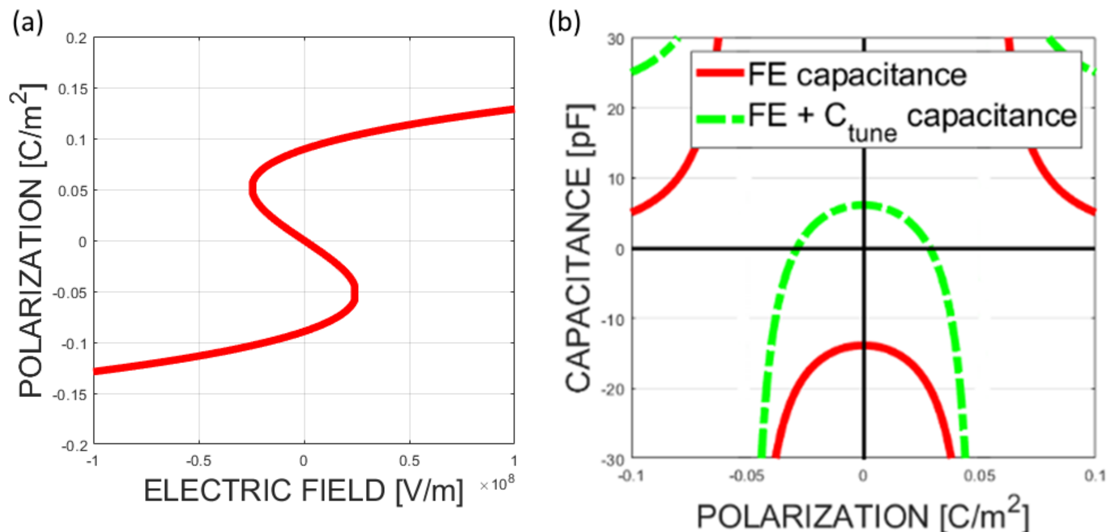

Fig. 5.2 (a) Plot of the ferroelectric polarization vs. electric field, where the slope of this plot is the capacitance of the ferroelectric. (b) Plot of ferroelectric capacitance vs. polarization.

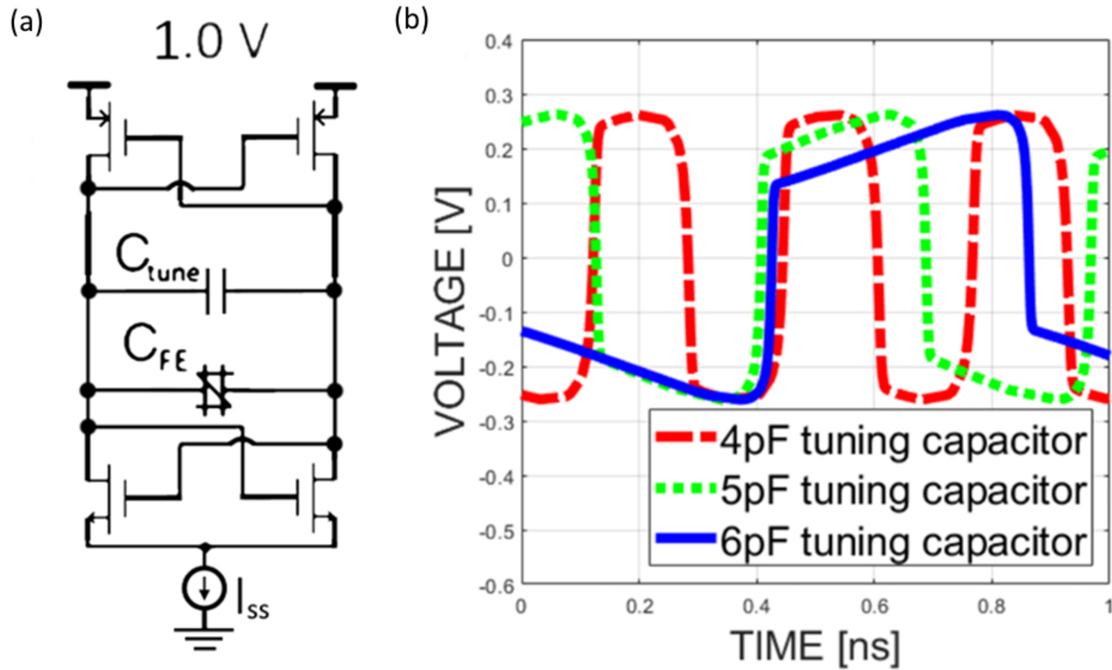

Fig. 5.3 (a) Circuit diagram of cross-coupled ferroelectric oscillator. (b) Plot of transient oscillations at various frequencies controlled by variable tuning capacitor.

5.3 Conclusion

Overall, the first two stages of work presented in Chapter 2 and 3 build a foundation by providing critical information and methods to evaluate the applicability of ferroelectric materials for use in IC design, while the continuation of this work in Chapter 4 proposes a technique for the first step of introducing ferroelectric materials into modern ICs as BEOL elements. Section 5.2 demonstrates an example of how the technique introduced in Chapter 4 can be expanded to yet unconsidered applications involving the use of ferroelectrics to advance the performance of nanoscale electronics. Thus, this thesis provides concrete contributions to the ongoing efforts of the electron-device community toward the realistic integration of ferroelectrics into modern electronics.

Appendix

We derive a minimum switching time for a ferroelectric capacitor regardless of the ferroelectric material used. For this analysis, as shown in Fig. A.1, we consider a simplified circuit consisting of a voltage source v_{IN}, resistor R, ferroelectric capacitor C_{FE}, and linear capacitor C_{MOS} in a series circuit, representing the relevant properties of a switching NCFET.

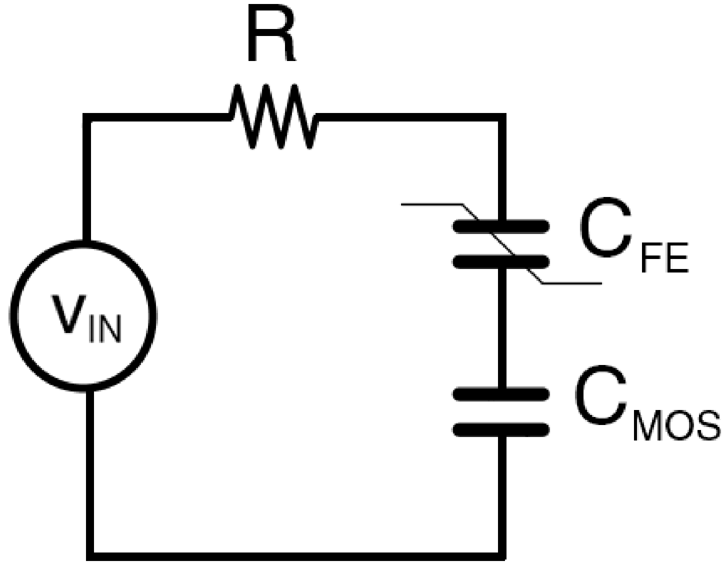

Fig. A.1. Simplified NCFET switching circuit, with a voltage v_{IN} applied to the gate.

We can say that the negative capacitance of the ferroelectric capacitor has provided a benefit if the voltage across the linear capacitor is greater than the voltage of the source. For simplicity, we use the single-domain LK equation,

$$\rho \frac{dP(t)}{dt} = E_{\mathrm{ext}}(t) - 2\alpha P(t) - 4\beta P^3(t) - 6\gamma P^5(t) \tag{A.1}$$

and consolidate the polarization polynomial into a single variable $E_{\mathrm{ext}}(t)$ with units of

V/m:

$$\rho \frac{dP(t)}{dt} = E_{\text{ext}}(t) - E_{\text{int}}(t) \tag{A.2}$$

where $E_{\text{ext}}(t)$ is the applied electric field across the ferroelectric capacitor and $E_{\text{int}}(t) = 2\alpha P(t) + 4\beta P^3(t) + 6\gamma P^5(t)$.

We now consider a single switching cycle, with v_{IN} increasing from 0 to a constant voltage $V_S > 0$, which eventually causes the ferroelectric capacitor to flip and hence an amplified voltage to appear across the linear capacitor. During this process, we know that the maximum applied electric field must be below V_S/t_{FE}, i.e., $E_{\text{ext}}(t) \leq V_S/t_{\text{FE}}$ for all t, because the ferroelectric capacitor cannot have more voltage across it than the source supplies. We assume that the maximum magnitude of the internal field remains below the coercive electric field E_{C} [100], i.e., the field required to flip the polarization; hence, $|E_{\text{int}}(t)| \leq E_{\text{C}}$, which is a necessary condition for the ferroelectric to provide voltage amplification [3]. The coercive electric field E_{C} must also be lower in magnitude than V_S/t_{FE}, because we have assumed that V_{S} is large enough to flip the ferroelectric capacitor. Therefore, the maximum magnitude of the internal field is also below V_S/t_{FE}, i.e., $|E_{\text{int}}(t)| \leq V_S/t_{\text{FE}}$. Thus, we can derive a maximum value for $E_{\text{ext}}(t)- E_{\text{int}}(t)$ of $2V_S/t_{\text{FE}}$ in the presumed switching cycle, occurring when a maximum $E_{\text{ext}}(t) = V_S/t_{\text{FE}}$ is applied to flip the ferroelectric while $E_{\text{int}}(t) = -V_S/t_{\text{FE}}$ retains its maximum magnitude but is opposite in sign:

$$\rho \frac{dP(t)}{dt}\bigg|_{\max} = [E_{\text{ext}}(t)- E_{\text{int}}(t)]_{\max} = 2\frac{V_{\text{S}}}{t_{\text{FE}}}. \tag{A.3}$$

We can also make an approximation on the charge accumulated on the ferroelectric capacitor:

$$Q(t) = \int \left[\varepsilon_0 \frac{v_{\text{FE}}(t)}{t_{\text{FE}}} + P(t)\right] dA \approx P(t)A \tag{A.4}$$

since for negative-capacitance operation, polarization must dominate the total charge contribution.

From the bounding values specified by (A.3) and (A.4), we can find the maximum current flowing through the circuit at any time:

$$I_{\max} = \frac{dQ(t)}{dt}\bigg|_{\max} = A\frac{dP(t)}{dt}\bigg|_{\max} = \frac{2AV_{\mathrm{S}}}{\rho t_{\mathrm{FE}}}. \tag{A.5}$$

If we determine how long it takes for a constant current of this magnitude to charge up the linear capacitor to a voltage of V_S, we will find the minimum time required for the ferroelectric capacitor to provide voltage amplification:

$$\tau_{\min} = \frac{CV_{\mathrm{S}}}{I_{\max}} = \frac{\rho t_{\mathrm{FE}}}{2}\left(\frac{C_{\mathrm{MOS}}}{A}\right). \tag{A.6}$$

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