Design and Investigation of Wide Frequency Tuning Range Millimeter-Wave Voltage Controlled Oscillators (VCO) in 65nm CMOS Technology

by

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Abstract

The available unlicensed spectrum in millimeter-wave (mm-wave) frequencies has been a very attractive candidate for high data rate wireless communications, high-resolution radars, and imaging applications. Voltage-controlled oscillators (VCO), which are essential building block of tunable multi-standard mm-wave transceivers or ultra-wideband radar front-ends, should provide a wide frequency tuning range (FTR), a low phase noise (PN), a low power consumption, and a low fabrication cost (i.e., small silicon area). For wideband radar applications and multi-standard wireless communication often a large FTR is required to achieve the desired resolution and communication data rates, respectively. In addition, because of the process and temperature variations in practical applications, more than allocated FTR is usually required to consider in design of single-standard mm-wave communication systems (e.g. 15% for 60 GHz). This thesis introduces new circuit architectures of mm-wave VCOs providing wide FTR and low phase noise circuits in a standard CMOS process.

First, a millimeter-wave wide tuning range voltage controlled oscillator incorporating two switchable decoupled VCO cores is introduced. When the first core is switched on producing the low-frequency band (LFB) signal and the second core is off, the inductors of the second core are reused to create additional buffers that pass the LFB signal to the output buffers. The generated high-frequency band (HFB) signals by the second core when turned on, are directly fed to the output buffers. Producing the outputs of both VCO cores across the same terminals without utilizing active/passive combiners and coupled inductors will enhance the PN performance of the VCO, increase its output power, and reduce the chip size. Fabricated in a 65 nm CMOC process, the VCO achieves a measured wide tuning range of 26.2% from 54.1 to 70.4 GHz while consuming 7.4-11.2 mA current from 1 V power supply. The peak measured phase noise at 10 MHz offset is -116.3 dBc/Hz and the corresponding FOM_T and FOM varies from -180.96 to -191.86 dB and -172.6 to -183.5 dB, respectively. The VCO core area occupies only 0.1 ×0.395 mm^2.

Second, a wide-tuning range dual-mode mm-wave VCO incorporating high quality-factor (Q) transformer-based variable inductors is presented. A high Q switched inductor with two different values is proposed by constructing the load of a transformer of a high Q fixed capacitor in series with a lossless switch structure that does not add any loss to the LC-tank as implemented by changing the signals mode across the

capacitor. By choosing a proper center frequency for each mode and sufficient frequency overlap, a wide FTR mm-wave VCO can be designed. It provides almost twice higher tuning range while keeping PN nearly the same as the two-mode VCO designed with two standalone inductors. Fabricated in a 65 nm CMOS process, the VCO demonstrates the measured FTR of 22.8% from 64.88 to 81.6 GHz range. The measured peak PN at 10 MHz offset is -114.63 dBc/Hz and the maximum and minimum corresponding figures of merit FOM and FOM_T are -181.07 to -189 dB and -173.9 to 181.84 dB, respectively. The VCO cores consume 10.2 mA current from 1 V power supply, and the occupied area is 0.146 ×0.205 mm^2.

Preface

This thesis is an original work by Ali Basaligheh. Chapter 3 is published as Ali Basaligheh, Parvaneh Saffari, Wolfgang Winkler and Kambiz Moez, "A Wide Tuning Range, Low Phase Noise, and Area Efficient Dual-Band Millimeter-Wave CMOS VCO Based on Switching Cores," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 8, pp. 2888-2897, Aug. 2019. I was responsible for the circuit design, fabrication and measurements. Parvaneh Saffari and Wolfgang Winkler assisted with the circuit measurements and contributed to manuscript edits. Kambiz Moez was the supervisory author and was involved with concept formation and manuscript composition.

Chapter 4 is submitted as Ali Basaligheh, Parvaneh Saffari, Igor Filanovsky and Kambiz Moez, "A 65-81 GHz CMOS Dual-Mode VCO Using High Quality Factor Transformer Based Inductors," to *IEEE Transactions on Microwave Theory and Techniques,* July. 2019. I was responsible for the circuit design, fabrication and measurements. Parvaneh Saffari assisted with the circuit measurements and contributed to manuscript edits. Kambiz Moez and Igor Filanovsky were the supervisory author and were involved with concept formation and manuscript composition.

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My warmest gratitude goes to my colleagues and friends at university of Alberta who made my stay here memorable, thanks to Payam Masoumi, Shila Shamsadini, Ahmad Adl, Danial Oloumi, Afshin Khan Amoorezaei, Alireza Saberkari, Mohammad Amin Karami, Fnu Aurangozeb, Xiaojian Yu, Sina Feghhi, Hojat Talezadeh, Souren Shamsinejad, Masoud Shabestary, Amin Ghazanfari, Mohammad-Reza Arani, Saman Jahani, Mohammad Shahabbasi, Mohammad Maadi, Atrin Tavakoli, Moosa Moghimi Haji, Ramin Razani, Yashar Kor, Mohammad Sahand Parniani, Moahammad Ebrahimi, Saeid Mahdiabadi, Mehdi Honari, Parinaz Jafari, Kambiz Afrooz, and many others.

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Chapter 1

Introduction

1.1 Motivation to Millimeter-Wave Communication

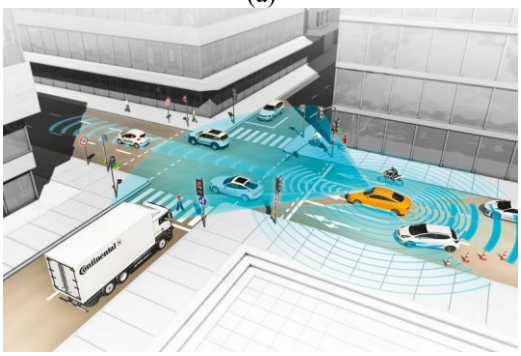
Based on Shannon's theorem of communications presented in late 1940 [1],

$$C = BW.log10(1 + SNR), \quad (1\text{-}1)$$

channel capacity (C) of a communication system in bits/sec is directly determined by the channel bandwidth (BW) and Signal to noise ratio (SNR) [1]. Hence, the available wide and underutilized spectrum in the millimeter-wave (mm-wave) frequencies (30-300 GHz), unfurl great opportunities for the high data rate wireless communications, medical imaging, and security applications.

The 60 GHz band (57 to 64 GHz) and E-band (71 to 76 and 81 to 86 GHz), both multi-GHz bandwidths, are two main allocated bands under 100 GHz by the U.S. Federal Communications Commission (FCC) to develop the next generation multi-gigabit-per-second wireless communication systems, point to point wireless link and automotive radar, respectively (Fig. 1.1). As shown in Fig. 1.2, because of the high oxygen absorption at 60 GHz, the signal attenuation is about 15 dB/km, which makes the available band suitable for short-range communications. In contrast, the attenuation drops to lower than 1 dB/km for the frequency band of 70-110 GHz and makes it an ideal candidate for high-data-rate long-range communications [2]-[12].

(a)



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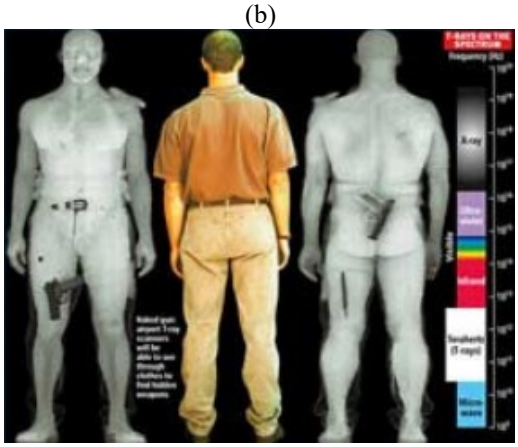


(c)

Fig. 1.1. Some applications for mm-wave band (a) multi-Gbps communication for multimedia, (b) automotive radar [13], and (c) security imaging [14].

1.2 Mm-wave Semiconductor Technology

Traditionally, III-V semiconductor processes were the semiconductor technology of choice for mm-wave integrated circuits design providing the desired transistor speeds at the cost often several times higher than standard silicon complementary metal-oxide-semiconductor (CMOS) processes. However, in recent years the unity gain frequency (f_T) and maximum oscillation frequency (f_{max}) of CMOS devices have exceeded 500 GHz thanks to the aggressive scaling of the transistors' sizes as shown Fig. 1.3. Providing the

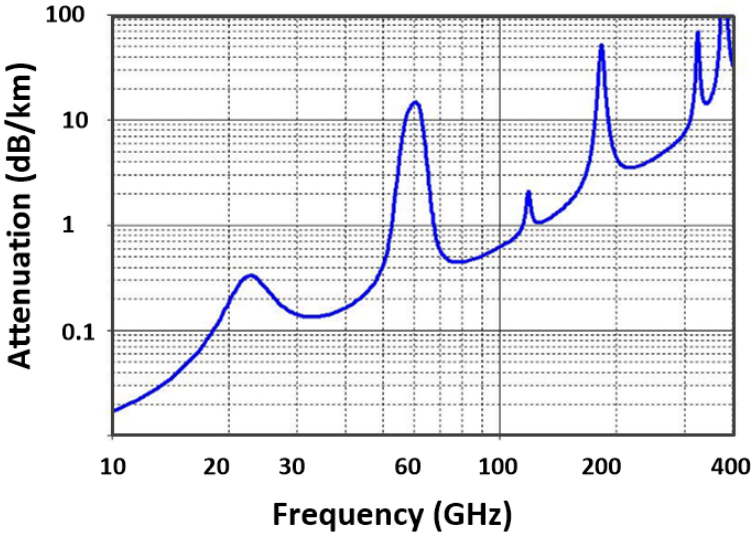


Fig. 1.2. Atmospheric and molecular absorption versus frequency [15].

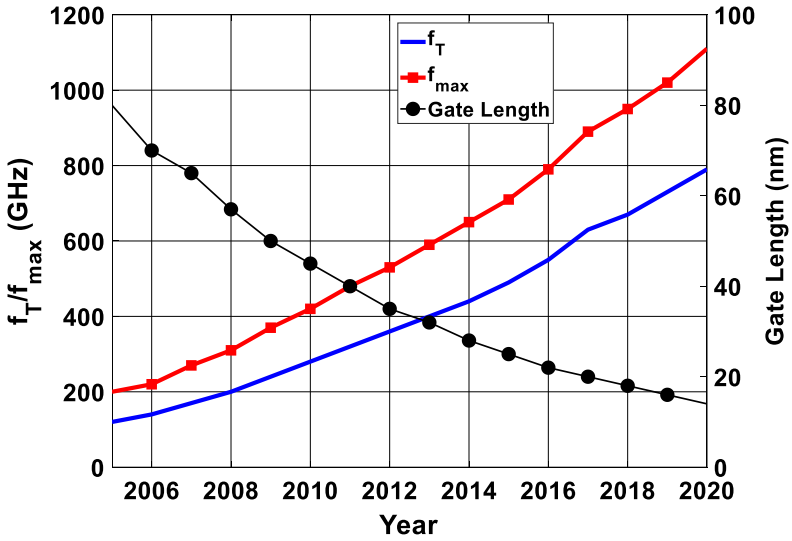


Fig. 1.3. International technology roadmap for semiconductors [16].

required ultra-fast transistors, CMOS is becoming the technology of choice for implementation of the mm-wave integrated circuits because of the lower implementation cost and the higher integration level than compound semiconductors enabling systems-on-a-chip (SoC) solutions [17]-[21].

1.3 Mm-wave VCO

Voltage-controlled oscillators (VCOs) are the essential building blocks of any mm-wave transceiver (TRX) [23]. LC-VCOs are widely used in radio frequency (RF) and mm-wave applications because of the low PN, moderate tuning range and dc power consumption. Moreover, as the physical size of inductors and capacitors are smaller at mm-wave frequencies compared to low-GHz frequencies, the structure exhibits more compact implementation at mm-wave frequencies. VCOs with large frequency tuning range (FTR) are required for up/down frequency conversion of different bands within such large allocated band and/or for supporting multi-standard and wideband wireless systems. In practice, FTR should cover more than the allocated band due to the temperature and process variation and a VCO with FTR of more than 15% is required for 60 GHz applications [23]. Moreover, some applications, such as rotational spectroscopy, need a FTR around 50% or more [24]. Fig. 1.4 illustrates the block diagram of a 60 GHz Transceiver for radar applications where a VCO with 7 GHz tuning range is needed for high-range and high-resolution.

Achieving a large FTR (e.g. more than 20%) is not possible using CMOS varactors with minimum channel length as the overlap capacitors will limit the capacitance range that can be produced by these devices. Use of long channel varactors for tuning oscillation frequency of LC-tank VCOs at mm-wave frequencies is also not a good solution because of their low-quality factor resulting in significant phase noise degradations. While multi-core VCOs can be utilized to produce the required tuning range, the existing multi-core VCOs suffer from low Q LC-tanks or large area occupation.

At low GHz frequencies, where high Q-factor (Q) on-chip capacitors and varactors are available [53],[55],[57],[58],[60],[80], switched capacitor arrays, switched inductors and resonators are commonly used for wide FTR VCO design. However, at mm-wave frequencies, because of the trade-off between the on-resistance and parasitic capacitance

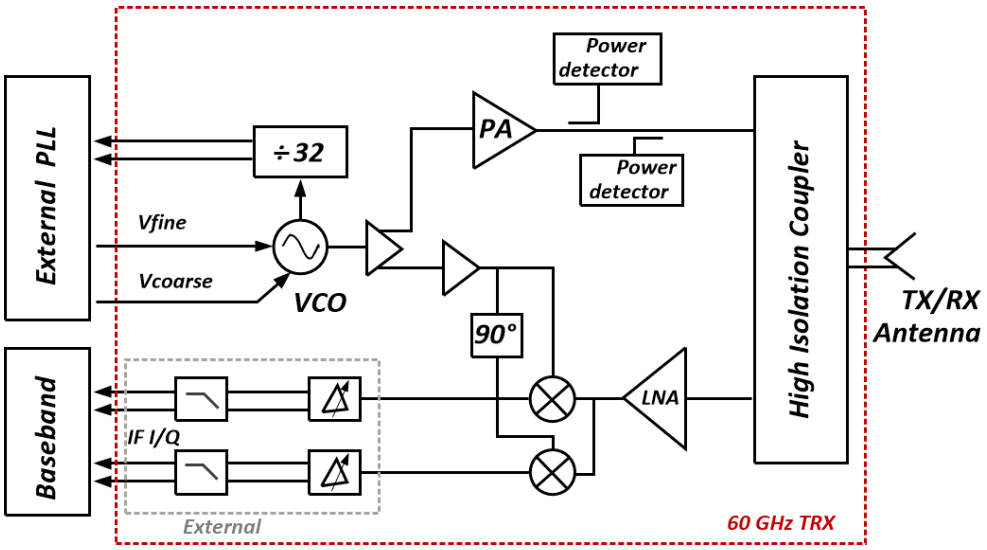


Fig. 1.4. Block diagram of a 60 GHz TRX for radar applications [22].

produced by switches, it is not possible to produce high Q switched-capacitor structures. Similarly, the trade-off between the tuning range and the size prevents mm-wave varactors to achieve high Q-factors. Therefore, the aforementioned methods cannot be used for low-PN VCO design at mm-wave frequencies.

Capacitive and inductive coupled LC resonators with almost ideal mode-switching, provide wide FTR without degrading the resonator Q at low-GHz frequencies [81]-[83]. These methods seem suitable for mm-wave application in the absence of lossy series switches and coupled inductors. However, the extra capacitance added to the resonator because of capacitive coupling further restricts the limited capacitance budget at mm-wave frequencies resulting in a lower tuning range. In addition, the inductive coupling technique requires the use of two uncoupled inductors which doubles the chip area of the oscillator's core.

Another approach to producing mm-wave oscillation is to use frequency multipliers in conjunction with an oscillator operating in sub-mm-wave where varactors exhibit significantly higher Q-factors compared to the mm-wave region [24],[61],[69]. However,

the required frequency multipliers add to the cost and power consumption of the overall VCO and often result in the structure with a low output power level.

Magnetically coupled multi-core VCOs with overlapping tuning ranges can be used to combine the tuning range of single-core VCOs [70]-[74]. However, the lossy coupled resonators along with the required power combiners at the output of these VCOs considerably add to the power consumption and area while degrading the noise performance of the oscillators.

An area-efficient dual-core VCO with small size-varactors and standalone inductors is presented in [77] to increase the FTR along with the high-Q resonator resulting in a better PN performance. There the inductor of high-frequency band core is used as the load for the internal buffer/combiner to pass the signal of the low-frequency band to the output buffer. Nevertheless, the untuned internal combiner reduces the output power level of the low-frequency band.

Recently, loaded transformer-based variable inductors (VIDs) are widely used to design wide tuning range mm-wave VCOs [3]-[6],[62]-[66],[84]. However, these VIDs often exhibit low-quality factor degrading the phase noise of these VCOs.

1.4 Thesis Overview

In this dissertation, first of all, passive and active components used for construction of mm-wave VCOs are studied. Then the conventional wide FTR mm-wave VCOs are reviewed to understand why these circuits suffer from poor PN performance (see Chapter 3). Then based on the existing problems, two low phase noise (PN) and wide FTR VCOs realized in 65 nm CMOS technology are presented.

In Chapter 4, a novel millimeter-wave wide tuning range voltage controlled oscillator incorporating two switchable decoupled VCO cores in 65nm CMOS technology is presented. When the first core (cross-coupled transistors, varactors, and inductors) is switched on, the second acts as a buffer producing the low-frequency band at the output, and when the second core is turned on, the first core is switched off, producing the high-frequency band at the same output. Hence, the outputs of both VCOs come from same terminals without utilizing bulky active/passive combiners. To enhance the phase noise

performance of the VCO, increase its output power, and reduce the chip size, the proposed structure avoids using lossy coupled inductors producing the outputs of both VCOs across the same terminals without utilizing active/passive combiners.

In Chapter 5, a wide-tuning range dual-mode millimeter-wave (mm-wave) voltage controlled oscillator (VCO) incorporating high quality-factor (Q) transformer-based variable inductors. A high Q switched inductor with two different values is proposed by constructing the load of a transformer of a high Q fixed capacitor in series with a lossless switch structure that does not add any loss to the LC-tank as implemented by changing the signals mode across the capacitor. By choosing a proper center frequency for each mode and sufficient frequency overlap, a wide frequency tuning range (FTR) mm-wave VCO can be designed. It provides almost twice higher tuning range while keeping phase noise (PN) nearly the same as the two-mode VCO designed with two standalone inductors.

Chapter 6 concludes the dissertation by summarizing the contributions of the presented works and highlighting the future research on the topic.

Chapter 2

Millimeter-Wave Active and Passive CMOS Components

Aggressive scaling in the size of CMOS devices toward smaller channel lengths, lower parasitic capacitances and a high number of available passive layers has resulted in performance improvement of the circuits at mm-wave frequencies enabling the integration of mm-wave front-end with digital processing unit to produce systems-on-a-chip (SoC) communication/radar solutions [25]-[34]. However, the design of mm-wave circuits with a performance comparable to that can be achieved with compound semiconductor processes is challenging because of lower speed transistors, low quality of passive devices, and higher noise of transistors. For example, mm-wave circuits suffer from low-Q passive components due to the low substrate resistivity of CMOS technology (10-15 Ω-cm).

To begin designing mm-wave circuits in CMOS, we have to first structure the available active and passive devices and their electrical/electromagnetic characteristics including transistors (MOSFETs), varactors, capacitors, and inductors and transmission lines. All of the active/passive components at mm-wave frequencies should be carefully modeled by utilizing electromagnetic (EM) simulators.

2.1 CMOS Transistors

In addition to the intrinsic parameters of CMOS transistors which are usually provided by the foundry, parasitic resistance, capacitance, and inductance due to the wiring became very important at mm-wave frequencies, and influence the important device parameters drastically. For example, f_{max} and f_T of a MOS transistor with the intrinsic model are given as [36]

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})}, \tag{2- 1}$$

and

$$f_{max} \approx \frac{1}{2} f_T \sqrt{\frac{R_{ds}}{R_g}} \tag{2- 2}$$

where the parameters are

- g_m: transistor transconductance

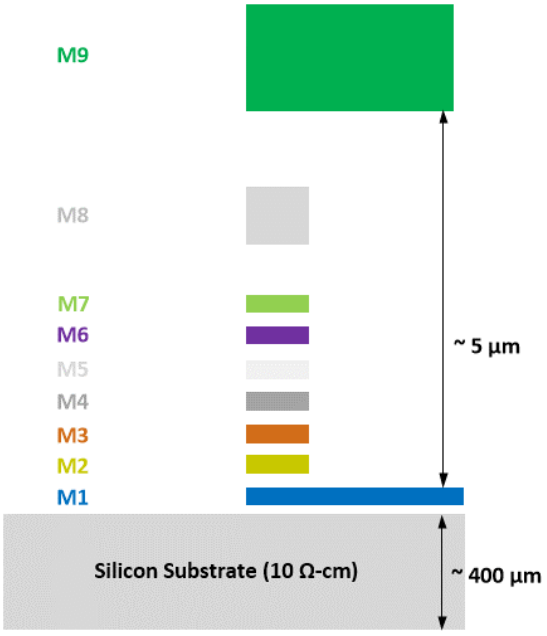


Fig. 2.1. 1P9M 65-nm CMOS technology cross-section.

- C_{gs}: gate-source capacitance
- C_{gd}: gate-drain capacitance
- R_{ds}: series drain-source resistance
- R_g: gate resistance

According to the above equations, f_T and f_{max} of a MOS transistor are limited with parasitic capacitive and resistive losses.

The most relevant and important parameter of a MOSFET for high-frequency design is f_{max} [35], which determines the maximum oscillation frequency of a VCO. Hence, an accurate equation including the layout parasitics, is needed for optimum design procedure at 60 GHz and beyond. Fig. 2.2 demonstrates the simplified high frequency model of a one finger NMOS transistor where the f_{max} based on the provided model and neglecting R_D and substrate losses is given by [36]

$$f_{max} \approx \frac{1}{2}\frac{f_T}{\sqrt{R_g\left(g_m+C_{gd}/C_{gg}\right)+\left(R_g+R_s+r_{ch}\right)g_{ds}}} \quad (2\text{-}3)$$

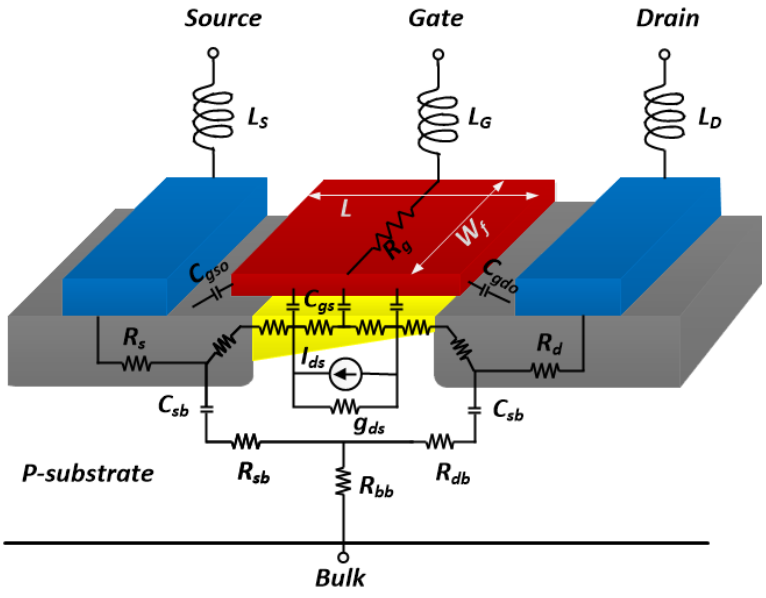
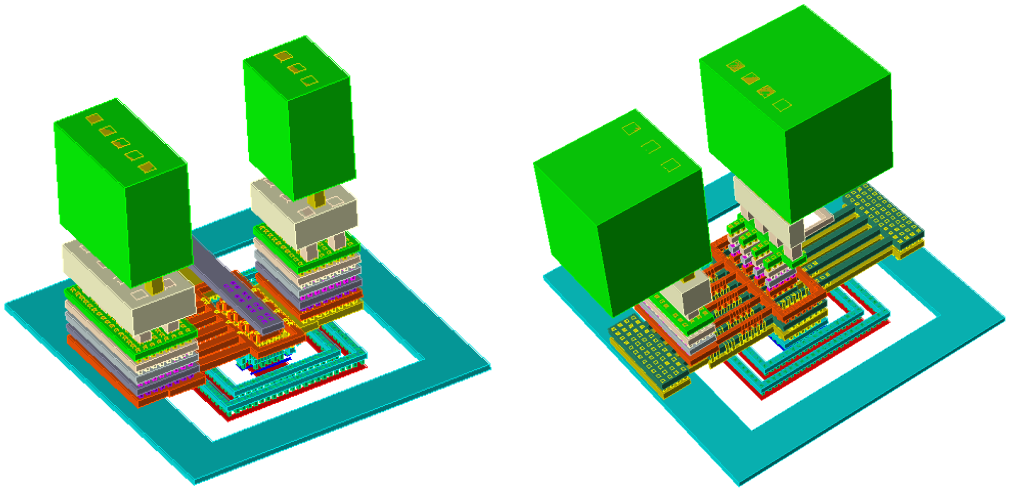


Fig. 2.2. Physical model for one finger NMOS transistor [36].

where C_{gg} and r_{ch} are total gate capacitance and channel resistance, respectively.

It is clear that f_{max} is mainly limited by R_g of the device which should be minimized by optimum physical layout. Fig. 2.1 shows the cross-section view of the 1P9M 65-nm CMOS technology where 9 metal layers that provide wirings between the active/passive components in the layout. Moreover, passive components such as inductors and capacitors



(a) (b)

Fig. 2.3. 3-D view interconects layout of a 7 finger RF transistor in 65-nm CMOS technology (a) provided by the foundary, (b) customized layout for higher f_{max}.

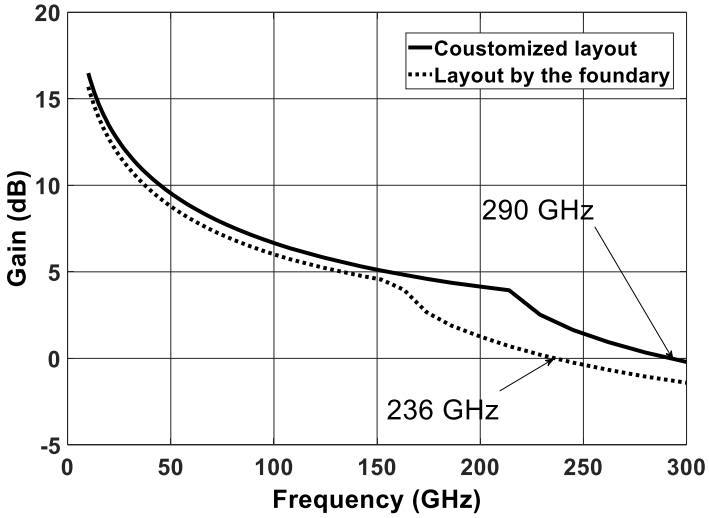


Fig. 2.4. Simulated f_{max} of a 7 finger transistor in 65-nm CMOS technology (a) layout provided by the foundary, (b) custom layout.

are realized by utilizing these metal layers as will be studied later in this section. Two different physical layout of a MOSFET with 7 fingers in 65-nm CMOS, are shown in Fig. 2.3(a) and (b), where the customized layout employs three stacked metal layers (M1-M3) to reduce the gate resistance. As the result, the simulated f_{max} of the transitor is improved as shown in Fig. 2.4.

2.2 MOS Varactors

Varactors are key components in RF/mm-wave circuit design such as VCO and phase shifter for tuning the circuit parameters. The varactors can be fabricated in P-substrate (MOS varactor) or isolated N-well (accumulation mode varactor) [41]-[43].

Based on the applied voltage to the gate (Vg) and the drain/source (Vd/s) nodes, varactor operates in accumulation (holes accumulates at the body surface), depletion (surface is depleted from carriers) and inversion (electrons are attracted at body surface) modes as shown in Fig. 2.5. The related C-V of MOS varactor is depicted in Fig. 2.6, where capacitance decreases with gate voltage. However, it increases to a maximum value when the device enters into inversion region and behaves such as a voltage-dependent gate capacitance of a regular MOSFET resulting in non-monotonic behavior which makes VCO design complicated [41]. Hence, accumulation-mode varactors are more popular in modern RF/mm-wave IC design.

In accumulation mode (A-mode), when Vg is higher than $V_{d/s}$, electrons are attracted to the body surface and accumulation layer is formed as shown in Fig. 2.7. If $V_{d/s}$ exceeds V_g, electrons are forced back from the surface of N-well and around SiO_2 creating depletion layer. Fig. 2.8 shows the related C-V of an A-mode varactor where there is no inversion region because the NMOS is implemented in the N-well substrate and the material under the gate is n-type [41].

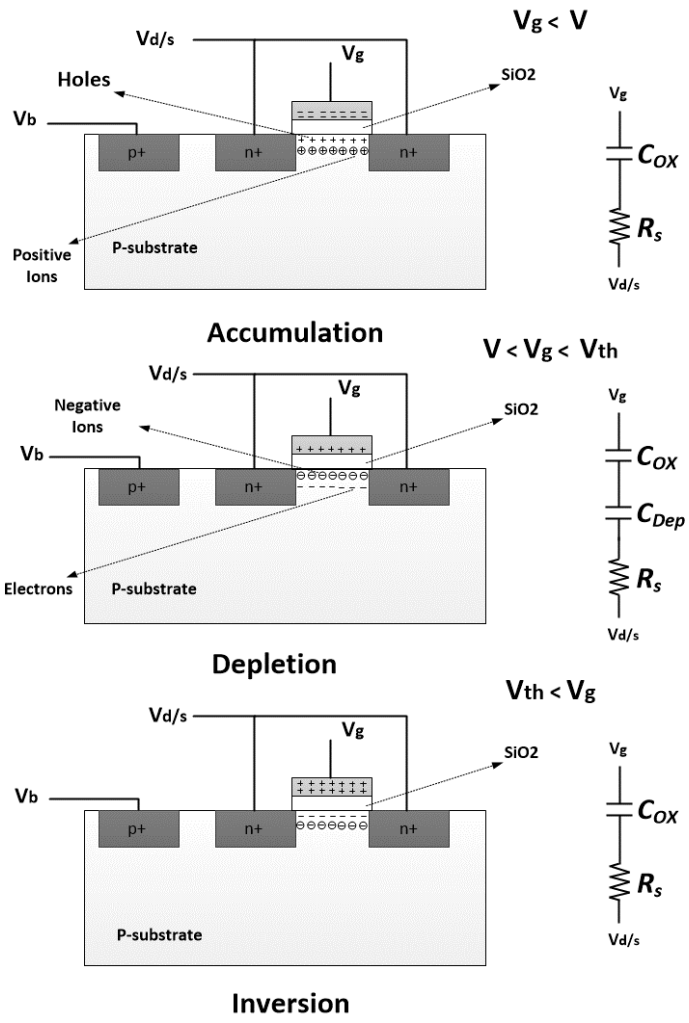


Fig. 2.5. MOS varactor operation in different regions.

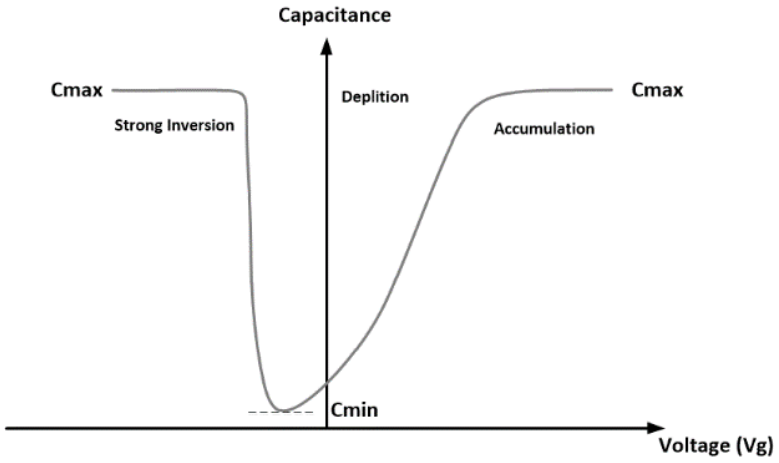


Fig. 2.6. C-V curve for MOS varactor (Vd/s=Vb).

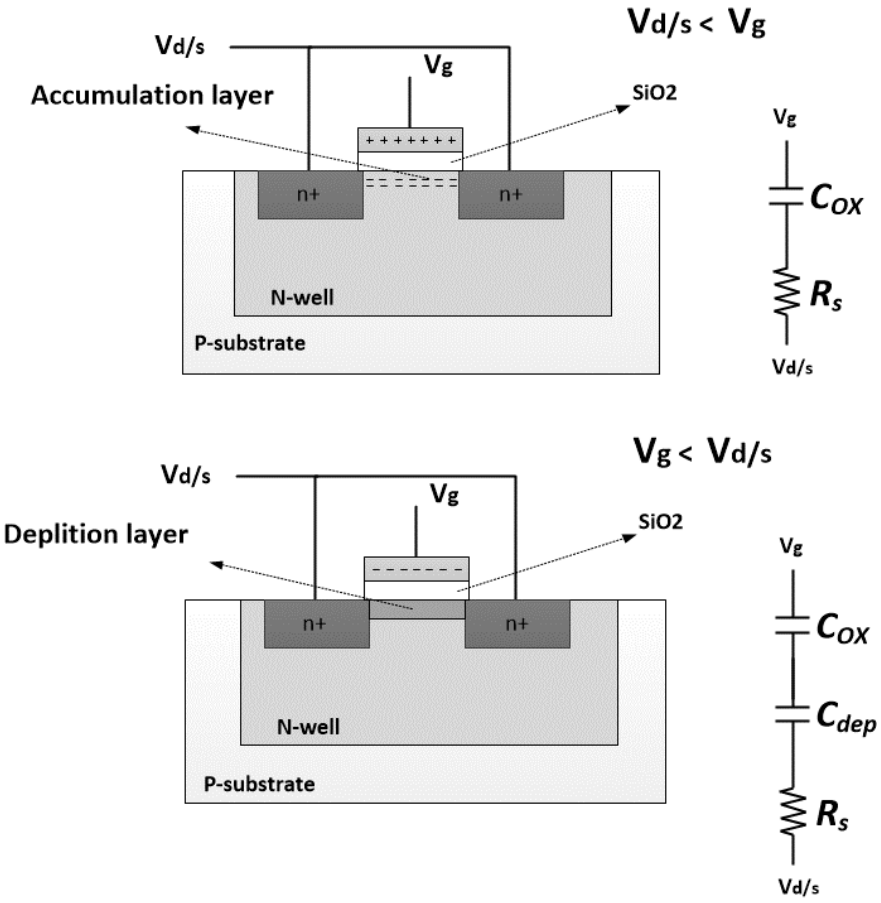


Fig. 2.7. A MOS varactor operation in different regions.

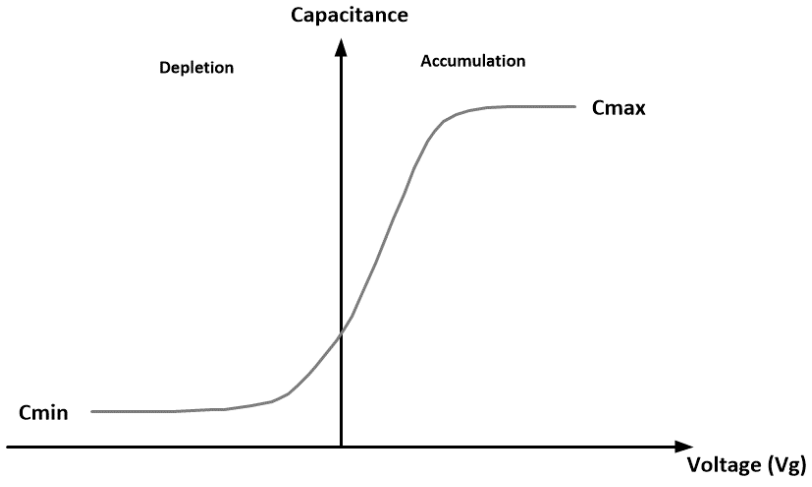


Fig. 2.8. C-V curve for A-MOS varactor.

Fig. 2.9 shows the equivalent mm-wave model of a varactor where the parameters can be described as below [43]:

- *Lg*: Parasitic inductance of gate
- *Rg*: Parasitic resistance of the gate
- *Cs*: Gate-oxide and depletion capacitance under the gate
- *Cf*: Fringing capacitance of the gate
- *Rch*: Channel resistance
- *Csub*: Depletion capacitance between n-well and p-well
- *Rsd*: Source and Drain resistance
- *Cnw*: Vertical capacitance of n-well
- *Rnw*: Vertical resistance of n-well
- *Rsub* & *Csub*: Modelling silicon loss at high frequencies

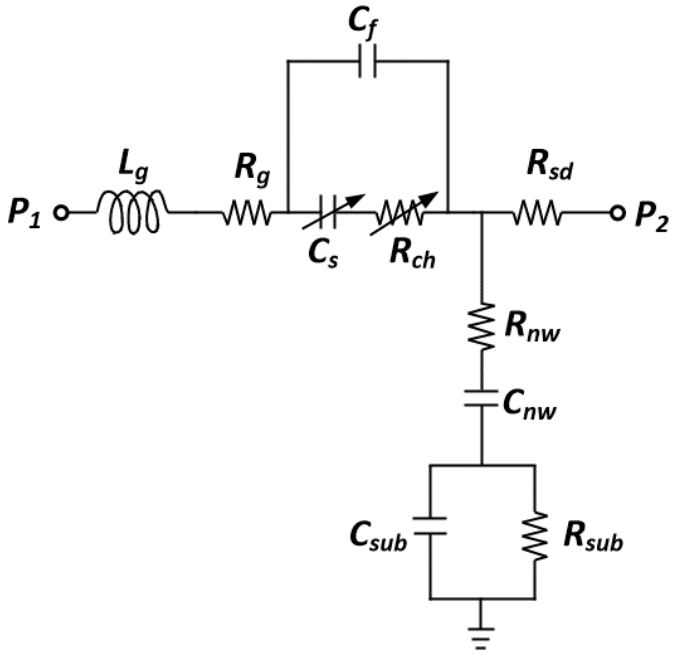
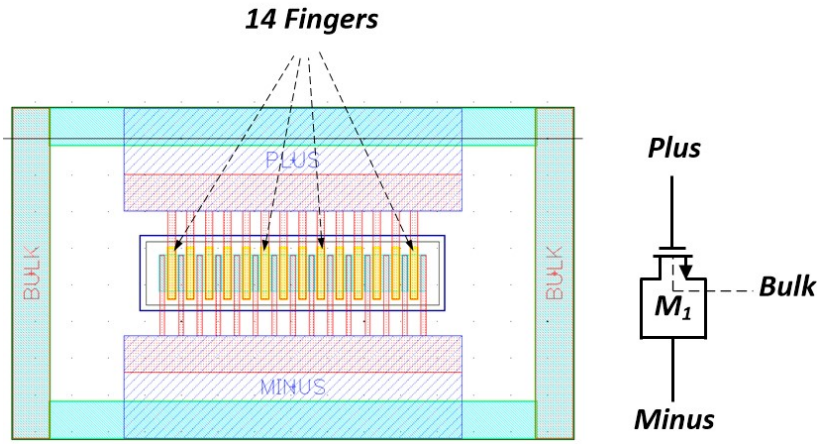
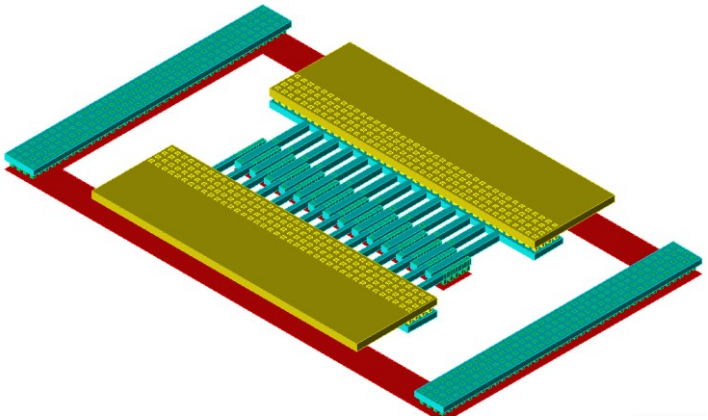


Fig. 2.9. Equivalent mm-wave circuit model for a MOS varactor.



(a)



(b)

Fig. 2.10. (a) Layout, and (b) 3D view of a 14 finger varactor in 65-nm CMOS.

Usually *Q* of a varactor is limited by *Rch* which will be discussed more in Chapter 4.

2.3 Fixed Capacitors

Fixed value capacitors are widely used in the design of matching circuits, AC coupling and DC bypass in RF/mm-wave frequencies [36]. Metal-Insulator-Metal (MIM) and Metal-Oxide-Metal (MOM) are two available high-Q capacitors in CMOS technologies. Despite achieving a high density, MIM capacitors are expensive because they require two additional layers in the fabrication process. They are more sensitive to the process variation in comparison to the MOM capacitors because of close proximity of these additional layers.

Fig. 2.11 shows the RF circuit model of a MIM capacitor with a ground plane under it. The capacitor parameters are

- C_{MIM}: Main capacitor
- R_{Top}: Resistance of the top plate
- L_{Top}: Inductance of the top plate
- C_{Par}: Parasitic capacitance between the bottom plate and ground plane
- R_{Bot}: Resistance of the bottom plate
- L_{Bot}: Inductance of the bottom plate

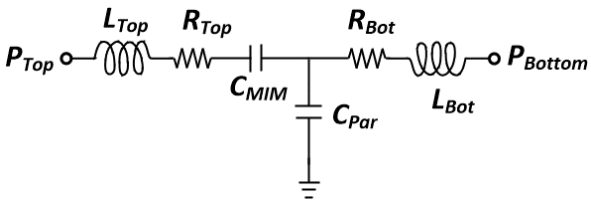


Fig. 2.11. MIM capacitor circuit model.

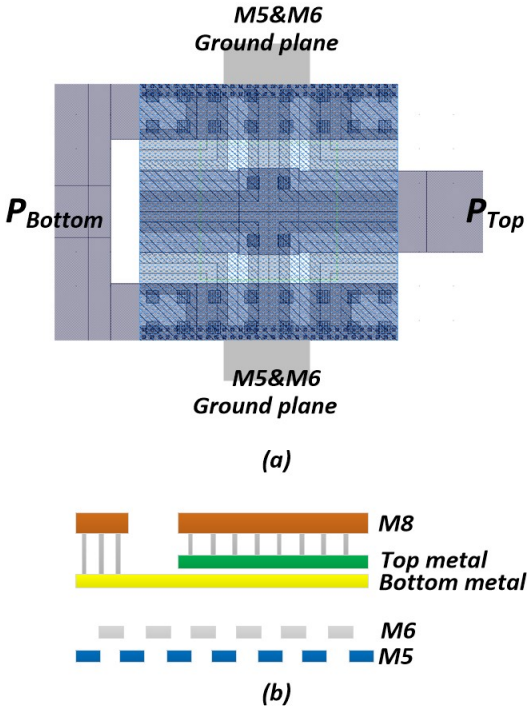


Fig. 2.12. (a) Top view layout, (b) cross-section of a MIM capacitor with underlying ground metal in 65-nm CMOS.

Conversely, MOM capacitors are less expensive and utilize parallel capacitance between the metals available in the CMOS process. Moreover, this capacitor provides a short pass with the lowest inductance from the capacitor plates to the ground [36]. Fig. 2.14 illustrates an equivalent circuit model for a MOM capacitor with a ground shield where the ground plane can be the lowest metal and parameters can be described as

- C_{MOM}: Main capacitor
- L_{Top}: Resistance of the top plates
- R_{Top}: Inductance of the top plates
- C_{Par}: Parasitic capacitance to the ground plane

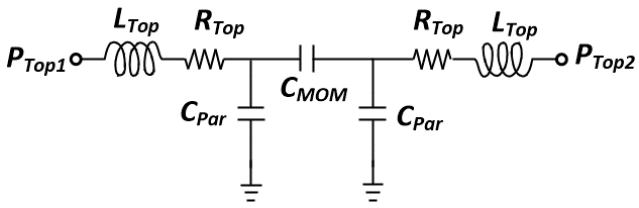
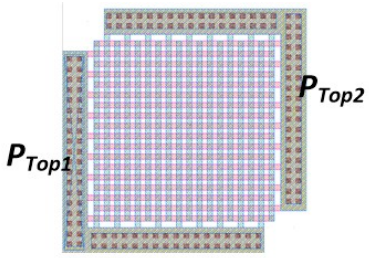


Fig. 2.13. MOM capacitor circuit model.



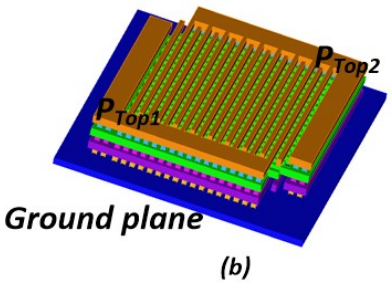


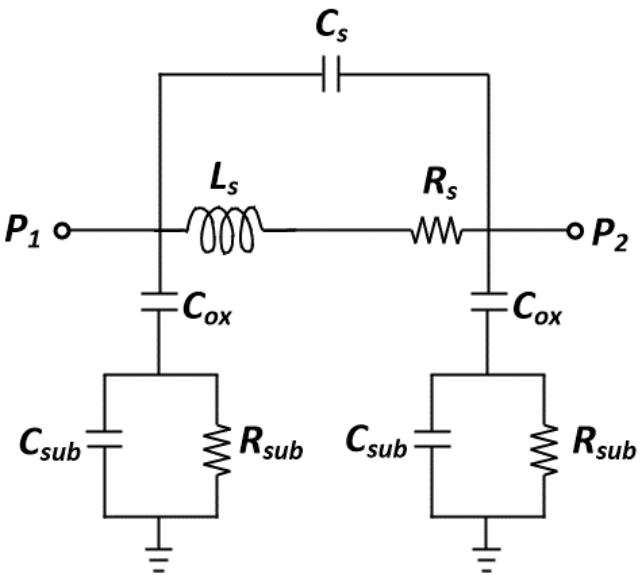
Fig. 2.14. (a) Cross-section of a MOM capacitor with undelying ground metal CMOS, (b) top view layout.

2.4 Inductors

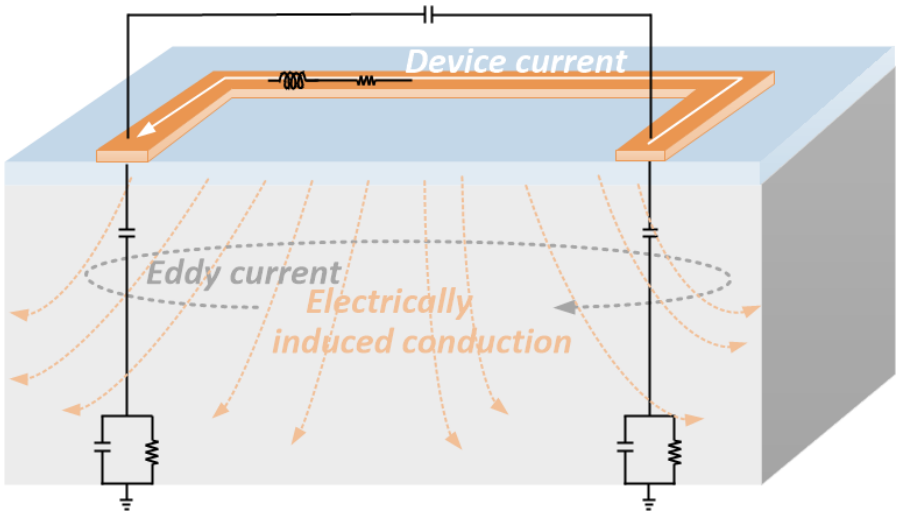
Inductors are employed extensively in RF/mm-wave circuit design for the design of matching networks, LC- tanks of VCOs, LNAs. Compared to low GHz inductors, the inductor sizes at mm-wave frequencies are reduced because of the smaller wavelengths. Fig. 2.15(a) and (b) show the equivalent circuit and the cross-section of a one-turn on-chip inductor. The inductor parameters are

- L_s: Main inductance
- R_s: Series resistance
- C_{ox}: Parasitic capacitance between the coil and substrate
- C_{sub}: Substrate capacitance
- R_{sub}: Substrate resistance

The performance of on-chip inductors is limited by the metal loss caused by the series resistance of the metal layer(s), the substrate loss caused by Eddy current flowing through the low-resistive silicon substrate itself produced by the penetrating magnetic field of the inductor, and the substrate loss caused by electric couplings of metal wires with substrate [36]-[41]. For accurate modelling of the on-chip inductors, it is essential to simulate the inductors by utilizing EM simulators. Fig. 2.16 illustrates 3D view layout of an orthogonal center-tap inductor in 65-nm CMOS technology including the dummy metal fills where the orthogonal structure exhibits minimum loss comparing with the other shapes such as square shape inductors [41]. Increasing the width of the inductor is the other option to reduce the series resistance and improve the quality factor at the cost of lowering self-resonance frequency.



(a)



(b)

Fig. 2.15. (a) Equivalent RF circuit model, (b) cross-section of an on-chip inductor.

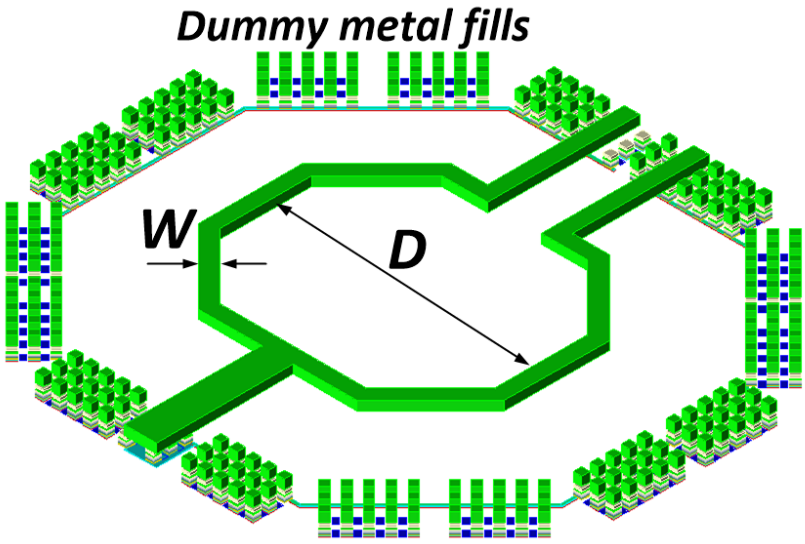


Fig. 2.16. 3D view of an on-chip inductor.

2.5 Transformers

The solid-state transformers are essential components of many wireless communication systems often employed in the design of impedance matching, AC coupling, driving balanced circuits at mm-wave frequencies [36], [40]. Transformer are often constructed using the top or the top two metal layers of CMOS chip with planar and stacked structures as depicted in Fig. 2.17. The windings are realized using two top thick metals to reduce the series resistance and increase the quality factor.

The on-chip transformer can be modelled in the most simplistic form using two coupled disk coils (Fig. 2.18) [86], [87]. It is frequently referred to as Bitter coils (referring to F. Bitter, who started to use such coils in electromagnets) or, simply, pancakes [87]. A well-known formula for the mutual inductance between two loops located in parallel planes

(Maxwell coils) is used in [40].to derive the approximate value of mutual inductance of two such coils with improved parameters.

Fig. 2.19 shows a single-turn transformer with two coupled inductors (Primary and secondary) with the following parameters [39]:

- L_P: Primary inductance
- L_s: Secondary inductance
- M: Mutual inductance

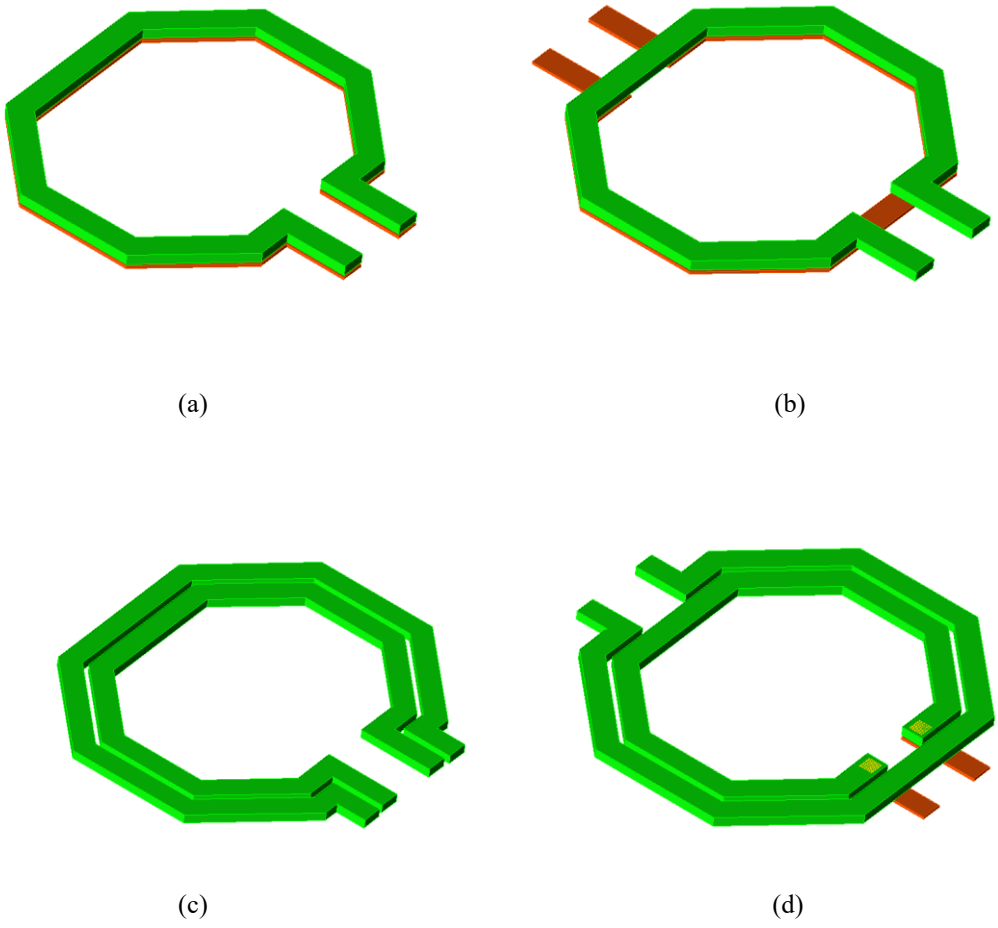


Fig. 2.17. 3D view of an on-chip transformers with different structures: (a) non-flipped Stacked, (b) flipped stacked, (c) non-flipped planar, and (d) flipped planar.

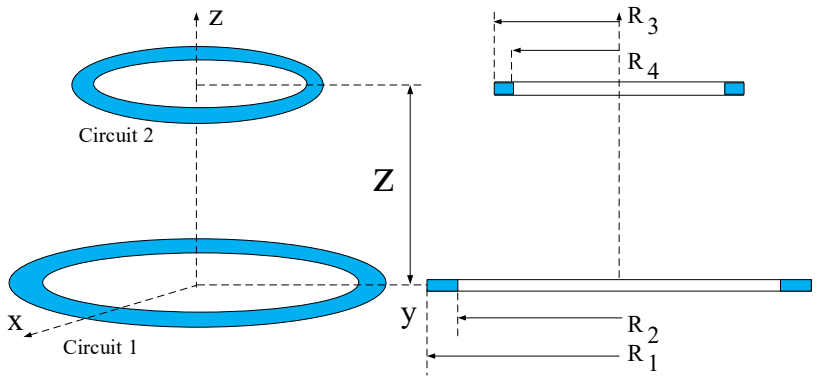


Fig. 2.18. Thin coaxial flat coils [40].

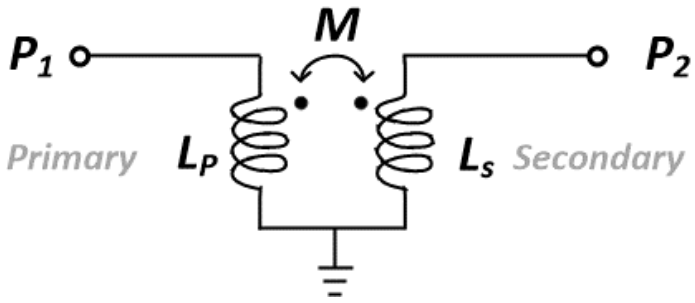


Fig. 2.19. Simplified equivalent model of a two port transformer.

The mentioned parameters including the Q of the primary and secondary coils (Q_P and Q_S) can be obtained as

$$L_P = \frac{Im(Z_{11})}{\omega} \tag{2-1}$$

$$L_S = \frac{Im(Z_{22})}{\omega} \tag{2-2}$$

$$M = \frac{Im(Z_{21})}{\omega} \tag{2-3}$$

$$Q_P = \frac{Im(Z_{11})}{Re(Z_{11})} \tag{2-4}$$

$$Q_S = \frac{Im(Z_{22})}{Re(Z_{22})} \tag{2-5}$$

However, this model does not predict important parameters of a transformer such as self-resonance frequency (SRF) at mm-wave frequencies and a more accurate model incorporating all parasitic components is needed. Fig. 2.20 shows the equivalent circuit model of a transformer [39] including the parasitics which can predict an accurate behavior of the device in RF/mm-wave frequencies where the parameters can be describe as

- L_P: Primary inductance
- R_P: Primary series resistance
- C_S: Parallel capacitance between the primary and secondary coils
- M: Mutual inductance
- C_{ox}: Parasitic capacitance between the coil and substrate
- C_{sub}: Substrate capacitance
- R_{sub}: Substrate resistance
- L_s: Secondary inductance
- R_s: Secondary series resistance

To verify the accuracy of the circuit model and extract its copayments, an on-chip transformer should be modeled using EM simulators with exact trace and spacing dimensions for the specific semiconductor process.

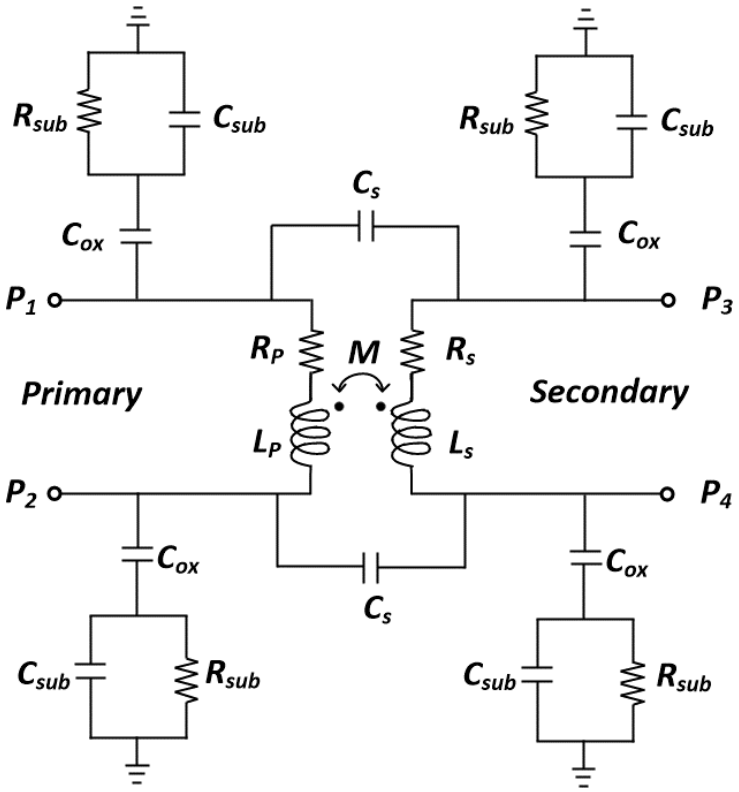


Fig. 2.20. Equivalent RF circuit model of transformer [39].

Chapter 3

Oscillator Design Fundamentals and Literature Review

3.1 Oscillator Fundamentals and Topologies

An oscillator is an important part of a Transceiver (TRx) which generates the required LO signal needed for mixers to perform up/down frequency conversion and usually uses a voltage signal to control its oscillation frequency, hence the name "voltage controlled oscillator". For a negative feedback system shown in Fig. 3.1 the transfer function is given by

$$\frac{Y}{X}(s) = \frac{H(s)}{1+H(s)}, \tag{3-1}$$

where "Barkhausen's criteria" for oscillation must be satisfied at ω_{osc}

$$|H(s = j\omega_{osc})| = 1, \tag{3-2}$$

$$\angle H(s = j\omega_{osc}) = 180°. \quad (3\text{-}3)$$

3.1.1 Ring Oscillator

Ring oscillator is an example of a feedback system oscillator, including a series of n delay stages depicted in Fig. 3.2 which starts oscillating when total phase shift and gain of the closed-loop reach 180° and more than unity, respectively. The oscillation frequency of an m-stage ring oscillator with the delay of τ_d is given by

$$\omega_{osc} = \frac{1}{2m\tau_d}, \quad (3\text{-}4)$$

$$m = 2n + 1,\ n = 1, 2, \ldots \quad (3\text{-}5)$$

Ring oscillators are area efficient as they do not require any on-chip inductor and the best choice for low power applications. However, this topology suffers from high PN because of a higher number of transistors and low operation frequency limited to low GHz.

3.1.2 LC Oscillators

LC oscillators because of low PN, moderate tuning range, and dc power consumption are widely used in radio frequency (RF) and mm-wave applications. Moreover, as the physical size of inductors and capacitors are much smaller at mm-wave frequencies compared to low-GHz frequencies, the structure exhibits more compact implementation at

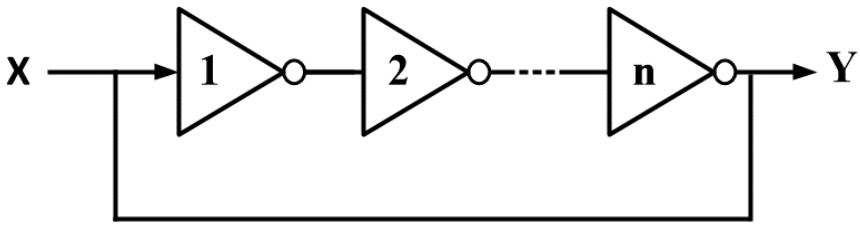


Fig. 3.2. Ring oscillator.

mm-wave frequencies. This type of oscillators can be analyzed as a one-port system including an LC tank with limited Q by a parallel resistor (R_P) [41], which requires a negative network to compensate the loss ($-R_P$) as depicted in Fig. 3.3.

Cross-coupled and Colpitts are two well-known LC-Oscillators used for RF/mm-wave applications.

3.2 LC-VCOs

3.2.1 Cross-coupled VCO

A simple cross-coupled VCO is shown in Fig. 3.4 where the cross-coupled transistors provide the required negative resistance of -2/gm to compensate for the loss of LC-tank with the oscillation condition of $g_m \geq \frac{2}{R_p}$. The oscillation frequency of LC-tank VCO is given by

$$\omega_0 \approx \frac{1}{\sqrt{L(C_{var}+C_{par})}} \tag{3-6}$$

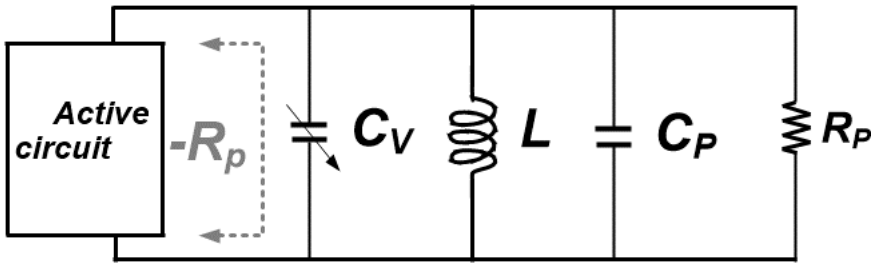


Fig. 3.3. LC oscillator.

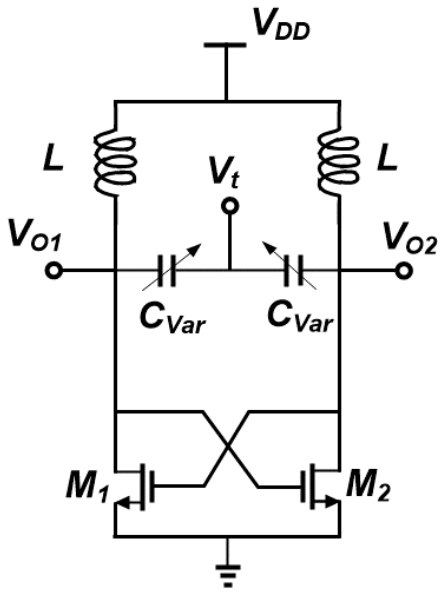


Fig. 3.4. Cross-coupled LC-oscillator.

where L is the loading inductor, C_{var} and C_{par} are the varactor capacitances, and parasitic capacitance at the output node, respectively.

3.2.2 Colpitts VCO

Colpitts is another topology of *LC*-oscillators and utilizes one transistor to create negative resistance as shown in Fig. 3.5. The startup condition of $g_m \geq \frac{1}{R_p} \frac{(C+C_{var})^2}{C \times C_{var}}$ must be satisfied for oscillation condition which can be expressed as

$$\omega_0 \approx \frac{1}{\sqrt{L\left(\frac{C \times C_{var}}{C+C_{var}}\right)}} \tag{3-7}$$

If $C = C_{var}$, oscillation condition is equal to $g_m \geq \frac{4}{R_p}$, which is two times more than the required dc power in a cross-coupled VCO for startup condition.

Moreover, cross-coupled VCOs generate differential output signals while the output signals of Colpitts oscillator are single-ended.

3.3 VCO Characteristics

3.3.1 Figure of merit

There are some trade-offs between the important parameters of a VCO such as tuning range and PN. Hence, usually the generally accepted figure of merits [11], [49], [62], *FOM* and FOM_T, are used to show the overall performance of the circuit and can be calculated as

$$FOM = PN(f_m) - 20\log\left(\frac{f_0}{f_m}\right) + 10\log\left(P_{DC}(mW)\right) \tag{3-8}$$

and

$$FOM_T = PN(f_m) - 20\log\left(\frac{f_0}{f_m}\frac{TR\%}{10}\right) + 10\log\left(P_{DC}(mW)\right) \tag{3-9}$$

where f_0 is the oscillation frequency, f_m is the frequency offset from the carrier, PN is the phase noise at f_m, TR is the frequency tuning range in percent, P_{DC} is the dc power

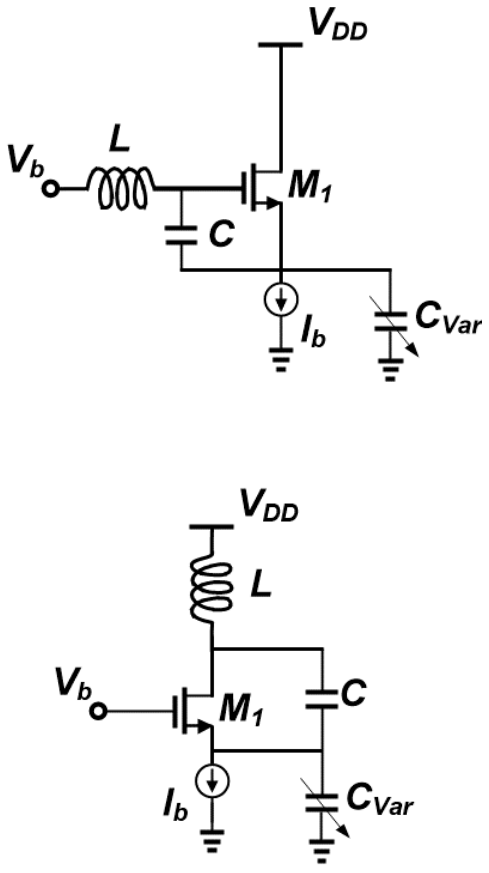


Fig. 3.5 Colpitts oscillator.

consumption expressed in mW. In this Chapter, all of the mentioned parameters will be studied.

3.3.2 Phase Noise (PN)

Fig. 3.6(a) and Fig. 3.6(b) show the output spectra of an ideal and noisy VCO, respectively. The output voltage of an ideal oscillator can be described as [45]-[46]:

$$V_{0ut} = Acos(\omega_0 t + \phi) \tag{3-10}$$

where A, ω_0 and ϕ are amplitude, oscillation frequency, and phase, respectively resulting in a spectrum at $\pm\omega_0$ without any sidebands. However, for a non-ideal oscillator, the output voltage is given as

$$V_{0ut} = A(t)cos\big(\omega_0 t + \phi(t)\big) \tag{3-11}$$

where amplitude and phase both are time-variant resulting in sidebands close to ω_0 and in most cases, phase variation is dominant. Phase noise is the popular way to quantify the output frequency content of a real VCO and is defined as

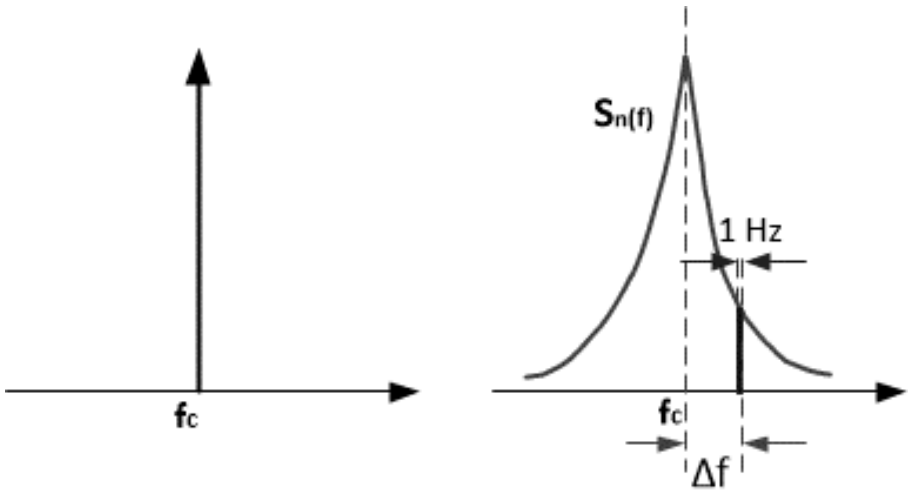


Fig. 3.6. Output spectrum of (a) an ideal VCO, (b) a real VCO.

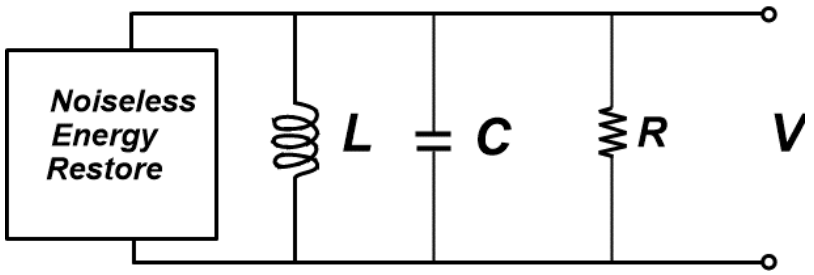


Fig. 3.7. Perfectly efficient RLC oscillator [46].

$$L(\Delta\omega) = 10\log\left(\frac{P_{sideband}\ (\omega_0+\Delta\omega,1\ Hz)}{Power\ of\ carrier}\right) \tag{3-12}$$

where $P_{sideband}$ is the single-sideband power at $\Delta\omega$ frequency offset from ω_0. For RLC tank shown in Fig. 3.7, mean-square noise voltage is

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f}.|Z|^2 \tag{3-13}$$

where $\frac{\overline{v_n^2}}{\Delta f}$ and $\frac{\overline{i_n^2}}{\Delta f}$ are the spectral density of the mean-square noise voltage and current, respectively, and Z is the tank impedance.

The equivalent mean square noise in the parallel resistance of tanks is equal to

$$\frac{\overline{i_n^2}}{\Delta f} = 4KTG \tag{3-14}$$

where k, T and G are the Boltzmann's constant, the absolute temperature and the tank conductance, respectively. Impedance of a parallel RLC-tank a small frequency offset from center frequency ($\Delta\omega << \omega_0$) can be approximated by

$$Z(\omega_0 + \Delta\omega) \approx j.\frac{\omega_0 L}{2\frac{\Delta\omega}{\omega_0}} \tag{3-15}$$

Q of the inductor is

$$Q = \frac{\mathrm{R}}{\omega_0 L} = \frac{1}{\omega_0 LG} \tag{3-16}$$

From (3-15) and (3-16), the impedance of tank is

$$|Z(\omega_0 + \Delta\omega)| = \frac{1}{G}\frac{\omega_0}{2Q(\Delta\omega)} \tag{3-17}$$

From (3-13) and (3-17), the spectral density of the mean-square noise voltage can be written as

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f}.|Z|^2 = 4kTR(\frac{\omega_0}{2Q(\Delta\omega)})^2 \tag{3-18}$$

which is frequency-dependent and the downward behavior is because of the tank filtering operation. From (3-13)-(3-18), a single-sideband spectral density, PN is given by

$$L(\Delta\omega) = 10log\frac{2\mathrm{kT}}{P_{sig}}\left(\frac{\omega_0}{2Q(\Delta\omega)}\right)^2 \tag{3-19}$$

and unit is (dBc/Hz).

This equation shows that the PN drops by the factor of $1/f^2$ or 20 dB/decade in the logarithmic system and it is clear that the quality factor of passive components affect PN performance by the factor of $\left(\frac{1}{Q}\right)^2$.

However, because of some simplifications, (3-19) does not describe the *1/f*^{3} behavior of spectrum, which is in practical measurements. Hence, Leeson added some modifications to (3-19) to predict this behavior

$$L(\Delta\omega) = 10\log[\frac{2FkT}{P_{sig}}\left(1 + \left(\frac{\omega_0}{2Q(\Delta\omega)}\right)^2\right)\left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)] \tag{3-20}$$

where *F* is the noise factor of the active device. This equation is also known as the Lesson-Cutler phase noise model and claims that $\Delta\omega_{1/f^3}$ is accurately equal to *1/f* corner of device noise. However, it is not completely fitted with the measurement results and does not predict the corner frequency and *F* factor when more than one source of *1/f* noises are present in the circuit. Flicker noise, thermal noise, the noise of the LC tank (Q of LC tank)

and noise figure of transistor amplifier all contribute to VCO PN. Based on (3-20), we can summarize the contribution of each noise on oscillator PN (SSB) as depicted in Fig. 3.8.

Later Ali Hajimiri [45], analyzed PN with a different approach which predicts $1/f^3$ behavior. For a better understanding that how phase variation can be translated in close to the oscillation frequency, assume $A(t) = A = 1$ and simplify (3-11) as below

$$V_{0ut} = cos\big(\omega_0 t + \phi(t)\big) = cos(\omega_0 t)cos\big(\phi(t)\big) - sin(\omega_0 t)sin\big(\phi(t)\big) \quad (3\text{-}21)$$

If $\phi(t) << 1$,

$$V_{0ut} \approx cos\big(\omega_0 t + \phi(t)\big) = cos(\omega_0 t) - \phi(t)sin(\omega_0 t) \quad (3\text{-}22)$$

For low frequency impulse noise sources ($i(t)_{low} = I_0 cos(\Delta\omega t)$), phase function is given by

$$\phi(t) = \frac{I_0 C_0}{2q_{max}} \frac{sin(\Delta\omega t)}{\Delta\omega} \quad (3\text{-}23)$$

so

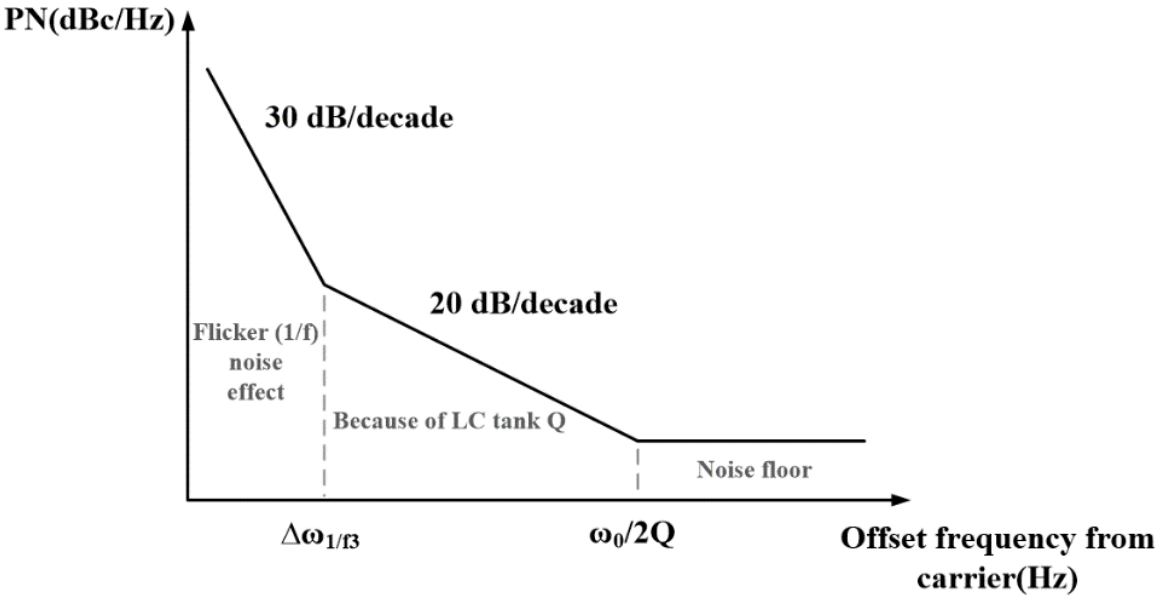


Fig. 3.8. General PN (SSB) characteristic.

$$\phi(t)sin(\omega_0 t) = \frac{I_0 C_0}{2q_{max}} \frac{sin(\Delta\omega t)}{\Delta\omega}\ sin(\omega_0 t) = \frac{I_0 C_0}{2q_{max}} \frac{1}{2} \cos[(\omega_0 \pm \Delta\omega)t] \quad (3\text{-}24)$$

Equation (3-24) shows that any low frequency noises such as the 1/f noise of transistors at Δω, will up-convert to the main carrier frequency with $\pm\Delta\omega$ offset. Moreover, all of the sideband noises around harmonics can be down converted around the main carrier frequency. Assume side band noises around n^{th} harmonic $i(t)_n = I_n cos(n\omega_0 + \Delta\omega t)$, phase function can be calculated as

$$\phi(t) = \frac{I_n C_n}{2q_{max}} \frac{sin(\Delta\omega t)}{\Delta\omega} \quad (3\text{-}25)$$

which results in

$$\phi(t)sin(\omega_0 t) = \frac{I_n C_n}{2q_{max}} \frac{sin(\Delta\omega t)}{\Delta\omega}\ sin(\omega_0 t) = \frac{I_n C_n}{2q_{max}} \frac{1}{2} \cos[(\omega_0 \pm \Delta\omega)t] \quad (3\text{-}26)$$

Hence, the injected current at $n\omega_0 + \Delta\omega$ generates sideband around $\pm\Delta\omega$ of the carrier signal.

3.3.3 Tuning Range

For a conventional cross-coupled LC-VCO, oscillation frequency is equal to $f_{osc} = \frac{1}{2\pi\sqrt{LC}}$ and with a fixed inductor (L), FTR can be obtained

$$FTR = \frac{f_{max-} f_{min}}{\frac{(f_{max+} f_{min})}{2}} = 2\frac{(\sqrt{C_{var,MAX} + C_{Par,FIX}} - \sqrt{C_{var,MIN} + C_{Par,FIX}})}{(\sqrt{C_{var,MAX} + C_{Par,FIX}} + \sqrt{C_{var,MIN} + C_{Par,FIX}})}, \quad (3\text{-}27)$$

where f_{max} / f_{min} , $C_{par,FIX}$, $C_{var,MAX}$ and $C_{var,MIN}$ are the maximum /minimum oscillation frequency, fixed parasitic capacitance, the maximum and minimum capacitance of the varactors, respectively. Assuming $C_{Par,FIX} = \alpha C_{var,MIN}$ and varactor's maximum tuning range is given by $TR_{var,MAX} = \frac{C_{var,MAX}}{Cvar,MIN}$, (3-27) can be simplified to:

$$FTR = 2\frac{(\sqrt{\frac{TR_{var,MAX}+\alpha}{1+\alpha}}-1)}{(\sqrt{\frac{TR_{var,MAX}+\alpha}{1+\alpha}}+1)}. \quad (3\text{-}28)$$

For maximum *FTR*, $TR_{var,MAX}$ should be maximized as $\frac{(\sqrt{X}-1)}{(\sqrt{X}+1)}$ is a strictly increasing function of *X,* and α should be minimized. Here α is determined by the ratio of the sum of fixed capacitors of other circuit element in parallel to the varactor to $C_{var,MIN}$. $TR_{var,MAX}$ is limited by Q of varactor and the latter depends on the size of the transistors that produce *-2/gm* resistance required for compensating the losses of the LC-tank. According to Fig. 3.9, the maximum achievable FTR for the VCO with typical $TR_{var,MAX} = 2.5$ and α=4 is approximately 13% which is almost in the same range reported in mm-wave VCOs [57].

Fig. 3.10(a) shows the layout of the varactor fabricated in a 65nm CMOS process where Open-Short-DUT de-embedding method is utilized for the device characterization. The measured capacitance and quality factor of the fabricated varactor are plotted in Fig. 3.10(b) where the maximum and minimum capacitances are 22 fF and 56 fF for the control voltages of -1V to 1.5V, respectively resulting in $TR_{var,MAX}$ of 2.5 and Q of 6 to 22. The scaling of the varactor width does not change $TR_{var,MAX}$ as the ratio of C_{max}/C_{min} both increase and decrease by the same factor. Increasing

varactor length however may improve the $TR_{var,MAX}$ at the price of increasing channel resistance which lowering Q of the varactor as Q factor is given by

$$Q = \frac{1}{\omega C R_S}, \quad (3\text{-}29)$$

where

$$R_S = \frac{1}{12\times A}\left(R_{nw,\square}\times L^2 + R_{poly,\square}\times W^2\right). \quad (3\text{-}30)$$

where A is varactor area, L and W are the length and width of each finger, $R_{nw\square}$ and $R_{poly\square}$ are the sheet resistance of n-well and polysilicon gate layer [47]; As $R_{poly\square}$ is small compared to $R_{nw\square}$, L determines the total series resistance and quality factor of varactor [47].

Equation (3-29) and (3-30) show that increasing channel length of varactors, decreases its quality factor. Moreover, Equation (3-27) verified by the measurement results in Fig. 3.10(c), indicates that the quality factor of a varactor is reduced to single digits as frequency moves into mm-wave region. Note that the quality factor of the tank for a VCO can be expressed as below

$$\frac{1}{Q_{tank}} = \frac{1}{Q_{var}} + \frac{1}{Q_{ind}} \approx \frac{1}{Q_{var}}, \tag{3-31}$$

At mm-wave frequencies, $Q_{var} \ll Q_{ind}$ and (3) can be simplified as

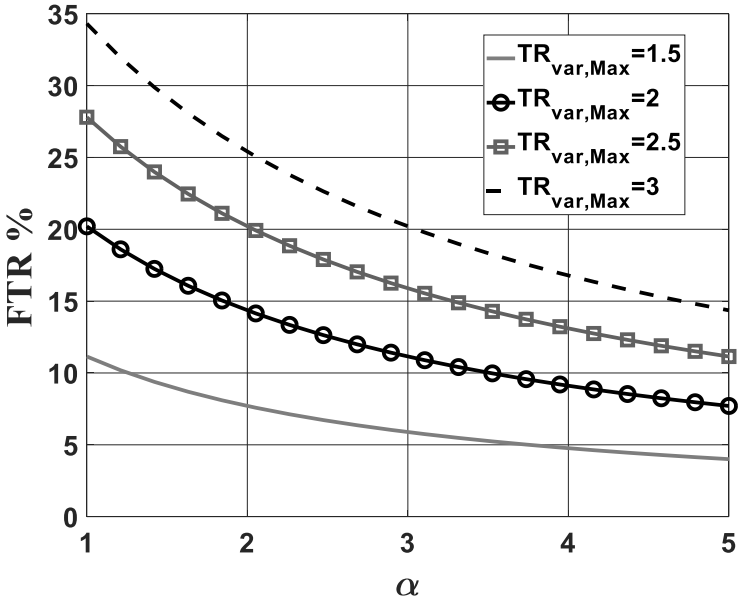


Fig. 3.9. Calculated FTR versus α.

$$Q_{tank} \approx Q_{var}, \tag{3-32}$$

It shows that the quality factor of varactor defines the quality factor of tank in mm-wave frequencies. The higher the losses of the tank (the lower quality factor of the tank), the larger transistor is required to overcome the losses resulting in lower alpha values and FTR.

From [48], the phase noise of a VCO can be express as

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{2kT}{P_S}\left(\frac{\omega_0}{2Q_{tank}\Delta\omega}\right)^2\right], \tag{3-33}$$

where k is the Boltzmann's constant, T is the absolute temperature and P_S is the output signal power. From (3-32) and (3-33), phase noise would be degraded drastically if LC-tank quality factor is low ($PN \sim \frac{1}{Q^2}$), and the tank quality factor is almost determined by Q_{var}. Therefore, enlarging varactor channel length is not a good solution for low phase noise and wide tuning range VCO design as it increases $C_{par,FIX}$, lowers resonance frequency and degrades Q of LC-tank drastically which needs high DC power for startup condition [11] and [49].

3.3.3.1 Varactor de-embedding

As it is shown in Fig. 3.11, varactor is connected to the signal pads (S) by a 66um GCPW as long as the minimum distance between two GSG probes recommended is 150um to reduce the coupling between the probes in measurement process (for my design that is 142 um). These lines and pads can be modeled as inductor and capacitor which are extra parasitic resulting in inaccuracy of measured data for DUT. Hence this parasitic must be removed. There are several ways to remove parasitics from the measurement and extract raw data.

Open-Short-DUT (device under test) method which is widely used in RF/mm-wave measurements is utilized for varactor characterization. First of all, we did S-parameter measurement using two GSG probes connected to the VNA for all cases and collected the data. Three-step de-embedding methods is proposed [50] up to few GHz. Five-step de-

embedding method for frequency up to 50GHz is presented in [51]with about 15 elements which is very complicated.

As long as we need only accurate results for the measured device, WinCal XE4.5 tools from Cascade Microtech are utilized for de-embedding and producing raw S-parameters of the varactor. Then we used ADS to plot the extracted data. It worthwhile to mention that in ADS gate terminal (shown in the figure) was connected to 50 Ohms port and drain/source to ground. Hence, the junction capacitors between drain/source and substrate are shorted to the ground and maximum TR is measured from gate side.

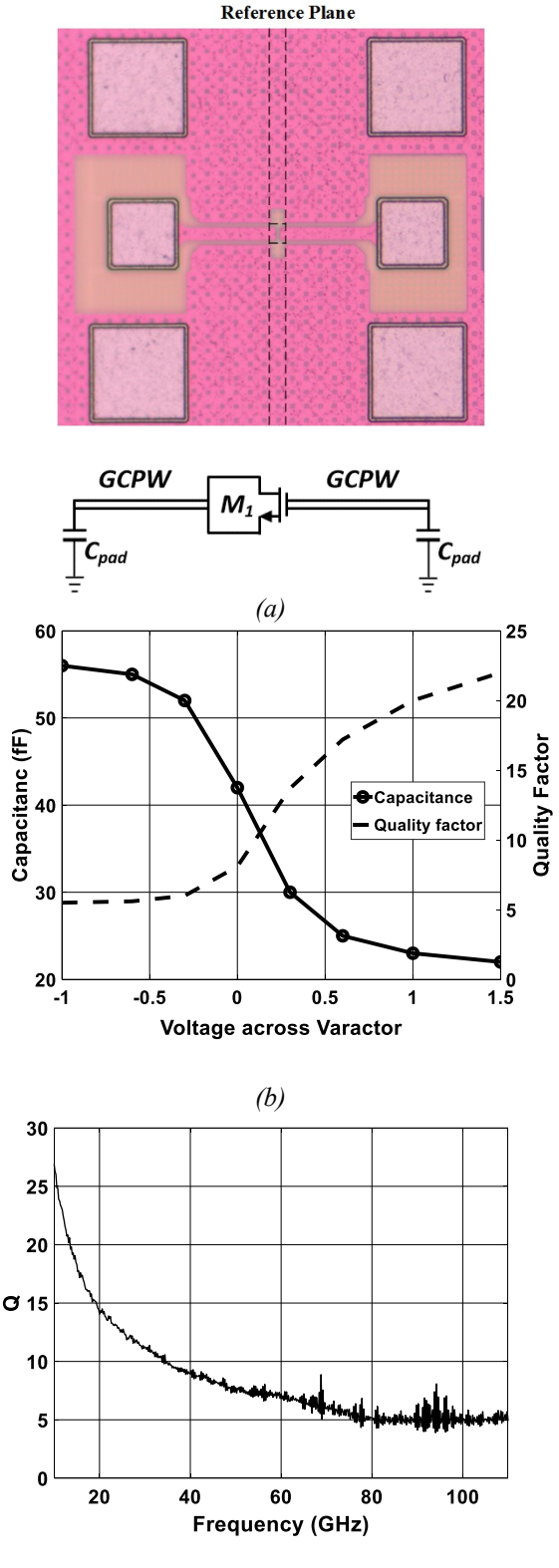


Fig. 3.10. (a) Chip micrograph of varactor, (b) measured capacitance and quality factor against various voltages, and (c) measured quality factor vs frequency in low Q mode.

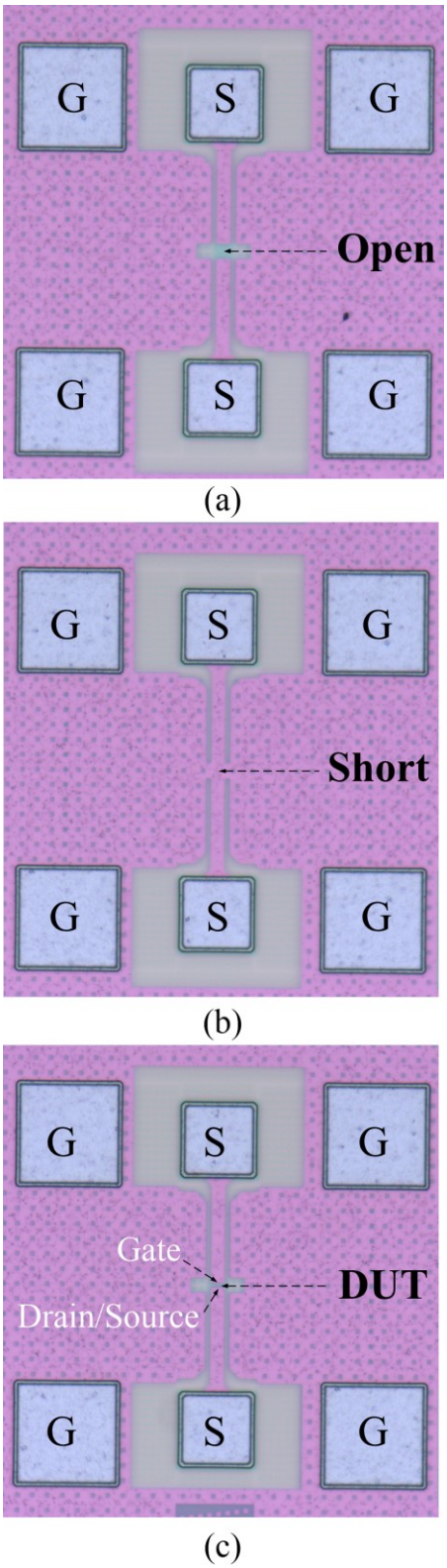


Fig. 3.11. Fabricated chip photo for Open-Short-DUT de-embedding method, (a) Open, (b) Short, and (c) DUT.

In summary, achieving a large FTR (e.g more than 20%) is not possible using long channel varactors for tuning oscillation frequency of LC-tank VCOs at mm-wave frequencies. Hence, several techniques are proposed to overcome these limitations as discussed in the next section.

3.3.4 Power consumption and area

Power consumption and chip area are two important parameters in VCOs design where the first and second parameters are added to the dc power and cost of the full system, respectively. In order to decrease the dissipated power, Q of the tank should be increased resulting in lower negative resistance needed for oscillation.

3.4 Wide Frequency Tuning Range VCOs

3.4.1 Low GHz Wide FTR VCOs

At low GHz frequencies, a parallel combination of high-Q switched capacitors/inductors and MOS varactors is used as the most common solution for obtaining large tuning range and low phase noise (PN) VCO design where switched capacitors/inductors are used for coarse tuning and varactors are used for fine-tuning of VCO frequency, respectively [53]-[60]. In [55], a switched resonator is proposed for low PN and wide FTR oscillator with a fundamental frequency below than 2 GHz (Fig. 3.12). To minimize the coupling effect between $L_{1(2)}$ and $L_{3(4)}$, the inductors are separated, and by controlling the gate voltage of M_3 and M_4, tank inductance can be tuned. When the switch transistors are on, L_1 and L_3 are determining the equivalent inductance of the tank. When the switches are off, the tank inductance is $L_1 + L_2$ and $L_3 + L_4$.

An ultra-wideband transformer-based VCO is presented in [56] where the transformer-based variable inductor (VID) which is explained later in this section and switched capacitors are used simultaneously (Fig. 3.13). However, at mm-wave frequencies, *LC*-tank quality factor (Q) drops drastically, when the switches are connected in series with the capacitors and inductors. Hence, to achieve a well-controlled oscillation using the aforementioned methods, the size of the switching transistors should be increased to compensate for the loss of *LC*-tank. As a result, in addition to the higher power dissipation, the large fixed parasitic capacitance of these transistors limits the maximum oscillation frequency and tuning range of mm-wave VCOs [49], [55] and [61]. In addition, other mm-

wave VCOs performance parameters such as the output power and phase noise are adversely affected by low Q of *LC*-tank mostly caused by low Q of varactors at mm-wave frequencies [49].

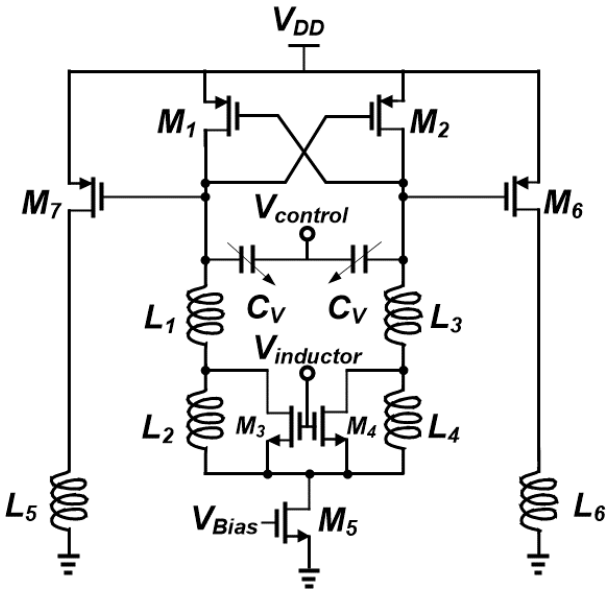


Fig. 3.12. Switched resonator VCO in [55].

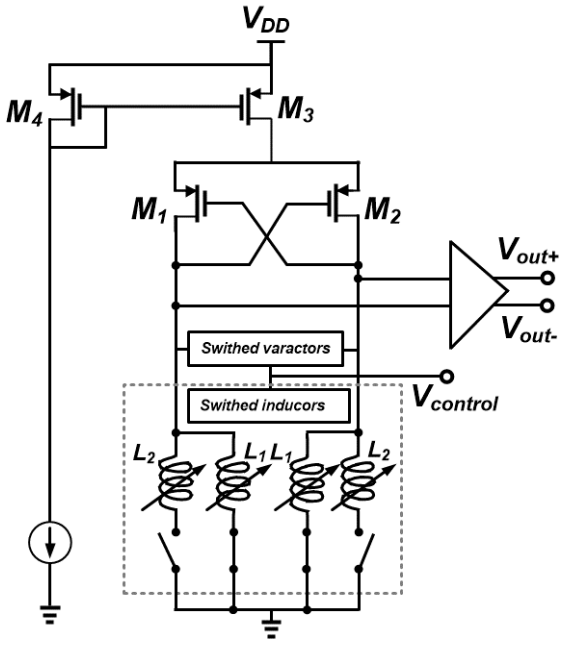


Fig. 3.13. VCO based on switchable inductors and varactors [56].

3.4.2 Mm-wave Wide FTR VCOs

In recent years, several solutions have been proposed for achieving a wide tuning range for mm-wave *LC*-VCOs. In the first approach, inductive tuning [3]-[6] and mode switching methods [11], [62]-[66] are used to compensate the limited varactor tuning range. In [3], a wide FTR VCO is described which utilizes a VID implemented by a tunable resistor as the transformer load. Furthermore, the transformer-based VID exhibits lower Q in comparison with that of the conventional inductors degrading PN performance of the VCO.

Capacitive-loaded transformers are the next alternative method for implementation of continually tunable VIDs allowing for large VCO tuning range [3]; nevertheless, the low Q of LC-tank results in poor PN and high power dissipation. In [4]-[6], an inductive-loaded transformer is proposed as another alternative for VID that utilizes current return path switching on different locations of the secondary winding. However, the loss of required

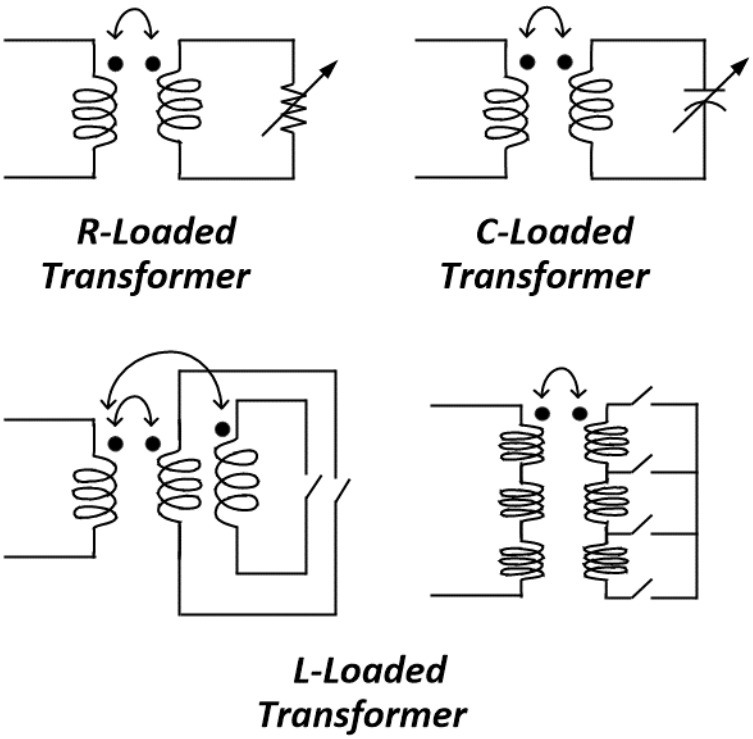


Fig. 3.14. Existing transformer-based VIDs [5].

switches further drops the quality factors of VIDs. Moreover, in some cases, effective sub-bands are limited because of the design complexity [5].

A continuous wide FTR VCO based on magnetically coupled LC network is implemented in [11], where even and odd modes combinations are employed to increase the FTR. In the odd mode, higher parasitic resistance than even mode is introduced to the inductors, which degrades phase noise performance of the VCO. In [62], by controlling the coupling coefficient of a compact switched-triple transformer, the tuning range of the VCO is increased. In summary, all the VCOs in this category exhibit relatively poor PN performance because of low-Q of VIDs.

The second technique is to design the mm-wave VCOs by multiplying the frequency of a VCO operating in sub-mm-wave region where high-Q varactors are available. However, these VCOs suffer from the low output power due to the loss of the multiplier, and occupy more chip area because of the larger inductors are required compared to those in mm-wave VCO designs.

In [24], a wide FTR *LC*-VCO is demonstrated that utilizes a passive multiplier (×4) with minimum fundamental to 4^{th} harmonics power conversion loss of 12.4 dB using switched variable inductors. Another wide tuning range VCO is demonstrated in [61] that employs two switchable coupled VCO-cores in low mm-wave frequency to cover the wide frequency range by combining low and high bands, and a frequency doubler provides a weak single-ended output signal. In both cases, the output signal has very limited output power because of the loss of multiplier necessitating the use of an ultra-wideband mm-wave power amplifiers (PA). As an example, a third-harmonic VCO is reported in [69], where a 3-stages power amplifier is used to deliver 0 dBm power to the output (Fig. 3.15).

3.4.3 Multi-core Wide FTR VCOs

Multi-core VCOs consisting of two or more coupled VCOs with overlapping frequency range can be used for design of ultra-wideband VCOs [61], [67], [70]-[74]. As shown in Fig. 3.16, Core switching method is suggested for high FTR without using output power combiner for low-GHz VCOs in [67] and [68]. However, the used switches are directly placed in the signal path which can degrade the PN performance and limit FTR in mm-wave frequencies because of added parasitic capacitance.

In other circuits, a transformer or coupled inductors provide two or more resonance modes that can be enabled by activating the corresponding core. However, the on-chip

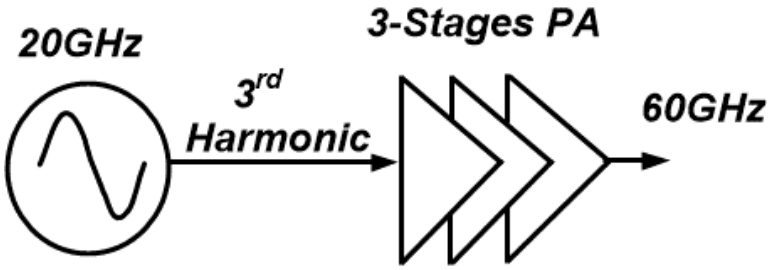


Fig. 3.15. Harmonic boosting VCO [69].

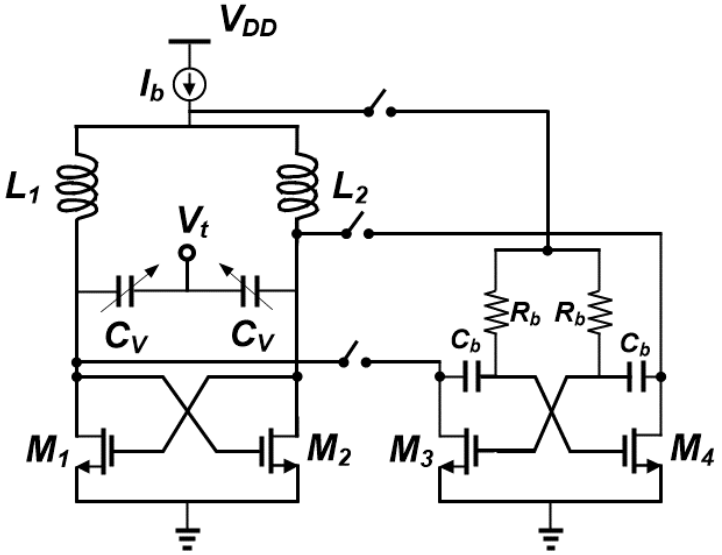


Fig. 3.16. Dual-core VCO [67].

transformers or coupled inductors exhibits much lower quality factor compared to the standalone inductors resulting in degraded their PN performance and increased power consumption. Moreover, the output power of these individual cores must be combined using active or passive power combiners in order to produce a single output wideband VCO. The use of these additions and often bulky power combiners further adds to the overall cost of these VCOs.

Switched buffer VCOs are used to provide wide FTR in low-GHz frequencies which employ two or more VCO cores connected to switchable buffers with a shared inductor [85]. For a two-core switched buffer VCO, at least three center-tapped inductors (or six individual inductors) are needed (Fig. 3.17); two for VCO cores and one for each buffer stage which must be with two VCO cores even when the output buffer stage is not needed for some applications.

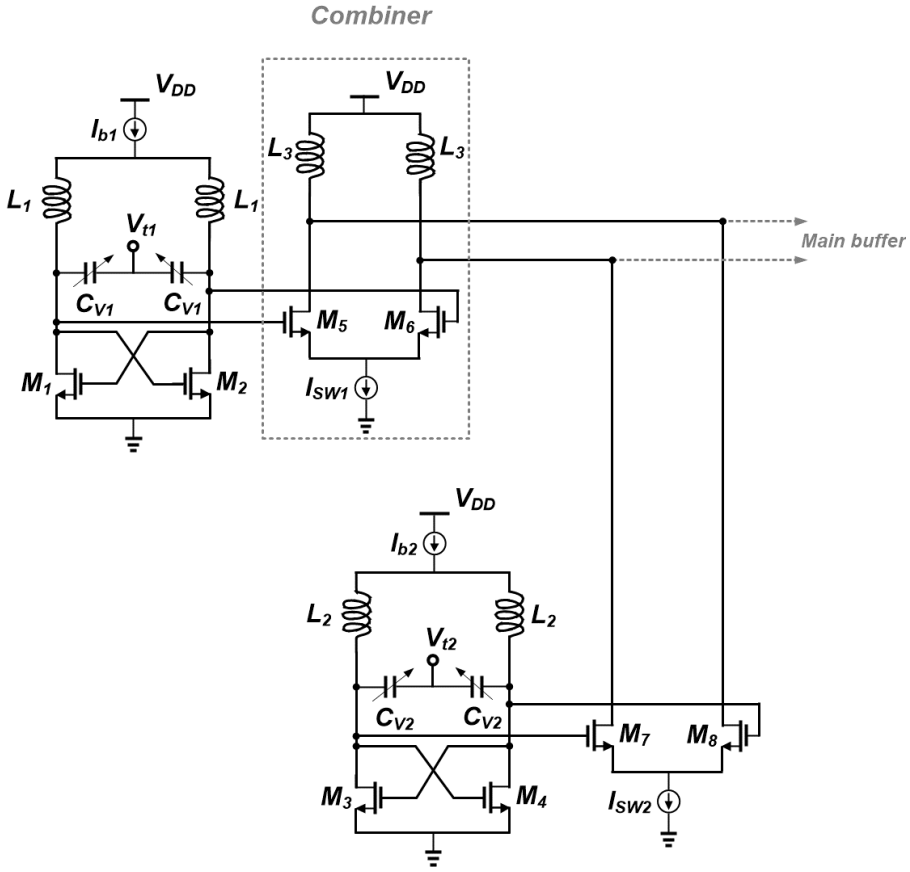


Fig. 3.17. VCOs with switched buffers.

3.5 Conclusion

In summary, achieving a large FTR (e.g. more than 20%) is not possible using CMOS varactors with minimum channel length as the overlap capacitors will limit the capacitance range that can be produced by these devices. Use of long channel varactors for tuning oscillation frequency of LC-tank VCOs at mm-wave frequencies is also not a good solution because of their low-quality factor resulting in significant phase noise degradations.

Switched capacitor arrays, switched inductors and resonators are commonly used for low-GHz wide FTR VCO design. However, at mm-wave frequencies, because of the trade-off between the on-resistance and parasitic capacitance produced by switches, it is not possible to produce high Q switched-capacitor structures.

Harmonic VCOs can generate wide FTR signal along with good PN at sub-mm-wave frequencies and provide the harmonics at mm-wave band. However, the required frequency multipliers add to the cost and power consumption of the overall VCO and often result in the structure with a low output power level. Magnetically coupled multi-core VCOs and loaded transformer-based variable inductors (VIDs) exhibit low-quality factor degrading the phase noise of these VCOs.

Chapter 4

A Wide Tuning Range, Low Phase Noise and Area Efficient Dual-Band CMOS VCO

4.1 Operation Principle and Tuning Range

The general idea of a dual-mode VCO utilizing coupled inductors can be explained using the circuit diagram shown in Fig. 4.1(a). The cores can be designed to oscillate at different oscillation frequencies as their *LC*-tanks exhibit different resonance frequencies shown in Fig. 4.1(b) as the input impedance of coupled inductors varies depending on which core is switched on and which one is switched off. However, for the coupled dual-band VCO, the high and low oscillation frequencies (ω_L and ω_H) of two cores are dependent as given by [62]

$$\omega_{H/L}^2 = \frac{{\omega_1}^2 + {\omega_2}^2 \pm \sqrt{({\omega_1}^2 - {\omega_2}^2)^2 + 4k^2{\omega_1}^2{\omega_2}^2}}{2(1-k^2)}, \quad (4\text{-}1)$$

where $\omega_1<\omega_2$, $\omega_1 = \frac{1}{\sqrt{L_1C_1}}$ and $\omega_2 = \frac{1}{\sqrt{L_2C_2}}$ are resonance frequencies of separate cores, and k is the coupling factor of coupled inductors. In other words, if the cores are decoupled (k=0), the separate cores will oscillate at

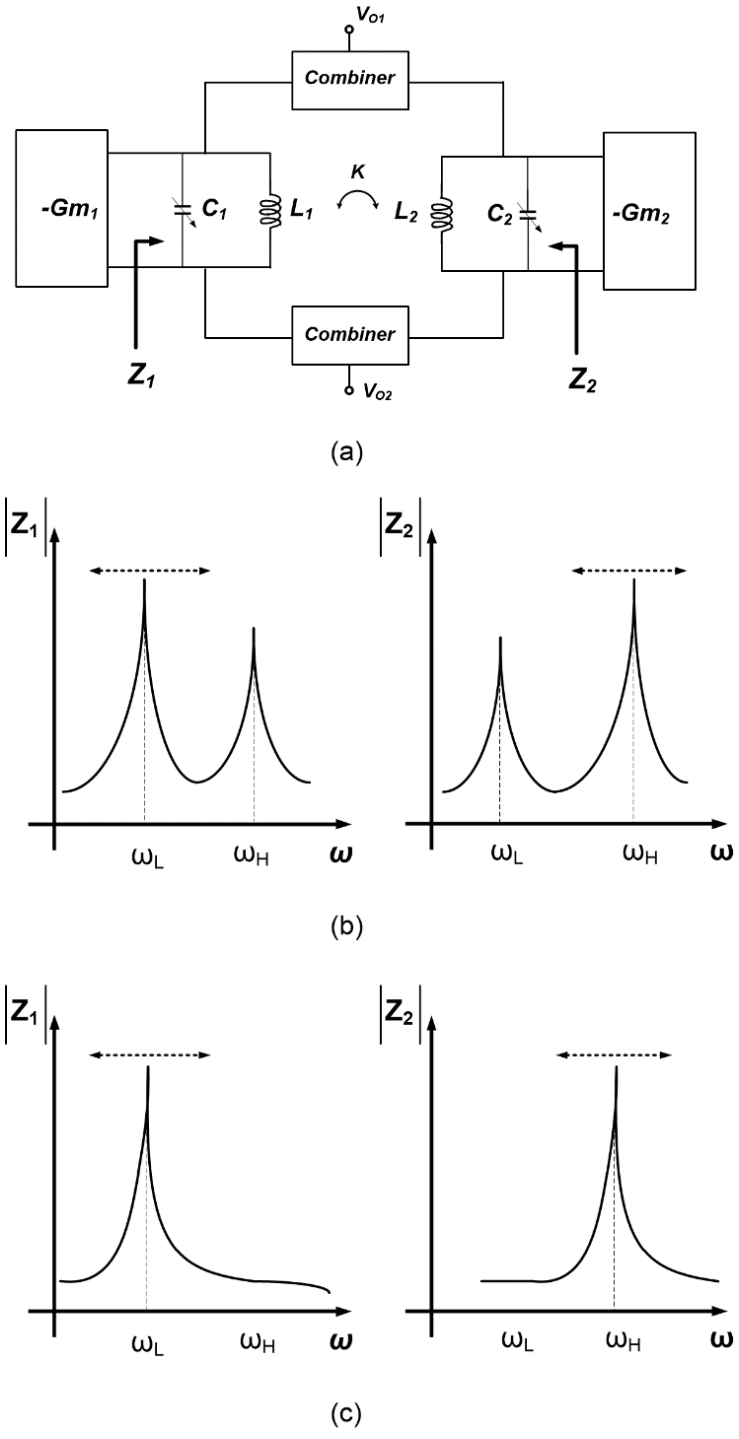
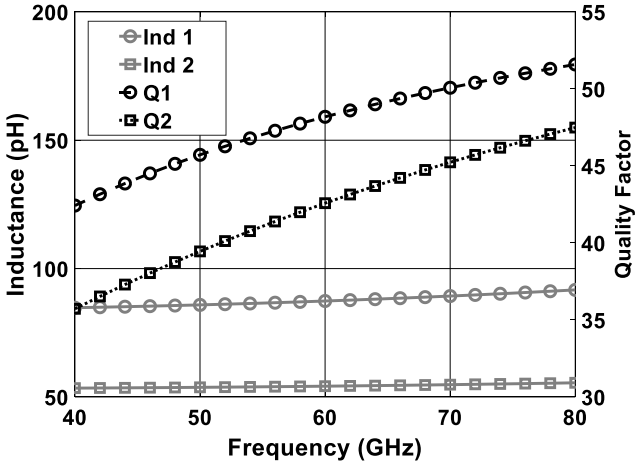


Fig. 4.1. (a) Impedance response of a dual-band VCO (b) weakly coupled inductors k≠0 (c) decoupled inductors k=0.

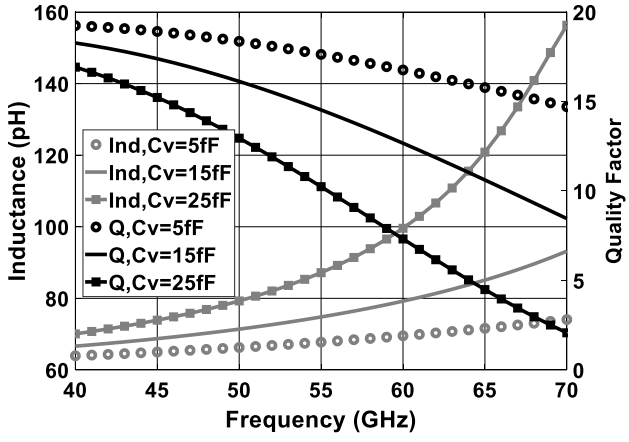
$$\omega_L = \omega_1 = \frac{1}{\sqrt{L_1 C_1}} \tag{4-2}$$

$$\omega_H = \omega_2 = \frac{1}{\sqrt{L_2 C_2}} \tag{4-3}$$

The major problem of the resonators with coupled inductors is their poor quality factors compared to standalone inductors, especially when the varactor is operating in high-Q mode. For example, the reported Q of the coupled inductors are around 10-15 in [3]-[6]. To make a fair comparison, the used standalone inductors and a capacitive-loaded VID in high-Q mode [3], are simulated in HFSS 3D EM simulator, and the results are shown in Fig. 4.2(a) and Fig. 4.2(b), respectively.



(a)



(b)

Fig. 4.2. EM simulated inductance and quality factor of (a) utilized standalone inductors (b) a transformer-based VID loaded by Cv= 5, 15 and 25 fF in parallel with a 900 Ω resistor (high-Q mode) [3].

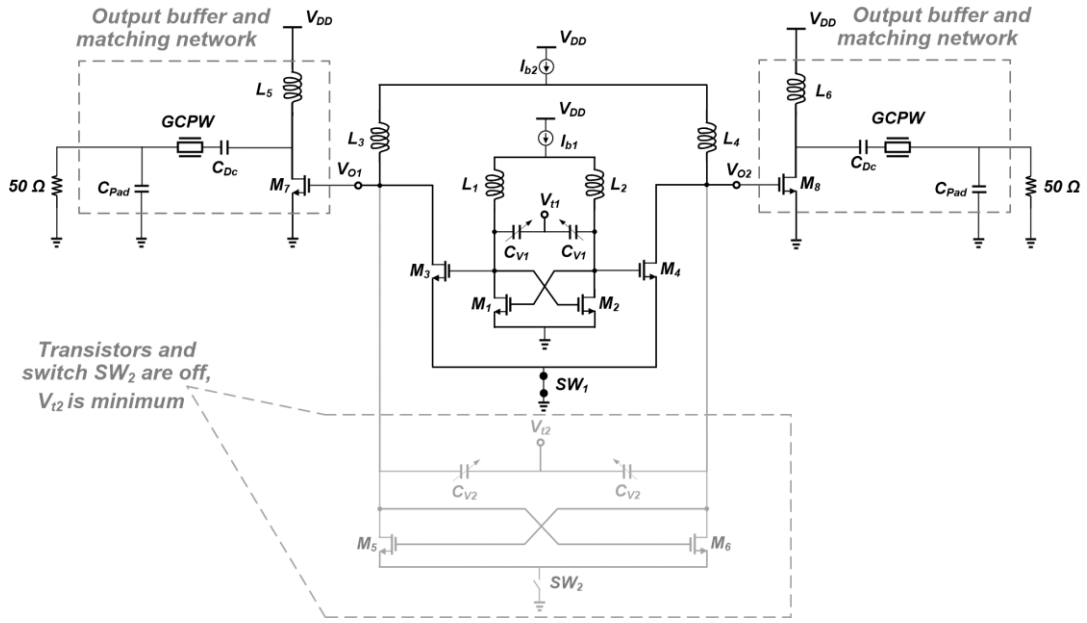
It is clear that the Q of standalone inductors are more than 30 for the entire frequency range of 40 GHz to 80 GHz. While for a Q close to 20 can be obtained for VID for the portion of the frequency band where its inductance does not vary significantly, it drops significantly to values in the range of 18 to 5 for the frequency range that the VIDs' inductance varies noticeably with the load capacitor.

The low quality of coupled inductors significantly degrades the PN performance of these dual-mode VCOs. Hence, creating a dual-band VCO with de-coupled cores (standalone inductors) is the proposed approach in this chapter for obtaining a high FTR while maintaining a low phase noise.

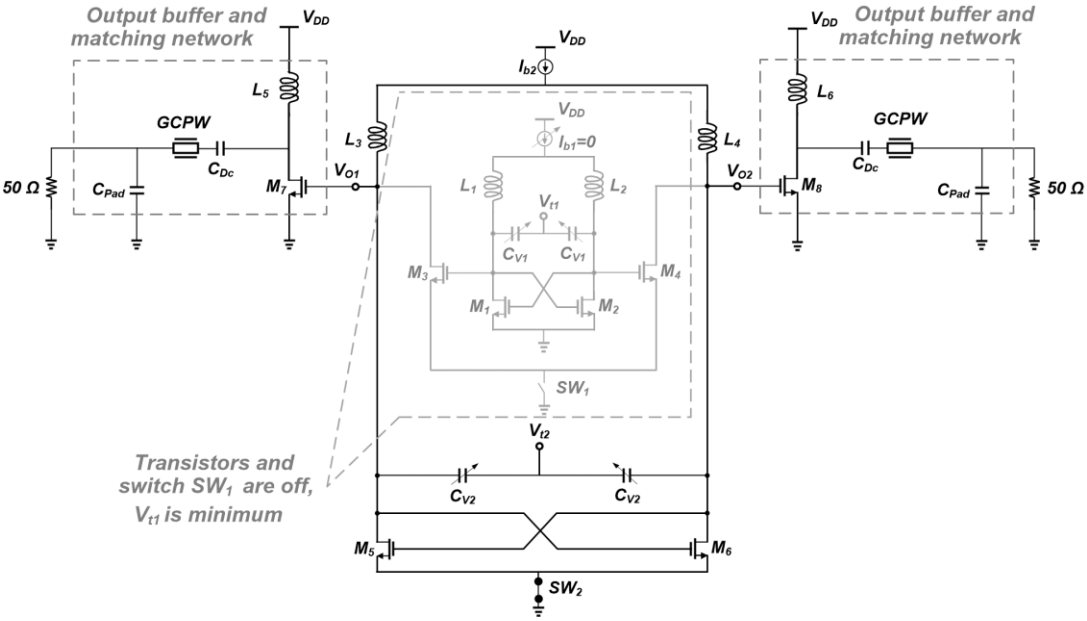
Fig. 4.3 shows the proposed dual-band VCO, where two switchable decoupled cores are utilized to achieve a high FTR in mm-wave frequencies while the output of the low-frequency band (LFB) and high-frequency band (HFB) operation can be obtained at the same output port and does not need any bulky passive/active voltage combiner.

By taking advantage of high-Q standalone inductors and small-sized high-Q varactors for both cores, high-Q *LC*-tank is achievable for such a conventional cross-coupled VCO. Transistors $M_{1\text{-}2}$ and $M_{5\text{-}6}$ are the cross-coupled pairs for LFB and HFB, generating the required negative resistance for oscillation. I_{b1} and I_{b2} are provided by large PMOS devices which force the dc currents of the cores. Moreover, by controlling I_{b1}, the LFB VCO can be switched on and off. The switches (SW_1 and SW_2) select the oscillation or buffering mode for the second *LC*-tank ($L_{3\text{-}4}$ and C_{v2}).

When SW_1 is on, and SW_2 is off, second core plays as a common-source amplifier which buffers the generated signal from the first core (LFB), as illustrated in Fig. 4.3(a). Conversely, when SW_1 is off, SW_2 is on, and I_{b1} is zero, the first core is off, and cross-coupled transistors ($M_{5\text{-}6}$) are on which provide oscillation condition for the second core (HFB), which is marked in Fig. 4.3(b).



(a)



(b)

Fig. 4.3. Proposed dual-band VCO at, (a) its LFB operation, and (b) HFB operation.

4.2 Effect of Added Buffer on FTR and Voltage Swing

In order to obtain a continuous frequency tuning range, the low and high bands should be designed with a sufficient overlap. Compared to a conventional VCO with the same size of the cores, the tuning range of the proposed circuit is equal to the sum of tuning ranges of two individual cores less the overlap range.

Now, the added buffer stage is designed in such a way that it does not occupy any extra chip area reusing the inductors of HFB core. For the LFB operation, the buffer ($L_{3\text{-}4}$ and $M_{3\text{-}4}$) does not affect tuning range as it does not introduce any parasitic capacitor more than that if it was directly connected to the output buffer. For the HFB, shown in Fig. 4.3(b), the single-ended fixed parasitic capacitance of the *LC*-tank (C_{P_fixHFB}) is

$$C_{P\_HFBfix} \approx C_{GS5\,(6)} + C_{DB5\,(6)} + 4 \times C_{GD5\,(6)} + C_{P_{Out}} + C_{Poff_{LFB}}, \tag{4-4}$$

where C_{GS}, C_{DB}, C_{GD}, C_{P_out} and C_{Poff_LFB} are gate-source, drain-bulk, gate-drain, output buffer, and LFB parasitic capacitors, respectively. The total capacitance contributed by $M_{3(4)}$ is

$$C_{Poff\_LFB} \approx C_{DB\_M3\,(4)} + C_{GD\_M3\,(4)} \tag{4-5}$$

The simulation results for C_{P_fixHFB} and C_{Poff_LFB} are shown in Fig. 4.5. They are extracted from the models of transistors provided by the foundry and EM models of passive structures simulated in HFSS. Based on these results plotted in in Fig. 4.5, the first core has added about 10 fF of parasitic capacitance to this node with minimal effect on HFB tuning range. As the inductor L_3 and L_4 are chosen to produce HFB oscillation and operate as the buffer of LFB core, there will be a mismatch between the resonance frequencies of *LC*-tanks in these two modes of the operation. To bring the buffer tank resonance frequency closer to that of LFB core, the HFB varactors control voltage must be set to produce the largest capacitance values possible. The minimum resonance frequency of the buffer tank (f_{minoff_HFB}) can be obtained as

$$f_{minoff\_HFB} \approx \frac{1}{2\pi\sqrt{L_{3(4)}(C_{var,MAX} + C_{Poff_{HFB}} + C_{P_{Out}})}} \quad (4\text{-}6)$$

where $C_{var,MAX}$, f_{minoff_HFB} and C_{Poff_HFB} are the maximum and minimum capacitance of the varactors, minimum operation frequency and parasitic capacitance of LFB in off mode, respectively. Fig. 4.6 shows the simulated buffer resonance impedance when V_{t2} is at minimum and maximum voltages indicating that the resonance frequency has been reduced from 74 GHz to 63 GHz. However, because of the lower quality of varactors producing the maximum capacitance, the tank maximum impedance is reduced from 180 Ω to 110 Ω.

Nevertheless, it produces an impedance larger than that can be produced by an untuned buffer. As a result of lower impedance in the LFB range of 50 Ω, the output signal power is reduced. This effect can be seen in time-domain simulations of the output voltage of LFB

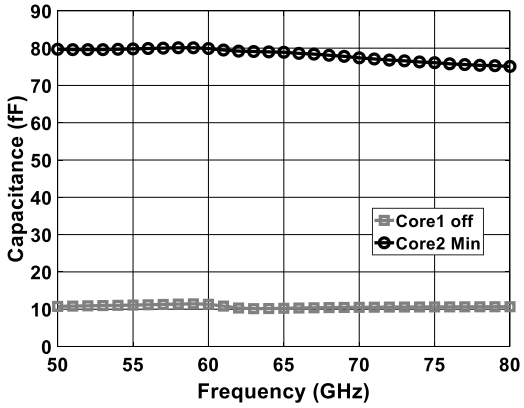


Fig. 4.4. Simulated fixed parasitic capacitance for HFB (Core2 Min) and contributed by $M_{3(4)}$ (Core1 Off).

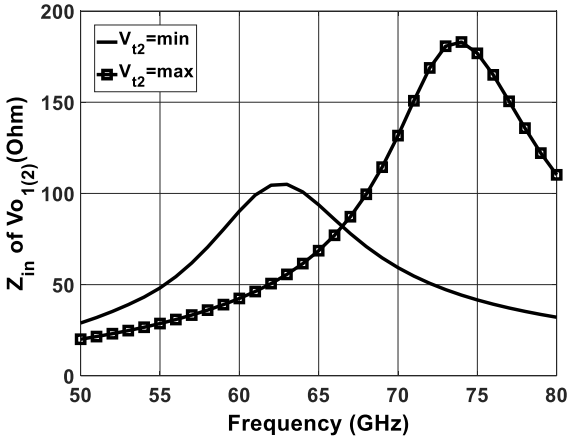


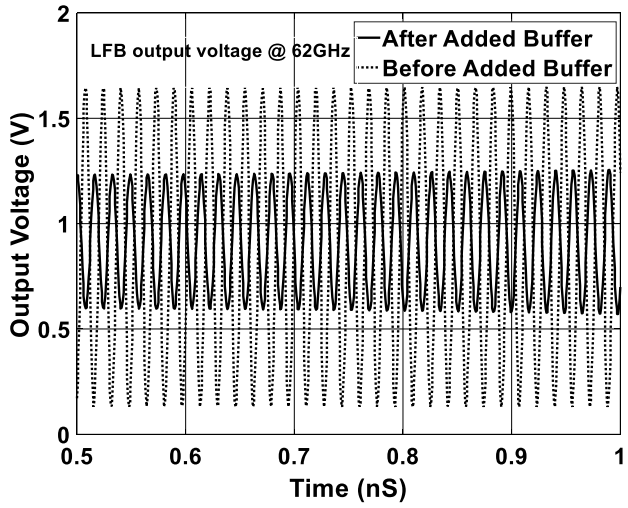
Fig. 4.5. Simulated impedance of $V_{O1(2)}$ when the VCO operates at LFB and the second core is off.

before and after the added buffer as depicted in Fig. 4.6(a) and Fig. 4.6(b), respectively. However, still the minimum output power is enough according to the comparison table.

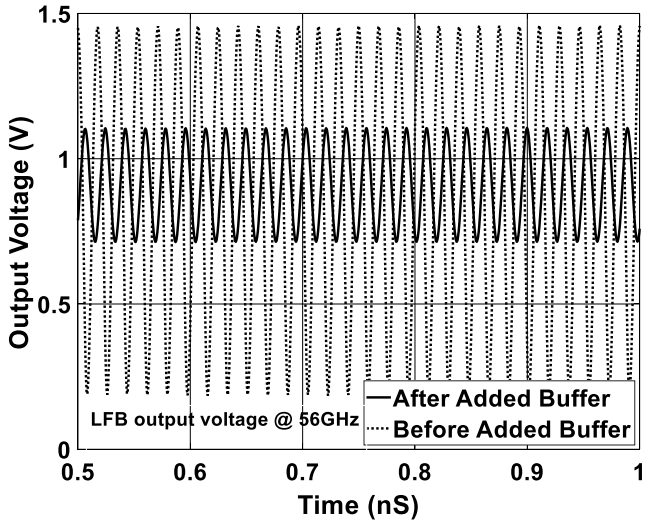
4.3 PN Improvement

As discussed before, Q of a standalone inductor is more than 30 while it is less than 15 of VIDs/coupled inductors. Q of an LC-tank affects the phase noise performance of a VCO [48], which can be expanded to

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{2kT}{P_S}\left(\frac{\omega_0}{2\Delta\omega}\right)^2\right] + 10\log\left[\left(\frac{1}{Q_{tank}}\right)^2\right], \quad (4\text{-}7)$$



(a)



(b)

Fig. 4.6. Simulated output voltage of HFB before and after added buffer at (a) 62 GHz, (b) 56 GHz.

The PN difference for the decoupled and coupled *LC*-tanks with the corresponding Qs of $Q_{tank,Stand}$ and $Q_{tank,VID,}$ respectively, can be expressed as

$$\Delta\mathcal{L}(\Delta\omega) = 10\log\left[\left(\frac{Q_{tank,VID}}{Q_{tank,Stand}}\right)^2\right], \tag{4-8}$$

where

$$Q_{tank,Stand} = \frac{Q_{Ind,Stand} \times Q_{Var}}{Q_{Ind,Stand} + Q_{Var}}, \tag{4-9}$$

$$Q_{tank,VID} = \frac{Q_{Ind,VID} \times Q_{Var}}{Q_{Ind,VID} + Q_{Var}}, \tag{4-10}$$

and Q_{Var}, $Q_{Ind,Stand}$ and $Q_{tank,VID}$ are the quality factors of the varactor, Q of the inductor with standalone and VID (coupled) inductors, respectively.

Assuming the underestimated Q of a standalone inductor equal to 30 and different Q of VID and varactor, PN improvement is depicted in Fig. 4.7. For example, $Q_{VID} = 10$ and $Q_{Var} \geq 10$, results in 3.5 to 5 dB better PN performance.

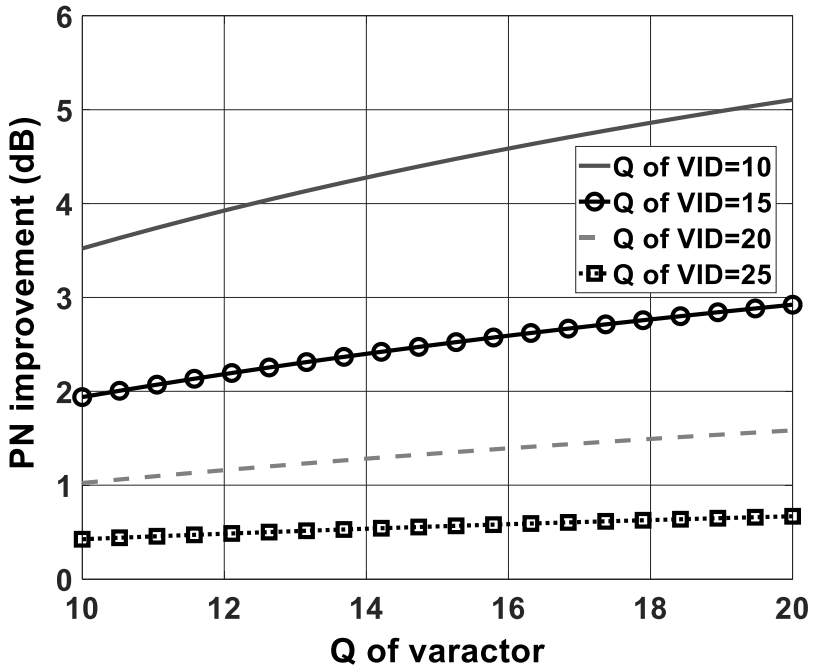


Fig. 4.7. Calculated PN improvement vs Q of varactor and VID with standalone inductor Q of 30.

4.4 Implementation

The proposed VCO is designed to achieve a tuning range of 54.1 to 70.4 GHz by combing the frequency ranges of two cores (54.1-62.52 GHz and 61.37-70.4 GHz) and fabricated in 65 nm CMOS technology. The size of each transistor for cross-coupled cores is chosen to provide negative resistance for oscillation at all process corners while introducing minimum parasitic capacitance. Furthermore, the number and width of transistor fingers are optimized for the highest transistor's maximum oscillation frequency (f_{MAX}).

The 3-D view of the total passive parts for the VCO including the pads is depicted in Fig. 4.8. All parts are modeled in ANSYS-HFSS 3D EM simulator. The varactors are carefully designed to achieve the largest FTR while maintaining a high-Q so that PN is not

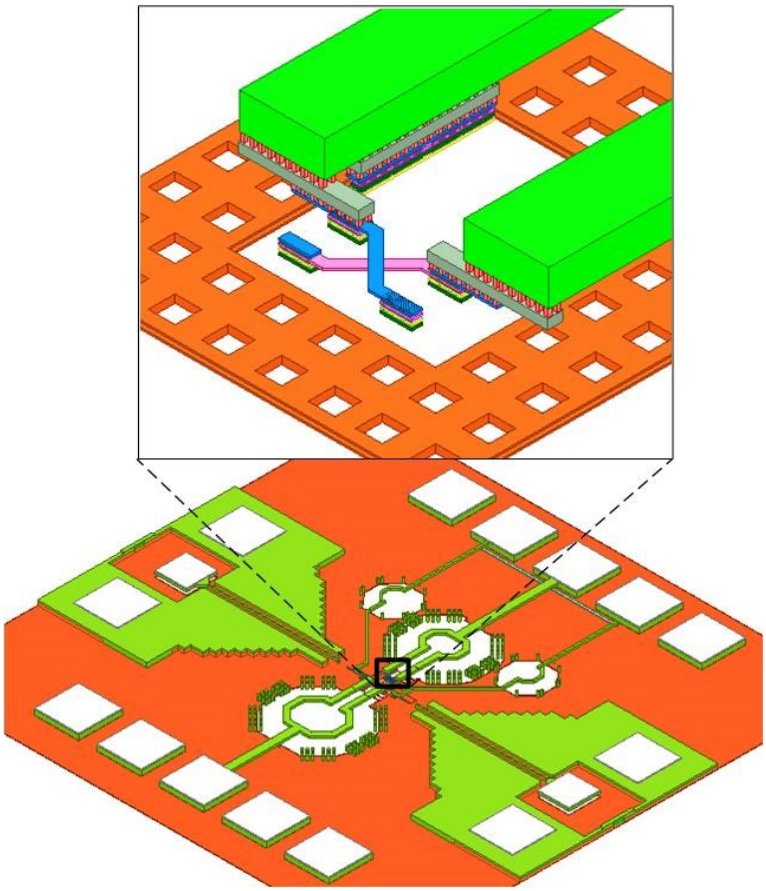


Fig. 4.8. Full 3-D EM model of proposed VCO.

adversely affected. The center-tapped inductors are routed with the top metal (M_9) and the widths are optimized for minimum resistance and highest quality factor.

The buffer transistors are sized such that the parasitic capacitance contributed by the buffer stages are much smaller than the total capacitance of cross-coupled cores. The main output buffer is matched to the output pad to deliver the maximum power at the output port. Hence, the conjugate matching network is utilized via an inductor connected to VDD, a metal-insulator-metal (MIM) capacitor which is for dc blocking, and a 50 ohms Grounded Coplanar Waveguide (GCPW) line where the line is realized with top metal as the signal paths and two bottom metal layers as the ground plane as shown in Fig. 4.9, where “G” is the distance between signal and ground, “W” is width of signal, “H” is the thickness of dielectric which is SiO2 in CMOS technology.

The 50×50 μm^2 output pad is designed using two top layers and it is isolated from lossy silicon substrate with a polysilicon layer. The measured capacitance and Q for the signal pad at 70 GHz are around 21 fF and 20, respectively.

4.5 Experimental Results

Fig. 4.10 shows the chip microphotograph of the fabricated VCO in 65 nm CMOS process where Vsw1 and Vsw2 are controlling switches 1 (Sw1) and 2 (Sw2), Vt1 and Vt2 are the control voltages for varactors of LFB and HFB cores, respectively. The VCO occupies a core area of 100×395 μm^2. The VCO is measured using an on-chip probe station, GSG probes, extended mixers and spectrum analyzer in a measurement setup shown in Fig. 4.11. The chip is mounted on a PCB (on-board packaging) and dc pads are connected by bond wires to the traces on PCB terminated to pin headers. A DC source with 16 independent channels is used for biasing, switching cores, and controlling varactors. VDD voltage is fixed to 1 V and varactor voltage is variable to sweep the frequency. The output signal is measured by R&S FSW signal and spectrum analyzer. Total loss path between chip and spectrum analyzer (cables, adaptor and mixer) is estimated in about4dB which is added to the measured output power in power meter. In PN measurement, digital monitors of the voltages sources are turned off to minimize the contribution of external noises from VDD.

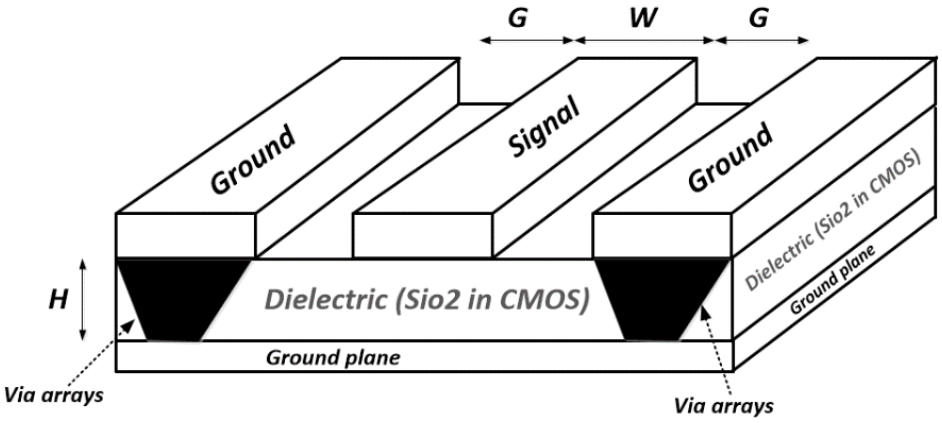


Fig. 4.9. Grounded coplanar waveguide (GCPW).

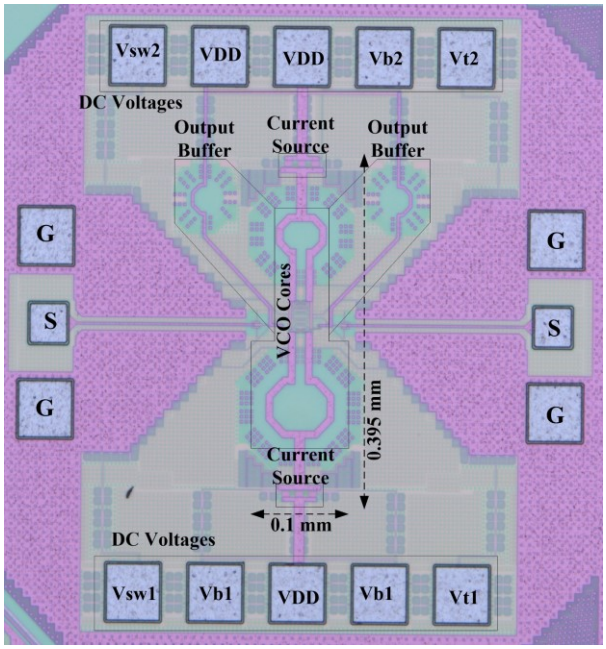


Fig. 4.10. Chip microphotograph of proposed VCO.

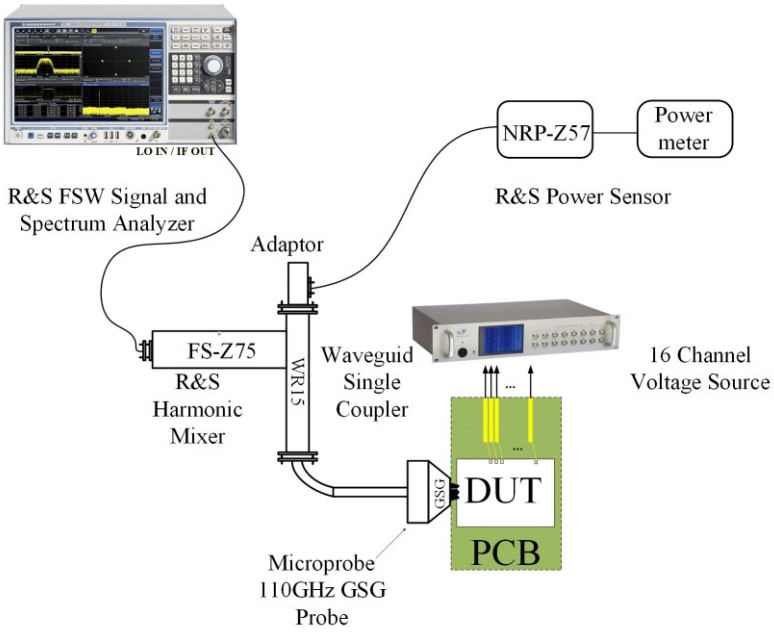
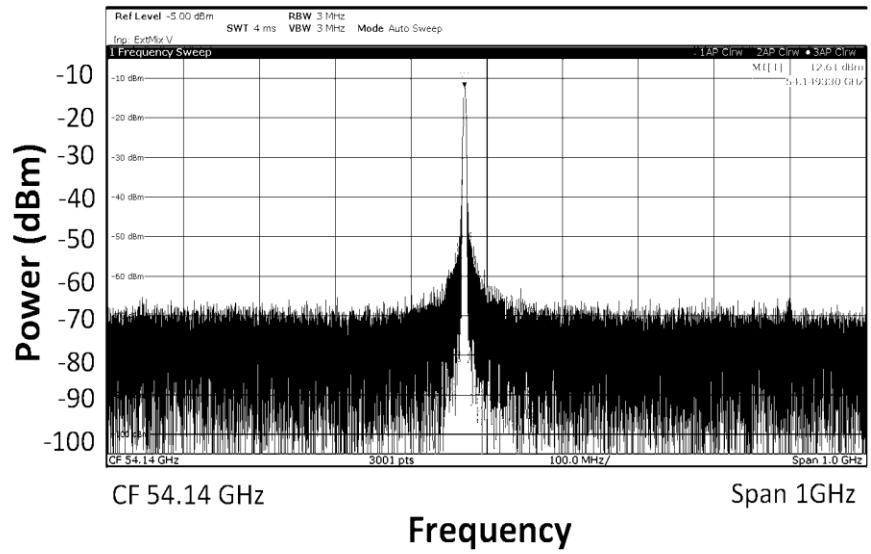
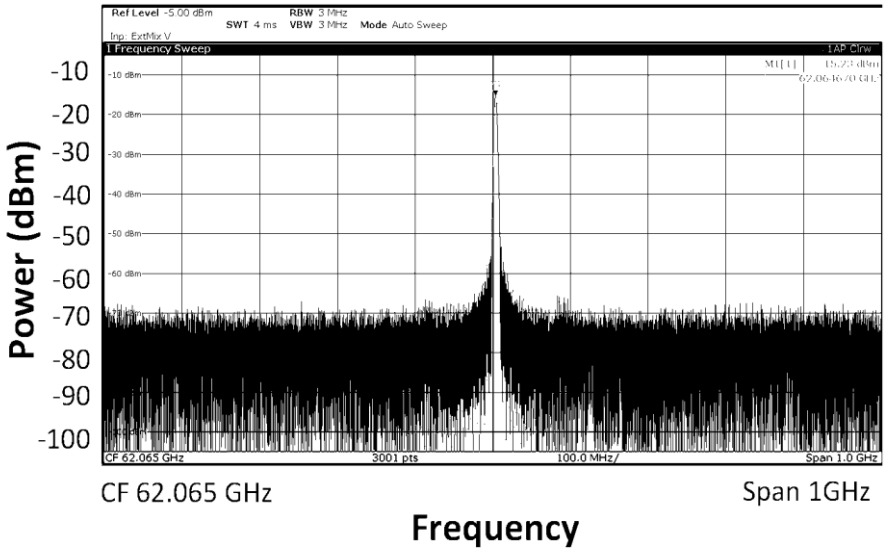


Fig. 4.11. Measurement setup.

Fig. 4.12 shows the measured spectrum for the LFB and HFB where the spectrum analyzer's resolution bandwidth is 3MHz and measured frequencies are 54.1 and 62.5 GHz, respectively.



(a)



(b)

Fig. 4.12. Measured spectrum for the minimum frequency of (a) low-band and (b) high-band.

The measured frequency tuning range as functions of the varactor's tuning voltage is depicted in Fig. 4.13 that shows the LFB and HFB are from 54.1 to 62.5 GHz and 61.37 to 70.4 GHz, respectively. Experimental phase noise results for both modes are plotted in Fig. 4.14 which the corresponding results for 54.2, 62.5 and 70.4 GHz are -107.2, -116.3 and -115.4 dBc/Hz at 10 MHz, respectively.

The power consumption is 11.2 mW for LFB where the first VCO and added buffer are turned-on, and 7.4 mW for HFB. Fig. 4.15 depicts the experimental results for PN and output power versus frequency. The measured K_{VCO} for the proposed circuit is shown in Fig. 4.16, where the maximum value is about 10.

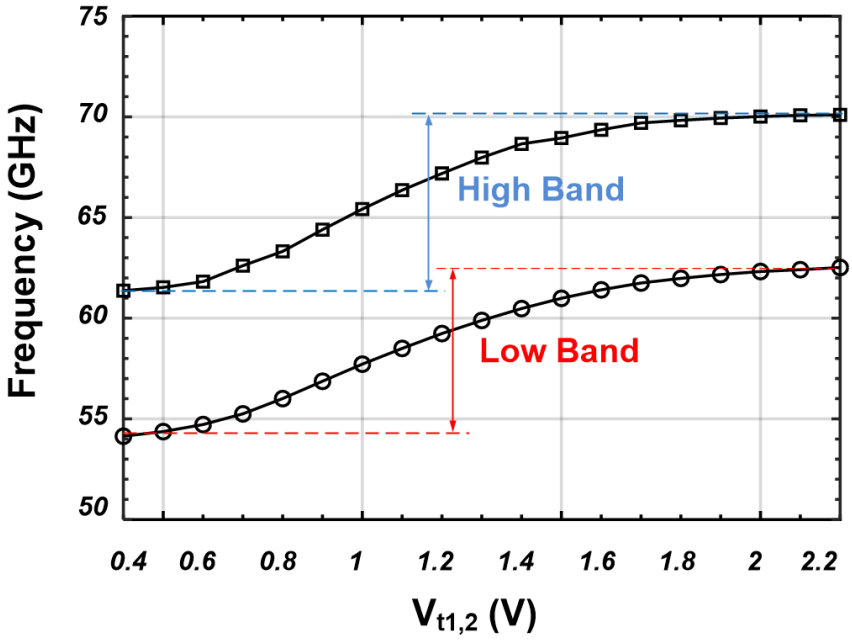
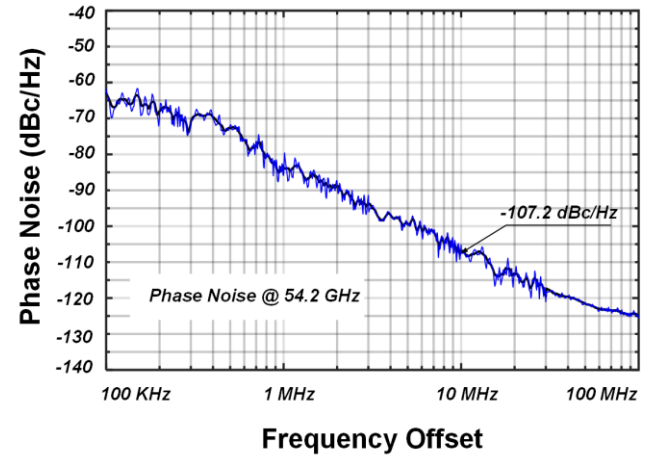
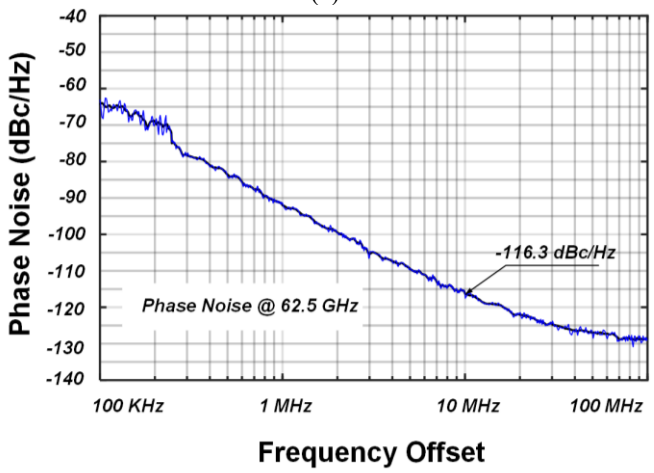


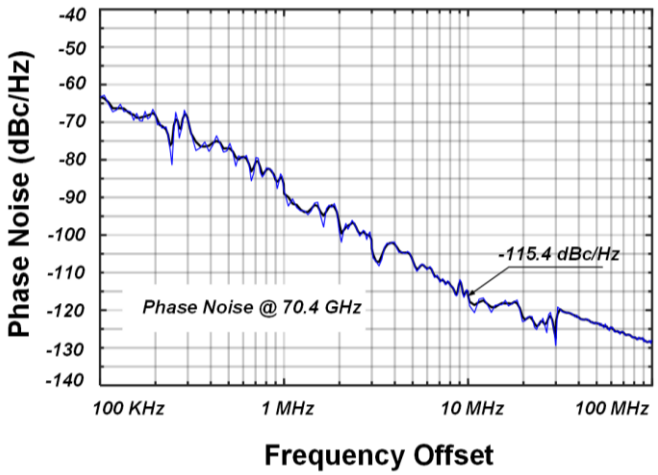
Fig. 4.13. Measured oscillation frequency of proposed VCO.



(a)



(b)



(c)

Fig. 4.14. Measured phase noise curve for (a) 54.1-GHz carrier, (b) 62.5-GHz carrier, (c) 70.4-GHz carrier.

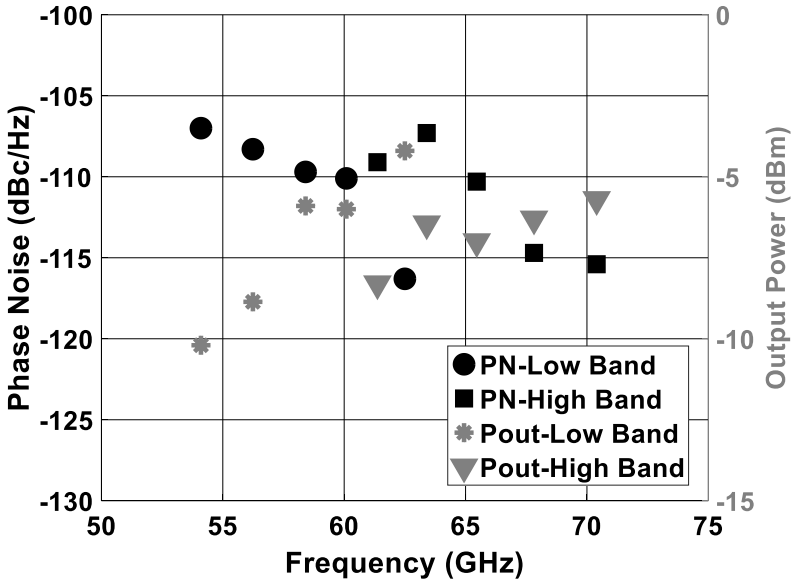


Fig. 4.15. Measured phase noise at 10 MHz offset frequency and output power for full frequency range.

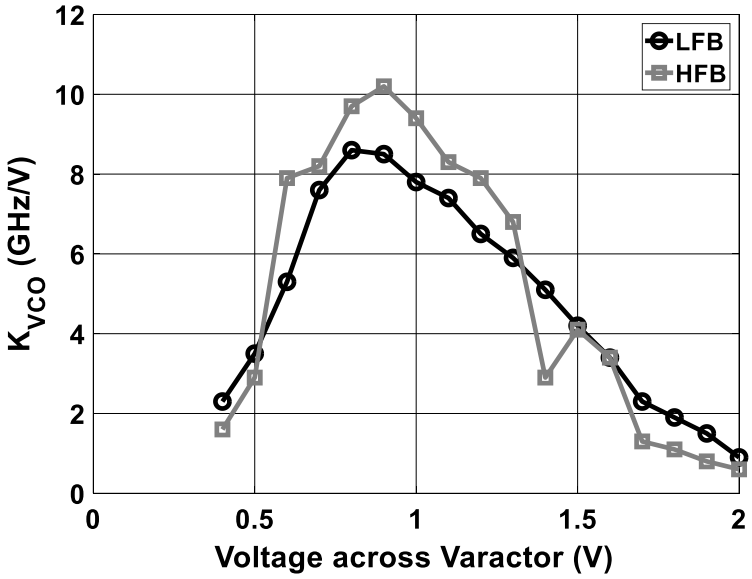


Fig. 4.16. Measured K_{VCO} versus $V_{t1\text{-}2}$.

Table 4-1 summarizes and compares the experimental performance of the proposed wide tuning range VCO with the recently reported state-of-art mm-wave VCOs where f_0 is the oscillation frequency, f_m is the frequency offset from the carrier, PN is the phase noise at f_m, TR is the frequency tuning range in percent, P_{DC} is the dc power consumption expressed in mW.

The proposed VCO achieves the highest $\mathrm{FOM_T}$ (3-9) compared to most of the state-of-art works in Table I except for [62] that reports a $\mathrm{FOM_T}$ 0.34 dB higher than this work because it has a 15% higher FTR than our VCO. However, [62] shows FOM 3.5 dB lower than the demonstrated VCO.

In FOM (3-8) comparison column, only [3] shows a maximum FOM 0.9 dB better than the maximum FOM of the proposed circuit while its minimum FOM is 10.1 dB lower than minimum FOM of our design. Besides, [3] reports a $\mathrm{FOM_T}$ 4.46 dB lower than that reported for this work.

4.6 Conclusion

This chapter presents a wide tuning range voltage controlled oscillator with switchable VCO cores for producing high tuning frequency ratio at millimeter waves by combining the tuning range of two cores. By switching the cross-coupled cores on and off modes, the circuit operates in two different bands with an overlap for continuous tuning range. As opposed to the coupled multicore VCOs, the proposed structure does not require any coupled inductor or transformer achieving a PN performance similar to single-core VCO utilizing standalone inductors.

Reusing the inductors of the external core as the buffer of the inductors, the proposed structure avoids using a bulky passive combiner to combine the output power of the cores. Implemented in 65 nm bulk CMOS, the proposed VCO achieves a measured wide tuning range of 26.2% from 54.1 to 70.4 GHz while consuming 7.4-11.2 mA current from 1.0-V power supply. The peak measured phase noise at 10-MHz offset is -116.3 dBc/Hz, and the corresponding $\mathrm{FOM_T}$ varies from -180.96 to -191.86 dB. The VCO core area is only $0.1\times0.395\ \mu m^2$.

Table 4.1. Performance Summary and Comparisons.

Ref.	**Process**	**Center Frequency (GHz)**	**Tuning Range (%)**	**P_{DC} (mW)**	**Output power (dBm)**	**Phase Noise (dBc/Hz)**	**FOM_T (dBc/Hz)**	**FOM (dBc/Hz)**	**Chip Area (mm^2)**
This work	**65nm CMOS**	**62.25**	**26.2**	**7.4-11.2**	**-10.2 to -4.2**	**-107.2 to -116.3 @10MHz**	**-180.96 to -191.86**	**-172.6 to -183.5**	**0.0395**
[3] TCAS-I 2013	90nm CMOS	56.75	16.07	8.7	-10.5 to -4	-97 to -118 @10MHz	-166.8 to -187.4	-162.7 to -184.3	0.1
[5] TCAS-I 2014	65nm CMOS	61	14.2	6	-30 to -20	-105.9 to -108.3 @10MHZ	-176.9 to -179.3	-173.8 to -176.2	0.031
[11] TMTT 2016	65nm CMOS	59.3	39	8.9 – 10.4	NA	-101.7 t0 -113.4@ 10MHz	-179.6 to -190.6	-167.8 to -179	0.074
[24] JSSC 2015	65nm CMOS	106.7	39.4	30-45	-23 to -15	-101.6 to -108.2@10MHz\	-179.3 to -185.9	-165.7 to -174	0.55[2]
[62] JSSC 2013	65nm CMOS	73.8	41.1	8.4-10.8	-25 to -20	-104 to -112. 4 @10MHz	-184.2 to -192.2	-172 to -180	0.03[1]
[61]TCAS-I 2015	0.18um BiCMOS	60.85	17.2	11.2-19.1	-28.9 to -32.7	-87.5 to -93.5@1MHz	-177.4 to -181	-170.4 to -176.2	0.347[2]
[74] TCAS-I 2016	65nm CMOS	70.2	22.3	7.7-8.8	NA to 1	-105.8 to -112 @10MHz	-180.3 to -187.4	-173.3 to -180.4	0.012
[75] TCAS-I 2017	65nm CMOS	59	14.2	18	NA	-90.7 to -94.1 @1MHz	-176.6 to -180	-169 to -172.4	0.1
[76] TMTT 2015	65nm CMOS	81.5	14	33	-1.5 to -0.5	-90 to -97.3 @1MHz	-176 to -182.6	-173 to -179.7	0.0462

[1] Excluding current source

[2] Full chip size

Chapter 5

A 65-81 GHz CMOS VCO using High-Q Dual-Mode Transformer-Based Inductors

5.1 Proposed Transformer-Based High-Q Variable Inductor

In this section, first, the existing variable/switched inductors based on loaded transformer for high FTR mm-wave VCOs will be reviewed to understand why these inductors cannot have high Q-factors and do not allow to achieve good phase noise performance. Then, a new Transformer-Based VID structure will be presented that can produce a high-Q VID utilizing a high-Q load along with the switches that do not introduce additional losses.

For a conventional cross-coupled LC-VCO [77], the oscillation frequency is given as

$$f_{OSC} = \frac{1}{2\pi\sqrt{L(C_{Fix} + C_{Var})}} \qquad (5-1)$$

where L, C_{Fix} and C_{Var} are inductance, fixed parasitic capacitance, and variable capacitance of the LC-tank, respectively. At mm-wave frequencies, large transistors are needed to produce *-2/g_m* resistance required for compensating the losses of the LC-tank resulting in a large C_{Fix}. On the other hand, the size of C_{Var} should be small to achieve a high Q (Q_{var}) at mm-wave frequencies.

When Q of the varactor reduces to single digits, the Q-factor of the LC-tank (Q_{tank}) is determined by Q_{var} as given by

$$\frac{1}{Q_{tank}} = \frac{1}{Q_{var}} + \frac{1}{Q_{ind}} \approx \frac{1}{Q_{var}}, \qquad (5-2)$$

where

$$Q_{var} = \frac{1}{\omega C R_S}. \qquad (5-3)$$

In the above equation, R_S models the losses of the varactor as a series resistor which is mostly determined by the sheet resistance of n-well for AMOS varactors [47]. Because of low Q of large varactors, the design of mm-wave VCO with wide tuning range and good phase noise performance and utilizing only varactors is not possible. One way to keep the LC tanks Q high enough to achieve a good PN performance is to use smaller varactor sizes along with switched/variable inductor to obtain the desired tuning range. Hence, different VIDs are proposed as a solution for wide FTR VCO design without adding any parasitic capacitance to the LC-tank [3]-[6],[62]-[66],[84].

5.2 Operation Principle and Limitations of Conventional Loaded Transformer-Based VIDs

Fig. 5.1 depicts the schematic of a loaded transformer-based VID where L_1, L_2, C_L, R_L, and k are the primary and secondary coil inductances, variable capacitor and load resistor, and coupling factor of the coils, respectively. If the transformer is assumed to be ideal, the input impedance can be calculated as

$$\mathrm{Z}_{in} = \mathrm{L}_1 s - \frac{M^2 s^2}{Z_L + \mathrm{L}_2 s}, \qquad (5-4)$$

where M ($M = k\sqrt{L_1 L_2}$) is the mutual inductance and Z_L is

$$\mathrm{Z}_L = \frac{R_L}{1 + j\omega C_L R_L}, \qquad (5-5)$$

The conventional variable loads realized in different ways such as a variable capacitor (varactor) [56], variable capacitors/resistors [3] and switched inductors [84], all of the suffer from low-quality factor less than 15 at around 60 GHz as will be discussed later in this section. Separating the real and imaginary part of *Zin*, the equivalent inductance (L_{eq}) and series resistance (R_{eq}) of the loaded transformer shown in Fig. 5.1 can be derived as

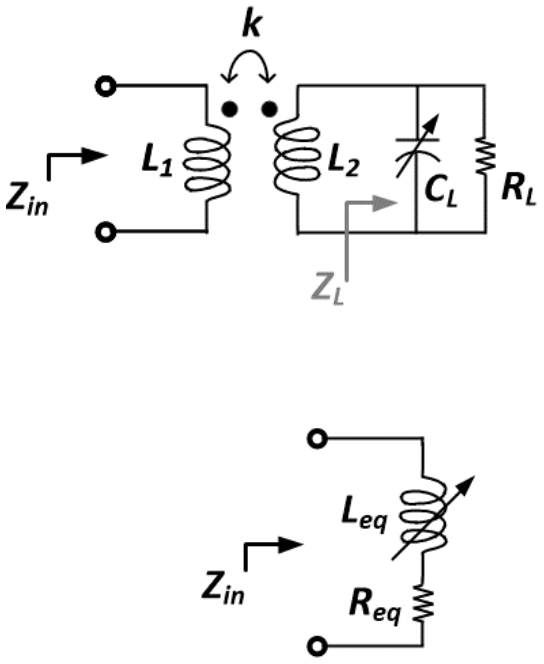


Fig. 5.1. Concept of conventional transformer-based VIDs.

$$L_{eq} = L_1 \frac{C_L{}^2 L_2{}^2 R_L{}^2 (1-k^2)\omega^4 + [(1-k^2)L_2 + C_L R_L{}^2 (2-k^2)]L_2\omega^2 + R_L{}^2}{C_L{}^2 L_2{}^2 R_L{}^2 \omega^4 + \left(L_2{}^2 - 2C_L L_2 R_L{}^2\right)\omega^2 + R_L{}^2} \quad (5-6)$$

and

$$R_{eq} = \frac{L_1 L_2 k^2 R_L \omega^2}{(C_L{}^2 R_L{}^2 \omega^2 + 1)L_2{}^2 \omega^2 - R_L{}^2 (1 - 2C_L L_2 \omega^2)}. \quad (5-7)$$

According to (5-6) and (5-7), the equivalent Q-factor can be calculated as

$$Q_{eq} = \frac{L_{eq}\omega}{R_{eq}} = \frac{L_2{}^2 \omega^2 (1 + C_L{}^2 R_L{}^2 \omega^2)(1-k^2) - L_2 C_L R_L{}^2 (2-k^2)\omega^2 + R_L{}^2}{R_L L_2{}^2 k^2 \omega}, \quad (5-8)$$

Two main types of existing loaded transformer-based VIDs, varactor-loaded and switch-loaded, are illustrated in Fig. 5.2(a) and (b), respectively. The simulated Q and inductance of a capacitor-loaded (CL) and open-load (OL) transformer-based VID is shown in Fig. 5.3 where it can be seen that the Q of a CL-VID is directly related to the Q of the capacitor. Note that the transformer is modeled and simulated in ANSYS HFSS 3D EM simulator and the loss from the transformer is included in the simulations. As an example, a 40fF capacitor with a Q equal to 50 results in Q of 25 for the VID at 65 GHz, while that drops to around 15 for the capacitor with Q of 10. As discussed earlier, varactors suffer from low-Q in mm-wave frequencies, and it is not a good choice for construction of high-Q VIDs.

However, the tunability of the load is essential to provide the variable inductance needed for tuning of the VCO. Instead of using low-Q varactors, the load of VID can be constructed using the switched capacitor consisting of a high Q fixed capacitor and a switch. Fig. 5.2(b) shows the switch-loaded (SL) transformer-based VID, where the input inductance varies when the switch is turned ON and OFF. Furthermore, the discrete value of VID can be increased utilizing multiple secondary coils and loads [6].

Fig. 5.4 shows the simulated inductance and Q of the SL-VID loaded with different size of switches in ON and OFF modes. Regardless of the size, non-ideal switch in ON mode, degrades Q of the VID from 20 to around 7 at 60 GHz. Hence, finding an ideal switching

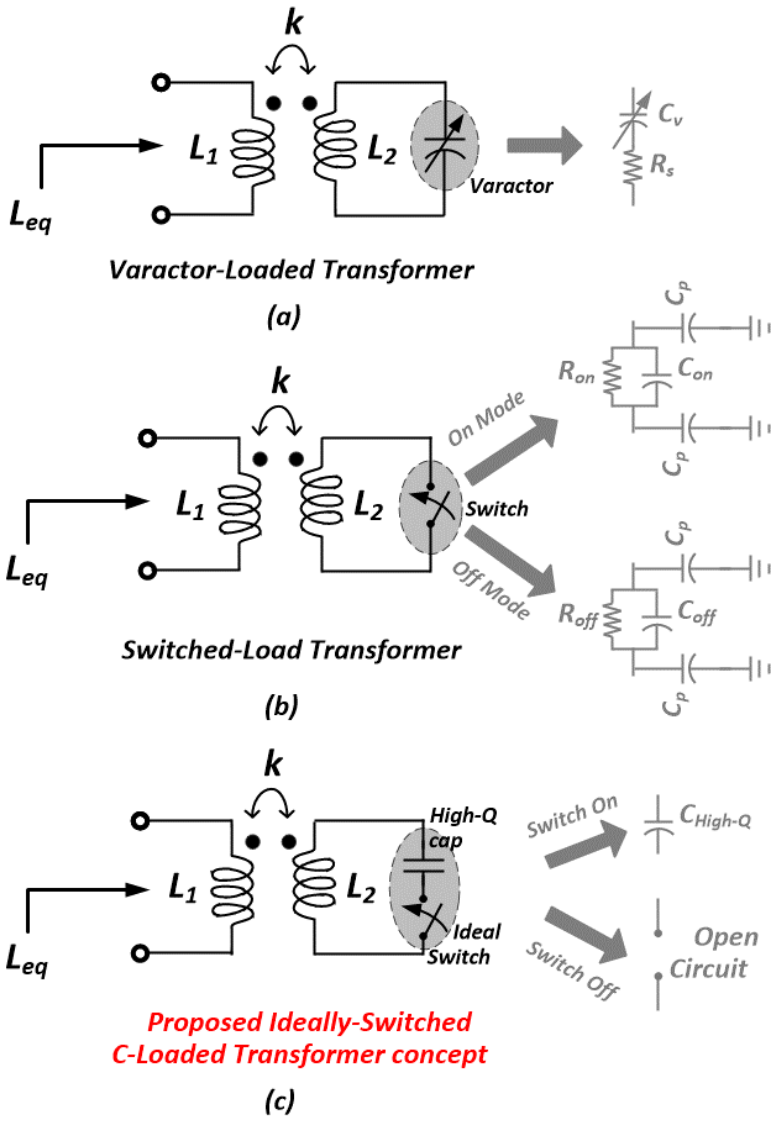


Fig. 5.2. Traditional (a) varactor-loaded, (b) switch-load, and (c) proposed ideally-switched *C*-loaded transformer-based VID.

method could increase Q of the VID to around 20. Furthermore, it is shown that there is a tradeoff between Q and self-resonance frequency of the VID with respect to the switch sizing in ON state.

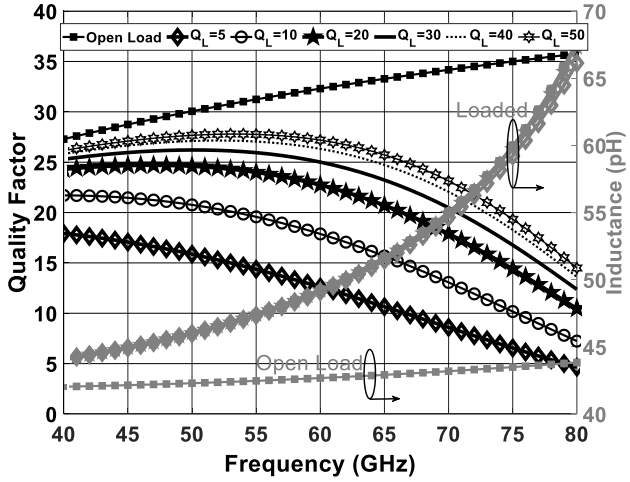


Fig. 5.3. Simulated: Q and inductance of transformer-based VID loaded by a 40fF capacitor in different quality factors and opened load.

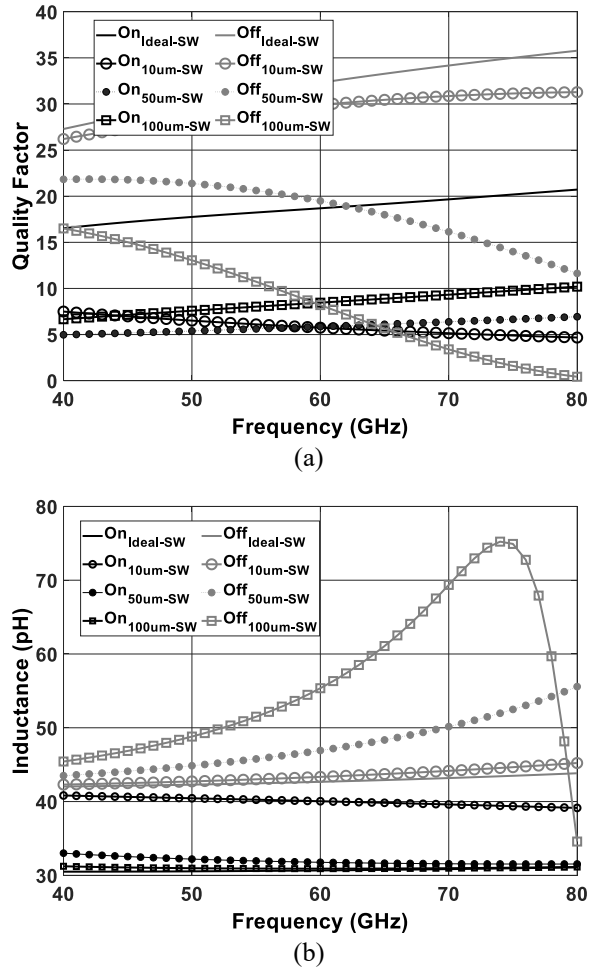


Fig. 5.4. Simulated: (a) Q and inductance of transformer-based VID loaded by a 40fF capacitor in different quality factors and opened load.

5.3 Principle of Proposed High-Q Switched Inductor Based on Loaded Transformer

The general idea and concept of the proposed technique can be explained by Fig. 5.2(c) where a high-Q capacitor at the load of the transformer has Q of about 50 at 65 GHz. When the switch is turned OFF and ON, the equivalent input inductances are around 42 pH and 52 pH with the Q of higher than 30 and 25 at 65 GHz, respectively (Fig. 5.4). Thus, a dual-inductance VID with minimum Q of higher than 20 can be achieved with an ideal switching method, any added loss due to the on-resistance of the switch can decrease the Q to around 10.

As illustrated in Fig. 5.5(a) and (b), even-mode, and odd-mode techniques are utilized to realize the concept proposed in Fig. 5.2(c). In the even-mode operation, the voltages across the capacitor are in phase and there is no current flowing through the capacitor (Fig. 5.5(a)). Hence, the equivalent circuit can be simplified to two similar transformers with open-loads. Based on (4), if $\mathrm{Z}_L = \infty$, the equivalent inductances seen at the terminals will be equal to

$$L_{eq} = L_1, \qquad (5-9)$$

and Q of the equivalent inductors will be same as of a standalone inductor (e.g. higher than 30) resulting in high Q of LC-tank and better PN performance.

In the odd mode, the voltages across the capacitor *C* are 180 degrees out of phase resulting in a virtual ground in the center of the capacitor. The equivalent circuit, in this case, is two separate transformers each loaded with 2*C* as shown in Fig. 5.5(b) and the equivalent input inductances can be calculated via equation (5-6) and using the Q of capacitors which is higher than that of existing transformer-based inductors. Hence, using the described switching method, two high-Q inductors can be realized for a dual-band VCO design.

By choosing proper center frequencies for each VCO and sufficient frequency overlap, a wide FTR mm-wave VCO can be designed which provides almost 90% (10% for overlap frequency range) higher tuning range while keeping PN performance almost same as a

VCO designed by standalone inductors. In the next section, the design and implementation considerations will be discussed.

5.4 Circuit Design

5.4.1 LC-tank Implementation

As discussed before, the varactors exhibit low Q-factor at mm-wave frequencies. The fixed metal-insulator-metal (MIM) and metal-oxide-metal (MOM) capacitors that are available in standard CMOS processes have higher Q at these frequencies. However, the parasitic capacitance of the node connected to the bottom plate of MIM capacitor is higher than that of the node connected to the top plate. MOM capacitors are chosen in our design because of their high-quality factor and symmetrical behavior as they show equal parasitic capacitances on both sides, which is needed for the proper even/odd mode operation. Fig. 5.6 shows the designed MOM capacitor where Metal 4, 5, 6 and 7 are employed as parallel conductors with a minimum allowed lateral space of 0.2 μm, a length of 4 μm, and a width of 7 μm to produce a high density and high-Q capacitor structure.

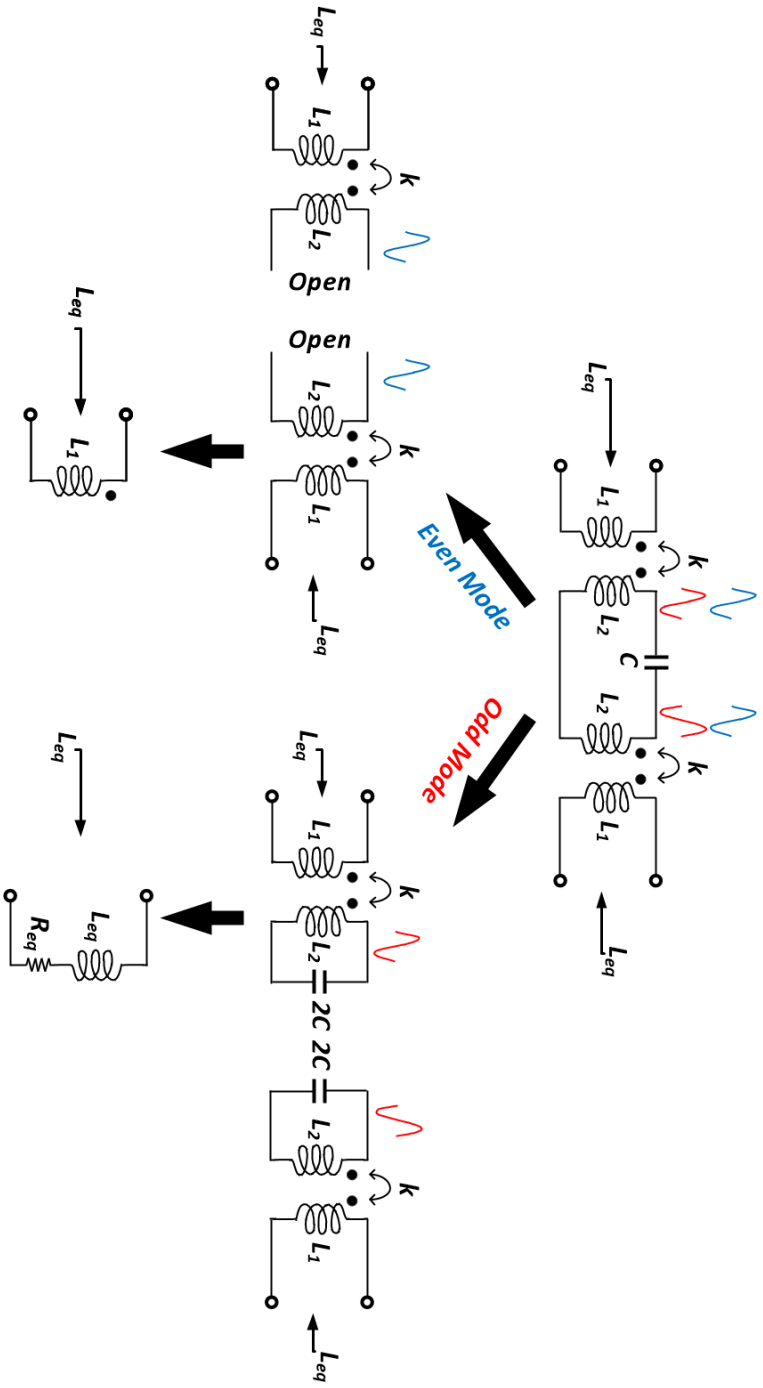


Fig. 5.5. Illustration of equivalent inductor (a) even mode, (b) odd mode.

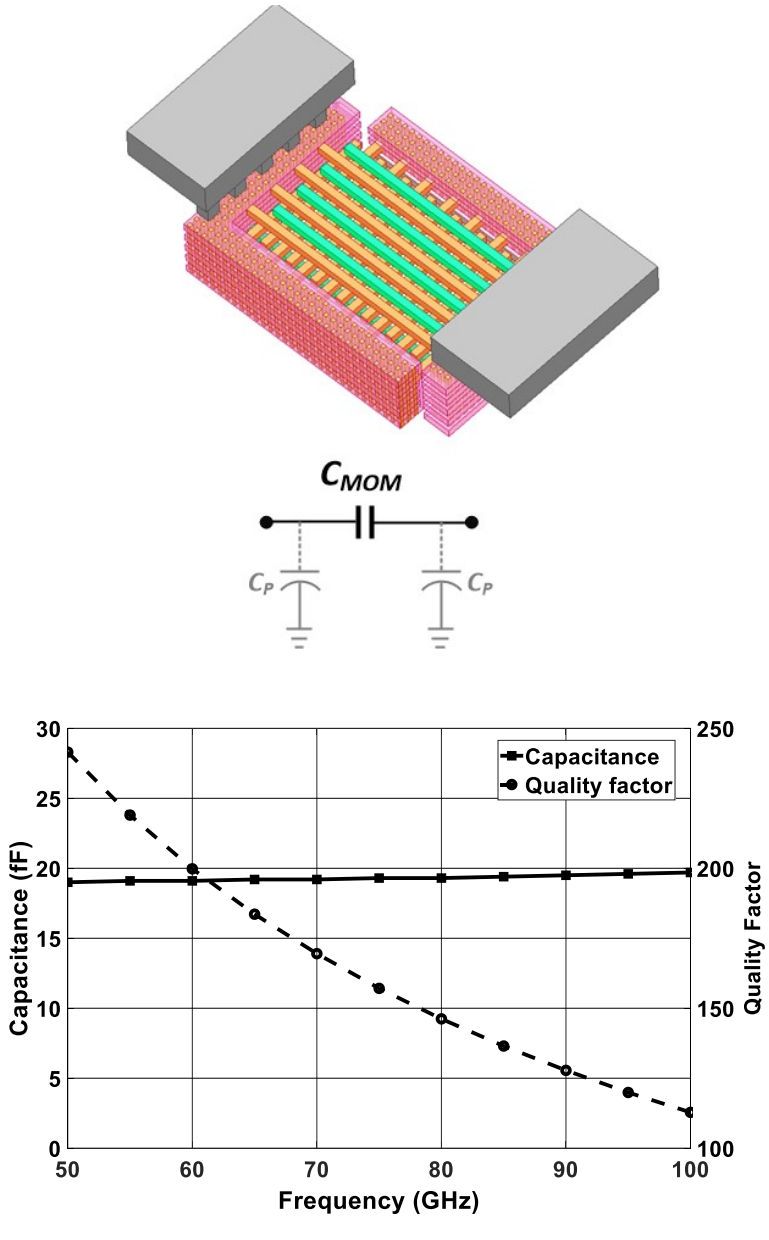
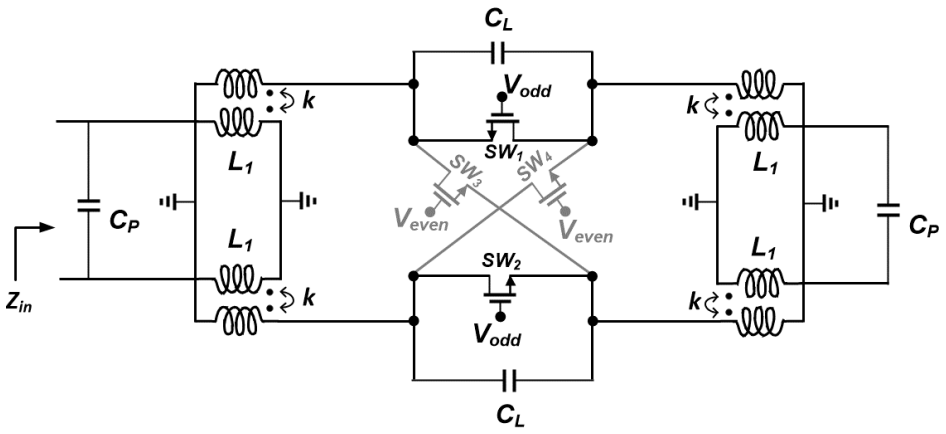
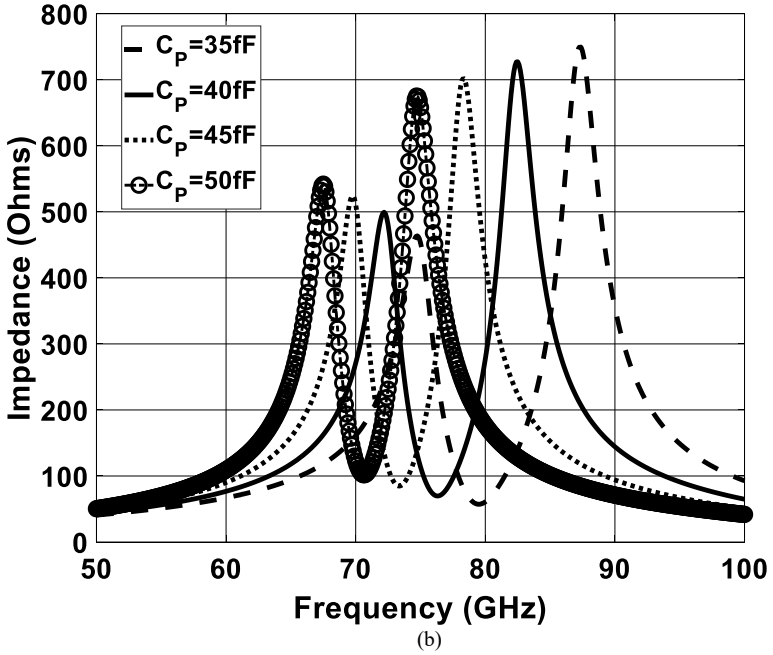


Fig. 5.6. (a) 3D view of modeled MOM capacitor in ANSYS HFSS simulator and its electrical view, (b) simulated capacitance and Q versus frequency.

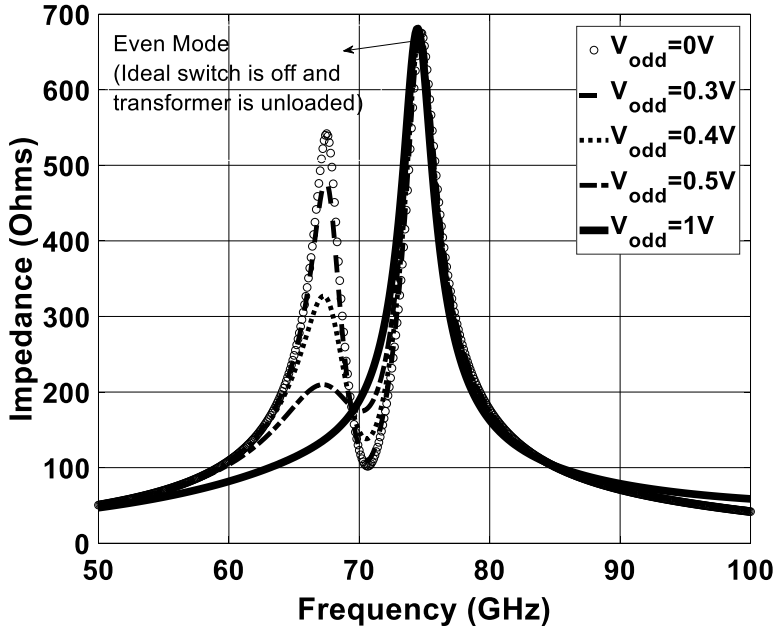


(a)

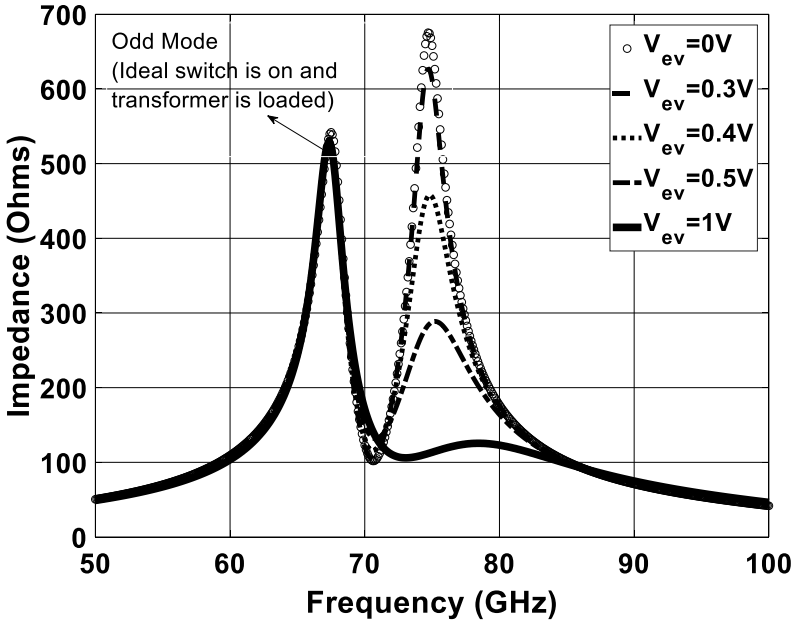


(b)

Fig. 5.7. Electrically coupled transformers and ustilized mode switching technique (b) corresponding input impedance when all of the switches are off.



(a)



(b)

Fig. 5.8. Input impedance response versus frequency based on voltage change on switches (a) even mode suppression, (b) odd mode suppression.

The switching method proposed in [82] is utilized in the design to realize the mode switching as shown in Fig. 5.7(a) where four switches (SW_1, SW_2, SW_3, SW_4) are employed to determine signal modes across the load capacitor (C_L=20 fF). As depicted in Fig. 5.7(b), when all switches are OFF (V_{even}=V_{odd}=0V), the input impedance shows two peaks. The resonance curves are sharp, which means that the phase shift between the signals located near resonance points is close to 180 degrees. This allows for the operation at one resonant point in even mode operation, and for operation at the other resonant point in odd mode operation.

The location of resonance points can be tuned using different values of parasitic capacitance C_P at the input. For example, for the designed transformer and MOM capacitor, C_P variation between 50fF and 35fF leads to a frequency tuning range of 66 to 87 GHz, respectively. As illustrated in Fig. 5.8(a), for even operation mode, increasing V_{odd} from 0 to 1 results in suppressing the odd mode impedance without changing the even mode impedance amplitude. Hence, the oscillation frequency is determined by existing high impedance which requires lower energy for oscillation and is given by

$$\mathrm{f}_{OSC,even} = \frac{1}{2\pi\sqrt{L_1 C_P}}. \qquad (5-10)$$

where C_P is fixed parasitic capacitances including cross-coupled transistors and minimum capacitance of varactor ($C_P = C_{P,fix} + C_{Pmin,var}$). Conversely, increasing V_{even} from 0 to 1V, suppresses the even mode impedance (Fig. 5.8(b)) leading to odd mode operation frequency of

$$\mathrm{f}_{OSC,odd} = \frac{1}{2\pi\sqrt{L_{eq} C_P}}. \qquad (5-11)$$

From (5-10) and (5-11), in perspective of dual-mode operation, the proposed circuit does not add any parasitic capacitance decreasing the FTR (the work in [82] adds extra capacitances to the LC-tank limiting the tuning range). Assuming $C_P = 80\mathrm{fF}$, $L_1 = 40\mathrm{pH}$ and $C_{var,max}/C_{var,min} = 60\mathrm{fF}/20\mathrm{fF}$, with mode switching in the proposed method, the equivalent inductance can be switched between $L_{eq} = 40 - 60\mathrm{pH}$, theoretically FTR of 40% is achievable (f_{LFB} =59.3-72.6 and $f_{HFB} = 72.6 - 88.9$ GHz). However, with the

same varactors and $C_L = 20$fF, the circuit proposed in [82] can provide maximum FTR of 34% (f_{LFB} =62.9-72.6 and $f_{HFB} = 72.6 - 88.9$ GHz) which is 7% lower than FTR of our presented circuit. Compared to [83] which employs mode-switched inductors to keep high FTR, our circuits occupies almost half of the corresponding chip area.

5.4.2 Circuit Implementation

Fig. 5.9 shows the proposed VCO which is designed to cover a frequency range of 64.88 -81.6 GHz by combining odd and even mode operations (64.88-73.2 GHz and 71.32-81.6 GHz). The VCO is implemented in standard 65 nm CMOS technology. The transistors for the cross-coupled cores have the size of 10 μm/60 nm to provide the needed negative resistance for startup oscillation frequency with optimized size and number of fingers to achieve the maximum oscillation frequency (f_{MAX}) over the all process corners.

The size of varactors are 14 μm/60 nm resulting in $C_{var,max}/C_{var,min} = 2.5$ and maximum Q of 20 at 70 GHz. The size of buffer transistors is 4 μm/60 nm which do not affect FTR of the VCO as their gate-source capacitance (C_{gs}) is much smaller than the total fixed capacitance at the output of the VCO ($4C_{gd} + C_{gs} + C_{db}$). For measurement purpose, one of the main buffers is matched to 50 Ohms by employing an inductor, metal-insulator-metal (MIM) capacitor and a Grounded Coplanar Waveguide (GCPW) line connected to the output pad. Other three buffers are internally terminated to the on-chip 50 Ohm resistors. The transformer has a planar structure and employs the top metal (M9) for main coils realization as shown in Fig. 5.10.

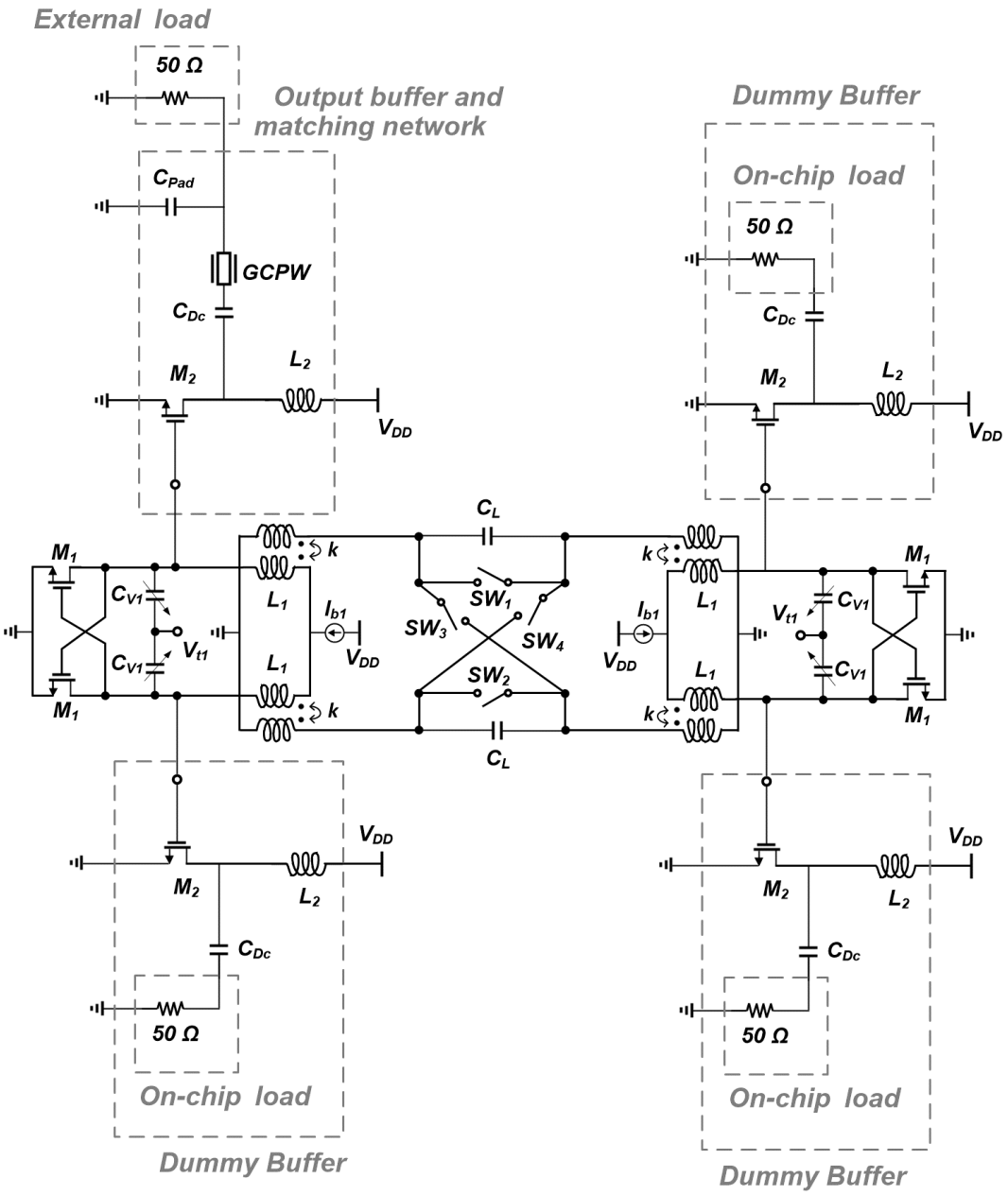


Fig. 5.9. Proposed dual-band VCO.

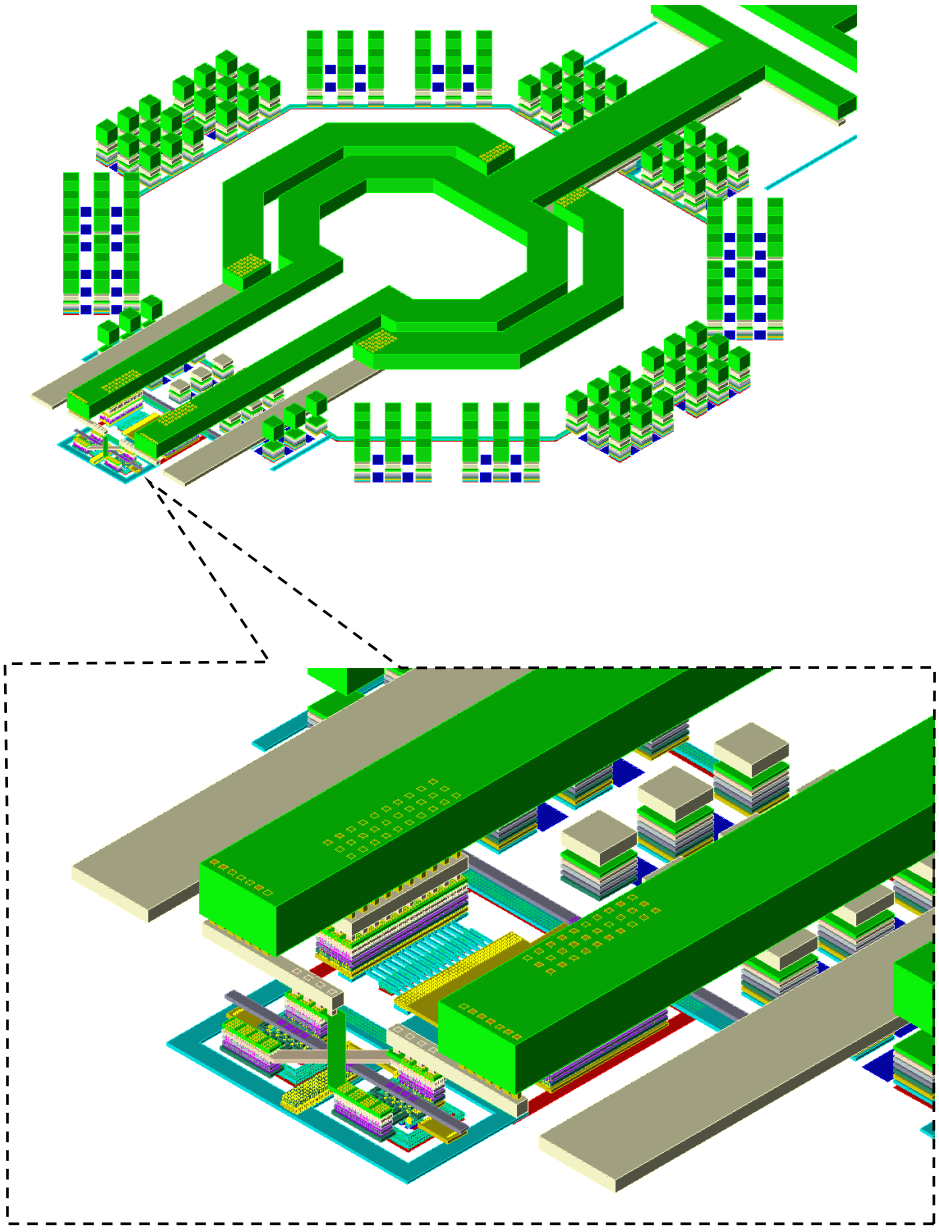


Fig. 5.10. Utilized transformer and cross-coupled part realization in 65-nm CMOS.

5.5 PN Improvement

The phase noise of an LC-tank VCO can be expressed as [48]

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{2kT}{P_S}\left(\frac{\omega_0}{2Q_{tank}\Delta\omega}\right)^2\right] \quad (5-12)$$

where k is the Boltzmann's constant, T is the absolute temperature and P_S is the output signal. Phase noise performance of a VCO would be degraded drastically if the LC-tank quality factor is low ($PN \sim \frac{1}{Q^2}$). From (5-2), if Q of the inductor is high (e.g. more than 30), Q of the tank is determined by Q_{var} in low-Q mode. However, as it is discussed in [77], higher Q of the inductor can improve the LC-tank quality factor leading to better PN performance. By expanding (5-12) to

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{2kT}{P_S}\left(\frac{\omega_0}{2\Delta\omega}\right)^2\right] + 10\log\left[\left(\frac{1}{Q_{tank}}\right)^2\right]. \quad (5\text{-}13)$$

one finds that PN difference for the LC-tanks with the corresponding Qs of $Q_{tank,prop}$ and $Q_{tank,VID,}$ can be expressed as

$$\Delta\mathcal{L}(\Delta\omega) = 10\log\left[\left(\frac{Q_{tank,VID}}{Q_{tank,Prop}}\right)^2\right], \quad (5-14)$$

where

$$Q_{tank,Prop} = \frac{Q_{Ind,1} \times Q_{Var}}{Q_{Ind,1} + Q_{Var}}, \quad (5-15)$$

$$Q_{tank,VID} = \frac{Q_{Ind,2} \times Q_{Var}}{Q_{Ind,2} + Q_{Var}}, \quad (5-16)$$

and $Q_{Ind,Prop}$, $Q_{Ind,VID}$ and Q_{Var} are quality factors of the proposed switched loaded inductor, existing variable/switched inductors and varactors, respectively. Based on the operation mode, the PN improvement can be calculated as below:

In the odd mode, $Q_{Ind,Prop}$ is higher than $Q_{Ind,VID}$ and close to the standalone inductor. Assuming $Q_{Ind,Prop} = 25$, $Q_{Ind,VID} = 10$, PN improvement of 3 to 4.5 dB can be achieved when the Q_{Var} changes from 10 to 20, respectively (Fig. 5.11).

In the even mode, $Q_{Ind,Prop}$ is equal to a standalone inductor and higher than 30 resulting in more PN improvement in comparison to the odd-mode. Hence, the VCO in both modes exhibits better PN performance in comparison to the reported mm-wave VCOs designed with VIDs.

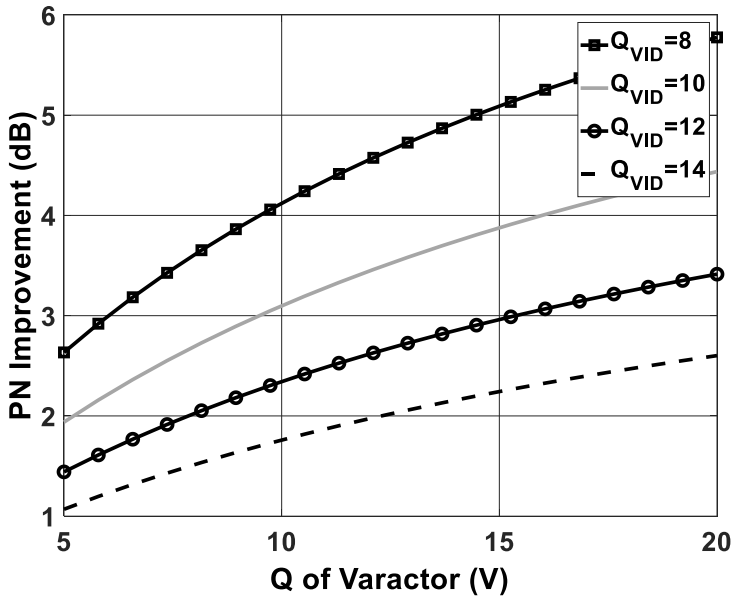


Fig. 5.11. Simulated PN improvement vs Q of varactor and VID when Q of proposed inductor is equal to 25.

5.6 Experimental results

The chip microphotograph of the proposed VCO is shown in Fig. 5.12. The VCO fabricated in 65 nm CMOS process occupies a core area of 146×205 μm^2. The fabricated VCO was measured on-wafer using a Cascade 110 GHz GSG probe and a 1mm 110 GHz cable to connect its output GSG port to R&S FSW85 spectrum analyzer as shown in Fig. 5.13.

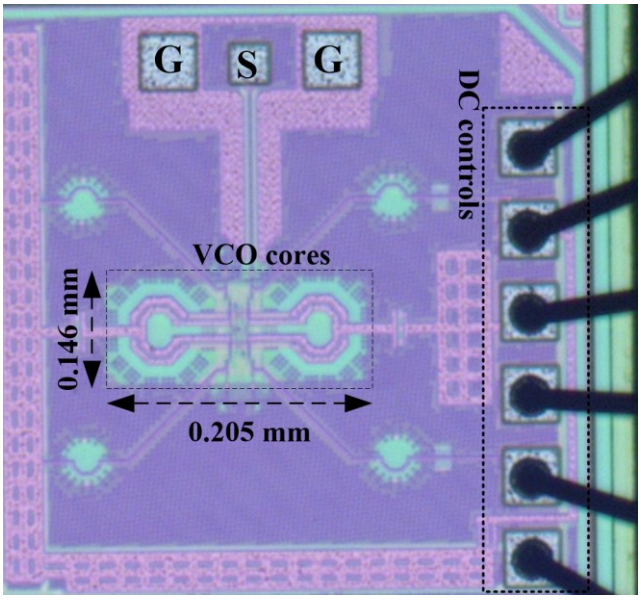


Fig. 5.12. Chip microphotograph of proposed VCO.

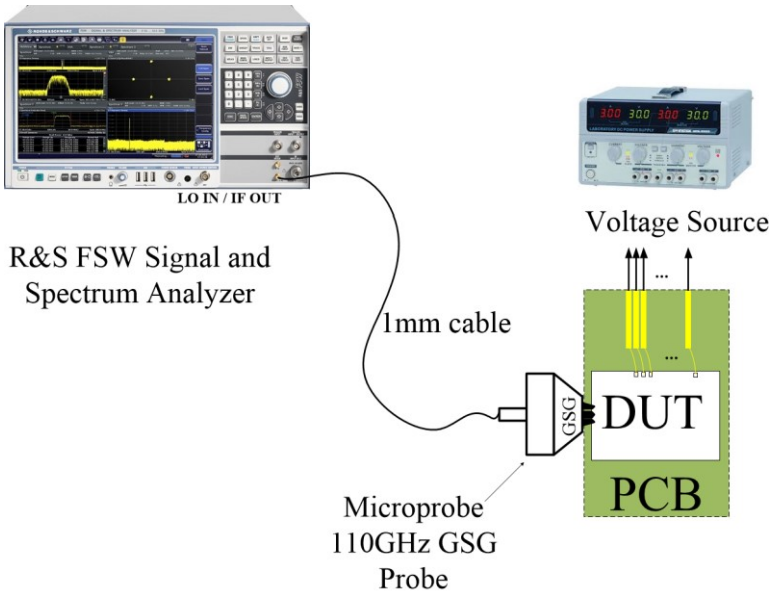
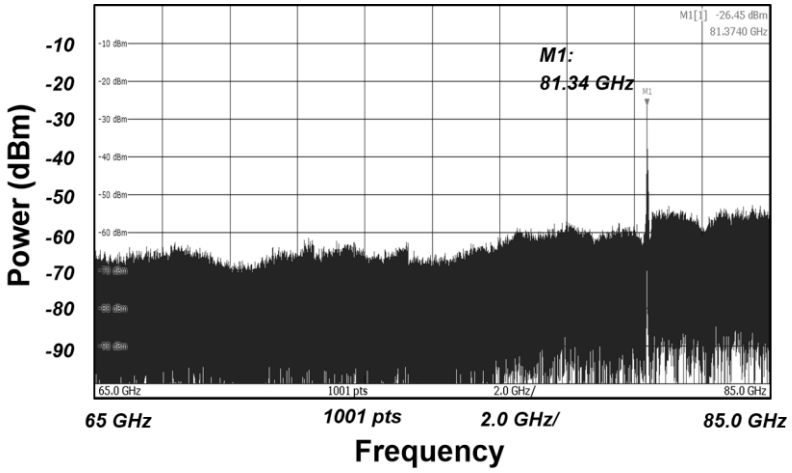
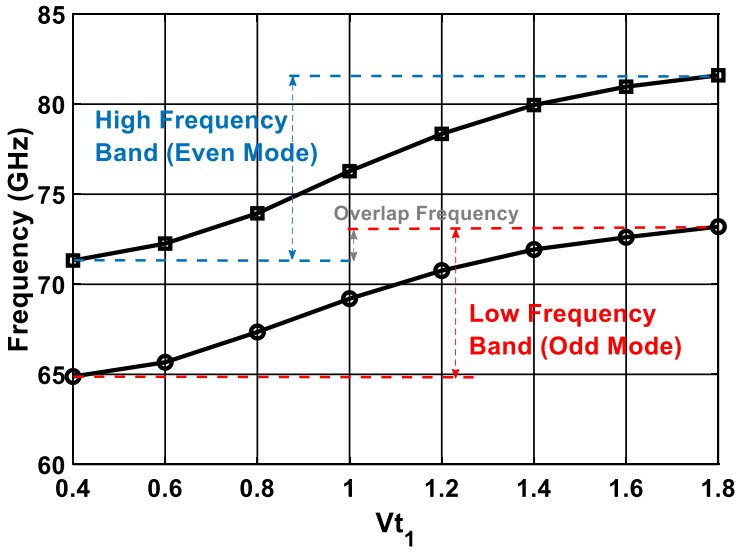


Fig. 5.13. Measurement setup.

Fig. 5.14(a) depicts the measured spectrum at 81.34 GHz and the frequency tuning range versus varactor's tuning voltage is shown in Fig. 5.14(b). The even-mode and odd-mode frequency bands are from 64.88 to 73.2 GHz and 71.37 to 81.6 GHz, respectively.



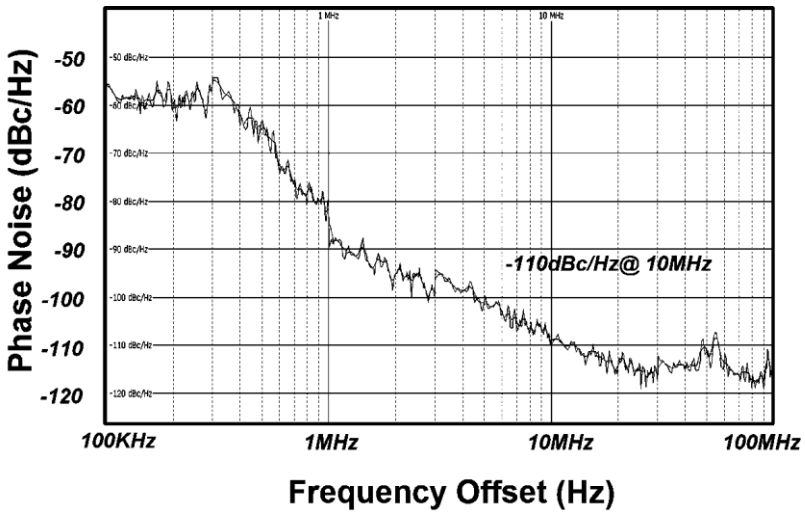
(a)



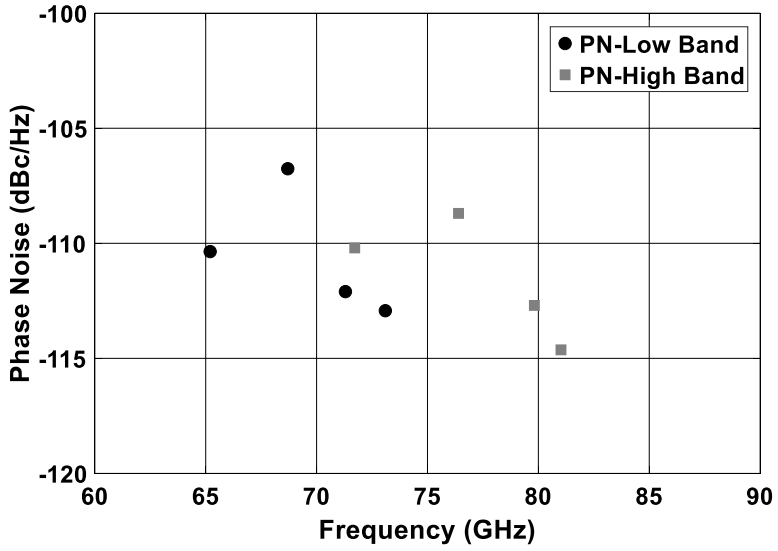
(b)

Fig. 5.14. Measured (a) spectrum at 81.37GHz, (b) frequency tuning range versus varactor's tuning voltage.

Experimental phase noise results for both modes are plotted in Fig. 5.15(a) and (b) where the maximum and minimum measured PN are at 68.7 and 81 GHz corresponding to -106.7 and -114.63 dBc/Hz, respectively. The measured power consumption for each VCO core is 10.2 mW.



(a)



(b)

Fig. 5.15. Measured phase noise at 10 MHz offset frequency (a) 65 GHz, (b) for entire frequency range.

The performance summary of the proposed VCO and recently reported state-of-art mm-wave VCOs are summarized in Table 5-1. The proposed VCO demonstrates as well comparable FOM (3-8) and FOM_T (3-9) figures of merit compared to most of the state-of-art works. Here f_m, f_0, TR% and P_{DC} are the frequency offset from the carrier, oscillation frequency, phase noise at f_m, percentage of FTR and dc power consumption in mW, respectively.

5.7 CONCLUSION

In this chapter, a mm-wave VCO with wide FTR and low PN is presented. By utilizing a high-Q capacitor and a lossless switch structure as the load of the transformer, a high-Q switched inductors are realized to design a dual-mode VCO. The center frequency of each mode is carefully chosen and with sufficient frequency overlap, so that the circuit presents the capability of high FTR along with improved PN performance in comparison to the existing VCO design with transformer-based inductors.

The VCO is implemented in 65nm CMOS technology and exhibits a measured wide FTR of 22.8% from 64.88 to 81.6 GHz. The peak measured PN at 10 MHz offset frequency for even-mode and odd-mode are 114.63 dBc/Hz and 112.93 dBc/Hz, respectively. The VCO cores consume 10.2 mA each from 1 V power supply and occupy 0.146 ×0.205 mm^2 chip area.

Table 5.1. Performance Summary and Comparisons.

Ref.	**Process**	**Center Frequency (GHz)**	**Tuning Range (%)**	**P_{DC} (mW)**	**Phase Noise (dBc/Hz)**	**FOM_T (dBc/Hz)**	**FOM (dBc/Hz)**	**Chip Area (mm^2)**
This work	**65nm CMOS**	**73.24**	**22.8**	**10.2**	**-106.7 to -114.63 @10MHz**	**-181.07 to -189**	**-173.9 to -181.84**	**0.03**
[77] TCAS-I 2019	65nm CMOS	62.25	26.2	7.4-11.2	-107.2 to -116.3 @10MHz	-180.96 to -191.86	-172.6 to -183.5	0.04
[11] TMTT 2016	65nm CMOS	59.3	39	8.9 – 10.4	-101.7 t0 -113.4@ 10MHz	-179.6 to -190.6	-167.8 to -179	0.074
[24] JSSC 2015	65nm CMOS	106.7	39.4	30-45	-101.6 to -108.2@10MHz	-179.3 to -185.9	-165.7 to -174	0.55[1]
[61]TCAS-I 2015	0.18um BiCMOS	60.85	17.2	11.2-19.1	-87.5 to -93.5@1MHz	-177.4 to -181	-170.4 to -176.2	0.347[1]
[3] TCAS-I 2013	90nm CMOS	56.75	16.07	8.7	-97 to -118 @10MHz	-166.8 to -187.4	-162.7 to -184.3	0.1
[5] TCAS-I 2014	65nm CMOS	61	14.2	6	-105.9 to -108.3@10MHz	-176.9 to -179.3	-173.8 to -176.2	0.031
[75] TCAS-I 2017	65nm CMOS	59	14.2	18	-90.7 to -94.1 @1MHz	-176.6 to -180	-169 to -172.4	0.1
[76] TMTT 2015	65nm CMOS	81.5	14	33	-90 to -97.3 @1MHz	-176 to -182.6	-173 to -179.7	0.0462

[1] Full chip size

Chapter 6

Conclusions and Future Research

6.1 Conclusions

VCOs with wide tuning range are critical building blocks of high-data-rate wireless communication and high-resolution radar operating in mm-wave band and beyond. CMOS is the technology of choice for implementing these systems on a single chip incorporating both mm-wave frond-end and baseband digital part of the system. However, because of limited tuning range and quality factor of CMOS varactors, it is not possible to design low phase-noise VCOs with wide tuning using congenital approaches. In this dissertation, we introduce novel circuit topologies for wide tuning range dual-band VCOs in standard CMOS process. The proposed circuits not only achieve large tuning ranges but also exhibit good phase noise performance as described below.

After an introduction of mm-wave applications, devices and VCOs in Chapter 1, studying passive and active components used for construction of mm-wave VCOS in Chapter 2, and background review of oscillators in Chapter 3, a wide tuning range voltage controlled oscillator with switchable VCO cores is presented in Chapter 4. By switching the cross-coupled cores on and off modes, the circuit operates in two different bands with an overlap for continuous tuning range. As opposed to the coupled multicore VCOs, the proposed structure does not require any coupled inductor or transformer achieving a PN performance similar to single-core VCO utilizing standalone inductors. Reusing the inductors of the external core as the buffer of the inductors, the proposed structure avoids

using a bulky passive combiner to combine the output power of the cores. Implemented in 65 nm bulk CMOS, the proposed VCO achieves a measured wide tuning range of 26.2% from 54.1 to 70.4 GHz while consuming 7.4-11.2 mA current from 1.0-V power supply. The peak measured phase noise at 10-MHz offset is -116.3 dBc/Hz and the corresponding FOM_T varies from -180.96 to -191.86 dB. The VCO core area is only 0.1×0.395 μm^2.

In Chapter 5, a mm-wave VCO with wide FTR and low PN is presented. By utilizing a high-Q capacitor and a lossless switch structure as the load of the transformer, a high-Q switched inductors are realized to design a dual-mode VCO. The center frequency of each mode is carefully chosen and with sufficient frequency overlap, so that the circuit presents the capability of high FTR along with improved PN performance in comparison to the existing VCO design with transformer-based inductors. The VCO is implemented in 65nm CMOS technology and exhibits a measured wide FTR of 22.8% from 64.88 to 81.6 GHz. The peak measured PN at 10 MHz offset frequency for even-mode and odd-mode are 114.63 dBc/Hz and 112.93 dBc/Hz, respectively. The VCO cores consume 10.2 mA from 1 V power supply and occupy 0.146×0.205 mm^2 chip area.

6.2 Future work

In this dissertation, we presented a wide FTR dual-core VCO where the employed axillary buffers attenuates the generated low frequency band signal because of the un-tuned LC tank of the second core. In the future, we plan to address this issue and suggest to use proper size of varactors for the second core (high frequency band) or switched capacitors with minimum introduced loss to the tank. The proposed circuits are designed in 65nm CMOS technology which suffers from low f_{max} (about 200 GHz) and low Q inductors/varactors. However, employing available advanced CMOS technologies such as 22nm FD-SOI with f_{max} of higher than 300 GHz, high resistive substrate and high Q passive components, leads to the design of low power, low phase noise and wide FTR VCOs beyond 100GHz. Moreover, presented circuits exhibit high K_{VCO} which is sensitive to the supply noise. Hence in the future we plan to decrease it for practical applications without sacrificing PN performance of the VCO.

6.3 Related Publications

JOURNALS:

As the result of the presented research work, the following articles have been published or submitted for publication:

Ali Basaligheh, Parvaneh Saffari, Wolfgang Winkler and Kambiz Moez, "A Wide Tuning Range, Low Phase Noise, and Area Efficient Dual-Band Millimeter-Wave CMOS VCO Based on Switching Cores," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 8, pp. 2888-2897, Aug. 2019.

Ali Basaligheh, Parvaneh Saffari, Igor Filanovsky and Kambiz Moez, "A 65-81 GHz CMOS Dual-Mode VCO Using High Quality Factor Transformer Based Inductors," to in *IEEE Transactions on Microwave Theory and Techniques,* July. 2019 (submitted).

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