

# Real-Time Device-Level Simulation of MMC-Based MVDC Traction Power System on MPSoC

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**Abstract**—Real-time simulation of device-level power electronic converter models plays an essential role in traction power systems by allowing accurate prediction of device stresses to design improved control and protection schemes. This paper proposes the electrothermal behavioral power electronic models for the modular multilevel converter (MMC)-based medium voltage direct current (MVDC) traction power system based on the Wiener–Hammerstein configuration. The new configuration introduces the carrier charge prerequisite dynamic transients before device turn-ON or turn-OFF operation. The equivalent carrier charge circuit is also proposed, and the first-order delay assumption of turn-ON and turn-OFF delay time has been proven by the device datasheet. The power electronic device models are implemented in a Xilinx<sup>®</sup> Zynq<sup>®</sup> multiprocessing system-on-chip platform. By utilizing hardware and software codesign, both 25- $\mu$ s time-step system-level and 100-ns time-step device-level transients can be captured in real time within a single device. The three-phase unbalance issue has been resolved by introducing the three-phase to single-phase MMC topology. In the case study, the MMC-based MVDC traction power system has been utilized for the performance of the proposed electrothermal behavioral power electronic models by the off-line simulation models on SaberRD<sup>®</sup> for device-level transients and PSCAD/EMTDC<sup>®</sup> for system-level transients.

**Index Terms**—Behavioral modeling, datasheet, diode, electrothermal, hardware-in-the-loop (HIL), insulated-gate bipolar transistor (IGBT), modular multilevel converter (MMC), multiprocessing system-on-chip (MPSoC), real-time systems, traction, Wiener–Hammerstein configuration.

## I. INTRODUCTION

MODERN electric railway system powered by galvanic cells dates back to early 1837. Traction power systems witnessed the significant changes at all levels: switch technology [mercury-arc valves to insulated-gate bipolar transistor (IGBT)] [1], [2], converter topology (mercury-arc rectifier to voltage source converter) [3]–[8], energy storage system (low energy density flywheel-based to high energy density supercapacitor-based) [9], [10], and advanced control methods (simple open loop to complex self-adaptive) [11]–[13]. The design and development of a reliable, efficient, and cost-effective traction drive system is a complex process requiring

several iterations on expensive and time-consuming hardware prototypes. Thus, real-time hardware-in-the-loop (HIL) simulation technology has come to play an essential role in the all transportation power systems and significantly reduced the cost in the early design period [14], [15]. Nevertheless, in almost all real-time system model implementation, the focus was mainly on the electric machine and propulsion components and seldom on the power electronic converters, which were usually represented by simplified system-level models. With a device-level model embedded into the HIL testing system, the power electronic system can be tautologically tested for the design in a nondestructive simulation environment, which would allow an accurate prediction of converter stresses [16], [17]. At the same time, advances in digital processor technology are enabling hardware acceleration HIL simulation with the integration of the multiple ARM<sup>®</sup> processors and FPGA-based programmable logic (PL) to function into a single chip [18]–[20]. FPGAs have been successfully utilized for real-time hardware emulation of detailed models of power systems and power electronic apparatus [17], [21]–[27].

Conventional power converters, such as the two-level dc–ac converter, neutral point clamping, and flying capacitor topology, are deficient in handling high voltage and complicated voltage balancing. The modular multilevel converter (MMC) is considered as a strong candidate to overcome the shortcomings in conventional converters [7], [8]. The advantages of MMC, such as flexible configuration, low applied voltage submodules, alternative submodule source, and strong harmonic suppression, gained broad application in wind farm [28], solar farm [29], railway system [5], and energy storage systems [30].

Both system-level and device-level models have been applied in the simulation of power converter behavior [31]–[40]. Device-level models help to simulate the electromagnetic and electrothermal transients of the devices. Three types of device-level models have been utilized in the simulation application: 1) analytical [35], [36]; 2) numerical [37], [38]; and 3) behavioral [39], [40]. Both analytical and numerical models apply complex nonlinear physical equations into the network calculation, which increases the iteration time and computation burden. Behavioral models circumvent the detailed physical calculations and predict the device operating point under certain circumstances. Both the Hammerstein and Wiener models are utilized in common behavioral models for various applications [41]–[50]. The single Hammerstein model contains a nonlinear static block

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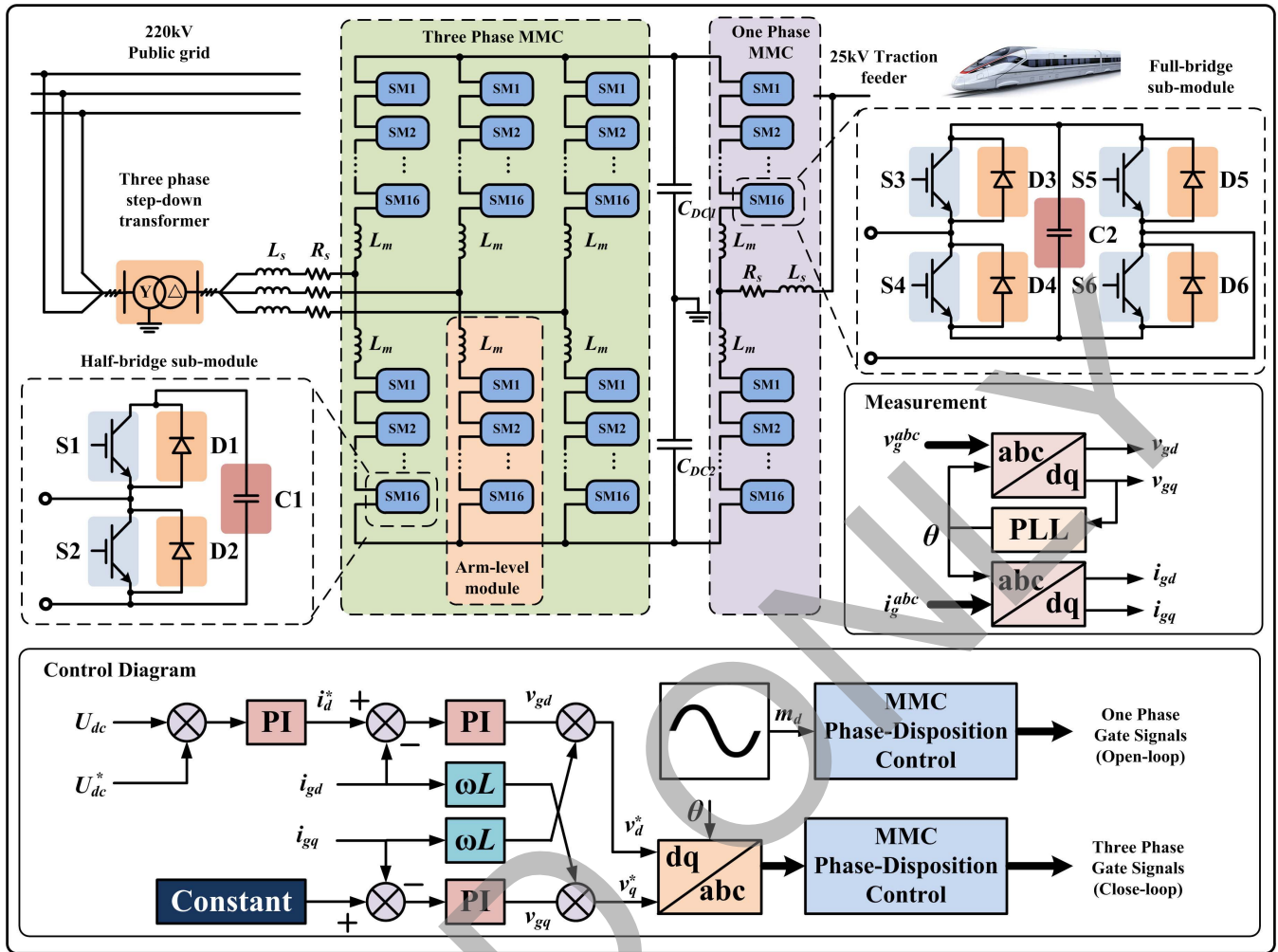


Fig. 1. MMC-based traction power system.

and a linear time-invariant (LTI) dynamic block, which cannot represent the exact prerequisites for physical processes. With the help of the Wiener–Hammerstein structure, the proposed models can present the exact carrier charge processes before the turn-ON and turn-OFF switching transient of the IGBT.

This paper proposes the electrothermal behavioral MMC models for device level and submodule level by using the Winner–Hammerstein configuration with the equivalent electrical element representation. For the traction power system, the detailed modeling and real-time simulation of the transformer also play a nonnegligible role in the transient analysis of the traction power system. In the study case, the transformer nonlinear saturation behavior is also included in the real-time transient simulation, which presents critical technical and economic challenges to traction loads and system operators. This paper is organized as follows. Section II explains the MMC-based traction power system, the MMC submodule equivalent representation, and the transformer model. Section III describes the construction of IGBT module electrothermal behavioral models by the Winner–Hammerstein configuration. Section IV gives a brief introduction to the Zynq<sup>®</sup> MPSoC platform and the details of the implementation.

Section V shows the device-level and system-level real-time simulation result and discussion, which is verified by SaberRD<sup>®</sup> and PSCAD/EMTDC<sup>®</sup>.

## II. MMC-BASED TRACTION POWER SYSTEM

The MMC-based traction power system, as shown in Fig. 1, consists of the 220-kV public grid, the three-phase step-down transformer, the three-phase MMC-based ac/dc converter, and the single-phase MMC dc/ac converter. The three-phase MMC-BASED ac/dc converter utilizes the half-bridge submodule, while the single-phase MMC dc/ac converter utilizes the full-bridge submodule [3]. The half-bridge MMC lacks the dc fault blocking capability but requires less-power electronic components, while the full-bridge MMC inherits the advantage of dc blocking features but increases the cost of the MMC system [48], [49]. In this paper, three-phase half-bridge MMC is considered to reduce the cost on the grid side, while the single-phase full-bridge MMC is utilized on the load side to enable the dc fault blocking feature. The three-phase transformer includes the calculation of the nonlinear saturation behavior, and a wye–delta configuration is employed

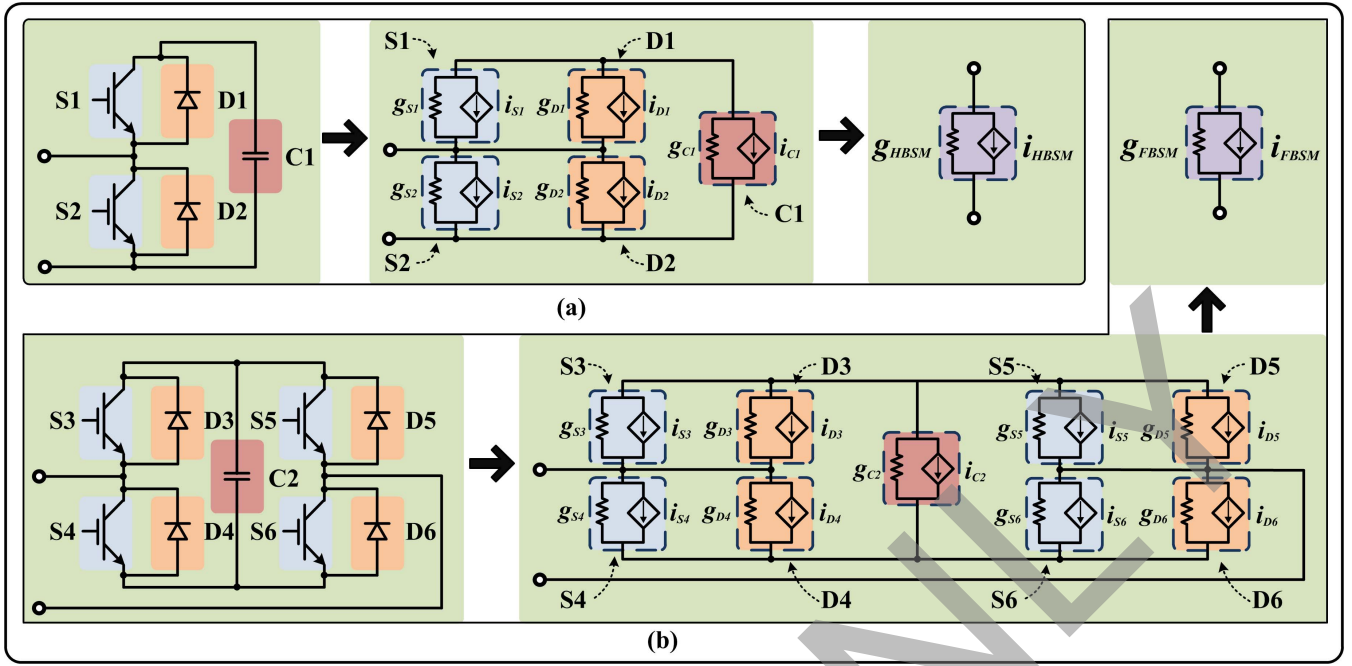


Fig. 2. Hierarchical Norton equivalent process. (a) Half-bridge submodule. (b) Full-bridge submodule.

inside the traction power system topology. The measurement unit calculates the  $dq$  transform of the three-phase grid-side voltage and current. With the phase-locked loop calculation, the  $dq$  phase angle  $\theta$  can be transmitted to the control system for closed-loop control. The control diagram of the traction power system is shown in Fig. 1 (bottom). The three-phase MMC is controlled by the dc-link voltage, and the objective of its control diagram is to maintain the voltage at the specific value. The single-phase MMC utilizes the open-loop control to operate at rated condition.

#### A. MMC Submodule

Fig. 2 shows the equivalent processes of the half-bridge and full-bridge submodule into the combination of conductance and voltage-controlled current source (VCCS). Each device inside the submodule is reduced to a conductance paralleled with controlled current source in the Norton equivalent. After the reduction process, the half-bridge or full-bridge submodule is equal to a conductance paralleled with VCCS. The Norton equivalent representation of the half-bridge submodule is shown in Fig. 2(a), given as

$$g_{HBSM} = \frac{g_1 \cdot g_{c1}}{g_1 + g_{c1}} + g_2 \quad (1)$$

$$i_{HBSM} = \frac{i_1 \cdot g_{c1} - i_3 \cdot g_1}{g_1 + g_{c1}} + i_2 \quad (2)$$

$$i_j = i_{Sj} + i_{Dj}, \quad j = 1, 2 \quad (3)$$

$$g_j = g_{Sj} + g_{Dj}, \quad j = 1, 2 \quad (4)$$

where  $g_{HBSM}$  and  $i_{HBSM}$  are the equivalent conductance and VCCS of the half-bridge submodule, respectively, and  $g_{Sj}$  and  $i_{Sj}$  are the equivalent conductance and VCCS of the IGBT, respectively.  $g_{Dj}$  and  $i_{Dj}$  are the equivalent conductance and VCCS of the diode, respectively, and  $g_j$  and  $i_j$  are

the equivalent conductance and VCCS of the IGBT module, respectively.

The Norton equivalent representation of the full-bridge submodule is shown in Fig. 2(b), given as

$$g_{FBSM} = \frac{(g_3g_4g_5 + g_3g_4g_6 + g_3g_5g_6 + g_3g_5g_2 + g_4g_5g_6 + g_3g_6g_2 + g_4g_5g_2 + g_4g_6g_2 + g_5g_6 + g_5g_2 + g_6g_2)}{(g_3g_4 + g_3g_6 + g_4g_5 + g_3g_2 + g_4g_2 + g_5g_6 + g_5g_2 + g_6g_2)} \quad (5)$$

$$i_{FBSM} = -\frac{(M_1g_3g_4g_5 + M_2g_3g_4g_6 + M_1g_3g_5g_6 + M_3g_3g_4g_5 + M_1g_3g_5g_2 + M_2g_3g_5g_6 + M_3g_3g_4g_6 + M_1g_3g_6g_2 + M_2g_3g_5g_2 + M_3g_3g_5g_6 + M_2g_4g_5g_2 + M_3g_3g_5g_2 + M_3g_4g_5g_6 + M_3g_3g_6g_2 + M_3g_4g_5g_2 + M_3g_4g_6g_2)}{(g_3g_4 + g_3g_6 + g_4g_5 + g_3g_2 + g_4g_2 + g_5g_6 + g_5g_2 + g_6g_2)} \quad (6)$$

$$M_1 = -i_3/g_3 - i_4/g_4 + i_7/g_7 \quad (7)$$

$$M_2 = i_5/g_5 + i_6/g_6 - i_7/g_7 \quad (8)$$

$$M_3 = i_4/g_4 - i_6/g_6 \quad (9)$$

$$g_j = g_{Sj} + g_{Dj}, \quad j = 3, 4, 5, 6 \quad (10)$$

$$i_j = i_{Sj} + i_{Dj}, \quad j = 3, 4, 5, 6 \quad (11)$$

where  $g_{FBSM}$  and  $i_{FBSM}$  are the equivalent conductance and VCCS of the full-bridge submodule, respectively.  $g_{Sj}$  and  $i_{Sj}$  are the equivalent conductance and VCCS of the IGBT, respectively,

$g_{Dj}$  and  $i_{Dj}$  are the equivalent conductance and VCCS of the diode, respectively, and  $g_j$  and  $i_j$  are the equivalent conductance and VCCS of the IGBT module, respectively.

## B. Transformer

In this paper, the admittance matrix-based model is employed to model the transformer, which includes the non-linear saturation phenomena [27]. The admittance matrix is based on the mutually coupled coils concept. By applying Trapezoidal rule, the discrete-time difference equations are given as

$$\mathbf{i}_T(t) = \mathbf{G}\mathbf{v}_T(t) + \mathbf{hist}_T(t - \Delta t) \quad (12)$$

$$\mathbf{hist}_T(t - \Delta t) = \mathbf{Y}_T\mathbf{v}_T(t - \Delta t) \quad (13)$$

$$+ (\mathbf{I}_T - 2\mathbf{G}_T\mathbf{R}_T)\mathbf{hist}_T(t - 2\Delta t)$$

$$\mathbf{Y}_T = 2(\mathbf{G}_T - \mathbf{G}_T\mathbf{R}_T\mathbf{G}_T) \quad (14)$$

$$\mathbf{G}_T = \left[ \mathbf{I}_T + \frac{\Delta t}{2}\mathbf{L}_T^{-1}\mathbf{R}_T \right]^{-1} \frac{\Delta t}{2}\mathbf{L}_T^{-1}. \quad (15)$$

where  $\mathbf{R}_T$  is the diagonal matrix of winding resistance,  $\mathbf{L}_T$  is the winding leakage inductances matrix,  $\Delta t$  is the electrical simulation time step,  $\mathbf{hist}_T(t - \Delta t)$  is the  $n \times 1$  history terms vector, and  $\mathbf{I}_T$  is the  $n \times n$  identity matrix.

The nonlinear saturation phenomena can be seen in the transformer's continuous magnetization curve. Thus, the modeling of transformer with nonlinear saturation feature and Newton-Raphson iteration is necessary in the real-time simulation of the traction power system, given as

$$\mathbf{J}_T(\mathbf{i}_{j+1} - \mathbf{i}_j) = -\mathbf{F}_T(\mathbf{i}_j) \quad (16)$$

$$\mathbf{J}_T = \frac{\partial \mathbf{F}_T(\mathbf{i}_j)}{\partial \mathbf{i}_j} = \mathbf{R}_{\text{thév}} + \frac{\partial \mathbf{f}_T(\mathbf{i}_j)}{\partial \mathbf{i}_j} \quad (17)$$

$$-\mathbf{F}_T = \mathbf{v}_{\text{oc}} - \mathbf{R}_{\text{thév}} \cdot \mathbf{i}_j - \mathbf{f}_T(\mathbf{i}_j) \quad (18)$$

where  $\mathbf{J}_T$  is the Jacobian matrix,  $\mathbf{i}_j$  is the current vector at the  $j$ th iterations  $\mathbf{v}_{\text{oc}}$  is the open-circuit voltage vector,  $\mathbf{R}_{\text{thév}}$  is the Thévenin equivalent resistance matrix, and  $\mathbf{f}_T(\mathbf{i}_j)$  is the nonlinear function.

## III. WIENER-HAMMERSTEIN CONFIGURATION-BASED DEVICE-LEVEL BEHAVIORAL ELECTROTHERMAL POWER CONVERTER MODEL

In this section, the Wiener-Hammerstein configuration is utilized to set up the modeling procedure in Section III-A. With the behavioral modeling methodology, the modeling procedure is separated into the dynamic carrier charge stage in Section III-B, the static electrical characteristic in Section III-C, the dynamic electrical characteristic in Section III-D, and power consumption and thermal calculation in Section III-E. The IGBT module used in this paper is 5SNA 1500E330305 from ABB whose datasheet parameters are provided in [52]. In Table I, datasheet plot utilization is shown in each modeling procedure.

### A. Wiener-Hammerstein Model Versus Wiener-Hammerstein Configuration

A Wiener-Hammerstein model contains a nonlinear static block sandwiched between two LTI dynamic blocks, while the Wiener-Hammerstein configuration separates the static block

TABLE I  
WIENER-HAMMERSTEIN CONFIGURATION MODELING PROCEDURE

Dynamic carrier charge	Static electrical characteristic	Dynamic electrical characteristic	Power consumption and thermal calculation
$V_{GE}-Q_g,$ $C-V_{CE},$ $t_{d,on}-R_G,$ $t_{d,off}-R_G$	$I_C-V_{CE},$ $I_F-V_F$	$t_r-I_c,$ $t_f-I_c,$ $t_r-R_G,$ $t_f-R_G,$ $Q_{rr}-I_F,$ $I_{rr}-I_F,$ $Q_{rr}-di/dt,$ $I_{rr}-di/dt$	$E_{on}^{IGBT}-I_C,$ $E_{off}^{IGBT}-I_C,$ $E_{on}^{IGBT}-R_G,$ $E_{off}^{IGBT}-R_G,$ $E_{rec}-I_F,$ $E_{rec}-di/dt,$ $Z_{thjc}^{IGBT}-t,$ $Z_{thjc}^{Diode}-t$

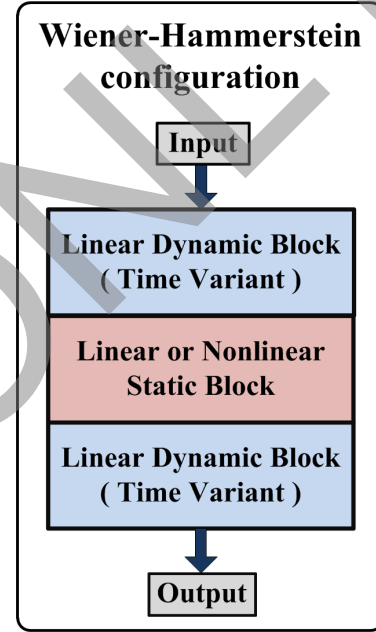


Fig. 3. Wiener-Hammerstein configuration.

from the forward linear time-variant (LTV) dynamic block and the backward LTV dynamic block. The detail of the Wiener-Hammerstein configuration is shown in Fig. 3.

The nonlinear static block of the Wiener-Hammerstein model leads to iteration processes in the calculation. The Wiener-Hammerstein configuration can simplify the nonlinear static block into quasi-linear one, which results in reduction of computation. Compared with the LTI dynamic block, the forward and backward LTV dynamic blocks are considered to have little impact on the system simulation result.

### B. Dynamic Carrier Charge and Discharge Electrical Characteristic

The carrier charge and discharge stage can be considered as a prerequisite condition to the dynamic turn-ON and turn-OFF transients. The equivalent IGBT capacitance circuit is shown in Fig. 4(a).  $R_{G(\text{int})}$  represents the equivalent internal resistance. The static gate charge plot is shown in Fig. 4(b), and linear approximation is applied for different  $V_{cc}$  values. The relation

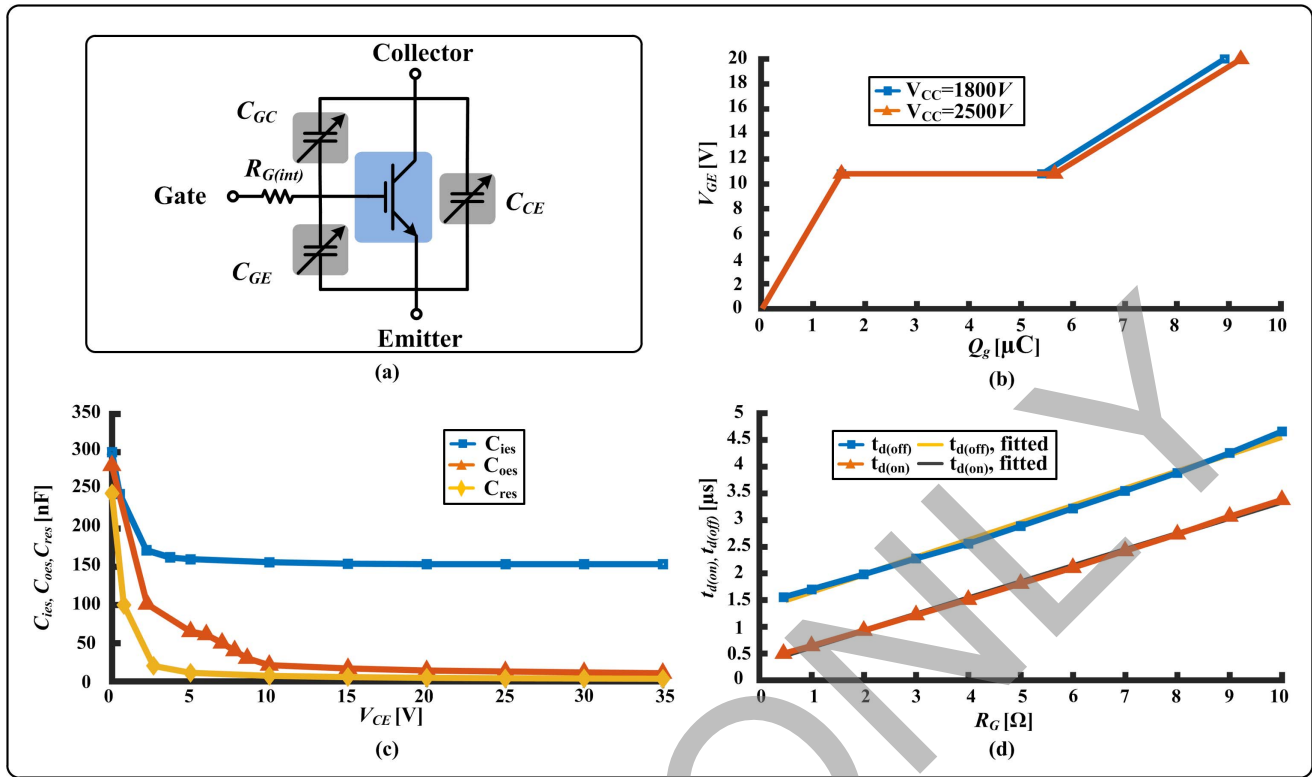


Fig. 4. Carrier charge. (a) Capacitance equivalent circuit. (b) Static gate charge. (c) Low-signal capacitance. (d) IGBT turn-ON and turn-OFF delay time.

of the parasitic and low-signal capacitances are given as

$$C_{ies} = C_{GE} + C_{GC} \quad (19)$$

$$C_{res} = C_{GC} \quad (20)$$

$$C_{oes} = C_{GC} + C_{CE} \quad (21)$$

where  $C_{ies}$ ,  $C_{res}$ , and  $C_{oes}$  are the input capacitance, the reverse transfer capacitance, and the output capacitance, respectively,  $C_{GE}$ ,  $C_{GC}$ , and  $C_{CE}$  are the gate-emitter capacitance, gate-collector capacitance, and collector-emitter capacitance, respectively.

The low-signal capacitance is not constant in the application, and the relation between  $V_{CE}$  and capacitance is given in Fig. 4(c). The gate resistance value has a linear relation with the turn-ON and turn-OFF delay time, as shown in Fig. 4(d).

The physical carrier charge and discharge procedures and the equivalent circuit are shown in Fig. 5. The detailed explanation of each stage will be described separately.

1) *Turn-ON Stage*: The turn-ON stage can be described into five carrier charge procedures.

$t_0-t_1$ : The gate current  $I_G$  rockets up and starts to decay to a constant value. The gate-emitter capacitor  $C_{GE}$  is charged to the turn-ON threshold voltage.

$t_1-t_2$ : The voltage of the gate-emitter capacitor  $C_{GE}$  reaches the threshold voltage  $V_{GE(th)}$  and continues to rise to the Miller plateau voltage, which will trigger the turn-ON transient. The collector current  $I_C$  starts ramping up with the overshoot phenomenon.

$t_2-t_3$ : The collector current  $I_C$  rising stage is finished at  $t_2$ , and  $V_{CE}$  begins to decrease. The voltage of the gate-emitter

capacitor  $C_{GE}$  remains in a stable range until the Miller plateau charge procedure is finished.

$t_3-t_4$ : The Miller plateau charge procedure continues. The gate-collector capacitor  $C_{GC}$  is being charged.

$t_4-t_5$ : The charging procedure continues on the gate-emitter capacitor  $C_{GE}$ , and its voltage reaches the desired gate voltage.

2) *Turn-OFF Stage*: The turn-OFF stage can be described into four carrier discharge procedures.

$t_6-t_7$ : The gate current  $I_G$  cascades down and starts to decay to a constant value. The gate-emitter capacitor  $C_{GE}$  is discharged to the Miller plateau voltage.

$t_7-t_8$ : The voltage of gate-emitter capacitor  $V_{GE}$  decreases to the Miller plateau, and the collector-emitter voltage  $V_{CE}$  increases slowly due to the nonlinear features of  $C_{GC}$ , which is a small value at this stage.

$t_8-t_9$ : The value of  $C_{GC}$  becomes large, and  $V_{CE}$  increases rapidly to the normal operating point.

$t_9-t_{10}$ : The voltage of gate-emitter capacitor  $V_{GE}$  decreases to threshold voltage, and the collector current  $I_C$  starts to decay.

The equivalent circuit of the gate charge and discharge is shown in Fig. 5. For the turn-ON stage, the equivalent circuit is a typical RC first-order delay one. The turn-ON delay time is highly relative to the gate resistance, given as

$$t_{d(ON)} = K_{ON} \cdot C_{GE} \cdot (R_{G(int)} + R_G) \quad (22)$$

where  $K_{ON}$  is the gate charge parameter for turn-ON transients and is related to the ON-state gate voltage  $V_{GE(ON)}$  and OFF-state voltage  $V_{GE(OFF)}$ .  $R_{G(int)}$  is considered as the internal

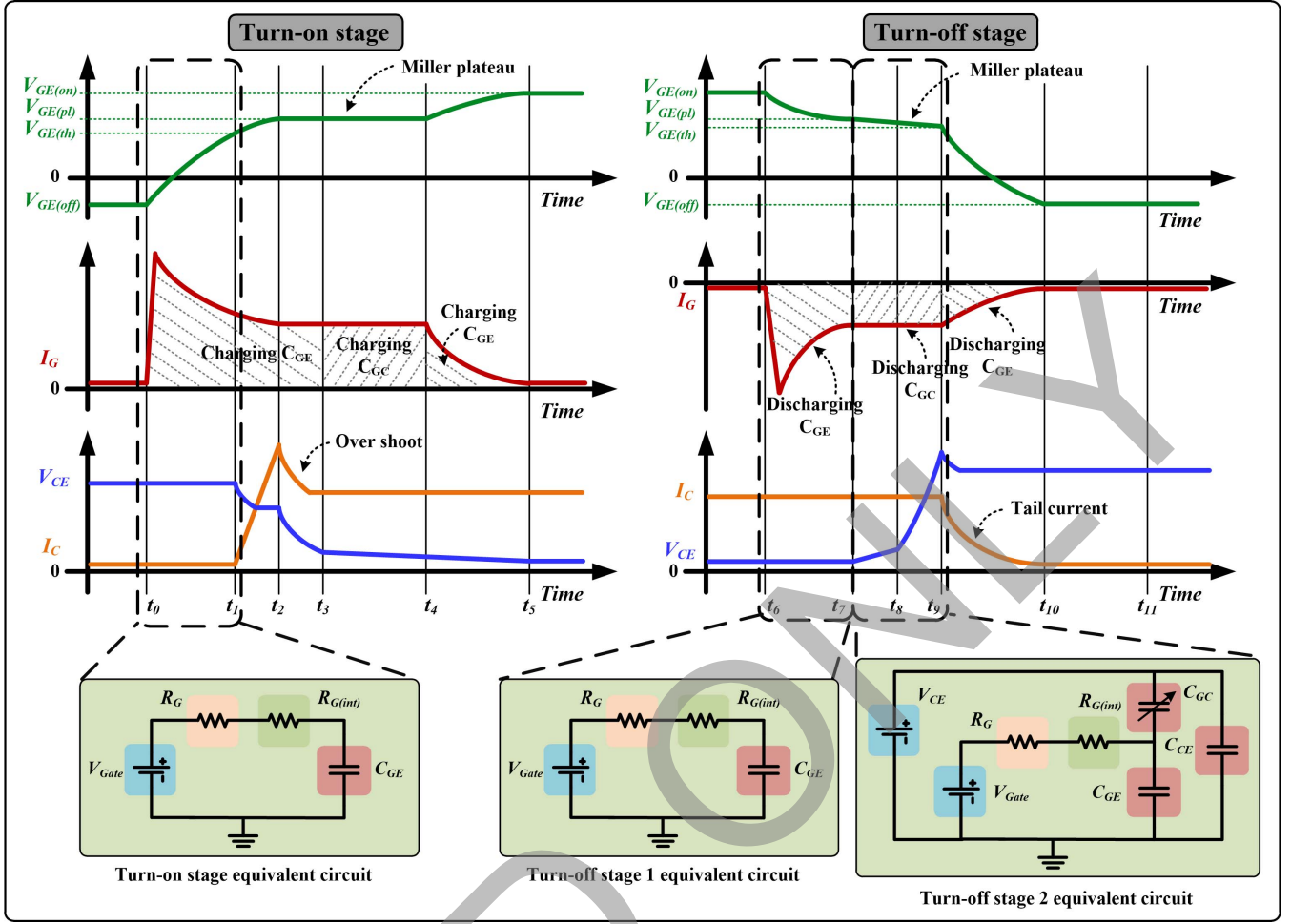


Fig. 5. Carrier charge procedures for turn-ON stage and turn-OFF stage and its equivalent circuit.

parasitic resistance. In Fig. 4(d), the linear fitted result also proves its linearity for the turn-ON delay time.

For the turn-OFF stage, the turn-OFF stage 1 is also considered as a typical RC first-order delay circuit, and the turn-OFF stage 2 can be considered as a constant time procedure. The turn-OFF delay time is highly relative to the gate resistance, given as

$$t_{d(on)} = K_{OFF} \cdot C_{GE} \cdot (R_{G(int)} + R_G) + t_{stage2} \quad (23)$$

where  $K_{ON}$  is the gate charge parameter for turn-ON transients and is related to the ON-state gate voltage  $V_{GE(ON)}$  and OFF-state voltage  $V_{GE(OFF)}$ .  $t_{stage2}$  is considered as a constant time for turn-OFF stage 2. In Fig. 4(d), the linear fitted result also proves its linearity for the turn-OFF delay time.

### C. Static Electrical Characteristic

The IGBT and diode static characteristic is shown in Fig. 6. For MMC application, the collector current of the IGBT module varies each time based on the control algorithm. It is necessary to model the low-current static characteristic in MMC scenario. Thus, the static characteristic separates into low current and normal operating current sections, and the boundary of these sections is defined as 60% of the

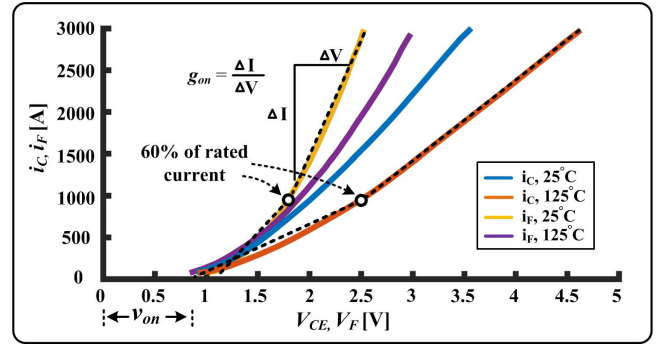


Fig. 6. Static characteristic of IGBT and diode.

rated current point. The static electrical model is made of a temperature-dependent conductance  $g_{low}(T_{vj})$  or  $g_{high}(T_{vj})$  in paralleled with a temperature-dependent VCCS  $i_{low}(T_{vj})$  or  $i_{high}(T_{vj})$ , which is the Norton equivalent expression of  $v_{low}(T_{vj})$  or  $v_{high}(T_{vj})$ . High conductance and a paralleled VCCS represent for the ON-state characteristic while low conductance behaves for the OFF-state characteristic. Based on the datasheet plots, the linear interpolation estimation method has been applied to  $g_{low}(T_{vj})$ ,  $g_{high}(T_{vj})$ ,  $v_{low}(T_{vj})$ ,

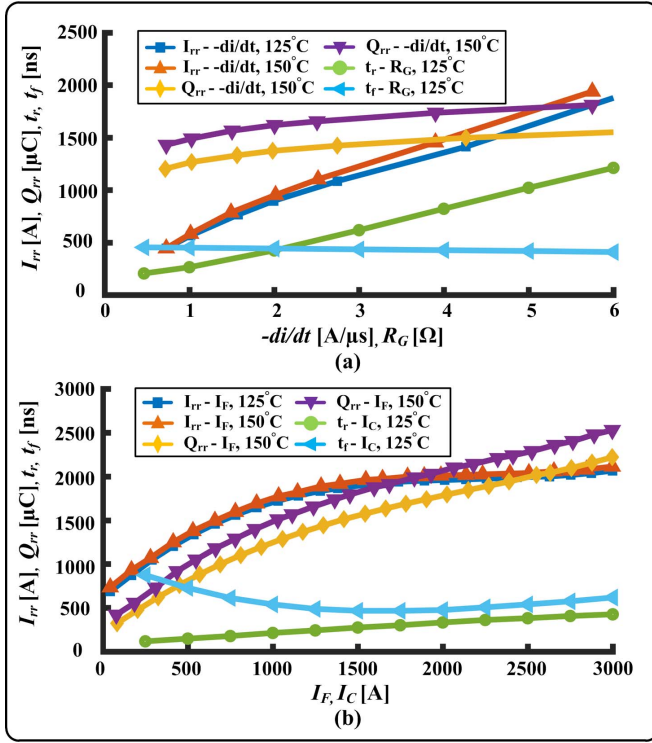


Fig. 7. Dynamic characteristic. (a) Diode  $I_{rr}-di/dt$  and  $Q_{rr}-di/dt$  curves and IGBT  $t_r-R_G$  and  $t_f-R_G$  curves. (b) Diode  $I_{rr}-I_F$  and  $Q_{rr}-I_F$  curves and IGBT  $t_r-I_C$  and  $t_f-I_C$  curves.

and  $v_{high}(T_{vj})$ , given as

$$g_{low}(T_{vj}) = \frac{T_{vj} - T_{25}}{T_{25} - T_{125}} (g_{low}^{T_{25}} - g_{low}^{T_{125}}) + g_{low}^{T_{25}} \quad (24)$$

$$v_{low}(T_{vj}) = \frac{T_{vj} - T_{25}}{T_{25} - T_{125}} (v_{low}^{T_{25}} - v_{low}^{T_{125}}) + v_{low}^{T_{25}} \quad (25)$$

$$i_{low}(T_{vj}) = v_{low}(T_{vj}) \cdot g_{low}(T_{vj}) \quad (26)$$

$$g_{high}(T_{vj}) = \frac{T_{vj} - T_{25}}{T_{25} - T_{125}} (g_{high}^{T_{25}} - g_{high}^{T_{125}}) + g_{high}^{T_{25}} \quad (27)$$

$$v_{high}(T_{vj}) = \frac{T_{vj} - T_{25}}{T_{25} - T_{125}} (v_{high}^{T_{25}} - v_{high}^{T_{125}}) + v_{high}^{T_{25}} \quad (28)$$

$$i_{high}(T_{vj}) = v_{high}(T_{vj}) \cdot g_{high}(T_{vj}) \quad (29)$$

where  $g_{low}(T_{vj})$ ,  $g_{high}(T_{vj})$ ,  $i_{low}(T_{vj})$ , and  $i_{high}(T_{vj})$  are low-current region conductance, high-current region conductance, low-current region VCCS, and high-current region VCCS, respectively.

#### D. Dynamic Electrical Characteristic

The dynamic characteristic parameters for the diode and the IGBT are shown in Fig. 7.

1) *Diode*: Compared with turn-OFF transient, the forward recovery phenomenon and energy loss in the turn-ON period can be negligible. Reverse recovery phenomenon is considered as the major dynamic transient of the diode. The VCCS  $i_{low}(T_{vj})$  or  $i_{high}(T_{vj})$  plays an important role in the turn-OFF operation with default blocking state for  $g_{low}(T_{vj})$  or  $g_{high}(T_{vj})$ . As shown in Fig. 8, the dynamic transients of reverse recovery phenomenon are separated into three stages:

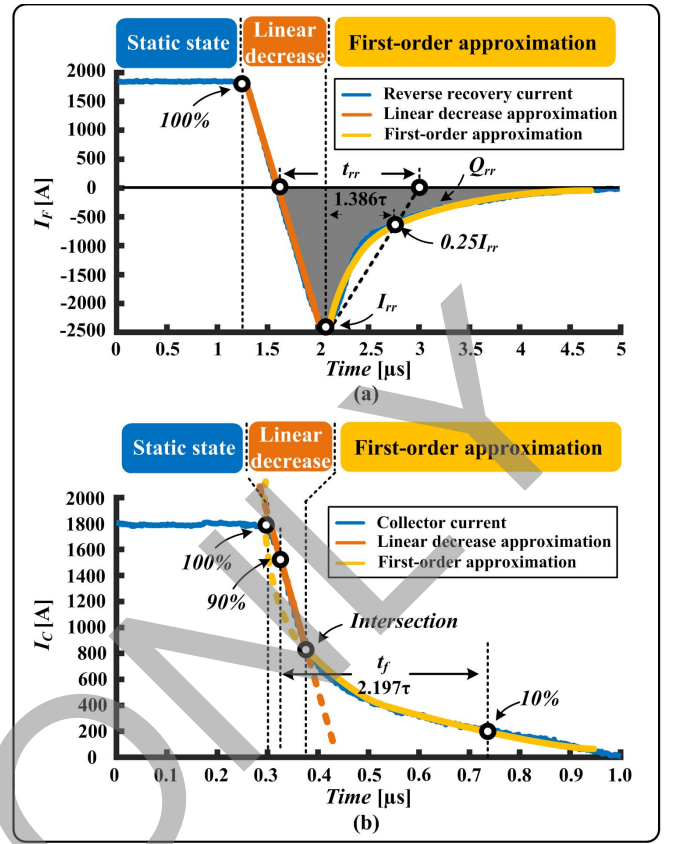


Fig. 8. Dynamic characteristics. (a) Diode reverse recovery. (b) IGBT tail current.

1) default static state; 2) linear reverse recovery current decrease; and 3) decay stage of reverse recovery current. The decay of stage 3 is considered as a first-order delay approximation curve. The reverse recovery time  $t_{rr}$  is estimated by the equation, given as

$$t_{rr} = \frac{2Q_{rr}}{I_{rr}}. \quad (30)$$

2) *IGBT*: The dynamic characteristics of the IGBT can be separated into two parts: 1) turn-ON and 2) turn-OFF. For the turn-ON period, the physic procedure of collector current  $I_c$  can be considered as the first-order delay approximation. For the turn-OFF period, the collector current  $I_c$  decreases at the rate of negative  $di/dt$ , given by

$$\frac{dI_c}{dt} = \frac{L_{stray}}{V_L} \quad (31)$$

where  $V_L$  is the transient overshoot voltage on the IGBT at the time of  $t_9$ , as shown in Fig. 5. After the linear decrease period,  $I_c$  begins to decay as the first-order approximation.

$2.197\tau$  is considered as the normalized time of the collector current rise and fall time of IGBT. With the calculation of the normalized variable  $\tau$ , the dynamic shape of the waveform can be determined.

#### E. Transient Power and Voltage Reconstruction

The total power loss for a dedicated ON or OFF transients in a single device can be derived from the datasheet under

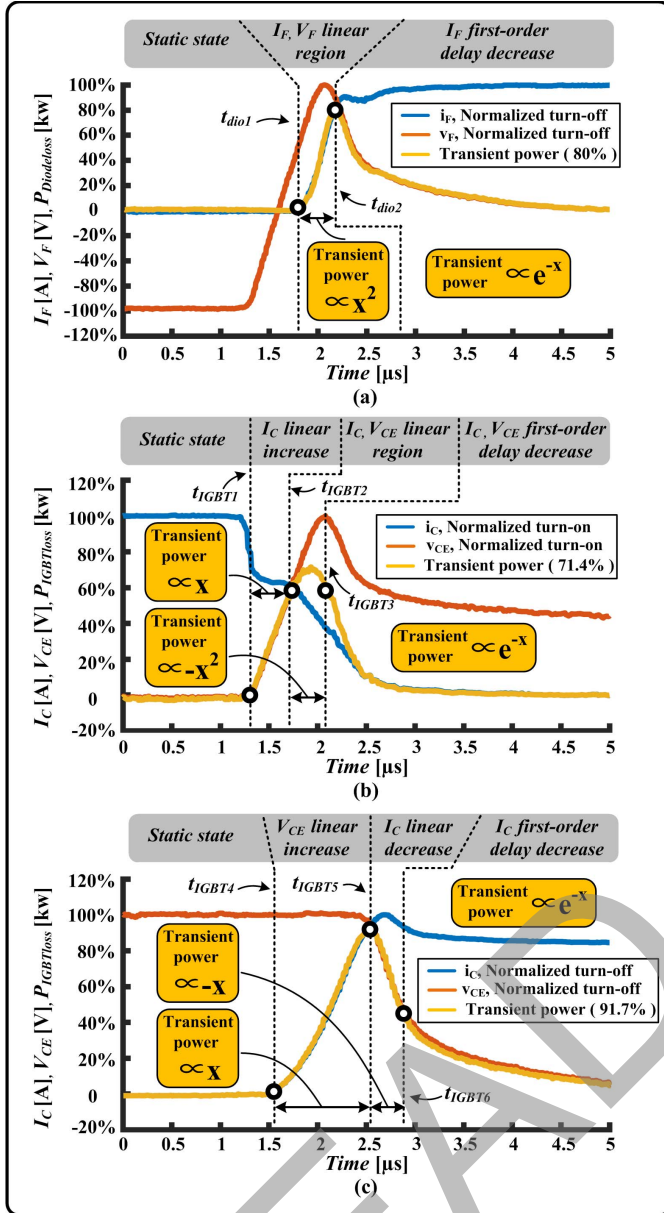


Fig. 9. Normalized transient power waveform. (a) Diode turn-OFF. (b) IGBT turn-ON. (c) IGBT turn-OFF.

the specific circumstance. The detailed transient waveform, as shown in Fig. 9, can be utilized to calculate the transient power loss. Both the device current and voltage have been normalized while its transient power degrades to a certain percentage in order to explain the relationship among current, voltage, and transient power.

Diode turn-OFF transient power, as shown in Fig. 9(a), is separated into square and first-order delay region, given as

$$P_{\text{loss}}^{\text{Diode}} = \int_{t_{\text{dio1}}}^{t_{\text{dio2}}} a_1 x^2 + \int_{t_{\text{dio2}}}^{\infty} (a_2 e^{-x} + c_2) \quad (32)$$

where  $P_{\text{loss}}^{\text{Diode}}$  is the total power loss of the diode,  $t_{\text{dio1}}$  and  $t_{\text{dio2}}$  indicate the start time of the linear region and the first-order delay region, respectively,  $a_1$  is the constant for linear approximation, and  $a_2$  and  $c_2$  are the constants for the first-order delay approximation calculation.

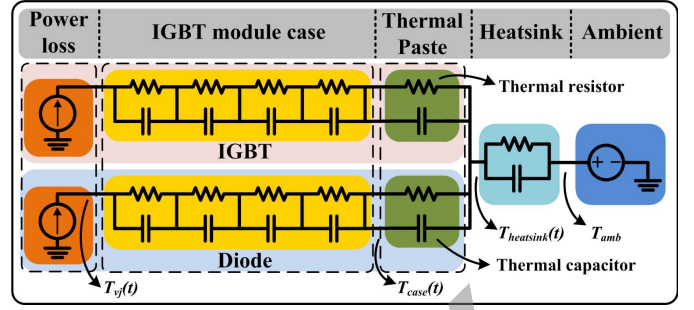


Fig. 10. Thermal calculation circuit of the IGBT module.

IGBT turn-ON transient power, as shown in Fig. 9(b), is separated into positive linear, square, and first-order delay region, given as

$$P_{\text{LossOn}}^{\text{IGBT}} = \int_{t_{\text{IGBT1}}}^{t_{\text{IGBT2}}} a_3 x + \int_{t_{\text{IGBT2}}}^{t_{\text{IGBT3}}} (a_4 x^2 + c_4) + \int_{t_{\text{IGBT3}}}^{\infty} (a_5 e^{-x} + c_5) \quad (33)$$

where  $P_{\text{LossOn}}^{\text{IGBT}}$  is the total power loss of the IGBT during the turn-ON period,  $t_{\text{IGBT1}}$ ,  $t_{\text{IGBT2}}$ , and  $t_{\text{IGBT3}}$  indicate the start time of the collector current linear region, the collector current and collector-emitter voltage linear region, and the first-order delay region, respectively, and  $a_3$ ,  $a_4$ ,  $c_4$ ,  $a_5$ , and  $c_5$  are the constants for the approximation calculation.

IGBT turn-OFF transient power, as shown in Fig. 9(c), is separated into positive linear, negative linear, and first-order delay region, given as

$$P_{\text{LossOff}}^{\text{IGBT}} = \int_{t_{\text{IGBT4}}}^{t_{\text{IGBT5}}} a_6 x + \int_{t_{\text{IGBT5}}}^{t_{\text{IGBT6}}} (-a_7 x + c_7) + \int_{t_{\text{IGBT6}}}^{\infty} (a_8 e^{-x} + c_8) \quad (34)$$

where  $P_{\text{LossOff}}^{\text{IGBT}}$  is the total turn-OFF power loss of the IGBT,  $t_{\text{IGBT4}}$ ,  $t_{\text{IGBT5}}$ ,  $t_{\text{IGBT6}}$ , and  $t_{\text{IGBT7}}$  indicate the start time of collector-emitter voltage linear increase region, collector current linear decrease region, and collector current first-order delay decrease region, respectively, and  $a_6$ ,  $a_7$ ,  $c_7$ ,  $a_8$ , and  $c_8$  are the constants for the approximation calculation.

By calculating the above-mentioned waveform, the exact transient power loss at each moment can be determined, and the device terminal voltage can be obtained.

#### F. Thermal Network Calculation

The thermal calculation circuit is shown in Fig. 10. The VCCS indicates the power loss consumption. Multiple levels of equivalent electrical components have been applied for computing the junction temperature, given as

$$T_{vj}(t) = P_{\text{loss}}(t) \cdot (Z_{\text{thjc}} + Z_{\text{thch}} + Z_{\text{thha}}) + T_{\text{amb}} \quad (35)$$

where  $P_{\text{loss}}(t)$  is the power loss for each device,  $T_{\text{amb}}$  is the ambient temperature,  $Z_{\text{thjc}}$  is the thermal impedance from junction to case,  $Z_{\text{thch}}$  is the thermal impedance from case to heat sink, and  $Z_{\text{thha}}$  is the thermal impedance from heat sink



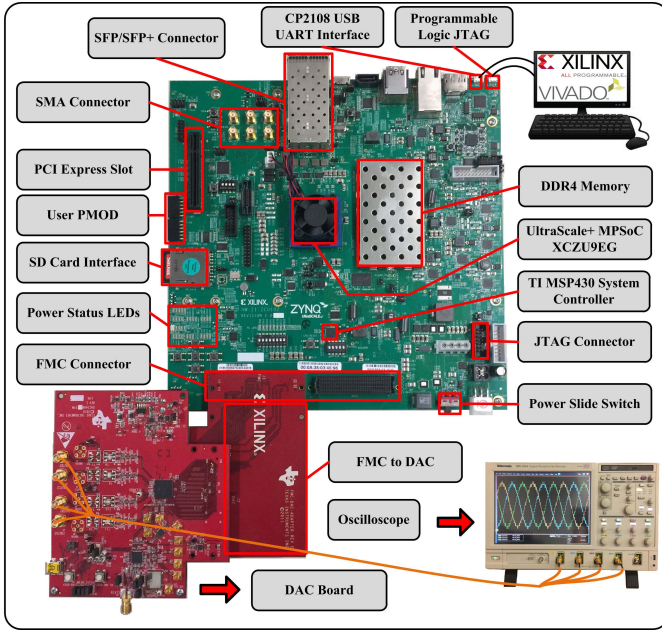


Fig. 11. MPSoC platform setup.

to ambient. A 10 K/kW water-cooled heat sink is mounted on each IGBT module in this paper. The junction temperature numerical solution is given as

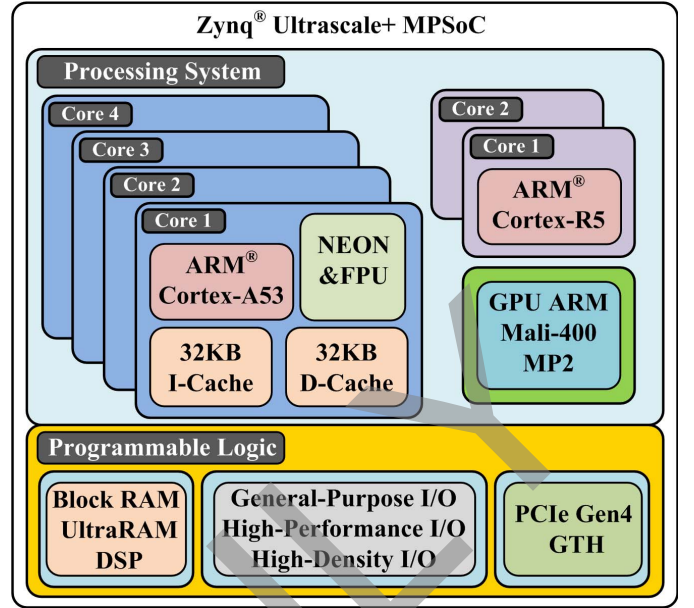
$$\begin{aligned}
 T_{vj}(t) &= \sum_{i=1}^6 \Delta T_{th}^i(t) + T_{amb} \\
 &= \sum_{i=1}^5 \left( \frac{R_{th}^i \cdot \Delta t_{thm}}{2\tau_{th}^i + \Delta t_{thm}} (P_{loss}(t) + P_{loss}(t - \Delta t_{thm})) \right. \\
 &\quad \left. + \frac{2\tau_{th}^i - \Delta t_{thm}}{2\tau_{th}^i + \Delta t_{thm}} \Delta T_{th}^i(t - \Delta t_{thm}) \right) \\
 &\quad + \frac{R_{th}^6 \cdot \Delta t_{thm}}{2\tau_{th}^6 + \Delta t_{thm}} (P_{total}(t) + P_{total}(t - \Delta t_{thm})) \\
 &\quad + \frac{2\tau_{th}^6 - \Delta t_{thm}}{2\tau_{th}^6 + \Delta t_{thm}} \Delta T_{th}^6(t - \Delta t_{thm}) + T_{amb} \quad (36)
 \end{aligned}$$

where  $\Delta t_{thm}$  is the thermal time step,  $\Delta T_{th}^i(t)$  is the node point junction temperature for each layer,  $P_{loss}(t)$  is the power loss for the individual device,  $T_{amb}$  is the ambient temperature,  $\tau_{th}^i$  is the multiplication product of  $R_{th}^i$  and  $C_{th}^i$ , and  $P_{total}(t)$  is the total power loss for each time step in a single device.

#### IV. HARDWARE AND SOFTWARE CODESIGN AND IMPLEMENTATION OF MMC-BASED TRACTION POWER SYSTEM ON ZYNQ<sup>®</sup> ULTRASCALE+<sup>™</sup> MPSOC PLATFORM

##### A. Zynq<sup>®</sup> Ultrascale+<sup>™</sup> MPSoC Platform

The Xilinx<sup>®</sup> Zynq<sup>®</sup> Ultrascale+<sup>™</sup> MPSoC system setup is shown in Fig. 11. The computer compiles and programs the VHDL code to dedicated MPSoC board via Xilinx<sup>®</sup> FPGA Mezzanine Card-to-digital to analog converter (DAC) converter board, which is connected to the TI DAC board. The DAC board converts the digital signals to the analog signals and transmits the analog signals to the oscilloscope to present the real-time implementation results.

Fig. 12. Zynq<sup>®</sup> Ultrascale+<sup>™</sup> MPSoC schematic.

The Zynq<sup>®</sup> Ultrascale+<sup>™</sup> MPSoC [51], as shown in Fig. 12, combines the processing system (PS) and the PL into the same device. The 16-nm PL fabric resources inside the device enable the hardware to compute acceleration in parallelism. The PS contains a 64-bit quad-core Cortex<sup>®</sup>-A53 processor, a real-time dual-core Cortex<sup>®</sup>-R5 processor, a Mali-400 MP2 GPU, and the peripheral device.

PL in the Zynq<sup>®</sup> Ultrascale+<sup>™</sup> (XCZU9EG) consists of 600 000 logic cells, 274 000 lookup tables (LUTs), 548 000 flip-flops, 912 block RAMs (BRAMs), 2520 DSP slices, analog-to-digital converter (XADC), integrated PCI Express communication block, and so on. Traditional VHDL programming is time-consuming while advanced algorithms in applications became increasingly sophisticated. With the help of Vivado High-Level Synthesis developed by Xilinx<sup>®</sup>, the programmer can utilize C, C++, and System C code to target the PL directly.

##### B. Hardware and Software Codesign

System-level circuit simulation is applied inside the PL to accelerate the computation speed. The calculation of the system-level circuit can be considered as matrix operations primarily, which can be accelerated and paralleled by PL (hardware design).

Device-level transients and system control are calculated in the PS (software design). The computation of system control is applied inside the real-time core Cortex<sup>®</sup>-R5 operating at 600 MHz. In each leg of the three-phase MMC and the single-phase MMC, one submodule is selected as the device-level transient calculation in each Cortex<sup>®</sup>-A53 respectfully. In a small-scale circuit, the simulation is highly sequential and not beneficial to be separated into multicore operation due to high latency in core-core communication. With enough high operating frequency, a single core can be optimum for small-scale circuit simulation such as the submodule in the MMC.

TABLE II

RESOURCE CONSUMPTION FOR MMC-BASED TRACTION POWER SYSTEM

Device	BRAM	DSP	FF	LUT
XCZU9EG	56 (3%)	908 (36%)	180895 (33%)	200167 (73%)

In each system-level time step, the system control signal generated from the Cortex<sup>®</sup>-R5 will be transmitted to the PL for system-level simulation and Cortex<sup>®</sup>-A53 for device-level simulation. Meanwhile, the PL updates the history terms to the quad-core Cortex<sup>®</sup>-A53 processor, which, in turn, updates the result to PL in the next time step.

## V. REAL-TIME SIMULATION RESULTS AND DISCUSSION

### A. Computing Hardware Resource Consumption and Computation Performance

In this section, the resource consumption and computation performance are explained in detail. The resource consumption is focused on the FPGA hardware resource allocation. FPGA hardware resource consists of BRAMs, DSP slices, flip-flops, and LUTs. Whether the simulation system can be fitted into the hardware is depended on the highest percentage usage hardware resource. In this case, equal allocation of each type of hardware resource makes a difference in resizing the simulation system scale. Computation performance is focused on the execution speed of PS. If the execution speed of the specific function is running faster than the real-time timing requirement, it can be considered as a real-time application.

Table II illustrates the PL resource consumption for the MMC-based traction power system. LUTs consumption percentage is the highest among all the other resources, up to 73%, followed by DSP (36%), flip-flops (33%), and BRAM (3%). The FPGA resource has been utilized for hardware computation acceleration. For example, large-scale matrix operation can be parallelized for execution in Electromagnetic Transients Program application. Since hardware resource applies low operating frequency in execution, slow processes, such as the thermal calculation, can also be calculated by applying FPGA hardware resource. In this case, high operating frequency cores can be allocated to highly sequential and time-consuming task.

Table III explains the latencies of each processing core. Each A53 Core is utilized to simulate the submodule device-level transients, and the resolution of the hardware timer is 10 ns. In that case, each core has an identical latency of execution (90 ns) and exchanges the history terms to the PL in the next system-level time step. The two most common control methods are phase-shifted carrier-based pulse width modulation (PSC-PWM) and phase-disposition PWM (PD-PWM). Both methods have their advantages and disadvantages. However, based on the requirements of the real-time implementation, the consumption of the hardware resource for the control system is the most important criteria for selecting the control method for the MMC. PSC-PWM requires averaging control and balancing control on every submodule. For a small-scale (low number of levels) MMC topology,

TABLE III

LATENCIES OF SUBMODULE DEVICE-LEVEL TRANSIENTS SIMULATION AND CONTROL SYSTEM

A53 Core 1	A53 Core 2	A53 Core 3	A53 Core 4	R5 Core 1
O3	O3	O3	O3	O3
1.2GHz	1.2GHz	1.2GHz	1.2GHz	0.6GHz
90 ns	90 ns	90 ns	90 ns	7290 ns

TABLE IV

LATENCIES OF HARDWARE RESOURCE AND COMMUNICATION

PL HLS 100MHz	R5 Core 1 - A53 Core X	R5 Core 1 - PL	Maximum delay per time-step	Averaged delay per time-step
22.24 $\mu$ s	120ns	1840ns	24.6 $\mu$ s	24.2 $\mu$ s

PSC-PWM does not require much hardware resources for real-time implementation. But for the scale of the study case in this paper, PD-PWM has a great advantage over PSC-PWM. The real-time Cortex<sup>®</sup>-R5 Core has been used for system control calculation, including PD-PWM and dc-link voltage balancing. Cortex<sup>®</sup>-A53 is operating at 1.2 GHz, and its code inside the MPSoC applied the highest optimization level (O3) of NEON parallel compute capability. Cortex<sup>®</sup>-R5 operates at 0.6 GHz and also utilizes NEON O3 optimization capability. The system-level time step is 25  $\mu$ s, and the execution time of the control system is 7.290  $\mu$ s, which is less than the system-level time-step requirement. The maximum latencies of the cores, calculating device-level electrothermal models, are 90 ns, which is lower than the device-level time step of 100 ns. The communication latency is also an essential factor of the real-time implementation, which will be described in Table IV.

Table IV shows the latencies of hardware system-level calculation with submodule thermal behavioral and communication. The system-level simulation time step is 25  $\mu$ s. The averaged calculation and communication delay per time step is 24.2  $\mu$ s, which is lower than the system-level simulation time step. The PL takes 22.24  $\mu$ s to compute the system-level results while the sent and receive communication time of Cortex<sup>®</sup>-R5 Core to Cortex<sup>®</sup>-A53 Core and Cortex<sup>®</sup>-R5 Core to PL are 120 and 1840 ns, respectively.

### B. Real-Time Experimental Results

Fig. 13(a)–(c) shows the MMC terminal and source voltages. Fast Fourier transform (FFT) has been used to analyze the high-frequency harmonic impact on the system. The three-phase and single-phase MMC terminal voltages show 17 levels of voltage difference. It is not obvious to observe the stepped voltage difference in the three-phase MMC source voltage because of the resistance and inductance interconnection between the terminal and the source point. From Fig. 13(d)–(f), the most observable high harmonic frequency is about 3000 Hz, and its amplitude can be negligible compared with the one at 60 Hz. The 3000-Hz high-frequency harmonic is introduced by the carrier wave in the control system. Fig. 13(g)–(i) gives the upper arm current of the three-phase MMC. This paper separates the full circuit topology  $12 \times 12$  admittance matrix into two small  $6 \times 6$  admittance

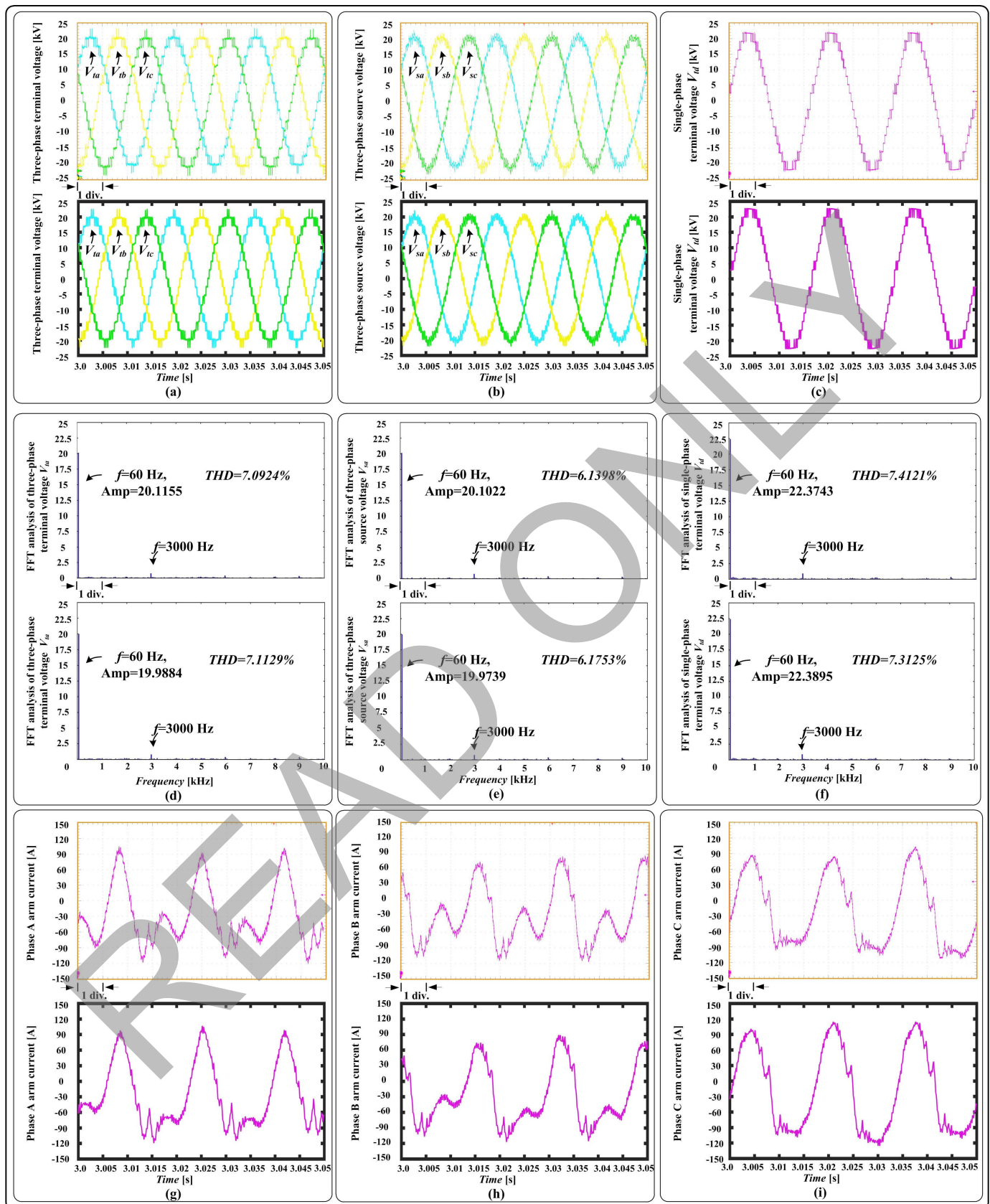


Fig. 13. System-level results for the MMC-based MVDC traction power system from real-time simulation (top oscilloscope subfigure) and off-line simulation by PSCAD/EMTDC<sup>®</sup> software (bottom subfigure) for (a) three-phase terminal voltage, (b) three-phase source voltage, (c) single-phase terminal voltage, (d) FFT analysis of three-phase terminal voltage, (e) FFT analysis of three-phase source voltage, (f) FFT analysis of single-phase terminal voltage, (g) phase A arm current, (h) phase B arm current, and (i) phase C arm current. Scale: (a)-(c), (g)-(i) x-axis: 5 ms/div. (d)-(f) x-axis: 1 kHz/div.

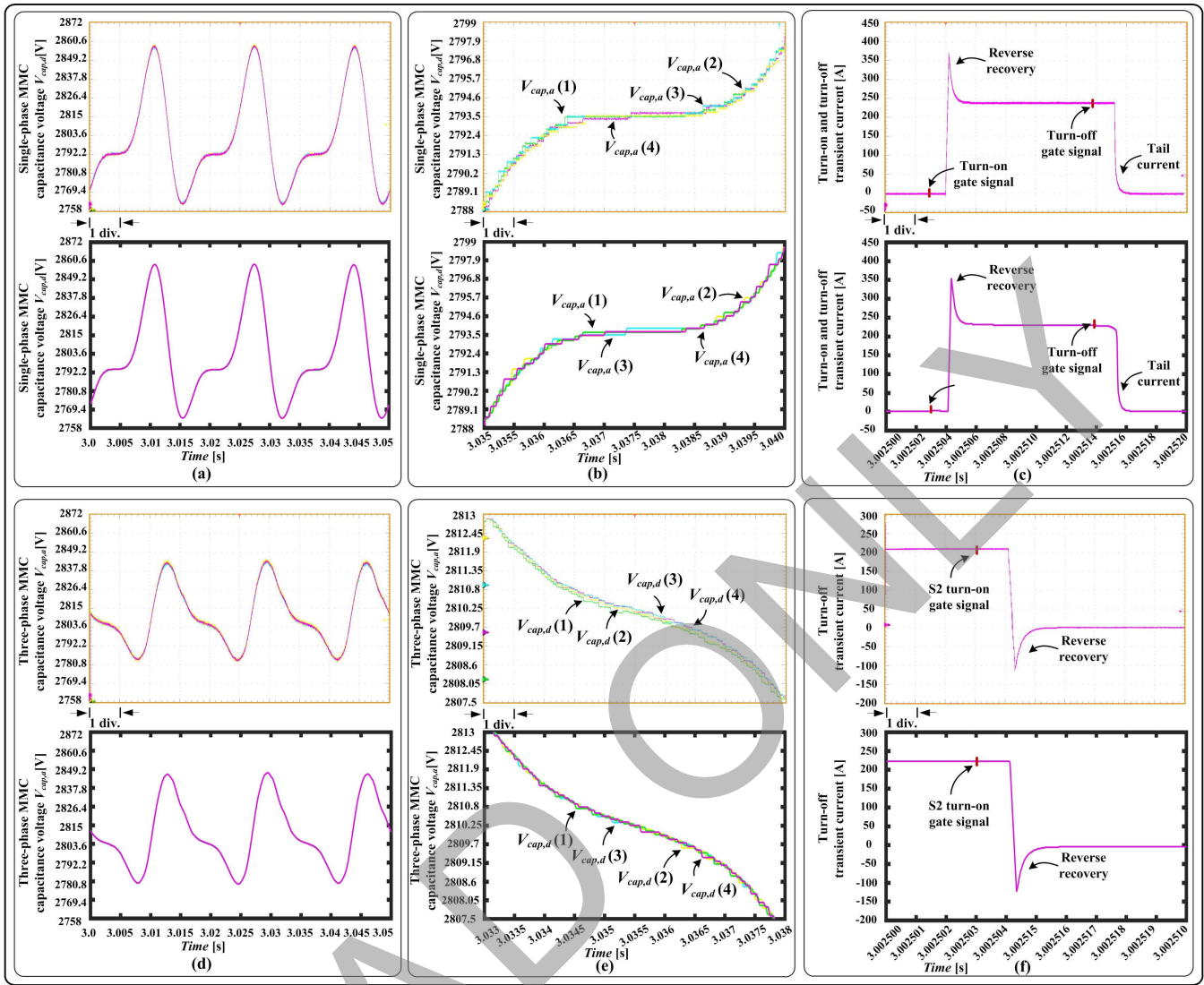


Fig. 14. System-level and device-level results for MMC-based MVDC traction power system from real-time simulation (top oscilloscope sub-figure) and off-line simulation by PSCAD/EMTDC® or SaberRD® software (bottom sub-figure) for: (a) Single-phase MMC capacitance voltage, (b) Zoomed-in singlephase MMC capacitance voltage, (c) Turn-ON and turn-OFF transient current for IGBT, (d) Three-phase MMC capacitance voltage, (e) Zoomed-in three-phase MMC capacitance voltage, (f) Turn-OFF transient current for diode. Scale: (a) and (d) x-axis: 5 ms/div. (b) and (e) x-axis: 0.5 ms/div. (c) x-axis: 2 μs/div. (f) x-axis: 1 μs/div.

matrices to accelerate the simulation speed by applying the transmission line modeling (TLM) method. Although the TLM may introduce small average error within 2% in the matrix calculation, the execution time makes the real-time simulation possible, especially on the occasion requiring Newton–Raphson method.

The capacitance voltages of the MMC submodule are shown Fig. 14. Four of the single-phase MMC capacitor voltages and zoomed-in figures are shown in Fig. 14(a) and Fig. 14(b), respectively.  $V_{cap,a}$  varies from 2758 to 2860 V. Four of the phase A capacitance voltage  $V_{cap,a}$  from the three-phase MMC are shown in Fig. 14(d), and Fig. 14(e) is the zoomed-in figure. The range of  $V_{cap,a}$  is between 2780 and 2849 V, and the voltage value between different capacitances varies within a small range. The variation percentage of capacitance in the three-phase MMC is 2.4%, while the one in the single-phase MMC is 3.5%. For the selected time window, the control system and the traction MMC system became stable, which is

suitable for capacitance voltage value comparison on single-phase and three-phase MMC. Fig. 14(c) shows the IGBT S2 turn-ON and turn-OFF transients. When the turn-ON gate signal is generated, the front linear dynamic block in the Wiener–Hammerstein configuration begins the calculation of carrier charge process. Once the gate-emitter capacitor inside the IGBT is charged to the turn-ON threshold voltage, the front linear dynamic block triggers the linear static block and the back linear dynamic block. The linear static block calculates the device conductance and VCCS value in the static state. The back linear dynamic block estimates the transient period by the first-order delay calculation. At the turn-ON stage, the collector current ramps up with the overshoot phenomenon, which is mainly introduced by the reverse recovery phenomenon by the diode D1, as shown in Fig. 14(f). When the turn-OFF gate signal is generated, the front linear dynamic block calculates the capacitor discharge status. Once the gate-emitter capacitor discharge voltage drops to the turn-OFF threshold

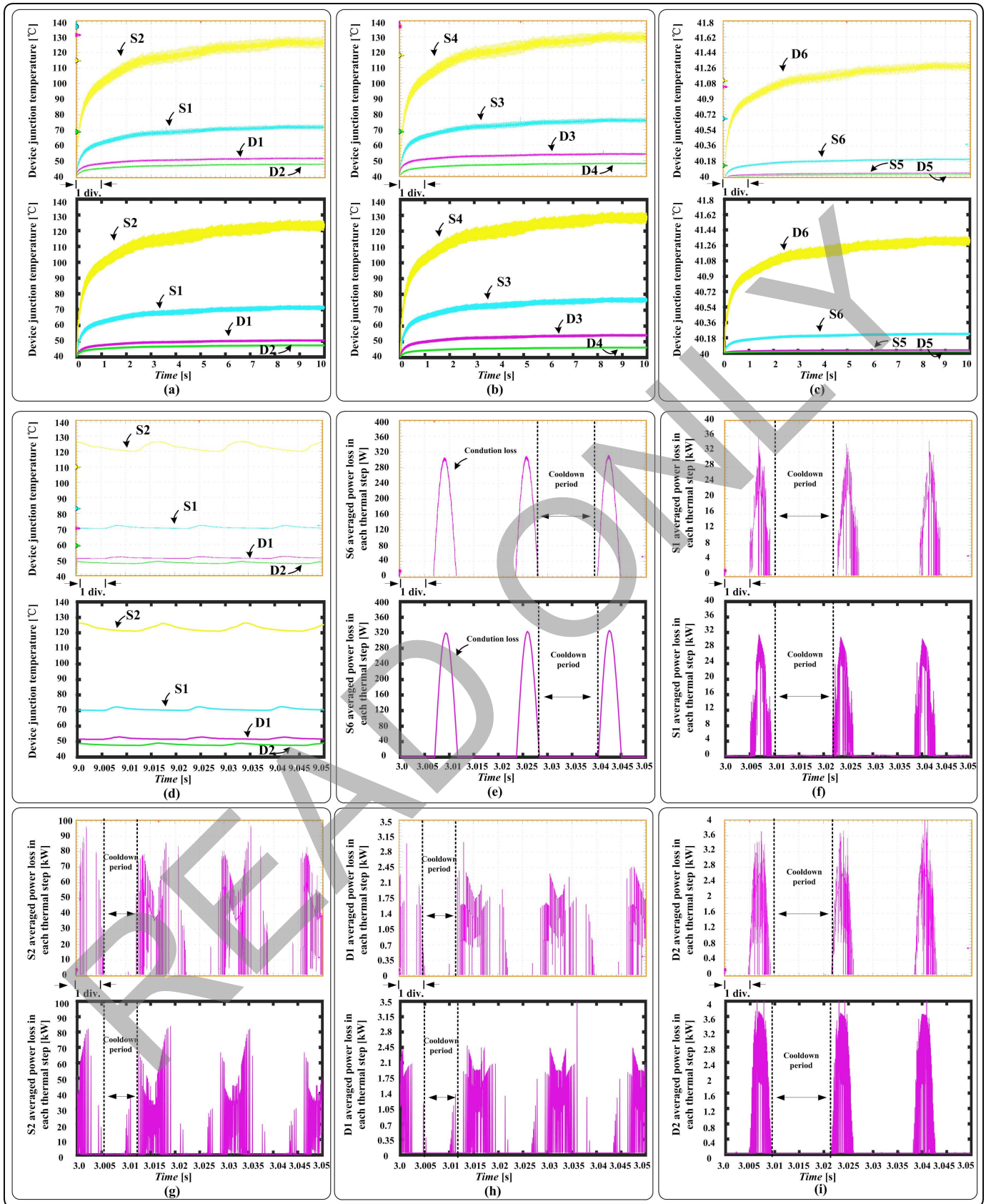


Fig. 15. System-level and device-level results for the MMC-based MVDC traction power system from real-time simulation (top oscilloscope subfigure) and off-line simulation by PSCAD/EMTDC<sup>®</sup> or SaberRD<sup>®</sup> software (bottom subfigure) for (a) S1, S2, D1, and D2 junction temperature, (b) S3, S4, D3, and D4 junction temperature, (c) S5, S6, D5, and D6 junction temperature, (d) zoomed-in S1, S2, D1, and D2 junction temperature, (e) S6 averaged power loss in each thermal time step, (f) S1 averaged power loss in each thermal time step, (g) S2 averaged power loss in each thermal time step, (h) D1 averaged power loss in each thermal time step, and (i) D2 averaged power loss in each thermal time step. Scale: (a)–(c) x-axis: 1 s/div. (d)–(i) x-axis: 5 ms/div.

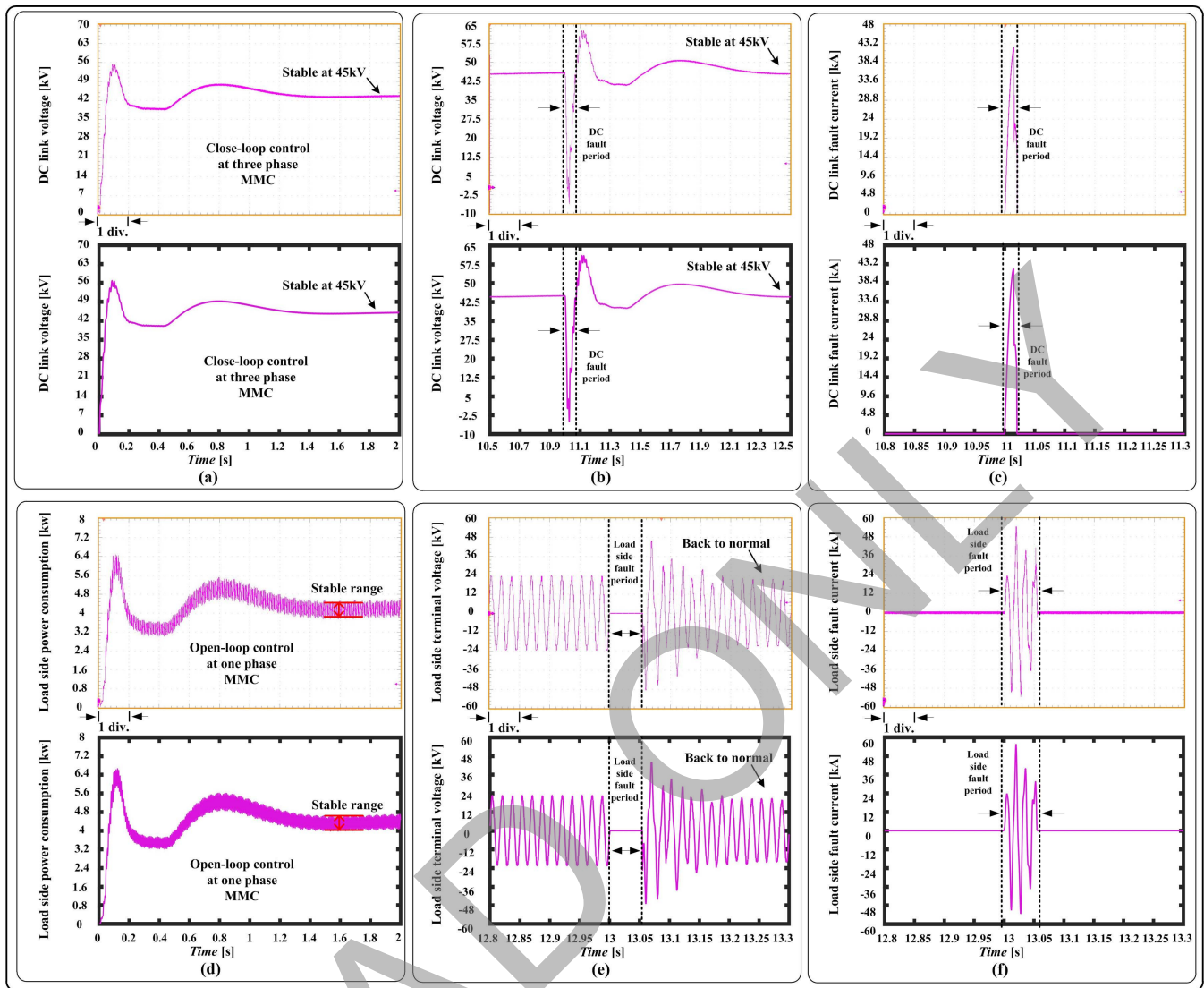


Fig. 16. System-level results for the MMC-based MVDC traction power system from real-time simulation (top oscilloscope subfigure) and off-line simulation by PSCAD/EMTDC<sup>®</sup> software (bottom subfigure) for (a) dc-link voltage on startup stage, (b) dc-link voltage under dc fault condition, (c) dc-link fault current, (d) load-side power consumption, (e) load-side terminal voltage under load-side fault condition, and (f) load-side fault current. Scale: (a)-(b), (d) x-axis: 0.2 s/div. (c), (e)-(f) x-axis: 50 ms/div.

voltage, the linear static block and the back linear block are triggered, and the static state and the tail current shape can be determined.

Fig. 15(a)–(d) shows the device junction temperature within 10 s and zoomed-in figures from 9.0 to 9.05 s, and Fig. 15(e)–(i) shows the device average power loss in each thermal time step from 3.0 to 3.05 s. The time period with no power loss or less power loss will introduce temperature cooldown in the specific device. The IGBT S1 works with the diode D2 in the submodule, while the IGBT S2 works with the diode D1. From Fig. 15(a), S1 and D2 start and end the switch power loss period at the same time, while S2 and D1 have the same scenario. S1 power loss in each thermal time step peaks at around 32 kW, and D2 peaks at about 3.4 kW. S2 power loss in each thermal time step peaks at around 90 kW, and D1 peaks at about 2.45 kW. The IGBTs consume at least eight times the power loss than the diodes in the submodule. From Fig. 15, IGBT S1 and S2 operate at much higher temperature than the diodes D1 and D2. In general, the amplitude variation of the

average power loss is related to the temperature variation, and the thermal accumulation process is highly related to time. To present the sinusoidal voltage waveform based on PD-PWM in this paper, the submodule capacitor voltage has to be cut out by conducting the lower device S2 and S4 by more than 50% of the operating time [53]. With more conducting time of the lower device, the lower device generates more conduction losses which resulted in device temperature rise, and the resistance of the device increased which resulted in more conduction losses. The temperature rise of the lower device also leads to higher switching losses.

In Fig. 16(a) and (d), dc-link voltage closed-loop control and load-side power consumption open-loop control results are shown during the 2 s of startup. The close-loop control objective of the three-phase MMC is to maintain the dc-link voltage stable at 45 kV. The open-loop control of the single-phase MMC helps the load operate at the rated condition, while the *R-L* load power consumption varies at the stable range. A dc-link fault is simulated at 11 s, and the link voltage

and fault current are shown in Fig. 16(b) and (c). At 12.5 s, the dc-link voltage runs back to 45 kV. The load-side fault happened at 13 s, and the load-side terminal voltage and fault current are shown in Fig. 16(e) and (f). At 13.5 s, the load-side terminal goes back to normal condition.

## VI. CONCLUSION

This paper proposed the Wiener–Hammerstein configuration-based device-level electrothermal model for power electronic components, which is demonstrated with a three-phase to single-phase MMC-based traction power system in real-time simulation on the MPSoC platform. The MMC submodule device-level transients are simulated in the Cortex<sup>®</sup>-A53 Core with the latency of 90 ns, and the three-phase to the single-phase MMC-based traction power system is simulated on the PL (FPGA) with the latency of 24.2  $\mu$ s. Both system-level and device-level results have been validated by the professional power system software PSCAD/EMTDC<sup>®</sup> and the power electronic simulation software SaberRD<sup>®</sup>. The modeling procedure of the Wiener–Hammerstein configuration has added the carrier charge process feature, which is based on physical processes and calculated by the first-order delay function. The timing of turn-ON and turn-OFF carrier charging has been indicated, and the equivalent circuit has been utilized for the dynamic calculation. The improved modeling of the static model and the first-order delay dynamic model gives the precise tailing current and reverse recovery waveform based on physical processes. The system-level closed-loop results show that the dc-link voltage has been maintained at the dedicated voltage and it meets the requirement of the system control. The system open-loop results indicate that the  $R$ – $L$  load is operated at the rated condition. The proposed device-level modules and real-time simulation enable a detailed evaluation of complex MVDC traction systems and controls with a low-cost and flexible hardware and software platform.

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