University of Alberta

Silicon Hybrid Plasmonic Waveguides and Passive Devices

by

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Abstract

The field of plasmonics has offered the promise to combine electronics and photonics at the nanometer scale for ultrafast information processing speeds and compact integration of devices. Various plasmonic waveguide schemes were proposed with the potential to achieve switching functionalities and densely integrated circuits using optical signals instead of electrons. Among these, the hybrid plasmonic waveguide stands out thanks to two sought-out properties: long propagation lengths and strong modal confinement. In this work, hybrid plasmonic waveguides and passive devices were theoretically investigated and experimentally demonstrated on an integrated silicon platform. A thin SiO_2 gap between a gold conductive layer and a silicon core provides subwavelength confinement of light inside the gap. A long propagation length of 40μm was experimentally measured. A system of taper coupler connects the plasmonic waveguide to conventional photonic waveguides at a high efficiency of 80%. Passive devices were also fabricated and characterized, including S-bends and Y-splitters.

Acknowledgements

I want to offer my deepest thanks to my supervisor, Vien Van, for his constant supervision, guidance and support in this project. He was the one who told me to look deeper in the subject and found a precious gem on which to work on. My thanks also go to Zhanghua Han for contributing to this project not only with the results of his own FDTD code but also with discussions in the topic of plasmonics and collaborative work in the nanofabrication facility. Many thanks are also due to my co-workers in the Nanophotonics Research Laboratory. Wise counsel has always come out of the mouth of my good friend Ashok Prabhu Masilamani. Special thanks are given to David Perron for sitting at my right hand side all this time and for our work in nonlinear thermal effects in SU-8 plasmonic waveguides. My appreciation also goes to Alan Tsay, Siamak Abdhullahi, Ken Lie, Rice Mi, Cameron Horvath and Daniel Bachman for good times spent together in the laboratory these past 3 years. To the staff and co-workers in the nanofabrication facility, I am grateful to Steve Buswell, Scott Munro, Eric Flaim, Les Schowalter, Jolene Chorzempa and Stephanie Bozic for their training and their support with the fabrication nanotools.

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List of abbreviations

CMOS	Complementary Metal-oxide-semiconductor
SPP	Surface plasmon polariton
FOM	Figure of merit
CGS	Conductor-gap-silicon
CGD	Conductor-gap-dielectric
IM	Insulator-metal
MIM	Metal-insulator-metal
DLSPP	Dielectric-loaded surface plasmon polariton
LRSPP	Long-range surface plasmon polariton
CPP	Channel plasmon polariton
NSOM	Near-field Scanning Optical Microscopy
TEM/TE/TM	Transverse electromagnetic/electric/magnetic
FVFD	Full vectorial finite difference
FDTD	Finite difference time domain
FEM	Finite element method
SOI	Silicon-on-insulator
PMMA	PolyMethylMethAcrylate
EBL	Electron beam lithography
SEM	Scanning electron microscope
I/O	Input/output
PECVD	Plasma enhanced chemical vapor deposition
ICPRIE	Inductively coupled plasma reactive ion etching
MIBK/IPA	Methyl IsoButyl Ketone/Isopropyl alcohol

List of symbols

ε	dielectric constant
ω	angular frequency (in rad/s); subscript "p" denotes plasma frequency
n	real part of the refractive index
κ	imaginary part of the refractive index
β	propagation constant
k_0	angular wavenumber
λ	wavelength; subscript "0" denotes free-space wavelength
γ	damping factor
I	intensity; subscript "0" denotes initial intensity
z	direction of propagation
L_p	propagation length
M_1^{2D}	figure of merit
A_e	effective area
α_z	attenuation coefficient or loss in the direction of propagation
h	height; subscripts denote the corresponding material
w	width
E_y	electric field component in the y-direction
P	power; subscript "0" denotes initial power, "in" denotes power at input
α	coupling coefficient

Introduction

As semiconductor electronic components, circuits and devices continue to miniaturize with transistors in microprocessors reaching down to tens of nanometers in gate lengths, today's information processing systems are facing speed limitations due to signal delay, interference and high power consumption. On the other hand, large amounts of data are transferred in optical fiber cables across database centers and networks around the world at nearly the speed of light. Recently there has been a push to put electronics and photonics on the same scale. For example, a new technology developed by Intel® called Thunderbolt™ will allow large bandwidth data transfer between computer and peripherals [1]. However, the optical signal still requires conversion into electrical signal at the board level. Beyond this, at the chip level, the integration and miniaturization of optical devices falls short comparatively to modern electronic on-chip devices and their ease of fabrication using semiconductor technologies. The scaling down of photonic components is hampered by the diffraction limit of light whereas the minimum dimension is limited to half the wavelength of light.

In the past decade, the field of plasmonics has been touted as the bridge between electronics and photonics. The potential to join together the advantages of these two fields has spurred research for chip-scale integration of photonic components at the nanometer scale [2]. By exploiting surface waves at the boundary of dielectric and metallic materials, an optical signal can be confined into dimensions smaller than the diffraction limit [3]. A circuit using plasmonic components will be able to convert and concentrate incoming light into these surface waves at the same frequency but smaller dimensions, providing guidance and processing it at fast speeds in a very compact space [4,5]. Plasmonics is thus a promising technology that will potentially allow the development of smaller and faster transistors and logic elements with the ability to be highly integrated on a single microprocessor chip [6,7]. Aside for the modulation capacity of these devices, the plasmonic transistor must also be compatible with CMOS manufacturing techniques universally employed in industry today [8]. Thus, semiconductor materials with particular optical properties and ease of fabrication are desirable. Research in these various directions is now generating solutions to the electronic speed bottleneck and the size limitation of photonics. Plasmonics is moving information processing to the next level of ever faster and smaller devices.

Plasmonic components include sources, detectors, interconnects and modulators. The most basic element in integrated optics is the waveguide. A common complication in most plasmonic waveguide structures is the trade-off between the propagation length of the signal and the confinement area of light. Ohmic losses from the metal layer naturally lead to a reduction of propagation distance of an electromagnetic field. However, the more the field interacts with the metal, the larger the losses. This occurs in small areas where light is strongly confined in the plasmonic waveguide.

In this thesis, a new class of plasmonic waveguides is explored and experimentally investigated. Our hybrid plasmonic waveguide offers long propagation lengths (40μm) and mode confinement below the diffraction limit.

This is made possible due to the gap mode that arises in a low index SiO_2 layer sandwiched between a gold metal layer and a high index silicon rectangular core. We also demonstrate monolithic integration of plasmonic and photonic devices on the same chip by using a system of taper couplers with 80% efficiency. Fabricated passive devices are also presented to serve as building blocks for more advanced plasmonic circuitry.

Silicon, the material chosen as the platform for our devices, is chosen for its unique optical properties. First, the high index contrast between silicon, silicon dioxide and air facilitates the confinement of the mode inside the waveguide thus making their dimensions small. Second, integration with silicon photonics enables access to a well-researched field of optical interconnects and modulators as well as the vast knowledge in CMOS fabrication [9]. Finally, silicon exhibits nonlinear properties due to two-photon absorption inducing free-carrier dispersion that can be exploited for ultrafast all-optical switching [10,11].

This work provides theoretical analysis and experimental characterization of silicon plasmonic waveguides and devices which can serve as basis for a plasmonic transistor and other components. Their compact size along with on-chip functionalities will usher the prospect of silicon plasmonic integrated circuits. Ultrafast all-optical processing of large bandwidths of information will then enable the next generation of computing technologies.

Chapter 1: Literature review

This section will present a brief literature review of the field of plasmonics with a larger focus on the subject of this thesis. With the background history and past research developments, one can better understand recent breakthroughs when compared against a backdrop of other results. The possibilities and potentials of plasmonics will also be presented as many have dreamed up new proposals and applications. Below is a brief introduction of the theory of the quasi-particles that are of interest in the field of plasmonics: surface plasmon polaritons.

1.1 Brief theory of surface plasmon polaritons

Surface plasmons polaritons (SPP's) are surface electromagnetic modes that propagate at the interface of a dielectric with real electric permittivity ε_1 and a metal with permittivity $\varepsilon_2(\omega)<0$ as shown in fig.1.

Figure 1. Metal-dielectric interface with direction of propagation in the z-axis and transverse vertical direction in the y-axis. Picture taken from [12].

The permittivity can be generally defined as follows:

$$\varepsilon = \varepsilon' + i\varepsilon'' \tag{1}$$

where ε' is the real part and ε'' is the imaginary part. Also note that $\varepsilon' = n^2 - \kappa^2$ and $\varepsilon'' = 2n\kappa$ where n and κ are the real and imaginary parts of the refractive index of the material. Using Maxwell's equations and the appropriate boundary conditions at the metal-insulator interface, one can arrive at the following dispersion relation:

$$\beta = k_0 \sqrt{\frac{\varepsilon_1 \varepsilon_2}{\varepsilon_1 + \varepsilon_2}} \tag{2}$$

where β is the propagation constant and $k_0 = 2\pi/\lambda$. Another condition for surface plasmon propagation is $|\text{real } \varepsilon'_2| > |\text{real } \varepsilon'_1|$, which is usually the case since metals have highly negative values for ε'. This constant is given by the Drude model for real metals including the plasma frequency ω_p and its damping factor γ:

$$\varepsilon_2(\omega) = 1 - \frac{\omega_p^2}{\omega(\omega + i\gamma)} \tag{3}$$

Gold and silver are common metals used in plasmonic devices due to their relatively low loss at near-infrared and visible wavelengths. Aluminum is also quite often used.

One important measurement in plasmonic waveguides is the propagation length of a supported guided mode. In order to correlate this quantity with experimental measurements, one can extract the propagation length L_p from the intensity I of the field:

$$I = I_0 \, e^{-z/L_p} \tag{4}$$

where z is the direction of propagation. In this way, the propagation distance is the length at which the intensity drops by 1/e. Knowing the distance at which the light propagates or, conversely, the losses that the light experiences, one can better engineer devices and their sizes. From the eigenvalue of the plasmonic mode, the effective index $n_{eff} - \mathrm{j}\cdot\kappa_{eff}$ can be extracted and the propagation distance L_p can thus also be defined as:

$$L_p = \frac{1}{2\beta_{imaginary}} = \frac{\lambda_0}{4\pi\,\kappa_{eff}} \tag{5}$$

where λ_0 is the free-space wavelength of light.

1.2 Waveguiding schemes in plasmonics

As a basic element in integrated photonic circuitry, the waveguide is fundamental in supporting and guiding the propagating light. In plasmonics, the addition of the metal layer opens up a myriad of structural possibilities. During the past decade, many of these schemes have been proposed. Each of them had their own characteristics, applications and explored devices. However, the common theme remains the same: there is a trade-off between the confinement area of the mode and its propagation length. In other words, the smaller the mode size, the more loss is experienced by the propagating field through the structure.

In this section, a few plasmonic waveguide designs will be presented and their properties discussed. In order to qualitatively benchmark the trade-off for each, a figure of merit (FOM) is introduced [13]:

$$M_1^{2D} = \sqrt{\frac{\pi}{A_e}}\frac{1}{\alpha_z} \tag{6}$$

where $\alpha_z = 1/(2L_p)$ is the attenuation constant and A_e is the effective area. The latter is taken as the size of the area occupied by a closed contour delimited at 1/e of the intensity profile relative to the global maximum. The concept of this FOM helps the optimization of various dimensions of a plasmonic waveguide. On the other hand, the dimensionless number obtained does not contain much description about the absolute modal confinement. As such, one might not clearly see if the mode is well confined at a subwavelength scale or not.

Note to the reader: unless explicitly indicated, the results discussed below assume an operating telecom wavelength at 1550nm.

1.2.1 Insulator-metal

The basic setup for a plasmonic waveguide is an insulator-metal (IM) interface as shown in fig.1. This structure supports surface plasmon polaritons at the boundary between the two materials. Inside the metal, the electric field quickly decays while it exponentially decays slowly on the dielectric side. By introducing air cladding on the sides, as shown in fig.2, lateral confinement of the mode facilitates guidance of the traveling mode.

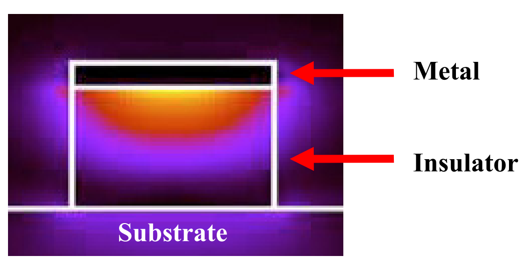

Figure 2. Cross-section of an insulator-metal structure from a numerical simulation of the plasmonic mode. A ridge waveguide core with a width of 300nm and height of 340nm sits on top of a SiO_2 substrate and is capped by a 50nm thick gold metal layer. The plasmonic mode clings to the metal while decaying into the core. The direction of propagation is in or out of the plane. This mode profile picture is taken from [14].

The structure shown here was experimentally tested by [14]. The core of this plasmonic waveguide has dimensions 300nm by 340nm and is made of silicon. It is capped on top by 50nm of gold as the metal layer. Underneath sits a silicon dioxide substrate. In theory and in practice, this fundamental structure has a propagation length around 2μm at a wavelength of 1550nm. By visually inspecting the mode size, the FOM was determined to be $M_1^{2D} \sim 100$. While the mode does not go far in distance, its relatively good confinement allows light to go through bends with just 14.6% loss. Also, the material used in fabrication allows monolithic integration with photonic components.

1.2.2 Dielectric-loaded SPP's

A similar waveguide scheme is the dielectric-loaded waveguide on top of a metallic sheet. By depositing a dielectric on top, the patterning becomes easier for fabrication purposes. Thus, many sizes and shapes can be designed. However, even in this kind of waveguide, the trade-off between propagation loss and confinement applies.

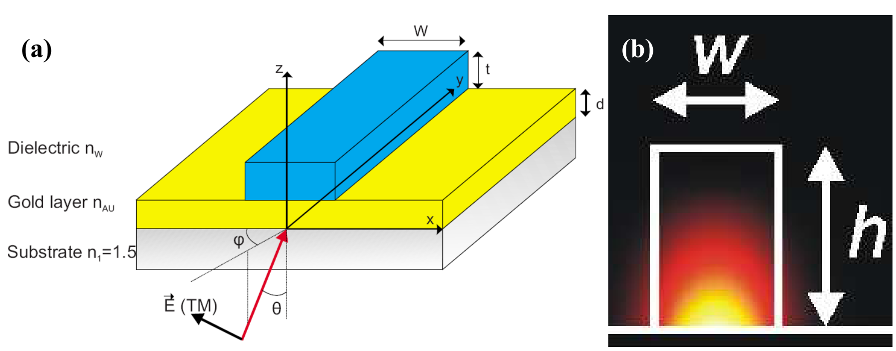

Figure 3. a) Schematic of a dielectric-loaded plasmonic waveguide. A dielectric (blue), with height *h* and width *w*, is deposited on a metal layer (yellow) and supported by a substrate. A TM-polarized wave is launched in order to excite the DLSPP mode shown in b). The pictures are taken from [15] and [16].

Conventionally, low-index polymers are used for the dielectric since only one simple lithography step is required for fabrication of the ridge on top of the metal sheet (illustration in fig.3a). For example, dielectric-loaded waveguides using a common photoresist called PolyMethylMethAcrylate (PMMA) with height h = 330nm and width w = 240nm have been fabricated and measured at a visible wavelength of 780nm [15]. Similarly, thinner SiO_2 waveguides with h = 70nm and variable widths were numerically investigated. Both of these structures have slightly better propagation length for SPP's going from 5µm to 25µm as both the physical dimensions and the mode size increase (fig.3b). The FOM ranges thus from 75 to 400, the higher number corresponding to smaller waveguide width. If sufficient propagation distance is to be maintained, it can be seen that downsizing the waveguide to the subwavelength scale becomes problematic. Even at near-infrared wavelength of 1.55µm, the typical waveguide size is around 600nm by 600nm with propagation length of 43µm and FOM ~ 400 for a polymer ridge on gold layer [17]. The large dimensions and subsequent modal size makes high-density integration much harder to achieve.

A solution to the confinement problem is to use a high-index dielectric. In a numerical simulation, a silicon ridge on aluminum or gold sheet was made as small as 100nm by 150nm though the mode begins to spill out of the core [16]. With a relatively long propagation length of 100µm, the effective area can be in the μm^2 size. On the other hand, upsizing the core size to 200nm by 300nm with modal area as small as $0.03um^2$ gives a propagation length of 5µm which is similar to the IM structure. The FOM for this scheme is 75~250. As we can see, there is effectively a quandary in this trade-off situation.

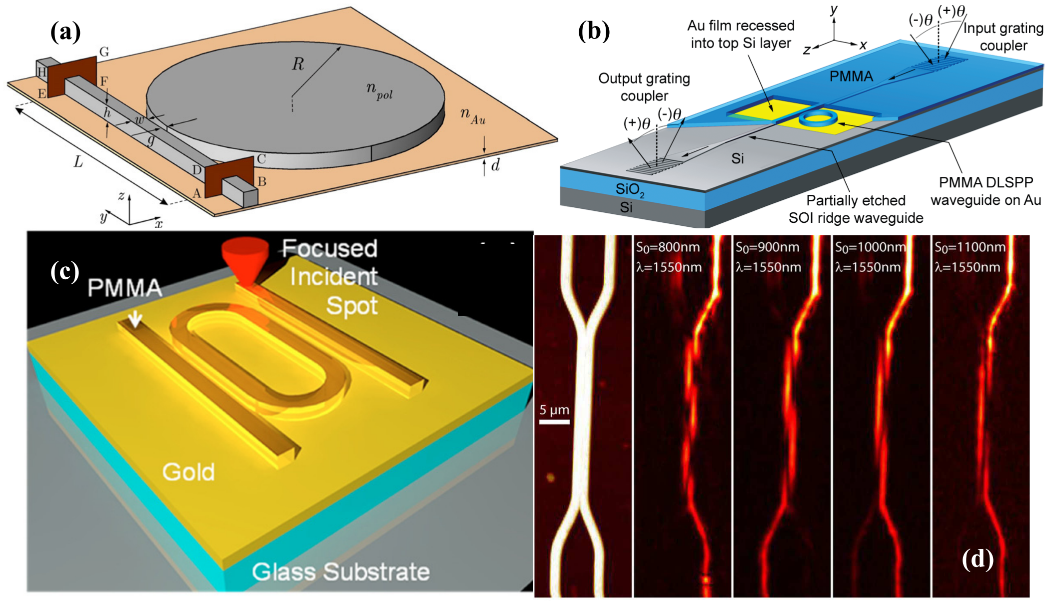

Figure 4. a) Schematic of a microdisk resonator using DLSPP waveguides [18]. b) Microring resonator made of PMMA with DLSPP waveguides coupled to SOI ridge waveguide [19]. c) Racetrack resonator in a add-drop filter configuration [20]. d) NSOM intensity mapping of directional couplers at various separations [21].

Despite the dilemma, dielectric-loaded plasmonic waveguides (DLSPP) have been exploited for their potential in integrated photonics. Their versatility allowed many passive devices to be experimentally fabricated using PMMA as dielectric and standard deep-UV or electron beam lithography for patterning (fig.4). First, bends and splitters set the building blocks for waveguiding [22,23]. Then, directional couplers and microring resonators followed suit along with racetracks, Bragg gratings and a proposed microdisk structure [18-21,24].

In addition, the simplicity of fabrication and the easy access to the waveguide core also gave rise to diverse ways to control the optical signal for active plasmonics. This subject will be discussed in section 1.3.1.

1.2.3 Long-range SPP's

Another scheme exploits surface plasmon polaritons on both sides of a metal strip. The coupling of two SPP modes on each metal-dielectric interface in a symmetric fashion gives rise to the long-range SPP mode (LRSPP) [25]. The mode that is excited in this plasmonic structure lives up to its name. In fact, the LRSPP is able to attain up to millimeters and even centimeters in propagation range.

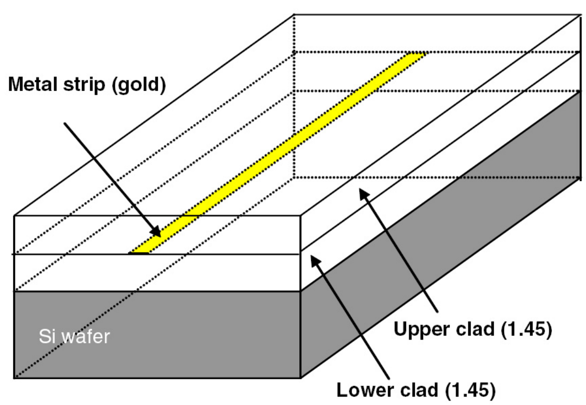

Figure 5. Schematic of a waveguide supporting LRSPPs. A thin and wide metal strip is enclosed in dielectric claddings above and below [26].

The characteristic setup for the LRSPP scheme is a thin metal strip embedded in upper and lower cladding made of the same material in order to preserve the mode symmetry (see fig.5). By choosing a sufficient small strip size, single mode operation can be achieved. Furthermore, one can decrease the metal film thickness and width as the propagation loss of the LRSPP decreases considerably. As a consequence, however, the plasmonic mode tends to turn into a photonic TEM mode, which reduces the confinement and extends its spatial size. This evanescent wave extends many microns into the cladding in all directions. In order to counter this, it is typical to leave one of the lateral dimensions of the strip large enough so as to provide minimum mode confinement in one axis. A common dimensional arrangement is to fix the width to a few microns while varying the thickness in the tens of nanometers. As we can see, the LRSPP shows one of the extremes of the trade-off by having extraordinarily long propagation length but very loose mode confinement. The theoretical and experimental FOM for this structure can be quite high with M_1^{2D} ranging from 1000 to 3000 [13]. This is mostly due to its exceedingly long propagation distance.

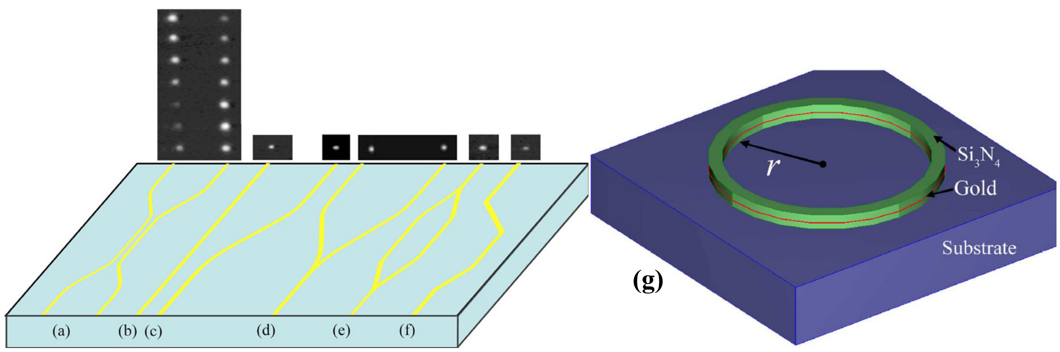

Figure 6. A plethora of LRSPP passive devices. a) Directional coupler; b) Straight waveguide; c) Bend; d) Splitter; e) Mach-Zehnder interferometer; f) Sharp bends; g) Microring resonator. Pictures taken from [25] and [27].

The exceptionally low loss mode in the LRSPP structure has been exploited in optical interconnects. One such experimental application was a 40 Gbps optical data transmission over 4cm using these waveguides [28]. Also, in the same manner as DLSPP's, passive devices were explored both numerically and experimentally. The group led by Berini put forward comprehensive research on LRSPP over the past decade. In addition to full analysis of LRSPP modes, a full array of devices, shown in fig.6a-f, were investigated including bends, splitters, couplers, Mach-Zehnder interferometers and Bragg gratings [25].

However, owing to the low mode confinement and large bending radius, it seems impractical to curve the LRSPP waveguide even more into a compact microring structure. A proposal by [27] combines LRSPP with DLSPP in order to overcome this difficulty. By cladding the LRSPP waveguide with air, improved confinement was achieved while maintaining reasonably long propagation lengths around 300µm. Incidentally, the FOM of this hybrid dielectric-metal-dielectric structure is around $M_1^{2D} \sim 1700$ calculated from a mode diameter of 700nm. An efficient microring with bending radius of 2-10microns is therefore possible as shown in fig.6g.

1.2.4 Metal-insulator-metal

On the other extreme, one can strongly confine the plasmonic mode while forfeiting the propagation length. In this manner, the metal-insulator-metal (MIM) sandwich scheme is the complete opposite of the LRSPP waveguide. The coupling of two SPP's from two metal-dielectric boundaries is the only aspect in common. In the MIM structure, these two SPP's couple into the central dielectric slot and thus gives rise to a huge field concentration. However, due to the close proximity of the mode with both metal layers, the losses are extremely large. A typical value for propagation length is in the few microns as in the IM case. The most noticeable advantage of the MIM mode is its subwavelength size.

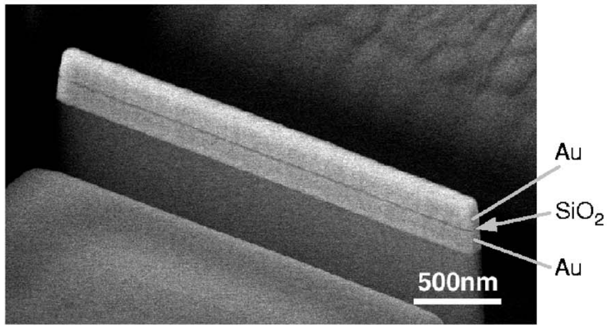

Figure 7. SEM micrograph of a fabricated nanosheet plasmonic cavity in the MIM configuration [29]. A thin nanoscale layer of SiO_2 is embedded between two covers of gold. The modal confinement in such a small area causes great intensity enhancement.

To demonstrate an extreme case, one can make the dielectric slot as small as 3.3nm [29]. This nanoscale thin layer of SiO_2 squeezed in between two gold layers forms a so-called nanosheet plasmonic cavity with an effective modal size around $0.001um^2$, calculated as the total dielectric slot area (fig.7). With a propagation length of only a few hundred nanometers, the experimental FOM is only 23. However, the intensity enhancement realized inside this cavity is 10^3, which is excellent for Raman spectroscopy yet impractical for waveguiding purposes.

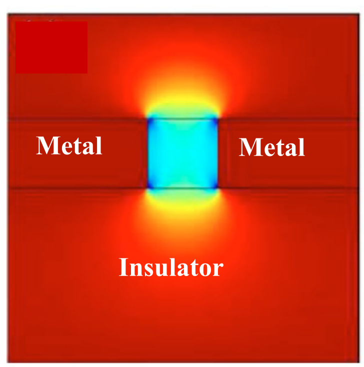

Figure 8. Field intensity profile of a plasmonic mode inside a MIM structure [30]. The mode is strongly confined in the space (PMMA) between the two metal slabs (gold) with finite height. Slightly asymmetric leakage into the top (PMMA, n=1.49) and bottom dielectric (SiO_2, n=1.45) can be observed.

A more representative waveguide dielectric core size is around 200nm by 200nm with propagation lengths around one micron and an experimental FOM ~ 25 [31,32]. If both claddings get index matched with the core, a longer propagation length of 5.56μm and FOM ~ 100 can be obtained (fig.8) [30].

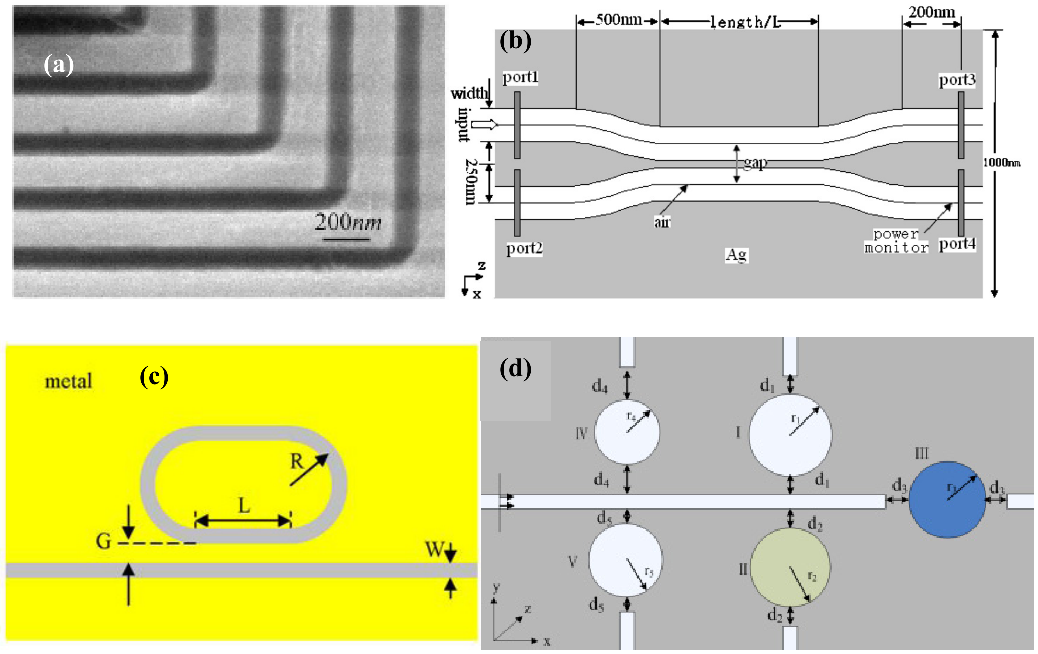

Figure 9. Passive devices using slot waveguides carved in metal layers based on the MIM scheme. a) SEM image of sharp bends [33]; b) Schematic of proposed directional coupler [34]; c) Ultracompact racetrack resonator [35]; d) Demultiplexer system using microdisk resonators [36].

While long propagating waveguide signal does not appear to be viable for MIM waveguides, they are often used for nanoscale devices that exploit the strong mode confinement at its best. Sharp bends even at 90 degrees angle have been experimentally tested (see fig.9a) [33]. Various other applications using subwavelength slots were proposed such as splitters, directional couplers, interferometers, microrings, apertured rings, disks, racetracks and Bragg gratings [34-38].

1.2.5 Channel SPP's

Channel SPP's (CPP) are generated in a structure cousin to the IM scheme in which the metal sheet is patterned with valleys or hills. A popular geometry is the V-groove pattern where a triangular pattern is etched unto the metal layer. The channel that is formed in this way supports SPP's at the bottom tip of the triangle and between the two slopes. This can also be seen as an MIM structure with the bottom side of the slot closed. A simple illustration can be seen in fig.10a.

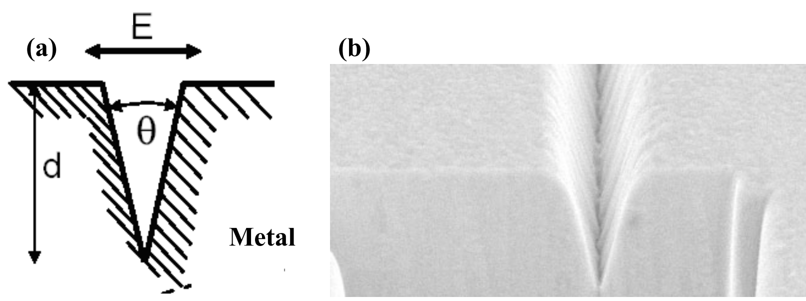

Figure 10. a) Diagram of a CPP-supporting V-groove channel [39]. A triangular trench is etched into the metal sheet at depth d, angle θ and width E. The CPP mode is confined at the bottom of the groove. b) SEM picture of the V-groove fabricated using focused ion beam milling.

The channels that support these SPP's are quite easy to fabricate, either through focused ion beam milling or standard wet etching (fig.10b). Silver and gold are often used for the metal layer. The behaviour of these SPP's resembles those in the MIM structure. Strong confinement, even in air, characterizes them due to the singularity at the tip where the electric field accumulates. A typical V-groove has dimensions around 600nm in width and 1μm in depth [39]. The mode in gold V-grooves propagates about 100μm and is usually fairly contained within the groove with a mode width of a micron. If one assumes the effective mode area to be the area of the triangular groove, the FOM would be around 650. Thus, channel SPP's offer relatively good mode confinement with fairly long propagation distances. In comparison, CPP's have substantially better propagation length than SPP's in MIM structures even though they share both a confined mode between two metal walls.

While channel and wedge SPP structures are relatively easy to make, it is quite tricky to measure. One needs near-field scanning optical microscopy (NSOM) in order to sense the plasmonic field very close above the metal. So far, there are no reports of an integrated coupling scheme for V-grooves.

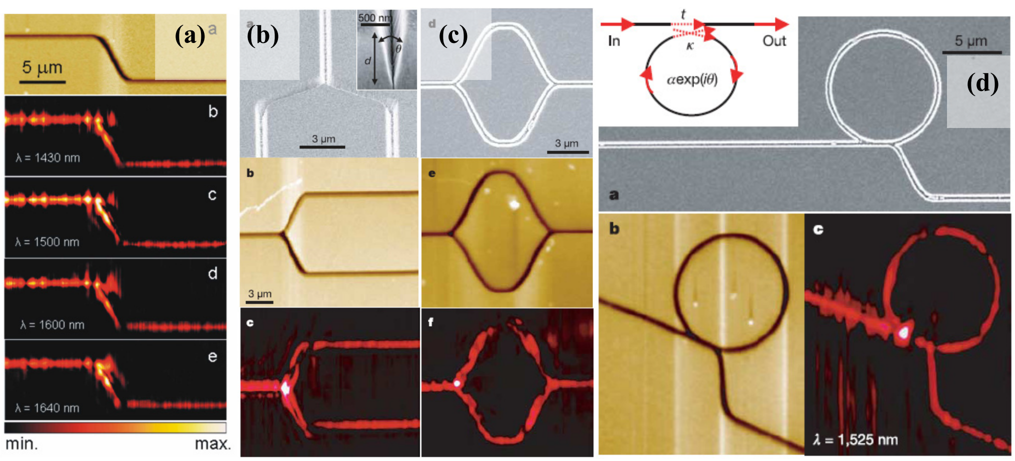

Figure 11. Various passive devices guiding CPPs in a) a bend, b) a splitter, c) Mach-Zehnder interferometer and d) microring resonator. Optical, SEM and NSOM micrographs taken from [40,41].

As for all the plasmonic waveguides encountered, passive devices can be straightforwardly fabricated by milling the desired pattern on a metal substrate. Strong modal confinement allows for very compact bends, splitters, interferometers and rings (see fig.11) [40,41].

1.3 Active plasmonics

The ultimate goal of all these plasmonic devices is to push forward toward fully integrated plasmonic circuitry. To do so, an optical analogue of the electronic transistor is needed. The next step that plasmonic technologies should offer is the development of plasmonic switches with the ability to modulate ultrafast signals at the nanoscale [42]. It combines the compact size of electronics with the high speeds and low power of photonics. With the help of the semiconductor industry, novel active nanoplasmonics devices can see the light of day. In this section, a quick overview of current schemes for active control of SPP's will be presented.

1.3.1 Active components in plasmonics

Since 2004, several active methods for SPP modulation have been both proposed and experimented [43]. The most common technique involves a change of refractive index of the material that supports SPP's in order to induce amplitude or phase change. An on-off switching contrast can then be induced.

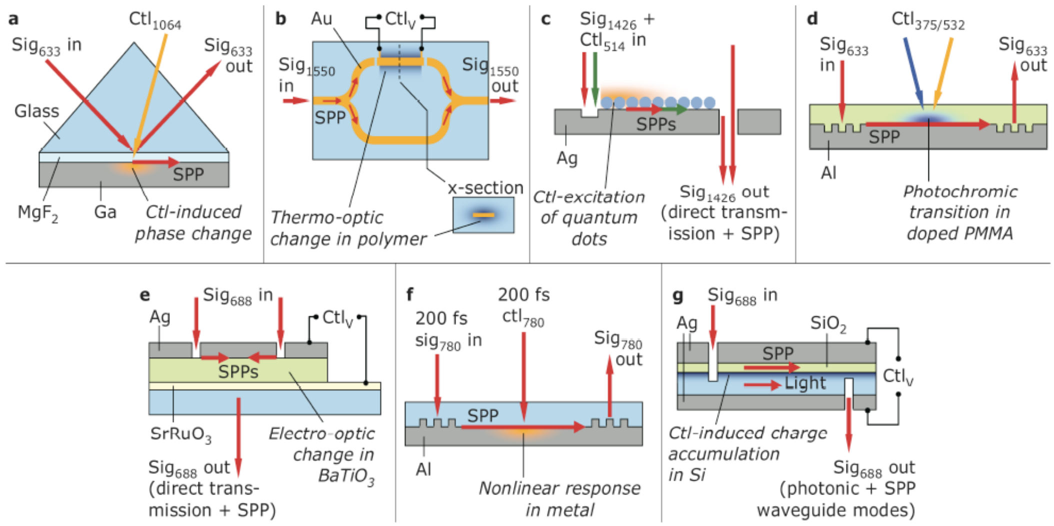

Figure 12. Overview of experimental active plasmonic modulator schemes using: a) light-induced solid-liquid phase transition in gallium metal layer in a prism configuration; b) voltage controlled thermo-optic switching in a LRSPP interferometer; c) CdSe quantum dot gain medium with an activating control signal; d) photochromic switching doped medium in metal-insulator setup; e) electro-optic switching by refractive index change in $BaTiO_3$; f) nonlinear all-optical switching on aluminum sheet; g) switching in silicon by carrier injection. Figure taken from [44].

The refractive index can be changed using many creative methods as displayed in fig.12. Two parameters can be distinctly chosen to produce modulation: the materials used and the external control method. On the material side, the phase transition of the metal or its nonlinear response can be exploited as shown in fig.12a and f. Nonlinearities will be further discussed in the next section. The properties of dielectrics can also be exploited by selecting sensitive materials that respond particularly well to an external signal such as in fig. 12d and e. Furthermore, some have taken advantage of gain media in order to assist SPP propagation or even induce lasing in plasmonic structures [45-47]. The other parameter is the application of an external signal which can be arranged in three categories: thermo-optic, electrical and all-optical switching. The first two can make use of the metal layers in plasmonic devices in order to apply an electric current or voltage. Thermo-optic switching uses the heat generated this way in order to change the refractive index and thus modify the propagated SPP (see fig.12b). It is the slowest method with time constants in the microseconds. In electrical switching, a current alters the charge distribution by injecting carriers and thus the traveling SPP's see a change in electron density (see fig.12g). Both these methods have been commonly employed in LRSPP and DLSPP schemes [25]. Finally, all-optical switching utilizes an external light source (usually a laser beam) to modify the material property and thus affecting the SPP moving through (see fig.12 a, c, d and f). All-optical switching using pulses has the advantage to be extremely fast yet often requires an external source to generate the second signal. This is impractical for integrated plasmonics especially if an out-of-plane setup is required.

1.3.2 Nonlinear plasmonics

The topic of nonlinear plasmonics deserves its own section due to the immense potential it can offer in active plasmonic devices, for example all-optical ultrafast switching. Nonlinearities present in the material open up new channels of control using a pump-probe setup. A plasmonic system contributes to this effect by providing strong field confinement in which light can efficiently interact with the nonlinear material.

In plasmonic waveguides, a nonlinear dielectric would the most common approach. The refractive index of this material is dependent on the strength of the nonlinearity and the pump power. Thus by pumping light into the waveguide, a modulation of the probe signal can occur. This method has been proposed for LRSPP and MIM type plasmonic waveguides via the optical Kerr effect [48,49]. The metal can be exploited for its nonlinear properties as well [50]. As shown in fig.12f, the nonlinear response of a metal can be used for ultrafast switching by a femtosecond pulse [51].

Silicon is one of the most promising nonlinear materials as a plethora of nonlinear optical effects have already been demonstrated in silicon waveguides [11]. This advantage has been carried over to plasmonic waveguides in recent years and is being hailed as a new field of silicon plasmonics [52]. In fact, both theoretical and experimental works have been undertaken with promises of ultrafast switching at low pump powers [53,54]. All in all, nonlinear plasmonics is offering the potential to achieve all-optical high-speed switching in nanoscale waveguides.

1.4. Hybrid plasmonic waveguides

In the past two to three years, a new class of plasmonic waveguide has come into prominence. With the simple introduction of a low index dielectric between the metal layer and the high index dielectric, the propagation length could be increased significantly while keeping a strongly confined mode in the middle layer. There came the hybrid plasmonic waveguide. First coined by [55] in 2008, the term was used for hybrid dielectric-plasmonic “slot” waveguides. Their paper presented an extensive theoretical analysis along with numerical simulations using a silicon/SiO_2/air system (fig.13). A ring resonator filter was also proposed.

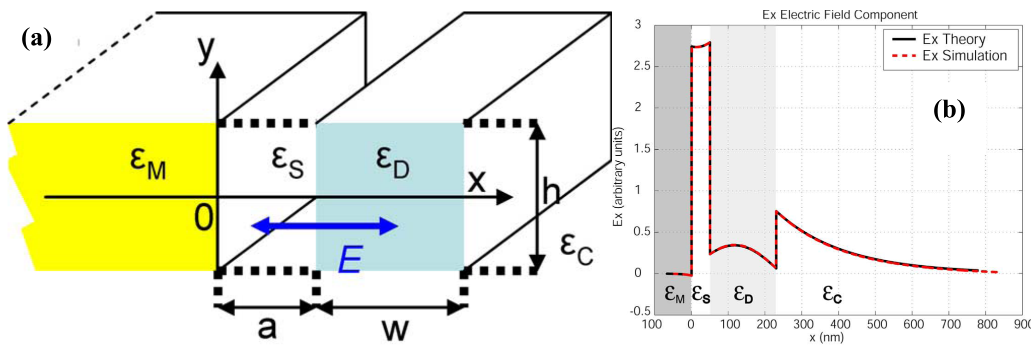

Figure 13. a) Schematic of a hybrid plasmonic waveguide. A low index gap is inserted between the metal (yellow) and the high index dielectric (blue). b) Numerical simulation and analytical result of the electric field distribution across the waveguide as a cut in the x-direction. Strong mode confinement can be observed in the gap. Figures taken from [55].

However, the concept was not completely new as a small number of research groups were testing low index materials in plasmonics. In 2004, plasmonic waveguides were fabricated on semiconductor substrates [56]. Incidentally, a thick 300nm of SiO_2 was added between the InP substrate and the metal strip leading to the observation of a propagation loss decrease in the waveguide. It is not until 2007 that another proposal came up in a conference paper [57]. A novel waveguide geometry was showcased with a low index dielectric spacer in a silicon/SiO_2/metal system. The hybrid mode was called "super mode" due to the coupling of SPP and a dielectric mode in the spacer and in the core, respectively. One can say this proposal was the first pioneer in the topic. Lastly, in early 2008, a group sought to extend the range of LRSPP by adding two low index layers between the metal strip and the high index cladding without sacrificing area confinement [58]. In simulations, ultra-long propagation distances up to 19cm were found along with very high FOM around 10^4.

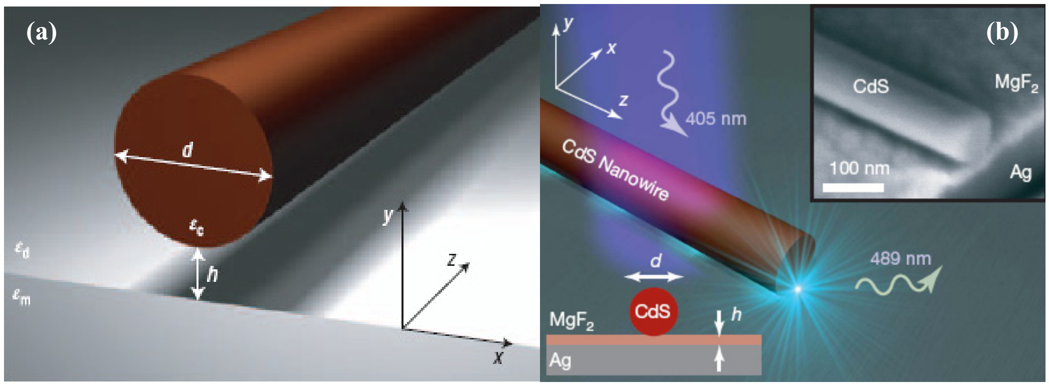

Figure 14. a) Representation of the hybrid plasmonic waveguide proposed by [59]. A semiconductor nanowire is separated from the metal substrate by a thin low index dielectric. b) Same schematic showing optical pumping at 405nm wavelength of a CdS nanowire resting on a MgF_2 thin sheet and a silver substrate [60]. Lasing from plasmons excited in the thin layer occurs at 489nm wavelength. Inset: SEM picture of the fabricated plasmon laser.

The year of 2008 gave more visibility to this novel concept. A paper in Nature Photonics theoretically proposed the use of semiconductor rods separated by a low index gap, see fig.14a [59]. The study showed subwavelength confinement of the mode in the gap while promising long propagation lengths around hundreds of microns at 1550nm wavelength. It was quickly followed by an experimental demonstration of a plasmonic laser (fig. 14b) as well as a color-tuning and switching mechanism both using the same CdS hybrid plasmonic waveguide configuration [60,61]. By optically pumping a 100nm diameter CdS rod sitting on top of a low index 5nm thin MgF_2 layer on a silver substrate, deep subwavelength scale emission via SPP's was achieved at 489nm wavelength. The concept of hybrid plasmonic waveguide was new yet its first active device was already fabricated.

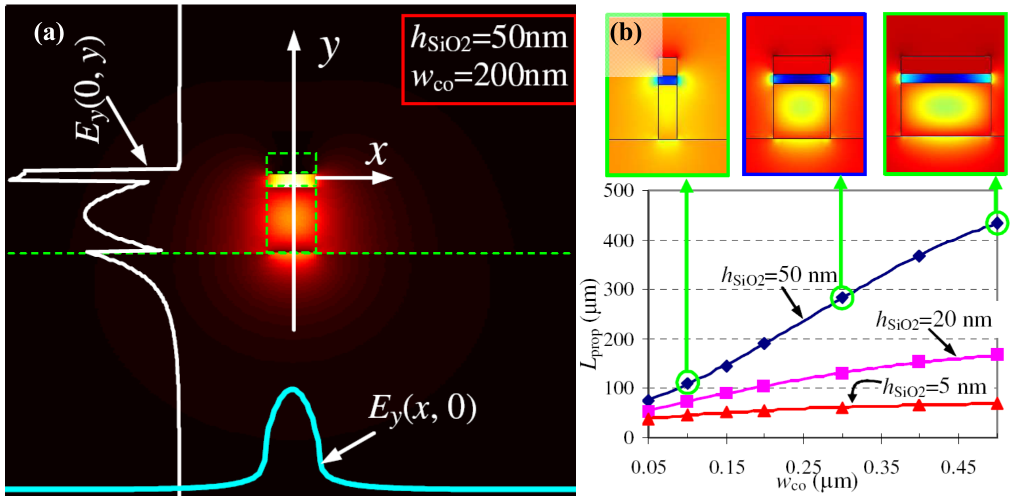

Figure 15. a) Mode profile of the hybrid plasmonic waveguide in the silicon platform as proposed by [62]. The field is well confined inside the SiO_2 gap. The metal used here is silver. b) Chart presenting numerical results for the propagation length at various waveguide widths w_{co} and SiO_2 heights h_{SiO2}. Top insets: shape of the plasmonic mode at different widths. The blue color indicates higher intensity.

The following years saw increased interest in the topic. Many more analytical papers and proposals were published [62-66]. On top of that, even more papers were using the hybrid plasmonic waveguide in microring resonators [67,68]. The next experimental paper was done in early 2010 in which hybrid plasmonic waveguides were fabricated in the LRSPP style [69]. In other words, low index dielectrics were inserted on each side of the metal strip before the outer higher index cladding. In the experiment, polymers were used as dielectrics and propagation lengths were reported in the tens to hundreds of microns.

In all the research done so far, the main advantages that surfaced in hybrid plasmonic waveguides are their long propagation distances and the strong confinement of the mode in the low index dielectric. To some extent, one can say that this new type of plasmonic waveguide is cheating the conventional trade-off of confinement versus propagation length. In fact, since 2010, there has been an explosion of research papers published. A paper focusing on the experimental realization of these waveguides on a silicon material system was published from the results in this thesis and can be seen as part of the huge expansion in this topic [70]. There is an excitement around the promising opportunities unfolded by this class of waveguides. A section will be dedicated to an overview of the latest developments since this paper.

Chapter 2: CGS design, simulations and analysis

The appeal of the hybrid plasmonic waveguide comes from two fronts: low loss or long propagation lengths and strong nanoscale confinement. These two criteria are usually antagonistic to each other as the previous chapter has shown. Thus, it is appealing to build these hybrid plasmonic waveguides since they offer the promise to slightly reconcile these two trade-offs even at subwavelength scales. In 2009, the goal was to experimentally exploit this novel phenomenon on an integrated plasmonic circuit platform using silicon as our material system.

2.1 Design

In order to accomplish this objective, an understanding of the hybrid plasmonic waveguide must be undertaken. A careful investigation of different possibilities was carried out to consider various physical properties and designs. Finally, an optimal structure was selected also according to suitability for fabrication. Our choice fell on a conductor-gap-silicon (CGS) plasmonic waveguide inspired from a similar structure depicted in [62] with the silicon layer completely etched through (see fig.15). The term also reflects the naming of the "conductor-gap-dielectric" (CGD) from [64].

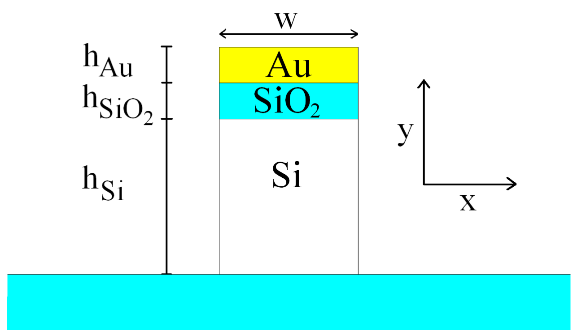

Figure 16. Schematics of the conductor-gap-silicon plasmonic waveguide. A ridge silicon waveguide lays on a substrate and is capped by a gold layer with a SiO_2 gap in between. The plasmonic waveguide has finite width to provide lateral confinement.

The layers Au/SiO_2/Si, pictured in fig.16, were chosen for their properties and advantages they bring. The waveguide gap consists of a thin layer of SiO_2 of thickness h_{SiO2} as the low index material at n = 1.44. It is sandwiched between a gold layer of thickness h_{Au} with dielectric constant ε = -132 – 12.65i at the telecommunication wavelength of 1550nm [71], and a Si layer of thickness h_{Si} with higher index n = 3.48. Silicon was selected for its low cost, its abundance in nature, and our large knowledge in fabrication leading to its ubiquitous use in today's semiconductor industry. Moreover, its nonlinear properties are an asset in both photonic and plasmonic devices as we have previously discussed. The other materials were chosen for their accessibility in our deposition machines. Gold was preferred over silver due to its immunity to oxidation and ease of fabrication. Lateral confinement of the mode is achieved by patterning through the three layers to form a rectangular waveguide of width *w* sitting on a SiO_2 substrate. Restrictions in our lithography process put limitations in the width of our waveguides due to fabrication consistency.

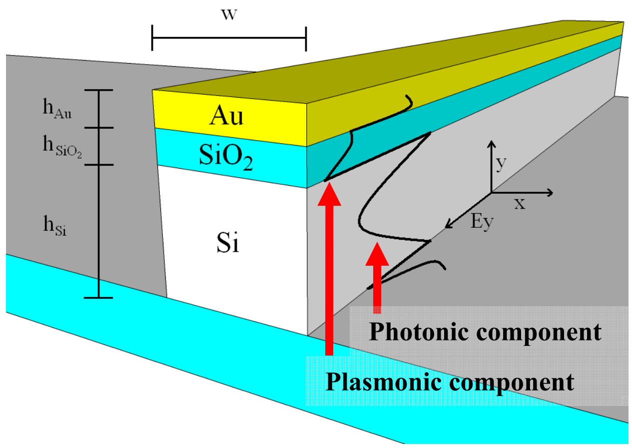

Figure 17. Three dimensional cross-section view of the conductor-gap-silicon waveguide. On the side of the waveguide is a depiction of the electric field E_y of the quasi-TM mode in the vertical direction. The field in the SiO_2 gap is labeled as the plasmonic component while one in the Si core is the photonic component.

The structure designed here should exhibit the intended behavior of the gap mode as simulated in [62] and identified in [64]. Looking vertically in the y-direction in fig.17, surface plasmons arise at the Au-SiO_2 interface which can only support the quasi-TM polarized mode. Moreover, due to the high index contrast at the SiO_2-Si interface, the y-component of the electric field E_y is highly discontinuous. Thus, the electric field distribution is strongly enhanced due to the small SiO_2 gap, forming the gap mode. Some residual power is guided in the rectangular silicon core due to another discontinuity at the Si-substrate interface. The modal shape formed in the silicon can be referred to as the photonic component of the mode which leads to the interpretation of the guided mode as hybrid in nature, hence the name “hybrid plasmonic waveguide”. The field inside the SiO_2 gap would therefore be referred to as the plasmonic component of the gap mode.

2.2 Numerical methods

The study of the behavior of the optical field in our CGS plasmonic waveguide requires the use of various numerical methods to find solutions to Maxwell's equations in a complex structure. This chapter uses predominantly the full-vectorial finite-difference (FVFD) and the finite-element method (FEM) as modesolvers. Both of these methods allow computing of the eigenmodes of the waveguide and display the mode profile in two dimensions. The first uses a uniform spatial grid to analyze the waveguide mode in both the transverse electric (TE) and transverse magnetic (TM) vectorial components of the electromagnetic field. In this work, we built our own FVFD program to simulate our CGS waveguides at a resolution of 2nm in each direction with Neumann boundary conditions. On the other hand, the FEM method uses a non-uniform triangular mesh and is able to solve for all components of the field. Its adaptive mesh is particularly effective in simulating thin layers (for example, our SiO_2 gap). Scattering boundary conditions were used. A commercially available FEM package called COMSOL® was employed to model the 2D waveguide structure. "Perfectly matched layers" were used as boundary conditions. Both modesolvers do give similar results which add credibility to our solution for the mode.

The experimental section in a later chapter will see the use of finite-difference method in cylindrical coordinates to numerically calculate the complex eigenvalue of waveguide bends [72]. The finite-difference time-domain (FDTD) method will also be used to calculate the propagation of light through various devices. The three-dimensional simulation of the interaction between light and the structures allows us to visualize the transmission and scattering of the field thus giving us estimations for the flow of power and loss in a system. All simulations were done at the telecommunication wavelength of 1550nm.

2.3 Analysis

As with all the plasmonic waveguides experimented with so far, an analysis must be performed to understand the various factors that influence the properties of the waveguide. Here, a full analysis using our numerical methods will be carried out to optimize the three properties of interest: propagation length, the mode confinement and the figure of merit. An examination of the refractive index of hybrid plasmonic waveguides will be omitted but can be found in another paper [62].

2.3.1 Propagation length

The most critical part of the hybrid plasmonic waveguide is its distinctive gap mode. Thus, the effect of height h_{SiO2} on the propagation length of our CGS waveguide will be studied first. For this first simulation, we used both the FVFD and FEM methods to solve for the eigenmode and extract the propagation length via the imaginary part of the effective refractive index. Usually, the gap size is in the sub-100nm range thus h_{SiO2} was varied between 0 to 120nm. The width w was temporarily maintained at dimensions prescribed by [62], therefore w = 200m. The metal height h_{Au} was first fixed around 50nm for ease of fabrication in terms of metal lift-off. The height of the silicon core was permanently set at h_{Si} = 340nm due to the standard silicon-on-insulator (SOI) wafer available in our possession. These are all nominal values that may vary during fabrication.

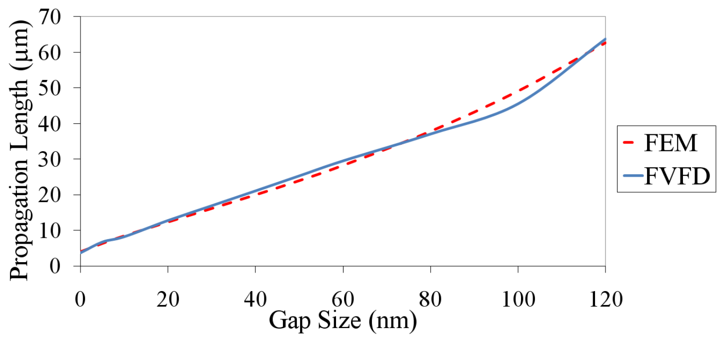

Figure 18. Propagation length of the CGS plasmonic waveguide at various gap sizes using both FEM and FVFD modesolvers. The rest of the dimensions were fixed at nominal values.

Fig.18 shows the dependence of the propagation length L_p of the CGS waveguide on the thickness of the SiO_2 gap. First, we notice that both numerical methods produce very similar results over some 100nm gap size range. Thus, our solutions to the eigenvalue can be seen as fairly accurate. Second, there is no distinctive feature in the figure since the propagation length increases monotonically with gap size. However, it can be observed that, over the mode profiles generated by our simulations, the plasmonic mode becomes increasingly more “photonic” at larger gap height. Third, the propagation distance is in the tens of microns which is promising compared to a simple IM structure (h_{SiO2} = 0nm) at 2μm theoretical propagation length [14].

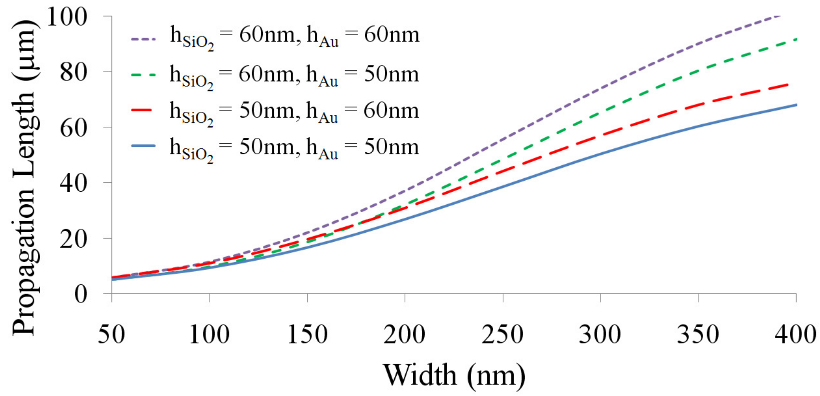

Figure 19. Propagation length of the CGS waveguide at various widths and also at a few representative gap sizes and gold thicknesses.

The other dimension affecting the gap size is the width *w* of the CGS waveguide. Fig.19 plots the propagation length of the waveguide at different widths around 200nm for some representative values of SiO_2 gap and metal thickness. Again, there is no particular feature on the graph. However, combining the effects of the SiO_2 thickness with the waveguide width, there can be as much as an order of magnitude difference in the propagation length.

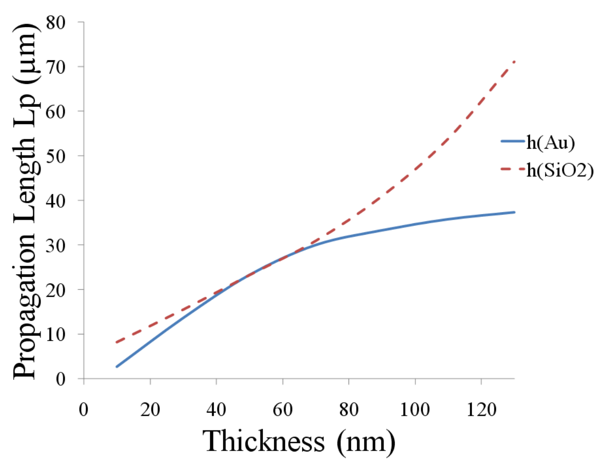

Figure 20. Propagation length at various metal thicknesses (blue line) and at various gap sizes (red dotted line).

The final factor is the metal thickness h_{Au}. Its influence on the propagation length is plotted in fig.20 (blue line) along with a comparative h_{SiO2} (red dotted line). The dramatic decrease in L_p only occurs at h_{Au} less than 50nm. After that, the loss slowly stabilizes. At more than 100nm, the metal layer becomes characteristic of bulk gold and thus the loss remains constant since surface waves have shallow field penetration into the metal. Accordingly, a good range of gold thickness is between 50nm and 100nm.

2.3.2 Mode confinement

The second property of interest is the mode confinement. An exploration of the effects of various dimensions on the shape, area and power flow of the mode will give us an understanding of the confinement strength and modal distribution.

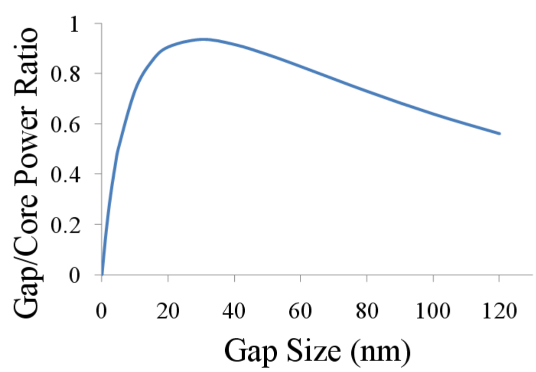

Figure 21. Ratio of the power inside the gap over the Si core various gap sizes.

First, we will vary the gap size h_{SiO2}. One way to measure the confinement of the gap mode is to compare the power flow in the gap versus its photonic counterpart in the Si layer. A power ratio can be obtained by integrating the field amplitude in the gap, dividing it by the area it occupies then take the ratio with the field in the Si core. The degree of hybridization gap versus photonic can thus be seen as a function of h_{SiO2} in fig.21. A maximum can be identified in the 20-60nm range in gap size which is indicative of a major plasmonic component. As h_{SiO2} decreases below 20nm, the total power inside the gap drops sharply due to the gap area decrease. For $h_{SiO2} > 60$nm, the power in the gap begins to leak out significantly into the Si core, thus lowering the ratio again.

Another measure of the confinement is the effective area of the mode. We have previously defined the effective area A_e as the 1/e field magnitude contour relative to the maximum. In our CGS waveguide, that area will be defined as the rectangular region enclosed by the gap due to the majority of the mode being confined in it. However, a portion of the photonic region will have to be incorporated once the field amplitude reaches 1/e of the maximum field of the plasmonic mode. Also, in the extreme case where the field in the gap is smaller than that in the silicon core, the effective area will be measured relative to the maximum of the photonic-shaped mode.

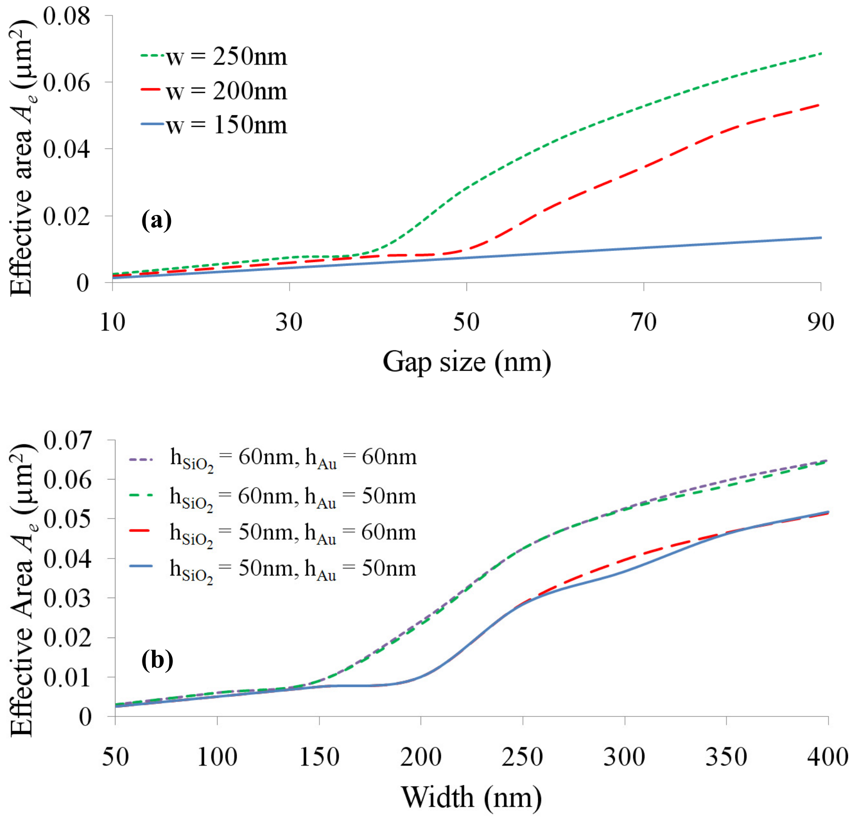

Figure 22. a) Effective area at different gap sizes for representative waveguide widths. The metal thickness remains at 50nm. b) Effective area at various waveguide widths for representative combination of gap sizes and metal thicknesses.

In fig.22, the effective area was calculated by varying the gap size and the width of the CGS waveguide. The effective area first scales with the area bounded by the gap. However, for gap sizes larger than 50nm and widths wider than 200nm, the linear trend gives place to a sudden increase. This indicates that the photonic component of the mode in the Si core has risen more than 1/e in amplitude relative to the maximum located in the gap. Thus, additional area is added to the effective area A_e. This trend is true except for a waveguide width of 150nm were the mode remains mainly in the gap. Another observation near the change in slope in both graphs shows an earlier increase in effective area at lower gap sizes for wider waveguides and smaller widths for larger h_{SiO2}. Thus, both dimensions must remain relatively small in order to maintain the majority of the gap mode inside the gap. Knowing that larger dimensions lead to longer propagation lengths, one must then find a good balance between these two. The trade-off thus still persists. However, a closer look at the figure of merit will help us make a better comparison and an optimal choice in the dimensions of our CGS waveguide.

As a side note for the other two dimensions h_{Au} and h_{Si}, an analysis of their effect on the effective area show an emergence of a major photonic component when $h_{Au} > 60$nm and $h_{Si} > 350$nm.

2.3.3 Figure of merit

Having propagation length and the effective area, we can now use equation 6 to calculate the figure of merit M_1^{2D} for the CGS waveguide.

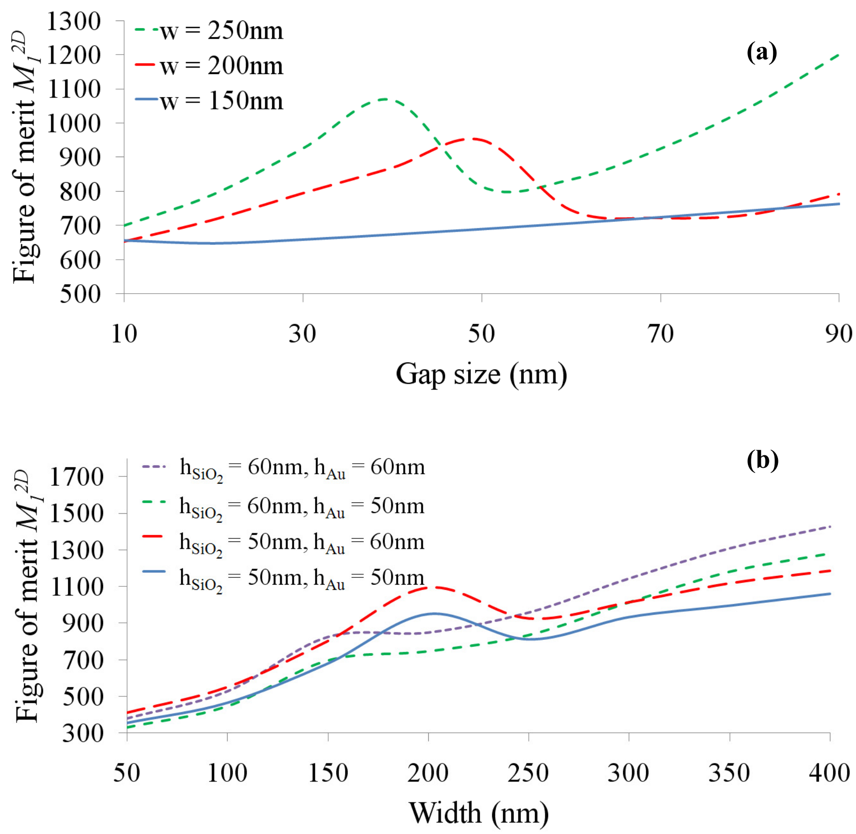

Figure 23. Figure of merit (FOM) of the CGS waveguide at various dimensions by a) varying the gap size and b) varying the waveguide width.

From both graphs in fig.23, the general trend shows an increase in the FOM as the dimension increases except for a waveguide width of 150nm. However, a surprising feature occurs in both graphs. There exists a local maximum where the FOM is greater at some dimensions. These take place near the sudden increase in effective area thus slightly lowering the FOM. From fig.23a (green line), at a width of 250nm, the FOM can reach as high as 1000 for a gap size of 40nm. The same FOM can be achieved for the local maxima in fig.23b (red line) at 200nm width, 50nm gap and 60nm gold thickness. However, looking at fig.22a (green line), at 250nm width, a significant portion of the mode in the Si core has appeared in the effective area. Thus, one might favor the latter over the first for better mode confinement. Another local maxima in the FOM occurs at 200nm width, 50nm gap and 50nm gold thickness with a value of 900 in fig.23a (red line). Though wider waveguides could have been chosen, the goal of compact integrated devices places our choice in the smaller widths such that the lateral confinement of the mode can be subwavelength in scale as well as the vertical.

2.3.4 Final design

Our final design for our CGS plasmonic waveguide includes the following nominal dimensions: width w = 200nm, gap size h_{SiO2} = 50nm, and gold thickness h_{Au} = 60nm. This waveguide will have the following properties: propagation length L_p = 29µm (loss = 0.14dB/µm), effective area A_e = 0.01µm^2, and figure of merit FOM = 1100. In comparison with other types of plasmonic waveguides, the CGS waveguide has very good characteristics. Its propagation distance is much higher than IM and MIM waveguides and same order as waveguides supporting CPP's and DLSPP's. Its effective area at $\lambda^2/240$ is as small as MIM waveguides. And finally, its FOM is comparable to that of LRSPP waveguides. Though not meant to be long-ranged, the CGS waveguide has the advantage of subwavelength confinement which reflects on the high FOM.

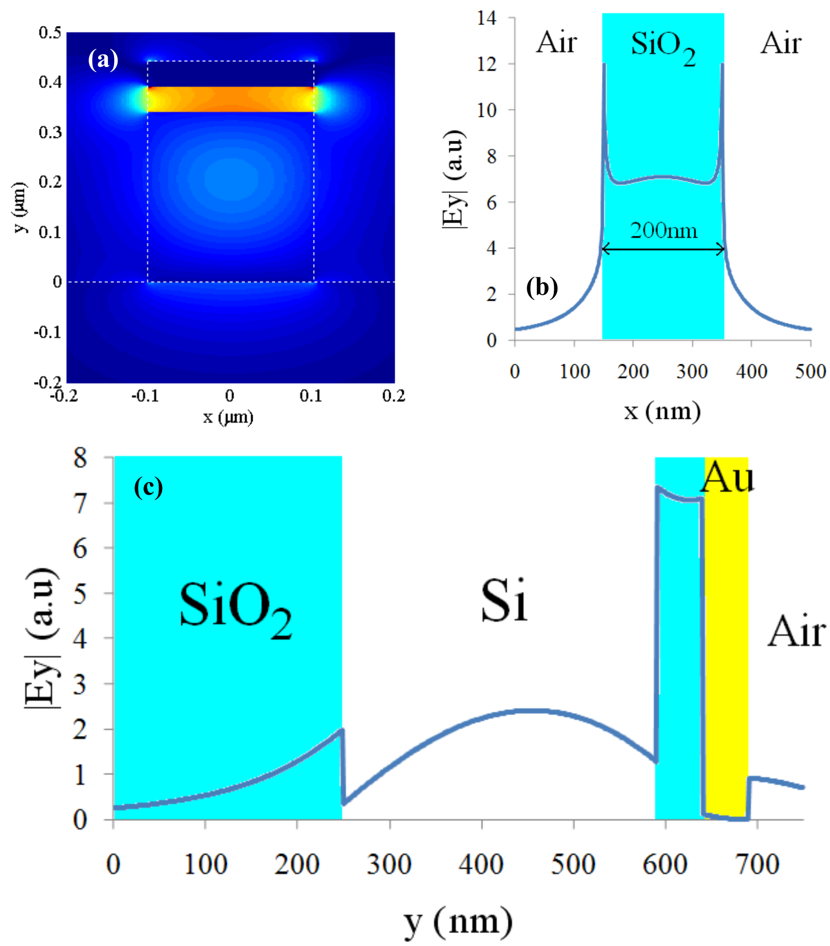

Figure 24. a) Simulated E_y field distribution cross section of the fundamental quasi-TM mode in the CGS plasmonic waveguide at nominal dimensions. The warmer the color, the stronger the field intensity. b) Linear cross section of the field distribution in the *x*-direction at the metal-SiO_2 interface. c) Cross section in the *y*-direction across the center of the waveguide.

Our numerical simulations also provided a field distribution profile for the quasi-TM plasmonic mode. For the sake of simplicity, we chose h_{Au} = 50nm for our profile simulations. Fig.24a shows the strongly confined mode residing in the 200nm by 50nm subwavelength gap. Fig.24b shows the lateral confinement of the mode in the gap thanks to the index contrast between the waveguide and the air cladding. Lastly, fig.24c paints a vertical cross section through the center of the mode showing discontinuity of the E_y field across boundaries. This allow for strong field enhancement inside the gap giving rise to a prominent plasmonic component. On the other hand, some residual field leaks into the Si core to form the photonic component of mode. At our nominal dimensions, this component is much weaker than the plasmonic one. However, this photonic component will play a role in the efficient coupling from the CGS waveguide to a Si photonic waveguide.

With design of the CGS waveguide completed, we can proceed to the fabrication of the device. However, we must note that fabrication margins may slightly shift the dimensions of our waveguides and thus its properties also. By varying the width w = 200-250nm, gap size h_{SiO2} = 50-60nm, and gold thickness h_{Au} = 50-60nm, the propagation length has a range of 26-52µm, the effective area 0.01-0.042µm^2, and the FOM 750 to 1100.

Chapter 3: Fabrication

In order to show monolithic integration of all the components on a single chip, the devices were fabricated using semiconductor technologies on a Silicon-on-insulator (SOI) platform. The CGD plasmonic waveguide was integrated to conventional photonic waveguides in order to facilitate butt coupling with a fiber lens system for laser input and output measurement. The fabrication itself was performed in the nanofabrication research facility at the University of Alberta. The facility includes a class 10 cleanroom, state of the art micro and nanofabrication equipment and support infrastructure along with professional staff.

The process flow of our fabrication procedures is depicted in fig.25. The starting point was a SOI wafer with a 340nm silicon layer. The first step involved the deposition of a thin 50nm SiO_2 film. It was followed by a PMMA resist spinning in preparation for an electron beam lithography (EBL) step in order to define the metallic pattern for the device. After exposure and development, a thin layer of gold (50-60nm) was sputtered on the chip. A lift-off process left the desired gold pattern of the device on the sample. A second EBL step was used to define the photonic waveguides employed for input/output (I/O) of light. Two etching processes transferred the resist pattern unto the chip. A delicate manual cleaving procedure exposed the facets of the I/O waveguides and the sample was ready for testing.

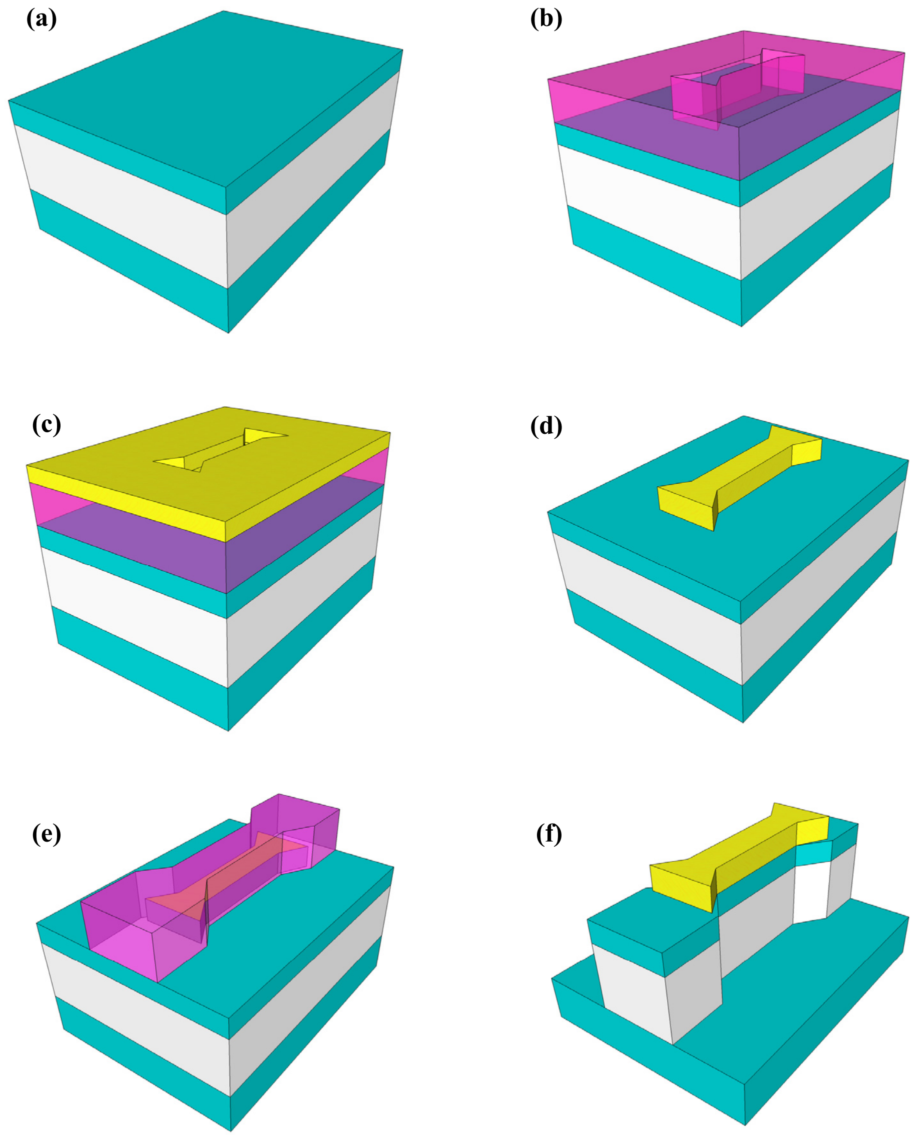

Figure 25. Schematics of the fabrication process. Color legend: white for silicon, blue for SiO_2, yellow for gold and translucent pink for PMMA. Dimensions not to scale. a) Deposition of SiO_2 unto a SOI chip. b) First EBL step defining metallic patterns. c) Gold metal deposition. d) Lift-off process. e) Second EBL step defining waveguide features. f) Etching processes transfer the pattern unto the SiO_2 and Si layers.

For more detailed fabrication steps, the reader is directed to the subsections below. Otherwise, one can proceed to the next chapter.

3.1 Sample Preparation

The substrate used for fabrication originates from a commercially available 10cm diameter SOI standard wafer. The layer of crystalline silicon was 340nm thick sitting on top of a 1μm buried oxide layer. Each sample was fabricated onto a 1cm by 1cm chip thus the wafer was first diced into small squares using a Dicing Saw. After a customary removal of organic residues using a Piranha cleaning process (sulfuric acid with hydrogen peroxide), a thin 50nm layer of SiO_2 was deposited using Plasma-enhanced Chemical Vapor Deposition (PECVD) on a Trion machine. The thickness of the SiO_2 on our samples was monitored via Filmetrics thickness mapping system and varied from 50nm up to 60nm.

3.2 1st Pattern Generation

Due to the subwavelength lateral dimension of the plasmonic waveguide, our devices were fabricated using electron beam lithography. The first pattern to be generated onto the sample was the metallic layer. A layer of PMMA A6 positive resist was spun to form a 400nm thick sheet on which a beam of electrons can inscribe a pattern. For a positive resist, the location where the beam exposes will be weakened and washed off after developing, leaving a patterned void. A thick resist was used to facilitate a lift-off process in the subsequent step. A half-hour long baking process at 180^{o}C was used to evaporate the solvent in order for the photoresist to stabilize and consolidate. The chip was then inserted into a Raith-150 Electron Beam Lithography tool for patterning at a voltage of 20kV with

10μm beam aperture, current set at $220\mu As/cm^2$ and the dose set at 1.3. After developing the resist for 45s in a Methyl Isobutyl Ketone/Isopropyl Alcohol (MIBK/IPA) solution, the sample was quickly cleaned under oxygen plasma for 25s in a process called “ashing” or “descum” in order to remove residue resist inside the patterned trenches and prepare for metal deposition.

3.3 Metallization and Lift-off

To form metal patterns, a lift-off process was carried out. By covering the sample with a metal layer, the patterned trenches filled at the desired thickness. Then, when the resist was washed off, any metal sitting on top of the resist was removed while patterned metal from the trenches stay on the sample. The metal was deposited using a sputtering machine at a pressure of 1mT. First, a 5nm of chrome was put down in order to promote adhesion between the dielectric and the gold layer. It was swiftly followed by a targeted 50nm gold deposition. However, we observed that the uncertainty in the deposition thickness from sputtering varies the gold thickness from 50 to 60nm. Lift-off was conducted by immersing the chip in acetone while vibrations from an ultrasonic bath helped stripping the resist and unwanted gold. The metal patterns were visualized under a scanning electron microscope (SEM), see fig.26.

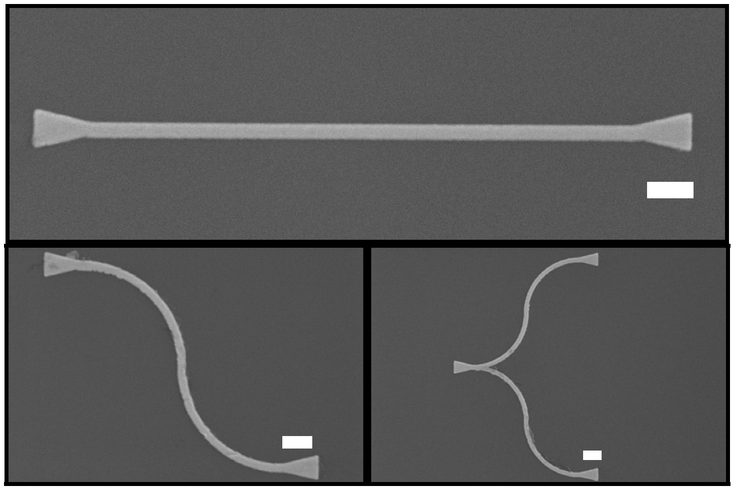

Figure 26. SEM pictures of various gold patterns on the substrate after a lift-off process. Each bar is 1μm in length.

3.4 2nd Pattern Generation

A second step of patterning was required to transfer the image of the waveguides, both plasmonic and photonic, unto the silicon and SiO_2 layers. First, a spinning of PMMA A2 photoresist at 100nm thickness was accompanied by 10min baking. Then, a more complex pattern on the electron beam lithography machine, Raith-150, was accomplished at 10kV voltage, 20μm beam aperture, 110μAs/cm^2 current and normal dosage. Since the image to be patterned was a centimeter in length, the electron beam machine was switched to Fixed Beam Moving Stage (FBMS) mode. In this configuration, the beam stays fixed while the entire stage moves to produce the pattern. In this way, larger patterns crossing multiple working fields can be produced. After the electron beam write, the sample was developed. Due to the nanoscale dimension of the waveguides, alignment issues arose during the second layer patterning over the first one. The Raith has a precision of about 50nm in the alignment. Thus, the underlying Si and SiO_2 layers, when patterned, can have a larger width than the metal layer by 50nm.

3.5 Pattern Transfer

The purpose of the next step was to transfer the waveguide pattern unto the layers through etching. First, to stabilize the sample, the chip was bonded on top of a dummy wafer covered with HPR504 resist. The topmost SiO_2 layer was anisotropically etched using a reactive ion etching (RIE) system for 20s. It was promptly followed by a silicon etching using inductively coupled plasma RIE (ICPRIE) machine for 27s to etch through 340nm of silicon. The sample was placed in an ultrasonic acetone bath to detach the chip from the sustaining wafer. Finally, the chip was manually cleaved on both ends to open up access to the photonic waveguides' facets. The finished product was then visually characterized again under SEM.

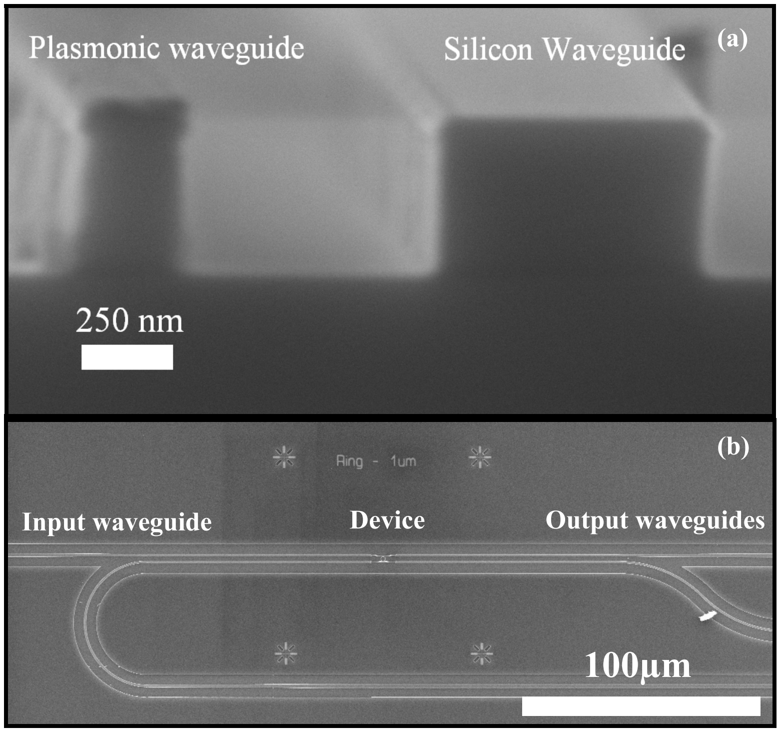

Figure 27. a) SEM image showing cross section view of a 250nm-wide CGS plasmonic waveguide (left) beside a 600nm-wide silicon waveguide for comparison. b) SEM image showing top view of a system of photonic waveguides connecting into the device of interest in the middle.

In fig.27a, a sample of the finished product is imaged in the cross section at the edge of a cleaved chip. Due to possible misalignments during the second lithography step, the width of the plasmonic waveguide can be up to 250nm. Photonic waveguides, with no metal layer, were fabricated on-chip to channel input/output (I/O) light into and out of the plasmonic waveguide as shown in fig.27b. These waveguides were directly coupled to each other using a taper structure in order to convert the photonic mode into the plasmonic mode. More detailed description and analysis of these plasmonic tapers will be done in the experimental chapter.

3.6 Fabrication improvements

After much experimentation with each step and each machine, it was found that there is room for improvement. One major point in the development of our process flow is the metallization process. The sputtering machine used in our current process operates by evenly coating of the sample with the target metal. This leaves metal on the side walls of our photoresist coating. In turn, it affects the easiness and quality of the subsequent lift-off process. In fact, the metal layer refused to be lifted off the substrate in most cases. An improvement in this direction will require the traditional use of the electron beam evaporation machine which applies a coat of metal in a directional way across the whole sample.

Another point of improvement would be the etching process. The surface roughness of the waveguides is a significant source of loss via scattering of light. Thus, a smoother etched side wall surface could potentially reduce the loss of signal in both the photonic and plasmonic waveguides.

Chapter 4: Experimental results

4.1 Experimental Setup

After fabrication, samples are taken to the Nanophotonics Research Laboratory for experimental testing. The experimental setup is schematically drawn in fig.28. A sample is mounted into a three-directional stage with accurate positional piezo-electric motors so as to align the facets with tapered fiber lens for butt coupling of light. On the input side, a tunable continuous wave laser at telecommunication wavelengths outputs light into an optical fiber which is first connected to a polarizer before directing the signal to the fiber lens. Light emerging from the fiber couples to the facet of the exposed photonic waveguide on the sample. These I/O waveguides carry light in and out of the device. On the output side, the signal comes out of the waveguide and couples into another fiber lens. The collected light is measured by a photodetector in the infrared range. A power meter then displays the power measured.

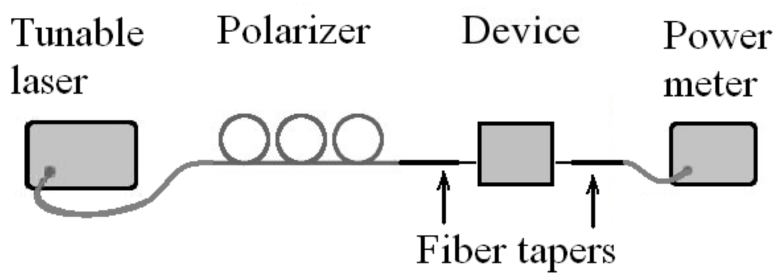

Figure 28. Schematics of the experimental setup. A light signal around 1550nm wavelength is produced in a tunable laser. It passes through a polarization-maintaining setup before exiting out of a fiber taper with a lens at the tip. The light then enters a waveguide on the chip via butt-coupling. After interaction with the device, the signal comes out, is coupled to another fiber taper and is collected by a photodetector. The intensity is finally measured in a power meter.

4.2 CGS waveguide

Straight CGS plasmonic waveguides of various lengths were fabricated: 10, 30, 50 and 70µm. They were measured by coupling TM-polarized light from the laser tuned at 1550nm wavelength. The transmission power from each waveguide was plotted in fig.29. An exponential curve was fitted to the plot using equation 4: $P(z) = P_0 e^{-z/L_p}$. The propagation length was extracted and we obtained an L_p of 40µm for our CGS plasmonic waveguides. This corresponds to a loss of 0.1dB/µm. Our experimental value is slightly above our nominal propagation distance of 29µm but it falls within the range of calculated values with fabrication margins.

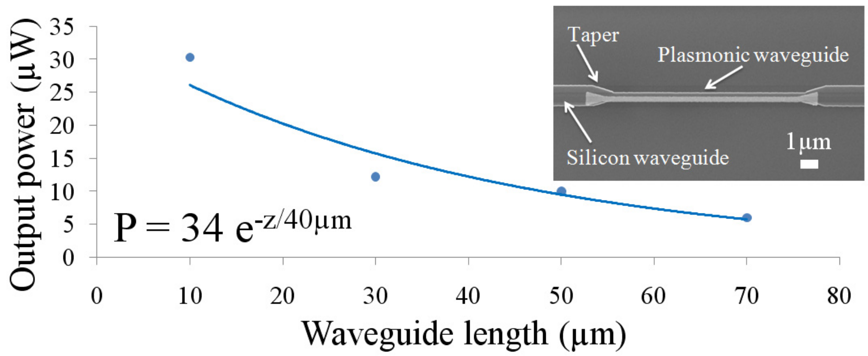

Figure 29. Output power of various CGS waveguides at different lengths (blue dots). By fitting to an exponential curve (blue line), the propagation length can be extracted. Inset: Top-view SEM image of the CGS plasmonic waveguide along with taper couplers and I/O silicon waveguides.

These results are encouraging considering that the absence of the SiO_2 gap will reduce the experimental propagation length down to a few microns as in the IM structure. Other than the propagation length, our CGS waveguides have been seamlessly integrated with photonic components on a single chip in contrast with V-groove waveguides supporting CPP's. Furthermore, the subwavelength scales of our waveguides and the strong mode confinement will allow dense integration of plasmonic devices unlike LRSPP and DLSPP waveguides. After publication of our paper, a few experimental works on hybrid plasmonic waveguides were published also. For example, one hybrid plasmonic waveguide fabricated using LOCOS technique was found to have a propagation length around 100μm in a silicon system with 75nm SiO_2 gap and 310nm silicon rib waveguide width at telecom wavelength [73]. The waveguide was coupled using a photonic waveguide at the input but the field was collected using NSOM. Another waveguide, a 170nm diameter silicon nanowire on top of 13nm of SiO_2 and a silver substrate, resulted in a propagation length of 30μm at a wavelength of 980nm [74].

4.3 Taper coupler

4.3.1 Design and analysis

The I/O of each plasmonic waveguide was directly connected to photonic waveguides via simple taper couplers. To facilitate mode transition, the taper was designed such that the degree of hybridization of the CGS mode can be continuously tuned by varying the width *w*. Thus, as the width decreases, the purely photonic mode incoming from the silicon waveguide slowly and efficiently transitions into the predominantly plasmonic mode as it enters the CGS waveguide.

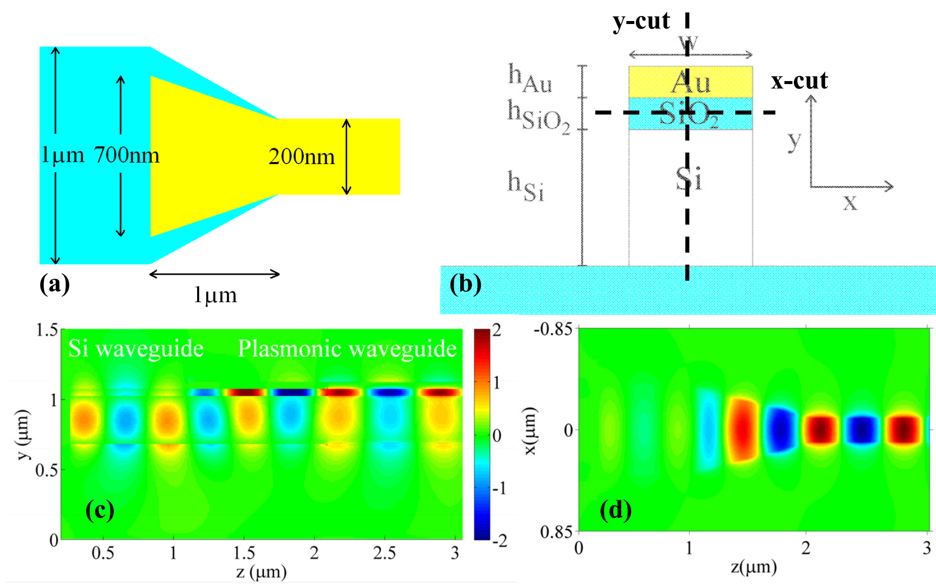

Figure 30. a) Schematic of the taper coupler. The gold layer (yellow) rests on the photonic waveguide (blue). b) Cross section of the plasmonic waveguide indicating the cuts for the 3D FDTD simulation of the taper coupler. c) Side view, showing the E_y field distribution in a vertical plane y-cut through the center of the coupler; d) Top view, showing the E_y field distribution in a horizontal plane x-cut through the center of the SiO_2 gap.

Fig.30a shows a schematic of the coupling structure. The silicon waveguide of 1µm width tapers down to the 200nm wide plasmonic waveguide over a short taper length of 1µm. The metal strip starts with a smaller width of 700nm to compensate for alignment issues in the fabrication process. At the mouth of the taper, the photonic mode from the silicon waveguide matches quite well with the photonic component of the plasmonic mode so that the coupling efficiency is fairly high. As the width tapers down, the mode becomes increasingly plasmonic as the power moves from the silicon layer up to the SiO_2 gap as expected from our calculations of the effective area in fig.22b. This power transfer process can now be visually observed in the three-dimensional FDTD simulation of the structure at 1550nm wavelength in fig.30c. It plots the E_y field distribution along the center plane of the taper as viewed from the side. The mode also undergoes a concentration process as the mode funnels into the taper as shown in fig.30d. This top-view of the taper coupler shows focusing in a horizontal plane through the center of the SiO_2 thin gap. The numerical computation of the power flow in and out of the taper coupler allowed us to calculate the theoretical coupling efficiency of the taper to be 88%.

4.3.2 Experimental results

As mentioned beforehand, the plasmonic tapers connected the I/O silicon waveguides with the plasmonic waveguide for effective mode transfer. The tapers were successfully fabricated as shown by the SEM image in fig.31.

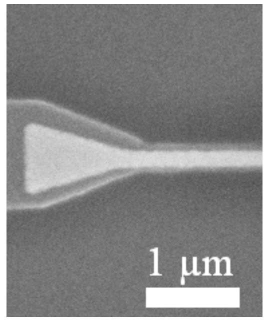

Figure 31. SEM image of the fabricated plasmonic taper coupler.

To compare with our theoretical result, the coupling efficiency was experimentally determined using data from the plasmonic waveguides. We noted that the initial power $P_0 = 33.5\mu W$ is equivalent to the transmitted power of a plasmonic waveguide of no length, thus making it a taper to taper junction. The value of P_0 corresponds thus to $\alpha^2 P_{in}$, where α is the coupling efficiency of a single taper and P_{in} is the power at the input of the taper. Using the measurement of a silicon waveguide without a plasmonic section, we obtained a reference power $P_{in} = 52.5\mu W$. Thus the experimental efficiency per taper coupler is α = 80%. This value is in good agreement with our FDTD simulated theoretical efficiency of 88%. Therefore, very high coupling efficiency can be obtained between conventional photonic waveguides and CGS plasmonic waveguides using simple taper structures.

Of course, one can further optimize the taper efficiency of the hybrid plasmonic waveguide structure. In fact, a comprehensive theoretical analysis of plasmonic taper couplers was published by Min Qiu's group shortly after our paper was published [75]. A few months after, a similar taper system was fabricated and an experimental coupling efficiency was found to be around 70%

[76]. This gives further credibility to the high efficiency achieved in our taper system.

4.4 S-bends

Just like in photonics, the density of integration of plasmonic components depends on how tightly plasmonic devices can be packed. This can be made possible only if the routing of light occurs without incurring a large bending loss in a bent waveguide. Thus, on a practical level, it is crucial to assess the bending loss of our CGS waveguide.

4.4.1 Design and analysis

On first observation of our structure, we notice that, although most of the field is confined in the SiO_2 thin gap, its lateral index contrast with the surrounding air is not large. There is therefore a possibility for the field to leak out on one side as the waveguide goes through a bend. The bending losses could be quite high. We first examined the theoretical loss in tightly-bent CGS waveguide by using finite-difference method in cylindrical coordinates to compute the bent mode as well as its complex eigenvalue. The theoretical loss extracted from the imaginary part of the effective index contains both the bending loss and the ohmic loss through the gold conductor layer.

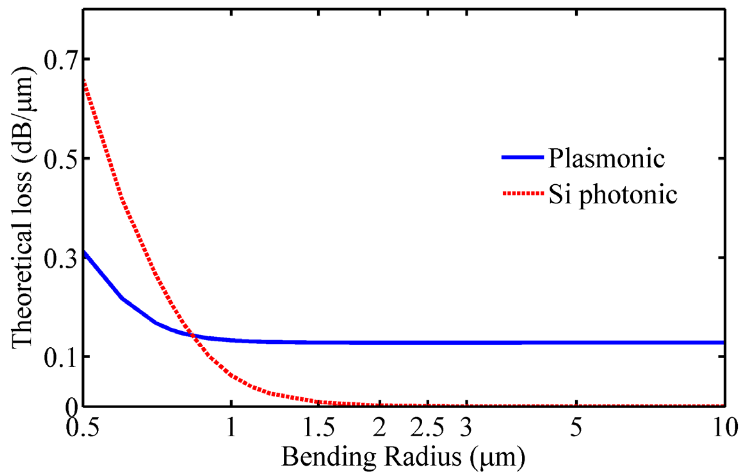

Figure 32. Theoretical loss in CGS plasmonic bends (solid blue line) and Si photonic bends (dashed red line) as functions of bending radius. Calculations were done using a Finite Difference modesolver in cylindrical coordinates. The dimensions of the bended waveguide are $h_{Au} = h_{SiO2} = 50$nm, $h_{Si} = 340$nm, $w = 200$nm at 1550 wavelength.

We plotted these losses as a function of bending radius in fig.32 (blue solid line). Evidently, a sharper bending radius translates into higher losses. The exponential increase in the loss as the radius becomes smaller is most significant for small radius below 1μm. Thus, bending losses dominate in this regime. At bending radii above 1μm, the loss is independent of bending radius, showing that attenuation from the metal dominates losses here. The bending loss is negligible. As a comparison, we plotted the bending loss of a silicon waveguide of the same dimensions as our plasmonic waveguide but without the metal layer in fig.32 (red dashed line). It can be observed that, with decreasing radii, the bending loss from the Si waveguide increases much more rapidly than the CGS bends. In fact, for bending radii below 0.8μm, the CGS bends are actually less lossy than its photonic counterpart. The strongly bound field of the surface plasmon polaritons seems to play an important role in reducing the bending loss in our CGS waveguides. From just these results, it suggests the possibility to realize very compact CGS ring resonators with higher intrinsic quality factor than comparable silicon microrings. Incidentally, an experimental work investigating the bending loss of hybrid plasmonic waveguides in an LRSPP scheme found similar results [77]. When compared to a single mode fiber, their hybrid plasmonic waveguide in a fiber exhibited much lower bending loss below a certain bending radius.

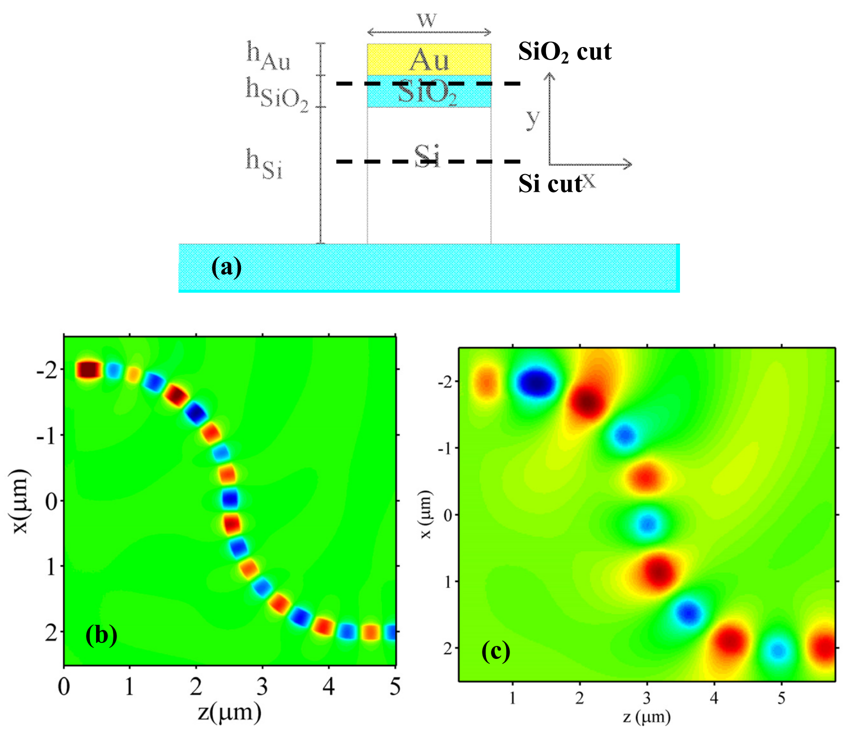

Figure 33. a) Cross section of the plasmonic waveguide indicating the cuts for the 3D FDTD simulations of the E_y field distribution in the 2μm-radius CGS S-bend at 1550nm. The horizontal cross section is in the b) SiO_2 gap and c) Si core layer. The field is much weaker in the latter such that the scattered field outside the S-bend is more visible.

We next performed 3D FDTD simulations of plasmonic S-bends formed by connecting two 90-degree bends to determine the total theoretical losses of these structures. The following analysis was done for both 1μm and 2μm radius bends. Here we just plot the results for the E_y field in the 2μm radius S-bend in fig. 33b and fig.33c. The first figure shows the field distribution on a horizontal plane through the center of the SiO_2 gap while the other figure is a cut through the silicon core. The losses are more visible in the latter since the field in the Si layer is weaker. The calculated total transmission loss through the S-bend is 2.3dB. Since the theoretical ohmic loss for two 90-degree bends at 2μm radius is 0.88dB, a big portion of the loss can be attributed to mode mismatch at the junction between the two 90-degree arcs. As for the 1μm radius S-bend, the 3D FDTD reported a theoretical loss of 3.14dB.

4.4.2 Experimental results

The conductor-gap-silicon S-bend structures designed above were fabricated and measured to obtain the experimental transmission loss. Figs.34a and b shows fabricated 1 and 2μm radius S-bends connected to silicon waveguides via our taper system.

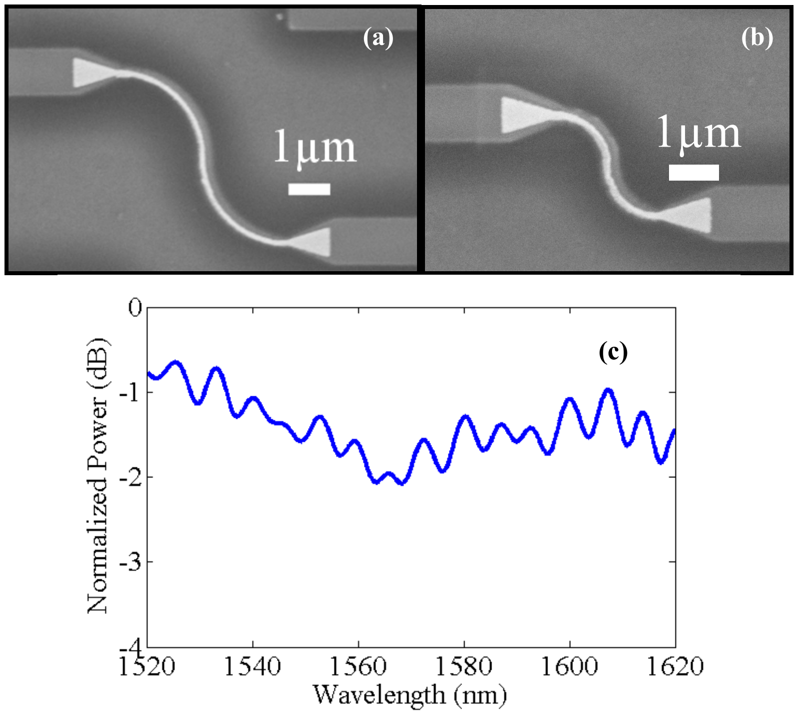

Figure 34. SEM images of fabricated CGS S-bends at a) 2μm radius and b) 1μm radius. c) Wavelength scan of the normalized transmitted power of the 2μm radius S-bend.

A wavelength scan was performed to show the broadband transmission of power at all wavelengths (fig.34c). A normalization procedure was undertaken such that the output power from the S-bend was compared to the power of a straight plasmonic waveguide with same length. In this way, the normalized plot represents only the excess loss in the S-bend caused by bending loss and junction loss. It effectively discards the loss from the taper system as well as metal losses. From the plot, an average excess loss over the scanned wavelength range is about 1.4dB. Since, from theory, the bending loss is negligible at this radius, we can attribute the loss to the junction loss. By adding the experimental metal loss, the total loss for the S-bend amounts to 2.05dB, which is in close agreement with the value of 2.3dB obtained from our FDTD simulations.

The 1μm radius S-bend was also fabricated and the measured loss is about 3dB. By adding metal losses from a straight plasmonic waveguide (~0.31dB), the total experimental loss of the S-bend is 3.31dB (excluding the tapers). From theory, only a small portion around 0.38dB can be attributed to bending loss, the majority of the loss is thus due to junction scattering. The results for both the 1μm and 2μm radius S-bends are compiled together in table 1.

1μm S-bend	*Metal loss*	*Bending loss*	*Junction loss*	*Total loss*
Theoretical	0.44 dB	negligible	2.7 dB*	3.14 dB
Experimental	0.31 dB	3 dB		3.31 dB*
2μm S-bend				
Theoretical	0.88 dB	negligible	1.42 dB*	2.3 dB
Experimental	0.62 dB	1.4 dB		2.02 dB*

Table 1. Total losses in S-bends for 1 and 2μm radius S-bends. *These values are calculated from the other values by addition or subtraction.

These results show that the junction is the most significant source of loss in plasmonic bends. To improve transmission in these bends, a junction offset could be considered to reduce the mode mismatch between the two arcs. However, our study of 90-degree arcs is a platform to better understand bending losses that will arise in microring resonators.

As a comparison with other fabricated S-bends, we note that bends using metallic V-grooves with 2.25μm radius were reported to have total transmission loss of about 2.3 dB [40]. DLSPP waveguide bends at 2μm and 4μm offset had

1.55dB and 2.2dB loss, respectively [23]. However, they were not strictly 90-degree arcs.

4.5 Y-splitters

Among the basic photonic structures, power splitters are also essential for routing of signal but also for building interferometers with switching functions.

4.5.1 Design

Our Y-splitters were designed by interposing two plasmonic S-bends. An electron micrograph of the structure using 2μm radius bends can be seen on fig.35a. Our 3D FDTD simulations show even splitting of power between the two branches in fig.35b. The combined transmission loss is 3.37dB.

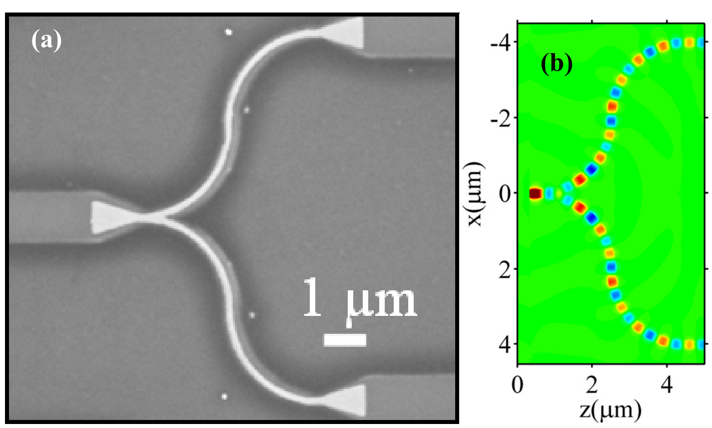

Figure 35. a) SEM image of the fabricated CGS plasmonic Y-splitter with 2μm radius along with taper couplers. b) 3D FDTD simulation of the E_y field distribution in the Y-splitter at the level of the SiO_2 gap.

4.5.2 Experimental results

The 2μm radius Y-splitter was fabricated as shown in fig.35a. Each output was measured separately and plotted in fig.36 along with the total power which is the addition of the two branches.

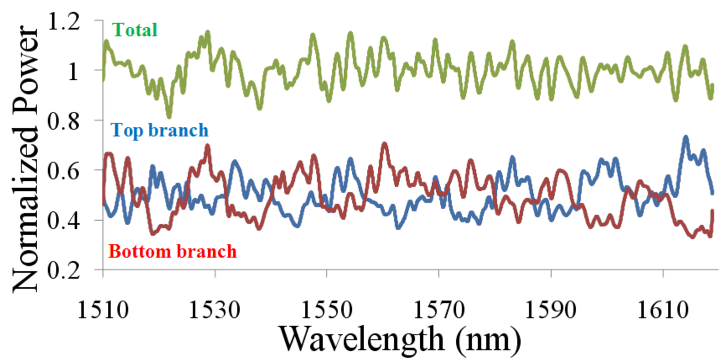

Figure 36. Wavelength scan of the transmitted power in the two output branches of the Y-splitter. The total power is the addition of the two branches. The total power can go above 1 due to the normalization value set to the average of the total power.

The transmitted power was normalized to the average total power from the two outputs. The scan across a broad wavelength range shows a relatively constant power splitting ratio of 50% (± 7%). Thus equal power splitting and broadband response is achieved. The noise from the signal is most probably due to reflections from the facets forming a Fabry-Perot cavity and to imperfections in fabrication. The Y-splitter has an experimental transmission loss of 3.57dB, in good agreement with our simulations. Other Y-splitters were fabricated, showing even splitting ratios within a standard deviation of ± 10%.

Experimentally, one could modify one of the branches of the Y-splitters to cause an uneven power split. Many schemes are possible: intentional fabrication design, local thermal heating, tuning through a nonlinear material and much more (see active plasmonics in chapter 1). We expect these broadband power splitters to be useful for building more advanced CGS devices such as Mach-Zehnder interferometers.

4.6 Advanced devices

Once the basic building blocks were analyzed and successfully fabricated, many advanced devices were then attempted. However, this next step was faced with numerous fabrication challenges as well as poor design. The results obtained were not satisfactory. All of the devices presented below require a coupling mechanism from either a plasmonic or photonic waveguide unto another plasmonic waveguide. However, due to the strong confinement of the mode in the gap, the evanescent wave extending out of the waveguide is much weaker. Also, the losses incurred in a resonator are much higher in plasmonic devices due to the presence of the metal. In order to obtain sufficient coupling, longer coupling distances are needed and a more useful scheme should be employed, for example a multi-mode interferometer (MMI) coupler as proposed by [78].

4.6.1 Microdisks

The first device attempted is actually a microring. In both fields of photonics and plasmonics, the microring resonator is an important structure due to the field enhancements obtained [79]. However, due to difficulties in the lift-off process, the center portion of our microrings did not properly peel off. As a result, there remains a metallic cover that is insulated from its dielectric foundation by a photoresist. This resulted inadvertently into plasmonic microdisks as shown in fig.37.

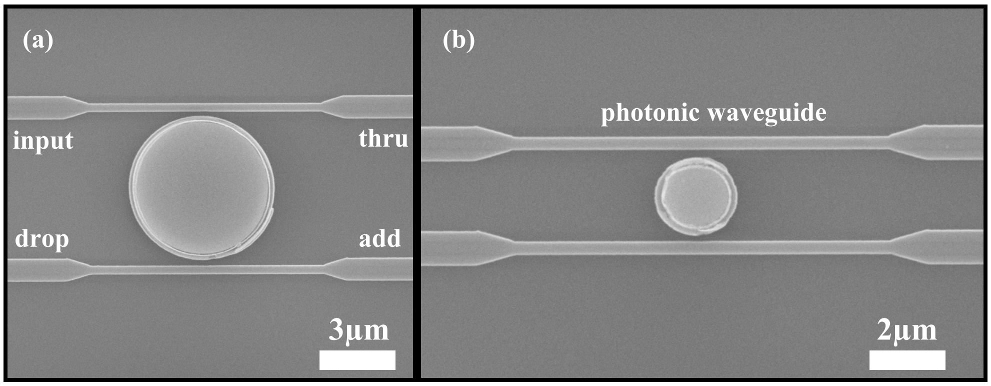

Figure 37. SEM pictures of a) a 3μm radius microdisk and b) a 1μm radius microdisk in an add-drop filter configuration. The photonic waveguides are 400nm in width. The separation from the microdisk to the photonic waveguide is 200nm.

These microdisks of radius ranging from 1μm to 3μm were built into an add-drop filter configuration in order to measure its resonances. The input signal comes from the top left photonic waveguide. The “thru” port leaves on the top right. On the bottom left side, the “drop” port can couple the signal out of the resonator. The bottom right side of the photonic waveguide is the “add” port where an additional signal can be added to the resonator. Fig.38 shows a representative output from a 2μm CGS plasmonic microdisk. The lack of sharp resonance dips at the “thru” port indicates poor coupling into the resonator.

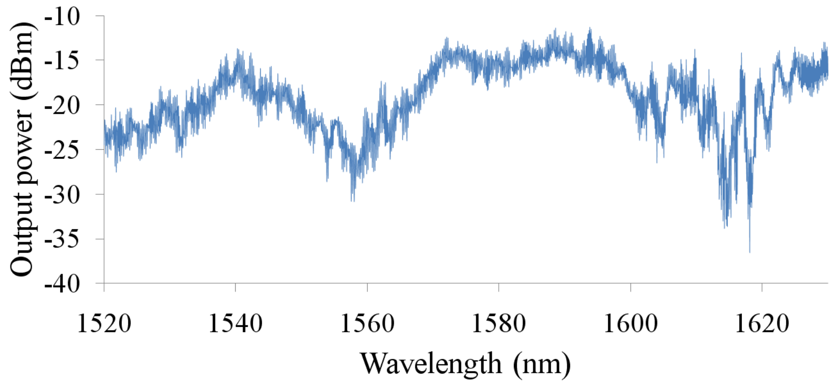

Figure 38. Wavelength scan of a 2μm microdisk from the output at the “thru” port.

4.6.2 Microrings

After many attempts, CGS plasmonic microring resonators were successfully fabricated. The 1-3μm radius resonators were made from 200nm wide CGS plasmonic waveguides. Photonic waveguides delivered light through evanescent coupling in an add-drop filter configuration as shown in fig.39.

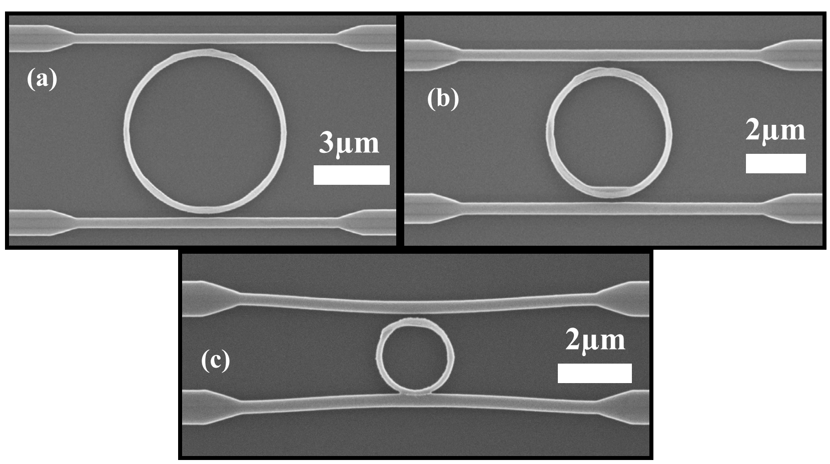

Figure 39. SEM pictures of microrings in the add-drop filter configuration at a) 3μm radius, b) 2μm radius and c) 1μm radius. The nominal separation between the photonic waveguide and the microring is 200nm.

The signal at the “thru” port was then measured. A representative graph for the outputs from 1 and 2μm radius microrings was plotted in fig.40.

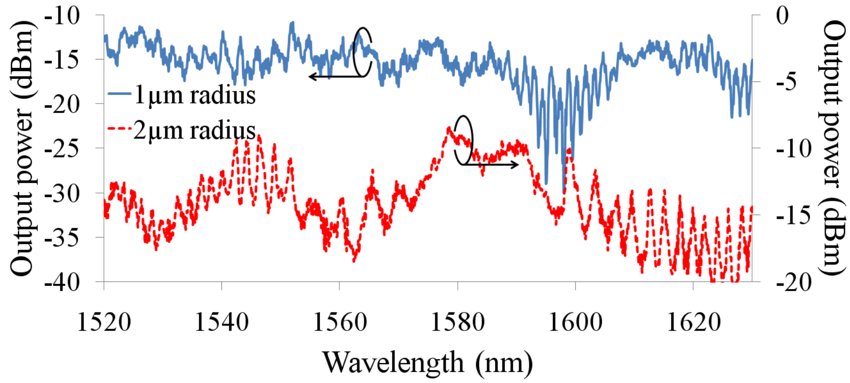

Figure 40. Wavelength scans of 1 and 2μm radius CGS plasmonic microring resonators measured at the “thru” port.

As in the case for microdisks, no significant resonance is found. Moreover, the noise level and Fabry-Perot interferences make up most of the landscape of the output signal.

4.6.3 Directional coupler

A directional coupler was also fabricated (fig.41). However, no particular signal was measured at either output. The power was low but the splitting was nearly equal.

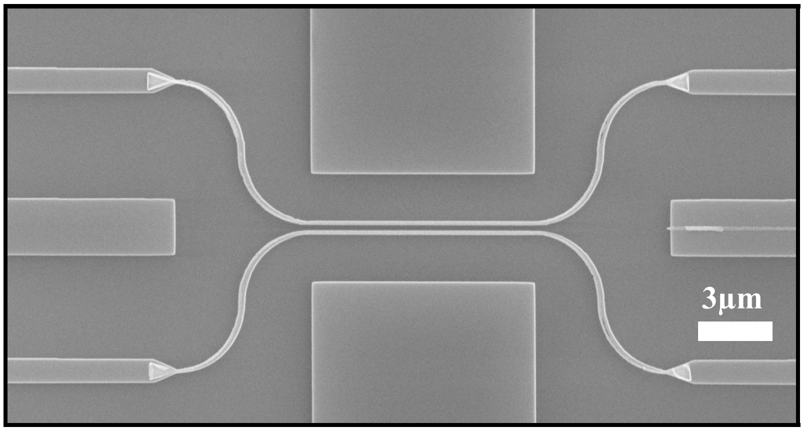

Figure 41. SEM image of a fabricated directional coupler using two 2μm radius S-bends. The separation between the two waveguides in the center is 200nm.

4.6.4 Sagnac interferometer

A Sagnac interferometer was fabricated using CGS plasmonic waveguides (see fig.42). The single loop in this interferometer allows for a single interference effect at the coupling junction.

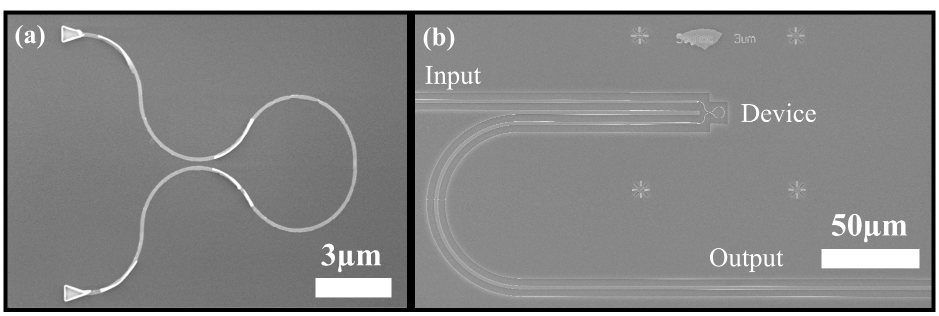

Figure 42. SEM image of a) a Sagnac interferometer metal layer using 3μm radius bends and a separation of 200nm; b) a far top view of the device along with the photonic waveguide system connecting to it.

An interesting signal was measured and plotted in fig. 43. A peak appears around 1540nm, albeit at low power. At the same time, for a range of wavelengths between 1550 and 1620nm, the signal disappears almost completely as it drops below the noise floor.

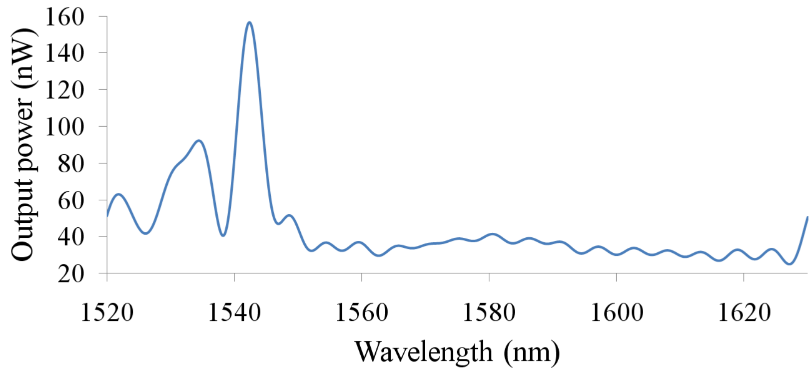

Figure 43. Wavelength scan of a Sagnac interferometer.

However, the lack of noteworthy features and noticing that the output signal is extremely low, the interference effects of the Sagnac device was not noticeable.

Chapter 5: Current and future research

5.1 Latest developments

In the past year or so, there has been broad interest in the topic of hybrid plasmonic waveguide as we have seen briefly in the experimental section. In terms of publications, starting from 2008, there were 3 papers published. In 2009, 6 papers were made public including one showcasing a plasmonic laser. The following year saw a sudden increase with around 19 publications, 15 of which were published after the results of this thesis. And, in the latest development, 4 papers came out in 2011 so far as of the day of writing of this thesis.

Many of the studies were still in the theoretical stage and include full analysis of various waveguide structures similar to ours [75,80-82]. A few groups combined other kinds of plasmonic waveguides to form a hybrid plasmonic waveguide by simply adding a low-index layer: DLSPP [83], MIM [84,85] and LRSPP (experimental study) [77]. Some have even used cylindrical or coaxial cable structures to show strong confinement as well as long propagation lengths [86,87]. Other than the waveguide itself, many coupling mechanisms were examined, notably plasmonic-plasmonic [78,83] and photonic-plasmonic [88]. Studies on optical forces, CMOS compatibility with on-chip integration and photonic crystals were also performed using the basis of hybrid plasmonic waveguides [89-91].

On the experimental side so far, most hybrid plasmonic waveguides were fabricated in the silicon material system due to the CMOS processes already in place. A waveguide using thin metal strips on a substrate separated by an oxide demonstrated propagation lengths up to 34cm [92]. The scheme is basically a modified LRSPP waveguide with long propagation lengths but very low confinement. Three hybrid plasmonic waveguides were already mentioned previously in another chapter. The first one showcased the use of a fabrication technique called LOCOS (local oxidation of silicon) [73]. The second one used nanowires [74]. The final one explored the coupling from photonic to plasmonic waveguide using a taper system much like ours [76].

5.2 Future research

The current attractiveness of hybrid plasmonic waveguides in the scientific community is opening the door to an expansion of future opportunities. As research groups move from theoretical investigations to experimentation, one can see a plethora of devices being developed. Passive and active devices with strong confinement and low loss will be fabricated as many are looking to exploit various nanoscale phenomena.

In the case of our own hybrid plasmonic waveguide design, possible future research directions include improved versions of our current passive devices. For example, racetrack resonators were attempted in order to increase coupling length. However, their fabrication was met with machine instability during a period of repairs in the facility. Future resonators will need to incorporate MMI junctions for enhanced coupling. Another opportunity lies in the metal layer cladding the top of the waveguide. By connecting this layer to an external electric source, the current generated can be used to induce switching by carrier injection. Conversely, an electric signal can be generated by the plasmonic field traveling though the waveguide and thereby producing a plasmonic detector. Finally, the materials used in the hybrid plasmonic waveguide can be exploited for active switching. In particular, one can take advantage of the silicon core in order to perform all-optical nonlinear modulation. The low index layer used for the gap can be doped with a gain material to support the propagation of SPP's and, at the same time, to allow switching functionalities via gain-loss mechanism [12]. However, it remains to be seen if one can achieve large enough gain coefficient in the range of a few microns with close proximity to a metal layer.

5.3 New current direction

Our current research is exploring nonlinear thermal effects in SU-8 DLSPP hybrid plasmonic waveguides. By exploiting the thermal conductivity of metal and the thermo-optic properties of SU-8 [93], the probe signal can be modulated by the power of the pump inside a cavity. Microring resonators based on SU-8 dielectric loaded waveguides have been successfully made on layers of SiO_2 and gold, schematically shown in fig.44a. The plasmonic mode excited in this hybrid plasmonic waveguide is mostly confined in the SiO_2 gap. However, due to the lower index of the SU-8 photoresist, the mode extends into the SU-8 core in an exponential decaying curve (see fig.44b top). The confinement in this case is not subwavelength but the propagation length achieved experimentally is around

60μm. Another advantage of this structure is the ease of fabrication using UV lithography.

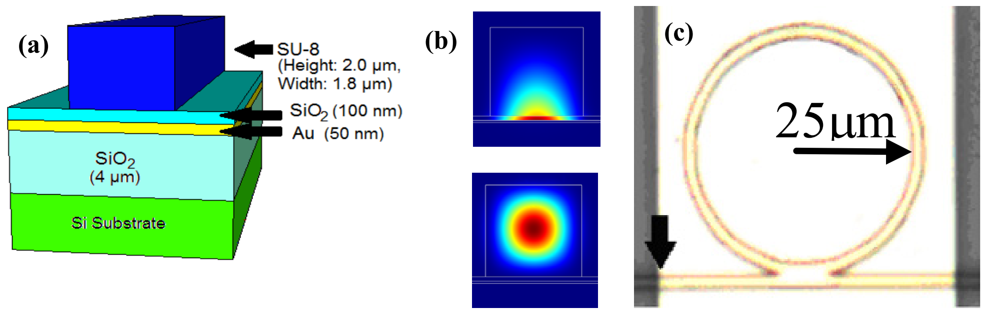

Figure 44. a) Schematics of the SU-8 DLSPP hybrid plasmonic waveguide. b) Mode profiles for the E_y field of the plasmonic quasi-TM mode (top) and photonic TE mode (bottom). c) Optical micrograph of a 25μm radius microring resonator. The arrow shows the beginning of the metal boundary.

The microring resonator was fabricated at a radius of 25μm and connected with the input waveguide by means of a MMI-type coupling as shown in fig.44c. Using this device with an optical amplifier, nonlinear thermal effects were observed. At stronger input powers, the resonance appeared to shift more. In fact, a TM polarized input gave a bigger shift than a TE polarized input and also even more than in a non-plasmonic microring resonator. The higher heat loss through the metal for the plasmonic mode actually enhanced the thermal-optic resonance shift. This effect can be used as a switching mechanism although at slow speeds. The analysis and results were accepted for presentation in a conference [94].

Conclusion

In this thesis, silicon hybrid plasmonic waveguides were analytically and experimentally investigated. A long propagation distance of 40µm was observed in our layer configuration of conductor-gap-silicon. A photonic-plasmonic waveguide coupling efficiency of 80% was achieved using taper couplers. This opens the door to integration with future photonic components in which the metal layer can also support electrical signals. Passive devices such as S-bends and Y-splitters were fabricated and characterized. More advanced devices were also attempted. Their small footprint can be exploited for densely packed ensemble of devices on an SOI platform. Various switching schemes can be implemented as the strong confinement of the plasmonic mode inside the gap can enhance modulation strength. These plasmonic building blocks will serve as first steps to plasmonic logic elements at subwavelength scales and ultrafast speeds. Future developments will allow further applications in highly integrated plasmonic circuits.

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